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EXAMINER
BIRKHIMER, CHRISTOPHER D

ART UNIT	PAPER NUMBER
2136	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 14/811,844	Applicant(s) Yeh, Chih-Kang	
	Examiner CHRISTOPHER D BIRKHIMER	Art Unit 2136	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 04/11/2019.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-2,4-7,9-12,14-19 and 21-22 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-2,4-7,9-12,14-19 and 21-22 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☑ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 07/29/2015 is/are: a)☐ accepted or b)☑ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

The current Office Action is in response to the papers submitted 04/11/2019. Claims 1 – 2, 4 – 7, 9 – 12, 14 – 19, and 21 - 22 are pending.

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Specification

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

Claims 1, 6, and 11 disclose the limitation of copying data based on a condition. The original specification discloses moving data based on the same condition but not copying data. The specification fails to provide proper antecedent basis for the copy limitation in the claims.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, **the copying the write data in the at least one second physical unit associated to the temporary area to a physical unit associated to the storage area if the usage status of the first physical units associated to the storage area does not conform to the first**

predetermined status must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> (a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. The following is a quotation of 35 U.S.C. 112(b):

> (b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims **1 – 2, 4 – 7, 9 – 12, and 14 - 15** are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for pre-AIA the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 1, 6, and 11 contain the limitation of copying data based on a condition. The process is shown in figure 10 at step S1005. The original disclosure though describes the process as moving the data not copying the data. A data move and copy operation may be similar operations but they are understood to different and executed differently. The original disclosure provides support for a move operation based on the condition in step S1003, not a copy operation as is currently claimed.

All remaining claims are rejected for being dependent on a rejected base claim.

7. Claims **1 – 2, 4 – 7, 9 – 12, and 14 - 15** rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as failing to set forth the subject matter

which the inventor or a joint inventor, or for pre-AIA the applicant(s) regard as their invention. Evidence that claim **1 – 2, 4 – 7, 9 – 12, and 14 - 15** fail(s) to correspond in scope with that which the inventor or a joint inventor, or for pre-AIA the applicant(s) regard as the invention can be found in the original disclosure submitted 07/29/2015. In that paper, the inventor or a joint inventor, or for pre-AIA the applicant has stated move operations are performed based on a first predetermined status, and this statement indicates that the invention is different from what is defined in the claim(s) because the claims now recite copy operations are performed based on a first predetermined status, not move operations.

All remaining claims are rejected for being dependent on a rejected base claim.

8. Claims **1 – 2, 4 – 7, 9 – 12, and 14 - 15** rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

Claims 1, 6, and 11 contain the limitation of copying data based on a condition. The original specification and drawings disclose that a move operation is performed based on the condition listed in the claims. This makes the claims unclear as to if a move or copy operation is performed. The copy and move operations may be similar but that are different distinct operations in the computer art. The limitation of performing a copy operation is indefinite since the original disclosure fails to support such an operation.

All remaining claims are rejected for being dependent on a rejected base claim.

Claim Rejections - 35 USC § 103

9. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

10. The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

11. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103 are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claims **1 – 2, 4 – 7, 9 – 12, 14 – 19, and 21 - 22** is/are rejected under 35 U.S.C. 103 as being unpatentable over Yeh (Pub. No.: US 2012/0317346 A1) referred to as Yeh in view of Yu et al. (Pu. No.: US 2014/0006688) referred to as Yu.

Regarding **claim 1**, Yeh teaches a memory management method **[Figs 16 – 17]** configured for a rewritable non-volatile memory module **[100, Fig 1; 100, Fig 4]**, wherein the rewritable non-volatile memory module **[100, Fig 1; 100, Fig 4]** comprises a plurality of physical units **[304(0) – 304(R), Fig 4]**, and the memory management method **[Figs 16 – 17]** comprises:

receiving a write command **[S1603, Fig 16; Paragraphs 0013 – 0015, 0034, 0051, 0057, 0061, and 0091 – 0095; The host sends write commands to write data in the memory]** and determining whether a usage status of a plurality of first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to a storage area **[402, Fig 6]** among the plurality of physical units **[304(0) – 304(R), Fig 4]** conforms to a first predetermined status **[S1607, Fig 16; Paragraphs 0072 – 0074; The predetermined status is when the number of storage units storing valid data is less than a first threshold]**;

storing write data corresponding to the write command **[S1603, Fig 16; Paragraphs 0013 – 0015, 0034, 0051, 0057, 0061, and 0091 – 0095; The host sends write commands to write data in the memory]** in at least one second physical unit **[304(D+1), 304(D+2), and 304(N), Fig 6; Paragraph 0061, 0068, 0070; When data is written into memory it is written into a spare area of memory]** associated to a temporary area **[252, Fig 5; Paragraphs 0051, 0055, 0061; All the memory in the system is associated to a temporary area since the buffer is part of the overall system or the physical storage units themselves that store data temporarily until**

an erase operation is performed] among the plurality of physical units **[304(0) – 304(R), Fig 4]**;

associating the at least one second physical unit **[304(D+1), 304(D+2), and 304(N), Fig 6; Paragraph 0061, 0068, 0070; When data is written into memory it is written into a spare area of memory]** storing the write data to the storage area **[402, Fig 6; Figs 8 – 15; Paragraphs 0068 – 0088; As a spare erase block is used to store data and the spare erase block is associated with the storage area using the mapping table]** and allocating at least one logical unit to map **[Figs 7 – 15; S1609 and S1611, Fig 16; Logical units are mapped to each physical unit in the storage area]** the at least one second physical unit **[304(D+1), 304(D+2), and 304(N), Fig 6; Paragraph 0061, 0068, 0070; When data is written into memory it is written into a spare area of memory]** associated to the storage area **[402, Fig 6]** if the usage status of the first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to the storage area **[402, Fig 6]** conforms to the first predetermined status **[S1607 and S1609, Fig 16; Paragraphs 0055, 0066, 0068, 0094; The logical address shows a logical unit was allocated due to the memory status confirming to a first predetermine status determined in step S1607]**; and

performing a write operation if the usage status of the first physical units **[304(0), 304(1), and 304(D), Fig 6]** associated to the storage area **[402, Fig 6]** does not conform to the first predetermined status **[S1611, Fig 16]**,

wherein one memory cell in the at least one second physical unit **[304(D+1), 304(D+2), and 304(N), Fig 6]** associated to the temporary area **[252, Fig 5;**

Paragraphs 0051, 0055, 0061; All the memory in the system is associated to a temporary area since the buffer is part of the overall system or the physical storage units themselves that store data temporarily until an erase operation is performed] is configured to store at least one first bit **[Paragraphs 0008 and 0044 – 0045; Each memory cell in the MLC NAND flash memory stores two bits and the most significant bit is the at least one first bit and the total number of the at least one first bit is one]**,

wherein one memory cell in the first physical units **[304(0), 304(1), and 304(D), Fig 6]** associated to the storage area **[402, Fig 6]** is configured to store a plurality of second bits **[Paragraphs 0008 and 0044 – 0045; Each memory cell in the MLC NAND flash memory stores two bits and the two bits together are the second bits and the total number of the second bits in the MLC is two]**.

However, Yeh may not disclose the limitation of copying the write data in the at least one second physical unit associated to the temporary area to a physical unit associated to the storage area if the usage status of the first physical units associated to the storage area does not conform to the first predetermined status, one memory cell in the at least one second physical unit associated to the temporary area is configured to store only at least one first bit and a total number of the at least one first bit is a first number, wherein one memory cell in the first physical units associated to the storage area is configured to store a plurality of second bits and a total number of the second bits is a second number, and wherein the first number is less than the second number.

Yu discloses copying the write data in the at least one second physical unit associated to the temporary area to a physical unit associated to the storage area if the

usage status of the first physical units associated to the storage area does not conform to the first predetermined status **[Paragraph 0097; The wear leveling process copies data from one location to another location when usage status of memory does not confirm to a status that does not require wear leveling to happen]**, one memory cell in the at least one second physical unit is configured to store only at least one first bit and a total number of the at least one first bit is a first number, wherein one memory cell in the first physical units is configured to store a plurality of second bits and a total number of the second bits is a second number, and wherein the first number is less than the second number. **[Figs 5 – 7, 9 – 11, 14C, 16C, 17C, 18E – 18F, Paragraphs 0053 – 0054, The flash memory is comprised of SLC, MLC, and TLC memory cells. When a cell is configured as an SLC cell the memory cell only stores one bit and when the cell is configured as an MLC cell the memory cell stores two bits and one bit is less than two bits]**.

It would have been obvious to one or ordinary skill in the art before the effective filing date of the claimed invention to use Yu in Yeh, because it there is a need in flash memory to have certain cells programmed as MLC cells and other cells to be programmed as SLC cells **[Paragraph 0012]** and helps to improve noise margins against read errors **[Paragraph 0054]**.

Regarding **claim 2**, Yeh teaches the step of determining whether the usage status of the first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to the storage area **[402, Fig 6]** among the plurality of physical units **[304(0) – 304(R), Fig 4]** conforms to the first predetermined status comprises **[S1607, Fig 16]**:

determining whether a usage capacity of the first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to the storage area **[402, Fig 6]** conforms to a first predetermined capacity **[S1607 and S1609; Paragraph 0074; The system determines if the number of physical units storing valid data is less than a first predetermined capacity threshold]**,

wherein the usage capacity of the first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to the storage area **[402, Fig 6]** corresponds to a total data size of valid data stored in the first physical units **[304(0), 304(1), and 304(D), Fig 6]** associated to the storage area **[402, Fig 6; Paragraph 0074; The usage capacity is based on valid data in the physical erase unit]**.

Regarding **claim 4**, Yeh teaches a total available capacity of the first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to the storage area **[402, Fig 6]** is less than a total logical capacity **[Fig 6 – 7; Paragraphs 0060 – 0063; The storage area has a total available capacity of units 304(0) – 304(D) while the logical address space is able to address areas 304(0) - 304(R) indicating the total logical capacity is more than the capacity of the storage units in the storage area]** accessible to a host system **[Paragraphs 0013 – 0014 and 0061 - 0063; A host system sends write commands to the physical units to store data]**.

Regarding **claim 5**, Yeh teaches the total logical capacity remains unchanged if the total available capacity is changed from a first capacity to a second capacity

[Paragraph 0061; Associating a spare area erase unit to storage area 402 changes the total available capacity to a second capacity while the logical capacity remains the same].

Regarding **claim 6**, Yeh teaches a memory control circuit unit **[104, Fig 4; Fig 5]** configured to control a rewritable non-volatile memory module **[100, Fig 1; 100, Fig 4]**, wherein the rewritable non-volatile memory module **[100, Fig 1; 100, Fig 4]** comprises a plurality of physical units **[304(0) – 304(R), Fig 4]**, and the memory control circuit unit **[104, Fig 4; Fig 5]** comprises:

a host interface **[204, Fig 5]** configured to be coupled to a host system **[Paragraph 0052]**;

a memory interface **[206, Fig 5]** configured to be coupled to the rewritable non-volatile memory module **[100, Fig 1; 100, Fig 4; Paragraph 0053]**; and

a memory management circuit **[202, Fig 5]** coupled to the host interface **[204, Fig 5]** and the memory interface **[206, Fig 5]**,

wherein the memory management circuit **[202, Fig 5; Paragraph 0048]** is configured to receive a write command **[S1603, Fig 16; Paragraphs 0013 – 0015, 0034, 0051, 0057, 0061, and 0091 – 0095; The host sends write commands to write data in the memory]** and determine whether a usage status of a plurality of first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to a storage area **[402, Fig 6]** among the plurality of physical units **[304(0) – 304(R), Fig 4]** conforms to a first predetermined status **[S1607, Fig 16; Paragraphs 0072 – 0074; The**

predetermined status is when the number of storage units storing valid data is less than a first threshold],

wherein the memory management circuit **[202, Fig 5; Paragraph 0048]** is further configured to send a write command sequence **[S1603, Fig 16; Paragraphs 0013 – 0015, 0034, 0051, 0057, 0061, and 0091 – 0095; The host sends write commands to write data in the memory]**, wherein the write command sequence **[S1603, Fig 16; Paragraphs 0013 – 0015, 0034, 0051, 0057, 0061, and 0091 – 0095; The host sends write commands to write data in the memory]** is configured to instruct storing write data corresponding to the write command **[S1603, Fig 16; Paragraphs 0013 – 0015, 0034, 0051, 0057, 0061, and 0091 – 0095; The host sends write commands to write data in the memory]** in at least one second physical unit **[304(D+1), 304(D+2), and 304(N), Fig 6; Paragraph 0061, 0068, 0070; When data is written into memory it is written into a spare area of memory]** associated to a temporary area **[252, Fig 5; Paragraphs 0051, 0055, 0061; All the memory in the system is associated to a temporary area since the buffer is part of the overall system or the physical storage units themselves that store data temporarily until an erase operation is performed]** among the plurality of physical units **[304(0) – 304(R), Fig 4; S1607 and S1609, Fig 16; Paragraph 0055; The buffer is temporary memory that is associated to a physical unit dependent on the determine in figure 16 since the determine in figure 16 determine where the data in the buffer is stored]**,

wherein the memory management circuit **[202, Fig 5; Paragraph 0048]** is further configured to associate the at least one second physical unit **[304(D+1), 304(D+2), and 304(N), Fig 6; Paragraph 0061, 0068, 0070; When data is written into memory it is**

written into a spare area of memory] storing the write data to the storage area **[402, Fig 6; Figs 8 – 15; Paragraphs 0068 – 0088; As a spare erase block is used to store data the spare erase block is associated with the storage area using the mapping table]** and allocate at least one logical unit to map **[Figs 7 – 15; S1609 and S1611, Fig 16; Logical units are mapped to each physical unit in a storage area]** the at least one second physical unit **[304(D+1), 304(D+2), and 304(N), Fig 6; Paragraph 0061, 0068, 0070; When data is written into memory it is written into a spare area of memory]** associated to the storage area **[402, Fig 6]** if the usage status of the first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to the storage area **[402, Fig 6]** conforms to the first predetermined status **[S1607 and S1609, Fig 16]**,

wherein the memory management circuit **[202, Fig 5; Paragraph 0048]** is further configured to perform a write operation if the usage status of the first physical units **[304(0), 304(1), and 304(D), Fig 6]** associated to the storage area **[402, Fig 6]** does not conform to the first predetermined status **[S1611, Fig 16]**,

wherein one memory cell in the at least one second physical unit **[304(D+1), 304(D+2), and 304(N), Fig 6]** associated to the temporary area **[252, Fig 5; Paragraphs 0051, 0055, 0061; All the memory in the system is associated to a temporary area since the buffer is part of the overall system or the physical storage units themselves that store data temporarily until an erase operation is performed]** is configured to store at least one first bit **[Paragraphs 0008 and 0044 – 0045; Each memory cell in the MLC NAND flash memory stores two bits and the**

most significant bit is the at least one first bit and the total number of the at least one first bit is one],

wherein one memory cell in the first physical units **[304(0), 304(1), and 304(D), Fig 6]** associated to the storage area **[402, Fig 6]** is configured to store a plurality of second bits **[Paragraphs 0008 and 0044 – 0045; Each memory cell in the MLC NAND flash memory stores two bits and the two bits together are the second bits and the total number of the second bits in the MLC is two]**.

However, Yeh may not disclose the limitation of copying the write data in the at least one second physical unit associated to the temporary area to a physical unit associated to the storage area if the usage status of the first physical units associated to the storage area does not conform to the first predetermined status , one memory cell in the at least one second physical unit associated to the temporary area is configured to store only at least one first bit and a total number of the at least one first bit is a first number, wherein one memory cell in the first physical units associated to the storage area is configured to store a plurality of second bits and a total number of the second bits is a second number, and wherein the first number is less than the second number.

Yu discloses copying the write data in the at least one second physical unit associated to the temporary area to a physical unit associated to the storage area if the usage status of the first physical units associated to the storage area does not conform to the first predetermined status **[Paragraph 0097; The wear leveling process copies data from one location to another location when usage status of memory does not confirm to a status that does not require wear leveling to happen]**, one memory cell in the at least one second physical unit is configured to store only at least

one first bit and a total number of the at least one first bit is a first number, wherein one memory cell in the first physical units is configured to store a plurality of second bits and a total number of the second bits is a second number, and wherein the first number is less than the second number. **[Figs 5 – 7, 9 – 11, 14C, 16C, 17C, 18E – 18F, Paragraphs 0053 – 0054, The flash memory is comprised of SLC, MLC, and TLC memory cells. When a cell is configured as an SLC cell the memory cell only stores one bit and when the cell is configured as an MLC cell the memory cell stores two bits and one bit is less than two bits]**.

It would have been obvious to one or ordinary skill in the art before the effective filing date of the claimed invention to use Yu in Yeh, because it there is a need in flash memory to have certain cells programmed as MLC cells and other cells to be programmed as SLC cells **[Paragraph 0012]** and helps to improve noise margins against read errors **[Paragraph 0054]**.

Regarding **claim 7**, Yeh teaches the operation of determining whether the usage status of first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to the storage area **[402, Fig 6]** among the plurality of physical units **[304(0) – 304(R), Fig 4]** conforms to the first predetermined status **[S1607, Fig 16]** by the memory management circuit **[202, Fig 5; Paragraph 0048]** comprises:

determining whether a usage capacity of the first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to the storage area **[402, Fig 6]** conforms to a first predetermined capacity **[S1607 and S1609; Paragraph 0074; The system**

determines if the number of physical units storing valid data is less than a first predetermined capacity threshold],

wherein the usage capacity of the first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to the storage area **[402, Fig 6]** corresponds to a total data size of valid data stored in the first physical units **[304(0), 304(1), and 304(D), Fig 6]** associated to the storage area **[402, Fig 6; Paragraph 0074; The usage capacity is based on valid data in the physical erase unit]**.

Regarding **claim 9**, Yeh teaches a total available capacity of the first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to the storage area **[402, Fig 6]** is less than a total logical capacity **[Fig 6 – 7; Paragraphs 0060 – 0063; The storage area has a total available capacity of units 304(0) – 304(D) while the logical address space is able to address areas 304(0) - 304(R) indicating the total logical capacity is more than the capacity of the storage units in the storage area]** accessible to a host system **[Paragraphs 0013 – 0014 and 0061 - 0063; A host system sends write commands to the physical units to store data]**.

Regarding **claim 10**, Yeh teaches the total logical capacity remains unchanged if the total available capacity is changed from a first capacity to a second capacity **[Paragraph 0061; Associating a spare area erase unit to storage area 402 changes the total available capacity to a second capacity while the logical capacity remains the same]**.

Regarding **claim 11**, Yeh teaches a connection interface **[204, Fig 5]** unit configured to be coupled to a host system **[Paragraph 0052]**;

a rewritable non-volatile memory module **[100, Fig 1; 100, Fig 4; Paragraph 0053]** comprising a plurality of physical units **[304(0) – 304(R), Fig 4]**; and

a memory control circuit unit **[202, Fig 5]** coupled to the connection interface unit **[204, Fig 5]** and the rewritable non-volatile memory module **[100, Fig 1; 100, Fig 4; Paragraph 0053]**,

wherein the memory control circuit unit **[202, Fig 5; Paragraph 0048]** is configured to receive a write command **[S1603, Fig 16; Paragraphs 0013 – 0015, 0034, 0051, 0057, 0061, and 0091 – 0095; The host sends write commands to write data in the memory]** and determine whether a usage status of a plurality of first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to a storage area **[402, Fig 6]** among the plurality of physical units **[304(0) – 304(R), Fig 4]** conforms to a first predetermined status **[S1607, Fig 16; Paragraphs 0072 – 0074; The predetermined status is when the number of storage units storing valid data is less than a first threshold]**,

wherein the memory control circuit unit **[202, Fig 5; Paragraph 0048]** is further configured to send a write command sequence **[S1603, Fig 16; Paragraphs 0013 – 0015, 0034, 0051, 0057, 0061, and 0091 – 0095; The host sends write commands to write data in the memory]**, wherein the write command sequence **[S1603, Fig 16; Paragraphs 0013 – 0015, 0034, 0051, 0057, 0061, and 0091 – 0095; The host sends write commands to write data in the memory]** is configured to instruct storing write

data corresponding to the write command **[S1603, Fig 16; Paragraphs 0013 – 0015, 0034, 0051, 0057, 0061, and 0091 – 0095; The host sends write commands to write data in the memory]** in at least one second physical unit **[304(D+1), 304(D+2), and 304(N), Fig 6; Paragraph 0061, 0068, 0070; When data is written into memory it is written into a spare area of memory]** associated to a temporary area **[252, Fig 5; Paragraphs 0051, 0055, 0061; All the memory in the system is associated to a temporary area since the buffer is part of the overall system or the physical storage units themselves that store data temporarily until an erase operation is performed]** among the plurality of physical units **[304(0) – 304(R), Fig 4; S1607 and S1609, Fig 16; Paragraph 0055; The buffer is temporary memory that is associated to a physical unit dependent on the determine in figure 16 since the determine in figure 16 determine where the data in the buffer is stored]**,

wherein the memory management circuit **[202, Fig 5; Paragraph 0048]** is further configured to associate the at least one second physical unit **[304(D+1), 304(D+2), and 304(N), Fig 6; Paragraph 0061, 0068, 0070; When data is written into memory it is written into a spare area of memory]** storing the write data to the storage area **[402, Fig 6; Figs 8 – 15; Paragraphs 0068 – 0088; As a spare erase block is used to store data the spare erase block is associated with the storage area using the mapping table]** and allocate at least one logical unit to map **[Figs 7 – 15; S1609 and S1611, Fig 16; Logical units are mapped to each physical unit in the storage area]** the at least one second physical unit **[304(D+1), 304(D+2), and 304(N), Fig 6; Paragraph 0061, 0068, 0070; When data is written into memory it is written into a spare area of memory]** associated to the storage area **[402, Fig 6]** if the usage status

of the first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to the storage area **[402, Fig 6]** conforms to the first predetermined status **[S1607 and S1609, Fig 16; Paragraphs 0055, 0066, 0068, 0094; The logical address shows a logical unit was allocated due to the memory status confirming to a first predetermine status determined in step S1607]**,

wherein the memory management circuit **[202, Fig 5; Paragraph 0048]** is further configured to perform a write operation if the usage status of the first physical units **[304(0), 304(1), and 304(D), Fig 6]** associated to the storage area **[402, Fig 6]** does not conform to the first predetermined status **[S1611, Fig 16]**

wherein one memory cell in the at least one second physical unit **[304(D+1), 304(D+2), and 304(N), Fig 6]** associated to the temporary area **[252, Fig 5; Paragraphs 0051, 0055, 0061; All the memory in the system is associated to a temporary area since the buffer is part of the overall system or the physical storage units themselves that store data temporarily until an erase operation is performed]** is configured to store at least one first bit **[Paragraphs 0008 and 0044 – 0045; Each memory cell in the MLC NAND flash memory stores two bits and the most significant bit is the at least one first bit and the total number of the at least one first bit is one]**,

wherein one memory cell in the first physical units **[304(0), 304(1), and 304(D), Fig 6]** associated to the storage area **[402, Fig 6]** is configured to store a plurality of second bits **[Paragraphs 0008 and 0044 – 0045; Each memory cell in the MLC**

NAND flash memory stores two bits and the two bits together are the second bits and the total number of the second bits in the MLC is two].

However, Yeh may not disclose the limitation of copying the write data in the at least one second physical unit associated to the temporary area to a physical unit associated to the storage area if the usage status of the first physical units associated to the storage area does not conform to the first predetermined status, one memory cell in the at least one second physical unit associated to the temporary area is configured to store only at least one first bit and a total number of the at least one first bit is a first number, wherein one memory cell in the first physical units associated to the storage area is configured to store a plurality of second bits and a total number of the second bits is a second number, and wherein the first number is less than the second number.

Yu discloses copying the write data in the at least one second physical unit associated to the temporary area to a physical unit associated to the storage area if the usage status of the first physical units associated to the storage area does not conform to the first predetermined status **[Paragraph 0097; The wear leveling process copies data from one location to another location when usage status of memory does not confirm to a status that does not require wear leveling to happen]**, one memory cell in the at least one second physical unit is configured to store only at least one first bit and a total number of the at least one first bit is a first number, wherein one memory cell in the first physical units is configured to store a plurality of second bits and a total number of the second bits is a second number, and wherein the first number is less than the second number. **[Figs 5 – 7, 9 – 11, 14C, 16C, 17C, 18E – 18F, Paragraphs 0053 – 0054, The flash memory is comprised of SLC, MLC, and TLC**

memory cells. When a cell is configured as an SLC cell the memory cell only stores one bit and when the cell is configured as an MLC cell the memory cell stores two bits and one bit is less than two bits].

It would have been obvious to one or ordinary skill in the art before the effective filing date of the claimed invention to use Yu in Yeh, because it there is a need in flash memory to have certain cells programmed as MLC cells and other cells to be programmed as SLC cells **[Paragraph 0012]** and helps to improve noise margins against read errors **[Paragraph 0054]**.

Regarding **claim 12**, Yeh teaches the operation of determining whether the usage status of the first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to the storage area **[402, Fig 6]** conforms to the first predetermined status **[S1607, Fig 16]** by the memory control circuit unit **[202, Fig 5; Paragraph 0048]** comprises:

determining whether a usage capacity of the first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to the storage area **[402, Fig 6]** conforms to a first predetermined capacity **[S1607 and S1609; Paragraph 0074; The system determines if the number of physical units storing valid data is less than a first predetermined capacity threshold]**,

wherein the usage capacity of the first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to the storage area **[402, Fig 6]** corresponds to a total

data size of valid data stored in the first physical units **[304(0), 304(1), and 304(D), Fig 6]** associated to the storage area **[402, Fig 6; Paragraph 0074; The usage capacity is based on valid data in the physical erase unit]**.

Regarding **claim 14**, Yeh teaches a total available capacity of the first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to the storage area **[402, Fig 6]** is less than a total logical capacity **[Fig 6 – 7; Paragraphs 0060 – 0063; The storage area has a total available capacity of units 304(0) – 304(D) while the logical address space is able to address areas 304(0) - 304(R) indicating the total logical capacity is more than the capacity of the storage units in the storage area]** accessible to a host system **[Paragraphs 0013 – 0014 and 0061 - 0063; A host system sends write commands to the physical units to store data]**.

Regarding **claim 15**, Yeh teaches the total logical capacity remains unchanged if the total available capacity is changed from a first capacity to a second capacity **[Paragraph 0061; Associating a spare area erase unit to storage area 402 changes the total available capacity to a second capacity while the logical capacity remains the same]**.

Regarding **claim 16**, Yeh teaches a memory management method **[Figs 16 – 17]** configured for a rewritable non-volatile memory module **[100, Fig 1; 100, Fig 4]**, wherein the rewritable non-volatile memory module **[100, Fig 1; 100, Fig 4]** comprises a plurality of physical units **[304(0) – 304(R), Fig 4]**, and the memory management method **[Figs 16 – 17]** comprises:

allocating a plurality of logical units to map **[Figs 7 – 15; S1609 and S1611, Fig 16; Logical units are mapped to each physical unit in a storage area]** a plurality of first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to a storage area **[402, Fig 6]** among the plurality of physical units **[304(0) – 304(R), Fig 4]**;

receiving an operation command **[S1603, Fig 16; Paragraphs 0013 – 0015, 0034, 0051, 0057, 0061, and 0091 – 0095; The host sends write commands to write data in the memory]** and determining whether a usage status of the first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to the storage area **[402, Fig 6]** conforms to a second predetermined status **[S1607, Fig 16]**;

associating at least one second physical unit **[Fig 6; Any erase unit in the first plurality of physical units]** of the first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to the storage area **[402, Fig 6]** to a temporary area **[402, Fig 6; Paragraphs 0055 and 0061; The physical storage units themselves store data temporarily until an erase operation is performed]** and removing a logical-to-physical mapping relationship corresponding to the at least one second physical unit **[Fig 6; Any erase unit in the first plurality of physical units]** changed to be associated to the temporary area instead **[Figs 8 – 11; Paragraph 0055, 0061, 0068, and 0094 - 0095; Erasing and programming the physical units of storage removes logical mapping information and replaces it with new logical mapping information]** if the usage status of the first physical units **[304(0), 304(1), and 304(D),**

Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data] associated to the storage area **[402, Fig 6]** conforms to the second predetermined status **[S1609, Fig 16; Erasing a physical program unit associates the physical program unit with other erased or invalid physical program units]**; and

keeping the at least one second physical unit **[Fig 6; Any erase unit in the first plurality of physical units]** being associated to the storage area **[402, Fig 6]** if the usage status of the first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to the storage area **[402, Fig 6]** does not conform to the second predetermined status **[S1611, Fig 16; Physical units that store data are associated with the storage area when the determination is "No"]**.

wherein one memory cell in the second physical unit **[304(D+1), 304(D+2), and 304(N), Fig 6]** associated to the temporary area **[252, Fig 5; Paragraphs 0051, 0055, 0061; All the memory in the system is associated to a temporary area since the buffer is part of the overall system or the physical storage units themselves that store data temporarily until an erase operation is performed]** is configured to store at least one first bit **[Paragraphs 0008 and 0044 – 0045; Each memory cell in the MLC NAND flash memory stores two bits and the most significant bit is the at least one first bit and the total number of the at least one first bit is one]**,

wherein one memory cell in the first physical units **[304(0), 304(1), and 304(D), Fig 6]** associated to the storage area **[402, Fig 6]** is configured to store a plurality of second bits **[Paragraphs 0008 and 0044 – 0045; Each memory cell in the MLC**

NAND flash memory stores two bits and the two bits together are the second bits and the total number of the second bits in the MLC is two].

However, Yeh may not disclose the limitation of wherein one memory cell in the at least one second physical unit associated to the temporary area is configured to store only at least one first bit and a total number of the at least one first bit is a first number, wherein one memory cell in the first physical units associated to the storage area is configured to store a plurality of second bits and a total number of the second bits is a second number, and wherein the first number is less than the second number.

Yu discloses one memory cell in the second physical unit is configured to store only at least one first bit and a total number of the at least one first bit is a first number, wherein one memory cell in the first physical units is configured to store a plurality of second bits and a total number of the second bits is a second number, and wherein the first number is less than the second number. **[Figs 5 – 7, 9 – 11, 14C, 16C, 17C, 18E – 18F, Paragraphs 0053 – 0054, The flash memory is comprised of SLC, MLC, and TLC memory cells. When a cell is configured as an SLC cell the memory cell only stores one bit and when the cell is configured as an MLC cell the memory cell stores two bits and one bit is less than two bits]**.

It would have been obvious to one or ordinary skill in the art before the effective filing date of the claimed invention to use Yu in Yeh, because it there is a need in flash memory to have certain cells programmed as MLC cells and other cells to be programmed as SLC cells **[Paragraph 0012]** and helps to improve noise margins against read errors **[Paragraph 0054]**.

Regarding **claim 17**, Yeh teaches the operation command instructs deleting first data **[Paragraph 0061; An erasing operation is deleting data]**.

Regarding **claim 18**, Yeh teaches the step of determining whether the usage status of the first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to the storage area **[402, Fig 6]** conforms to the second predetermined status **[S1607 and S1611, Fig 16]** comprises:

determining whether the first data is stored in a predetermined physical unit that can be associated to the temporary area among the first physical units **[Paragraphs 0055 and 0061; An erase operation determines where data is in the physical units to perform the erase operation and each physical unit is associated to the temporary area since each unit stores data temporarily until an erase operation is performed]**.

Regarding **claim 19**, Yeh teaches the step of determining whether the usage status of the first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to the storage area **[402, Fig 6]** conforms to the second predetermined status **[S1607 and S1611, Fig 16]** comprises:

determining whether a usage capacity of the first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to the storage area **[402, Fig 6]** conforms to a second predetermined capacity **[S1607; Paragraph 0074; The system**

determines if the number of physical units storing valid data is less than a first predetermined capacity threshold],

wherein the usage capacity of the first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to the storage area **[402, Fig 6]** corresponds to a total data size of valid data stored in the first physical units **[304(0), 304(1), and 304(D), Fig 6]** associated to the storage area **[402, Fig 6; Paragraph 0074; The usage capacity is based on valid data in the physical erase unit]**.

Regarding **claim 21**, Yeh teaches a total available capacity of the first physical units **[304(0), 304(1), and 304(D), Fig 6; Paragraph 0074; The first physical units are the physical storage units storing valid data]** associated to the storage area **[402, Fig 6]** is less than a total logical capacity **[Fig 6 – 7; Paragraphs 0060 – 0063; The storage area has a total available capacity of units 304(0) – 304(D) while the logical address space is able to address areas 304(0) - 304(R) indicating the total logical capacity is more than the capacity of the storage units in the storage area]** accessible to a host system **[Paragraphs 0013 – 0014 and 0061 - 0063; A host system sends write commands to the physical units to store data]**.

Regarding **claim 22**, Yeh teaches the total logical capacity remains unchanged if the total available capacity is changed from a first capacity to a second capacity **[Paragraph 0061; Associating a spare area erase unit to storage area 402 changes the total available capacity to a second capacity while the logical capacity remains the same]**.

Response to Arguments

13. Applicant's arguments filed 04/11/2019 have been fully considered but they are not persuasive.

The Applicant argues on page 11 that the amendments are supported by paragraphs 0087 and 0093 of the originally filed specification. After careful consideration of the Applicant's arguments the Examiner respectfully disagrees.

The amended claims 1, 6, and 11 recite the limitation of copying data. Paragraph 0087 specifically discloses the operation performed is a move operation. A move and copy operation in computer memory may be similar but are two different distinct operations. This shows the originally filed specification fails to properly support the claimed limitation of a copy operation.

The Applicant argues on pages 11 – 17 that Yeh fails to teach the associating and the allocating operations or the copying operation on the blocks storing data based on whether the usage status of other physical blocks associated to the storage area conform to a predetermined status as recited in claims 1, 6, and 11 along with the associating and the removing operations or the keeping operation on the blocks storing data based on whether the usage status of other physical blocks associated to the "storage area" conform to a predetermined status of claim 16 and that Yu fails to cure the argued deficiencies of Yeh. After careful consideration of the Applicant's arguments the Examiner respectfully disagrees.

The arguments fail to properly explain how the claim limitations are not taught by the prior art other than saying they do not. There are no specific examples or explanation detailing how the prior art is different from the current claim limitations. The

rejections contain citations and explanation explaining and detailing how the prior art teaches the current claim limitations. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Carannante et al. (Pat 8,924,638) discloses flash memory using wear-leveling where data stored in one section of memory is moved to another section of memory and the associated mapping information is changed to reflect the new storage location of the data.

Chang et al. (Pat 8,909,846) discloses if a physical block address has met the wear-leveling condition, and the address of the logical block to which the source pointer register points does not appear in the hot data list, it can be determined that the data in the logical block is infrequently updated which should be moved to a physical block having overly high erase count to prevent the physical block from undertaking excessive erase wearing.

Davis et al. (Pat 8,874,835) discloses flash memory using wear-leveling where data stored in one section of memory is moved to another section of memory and the associated mapping information is changed to reflect the new storage location of the data.

Jones et al. (Pat 8,972,681) discloses a wear-leveling module selects a physical block from a free block list and writes the new data to the new physical block. The wear-leveling module modifies the mapping table to map the new physical block to the first logical block address received with the ECOW command.

Jones et al. (Pat 8,868,869) discloses a wear-leveling module selects a physical block from a free block list and writes the new data to the new physical block. The wear-leveling module modifies the mapping table to map the new physical block to the first logical block address received with the ECOW command.

Rao (Pat 8,891,298) discloses a controller's wear-leveling algorithm determines which physical block to use each time data is programmed, eliminating the relevance of the physical location of data and enabling data to be stored anywhere within the memory array and thus prolonging the service life of the flash memory. Depending on the wear-leveling method used, the controller typically either writes to the available erased block with the lowest erase count (dynamic wear leveling); or it selects an available target block with the lowest overall erase count, erases the block if necessary, writes new data to the block, and ensures that blocks of static data are moved when their block erase count is below a certain threshold (static wear leveling).

Wu et al. (Pub. No.: US 2014/0331024) discloses when data is moved within the non-volatile memory due to the operations such as trim, wear-leveling and mapping transformation, some data stored in the non-volatile memory may be marked as invalid data. When the amount of invalid data increases and occupies considerable storage space, the memory controller may use the garbage collection to erase the invalid data, in order to clear out the memory space. In general, a physical block with more invalid

data is more likely to undergo the garbage collection. After garbage collection is performed on a physical block, the physical block is cleared out to be an unmapped block and can be utilized for storing new data. Therefore, the number of unmapped blocks may be increased.

Yu et al. (Pat 8,959,280) discloses two types of wear leveling methods. One is to dynamically choose the lowest wear leveling count block from the available empty blocks to write data to. The other method is based on the criteria of a wear leveling count threshold. Once this threshold is reached, blocks of flash data are moved from one physical block (with a low wear leveling count) to another empty physical block (with a high wear leveling count) in flash memory. Updates are made to the logical-to-physical mapping in mapping tables that are managed by table manager. Table manager also tracks the type of data that is stored in each logical block so that temp files, paging files, FAT, FDB, and user data files are tracked once identified and categorized.

Yu et al. (Pat 8,954,654) discloses two methods for wear leveling. One method is to dynamically choose the lowest wear leveling count block from the available empty blocks to write data to. The other method is based on a wear leveling count threshold. Once this threshold is reached, blocks of flash data are moved from one physical block (with a low wear leveling count) to another empty physical block (with a high wear leveling count) in flash memory.

Yu et al. (Pub. No.: US 2014/0310574) discloses two methods for wear leveling. One method is to dynamically choose the lowest wear leveling count block from the available empty blocks to write data to. The other method is based on a wear leveling

count threshold. Once this threshold is reached, blocks of flash data are moved from one physical block (with a low wear leveling count) to another empty physical block (with a high wear leveling count) in flash memory.

Yu et al. (Pub. No.: US 2014/0281151) discloses two methods for wear leveling. One method is to dynamically choose the lowest wear leveling count block from the available empty blocks to write data to. The other method is based on a wear leveling count threshold. Once this threshold is reached, blocks of flash data are moved from one physical block (with a low wear leveling count) to another empty physical block (with a high wear leveling count) in flash memory.

Microsoft (Computer Dictionary) discloses the differences between a copy operation and a move operation.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER D BIRKHIMER whose telephone number is (571)270-1178. The examiner can normally be reached on 8-5 Hoteling.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Rones can be reached on 571-272-4085. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Christopher D Birkhimer/
Primary Examiner, Art Unit 2136

Notice of References Cited	Application/Control No. 14/811,844	Applicant(s)/Patent Under Reexamination Yeh, Chih-Kang	
	Examiner CHRISTOPHER D BIRKHIMER	Art Unit 2136	Page 1 of 1

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*	A	US-8972681-B2	03-2015	Jones; Carl Evan	G06F3/065	707/639
*	B	US-8959280-B2	02-2015	Yu; Frank	G06F3/0608	711/103
*	C	US-8954654-B2	02-2015	Yu; Frank	G06F12/0246	711/103
*	D	US-8924638-B2	12-2014	Carannante; Procolo	G06F12/0246	711/103
*	E	US-8909846-B2	12-2014	Chang; Li-Pin	G06F12/0246	711/103
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*	G	US-8874835-B1	10-2014	Davis; John	G06F3/0679	711/103
*	H	US-20140331024-A1	11-2014	Wu; Yi-Cheng	G06F12/06	711/209
*	I	US-8868869-B2	10-2014	Jones; Carl Evan	G06F3/065	707/639
*	J	US-20140310574-A1	10-2014	Yu; Frank	G06F11/1072	714/773
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	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Microsoft, "Computer Dictionary", Fifth Edition, 2002, Pages 130 and 349 (Year: 2002)
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14/811,844	Yeh, Chih-Kang
	Examiner	**Art Unit**
	CHRISTOPHER D BIRKHIMER	2136

CPC - Searched*		
Symbol	**Date**	**Examiner**
G06F3/061 or G06F3/064 or G06F3/0679 or G06F12/0246 or G06F2212/7201 with and without text	12/01/2017	CDB
G06F3/061 or G06F3/064 or G06F3/0679 or G06F12/0246 or G06F2212/7201 with and without text	04/12/2018	CDB
G06F3/061 or G06F3/064 or G06F3/0679 or G06F12/0246 or G06F2212/7201 with and without text	09/06/2018	CDB
G06F3/061 or G06F3/064 or G06F3/0679 or G06F12/0246 or G06F2212/7201 with and without text	01/03/2019	CDB
G06F3/061 or G06F3/064 or G06F3/0679 or G06F12/0246 or G06F2212/7201 with and without text	05/07/2019	CDB

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

/Christopher D Birkhimer/ Primary Examiner, Art Unit 2136	

Vervain Ex. 2046 p. 37 of 45
Vervain v. Phison
IPR2025-00215

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14/811,844	Yeh, Chih-Kang
	Examiner	**Art Unit**
	CHRISTOPHER D BIRKHIMER	2136

Search Notes		
Search Notes	**Date**	**Examiner**
EAST search performed	12/01/2017	CDB
Assignee search performed in EAST	12/01/2017	CDB
Inventor search performed in EAST	12/01/2017	CDB
Google Internet database search performed	12/01/2017	CDB
EAST search updated	04/12/2018	CDB
Assignee search updated in EAST	04/12/2018	CDB
Inventor search updated in EAST	04/12/2018	CDB
EAST search updated	09/06/2018	CDB
Assignee search updated in EAST	09/06/2018	CDB
Inventor search updated in EAST	09/06/2018	CDB
EAST search updated	01/03/2019	CDB
Assignee search updated in EAST	01/03/2019	CDB
Inventor search updated in EAST	01/03/2019	CDB
Google Internet database search updated	01/03/2019	CDB
EAST search updated	05/07/2019	CDB
Assignee search updated in EAST	05/07/2019	CDB
Inventor search updated in EAST	05/07/2019	CDB

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**

/Christopher D Birkhimer/ Primary Examiner, Art Unit 2136	

Vervain Ex. 2046 p. 38 of 45
Vervain v. Phison
IPR2025-00215

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14/811,844	Yeh, Chih-Kang
	Examiner	**Art Unit**
	CHRISTOPHER D BIRKHIMER	2136

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/01/2017	04/12/2018	09/06/2018	01/03/2019	05/07/2019				
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	3	✓	✓	-	-	-				
	4	✓	✓	✓	✓	✓				
	5	✓	✓	✓	✓	✓				
	6	✓	✓	✓	✓	✓				
	7	✓	✓	✓	✓	✓				
	8	✓	✓	-	-	-				
	9	✓	✓	✓	✓	✓				
	10	✓	✓	✓	✓	✓				
	11	✓	✓	✓	✓	✓				
	12	✓	✓	✓	✓	✓				
	13	✓	✓	-	-	-				
	14	✓	✓	✓	✓	✓				
	15	✓	✓	✓	✓	✓				
	16	✓	✓	✓	✓	✓				
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	18	✓	✓	✓	✓	✓				
	19	✓	✓	✓	✓	✓				
	20	✓	✓	-	-	-				
	21	✓	✓	✓	✓	✓				
	22	✓	✓	✓	✓	✓				

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S168	200	S165 and flash and ((wear-level$4 or (wear near2 level$2)) same moved)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 11:46
S167	2026	S165 and flash and (wear-level$4 or (wear near2 level$2) same moved)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 11:45
S166	2792	S165 and flash and (wear-level$4 or (wear near2 level$2))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 11:42
S165	66534	(G06F3/061 or G06F3/064 or G06F3/0679 or G06F12/0246 or G06F2212/7201).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 11:42
S164	110	hybrid near5 (MLC/SLC or (MLC near5 SLC)) near5 flash	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/05/06 10:24
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S162	168	S161 and (usage near5 status) and (logical same physical)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S161	66534	(G06F3/061 or G06F3/064 or G06F3/0679 or G06F12/0246 or G06F2212/7201).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S160	10	(S157 or S158) and S155 and (usage near5 status)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S159	742	(S157 or S158) and S155	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S158	2179	(PHISON near3 ELECTRONICS near3 CORP).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S157	245	(Yeh near3 Chih-Kang).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24

S156	114	(("YEH") near3 ("Chih-Kang")).INV.	USPAT	OR	OFF	2019/05/06 10:24
S155	66534	(G06F3/061 or G06F3/064 or G06F3/0679 or G06F12/0246 or G06F2212/7201).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S154	3	"20120317346"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S153	8	"201351140"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S152	168	S151 and (usage near5 status) and (logical same physical)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S151	66534	(G06F3/061 or G06F3/064 or G06F3/0679 or G06F12/0246 or G06F2212/7201).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S150	10	(S147 or S148) and S145 and (usage near5 status)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S149	742	(S147 or S148) and S145	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S148	2179	(PHISON near3 ELECTRONICS near3 CORP).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S147	245	(Yeh near3 Chih-Kang).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S146	114	(("YEH") near3 ("Chih-Kang")).INV.	USPAT	OR	OFF	2019/05/06 10:24
S145	66534	(G06F3/061 or G06F3/064 or G06F3/0679 or G06F12/0246 or G06F2212/7201).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S144	3	"20120317346"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S143	8	"201351140"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S142	168	S141 and (usage near5 status) and (logical same physical)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S141	66534	(G06F3/061 or G06F3/064 or G06F3/0679 or G06F12/0246	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	OFF	2019/05/06 10:24

		or G06F2212/7201).cpc.	JPO; DERWENT; IBM_TDB			
S140	10	(S137 or S138) and S135 and (usage near5 status)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S139	742	(S137 or S138) and S135	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S138	2179	(PHISON near3 ELECTRONICS near3 CORP).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S137	245	(Yeh near3 Chih-Kang).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S136	114	(("YEH") near3 ("Chih-Kang")).INV.	USPAT	OR	OFF	2019/05/06 10:24
S135	66534	(G06F3/061 or G06F3/064 or G06F3/0679 or G06F12/0246 or G06F2212/7201).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S134	3	"20120317346"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S133	8	"201351140"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S132	168	S131 and (usage near5 status) and (logical same physical)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S131	66534	(G06F3/061 or G06F3/064 or G06F3/0679 or G06F12/0246 or G06F2212/7201).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S130	10	(S127 or S128) and S125 and (usage near5 status)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S129	742	(S127 or S128) and S125	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S128	2179	(PHISON near3 ELECTRONICS near3 CORP).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S127	245	(Yeh near3 Chih-Kang).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S126	114	(("YEH") near3 ("Chih-Kang")).INV.	USPAT	OR	OFF	2019/05/06 10:24

S125	66534	(G06F3/061 or G06F3/064 or G06F3/0679 or G06F12/0246 or G06F2212/7201).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S124	3	"20120317346"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S123	8	"201351140"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S122	168	S121 and (usage near5 status) and (logical same physical)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S121	66534	(G06F3/061 or G06F3/064 or G06F3/0679 or G06F12/0246 or G06F2212/7201).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S120	10	(S117 or S118) and S115 and (usage near5 status)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S119	742	(S117 or S118) and S115	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S118	2179	(PHISON near3 ELECTRONICS near3 CORP).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S117	245	(Yeh near3 Chih-Kang).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S116	114	(("YEH") near3 ("Chih-Kang")).INV.	USPAT	OR	OFF	2019/05/06 10:24
S115	66534	(G06F3/061 or G06F3/064 or G06F3/0679 or G06F12/0246 or G06F2212/7201).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S114	3	"20120317346"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S113	8	"201351140"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S112	168	S111 and (usage near5 status) and (logical same physical)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S111	66534	(G06F3/061 or G06F3/064 or G06F3/0679 or G06F12/0246 or G06F2212/7201).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24

S110	10	(S107 or S108) and S105 and (usage near5 status)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S109	742	(S107 or S108) and S105	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S108	2179	(PHISON near3 ELECTRONICS near3 CORP).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S107	245	(Yeh near3 Chih-Kang).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S106	114	(("YEH") near3 ("Chih-Kang")).INV.	USPAT	OR	OFF	2019/05/06 10:24
S105	66534	(G06F3/061 or G06F3/064 or G06F3/0679 or G06F12/0246 or G06F2212/7201).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S104	3	"20120317346"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S103	8	"201351140"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S102	168	S101 and (usage near5 status) and (logical same physical)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S101	66534	(G06F3/061 or G06F3/064 or G06F3/0679 or G06F12/0246 or G06F2212/7201).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S100	10	(S97 or S98) and S95 and (usage near5 status)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S99	742	(S97 or S98) and S95	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S98	2179	(PHISON near3 ELECTRONICS near3 CORP).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S97	245	(Yeh near3 Chih-Kang).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S96	114	(("YEH") near3 ("Chih-Kang")).INV.	USPAT	OR	OFF	2019/05/06 10:24
S95	66534	(G06F3/061 or G06F3/064 or G06F3/0679 or G06F12/0246	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	OFF	2019/05/06 10:24

		or G06F2212/7201).cpc.	JPO; DERWENT; IBM_TDB			
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S93	8	"201351140"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S92	168	S91 and (usage near5 status) and (logical same physical)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
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S88	2179	(PHISON near3 ELECTRONICS near3 CORP).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S87	245	(Yeh near3 Chih-Kang).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
S86	114	(("YEH") near3 ("Chih-Kang")).INV.	USPAT	OR	OFF	2019/05/06 10:24
S85	66534	(G06F3/061 or G06F3/064 or G06F3/0679 or G06F12/0246 or G06F2212/7201).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24
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S83	8	"201351140"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/05/06 10:24

EAST Search History (Interference)

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