UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

PHISON ELECTRONICS CORPORATION,

Petitioner

v.

VERVAIN, LLC,

Patent Owner

Inter Partes Review Case No. IPR2025-00215

Patent 10,950,300

PETITIONER'S OPPOSITION TO PATENT OWNER'S SUPPLEMENTAL BRIEF

LIST OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 10,950,300, titled "LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM," to Rao
1002	Declaration of Carl Sechen, Ph.D.
1003	U.S. Provisional Application No. 61/509,257, titled "IMPROVED LIFETIME MIXED LEVEL NAND FLASH SYSTEM" by Rao
1004	U.S. Patent No. 7,855,916, titled "NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES," to Rao
1005	U.S. Patent No. 8,891,298, titled "LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM," to Rao
1006	Excerpts from prosecution history of '298 patent
1007	U.S. Patent No. 9,196,385, titled "LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM," to Rao
1008	Excerpts from prosecution history of '385 patent
1009	U.S. Patent No. 9,997,240, titled "LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM," to Rao
1010	Excerpts from prosecution history of '240 patent
1011	*Intentionally omitted*
1012	Excerpts from prosecution history of '300 patent
1013-1024	*Intentionally omitted*
1025	Excerpts from Rino Micheloni, et al., INSIDE NAND FLASH MEMORIES (Springer 2010)

1026	Excerpts from NONVOLATILE MEMORY TECHNOLOGIES WITH EMPHASIS ON FLASH: A COMPREHENSIVE GUIDE TO UNDERSTANDING AND USING NVM DEVICES (Joe E. Brewer & Manzur Gill eds. Wiley-IEEE Press 2008)
1027	Excerpts from MICROSOFT COMPUTER DICTIONARY (5th ed. 2002)
1028-1029	*Intentionally omitted*
1030	Yu Cai et al., *Program Interference in MLC NAND Flash Memory: Characterization, Modeling and Mitigation* (IEEE 2013)
1031	Kang-Deog Suh et al., *A 3.3 V 32 Mb NAND Flash Memory with Incremental Step Pulse Programming Scheme*, 30 IEEE J. Solid State Circuits 1149 (Nov. 1995)
1032	Eitan Yaakobi et al., *Error Characterization and Coding Schemes for Flash Memories* (2010 IEEE Globecom Workshops, Miami, FL at 1856-60)
1033	Evans, Chris, "Enterprise MLC: How flash vendors are boosting MLC write endurance" (June 3, 2011)
1034	Nelson Duann, SLC & MLC Hybrid (Silicon Motion Flash Memory Summit, Santa Clara, CA, Aug. 12, 2008)
1035	Ashish Jagmohan et. al., *Adaptive Endurance Coding for NAND Flash* (2010 IEEE Globecom Workshops, Miami, FL at 1841-45)
1036	Sungjin Lee et al., *FlexFS: A Flexible Flash File System for MLC NAND Flash Memory* (2009 USENIX Annual Technical Conference, San Diego, CA, June 14-19, 2009)
1037	Minyoung Sung & Kanghee Kim, *Asymmetric Flash Volume Management*, 58 *IEEE Transactions on Consumer Electronics* 455 (May 2012)
1038	Greg Atwood et al., *Intel StrataFlash*™ Memory Technology Overview at 4, Intel Technology J. (Q4 1997)

1039	Taehee Cho et al., "A 3.3 V 1 Gb multi-level NAND flash memory with non-uniform threshold voltage distribution," *2001 IEEE International Solid-State Circuits Conference. Digest of Technical Papers,* ISSCC (Cat. No. 01CH37177) (2001)
1040	U.S. Patent No. 6,456,528, titled for "SELECTIVE OPERATION OF A MULTI-STATE NON-VOLATILE MEMORY SYSTEM IN A BINARY MODE" to Chen
1041	U.S. Patent No. 8,078,794, titled "HYBRID SSD USING A COMBINATION OF SLC AND MLC FLASH MEMORY ARRAYS," to Lee et al.
1042	U.S. Patent Appl. Pub. No. 2008/0140918, titled "HYBRID NON-VOLATILE SOLD STATE MEMORY SYSTEM" by Sutardja
1043	U.S. Patent Appl. Pub. No. 2009/0327591, titled "SLC-MLC COMBINATION FLASH STORAGE DEVICE," by Moshayedi
1044	U.S. Patent Appl. Pub. No. 2010/0172179, titled "SPARE BLOCK MANAGEMENT OF NON-VOLATILE MEMORIES," by Gorobets et al.
1045	U.S. Patent No. 8,634,240, titled "NON-VOLATILE MEMORY AND METHOD WITH ACCELERATED POST-WRITE READ TO MANAGE ERRORS," to Gavens et al.
1046	U.S. Patent No. 8,806,301, titled "DATA WRITING METHOD FOR A FLASH MEMORY, AND CONTROLLER AND STORAGE SYSTEM USING THE SAME," to Yu et al.
1047	U.S. Patent Appl. Pub. No. 2010/0115192, titled "WEAR LEVELING METHOD FOR NON-VOLATILE MEMORY DEVICE HAVNG SINGLE AND MULTI LEVEL MEMORY CELL BLOCKS," by Lee
1048	U.S. Patent Appl. Pub. No. 2011/0271043, titled "SYSTEM AND METHOD FOR ALLOCATING AND USING SPARE BLOCKS IN A FLASH MEMORY," to Segal et al.

1049	U.S. Patent Appl. Pub. No. 2011/0153912, titled "MAINTAINING UPDATES OF MULTI-LEVEL NON-VOLATILE MEMORY IN BINARY NON-VOLATILE MEMORY," by Gorobets et al.
1050	U.S. Patent No. 5,930,167, titled "MULTI-STATE NON-VOLATILE FLASH MEMORY CAPABLE OF BEING ITS OWN TWO STATE WRITE CACHE," to Lee et al.
1051	U.S. Patent Appl. Pub. No. 2010/0172180, titled "NON-VOLATILE MEMORY AND METHOD WITH WRITE CACHE PARTITIONING," by Paley et al.
1052-1055	*Intentionally omitted*
1056	U.S. Patent App. Pub. No. 2009/0172267, "REFRESH METHOD OF A FLASH MEMORY," by Oribe et al.
1057	U.S. Patent No. 5,936,971, titled "MULTI-STATE FLASH EEPROM SYSTEM WITH CACHE MEMORY, to Harari et al.
1058	PCT Pub. No. WO 03/027828, "METHOD OF WRITING DATA TO NON-VOLATILE MEMORY," by Gorobets et al.
1059-1060	*Intentionally omitted*
1061	Duane H. Oto et al., *High-Voltage Regulation and Process Considerations for High-Density 5 V-Only E^2PROM's*, SC-18 IEEE J. Solid State Circuits 532 (Oct. 1983)
1062	Gheorghe Samachisa et al., *A 128K Flash EEPROM Using Double-Polysilicon Technology*, SC-22 IEEE J. Solid State Circuits 676 (Oct. 1987)
1063	Masaki Momodomi et al., *An Experimental 4-Mbit CMOS EEPROM with a NAND-Structured Cell*, 24 IEEE J. Solid State Circuits 1238 (Oct. 1989)
1064	Tae-Sun Chung et al., *A survey of Flash Translation Layer*, 55 J. Systems Architecture 332-43 (2009)

1065	Yoshiba Iwata et al., *A High-Density NAND EEPROM with Block-Page Programming for Microcomputer Applications*, 25 IEEE J. Solid-State Circuits 417 (Apr. 1990)
1066	Simona Boboila and Peter Desmoyers, *Write Endurance in Flash Drives: Measurements and Analysis*, Usenix Conference (Feb. 2010)
1067	SiliconSystems, *Increasing Flash SSD Reliability*, StorageSearch.com (April 2005)
1068	Taehee Cho et al., *A Dual-Mode NAND Flash Memory: 1-Gb Multilevel and High-Performance 512-Mb Single Level Modes*, 36 IEEE J. Solid State Circuits 1700 (Nov. 2001)
1069	Ken Takeuchi, *A Multipage Cell Architecture for High-Speed Programming Multilevel NAND Flash Memories*, 33 IEEE J. Solid-State Circuits 1228 (Aug. 1998)
1070	Garth Goodson & Rahul Iyer, *Design Tradeoffs in a Flash Translation Layer*, HPCA [High Performance Computer Architecture] WEST 2010 Conference, Bangalore, India
1071-1079	*Intentionally omitted*
1080	Docket list for *Vervain, LLC v. Phison Electronics Corp.*, No. 1:24-cv-00259 (W.D. Tex., filed March 8, 2024)
1081	Docket list for *Vervain, LLC v. Kingston Technology Company, Inc*., No. 1:24-cv-00254 (W.D. Tex. filed March 7, 2024)
1082	First Amended Complaint, Doc. No. 9 in *Vervain, LLC v. Phison Electronics Corp.*, No. 1:24-cv-00259 (W.D. Tex.)
1083	Signed Agreed Scheduling Order, Doc. No. 16 in *Vervain, LLC v. Phison Electronics Corp.*, No. 1:24-cv-00259 (W.D. Tex.)
1084	"Interim Processes for PTAB Workload Management," issued March 26, 2025

1085	Active Cases Before Judge Alan D. Albright as of June 2, 2025
1086	Statistics on Median Time-to-Trial between June 2, 2024 and June 2, 2025
1087	"Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation," issued March 24, 2025
1088	Western District of Texas Calendar Year 2024 Statistical Public Report
1089	Amended Order Assigning the Business of The Court (January 31, 2025)
1090	Consolidated Trial Practice Guide (Nov. 2019)
1091	Docket Entry No. 61, Redacted Copy of 59 Unopposed Sealed Motion FOR LEAVE TO AMEND FINALINVALIDITY CONTENTIONS by Phison Electronics Corporation by Phison Electronics Corporation, filed on April 2, 2025 in *Vervain, LLC v. Phison Electronics Corp.*, No. 1:24-cv-00259 (W.D. Tex., filed March 8, 2024)
1092	Email from PO's Counsel re: Reduction to No More Than Five Asserted Claims Per Patent and Sixteen Total Across the Eight Patents-in-Suit (June 9, 2025)
1093	Docket list for *Vervain, LLC v. Micron Technology Inc., et al.*, No. 6:21-cv-00487 (W.D. Tex. filed May 10, 2021)
1094	Docket list for *Vervain, LLC v. Western Digital Corp. et al.*, No. 6:21-cv-00488 (W.D. Tex. filed May 10, 2021)

Petitioner respectfully opposes Patent Owner's ("PO's") Supplemental Brief regarding "Settled Expectations" in *iRhythm Techs., Inc. v. Welch Allyn, Inc.*, IPR2025-00363, Paper 10 (P.T.A.B. June 6, 2025). In *iRhythm*, the petitioner *itself* affirmatively cited the relevant pending application in an Information Disclosure Statement and did not seek early review. Here, the Examiner, not the Petitioner, cited U.S. Patent 8,891,298 ("the '298 patent") among ten other U.S. patent documents during the prosecution of U.S. Patent 10,824,340 ("the '340 patent). The Examiner merely considered the '298 patent and the other patent documents as being *pertinent*, but did not apply any of them to the '340 patent's then pending claims. Discretionary denial based upon Patent Owner's arguments would impose undue burden upon *all* applicants, whenever a reference is considered *pertinent* during the prosecution of *all* applications. It would also encourage stakeholders to file premature, unnecessary challenges against any *pertinent* patents/applications, simply to preserve standing. As such, no Petitioner should be required to proactively seek the Board's review under such circumstances. Petitioner diligently and timely filed this *inter partes* review after Patent Owner served its infringement contentions, consistent with the Board's precedent. Ex. 1083. See, e.g., *Fintiv* at 11 (Noting reasonableness of waiting to file petition until after "[petitioner] learns which claims are being asserted against it in the parallel proceeding."). Thus, there are no "settled expectations" that would warrant denial of institution.

Date: June 17, 2025

Respectfully submitted,
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CERTIFICATION OF SERVICE (37 C.F.R. § 42.6(e))

The undersigned hereby certifies pursuant to 37 C.F.R. §§ 42.6(e) that the above-captioned Petitioner's Opposition to Patent Owner's Supplemental Brief, was served in its entirety on June 17, 2025, via electronic mail upon the following counsel of record for Patent Owner:

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