

Agenda Item : 13.1
Source : Nortel Networks
Title : Fractional dedicated physical channel, discussion on multiplexing options
Document for : Discussion

1. Introduction

During RAN1#32, R1-030546 was presented which introduced the fractional dedicated physical channel concept. This concept allows to reduce the code consumption of HSDPA data-only users allowing to time multiplex several users on the same code channel.

In this contribution, we present further details and implementation options of the proposed scheme with a particular focus on inner loop power control.

This contribution also contains a text proposal for TR25.899.

2. Principles and summary of the proposal

The current specifications mandate the set up of dedicated physical channels both in the UL and in the DL for any user operating in HSDPA. However with the development of data-only applications especially for low to medium bit rates, the cost of the dedicated channel may restrict a wider use of HSDPA. With the current specifications, the associated dedicated channel of these HSDPA data-only users will carry pilots and TPC bits (control part) and possibly the associated RRC signalling which will be DTX'ed for most of the connection.

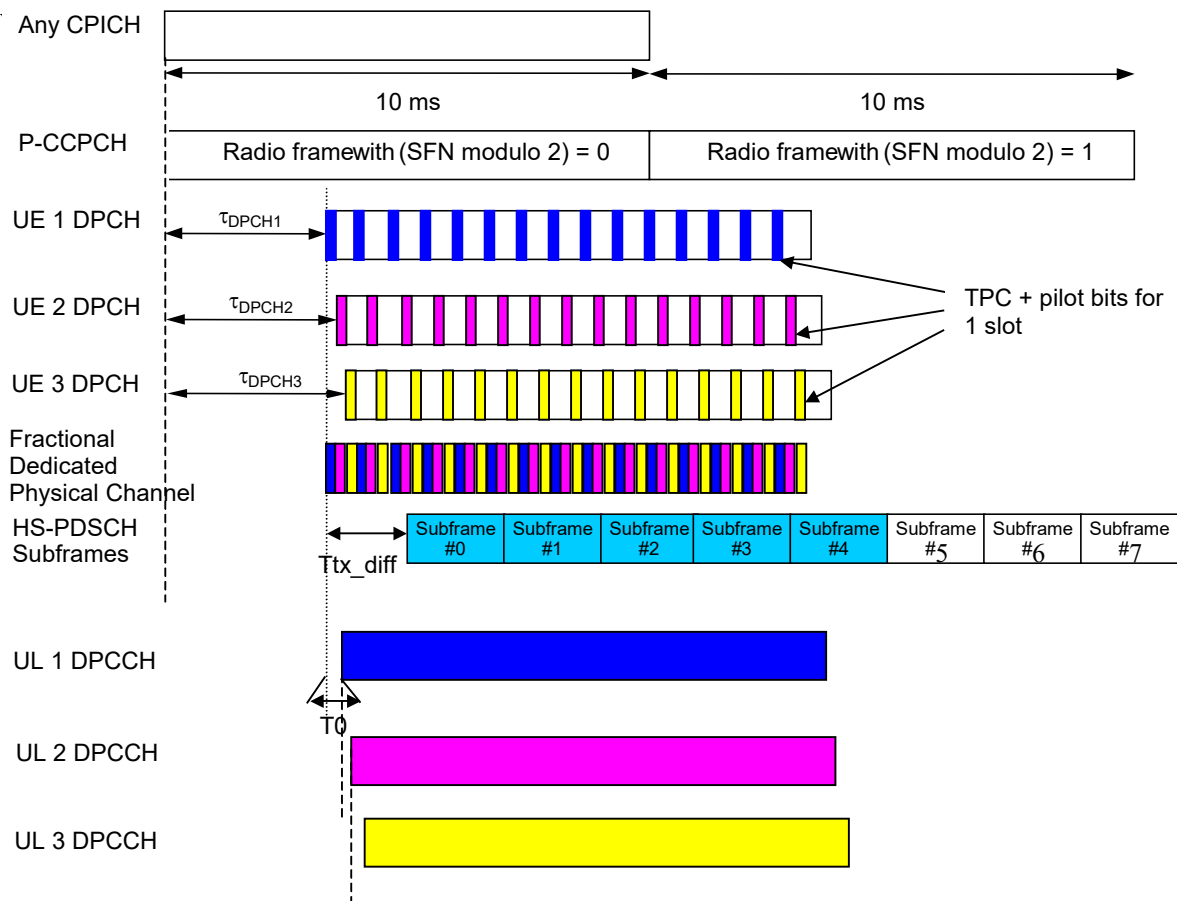
The objective of this proposal is to share given codes among HSDPA users to allow more users to share the same resource with the following requirements

- Keep the UL timing unchanged
- Maintain UL inner loop power control periods
- Maintain Layer 1 synchronisation
- Dedicated channel establishment can be performed directly with fractional dedicated channel in the downlink and dedicated channel in the uplink
- Compatibility with soft handover, compressed mode, open-loop Tx diversity
- Keep downlink power control active to avoid transmitting at the maximum power.

In order to fulfil these requirements :

- *UE specific TPC bits* are needed to keep the UL power control loop for each UE
- *Pilot bits* are needed to allow the Fractional dedicated physical channel to be power controlled and allow DL synchronisation to be maintained by each UE.

The fractional dedicated channel can thus be seen as a shared power control channel i.e. one code is shared between different users to carry power control and pilot bits. The principle is illustrated on the figure below.



On the above figure, DPCH1 DPCH2 and DPCH3 illustrate the dedicated channels which are set up for 3 different UEs operating in HSDPA with no conversational service and DCCH signalling mapped onto HS-DSCH. When the DL timings of these channels are properly chosen, it appears that the code dimension is not necessary to distinguish between the UEs.

Therefore a single code is sufficient to carry TPC and pilot bits associated to these HSDPA Ues. and still maintain the same periodicity of one slot for the transmission of these information in the downlink.

Note that the number 3 was chosen for illustrative purposes. The exact number of UEs mapped on such a channel will depend on the chosen structure (see following sections).

3. Fractional dedicated physical channel (F-DPCH) multiplexing options and impact on power control loops

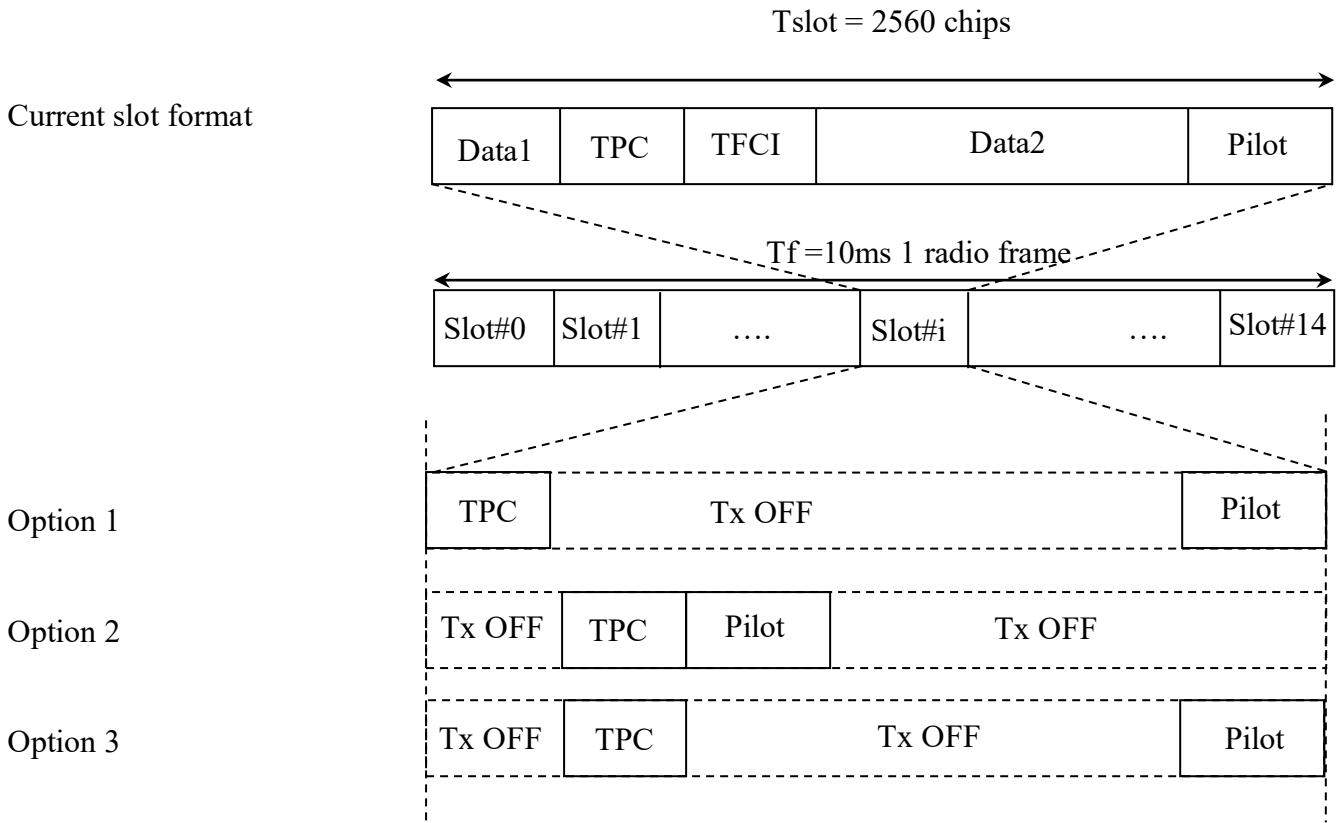
In the previous meeting, a possible structure was presented where for each UE the F-DPCH carries pilot and TPC bits which are grouped together at the beginning of the slot. For simplification reasons no particular attention had been paid to the timing structure. In the following, several alternatives are presented and their respective impact on inner and outer loop power control are discussed.

Option 1 : pilot position is unchanged, TPC bits are advanced in time

Option 2 : TPC position is unchanged, pilots are advanced in time

Option 3 : same as current

The corresponding slot structures are presented below



In the following, we consider that the relative timing between F-DPCH and UL DPCH for a given UE is the same as the current relative timing between DPCH and UL DPCH. This is made possible by keeping the frame and slot structure as currently seen from the UE.

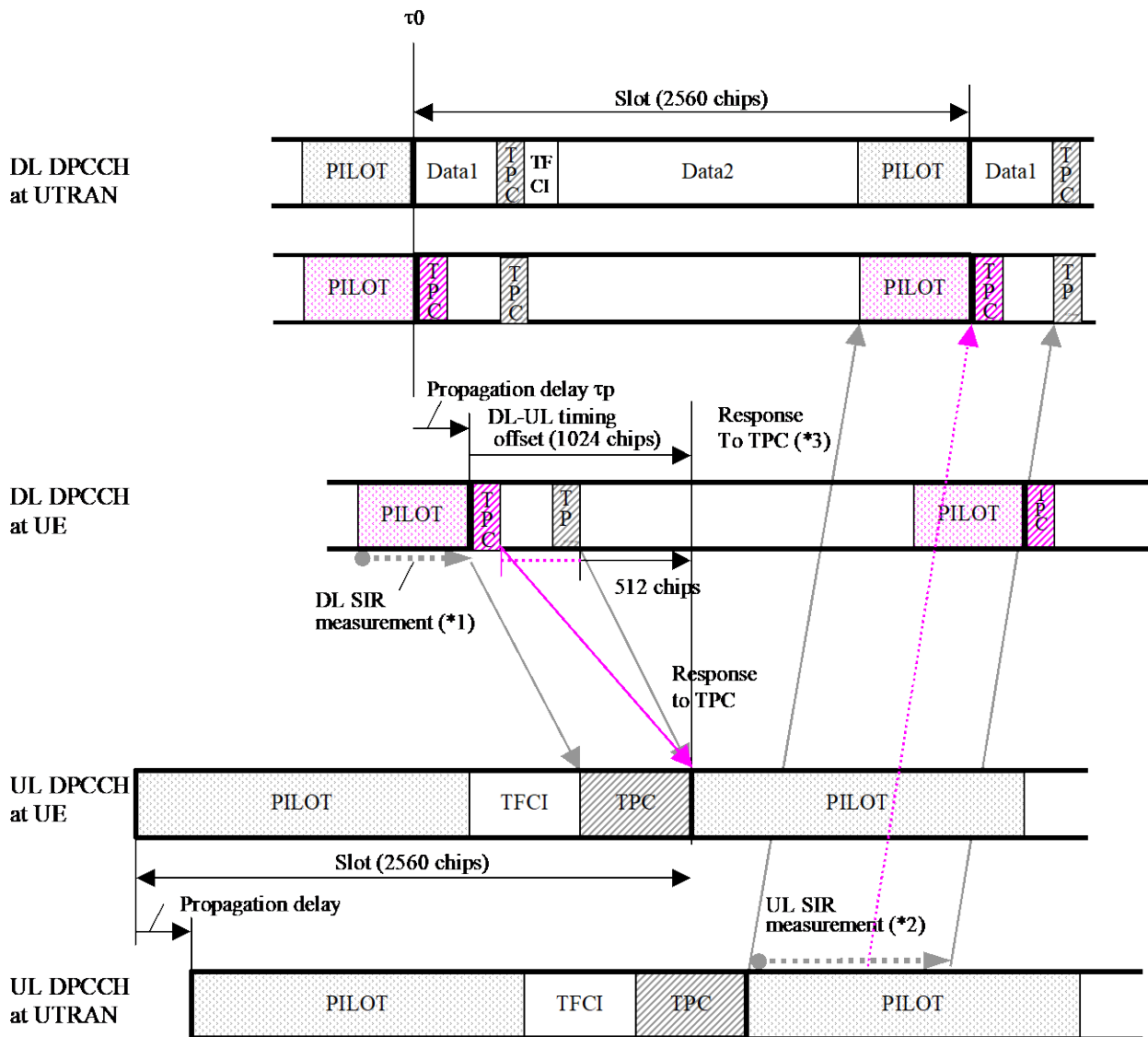
3.1. Option 1 : pilot position is unchanged, TPC bits are advanced in time

In this configuration, DL power control is not impacted as both UE processing timing (from reception of DL pilots to UL TPC command setting) and UTRAN processing time (from reception of UL TPC command to DL power change) is not affected by this change.

However as the position of DL TPC bits is modified both UE and UTRAN processing time for UL power control will be affected.

- UE processing time (from reception of DL TPC command to UL power change) : this time increases from 512 chips to $512 + \text{size of Data1 field chips}$
- UTRAN processing time is decreased by the same amount i.e. the size of Data1 field (768 chips = 0.2ms at SF = 128 or 64 and 896 chips = 0.23ms)

These changes are illustrated on the following figure (taken from annex B of 25.214)



UTRAN processing time depends on the SIR estimation accuracy one wants to obtain. The current slot format give UTRAN processing time of $T_{\text{slot}} + T_{\text{data1}} - T_0 - 2\tau_p$ which becomes $T_{\text{slot}} - T_0 - 2\tau_p$

This means that the cell radius for which a one slot delay can be achieved is further reduced compared to the current situation.

3.2. Option 2 : TPC position is unchanged, pilot bits are advanced in time

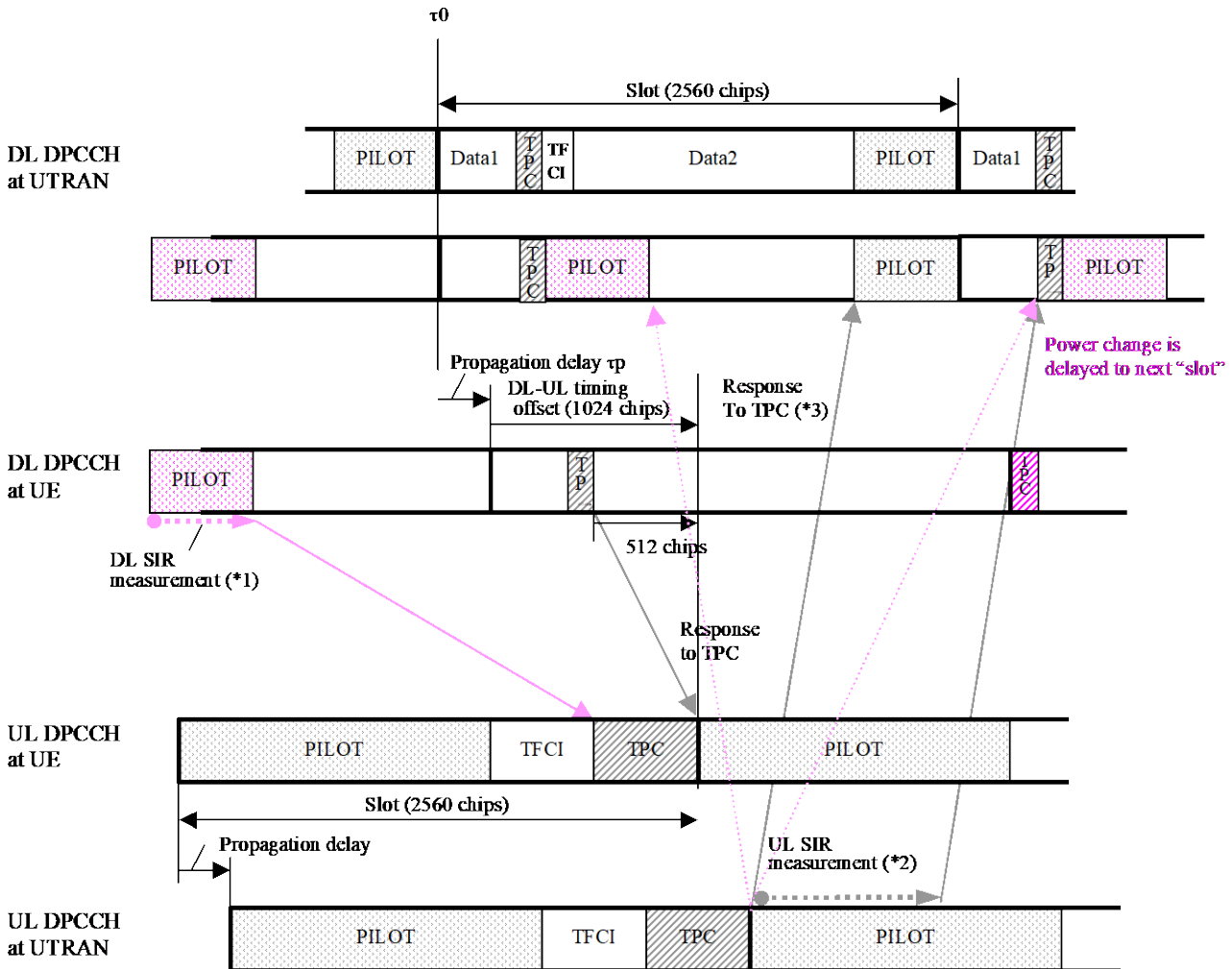
In this configuration, UL power control is not impacted as both UE processing time (from reception of DL TPC to UL pilot change) and UTRAN processing time (from reception of UL pilot to DL TPC command setting) is not affected by this change.

However as the position of pilot bits is modified both UE and UTRAN processing time for DL power control will be affected.

- UE processing time (from reception of DL pilots to UL TPC command setting) : increased by size of TFCI + data2. The UE has enough processing time but information is less accurate.

- UTRAN processing time (from reception of UL TPC command to DL power change) : decreased by size of TFCI + data2. This means that the power change will be delayed to the next slot.

These changes are illustrated on the following figure



The impact on UTRAN processing is a delay in the power change, compared to the current implementation (assuming we are in a case where a one slot delay can be achieved), the power change will only be delayed by the size of pilot + data1 field (see above figure) i.e. 200/266μs depending on the size of the pilot field.

The objective is that the F-DPCH is power control by the Ues such that each group of TPC + pilots bits intended for one UE is transmitted at the relevant power for this UE. With option 2 this is possible however more investigation is needed on the expected cell sizes for which a one delay as in R99 is achievable.

3.3. Option 3 : Same slot structure as the current one is kept

The main advantage with this approach is that UL and DL power control loop are not affected at all. However since there is a fixed time offset between pilot and TPC field intended for a given UE, this option will considerably limit the number of UE which can be multiplexed in the same time slot duration.

At SF = 128 there are 28 bits between TPC and pilot bits, this limits the number of Ues which can be multiplexed in a one time slot duration to 2.
 With option 3 it seems the gain in terms of OVSF codes consumption is lost i.e. 2 Ues on 1 SF = 128 F-DPCH code is equivalent to 2 Ues on SF = 256 dedicated codes (carrying only DCCH signalling).

4. Conclusion

In this contribution, several multiplexing options are presented and discussed to analyse the impact of F-DPCH on UL and DL power control loops. It is proposed that these options are listed in TR25.899 as possible choices for F-DPCH structure.

The following text is proposed for inclusion in TR25.899

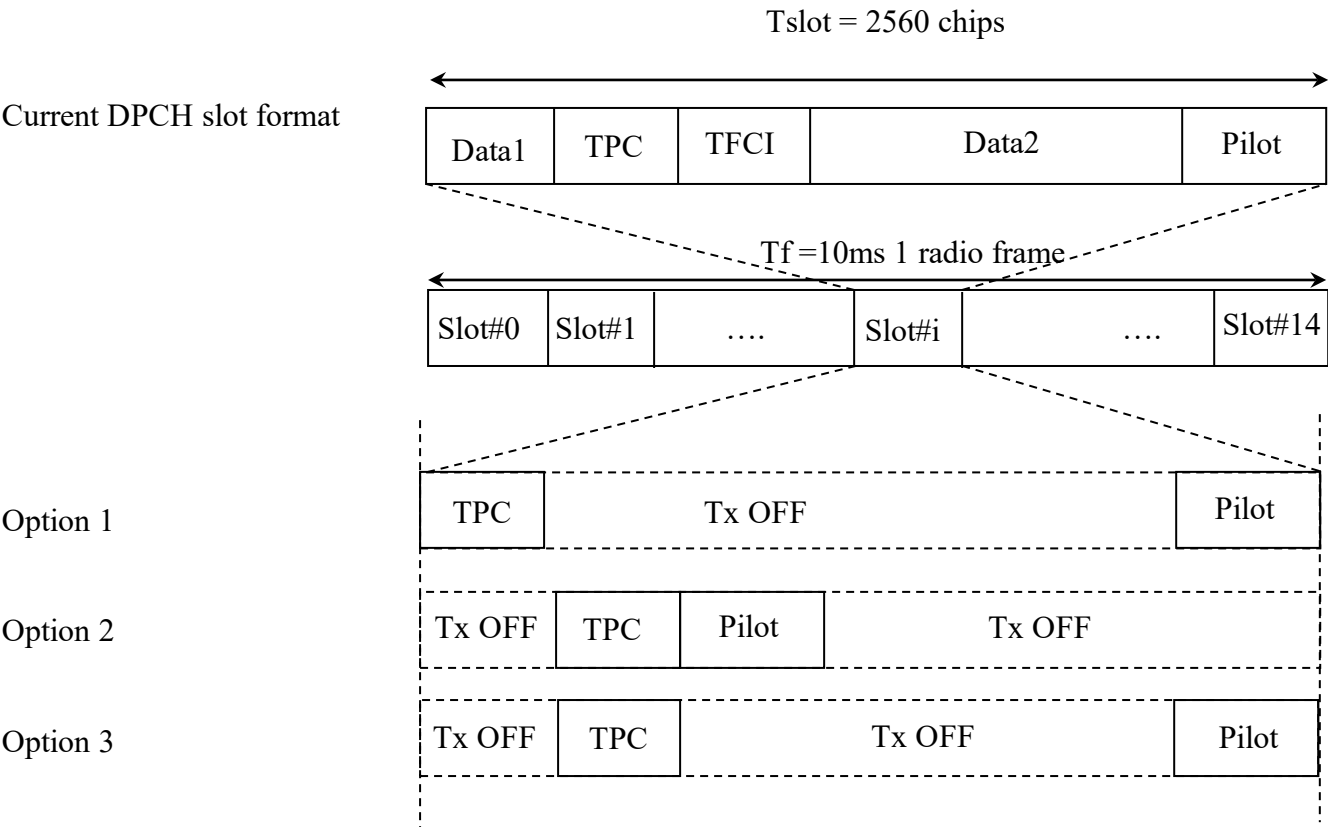
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6.x.2 F-DPCH structure

F-DPCH follows the same frame structure as existing physical channels, a 10 ms frame divided into 15 slots.

- In the following several slot structures are discussed :
- Option 1 : pilot position is unchanged, TPC bits are advanced in time
 - Option 2 : TPC position is unchanged, pilots are advanced in time
 - Option 3 : same as current

These options are illustrated below



In the following, we consider that the relative timing between F-DPCH and UL DPCH for a given UE is the same as the current relative timing between DPCH and UL DPCH. This is made possible by keeping the frame and slot structure as currently seen from the UE.

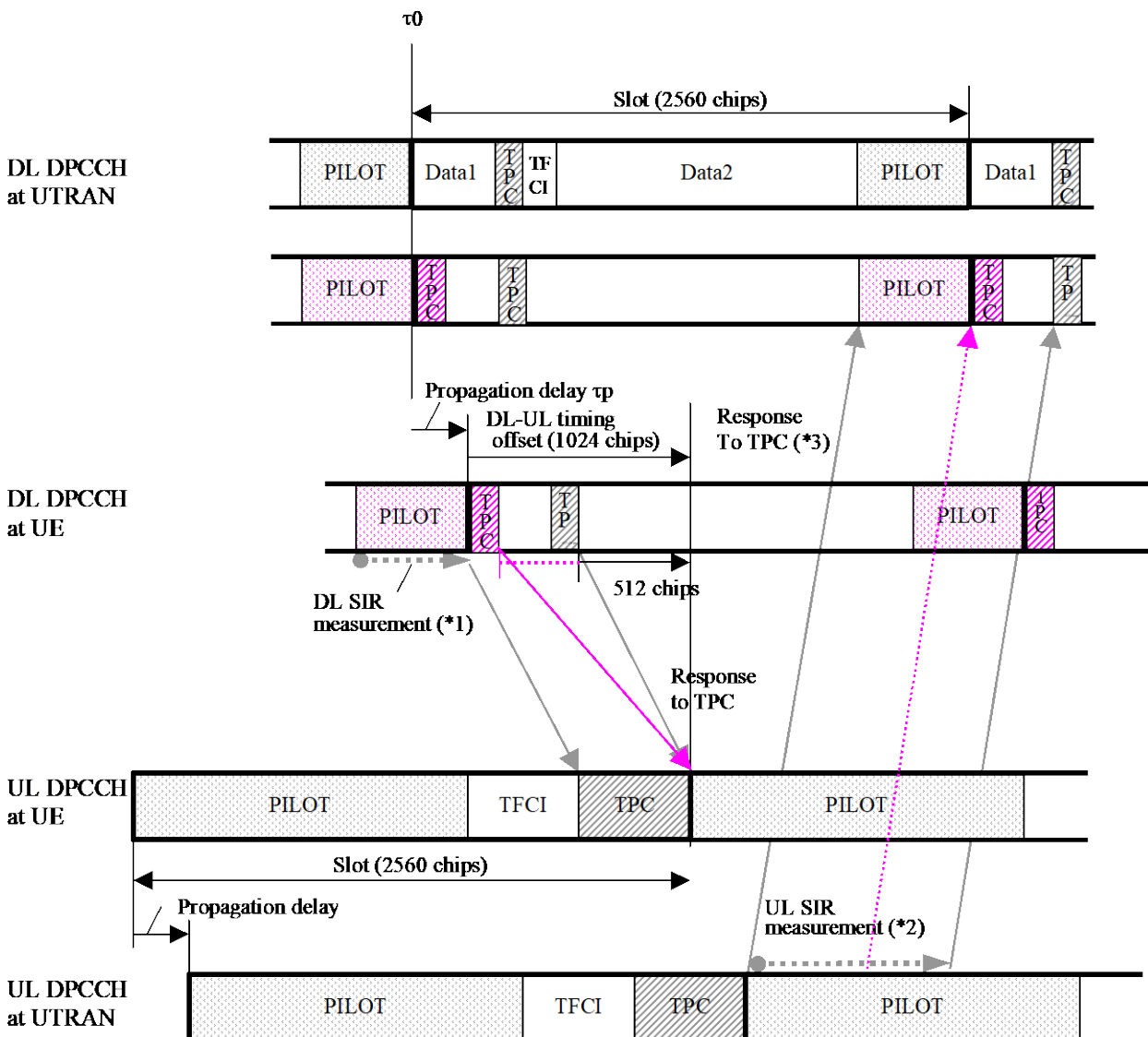
6.x.2.1 Option 1 : pilot position is unchanged, TPC bits are advanced in time

In this configuration, DL power control is not impacted as both UE processing timing (from reception of DL pilots to UL TPC command setting) and UTRAN processing time (from reception of UL TPC command to DL power change) is not affected by this change.

However as the position of DL TPC bits is modified both UE and UTRAN processing time for UL power control will be affected.

- UE processing time (from reception of DL TPC command to UL power change) : this time increases from 512 chips to 512 + size of Data1 field chips
- UTRAN processing time is decreased by the same amount i.e. the size of Data1 field (768 chips = 0.2ms at SF = 128 or 64 and 896 chips = 0.23ms)

These changes are illustrated on the following figure (taken from annex B of 25.214)



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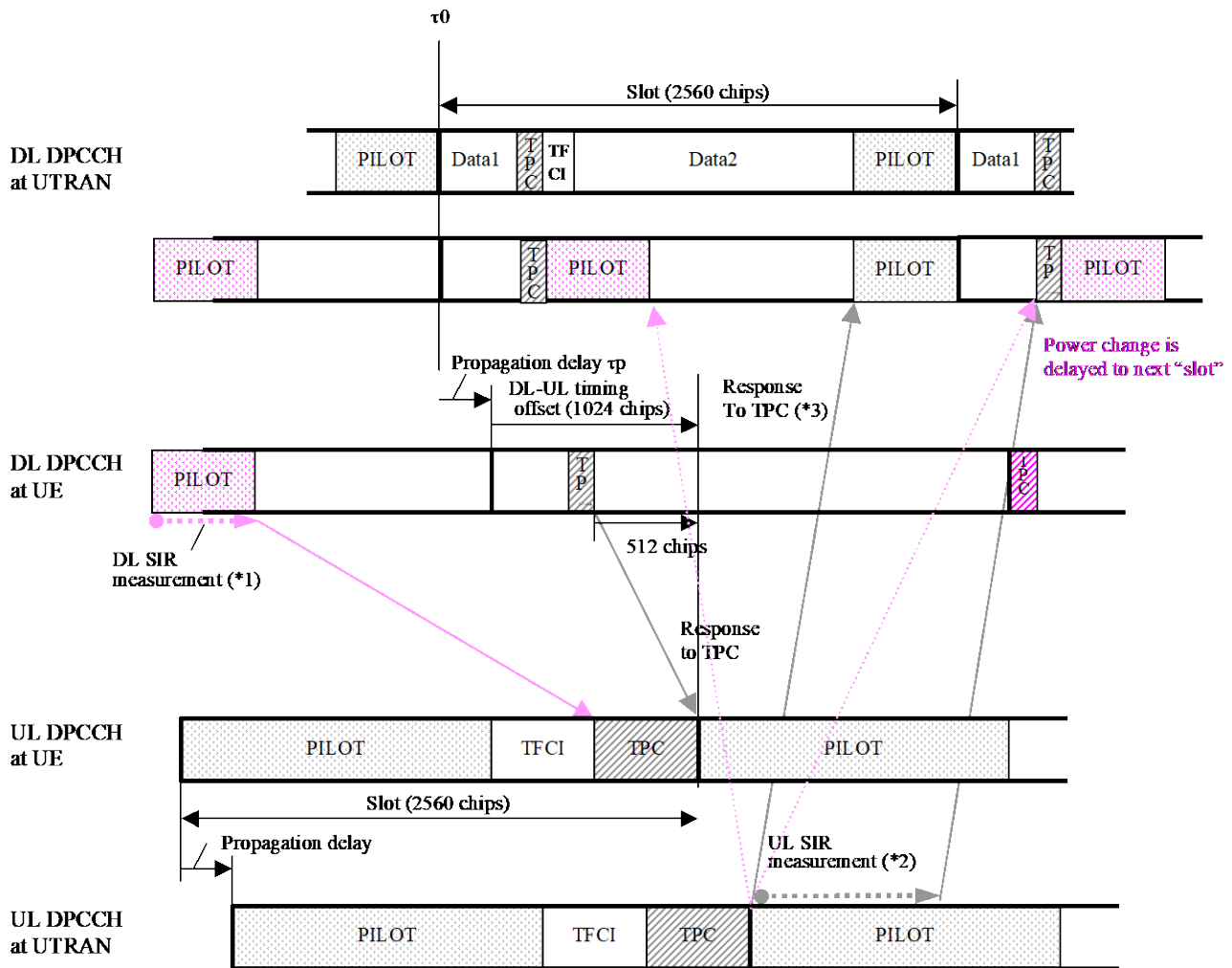
6.x.2.2 Option 2 : TPC position is unchanged, pilot bits are advanced in time

In this configuration, UL power control is not impacted as both UE processing time (from reception of DL TPC to UL pilot change) and UTRAN processing time (from reception of UL pilot to DL TPC command setting) is not affected by this change.

However as the position of pilot bits is modified both UE and UTRAN processing time for DL power control will be affected.

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The objective is that the F-DPCH is power control by the Ues such that each group of TPC + pilots bits intended for one UE is transmitted at the relevant power for this UE. With option 2 this is possible however more investigation is needed on the expected cell sizes for which a one delay as in R99 is achievable.

6.x.3 Option 3 : Same slot structure as DPCH

The main advantage with this approach is that UL and DL power control loop are not affected at all. However since there is a fixed time offset between pilot and TPC field intended for a given UE, this option will considerably limit the number of UEs which can be multiplexed in the same time slot duration.

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-----End of text proposal-----