



Kodak Digital Science KAC-0311 Image Sensor

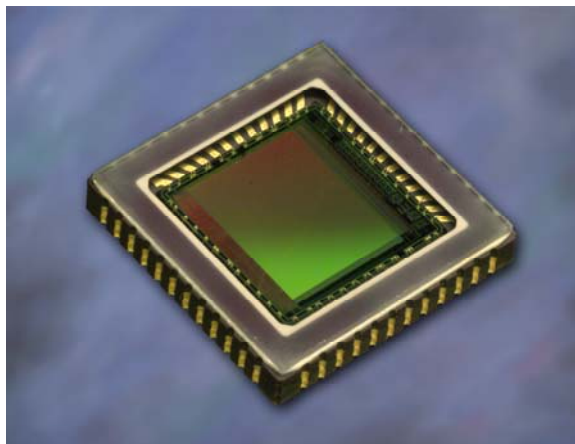
KAC – 0311

640 x 480 VGA CMOS Image Sensor

Fully Integrated Timing, Analog Signal Processing & 10 bit ADC

Features

- 1/3" Color VGA Digital Image Sensor
- 640 x 480 pixel progressive/interlace scan
- 7.8 μ m square pixels with patented pinned photodiode architecture
- Bayer - CMY CFA, Monochrome
- High sensitivity, quantum efficiency, and charge conversion efficiency
- Low fixed pattern noise / Wide dynamic range
- Patented Electronic Shutter Operation
- 30fps full VGA at 10MHz Master Clock Rate
- 60fps full VGA at 20MHz Master Clock Rate
- Antiblooming and continuous variable speed shutter
- 10x linear programmable gain
- 10-bit, pipelined algorithmic RSD ADC
- User selectable digital output formats:
 - 8-bit companded data
 - 10-bit linear data
- Pixel addressability to support 'Window of Interest' windowing, resolution, and sub-sampling
- Analog column offset correction
- Integrated on-chip timing/logic circuitry
- Digitally programmable via I²C interface
- CDS sample and hold for suppression of low frequency and correlated reset noise
- Dark reference pixels with automatic Frame Rate Clamp
- Single master clock operation
- Single 3.3V power supply
- 48 pin CLCC package



Key Specifications

- **Pixel Size:** 7.8 μ m x 7.8 μ m
- **Fill factor:** 40%
- **Image Size:** 5.0mm x 3.7mm (1/3")
- **Responsivity:** 90,000 electrons/Lux-sec
- **Saturation Signal:** 45,000 electrons
- **Min Light:** 5 Lux at 30FPS/F2 lens
- **Scan Modes:** Progressive/Interlace
- **Operation Modes:** Continuous & Single
- **Shutter Modes:** Rolling or Global
- **Nominal Readout Rate:** 14 MHz
- **Maximum Readout Rate:** 20 MSPS
- **Frame Rate:** 0-60 frames per second
- **System Dynamic Range:** 49 dB
- **Programmable gain:** -3.0dB to 17.4dB
- **ADC:** 10-bit, RSD ADC (DNL +/-0.5 LSB, INL +/-1.0 LSB)
- **Power Dissipation:** 215mW (dynamic) / 25mW (standby)

Release Date: 8/5/2002

Eastman Kodak Company - Image Sensor Solutions

For the most current information regarding this product:

Web: www.kodak.com/go/imagers Phone: (585) 722-4385 Email: imagers@kodak.com

Revision No. 1
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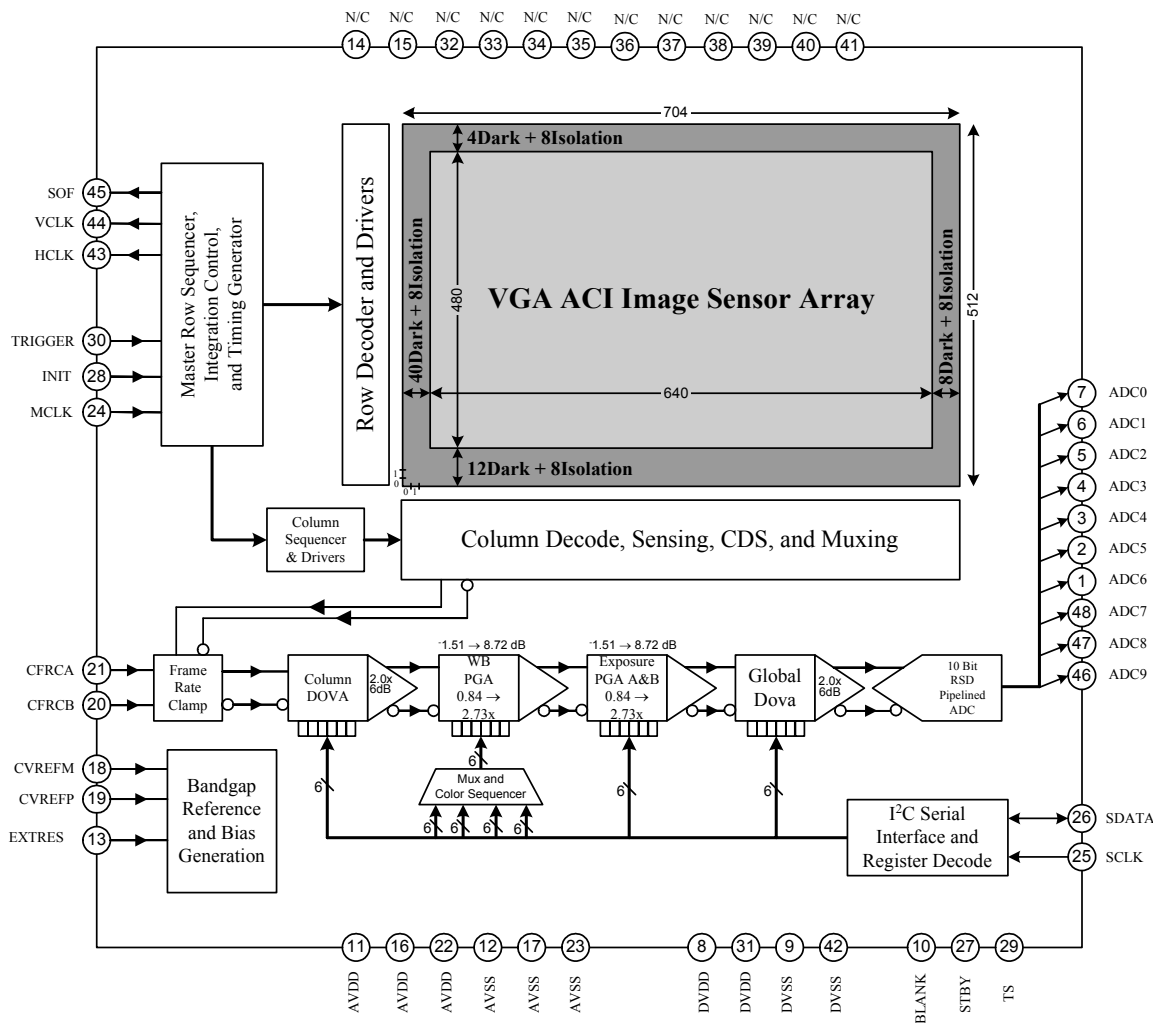


Figure 1: KAC-0311 Block Diagram

The KAC-0311 is a fully integrated, high performance 1/3" optical format VGA CMOS image sensor including integrated timing control and programmable analog signal processing. This sensor provides system designers a complete imaging solution with a monolithic image capture and processing engine. System benefits enable design of smaller, portable, low cost and low power systems. Each pixel on the sensor is individually addressable allowing the user to control the "Window of Interest" (WOI), panning and zooming, sub-sampling, resolution, exposure, white balance, and other image processing features via a two pin I²C compatible interface. This device runs from a single 3.3V supply and single master clock.

The imager uses Kodak's patented Pinned Photodiode CMOS active pixels. The 7.8µm pixel design provides true correlated double sampling for low read noise operation, high quantum efficiency, low dark current, and no image lag. Kodak's patented pixel design combined with low noise mixed signal circuits provides a high sensitivity, low noise integrated "camera on a chip".



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Pin No.	Pin Name	Description	Pin Type	Power	Value	Pin No.	Pin Name	Description	Pin Type	Power	Value
1	ADC6	Output Bit 6=64d	O	D		25	SCLK	I ² C Serial Clock Line	I	D	
2	ADC5	Output Bit 5=32d	O	D		26	SDATA	I ² C Serial Data Line	I/O	D	
3	ADC4	Output Bit 4=16d	O	D		27	STBY	Power Down Standby Enable	I	D	
4	ADC3	Output Bit 3=8d	O	D		28	INIT	Sensor Initialize	I	D	
5	ADC2	Output Bit 2=4d	O	D		29	TS	Dig Output Tri-State Enable	I	D	
6	ADC1	Output Bit 1=2d	O	D		30	TRIGGER	Still Frame Capture Trigger	I	D	
7	ADC0	Output Bit 0=1d	O	D		31	DVDD	Digital Power	P	D	3.3 V
8	DVDD	Digital Power	P	D	3.3 V	32	NC	Unused	I	D	
9	DVSS	Digital Ground	G	D	0 V	33	NC	Unused	I	D	
10	BLANK	Pixel Invalid	O	D		34	NC	Unused	I	D	
11	AVDD	Analog Power	P	A	3.3 V	35	NC	Unused	I	D	
12	AVSS	Analog Ground	G	A	0 V	36	NC	Unused	I	D	
13	EXTRES	External Bias Resistor	I	A	27k Ω	37	NC	Unused	I	D	
14	NC	Unused		A		38	NC	Unused	I	D	
15	NC	Unused		A		39	NC	Unused	I	D	
16	AVDD	Analog Power	P	A	3.3 V	40	NC	Unused	I	D	
17	AVSS	Analog Ground	G	A	0 V	41	NC	Unused	I	D	
18	CVREFM	ADC Bottom Bias Ref Capacitor	O	A	0.1 μ F	42	DVSS	Digital Ground	G	D	0 V
19	CVREFP	ADC Top Bias Ref Capacitor	O	A	0.1 μ F	43	HCLK	Pixel Sync	O	D	
20	CFRCB	Frame Rate Clamp Capacitor	O	A	1.0 μ F	44	VCLK	Line Sync	O	D	
21	CFRCA	Frame Rate Clamp Capacitor	O	A	1.0 μ F	45	SOF	Start of Frame Sync	O	D	
22	AVDD	Analog Power	P	A	3.3 V	46	ADC9	Output Bit 9=512d	O	D	
23	AVSS	Analog Ground	G	A	0 V	47	ADC8	Output Bit 8=256d	O	D	
24	MCLK	Master Clock = Pixel Rate	I	D		48	ADC7	Output Bit 7=128d	O	D	

KAC-0311 Pin Definitions

Legend:
P = VDD
G = VSS
I = Input
O = Output
D = Digital
A = Analog

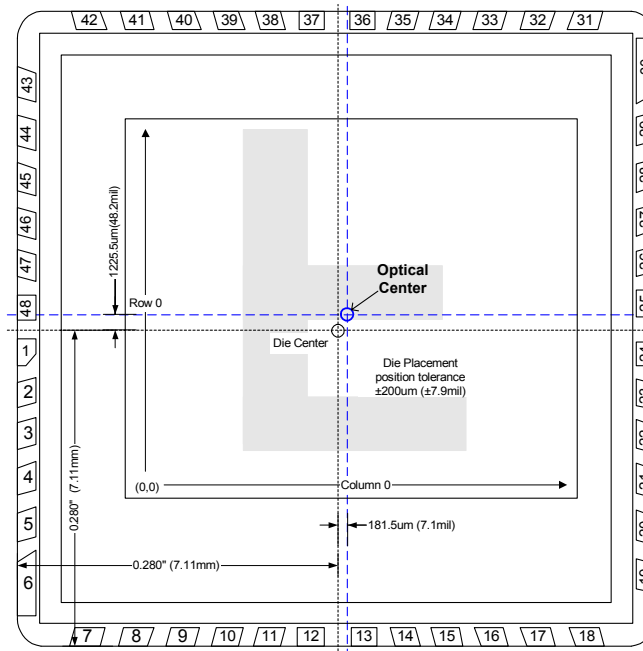


Figure 2 Pinout Diagram

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**Kodak Digital Science KAC-0311 Image Sensor**

1 Overview

The KAC-0311 is a solid state CMOS Active CMOS Imager (ACI™) that integrates the functionality of complete analog image acquisition, digitizer, and digital signal processing system on a single chip. The image sensor comprises a VGA format pixel array with 640x480 active elements. The image size is fully programmable to user defined windows of interest. The pixels are on a 7.8μm pitch. High sensitivity and low noise are a characteristic of the pinned photodiode² architecture utilized in the pixels. The sensor is available in a Monochrome version without microlenses, or with Bayer (CMY) patterned Color Filter Arrays (CFAs) without microlenses.

Integrated timing and programming controls allow video or still image capture progressive scan modes. Frame rates are programmable while keeping the Master Clock frequency constant. User programmable row and column start/stop allow windowing down to a 1x1 pixel window for digital zoom of a panable viewport. Subsampling provides reduced resolution while maintaining constant field of view.

The analog video output of the pixel array is processed by an on-chip analog signal pipeline. Correlated Double Sampling (CDS) eliminates the pixel reset temporal and pattern noise. The Frame Rate Clamp (FRC) enables real time optical black level calibration and offset correction. The programmable analog gain consists of exposure/global gain to map the signal swing to the ADC input range, and white balance gain to perform color balance in the analog domain. The ASP signal chain consists of (1) Column op-amp; (2) Column DOVA; (3) White Balance PGA (0.84 → 2.73); (4) Global PGA (0.84 → 2.73); and (5) Global DOVA. These Digitally Programmable Amplifiers (DPGAs) allow real time color gain correction for Auto White Balance (AWB) as well as exposure gain adjustment. Offset calibration can be done on a per column basis and globally. This per-column offset correction can be applied by using stored values in the on chip registers. A 10-bit Redundant Signed Digit (RSD) ADC converts the analog data to a 10-bit digital word stream. The fully differential analog signal processing pipeline serves to improve noise immunity, signal to noise ratio, and system dynamic range. The sensor uses an industry standard two line I²C compatible serial interface. It operates with a single 3.3V power supply with no additional biases and requires only a single Master Clock for operation up to 20 MHz. It is housed in a 48 pin ceramic LCC package.

The KAC-0311 is designed taking into consideration interfacing requirements to standard video encoders. In addition to the 10 bit Bayer (CMY) encoded data stream, the sensor outputs the valid frame, line, and pixel sync signals needed for encoding. The sensor interfaces with a variety of commercially available video image processors to allow encoding into various standard video formats. In addition, the 3 sync signals can be integrated into the video data stream eliminating the need of the 3 sync outputs

The KAC-0311 is an elegant and extremely flexible single chip solution that simplifies a system designer's tasks of image sensing, processing, digital conversion, and digital signal processing to a high performance, low cost, low power IC. It supports a wide range of low power, portable, consumer digital imaging applications.

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2 Sensor Interface

2.1 Pixel Architecture

The KAC-0311 ImageMOS TM¹ sensor comprises a 640x480 active pixel array and supports both progressive and interlaced scan readout modes. The basic operation of the pixel relies on the photoelectric effect where, due to its physical properties, silicon is able to detect photons of light. The photons generate electron-hole pairs in direct proportion to the intensity and wavelength of the incident illumination. The application of an appropriate bias allows the user to collect the electrons and meter the charge in the form of a useful parameter such as voltage.

The pixel architecture is based on a four transistor (4T) Advanced CMOS Imager TM² pixel which requires all pixels in a row to have common Reset, Transfer, and Row Select controls. In addition all pixels have common supply (V_{DD}) and ground (V_{SS}) connections. An optimized cell architecture provides enhancements such as noise reduction, fill factor maximization, and anti-blooming. The use of pinned photodiodes³ and proprietary transfer gate devices in the photoelements enables enhanced sensitivity in the entire visual spectral range and a low lag operation. The nominal photoresponse of the KAC-0311 is shown in Figure 3.

In addition to the imaging pixels, there are additional pixels called dark and dummy pixels at the periphery of the imaging section (see Figure 1). The dark pixels are covered by a light blocking shield rendering the pixels underneath insensitive to photons. These pixels provide the sensor means to measure the dark level offset which is used downstream in the signal processing chain to perform auto black level calibration. The dummy pixels are provided at the array's periphery to eliminate inexact measurements due to light piping into the dark pixels adjacent to active pixels and for extra pixels needed for some color interpolation algorithms.

Electronic shuttering, also known as electronic exposure timing in photographic terms, is a standard feature. The pixel integration time can be widely varied from a small fraction of a given frame readout time to the entire frame time. This feature can be especially useful in situations such as imaging of fast moving objects where normal integration times cause smear, blurring, or image tear.

¹ ImageMOS is a Motorola trademark

² Advanced CMOS Imager is a Kodak trademark

³ Patents held jointly by Kodak and Motorola



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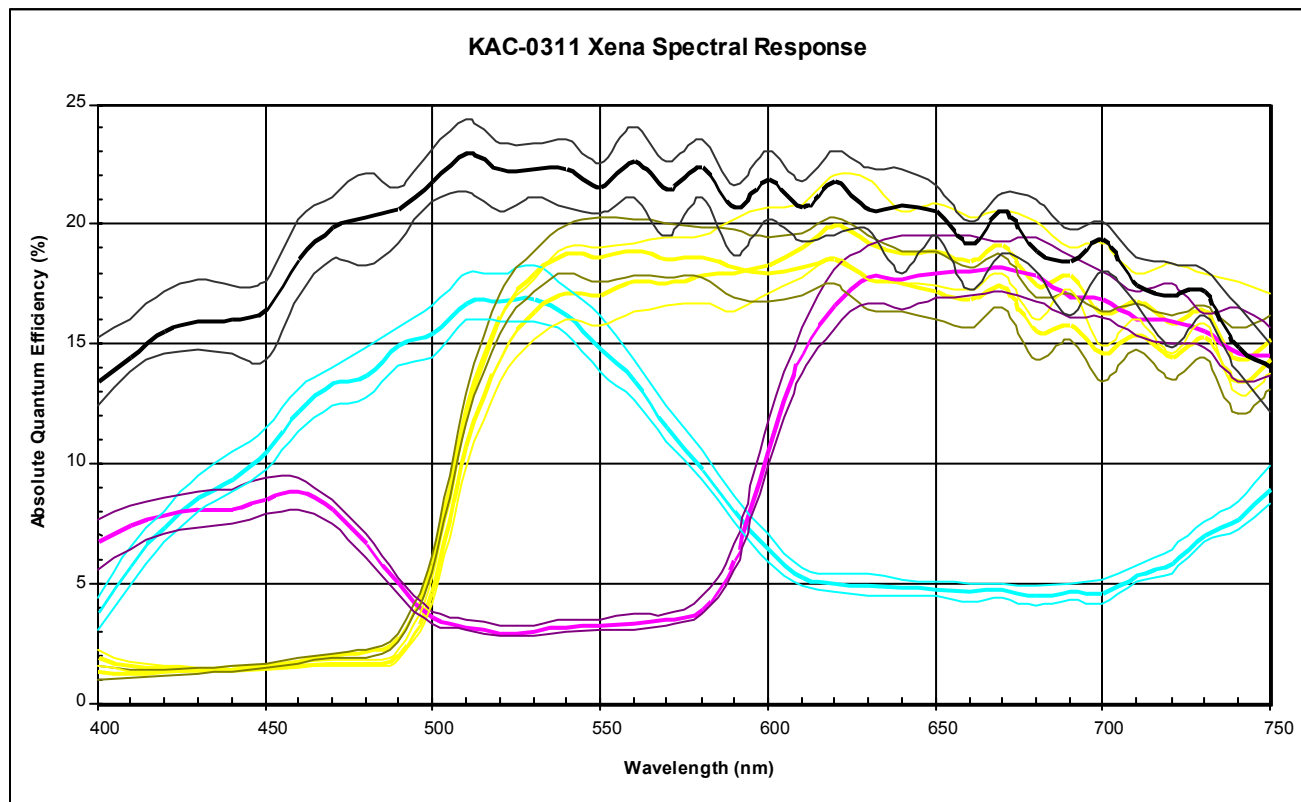


Figure 3: KAC-0311 Spectral Response

2.2 Color Filters

The KAC-0311 family is offered with the option of monolithic polymer color filter arrays (CFAs). The combination of an extremely planarized process and proprietary color filter technology results in CFAs with superior spectral and transmission properties. The standard option (Part # KAC-0311C-x-A) is a complimentary (CMY) “Bayer” pattern (see Figure 4). The complimentary Bayer CMY array provides a 50% increase in sensitivity over primary RGB pattern and are often the best choice for low light applications. This is due to the higher quantum efficiency (QE) and larger wavelength spread per color. If the application is utilizing a color correction matrix, then this matrix will automatically convert the CMY to RGB. Other wise a simple matrix must be applied to affect the conversion from CMY to RGB space.

Y1	M	Y1	M
C	Y2	C	Y2
Y1	M	Y1	M
C	Y2	C	Y2

Figure 4: Optional Bayer CMY Pattern CFA

**Kodak Digital Science KAC-0311 Image Sensor****2.3 Frame Capture Modes**

There are three frame capture modes:

- 1) Continuous Frame Rolling Shutter (CFRS)
- 2) Single Frame Rolling Shutter (SFRS)
- 3) Single Frame Global Shutter (SFGS)

The sensor can be put into any of these modes by setting the Capture Mode Control Register (40_h) (Table 19 on page 35).

2.3.1 Continuous Frame Rolling Shutter Capture Mode (CFRS)

The default mode of image capture is the Continuous Frame Rolling Shutter Capture Mode (CFRS). In this mode the TRIGGER input pin is ignored. This mode is most suitable for full motion video capture and will yield VGA sized Frame Rates up to 60 FPS at 20 MHz MCLK. In this mode the image integration and row readout take place in parallel. While a row of pixels is being readout, another row or rows are being integrated. Since the integration time (T_{int}) must be equal for all rows, the start of integration for rows is staggered.

2.3.2 Single Frame Rolling Shutter capture mode (SFRS)

In this mode of capture, the start of integration is triggered by the TRIGGER signal. Similar to the CFRS capture mode, readout of each row follows the integration of that row. The imager can be placed in SFRS capture mode using register 40_h (see Table 19 on page 35). In this mode the imager will remain idle until the TRIGGER pin is pulled high. The imager then begins integration followed by image readout. If the TRIGGER input is still high when the SFRS Frame is finished reading out, then a second Frame is started. Detailed timing can be found in Figure 15.

As in any SLR camera system, long integration times can cause blur for fast moving objects. And short integration times cause image tear where the moving object's horizontal image is distorted at the bottom of the image relative to the top of the image. Rapidly varying illumination (ex. Flickering lights) can also cause distortion of the image. For these cases special consideration must be applied to the capture sequence or SFGS can be used.

2.3.3 Single Frame Global Shutter capture mode (SFGS)

This mode consists of global integration of all pixels, next a simultaneous transfer to the Floating Diffusion (FD) node of all pixels followed by a sequential read out of all rows. This mode is best suited for still or "single snap shot" capture of an image where a flash illumination is utilized. SFGS should only be used when the ambient lighting will not cause the pixels to saturate during the readout time. In this mode the imager will remain idle until the TRIGGER pin is pulled high. The imager then begins integration followed by image readout. If the TRIGGER input is still high when the SFRS Frame is finished reading out, then a second Frame is started. Detailed timing can be found in Figure 19

2.3.4 Image Scan Modes

The KAC-0311 has two available image scanning modes: interlaced and progressive.

Interlacing is a technique used in TV systems that is used to enhance the vertical resolution of the picture without increasing the bandwidth of the transmission system. A spatial offset is introduced on the display system between the odd and even fields. An odd field consists of rows 1,3,5,7,9.... while an even field comprises rows 2,4,6,8.... Since the spatial offset is exactly half the vertical pitch of the sensor, the even and odd fields appear interdigitated when displayed on top of one another, thus appearing to improve the sensor's vertical resolution. By definition two interlaced fields comprise a frame. It should be noted that at high frame rates, motion between fields in interlaced video can cause smear and/or serration to appear in the image.

Progressive scanning refers to non-interlaced or sequential row by row scanning of the entire sensor in a single pass. The image capture happens at one instant of time. This mode is primarily used in applications where vertical resolution is of prime importance and available bandwidth of the transmission system does not impose any limitations.

The scan mode is controlled via the Sub-Sample Control Register, (Table 20), on page 36.



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2.3.5 Window of Interest Control

The pixel data to be read out of the device is defined as a 'Window of Interest' (WOI). The window of interest can be defined anywhere on the pixel array at any size. The user provides the upper-left pixel location and the size in both rows and columns to define the WOI. The WOI is defined using the WOI Pointer, WOI Depth, and WOI Width registers, (Table 21 on page 37 through Table 28 on page 39). Refer to Figure 5 for a pictorial representation of the WOI within the active pixel array.

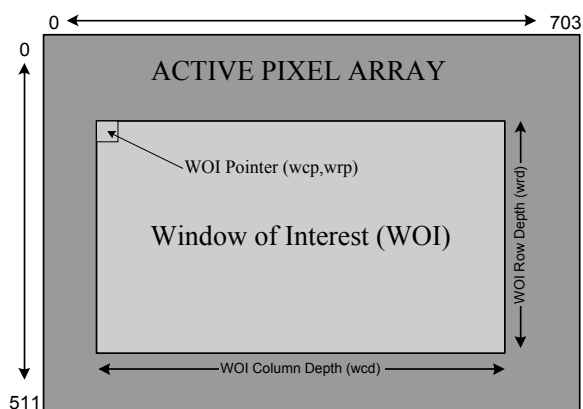


Figure 5: WOI Definition

2.3.6 Sub-Sampling Control(Resolution)

The WOI can be sub-sampled in either monochrome or Bayer pixel space in four different sampling rates in each direction: full, $\frac{1}{2}$, $\frac{1}{4}$, or $\frac{1}{8}$. Sub-sampling the imager by $\frac{1}{8}$ in both horizontal and vertical directions results in only $\frac{1}{16}$ of the pixel being readout. The frame readout rate is therefore increased by 16x. The user controls the sub-sampling via the Sub-sample Control Register, (Table 20 on page 36). An example of Bayer space sub-sampling is shown in Figure 6. Note that this imager is available in CMY color filters. If the imager is set as a color imager then the sub-sampling is done by reading out two cols/rows and then skipping two. This prevents the sub-sampling from breaking up a color kernel. If the imager is set to Monochrome mode the sub-sampling will skip every other col/row performing a more uniform reduction in resolution. Activating Sub-Sampling alone will not

increase the Frame Rate. The Frame Rate is controlled by the Virtual Frame (see Section 2.4). For example, if Sub-Sampling is first turned on to $\frac{1}{8} \times \frac{1}{8}$ mode, the WOI will shrink by $\frac{1}{64}$. To keep the Frame Rate constant, the KAC-0311 fills in the rest of the rows and columns with blanking pixels. The Virtual Frame can now be reduced by $\frac{1}{8} \times \frac{1}{8}$ to take advantage of the Sub-Sampled WOI. The Frame Rate will now have increased by 64x with no compromise to the field of view (in CFRS mode).

G	R	G	R	G	R	G	R	G	R	G	R
B	G	B	G	B	G	B	G	B	G	B	G
G	R	G	R	G	R	G	R	G	R	G	R
B	G	B	G	B	G	B	G	B	G	B	G
G	R	G	R	G	R	G	R	G	R	G	R
B	G	B	G	B	G	B	G	B	G	B	G
G	R	G	R	G	R	G	R	G	R	G	R
B	G	B	G	B	G	B	G	B	G	B	G
G	R	G	R	G	R	G	R	G	R	G	R
B	G	B	G	B	G	B	G	B	G	B	G
G	R	G	R	G	R	G	R	G	R	G	R
B	G	B	G	B	G	B	G	B	G	B	G

Figure 6: Bayer $\frac{1}{2} \times \frac{1}{2}$ Sub-sample Example.

Sub-sample Control Register (41_h) = x01x0101_b

2.4 Virtual Frame (VF)

Changing the WOI does not change the Frame Rate of the imager. This is done by varying the size of a Virtual Frame surrounding the WOI. Refer to Figure 7 for a pictorial description of the Virtual Frame and its relationship to the WOI.

The VF is a method for defining the horizontal and vertical blanking (over clocking) in Frame Readout. As the WOI is adjusted, the total Frame Size is set by the VF. To maintain constant Frame Rate, the KAC-0311 adjusts the number of blanking pixels to account for changes in the WOI. The VF can be set to any size. If the VF is greater than the WOI then the readout is padded with blanking pixels (invalid dark pixels). The WOI and the VF may both be larger than the actual imager size. In this case the



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WOI is also padded with blanking pixels (invalid dark pixels). Figure 7 illustrates a WOI smaller than the VF. If the WOI is set larger than the VF, then the WOI will be clipped by the VF and the Frame Rate will still be equal to the VF size.

The first pixel of the VF is always equal to the first pixel of the WOI. Thus the WOI is always in the upper left corner of the VF.

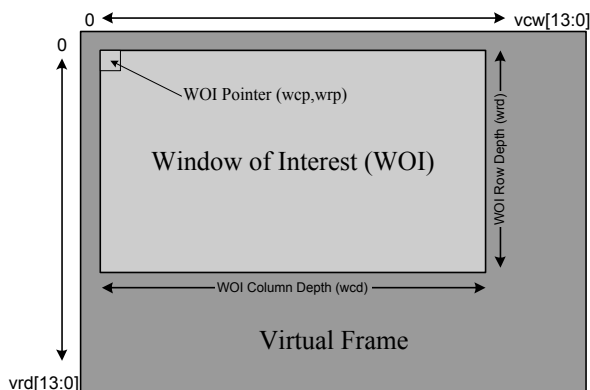


Figure 7: Virtual Frame Definition

2.5 Integration Time

Note: All calculations in this section assume Reg 60_h = 00_h

2.5.1 CFRS Integration Time

The Integration Time in CFRS is defined and quantized by the time to read out a single row. Once a Virtual Frame has been defined, the time to read out one row can be calculated. Any integer multiple of the Row Time (T_{row}) can be selected. The number of Row Times desired for integration time is programmed into the Integration Time Registers. The Integration Time is defined by a combination of the width of the VF and the Integration Time Registers (4E_h and 4F_h), (Table 29 and Table 30 on page 40); and can be expressed as:

For $vcw_d > 704$ (or FRC off):

$$\text{Integration Time } (T_{int}) = (cint_d + 1) * T_{row}$$

For $vcw_d < 704$:

$$\text{Integration Time } (T_{int}) = (cint_d - 1) * T_{row} + FRC_{time}$$

where $cint_d$ is the number of virtual frame row times desired for integration time. Therefore, the integration time can be adjusted in steps of VF row times.

$$\text{Row Time } (T_{row}) = (vcw_d + 51) * MCLK_{period}$$

If the integration time is programmed to be larger than the VF then it will be truncated to the number of rows in the VF. The VF must be increased before the Integration Time can be increased further.

2.5.2 SFRS Integration Time

Just as with operation in CFRS mode, the integration time is defined by a number of Row Times. As before:

$$\text{Row Time } (T_{row}) = (vcw_d + 51) * MCLK_{period}$$

$$\text{Integration Time } (T_{int}) = (cint_d + 1) * T_{row}$$

Note: In CFRS operation, the integration time is limited (clipped) by the readout time (which is also the Frame Time). In SFRS mode, the Frame Time is expanded to include any programmed integration time. Thus in SFRS operation there is no boundary to the integration time.

2.5.3 SFGS Integration Time Control

The Integration Time for the SFGS is defined by the integration time register (Table 29 to 31 on page 40) and can be expressed as:

$$\text{Integration Time } (T_{int}) = sint_d * 16 * MCLK_{period}$$

where $sint_d$ is a number. Therefore, the user can adjust integration time in steps of 16 MCLK periods.

2.6 Frame Rate

The Frame Rate can be defined as the time required to readout an entire frame of data plus the required blanking time. There is a different relationship between the Frame Rate and Virtual Frame for CFRS and SFRS mode operation.



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2.6.1 CFRS Frame Rate

In CFRS, the Frame Rate of the imager is controlled by varying the size of the Virtual Frame surrounding the WOI, and is independent of Integration Time. Refer to Figure 7 for a pictorial description of the Virtual Frame (VF) and its relationship to the WOI. In CFRS operation, the Frame Rate (FR) (Frame Rate = 1/Frame Time) is defined by the VF size and clock speed (MCLK). The Frame Time (FT) and can be expressed as:

$$\begin{aligned} FT &= \#rows * \#columns * MCLK_{period} \\ &= \#rows * T_{row} \end{aligned}$$

For $vcw_d > 704$:

$$FT = (vrd_d + 1) * T_{row}$$

For $vcw_d < 704$:

$$FT = (vrd_d - 1) * T_{row} + FRC_{time}$$

VF Row Time (T_{row}) is the length of time required to read one row of the virtual frame and can be defined as:

$$T_{row} = (vcw_d + 51) * MCLK_{period}$$

$$FRC_{time} = (770) * MCLK_{period}$$

vrd_d defines the number of rows in the virtual frame. The user controls vrd_d via the Virtual Frame Row Depth registers (Table 32 and Table 33 on page 41).

vcw_d defines the number of columns in the virtual frame. The user controls vcw_d via the Virtual Frame Column Width registers (Table 34 and Table 35 on page 42).

If the VF width (vcw_d) is < 704 , then the timing block holds the two Frame Rate Clamp (FRC) rows to a length of 704 even while all of the other rows are shorter. This is to ensure enough time for the clamping circuit. If the FRC is turned off, then the equation for FT when $vcw_d > 704$ can be used no matter what the value of vcw_d . In this case, it is recommended that the CFRCA and CFRCB pins be tied to ground (i.e. no 1 μ F capacitor). The above equations can be combined as follows:

For $vcw_d > 704$ (or FRC off):

$$FT = (vrd_d + 1) * (vcw_d + 51) * MCLK_{period}$$

For $vcw_d < 704$:

$$FT = [((vrd_d - 1) * (vcw_d + 51)) + 770] * MCLK_{period}$$

NOTE: The WOI and Integration Time will be clipped by the VF.

2.6.2 SFRS Frame Rate

There are two main differences when running in SFRS mode versus CFRS mode. The first is that the Frame Rate is no longer the readout rate. In SFRS mode there is no overlap of the Integration and the readout. Therefore, at the top of each frame, integration must first occur then readout. The Frame Rate is now Integration Time plus readout.

The second major difference is the length of readout. In CFRS mode, the only reason for making the VF length larger than the WOI length ($vrd > wrd$) is to add vertical blanking rows to control the time between frames. In SFRS mode, the time between frames is controlled by the TRIGGER input pin, and therefore vertical blanking serves no purpose. Rather than have the user change the VF depth (vrd), the imager uses the WOI depth (wrd).

Therefore, the Frame Rate equations are:

For $vcw_d > 704$,

$$FT = [(vrd_d + 1) * (vcw_d + 51) * MCLK_{period}] + T_{int}$$

For $vcw_d < 704$:

$$FT = \{ [((vrd_d - 1) * (vcw_d + 51)) + 770] * MCLK_{period} \} + T_{int}$$

$$\text{Readout Time } (T_{rd}) = T_{row} * (wrd_d + 1)$$

$$\begin{aligned} \text{Frame Time } (FT) &= T_{int} + T_{rd} \\ &= [(vrd_d) + (cint_d) + 2] * T_{row} \end{aligned}$$

$$\text{Frame Rate} = 1/\text{Frame Time}$$

2.6.3 SFGS Frame Rate

The Frame Rate equations for SFGS are similar to the SFRS. In the SFGS mode, all the pixels integrate simultaneously. It provides an electronic shutter, which uniformly captures motion without the risk of image tear, which can occur in the SFRS mode. Note that if the readout time is greater than Integration time, it is possible to corrupt the image in certain scenes.

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SFGS mode consists of global integration of all pixels, next a simultaneous transfer to the Floating Diffusion (FD) node of all pixels followed by a sequential read out of all rows. This mode is best suited for still or “single snap shot” capture of an image where a flash illumination is utilized. SFGS should only be used when the ambient lighting will not cause the pixels to saturate during the readout time.

For $vcw_d > 704$:

$$\mathbf{FT} = [(\mathbf{wrd}_d+1) * (\mathbf{vcw}_d+51) * \mathbf{MCLK}_{\text{period}}] + \mathbf{T}_{\text{int}}$$

For $vcw_d < 704$:

$$\mathbf{FT} = \{[(\mathbf{wrd}_d - 1) * (\mathbf{vcw}_d + 51)) + 770] * \mathbf{MCLK}_{\text{period}}\} + \mathbf{T}_{\text{int}}$$

$$\text{Readout Time (T}_{rd}) = T_{row} * (wrd_d + 1)$$

$$\text{Frame Time (FT)} = T_{\text{int}} + T_{\text{rd}}$$

$$\mathbf{FT} = \mathbf{sint}_d * 16 * \mathbf{MCLK} \text{ period} + \mathbf{T}_{\text{row}} * (\mathbf{wrd}_d + 1)$$

Frame Rate = 1/Frame Time

3 Analog Signal Processing Chain Overview

The KAC-0311's analog signal processing (ASP) chain incorporates Correlated Double Sampling (CDS), Frame Rate Clamp (FRC), two Digitally Programmable Gain Amplifiers (DPGA), Offset Correction (DOVA), and a 10-bit Analog to Digital Converter (ADC).

3.1 Correlated Double Sampling (CDS)

The uncertainty associated with the reset action of a capacitive node results in a reset noise which is proportional to kTC ; 'C' being the capacitance of the node, 'T' the temperature, and 'k' the Boltzmann constant. A common way of eliminating this noise source in all image sensors is to use Correlated Double Sampling. The output signal is sampled twice, once for its reset (reference) level and once for the actual video signal. These values are sampled and held while a difference amplifier subtracts the reference level from the signal output. Double sampling of the signal eliminates correlated noise sources.

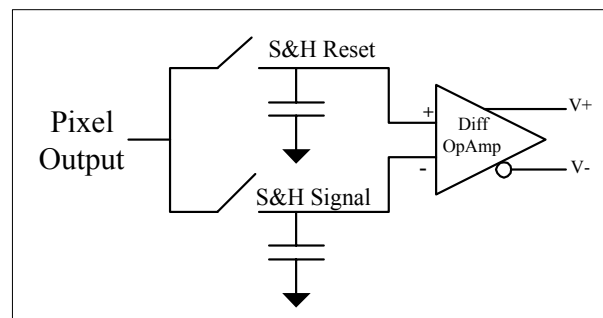


Figure 8: Conceptual block diagram of CDS

3.2 Frame Rate Clamp (FRC)

The FRC (Figure 9) is designed to provide a feed-forward dark level compensation. In the automatic FRC mode, the optical black level reference is reestablished each time that the image sensor begins a new frame. The KAC-0311 uses optical black (dark) pixels to establish this reference.

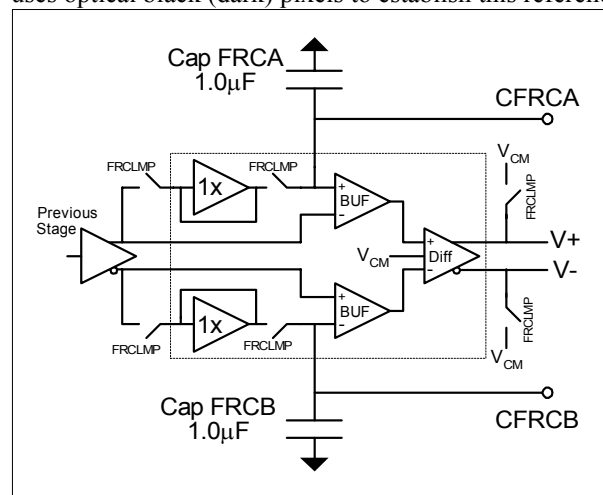


Figure 9: FRC Conceptual Block Diagram

The dark pixel sample period is automatically controlled internally and it is set to skip the first 3 dark rows and then sample the next 2 dark rows. When “dark clamping” is active, each dark pixel is processed and held to establish pixel reference level at the CFRCA and CFRCB pins. During this period, the FRC’s differential outputs (V^+ and V^- on the Diff Amp) shown in Figure 13 are clamped to V_{cm} . Together, these actions help to eliminate the dark level offset, simultaneously establishing the desired zero code at the ADC output. The user can disable the FRC via

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the Clamp Control which allows the ASP chain to drift in offset. If the FRC is disabled, it is recommended that the CFRCA and CFRCB pins be grounded. Care should be exercised in choosing the capacitors for the CFRCA and CFRCB pins to reflect different Frame Rates. For small WOI or fast Frame Rates, a smaller capacitor may be used.

3.2.1 Column Digital Offset Voltage Adjust (DOVA)

A programmable per-column offset adjustment is available on the KAC-0311. A user defined offset value can be loaded via a 4-bit signed magnitude register value. This programmable DOVA allows the user to select offset coefficients for FPN and pre-gain offset cancellation, and is used to correct for column induced errors. The user must generate and load data for this function. A dark frame can be analyzed to determine the appropriate values to be loaded into the 4-bit Per-Column DOVA RAM (Table 16 on page 32).

When the per-column feature is not used or necessary, the user loads a 6-bit value into the Column DOVA DC Register, (Table 14), on page 30 to perform a pre-gain offset cancellation prior to the gain stages of the ASP.

3.2.2 Digitally Programmable Gain Amplifiers (DPGA)

Two DPGAs are available in the analog signal processing chain. These are used to perform white balance and exposure gain functions. Both are linearly programmable via 6-bit registers.

3.2.3 White Balance Control PGA

[For the purposes of illustration, the following discussion assumes a Bayer RGB color pattern; with the appropriate correlation (as shown in Figure 9), the CMY Bayer pattern may be substituted throughout.]

The sensor produces three primary color outputs, Red, Green and Blue. These are monochrome signals that represent luminance values in each of the primary colors. When added in equal amounts they mix to make neutral color. White balancing is a technique where the gain coefficients of the green(0), red, blue, and green(3) pixels

comprising the Bayer pattern (see Figure 10) are set so as to equalize their outputs for neutral color scenes. Since the sensitivity of the two green pixels in the Bayer pattern may not be equal, an individual color gain register is provided for each component of the Bayer pattern.

Once all color gain registers are loaded with the desired gain coefficients, white balance is achieved in real time and in analog space. The appropriate values are selected and applied to the pixel output via a high speed path, the delay of which is much shorter than the pixel clock rate. Real time updates can be performed to any of the gain registers. However, latency associated with the I²C interface should be taken into consideration before changes occur. In most applications, users will be able to assign predefined settings such as daylight, fluorescent, tungsten, and halogen to cover a wide gamut of illumination conditions.

Both DPGA designs use switched capacitors to minimize accumulated offset and improve measurement accuracy and dynamic range. The white balance gain registers are 6-bits and can be programmed to allow gain of 0.84 to 2.73 in steps of 0.03x.

The user programs the individual gain coefficients into the KAC-0311 via the Color Gain Registers (Table 5 through Table 8). For the default Bayer configuration of the color filter array; Figure 4, the Color Gain Register addresses are as follows: Reg (00_h): green pixel green-red row; Reg (01_h): red pixel; Reg (02_h): blue pixel; and Reg (03_h): green pixel of a blue-green row.



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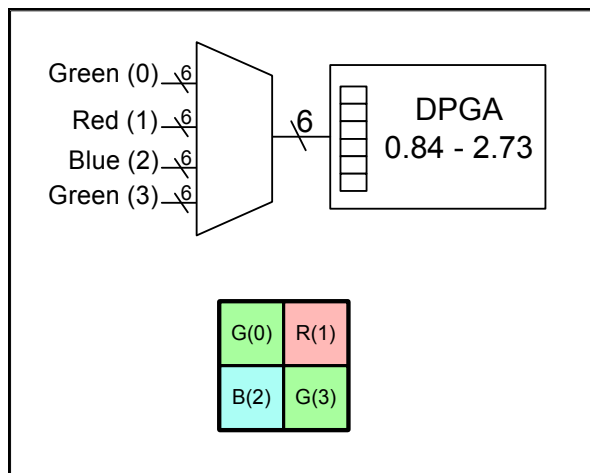


Figure 10: Color Gain Register Selection

3.2.4 Global Gain PGA

The global gain DPGA provides a 0.84 to 2.73 programmable gain adjustment for dynamic range. The gain of the amplifier is linearly programmable using a six bit gain coefficient in steps of 0.03x. The user programs the global gain via the DPGA Global Gain Register, (Table 13), on page 29.

3.2.5 Global Digital Offset Voltage Adjust (DOVA)

A programmable global offset adjustment is available on the KAC-0311. A user defined offset value is loaded via a 6-bit signed magnitude programming code via the Global DOVA Register, (Table 17), on page 33.

Offset correction allows fine-tuning of the signal to remove any additional residual error which may have accumulated in the analog signal path. This function is performed directly before analog to digital conversion and allows the user to set the 'black' level in the ADC range.

3.2.6 Analog to Digital Converter (ADC)

The ADC is a fully differential, low power circuit. A pipe-lined, Redundant Signed Digit (RSD) algorithmic

technique is used to yield an ADC with superior characteristics for imaging applications.

Integral Noise Linearity (INL) and Differential Noise Linearity (DNL) performance is specified at ± 1.0 and ± 0.5 , respectively, with no missing codes. The input dynamic range of the ADC is programmed via a Programmable Voltage Reference Generator. The positive reference voltage (VREFP) and negative reference voltages (VREFM) can be programmed from 2.5V to 1.25V and 0V to 1.25V respectively in steps of 5mV via the Reference Voltage Registers (Table 9 and Table 10). This feature is used independently or in conjunction with the DPGAs to maximize the system dynamic range based on incident illumination. The default input range for the ADC is 1.9V for VREFP and 0.6V for VREFM hence allowing a 10 bit digitization of a 1.3V peak to peak signal.

$$\frac{mV}{10dn} = \frac{2(V^+ - V^-)}{1024} = \frac{2(1.86 - 0.59)}{1024} = 2.48 \frac{mV}{10dn}$$

If the 20x gain provided by the PGAs is not sufficient, the ADC references can be used to apply additional gain to the ASP. To increase the gain the ADC references need to be moved closer to V_{cm} (1.25V). This should be used only after the PGAs have been used to their fullest since moving the ADC references too far will degrade the ADC performance. The effective gain of the ADC block will be:

$$Gain = \frac{2.48}{\frac{2(V^+ - V^-)}{1024}}$$

Ex. If Reg 0A_h=Reg 0B_h=BA_h then the ADC Gain = 2.

$$Gain = \frac{2.48}{\frac{2(1.57 - 0.93)}{1024}} = 1.98$$

The user should connect 0.1μF capacitors to the CVREFP and CVREFM pins (#19 and #18 respectively) to accurately hold the biases.

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3.2.7 Digital Signal Post Processing Data Compander

The post ADC functions provide means for manipulating the 10-bit imager data. The Data Compander allows coring of the lower order bits. In effect, it expands the values of lower signal levels and compresses high light scenes thereby allowing for on-chip contrast adjustments. The companding function performs an 8-bit transformation on the in-coming 10-bit data stream. The output is made available on the upper 8 MSBs of the 10-bit output bus. The user can select one of the 8 transformation curves shown in Figure 11 via the Post ADC Control Register, (Table 18), on page 34. The bottom curve is linear in which the input is divided by four. For other choices, the I/O relationship is kept 1:1 up to a certain breakpoint. There onwards a straight line equation is used to transform the remaining input values. The default is the linear curve, breakpoints can be selected via the slope and breakpoint control bits on the Post ADC Control Register. This function can be by-passed to output 10-bit linear data.

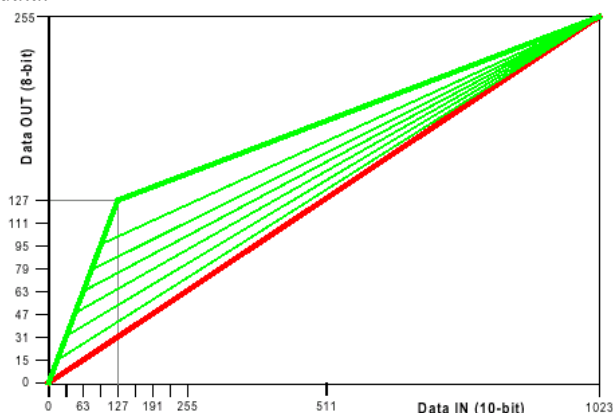


Figure 11: Available Companding Curves

4 Additional Operational Conditions

The KAC-0311 includes initialization, standby modes, and external reference voltage outputs to afford the user additional applications flexibility.

4.1 Initialization

The INIT input pin (#28) controls re-initialization of the KAC-0311. This serves to assure controlled chip and sys-

tem startup. Control is asserted via a logic high in-put. This state must be held a minimum of 1 ms. A 1 ms “wait period” should be allowed before chip processing to ensure that the start-up routines within the KAC-0311 have run to completion and to guarantee that all holding and bypass capacitors, etc. have achieved their required steady state values.

Tasks which are accomplished during startup include reset of the utility programming registers and initialization to their default values (refer to previous section for settings), reset of all internal counters and latches, and setup of the analog signal processing chain.

4.2 Standby Mode

The standby mode option is implemented to allow the user to reduce system power consumption during periods which do not require operation of the KAC-0311. This feature allows the user to extend battery life in low power applications.

By utilizing this mode, the user may reduce dynamic power consumption from 400mW, in the active processing, 13 MSPS mode, to <50 mW in the standby mode (note that dynamic power consumption is also reduced in slower conversion speed applications).

The standby mode is activated by applying an active high signal to the STBY pin (#27). The sensor can also be put in the stand by mode via bit <0> on the Power Configuration Register (OC_h)

The user may also reduce power consumption in the active processing mode by placing the KAC-0311's outputs in the tri-state mode. This action may be accomplished by placing the TS pin in the active high state. This action can also be accomplished by setting the **dbt** bit on the Power Configuration Register; Table 11, (OC_h) page 28.

Activating standby mode retains all programmed registers.

4.3 Internal Bias Current Control

The ASP chain has internally generated bias currents that result in an operating power consumption of nearly



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400mW. By attaching a resistor between pin 13, EXTRES; and ground, the user can reduce the power consumption of the device. This feature is enabled by writing a 1_b to bit **res** of the Power Configuration Register. Figure 12 depicts the power savings that can be achieved with an external resistor at a specific clock rate. Additional power savings can be achieved at lower clock rates.

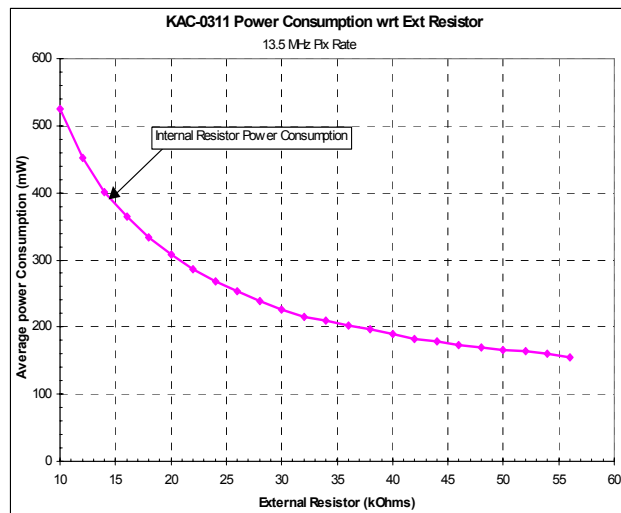


Figure 12: Power Consumption dependence on External Resistor

4.4 Readout Speed

The imager will hold all specifications from 1 MHz to 10 MHz. The nominal maximum speed is 10 MHz (30FPS). The imager will work well beyond this nominal maximum speed. As the speed increases beyond 10 MHz, the power consumption increases slightly and temporal noise rises resulting in a decrease in dynamic range and ADC INL degrades. Severe degradation in sensor performance will occur when operating in excess of 20 MHz.

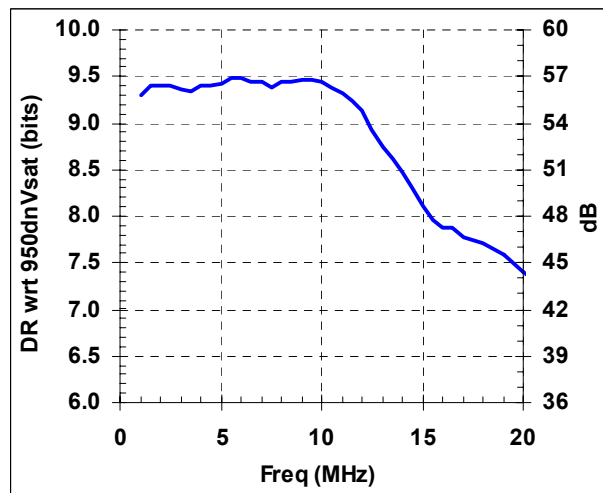


Figure 13 : Dynamic Range wrt Mclk Frequency

When operating at higher speeds, it is possible that horizontal banding might occur. This is due to one of the sample and hold stages not settling. If this condition is observed, it can be rectified by widening the SHA and SHB pulses in registers 60_h (page 44).

Note: this will change the T_{row} equation given on page 13.

T_{row} is more precisely expressed as:

$$T_{row} = (vcw_d + SHA + SHB + 19) * MCLK_{period}$$

At default conditions, $SHA = SHB = 6$, T_{row} is expressed as shown on page 13. It is recommended (see Table 2) that Reg 60h be set to 00h. This will extend the settling time to 16 clocks. Further image improvements can also be obtained by increasing the power of the chip with the external resistor (see section 4.3).



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5 KAC-0311 Waveform Diagrams

The following set of diagrams depict the input/output waveform relationships for the pixel data.

5.1 CFRS Data Waveforms

The following set of waveforms depict the CFRS output data stream from a complete frame down to individual signal relationships. Figure 14 depicts a complete frame of a CFRS output data stream in default mode. Figure 15 depicts the first row of data in the frame. Figure 16 depicts a single frame output using SFRS. This is created by setting the **cms** bit of the Capture Mode Control Register, (Table 19), on page 35 to 1_b. Figure 17 depicts the SFRS in interlaced output mode. This is created by setting the **sm** bit of the Sub-sample Control Register, (Table 20), on page 36 to 1_b.

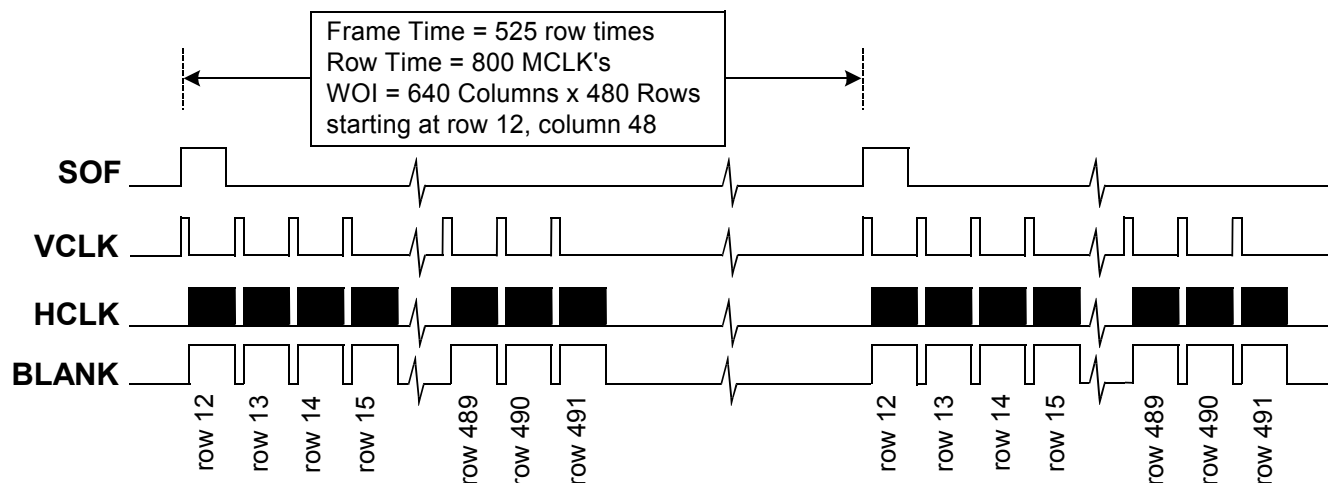


Figure 14: CFRS Default Frame Sync Waveforms

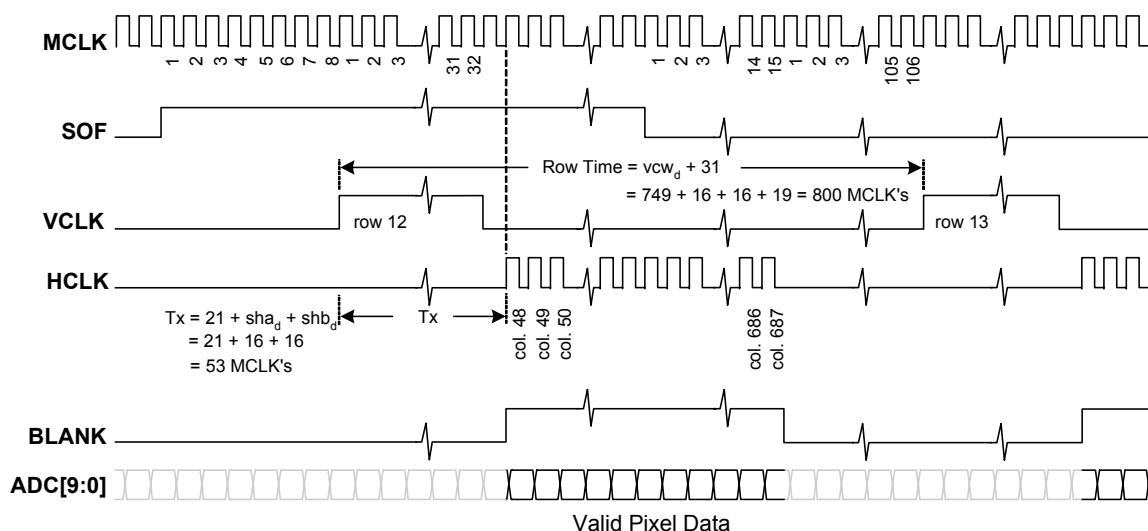


Figure 15: CFRS Default Row Syncs Waveforms



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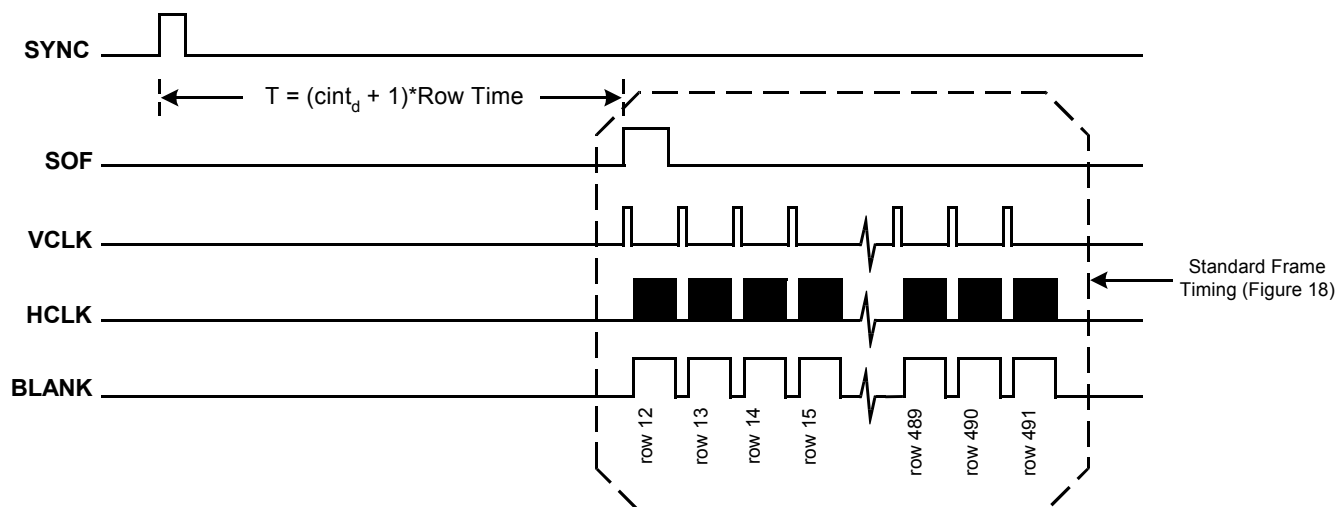


Figure 16: SFRS Single Frame Mode Sync Waveforms

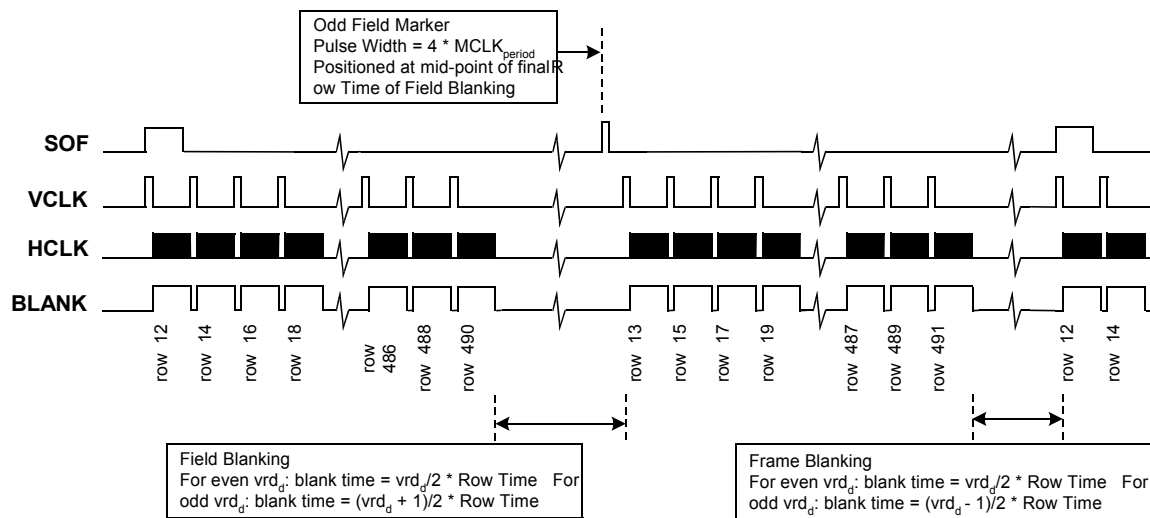


Figure 17: SFRS Interlaced Scan Mode Sync Waveforms



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5.2 SFGS Data Waveforms

The following waveforms depict the SFGS output data stream from a complete frame down to individual signal relationships. Figure 18 depicts a complete frame of a SFGS output data stream in default mode. Figure 19 depicts the first row of data in the frame.

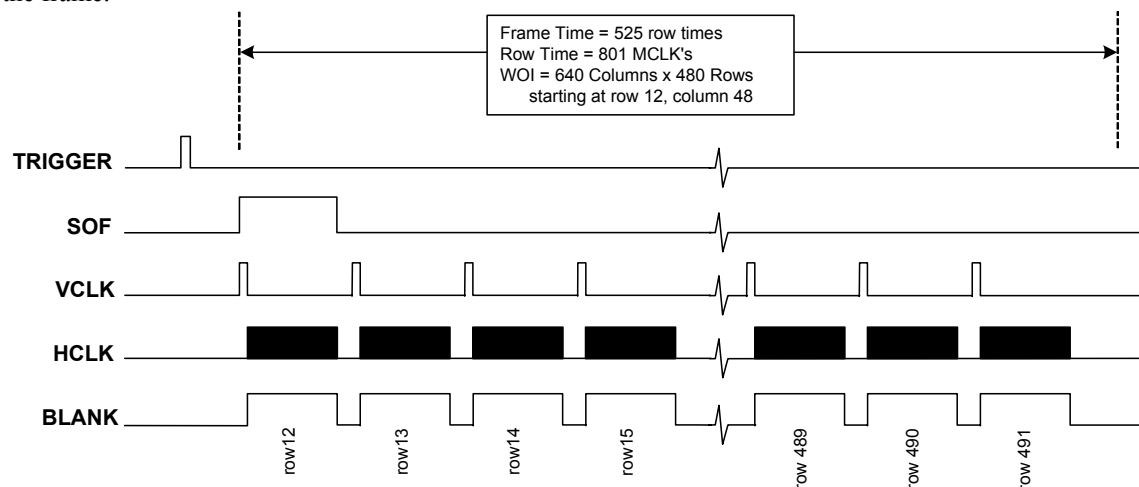


Figure 18: Frame View of SFGS Sync Waveforms

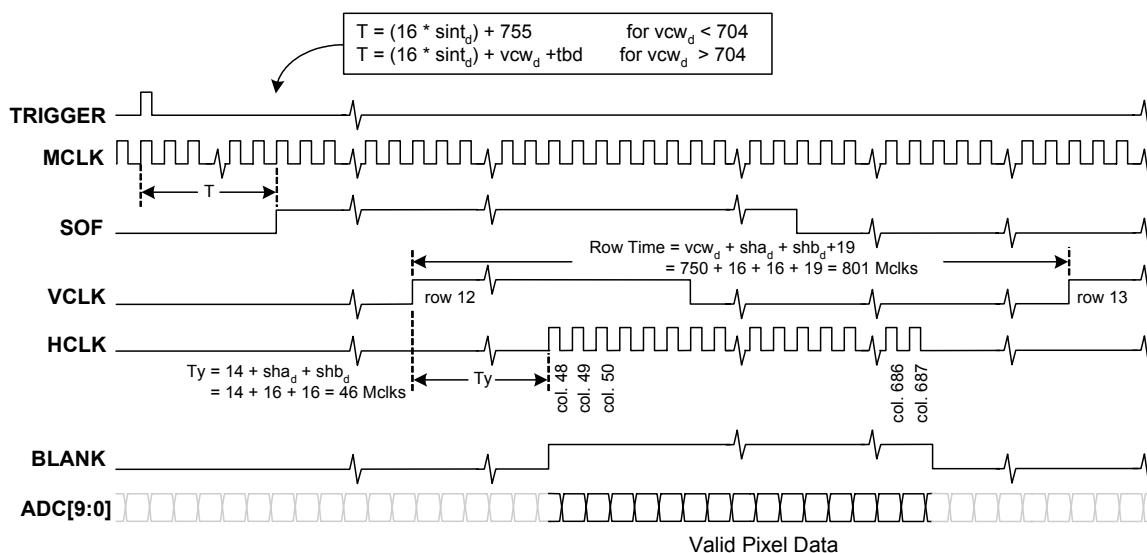


Figure 19: One row view of SFGS Sync Waveforms



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6 KAC-0311 Register Reference Map

The I²C addressing is broken up into groups of 16 and assigned to a specific digital block. The designated block is responsible for driving the internal control bus, when the assigned range of addresses are present on the internal address bus. The grouping designation and assigned range are listed in Table 1. Each block contains registers which are loaded and read by the digital and analog blocks to provide configuration control via the I²C serial interface. Table 3 contains all the I²C address assignments. The table includes a column indicating whether the register values are shadowed with respect to the sensor interface. If the register is shadowed, the sensor interface will only be updated upon frame boundaries, thereby eliminating intraframe artifacts resulting from register changes.

Address Range	Block Name
00 _h → 0F _h	Analog Register Interface
10 _h → 1F _h	Global Gain
20 _h → 2F _h	Offset Calibration
30 _h → 3F _h	Post ADC
40 _h → 60 _h	Sensor Interface
61 _h → FF _h	Factory Use

Table 1: I²C Address Ranges

The following script provides recommended chip register settings for the KAC-0311 image sensor.

Register Address (HEX)	Control Register Description	Hex Value	Decimal Value	Comments
0x0E	General Control Register	0x03	3	Set all registers to default values
0x0E	General Control Register	0x00	0	Disable Reset mode
0x60	Column Sample and Hold Control	0x00	0	Sets S&H Settling Time
0x61	Floating Diffusion Transfer Pulse Gate Width	0x1D	29	Transfer gate pulse width adj.
0x32	Post ADC Control Register	0x00	0	Turns off post ADC functions
0x20	Column DOVA DC Register	0x03	3**	Sets initial offset of the pixel. Offset is 2*bits[6..0]
0x23	Global DOVA Register	0x05	5**	Sets Global Offset bit 5 is sign bit. Bit[4..0] sets value of offset. +124 LSB in 10-bit system
0x0A	Negative ADC Reference Register	0x5F	95	Adjust ADC Gain
0x0B	Positive ADC Reference Register	0x69	105	Adjust ADC Gain
0x40	Mode Control	0x3E	36	Defines how data is capture. Sets a continuous pixel clock.

** These are recommended, however optimum values may differ from device to device.

Table 2 : I²C Initialization Register Script



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Address (Hex)	Register Function	Default	Ref Table	Shadowed?
00 _h	DPGA Color 1 Gain Register (Green of Green-Red Row)	02 _h	Table 5, Page 25	Yes
01 _h	DPGA Color 2 Gain Register (Red)	02 _h	Table 6, Page 25	Yes
02 _h	DPGA Color 3 Gain Register (Blue)	02 _h	Table 7, Page 26	Yes
03 _h	DPGA Color 4 Gain Register (Green of Blue-Green Row)	02 _h	Table 8, Page 26	Yes
04 _h	<i>Unused</i>			
05 _h	<i>Factory Use Only</i>	05 _h		No
06 _h	<i>Factory Use Only</i>	44 _h		No
07 _h	<i>Factory Use Only</i>	EE _h		No
08 _h	<i>Factory Use Only</i>	00 _h		No
09 _h	<i>Factory Use Only</i>	00 _h		No
0A _h	Negative ADC Reference Register	76 _h	Table 9, Page 27	No
0B _h	Positive ADC Reference Register	80 _h	Table 10, Page 27	No
0C _h	Power Configuration Register	00 _h	Table 11, Page 28	No
0D _h	<i>Factory Use Only</i>	00 _h		
0E _h	Reset and Tristate Control Register	00 _h	Table 12, Page 29	No
0F _h	Device Identification (read only)	23 _h		No
10 _h	DPGA Global Gain Register	00 _h	Table 13, Page 30	Yes
11 _h - 1F _h	<i>Unused</i>			
20 _h	Column DOVA DC Register	00 _h	Table 14, Page 30	Yes
21 _h	Column DOVA Control Register	00 _h	Table 15, Page 31	No
22 _h	Column DOVA RAM	00 _h	Table 16, Page 32	No
23 _h	Global DOVA Register	00 _h	Table 17, Page 33	Yes
24 _h - 2F _h	<i>Unused</i>			
30 _h	<i>Factory Use Only</i>	FE _h		No
31 _h	<i>Factory Use Only</i>	01 _h		No
32 _h	Post ADC Control Register	30 _h	Table 18, Page 34	No
33 _h - 3F _h	<i>Unused</i>			

Table 3: I²C Address Assignments (0_h- 3F_h)



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Address (Hex)	Register Function	Default	Ref Table	Shadowed?
40 _h	Capture Mode Register	35 _h	Table 19, Page 35	Yes
41 _h	Sub-Sample Control Register	00 _h	Table 20, Page 36	Yes
42 _h - 44 _h	<i>Unused</i>			
45 _h	WOI Row Pointer MSB Register	00 _h	Table 21, Page 37	Yes
46 _h	WOI Row Pointer LSB Register	0C _h	Table 22, Page 37	Yes
47 _h	WOI Row Depth MSB Register	01 _h	Table 25, Page 38	Yes
48 _h	WOI Row Depth LSB Register	DF _h	Table 26, Page 38	Yes
49 _h	WOI Column Pointer MSB Register	00 _h	Table 23, Page 37	Yes
4A _h	WOI Column Pointer LSB Register	30 _h	Table 24, Page 38	Yes
4B _h	WOI Column Width MSB Register	02 _h	Table 27, Page 39	Yes
4C _h	WOI Column Width LSB Register	7F _h	Table 28, Page 39	Yes
4D _h	Integration Time MSB Register	00 _h	Table 29, Page 40	Yes
4E _h	Integration Time ISB Register	02 _h	Table 30, Page 40	Yes
4F _h	Integration Time LSB Register	0C _h	Table 31, Page 40	Yes
50 _h	CFCM Virtual Frame Row Depth MSB Register	02 _h	Table 32, Page 41	Yes
51 _h	CFCM Virtual Frame Row Depth LSB Register	0C _h	Table 33, Page 41	Yes
52 _h	CFCM Virtual Frame Column Width MSB Register	02 _h	Table 34, Page 42	Yes
53 _h	CFCM Virtual Frame Column Width LSB Register	E0 _h	Table 35, Page 42	Yes
54 _h	SOF Control Register	C0 _h	Table 36, Page 43	No
55 _h	VCLK Control Register	90 _h	Table 37, Page 43	No
56 _h - 5F _h	<i>Unused</i>			
60 _h	Sample and Hold width Register	66 _h	Table 38, Page 44	Yes
61 _h - 64 _h	<i>Factory Use Only</i>			
65 _h - FF _h	<i>Unused</i>			

Table 4: I²C Address Assignments (40_h - FF_h)



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7 Detailed Register Block Assignments

This section describes in further detail the functional operation of the various KAC-0311 programmable registers. The registers are subdivided into various blocks for ease of addressability and use (see Tables 3 and 4). In each table where a suffix code is used; h = hex, b = binary, and d = decimal.

7.1 Color Gain Registers 00h → 03h

The four Color Gain Registers, Color Tile Configuration Register, and four Color Tile Row definitions define how white balance is achieved on the device. Six-bit gain codes can be selected for four separate colors: Table 5, Table 6, Table 7, and Table 8. Gain for each individual color register is programmable given the gain function defined in the table. The user programs these registers to account for changing light conditions to assure a white balanced output. The default value in each register is provided for a unity gain. In addition, the default CFA pattern color is listed in the title of each register.

Address		DPGA Color 1 Gain Code					Default
00h		Green of Green-Red Row					02 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
x	x	cg1[5]	cg1[5]	cg1[5]	cg1[5]	cg1[5]	cg1[5]
Bit Number	Function	Description					Reset State
7 - 6	Unused	Unused					xx _b
5 - 0	Gain	Gain = 0.84 + (0.03 * cg1 _d)					000010 _b

Table 5: DPGA Color 1 Gain Register (00_h)

Address		DPGA Color 2 Gain Code					Default
01h		Red					02 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
x	x	cg2[5]	cg2[5]	cg2[5]	cg2[5]	cg2[5]	cg2[5]
Bit Number	Function	Description					Reset State
7 - 6	Unused	Unused					xx _b
5 - 0	Gain	Gain = 0.84 + (0.03 * cg2 _d)					000010 _b

Table 6: DPGA Color 2 Gain Register (01_h)



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Address		DPGA Color 3 Gain Code					Default
02h		Blue					02 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
x	x	cg3[5]	cg3[5]	cg3[5]	cg3[5]	cg3[5]	cg3[5]
Bit Number	Function	Description					Reset State
7 - 6	Unused	Unused					xx _b
5 - 0	Gain	Gain = 0.84 + (0.03 * cg3 _d)					000010 _b

Table 7: DPGA Color 3 Gain Register (02_h)

Address		DPGA Color 4 Gain Code					Default
03h		Green of Blue-Green Row					02 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
x	x	cg4[5]	cg4[5]	cg4[5]	cg4[5]	cg4[5]	cg4[5]
Bit Number	Function	Description					Reset State
7 - 6	Unused	Unused					xx _b
5 - 0	Gain	Gain = 0.84 + (0.03 * cg4 _d)					000010 _b

Table 8: DPGA Color 4 Gain Register (03_h)



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7.2 Reference Voltage Adjust Registers (0A_h, 0B_h)

The analog register block allows programming the input voltage range of the analog to digital converter to match the saturation voltage of the pixel array. The voltage reference generator can be programmed via two registers; **prv**(2.5V to 1.25V) Table 10, **nrv**(0 to 1.25V) Table 9, in 5mV steps. The default settings for **prv** produce a 1.86V positive reference. The default settings for **prv** produce a 0.59V negative reference. These two references define the ADC analog input range. When adjusting these values, the user should keep the voltage range centered around 1.25V. These ADC references can be adjusted to mV/DN of the ADC. This effectively acts as another gain stage just before the ADC. Excessive adjustment of these values from their default can result in increased power consumption and increased image artifacts. The following equation defines the determination of mV/DN:

$$\frac{mV}{10dn} = \frac{2(V^+ - V^-)}{1024} = \frac{2(1.86 - 0.59)}{1024} = 2.48 \frac{mV}{10dn}$$

If the 20x gain provided by the PGAs is not sufficient, the ADC references can be used to apply additional gain to the ASP. To increase the gain the ADC references need to be moved closer to V_{cm} (1.25V). This should be used only after the PGAs have been used to their fullest since moving the ADC references too far will degrade the ADC performance. The effective gain of the ADC block will be:

$$Gain = \frac{2.48}{\frac{2(V^+ - V^-)}{1024}}$$

Address 0A _h		"Negative" ADC Reference Voltage						Default 76 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)	
nrv[7]	nrv[6]	nrv[5]	nrv[4]	nrv[3]	nrv[2]	nrv[1]	nrv[0]	
Bit Number	Function	Description						Reset State
7 - 0	Reference	Voltage = 0.0 + (5mV * nrv _d)						01110110 _b (0.59V)

Table 9: Negative Voltage Reference Register (0A_h)

Address 0B _h		"Positive" ADC Reference Voltage						Default 80 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)	
prv[7]	prv[6]	prv[5]	prv[4]	prv[3]	prv[2]	prv[1]	prv[0]	
Bit Number	Function	Description						Reset State
7 - 0	Reference	Voltage = 2.5 - (5mV * prv _d)						10000000 _b (1.86V)

Table 10: Positive Voltage Reference Register (0B_h)



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7.3 Power Configuration Registers (0C_h)

The Analog Register Block also contains a Power Configuration Register and a Reset Control Register. The Power Configuration Register controls the internal analog functionality that directly effect power consumption of the device. An external precision resistor pin is available on the KAC-0311 that may be used to more accurately regulate the internal current sources. This serves to minimize variations in power consumption that are caused by variations in internal resistor values as well as offer a method to reduce the power consumption of the device. The default for this control uses the internally provided resistor which is nominally 12.5k Ω . This feature is enabled by setting the **res** bit of the Power Configuration Register and placing a resistor between the pin; EXTRES, and ground. Figure 12 depicts the power savings that can be achieved with an external resistor at a specific clock rate. Power is further reduced at lower clock rates. The databus output; ADC[9:0], is tristated using the Power Configuration Register by setting the **dbt** bit. The KAC-0311 is put into a standby mode via the I²C interface by setting the **sby** bit of the Power Configuration Register.

Address 0C _h		Power Configuration					Default 00 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
x	res	fuo	fuo	fuo	fuo	dbt	sby
Bit Number	Function	Description	Reset State				
7	Unused	Unused	x _b				
6	Int/Ext Resistor	0 _b = Internal Resistor 1 _b = External Resistor	0 _b				
5 - 2	FUO	Factory Use Only	0000 _b				
1	Tristate Enable	0 _b = Output Data Bus enabled 1 _b = Output Data Bus Tristated	0 _b				
0	Software Standby	0 _b = Soft Standby Inactive 1 _b = Soft Standby Active	0 _b				

Table 11: Power Configuration Register (0C_h)



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7.4 Reset and Tristate Control Register (0E_h)

Additional control of the KAC-0311 can be had using the Reset Control Register. Setting the **clt** bit of this register will tristate the sync signals SOF, VCLK, and HCLK. Setting the **ssr** bit of this register will reset all the non-user programmable registers to a known reset state. This is useful in situations when control of the KAC-0311 has been lost due to system interrupts and the device needs only be restarted using the earlier user programmed values. Setting the **sit** bit allows the user to completely reset the KAC-0311 to the default state via the serial control interface. For both reset bits **ssr**, and **sit**, the user must return those bits to 0 to enable continued operation.

Address 0E _h		Reset and Tristate Control					Default 00 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
x	x	x	x	x	clt	ssr	sit
Bit Number	Function	Description					Reset State
7 - 3	Unused	Unused					xxxxxx _b
2	Tristate	0 _b = SOF, VCLK, HCLK Output Enabled 1 _b = SOF, VCLK, HCLK Output in Tristate					0 _b
1	State Reset	0 _b = Normal Mode 1 _b = Reset all non-programmable registers to default state					0 _b
0	Soft Reset	0 _b = Normal Mode 1 _b = Reset all registers to default state					0 _b

Table 12: Reset and Tristate Control Register (0E_h)**7.5 Global Gain Register (10_h)**

The DPGA Gain Register allows the user to set a global gain via a 6 bit register. This is applied universally to all the pixel outputs. This enables the user to account for varying light conditions using a gain range of 1x to 8x in steps of 0.12x. The default value for this register results in unity gain.

Address 10 _h		Global Gain					Default 00 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
x	x	gg[5]	gg[4]	gg[3]	gg[2]	gg[1]	gg[0]
Bit Number	Function	Description					Reset State
7 - 6	Unused	Unused					xx _b
5 - 0	Gain	Gain = 0.84 + (0.03 * gg _d)					000000 _b

Table 13: DPGA Global Gain Register (10_h)**7.6 Column DOVA DC Register (20_h)**

Offset adjustments for the KAC-0311 are done in separate sections of the ASP to facilitate FPN removal and final image black level set. The primary purpose of the Column DOVA DC Register is to compensate for pre-gain offset. If this register



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is set to zero the user may find that the dark level of some chips may move with different programmed gain values. In addition the white balance gain stage can result in different effective dark levels for different colors. These effects MAY cause distortion with certain post image signal processing. In these cases the Column DOVA DC Register can be programmed such that the dark pixel level is independent of programmed gain values. The simplest method for setting this register is to place the imager in the dark and record the mean value for the dark pixels. Then increase the global gain register(10_h) to the maximum gain to be used in the application. Adjust register 20_h until the dark level has returned to the level previously recorded with unity gain. This process can be repeated again for greater accuracy since the dark level at unity gain will now have shifted slightly. For many operational scenarios, this register can be left in its default state of 00_h. In such cases this register can be used to apply additional global offset. If during the calibration of the register value the any pixel are observed to be clipping at zero counts, it is then necessary to temporarily increase the global DOVA(reg 23_h) to avoid clipping.

Address		Column DOVA DC					Default
20 _h							00 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
x	x	cdd[5]	cdd[4]	cdd[3]	cdd[2]	cdd[1]	cdd[0]
Bit Number	Function	Description					Reset State
7 - 6	Unused	Unused					xx _b
5	Sign	0 _b = Positive Offset 1 _b = Negative Offset					0 _b
4 - 0	Column DC Offset	Offset = 2 * cdd _d					00000 _b

Table 14: Column DOVA DC Offset (20_h)



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7.7 Column DOVA Control (21_h)

The Column DOVA Control Register is used to control the Column DOVA functionality and operation modes. Setting bit **ece** enables the per-column DOVA to be used and the per-column offset values loaded into the DOVA RAM will be applied to the pixel output. When **ece**=0 the value in register 20_h is ignored. The global DOVA adjust circuit is enabled by default(**ece**=0).

Once the Column DOVA RAM has been enabled the random values of the RAM are applied to each column. This will result in larger column noise, but random. Typical use requires that the RAM be programmed by the user. Programming the Ram requires repeated writes to the Column DOVA RAM Register (22_h). The first write sets the RAM location for the first column, and internal counter is incremented and the second write to the same register is placed into the second memory location for the second column. In the case of loss of control of the I²C bus during the write process setting the **cntr** bit will reset the internal counter to the first column memory location. It is recommended that the **cntr** bit is set prior to programming the Column DOVA RAM. This bit will auto-clear, so there is no need to set it back to zero after having set it to one.

Address 21 _h		Column DOVA Control					Default 00 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
fuo	fuo	fuo	ece	fuo	fuo	cntr	fuo
Bit Number	Function	Description	Reset State				
7 - 5	FUO	Factory Use Only	000 _b				
4	Column DOVA mode	0 _b = Column DOVA DC enabled (Register 20 _h) 1 _b = Column DOVA RAM enabled (Register 22 _h)	0 _b				
3 - 2	FUO	Factory Use Only	00 _b				
1	Counter Reset	0 _b = Column RAM counter incrementing 1 _b = Reset Column RAM counter	0 _b				
0	FUO	Factory Use Only	0 _b				

Table 15: Column DOVA Control (21_h)



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7.8 Column DOVA RAM (22_h)

The Column DOVA RAM is a 704 by 4-bit memory that contains the per-column offset adjustment used to eliminate column offset FPN. The RAM powers up with random values and must be programmed by the user before being applied to the image. The RAM can be programmed even while the Column DOVA Control register is set to use the Column DOVA DC. One method of calculating the needed RAM values is to average all of the pixels in each column in a dark image capture. This column average will identify which columns may need an adjustment. An internal counter will step the internal RAM address automatically from column 0 to column 703; where column 0 is defined as the left-most column of the pixel array. The user should set the **cntr** bit of the Column DOVA Control Register(21_h) prior to loading the Column DOVA RAM to assure proper addressing. Each time a value is written to the Column DOVA RAM the value is place in the memory location of the present column and the internal column address is automatically incremented. The next value that is written to the Column DOVA RAM register will go in this next column and the column address pointer will again be auto-incremented. If the exact location of the column RAM pointer is not known then the user must reset the counter with the reset bit in the Column DOVA Control Register and then start sending column offset values for column 0 again.

Note that the imager cannot be in DC mode and RAM mode at the same time. Thus any value that had been placed in the Column DOVA DC Register to compensate for pre-gain offset must be added to every column in the Column DOVA RAM to compensate for both pre-gain offset and objectionable column offset FPN. In order to have enough range to compensate both pre-gain and column offset each count of the 4-bit memory is set to move the column offset by 2DN. The user must divide the calculated offset needed by 2 before programming the value into the Column DOVA RAM.

Address 22 _h		Column DOVA RAM					Default 00 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
x	x	x	x	cor[3]	cor[2]	cor[1]	cor[0]
Bit Number	Function	Description	Reset State				
7 - 4	Unused	Unused	xxxx _b				
3	Sign	0 _b = Positive Offset 1 _b = Negative Offset	0 _b				
2 - 0	Column Offset	Offset = 2 * cor _d	000 _b				

Table 16: Column DOVA RAM (22_h)



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7.9 Global DOVA (23_h)

The Global DOVA Register performs a final offset adjustment in analog space just prior to the ADC. The 6-bit register uses its MSB to indicate positive or negative offset. Each register value changes the offset by 4 LSB code levels hence giving an offset range of ± 124 DN. As an example, to program an offset of +92 DN, the value of 010111_b (23_d or 17_h) should be loaded. This offset is used to place the dark level within the ADC range.

Address 23 _h		Global DOVA					Default 00 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
x	x	gd[5]	gd[4]	gd[3]	gd[2]	gd[1]	gd[0]
Bit Number	Function	Description	Reset State				
7 - 6	Unused	Unused	xx _b				
5	Sign	0 _b = Positive Offset 1 _b = Negative Offset	0 _b				
4 - 0	Column DC Offset	Offset = 2 * gd _d	00000 _b				

Table 17: Global DOVA Register (23_h)



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7.10 Post ADC Control (32_h)

The post ADC Control Register performs certain rudimentary transformation to the digitized data. The **cpe** bit enables the compander which provides for the 10 to 8 bit noise coring described in section 3.2.7 on page 17. One of 8 available transform curves can be selected by using the **cps** and **cpb[2:0]** bits. The slope of the transform is defined using **cps** while the breakpoint is defined by **cpb[2:0]**. See Figure 11 on page 17. It is recommended that this register be set to 00h to clear bits 6-4.

Address 32 _h		Post ADC Control						Default 30 _h (00 _h)
7 (msb)	6	5	4	3	2	1	0 (lsb)	
cpe	fuo	fuo	fuo	cps	cpb[2]	cpb[1]	cpb[0]	
Bit Number	Function	Description						Reset State
7	Compander Enable	0 _b = Compander Disabled 1 _b = Compander Enabled						0 _b
6-4	FUO	FUO						011 _b
3	Compander Slope	0 _b = Invalid when cpb[2:0] != 000 _b 1 _b = 1:1 input:output						0 _b
2 - 0	Compander Knee	000 _b = Linear 001 _b = 15 on the output axis 010 _b = 31 on the output axis 011 _b = 47 on the output axis 100 _b = 63 on the output axis 101 _b = 79 on the output axis 110 _b = 95 on the output axis 111 _b = 127 on the output axis						000 _b

Table 18: Post ADC Control Register (32_h)



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7.11 Capture Mode Control (40_h)

The Capture Mode Control Register defines how the data is captured and how the data is to be provided at the output. The **sms** bit defines the shutter mode, CFRS or SFGS, of the device as described section 2.3. CFRS (Continuous Frame Capture Mode) is the default mode. In this mode frames are captured with a rolling shutter.

Setting the **cms** bit will stop the current CFRS output data stream at the end of the current frame. While the **cms** bit is high(=1), the output of frames can be paused with the TRIGGER input pin. When the TRIGGER pin is low (zero volts) frames are continuous. When the TRIGGER pin is high (3.3 V) the output of frames is suspended. The default for **cms** is low(=0). In this mode the frames are continuously output and the TRIGGER pin is ignored. The frame rate is slightly reduced when the **cms** is high(=1) because care is taken in the startup such that the first frame output is valid. This causes a slight delay at the start of each frame. With the **cms** low(=0), the frame rate is faster, but the first frame may be corrupt.

The **frc** bit is used to enable or disable the Frame Rate Clamp (FRC). Unsetting this bit will turn off the FRC and the output dark level will drift slowly with time. The FRC is enabled by default. The **sp** bit is used to define whether SOF is active high or low. SOF is active high in default. The **ve** bit is used to determine whether VCLK is output at the beginning of the virtual frame rows or only for the WOI rows. The **ve** bit defaults to VCLK on WOI rows only. The **vp** bit is used to define whether VCLK is active high (the default) or active low. The **he** bit is used to determine whether HCLK is output continuously (needed for some frame grabbers) or only for pixels within the WOI (default). The **hp** bit is used to define whether HCLK is active high (default) or low.

Address 40 _h		Capture Mode Control						Default 35 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)	
sms	cms	frc	sp	ve	vp	he	hp	
Bit Number	Function	Description	Reset State					
7	Shutter Mode	0 _b = Rolling Shutter 1 _b = SFGS Global Shutter	0 _b					
6	Rolling Shutter Mode	0 _b = Continuous Frames Output (CFRS) 1 _b = Single Frames gated by TRIGGER pin (SFRS)	0 _b					
5	Frame Clamp	0 _b = FRC Disabled 1 _b = FRC Enabled	1 _b					
4	SOF Phase	0 _b = SOF sync active low 1 _b = SOF sync active high	1 _b					
3	VCLK Enable	0 _b = VCLK Sync on WOI rows only 1 _b = VCLK Sync on WOI and Virtual Rows	0 _b					
2	VCLK Phase	0 _b = Active low 1 _b = Active high	1 _b					
1	HCLK Enable	0 _b = Pixel sync on WOI pixels only 1 _b = Continuous pixel sync	0 _b					
0	HCLK Phase	0 _b = Active low 1 _b = Active high	1 _b					

Table 19: Capture Mode Register (40_h)



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7.12 Subsample Control (41_h)

The sub-sample Control Register is used to define what pixels of the WOI are read and the method they are output. See section 2.3.4 Image Scan Modes on page 10 for details on the readout modes. The **sm** bit is used to readout the frame in interlaced mode. Bit **cm** must be set to enable color kernel sub-sampling for color imagers rather than pixel sub-sampling which is appropriate for Monochrome imagers. By default sub-sampled frames readout faster than the full frame image. Any pixel not selected in the sub-sample mode is ignored, thereby not slowing the frame rate. The **ptm** bit can be set to force the frame rate to remain at full frame even during sub-sampling. The 'skipped' pixels remain as place-holders slowing integration time and readout rate. The data output at these skipped pixel is the last valid pixel. The sub-sample mode of the rows is defined by **rf**[1:0] while the column mode is independently defined by **cf**[1:0].

Address 41 _h		Subsample Control					Default 00 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
x	sm	cm	ptm	rf[1]	rf[0]	cf[1]	cf[0]
Bit Number	Function	Description	Reset State				
7	Unused	Unused	x _b				
6	Scan Mode	0 _b = Progressive scan 1 _b = Interlaced scan	0 _b				
5	Color Mode	0 _b = Monochrome Pattern Sampling 1 _b = Bayer Pattern Sampling	0 _b				
4	Pixel Timing Mode	0 _b = Frame rate compression with sub-sampling 1 _b = Constant frame rate independent of sub-sampling	0 _b				
3 - 2	Row Sub-Sampling Mode	00 _b = Full WOI readout 01 _b = Read one kernel, skip one (1/2 sampled) 10 _b = Read one kernel, skip three (1/4 sampled) 11 _b = Read one kernel, skip seven (1/8 sampled)	00 _b				
1 - 0	Column Sub-Sampling Mode	00 _b = Full WOI readout 01 _b = Read one kernel, skip one (1/2 sampled) 10 _b = Read one kernel, skip three (1/4 sampled) 11 _b = Read one kernel, skip seven (1/8 sampled)	00 _b				

Table 20: Sub-Sample Control Register (41_h)



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7.13 Programmable Window of Interest (WOI) (45_h-4C_h)

The WOI is defined by a set of registers that indicate the upper-left starting point for the window and another set of registers that define the size of the window. Refer to Figure 5: WOI Definition on page 11 for a pictorial representation of the WOI within the active pixel array. The WOI Row Pointer, **wrp**[8:0], and the WOI Column Pointer, **wcp**[9:0], mark the upper-left starting point for the WOI. The WOI Row Depth, **wrd**[8:0] and the WOI Column Depth, **wcd**[9:0] indicate the size of the WOI. If the WOI is programmed to be bigger than the virtual window, the virtual window will be expanded to fit the WOI.

Address		WOI Row Pointer MSB						Default
45 _h								00 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)	
x	x	x	x	x	x	x		wrp[8]
Bit Number	Function	Description						Reset State
7 - 1	Unused	Unused						xxxxxxx _b
0	WOI Row Pointer	Forms 9-bit Row address (with Reg 46 _h) for the top of the WOI						0 _b

Table 21: WOI Row Pointer MSB Register (45_h)

Address		WOI Row Pointer LSB						Default
46 _h								0C _h
7 (msb)	6	5	4	3	2	1	0 (lsb)	
wrp[7]	wrp[6]	wrp[5]	wrp[4]	wrp[3]	wrp[2]	wrp[1]	wrp[0]	
Bit Number	Function	Description						Reset State
7 - 0	WOI Row Pointer	Forms 9-bit Row address (with Reg 45 _h) for the top of the WOI						00001100 _b (12 _d)

Table 22: WOI Row Pointer LSB Register (46_h)

Address		WOI Column Pointer MSB						Default
49 _h								00 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)	
x	x	x	x	x	x	wcp[9]	wcp[8]	
Bit Number	Function	Description						Reset State
7 - 2	Unused	Unused						xxxxxxx _b
1 - 0	WOI Col Pointer	Forms 10-bit Column address (with Reg 4A _h) for the left of the WOI						00 _b

Table 23: WOI Column Pointer MSB Register (49_h)



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Address 4A _h	WOI Column Pointer LSB						Default 30 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
wcp[7]	wcp[6]	wcp[5]	wcp[4]	wcp[3]	wcp[2]	wcp[1]	wcp[0]
Bit Number	Function	Description					Reset State
7 - 0	WOI Col Pointer	Forms 10-bit Column address (with Reg 49 _h) for the left of the WOI					00110000 _b (48 _d)

Table 24: WOI Column Pointer LSB Register (4A_h)

Address 47 _h	WOI Row Depth MSB						Default 01 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
x	x	x	x	x	x	x	wrd[8]
Bit Number	Function	Description					Reset State
7 - 1	Unused	Unused					xxxxxxx _b
0	WOI Row Depth	Forms 9-bit number of row address (with Reg 47 _h) for the depth of the WOI. Depth = wrd _d + 1 (default = 480 rows)					1 _b

Table 25: WOI Row Depth MSB Register (47_h)

Address 48 _h	WOI Row Depth LSB						Default DF _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
wrd[7]	wrd[6]	wrd[5]	wrd[4]	wrd[3]	wrd[2]	wrd[1]	wrd[0]
Bit Number	Function	Description					Reset State
7 - 0	WOI Row Depth	Forms 9-bit number of row address (with Reg 47 _h) for the depth of the WOI. Depth = wrd _d + 1 (default = 480 rows)					11011111 _b

Table 26: WOI Row Depth LSB Register (48_h)



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Address 4B _h	WOI Column Width MSB						Default 02 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
x	x	x	x	x	x	wcw[9]	wcw[8]
Bit Number	Function	Description					Reset State
7 - 2	Unused	Unused					xxxxxx _b
1 - 0	WOI Col Width	Forms 10-bit number of column address (with Reg 4C _h) for the width of the WOI. Width=wcw _d +1 (default = 640 cols)					10 _b

Table 27: WOI Column Depth MSB Register (4B_h)

Address 4C _h	WOI Column Width LSB						Default 7F _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
wcw[7]	wcw[6]	wcw[5]	wcw[4]	wcw[3]	wcw[2]	wcw[1]	wcw[0]
Bit Number	Function	Description					Reset State
7 - 0	WOI Col Pointer	Forms 10-bit number of column address (with Reg 4B _h) for the width of the WOI. Width=wcw _d +1 (default = 640 cols)					01111111 _b

Table 28: WOI Column Depth LSB Register (4C_h)



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7.14 Integration Time Control (4D_h → 4F_h)

The integration Time registers control the integration time for the pixel array. Integration time for SFGS, **sint**[19:0], is measured in MCLK cycles while the integration time for CFRS, **cint**[15:0], is measured in Virtual Row times. Refer to Figure 7 on page 12 for a pictorial description of the Virtual Frame and its relationship to the WOI. A Virtual Frame is the mechanism by which the user controls the integration time and frame time for the output data stream. By adding additional rows or columns as 'blanking' to the WOI to form the Virtual Frame, the user can control the amount of blanking in both horizontal and vertical space. The MSB of the Integration Time registers (4D_h) is only used in SFGS. It is ignored in CFRS.

Integration Time_{SFGS} = sint_d * 16 * (MCLKC period) (default = 8400 Mclks)

Integration Time_{CFRS} = cint_d * vcw_d * (MCLKC period) (default = 525 Rows = 409,500 MCLKs)

Address 4D _h		Integration Time MSB					Default 00 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
x	x	x	x	sint[19]	sint[18]	sint[17]	sint[16]
Bit Number	Function	Description					Reset State
7 - 4	Unused	Unused					xxxx _b
3 - 0	Integration Time	SFCM: MSB of sint[19:0]; integration MCLK's CFCM: Unused					0000 _b

Table 29: Integration Time MSB Register (4D_h)

Address 4E _h		Integration Time ISB					Default 02 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
sint[15]	sint[14]	sint[13]	sint[12]	sint[11]	sint[10]	sint[9]	sint[8]
cint[15]	cint[14]	cint[13]	cint[12]	cint[11]	cint[10]	cint[9]	cint[8]
Bit Number	Function	Description					Reset State
7 - 0	Integration Time	SFCM: ISB of sint[19:0]; integration MCLK's CFCM: MSB of cint[15:0]; Integration Rows					00000010 _b

Table 30: Integration Time ISB Register (4E_h)

Address 4F _h							Default 0C _h
Integration Time ISB							
7 (msb)	6	5	4	3	2	1	0 (lsb)
sint[7]	sint[6]	sint[5]	sint[4]	sint[3]	sint[2]	sint[1]	sint[0]
cint[7]	cint[6]	cint[5]	cint[4]	cint[3]	cint[2]	cint[1]	cint[0]
Bit Number	Function	Description					Reset State
7 - 0	Integration Time	SFCM: LSB of sint[19:0]; integration MCLK's CFCM: LSB of cint[15:0]; Integration Rows					00001100 _b

Table 31: Integration Time LSB Register (4F_h)



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7.15 Programmable Virtual Frame (50_h → 53_h)

A Virtual Frame is the mechanism by which the user controls the integration time and frame time for the output data stream. By adding additional rows or columns as ‘blanking’ to the WOI to form the Virtual Frame, the user can control the amount of blanking in both horizontal and vertical space. Both the Virtual Frame Row Depth, **vr_d**[13:0], and the Virtual Frame Column Width, **vc_w**[9:0], have a range of 0_d to 16384_d. If the Virtual Frame is programmed to be smaller than the WOI then the WOI will be shrunk to fit in the virtual frame. The Virtual Frame must be 1 row and 6 columns larger than the WOI or image artifacts may occur. The Virtual Frame defines the maximum integration time in CFRS mode. If the integration register is programmed with more rows than are in the Virtual Frame then the integration time will be clipped to the number of rows in the virtual frame. The number of Virtual rows has no meaning in SFGS mode, but the Virtual Columns CAN be extended to slow readout rate.

Address		Virtual Frame Row Depth MSB					Default
50 _h							02 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
x	x	vr _d [13]	vr _d [12]	vr _d [11]	vr _d [10]	vr _d [9]	vr _d [8]
Bit Number	Function	Description					Reset State
7 - 6	Unused	Unused					xx _b
5 - 0	Virtual Row Depth	MSB of 14-bit vr _d [13:0], definition of the number of rows in the Virtual Frame					000010 _b

Table 32: Virtual Frame Row Depth MSB (50_h)

Address 51 _h	Virtual Frame Row Depth LSB						Default 0C _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
vr _d [7]	vr _d [6]	vr _d [5]	vr _d [4]	vr _d [3]	vr _d [2]	vr _d [1]	vr _d [0]
Bit Number	Function	Description					Reset State
7 - 0	Virtual Row Depth	LSB of 14-bit vr _d [13:0], definition of the number of rows in the Virtual Frame					00001100 _b

Table 33: Virtual Frame Row Depth LSB (51_h)



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Address 52 _h	Virtual Frame Column Width MSB						Default 02 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
x	x	vcw[13]	vcw[12]	vcw[11]	vcw[10]	vcw[9]	vcw[8]
Bit Number	Function	Description					Reset State
7 - 6	Unused	Unused					xx _b
5 - 0	Virtual Col Width	MSB of 14-bit vcw[13:0], definition of the number of columns in the Virtual Frame					000010 _b

Table 34: Virtual Frame Column Width MSB (52_h)

Address 53 _h	Virtual Frame Column Width LSB						Default ED _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
vrđ[7]	vrđ[6]	vrđ[5]	vrđ[4]	vrđ[3]	vrđ[2]	vrđ[1]	vrđ[0]
Bit Number	Function	Description					Reset State
7 - 0	Virtual Col Width	LSB of 14-bit vcw[13:0], definition of the number of columns in the Virtual Frame					11101101 _b 750 cols

Table 35: Virtual Frame Column Width LSB (53_h)



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7.16 SOF Control Register (54_h)

The SOF Control Register is used to define the size and position of the SOF sync pulse. This adjust can be used to vary the sync positions relative to valid pixel data. In this way an acquisition system that uses the sync pulses for display can be shifted to add or avoid image borders. Adjusting the position or length of the SOF sync does NOT alter the frame rate, the sync signal is simply shifted and overlaps the valid line and pixel data. Moving the rising edge of the SOF will also move the rising edge of the VCLK(Reg 55_h). This is so that the VCLK sync does not occur before the SOF pulse. The delay adjust is in ½ cycles, it takes two programmed counts to delay the rising edge by one image pixel.

Address 54 _h		SOF Control					Default C0 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
sof[7]	sof[6]	sof[5]	sof[4]	sof[3]	sof[2]	sof[1]	sof[0]
Bit Number	Function	Description					Reset State
7 - 6	SOF Control	00 _b = 1 MCLK Wide					11 _b
		01 _b = 8 MCLK Wide					
		10 _b = 32 MCLK Wide					
		11 _b = Full Row Wide					
5 - 0	SOF Delay	Half cycles of delay = sof[5:0]					000000 _b

Table 36: SOF Control Register (54_h)**7.17 VCLK Control Register (55_h)**

The VCLK Control Register is used to define the size and position of the VCLK sync pulse. This adjust can be used to vary the sync positions relative to valid pixel data. Adjusting the position or length of the VCLK sync does NOT alter the frame rate, the sync signal is simply shifted and overlaps the valid line and pixel data. The delay adjust is in ½ cycles, it takes two programmed counts to delay the rising edge by one image pixel.

Address		VCLK Control					Default
55 _h							90 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)
vck[7]	vck[6]	vck[5]	vck[4]	vck[3]	vck[2]	vck[1]	vck[0]
Bit Number	Function	Description					Reset State
7 - 6	VCLK Control	00 _b = 1 MCLK Wide					10 _b
		01 _b = 8 MCLK Wide					
		10 _b = 32 MCLK Wide					
		11 _b = Full Row Wide					
5 - 0	VCLK Delay	Half cycles of delay = vck[5:0]					010000 _b

Table 37: VCLK Control Register (55_h)



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7.18 Internal Timing Control Register (60h)

These registers are used to define the size of internal timing pulse widths shA (sample & hold sample) and shB (sample & hold reset). In default, both are 10 MCLKs wide. A maximum of 16 MCLKs can be programmed for the shA delay and another 16 MCLKs for the shB delay. Writing 00h to either register will provide the maximum timing delay of 32 MCLKs.

Address 60 _h		Internal Timing Control						Default 66 _h
7 (msb)	6	5	4	3	2	1	0 (lsb)	
shA[3]	shA[2]	shA[1]	shA[0]	shB[3]	shB[2]	shB[1]	shB[0]	
Bit Number	Function	Description						Reset State
7	shA	shA[3:0]=0000b=16 MCLKs Wide shA[3:0]=0001b=1d MCLKs Wide shA[3:0]=0010b=2d MCLKs Wide shA[3:0]=0011b=3d MCLKs Wide shA[3:0]=1111b=15d MCLKs Wide						0110b
5 - 0	shB	shB[3:0]=0000b=16 MCLKs Wide shB[3:0]=0001b=1d MCLKs Wide shB[3:0]=0010b=2d MCLKs Wide shB[3:0]=0011b=3d MCLKs Wide shB[3:0]=1111b=15d MCLKs Wide						0110b

Table 38: Internal Timing Control Register (60_h)



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8 I²C Serial Interface

The I²C is an industry standard which is also compatible with the Motorola bus (called M-Bus) that is available on many microprocessor products. The I²C contains a serial two-wire half-duplex interface that features bi-directional operation, master or slave modes, and multi-master environment support. The clock frequency on the system is governed by the slowest device on the board. The SDATA and SCLK are the bi-directional data and clock pins, respectively. These pins are open drain and will require a pull-up resistor to VDD of 1.5 K Ω to 10K Ω .

The I²C is used to write the required user system data into the Program Control Registers in the KAC-0311. The I²C bus can also read the data in the Program Control Register for verification or test considerations. The KAC-0311 is a slave only device that supports a maximum clock rate (SCLK) of 100 kHz while reading or writing only one register address per I²C start/stop cycle. The following sections will be limited to the methods for writing and reading data into the KAC-0311 register.

For a complete reference to I²C, see "The I²C Bus from Theory to Practice" by Dominique Paret and Carll-Fenger, published by John Wiley & Sons, ISBN 0471962686.

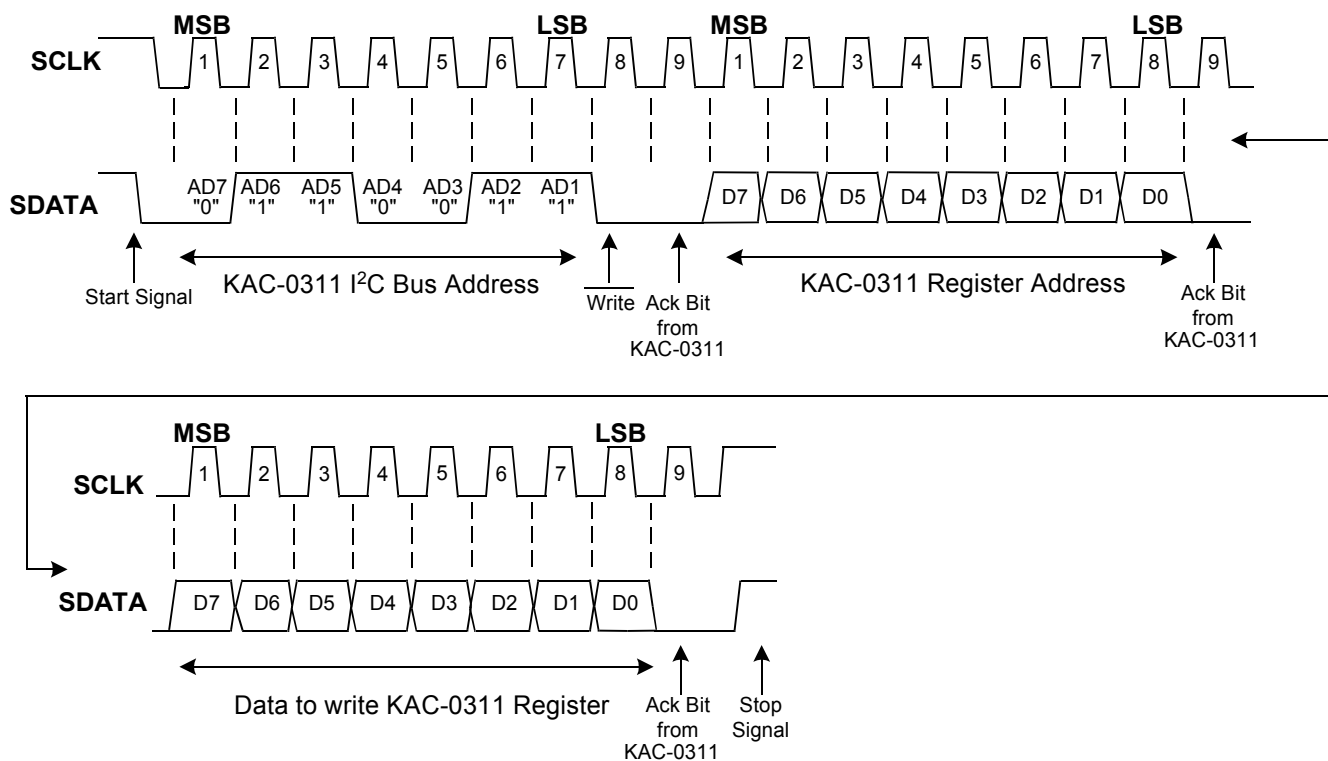


Figure 20: I²C Bus WRITE Cycle

**Kodak Digital Science KAC-0311 Image Sensor****8.1 KAC-0311 I²C Bus Protocol**

The KAC-0311 uses the I²C bus to write or read one register byte per start/stop I²C cycle as shown in Figure 20 and Figure 20. These figures will be used to describe the various parts of the I²C protocol communications as it applies to the KAC-0311. KAC-0311 I²C bus communication is basically composed of following parts: START signal, KAC-0311 slave address (0110011_b) transmission followed by a R/W bit, an acknowledgment signal from the slave, 8-bit data transfer followed by another acknowledgment signal, STOP signal, Repeated START signal, and clock synchronization.

8.2 START Signal

When the bus is free, i.e. no master device is engaging the bus (both SCLK and SDATA lines are at logical “1”), a master may initiate communication by sending a START signal. As shown in Figure 19, a START signal is defined as a high-to-low transition of SDATA while SCLK is high. This signal denotes the beginning of a new data transfer and wakes up all the slaves on the bus.

8.3 Slave Address Transmission

The first byte of a data transfer, immediately after the START signal, is the slave address transmitted by the master. This is a 7-bit calling address followed by a R/W bit. The 7-bit address for the KAC-0311, starting with the MSB (AD7), is 0110011_b. The transmitted calling address on the SDATA line may only be changed while SCLK is low as shown in Figure 20. The data on the SDATA line is valid on the High to Low signal transition on the SCLK line. The R/W bit following the 7-bits tells the slave the desired direction of data transfer: 1 = Read transfer, the slave transitions to a slave transmitter and sends the data to the master; 0 = Write transfer, the master transmits data to the slave.

8.4 Acknowledgment

Only the slave with a calling address that matches the one transmitted by the master will respond by sending back an acknowledge bit. This is done by pulling the SDATA line low at the 9th clock (see Figure 20). If an acknowledgement is not received, many I²C master devices will assume that the slave device is not functioning. No two slaves in the system may have the same address. The KAC-0311 is configured to be a slave only.

8.5 Data Transfer

Once successful slave addressing is achieved, data transfer can proceed between the master and the selected slave in a direction specified by the R/W bit sent by the calling master. Note that for the first byte after a start signal (in Figure 20 and Figure 20), the R/W bit is always a “0” designating a write transfer. This is required since the next data transfer will contain the register address to be read or written. All transfers that come after a calling address cycle are referred to as data transfers, even if they carry sub-address information for the slave device. Each data byte is 8 bits long. Data may be changed only while SCLK is low and must be held stable while SCLK is high as shown in Figure 20. There is one clock pulse on SCLK for each data bit, the MSB being transferred first.

Each data byte has to be followed by an acknowledge bit, which is signaled from the receiving device by pulling the SDATA line low at the ninth clock. So one complete data byte transfer needs nine clock pulses. If the slave receiver does not acknowledge the master, the SDATA line must be left high by the slave. The master can then generate a stop signal to abort the data transfer or a start signal (repeated start) to commence a new calling. If the master receiver does not acknowledge the slave transmitter after a byte transmission, it means 'end of data' to the slave, so the slave releases the SDATA line for the master to generate STOP or START signal.

**Kodak Digital Science KAC-0311 Image Sensor****8.6 Stop Signal**

The master can terminate the communication by generating a STOP signal to free the bus. However, the master may generate a START signal followed by a calling command without generating a STOP signal first. This is called a Repeated START. A STOP signal is defined as a low-to-high transition of SDATA while SCLK is at logical "1" (see Figure 20). The master can generate a STOP even if the slave has generated an acknowledge bit at which point the slave must release the bus.

8.7 Repeated START Signal

A Repeated START signal is a START signal generated without first generating a STOP signal to terminate the communication. This is used by the master to communicate with another slave or with the same slave in a different mode (transmit/receive mode) without releasing the bus. As shown in Fig. 20, pg 49, a Repeated START signal is being used during the read cycle and to redirect the data transfer from a write cycle (master transmits the register address to the slave) to a read cycle (slave transmits the data from the designated register to the slave).

8.8 I²C Bus Clocking and Synchronization

Open drain outputs are used on the SCLK outputs of all master and slave devices so that the clock can be synchronized and stretched using wire-AND logic. This means that the slowest device will keep the bus from going faster than it is capable of receiving or transmitting data.

After the master has driven SCLK from High to Low, all the slaves drive SCLK Low for the required period that is needed by each slave device and then releases the SCLK bus. If the slave SCLK Low period is greater than the master SCLK Low period, the resulting SCLK bus signal Low period is stretched. Therefore, synchronized clocking occurs since the SCLK is held low by the device with the longest Low period. Also, this method can be used by the slaves to slow down the bit rate of a transfer. The master controls the length of time that the SCLK line is in the High state. The data on the SDATA line is valid when the master switches the SCLK line from a High to a Low. Slave devices may hold the SCLK low after completion of one byte transfer (9 bits). In such case, it halts the bus clock and forces the master clock into wait states until the slave releases the SCLK line.

8.9 Register Write

- Writing the KAC-0311 registers is accomplished with the following I²C transactions (see Figure 20 pg 45):
- Master transmits a START
- Master transmits the KAC-0311 Slave Calling Address with "WRITE" indicated (BYTE=66_b, 102_d, 01100110_b)
- KAC-0311 slave sends acknowledgment by forcing the SDATA Low during the 9th clock, if the Calling Address was received
- Master transmits the KAC-0311 Register Address
- KAC-0311 slave sends acknowledgment by forcing the SDATA Low during the 9th clock after receiving the Register Address
- Master transmits the data to be written into the register at the previously received Register Address
- KAC-0311 slave sends acknowledgment by forcing the SDATA Low during the 9th clock after receiving the data to be written into the Register Address
- The Master transmits STOP to end the write cycle



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8.10 Register Read

Reading the KAC-0311 registers is accomplished with the following I²C transactions (see Figure 20, pg 49):

- Master transmits a START
- Master transmits the KAC-0311 Slave Calling Address with “WRITE” indicated (BYTE=66_b, 102_d, 01100110_b)
- KAC-0311 slave sends acknowledgment by forcing the SDATA Low during the 9th clock, if the Calling Address was received
- Master transmits the KAC-0311 Register Address
- KAC-0311 slave sends acknowledgment by forcing the SDATA Low during the 9th clock after receiving the Register Address
- Master transmits a Repeated START
- Master transmits the KAC-0311 Slave Calling Address with “READ” indicated (BYTE = 67_b, 103_d, 01100111_b)
- KAC-0311 slave sends acknowledgment by forcing the SDATA Low during the 9th clock, if the Calling Address was received
- At this point, the KAC-0311 transitions from a “Slave-Receiver” to a “Slave-Transmitter”
- KAC-0311 sends the SCLK and the Register Data contained in the Register Address that was previously received from the master; KAC-0311 transitions to slave-receiver
- Master does not send an acknowledgment (NAK)
- Master transmits STOP to end the read cycle



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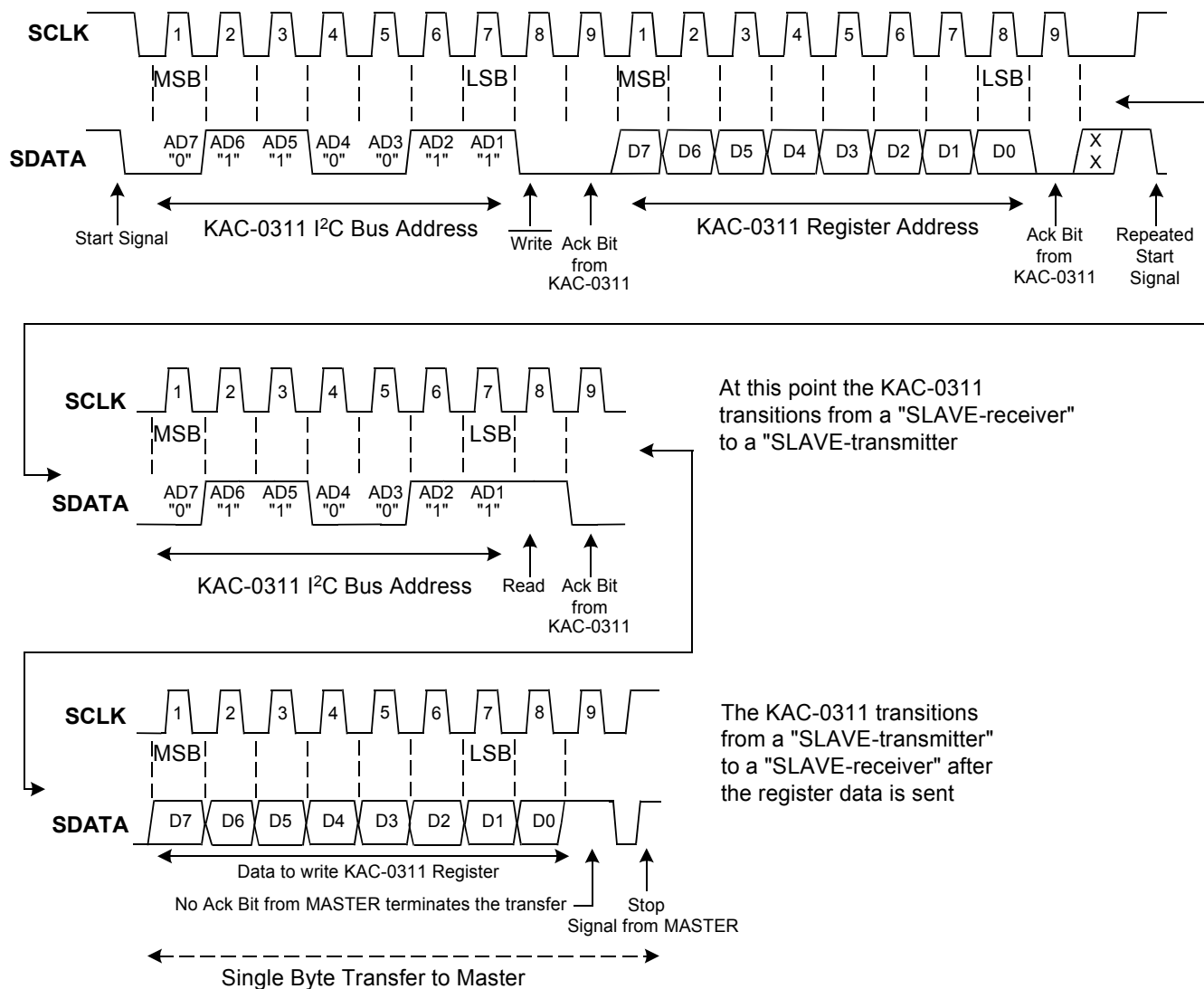


Figure 21: I²C Bus READ Cycle



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9 Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to VSS)			
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to 3.8	V
V_{in}	DC Input Voltage	0.5 to $V_{DD} + 0.5$	V
V_{out}	DC Output Voltage	-0.5 to $V_{DD} + 0.5$	V
I	DC Current Drain per Pin, Any Single Input or Output	± 50	mA
I	DC Current Drain, V_{DD} and V_{SS} Pins	± 100	mA
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature (10 second soldering)	300	°C

Voltages referenced to VSS

Maximum Ratings are those values beyond which damage to the device may occur.

$V_{SS} = AV_{SS} = DV_{SS} = V_{SSO}$ ($DV_{SS} = V_{SS}$ of Digital circuit, $AV_{SS} = V_{SS}$ of Analog Circuit)

$V_{DD} = AV_{DD} = DV_{DD} = V_{DDO}$ ($DV_{DD} = V_{DD}$ of Digital circuit, $AV_{DD} = V_{DD}$ of Analog Circuit)

RECOMMENDED OPERATING CONDITIONS (to guarantee functionality; voltage referenced to VSS)				
Symbol	Parameter	Min	Max	Unit
V_{DD}	DC Supply Voltage, $V_{DD} = 3.3V$ (Nominal)	3.0	3.6	V
T_A	Commercial Operating Temperature	0	40	°C
T_J	Junction Temperature	0	55	°C

Notes:

- All parameters are characterized for DC conditions after thermal equilibrium has been established.
- Unused inputs must always be tied to an appropriate logic level, e.g., either VSS or VDD.
- For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$.

DC ELECTRICAL CHARACTERISTICS ($V_{DD} = 3.3V \pm 0.3V$; V_{DD} referenced to V_{SS} ; $T_a = 0^\circ C$ to $40^\circ C$)					
Symbol	Characteristic	Condition	$T_A = 0^\circ C$ to $40^\circ C$		Unit
			Min	Max	
V_{IH}	Input High Voltage		2.0	$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3	0.8	V
I_{in}	Input Leakage Current, No Pull-up Resistor	$V_{in} = V_{DD}$ or V_{SS}	-5	5	μA
I_{OH}	Output High Current	$V_{DD} = \text{Min}$, $V_{OH} \text{ Min} = 0.8 * V_{DD}$	-3		mA
I_{OL}	Output Low Current	$V_{DD} = \text{Min}$, $V_{OL} \text{ Max} = 0.4V$	3		mA
V_{OH}	Output High Voltage	$V_{DD} = \text{Min}$, $I_{OH} = -100\mu A$	$V_{DD} - 0.2$		V
V_{OL}	Output Low Voltage	$V_{DD} = \text{Min}$, $I_{OL} = 100\mu A$		0.2	V
I_{OZ}	3-State Output Leakage Current	Output = High Impedance, $V_{out} = V_{DD}$ or V_{SS}	-10	10	μA
I_{DD}	Maximum Standby Supply Current	$I_{out} = 0mA$, $V_{in} = V_{DD}$ or V_{SS}	0	15	mA



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POWER DISSIPATION (VDD = 3.0V, VDD referenced to VSS; At = 25 C				
Symbol	Parameter	Condition	Typ	Unit
P _{DYN}	Dynamic Power	13.5 MHz MCLK Clock frequency	400	mW
P _{STDBY}	Standby Power	STDBY Pin Logic High	50	mW
P _{AVG}	Average Power	13.5 MHz Operation (using STDBY)	200	mW

V_{DD} = 3.0V, V_{DD} referenced to V_{SS}, 25 °C

KAC-0311 MONOCHROME CMOS IMAGE SENSOR ELECTRO-OPTICAL CHARACTERISTICS				
Symbol	Parameter	Typ	Unit	Notes
E _{sat}	Saturation Exposure	0.14	μJ/cm ²	1
QE	Peak Quantum Efficiency (@550nm)	23	%	2
PRNU	Photoresponse Non-uniformity	12	% pk-pk	3
	Sensitivity	5.0	V/lux-sec	
		58,000	e/Lux-Sec	
I _d	Photodiode Dark Current	0.2	nA/cm ²	
DSNU	Dark Signal Non-Uniformity (Entire Field)	0.4	% rms	
Lag	Pixel Charge Transfer Efficiency	<1	%	4
X _{ab}	Blooming Margin - shuttered light	200		5,6,7

Notes:

1. For wavelength = 550 nm .
2. Refer to typical values from figure 3, KAC-0311 nominal spectral response.
3. For a 100 x 100 pixel region under uniform illumination with output signal equal to 80% of saturation signal.
4. Transfer efficiency of photosite.
5. X_{ab} represents the increase above the saturation-irradiance level (H_{sat}) that the device can be exposed to before blooming for the pixel will occur.
6. No column streaking.
7. At 30fps VGA.

KAC-0311 COLOR CMOS IMAGE SENSOR ELECTRO-OPTICAL CHARACTERISTICS				
Symbol	Parameter	Typ	Unit	Notes
Esat	Saturation Exposure	0.3	μJ/cm ²	1
QE _r	Red Peak Quantum Efficiency @ λ = 650 nm	12	%	2
QE _g	Green Peak Quantum Efficiency @ λ = 550 nm	11	%	2
QE _b	Blue Peak Quantum Efficiency @ λ = 450 nm	8	%	2

Notes:

1. For λ = 550 nm.
2. Refer to typical values from figure 3, KAC-0311 nominal spectral response.



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I ² C SERIAL INTERFACE ⁶ TIMING SPECIFICATIONS				
Symbol	Characteristic	Min	Max	Unit
f _{max}	SCLK maximum frequency	50	1/24 MCLK	KHz
M1	Start condition SCLK hold time	4	-	T _{MCLK} ⁷
M2	SCLK low period	8	-	T _{MCLK}
M3	SCLK/SDATA rise time [from V _{IL} = (0.2)*V _{DD} to V _{IH} = (0.8)*V _{DD}]	-	0.3	μs ⁸
M4	SDATA hold time	4	-	T _{MCLK} ⁷
M5	SCLK/SDATA fall time (from V _H = 2.4V to V _L = 0.5V)	-	0.3	μs ⁸
M6	SCLK high period	4	-	T _{MCLK}
M7	SDATA setup time	4	-	T _{MCLK} ⁷
M8	Start / Repeated Start condition SCLK setup time	4	-	T _{MCLK}
M9	Stop condition SCLK setup time	4	-	T _{MCLK}
C ₁	Capacitive for each I/O pin	-	10	pF
C _{bus}	Capacitive bus load for SCLK and SDATA	-	200	pF
R _p	Pull-up Resistor on SCLK and SDATA	1.5	10	kΩ ⁹

Notes:

⁶ I²C is a proprietary Philips interface bus.

⁷ The unit T_{MCLK} is the period of the input master clock; the frequency of MCLK is assumed 13.5 MHz.

⁸ The capacitive load is 200 pF

⁹ A pull-up resistor to VDD is required on each of the SCLK and SDATA lines; for a maximum bus capacitive load of 200pF, the minimum value of R_p should be selected in order to meet specifications.

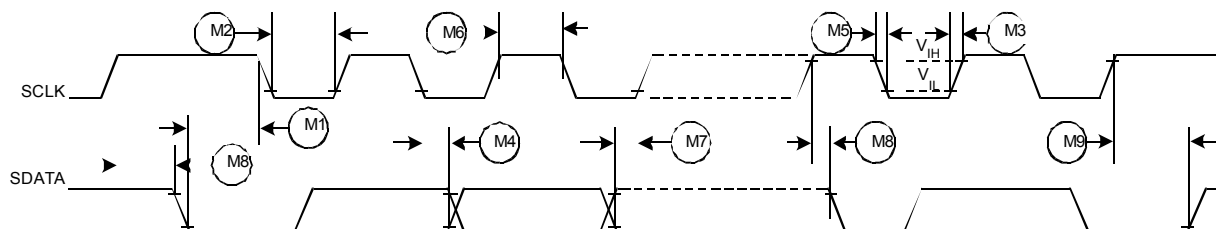


Figure 22: I²C Bus Timing



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PIXEL DATA BUS INTERFACE TIMING SPECIFICATIONS (see Figure 22)					
Symbol	Characteristic	Min	Typ	Max	Unit
$f_{\max}$	MCLK maximum frequency	1	11.5	13.5	MHz
t_{hsync}	SYNC hold time w.r.t. MCLK	3.5	-	9	ns
t_{susync}	SYNC setup time w.r.t. MCLK	3.0	-	8.5	ns
t_{dsof}	MCLK to SOF delay time	8	13	21.5	ns
t_{dvclk}	MCLK to VCLK delay time	8.5	13.5	22	ns
t_{drhclk}	Rising edge of MCLK to rising edge of HCLK delay time	7.5	13	22	ns
t_{dfhclk}	Falling edge of MCLK to falling edge of HCLK delay time	3	5	10.5	ns
t_{dadc}	MCLK to ADC[9:0] delay time	8	13	21.5	ns
t_{dblank}	MCLK to BLANK delay time	8	13	21.5	ns

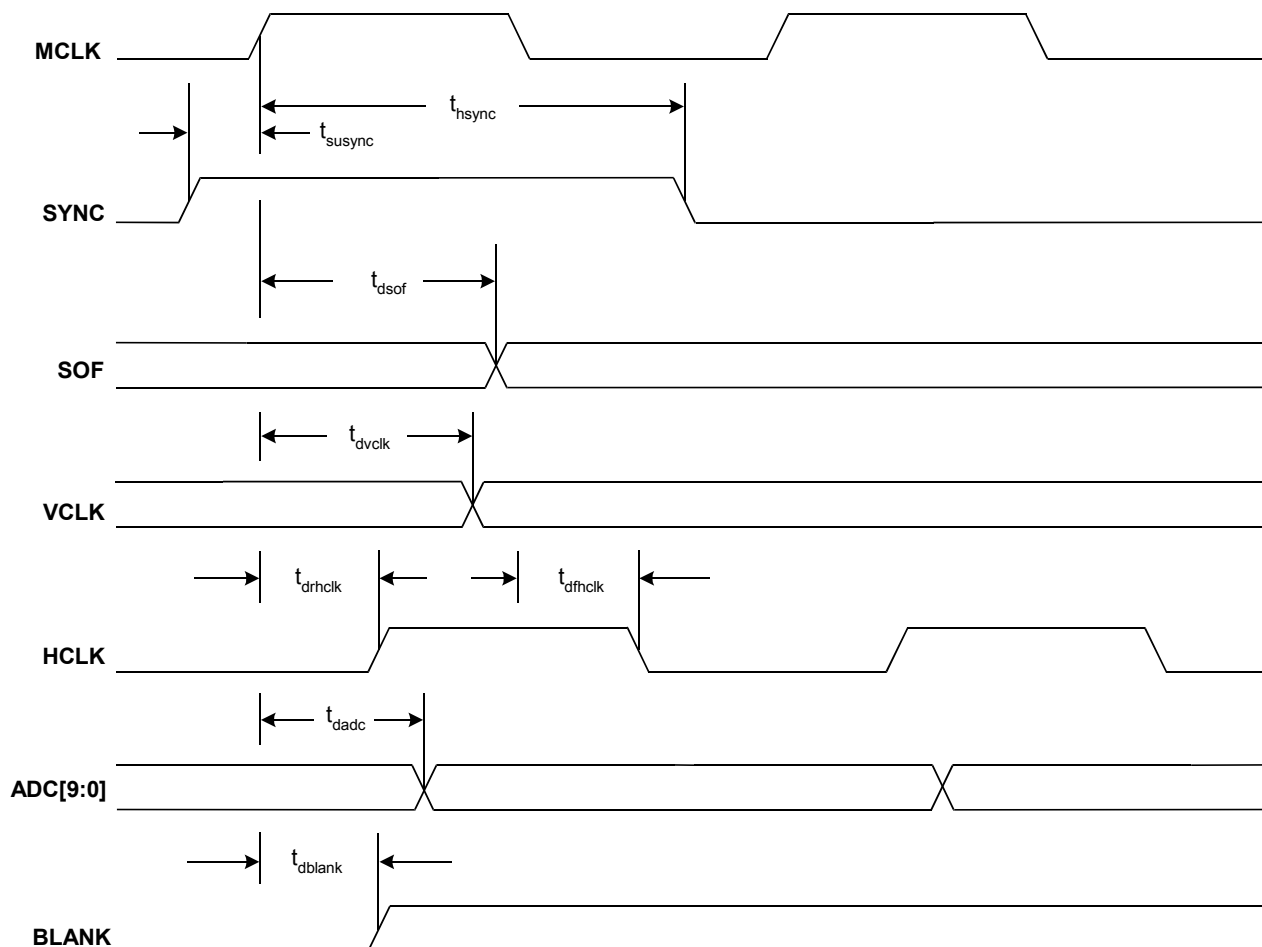
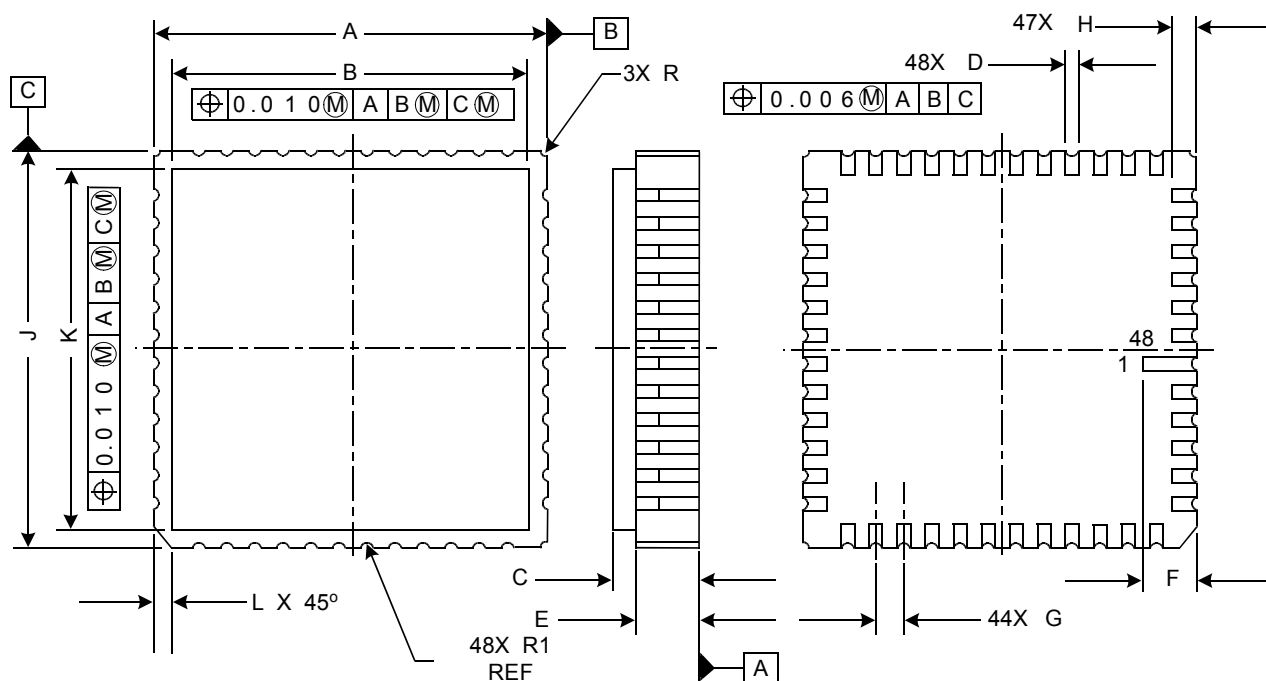


Figure 23: Pixel Data Bus Timing Diagram

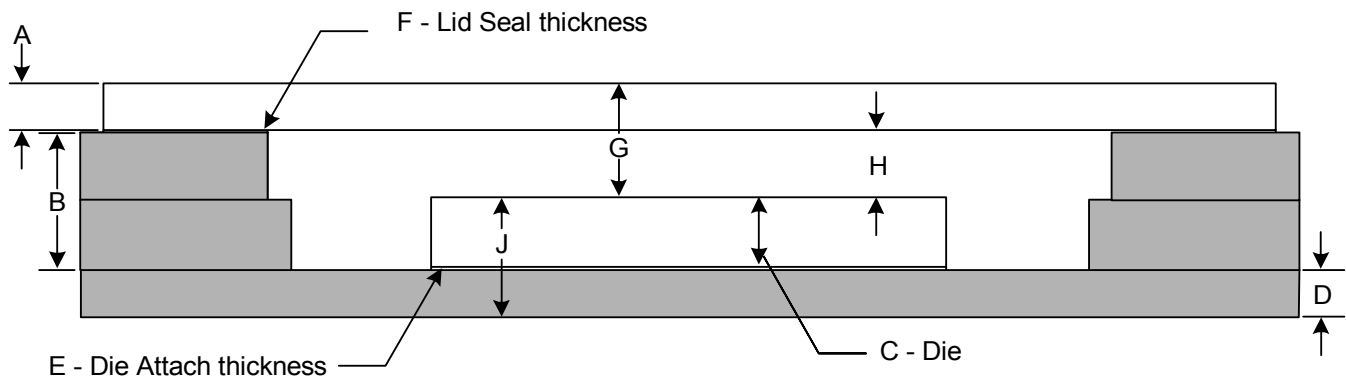


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Dim	Min(Mils)	Max(mils)
A	0.555	0.572
B	0.525	0.545
C	---	0.120
D	0.016	0.024
E	0.067	0.083
F	0.075	0.095
G	0.040 BSC	
H	0.033	0.047
J	0.555	0.572
K	0.525	0.545
L	0.028 REF	
R	0.028 REF	
R1	0.028 REF	

Figure 24: 48 Terminal ceramic leadless chip carrier

**Kodak Digital Science KAC-0311 Image Sensor****48 Ceramic LCC - Matrix Format (all dim in mm)**

Dimension	Description	Nominal	Min	Max
A	Glass (Thickness)	0.55	0.5	0.6
B	Cavity (Depth)	1.27	1.143	1.397
C	Die - Si (Thickness)	0.725	0.705	0.745
D	Bottom Layer (Thickness)	0.635	0.5588	0.7112
E	Die Attach - bondline (Thickness)	0.0254	0.0127	0.0762
F	Glass Attach - bondline (Thickness)	0.0254	0.0127	0.0508

Figure 25: Focal plane with respect to package



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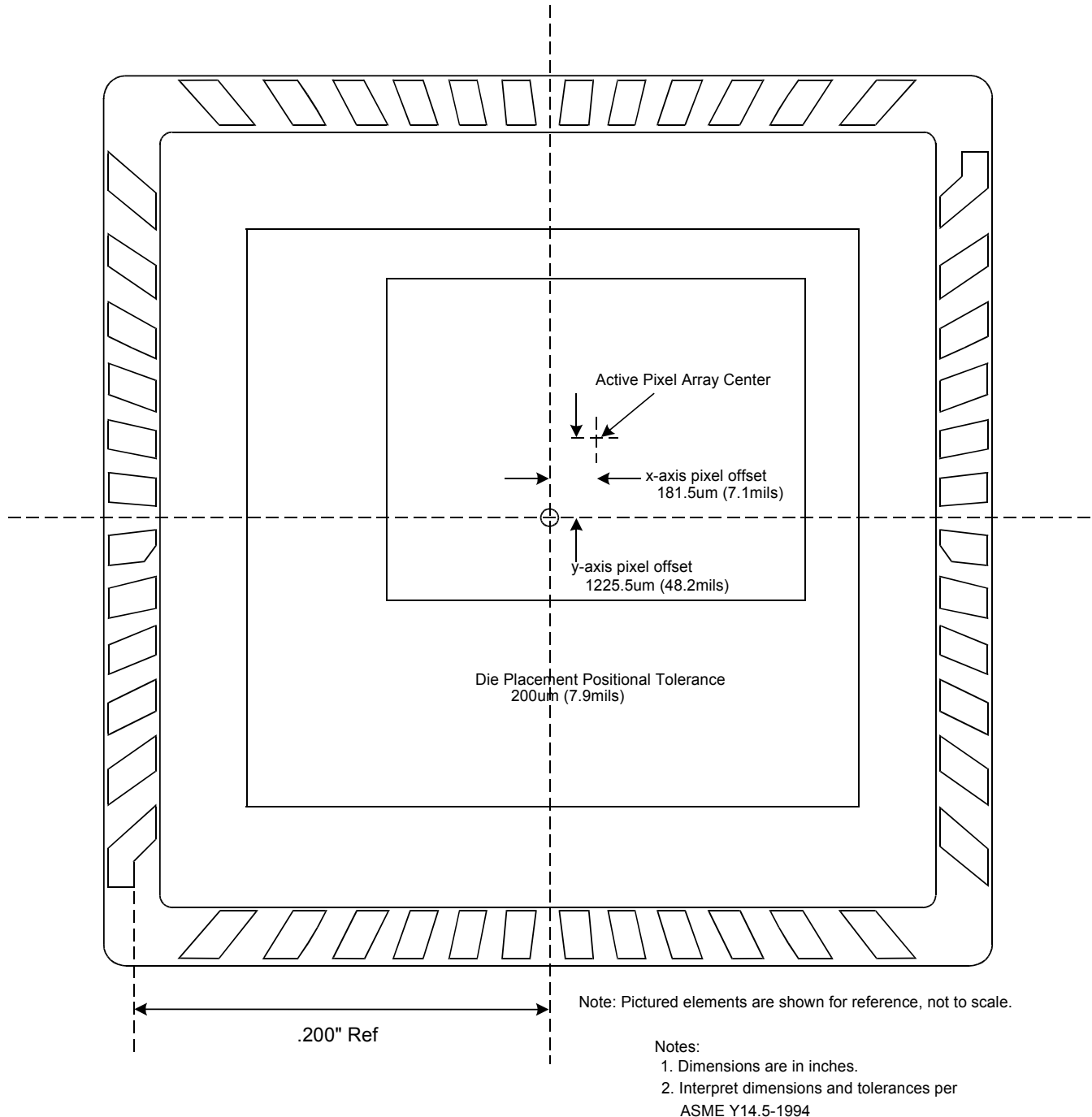


Figure 26: Center of the focal plane array with respect to the die cavity (top view)