

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC. and
PENSANDO SYSTEMS, INC.,
Petitioner,

v.

XTREAMEDGE, INC.,
Patent Owner.

IPR2025-00223
Patent 10,985,943 B1

Before KARL D. EASTHOM, JUSTIN T. ARBES, and
IFTIKHAR AHMED, *Administrative Patent Judges*.

AHMED, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Advanced Micro Devices, Inc. and Pensando Systems, Inc. (collectively, “Petitioner”) filed a Petition for *inter partes* review of claims 1–18 (the “Challenged Claims”) of U.S. Patent No. 10,985,943 B1 (Ex. 1001, “the ’943 patent”). Paper 2 (“Pet.”). XtreamEdge, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”). The Petition was referred to the Board. Paper 12.

We have authority to determine whether to institute an *inter partes* review. *See* 35 U.S.C. § 314 (2018); 37 C.F.R. § 42.4(a) (2022). To institute an *inter partes* review, we must determine that the information presented in the Petition shows “a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). Based on the information presented in the Petition and the supporting evidence, we are persuaded that there is a reasonable likelihood that Petitioner would prevail with respect to at least one of the challenged claims. Accordingly, we institute an *inter partes* review of the challenged claims on the grounds set forth in the Petition.

II. BACKGROUND

A. *Real Parties in Interest*

Petitioner identifies itself, Advanced Micro Devices, Inc. and Pensando Systems, Inc., as the real parties in interest. Pet. 98. Patent Owner identifies itself, XtreamEdge, Inc., as well as Concurrent Ventures, LLC, as the real parties in interest. Paper 4, 2.

B. Related Matter

The parties identify the following proceeding as a related matter involving the '943 patent: *Concurrent Ventures, LLC v. Advanced Micro Devices, Inc.*, 1:24-cv-00335 (W.D. Tex.). Pet. 98; Paper 4, 2.

C. The '943 patent

The '943 patent, titled “Hardware Defined Anything in a Platform with Swappable Pods, Message Interface, Sandboxes and Memory Superposition,” issued on April 20, 2021, with claims 1–18. Ex. 1001, codes (45), (54), 17:39–19:7. The '943 patent discloses a chassis server with “hardware-defined and software-defined functionality in data streaming and data processing systems,” where various “[p]ods and cards are removable, insertable, replaceable and optionally hot-swappable in the chassis.” *Id.* at 2:49–57. In particular, an “FPGA (field programmable gate array), PLD (programmable logic device), ASIC (application specific integrated circuit), or some hybrid of FPGA/PLD/ASIC, which can be used in pods and cards, has a bridge with an MMI [(Module Message Interface)] router, and one or more sandboxes for user-defined electronic circuits, optionally including processors.” *Id.* at 3:8–13.

Figure 3 illustrates a block diagram of a programmable device, and is reproduced below.

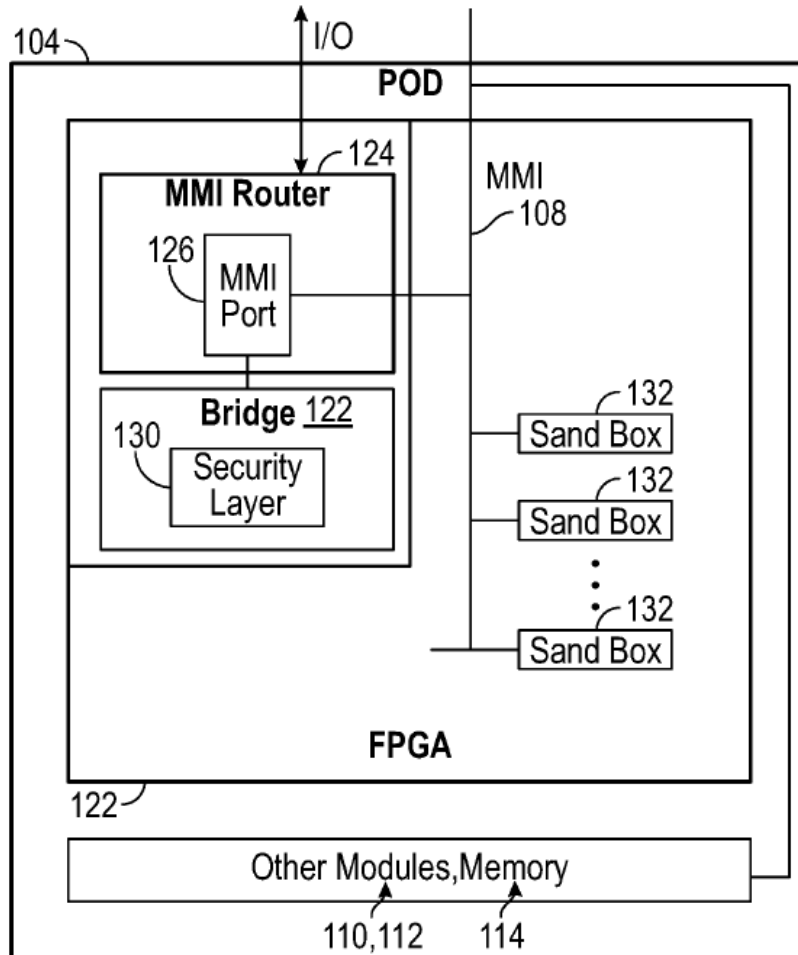


FIG. 3

As shown in Figure 3, the programmable device may be FPGA 122 in pod 104, but it could also be “a PLD or an ASIC, or more than one of these, or some combination of these.” Ex. 1001, 4:30–33. FPGA 122 includes “Module Message Interface router 124, a bridge 128¹, and sandboxes 132 for configurable modules.” *Id.* at 4:27–30. Bridge 128 may contain security

¹ According to Patent Owner, Bridge 128 is mislabeled as Bridge 122 in Figure 3. Prelim. Resp. 4 n.2.

layer 130 that may be “a firewall for MMI message traffic policies.” *Id.* at 4:60–62. Further, security layer 130 could be used “to protect the circuitry of the bridge, including the MMI router 124 in embodiments that have one, from being reprogrammed,” and for “authentication of a user or other verification of permission to reconfigure a sandbox 132.” *Id.* at 5:40–45. Bridge 128 may be “locked to prevent user access, in an FPGA 122 that supports partial reconfiguration, so that a user can configure or reconfigure one or more modules in one or more sandboxes 132, but cannot reconfigure the bridge 128.” *Id.* at 5:30–34.

D. Challenged Claims

Petitioner challenges claims 1–18 of the ’943 patent. Claims 1 and 10 are independent. Claim 1 is illustrative of the claimed subject matter and is reproduced below:

1. [pre] A programmable device for data flow processing in a user-configurable server with swappable pods or cards, comprising:
 - [a] a programmable logic device (PLD) having a first region and a second region;
 - [b] the first region comprising a hardware-based or firmware-based router with a port enabling communication between the router and the second region; and
 - [c] the second region comprising one or more sandboxes with user-definable programmable electronic circuits of the PLD,
 - [d] wherein the port comprises: a bridge being lockable to prevent user access, and unlockable to enable user access, to each of the sandboxes and the user-definable programmable electronic circuits therein.

Ex. 1001, 17:39–53 (Petitioner’s bracketed designations added); Pet. 100.

E. Asserted Grounds of Unpatentability

Petitioner contends that the challenged claims are unpatentable based on the following grounds:

Claim(s) Challenged	35 U.S.C. §²	Reference(s)/Basis
1–5, 10–14	103	Seshadri ³
1–5, 9–14, 18	103	Seshadri, Biederman ⁴
1–5, 10–14	103	Atsatt-113 ⁵
1–5, 9–14, 18	103	Atsatt-113, Beiderman
6, 15	103	Grounds 1–4, ⁶ Tarafdar ⁷
7, 16	103	Grounds 1–4, Kulkarni ⁸
8, 17	103	Grounds 1–4, Atsatt-923 ⁹

Pet. 16. Petitioner offers declaration testimony of Dr. Donald Alpert in support of its contentions. Ex. 1003.

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 285–88 (2011), amended 35 U.S.C. § 103 effective March 16, 2013. Because the challenged claims of the ’943 patent have an effective filing date after March 16, 2013, patentability is governed by the AIA version of § 103. *See* Ex. 1001, code (22).

³ U.S. Patent No. US 10,776,142 B1, filed on Dec. 13, 2017, issued on Sep. 15, 2020 (Ex. 1004, “Seshadri”).

⁴ U.S. Patent Publication No. US 2018/0191642 A1, published on July 5, 2018 (Ex. 1005, “Biederman”).

⁵ U.S. Patent Publication No. US 2019/0095113 A1, filed on Sep. 28, 2017, published on Mar. 28, 2019 (Ex. 1006, “Atsatt-113”).

⁶ For ease of reference, we use this format for listing Petitioner’s asserted grounds, consistent with the Petition. *See* Pet. 16. Each of Petitioner’s additional grounds based in part on “Grounds 1–4,” however, constitutes four separate grounds of unpatentability.

⁷ *Enabling Flexible Network FPGA Clusters in a Heterogeneous Cloud Data Center*, Proceedings of the 2017 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (February 2017) (Ex. 1007, “Tarafdar”). *See also* Ex. 1022 ¶ 9.

III. ANALYSIS

A. Legal Standards – Obviousness

A claim is unpatentable if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which said claimed invention pertains. 35 U.S.C. § 103; *see KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations, including commercial success, long-felt but unsolved needs, failure of others, and unexpected results.¹⁰ *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17–18 (1966).

When evaluating a combination of teachings, we must also “determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). “[T]here must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *Kahn*, 441 F.3d at 988.

“[W]here a party argues a skilled artisan would have been motivated to combine references, it must show the artisan ‘would have had a

⁸ U.S. Patent No. US 8,015,386 B1, issued on Sept. 6, 2011 (Ex. 1008, “Kulkarni”).

⁹ U.S. Patent Publication No. US 2019/0041923 A1, filed on Dec. 27, 2017, published on Feb. 7, 2019 (Ex. 1009, “Atsatt-923”).

¹⁰ The parties do not present arguments or evidence regarding objective indicia of non-obviousness.

reasonable expectation of success from doing so.” *Arctic Cat Inc. v. Bombardier Recreational Prods. Inc.*, 876 F.3d 1350, 1360–61 (Fed. Cir. 2017) (quoting *In re Cyclobenzaprine Hydrochloride Extended-Release Capsule Patent Litig.*, 676 F.3d 1063, 1068–69 (Fed. Cir. 2012)).

B. Level of Ordinary Skill in the Art

We review Petitioner’s asserted obviousness grounds in view of the understanding of a person of ordinary skill in the art at the time of the invention. *Graham*, 383 U.S. at 17. The person of ordinary skill in the art is a hypothetical person who is presumed to have known the relevant art at the time of the invention. *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995).

Petitioner contends that a person having ordinary skill in the art would have had “a bachelor’s degree in electrical engineering or a similar major with at least two years of experience in the field; or a master’s degree with specialization in the field.” Pet. 14 (citing Ex. 1003 ¶¶ 37–38). In addition, Petitioner asserts that “[a] person with less education but more relevant practical experience may also meet this standard.” *Id.*

Petitioner’s proposal is undisputed at this stage. *See generally* Prelim. Resp. For purposes of this Decision, and based on the current record, we adopt Petitioner’s assessment of the level of ordinary skill, except we decline to adopt “at least” as that language is vague and open-ended. Otherwise, we find, based on the preliminary record before us, that Petitioner’s proposed level of ordinary skill is consistent with the ’943 patent and the asserted prior art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *GPAC Inc.*, 57 F.3d at 1579.

C. Claim Construction

In *inter partes* reviews, the Board interprets claim language using the same standard as the district courts, as described in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 37 C.F.R. § 42.100(b) (2024). Under that standard, we generally give claim terms their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history. *See Phillips*, 415 F.3d at 1313–14.

Petitioner proposes a construction for the claim term “programmable logic device” as “an [Integrated Circuit] where the user can alter the connection pattern of the circuits,” but contends that for this *inter partes* review, the art asserted in each of Petitioner’s grounds teaches a “programmable logic device,” irrespective of whether that construction is adopted. Pet. 15 (citing Ex. 1001, 3:8–12,¹¹ 4:30–47; Ex. 1002, 130–132; Ex. 1029, 18;¹² Ex. 1030, 14¹³). At this juncture, Patent Owner does not propose express constructions for any claim terms. *See generally* Prelim. Resp.

For purposes of this Decision, we determine that no claim terms require express construction. *See Realtime Data LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve

¹¹ Petitioner inadvertently cites to Exhibit 1004 instead of Exhibit 1001.

¹² We find a definition for “programmable logic device (PLD)” on page 17, rather than page 18, of this exhibit. Ex. 1029, 17.

¹³ We find a definition for “programmable logic devices” on page 15, rather than page 14, of this exhibit. Ex. 1030, 15.

the controversy.” (quoting *Vivid Techs., Inc. v. Am. Sci. Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

*D. Obviousness Based on Seshadri or
Seshadri and Biederman*

Petitioner asserts that claims 1–5 and 10–14 of the ’943 patent are unpatentable under 35 U.S.C. § 103 as obvious over Seshadri. Pet. 16. Petitioner also asserts that claims 1–5, 9–14, and 18 are unpatentable as obvious over Seshadri and Biederman. *Id.* Patent Owner argues that Seshadri does not teach certain limitations for which Petitioner relies upon this reference. Prelim. Resp. 8–19.

1. Scope and Content of the Prior Art

a) Seshadri

Seshadri is a U.S. patent application publication titled “Reconfiguring Programmable Hardware when a Virtual Machine is Active.” Ex. 1004, code (54). Seshadri relates to “configuring a configurable shell logic in a configurable computing system while a client virtual machine (VM) using the shell logic is active.” *Id.* at 1:66–2:2. The configurable shell logic includes a static shell and a reconfigurable shell, and the static shell handles requests from a “client virtual machine or a host that executes the client virtual machine, such as packet processing or memory access requests,” when the reconfigurable shell is being reconfigured. *Id.* at 2:6–22.

A block diagram of an exemplary computing system, reproduced below, is shown in Seshadri's Figure 2. Ex. 1004, 1:40–41.

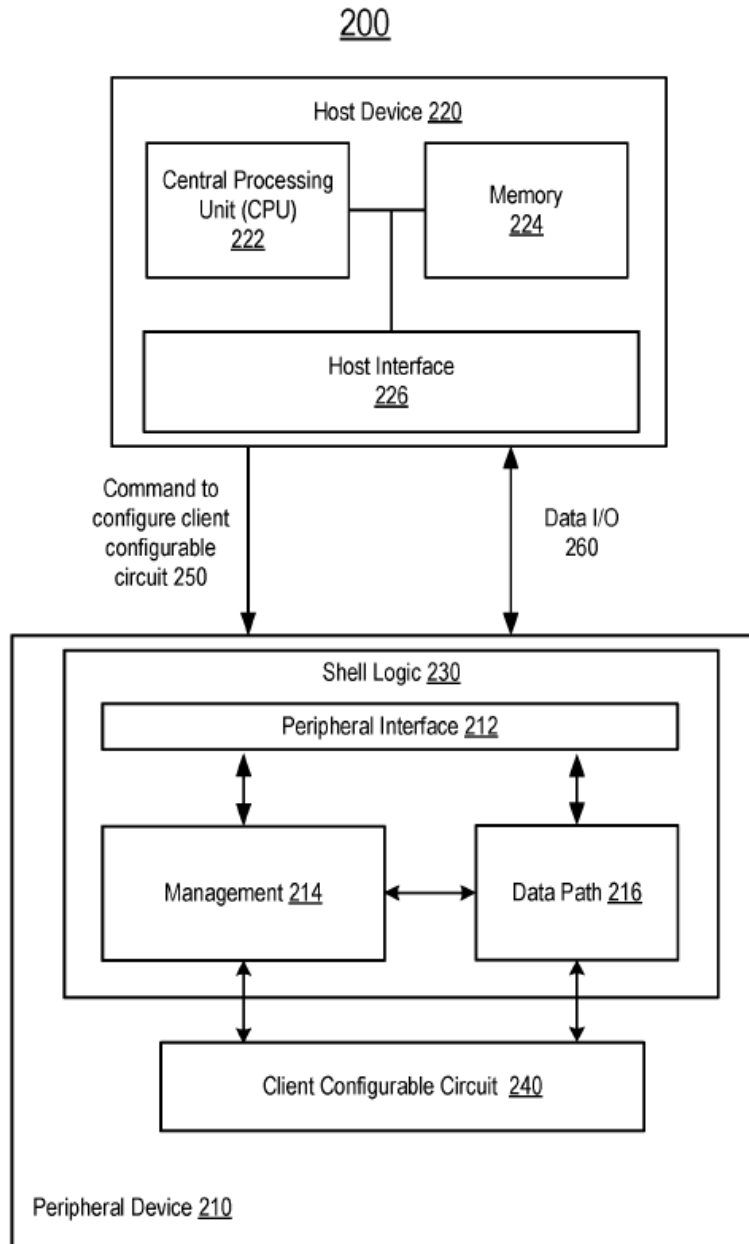


FIG. 2

Figure 2 shows computing system 200, which includes peripheral device 210 and host device 220, which may communicate via a “Peripheral Component Interconnect (PCI), PCI express (PCIe), or another physical interconnect that

couples” the two devices together. *Id.* at 7:16–19. “Peripheral device 210 may include a client configurable circuit 240 that may be used to implement a customer logic for the client.” *Id.* at 7:22–24. “Peripheral device 210 may also include a shell logic 230 for configuring and managing client configurable circuit 240.” *Id.* at 7:37–39. “Shell logic 230 can include logics that can isolate different components of peripheral device 210 or host device 220 from client configurable circuit 240.” *Id.* at 7:49–51.

In operation, security issues may arise when, for example, replacing first customer logic with second customer logic on the client configurable circuit, and replacing the existing reconfigurable shell logic with new shell logic to work with the second customer logic. Ex. 1004, 9:29–43. Namely, “the first customer logic may perform unauthorized operations if the reconfigurable shell is inactive because the reconfigurable shell is being replaced,” because “the protection logic within the reconfigurable shell may be temporarily inactive.” *Id.* at 9:43–47. To address this, a configuration sequence “can include deactivating at least a portion of the peripheral device used for the client virtual machine.” *Id.* at 9:65–10:1. “Existing customer logic within the client configurable circuit in the peripheral device can then be cleared or deactivated,” and, “[s]ubsequently, the reconfigurable shell can then be configured on the host configurable circuits, and the customer logic can be configured on the client configurable circuits and activated using the reconfigurable shell.” *Id.* at 10:5–11. “The portion of the peripheral device used for the client virtual machine can then be activated” *Id.* at 10:11–13.

Seshadri’s Figure 3, reproduced below, shows a block diagram of a computing system with details related to configuration of shell logic 340 and

client configurable circuit 350 in peripheral device 315. *See* Ex. 1004, 1:43–45; 10:16–19, 10:66–11:30, 13:19–39.

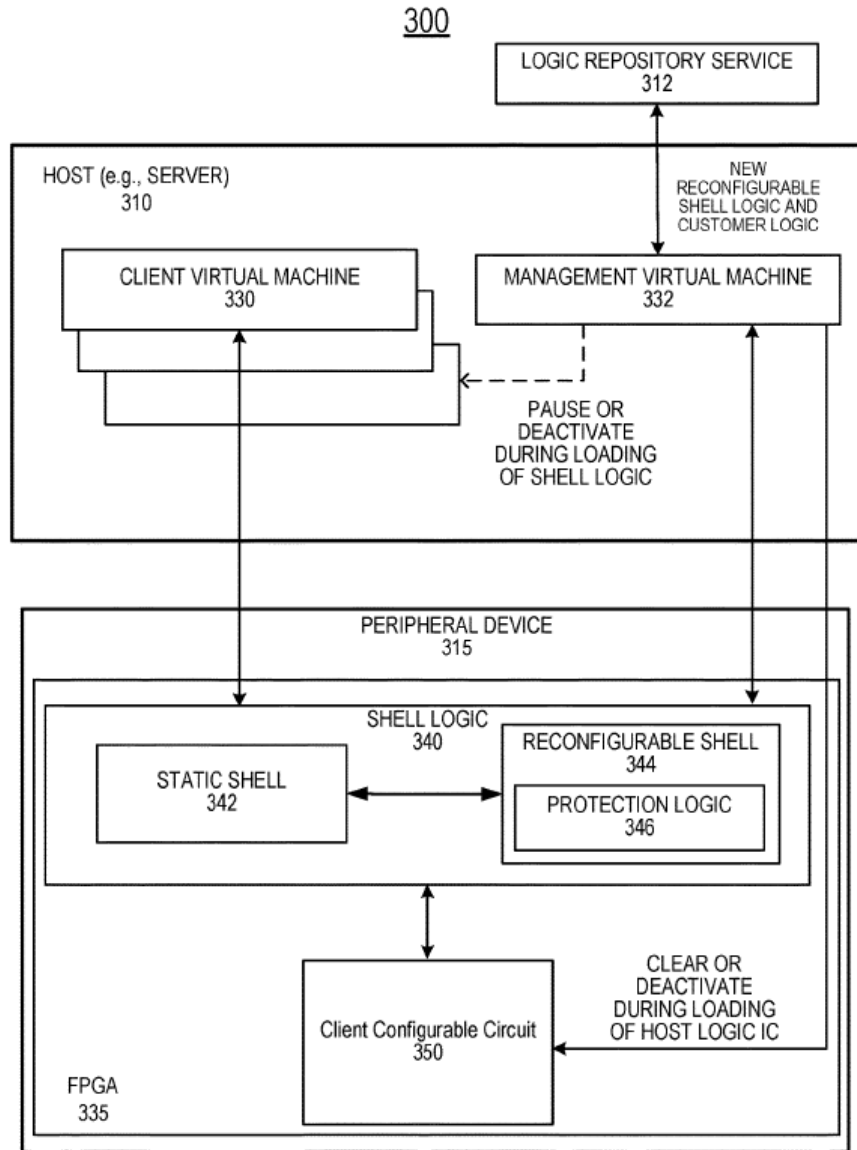


FIG. 3

In particular, as shown in Figure 3, “[s]hell logic 340 may provide encapsulation or sandboxing of client configurable circuit 350” and may include static shell 342 and reconfigurable shell 344. *Id.* at 11:4–9. Reconfigurable shell 344 may include “protection logic 346 for device

management and security enforcement.” *Id.* at 11:28–30. “[R]econfigurable shell 344 can be dynamically changed in response to one of the client virtual machines 330 requesting an update to the configurable logic within reconfigurable shell 344 and/or client configurable circuit 350.” *Id.* at 11:18–22. But, in order to close a potential security loophole, management virtual machine 332 in host 310 “may prevent the customer defined logic from communicating with other circuits of computing system 300,” for example, “by clearing or deactivating the customer defined logic during the reconfiguration or reprogramming of reconfigurable shell 344.” *Id.* at 13:19–25. In addition, “during the transition period, management virtual machine 332 may pause or deactivate client virtual machine 330,” and “[s]tatic shell 342 may remain active during the transition period to manage the reconfiguration of reconfigurable shell 344.” *Id.* at 13:26–30.

b) Biederman

Biederman is a U.S. patent application publication titled “Intelligent Packet Aggregation.” Ex. 1005, code (54). Biederman addresses the need for effective packet processing in a computer network at the network card level, “[b]y offloading some tasks from the CPU to a network interface device (NID),” so that “overall packet processing speed may be increased and streamlined.” *Id.* ¶¶ 2, 24. Biederman provides that “[t]he NID may be used as a centralized controller to handle packets and route them to the CPU, co-processors, application-specific integrated circuits (ASICs), or field-programmable gate arrays (FPGAs).” *Id.* ¶ 24. In an embodiment, an NID includes coordinator circuit 110, which “may interface with an FPGA 180 to determine its status, request a reconfiguration (or partial reconfiguration), or provide data for the FPGA 180 to act upon.” *Id.* ¶ 59. If a packet arrives at

the NID that “FPGA 180 is able to process, then it is referred to as a ‘FPGA hit’ in a manner similar to a cache hit.” *Id.* Coordinator circuit 110 interfaces with FPGA 180 “to reduce FPGA misses or increase FPGA hits.” *Id.* For example, in an embodiment, “coordinator circuit 110 may transmit a request to the FPGA 180 to determine the contents of the FPGA’s partitions,” “in conjunction with a FPGA interface controller 804.” *Id.* ¶ 126. Further, coordinator circuit 110 may use FPGA interface controller 804 to “load or unload FPGA programs in a partition that is controlled by the FGPA interface controller 804.” *Id.* ¶ 128.

2. Rationale to Combine Seshadri and Biederman

Petitioner contends that combining Seshadri with Biederman would have been a matter of “combin[ing] prior art elements according to known methods to yield” “the predictable result of partitioning the client-configurable circuit [of Seshadri] into distinct areas for customer logic from different users.” Pet. 34 (citing Ex. 1003 ¶ 100). This combination, according to Petitioner, would “serve[] more users with a smaller number of FPGAs, providing cost savings for cloud providers and reducing the entry barrier,” as well as “improve[] performance by reducing assignment switching of FPGAs.” *Id.* at 35 (citing Ex. 1003 ¶ 101). In addition, Petitioner asserts that this combination would have had a reasonable expectation of success because “Seshadri would still be used to sandbox client-configurable circuits in an FPGA” and “Biederman would still be used for partitioning.” *Id.* (citing Ex. 1003 ¶ 102).

Patent Owner does not specifically respond to these arguments. *See* Prelim. Resp. 19 n. 7. On the current record, Petitioner provides adequate reasoning, with rational underpinning, why an ordinarily skilled artisan

would have combined Biederman’s partitioned FPGA with Seshadri’s client configurable circuit in the manner proposed by Petitioner.

3. *Independent Claim 1*

- a) *Preamble 1[pre]: A programmable device for data flow processing in a user-configurable server with swappable pods or cards, comprising:*

Petitioner contends that Seshadri teaches using FPGAs “in a ‘configurable computing system’ with ‘configurable devices’ allowing remote users to load custom logic on the FPGAs to configure” “servers providing ‘networked computing resources.’” Pet. 20 (citing Ex. 1004, code (57), 1:7–22, 2:44–3:11, 10:36–65, 13:40–14:6, 20:67–21:4, Figs. 1, 2, 4, 8). Further, Petitioner contends that Seshadri discloses “swapping out FPGA cards and loading custom logic” on the servers. *Id.* at 21 (citing Ex. 1004, code (57), 2:60–3:11, 13:40–14:6; Ex. 1003 ¶ 66).

Patent Owner does not specifically respond to these arguments. *See* Prelim. Resp. Based on our review of the current record, at this stage of the proceeding, we determine that the information presented sufficiently supports Petitioner’s contentions relating to the preamble of claim 1.¹⁴

- b) *Limitation 1[a]: a programmable logic device (PLD) having a first region and a second region;*

Petitioner contends that “Seshadri discloses ‘programmable integrated circuits (ICs)’ that have a first ‘shell logic’ region and a second ‘client configurable circuit’ region.” Pet. 21 (citing Ex. 1004, 2:44–3:11, 10:36–47, Figs. 2–5; Ex. 1003 ¶ 69). In particular, Petitioner points to Seshadri’s Figure 5, which shows “functional blocks within the shell logic for

¹⁴ At this stage in the proceeding, we do not decide whether the preamble of claim 1 is limiting.

continuous operation during reconfiguration.” *Id.* at 22 (citing Ex. 1004, 1:40–51, 6:42–52, 10:16–11:30, 13:40–47, 16:61–17:15, Figs. 2– 5).

Patent Owner does not specifically respond to these arguments. *See generally* Prelim. Resp. Based on our review of the current record, at this stage of the proceeding, we determine that the information presented sufficiently supports Petitioner’s assertions as to this limitation.

c) Limitation 1[b]: the first region comprising a hardware-based or firmware-based router with a port enabling communication between the router and the second region; and

Petitioner contends that Seshadri’s “shell logic region includes functionality that ‘perform[s] bridging functions between the local interconnect (e.g., the PCIe interconnect) and the client configurable logic.’” Pet. 24 (citing Ex. 1004, 6:11–41). Petitioner further contends that Seshadri’s system “routes communication between the shell logic and the client-configurable circuit in order to convey messages to/from the host device.” *Id.* (citing Ex. 1004, 8:37–61, Fig. 2). Petitioner asserts that “Seshadri’s routing functionality further includes a port that enables communication with the second region,” for example, in the form of “management functions and the data-path, such as mailbox functionality through which messages are passed between the control plane (including shell logic) and data plane (including client-configurable circuits).” *Id.* at 25 (citing Ex. 1004, 12:32–49, 14:63–15:8). Petitioner also contends that the “router in the shell logic is hardware-based because it is implemented in the hardware programmable fabric[] of the FPGA.” *Id.* at 27 (citing Ex. 1004, 2:2–5, 3:24–27; Ex. 1003 ¶ 78).

Patent Owner responds that Petitioner has not shown that Seshadri discloses a hardware-based router. Prelim. Resp. 12–17. Patent Owner

argues that “the mere fact that something is ‘implemented’ in hardware does not make it ‘hardware-based.’” *Id.* at 14 (citing Pet. 27). Patent Owner argues Petitioner’s position effectively eliminates the distinction between hardware and firmware-based routers—improperly rendering the “firmware-based” claim language superfluous. *Id.* Patent Owner further argues that Petitioner has not shown “what specific shell logic component is responsible for the identified ‘functionality,’ and never ties any of the functionalities discussed to any particular piece of hardware.” *Id.* at 16. According to Patent Owner, “shell logic functionality is simply ‘programmed’ on the hardware, which does not necessarily show that it is hardware-based.” *Id.*

Based on the current record and for the purposes of institution, Seshadri sufficiently teaches limitation [1b]. As an initial matter, we are not persuaded by Patent Owner’s reading of the claim term “hardware-based” as requiring something more than being implemented in hardware.¹⁵ On this record, the Specification supports that the plain and ordinary meaning of the term covers functionality implemented in hardware. As shown in Figure 3 (reproduced above), the programmable device may be FPGA 122 in pod 104, but it could also be “a PLD or an ASIC, or more than one of these, or some combination of these.” Ex. 1001, 4:30–33; *see also id.* at 3:8–12 (listing FPGAs, PLDs, ASICs, or some hybrid of the three). In light of this disclosure, we reject Patent Owner’s narrow interpretation of the term “hardware-based.”¹⁶

¹⁵ As noted above, Patent Owner does not propose any claim constructions for any of the claim terms. *See generally* Prelim. Resp.

¹⁶ If Patent Owner believes the term “hardware-based” should be construed differently than its plain and ordinary meaning, Patent Owner should propose a construction and identify where the intrinsic and/or extrinsic evidence supports its construction.

Notably, Petitioner points to the very same “FPGA” in Seshadri as meeting the “hardware-based” limitation. Pet. 27 (citing Ex. 1003 ¶ 78); *see also* Ex. 1004, 2:2–5, 3:2–14. Dr. Alpert testifies that “[b]ecause the shell logic is implemented using electronic circuits configured in the hardware of an IC, it is hardware-based.” Ex. 1003 ¶ 78. As Patent Owner acknowledges, the Petition “points to evidence that the identified ‘router’ (the shell logic functionality) is implemented in hardware.” Prelim. Resp. 17. For the purposes of institution, we find Dr. Alpert’s testimony supports Petitioner’s contentions, and determine that Seshadri teaches this claim limitation under its plain and ordinary meaning.

d) Limitation 1[c]: the second region comprising one or more sandboxes with user-definable programmable electronic circuits of the PLD,

Petitioner contends that “Seshadri teaches ‘sandboxing’ of a user’s client-configurable circuits (in the second region) to ‘isolate’ it from other clients’ custom logic.” Pet. 27 (citing Ex. 1004, 2:44–59, 6:11–41, 10:66–11:16; Ex. 1003 ¶ 81). Petitioner further contends that Seshadri’s “circuits are defined by the user because the user programs the actual circuit interconnections of PLD/FPGA circuits to create logical functions defined by the user.” *Id.* at 27–28 (citing Ex. 1004, 7:22–36, 10:36–65, 12:10–31, 17:16–36).

Patent Owner does not specifically respond to these arguments. *See generally* Prelim. Resp. Based on our review of the current record, at this stage of the proceeding, we determine that the information presented sufficiently supports Petitioner’s assertions as to this limitation.

- e) *Limitation 1[d]: wherein the port comprises: a bridge being lockable to prevent user access, and unlockable to enable user access, to each of the sandboxes and the user-definable programmable electronic circuits therein.*

Petitioner contends that the “port functionality that enables communication with the client-configurable circuits,” which Petitioner identifies in Seshadri’s shell logic, further “comprises functionality to perform ‘bridging functions’ between the PCIe interface and the client-configurable logic.” Pet. 28 (citing Ex. 1004, 3:41–64, 4:11–41, 6:11–41). Petitioner asserts that this “bridge is lockable/unlockable to prevent or enable user access to each sandbox,” because “the shell logic includes functionality to ‘isolate a configuration access port,’” which “functionality is locked/unlocked to disallow or allow configuration of client-configurable circuits.” *Id.* at 29 (citing Ex. 1004, 6:11–41, 12:10–31; Ex. 1003 ¶ 88).

Petitioner contends that the “bridging functionality is part of the bridge on the port because it is the portion of the shell logic that enables/disables communications for reconfiguring the client-configurable circuits.” Pet. 30 (citing Ex. 1004, 6:11–41, 9:48–10:15, 12:10–31). Alternatively, Petitioner contends, “this would have been obvious because Seshadri teaches that the shell logic includes routing functionality with a port for enabling communications to the client-configurable circuits . . . and that is what the bridging functionality performs for reconfiguration communications.” *Id.* at 30–31 (citing Petitioner’s contentions for limitation 1[b]).

Patent Owner responds that Petitioner fails to identify an alleged “bridge” in Seshadri that is lockable and unlockable. Prelim. Resp. 9–12. According to Patent Owner, Petitioner alleges that the shell logic’s mailbox 588 may be used as a bridge, but Petitioner does not show that that bridge

can be lockable and unlockable. *Id.* at 9–10 (citing Pet. 28). Instead, Patent Owner argues, Petitioner relies on wholly different features of Seshadri’s “static shell,” relating to isolation of configuration access ports, as meeting the lockable requirement. *Id.* at 10–11 (citing Pet. 29–30). Patent Owner further argues that nothing in Seshadri links isolation of configuration access ports by the shell logic to the disclosed mailboxes or suggests that mailboxes would ever be locked. *Id.* at 11–12 (citing Ex. 1004, 9:19–22, 17:47–49).

Based on the current record and for the purposes of institution, we are persuaded that Petitioner’s contentions show that Seshadri sufficiently teaches limitation 1[d]. We do not agree with Patent Owner that Petitioner’s contentions as to the port and bridge limitations of claim 1 are limited to Seshadri’s mailboxes. As to limitation 1[b], Petitioner contends Seshadri’s disclosure of routing functionality “includes, *for example*, management functions and the data-path, *such as* mailbox functionality,” and that “Seshadri teaches a router that comprises the shell logic port *and other functionality in the shell logic* for bridging and routing communications.” Pet. 25–26 (emphases added). As to limitation 1[d], Petitioner refers back to its contentions for limitation 1[b], and further contends that “Seshadri’s shell logic includes port functionality that enables communication with the client-configurable circuits.” *Id.* at 28 (citing Pet. §V.A.3[1b]). Petitioner also contends that the “port comprises functionality to perform ‘bridging functions’ between the PCIe interface and the client-configurable logic.” *Id.* (citing Ex. 1004, 3:41–64, 4:11–41, 6:11–41, 17:37–57, 18:4–24). Petitioner therefore relies more broadly on Seshadri’s shell logic as meeting the claimed port and bridge limitations. And although Petitioner’s contentions do cite to Seshadri’s mailbox 588, that is part of the functionality within the shell logic that Petitioner relies on as enabling communications between the

management virtual machine and the client virtual machines. *See id.* at 25–28; Ex. 1004, Fig. 4, 14:63–67, 17:37–57, 18:4–24.

Petitioner points to the same “shell logic” functionality as meeting the lockable/unlockable claim requirement. For example, Petitioner argues that “the shell logic includes functionality to ‘isolate a configuration access port’; this functionality is locked/unlocked to disallow or allow configuration of client-configurable circuits.” Pet. 29 (citing Ex. 1004, 6:11–41, 12:10–31; Ex. 1003 ¶ 88); *see also id.* at 30 (“the shell logic checks ‘customer account permissions’[] to reject or accept the request to unlock the reprogramming functionality”) (citing Ex. 1004, 3:41–64, 9:48–10:15; Ex. 1003 ¶ 89). Petitioner further contends that this bridging functionality “is the portion of the shell logic that enables/disables communications for reconfiguring the client-configurable circuits.” *Id.* (citing Ex. 1004, 6:11–41, 9:48–10:15, 12:10–31); *see also* Ex. 1003 ¶¶ 88–90.

Patent Owner does not dispute Petitioner’s contentions regarding Seshadri’s disclosure of the shell logic functionality. *See* Prelim. Resp. 10–12 (arguing why the mailbox would never be locked). For the purposes of institution, we therefore determine that Petitioner has sufficiently shown that Seshadri discloses this limitation.¹⁷

¹⁷ Petitioner also contends that the claimed bridging functionality “would have been obvious because Seshadri teaches that the shell logic includes routing functionality with a port for enabling communications to the client-configurable circuits . . . and that is what the bridging functionality performs for reconfiguration communications.” Pet. 30–31 (citing Ex. 1003 ¶ 90). Because, on this preliminary record, Petitioner sufficiently shows that Seshadri discloses the claimed functionality, we need not address this argument.

f) Summary as to Claim 1

For the reasons discussed above, on the present record we find that Petitioner has established that Seshadri teaches each of the elements of claim 1. Although Petitioner alternatively asserts that claim 1 is unpatentable over the combination of Seshadri and Biederman (Pet. 16), Petitioner does not present contentions for claim 1 that rely on Biederman (*see id.* at 20–31), and so we do not address this additional ground for claim 1.

g) Objective Indicia of Nonobviousness

In the record presently before us, neither party has presented any evidence of objective indicia of nonobviousness.

h) Weighing the Graham Factors

“Once all relevant facts are found, the ultimate legal determination [of obviousness] involves the weighing of the fact findings to conclude whether the claimed combination would have been obvious to an ordinary artisan.” *Arctic Cat*, 876 F.3d at 1361. On balance, considering the record presently before us, Petitioner has established a reasonable likelihood that it would prevail in showing that Seshadri would have rendered the subject matter of claim 1 of the ’943 patent obvious to one of ordinary skill in the art.

4. Independent Claim 10

Petitioner contends that Seshadri teaches similar limitations in claim 10 as recited in claim 1 for the reasons discussed above.

Pet. 31–32, 38 (citing Ex. 1003 ¶¶ 93–104, 109–111).

For claim limitation 10[c], which additionally recites “the second region comprising a plurality of sandboxes,” Petitioner contends that both Seshadri and Biederman teach “a plurality of sandboxes.” Pet. 32–34 (citing

Ex. 1003 ¶¶ 97–99). As discussed above, Petitioner sufficiently shows on this record that a person of ordinary skill in the art would have been motivated to combine the teachings of Seshadri and Biederman because Seshadri teaches a known FPGA configuration where the programmable fabric is partitioned into a shell area and a client-configurable circuit area, Biederman teaches a known technique for partitioning the programmable fabric of an FPGA, and the combination would have provided several benefits. *Id.* at 34 (citing Ex. 1003 ¶¶ 100–103).

Petitioner contends that Seshadri teaches claim limitation 10[d], which recites “an internal communication network in the PLD, coupling the port of the bridge of the router and the one or more sandboxes for the data flow processing.” Pet. 36–37 (citing Ex. 1003 ¶¶ 105–107).

For claim limitation 10[e], which recites “wherein the bridge is lockable to prevent user access, and unlockable to enable user access, to the plurality of sandboxes and user-definable programmable electronic circuits therein,” Petitioner contends that Seshadri teaches the language that overlaps with language recited in claim limitation 1[d] for the reasons discussed above, and that Seshadri teaches the additional language as well. *Id.* at 38 (citing Ex. 1003 ¶¶ 109–111).

Patent Owner argues independent claims 1 and 10 together. *See* Prelim. Resp. 8–18 & n.3.

Based on our review of the current record, at this stage of the proceeding, we determine that Petitioner has established a reasonable likelihood that it would prevail in showing that the combination of Seshadri and Biederman would have rendered the subject matter of claim 10 of the ’943 patent obvious to one of ordinary skill in the art, and thus need not address Petitioner’s additional ground for claim 10 based on Seshadri alone.

5. Dependent Claims 2–5, 9, 11–14, and 18

Each of claims 2–5, 9, 11–14, and 18 depend directly from claims 1 or 10. *See* Ex. 1001, 17:54–18:5, 18:19–22, 18:41–58, 19:5–7. Petitioner asserts that claims 2–5 and 11–14 are unpatentable over Seshadri, and that claims 2–5, 9, 11–14, and 18 are unpatentable over Seshadri and Biederman. Pet. 38–51.

Patent Owner does not specifically respond to Petitioner’s contentions as to these claims. *See generally* Prelim. Resp.

Based on our review of the current record, at this stage of the proceeding, we determine that Petitioner has established a reasonable likelihood that it would prevail in showing that the combination of Seshadri and Biederman would have rendered the subject matter of claims 2–5, 9, 11–14, and 18 of the ’943 patent obvious to one of ordinary skill in the art, and thus need not address Petitioner’s additional ground based on Seshadri alone.

E. The Remaining Grounds

Petitioner asserts that claims 1–5 and 10–14 of the ’943 patent are unpatentable under 35 U.S.C. § 103 as obvious over Atsatt-113 (Ground 3). Pet. 16. Petitioner also asserts that claims 1–5, 9–14, and 18 are unpatentable as obvious over Attsatt-113 and Biederman (Ground 4). *Id.* Petitioner further asserts that claims 6 and 15 are unpatentable as obvious over Grounds 1–4 when further combined with Tarafdar.¹⁸ *Id.* Petitioner also asserts that claims 7 and 16 are unpatentable as obvious over

¹⁸ For ease of reference, we use this format for listing Petitioner’s asserted grounds, consistent with the Petition. *See* Pet. 16. Each of Petitioner’s additional grounds based in part on “Grounds 1–4,” however, constitutes four separate grounds of unpatentability.

Grounds 1–4 when further combined with Kulkarni. *Id.* Lastly, Petitioner asserts that claims 8 and 17 are unpatentable as obvious over Grounds 1–4 when further combined with Atsatt-923. *Id.*

Patent Owner responds that, for reasons similar to those with Grounds 1 and 2, Petitioner has failed to show that the prior art asserted in Grounds 3–4 teaches limitations 1[b] and 1[d]. Prelim. Resp. 19–23. Patent Owner does not present separate arguments for Petitioner’s Grounds 5–7. *See* Prelim. Resp. 24–26.

Because we have determined above that, at this stage of the proceeding and on the present record, the information presented in the Petition shows that there is a reasonable likelihood that Petitioner will prevail with respect to its challenges based on Seshadri and Biederman (Grounds 1 and 2), we need not address, in this Decision, Petitioner’s additional challenges (Grounds 3–7). *See* 35 U.S.C. § 314(a); *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1356 (2018) (“Section 314(a) does not require the Director to evaluate every claim individually. Instead, it simply requires him to decide whether the petitioner is likely to succeed on ‘at least 1’ claim. Once that single claim threshold is satisfied, it doesn’t matter whether the petitioner is likely to prevail on any *additional* claims; the Director need not even consider any other claim before instituting review”); 37 C.F.R. § 42.108(a).

IV. CONCLUSION

Based on the arguments and evidence presented by the parties, we conclude that Petitioner has demonstrated a reasonable likelihood of prevailing with respect to at least one claim of the ’943 patent challenged in

the Petition. Our analysis is based on the preliminary record developed thus far and may change after the record is developed fully, during trial.

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review is instituted for claims 1–18 of the '943 patent on the unpatentability grounds asserted in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which commences on the entry date of this Decision.

IPR2025-00223
Patent 10,985,943 B1

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