



March 9, 2026

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VIA E-MAIL

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Re: Concurrent Ventures, LLC and XtreamEdge, Inc. v. Advanced Micro Devices, Inc., and Pensando Systems, Inc., Case No. 4:25-cv-09567 (N.D. Cal.)

Counsel:

We write regarding your letter dated February 20, 2026. We have reviewed the purported deficiencies identified in your letter and disagree. Plaintiffs' requests, complaints, and asserted "deficiencies" amount to an effort to eliminate properly disclosed invalidity theories and to force Defendants to finalize their invalidity arguments (not just their contentions) before fact and expert discovery, something that is not required by this Court's Local Patent Rules.

Sotera Stipulation

Defendants confirm that they will not pursue invalidity theories covered by the *Sotera* stipulation, and Plaintiffs have no need to respond to theories covered by the stipulation. Contrary to Plaintiffs' accusation, Defendants' invalidity contentions do not violate the *Sotera* stipulation because the identified references (1) are disclosed as part of system prior art theories; or (2) are disclosed to preserve Defendants' rights in the unlikely event that an IPR is de-instituted.

First, Defendants' *Sotera* stipulation is limited to grounds "raised or could have been reasonably raised in an IPR (i.e., any ground that could be raised under §§ 102 or 103 on the basis of prior art patents or printed publications)," and therefore does not reach invalidity theories based on system prior art. *See Sotera Stipulation*, Dkt. 78. As disclosed by Defendants' contentions, the following references are part of system prior art theories:

- For the '596 patent, Drews, Gewirtz, Goyal, Kolinummi, Ohkawa, Rosenthal, Borkowski, Hughes, Kim, Tuan, Kanai, Matsunami, Alexander, Buchko, Dongare, Hammer, Khawand, Michaylov, and Van Loo (Invalidity Contentions ("Inv. Cont."), 31–37, 40–44);
- For the '753 patent, Pierson, Stroud, RFC 791, Da Silva, Cragon, Ramanujan, Cullison, and Saulsbury (Inv. Cont. 61–69, 73–74); and
- For the '943 patent, Jacobson, Schultz, Seshadri, Atsatt-113, Cervero, Pogliani, Bernat, Abdelfattah, and Rahim (Inv. Cont. 79–99).

These portions of Defendants' invalidity contentions properly provide notice of Defendants' invalidity theories based on system prior art and are not barred by the *Sotera* stipulation.

Second, the Director has recently de-instituted IPRs. See, e.g., Theresa Schliep, *Squires Sinks 2 PTAB Challenges, Including 1 He Instituted*, Law360 (Feb. 20, 2026), <https://www.law360.com/articles/2444138/squires-sinks-2-ptab-challenges-including-1-he-instituted>. In the unlikely event that one of Defendants' IPRs is de-instituted, the *Sotera* stipulation would no longer bar Defendants from pursuing any grounds of invalidity for the affected patent. So long as the IPRs remain instituted, Defendants will not pursue invalidity theories covered by the *Sotera* stipulation, and Plaintiffs have no need to respond to those theories.

Identification of System Prior Art

Defendants have complied with Patent Local Rule 3-3(a) by disclosing the information of which they are aware, without the benefit of having taken third party discovery, including, for each prior art system, "the date the offer [for sale] or [public] use took place or the information became known, and the identity of the person or entity which made the use or which made and received the offer, or the person or entity which made the information known or to whom it was made known." Plaintiffs' complaint amounts to premature requests for Defendants to provide information regarding third-party products that is not in Defendants' possession absent full discovery, and to finalize invalidity theories before discovery has concluded. This is again contrary to this District's practice.

First, Defendants disagree that the list of ARM products constitutes "open unlimited categories of systems." Defendants have provided a list of concrete example products and designs offered by ARM and identified them by specific names to the best of their current ability: "TCP/IP RTOS, ARM1156T2-S, Cortex-R5, Cortex-A, ARMv7, and Corelink CCI-400." Moreover, the inclusion of "including but not limited to" is justified because, as generally known in the industry, ARM provides designs and technological support to its customers. The same design or solution provided by ARM may given different names depending on the specific customer or industry even if the product or design is the same, and without discovery, Defendants do not possess the information necessary to finalize the list.

Second, the exact dates on which the "offer [for sale] or [public] use took place or the information became known [] and the identity of the person or entity which made the use or which made and received the offer, or the person or entity which made the information known or to whom it was made known," is third-party information not currently within Defendants' possession. Notwithstanding the present unavailability of that information, Defendants disclosed, based on the release dates reflected in the publicly available ARM documentation, that the offer for sale or public use took place or the information became known occurred at least "before December 6, 2013." Inv. Cont. 8; Ex. 596-18 at 1 (ARM documentation dated 1996–2011). Moreover, Plaintiffs cite Defendants' disclosure of ARM—a specific entity that made the use or offer—yet still characterize Defendants' disclosure as a "diffuse list that encompass[es] the marketplace." Such inconsistency is untenable.

With respect to system prior art within Defendants' control, Defendants have disclosed "the date the offer or use took place or the information became known" and "the identity of the person or entity which made the use or which made and received the offer" by diligently producing

documents evidencing product sales. Inv. Cont. 77 (citing AMD-CV-0149659 (sales data for prior art Xilinx XCZU9EG)).

As the ARM example discussed above illustrates, Defendants have disclosed—based on their current knowledge—the information required by the Local Patent Rules, are actively pursuing discovery to obtain more detailed information, and therefore expressly reserve the right to supplement their invalidity contentions as discovery proceeds, as Local Patent Rule 3-6(b) and (c) permit. See, e.g., Defs.’ Notice of Subpoena to ARM, Ex. 1 at 8 (seeking “[d]ocuments sufficient to show the public disclosure, use, offer for sale, or sale in the United States”), 11 (seeking testimony regarding “[t]he facts and circumstances surrounding the public disclosure, public use, offer for sale, or sale of each Subpoenaed System”).

If, notwithstanding Defendants’ compliant disclosures and the ongoing discovery, Plaintiffs maintain that the invalidity contentions are deficient, then Plaintiffs should move to strike now. A later motion to strike would unnecessarily waste both judicial, party, and third-party resources because, by the time the Court rules, the parties will likely have already expended substantial time and money conducting third party discovery and preparing expert reports and related submissions.

Obviousness Assertions

Plaintiffs fail to acknowledge that Defendants have provided a concrete list of obviousness combinations for each primary reference. See, e.g., Inv. Cont. 31 (listing combinations starting with “ARM System(s) + Drews ... ”); 33–34 (same for Intel/Fulcrum System(s)); 36 (same for NVIDIA System(s)); 38–39 (same for Hughes); 40 (listing combinations starting with “IBM Cell Broadband System(s) + Alexander”). For each of these references, Defendants provided clear disclosure of the theory of obviousness, motivations to combine, and why the theory and motivations apply to each combination. *Id.* at 32–41.

Given the extensive list of purported challenges raised elsewhere in your letter, Plaintiffs’ silence regarding these expressly listed combinations implicitly concedes that there is no basis to challenge those combinations.

Moreover, Plaintiffs continue to press for premature, front-loaded disclosures that are inconsistent with this District’s practice. For example, Plaintiffs’ demand that Defendants produce charts mapping each asserted obviousness combination is baseless. See *Fujifilm Corp. v. Motorola Mobility LLC*, No. 12-cv-03587-WHO, 2015 WL 757575, at *28 (N.D. Cal. Feb. 20, 2015) (“Courts in this district have held that Rule 3–3(b) does not always require the accused infringer to spell out in exact detail every particular combination it intends to assert.”); *Slot Speaker Techs., Inc. v. Apple, Inc.*, No. 13-cv-01161-HSG (DMR), 2017 U.S. Dist. LEXIS 8414, at *16 (N.D. Cal. Jan. 19, 2017) (a party “need not list every combination of prior art when the theory of obviousness is the same for each and every possible combination of prior art” and “may instead so state”).

Indeed, the purported “boilerplate” language Plaintiffs single out has been deemed sufficient by courts in this District. See *Avago Techs. Gen. IP PTE Ltd. v. Elan Microelectronics Corp.*, No. C 04-05385 JW (HRL), 2007 WL 951818, at *4 (N.D. Cal. Mar. 28, 2007) (finding adequate a disclosure identifying references “in combination with” a list of other references).

As such, Defendants reserve every obviousness combination explicitly listed, and reserve every obviousness combination of “any reference in Table [A/B/C/D/E] with any other reference(s) in Table [A/B/C/D/E].” Defendants have explained their obviousness theories and have alleged that those theories apply across the prior-art references listed in each table. See, e.g., Inv. Cont. 103–105 (explaining that “[a]ll of these items of prior art are directed to networking systems and architectures, and propose solutions similar to those discussed in the ‘634 patent,” and then providing specific illustrative combinations and theories). This type of grouped disclosure is consistent with Northern District practice. See *Avago Techs.*, 2007 WL 951818, at *4 (holding sufficient a disclosure organizing references into groups and representing that “its theory of obviousness is the same for each and every possible combinations of the two groups,” and finding the defendant “reasonably specifies the combination of prior art references” alleged to render the claims obvious).

Specificity of Claim Charts

Plaintiffs’ complaints about purported lack of specificity are ironic and laughable in light of Plaintiffs’ infringement contentions.

As just one example, the infringement contentions for the ‘596 patent contain an ever-expanding thicket of mappings and purported theories. Defendants have repeatedly raised this issue and requested that Plaintiffs narrow their contentions, yet Plaintiffs have failed to remedy the issue and instead have continued to expand them. See Defs.’ Letter re Inf. Cont. dated November 5, 2024 and February 12, 2025. Your infringement contentions hint that at least 11 different components might be the first processing element (e.g., server/host processor, external VMs, table engines, match processing units, scheduler, doorbell engine, parser, deparser, PDMA splitter, and ARM cores). You then suggest at least 6 different theories on what might be a reservation register, including a register interface that itself encompasses many additional registers, along with allegations that at least 11 different queues might be the claimed input or output queues, including accusations against “16 million hardware queues. Taken together, the contentions include a sprawling morass of permutations, without articulating any coherent theory that connects the mappings in a manner that that satisfies the requirements of the ‘596 patent.

Defendants also note that, to the extent any of Plaintiffs’ objections rests on any legal significance of the terms “disclosed in prose” or “prose,” Defendants are unaware of any authority recognizing such a requirement or explaining what Plaintiffs mean by it. Please provide an explanation and any supporting authority for this complaint.

In any event, the claim charts provide sufficient specificity for each limitation. For example, with respect to the NVIDIA/Mellanox System you reference, Defendants identify a specific mapping for the “second processing element” (an adapter) and provide five pages of supporting citations and explanation as to why it meets the limitation. Inv. Cont., Ex. 596-20 at 17–22.

More broadly, Defendants’ invalidity charts provide ample explanation and evidentiary support for the asserted mappings. See, e.g., Ex. 596-19 (average of approximately 4 pages of disclosure per limitation, totaling 67 pages); Ex. 596-25 (average of approximately 11 pages per limitation); Ex. 753-01 (average of approximately 20 pages per limitation); Ex. 767-03 (average of approximately 9 pages per limitation).

It should also be noted that some of these charts are based on system prior art, information to which Defendants do not yet have full access, and Defendants intend to supplement their contentions as discovery proceeds, consistent with Patent L.R. 3-6. See *Verinata Health, Inc. v. Ariosa Diagnostics, Inc.*, No. C 12-05501 SI, 2014 WL 1648175, at *2 (N.D. Cal. Apr. 25, 2014) (“The local patent rules in the Northern District of California ... requir[e] both the plaintiff and the defendant in patent cases to provide early notice of their infringement and invalidity contentions, and to proceed with diligence in amending those contentions when new information comes to light in the course of discovery.”) (internal quotation omitted). Nevertheless, even at this early stage and based on currently available information, Defendants have disclosed their invalidity theories, and Defendants are actively pursuing third-party discovery to obtain additional detail.

As such, Defendants are *not* strictly limited to the elements currently identified in their charts and reserve the right to supplement with additional mappings and amend their invalidity theories as soon as they receive the discovery results from the subpoenaed third parties. See *Symantec Corp. v. Veeam Corp.*, No. 12-cv-05443, 2013 WL 3490392, at *2 (N.D. Cal. July 11, 2013) (finding “good cause to amend the invalidity contentions,” as “discovery is still ongoing, [the defendant] may learn more facts that support its invalidity contentions.”).

Document Production Accompanying Invalidity Contentions

Your complaints about document production are similarly baseless and disregard the Local Patent Rules’ plain requirement that a producing party provide “source code, specifications, schematics, flow charts, artwork, formulas, or other documentation sufficient to show the operation of any aspects or elements of an Accused Instrumentality”—not every document that might conceivably bear on that operation. Defendants have produced and made available sufficient documents and source code to comply with the Local Patent Rules.

First, given the unusual procedural posture of this case (including venue discovery), discovery has been ongoing since July 24, 2025, when Judge Albright entered the protective order. Before and since then, Defendants have produced thousands of documents relating to the operation of the Accused Instrumentalities. See, e.g., AMD-CV-VOL018; AMD-CV-VOL019 (addressing the design and operation of the accused products with respect to, *inter alia*, NVMe and RDMA protocols); AMD-CV-VOL026; AMD-CV-VOL028 (addressing the operation of the accused products with respect to, *inter alia*, metrics/telemetry and the doorbell mechanism). Plaintiffs have been aware of these productions for months, as reflected in their infringement contentions. See, e.g., Am. Compl., Dkt. 142, Ex. D, at 76; Ex. E, at 120 (citing documents from AMD-CV-VOL018 and AMD-CV-VOL019).

Second, Defendants have long made available for inspection source code for the accused products, including at least Capri, Elba, Giogilio, and Salina, since June 17, 2025, and Defendants have supplemented the source code available on December 30, 2025, and February 12, 2026. Similarly, Defendants have made available for inspection prior art source code, including source code for Xilinx Zynq Ultrascale+ System(s) (e.g., the representative XCZU9EG, as disclosed in Inv. Cont. at 77). As you stated in your February 18, 2026 email, you were aware of the availability of source code for inspection and intended to inspect source code during the week of March 9. Defendants promptly confirmed the availability of the source code the following day and, pursuant to the Protective Order, requested advance notice of the date(s) of review and the identities of those who will attend. Instead of the required notices (which were not given until March 6), Defendants received your letter questioning the sufficiency of Defendants’ diligent source code disclosures.

Finally, Plaintiffs complain that Defendants have referenced the possibility of producing “[a]dditional responsive agreements” as discovery continues in this case. To be clear, Defendants are not currently aware of any additional license agreements that they intend to rely upon in this litigation that were not identified in the Patent L.R. 3-4 disclosures. Defendants have, however, produced additional documents that are related to the identified license agreements. For example, AMD-CV-VOL038 includes schedules of licensed patents related to the Future Link, Longitude AIS, Longitude Elpida, and Monterey RPX licenses. Defendants also anticipate producing a similar schedule related to the Intellectual Ventures license agreement. Further, defendants expect to produce other (non-license) agreements, including agreements with HPE and Meta.

If Plaintiffs contend that Defendants must seek leave from the Court to produce or rely on these documents, Defendants ask that Plaintiffs state their position clearly in response to this letter so that Defendants may seek leave. Further, Defendants ask that Plaintiffs state whether they will oppose such a motion for leave and, if so, the basis for their opposition.

Defendants are available for a meet and confer at the following times:

- Thursday, March 12 between 9:30-11:30 am, 1-3:30 pm PT
- Friday, March 13 between 10am-12 pm, 1-3 pm PT

Sincerely,

/s/ Christopher Ponder
Christopher Ponder
for SHEPPARD, MULLIN, RICHTER & HAMPTON LLP