

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00228
U.S. Patent No. 11,101,276
Issue Date: August 24, 2021

Title: WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL
MEMORY DEVICES AND FABRICATION METHODS THEREOF

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 11,101,276
PURSUANT TO 35 U.S.C. §§311-319 and 37 C.F.R. §42**

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LISTING OF EXHIBITS

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1001	U.S. Patent No. 11,101,276 to Zhu et al. (“the ’276 patent”)
1002	File History of U.S. Patent No. 11,101,276 (“the ’276 FH”)
1003	Declaration of Dr. Sanjay Banerjee (“Banerjee”)
1004	<i>Curriculum Vitae</i> of Dr. Sanjay Banerjee
1005	U.S. Patent Publication No. 2012/0070944A1 (“Kim”)
1006	U.S. Patent Publication No. 2019/0067306A1 (“Fang”)
1007	U.S. Patent Publication No. 2017/0062470A1 (“Han”)
1008	U.S. Patent Publication No. 2017/0294384A1 (“Chen”)
1009	U.S. Patent Publication No. 2018/0330985A1 (“Yu”)
1010	Aritome, “NAND Flash Memory Technologies” (2016)
1011	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
1012	Micheloni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)
1013	U.S. Patent Publication No. 2017/0117222A1 to Kim et al.
1014	Chang and Sze, “ULSI Technology” (1996)
1015	Orlowski et al., <i>Si, SiGe, Ge, and III-V Semiconductor Nanomembranes and Nanowires Enabled by SiGe Epitaxy</i> , ECS Transactions Vo. 33, No. 6 (2010), 777-89
1016	U.S. Patent No. 9,728,547 (“Ohsaki”)
1017	U.S. Patent Publication No. 2017/0148677A1 (“Shin”)

EXHIBIT NO.	DESCRIPTION
1018	U.S. Patent No. 10,672,711 to Zhu et al. (“the ’711 patent”)
1019	Excerpt from YMTC’s Exemplary Infringement Claim Chart for U.S. Patent No. 11,101,276 (Ex. H-1 to Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024) (“YMTC2 Infringement Contentions, Ex. H-1”) [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]
1020	Korean Patent Publication No. KR10-2013-0015120 (“Lee”) with machine translation
1021	Wolf S., et al., “Silicon Processing for the VLSI Era, Volume 1 – Process Technology, Chapter 15, Multilevel Interconnects for ULSI” (2nd Ed. 2000)
1022	CN Patent Publication No. 107658309 A with certified translation (Priority application to the ’276 patent)
1023	Wang, et al., “Low DC-Bias Silicon Nitride Anisotropic Etching,” Journal of Vacuum Science & Technology B, Vol. 33, Issue 6 (Sept. 10, 2015)
1024	U.S. Patent Publication No. 2014/0284661A1 (“Williams”)
1025	Shamiryan D., et al., “Selective Removal of High-K Gate Dielectrics,” Chemical Engineering Communications (2009)
1026	Morel, et al., “Tungsten metal gate etching in Cl ₂ /O ₂ inductively coupled high density plasmas,” Journal of Vacuum Science and Technology B (Nov. 3, 2008)
1027	Kim, et al., “Dry Etching of High-k Dielectric Thin Films in HBr/Ar Plasma,” Journal of the Korean Physical Society, Vol. 54, No. 2, pp. 934-38 (February 2009)
1028	U.S. Patent No. 10,297,543 to Park et al.

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EXHIBIT NO.	DESCRIPTION
1029	Minute Order (case schedule), Dkt. No. 141, dated September 18, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1030	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1031	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, LTD.'s Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1032	Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:24-cv-04223-RFL which has been consolidated with Case No. 3:23-cv-05792-RFL

LISTING OF CHALLENGED CLAIMS

Ref. #	Listing of Challenged Claims
Claim 1:	
[1.PRE]	A method for forming a semiconductor structure, comprising:
[1.A]	forming a staircase structure having a plurality of steps, wherein the forming of each step of the plurality of steps comprises disposing a sacrificial layer over a dielectric layer;
[1.B]	disposing an etch-stop layer on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer;
[1.C]	disposing an insulating layer on the etch-stop layer;
[1.D]	replacing the sacrificial layer of each step with a gate stack, the gate stack comprising a conductive layer and a first high-k dielectric layer;
[1.E]	forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer;
[1.F]	etching the exposed portions of the etch-stop layer in the plurality of openings and exposing at least a portion of the conductive layer of each step; and
[1.G]	forming a plurality of conductive structures in each of the plurality of openings.
Claim 2:	
[2]	The method of claim 1, wherein the forming the plurality of openings comprises performing an etching process on the insulating layer, wherein an etching rate of the insulating layer is higher than an etching rate of the etch-stop layer.

Ref. #	Listing of Challenged Claims
Claim 3:	
[3]	The method of claim 2, wherein the etching process comprises anisotropic dry etching.
Claim 4:	
[4]	The method of claim 1, wherein etching the exposed portions of the etch-stop layer comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer of each step.
Claim 5:	
[5]	The method of claim 4, wherein etching the exposed portions of the etch-stop layer further comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the first high-k dielectric layer.
Claim 6:	
[6]	The method of claim 1, wherein disposing the etch-stop layer comprises disposing hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, and/or any combination thereof.
Claim 7:	
[7]	The method of claim 1, wherein disposing the etch-stop layer comprises disposing the etch-stop layer with a thickness in a range between 10 nm to 100 nm.
Claim 8:	
[8]	The method of claim 1, wherein disposing the etch-stop layer comprises performing chemical vapor deposition (CVD), physical vapor deposition (PVD), sputtering, atomic layer deposition (ALD), spin-coating, or any combination thereof.

Ref. #	Listing of Challenged Claims
Claim 9:	
[9]	The method of claim 1, further comprising: after disposing the insulating layer on the etch-stop layer, planarizing the insulating layer and the staircase structure by using chemical-mechanical-polishing (CMP).
Claim 10:	
[10]	The method of claim 1, wherein forming the plurality of conductive structures comprises disposing conductive materials inside the plurality of openings, the conductive materials directly on the exposed conductive layer of the each step.
Claim 11:	
[11]	The method of claim 1, wherein forming the plurality of conductive structures further comprises planarizing the conductive materials and the insulating layer.
Claim 12:	
[12]	The method of claim 1, wherein forming the staircase structure further comprises performing a repetitive etch-trim process on the sacrificial layers and the dielectric layers.
Claim 13:	
[13.PRE]	The method of claim 1, wherein replacing the sacrificial layer of each step with the gate stack comprises:
[13.A]	forming a substrate opening through the staircase structure;
[13.B.]	removing the sacrificial layer of each step through the substrate; and
[13.C]	disposing the first high-k dielectric layer and the conductive layer in place of the sacrificial layer.

Ref. #	Listing of Challenged Claims
Claim 14:	
[14]	The method of claim 13, wherein disposing the first high-k dielectric layer comprises disposing hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide and/or any combination thereof.
Claim 15:	
[15]	The method of claim 13, wherein disposing the conductive layer comprises disposing tungsten, cobalt, nickel, copper, aluminum, and/or any combination thereof.
Claim 16:	
[16]	The method of claim 13, wherein disposing the conductive layer comprises disposing poly-crystalline silicon, poly-crystalline germanium, or poly-crystalline germanium-silicon.
Claim 17:	
[17]	The method of claim 1, further comprising: prior to disposing the etch-stop layer, disposing a barrier layer on each step of the plurality of steps, wherein the barrier layer protects underlying structures during the etching of the exposed portions of the etch-stop layer.
Claim 18:	
[18]	The method of claim 17, wherein disposing the barrier layer comprises disposing one or more of silicon oxide, silicon oxynitride, silicon nitride, TEOS, aluminum oxide, and silicon oxide incorporated with F, C, N, or H.

I. INTRODUCTION

Petitioner Micron Technology, Inc. (“Petitioner”) respectfully requests *inter partes* review of claims 1-18 (the “Challenged Claims”) of U.S. Patent No. 11,101,276 (the “’276 patent”) assigned to Yangtze Memory Technologies Co., Ltd. (“YMTC” or “PO”). There is more than a reasonable likelihood that Petitioner will prevail with respect to at least one Challenged Claim.

The ’276 patent relates to a method of forming a conventional “staircase structure on an alternating conductor/dielectric stack” (*i.e.*, stack of alternating gate and dielectric layers). Ex 1001, 5:38-46. Such staircase structures provide landing areas, *i.e.*, steps, for the contacts (called “conductive structures” in the ’276 patent) that physically connect to the gate layers. Because it is a staircase, the landing areas are at different depths in the device. Etching contact holes to different depths allegedly required fabrication techniques that were either costly or prone to inadvertently punching through the target landing area. *Id.*, 5:54-6:10. The ’276 patent purports to solve this issue by forming an etch-stop layer and an optional barrier layer over the staircase landing areas:

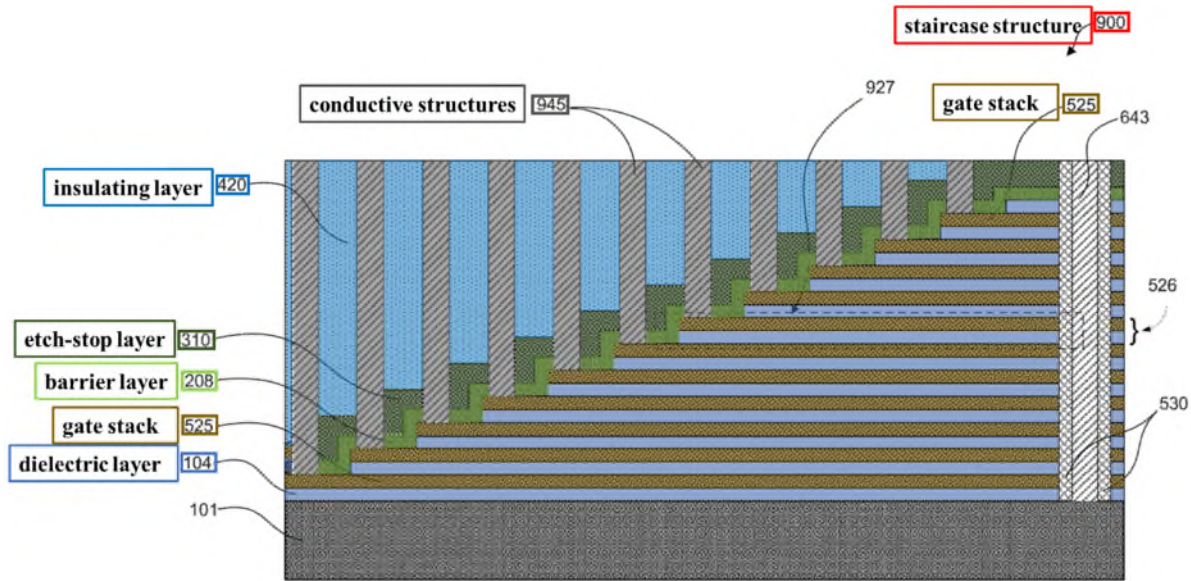


FIG. 9A

Ex. 1001, Fig. 9A.¹ Additionally, the '276 patent requires forming high-k dielectric layers around the conductive layers:

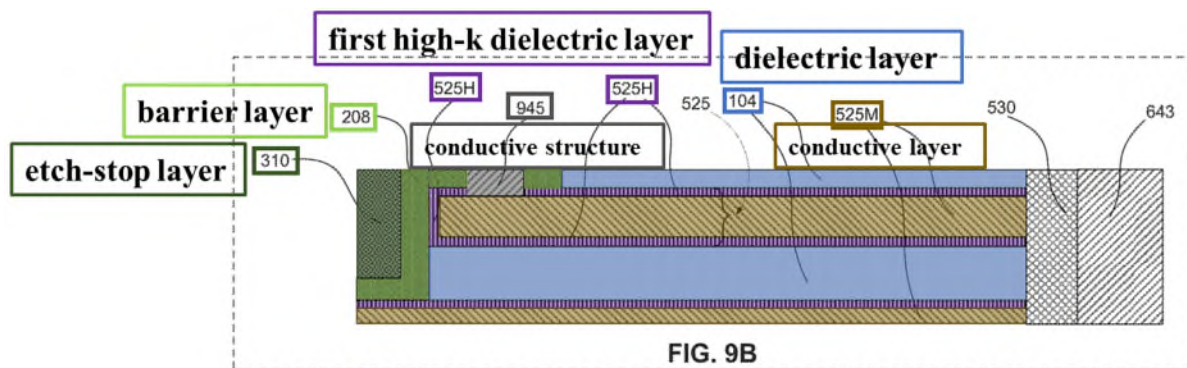


FIG. 9B

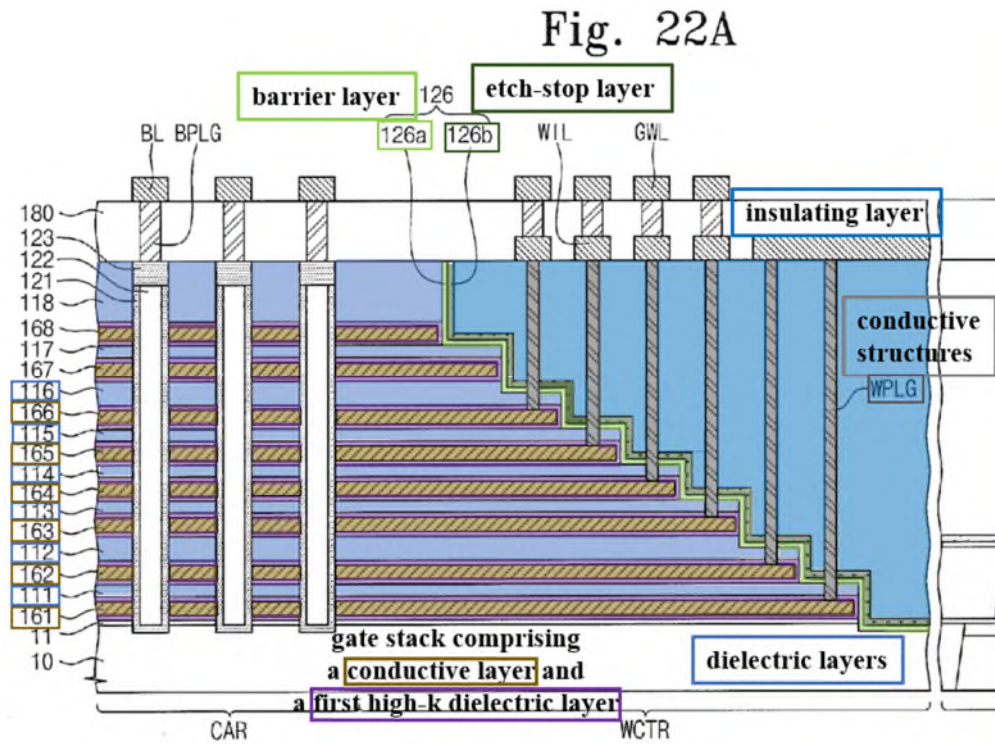
These alleged improvements, however, were no improvement at all, and the Examiner rejected seventeen of twenty pending claims as obvious over two prior-art combinations. Ex. 1002, 90-95. In response, the Applicant amended the

¹ All color annotations in this Petition are added except where noted otherwise.

independent claim to require the etch-stop layer to comprise a second high-k dielectric layer, which led to allowance. *Id.*, 114-18, 128.

As this Petition demonstrates, the Examiner erred in allowing the claims: a high-k-dielectric etch-stop layer was known in the art. Further, PO's infringement contentions against Petitioner in district court assert that silicon nitride is a high-k dielectric. Ex. 1019, 9. PO's broad infringement read ensnares additional prior art.

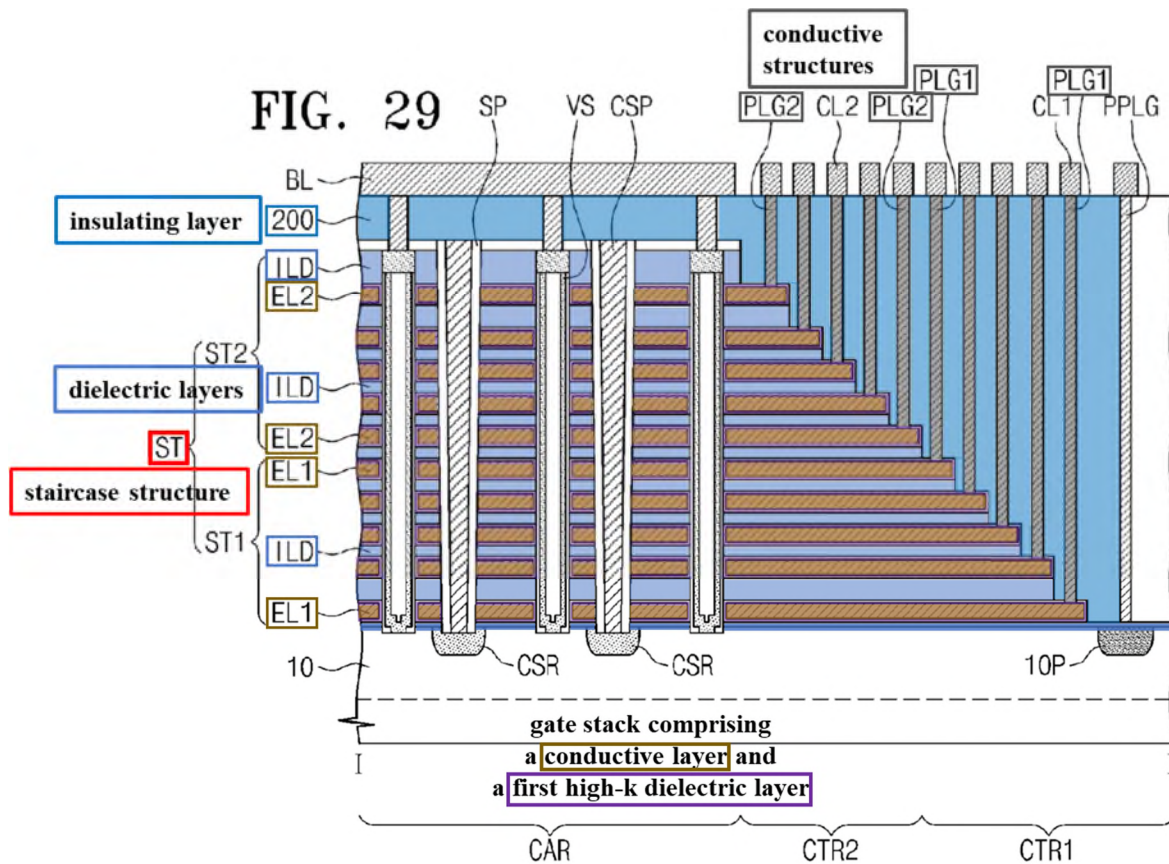
This Petition relies on two primary references: Kim and Han. Neither was before the Examiner during prosecution. Notably, Kim discloses the alleged point of novelty under PO's broad read: a staircase structure with a silicon-nitride etch-stop layer and a barrier layer.



Ex. 1005 (“Kim”), Fig. 22A.² Kim renders obvious fourteen of the Challenged Claims. Kim in view of Fang renders obvious all Challenged Claims under the correct interpretation of high-k dielectric.

The other primary reference, Han, discloses all required elements of the sole independent claim except the etch-stop layer:

² All Kim and Han staircase images shown herein omit a portion (the peripheral-circuit region) irrelevant to this Petition.



Ex. 1007 (“Han”), Fig. 29. Fang supplies a high-k etch-stop layer to a similar structure:

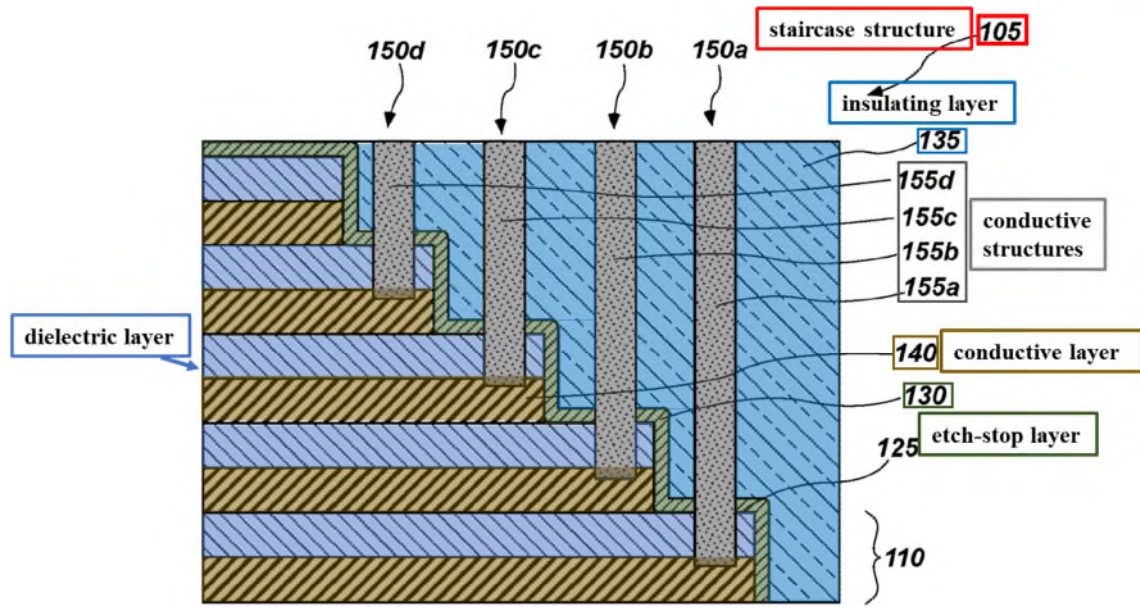
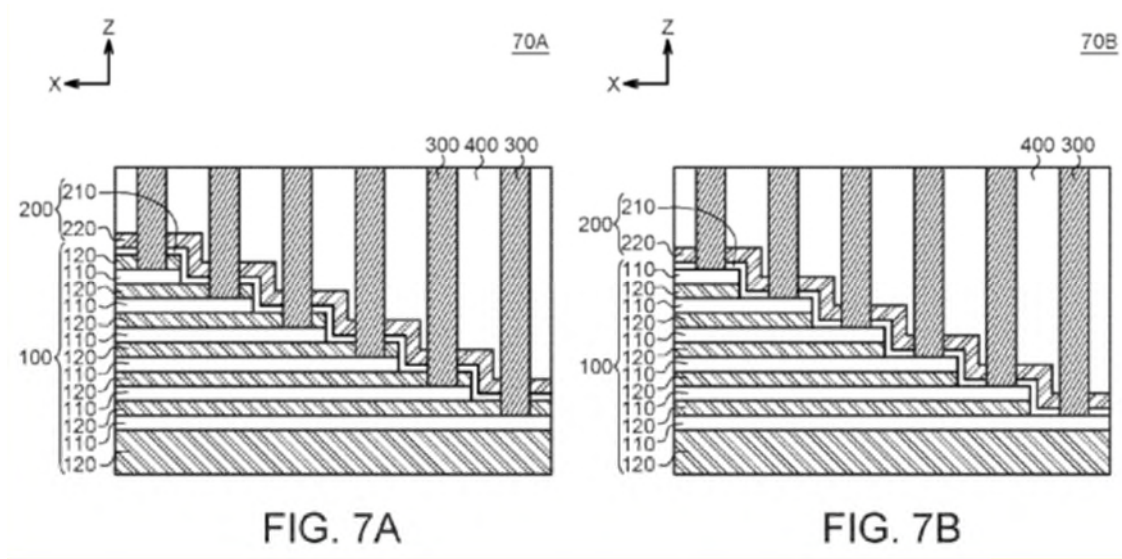


FIG. 6

Ex. 1006 (“Fang”), Fig. 6. Han in view of Fang renders obvious all but three claims. In fact, Fang discloses the exact problem and solution alleged in the ’276 patent—but Fang did it earlier. Han, Fang, and Chen together render obvious two more claims.

Although the ’276 patent illustrates a dielectric layer *under* the corresponding conductive layer at each step, whereas the figures from Kim (and Fang) show the dielectric layer *above* the corresponding conductive layer at each step, that distinction is immaterial because Kim also discloses having the conductive layer over the dielectric layer. Indeed, prior art demonstrates that both orders were conventional:



Ex. 1008 (“Chen”), Fig. 7A (dielectric on top), Fig. 7B (conductor on top); *see also* Ex. 1009, [0034]-[0035] (disclosing both orders).

Petitioner requests that the Board institute trial and find the Challenged Claims unpatentable under §103.

II. MANDATORY NOTICES

A. Real Party-in-Interest

Petitioner Micron Technology, Inc. and its subsidiaries, including Micron Consumer Products Group LLC, are the real parties-in-interest.

B. Related Matters

According to USPTO assignment records, the '276 patent is currently assigned to YMTC. On July 12, 2024, YMTC asserted the '276 patent and U.S. Patent Nos. 10,672,711, 10,879,164, 10,879,254, 10,886,291, 11,145,666, 11,450,604, 11,482,532, 11,568,941, 11,581,322, and 12,010,838 against Micron (the “YMTC2 case”). On August 21, 2024, the litigation was consolidated with

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Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023) (“Co-Pending Litigation”).

In addition to this Petition, Petitioner is filing (or has filed) petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation:

Patent	PTAB Proceeding	Wave
10,658,378 (claims 15-17 and 19-20)	IPR2024-00788	Wave 1 Petitions
10,861,872 (claims 1-6 and 11-13)	IPR2024-00789	
10,868,031	IPR2024-00790	
10,937,806 (claims 8-9 and 11-12)	IPR2024-00791	
10,950,623	IPR2024-00794	
11,468,957	IPR2024-00792	
11,501,822	IPR2024-00795	
11,600,342 (claims 1-6 and 8-20)	IPR2024-00793	
10,658,378 (claims 1-7 & 18)	IPR2024-00909	Wave 2 Petitions
10,861,872 (claims 7-10)	IPR2024-00910	
10,937,806 (claim 10)	IPR2024-00911	
11,600,342 (claim 7)	IPR2024-00912	
10,672,711	IPR2025-00117	Wave 3 Petitions
10,879,164	IPR2025-00118	
10,879,254	IPR2025-00034	

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Patent	PTAB Proceeding	Wave
10,879,254	IPR2025-00119	
10,886,291	IPR2025-TBD	
11,101,276	IPR2025-00228	
11,145,666	IPR2025-00189	
11,450,604	IPR2025-00035	
11,482,532	IPR2025-TBD	
11,568,941	IPR2025-00190	
11,581,322	IPR2025-00191	
12,010,838	IPR2025-00229	

The Director and the Board should allow this Petition under 35 U.S.C. §314(a), 35 U.S.C. §325(d), and/or 37 C.F.R. §42.108(a).

C. Counsel, Service, and Fee Information

Petitioner designates the following counsel:

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YMTC_OHS@orrick.com. Pursuant to 37 C.F.R. §42.10(b), Petitioner's Power of Attorney is attached.

The USPTO is authorized to charge the filing fee and any other fees incurred by Petitioner to the deposit account of Orrick, Herrington, & Sutcliffe LLP: 15-0665.

III. REQUIREMENTS FOR *INTER PARTES* REVIEW

A. Grounds for Standing

Petitioner certifies that the '276 patent is available for IPR, and that Petitioner is not barred or estopped from requesting this IPR. Petitioner was served with a complaint alleging infringement of the '276 patent on July 12, 2024.

B. Identification of Challenge and Statement of Precise Relief Requested

Petitioner requests IPR of claims 1-18. This Petition is supported by the accompanying Declaration of Dr. Sanjay Banerjee (Ex. 1003, "Banerjee"), a leading expert in the 3D NAND field.

The '276 patent claims priority to a CN application filed on August 31, 2017. Ex. 1001, Cover. For this Petition, Petitioner assumes the '276 patent is entitled to that 2017 priority date.

Petitioner relies on the following references:

(1) U.S. Patent Publication No. 2012/0070944A1 ("Kim"). Kim was filed on September 13, 2011 and was published on March 22, 2012. Kim, Cover. Kim is prior art under 35 U.S.C. §§ 102(a)(1)-(a)(2).

(2) U.S. Patent Publication No. 2019/0067306A1 (“Fang”). Fang was filed on August 24, 2017 and was published on February 28, 2019. Fang, Cover. Fang is prior art under 35 U.S.C. § 102(a)(2).

(3) U.S. Patent Publication No. 2017/0062470A1 (“Han”). Han was filed on August 26, 2016 and claims priority to a Korean patent application filed on August 28, 2015. Han, Cover. Han is prior art under 35 U.S.C. §§ 102(a)(1)-(a)(2).

(4) U.S. Patent Publication No. 2017/0294384A1 (“Chen”). Chen was filed on April 12, 2016 and was published on October 12, 2017. Chen, Cover. Chen is prior art under 35 U.S.C. § 102(a)(2).

Petitioner challenges the claims on the following grounds:

Ground 1: Claims 1-2, 4-5, 9-18 are obvious over Kim in view of a POSITA’s knowledge;

Ground 2: Claims 1-18 are obvious over Kim in view of Fang.

Ground 3: Claims 1-15 are obvious over Han in view of Fang.

Ground 4: Claims 17-18 are obvious over Han in view of Fang and in further view of Chen.

IV. INSTITUTION SHOULD BE GRANTED

Petitioner has established a reasonable likelihood of success on the merits. All other requirements for IPR have been met. The Board should institute IPR.

A. There are No Grounds for a § 314 Discretionary Denial in this Case

The PTAB “will not ... discretionarily deny institution in view of parallel district court litigation where a petition presents compelling evidence of unpatentability.” 6/21/22 Interim Procedure, 2, 4-5. Petitioner presents a compelling case here.

Petitioner also notes that the factors considered by the Board when assessing IPR institution in light of a parallel proceeding collectively weigh in favor of institution. *See Apple Inc. v. Fintiv, Inc.*, Case No. IPR2020-00019, Paper No. 11 (PTAB Mar. 20, 2020) (precedential).

1. Possibility of a Stay

Petitioner intends to seek a stay if the Board institutes IPR. This factor is neutral. *See Sand Revolution II, LLC v. Continental Intermodal Grp. – Trucking LLC*, IPR2019-01393, Paper 24, 7 (PTAB June 16, 2020) (informative); *Fintiv*, 6-9, 12 (similar).

2. Proximity of the Court’s Trial Date

On September 18, 2024, the district court entered a scheduling order which set a trial date of June 15, 2026. *See* Ex. 1029. If IPR is instituted, it should be completed before this date. *See also* Ex. 1030 (indicating an average of 48.9 months to trial). This weighs strongly in favor of institution.

3. Investment in the Parallel Proceeding

To date, the parties and Court have invested very little in the parallel proceeding. Indeed, beyond engaging in some motion practice regarding the pleadings and consolidation, little substantive progress has been made. See §II.B. Virtually no progress has been on the Wave 3 patents (which includes the '276 patent). The parties have just completed the exchange of contentions for the Wave 3 patents (from the YMTC2 case) but have not taken any depositions in the entire Co-Pending Litigation. Fact discovery is in its infancy. No claim construction positions have been exchanged for the Wave 3 patents, no claim construction order has issued, no infringement or invalidity expert discovery has occurred, and no summary judgment motions have been filed. This weighs in favor of institution. See *Sand Revolution*, 10-11.

The Board also has explained that institution is appropriate where “the petitioner filed the petition expeditiously....” *Fintiv*, 11. Here, on July 12, 2024, PO asserted eleven Wave 3 patents against Petitioner, and later asserted 149 claims across those patents. Ex. 1031. Petitioner proceeded with diligence, starting the filing of eleven petitions approximately three months after being served with the YMTC2 complaint. Ex. 1032. This also weighs strongly in favor of institution.

4. Issue Overlap

Should the Board institute, Micron stipulates that it will not advance, in

District Court, any ground asserted in this Petition. This eliminates any potential issue overlap between these proceedings and in District Court. The Board has found that such stipulations weigh in favor of institution. *Sand Revolution* at 11-12.

5. Party Overlap

Both Petitioner and PO, as is typical, are parties in the parallel proceeding.

6. Other Circumstances

Here, the Petition has significant substantive merit. It is premised on clear, understandable prior art that the Patent Office did not previously consider. Thus, this factor also weighs in favor of institution.

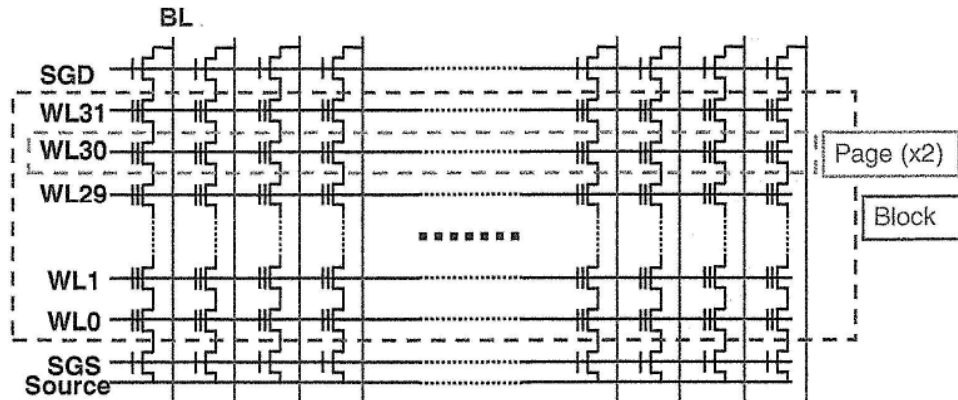
B. Denial Under §325(d) Would Be Inappropriate

The Examiner did not consider Kim, Fang, Han, or Chen, and thus denial under §325(d) would be inappropriate. Ex. 1001, Cover. Moreover, Kim discloses the alleged point of novelty in the specification (an etch-stop layer on the staircase) and, at least under PO's broad interpretation, the reason for allowance (a high-k dielectric etch-stop layer). §§VI, IX.A. And either Kim or Han in view of Fang squarely discloses the alleged point of novelty and reason for allowance under the correct construction. §§IX.A-IX.C. At bottom, Fang demonstrates that a high-k etch stop does not distinguish the prior art.

V. TECHNOLOGY BACKGROUND

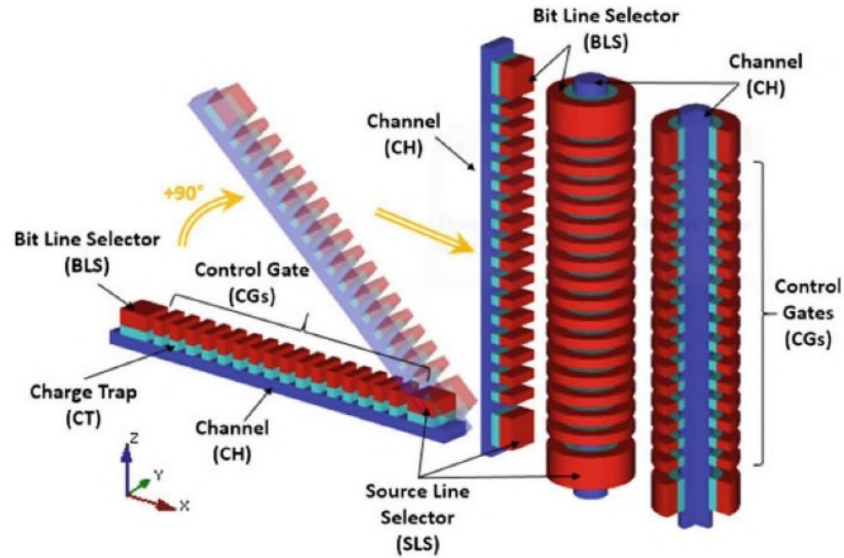
The '276 patent and the prior art discussed in this Petition relate to fabricating three-dimensional (3D) memory devices. Banerjee ¶ 46.

NAND memory cells are arranged in “strings.” Ex. 1010, 38. Early devices were formed as two-dimensional cell arrays on a substrate. *Id.*, 58; Banerjee ¶ 47.

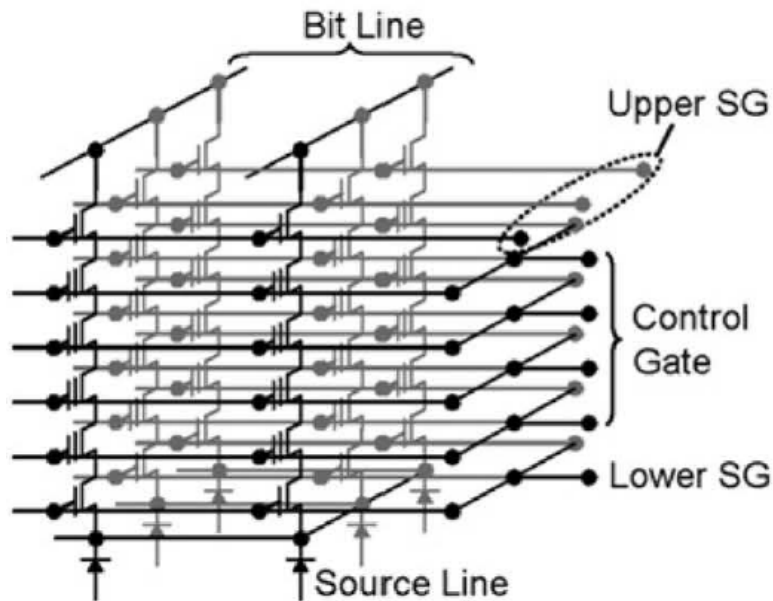


Ex. 1010, 40.

“Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block” and “turning the 2D NAND string upside,” “resulting” in a “3D structure” with a “vertical channel.” Ex. 1011, 3.

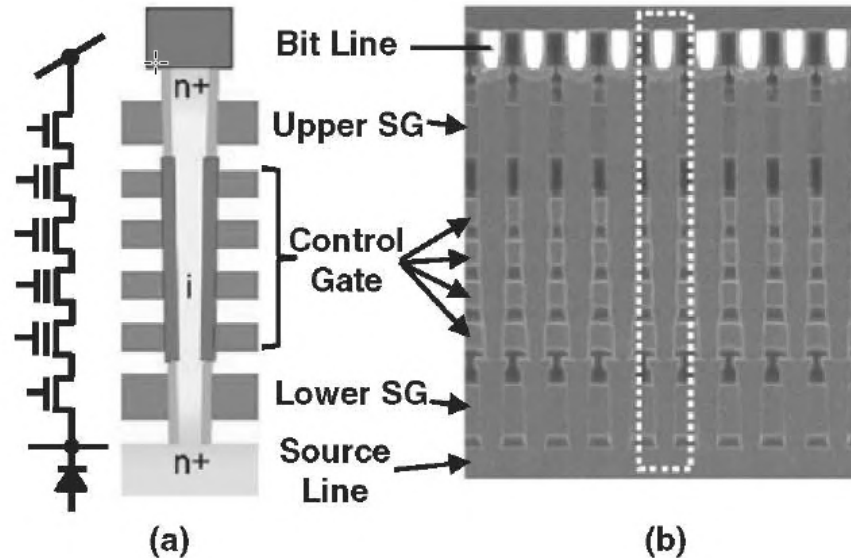


Ex. 1012, 122 (colors in the original). Multiple vertical channels are repeated in a three-dimensional array:



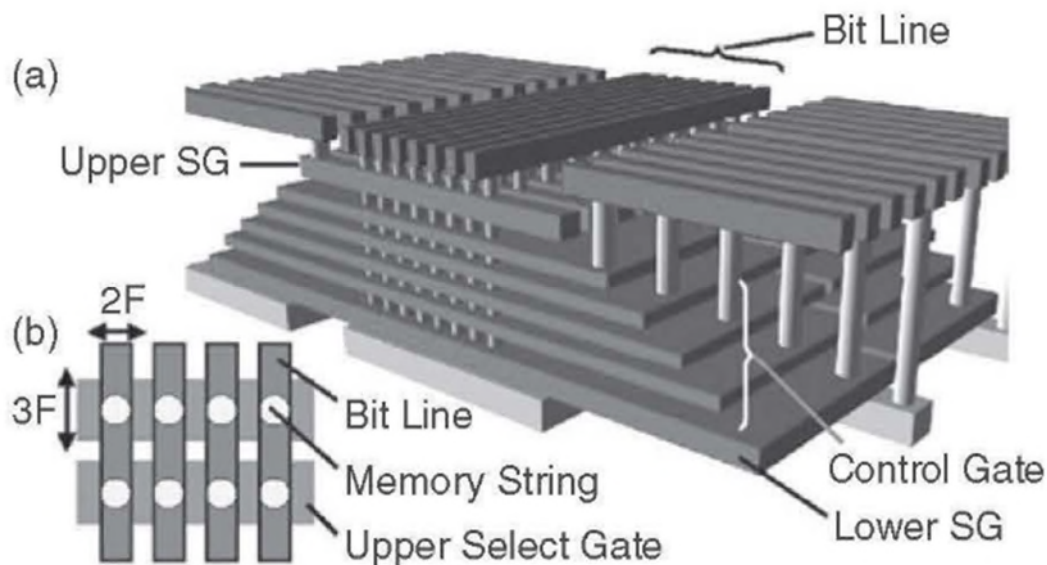
Ex. 1010, 296. Access operations, *e.g.*, a read operation, involves applying voltages to the control gate (also known as a word line). Banerjee ¶ 48. A memory cell “is

located in the intersection of a control gate plate” and the channel of the string. Ex. 1010, 295-96. An example 3D vertical-memory-cell string is shown below:



Ex. 1010, 296; Banerjee ¶ 49.

3D NAND memory includes “multi-stacked layers of [control] gate (plate)” material alternated with “dielectric” (*i.e.*, insulator) in a “[s]tack.” Ex. 1010, 294. “Each” layer of “electrode plate acts as a control gate.” *Id.* “[T]he control gates ... are connected ... [in a] stair-like gate structure.” *Id.*, 295-97.

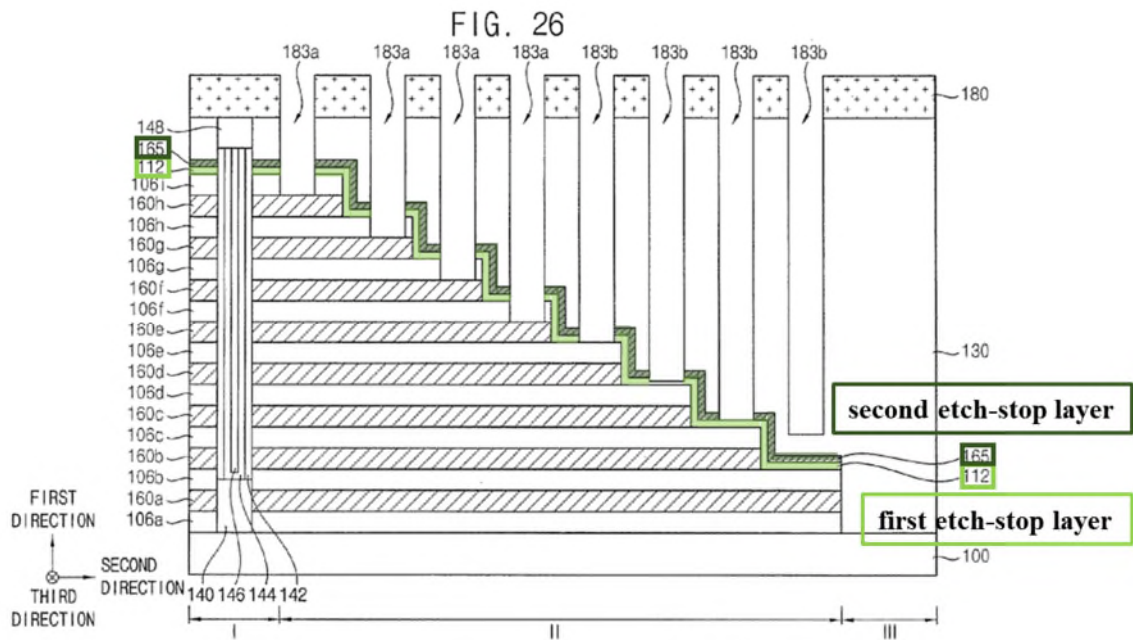
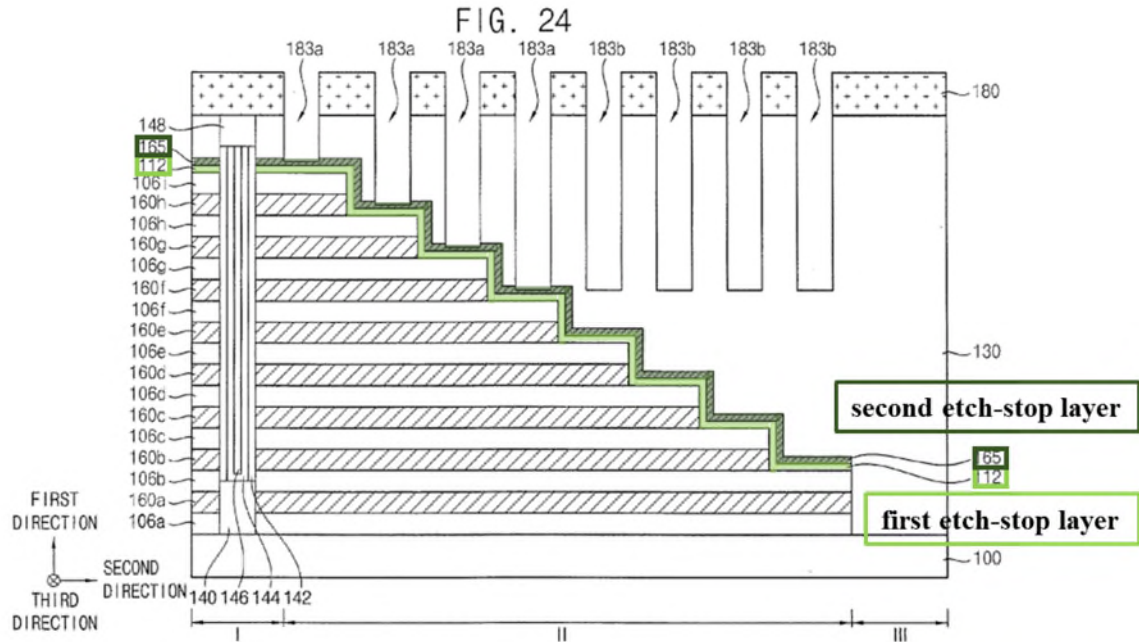


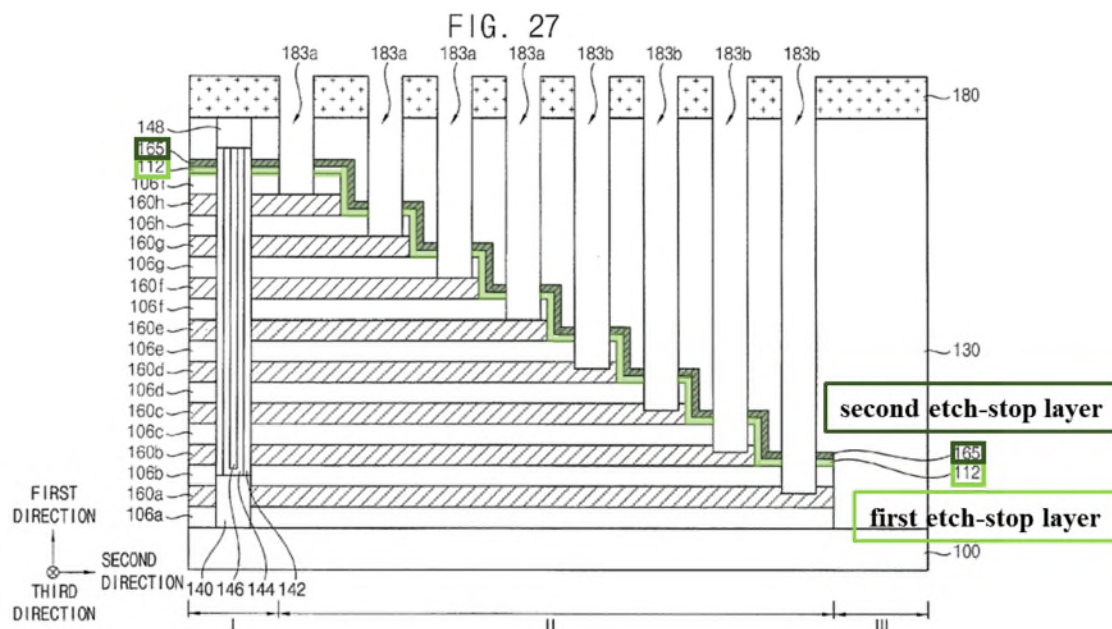
Ex. 1010, 296 (Fig. 7.6). The staircase provides landing areas on the control gates for contacts with vertical conductive structures to couple the control gates to control voltages. *Id.*, 298; Banerjee ¶ 50.

As shown in the figure above, the vertical conductive structures contacting the different control-gate plates have various lengths. The '276 patent and the prior art address the challenge of fabricating these structures in a reliable and cost-effective manner. Banerjee ¶ 51.

Specifically, the vertical conductive structures are formed by etching holes through an insulating layer above the staircase and depositing a conductive material within. Techniques were developed to etch holes to their respective lengths. Ex. 1001, 5:58-60. One such technique is to place one or more etch-stop layers above the staircase. The etch-stop layers have a lower etching rate than the insulating layer. As shown below, upon reaching the etch-stop layers, etching slows down, protecting

the underlying layers and preventing over-etching shallower holes while etching deeper holes. Fang, [0008], [0028].





Ex. 1013, Figs. 24, 26-27; Banerjee ¶¶ 52-53.

More generally, a layer (“layer 2”) functions as an etch-stop layer when its etching rate is lower than that of the layer immediately above (“layer 1”).³ This is known as selective etching, based on the relative etch selectivity of materials in the layers. Ex. 1014, 220, 390. Etch selectivity depends on the etchant: layer 1 may have a higher etching rate than layer 2 when one etchant is used, but a lower etching rate when a different etchant is used. These conventional processes were known as “selective etching” and “reverse selective etching.” Ex. 1015, 4, 6 (internal

³ This implies that layers 1 and 2 cannot be the same material if layer 2 is to function as an etch-stop layer because the same material will have the same etching rate.

quotation marks omitted). Using different etchants allows greater flexibility in the choices of materials to use as an etch stop. Banerjee ¶¶ 54-55.

VI. THE '276 PATENT AND ITS PROSECUTION HISTORY

The '276 patent relates to forming “word line contact structures” for 3D memories. Ex. 1001, Abstract. As shown below, the word-line contact structure is the landing area in which a vertical conductive structure 945 contacts a particular step. The '276 patent discloses a conventional staircase structure 900 with alternating gate stacks 525 and dielectric layers 104:

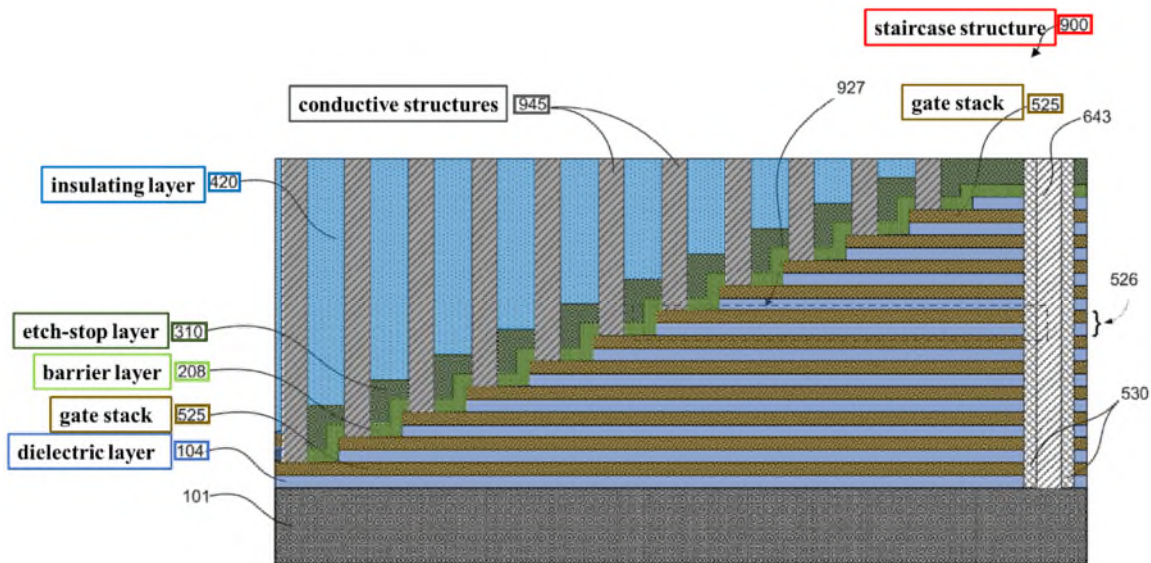


FIG. 9A

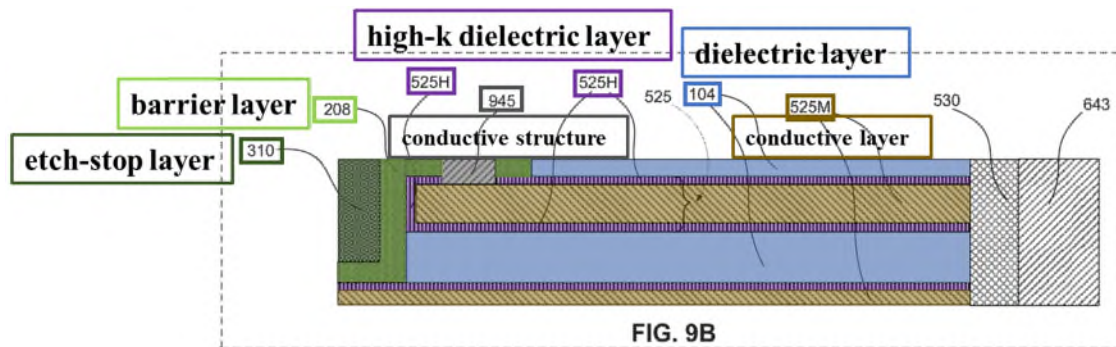
Ex. 1001, Fig. 9A, 8:60-61. An optional barrier layer 208 and an etch-stop layer 310 cover the exposed surfaces of each step. *Id.*, 5:61-6:5, 7:36-45, 7:62-64, 8:5-9. An insulating layer 420 is disposed on the etch-stop layer 310. Conductive structures 945 (*i.e.*, staircase contacts) penetrate the insulating layer 420, the etch-stop layer

310, and the barrier layer 208, and contact the gate stacks 525. *Id.*, 10:60-67, 11:17-22; Banerjee ¶ 56.

In this context, the optional barrier layer is simply an additional etch-stop layer. Banerjee ¶ 57. Consistent with background concepts (§V), the '276 patent states that relative etch selectivity is what enables a layer to “function as an etch-stop layer,” *i.e.*, to slow down etching to protect the underlying layers. Ex. 1001, 7:1-6. The only statement in the patent regarding the function of the barrier layer describes it as an etch-stop: “protecting the underlying structure during subsequent *etching* processes.” *Id.*, 7:42-45 (emphasis added). The descriptions of insulating layer 208, which is not necessarily a barrier layer (*id.*, 7:41-45), confirms that, for the '276 patent, a barrier layer is just another etch-stop layer. For example, the second insulating layer and the etch-stop layer are formed sequentially to the same step shape and have the same thickness characteristics. *Id.*, 7:36-40, 7:45-50, 7:62-64, 8:9-16. Further, when the barrier layer is absent, the etch-stop layer would substitute for it structurally. *Compare id.*, 8:6-12 with 7:36-40. Tellingly, when present, the barrier layer simply does what an etch-stop layer would do in its absence with respect to protecting the structure during etching. *Id.*, 8:62-9:3. Both layers comprise an insulating material. *Id.*, 7:57-58. But, consistent with the barrier layer’s role as an etch stop, the two layers have different materials. *Id.*, 8:3-5; §V. Both have an etching rate needed for etch stopping, *i.e.*, a rate lower than that of the layer

immediately above. Ex. 1001, 9:66-10:1, 10:49-51; §V. Thus, both serve the same purpose, *i.e.*, to protect the underlying layers from over-etching. Ex. 1001, 6:1-3, 7:42-45, 10:9-19; Banerjee ¶ 57.

Each gate stack 525 may comprise a conductive layer 525M at the core surrounded on three sides by a high-k dielectric layer 525H:



Ex. 1001, Fig. 9B, 9:4-10. The conductive structure 945 penetrates the layers above the conductive layer 525M to form a contact to the control gate. *Id.*, 10:60-67, 11:17-25; Banerjee ¶ 58.

The '276 patent asserts that by using an etch-stop layer, the staircase contacts may be formed simultaneously with a single lithography mask, while also preventing over-etching. Ex. 1001, 5:47-6:5.

During prosecution, the Examiner rejected various claims under §103 over Shin, Nam, and Kim '222. Ex. 1002, 90-95. The Examiner found claims 4, 7, and 18 allowable if rewritten in independent form. *Id.*, 95. Notably, the Applicant then amended claim 1, adding the allowable features of claim 7, requiring that “the etch-stop layer comprises a second high-k dielectric layer.” *Id.*, 114, 118. With

Applicant's authorization, the Examiner canceled pending claim 6, which required the etch-stop layer to comprise a material that is not a high-k dielectric, and allowed the remaining claims 1-5 and 8-20. *Id.*, 115, 128; Banerjee ¶ 60.

What the Applicant failed to acknowledge in the specification or during prosecution, however, is that every aspect of its alleged invention, including the second high-k dielectric layer that secured allowance, was conventional by the time of the application was filed, as this Petition demonstrates. Banerjee ¶ 61.

VII. CLAIM CONSTRUCTION

The Board in IPR proceedings applies the same *Phillips* claim construction standard used in district court cases. *See Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005). For purposes of institution, Petitioner submits that all terms of the '276 patent's claims may be afforded their plain and ordinary meaning. Banerjee ¶ 62.

For clarity, Petitioner submits that the plain and ordinary meaning of "high-k dielectric" on the priority date of the '276 patent is a dielectric whose dielectric constant is higher than that of silicon nitride. Ex. 1022, [0051] ("a high-k film ... refers to a film having a dielectric constant (permittivity) higher than that of silicon nitride."); Ex. 1001, 8:16-20 ("etch-stop layer 310 can be made of *silicon nitride*, silicon oxynitride, spin-on-dielectric, *and/or high-k dielectric films....*") (emphasis added). Banerjee ¶¶ 94-95.

VIII. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA in the field of the '276 patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (*e.g.*, researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience). This POSITA would have been aware of and generally knowledgeable about 3D NAND's structure, how it is manufactured, and its component parts. Banerjee ¶ 42.

IX. DESCRIPTION OF THE PRIOR ART

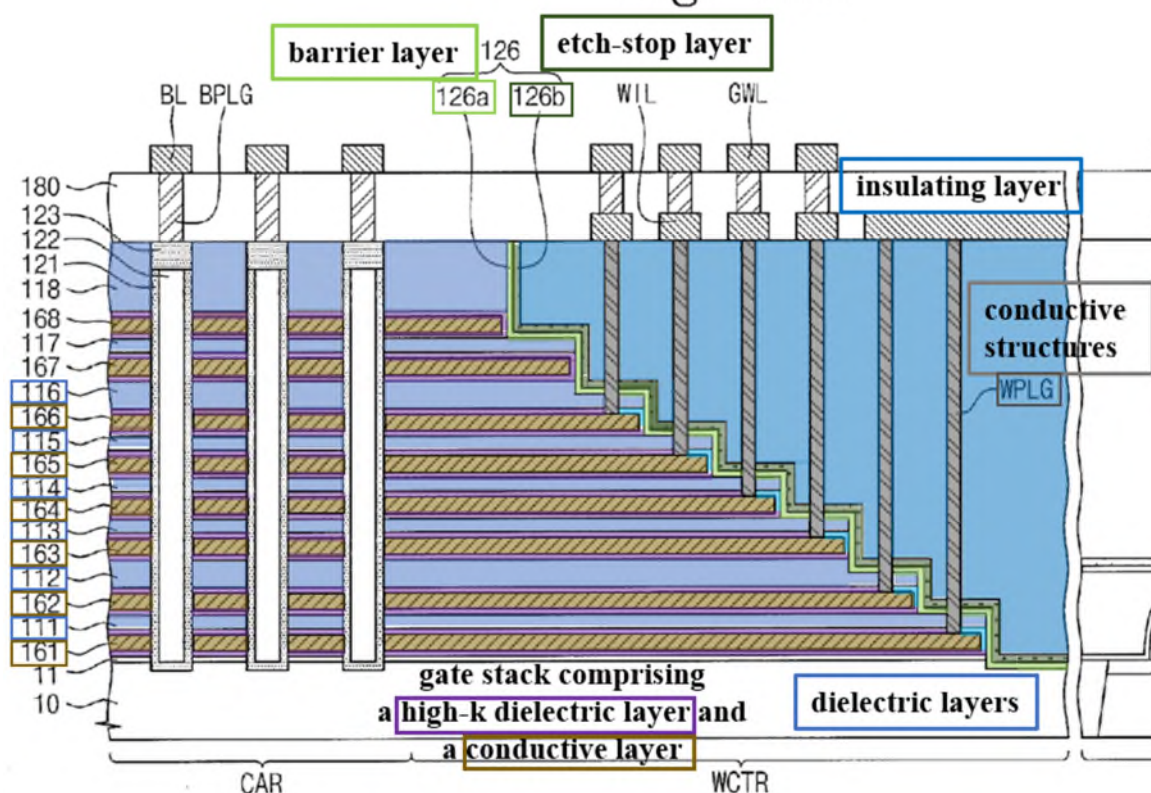
The prior-art references are analogous to the '276 patent, *e.g.*, they are in the same field of endeavor of improving 3D memory devices. Banerjee ¶ 65.

A. Kim

Kim discloses methods of manufacturing a 3D semiconductor memory device with a cell-array region, a peripheral-circuit region, and a word-line contact region WCTR disposed therebetween. Kim, Abstract, [0037]. Kim focuses on issues relating to the interlayer dielectric (analogous to the insulating layer of the '276 patent). *Id.*, [0024]-[0025]; Banerjee ¶¶ 66-67.

Kim's Figure 22A depicts a 3D NAND device with an etch-stop layer, a barrier layer, and other structures relevant to the '276 patent:

Fig. 22A



Kim, Fig. 22A; Banerjee ¶ 68.

Kim discloses a silicon-nitride etch-stop layer, which under PO's apparent interpretation, is a high-k dielectric. Ex. 1019, 9; Banerjee ¶ 69. As noted below, both Fang and Chen squarely disclose a high-k etch-stop layer as a POSITA would understand that term. §§IX.B, IX.D.

Kim discloses embodiments in which a sacrificial layer is disposed over a dielectric layer at each step, even though its figures show the opposite order. After describing the layer ordering in its figures, Kim discloses that “[i]n other embodiments, each of top surfaces of the sacrificial layers SC1 to SC8, not the top surfaces of the insulating layers 111 to 118, may be partially exposed in the word

line contact region WCTR.” Kim, [0090]. More specifically, the edge portions of the sacrificial layers SC1-SC8 may be exposed as the top surfaces of the steps. *Id.*, [0091], [0240]. Accordingly, Kim discloses disposing a sacrificial layer over a dielectric layer at each step. Banerjee ¶ 70.

B. Fang

Fang discloses methods of forming a 3D semiconductor memory device with a staircase structure. Fang, [0001]-[0002]. The device further comprises a silicon-nitride etch-stop layer and an oxide insulating layer. *Id.* Conductive word-line structures contacting the conductive layers are formed in openings through the insulating layer, the etch-stop layer, and the dielectric layers:

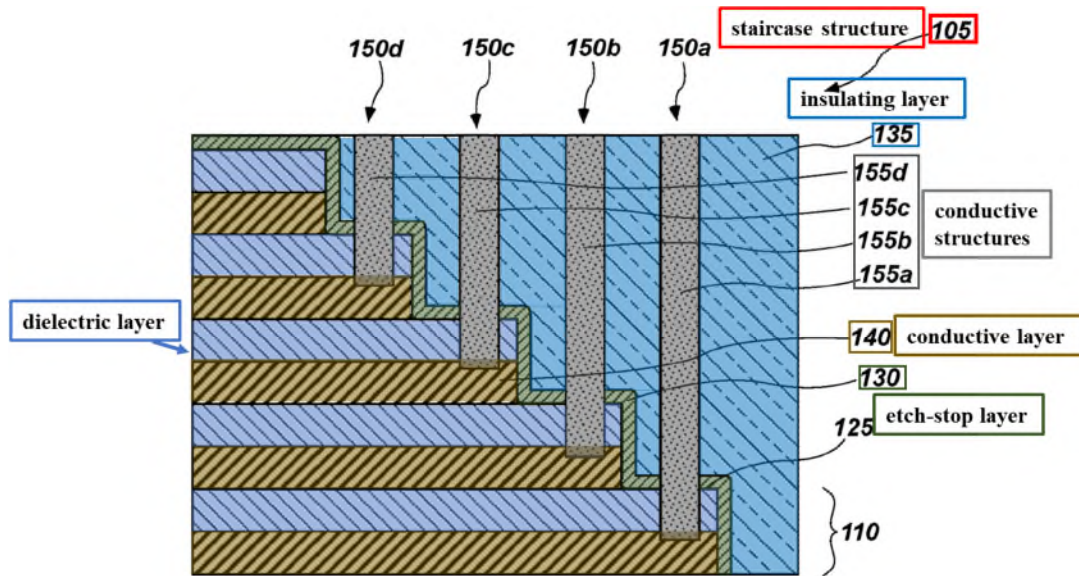


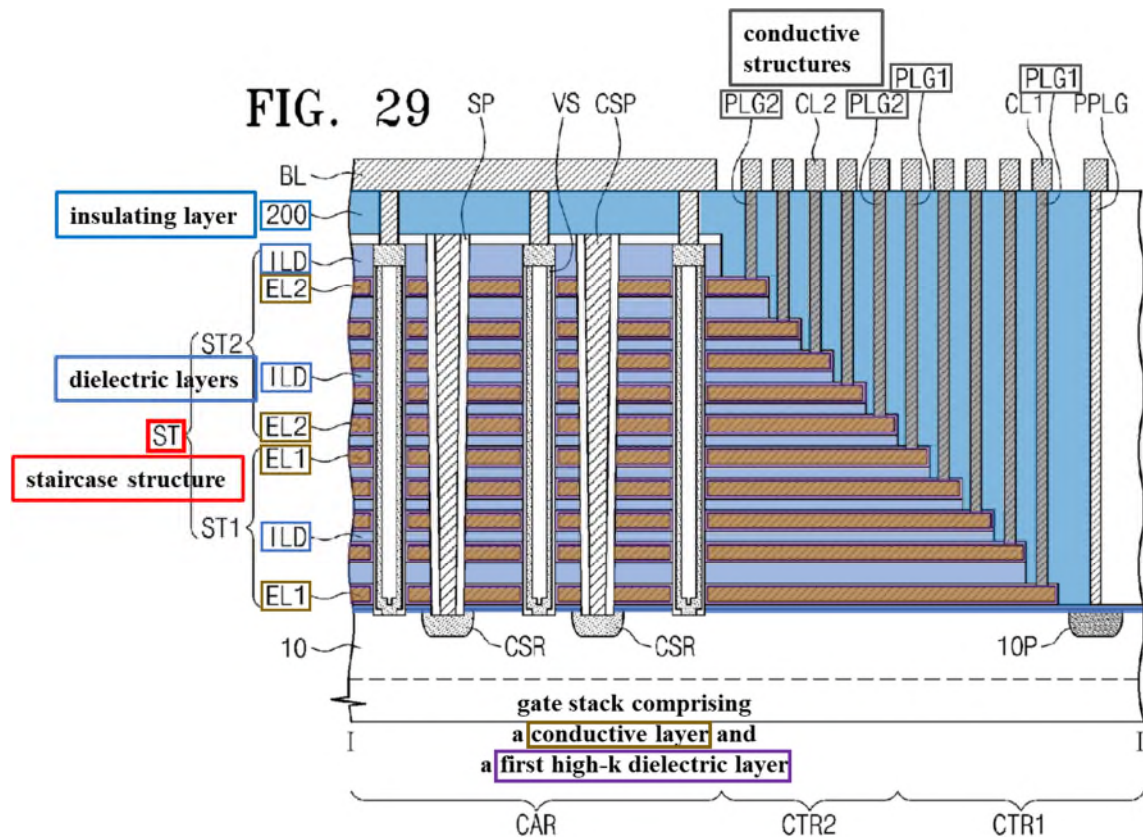
FIG. 6

Fang, Fig. 6.

Notably, Fang discloses: “Alternatively, the etch stop material ... may be a high-k dielectric material, such as hafnium oxide.” *Id.*, [0022]; Banerjee ¶¶ 71-73.

C. Han

Han discloses methods of forming a 3D semiconductor memory device with a staircase structure. Han, [0142], [0151]. The structure comprises alternating dielectric layers and gate stacks comprising high-k dielectric layers surrounding conductive layers. *Id.*, [0096], [0118]-[0120], [0134]-[0141]. Conductive structures contacting the conductive layers are formed in openings through an insulating layer and the high-k dielectric layer:



Han, Fig. 29. Banerjee ¶¶ 74-75.

D. Chen

Chen discloses manufacturing methods of forming 3D memory devices comprising “stack structure, an etching stop layer, and a conductive structure.” Chen, Abstract, [0027]-[0029]. The dielectric and conductive layers in the stack structure may be positioned above or below each other at each step. *Id.*, Figs. 7A-7B, [0045]-[0046]. The etch-stop layer may comprise a single layer or be divided into two layers. *Id.*, [0037]. A two-layer configuration is shown below:

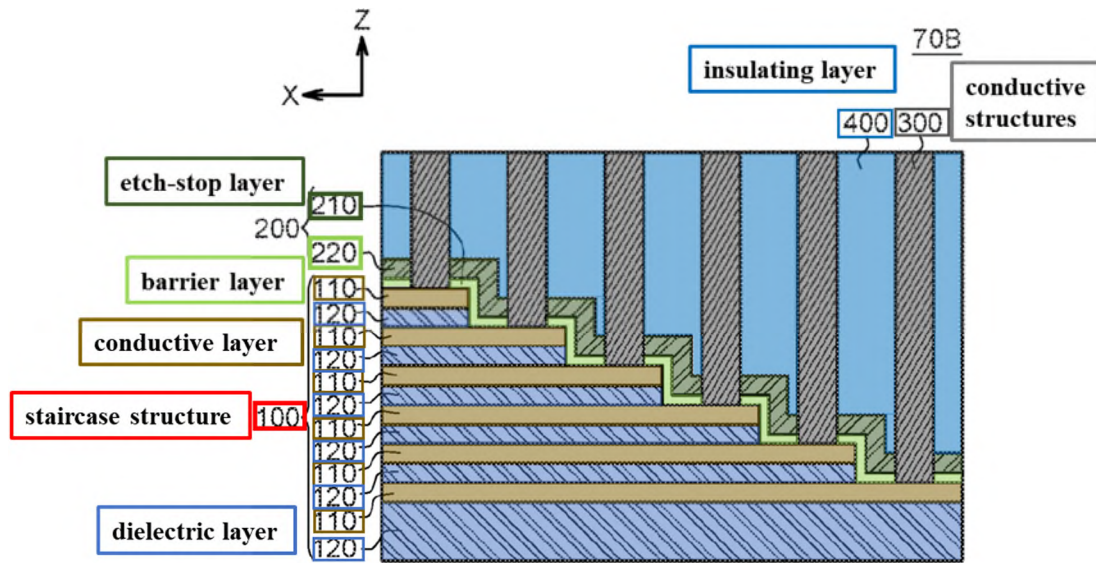


FIG. 7B

Chen, Fig. 7B. Notably, in the single- or two-layer configuration, the etch-stop layer (*e.g.*, the upper layer in the two-layer configuration) may comprise a high-k dielectric. *Id.*, [0041], [0048]-[0049]. Having a high-k dielectric or having two layers increases the tunneling length of the etch-stop layer(s), resulting in increased electrical isolation between the conductive layers and increased device stability. *Id.*, [0004], [0049], [0053]; Banerjee ¶¶ 76-78.

X. GROUND 1: KIM IN VIEW OF A POSITA'S KNOWLEDGE

Ground 1 applies PO's interpretation of "high-k," and Ground 2 applies Petitioner's interpretation. Banerjee ¶ 79.

Grounds 1 and 2 rely on Kim's Figures 17A-22B embodiment comprising an etch-stop layer and a barrier layer. Kim discloses other embodiments, *e.g.*, Figures 5A-14B.

A POSITA would have understood that descriptions of one of Kim's embodiments apply to other embodiments except where the embodiments differ. Banerjee ¶¶ 80-81. Closely related embodiments with many of the same elements are denoted by the same reference numerals. Kim, [0184]. For example, the embodiments shown in Figures 5A-14B and in Figures 17A-22B are closely related. Thus, Kim states that overlapping descriptions of the same elements are omitted in the descriptions of Figures 17A-22B. *Id.* Further, the descriptions of Figures 17A-22B extensively reference Figures 9A-14B. *Id.*, [0183]-[0212]. Similarly, as another example, descriptions of Figures 26-27 refer to the two embodiments in Figures 17A-22A and 8A-11A. *Id.*, [0221], [0223]-[0224].

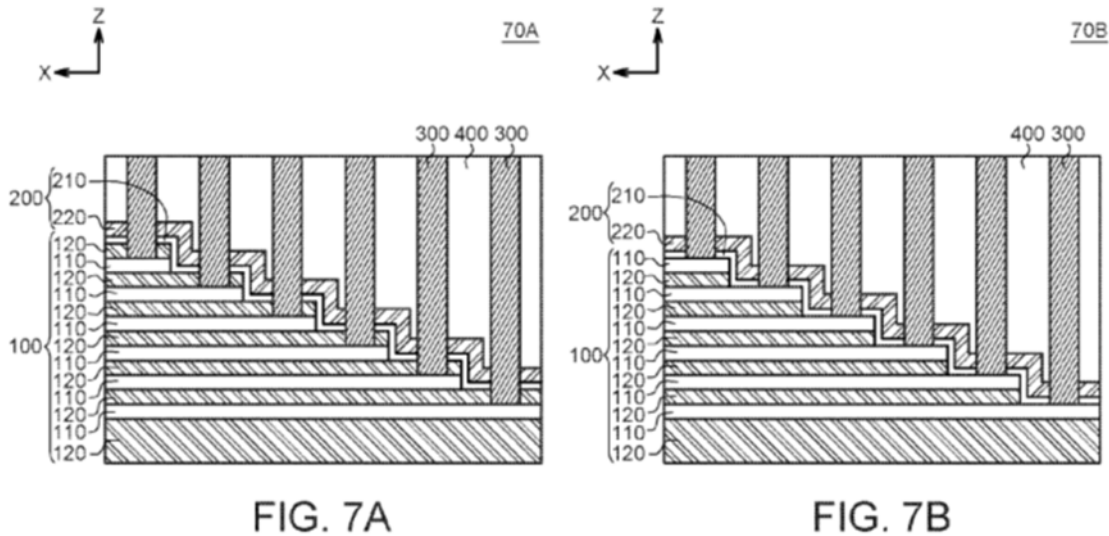
A. Kim Discloses “Disposing a Sacrificial Layer over a Dielectric Layer”

As a preliminary matter, sacrificial layers are replaced with, and positionally correspond to, gate stacks in the fully formed claimed semiconductor structure. §X.B.5. Thus, “disposing a sacrificial layer over a dielectric layer” results in a structure whose gate stack is disposed over a dielectric layer. Banerjee ¶ 82.

Kim discloses the sacrificial-layer-on-top/gate-stack-on-top ordering even though its figures show the opposite order. §IX.A. This teaching of the gate-stack-on-top layer ordering applies to the Figure 17A-22B embodiment. §X (Kim's descriptions apply to common aspects across embodiments); Banerjee ¶ 83. Kim's teaching at least renders the limitation obvious. *Chamberlain Grp., Inc. v.*

Techtronic Indus. Co., 935 F.3d 1341, 1350 (Fed. Cir. 2019) (a reference invalidates if it enables a POSITA to “at once envisage” “the claimed arrangement”).

Additionally, a POSITA would have known that either order was a common alternative. For example, Chen discloses both orders side-by-side:



Chen, Figs. 7A (dielectric on top), 7B (conductor on top), [0044]-[0046]. Yu also teaches that the layers may be formed in either order. Ex. 1009, [0034]-[0035]. A POSITA would have known that either order was routine, highly predictable, and would have had a reasonable expectation of success for implementing a gate-stack-on-top embodiment.

At a minimum, Kim’s teaching on reversing the order represents a “known technique” that is at least “a *suitable* option” for the Figure 17A-22B embodiment. *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023) (emphasis in original); Banerjee ¶¶ 84-85.

Below, Kim's figures are modified to show this sacrificial-layer-on-top/gate-stack-on-top ordering. Based on Kim's express teaching and a POSITA's knowledge, a POSITA would have "at once envisage[d]" "the claimed arrangement." *Chamberlain Grp.*, 935 F.3d at 1350; Banerjee ¶¶ 86-87. For example, prior-art references with gate-stack-on-top configurations (two additional examples below) would have helped a POSITA visualize a Kim embodiment with gate stacks on top:

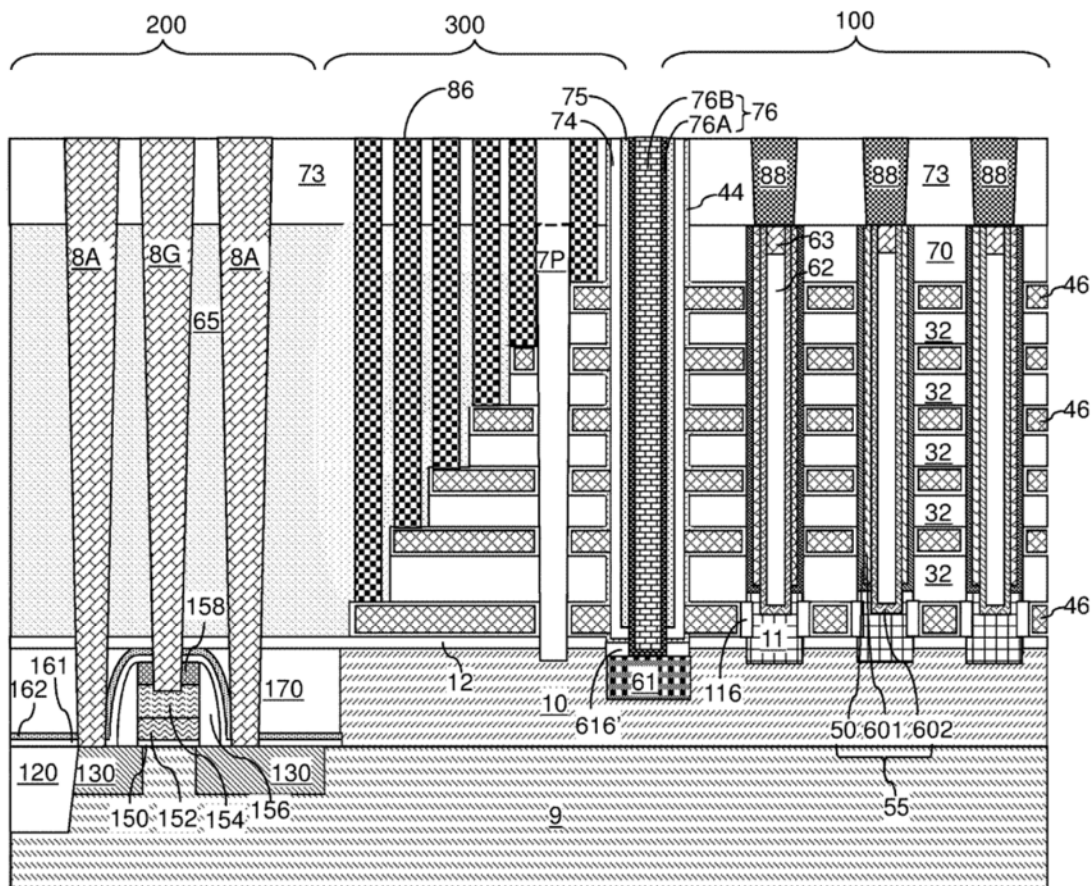
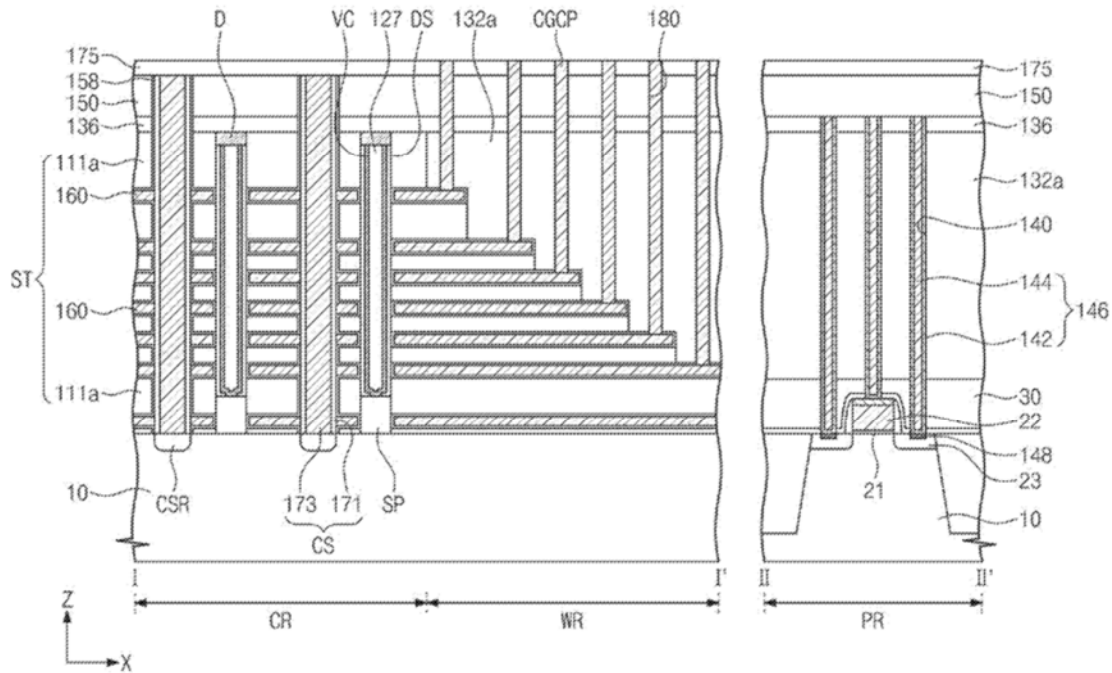


FIG. 13

Ex. 1016, Fig. 13.

FIG. 20



Ex. 1017, Fig. 20.

For clarity, the modified Kim figures are annotated with “Gate-Stack-on-Top.”

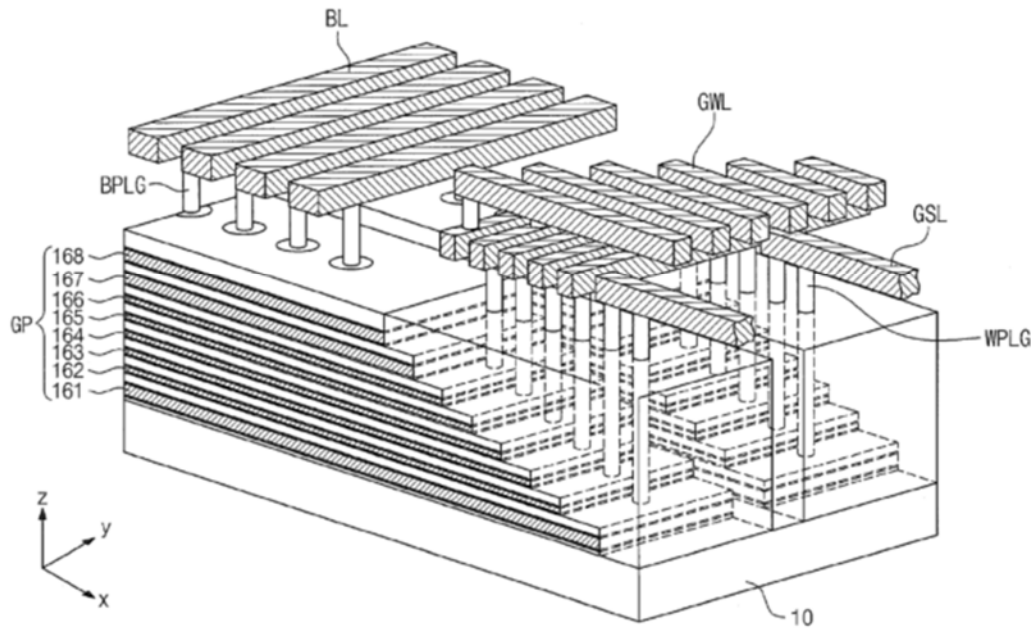
B. Claim 1:

- 1. [1.PRE] “A method for forming a semiconductor structure, comprising:”**

Kim discloses *[a] method for forming a semiconductor structure, e.g., “methods of manufacturing a three dimensional semiconductor device.”*⁴ Kim, Abstract.

⁴ Red italics in the claim-mapping sections denote claim language.

Fig. 4

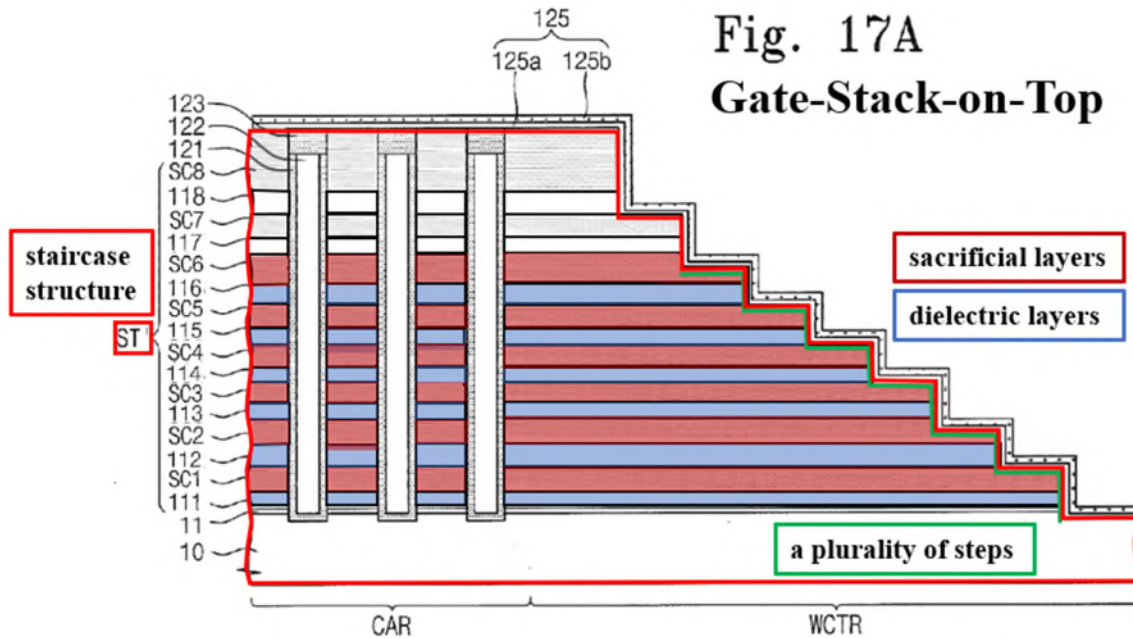


Kim, Fig. 4. Kim's Figures 17A-22A shows a structure at successive stages of manufacturing. *Id.*, [0183]; Banerjee ¶ 88.

2. [1.A] “forming a staircase structure having a plurality of steps, wherein the forming of each step of the plurality of steps comprises disposing a sacrificial layer over a dielectric layer;”

Kim at least renders limitation [1.A] obvious.

Kim's method comprises *forming a staircase structure* (“stepwise stacked layer structure ST”) *having a plurality of steps, wherein the forming of each step of the plurality of steps comprises disposing a sacrificial layer* (one of “sacrificial layers” SC1-SC6) *over a dielectric layer* (one of “insulating layers” 111-116):



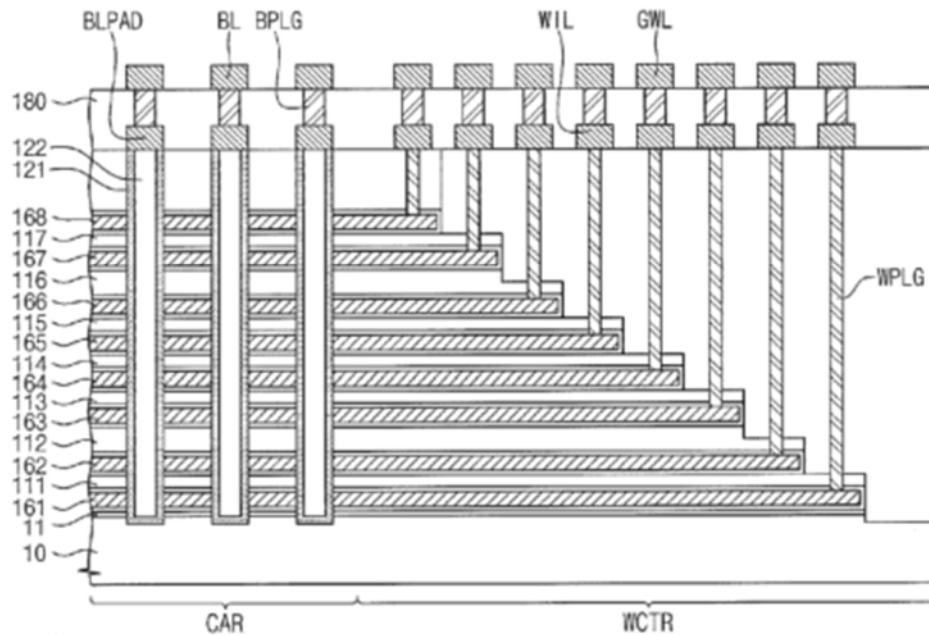
Kim, Fig. 17A, [0007]-[0008] (“a stepwise structure”), [0064] (forming a stacked layer structure comprising a plurality of insulating layers and sacrificial layers), [0086]; §X (description of Figures 5A-14B applies). Banerjee ¶¶ 89-90.

As shown above, the *plurality of steps* may be the bottom six steps. This is relevant to limitation [1.F], which requires “exposing ... the conductive layer of *each* step” of the plurality of steps to allow contacts between the conductive layers and the conductive structures. The *plurality of steps* need not include all steps of the *staircase structure*, because this limitation permits additional steps given the use of *having*. *Regents of the Univ. of Cal. v. Eli Lilly & Co.*, 119 F.3d 1559, 1573 (Fed. Cir. 1997). Relatedly, a parallel limitation of the parent ’711 patent further confirms the staircase structure may include additional steps. Banerjee ¶ 91.

Additionally, it would have been understood, and certainly obvious, that there are conductive structures not shown on the top steps, and the *plurality of steps* would then include all steps. This is because the channel structures are effectively a string of memory cells at the interface of the channel and the word lines (coupled to the conductive structures). And for various operations (*e.g.*, read operations) targeting a memory cell in the middle of the string, it is necessary to turn on all memory cells above and below the target cell by applying a voltage to their word lines (*i.e.*, gates).

§V. Put simply, the memory could not properly function without a contact to each gate layer. Indeed, usually the top gate layer is a select layer, *e.g.*, drain-select layer, to turn on the memory string. Not surprisingly, it was thus conventional for a staircase to have a conductive structure on every step. Fang, Fig. 6; Chen, Figs. 7A-7B. Indeed, Kim discloses such an embodiment, further demonstrating that it would have been understood, and obvious, to include a contact on the top steps:

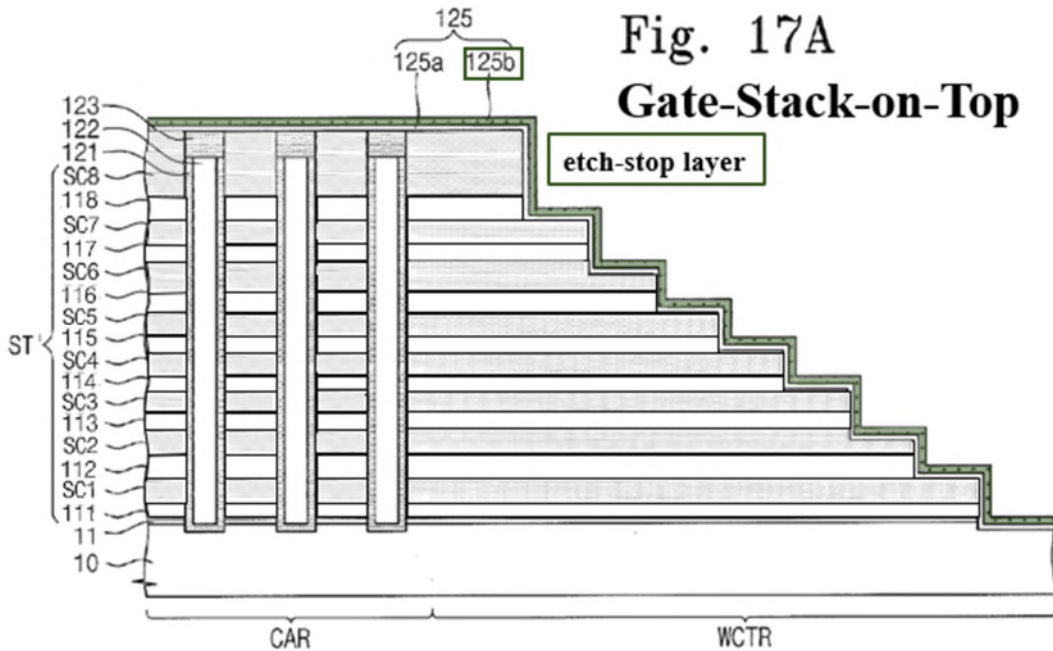
Fig. 30



Kim, Fig. 30; Banerjee ¶ 92. While Kim's figures do not annotate the top steps, Grounds 1-2 equally apply to including contacts on each step of the staircase.

3. [1.B] “disposing an etch-stop layer on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer;”

Kim discloses *disposing an etch-stop layer* (“second stop layer” 125b) *on each step of the plurality of steps*:



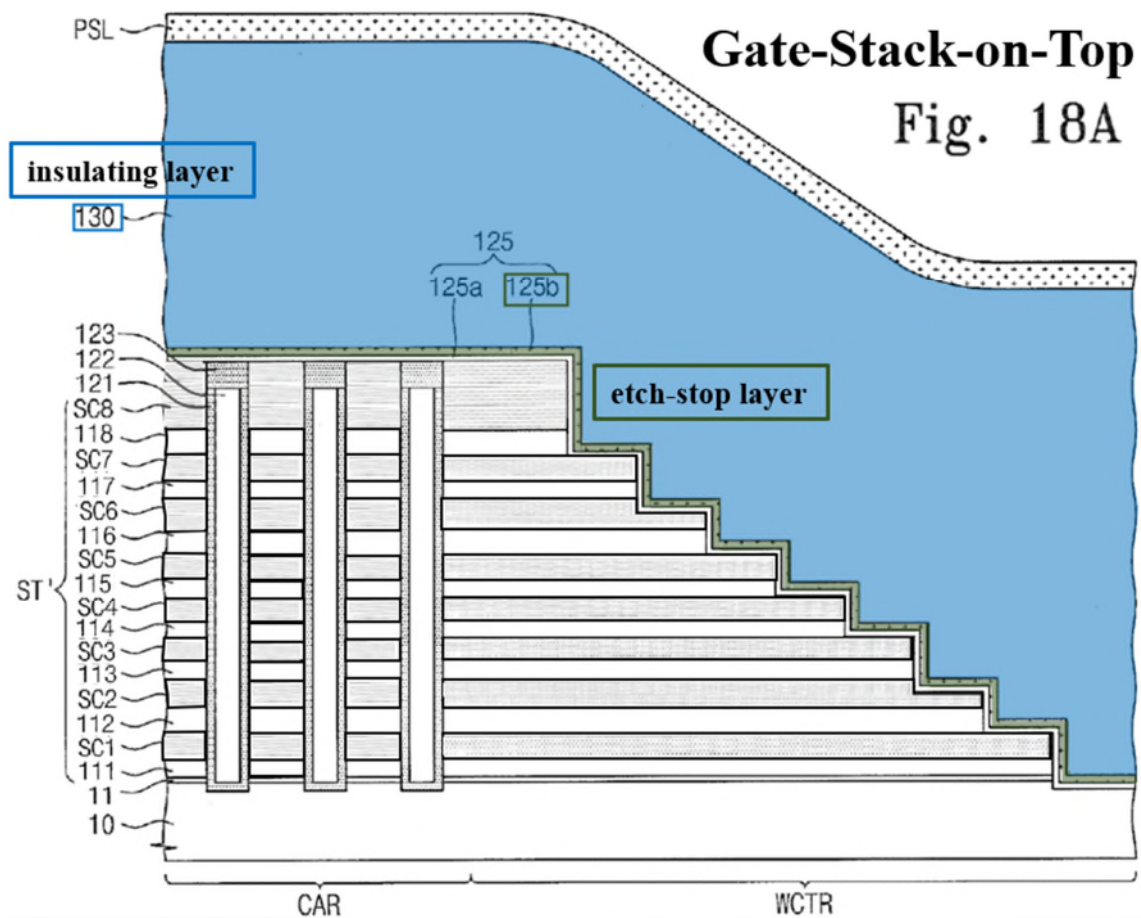
Kim, Fig. 17A, [0185] (forming an etch-stop layer after forming the stepwise stacked layer structure ST), [0213]. A POSITA would have understood the etch selectivity of the etch-stop layer to serve its purpose of preventing punch-through. *Id.*, [0186]-[0187]; Banerjee ¶ 93.

Kim further discloses that *the etch-stop layer comprises a second high-k dielectric layer* under PO's incorrect interpretation of high-k dielectric. Specifically, Kim's etch-stop layer may comprise silicon nitride, which, contrary to the '276 patent and a POSITA's knowledge, PO considers to be a high-k dielectric. Ex. 1019, 9 (PO alleging that "forming the etch-stop layer SiN" satisfies limitation [1.B]). In fact, Kim, too, defines silicon nitride to be a high-k material because its dielectric constant is higher than silicon oxide. Kim, [0186], [0064]; *but see* §VII (correct meaning).

To a POSITA, a high-k dielectric has a dielectric constant higher than that of silicon oxide and silicon nitride. Banerjee ¶¶ 94-95. Ground 2 demonstrates that Fang renders it obvious to employ an etch stop of an actual high-k material.

4. [1.C] “disposing an insulating layer on the etch-stop layer;”

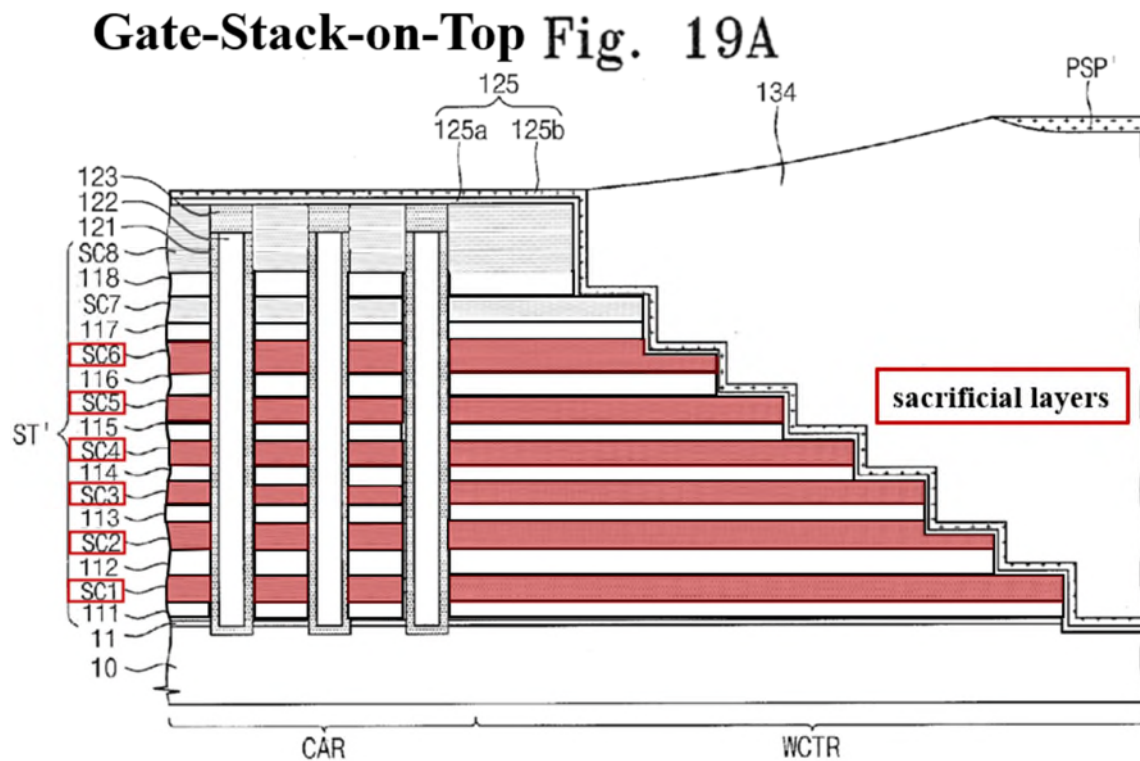
Kim discloses *disposing an insulating layer* (“interlayer dielectric” 130) *on the etch-stop layer* (“second stop layer” 125b):



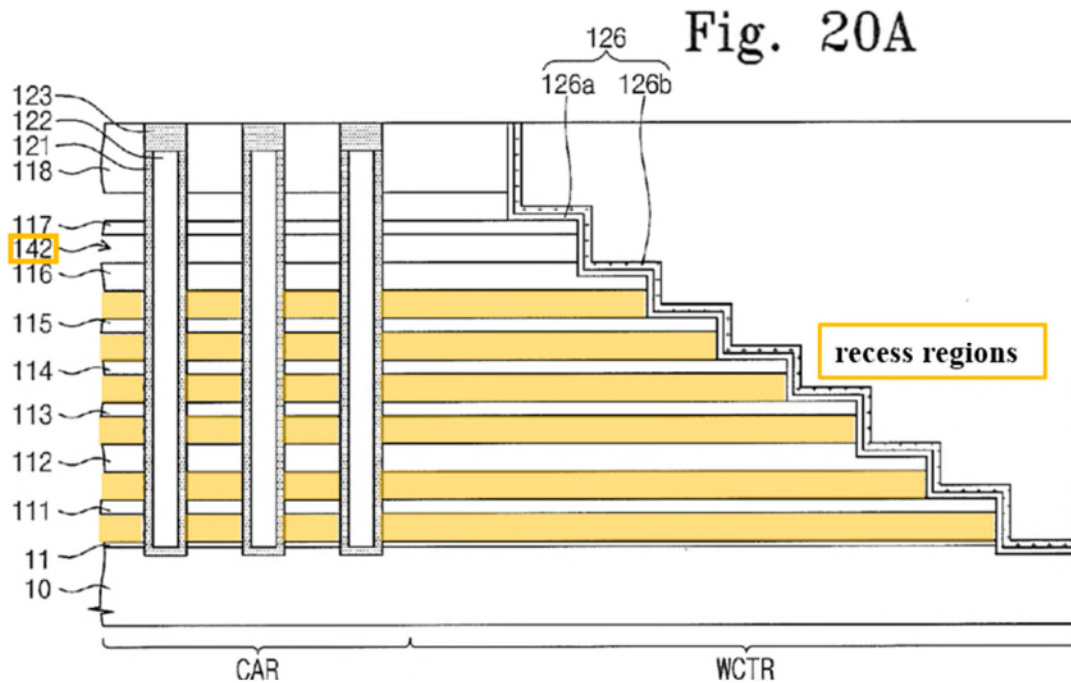
Kim, Fig. 18A, [0188] (“the interlayer dielectric 130 ... may be ... formed on the etch stop layer 125.”); *id.*, [0007]-[0008], [0094], [0097], [0213]; Banerjee ¶ 96.

5. [1.D] “replacing the sacrificial layer of each step with a gate stack, the gate stack comprising a conductive layer and a first high-k dielectric layer;”

As shown below, Kim discloses *replacing the sacrificial layer* (one of “sacrificial layers” SC1-SC6) *of each step with a gate stack*. Figure 19A shows the sacrificial layers:

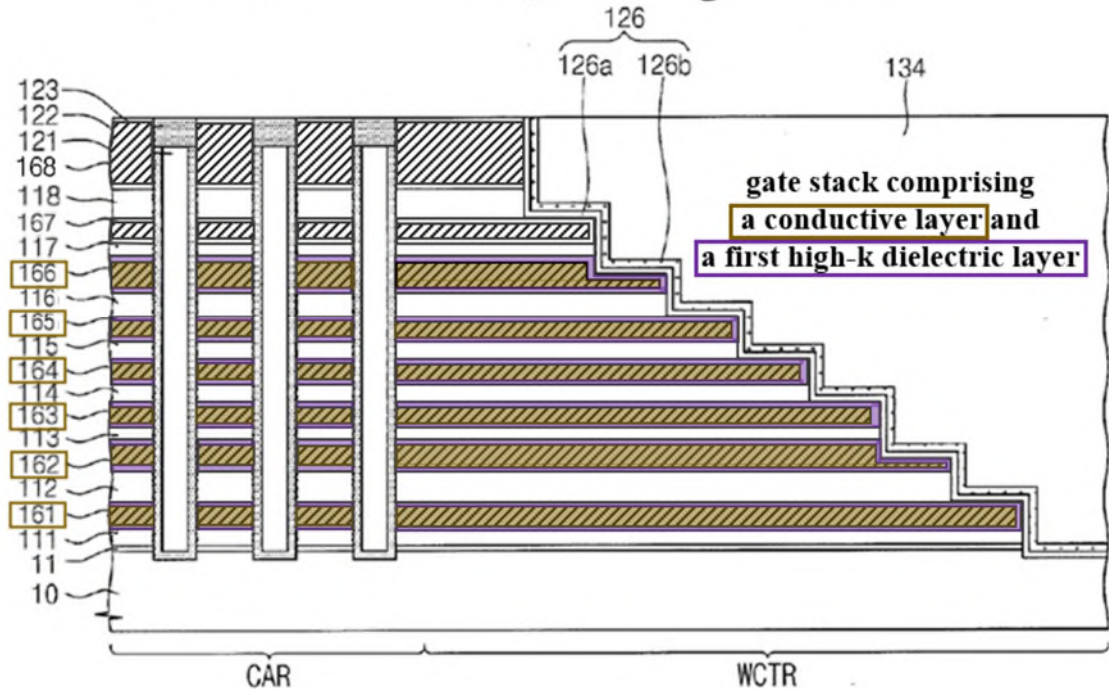


Kim, Fig. 19A. Figure 20A shows sacrificial layers having been removed, creating recess regions:



Kim, Fig. 20A, [0198]-[0200] (“selectively removing the sacrificial layers ... to form recess regions 142 between the insulating layers....”). Figure 21A shows *gate stack[s] [each] comprising a conductive layer* (one of “gate electrodes” 161-166) *and a first high-k dielectric layer* (“blocking insulating layer” in a “data storing layer”) formed in the recess regions, thereby *replacing the sacrificial layer of each step*.

Gate-Stack-on-Top Fig. 21A



Kim, Fig. 21A, [0200]-[0202] (“forming a data storing layer 150 and gate electrodes 161 to 168 in the recess regions 142.”), [0134]. The reverse layer ordering at each step does not impact this process. Banerjee ¶ 97.

Kim discloses that *the gate stack compris[es] a conductive layer*, which Kim calls a “gate conductive layer” or “gate electrode.” Kim, [0202].

Kim discloses that *the gate stack compris[es] ... a first high-k dielectric layer*, specifically, “a data storing layer 150” surrounding gate electrodes between insulating layers. *Id.*, [0200]-[0202], Figs. 13A-13B. The data-storing layer may include a blocking insulating layer, comprising *a first high-k dielectric* such as aluminum oxide. *Id.*, [0148], [0151], Figs. 15B-15D; Banerjee ¶¶ 98-99.

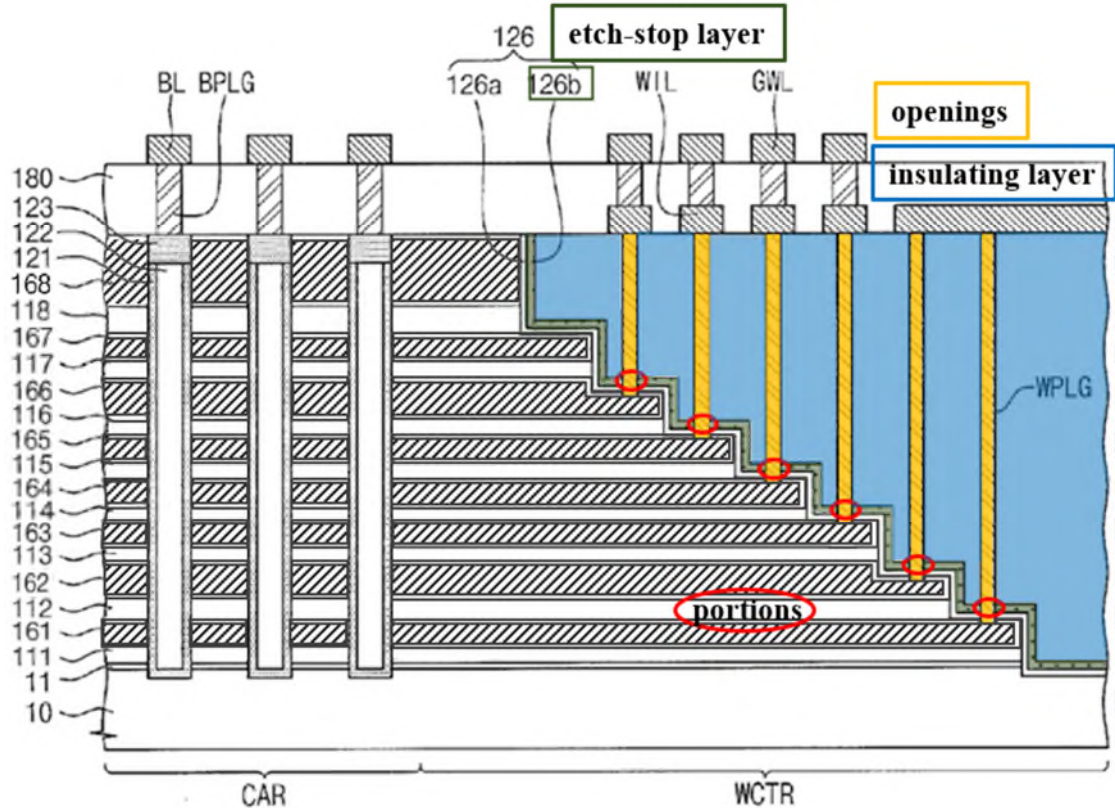
6. [1.E] “forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer;”

Preliminarily, Kim’s disclosures of the second stop layer 125b apply to the layer labeled 126b for purposes of these claims. The “stepwise etch stop pattern 126[b]” simply results from removing the portion of the second stop layer 125b at the top surface of Kim’s staircase. Kim, [0201]; *compare id.*, Fig. 19A (125a-125b) *with id.*, Fig. 20A (126a-126b).

Similarly, Kim’s descriptions of the interlayer dielectric 130 apply to the interlayer insulating pattern 134. The interlayer insulating pattern 134 results from the interlayer dielectric 130 after a planarization process. Kim, [0193]; *compare id.*, Fig. 18A (pre-planarization interlayer dielectric 130) *with id.*, Fig. 19A (post-planarization pattern 134). Banerjee ¶¶ 100-01.

Kim discloses *forming a plurality of openings* (“contact holes”) *in the insulating layer* (“interlayer insulating pattern” 134) *exposing portions of the etch-stop layer* (“etch stop pattern” 126b):

Gate-Stack-on-Top Fig. 22A



Kim, Fig. 22A, [0173]-[0174] (“the formation of word line contact plugs WPLG[s] ... include[s] forming contact holes to penetrate the interlayer insulating pattern....”). These contact holes get extended to the gate electrodes 161-166 (colored orange above to illustrate the openings) and subsequently filled with a conductive material to become word-line contact plugs WPLGs. *Id.*, [0173]; Banerjee ¶ 102.

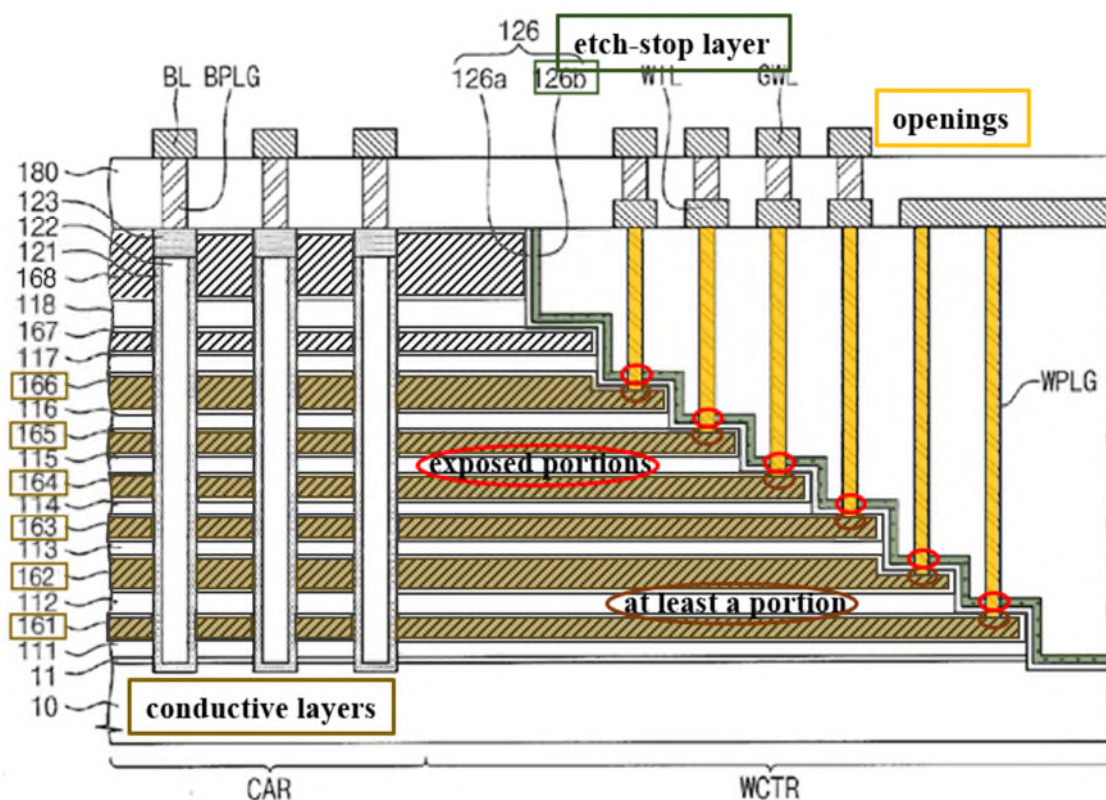
Kim’s opening formation comprises a step where etching penetrates *the insulating layer exposing*—but not penetrating—*portions of the etch-stop layer*. A POSITA would have recognized this step from Kim’s disclosure that “[t]he etch stop

layer 125[/126] may be formed of a material having an etch selectivity with respect to the interlayer dielectric 130.” *Id.*, [0213]. The relative etch selectivity allows the interlayer dielectric to be etched away without penetrating the etch-stop layer. Thus, the etch-stop layer protects the layers beneath and prevents over-etching, especially of shallow openings. Accordingly, after the openings reach the etch-stop layer, most of the etch-stop layer would remain, exposing portions of it at the bottom of the openings. Banerjee ¶ 103.

7. [1.F] “etching the exposed portions of the etch-stop layer in the plurality of openings and exposing at least a portion of the conductive layer of each step; and”

Kim discloses *etching the exposed portions of the etch-stop layer* (“etch stop pattern” 126b) *in the plurality of openings* (“contact holes”) *and exposing at least a portion of the conductive layer of each step* (“gate electrodes” 161-166):

Gate-Stack-on-Top Fig. 22A



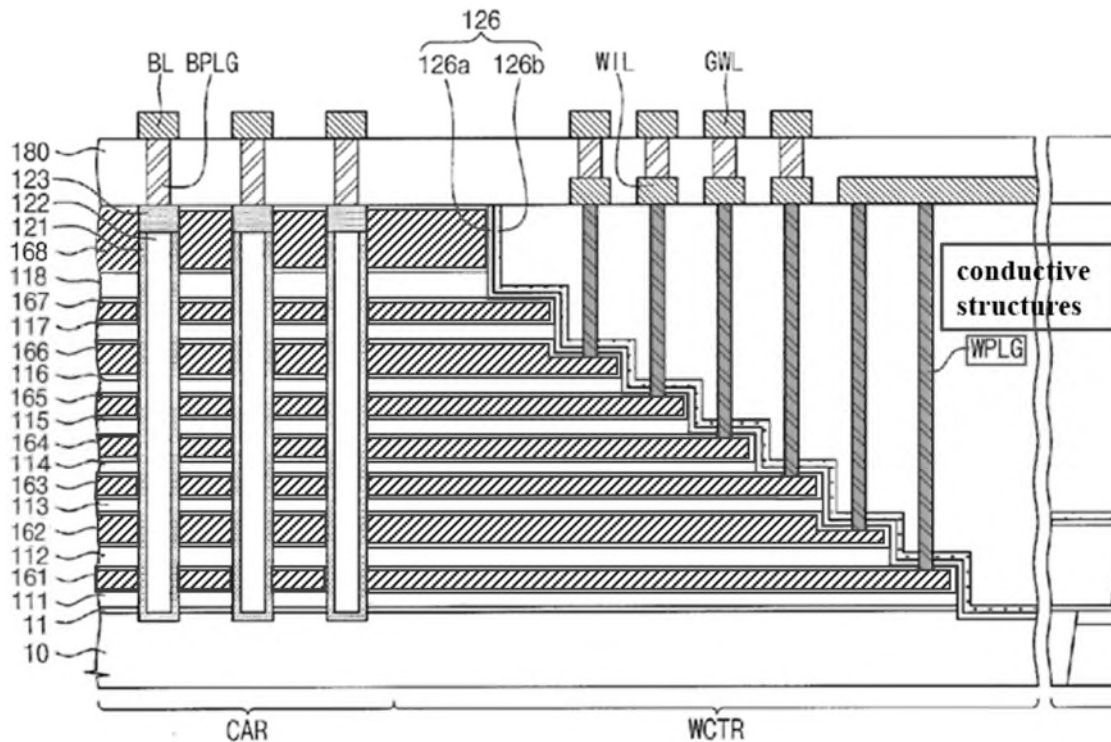
Kim, Fig. 22A. After step [1.E], etching must continue by penetrating the etch-stop layer because the contact holes and the conductive structures to be formed therein must reach the gate electrodes by penetrating the layers above them. *Id.*, [0211] (disclosing contacts between gate electrodes and word-line contact plugs WPLGs formed in the contact holes). Therefore, *the exposed portions of the etch-stop layer in the plurality of openings* must be etched away and *at least a portion of the conductive layer of each step* must be *expos[ed]*. Such penetration can be effectuated through one or more etching steps involving different relative etch selectivities after step [1.E]. Banerjee ¶ 104.

The reverse layer ordering at each step does not change this analysis because the function of the WPLGs (formed in the openings) is to electrically connect the gate electrodes with global word lines GWL. Kim, [0175], [0210], [0251]-[0252]; Banerjee ¶ 105.

8. [1.G] “forming a plurality of conductive structures in each of the plurality of openings.”

Kim discloses *forming a plurality of conductive structures* (“WPLG[s]”) *in each of the plurality of openings* (“contact holes”):

Gate-Stack-on-Top Fig. 22A



Kim, Fig. 22A, [0173] (“the formation of word line contact plugs WPLG ... may include ... filling the contact holes with a conductive material.”); *id.*, [0210]-[0211], [0251]-[0252]; Banerjee ¶ 106.

C. Claim 2:

1. [2] **“The method of claim 1, wherein the forming the plurality of openings comprises performing an etching process on the insulating layer, wherein an etching rate of the insulating layer is higher than an etching rate of the etch-stop layer.”**

Kim discloses the additional limitation of claim 2. Specifically, “[t]he etch stop layer 125[/126] may be formed of a material having an etch selectivity with respect to the interlayer dielectric 130[/134].” Kim, [0213]. The references to etch selectivity mean *the forming the plurality of openings* (“contact holes”) *comprises performing an etching process on the insulating layer* (“interlayer insulating pattern” 134). Further, the relative etch selectivity of the etch-stop layer and interlayer dielectric means that *an etching rate of the insulating layer* (“interlayer insulating pattern” 134) *is higher than an etching rate of the etch-stop layer* (“etch stop pattern” 126b) so that the etch-stop layer 126b would protect its underlying layers and prevent over-etching, especially of shallower openings. §V; Banerjee ¶ 107.

D. Claim 4:

1. [4] **“The method of claim 1, wherein etching the exposed portions of the etch-stop layer comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer of each step.”**

Claim 4 is obvious in view of a POSITA’s knowledge. In limitation [1.F], portions of the etch-stop layer in the openings are etched to expose a portion of the conductive layer of each step. §X.B.7. One common approach to this is to extend

the etching time to penetrate both the etch-stop layer and the first high-k dielectric layer until the openings reach the conductive layers. See Fang, [0029] (disclosing the same regarding etching the etch-stop layer). But since punch-through of gate electrodes must be prevented, it would have been prudent and obvious to slow down etching once it reaches the conductive layer. This means that *the etch-stop layer [has] a higher etching rate than an etching rate of the conductive layer of each step*. Moreover, because the first high-k dielectric layer is typically very thin, even when that layer is configured to slow down etching to protect the underlying conductive layer, it would have still been desirable to have a conductive layer with low etching rate relative to that of the etch-stop layer for additional protection. Finally, there are only three possible relationships of one etching rate relative to another: higher, equal, or lower. It would have made no sense for the conductive layer to have a higher etching rate than that of the etch-stop layer since the conductive layer must be preserved. Since the two layers have different materials, they do not have equal etching rates. Thus, the only remaining possibility is the claimed relationship. As an example, a silicon-nitride etch-stop layer has a higher etching rate than metal conductive layers relative to SF_6 and C_4F_8 . Banerjee ¶ 108 (citing Ex. 1023).

The conductive layer needs to be preserved for word-line contacts regardless of the layer ordering at each step. The reverse order of the layers at each step renders

this limitation obvious because the gate stack resides immediately below the etch-stop layer. Banerjee ¶ 109.

E. Claim 5:

1. [5] **“The method of claim 4, wherein etching the exposed portions of the etch-stop layer further comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the first high-k dielectric layer.”**

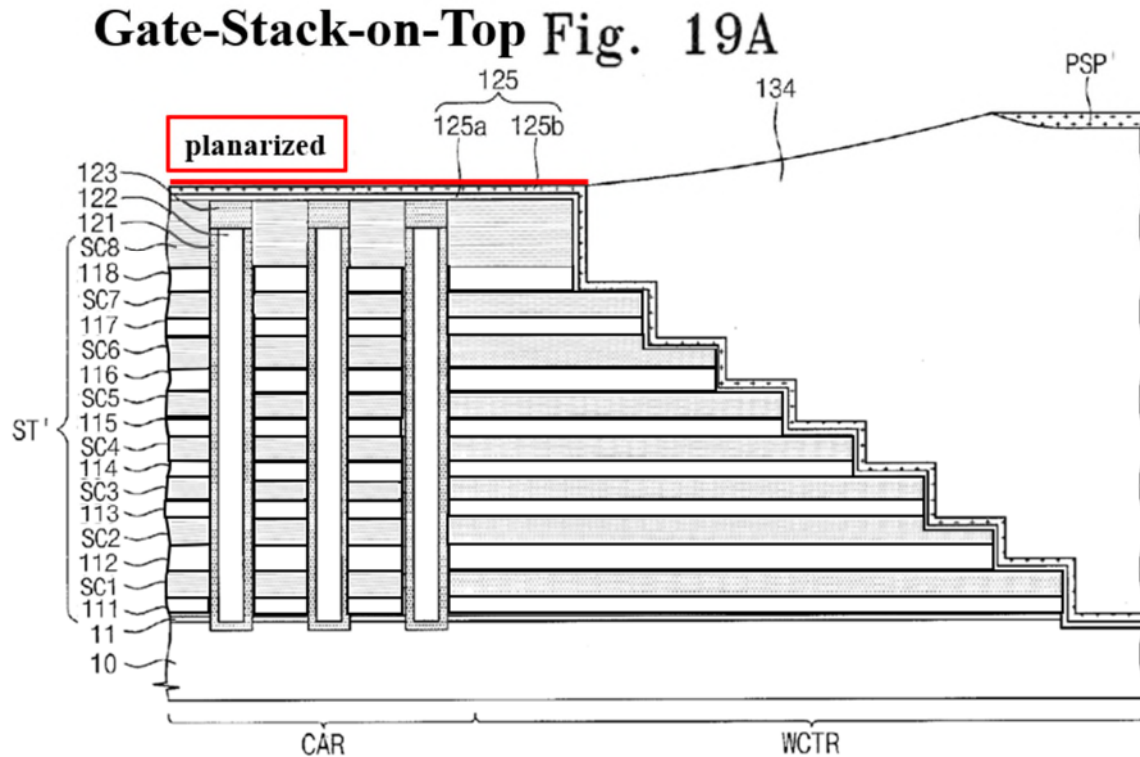
Claim 5 is obvious in view of a POSITA’s knowledge. Since punch-through of gate-electrode layers must be prevented, it would have been desirable to further protect the gate electrode layer in addition to relying on the layers’ low etching rate. Accordingly, the first high-k dielectric layer may be advantageously used as an etch stop to protect the conductive layer below. That means that *the etch-stop layer [has] a higher etching rate than an etching rate of the first high-k dielectric layer.* §V. Further, only the claimed relative etching rates have a sensible relationship. The two layers do not have the same etching rate since they comprise different materials. And it would not have made sense for the etch-stop layer to have a lower etching rate because the etch-stop layer is thicker and because it is desirable for the first high-k dielectric layer to serve as an etch stop to protect the gate conductive layer when the etch-stop layer is etched. As an example, selective etching of silicon nitride relative to aluminum oxide was well known. Banerjee ¶ 110 (citing Ex. 1024).

The reverse order of the layers at each step renders obvious the additional limitation of claim 5, especially considering Kim's disclosure of the etch selectivity between the etch-stop layer and the dielectric layers for its default dielectric-layer-on-top configuration. Banerjee ¶ 111.

F. Claim 9:

1. [9] **“The method of claim 1, further comprising: after disposing the insulating layer on the etch-stop layer, planarizing the insulating layer and the staircase structure by using chemical-mechanical-polishing (CMP).”**

Kim discloses the additional limitation of claim 9. Specifically, Figures 19A-19B show the word line contact structure *after disposing the insulating layer on the etch-stop layer* (after the step of limitation [1.C], §X.B.4), and “[r]eferring to FIGS. 19A and 19B, a planarization process on the interlayer dielectric 130 [*the insulating layer*] may be performed using a *chemical mechanical polishing (CMP)* technique.” Kim, [0191], [0104], [0118]. *[T]he staircase structure* is *planariz[ed]* as well:



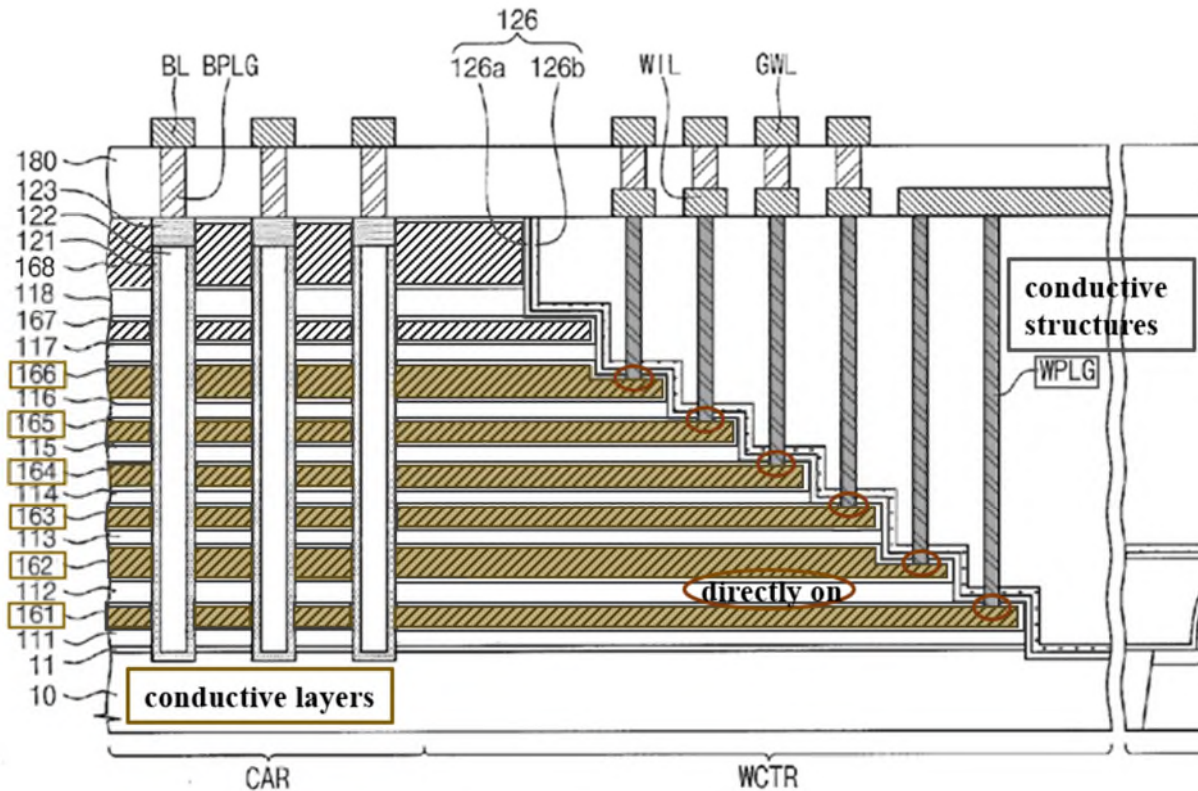
Kim, Fig. 19A; see also §X.H.1 (showing coplanar top surfaces of the etch-stop layer and the insulating layer); Banerjee ¶ 112.

G. Claim 10:

1. [10] “The method of claim 1, wherein forming the plurality of conductive structures comprises disposing conductive materials inside the plurality of openings, the conductive materials directly on the exposed conductive layer of the each step.”

Kim discloses *forming the plurality of conductive structures* (“WPLG[s]”) *comprises disposing conductive materials inside the plurality of openings* (“contact holes”), *the conductive materials directly on the exposed conductive layer* (“gate electrodes” 161-166) *of the each step*:

Gate-Stack-on-Top Fig. 22A



Kim, Fig. 22A, [0173] (“filling the contact holes with a conductive material.”); [0210]-[0211] (“WPLG may be formed to connect the global word lines GWL and the gate electrodes 161 to 168.”).

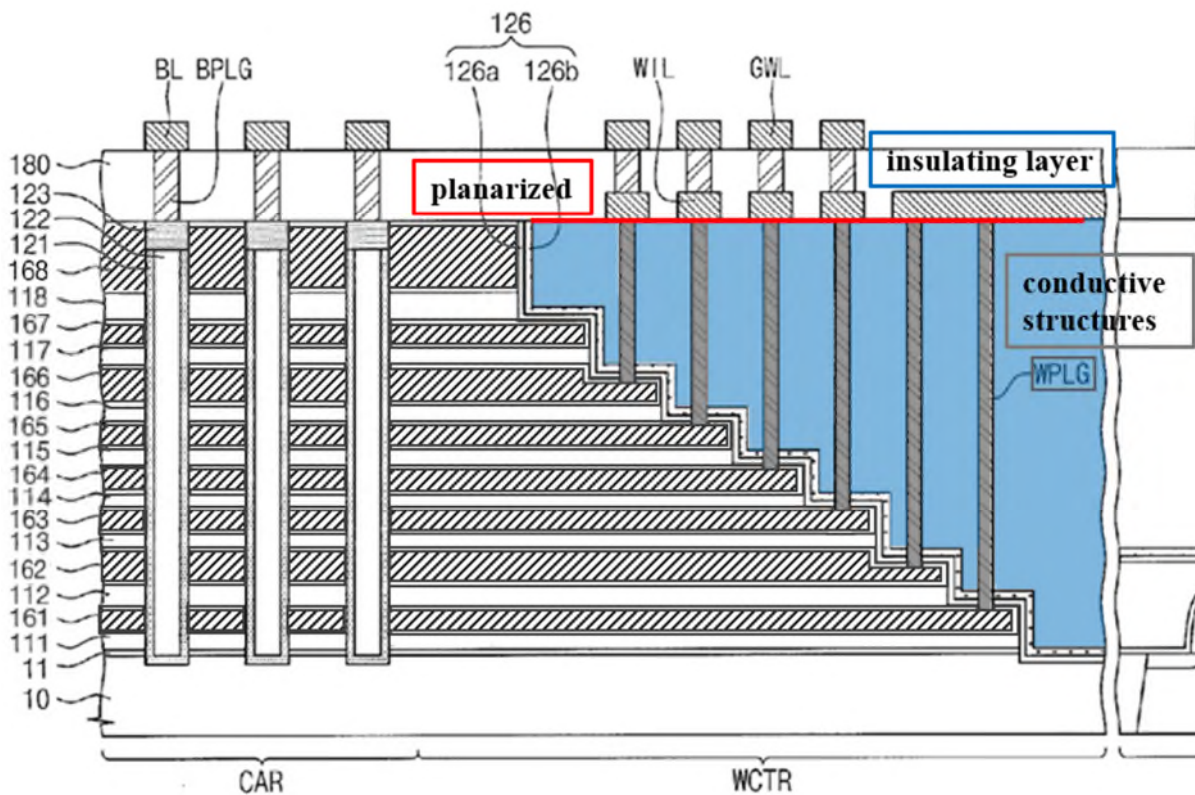
The layer ordering at each step does not impact this explanation because direct contacts between WPLGs and the gate electrodes are needed for the word lines to function. Banerjee ¶¶ 113-14.

H. Claim 11:

1. [11] “The method of claim 1, wherein forming the plurality of conductive structures further comprises planarizing the conductive materials and the insulating layer.”

Kim at least renders obvious *forming the plurality of conductive structures* (“WPLG[s]”) *further comprises planarizing the conductive materials* (of “WPLG[s]”) *and the insulating layer* (“interlayer insulating pattern” 134):

Gate-Stack-on-Top Fig. 22A



Kim, Fig. 22A.

A POSITA would have understood that a planar top surface is advantageous and required for forming the word line connecting lines (WIL in Figure 22A) on the surface. Kim, [0209], Banerjee ¶¶ 115-16 (citing Ex. 1021). This is consistent with

Kim's planarizing the top surfaces of other components. Kim, [0119], [0206]. Thus, a POSITA would have understood, or at least found obvious, this limitation.

I. Claim 12:

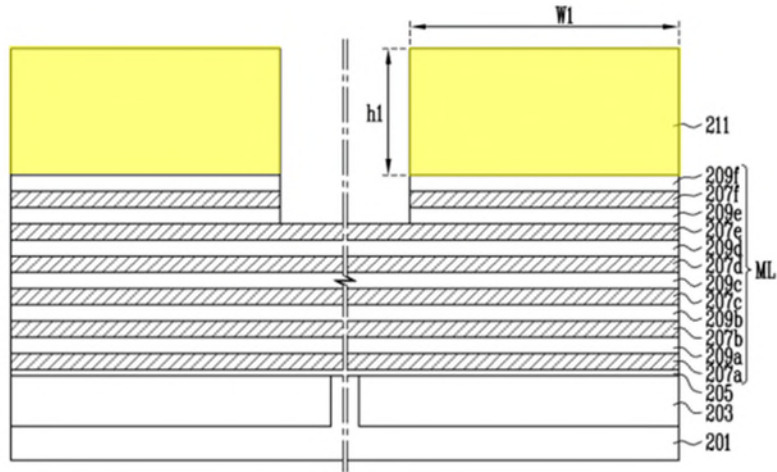
1. [12] **"The method of claim 1, wherein forming the staircase structure further comprises performing a repetitive etch-trim process on the sacrificial layers and the dielectric layers."**

Kim discloses *forming the staircase structure* ("stepwise stacked layer structure ST") *further comprises performing a repetitive etch-trim process on the sacrificial layers* ("sacrificial layers" SC1-SC6) *and the dielectric layers* ("insulating layers" 111-116).

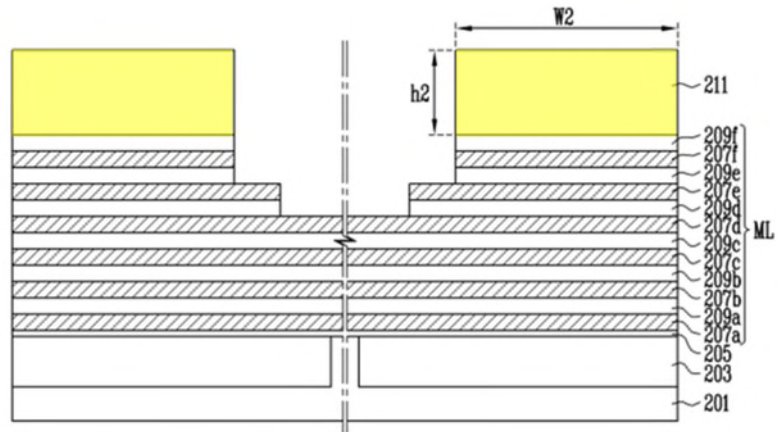
Specifically, "the patterning of the stepwise stacked layer structure ST' may include steps of reducing a horizontal area occupied by a mask pattern MP and etching the stacked layer structure ST, which are alternately performed." Kim, [0087], [0182]. That reduction is a trimming process. Ex. 1001, 7:19-28. Thus, the two alternately performed steps constitutes a *repetitive etch-trim process*. Kim, [0182]; Banerjee ¶¶ 117-20.

The unmasked portion is etched, the mask is trimmed, and the process is repeated. This is illustrated in the following sequence of figures:

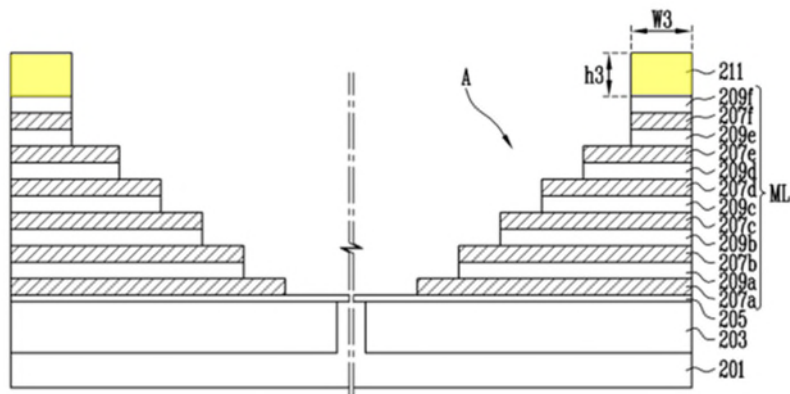
도면3a



도면3b



도면3c



Ex. 1020, Figs. 3a-3c. The layer ordering at each step does not affect this analysis.

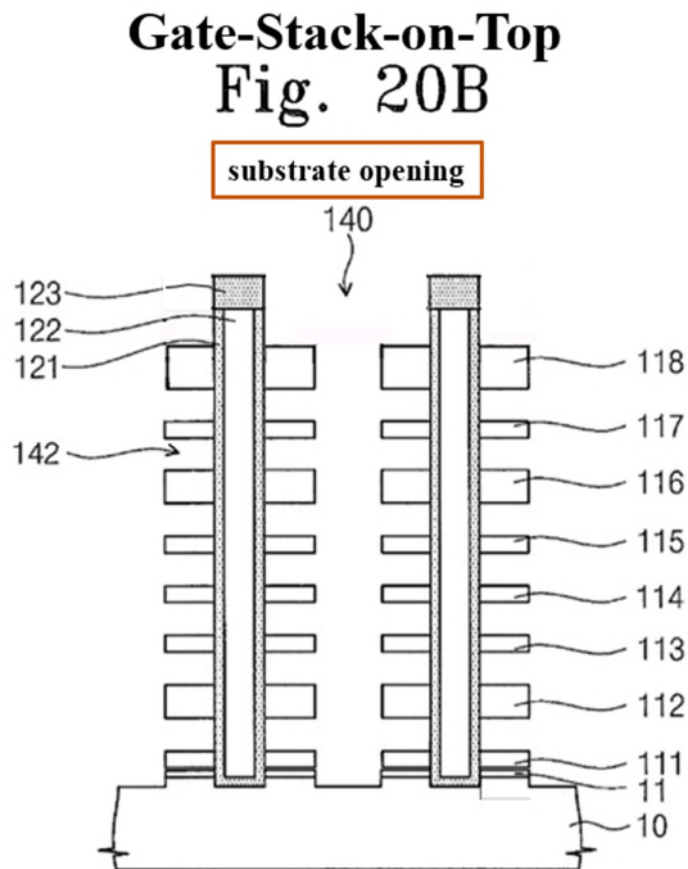
J. Claim 13:

1. [13.PRE] “The method of claim 1, wherein replacing the sacrificial layer of each step with the gate stack comprises:”

This preamble simply repeats limitation [1.D]. §X.B.5.

2. [13.A] “forming a substrate opening through the staircase structure;”

Kim discloses *forming a substrate opening* (“trench” 140) *through the staircase structure*:



Kim, Fig. 20B, [0198]-[0199] (“The formation of the gate electrodes ... may include forming the trenches 140 ... and replacing the sacrificial layers....”). Trench 140 constitutes a substrate opening because its opening extends to the substrate surface.

Id., [0199]. That matches the '276 patent's substrate opening, which also penetrates the stack and exposes the substrate surface. Ex. 1001, 8:45-53. Additionally, trench 140 must extend into the substrate, because the structure to be formed in the trench provides a connection to a doped region of the substrate that serves as the common source line. Kim, [0203]-[0204]; Banerjee ¶ 122.

3. [13.B] “removing the sacrificial layer of each step through the substrate; and”

Preliminarily, *the substrate* appears to be an error. For the purpose of this Proceeding only, it is treated as *the substrate opening*. §X.J.2; Ex. 1001, 8:45-53, 12:29-36.

Kim discloses *removing the sacrificial layer* (one of “sacrificial layers” SC1-SC6) *of each step through the substrate [opening]* (“trench” 140), specifically, “selectively removing the sacrificial layers ... exposed by the trenches 140 to form recess regions 142 between the patterned insulating layers....” Kim, [0140], Figs. 20A-20B; *id.*, [0142], [0200]. The layer ordering at each step does not impact this explanation. Banerjee ¶¶ 123-24.

4. [13.C] “disposing the first high-k dielectric layer and the conductive layer in place of the sacrificial layer.”

Kim discloses *disposing the first high-k dielectric layer* (“blocking insulating layer” 150c of “data storing layer” 150) *and the conductive layer* (one of “gate electrodes” 161-166) *in place of the sacrificial layer* (corresponding one of

“sacrificial layers” SC1-SC6). This is performed through “forming a data storing layer 150 and gate electrodes 161 to 168 in the recess regions 142.” Kim, [0200]; §X.B.5 (showing sequence of replacing the sacrificial layers with the gate stacks); Kim, [0202], [0144], [0148] (“the data storing layer 150 may include ... a blocking insulating layer 150c....”), [0198]. The layer ordering at each step does not affect this analysis. Banerjee ¶ 125.

K. Claim 14:

1. [14] “The method of claim 13, wherein disposing the first high-k dielectric layer comprises disposing hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide and/or any combination thereof.”

Kim discloses that *disposing the first high-k dielectric layer* (“blocking insulating layer” 150c) *comprises disposing hafnium oxide, zirconium oxide, aluminum oxide, [or] tantalum oxide....* Kim, [0151] (“The blocking insulating layer 150c may include ... [a] high-k dielectric, ... e.g., tantalum oxide, ... , hafnium oxide, zirconium oxide, [or] aluminum oxide....”). Banerjee ¶ 126.

L. Claim 15:

1. [15] “The method of claim 13, wherein disposing the conductive layer comprises disposing tungsten, cobalt, nickel, copper, aluminum, and/or any combination thereof.”

Kim discloses that *disposing the conductive layer* (one of “gate conductive layers” 161-166) *comprises disposing tungsten....* Kim, [0157] (“The gate

conductive layer may include ... tungsten....”); §X (description of Figures 5A-14B applies); Banerjee ¶ 127.

M. Claim 16:

1. [16] “The method of claim 13, wherein disposing the conductive layer comprises disposing poly-crystalline silicon, poly-crystalline germanium, or poly-crystalline germanium-silicon.”

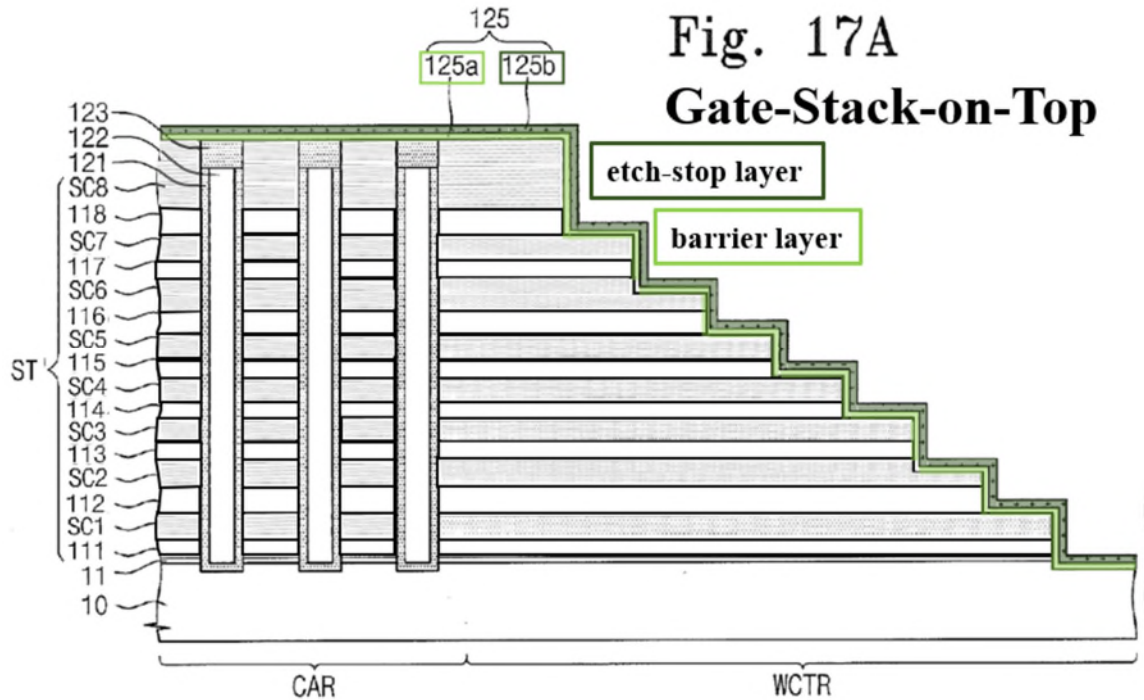
Kim discloses that *disposing the conductive layer* (“gate conductive layers” 161-166) *comprises disposing poly-crystalline silicon...* Kim, [0230] (“The gate conductive layers 101 to 108 may be a polysilicon....”); §X (shared descriptions across embodiments); Banerjee ¶ 128.

N. Claim 17:

1. [17] “The method of claim 1, further comprising: prior to disposing the etch-stop layer, disposing a barrier layer on each step of the plurality of steps, wherein the barrier layer protects underlying structures during the etching of the exposed portions of the etch-stop layer.”

Kim at least renders claim 17 obvious.

Kim discloses that *prior to disposing the etch-stop layer* (“second stop layer” 125b), *disposing a barrier layer* (“first stop layer” 125a) *on each step of the plurality of steps:*



Kim, Fig. 17A, [0185], [0187] (describing the sequence of forming conformal layers 125a and 125b).

Kim renders obvious that *the barrier layer* (“first stop layer” 125a) *protects underlying structures*. §VI (explaining that a barrier layer of the ’276 patent is simply another etch-stop layer). Kim discloses etching selectivity of its etch-stop layer 125 and etching selectivities of the first stop layer 125a and 125b. Kim, [0186]-[0187]. Indeed, the etching profiles of the first and second stop layers 125a-125b together match that of the single etch-stop layer 125. *Id.*, [0187]. Accordingly, it would have been obvious that the first stop layer 125a would perform part of the function of the etch-stop layer 125, which includes *protect[ing] underlying structures during ... etching*.

It would have been also obvious that this protection includes that *during the etching of the exposed portions of the etch-stop layer*. In general, to prevent over-etching, a layer has an etching rate lower than the layer above it and the two layers cannot have the same material. §V. Kim discloses exactly that: “the first stop layer 125a may be formed of silicon oxide and the second stop layer 125b may be formed of silicon nitride.” Kim, [0187]. The flexibility in the choice of etchants and the availability of selective etching and reverse selective etching (§V, citing Ex. 1015) would have rendered it obvious that the first stop layer could, and would, have a lower etching rate than the second stop layer, thereby slowing down etching when the second stop layer is penetrated. This renders the limitation obvious. Banerjee ¶¶ 129-32.

O. Claim 18:

1. [18] **“The method of claim 17, wherein disposing the barrier layer comprises disposing one or more of silicon oxide, silicon oxynitride, silicon nitride, TEOS, aluminum oxide, and silicon oxide incorporated with F, C, N, or H.”**

Kim discloses that *disposing the barrier layer* (“first stop layer” 125a) *comprises disposing ... silicon oxide....* Kim, [0187] (“the first stop layer 125a may be formed of silicon oxide”); Banerjee ¶ 133.

XI. GROUND 2: KIM IN VIEW OF FANG

In addition to four claims not included in Ground 1, Ground 2 also presents an alternative combination against all Challenged Claims. Specifically, Fang

discloses a high-k dielectric etch-stop layer under the correct scope of limitation [1.B]. Explanations of remaining limitations in Ground 1 are unchanged and are not repeated. Banerjee ¶ 134.

A. Claim 1:

1. [1.B] “disposing an etch-stop layer on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer;”

Kim discloses *disposing an etch-stop layer on each step of the plurality of steps*. §X.B.3. Fang discloses that *the etch-stop layer comprises a second high-k dielectric layer* under a correct interpretation of high-k dielectric, *i.e.*, Fang’s etch-stop layer “may be a high-k dielectric material, such as hafnium oxide.” Fang, [0022]; §VII. Kim in view of Fang thus renders this limitation obvious under its correct scope.⁵ Banerjee ¶ 135.

B. Claim 3:

1. [3] “The method of claim 2, wherein the etching process comprises anisotropic dry etching.”

Kim in view of Fang renders obvious claim 3.

⁵ Ground 3 addresses the etching rates of a true high-k dielectric etch-stop layer. §§XII.B, XII.D, XII.E. Those discussions apply to Ground 2 since both use Fang’s etch-stop layer and may use the same materials for other layers.

[T]he etching process is performed on the insulating layer in forming the plurality of openings. §X.C. Fang discloses “[o]penings 145 may be formed in the another oxide material 135,” *i.e.*, the insulating layer. Fang, [0027]-[0028].

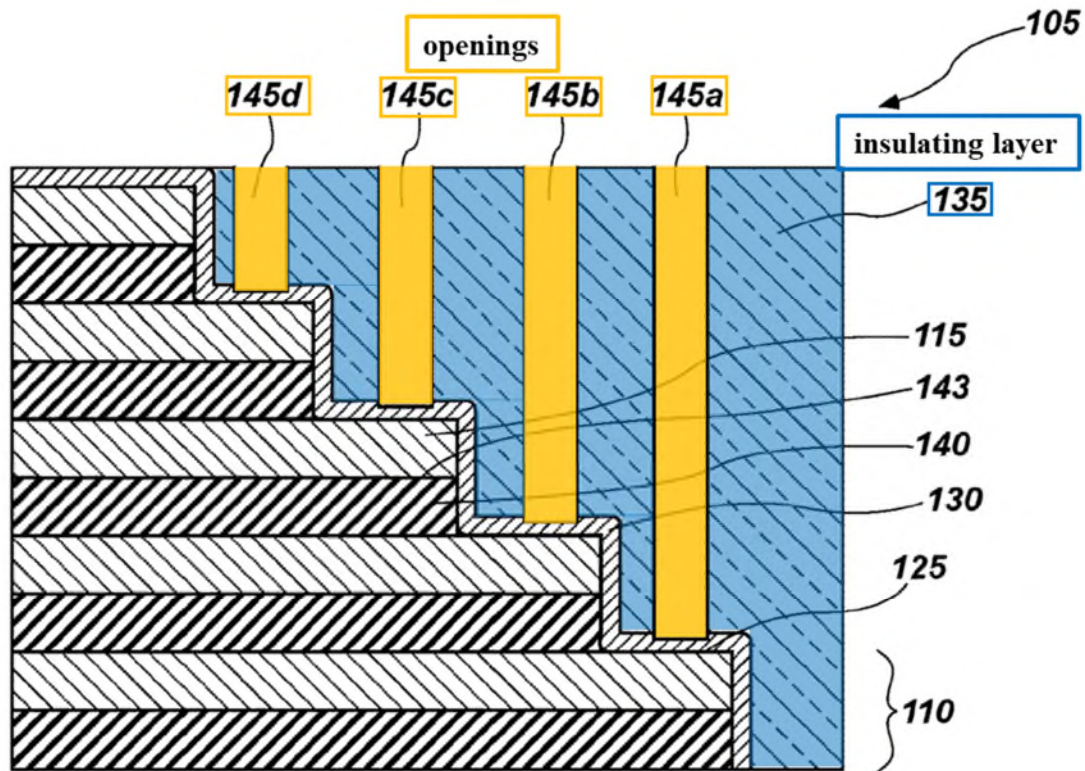


FIG. 5

Fang, Fig. 5. *Anisotropic dry etching* may be used during this *etching process*. *Id.*, [0028], [0008], [0020].

Kim also uses anisotropic etching. Kim, [0070], [0199], Figs. 6A, 12B. A POSITA would have understood these disclosures to refer to anisotropic dry etching because of the directionality required to etch deep vertical holes. Since Kim already uses this process, applying the same process to etch the insulating layer would have

been nothing more than applying what Kim already uses to form openings with a similar profile. Banerjee ¶¶ 136-38. This “‘known-technique’ rationale” renders the claimed process obvious and supplies a motivation to combine. *Intel*, 61 F.4th at 1380.

C. Claim 6:

1. [6] **“The method of claim 1, wherein disposing the etch-stop layer comprises disposing hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, and/or any combination thereof.”**

Kim in view of Fang renders obvious claim 6. Specifically, Fang discloses that *the etch-stop layer* may comprise silicon nitride or, “[a]lternatively, ... a high-k dielectric material, such as *hafnium oxide*.” Fang, [0022]. Both alternatives would function as an etch stop and meet Fang’s criterion of not removing the etch-stop material when removing the sacrificial layers. *Id.*, [0025]. Kim also discloses silicon nitride as a material for the etch-stop layer. Kim, [0186]. Thus, applying Fang’s “alternative[]” to silicon nitride (Fang, [0022]) represents nothing more than applying the same alternative toward Kim’s “similar device[] in the same way.” *Intel*, 61 F.4th at 1380; Banerjee ¶ 139.

D. Claim 7:

- 1. [7] “The method of claim 1, wherein disposing the etch-stop layer comprises disposing the etch-stop layer with a thickness in a range between 10 nm to 100 nm.”**

As an initial matter, as the Examiner noted, “the specification ... reveals no particular benefit to any particular thickness.” Ex. 1002, 92 (citing the equivalent of Ex. 1001, 7:62-8:25). And the cited range—spanning orders of magnitude—indicates that no particular thickness “is particularly critical.” *Id.*, 92-93. Where, as here, the “[d]ifferences between the prior art and the claimed invention[, if any, is merely] dimensional” not resulting in “differences in performance,” the claim is not valid. *Gardner v. TEC Sys., Inc.*, 725 F.2d 1338, 1345-46 (Fed. Cir. 1984).

If more is required (it is not), Kim in view of Fang renders claim 7 obvious. Fang discloses an analogous semiconductor structure with an etch-stop layer. Fang, Fig. 6, [0020]. To start, Kim’s and Fang’s etch-stop layers are similar. For example, both of their etch-stop layers may comprise silicon nitride. Kim, [0187]; Fang, [0022]. And Fang’s alternative (a high-k dielectric) is applicable to Kim. §XI.C.1. Fang’s etch-stop layer “may be formed by conventional techniques....” Fang, [0020]. A POSITA could, and would, apply such conventional techniques to form Kim’s etch-stop layer. Additionally, Fang’s disclosed thickness range of 5-100 nm may be adjusted to 5-26.7 nm based on Kim’s staircase structure. Both the disclosed and the adjusted thickness ranges overlap with the claimed *range between 10 nm*

and 100 nm, and making the adjustment would have been well within the knowledge and skill of a POSITA.⁶ Thus, Kim in view of Fang renders claim 7 obvious. Banerjee ¶¶ 140-41.

E. Claim 8:

1. [8] **“The method of claim 1, wherein disposing the etch-stop layer comprises performing chemical vapor deposition (CVD), physical vapor deposition (PVD), sputtering, atomic layer deposition (ALD), spin-coating, or any combination thereof.”**

Kim in view of Fang renders obvious claim 8.

Fang discloses forming the etch-stop layer using “conventional techniques including, but not limited to, *chemical vapor deposition (CVD)*, *physical vapor deposition (PVD)*, *atomic layer deposition (ALD)*, or a diffusion process.” Fang, [0020].

Kim’s method also uses at least CVD and ALD processes. Kim, [0079], [0236]. Thus, applying CVD or ALD toward *disposing the etch-stop layer* represents nothing more than applying a known technique, which itself provides a motivation. *Intel*, 61 F.4th at 1380; Banerjee ¶¶ 142-44.

⁶ Claim 7 is directed toward a structure with only an etch-stop layer and without an optional barrier layer. Ex. 1001, claims 1, 17. A single layer is what Fang discloses. Fang, Fig. 6.

F. Motivation to Combine

In addition to the reasons stated above in this Ground, a POSITA would have been motivated to combine Fang's disclosure related to the etch-stop layer and contact-hole etching on Kim's word-line structure and would have had a reasonable expectation of success in doing so. Banerjee ¶ 145.

Kim focuses on resolving the difficulty of planarizing the interlayer dielectric to reduce the height difference between the cell-array and peripheral-circuit regions. Kim, [0024]-[0025]. Accordingly, Kim does not detail certain aspects of the word-line contact region WCTR that were well-known in the art. Fang, on the other hand, focuses on preventing over-etching shallower openings for the word-line conductive structures. Fang, [0004], [0008]. A POSITA would have known that Fang's focus is an important consideration for manufacturing 3D memory devices and dovetails with Kim's focus to reduce or prevent damages to the device during manufacturing. Kim, [0027]. Further, a POSITA would have known that the thickness and material of an etch-stop layer are at least necessary (but routine) design parameters and may be important to its purpose of preventing punch-through to underlying layers. Thus, a POSITA would have been motivated to adapt Kim's etch-stop layer in view of Fang.

Along with those parameters, a POSITA also would have considered Fang's techniques for forming the etch-stop layer and etching the insulating layer for a

comprehensive treatment of the related subject matter. Additionally, Fang simply applies techniques that Kim already uses. §§XI.B.1, XI.E.1. Thus, a POSITA would have found adopting Fang's techniques to be cost effective because it merely expands the use of Kim's existing techniques to another layer. Banerjee ¶¶ 146-47.

Adopting Fang's etching and deposition techniques and alternative material for the etch-stop layer represents applying what is already known to work in a similar device. Thus, a POSITA would have had a reasonable expectation of success in doing so. Banerjee ¶ 148.

A POSITA would also have had a reasonable expectation of success in applying Fang's etch-stop-layer thickness to Kim because Fang's range (5-100 nm, or 5-26.7 nm adjusted) was reasonable. Further, a POSITA would have had a reasonable expectation of success because of similarities between Kim's and Fang's disclosures regarding the etch-stop layer. For example, Kim discloses that its "etch stop layer 125 may ... hav[e] an etch selectivity with respect to the interlayer dielectric 130." Kim, [0213]. Fang discloses the same. Fang, [0020] ("The etch stop material 130 may also be substantially resistant to dry etch chemistries used to form openings 145 [through the insulating layer.]."). Kim discloses that its "second stop layer 125b may be formed of silicon nitride." Kim, [0187]. So does Fang. Fang, [0020].

More generally, a POSITA would have had a reasonable expectation of success because both disclosures are directed to similar 3D memory devices with word-line structures, *e.g.*, both comprising alternating conductive and dielectric layers in a staircase, an etch-stop layer and an insulating layer above, and conductive structures penetrating various layers to form contacts with the conductive layers. Banerjee ¶¶ 149-50.

A POSITA would have been motivated to use Fang’s “[a]lternative[]” material, *i.e.*, a high-k dielectric material such as hafnium oxide, for the etch-stop layer. Fang, [0022]. Chen discloses increasing the tunneling length of the etch-stop layer to reduce tunneling current, thereby “more effectively electrically isolat[ing] [the conductive layers] from one another.” Chen, [0004]. A high-k-dielectric etch-stop layer has a greater tunneling length (L2 in Figure 8B) compared to that of a silicon-nitride etch-stop layer (L1 in Figure 8A):

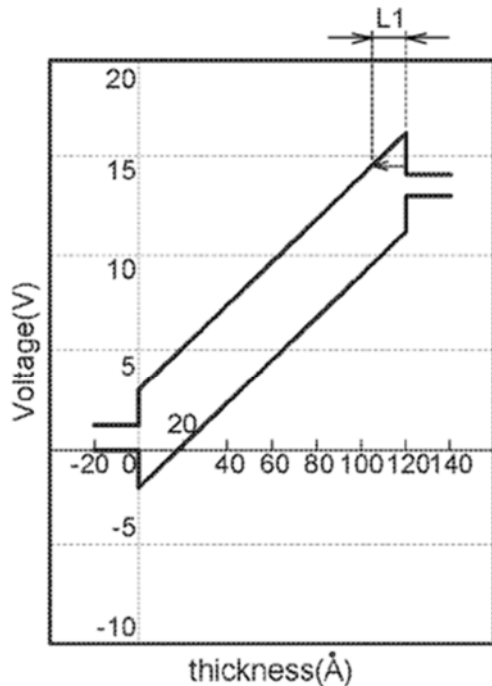


FIG. 8A

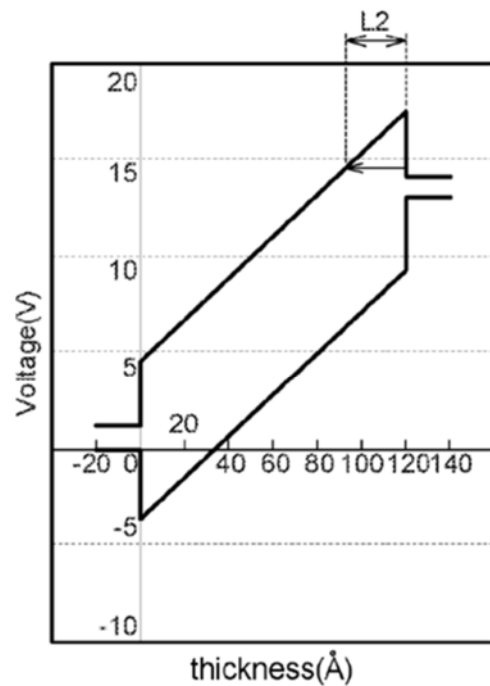


FIG. 8B

Chen, Figs. 8A-8B, [0047]-[0048]. Specifically, the energy gap is increased, improving “the stability” of the device. *Id.*, [0049], [0031].

At minimum, Fang presents a high-k dielectric as a suitable alternative for the etch-stop layer. Banerjee ¶¶ 151-52. Such an alternative presents a suitable option, which itself provides a motivation to combine. *Intel*, 61 F.4th at 1380.

Were PO to argue against the combination because Kim discloses an additional barrier layer, PO would be wrong. First, none of claims 1, 3 and 6-8 requires or prohibits a barrier layer. Second, like Fang, Kim discloses an embodiment with a single etch-stop layer 125. Kim, [0256]; §X (Kim’s descriptions apply to common aspects across embodiments). And Kim does not teach or suggest that the thickness or deposition method of the etch-stop layer would be impacted by

the number of etch-stop layers. *See generally* Kim. Thus, the presence or absence of a barrier layer does not impact either the motivation to combine or the expectation of success. Banerjee ¶ 153.

XII. GROUND 3: HAN IN VIEW OF FANG

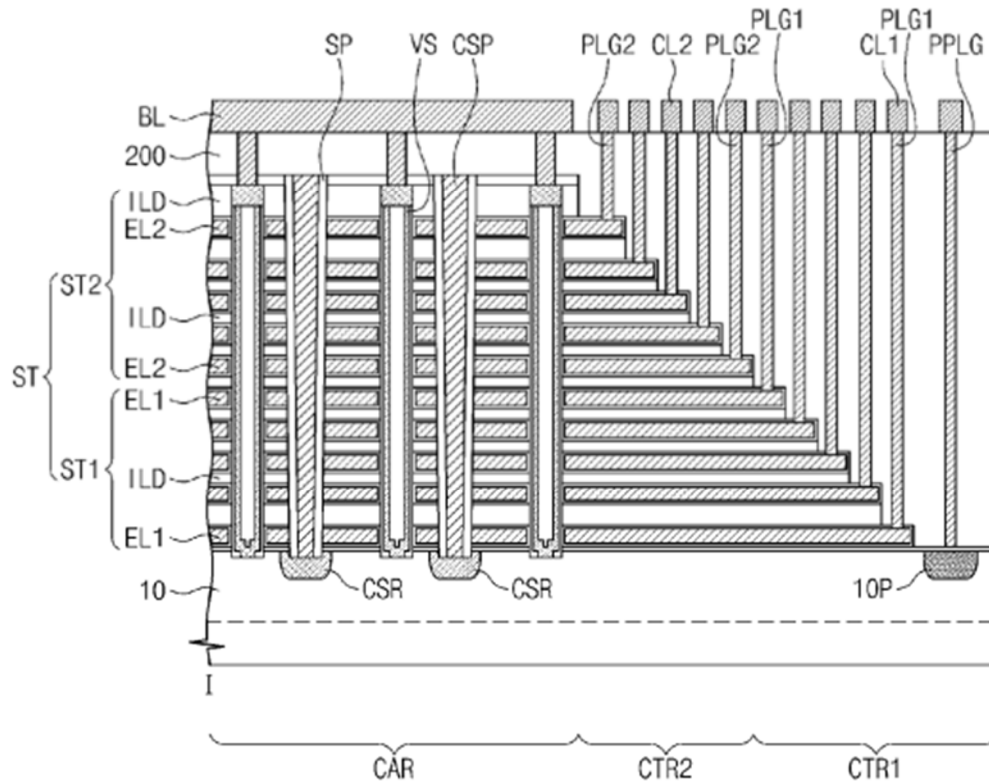
Grounds 3-4 rely on Han's method that forms the word-line contact structure shown in Figure 29. Although Han discloses several embodiments, the descriptions of these other embodiments apply to the method associated with Figure 29. Figures 27-29 together illustrate one method. Han, [0026], [0142]. Figures 30 and 31 are enlarged partial views of Figure 29. *Id.*, [0027], [0142]. In describing Figures 27-29, Han discloses that the process illustrated via Figures 15-26 to fabricate the device shown in Figure 14 may be used. *Id.*, [0143], [0150]. The Figure 29 embodiment is further linked directly and indirectly to the process illustrated in Figures 1-11. *Id.*, [0162], [0126]. Therefore, the descriptions of at least Figures 1-11 and 14-31 are all applicable to the method forming the device shown in Figure 29. Banerjee ¶ 155.

A. Claim 1:

1. [1.PRE] "A method for forming a semiconductor structure, comprising:"

Han discloses *[a] method for forming a semiconductor structure, e.g.,* methods for fabricating semiconductor devices. Han, Title. An embodiment is shown below:

FIG. 29



Han, Fig. 29; Banerjee ¶ 156.

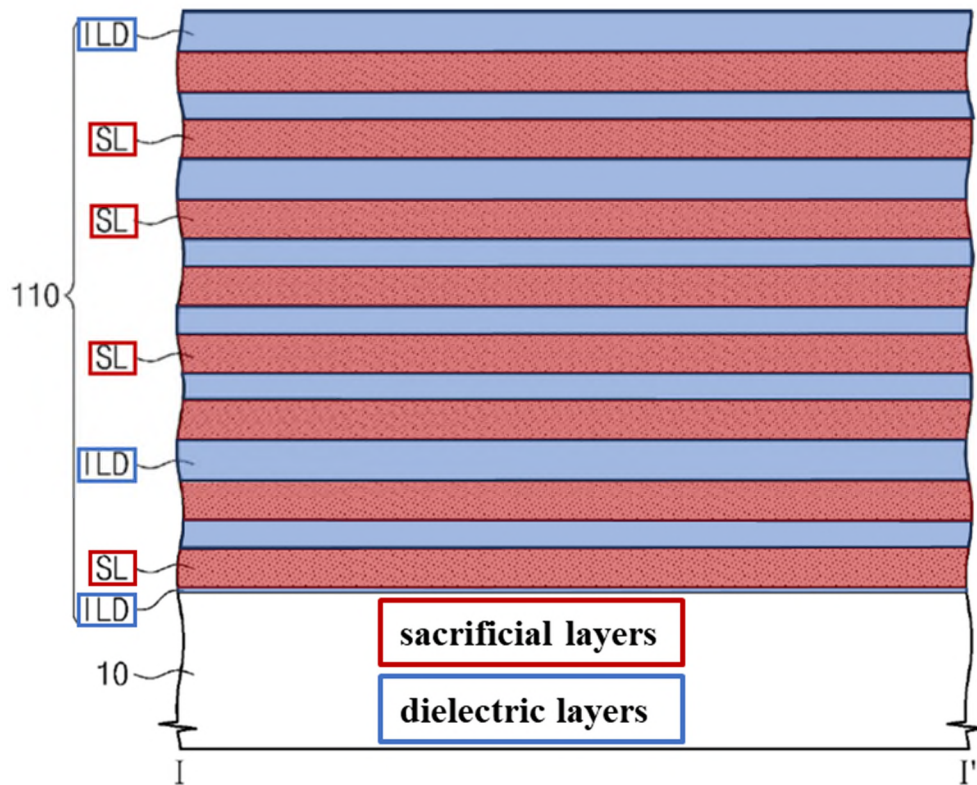
Fang also discloses the preamble. Banerjee ¶ 157.⁷

⁷ Explanations of elements not used in the combination lay a foundation for motivation to combine and are detailed in Dr. Banerjee's declaration. Banerjee ¶ 154.

2. [1.A] “forming a staircase structure having a plurality of steps, wherein the forming of each step of the plurality of steps comprises disposing a sacrificial layer over a dielectric layer;”

Han’s method comprises *forming a staircase structure* (“stepwise structure” ST) *having a plurality of steps*. It discloses forming “a stepwise structure” ST wherein “[a]reas of the ... electrodes ... may decrease as a vertical distance from the top surface of the substrate 10 increases.” Han, [0151]-[0152]. This structure ST may be formed using the method illustrated via Figure 15-26. §XII. Figure 15 shows *wherein the forming of each step of the plurality of steps comprises disposing a sacrificial layer* (one of “sacrificial layers SL”) *over a dielectric layer* (one of “insulating layers ILD”):

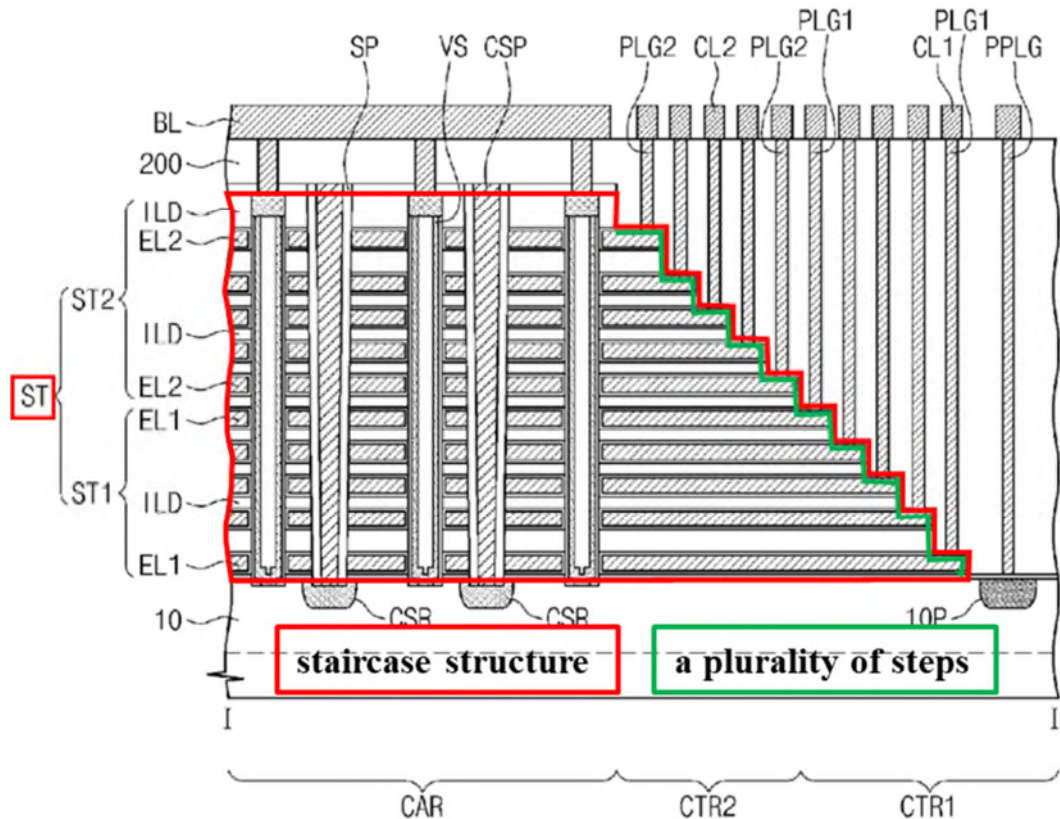
FIG. 15



Han, Fig. 15, [0096] (“sacrificial layers SL and insulating layers ILD may be alternately and repeatedly stacked on a substrate...”). As shown above, a thin insulating layer ILD resides at the bottom of the structure 110, and the lowest sacrificial layer SL is deposited on top of that bottom ILD layer. This bottom ILD layer is preserved when the sacrificial layer is removed and forms a step with the gate stack above. *Id.*, Figs. 18, 29.

In the final device, a gate stack is disposed over the corresponding dielectric layer at each step:

FIG. 29



Id., Fig. 29. Gate stacks in the fully formed device replace and positionally correspond to the sacrificial layers. *Id.*, [0115]. The gate-stack-on-top configuration results from *disposing a sacrificial layer over a dielectric layer*. Banerjee ¶¶ 158-59.

Fang's staircase structure and the layer materials are similar to Han's. Banerjee ¶¶ 160-61.

3. [1.B] “disposing an etch-stop layer on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer;”

Fang discloses *disposing an etch-stop layer* (“etch stop material 130”) *on each step of the plurality of steps* (“tiers 110”):

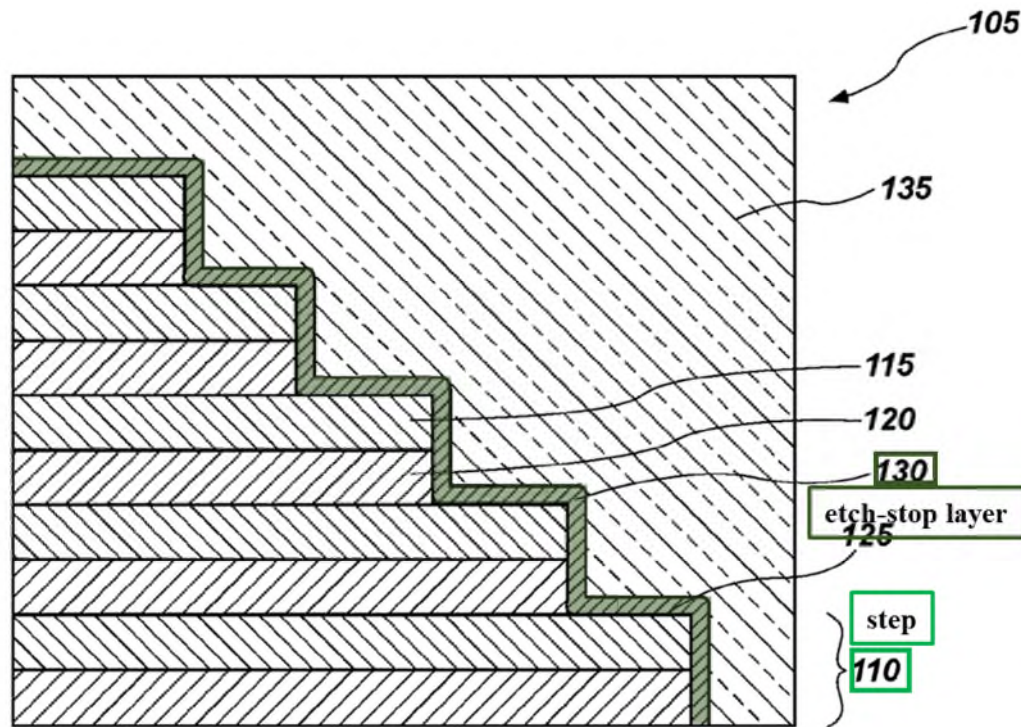


FIG. 2

Fang, Fig. 2, [0020] (depositing etch-stop material over exposed surfaces of the steps, thereby forming a layer of “a stepped profile over the stairs”).

In the combination, the etch-stop material is deposited over Han’s staircase structure, which may comprise the same materials as Fang’s staircase, *e.g.*, silicon-nitride sacrificial layers and silicon-oxide dielectric layers. Han, [0099]; Banerjee ¶¶ 162-63.

Fang further discloses that *the etch-stop layer* (“etch stop material 130”) *comprises a second high-k dielectric layer*. Specifically, the layer “may [comprise] a high-k dielectric material, such as hafnium oxide.” Fang, [0022]; §VII; Banerjee ¶ 164.

4. [1.C] “disposing an insulating layer on the etch-stop layer;”

Fang discloses *disposing an insulating layer* (“another oxide material 135”) *on the etch-stop layer* (“etch stop material 130”):

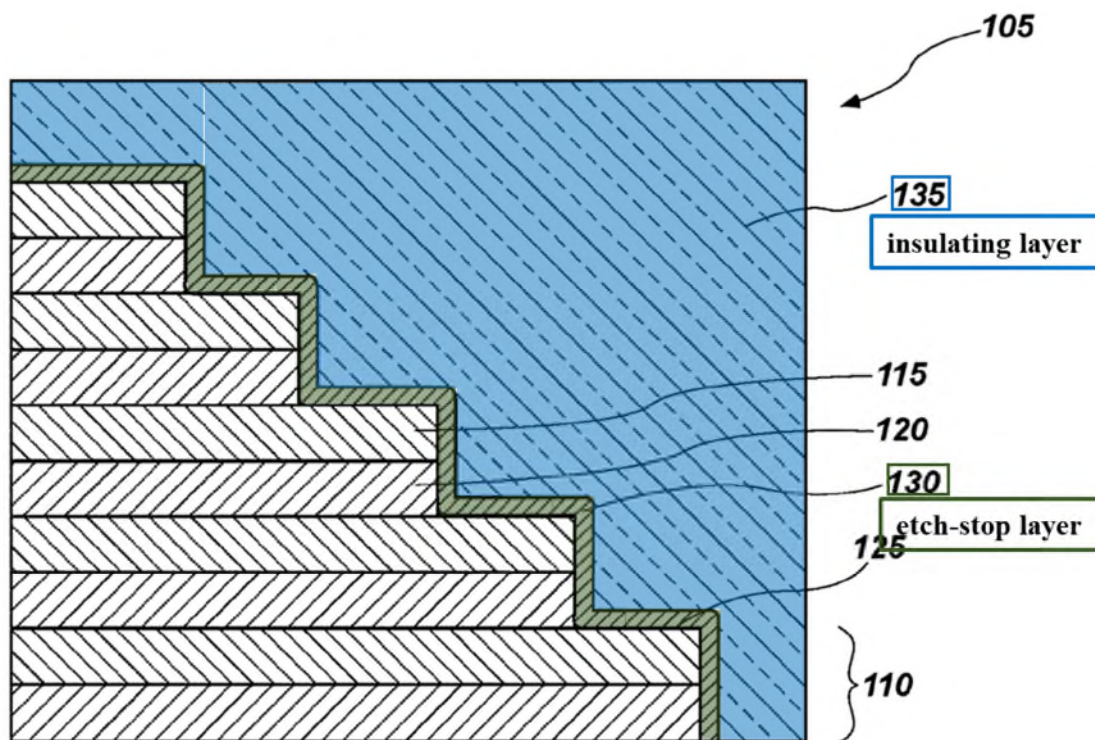
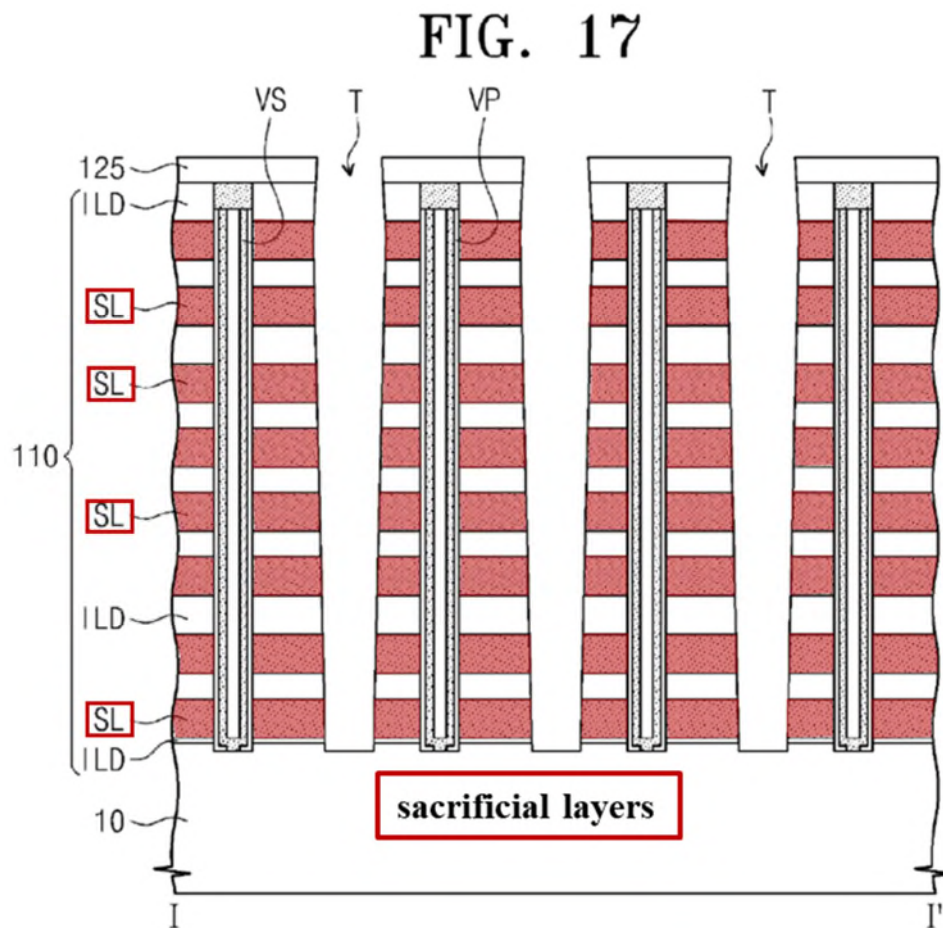


FIG. 2

Fang, Fig. 2, [0023] (“Another oxide material 135 may be formed over the etch stop material 130....”).

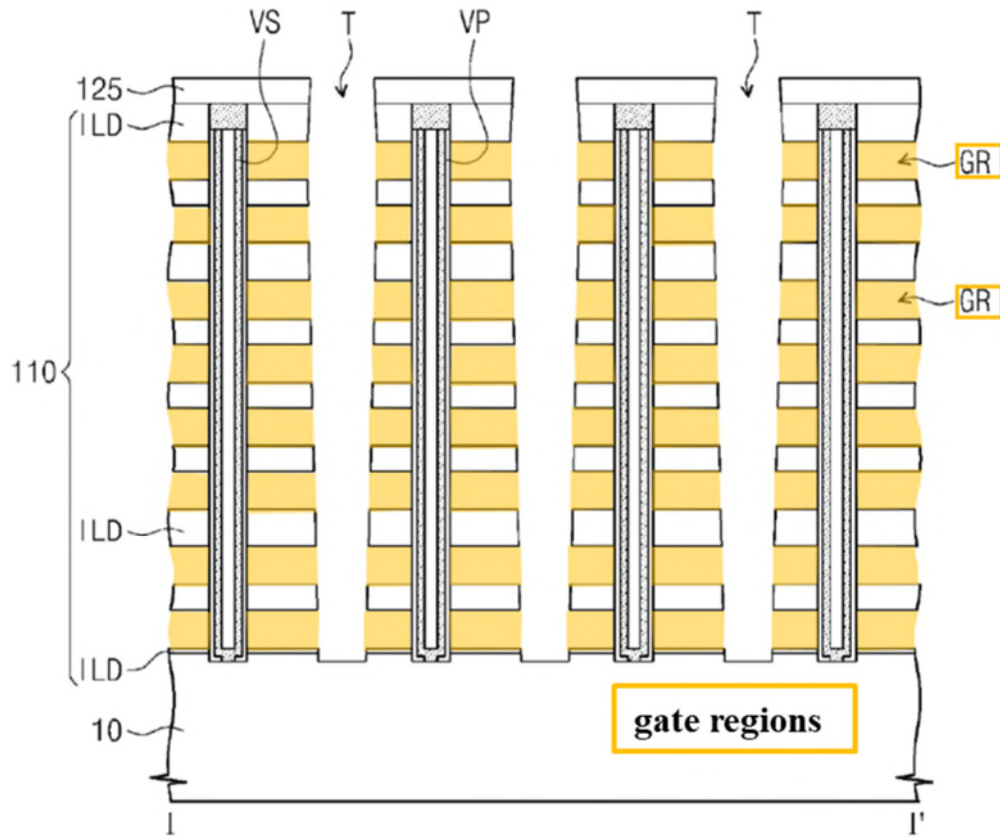
5. [1.D] “replacing the sacrificial layer of each step with a gate stack, the gate stack comprising a conductive layer and a first high-k dielectric layer;”

Han discloses *replacing the sacrificial layer (“SL”) of each step with a gate stack*. This can be seen through the Figure 17-19 progression. Figure 17 shows the sacrificial layers after trenches T have been formed:



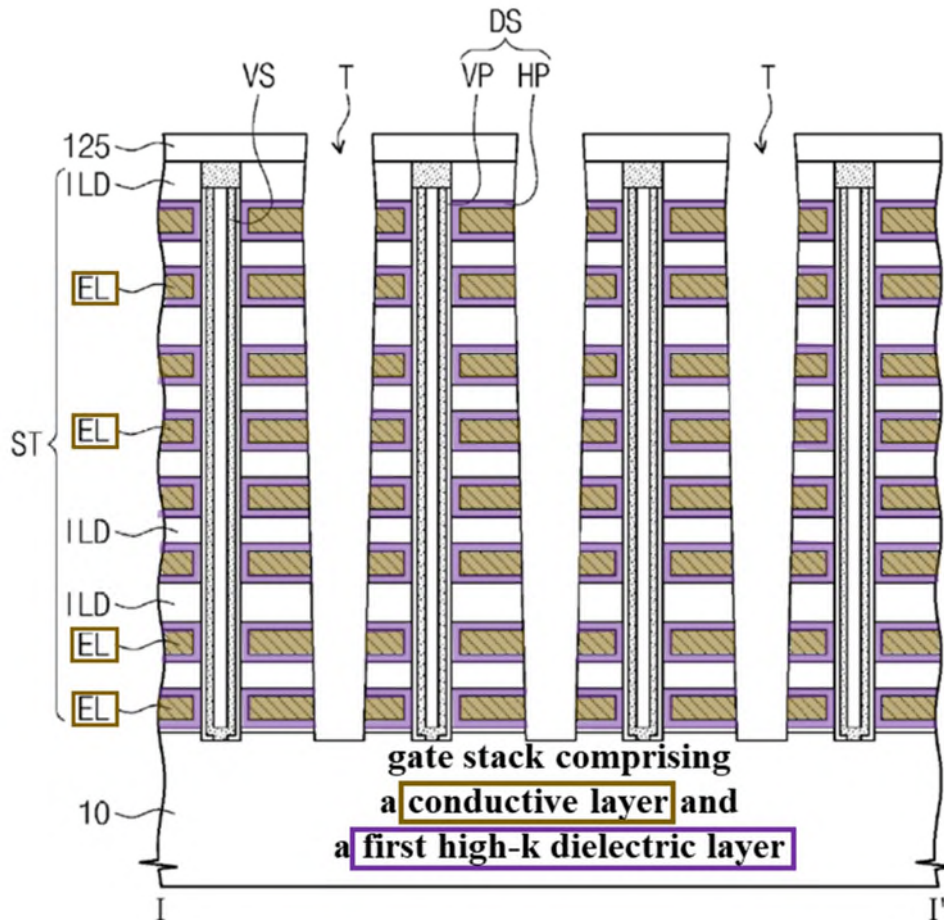
Han, Fig. 17, [0110]. Figure 18 shows “the sacrificial layers SL exposed by the trenches T [have been] removed to form gate regions GR between the insulating layers ILD.” *Id.*, [0115]:

FIG. 18



Id., Fig. 18. Figure 19 shows *gate stack[s] [each] comprising a conductive layer* (one of “electrodes EL”) *and a first high-k dielectric layer* (“horizontal insulating layer”) have been formed in the gate regions GR, thereby *replacing the sacrificial layer of each step*.

FIG. 19



Id., Fig. 19, [0118]-[0120] (“cover[ing] inner surfaces of the gate regions GR” with a conformal horizontal insulating layer and subsequently filling GR with a gate conductive layer). Banerjee ¶ 168.

[T]he gate stack compris[es] a conductive layer, i.e., a “gate conductive layer” or “electrodes EL.” *Id.*, [0119].

[T]he gate stack compris[es] ... a first high-k dielectric layer. “[T]he horizontal insulating layer may be a portion of a data storage layer of a charge trap-type flash memory transistor.” *Id.* “[T]he data storage layer ... may include a tunnel

insulating layer TIL, a charge storage layer CIL, and a blocking insulating layer BK.” *Id.*, [0134]. All three sub-layers may extend into the gate region. *Id.*, [0136]-[0138], Figs. 26B-D. The tunnel insulating layer TIL or the blocking insulating layer BK may comprise a high-k dielectric layer. *Id.*, [0140]-[0141]. Thus, *the gate stack compris[es] ... a first high-k dielectric layer*, e.g., the tunnel insulating layer TIL or the blocking insulating layer BK. Banerjee ¶¶ 169-70.

Similarly, Fang discloses *replacing the sacrificial layer of each step layer with ... a conductive layer*, rendering the combination obvious and increasing an expectation of success. *Id.* ¶¶ 171-72.

The combination comprises Han’s gate stack including the first high-k dielectric layer.

6. [1.E] “forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer;”

Fang discloses *forming a plurality of openings* (“openings 145”) *in the insulating layer* (“another oxide material 135”) *exposing portions of the etch-stop layer* (“etch stop material 130”):

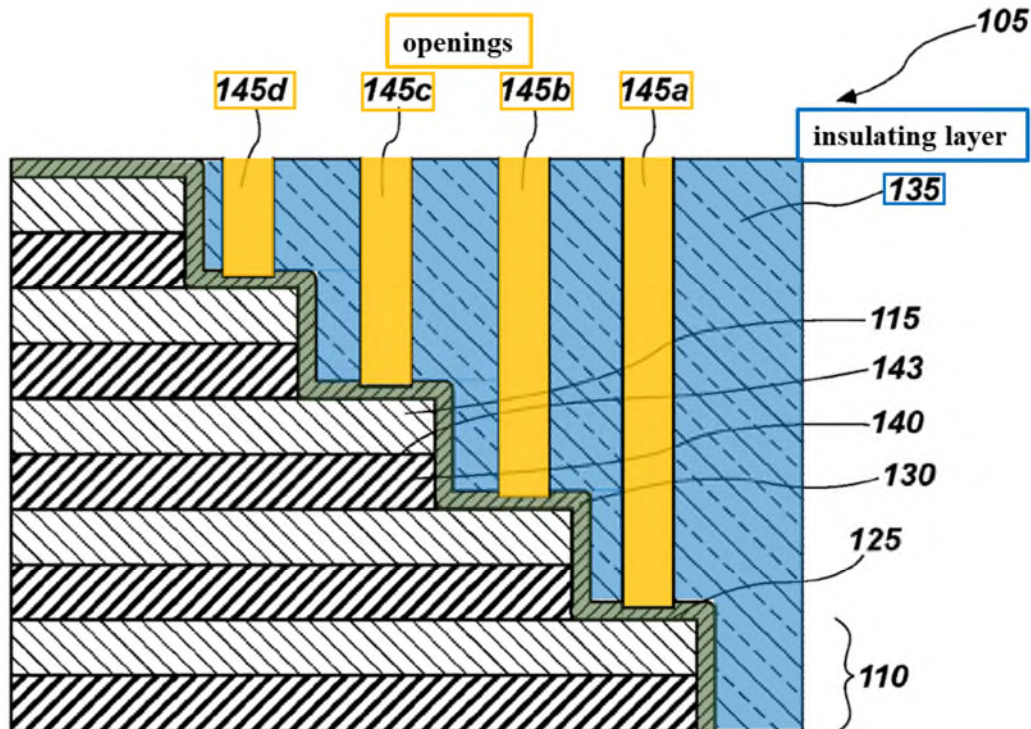
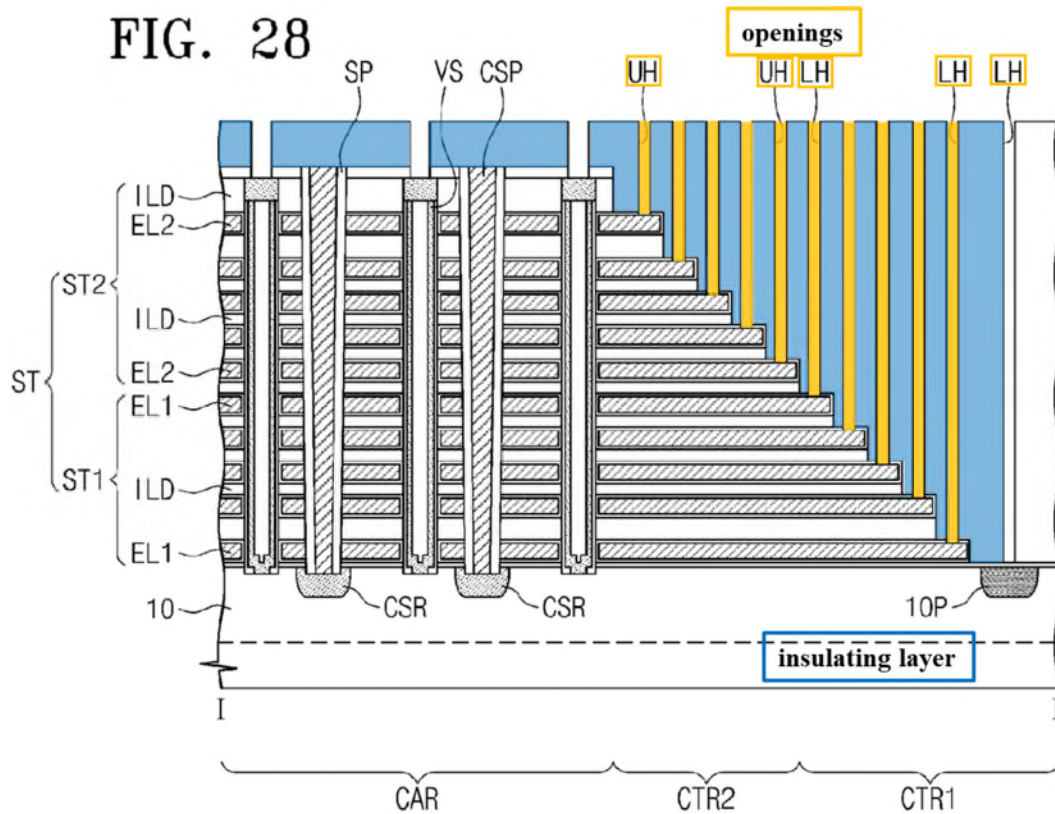


FIG. 5

Fang, Fig. 5, [0027]-[0028] (“Openings 145 may be formed in the another oxide material 135 ... [and] extend ... to an upper surface of the etch stop material 130 overlying each of the stairs 125.”); Banerjee ¶ 173.

Han also discloses *forming a plurality of openings* (“upper contact holes UH” and “lower contact holes LH”) *in the insulating layer* (“upper filling insulation layer 200”):



Id., Fig. 28, [0156] (“process may be performed on the upper filling insulation layer 200 to form lower contact holes LH ... [and] upper contact holes UH....”).

In the combination, *forming a plurality of openings* (Han’s “upper contact holes UH” and “lower contact holes LH”) *in the insulating layer* (Han’s “upper filling insulation layer 200”) would *expos[e] portions of the etch-stop layer* (Fang’s “etch stop material 130”) since Fang’s etch-stop layer covers the steps of the staircase structure. Banerjee ¶¶ 174-75.

7. [1.F] “etching the exposed portions of the etch-stop layer in the plurality of openings and exposing at least a portion of the conductive layer of each step; and”

Fang discloses *etching the exposed portions of the etch-stop layer* (“etch stop material 130”) *in the plurality of openings* (“contact holes 150”) *and exposing at least a portion of the conductive layer* (“conductive materials 140”) *of each step* (“tier 110”):

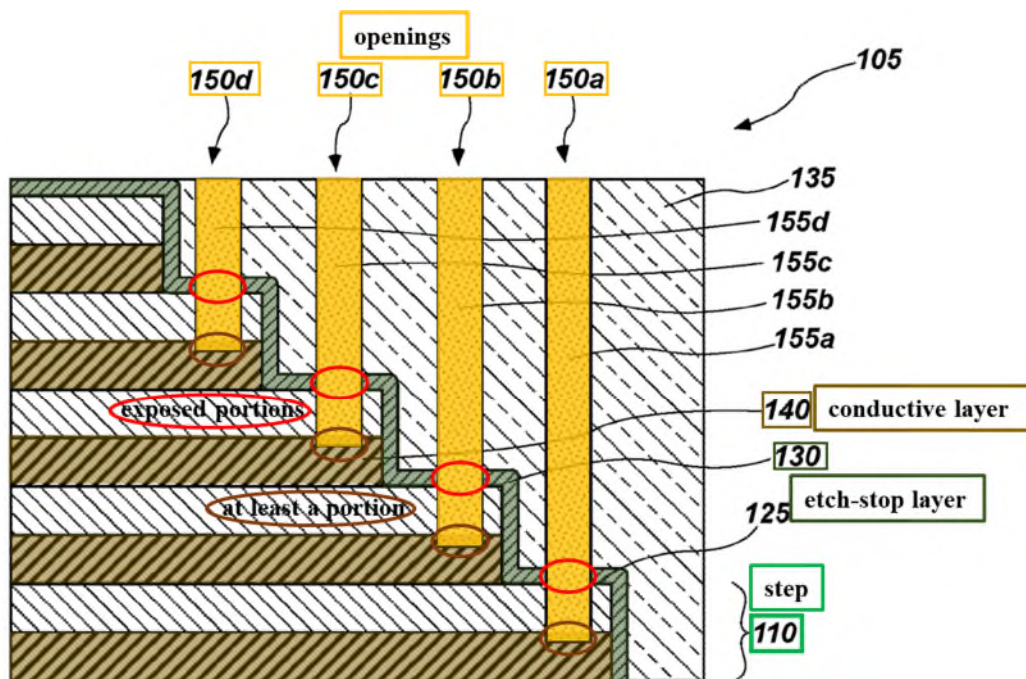


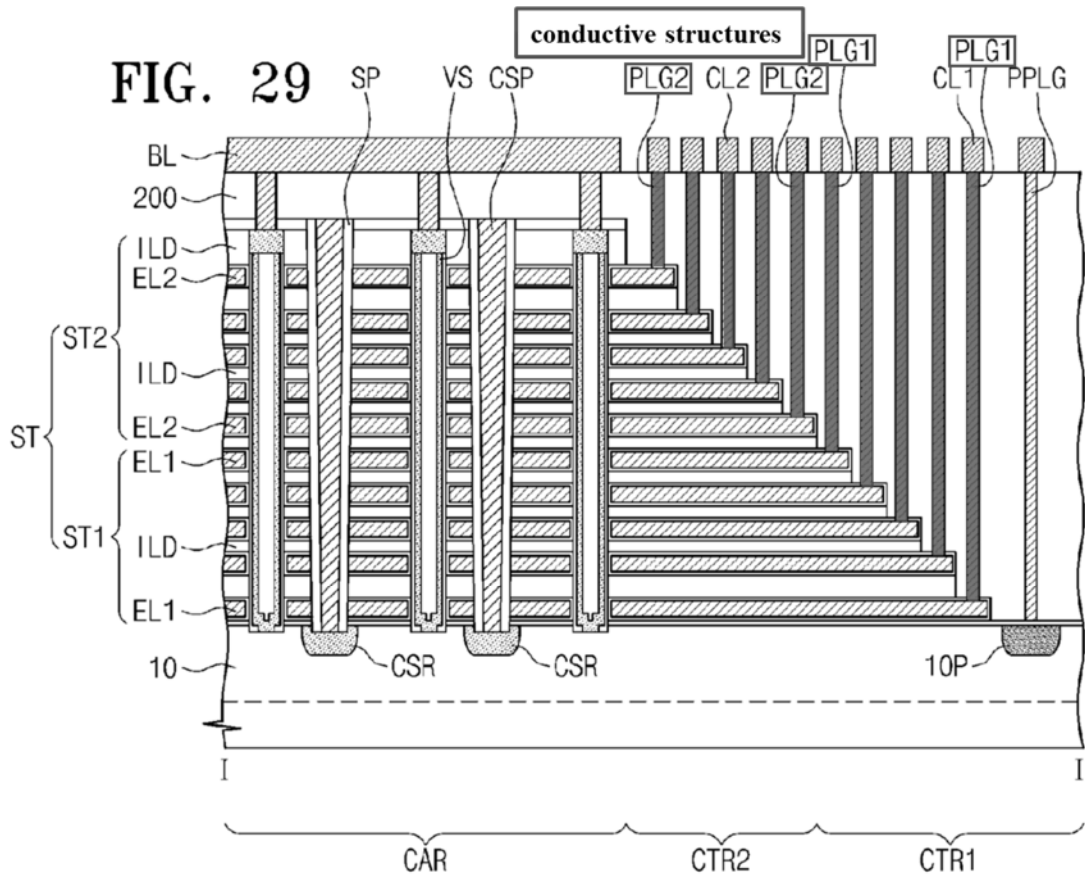
FIG. 6

Fang, Fig. 6. After the openings 145 are etched to the upper surface of the etch stop material 130, they are “extended through the oxide materials 115 and into the conductive materials 140 to form the contact holes 150.” *Id.*, [0027], [0029]. Fang’s process involves going through the oxide materials of the dielectric layers because those layers are above the conductive gate layers.

The combination comprises *etching the exposed portions of the etch-stop layer* (Fang’s “etch stop material 130”) *in the plurality of openings* (Han’s “upper contact holes UH” and “lower contact holes LH”) *and exposing at least a portion of the conductive layer of each step* (Han’s “electrodes EL”). Han and Fang both disclose *exposing at least a portion of the conductive layer of each step*, necessary for the subsequently formed conductive structures to contact the conductive gate layers. In the combination, the openings extend through the first high-k dielectric layer but not the dielectric layer. Banerjee ¶ 176-77.

8. [1.G] “forming a plurality of conductive structures in each of the plurality of openings.”

Han discloses *forming a plurality of conductive structures* (“first contact plugs PLG1” and “second contact plugs PLG2”) *in each of the plurality of openings* (“lower contact holes LH” and “upper contact holes UH”):



Han, Fig. 29, [0159], [0161] (forming PLG1 and PLG2 in LH and UH, respectively, by forming a conductive layer filling in the contact holes). Banerjee ¶ 178.

Similarly, Fang discloses this limitation. Banerjee ¶¶ 179-80.

B. Claim 2:⁸

Fang discloses the additional limitation of claim 2. *[T]he forming the plurality of openings* (“openings 145”) *comprises performing an etching process on the insulating layer* (“another oxide material 135”). Specifically, “portions of the another oxide material 135 are removed until the upper surface of the etch stop

⁸ Claim language in section headings are omitted hereafter for brevity.

material 130 is exposed at a bottom portion of the openings 145.” Fang, [0028]. This removal involves “dry etch chemistries” to which the etch-stop layer is “substantially resistant.” *Id.*, [0020]. In other words, *an etching rate of the insulating layer* (“another oxide material 135”) *is higher than an etching rate of the etch-stop layer* (“etch stop material 130”) such that the etch-stop layer slows down etching when it reaches the layer. Fang describes this as “selectively etchable” and discloses the claimed relative etching rates. *Id.*, [0018], [0023].

In the combination, Han’s upper filling insulation layer 200 comprises oxide material as disclosed in Fang. Banerjee ¶¶ 181-82.

C. Claim 3:

Fang discloses the additional limitation of claim 3.

[T]he etching process is performed on the insulating layer (e.g., Han’s upper filling insulation layer 200, or, equivalently, Fang’s another oxide material 135) when forming the openings. §XII.B. Fang discloses “[a] *dry etch[]* process (e.g., an *anisotropic* etch process) may be used to form the openings 145.” Fang, [0028]; *id.*, [0008], [0020].

Han similarly uses anisotropic etching to form openings. Han, [0041], [0105], [0111]. Banerjee ¶¶ 183-85.

D. Claim 4:

Claim 4 is obvious in view of a POSITA’s knowledge. §X.D.1.

Additionally, Fang further renders claim 4 obvious. Fang discloses that its etch-stop layer is “selectively etchable relative to specific other materials in the ... structure.” Fang, [0008]. Moreover, after etching reaches the etch-stop layer and exposes a portion of it, “the exposed portions of the etch stop material 130 are removed to expose the underlying [layer].” *Id.*, [0029]. Thereafter, portions of conductive material 140 are also removed to extend the openings into them. *Id.* The etch-stop-layer removal may use the same or a different etch chemistry compared to that used to extend the openings into the conductive layers. *Id.* The flexibility is beneficial toward reaching the objective of protecting the conductive layer through configuring it with a lower etching rate. Although a high-k dielectric layer is present between the etch-stop and conductive layers in the combination, the flexibility taught by Fang is still advantageous. As an example, a high-k hafnium dioxide etch-stop layer has a higher etching rate than tungsten conductive layers relative to Cl_2 . Banerjee ¶¶ 186-88 (citing Exs. 1025-26).

E. Claim 5:

Claim 5 is obvious in view of a POSITA’s knowledge. As an example, a high-k Al_2O_3 etch-stop layer has a higher etching rate than high-k HfO_2 dielectric layers relative to argon plasma. §X.E.1; Banerjee ¶¶ 189-90 (citing Ex. 1027).

F. Claim 6:

Fang discloses the additional limitation of claim 6. Specifically, *the etch-stop layer* may comprise silicon nitride or, “[a]lternatively, ... a high-k dielectric material, such as *hafnium oxide*.” Fang, [0022]; Banerjee ¶ 191.

G. Claim 7:

Fang discloses the additional limitation of claim 7.

Fang discloses a semiconductor structure with only an etch-stop layer, analogous to the structure formed by Claim 7. Fang, Fig. 6, [0020]; Ex. 1001, claim 1, 17. The layer “may be formed over the stairs 125 at a thickness ranging from about 50 Å to about 1000 Å,” or about 5 nm to 100 nm. Fang, [0021]. Fang’s thickness range overlaps with the claimed *range between 10 nm and 100 nm*. Banerjee ¶¶ 192-93.

H. Claim 8:

Fang discloses the additional limitation of claim 8, specifically, forming the etch-stop layer using “conventional techniques including ... *chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD)*....” Fang, [0020].

Han’s method also uses these processes. *See, e.g.*, Han, [0046], [0048], [0101], [0139]-[0141]. Thus, applying one of these conventional techniques to form etch-stop layer represents nothing more than applying a known technique, which itself provides a motivation and renders claim 8 obvious. *Intel*, 61 F.4th at 1380.

Further, using an existing technique avoids retooling cost of the additional etch-stop layer in the combination, which would have motivated a POSITA to do so. Banerjee ¶¶ 194-95.

I. Claim 9:

Fang discloses the additional limitation of claim 9.

Fang discloses using CMP to planarize the insulating layer and the etch-stop layer so that their top surfaces become coplanar. Fang, [0024]. Since the etch-stop layer covers the staircase, Fang's process *planariz[es] the insulating layer and the staircase structure by using chemical-mechanical-polishing (CMP)*:

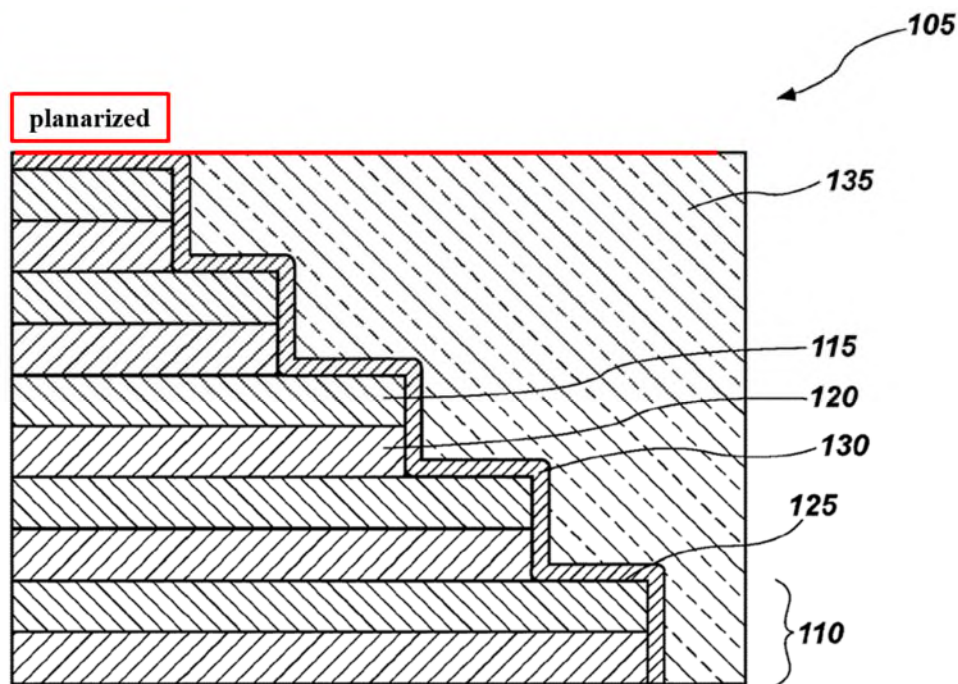


FIG. 3

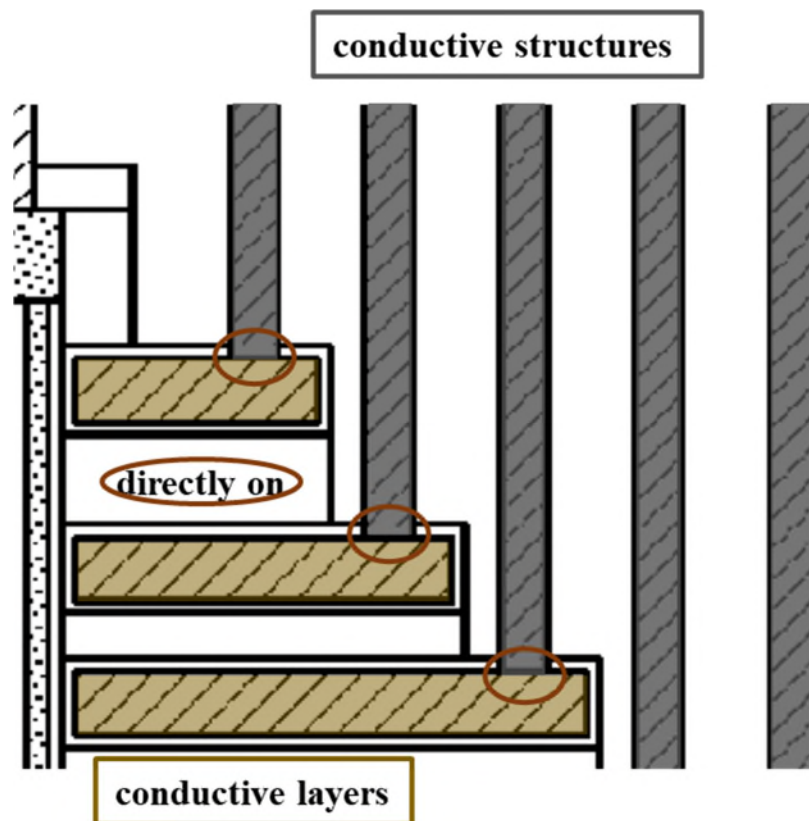
Id., Fig. 3. Fang's process necessarily occurs *after disposing the insulating layer on the etch-stop layer* since the layer must be disposed before it can be planarized.

Han discloses using CMP to planarize the conductive structures. Han, [0065].

Banerjee ¶¶ 196-98.

J. Claim 10:

Han discloses *forming the plurality of conductive structures* (“first contact plugs PLG1” and “second contact plugs PLG2”) *comprises disposing conductive materials inside the plurality of openings* (“lower contact holes LH” and “upper contact holes UH”), *the conductive materials directly on the exposed conductive layer* (“electrodes EL”) *of the each step*:



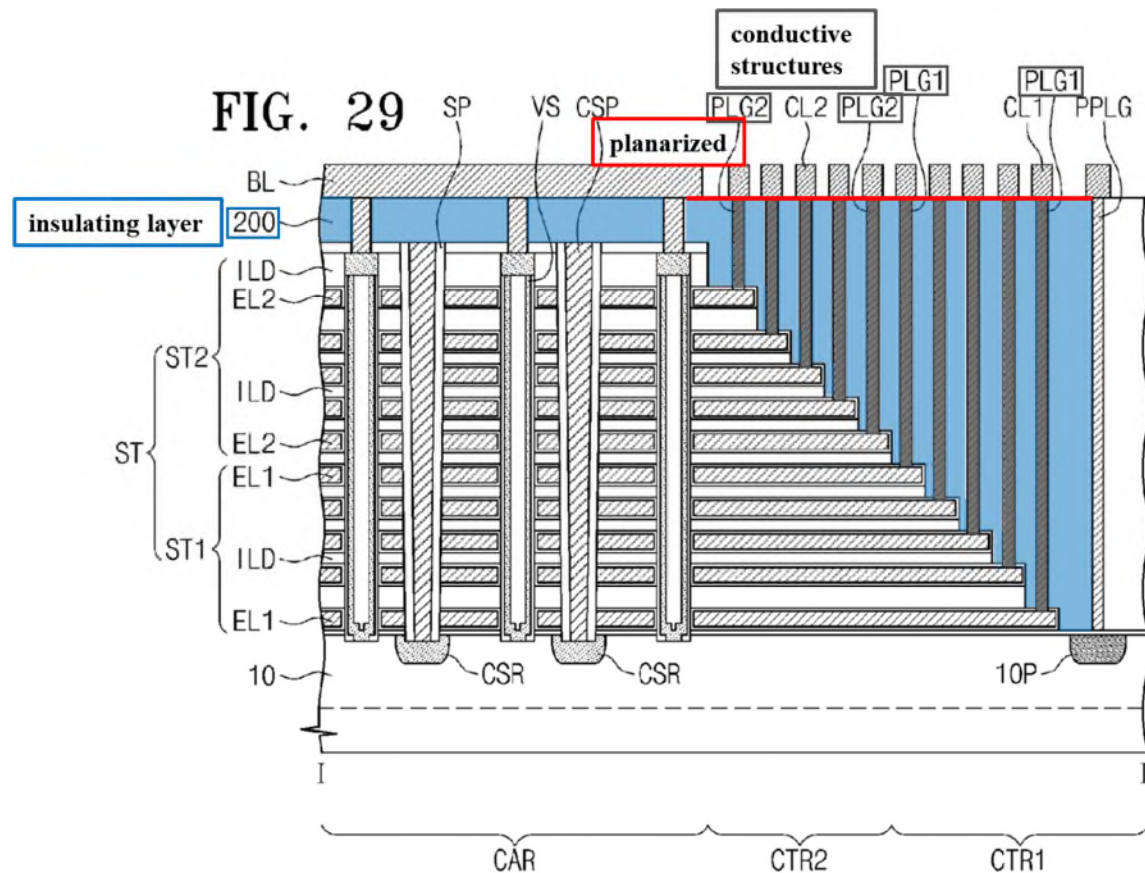
Han, Fig. 29 (partial, enlarged). Specifically, the contact holes LH and UH are etched to expose portion of the electrodes. *Id.*, [0156]. The holes are subsequently

filled with a conductive filling to form contact plugs PLG1 and PLG2. *Id.*, [0161]. The contact plugs “electrically connect the electrodes EL1 and EL2 to the peripheral logic structure.” *Id.*, [0151].

Similarly, Fang discloses the additional limitation of claim 10. Banerjee ¶¶ 199-200.

K. Claim 11:

Han discloses *forming the plurality of conductive structures* (“first contact plugs PLG1” and “second contact plugs PLG2”) *further comprises planarizing the conductive materials* (of the contact plugs) *and the insulating layer* (“upper filling insulation layer” 200). Specifically, when forming the contact plugs, Han “perform[s] a planarization process on the conductive [structure] until a top surface of the upper filling insulation layer 200 is exposed.” Han, [0161]. After planarization, “top surfaces of the first and second contact plugs PLG1 and PLG2 may be substantially coplanar” (*id.*) with other surfaces:



Id., Fig. 29.

Fang also discloses planarizing the insulating layer and the etch-stop layer.

§XII.I. A POSITA would have found it obvious that Han’s and Fang’s planarization processes are at least compatible. Banerjee ¶¶ 201-02.

L. Claim 12:

Han in view of Fang renders obvious *forming the staircase structure* (“stepwise structure” ST) *further comprises performing a repetitive etch-trim process on the sacrificial layers* (“sacrificial layers SL”) *and the dielectric layers* (“insulating layers ILD”).

Fang discloses that “[t]he stairs are formed by repeatedly trimming and etching exposed regions of the conductive structures.” Fang, [0003]. “By conducting repeated etch and trim acts, the stepped profile (e.g., stairs 125) of the staircase structure 105 is formed.” *Id.*, [0019].

A POSITA would have understood Fang’s *repetitive etch-trim process* can be applied on Han’s staircase structure if it is not implied by Han’s disclosure. Specifically, Han discloses that the relative etching selectivities between its sacrificial layers SL and insulating layers ILD “may be relatively great in a wet etching process” but “relatively small in a dry etching process.” Han, [0098]. The former is needed for removing the sacrificial layers while preserving the insulating layers. *Id.*, [0116] (describing a wet etching process “using an etching solution” to remove sacrificial layers SL). The “relatively small” etching selectivities is conducive to the etching process to form the staircase. A mask-trimming process was a conventional process of forming a staircase. Therefore, either Han implies the use of a repetitive etch-trim process, or its use would have been obvious in view of Fang. Banerjee ¶¶ 203-05.

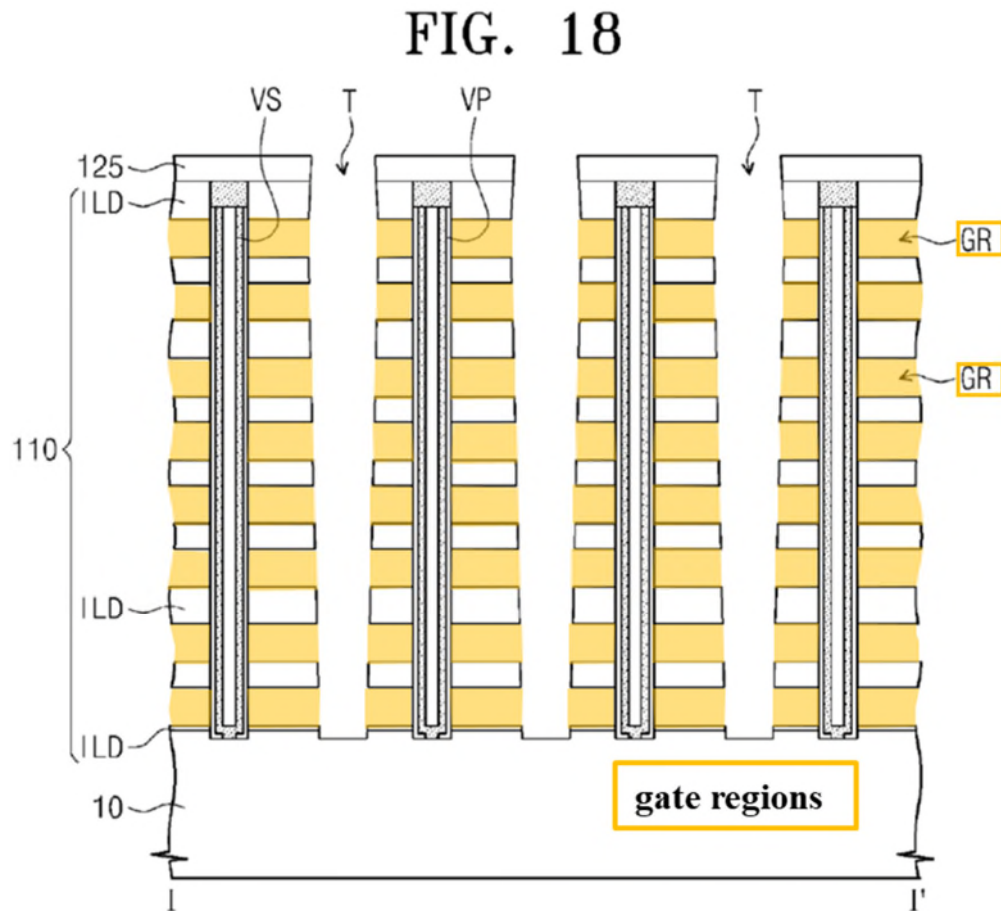
M. Claim 13:

1. [13.PRE]

This preamble simply repeats limitation [1.D]. §XII.A.5; Banerjee ¶ 206.

2. [13.A]

Han discloses *forming a substrate opening* (“trench T”) *through the staircase structure* (“stepwise structure” ST):



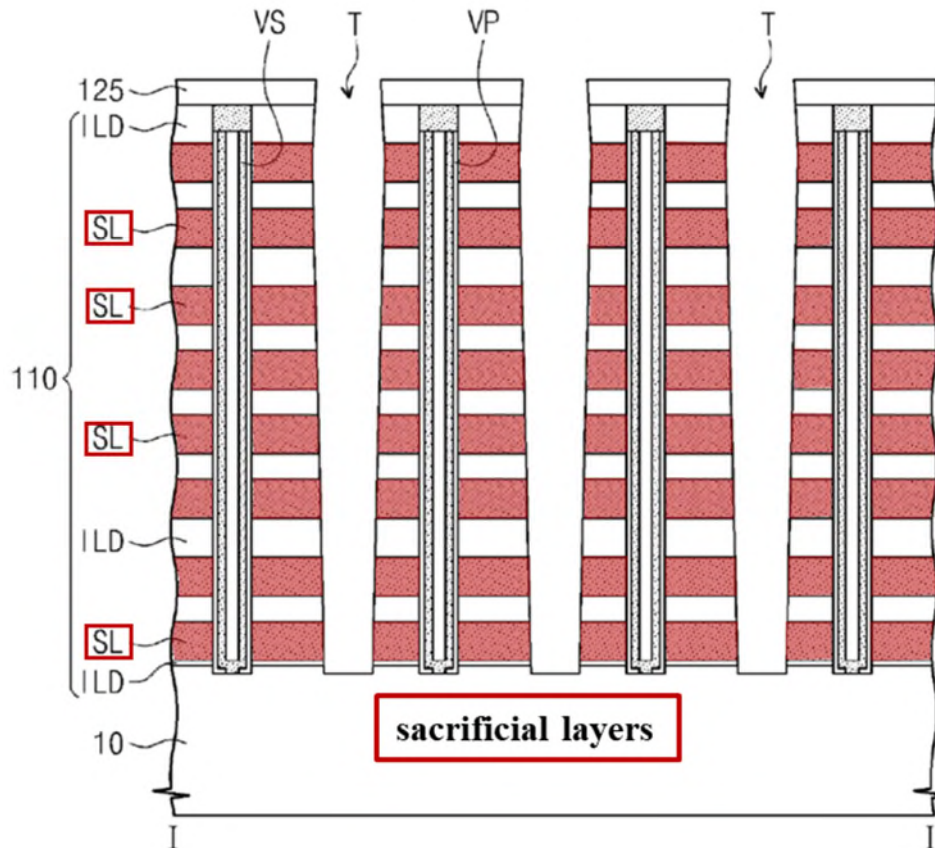
Han, Fig. 18. Trench T “expos[es] the substrate 10 between the vertical structures VS.” *Id.*, [0110], [0112]; Banerjee ¶ 207.

3. [13.B]

Preliminarily, *the substrate* is treated as *the substrate opening*. §X.J.3.

Han discloses *removing the sacrificial layer* (“sacrificial layer SL”) *of each step through the substrate [opening]* (“trench T”). Specifically, trenches T “expose sidewalls of the sacrificial layers SL and the insulating layers ILD.” Han, [0112]:

FIG. 17



Id., Fig. 17. Then, “the sacrificial layers SL exposed by the trenches T may be removed to form gate regions GR between the insulating layers ILD.” *Id.*, [0115]-[0116]; Banerjee ¶¶ 208-09.

4. [13.C]

Han discloses *disposing the first high-k dielectric layer* (“horizontal insulating layer”) *and the conductive layer* (one of “electrodes EL”) *in place of the sacrificial*

layer (“sacrificial layer SL”). Specifically, after the sacrificial layers have been replaced by the gate regions GR, “a horizontal insulating layer may be formed to conformally cover inner surfaces of the gate regions GR.” Han, [0118]. “Subsequently, a gate conductive layer may be formed to fill the gate regions GR....” *Id.*, [0119], §XII.A.5 (showing processing sequence of removing the sacrificial layers and disposing the gate stack layers).

Fang discloses a replacement gate process that was at least compatible with Han’s process. Banerjee ¶¶ 210-11.

N. Claim 14:

Han discloses that *disposing the first high-k dielectric layer* (“horizontal insulating layer”) *comprises disposing hafnium oxide ... [or] aluminum oxide...* As explained, the horizontal insulating layer may comprise a tunnel insulating layer TIL and a blocking insulating layer BK. §XII.A.5. Both sublayers may comprise *hafnium oxide* or *aluminum oxide*. Han, [0140]-[0141]; Banerjee ¶ 212.

O. Claim 15:

Han discloses that *disposing the conductive layer* (one of “electrodes EL”) *comprises disposing tungsten, cobalt, ... copper, [or] aluminum...* Han, [0119] (“the metal layer may include a metal material such as W, Al, ..., Co, or Cu.”).

Similarly, Fang satisfies the additional limitation of claim 15. Banerjee ¶¶ 213-14.

P. Motivation to Combine

A POSITA would have been motivated to adapt Han's staircase by adding Fang's etch-stop layer. It would have been obvious and indeed readily apparent that "the conductive structures [conventionally used for word-line contacts of 3D memory devices] include both shallower conductive structures and the deeper conductive structures." Fang, [0003]. Thus, openings of "various depths" needed to be etched. *Id.*, [0004]. But that resulted in an increased likelihood of "overetch[ing] (*e.g.*, punch through) into the conductive structures." *Id.* "Adjustments to etch chemistries ...[, however,] ha[d] not sufficiently addressed this problem." *Id.* Using multiple masks to prevent punch-through "add[ed] additional processing acts, complexity, and cost to the overall process." *Id.* A POSITA would have recognized Han's method suffered from this exact problem and the shortcomings of the conventional solutions and would have been motivated to apply Fang's solution of adding an etch-stop layer to resolve this problem to "reduc[e] the likelihood of punch through." *Id.*, [0026], [0028].

Notably, this is exactly the problem and purported solution described in the '276 patent. §VI. The '276 patent, however, came later.

The combination also references Fang for dry etching (§XII.C), CMP (§XII.I), and etch-trim (§XII.L). In each case, Han discloses using the same method, and a POSITA would have been motivated to follow Fang's teaching because doing so

would have been cost efficient for reusing the same tools and time efficient for leveraging a POSITA's familiarity with Han. Other specific factors would have further motivated applying Fang's teaching. Anisotropic dry etching, having good directionality, is well suited for etching small but deep openings. CMP was well-known, routine, and well suited for planarizing a top semiconductor surface. And Han implies the use of an etch-and-trim process (§XII.L), which was also well known and routine. Further, a POSITA would have had a reasonable expectation of success in simply applying a method already disclosed by both Han and Fang to the combined, similar embodiment.

The similarities and compatibility of Han and Fang noted throughout this Ground, a POSITA's knowledge of etch-stop layers (as reflected in, *e.g.*, §V, Kim, Chen) and the well-known and routine processes, and the flexibility of layer materials and etchants all would have provided a POSITA a reasonable expectation of success. Banerjee ¶¶ 215-18.

XIII. GROUND 4: HAN IN VIEW OF FANG IN FURTHER VIEW OF CHEN

A. Claim 17:

Chen discloses the additional limitation of claim 17.

Chen discloses *prior to disposing the etch-stop layer* ("second stop layer 220"), *disposing a barrier layer* ("first stop layer 210") *on each step of the plurality of steps*:

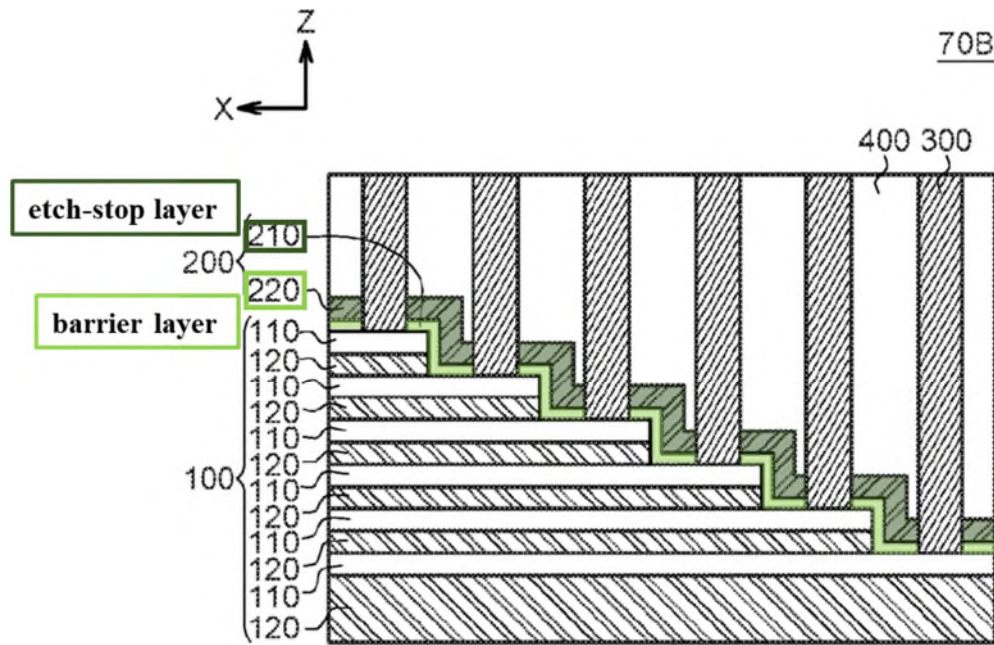


FIG. 7B

Chen, Fig. 7B, [0046] (“the first stop layer 210 is formed on the surfaces of the conductive layers 110, and the second stop layer 220 is formed on the first stop layer 210.”); [0037], [0039].

Chen renders obvious that *the barrier layer* (“first stop layer 210”) *protects underlying structures during the etching of the exposed portions of the etch-stop layer* (“second stop layer 220”). First, these two layers take the place of an *etching stop layer* 200. *Id.*, [0037]. That name indicates that the function of the first stop layer is to stop (or, more precisely, slow down) etching when it reaches the layer, thereby protecting the underlying structures. Moreover, after disclosing many suitable materials for the first and second stop layers, Chen specifically notes that the two layers have “different” materials. Chen, [0041]. A POSITA would have

understood this restriction to mean that the first stop layer serves as an etch stop to the layer above it, *i.e.*, the second stop layer or *the etch-stop layer*. §V; Banerjee ¶¶ 219-221.

B. Claim 18:

Chen discloses that *disposing the barrier layer* (“first stop layer 210”) *comprises disposing one or more of silicon oxide, ... [and] aluminum oxide....* Chen, [0041] (“the first stop layer 210 may include silicon oxide (SiO₂), aluminum oxide (Al_xO_y, *e.g.* Al₂O₃)....”); Banerjee ¶ 222.

C. Motivation to Combine

A POSITA would have been motivated to add Chen’s barrier layer to Han’s staircase structure with Fang’s etch-stop layer.

Unintended short circuits between circuit components are a basic electrical-engineering problem to be avoided. Short circuit between conductive layers in a word-line staircase was also known to be an issue to be prevented. Ex. 1028, 6:22-28. Chen discloses a short-circuit phenomenon through electron tunneling between conductive layers of a word-line staircase. Chen, [0049]. A POSITA would have recognized this phenomenon should be avoided. Banerjee ¶¶ 223-24.

Chen also discloses a solution: increasing the tunneling length of the etch-stop layer(s) to reduce tunneling current, thereby “more effectively electrically isolat[ing] [the conductive layers] from one another.” Chen, [0004]. Adding a first stop layer

increases the tunneling length. Specifically, Fang’s etch-stop layer may comprise a high-k dielectric. Fang, [0022]. A single aluminum-oxide high-k-dielectric etch-stop layer can have a tunneling length L_2 shown in Figure 8B. Chen, [0048]. When a silicon-oxide barrier layer is added, the total tunneling length becomes L_4 as shown in Figure 8D. *Id.*, [0052]. It is evident that L_4 is larger than L_2 :

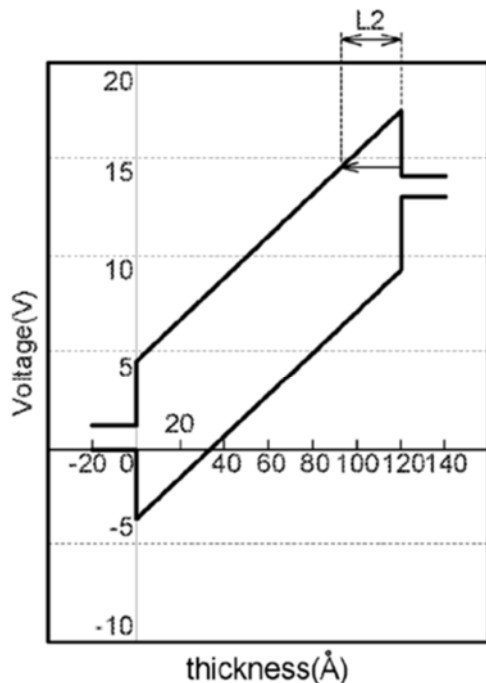


FIG. 8B

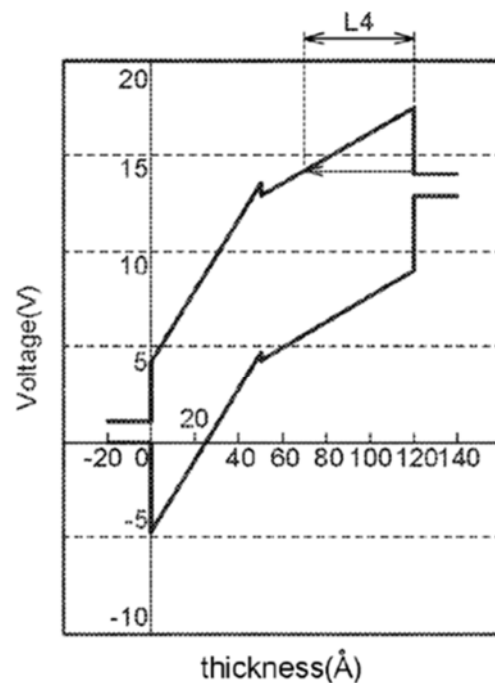


FIG. 8D

Id., Figs. 8B, 8D. Thus, by adding a barrier layer to a high-k dielectric etch-stop layer, “the overall etching stop layer 200 [including the barrier layer] can further provide a relatively large tunneling length,” reducing the “occurrence of short circuit between different conductive layers” and increasing “the stability of the semiconductor device.” *Id.*, [0053].

Further, like Fang, Chen discloses an embodiment with only one etch-stop layer 200. Chen, Fig. 4B, [0035]. The etch-stop layer 200 may comprise two stop layers 210 and 220 as shown in Figure 7B. *Id.*, [0037], [0046]. Thus, a one- or two-stop-layer embodiment represents a design choice, both suitable for word-line contact structures. Such a suitable option itself provides a motivation to combine. *Intel*, 61 F.4th at 1380.

The manufacturing methods to form two etch-stop layers is simply that one step of forming layer 200 “is divided into two separate steps.” Chen, [0059]. A POSITA would have had a reasonable expectation of success of dividing one deposition step into two. Indeed, reflecting the knowledge of a POSITA, Kim also discloses both one- and two-etch-stop-layer embodiments and simply notes “[i]n some embodiments, the etch stop layer 125 may include a first stop layer 125a ... and a second stop layer 125b....” Kim, [0187]. The brevity of both Chen’s and Kim’s descriptions confirms that implementing a two-layer embodiment was well within the knowledge and skill of a POSITA, leading to a reasonable expectation of success. Banerjee ¶¶ 225-27.

XIV. SECONDARY CONSIDERATIONS

Petitioner is unaware of any applicable secondary considerations of nonobviousness. None were identified during prosecution. See generally Ex. 1002.

Even if such considerations existed, none would overcome the strong *prima facie* showing of obviousness. Banerjee ¶ 228.

XV. CONCLUSION

Petitioner respectfully requests that the Board enter a final written decision finding the Challenged Claims unpatentable.

Respectfully submitted,

Dated: November 29, 2024

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 13,881 words.

Dated: November 29, 2024

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Petition for *Inter Partes* Review and associated exhibits were caused to be served on November 29, 2024 via overnight courier upon the following counsel of record for Patent Owner:

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Copies of this Petition and accompanying documents and exhibits were also served via electronic mail on Patent Owner's counsel of record for related PTAB proceedings and in the related district court litigation – ROPES & GRAY LLP and LATHAW & WATKINS LLP:

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