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Application Number: 16865056

Document Date: 05/01/2020

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Form Revision Date: March 1, 2019

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UTILITY PATENT APPLICATION TRANSMITTAL <i>(Only for new nonprovisional applications under 37 CFR 1.53(b))</i>	Attorney Docket No.	4123.0480003
	First Named Inventor	Jifeng ZHU
	Title	See 1 in Addendum
	Priority Mail Express® Label No.	

APPLICATION ELEMENTS <i>See MPEP chapter 600 concerning utility patent application contents.</i>	Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450
1. ☐ Fee Transmittal Form (PTO/SB/17 or equivalent) 2. ☐ Applicant asserts small entity status. See 37 CFR 1.27 3. ☐ Applicant certifies micro entity status. See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent. 4. ☒ Specification [Total Pages <u>21</u>] Both the claims and abstract must start on a new page. (See MPEP § 608.01(a) for information on the preferred arrangement) 5. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets <u>13</u>] 6. ☒ Inventor's Oath or Declaration [Total Pages <u>4</u>] (including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e)) a. ☐ Newly executed (original or copy) b. ☒ A copy from a prior application (37 CFR 1.63(d)) 7. ☒ Application Data Sheet * See note below. See 37 CFR 1.76 (PTO/AIA/14 or equivalent) 8. CD-ROM or CD-R in duplicate, large table, or Computer Program (Appendix) ☐ Landscape Table on CD 9. Nucleotide and/or Amino Acid Sequence Submission (if applicable, items a. – c. are required) a. ☐ Computer Readable Form (CRF) b. ☐ Specification Sequence Listing on: i. ☐ CD-ROM or CD-R (2 copies); or ii. ☐ Paper c. ☐ Statements verifying identity of above copies	ADDRESS TO: ACCOMPANYING APPLICATION PAPERS 10. ☐ Assignment Papers (cover sheet & document(s)) Name of Assignee <u>Yangtze Memory Technologies Co., Ltd.</u> 11. ☐ 37 CFR 3.73(c) Statement ☒ Power of Attorney (when there is an assignee) 12. ☐ English Translation Document (if applicable) 13. ☒ Information Disclosure Statement (PTO/SB/08 or PTO-1449) ☐ Copies of citations attached 14. ☐ Preliminary Amendment 15. ☐ Return Receipt Postcard (MPEP § 503) (Should be specifically itemized) 16. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed) 17. ☐ Nonpublication Request Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent. 18. ☒ Other: Authorization under 37 CFR 1.136(a)(3) _____ _____ _____ _____

***Note:** (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS					
☒ The address associated with Customer Number: <u>26111</u> OR ☐ Correspondence address below					
Name					
Address					
City		State		Zip Code	
Country		Telephone		Email	
Signature	/Donald J. Featherstone/			Date	5/1/2020
Name (Print/Type)	Donald J. Featherstone			Registration No. (Attorney/Agent)	33,876

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Addendum

1. WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: ZHU *et al.*

Applicant: YANGTZE MEMORY
TECHNOLOGIES CO., LTD.

Application No.: To Be Assigned

(Divisional of Appl. No. 16/126,947 ; Filed:
September 10, 2018)

Filed: Herewith

Confirmation No.: To Be Assigned

Art Unit: To Be Assigned

Examiner: To Be Assigned

Atty. Docket: 4123.0480003

Title: **WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY
DEVICES AND FABRICATION METHODS THEREOF**

**Authorization to Treat a Reply as Incorporating an
Extension of Time Under 37 C.F.R. § 1.136(a)(3)**

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

The U.S. Patent and Trademark Office is hereby authorized to treat any concurrent or future reply that requires a petition for an extension of time under this paragraph for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. The U.S. Patent and Trademark Office is hereby authorized to charge all required extension of time fees to our Deposit Account No. 19-0036, if such fees are not otherwise provided for in such reply.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: 5/1/2020

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0480003
		Application Number	
Title of Invention	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1					Remove	
Legal Name						
Prefix	Given Name	Middle Name	Family Name	Suffix		
	Jifeng		ZHU			
Residence Information (Select One) US Residency • Non US Residency Active US Military Service						
City	Wuhan	Country of Residence ⁱ		CN		
Mailing Address of Inventor:						
Address 1		Yangtze Memory Technologies Co., Ltd.				
Address 2		18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone				
City	Wuhan	State/Province				
Postal Code		Country ⁱ	CN			
Inventor 2					Remove	
Legal Name						
Prefix	Given Name	Middle Name	Family Name	Suffix		
	Zhenyu		LU			
Residence Information (Select One) US Residency • Non US Residency Active US Military Service						
City	Wuhan	Country of Residence ⁱ		CN		
Mailing Address of Inventor:						
Address 1		Yangtze Memory Technologies Co., Ltd.				
Address 2		18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone				
City	Wuhan	State/Province				
Postal Code		Country ⁱ	CN			
Inventor 3					Remove	
Legal Name						

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0480003
		Application Number	
Title of Invention	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jun		CHEN	
Residence Information (Select One) US Residency ☒ Non US Residency Active US Military Service				
City	Wuhan	Country of Residence ⁱ	CN	

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.			
Address 2	18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone			
City	Wuhan	State/Province		
Postal Code		Country ⁱ	CN	
Inventor	4	Remove		
Legal Name				

Prefix	Given Name	Middle Name	Family Name	Suffix
	Si Ping		HU	
Residence Information (Select One) US Residency ☒ Non US Residency Active US Military Service				
City	Wuhan	Country of Residence ⁱ	CN	

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.			
Address 2	18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone			
City	Wuhan	State/Province		
Postal Code		Country ⁱ	CN	
Inventor	5	Remove		
Legal Name				

Prefix	Given Name	Middle Name	Family Name	Suffix
	Xiaowang		DAI	
Residence Information (Select One) US Residency ☒ Non US Residency Active US Military Service				
City	Wuhan	Country of Residence ⁱ	CN	

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.			
Address 2	18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone			
City	Wuhan	State/Province		
Postal Code		Country ⁱ	CN	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0480003
		Application Number	
Title of Invention	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		

Inventor 6 Remove				
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	an		YAO	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Wuhan	Country of Residence ⁱ	CN	

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.			
Address 2	18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone			
City	Wuhan	State/Province		
Postal Code		Country ⁱ	CN	

Inventor 7 Remove				
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Li Hong		XIAO	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Wuhan	Country of Residence ⁱ	CN	

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.			
Address 2	18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone			
City	Wuhan	State/Province		
Postal Code		Country ⁱ	CN	

Inventor 8 Remove				
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	A Man		ZHENG	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Wuhan	Country of Residence ⁱ	CN	

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.			
Address 2	18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone			

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0480003
		Application Number	
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City	Wuhan		State/Province	
Postal Code		Country i	CN	
Inventor	9		Remove	
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Kun		BAO	

Residence Information (Select One)		US Residency	☒ Non US Residency	Active US Military Service
City	Wuhan	Country of Residence i	CN	

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.			
Address 2	18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone			
City	Wuhan		State/Province	
Postal Code		Country i	CN	
Inventor	10		Remove	
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Haohao		YANG	

Residence Information (Select One)		US Residency	☒ Non US Residency	Active US Military Service
City	Wuhan	Country of Residence i	CN	

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.			
Address 2	18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone			
City	Wuhan		State/Province	
Postal Code		Country i	CN	

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button.

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ An Address is being provided for the correspondence information of this application.

Customer Number	26111		
Email Address		Add Email	Remove Email

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0480003
		Application Number	
Title of Invention	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		

Application Information:

Title of the Invention	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		
Attorney Docket Number	4123.0480003	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	13	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	26111		

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0480003
		Application Number	
Title of Invention	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Division of	16126947	2018-09-10
Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16126947	Continuation of	PCT/CN2018/101308	2018-08-20
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)ⁱ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Remove
201710774754.6	CN	2017-08-31	Access Code ^j (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013. ☐ NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.
--

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0480003
		Application Number	
Title of Invention	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0480003
		Application Number	
Title of Invention	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.			
Applicant 1		Remove	
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.			
		Clear	
☒ Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor	
Person to whom the inventor is obligated to assign.		Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:			
Name of the Deceased or Legally Incapacitated Inventor:			
If the Applicant is an Organization check here. ☒			
Organization Name	Yangtze Memory Technologies Co., Ltd.		
Mailing Address Information For Applicant:			
Address 1	18 Gaoxin 4th Road		
Address 2	East Lake High-Tech Development Zone		
City	Wuhan	State/Province	
Country	CN	Postal Code	
Phone Number		Fax Number	
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button. Add			

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0480003
		Application Number	
Title of Invention	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		

Assignee	1		
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.			
Remove			
If the Assignee or Non-Applicant Assignee is an Organization check here. ☒			
Organization Name	Yangtze Memory Technologies Co., Ltd.		
Mailing Address Information For Assignee including Non-Applicant Assignee:			
Address 1	18 Gaoxin 4th Road		
Address 2	East Lake High-Tech Development Zone		
City	Wuhan	State/Province	
Country ⁱ	CN	Postal Code	
Phone Number		Fax Number	
Email Address			
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add			

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). However, if this Application Data Sheet is submitted with the **INITIAL** filing of the application and either box A or B is **not** checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Donald J. Featherstone/		Date (YYYY-MM-DD)	2020-05-01
First Name	Donald	Last Name	Featherstone	Registration Number
				33,876
Additional Signature may be generated within this form by selecting the Add button.				Add

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0480003
		Application Number	
Title of Invention	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF

CROSS-REFERENCE TO RELATED APPLICATIONS AND INCORPORATION BY REFERENCE

[0001] This application is a divisional of U.S. Non-provisional Patent Application No. 16/126,947 filed on September 10, 2018 and titled “Word Line Contact Structure For Three-Dimensional Memory Devices And Fabrication Methods Thereof,” which claims priority to Chinese Patent Application No. 201710774754.6, filed on August 31, 2017 and PCT Patent Application No. PCT/CN2018/101308, filed on August 20, 2018, which are incorporated herein by reference in their entirety.

TECHNICAL FIELD

[0002] The present disclosure generally relates to the field of semiconductor technology, and more particularly, to a method for forming a three-dimensional (3D) memory device.

BACKGROUND

[0003] Planar memory cells are scaled to smaller sizes by improving process technology, circuit design, programming algorithm, and fabrication process. However, as feature sizes of the memory cells approach a lower limit, planar process and fabrication techniques become challenging and costly. As such, memory density for planar memory cells approaches an upper limit. A three-dimensional (3D) memory architecture can address the density limitation in planar memory cells.

BRIEF SUMMARY

[0004] Embodiments of a word line contact structure for three-dimensional (3D) memory array and methods for forming the same are described in the present disclosure.

[0005] In some embodiments, a method for forming a 3D memory structure is described. The method includes forming a stack of films on a substrate. The stack of films includes a plurality of alternately-arranged oxide and nitride layers. The method also includes etching

the stack of films to form a staircase structure. The method further includes forming a second oxide layer on the stack of films. The method includes forming an etch-stop layer on the top surface of the second oxide layer of the staircase structure.

[0006] The method further includes disposing a filling material on the etch-stop layer of the staircase structure. The filling material can be a third oxide layer. Using chemical-mechanical-polishing (CMP) processes, for example, the top surface of the third oxide layer over each level of staircase structure is made coplanar with the top surface of the uppermost portion of the etch-stop layer.

[0007] The method also includes etching through the stack of films, from the top surface of the uppermost etch-stop layer down to the substrate surface, to form openings that expose the substrate. Through these openings, nitride layers of the staircase structure can be removed and replaced by high-k dielectric materials and metal films.

[0008] The method also includes etching the third oxide layer with highly selective etching and exposing the etch-stop layer of each level of the staircase structure for vertical interconnect access (VIA). The method also includes removing exposed etch-stop layer in the openings of contact VIAs by reverse selective etching and further exposing the second oxide layer on each level of the staircase structure. The method includes removing the exposed second oxide layer and high-k dielectric material in the openings of contact VIAs and exposing the metal film of each level of the staircase structure. The method also includes forming metallic connections to the metal film of each level of the staircase structure through subsequent metal filling and polishing.

[0009] In some embodiments, the etch-stop layer can include silicon nitride.

[0010] In some embodiments, the metal film surrounded by high-k dielectric material can include tungsten.

[0011] In some embodiments, the high-k dielectric material can include hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide films, or a combination thereof.

[0012] In some embodiments, the 3D memory structure can be formed with any one of the processes stated above.

[0013] In some embodiments, a 3D memory structure includes a substrate and a film stack having a plurality of alternately-arranged first oxide and metal films surrounded by high-k

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dielectric layers. The film stack has a staircase shape and is formed on the surface of the substrate. The 3D memory structure further includes a second oxide layer, also in the shape of staircase, over the film stack of the staircase structure. The 3D memory structure also includes an etch-stop film, in the shape of staircase, over the second oxide layer of the staircase structure. The 3D memory structure further includes a third oxide film formed on the etch-stop layer. A top surface of the third oxide film is formed coplanar with a top surface of the uppermost portion of etch-stop layer over the staircase structure. The 3D memory structure further includes openings for vertical interconnect access (VIA) that extend through the third oxide layer, the etch-stop film, the second oxide layer, and the high-k dielectric layers to expose the metal film. The 3D memory structure further includes contact openings that extend through the staircase structure that expose the substrate to facilitate the formation of contacts.

[0014] Other aspects of the present disclosure can be understood by those skilled in the art in light of the description, the claims, and the drawings of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate embodiments of the present disclosure and, together with the description, further serve to explain the principles of the present disclosure and to enable a person skilled in the pertinent art to make and use the present disclosure.

[0016] Fig. 1 illustrates a cross-sectional view of a staircase structure with a stack of films including a plurality of alternately insulating layers and sacrificial layers, in accordance with some embodiments of the present disclosure.

[0017] Fig. 2 illustrates a cross-sectional view of a staircase structure and an insulating layer formed on the staircase structure, in accordance with some embodiments of the present disclosure.

[0018] Fig. 3 illustrates a cross-sectional view of a staircase structure and an etch-stop layer formed on the staircase structure, in accordance with some embodiments of the present disclosure.

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- [0019] Fig. 4 illustrates a cross-sectional view of a staircase structure filled with an insulating material, in accordance with some embodiments of the present disclosure.
- [0020] Fig. 5A and 5B illustrate cross-sectional views of a staircase structure having alternately-arranged insulating and gate materials, in accordance with some embodiments of the present disclosure.
- [0021] Fig. 6 illustrates a cross-sectional view of a staircase structure after the etching of the insulating films, in accordance with some embodiments of the present disclosure.
- [0022] Fig. 7 illustrates a cross-sectional view of a staircase structure after the etching of an etch-stop layer and exposing of an insulating layer, in accordance with some embodiments of the present disclosure.
- [0023] Fig. 8A and 8B illustrate cross-sectional views of a staircase structure after the etching of an insulating layer and a high-k dielectric layer, in accordance with some embodiments of the present disclosure.
- [0024] Fig. 9A and 9B illustrate cross-sectional views of a staircase structure after the filling of openings with a conductive film, in accordance with some embodiments of the present disclosure.
- [0025] Fig. 10 illustrates a process flow for forming multi-level contacts in a 3D memory structure, in accordance with some embodiments of the present disclosure.
- [0026] The features and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings, in which like reference characters identify corresponding elements throughout. In the drawings, like reference numbers generally indicate identical, functionally similar, and/or structurally similar elements. The drawing in which an element first appears is indicated by the leftmost digit(s) in the corresponding reference number.
- [0027] Embodiments of the present disclosure will be described with reference to the accompanying drawings.

DETAILED DESCRIPTION

- [0028] Although specific configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the pertinent art

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will recognize that other configurations and arrangements can be used without departing from the spirit and scope of the present disclosure. It will be apparent to a person skilled in the pertinent art that the present disclosure can also be employed in a variety of other applications.

[0029] It is noted that references in the specification to “one embodiment,” “an embodiment,” “an example embodiment,” “some embodiments,” etc., indicate that the embodiment described can include a particular feature, structure, or characteristic, but every embodiment can not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in connection with an embodiment, it would be within the knowledge of a person skilled in the pertinent art to affect such feature, structure or characteristic in connection with other embodiments whether or not explicitly described.

[0030] In general, terminology can be understood at least in part from usage in context. For example, the term “one or more” as used herein, depending at least in part upon context, can be used to describe any feature, structure, or characteristic in a singular sense or can be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as “a,” “an,” or “the,” again, can be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context. In addition, the term “based on” can be understood as not necessarily intended to convey an exclusive set of factors and may, instead, allow for existence of additional factors not necessarily expressly described, again, depending at least in part on context.

[0031] It should be readily understood that the meaning of “on,” “above,” and “over” in the present disclosure should be interpreted in the broadest manner such that “on” not only means “directly on” something, but also includes the meaning of “on” something with an intermediate feature or a layer therebetween. Moreover, “above” or “over” not only means “above” or “over” something, but can also include the meaning it is “above” or “over” something with no intermediate feature or layer therebetween (i.e., directly on something).

[0032] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper,” and the like, can be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The

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spatially relative terms are intended to encompass different orientations of the device in use or process step in addition to the orientation depicted in the figures. The apparatus can be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein can likewise be interpreted accordingly.

[0033] As used herein, the term “substrate” refers to a material onto which subsequent material layers are added. The substrate includes a top surface and a bottom surface. The top surface of the substrate is where a semiconductor device is formed, and therefore the semiconductor device is formed at a top side of the substrate. The bottom surface is opposite to the top surface and therefore a bottom side of the substrate is opposite to the top side of the substrate. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.

[0034] As used herein, the term “layer” refers to a material portion including a region with a thickness. A layer has a top side and a bottom side where the bottom side of the layer is relatively close to the substrate and the top side is relatively away from the substrate. A layer can extend over the entirety of an underlying or overlying structure, or can have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any set of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend horizontally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow. A layer can include multiple layers. For example, an interconnect layer can include one or more conductor and contact layers (in which contacts, interconnect lines, and/or vias are formed) and one or more dielectric layers.

[0035] As used herein, the term “nominal/nominally” refers to a desired, or target, value of a characteristic or parameter for a component or a process step, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances.

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As used herein, the term “about” indicates the value of a given quantity that can vary based on a particular technology node associated with the subject semiconductor device. Based on the particular technology node, the term “about” can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., $\pm 10\%$, $\pm 20\%$, or $\pm 30\%$ of the value).

[0036] In the present disclosure, the term “horizontal/horizontally/lateral/laterally” means nominally parallel to a lateral surface of a substrate. In the present disclosure, the term “each” may not only necessarily mean “each of all,” but can also mean “each of a subset.”

[0037] As used herein, the term “3D memory device” refers to a semiconductor device with vertically oriented strings of memory cell transistors (referred to herein as “memory strings,” such as NAND strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate. As used herein, the term “vertical/vertically” means nominally perpendicular to the lateral surface of a substrate.

[0038] In some embodiments, a NAND string or a 3D memory device includes a semiconductor pillar (e.g., silicon pillar) that extends vertically through a plurality of conductor/dielectric layer pairs. The plurality of conductor/dielectric layer pairs are also referred to herein as an “alternating conductor/dielectric stack.” The conductor layer of the alternating conductor/dielectric stack can be used as a word line (electrically connecting one or more control gates). An intersection of a word line and the semiconductor pillar forms a memory cell. Vertically-oriented memory strings require an electrical connection between the conductors materials (e.g., word line plates or control gates) and access lines (e.g., back end of line interconnection) so that each of the memory cells along the memory strings or in the 3D memory device can be uniquely selected for writing or reading functions. One method of forming electrical connections includes forming a staircase structure on an alternating conductor/dielectric stack.

[0039] As the demand for higher storage capacity continues to increase, the number of vertical levels of the memory cells and staircase structures also increases. Accordingly, it is challenging to balance the manufacturing throughput and the process complexity/cost.

[0040] Lithography and etching processes can be used to open contact areas for forming electrical connection to the conductive layer on each level of the staircase structure. Due to topology of staircase structures, depth of the contact hole from the top surface to each level of the staircase depends on the location of each level. For example, contact holes for lower

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levels may be deeper than contact holes for upper levels. Typically, all of the contact holes are formed with a single lithography mask and etching process. Often, before contact holes to the bottom levels are entirely formed, the materials exposed in contact holes at the upper levels are over-etched and lost. To resolve this issue, two or more lithography masks are used to separate etching processes, which adds cost and complexity to the fabrication process.

[0041] Various embodiments in the present disclosure provide methods and structures for improving word line contacts for 3D memory devices. In the present disclosure, a single lithography mask can be used to form contact areas for word lines of 3D memory array. By adding an etch-stop film over the staircase structure, openings of the vertical interconnect access (VIA) contacts for each level of the staircase structure can be formed simultaneously. The etch-stop film protects underlying layers during etching processes that form contact VIAs. The etch-stop film is exposed on each level of the staircase structure by a selective etching process, and then removed by reverse selective etching. Accordingly, the disclosed methods and structures can improve fabrication yield and reduce cost. The methods and structures described herein can be used to form semiconductor interconnect structures for inter-connecting components at different layers with an uneven topology.

[0042] Fig. 1 illustrates a staircase structure 100 having an alternating layer stack on a top surface of a substrate 101. Each staircase step includes a staircase layer (SC layer) 102, wherein the SC layer 102 includes an exposed top surface 102T and a side surface 102S. Each SC layer 102 includes a first insulating layer 104 and a sacrificial layer 106. The bottommost and the uppermost material of the staircase structure 100 can include the first insulating layer 104.

[0043] In some embodiments, the substrate 101 includes any suitable material for supporting the 3D memory structure. For example, the substrate 101 can include silicon, silicon germanium, silicon carbide, silicon on insulator (SOI), germanium on insulator (GOI), glass, gallium nitride, gallium arsenide, any suitable III-V compounds, any other suitable material, and/or combinations thereof.

[0044] In some embodiments, the first insulating layer 104 can include any suitable insulating materials, for example, silicon oxide, silicon oxynitride, silicon nitride, TEOS, aluminum oxide, or silicon oxide with F-, C-, N-, and/or H- incorporation.

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- [0045]** In some embodiments, the sacrificial layer 106 includes any suitable material that is different from the first insulating layer 104 and can be removed selectively. For example, the sacrificial layer 106 can include silicon oxide, silicon oxynitride, silicon nitride, TEOS, polycrystalline silicon, polycrystalline germanium, polycrystalline germanium-silicon, and/or combinations thereof. In some embodiments, the sacrificial layer 106 also includes amorphous semiconductor materials, such as amorphous silicon or amorphous germanium.
- [0046]** In some embodiments, the first insulating layer 104 can be silicon oxide and the sacrificial layer 106 can be silicon nitride.
- [0047]** In some embodiments, a thickness of the first insulating layer 104 or the sacrificial layer 106 can be between about 10 nm and about 200 nm. In some embodiments, a thickness of the SC layer 102 can be different for each staircase level.
- [0048]** The formation of the first insulating layer 104 and the sacrificial layer 106 can include any suitable deposition methods such as, chemical vapor deposition (CVD), physical vapor deposition (PVD), plasma-enhanced CVD (PECVD), low pressure chemical vapor deposition (LPCVD), sputtering, metal-organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), any other suitable deposition method, and/or combinations thereof. In some embodiments, polycrystalline semiconductor material can be deposited in an amorphous state and converted to polycrystalline through subsequent thermal treatments.
- [0049]** The plural steps of the staircase structure 100 is formed by applying a repetitive etch-trim process on the disposed film stacks using a mask stack (not shown). In some embodiments, the mask stack can include a photoresist or carbon-based polymer material. In some embodiments, the mask stack is removed after forming the staircase structure 100.
- [0050]** The etch-trim process includes an etching process and a trimming process. During the etching process, the portion of SC layer 102 with exposed top surface 102T are removed. The etch depth is a thickness of the SC layer 102. The etching process for the first insulating layer 104 can have a high selectivity over the sacrificial layer 106, and/or vice versa. Accordingly, an underlying SC layer 102 can function as an etch-stop layer. As a result, one staircase step is formed during each etch-trim cycle.
- [0051]** In some embodiments, the SC layer 102 can be etched using an anisotropic etching such as a reactive ion etch (RIE) or other dry etch processes. In some embodiments, the etchant can include fluorine based gases such as, for example, carbon-fluorine (CF₄) based

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gases, hexafluoroethane (C₂F₆) based gases, and/or any other suitable gases. In some embodiments, the SC layer 102 can be removed by wet chemistry, such as hydrofluoric acid or a mixture of hydrofluoric acid and ethylene glycol. In some embodiments, a timed etching approach can be used. The methods and etchants to remove a single layer stack should not be limited by the embodiments of the present disclosure.

[0052] The trimming process includes applying a suitable etching process (e.g., an isotropic dry etch or a wet etch) on the mask stack such that the mask stack can be pulled back laterally. The lateral pull-back dimension determines the lateral dimension “a” of each step of the staircase structure 100, as illustrated in Fig. 1. After mask stack trimming, one portion of the topmost SC layer 102 is exposed and the other portion of the topmost SC layer 102 remains covered by the mask stack. The next cycle of etch-trim process resumes with the etching process.

[0053] In some embodiments, the mask stack trimming process can include dry etching, such as RIE using O₂, Ar, N₂, etc.

[0054] In some embodiments, the topmost SC layer 102 can be covered by the first insulating layer 104. A process step of removing the first insulating layer 104 can be added to the etching process of each etch-trim cycle to form the staircase structure 100.

[0055] Referring to Fig. 2, a staircase structure 200 is formed by disposing a second insulating layer 208 on the staircase structure 100. The second insulating layer 208 covers the staircase structure 100, including a top surface 102T and a side surface 102S of each SC layer 102 (shown in Fig. 1). In some embodiments, the second insulating layer 208 can be an optional barrier layer. For example, the second insulating layer 208 can be used as a barrier layer for protecting the underlying structure during subsequent etching processes. In some embodiments, thicknesses of the second insulating layer 208 can be about the same on a side surface 102S and a top surface 102T. In some embodiments, thickness of the second insulating layer 208 on the side surface 102S can be thicker or thinner than that on the top surface 102T. In some embodiments, a thickness of the second insulating layer 208 can be in a range between 1 nm to 200 nm (e.g., 1 nm, 2 nm, 3 nm, 4 nm, 5 nm, 6 nm, 7 nm, 8 nm, 9 nm, 10 nm, 20 nm, 40 nm, 50 nm, 60 nm, 80 nm, 90 nm, 100 nm, 140 nm, 160 nm, 170 nm, 200 nm, any range bounded by the lower end by any of these values, or in any range defined by any two of these values). In some embodiments, the second insulating layer 208 can be

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made of similar material as the first insulating layer 104. In some embodiments, the second insulating layer 208 can be formed using similar techniques as the processes used to form the first insulating layer 104.

[0056] Referring to Fig. 3, a staircase structure 300 is formed by disposing an etch-stop layer 310 on the staircase structure 200. A thickness of the etch-stop layer 310 can be in a range between 10 nm to 1000 nm (e.g., 10 nm, 20 nm, 30 nm, 40 nm, 50 nm, 60 nm, 70 nm, 80 nm, 90 nm, 100 nm, 200 nm, 300 nm, 400 nm, 500 nm, 600 nm, 700 nm, 800 nm, 900 nm, 1000 nm, any range bounded by the lower end by any of these values, or in any range defined by any two of these values). The etch-stop layer 310 can be made of any suitable insulating material that is different from the second insulating layer 208. In some embodiments, the etch-stop layer 310 can be disposed on the second insulating layer 208. In some embodiments, the second insulating layer 208 is optional and the etch-stop layer 310 can be directly disposed on the staircase structure 100. In some embodiments, the etch-stop layer 310 can cover the staircase structure 200, including the top surface 102T and the side surface 102S of each SC layer 102. In some embodiments, the thickness of the etch-stop layer 310 on a side surface 102S can be the same as that on a top surface 102T. In some embodiments, the thickness of the etch-stop layer 310 on the side surface 102S can be thicker or thinner than that on the top surface 102T. In some embodiments, etch-stop layer 310 can be made of silicon nitride, silicon oxynitride, spin-on-dielectric, and/or high-k dielectric films such as hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, or lanthanum oxide films. In some embodiments, etch-stop layer 310 can be disposed by any suitable methods such as CVD, PVD, PECVD, LPCVD, sputtering, MOCVD, ALD, spin-coating, or any other suitable deposition method, and/or combinations thereof.

[0057] Referring to Fig. 4, a staircase structure 400 is formed by disposing a third insulating layer 420 over the staircase structure 300, with a top surface 420S being coplanar with the top surface 310S of the uppermost portion of the etch-stop layer 310. The third insulating layer 420 can be made of any a suitable insulator that is different from the etch-stop layer 310. In some embodiments, the third insulating layer 420 is made of a similar material as the first insulating layer 104. In some embodiments, the forming of the third insulating layer 420 can use similar techniques as forming the first insulating layer 104. In some embodiments, the forming of the third insulating layer 420 can use any suitable processes such as, for

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example, a spin-coating process, CVD or high density plasma (HDP) deposition. In some embodiments, the forming of the third insulating layer 420 further includes a planarization process such as chemical-mechanical planarization (CMP). In some embodiments, the third insulating layer 420 can cover each step of the staircase structure 300.

[0058] Referring to Fig. 5A, a substrate opening 522 is formed in a staircase structure 500 by etching through the entire film stack of the staircase structure 400, exposing the surface of the substrate 101. (Although Figs. 5A and 5B illustrate one substrate opening 522, it is noted that, the location, shape, total number, and arrangement of the substrate opening 522, relative to the staircase structure 400, is only used for illustration purpose in the present disclosure, which does not limit the scope of the present disclosure.)

[0059] In some embodiments, through the substrate opening 522, the sacrificial layer 106 of each SC layer 102 in the staircase structure 400 is removed and replaced by a gate stack 525. The staircase structure 500 includes a plurality of replacement SC layers 526, wherein the replacement SC layer 526 includes the first insulating layer 104 and the gate stack 525. The first insulating layer 104 and the gate stack 525 are alternately arranged in the staircase structure 500.

[0060] In some embodiments, removing the sacrificial layer 106 includes wet etching or isotropic dry etching that is selective to the first insulating layer 104. For example, the etching rate of the first insulating layer 104 is slower than the etching rate of the sacrificial layer 106. In some embodiments, removing the sacrificial layer 106 is also selective to the second insulating layer 208. In some embodiments, the second insulating layer 208 is optional, and removing the sacrificial layer 106 is selective to the etch-stop layer 310.

[0061] Fig. 5B illustrates the details of a region 527 in Fig. 5A, in accordance with some embodiments of the present disclosure. The gate stack 525 can include a high-k dielectric layer 525H and a gate conductive layer 525M. The gate conductive layer 525M is surrounded by the high-k dielectric layer 525H, with one side next to the substrate opening 522.

[0062] In some embodiments, the high-k dielectric layer 525H can include hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, or lanthanum oxide films, and/or any combination thereof. The high-k dielectric layer 525H can be disposed by any suitable methods such as CVD, PVD, PECVD, LPCVD, MOCVD, ALD, and/or combinations thereof.

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- [0063]** In some embodiments, the gate conductive layer 525M can be made from a metal, such as tungsten, cobalt, nickel, copper, or aluminum, and/or combinations thereof. The metal can be formed by any suitable deposition methods, for example, sputtering, thermal evaporation, e-beam evaporation, ALD, PVD, and/or combinations thereof.
- [0064]** In some embodiments, the gate conductive layer 525M can also be poly-crystalline semiconductors, such as poly-crystalline silicon, poly-crystalline germanium, poly-crystalline germanium-silicon and any other suitable material, and/or combinations thereof. In some embodiments, the poly-crystalline material can be incorporated with any suitable types of dopant, such as boron, phosphorous, or arsenic, and in the form of elements or a compound. In some embodiments, the gate conductive layer 525M can also be amorphous semiconductors.
- [0065]** In some embodiments, the gate conductive layer 525M can be made from a metal silicide, including WSi_x , $CoSi_x$, $NiSi_x$, or $AlSi_x$, etc. The forming of the metal silicide material can include forming a metal layer and a poly-crystalline semiconductor using similar techniques described above. The forming of metal silicide can further include applying a thermal annealing process on the deposited metal layer and the poly-crystalline semiconductor layer, followed by removal of unreacted metal.
- [0066]** In some embodiments, the gate stack 525 includes an interface material between the high-k dielectric layer 525H and the gate conductive layer 525M. The interface material can include silicon oxide or silicon oxynitride, etc.
- [0067]** The portion of the gate conductive layer 525M located on the sidewalls of the substrate opening 522 (not illustrated in Fig. 5A or 5B for simplicity), can be removed and replaced by a fifth insulating layer 530. Removal of sidewall portions of gate conductive layer 525M can be achieved by wet-etching or dry-etching. In some embodiments, the fifth insulating layer 530 can be made of the same material as the first insulating layer 104 or the etch-stop layer 310, and formed by similar techniques. In some embodiments, a portion of the fifth insulating layer 530 can be removed from the top surface of substrate 101 and the substrate surface can be exposed for electrical contacts in the subsequent processes. Removing the fifth insulating layer 530 from the substrate surface can be achieved by, for example, anisotropic dry-etching.

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[0068] Referring now to Fig. 6, a staircase structure 600 includes vertical interconnect access (VIA) openings 640 for each replacement SC layer 526. In some embodiments, photoresist or polymer material can be used as a mask layer (not shown in the figure). A selective etching process can be used such that the etching rate of the third insulating layer 420 is higher than the etching rate of the etch-stop layer 310. During the one or more etching processes that form the VIA openings 640, the etch-stop layer 310 protects the underlying structure until all the VIA openings 640 are formed throughout the staircase structure 600. For example, a VIA opening 640L for a lower replacement SC layer 526L requires longer etch time than a VIA opening 640U for an upper replacement SC layer 526U. An additional thickness H of the third insulating layer 420 needs to be removed. The etch-stop layer 310 can protect underlying materials of the replacement SC layers 526 on upper levels, before the VIA openings 640 are formed for the replacement SC layers 526 on lower levels. For example, during the removal process of the extra thickness H of third insulating layer 420, the etch-stop layer 310 on top of the upper replacement SC layer 526U is not etched through, with a remaining etch stop layer 310R. The remaining etch-stop layer 310R provides protection for the replacement SC layers 526U, where the VIA openings 640U are already formed. The staircase structure 600 is formed after the portion of the third insulating layer 420 inside all the VIA openings 640 are removed for each replacement SC layer 526. The VIA openings 640 extend through the third insulating layer 420 and expose the underlying etch-stop layer 310. In some embodiments, the etch-stop layer 310 can be partially etched in some VIA openings 640, as shown in Fig. 6. In some embodiments, the thickness of the etch-stop layer 310 remains substantially the same during the one or more etching processes that form the VIA openings 640, because etch-stop layer 310 can be inert to the etchant used in the etching processes. In some embodiments, the selective etching includes anisotropic dry etching using chemical etchant such as, for example, CF₄, CHF₃, C₂F₆, or C₃F₆, and/or other suitable etchants.

[0069] In some embodiments, prior to forming VIA openings 640, a second conductive material can be disposed inside the substrate opening 522 of the staircase structure 500 (see FIG. 5) to form a substrate conductive structure 643 (see FIG. 6). Accordingly, an electrical connection is provided to the substrate 101 from the surface of the staircase structure 600. In some embodiments, the substrate conductive structure 643 can be formed with any suitable

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conductive material that can be the same as or can be different from the gate conductive layer 525M, and can be disposed using similar techniques. Additional planarization process can be included to form a top surface coplanar with the top surface of the third insulating layer 420.

[0070] Referring to Fig. 7, portions of the etch-stop layer 310 inside VIA openings 740 are removed by reverse selective etching. During reverse selective etching, the etch-stop layer 310 can be etched faster than the second insulating layer 208. In some embodiments, the reverse selective etching process includes anisotropic or isotropic dry etching using chemistry, for example, O₂, N₂, CF₄, NF₃, Cl₂, HBr, BCl₃, and/or combinations thereof. In some embodiments, the reverse selective etching process includes wet chemical etching, for example, phosphorus acid. A staircase structure 700 is formed after the portion of etch-stop layer 310 inside the VIA openings 740 is removed for each replacement SC layer 526.

[0071] Referring to Fig. 8A and 8B, a portion of the second insulating layer 208 and a portion of the high-k dielectric layer 525H in gate stack 525 are removed inside the VIA openings 840, forming VIA openings 840 that extend through the third insulating layer 420, the etch-stop layer 310, the second insulating layer 208, and the high-k dielectric layer 525H and exposing the gate conductive layer 525M. In some embodiments, the etching process for etching the second insulating layer 208 and the high-k dielectric layer 525H can be similar to that used for etching the third insulating layer 420 or the etch-stop layer 310. A staircase structure 800 includes a portion of gate conductive layer 525M, which is exposed inside the VIA openings 840 for each replacement SC layer 526, enabling gate contacts for every 3D memory cell.

[0072] In some embodiments, the second insulating layer 208 is optional and the etching of the etch stop layer 310 exposes the high-k dielectric layer 525H inside the VIA openings 740/840. The high-k dielectric layer 525H can be removed in the subsequent etching process to further expose the gate conductive layer 525M inside the VIA openings 740/840. The VIA openings 840 extend through the third insulating layer 420, etch-stop layer 310 and the high-k dielectric layer 525H, exposing the gate conductive layer 525M.

[0073] Referring to Fig. 9A and 9B, a staircase structure 900 includes disposing a third conductive material to form VIA conductive structures 945 in the VIA openings 840. The VIA conductive structures 945 can be formed by disposing a third conductive material in the formed openings 840 and directly on the exposed portions of gate conductive layer 525M. In

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some embodiments, the VIA conductive structures 945 are directly disposed on the exposed gate conductive layer 525M. In some embodiments, the VIA conductive structures 945 can be made from a similar material as the gate conductive layer 525M. In some embodiments, the VIA conductive structures 945 can be disposed using a similar technique as the gate conductive layer 525M. In some embodiments, the VIA conductive structures 945 can be coplanar with the third insulating layer 420 using a planarization process such as, for example, a CMP process. In the staircase structure 900, the VIA conductive structures 945 can extend through the third insulating layer 420, the etch-stop layer 310, the second insulating layer 208 and the gate dielectric layer 525H, directly contacting and electrically connecting to the gate conductive layer 525M for each corresponding replacement SC layer 526. As discussed above, the second insulating layer 208 can be optional and in such scenarios the VIA conductive structures 945 can extend through the third insulating layer 420, the etch-stop layer 310 and the gate dielectric layer 525H, directly contacting and connected to the gate conductive layer 525M for each corresponding replacement SC layer 526. Therefore, the electrical conductive path for gate stack 525 of each memory cell can be wired up to the surface of the wafer, enabling various configurations of word lines for the 3D memory in the back-of-line process.

[0074] Fig. 10 illustrates an exemplary method 1000 for forming the word line contacts for a three-dimensional memory array, according to some embodiments. The processing steps of the method 1000 can be used to form memory device structures illustrated in Figs. 1-9. The processing steps shown in method 1000 are not exhaustive and other processing steps can be performed as well before, after, or between any of the illustrated process steps. In some embodiments, some processing steps of exemplary method 1000 can be omitted or include other processing steps that are not described here for simplicity. In some embodiments, processing steps of method 1000 can be performed in a different order and/or vary.

[0075] At process step 1010, an alternating layer stack is disposed over a substrate, followed by a repetitive etch-trim process to form a staircase structure. An example of the substrate can be the substrate 101 described in Fig. 1. A layer stack within the alternating layer stack can include a dielectric layer pair with a first insulating layer over a sacrificial layer. The first insulating layer can be the first insulating layer 104 in Fig. 1 and the sacrificial layer can be

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the sacrificial layer 106 in Fig. 1, and the dielectric layer pair can be formed using similar techniques as the first insulating layer 104 and the sacrificial layer 106.

[0076] One cycle of the repetitive etch-trim process includes an etching process that etches a height of a staircase step and a trimming process that determines a width of a staircase step. The etch-trim process is repeated for a number of cycles, corresponding to the number of steps or the number of dielectric layer pairs on the staircase structure. A mask stack can be used for patterning and can be removed after the etch-trim process.

[0077] At process step 1020, a second insulating layer is disposed on the staircase structure with alternating film stacks. The second insulating layer can be the second insulating layer 208 in Fig. 2 and can be formed using a similar technique.

[0078] At process step 1030, an etch-stop layer is disposed on the top surface of the second insulating layer on the staircase structure. The etch-stop layer can be the etch stop layer 310 in Fig. 3, and can be formed using a similar technique.

[0079] At process step 1040, a third insulating layer is disposed on the top surface of the etch-stop layer over the staircase structure, followed by an optional planarization process, to form a surface coplanar with the uppermost portion of the etch-stop layer. The third insulating layer can be the third insulating layer 420 in Fig. 4, and can be formed using a similar technique.

[0080] At process step 1050, an opening to the substrate is formed by etching through the entire film stack. Through the opening, the sacrificial layer of each dielectric layer pair in the staircase structure is removed and replaced by a gate stack. A similar structure is shown in Fig. 5A and 5B. The gate stack can be the gate stack 525 in Fig. 5A and 5B. The opening to the substrate can be the substrate opening 522 in Fig. 5A. Removing the sacrificial layer includes wet etching or isotropic dry etching that is selective to the surrounding first and second insulating layer. Disposing the gate stack includes first disposing a high-k dielectric layer and then a gate conductive layer. The high-k dielectric layer can be the high-k dielectric layer 525H in Fig. 5B, and can be formed using a similar technique. The gate conductive layer can be the gate conductive layer 525M, and can also be formed using a similar technique.

[0081] Process step 1050 also includes removing the gate conductive layer (or the conductive portion) from the sidewalls of the substrate opening and forming an isolation barrier layer.

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Removing the gate conductive layer from the sidewall can be achieved by wet-etching or dry-etching. The sidewall isolation layer can be fifth insulating layer 530 in Fig. 5A and 5B, and can be formed using a similar technique. The sidewall isolation material deposited on the substrate surface at the bottom of the opening can be removed by anisotropic dry-etching.

[0082] At process step 1060, a second conductive material can be disposed over the staircase structure, forming a substrate conductive structure inside the substrate opening. The substrate conductive structure can be the substrate conductive structure 643 in Fig. 6. A planarization process, for example, chemical mechanical polishing, can be used to form coplanar top surfaces between the substrate conductive structure and the third insulating layer.

[0083] At process step 1060, contact VIA openings are also formed for each staircase level with selective etching. The contact VIA openings can be the same VIA openings 640 in Fig. 6. The etching rate of the third insulating layer can be higher than the etching rate of the etch-stop layer. Therefore, deep openings can be made for the bottom staircase level, while the etch-stop layer is not punched through on the uppermost staircase level.

[0084] At process step 1070, the etch-stop materials inside the VIA openings are removed by reverse selective etching. During reverse selective etching, the etch-stop layer can be etched faster than the second insulating layer. At this step, the VIA openings can be the VIA openings 740 in Fig. 7.

[0085] At process step 1080, the second insulating layer and the high-k dielectric layer of the gate stack is removed inside the VIA openings, by using a similar etching process as that for the third insulating layer or the etch-stop layer. The conductive material of the gate stack is exposed inside the VIA openings, enabling electrical connections to the gate of every 3D memory cell. At this step, the VIA openings can be the VIA openings 840 in Fig. 8A and 8B.

[0086] At process step 1090, VIA conductive structures are formed by disposing and filling a third conductive material in all the VIA openings in the structure. The VIA conductive structure can be the VIA conductive structures 945 in Fig. 9A and 9B. The third conductive material can be planarized subsequently to form a coplanar surface with the top surface of the third insulating layer. The planarization process includes chemical mechanical polishing (CMP). Residual conductive materials outside the VIA openings can be removed by touch-up dry etching or wet etching. As a result, the conductive material in the VIA openings is connected with the conductive material of the gate stack for each level of the staircase

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structure. Therefore, the embedded gates of the vertically stacked 3D memory cells can be electrically connected from a planar surface on the top of the structure in the subsequent back-of-line processes, enabling various configurations of word lines for the 3D memory array.

[0087] Process steps 1010-1050 illustrate the formation of the staircase structure 500 in Fig. 5, in accordance with some embodiments of the present disclosure, using a replacement gate technique. In this example, the sacrificial layer 106 is formed first on the staircase structure 100 in Figs. 1 at process steps 1010. The sacrificial layer 106 can be replaced by the gate stack 525 at process step 1050 to form staircase structure 500. Detailed structure and method of 3D memory with replacement gate is described in co-pending U.S. patent application, titled “Method for Forming Gate Structure of Three-Dimensional Memory Device,” (Application No. 16/047,158 and filed on July 27, 2018), which is incorporated herein by reference in its entirety.

[0088] In some embodiments, the staircase structure 500 can also be formed with a so called “gate-first” approach, where a gate conductive layer can be disposed in Fig. 1 and at process steps 1010, in place of the sacrificial layer 106. The gate conductive layer can be a similar material as the gate conductive layer 525M in Fig. 5B and can be formed using similar techniques. The etch-trim process to form the staircase structure 100 can be modified accordingly so that the gate conductive layer 525M can be etched instead of the sacrificial layer 106. As such, the sacrificial layer 106 in Figs. 2-4 can also be replaced by the gate conductive layer 525M. At process step 1050, the step of removing the sacrificial layer 106 can be skipped in this embodiment. The substrate opening 522, the VIA openings 640/740/840, and the conductive structures 643/945 can be formed similarly as the ones in Figs. 5-9 and using similar methods in process steps 1050-1090.

[0089] In some embodiments, a semiconductor structure includes a staircase structure having a plurality of steps, and each step includes a conductive layer disposed over a dielectric layer. The semiconductor structure further includes a barrier layer disposed over a portion of the conductive layer of the each step. The semiconductor structure also includes an etch-stop layer disposed on the barrier layer and an insulating layer disposed on the etch-stop layer. The semiconductor structure also includes a plurality of conductive structures formed in the

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insulating layer and extending through the etch-stop layer and the barrier layer. Each conductive structure directly contacts the conductive layer of the each step.

[0090] In some embodiments, a semiconductor structure includes a staircase structure having a plurality of steps, and each step includes a conductive layer disposed over a dielectric layer. The semiconductor structure further includes an etch-stop layer disposed over a portion of the conductive layer of the each step and an insulating layer disposed on the etch-stop layer. The semiconductor structure further includes a plurality of conductive structures formed in the insulating layer and extending through the etch-stop layer. Each of the conductive structure directly contacts the corresponding conductive layer of the each step.

[0091] In some embodiments, a method for forming a semiconductor structure includes forming a plurality of steps of a staircase structure. Forming each step of the plurality of steps includes disposing a sacrificial layer over a dielectric layer and disposing an etch-stop layer on each step of the plurality of steps. The method further includes disposing an insulating layer on the etch-stop layer and replacing the sacrificial layer with a conductive layer for each step of the staircase structure. The method also includes forming a plurality of openings in the insulating layer and exposing portions of the etch-stop layer. The method also includes etching the exposed portions of the etch-stop layer in the plurality of openings and exposing the conductive layer of each step. The method also includes forming a plurality of conductive structures and each conductive structure is respectively formed in each opening of the plurality of openings.

[0092] The foregoing description of the specific embodiments will so fully reveal the general nature of the present disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt, for various applications, such specific embodiments, without undue experimentation, and without departing from the general concept of the present disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the disclosure and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the disclosure and guidance.

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[0093] Embodiments of the present disclosure have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

[0094] The Summary and Abstract sections can set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s), and thus, are not intended to limit the present disclosure and the appended claims in any way.

[0095] The breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

WHAT IS CLAIMED IS:

1. A method for forming a semiconductor structure, comprising:
 - forming a staircase structure having a plurality of steps, wherein the forming of each step of the plurality of steps comprises disposing a sacrificial layer over a dielectric layer;
 - disposing an etch-stop layer on each step of the plurality of steps;
 - disposing an insulating layer on the etch-stop layer;
 - replacing the sacrificial layer of each step with a gate stack, the gate stack comprising a conductive layer and a first high-k dielectric layer;
 - forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer;
 - etching the exposed portions of the etch-stop layer in the plurality of openings and exposing at least a portion of the conductive layer of each step; and
 - forming a plurality of conductive structures in each of the plurality of openings.
2. The method of claim 1, wherein the forming the plurality of openings comprises performing an etching process on the insulating layer, wherein an etching rate of the insulating layer is higher than an etching rate of the etch-stop layer.
3. The method of claim 2, wherein the etching process comprises anisotropic dry etching.
4. The method of claim 1, wherein etching the exposed portions of the etch-stop layer comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer of each step.
5. The method of claim 4, wherein etching the exposed portions of the etch-stop layer further comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the first high-k dielectric layer.
6. The method of claim 1, wherein disposing the etch-stop layer comprises disposing one or more of silicon nitride, silicon oxynitride, and silicon oxide.

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7. The method of claim 1, wherein disposing the etch-stop layer comprises disposing a second high-k dielectric layer.
8. The method of claim 7, wherein disposing the second high-k dielectric layer comprises disposing hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, and/or any combination thereof.
9. The method of claim 1, wherein disposing the etch-stop layer comprises disposing the etch-stop layer with a thickness in a range between 10 nm to 100 nm.
10. The method of claim 1, wherein disposing the etch-stop layer comprises performing chemical vapor deposition (CVD), physical vapor deposition (PVD), sputtering, atomic layer deposition (ALD), spin-coating, or any combination thereof.
11. The method of claim 1, further comprising:
after disposing the insulating layer on the etch-stop layer, planarizing the insulating layer and the staircase structure by using chemical-mechanical-polishing (CMP).
12. The method of claim 1, wherein forming the plurality of conductive structures comprises disposing conductive materials inside the plurality of openings, the conductive materials directly on the exposed conductive layer of the each step.
13. The method of claim 6, wherein forming the plurality of conductive structures further comprises planarizing the conductive materials and the insulating layer.
14. The method of claim 1, wherein forming the staircase structure further comprises performing a repetitive etch-trim process on the sacrificial layers and the dielectric layers.
15. The method of claim 1, wherein replacing the sacrificial layer of each step with the gate stack comprises:

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forming a substrate opening through the staircase structure;
removing the sacrificial layer of each step through the substrate; and
disposing the first high-k dielectric layer and the conductive layer in place of the sacrificial layer.

16. The method of claim 15, wherein disposing the first high-k dielectric layer comprises disposing hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide and/or any combination thereof.
17. The method of claim 15, wherein disposing the conductive layer comprises disposing tungsten, cobalt, nickel, copper, aluminum, and/or any combination thereof.
18. The method of claim 15, wherein disposing the conductive layer comprises disposing polycrystalline silicon, polycrystalline germanium, or polycrystalline germanium-silicon.
19. The method of claim 1, further comprising:
prior to disposing the etch-stop layer, disposing a barrier layer on each step of the plurality of steps, wherein the barrier layer protects underlying structures during the etching of the exposed portions of the etch-stop layer.
20. The method of claim 19, wherein disposing the barrier layer comprises disposing one or more of silicon oxide, silicon oxynitride, silicon nitride, TEOS, aluminum oxide, and silicon oxide incorporated with F, C, N, or H.

ABSTRACT

Embodiments of semiconductor structures including word line contact structures for three-dimensional memory devices and fabrication methods for forming word line contact structures are disclosed. The semiconductor structures include a staircase structure having a plurality of steps, and each step includes a conductive layer disposed over a dielectric layer. The semiconductor structures further include a barrier layer disposed over a portion of the conductive layer of each step. The semiconductor structures also include an etch-stop layer disposed on the barrier layer and an insulating layer disposed on the etch-stop layer. The semiconductor structures also include a plurality of conductive structures formed in the insulating layer and each conductive structure is formed on the conductive layer of each step.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Application No.: To Be Assigned

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Atty. Docket: 4123.0480003

Title: **WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY
DEVICES AND FABRICATION METHODS THEREOF**

Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

Listed on accompanying IDS Forms PTO/SB/08a and PTO/SB/08b are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Applicant has listed publication dates on the attached IDS Forms based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicant has checked the appropriate boxes below.

- ☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement: (i) was first cited in any communication from a patent office in a counterpart¹ foreign or international application or from the Office; and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of this information disclosure statement; OR (ii) is a communication that was issued by a patent office in a counterpart foreign or international application or by the Office, and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of the information disclosure statement.
- ☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.
- ☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office

¹ The term counterpart foreign patent application means that a claim for priority has been made in either the U.S. application or a foreign application based on the other, or that the disclosures of the U.S. and foreign patent applications are substantively identical (e.g., an application filed in the European Patent Office claiming the same U.K. priority as claimed in the U.S. application).

Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

- ☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
- ☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).
- ☐ c. The required fee is provided through online credit card payment authorization in the amount of \$240.00 in payment of the fee under 37 C.F.R. § 1.17(p).
- ☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but on or before payment of the Issue Fee. The required fee is provided through online credit card payment authorization in the amount of \$240.00 in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

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- ☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
- ☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).
- ☒ 5. The patent family for one or more foreign language documents submitted herewith includes a United States patent, and other patent, in the English language. Copies of both the particular foreign patent(s) or published foreign patent applications cited in the foreign patent office communication, and that are not already of record in this application, are enclosed. Copies of the related United States or other English language patent or published application from the family list, if not already of record, are listed on the accompanying SB/08A form. For the purposes of a statement under 37 CFR 1.97(e)(1), the United States or other English language patent or published application are to be construed as being cited by the foreign patent office. MPEP 609.04(b)(V).

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- ☐ 6. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. MPEP 609.04(a)(III).
- ☒ 7. A concise explanation of the relevance of the non-English language document(s) appears below in accordance with 37 C.F.R. § 1.98(a)(3).
- Document **US12** (2017/0236836 A1) is submitted herewith as the English-language counterpart of document **FP1** (CN 104157654 A).
- Document **US13** (8,828,884 B2) is submitted herewith as the English-language counterpart of document **FP2** (CN 104396004 A).
- ☒ 8. In accordance with 37 C.F.R. § 1.98(a)(2)(ii), no copies of the U.S. patents and patent application publications cited as documents **US1-US16** on the attached IDS Forms are submitted.
- ☒ 9. Copies of the documents **FP1-FP2** and **NPL1** were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No. 16/126,947, filed September 10, 2018, (now pending), which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).
- ☒ 10. It is expected that the examiner will review the prosecution and cited art in the parent Application No. 16/126,947, filed September 10, 2018, (now pending), in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited

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in the earlier prosecution history has been reviewed in connection with the present application.

☐ 11. Applicants submit herewith Office Actions from the co-pending U.S. Patent Application

No. _____, filed _____, as documents _____ to _____.

The identification of these Office Actions is not to be construed as a waiver of secrecy as to those applications now or upon issuance of the present application as a patent. The Examiner is respectfully requested to consider the cited applications and the art cited therein during examination.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Application Number	To Be Assigned
		Filing Date	Herewith
		First Named Inventor	Jifeng ZHU
		Art Unit	To Be Assigned
		Examiner Name	To Be Assigned
Sheet 1 of 1	Attorney Docket Number	4123.0480003	

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	US1	US- 2010/0013049 A1	01-21-2010	Tanaka et al.	
	US2	US- 2010/0207195 A1	08-19-2010	Fukuzumi et al.	
	US3	US- 2011/0031546 A1	02-10-2011	Uenaka et al.	
	US4	US- 2011/0169071 A1	07-14-2011	Uenaka et al.	
	US5	US- 2013/0313627 A1	11-28-2013	Lee et al.	
	US6	US- 2013/0337646 A1	12-19-2013	Cernea et al.	
	US7	US- 2014/0106569 A1	04-17-2014	Oh et al.	
	US8	US- 2014/0284675 A1	09-25-2014	Watanabe	
	US9	US- 2016/0118398 A1	04-28-2016	Yon et al.	
	US10	US- 2016/0020169 A1	01-21-2016	Matsuda	
	US11	US- 2016/0358855 A1	12-08-2016	Oh	
	US12	US- 2017/0236836 A1	08-17-2017	Huo et al.	
	US13	US- 7,539,056 B2	05-26-2009	Katsumata et al.	
	US14	US- 8,828,884 B2	09-09-2014	Lee et al.	
	US15	US- 9,419,013 B1	08-16-2016	Lee et al.	
	US16	US- 9,515,086 B2	12-06-2016	Yon et al.	
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
	FP1	CN 104157654 A	11-19-2014	INST OF MICROELECTRONICS		
	FP2	CN 104396004 A	03-04-2015	SANDISK TECHNOLOGIES INC.		

Examiner Signature	Date Considered
--------------------	-----------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Complete if Known	
		Application Number	To Be Assigned
		Filing Date	Herewith
		First Named Inventor	Jifeng ZHU
		Art Unit	To Be Assigned
		Examiner Name	To Be Assigned
Sheet	1	of	1
		Attorney Docket Number	4123.0480003

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	NPL1	International Search Report and Written Opinion of the International Searching Authority directed to related International Patent Application No. PCT/CN2018/101308, mailed November 21, 2018; 6 pages.	

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO:**
Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA/82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	To Be Assigned
Filing Date	To Be Assigned
First Named Inventor	Jifeng ZHU
Title	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF
Art Unit	To Be Assigned
Examiner Name	To Be Assigned
Attorney Docket Number	

SIGNATURE of Applicant or Patent Practitioner

Signature	/Donald J. Featherstone/	Date (Optional)	
Name	Donald J. Featherstone	Registration Number	33,876
Title (if Applicant is a juristic entity)	Attorney for Applicant		
Applicant Name (if Applicant is a juristic entity)		Yangtze Memory Technologies Co., Ltd.	

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.



*Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..

Document Description: Power of Attorney

PTO/AIA/82B (07-13)

Approved for use through 01/31/2018, OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY BY APPLICANTI hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below:

Application Number

Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)



I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

26111

OR



I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:



The address associated with the above-mentioned Customer Number.

OR



The address associated with Customer Number:

26111

OR

Firm or
Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Yangtze Memory Technologies Co., Ltd.



Inventor or Joint Inventor (title not required below)



Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)



Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)



Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)



1

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

Name

Simon Shi-Ning Yang

Title

CEO

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

Total of

forms are submitted

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

COMBINED DECLARATION AND ASSIGNMENT

DECLARATION

As the below named inventors, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ☒ United States application or PCT international application number 16/126,947
filed on September 10, 2018

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar (\$1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is 18 Gaoxin 4th Road, East Lake High-Tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF** for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 26111** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: Jifeng ZHU Date: 2018.10.22

Signature of Inventor: Jifeng ZHU

LEGAL NAME OF INVENTOR

Inventor: Zhenyu LU Date: 2018.10.23

Signature of Inventor: Zhenyu Lu

LEGAL NAME OF INVENTOR

Inventor: Jun CHEN Date: 2018.10.23

Signature of Inventor: Jun CHEN

LEGAL NAME OF INVENTOR

Inventor: Si Ping HU Date: 2018.11.05

Signature of Inventor: Si Ping HU

LEGAL NAME OF INVENTOR

Inventor: Xiaowang DAI Date: 2018.11.2

Signature of Inventor: Xiaowang DAI

LEGAL NAME OF INVENTOR

Inventor: Lan YAO Date: 2018. 10. 22

Signature of Inventor: Lan Yao

LEGAL NAME OF INVENTOR

Inventor: Li Hong XIAO Date: 2018. 10. 22.

Signature of Inventor: Lihong Xiao

LEGAL NAME OF INVENTOR

Inventor: A Man ZHENG Date: 2018. 10. 22

Signature of Inventor: A Man ZHENG

LEGAL NAME OF INVENTOR

Inventor: Kun BAO Date: 2018. 10. 22

Signature of Inventor: Kun BAO

LEGAL NAME OF INVENTOR

Inventor: Haohao YANG Date: 2018/10/22

Signature of Inventor: Haohao YANG

10202996_1.docx

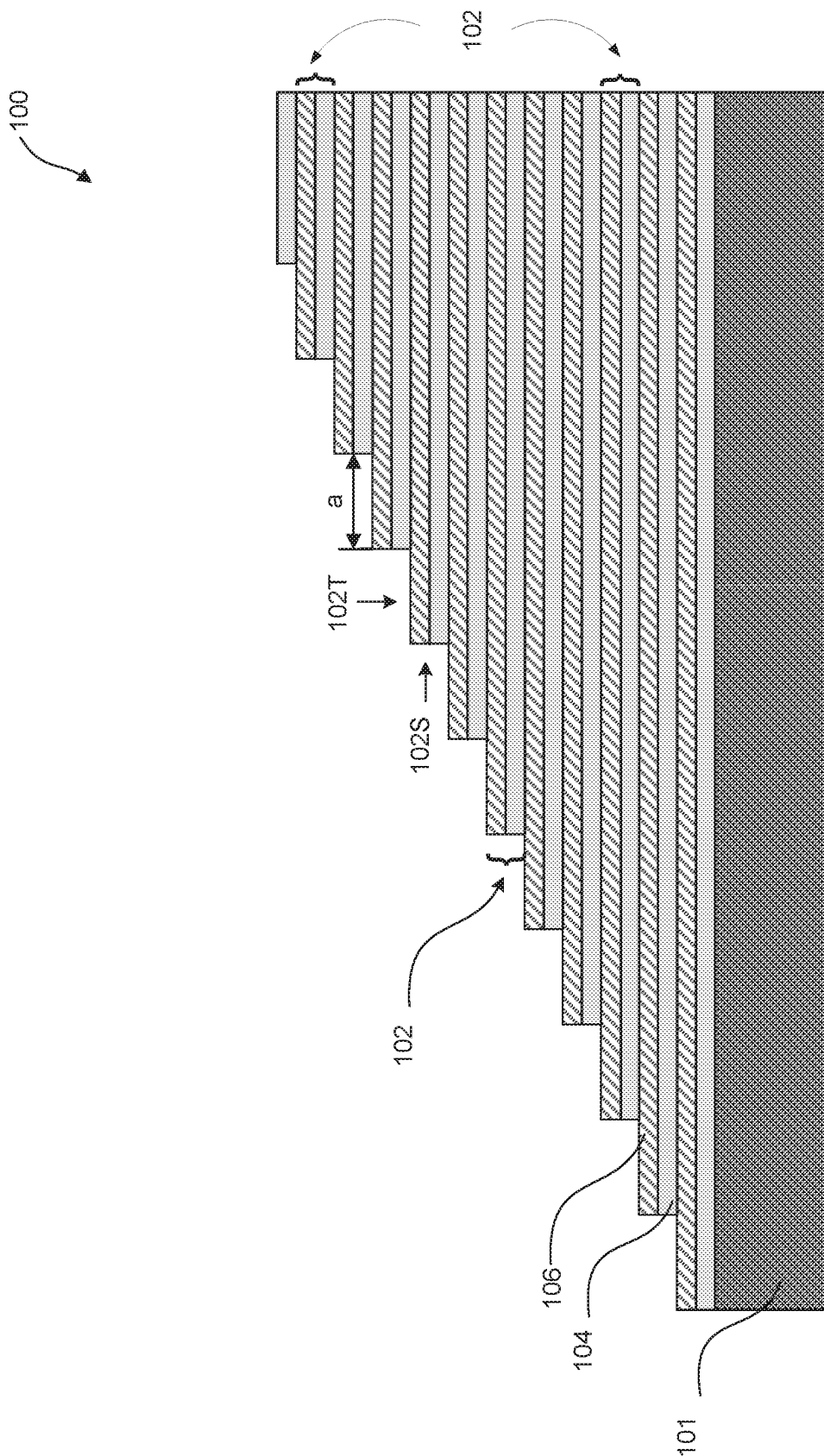


FIG. 1

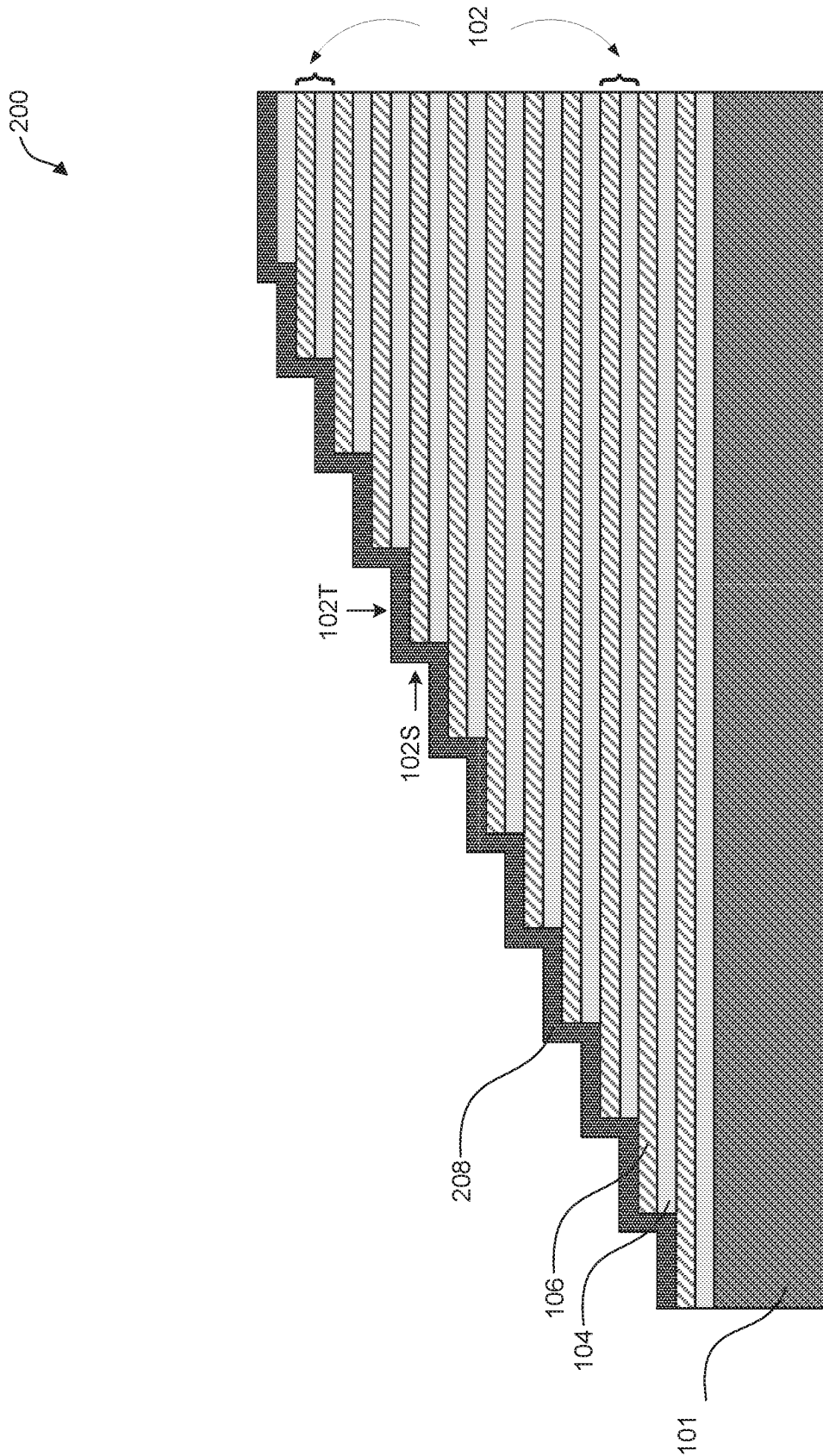


FIG. 2

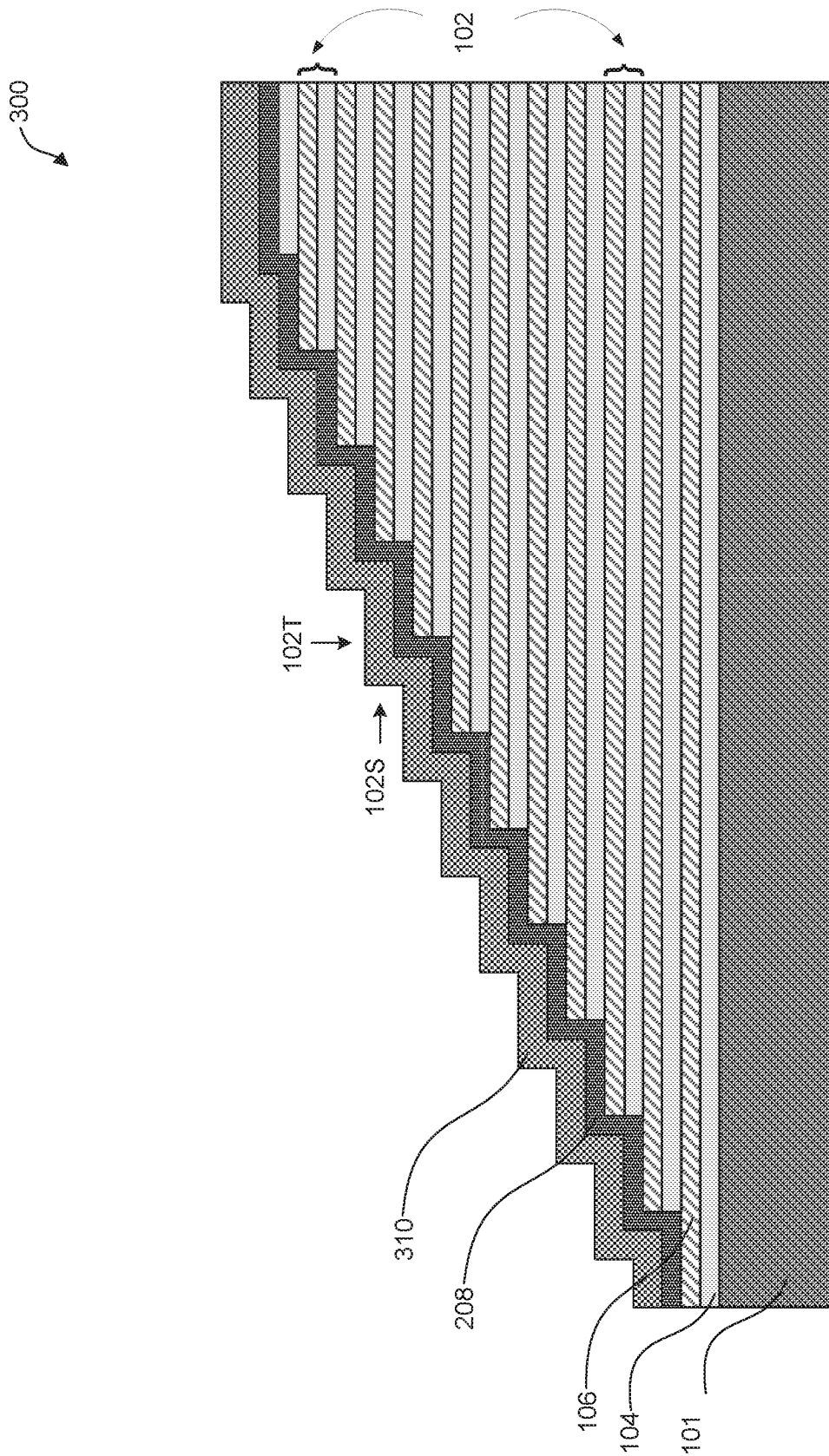


FIG. 3

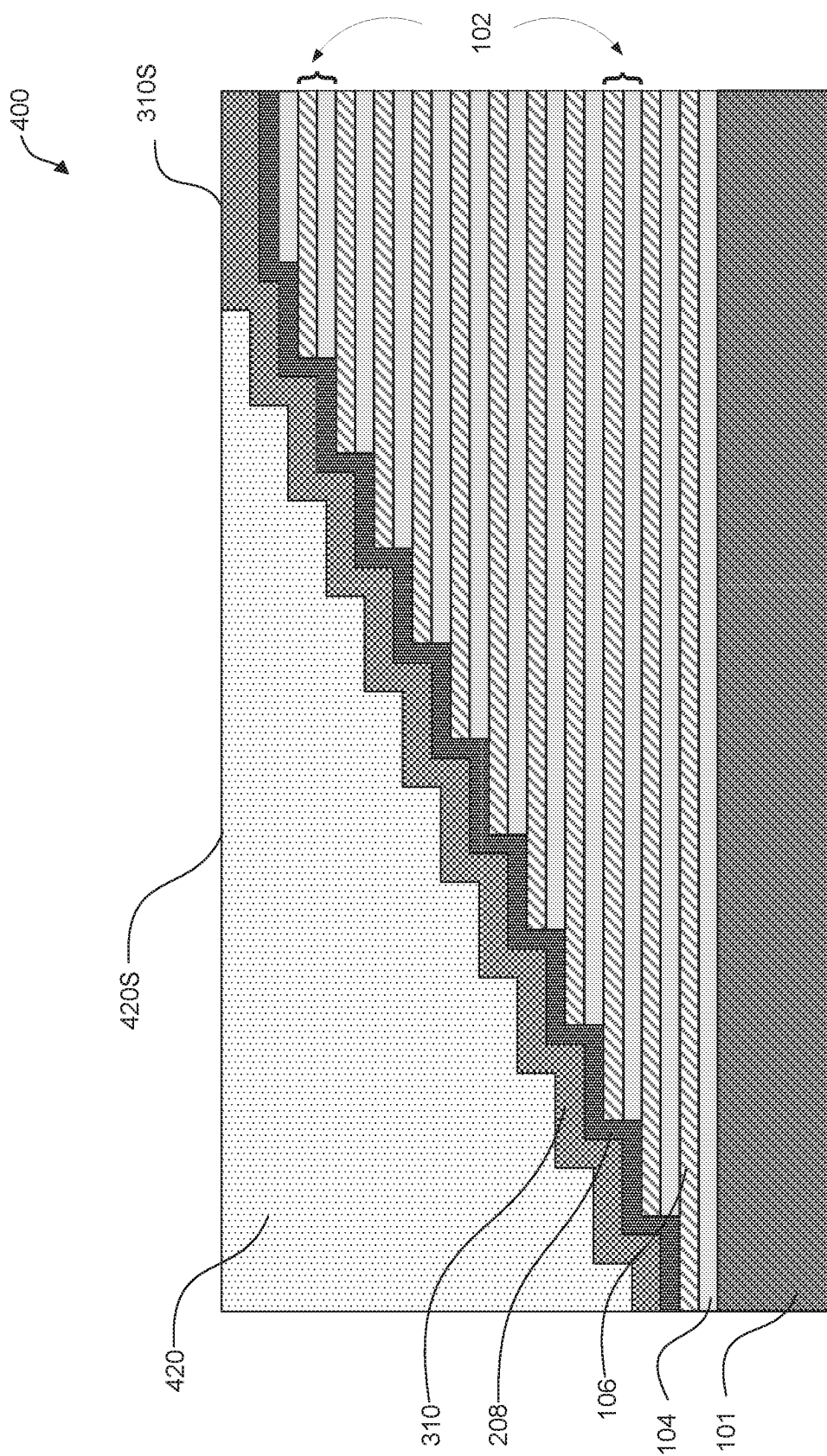


FIG. 4

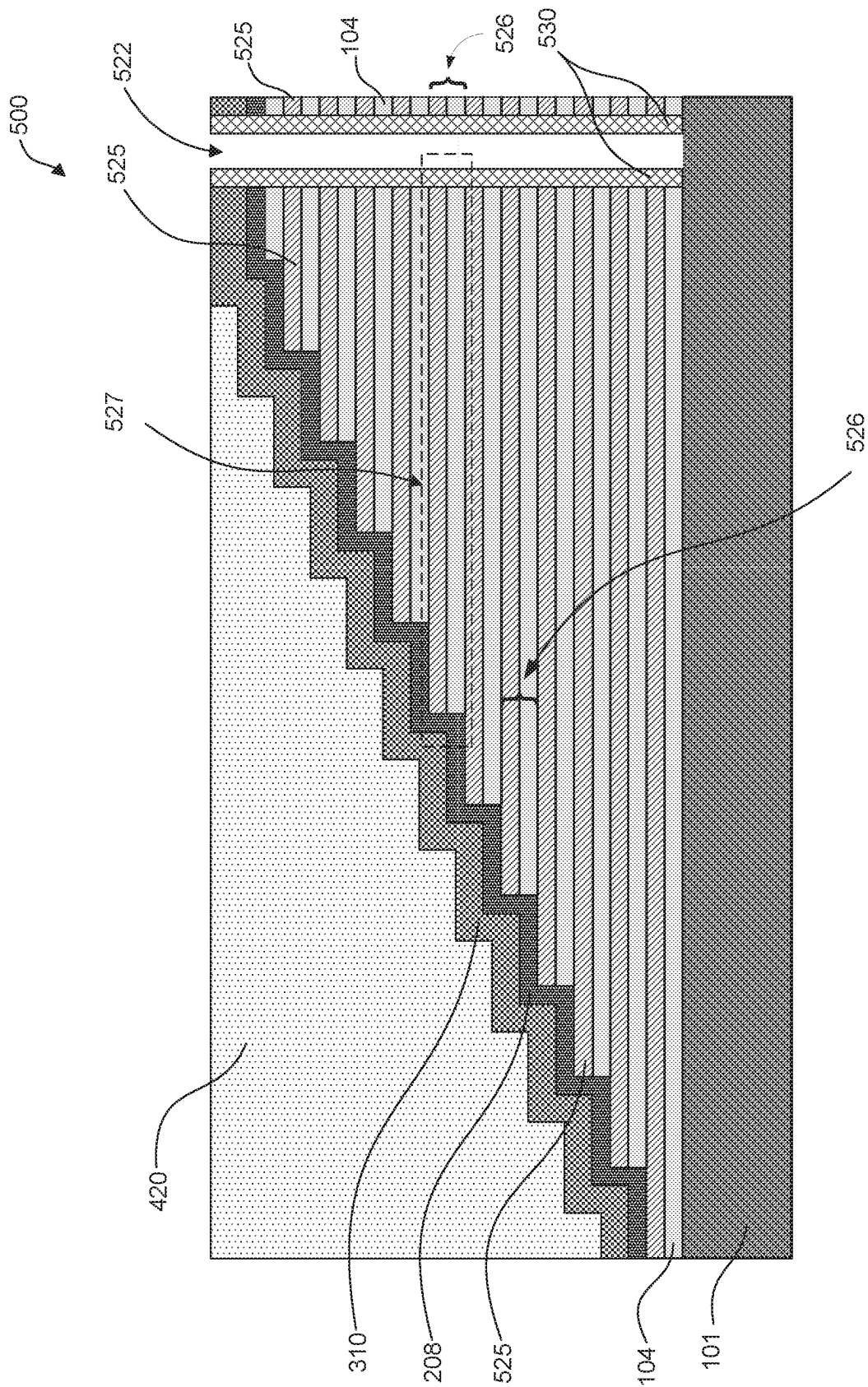


FIG. 5A

527

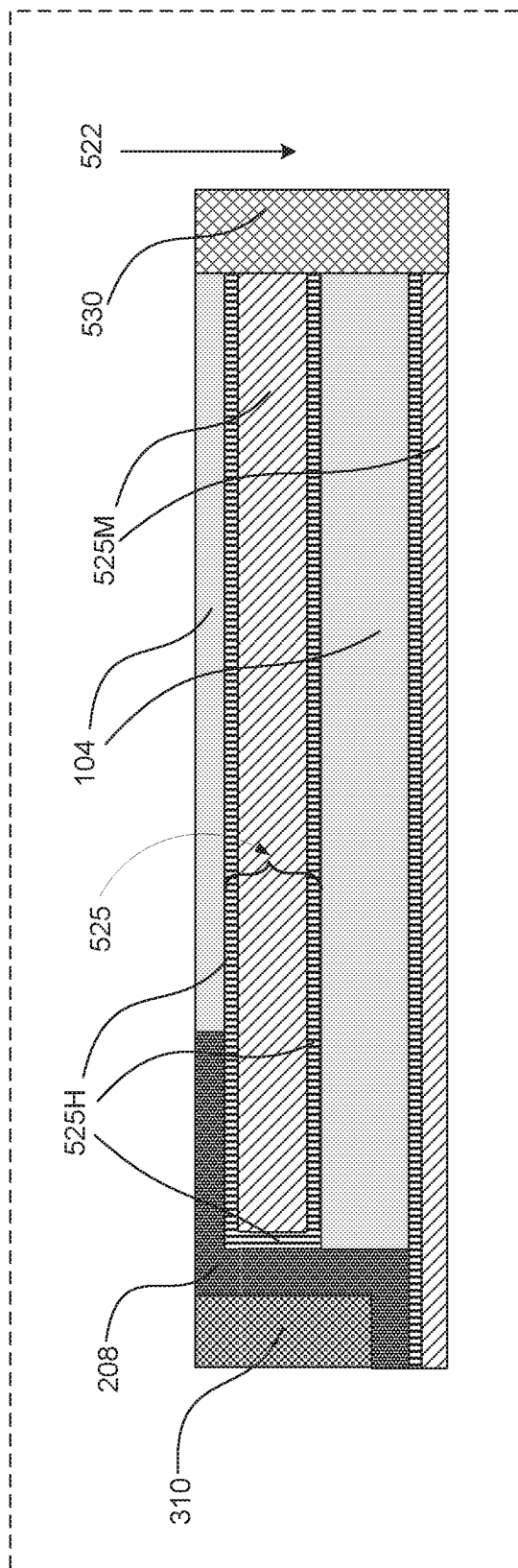


FIG. 5B

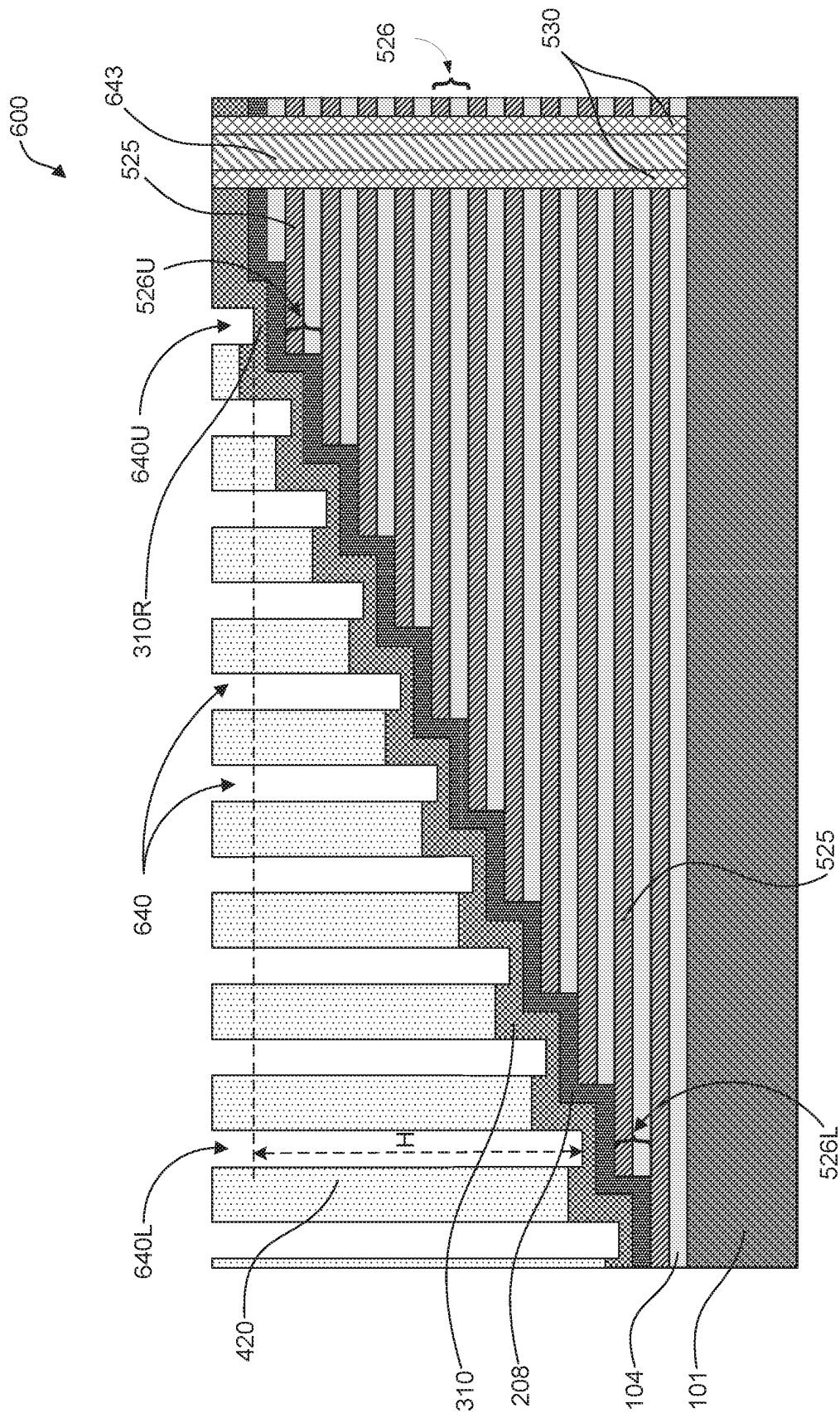


FIG. 6

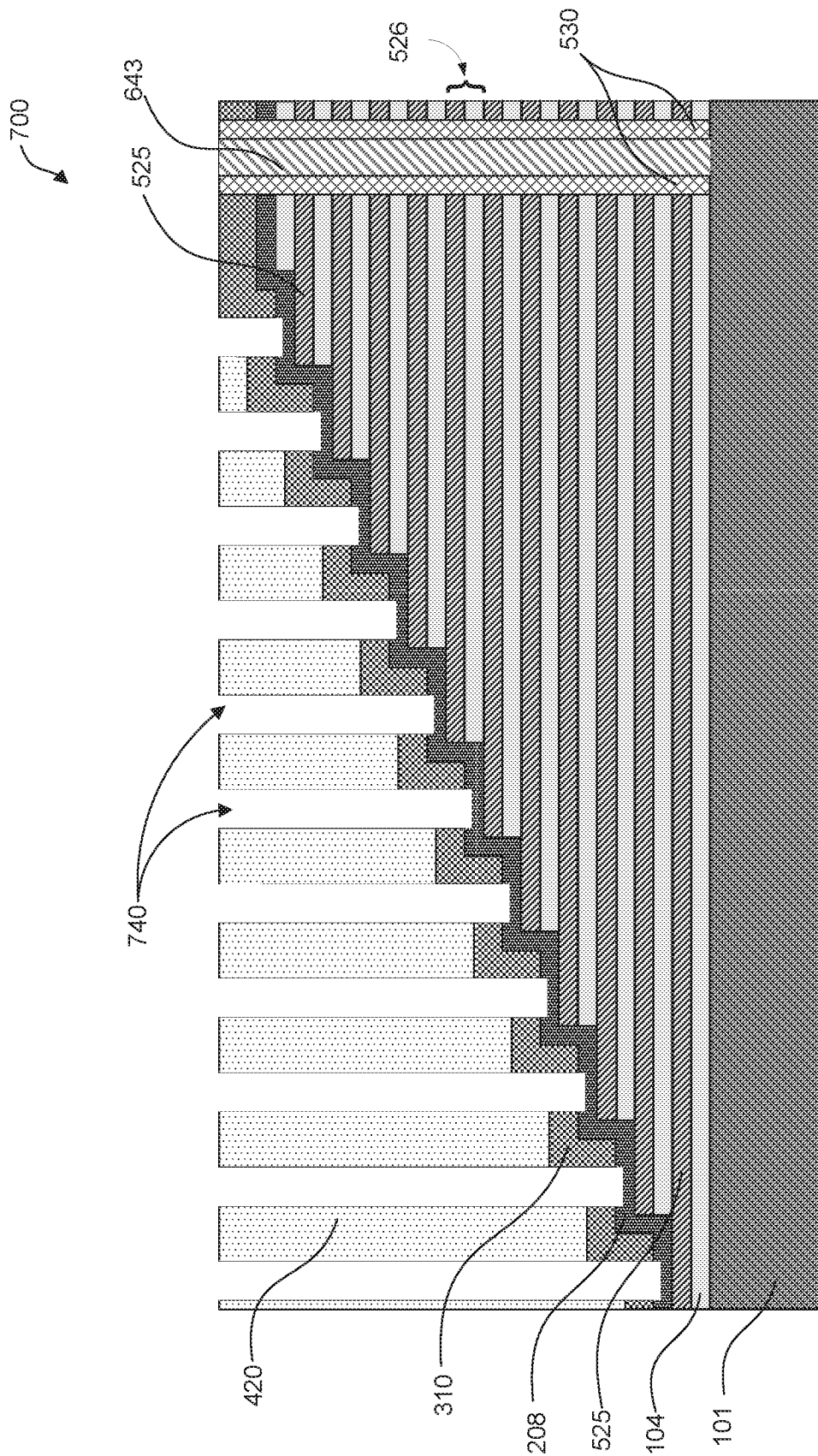


FIG. 7

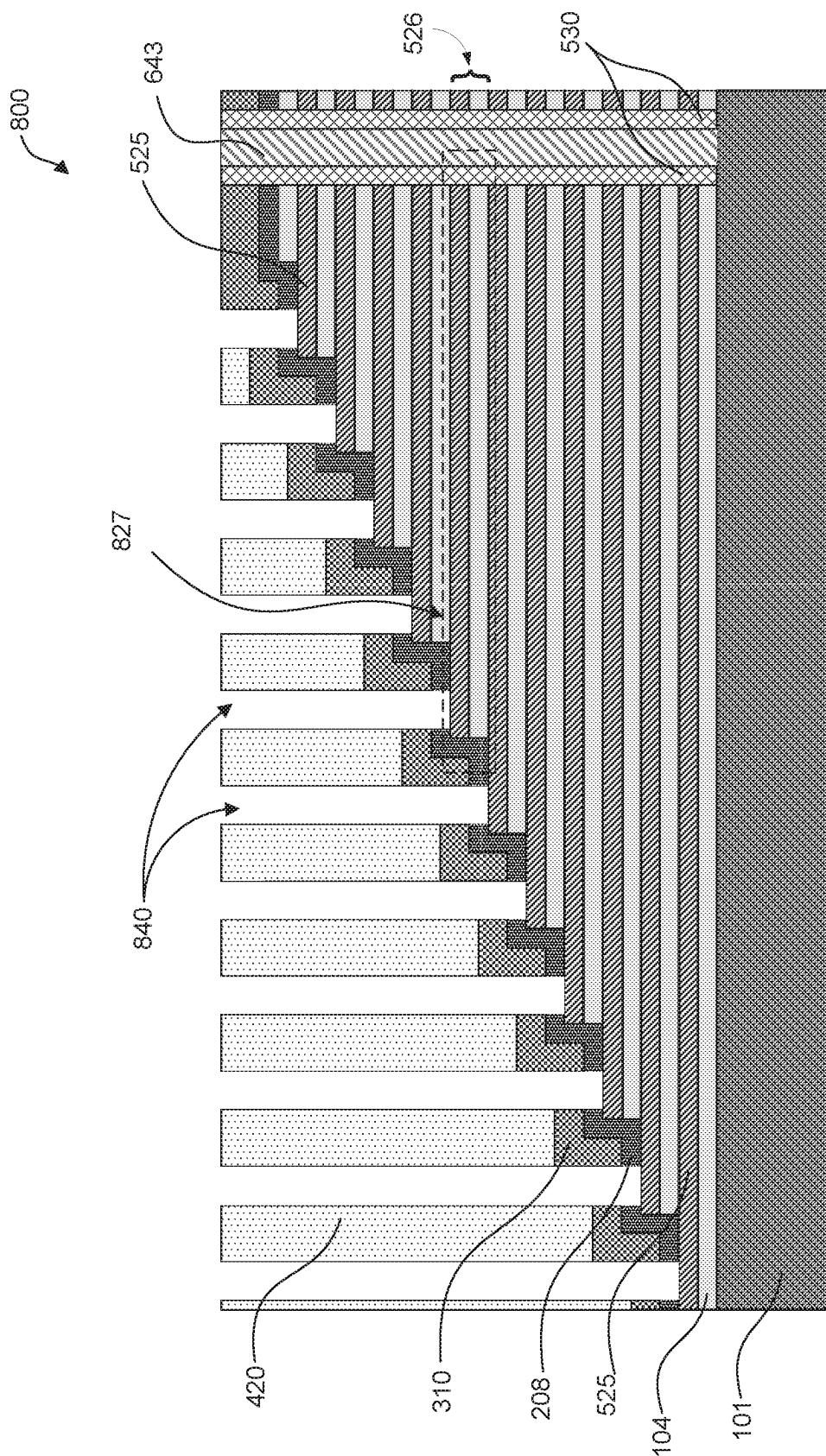


FIG. 8A

827

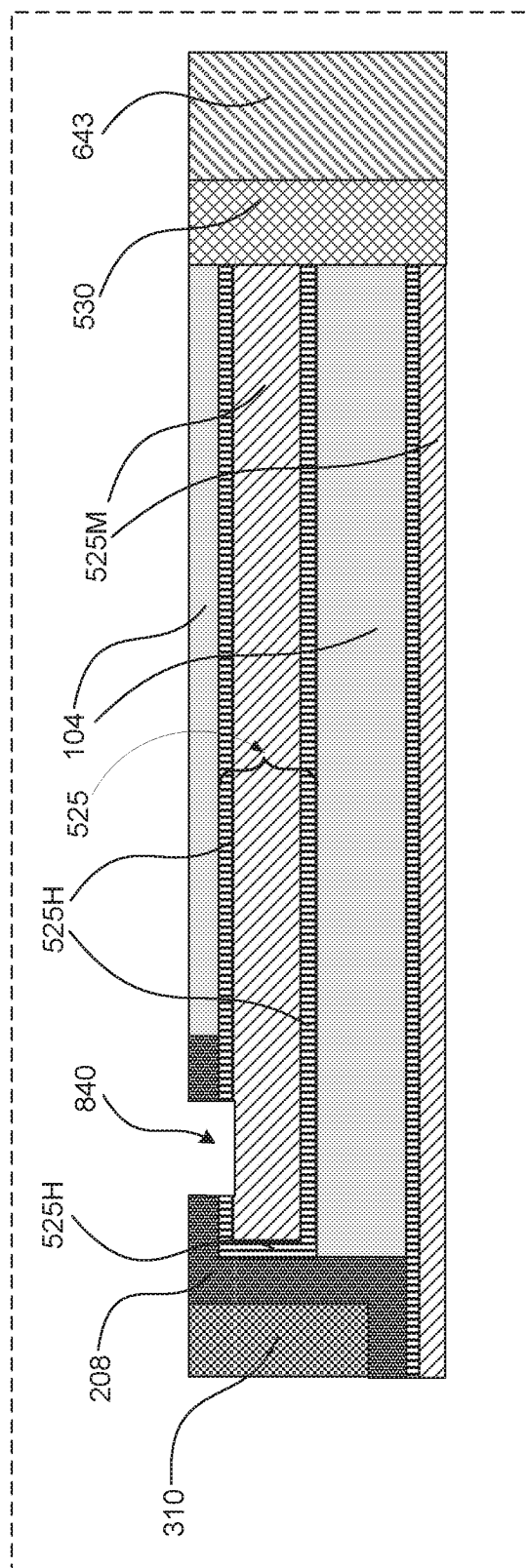


FIG. 8B

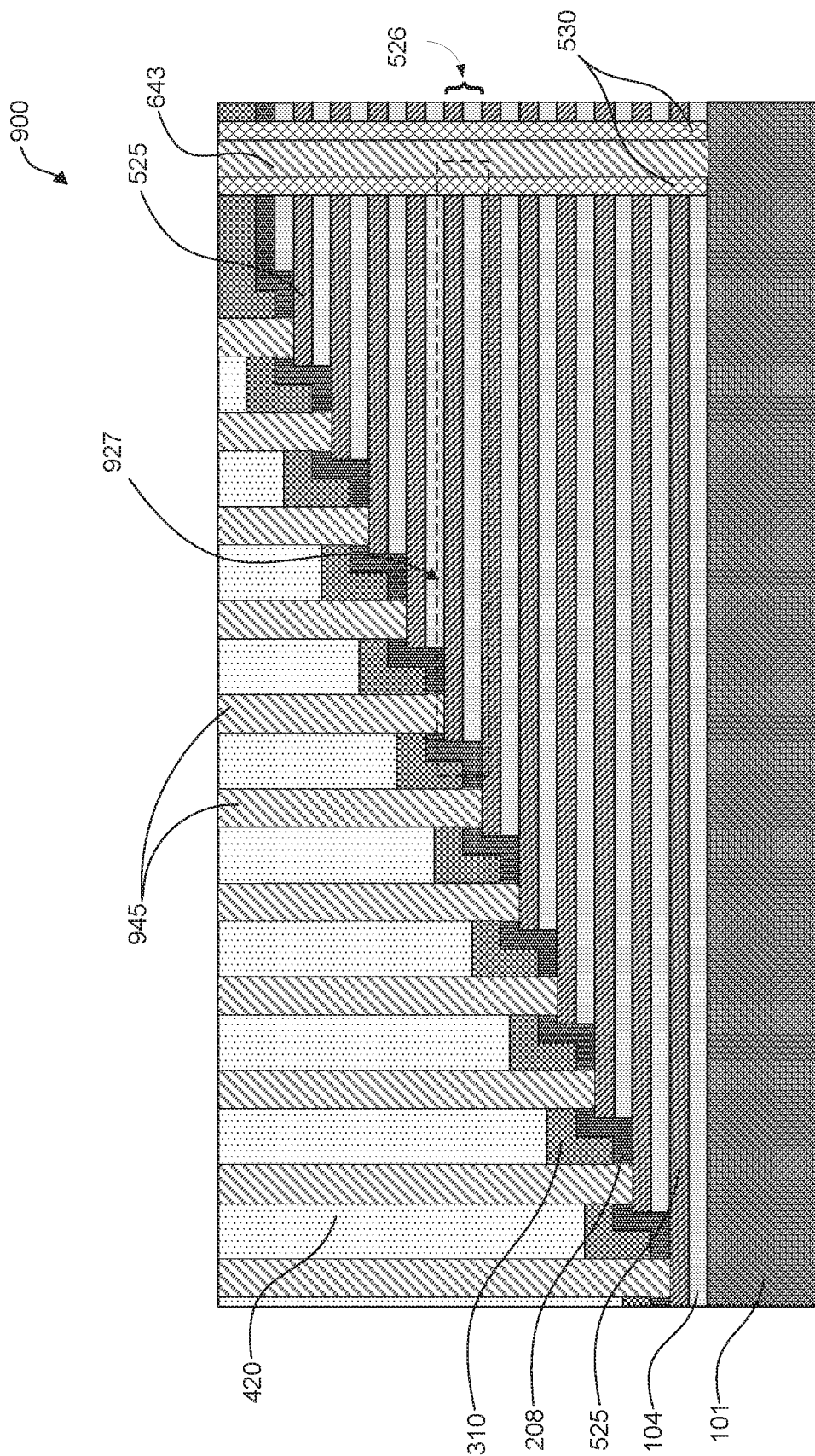


FIG. 9A

927

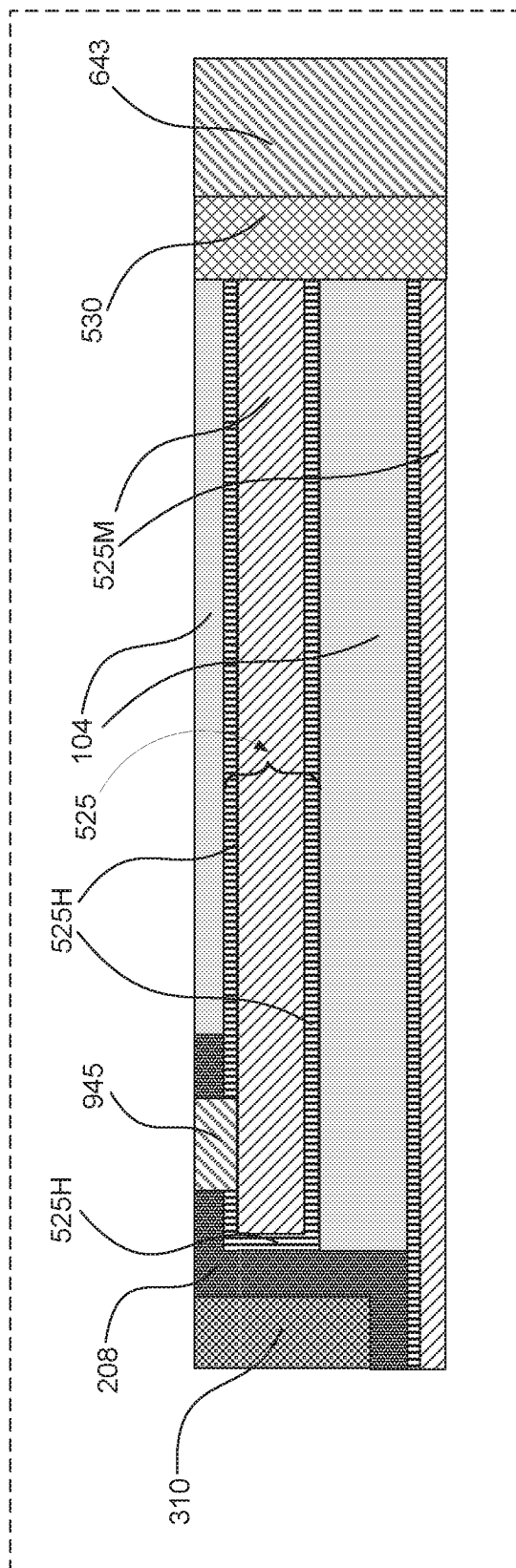


FIG. 9B

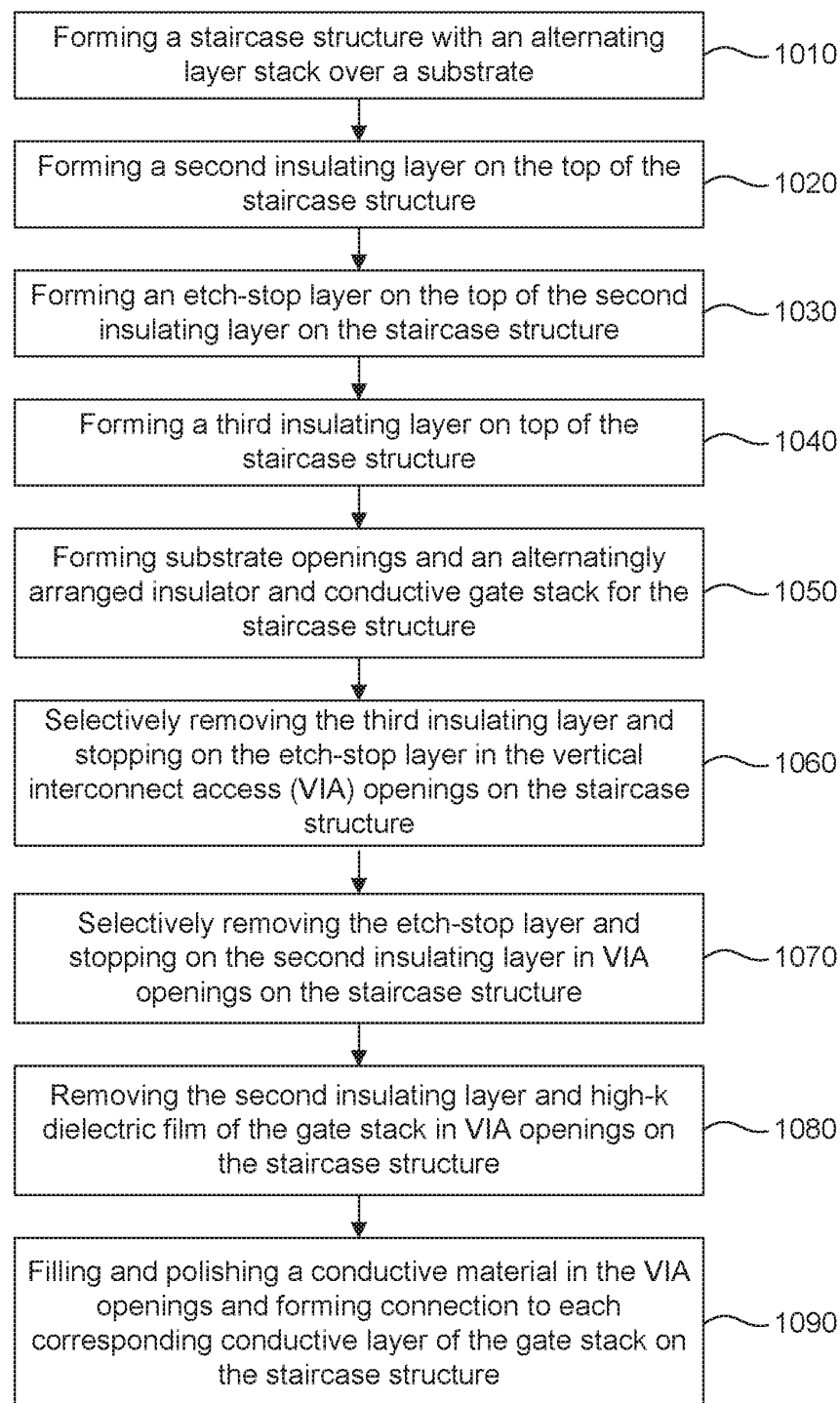


FIG. 10

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		Word Line Contact Structure for Three-Dimensional Memory Devices and Fabrication Methods Thereof		
First Named Inventor/Applicant Name:		Jifeng ZHU		
Filer:		Donald J. Featherstone/Kim Perry		
Attorney Docket Number:		4123.0480003		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1720

Electronic Acknowledgement Receipt	
EFS ID:	39332260
Application Number:	16865056
International Application Number:	
Confirmation Number:	6601
Title of Invention:	Word Line Contact Structure for Three-Dimensional Memory Devices and Fabrication Methods Thereof
First Named Inventor/Applicant Name:	Jifeng ZHU
Customer Number:	26111
Filer:	Donald J. Featherstone/Kim Perry
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0480003
Receipt Date:	01-MAY-2020
Filing Date:	
Time Stamp:	18:03:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 1720
RAM confirmation Number	E202051103267197
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	Cover-Letter-4123-0480003.pdf	349037	no	2
			7d7d4d8f3e126c83a4d25adfab6426f66c60ed17		
Warnings:					
Information:					
2	Transmittal of New Application	Utility-Transmittal-4123-0480003.PDF	386300	no	2
			ef392e7acba41494449bc2bfe152bbcc1f022d9		
Warnings:					
Information:					
3	Authorization for Extension of Time all replies	EOT-Authorization-4123-0480003.pdf	133504	no	1
			8f5a79fbf507cbdfb3d541375a1b970870d08d3d		
Warnings:					
Information:					
4	Application Data Sheet	ADS-4123-0480003.PDF	1256577	no	11
			bd5b5e672d10624613ffa0bf385a30c95a9e467c		
Warnings:					
Information:					
5		Divisional-Application-4123-0480003.pdf	248780	yes	25
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	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	21	
	Claims		22	24	
	Abstract		25	25	

Warnings:					
Information:					
6	Transmittal Letter	IDS-4123-0480003.pdf	161396	no	6
			f4bd677a0eec785e63547f13965d9ed3fa89d503		
Warnings:					
Information:					
7	Information Disclosure Statement (IDS) Form (SB08)	PTOSB08a-4123-0480003.PDF	208805	no	1
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Information:					
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Information:					
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Information:					
10	Power of Attorney	POA-82B-4123-0480003.PDF	543765	no	1
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Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
11	Oath or Declaration filed	Declaration-4123-0480003.PDF	139113	no	4
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Warnings:					
Information:					

12	Drawings-other than black and white line drawings	Drawings-4123-0480003.pdf	132454	no	13
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Warnings:					
Information:					
13	Fee Worksheet (SB06)	fee-info.pdf	35313	no	2
			37dd567905e05e5845496c9a7c1d519985185289		
Warnings:					
Information:					
Total Files Size (in bytes):			4078471		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM

May 1, 2020

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: U.S. Non-Provisional Patent Application under 37 C.F.R. § 1.53(b)
(*Divisional of Appl. No. 16/126,947 ; Filed: September 10, 2018*)
Appl. No. To Be Assigned; Filed: Herewith
For: **WORD LINE CONTACT STRUCTURE FOR THREE-
DIMENSIONAL MEMORY DEVICES AND FABRICATION
METHODS THEREOF**
Inventors: ZHU *et al.*
Our Ref: 4123.0480003

Commissioner:

The following documents are transmitted herewith for appropriate action by the U.S.
Patent and Trademark Office:

1. Utility Patent Application Transmittal Form (PTO/AIA/15);
2. Payment made electronically for \$1,720.00 to cover:

\$1,720.00 Patent Application fees (including basic filing, search, and
examination fees);
3. Authorization to Treat a Reply As Incorporating An Extension of Time
Under 37 C.F.R. § 1.136(a)(3);
4. U.S. Utility Patent Application entitled:

**WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL
MEMORY DEVICES AND FABRICATION METHODS THEREOF**

and naming as inventors:

Jifeng ZHU, Zhenyu LU, Jun CHEN, Si Ping HU, Xiaowang DAI, Lan YAO, Li
Hong XIAO, A Man ZHENG, Kun BAO and Haohao YANG

the application consisting of:

Sterne, Kessler, Goldstein & Fox P.L.L.C. | 1100 New York Avenue, NW | Washington, D.C. 20005
P 202.371.2600 | F 202.371.2540 | sternekessler.com

- a. An Application Data Sheet (37 C.F.R. § 1.76);
 - b. Signed Inventors' Declarations as originally filed in prior U.S. Appl. No. 16/126,947;
 - c. A specification containing:
 - i. 21 pages of description prior to the claims;
 - ii. 3 pages of claims (20 claims);
 - iii. a one (1) page abstract;
 - d. 13 sheets of drawings: (Figure(s) 1-4, 5A-5B, 6-7, 8A-8B, 9A-9B, 10);
5. An executed Power of Attorney by Applicant (PTO/AIA/82B) and the Transmittal for Power of Attorney form (PTO/AIA/82A);
 6. An Information Disclosure Statement (IDS);
 7. Form PTO/SB/08a (1 sheet) listing 18 documents (**US1-US16** and **FP1-FP2**); and
 8. Form PTO/SB/08b (1 sheet) listing 1 document (**NPL1**).

The above-listed documents are filed electronically.

Fee payment is provided via electronic filing. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/M-Y/jcv
Enclosure(s)

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

EPAS ID: PAT6090542

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT
CONVEYING PARTY DATA	
Name	Execution Date
JIFENG ZHU	10/22/2018
ZHENYU LU	10/23/2018
JUN CHEN	10/23/2018
SI PING HU	11/05/2018
XIAOWANG DAI	11/02/2018
LAN YAO	10/22/2018
LI HONG XIAO	10/22/2018
A MAN ZHENG	10/22/2018
KUN BAO	10/22/2018
HAOHAO YANG	10/22/2018
RECEIVING PARTY DATA	
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Street Address:	18 GAOXIN 4TH RD., EAST LAKE HIGH-TECH DEVELOPMENT ZONE
City:	WUHAN, HUBEI
State/Country:	CHINA
PROPERTY NUMBERS Total: 1	
Property Type	Number
Application Number:	16865056
CORRESPONDENCE DATA	
Fax Number:	(202)371-2540
<i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>	
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Address Line 4:	WASHINGTON, D.C. 20005
ATTORNEY DOCKET NUMBER:	4123.0480003
NAME OF SUBMITTER:	DONALD J. FEATHERSTONE

SIGNATURE:	/Donald J. Featherstone/
DATE SIGNED:	05/04/2020
	This document serves as an Oath/Declaration (37 CFR 1.63).
Total Attachments: 4 source=2020-05-04-Assignment-4123-0480003#page1.tif source=2020-05-04-Assignment-4123-0480003#page2.tif source=2020-05-04-Assignment-4123-0480003#page3.tif source=2020-05-04-Assignment-4123-0480003#page4.tif	

COMBINED DECLARATION AND ASSIGNMENT

DECLARATION

As the below named inventors, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ☒ United States application or PCT international application number 16/126,947
filed on September 10, 2018

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar (\$1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is 18 Gaoxin 4th Road, East Lake High-Tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF** for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 26111** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: Jifeng ZHU Date: 2018.10.22

Signature of Inventor: Jifeng ZHU

LEGAL NAME OF INVENTOR

Inventor: Zhenyu LU Date: 2018.10.23

Signature of Inventor: Zhenyu Lu

LEGAL NAME OF INVENTOR

Inventor: Jun CHEN Date: 2018.10.23

Signature of Inventor: Jun CHEN

LEGAL NAME OF INVENTOR

Inventor: Si Ping HU Date: 2018.11.05

Signature of Inventor: Si Ping HU

LEGAL NAME OF INVENTOR

Inventor: Xiaowang DAI Date: 2018.11.2

Signature of Inventor: Xiaowang DAI

LEGAL NAME OF INVENTOR

Inventor: Lan YAO Date: 2018. 10. 22

Signature of Inventor: Lan Yao

LEGAL NAME OF INVENTOR

Inventor: Li Hong XIAO Date: 2018. 10. 22.

Signature of Inventor: Lihong Xiao

LEGAL NAME OF INVENTOR

Inventor: A Man ZHENG Date: 2018. 10. 22

Signature of Inventor: A Man ZHENG

LEGAL NAME OF INVENTOR

Inventor: Kun BAO Date: 2018. 10. 22

Signature of Inventor: Kun Bao

LEGAL NAME OF INVENTOR

Inventor: Haohao YANG Date: 2018/10/22

Signature of Inventor: Haohao YANG

10202996_1.docx



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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
16/865,056	05/01/2020	2811	1720	4123.0480003	20	1

CONFIRMATION NO. 6601

26111

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

FILING RECEIPT



CC000000118846207

Date Mailed: 05/08/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Jifeng ZHU, Wuhan, CHINA;
Zhenyu LU, Wuhan, CHINA;
Jun CHEN, Wuhan, CHINA;
Si Ping HU, Wuhan, CHINA;
Xiaowang DAI, Wuhan, CHINA;
Lan YAO, Wuhan, CHINA;
Li Hong XIAO, Wuhan, CHINA;
A Man ZHENG, Wuhan, CHINA;
Kun BAO, Wuhan, CHINA;
Haohao YANG, Wuhan, CHINA;

Applicant(s)

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA;

Assignment For Published Patent Application

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Power of Attorney: The patent practitioners associated with Customer Number 26111

Domestic Priority data as claimed by applicant

This application is a DIV of 16/126,947 09/10/2018
which is a CON of PCT/CN2018/101308 08/20/2018

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

CHINA 201710774754.6 08/31/2017 No Access Code Provided

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 05/07/2020

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/865,056**

Projected Publication Date: 08/13/2020

Non-Publication Request: No

Early Publication Request: No

Title

WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND
FABRICATION METHODS THEREOF

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign

page 2 of 4

patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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NOT GRANTED

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SelectUSA

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 16/865,056	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	20	minus 20 = *				x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1	minus 3 = *				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720
APPLICATION AS AMENDED - PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
			TOTAL ADD'L FEE			TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
			TOTAL ADD'L FEE			TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/865,056	05/01/2020	Jifeng ZHU	4123.0480003

CONFIRMATION NO. 6601

26111

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

PUBLICATION NOTICE



OC000000119231765

Title:WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF

Publication No.US-2020-0258837-A1

Publication Date:08/13/2020

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publicly available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <https://portal.uspto.gov/pair/PublicPair>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/865,056	05/01/2020	Jifeng ZHU	4123.0480003	6601
26111	7590	03/25/2021		
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C. 1100 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			EXAMINER GEYER, SCOTT B	
			ART UNIT	PAPER NUMBER
			2812	
			NOTIFICATION DATE	DELIVERY MODE
			03/25/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

e-office@sternekessler.com

DETAILED ACTION

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119 (a)-(d). The certified copy has been filed in parent Application No. 16/126,947, filed on September 10, 2018.

Information Disclosure Statement

The references cited within the IDS documents submitted on May 1, 2020 have been considered.

Claim Objections

Claim 13 is objected to because of the following informality:

In claim 13, line 1: change "claim 6" to - - claim 1 - -

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having

ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3, 9, 10, and 12-17 are rejected under 35 U.S.C. 103 as being unpatentable over Shin (US 2017/0148677 A1) in view of Nam et al. (US 2019/0013237 A1, hereinafter referred to as 'Nam').

As to **claim 1**, Shin teaches a method of making a semiconductor structure (see e.g. figures 14-20), comprising:

forming a staircase structure having a plurality of steps (see fig. 14), wherein the forming of each step of the plurality of steps comprises disposing a sacrificial layer (SC) over a dielectric layer (111);

disposing an insulating layer (132) on the staircase structure (fig. 14);

replacing the sacrificial layer of each step with a gate stack (see figs. 17 and 18), the gate stack comprising a conductive layer (160) and a first high-k dielectric layer (158) – see also fig. 4 for detail;

forming a plurality of openings (180) in the insulating layer exposing portions of the staircase structure (see fig. 19);

etching the to expose portions of the conductive layer of each step (also fig. 19, and see paragraph 0124); and

forming a plurality of conductive structures (CGCP) in each of the plurality of openings (fig. 20).

Shin does not teach an etch-stop layer disposed on the plurality of steps.

However, Nam teaches a related method of forming a staircase memory structure (see figs. 14-19), wherein an etch-stop layer (30, in fig. 15) is utilized to cover each step.

It would have been obvious to a person of ordinary skill in the art, at the time the invention was filed, to modify the teaching so Shin in order to add an etch-stop layer as taught by Nam, so as to provide additional structure to aid in proper etching of the gate/wordline contacts; such use of etch-stop layers being readily known and widely utilized in the art of semiconductor manufacturing.

As to **claim 2**, Nam teaches performing an etching process on the insulating layer, wherein an etching rate of the insulating layer is higher than an etching rate of the etch-stop layer. See figures 19-21 and paragraphs 0122 & 0132-0137.

As to **claim 3**, Nam teaches the etching process comprises anisotropic dry etching. See paragraphs 0133-0134.

As to **claim 9**, Nam teaches an etch-stop layer (30, fig. 15, see also e.g. paragraphs 0037 and 0121). Nam does not teach a specific thickness of the etch-stop layer. However, it has long been held that **does not explicitly teach the thickness of the layer**. However, it has long been held that mere scaling up of a prior art process capable of being scaled up, if such were the case, would not establish patentability in a claim to an old process so scaled (See MPEP 2144.04 IV B). In this case, a review of the specification (paragraph 0056) reveals no particular benefit to any particular thickness, and in fact a range of 3 orders of magnitude is provided (10nm to 1000 nm), deflating an

argument that the thickness is particularly critical. In addition, nothing on the record indicates that the difference in thickness between the claim and the reference would operate differently.

As to **claim 10**, Nam teaches disposing the etch-stop layer comprises performing chemical vapor deposition (CVD), physical vapor deposition (PVD), sputtering, atomic layer deposition (ALD), spin-coating, or any combination thereof. See paragraphs 0039-0040.

As to **claim 12**, Shin teaches forming the plurality of conductive structures (CGCP) comprises disposing conductive materials inside the plurality of openings, the conductive materials directly on the exposed conductive layer (160) of the each step (shown in fig. 20).

As to **claim 13**, Shin teaches forming the plurality of conductive structures further comprises planarizing the conductive materials and the insulating layer (see paragraph 0127).

As to **claim 14**, Shin teaches forming the staircase structure further comprises performing a repetitive etch-trim process on the sacrificial layers and the dielectric layers (see paragraphs 0091-0092).

As to **claim 15**, Shin teaches replacing the sacrificial layer of each step with the gate stack comprises:

- forming a substrate opening (T, see fig. 16) through the staircase structure;
- removing the sacrificial layer of each step through the substrate (see fig. 17); and

disposing the first high-k dielectric layer and the conductive layer in place of the sacrificial layer (see fig. 18).

As to **claim 16**, Shin teaches disposing the first high-k dielectric layer (158) comprises disposing *hafnium oxide, zirconium oxide, aluminum oxide*, tantalum oxide, lanthanum oxide and/or any combination thereof (see paragraph 0116).

As to **claim 17**, Shin teaches disposing the conductive layer (160) comprises disposing *tungsten, cobalt, nickel, copper, aluminum*, and/or any combination thereof (see paragraph 0117).

//

Claims 6, 11, 19, and 20 are rejected under 35 U.S.C. 103 as being unpatentable over Shin and Nam as applied to claim 1 above, and further in view of Kim et al. (US 2017/0117222 A1, hereinafter referred to as 'Kim').

As to **claim 6**, neither Shin nor Nam teach an etch-stop layer comprising silicon nitride, silicon oxynitride, and silicon oxide. However, Kim teach a related method of making a staircase memory structure, wherein an etch-stop layer is disposed on the plurality of steps (see figures 5-6). The etch-stop layer (115) comprises silicon nitride (see paragraphs 0079-0080). As to **claims 19 and 20**, Kim teaches prior to disposing the etch-stop layer, disposing a barrier layer (110) on each step of the plurality of steps, wherein the barrier layer protects underlying structures during the etching of the

exposed portions of the etch-stop layer. Kim also teaches the barrier layer comprises silicon oxide. See figure 6 and paragraphs 0079-0080. It would have been obvious to a person of ordinary skill in the art, at the time of the filing of the invention, to modify the methods of Shin and Kim with an etch-stop and barrier layer as taught by Kim, so as to ensure proper etch selectivity compared to the insulation material and to ensure adequate protection of the wordlines during the various etching steps.

As to **claim 11**, Shin and Nam teach planarizing after formation of the insulation layer (Shin: paragraphs 0104-0105; Nam: paragraphs 0122-0123). However, neither Shin nor Nam explicitly state that the planarizing is performed by chemical-mechanical-polishing (CMP). However, Kim teaches CMP to planarized the insulation layer after formation (see paragraph 0083). It would have been obvious to a person of ordinary skill in the art, at the time of the filing of the invention, to modify the teachings of Shin and Nam with CMP as taught by Kim, so as to realize the benefits of chemical-mechanical polishing in order to obtain a flat planar surface, as CMP is a notoriously well-known and utilized process in the semiconductor industry.

Allowable Subject Matter

Claims 4, 7, and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim **and any intervening claims**. (Claims 5 and 8 are also objected to, as being dependent upon objected claims.)

Cited Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: see the attached form PTO-892 for pertinent cited art.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott B. Geyer (telephone: 571-272-1958). The examiner can normally be reached on Monday to Friday, 10AM - 4PM. Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at: <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles D Garber (telephone: 571-272-2194). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the

Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (in U.S.A. or Canada) or 571-272-1000.

/SCOTT B GEYER/
Primary Examiner, Art Unit 2812

Notice of References Cited	Application/Control No. 16/865,056		Applicant(s)/Patent Under Reexamination ZHU et al.	
	Examiner Scott B Geyer		Art Unit 2812	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20170148677-A1	05-2017	SHIN; JoongShik	H01L23/53266	1/1
*	B	US-20190013237-A1	01-2019	Nam; Phil Ouk	H01L21/76816	1/1
*	C	US-20170117222-A1	04-2017	KIM; Hyuk	H01L21/76829	1/1
	D					
	E					
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	I					
	J					
	K					
	L					
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
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	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Search Notes</i> 	Application/Control No. 16/865,056	Applicant(s)/Patent Under Reexamination ZHU et al.
	Examiner Scott B Geyer	Art Unit 2812

CPC - Searched*		
Symbol	Date	Examiner
H01L27/11514 H01L27/11551 H01L27/11578 H01L27/11597	03/22/2021	SBG
H01L27/11509 H01L27/11512 H01L27/11526 H01L27/11529 H01L27/11573 H01L27/11575 H01L27/11592 H01L27/11595	03/22/2021	SBG
H01L21/76829-76834	03/22/2021	SBG
H01L23/5329 H01L23/53295 H01L21/76801	03/22/2021	SBG
H01L21/76802 H01L21/76805 H01L21/76816 H01L21/76877 H01L21/76879	03/22/2021	SBG

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Parent Application (16/126947) - references checked	03/22/2021	SBG
PE2E-Search, details attached	03/22/2021	SBG

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<i>Search Notes</i> 	Application/Control No. 16/865,056	Applicant(s)/Patent Under Reexamination ZHU et al.
	Examiner Scott B Geyer	Art Unit 2812

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L2	2	("20160358855" "20160020169").pn.	(US-PGPUB ; USPAT)	OR	ON	ON	2021/03/18 03:03 PM
L3	1	("10672711").pn.	(USPAT)	OR	ON	ON	2021/03/18 03:03 PM
L4	16	("7539056" "8828884" "9419013" "9515086" "20100013049" "20100207195" "20110031546" "20110169071" "20130313627" "20130337646" "20140106569" "20140284675" "20160020169" "20160118398" "20160358855" "20170236836").pn. OR ("10672711").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB ; USPAT ; USOCR)	OR	ON	ON	2021/03/18 03:03 PM
L5	708	((Yangtze WITH Memory).as. (Jifeng WITH ZHU).in. (Zhenyu WITH LU).in. (Jun WITH CHEN).in. (Si WITH HU).in. (Xiaowang WITH DAI).in. (Lan WITH YAO).in. (Li WITH XIAO).in. (Man WITH ZHENG).in. (Kun WITH BAO).in. (Haohao WITH YANG).in.) AND (staircase staircase stair-case stair-step (stair ADJ case) (stair ADJ step))	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD DE , EA , EP , ES , FR GB , JP , KR , OA , RU SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/18 03:03 PM
L6	288	5 AND (etch\$3 WITH (hi-k high-k dielectric insulat\$3))	(US-PGPUB ; USPAT ; USOCR ; FIT (AU , AP AT , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/18 03:03 PM
L7	132	6 AND (etchstop etch- stop (etch ADJ stop) ESL)	(US-PGPUB ; USPAT ; USOCR ; FIT (AU , AP AT , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/18 03:03 PM

L8	69750	(H01L23/535 H01L21/76895 H01L27/11529 H01L27/11551 H01L27/1157 H01L27/11573 H01L27/11575 H01L27/11578 H01L27/11582).cpc.	(US-PGPUB ; USPAT ; USOCR ; FIT (AU , AP , AT , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/18 03:03 PM
L9	91041	(H01L21/76802 H01L21/76805 H01L21/76816 H01L21/76877 H01L21/76879).cpc.	(US-PGPUB ; USPAT ; USOCR ; FIT (AU , AP , AT , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/19 01:03 PM
L10	74625	(H01L23/5329 H01L23/53295 H01L21/76801 H01L21/76829- 76834).cpc.	(US-PGPUB ; USPAT ; USOCR ; FIT (AU , AP , AT , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/19 01:03 PM
L11	196489	((H01L23/5329 H01L23/53295 H01L21/76801 H01L21/76829- 76834).cpc. OR hi-k OR high-k)	(US-PGPUB ; USPAT ; USOCR ; FIT (AU , AP , AT , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/19 01:03 PM
L12	13629	(H01L27/11514 H01L27/11551 H01L27/11578 H01L27/11597).cpc.	(US-PGPUB ; USPAT ; USOCR ; FIT (AU , AP , AT , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/19 01:03 PM
L13	33097	(H01L27/11509 H01L27/11512 H01L27/11526 H01L27/11529 H01L27/11573 H01L27/11575 H01L27/11592 H01L27/11595).cpc.	(US-PGPUB ; USPAT ; USOCR ; FIT (AU , AP , AT , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/19 01:03 PM
L14	796	L12 AND L9	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/19 01:03 PM
L15	2546	L13 AND L9	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/19 01:03 PM

L16	294	L12 AND L9 AND L11	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/19 01:03 PM
L17	1080	L13 AND L9 AND L11	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/19 01:03 PM
L18	245	16 NOT ("2021" "2020" "2019").ay.	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/19 01:03 PM
L19	877	17 NOT ("2021" "2020" "2019").ay.	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/19 01:03 PM
L20	81	(etch-stop ADJ layer).ti.	(US-PGPUB ; USPAT)	OR	ON	ON	2021/03/19 01:03 PM
L21	164701	((H01L23/5329 H01L23/53295 H01L21/76801).cpc. OR hi-k OR high-k)	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/19 01:03 PM
L23	231237	((H01L21/76829- 76834).cpc. ESL (etch- stop)(etch ADJ stop))	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/19 01:03 PM
L24	443	(L12 OR L13) AND L21 AND L23 AND L9	(US-PGPUB ; USPAT ; USOCR ; FIT (AU , AP , AT , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/19 01:03 PM
L25	1127	(L12 OR L13) AND L23 AND L9	(US-PGPUB ; USPAT ; USOCR ; FIT (AU , AP , AT , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/19 01:03 PM

L26	922	25 NOT ("2021" "2020" "2019").ay.	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/19 01:03 PM
L27	1012	(WL wordline word-line (word ADJ line)) WITH (highK high-K (high ADJ K))	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/19 03:03 PM
L28	31	27 AND L9	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/19 03:03 PM
L30	6433	(H01L27/115-11597).cpc. AND ((gate WL wordline word-line (word ADJ line) gate) WITH (highK high-K (high ADJ K)))	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/19 04:03 PM
L31	213	L30 AND L9	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/19 04:03 PM
L32	167	31 NOT ("2021" "2020" "2019").ay.	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/19 04:03 PM
L40	148	(memory WITH (staircase staircase stair stair-case stair-step)) AND L21 AND L23 AND L9	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/19 06:03 PM
L41	93	40 NOT ("2021" "2020" "2019").ay.	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/19 06:03 PM

L42	280	(WL wordline word-line (word ADJ line) gate) WITH (highK high-K (high ADJ K)) AND (memory WITH (staircase stairstep stair stair-case stair-step))	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/22 11:03 AM
L43	208	42 NOT ("2021" "2020" "2019").ay.	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/22 11:03 AM
L44	5	("20150294980" "20170148677" "20140054789" "20190013237" "20140021632").pn.	(US-PGPUB ; USPAT)	OR	ON	ON	2021/03/22 12:03 PM
L45	2	("20170148677" "20190013237").pn.	(US-PGPUB ; USPAT)	OR	ON	ON	2021/03/22 02:03 PM
L46	2	45 AND anisotropic	(US-PGPUB ; USPAT)	OR	ON	ON	2021/03/22 04:03 PM
L48	134	(L12 OR L13) AND ((etch-stop ESL) WITH (nitride oxynitride oxide))	(US-PGPUB ; USPAT)	OR	ON	ON	2021/03/22 05:03 PM
L49	102	48 NOT ("2021" "2020" "2019").ay.	(US-PGPUB ; USPAT)	OR	ON	ON	2021/03/22 05:03 PM
L50	147	(L12 OR L13) AND ((etch-stop ESL) WITH (nitride oxynitride oxide))	(US-PGPUB ; USPAT ; USOCR ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/22 05:03 PM
L51	115	49 NOT ("2021" "2020" "2019").ay.	(US-PGPUB ; USPAT ; USOCR ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/22 05:03 PM
L52	53	(L12 OR L13) AND ((etch-stop ESL) WITH ((hafnium ADJ oxide) (zirconium ADJ oxide) (aluminum ADJ oxide) (tantalum ADJ oxide) (lanthanum ADJ oxide)))	(US-PGPUB ; USPAT ; USOCR ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/22 05:03 PM
L53	31	52 NOT ("2021" "2020" "2019").ay.	(US-PGPUB ; USPAT ; USOCR ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/22 05:03 PM
L54	392	((etch-stop ESL) WITH ((hafnium ADJ oxide) (zirconium ADJ oxide) (aluminum ADJ oxide) (tantalum ADJ oxide) (lanthanum ADJ oxide)))	(US-PGPUB ; USPAT ; USOCR ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/22 05:03 PM
L55	32	54 AND (staircase stairstep stair stair-case stair-step)	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/22 05:03 PM

L56	250	54 AND (memory)	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/22 05:03 PM
L57	135	56 NOT ("2021" "2020" "2019").ay.	(US-PGPUB ; USPAT ; USOCR ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/22 05:03 PM
L58	53	L54 AND (L12 OR L13)	(US-PGPUB ; USPAT ; USOCR ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/22 05:03 PM
L59	31	58 NOT ("2021" "2020" "2019").ay.	(US-PGPUB ; USPAT ; USOCR ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/22 05:03 PM
L60	1	("20170117222").pn.	(US-PGPUB ; USPAT)	OR	ON	ON	2021/03/22 05:03 PM
L61	38	(L12 OR L13) AND ((etch-stop ESL) WITH (depth dimension thick thickness) WITH (nm nms angstrom nanometer nanometre))	(US-PGPUB ; USPAT ; USOCR ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/22 06:03 PM
L62	18	61 NOT ("2021" "2020" "2019").ay.	(US-PGPUB ; USPAT ; USOCR ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/22 06:03 PM
L63	1014	((etch-stop ESL) WITH (depth dimension thick thickness) WITH (nm nms angstrom nanometer nanometre))	(US-PGPUB ; USPAT ; USOCR ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/22 06:03 PM
L64	311	((etch-stop ESL) WITH (depth dimension thick thickness) WITH (nm nms angstrom nanometer nanometre)) AND (memory)	(US-PGPUB ; USPAT ; USOCR ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/22 06:03 PM
L65	17	((etch-stop ESL) WITH (depth dimension thick thickness) WITH (nm nms angstrom nanometer nanometre)) AND (staircase stairstep stair stair-case stair- step)	(US-PGPUB ; USPAT ; USOCR ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/22 06:03 PM
L66	59	(L12 OR L13) AND ((etch-stop ESL) WITH (depth dimension thick thickness))	(US-PGPUB ; USPAT ; USOCR ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/22 06:03 PM
L67	38	66 NOT ("2021" "2020" "2019").ay.	(US-PGPUB ; USPAT ; USOCR ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/22 06:03 PM
L68	3	("20170148677" "20190013237" "20170117222").pn.	(US-PGPUB ; USPAT)	OR	ON	ON	2021/03/22 06:03 PM

L70	5287	(L12 OR L13) AND (WL wordline word-line (word ADJ line)) WITH (silicon si poly-si polysi polysilicon ge germanium)	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/22 07:03 PM
L71	1621	70 AND (remov\$3 WITH sacrificial)	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/22 07:03 PM
L72	530	71 NOT ("2021" "2020" "2019" "2018" "2017").ay.	(US-PGPUB ; USPAT)	OR	ON	ON	2021/03/22 07:03 PM
L73	266	71 NOT ("2021" "2020" "2019" "2018" "2017").ay.	(USPAT)	OR	ON	ON	2021/03/22 07:03 PM
L74	1059	70 AND (staircase stairstep stair stair-case stair-step)	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/22 07:03 PM
L75	569	74 AND (remov\$3 WITH sacrificial)	(US-PGPUB ; USPAT ; USOCR ; FIT (AP , AT , AU , CA , CH , CN , DD , DE , EA , EP , ES , FR , GB , JP , KR , OA , RU , SU , WO) ; FPRS ; EPO ; JPO ; DERWENT ; IBM_TDB)	OR	ON	ON	2021/03/22 07:03 PM
L76	166	75 NOT ("2021" "2020" "2019" "2018" "2017").ay.	(US-PGPUB ; USPAT)	OR	ON	ON	2021/03/22 07:03 PM

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

Receipt date: 05/01/2020

16/865,056 - GAU: 2812

PTO/SB/08a (07-09)

Approved for use through 11/30/2020. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Application Number	~~To Be Assigned~~
		Filing Date	Herewith
		First Named Inventor	Jifeng ZHU
		Art Unit	~~To Be Assigned~~
		Examiner Name	~~To Be Assigned~~ Scott Geyer
Sheet 1	of 1	Attorney Docket Number	4123.0480003

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
/SG/	US1	US- 2010/0013049 A1	01-21-2010	Tanaka et al.	
/SG/	US2	US- 2010/0207195 A1	08-19-2010	Fukuzumi et al.	
/SG/	US3	US- 2011/0031546 A1	02-10-2011	Uenaka et al.	
/SG/	US4	US- 2011/0169071 A1	07-14-2011	Uenaka et al.	
/SG/	US5	US- 2013/0313627 A1	11-28-2013	Lee et al.	
/SG/	US6	US- 2013/0337646 A1	12-19-2013	Cernea et al.	
/SG/	US7	US- 2014/0106569 A1	04-17-2014	Oh et al.	
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/SG/	US9	US- 2016/0118398 A1	04-28-2016	Yon et al.	
/SG/	US10	US- 2016/0020169 A1	01-21-2016	Matsuda	
/SG/	US11	US- 2016/0358855 A1	12-08-2016	Oh	
/SG/	US12	US- 2017/0236836 A1	08-17-2017	Huo et al.	
/SG/	US13	US- 7,539,056 B2	05-26-2009	Katsumata et al.	
/SG/	US14	US- 8,828,884 B2	09-09-2014	Lee et al.	
/SG/	US15	US- 9,419,013 B1	08-16-2016	Lee et al.	
/SG/	US16	US- 9,515,086 B2	12-06-2016	Yon et al.	
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)	MM-DD-YYYY			
/SG/	FP1	CN 104157654 A	11-19-2014	INST OF MICROELECTRONICS		
/SG/	FP2	CN 104396004 A	03-04-2015	SANDISK TECHNOLOGIES INC.		

Examiner Signature	/SCOTT B GEYER/	Date Considered	03/18/2021
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Micron Ex. 1002, p. 108

Micron v. YMTc

IPR2025-00228

Receipt date: 05/01/2020

16/865,056 - GAU: 2812

PTO/SB/08b (07-09)

Approved for use through 11/30/2020. OMB 0651-0031

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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Complete if Known	
		Application Number	~~To Be Assigned~~
		Filing Date	Herewith
		First Named Inventor	Jifeng ZHU
		Art Unit	~~To Be Assigned~~
		Examiner Name	~~To Be Assigned~~ Scott Geyer
Sheet 1	of 1	Attorney Docket Number	4123.0480003

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
/SG/	NPL1	International Search Report and Written Opinion of the International Searching Authority directed to related International Patent Application No. PCT/CN2018/101308, mailed November 21, 2018; 6 pages.	

Examiner Signature	/SCOTT B GEYER/	Date Considered	03/18/2021
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¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO:

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Micron Ex. 1002, p. 109

Micron v. YMTC

IPR2025-00228

Bibliographic Data

Application No: 16/865,056

Foreign Priority claimed: ☒ Yes ☐ No

35 USC 119 (a-d) conditions met: ☒ Yes ☐ No ☐ Met After Allowance

Verified and Acknowledged: /SCOTT B GEYER/

Examiner's Signature

Initials

Title:

WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
05/01/2020	257	2812	4123.0480003
RULE			

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CONTINUING DATA

This application is a DIV of 16126947 09/10/2018 PAT 10672711

16126947 is a CON of PCT/CN2018/101308 08/20/2018

FOREIGN APPLICATIONS

CHINA CN201710774754.6 08/31/2017

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05/07/2020

STATE OR COUNTRY

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WASHINGTON, DC 20005
UNITED STATES

FILING FEE RECEIVED

\$1,720

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 16/865,056		Filing Date 05/01/2020		☐ To be Mailed	
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO									
APPLICATION AS FILED - PART I									
		(Column 1)			(Column 2)				
FOR		NUMBER FILED			NUMBER EXTRA			RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A			N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A			N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A			N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(j))		20 minus 20 =			* 0			x \$100 =	0
INDEPENDENT CLAIMS (37 CFR 1.16(h))		1 minus 3 =			* 0			x \$460 =	0
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).							
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL		0	
APPLICATION AS AMENDED - PART II									
		(Column 1)			(Column 2)			(Column 3)	
AMENDMENT	05/25/2021	CLAIMS REMAINING AFTER AMENDMENT			HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(j))	* 19	Minus	** 20	= 0			x \$100 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0			x \$480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
								TOTAL ADD'L FEE	0
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT			HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(j))	*	Minus	**	=			x \$0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=			x \$0 =	
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
								TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.								LIE	
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".								/GERALDINE L STANLEY/	
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".									
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.									

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Jifeng ZHU

Applicant: YANGTZE MEMORY
TECHNOLOGIES CO., LTD.

Application No.: 16/865,056

Filed: May 1, 2020

Confirmation No.: 6601

Art Unit: 2812

Examiner: GEYER, SCOTT B

Atty. Docket: 4123.0480003

Title: **WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY
DEVICES AND FABRICATION METHODS THEREOF**

Amendment and Reply Under 37 C.F.R. § 1.111

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

In reply to the Office Action dated **March 25, 2021** ("Office Action"), Applicant submits the following Amendment and Remarks.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A method for forming a semiconductor structure, comprising:
 - forming a staircase structure having a plurality of steps, wherein the forming of each step of the plurality of steps comprises disposing a sacrificial layer over a dielectric layer;
 - disposing an etch-stop layer on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer;
 - disposing an insulating layer on the etch-stop layer;
 - replacing the sacrificial layer of each step with a gate stack, the gate stack comprising a conductive layer and a first high-k dielectric layer;
 - forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer;
 - etching the exposed portions of the etch-stop layer in the plurality of openings and exposing at least a portion of the conductive layer of each step; and
 - forming a plurality of conductive structures in each of the plurality of openings.
2. (Original) The method of claim 1, wherein the forming the plurality of openings comprises performing an etching process on the insulating layer, wherein an etching rate of the insulating layer is higher than an etching rate of the etch-stop layer.
3. (Original) The method of claim 2, wherein the etching process comprises anisotropic dry etching.
4. (Original) The method of claim 1, wherein etching the exposed portions of the etch-stop layer comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer of each step.
5. (Original) The method of claim 4, wherein etching the exposed portions of the etch-stop layer further comprises etching the exposed portions of the etch-stop layer at a higher

Atty. Dkt. No. 4123.0480003

etching rate than an etching rate of the first high-k dielectric layer.

6. (Original) The method of claim 1, wherein disposing the etch-stop layer comprises disposing one or more of silicon nitride, silicon oxynitride, and silicon oxide.
7. (Cancelled).
8. (Currently Amended) The method of claim [[7]] 1, wherein disposing the ~~second high-k dielectric~~ etch-stop layer comprises disposing hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, and/or any combination thereof.
9. (Original) The method of claim 1, wherein disposing the etch-stop layer comprises disposing the etch-stop layer with a thickness in a range between 10 nm to 100 nm.
10. (Original) The method of claim 1, wherein disposing the etch-stop layer comprises performing chemical vapor deposition (CVD), physical vapor deposition (PVD), sputtering, atomic layer deposition (ALD), spin-coating, or any combination thereof.
11. (Original) The method of claim 1, further comprising:
after disposing the insulating layer on the etch-stop layer, planarizing the insulating layer and the staircase structure by using chemical-mechanical-polishing (CMP).
12. (Original) The method of claim 1, wherein forming the plurality of conductive structures comprises disposing conductive materials inside the plurality of openings, the conductive materials directly on the exposed conductive layer of the each step.
13. (Currently Amended) The method of claim [[6]] 1, wherein forming the plurality of conductive structures further comprises planarizing the conductive materials and the insulating layer.

14. (Original) The method of claim 1, wherein forming the staircase structure further comprises performing a repetitive etch-trim process on the sacrificial layers and the dielectric layers.
15. (Original) The method of claim 1, wherein replacing the sacrificial layer of each step with the gate stack comprises:
 - forming a substrate opening through the staircase structure;
 - removing the sacrificial layer of each step through the substrate; and
 - disposing the first high-k dielectric layer and the conductive layer in place of the sacrificial layer.
16. (Original) The method of claim 15, wherein disposing the first high-k dielectric layer comprises disposing hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide and/or any combination thereof.
17. (Original) The method of claim 15, wherein disposing the conductive layer comprises disposing tungsten, cobalt, nickel, copper, aluminum, and/or any combination thereof.
18. (Original) The method of claim 15, wherein disposing the conductive layer comprises disposing poly-crystalline silicon, poly-crystalline germanium, or poly-crystalline germanium-silicon.
19. (Original) The method of claim 1, further comprising:
 - prior to disposing the etch-stop layer, disposing a barrier layer on each step of the plurality of steps, wherein the barrier layer protects underlying structures during the etching of the exposed portions of the etch-stop layer.
20. (Original) The method of claim 19, wherein disposing the barrier layer comprises disposing one or more of silicon oxide, silicon oxynitride, silicon nitride, TEOS, aluminum oxide, and silicon oxide incorporated with F, C, N, or H.

Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1-20 are pending in the application, with claim 1 being the sole independent claim. Claims 1, 8 and 13 are sought to be amended. Claim 7 is sought to be canceled without prejudice to or disclaimer of the subject matter therein. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Allowable Subject Matter

Claims 4, 7, 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 5 and 8 are also objected to, as being dependent upon objected claims.

Applicant thanks the Examiner for indicating the allowable subject matter. The distinguishing features of claim 7 have been incorporated into independent claim 1, and claim 7 is cancelled accordingly. As such, Applicant respectfully requests that the objections be withdrawn.

Claim Objections

Claim 13 is objected to because of its informality. Without acquiescing to the propriety of the objection, claim 13 has been amended to depend from claim 1. Therefore, Applicant respectfully requests the objection be withdrawn.

Rejections under 35 U.S.C. § 103

Claims 1-3, 9, 10 and 12-17 are rejected under 35 U.S.C. § 103 as being allegedly unpatentable over U.S. Publication No. 2017/0148677 to Shin (“Shin”) in view of U.S. Publication No. 2019/0013237 to Nam *et al.* (“Nam”). Claims 6, 11, 19 and 20 are rejected under 35 U.S.C. § 103 as being allegedly unpatentable over Shin and Nam as applied to claim 1, and further in view of U.S. Publication No. 2017/0117222 to Kim *et al.* (“Kim”). Applicant respectfully traverses these rejections.

Without acquiescing to the propriety of the rejections and reserving the right to argue additional or different distinguishing features in the future, independent claim 1 has been amended to incorporate the allowable features of claim 7. Therefore, Applicant respectfully requests the rejections to be withdrawn and claim 1 be passed onto allowance.

Claims 2-3, 6, 9-17 and 19-20 are allowable at least because they recite all of the features of independent claim 1 from which they respectively depend, as well as for their additional distinguishing features. Applicant respectfully requests the rejections to be reversed and claims 2-3, 6, 9-17 and 19-20 be passed onto allowance.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that

Reply to Office Action of March 25, 2021

Jifeng ZHU
Application No. 16/865,056

personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: 5/25/21
1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

16513452.3

Atty. Dkt. No. 4123.0480003

Electronic Acknowledgement Receipt	
EFS ID:	42812122
Application Number:	16865056
International Application Number:	
Confirmation Number:	6601
Title of Invention:	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF
First Named Inventor/Applicant Name:	Jifeng ZHU
Customer Number:	26111
Filer:	Donald J. Featherstone/Julia Vang
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0480003
Receipt Date:	25-MAY-2021
Filing Date:	01-MAY-2020
Time Stamp:	13:40:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	2021-05-25-Cover-Letter-4123-0480003.pdf	196399	no	1
			b2cd64fde64044229486bad069b703132a348466		
Warnings:					

Information:					
2		2021-05-25- Amendment-4123-0480003.pdf	154492 554ef41d57a42e28ec6f289689c103dd9c60af37	yes	7
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Claims		2	4	
	Applicant Arguments/Remarks Made in an Amendment		5	7	
Warnings:					
Information:					
Total Files Size (in bytes):			350891		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. New Applications Under 35 U.S.C. 111 If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. National Stage of an International Application under 35 U.S.C. 371 If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. New International Application Filed with the USPTO as a Receiving Office If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

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May 25, 2021

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 6601
Art Unit: 2812
Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Appl. No. 16/865,056; Filing Date: May 1, 2020
For: **WORD LINE CONTACT STRUCTURE FOR THREE-
DIMENSIONAL MEMORY DEVICES AND FABRICATION
METHODS THEREOF**
First Named Inventor: Jifeng ZHU
Our Ref: 4123.0480003

Commissioner:

Transmitted herewith for appropriate action is a document entitled Amendment and Reply Under 37 C.F.R. § 1.111, which is submitted electronically.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office hereby authorized to charge any fee deficiency and any additional fees required to continue prosecution or appeal of this application (including issue fees for net addition of claims or forwarding to appeal) or credit any overpayment to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/M-Y/jcv
Enclosure(s)



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
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NOTICE OF ALLOWANCE AND FEE(S) DUE

26111 7590 06/09/2021
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER

GEYER, SCOTT B

ART UNIT

PAPER NUMBER

2812

DATE MAILED: 06/09/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/865,056	05/01/2020	Jifeng ZHU	4123.0480003	6601

TITLE OF INVENTION: WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	09/09/2021

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980.

It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26111 7590 06/09/2021
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/865,056	05/01/2020	Jifeng ZHU	4123.0480003	6601

TITLE OF INVENTION: WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	09/09/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
GEYER, SCOTT B	2812	257-751000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/865,056	05/01/2020	Jifeng ZHU	4123.0480003	6601
26111 7590 06/09/2021 STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C. 1100 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			EXAMINER GEYER, SCOTT B	
			ART UNIT 2812	PAPER NUMBER
DATE MAILED: 06/09/2021				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b) (2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/865,056	Applicant(s) ZHU et al.	
	Examiner Scott B Geyer	Art Unit 2812	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to papers filed by the applicant on May 25, 2021.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-5 and 8-20. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:
a) ☒ All b) ☐ Some *c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 16/126,947.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892) 2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date ____. 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material ____. 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date ____.	5. ☒ Examiner's Amendment/Comment 6. ☒ Examiner's Statement of Reasons for Allowance 7. ☐ Other ____.
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DETAILED ACTION

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee. Authorization for this examiner's amendment was given in an interview with Mr. Donald Featherstone on June 3, 2021.

The application has been amended as follows:

Cancel claim 6

Allowable Subject Matter

Claims 1-5 and 8-20 are allowed.

The following is an examiner's statement of reasons for allowance: independent claim 1 has been amended by the applicant to incorporate allowable subject matter as directed in the previous office action (mail date March 25, 2021).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Cited Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: see the attached form PTO-892 for pertinent cited art.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott B. Geyer (telephone: 571-272-1958). The examiner can normally be reached on Monday to Friday, 10AM - 4PM. Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at: <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles D Garber (telephone: 571-272-2194). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like

assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (in U.S.A. or Canada) or 571-272-1000.

/SCOTT B GEYER/
Primary Examiner, Art Unit 2812

<i>Notice of References Cited</i>	Application/Control No. 16/865,056		Applicant(s)/Patent Under Reexamination ZHU et al.	
	Examiner Scott B Geyer		Art Unit 2812	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20120119283-A1	05-2012	Lee; Jaegoo	H01L27/11565	257/316
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Search Notes</i> 	Application/Control No. 16/865,056	Applicant(s)/Patent Under Reexamination ZHU et al.
	Examiner Scott B Geyer	Art Unit 2812

CPC - Searched*		
Symbol	Date	Examiner
H01L27/11514 H01L27/11551 H01L27/11578 H01L27/11597	03/22/2021	SBG
H01L27/11509 H01L27/11512 H01L27/11526 H01L27/11529 H01L27/11573 H01L27/11575 H01L27/11592 H01L27/11595	03/22/2021	SBG
H01L21/76829-76834	03/22/2021	SBG
H01L23/5329 H01L23/53295 H01L21/76801	03/22/2021	SBG
H01L21/76802 H01L21/76805 H01L21/76816 H01L21/76877 H01L21/76879	03/22/2021	SBG

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Parent Application (16/126947) - references checked	03/22/2021	SBG
PE2E-Search, details attached	03/22/2021	SBG
PE2E-Search updated, details attached	06/03/2021	SBG

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<i>Search Notes</i> 	Application/Control No. 16/865,056	Applicant(s)/Patent Under Reexamination ZHU et al.
	Examiner Scott B Geyer	Art Unit 2812

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	Interference Search	06/03/2021	SBG

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Issue Classification 	Application/Control No. 16/865,056	Applicant(s)/Patent Under Reexamination ZHU et al.
	Examiner Scott B Geyer	Art Unit 2812

CPC						
Symbol					Type	Version
H01L	/	27	/	11529	F	2013-01-01
H01L	/	23	/	535	I	2013-01-01
H01L	/	27	/	11551	I	2013-01-01
H01L	/	21	/	76895	I	2013-01-01
H01L	/	27	/	11573	I	2013-01-01
H01L	/	27	/	11578	I	2013-01-01
H01L	/	27	/	11582	I	2013-01-01
H01L	/	27	/	1157	I	2013-01-01
H01L	/	27	/	11575	I	2013-01-01

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version
/		/		

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	18	
/SCOTT B GEYER/ Primary Examiner, Art Unit 2812	03 June 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	9A, 9B

U.S. Patent and Trademark Office

Part of Paper No.: 20210603

Issue Classification 	Application/Control No. 16/865,056	Applicant(s)/Patent Under Reexamination ZHU et al.
	Examiner Scott B Geyer	Art Unit 2812

INTERNATIONAL CLASSIFICATION			
CLAIMED			
H01L27/11529		27	11529
NON-CLAIMED			

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	18	
/SCOTT B GEYER/ Primary Examiner, Art Unit 2812	03 June 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	9A, 9B

U.S. Patent and Trademark Office

Part of Paper No.: 20210603

Issue Classification 	Application/Control No. 16/865,056	Applicant(s)/Patent Under Reexamination ZHU et al.
	Examiner Scott B Geyer	Art Unit 2812

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	8	10	17	19										
2	2	9	11	18	20										
3	3	10	12												
4	4	11	13												
5	5	12	14												
	6	13	15												
	7	14	16												
6	8	15	17												
7	9	16	18												

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	18	
/SCOTT B GEYER/ Primary Examiner, Art Unit 2812	03 June 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	9A, 9B

U.S. Patent and Trademark Office

Part of Paper No.: 20210603

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L2	2	("20160358855" "20160020169").pn.	(US-PGPUB; USPAT)	OR	ON	ON	2021/03/18 03:29 PM
L3	1	("10672711").pn.	(USPAT)	OR	ON	ON	2021/03/18 03:31 PM
L4	16	("7539056" "8828884" "9419013" "9515086" "20100013049" "20100207195" "20110031546" "20110169071" "20130313627" "20130337646" "20140106569" "20140284675" "20160020169" "20160118398" "20160358855" "20170236836").pn. OR ("10672711").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2021/03/18 03:31 PM
L5	708	((Yangtze WITH Memory).as. (Jifeng WITH ZHU).in. (Zhenyu WITH LU).in. (Jun WITH CHEN).in. (Si WITH HU).in. (Xiaowang WITH DAI).in. (Lan WITH YAO).in. (Li WITH XIAO).in. (Man WITH ZHENG).in. (Kun WITH BAO).in. (Haohao WITH YANG).in.) AND (staircase staircase stair-case stair-step (stair ADJ case) (stair ADJ step))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/18 03:44 PM
L6	288	5 AND (etch\$3 WITH (hi-k high-k dielectric insulat\$3))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/18 03:44 PM
L7	132	6 AND (etchstop etch- stop (etch ADJ stop) ESL)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU,	OR	ON	ON	2021/03/18 03:45 PM

			SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L8	69750	(H01L23/535 H01L21/76895 H01L27/11529 H01L27/11551 H01L27/1157 H01L27/11573 H01L27/11575 H01L27/11578 H01L27/11582).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/18 03:46 PM
L9	91041	(H01L21/76802 H01L21/76805 H01L21/76816 H01L21/76877 H01L21/76879).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/19 01:04 PM
L10	74625	(H01L23/5329 H01L23/53295 H01L21/76801 H01L21/76829- 76834).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/19 01:05 PM
L11	196489	((H01L23/5329 H01L23/53295 H01L21/76801 H01L21/76829- 76834).cpc. OR hi-k OR high-k)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/19 01:05 PM
L12	13629	(H01L27/11514 H01L27/11551 H01L27/11578 H01L27/11597).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/19 01:07 PM
L13	33097	(H01L27/11509 H01L27/11512 H01L27/11526 H01L27/11529 H01L27/11573 H01L27/11575 H01L27/11592 H01L27/11595).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/19 01:08 PM
L14	796	L12 AND L9	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD,	OR	ON	ON	2021/03/19 01:09 PM

			DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L15	2546	L13 AND L9	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/19 01:09 PM
L16	294	L12 AND L9 AND L11	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/19 01:10 PM
L17	1080	L13 AND L9 AND L11	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/19 01:10 PM
L18	245	16 NOT ("2021" "2020" "2019").ay.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/19 01:10 PM
L19	877	17 NOT ("2021" "2020" "2019").ay.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/19 01:10 PM
L20	81	(etch-stop ADJ layer).ti.	(US-PGPUB; USPAT)	OR	ON	ON	2021/03/19 01:11 PM
L21	164701	((H01L23/5329 H01L23/53295 H01L21/76801).cpc. OR hi-k OR high-k)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/19 01:13 PM

L23	231237	((H01L21/76829-76834).cpc. ESL (etch-stop)(etch ADJ stop))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/19 01:15 PM
L24	443	(L12 OR L13) AND L21 AND L23 AND L9	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/19 01:16 PM
L25	1127	(L12 OR L13) AND L23 AND L9	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/19 01:16 PM
L26	922	25 NOT ("2021" "2020" "2019").ay.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/19 01:17 PM
L27	1012	(WL wordline word-line (word ADJ line)) WITH (highK high-K (high ADJ K))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/19 03:58 PM
L28	31	27 AND L9	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/19 03:58 PM
L30	6433	(H01L27/115-11597).cpc. AND ((gate WL wordline word-line (word ADJ line) gate) WITH (highK high-K (high ADJ K)))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2021/03/19 04:00 PM

			IBM_TDB)				
L31	213	L30 AND L9	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO)); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/19 04:00 PM
L32	167	31 NOT ("2021" "2020" "2019").ay.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO)); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/19 04:00 PM
L40	148	(memory WITH (staircase stairstep stair stair-case stair-step)) AND L21 AND L23 AND L9	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO)); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/19 06:22 PM
L41	93	40 NOT ("2021" "2020" "2019").ay.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO)); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/19 06:22 PM
L42	280	(WL wordline word-line (word ADJ line) gate) WITH (highK high-K (high ADJ K)) AND (memory WITH (staircase stairstep stair stair-case stair-step))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO)); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/22 11:15 AM
L43	208	42 NOT ("2021" "2020" "2019").ay.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO)); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/22 11:15 AM
L44	5	("20150294980" "20170148677" "20140054789" "20190013237" "20140021632").pn.	(US-PGPUB; USPAT)	OR	ON	ON	2021/03/22 12:48 PM
L45	2	("20170148677"	(US-PGPUB; USPAT)	OR	ON	ON	2021/03/22

		"20190013237").pn.					02:22 PM
L46	2	45 AND anisotropic	(US-PGPUB; USPAT)	OR	ON	ON	2021/03/22 04:42 PM
L48	134	(L12 OR L13) AND ((etch-stop ESL) WITH (nitride oxynitride oxide))	(US-PGPUB; USPAT)	OR	ON	ON	2021/03/22 05:24 PM
L49	102	48 NOT ("2021" "2020" "2019").ay.	(US-PGPUB; USPAT)	OR	ON	ON	2021/03/22 05:25 PM
L50	147	(L12 OR L13) AND ((etch-stop ESL) WITH (nitride oxynitride oxide))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/22 05:25 PM
L51	115	49 NOT ("2021" "2020" "2019").ay.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/22 05:25 PM
L52	53	(L12 OR L13) AND ((etch-stop ESL) WITH ((hafnium ADJ oxide) (zirconium ADJ oxide) (aluminum ADJ oxide) (tantalum ADJ oxide) (lanthanum ADJ oxide)))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/22 05:44 PM
L53	31	52 NOT ("2021" "2020" "2019").ay.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/22 05:44 PM
L54	392	((etch-stop ESL) WITH ((hafnium ADJ oxide) (zirconium ADJ oxide) (aluminum ADJ oxide) (tantalum ADJ oxide) (lanthanum ADJ oxide)))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/22 05:45 PM
L55	32	54 AND (staircase stairstep stair stair-case stair-step)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/22 05:46 PM
L56	250	54 AND (memory)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/22 05:47 PM
L57	135	56 NOT ("2021" "2020"	(US-PGPUB; USPAT;	OR	ON	ON	2021/03/22

		"2019").ay.	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				05:47 PM
L58	53	L54 AND (L12 OR L13)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/22 05:47 PM
L59	31	58 NOT ("2021" "2020" "2019").ay.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/22 05:48 PM
L60	1	("20170117222").pn.	(US-PGPUB; USPAT)	OR	ON	ON	2021/03/22 05:50 PM
L61	38	(L12 OR L13) AND ((etch-stop ESL) WITH (depth dimension thick thickness) WITH (nm nms angstrom nanometer nanometre))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/22 06:19 PM
L62	18	61 NOT ("2021" "2020" "2019").ay.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/22 06:19 PM
L63	1014	((etch-stop ESL) WITH (depth dimension thick thickness) WITH (nm nms angstrom nanometer nanometre))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/22 06:20 PM
L64	311	((etch-stop ESL) WITH (depth dimension thick thickness) WITH (nm nms angstrom nanometer nanometre)) AND (memory)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/22 06:20 PM
L65	17	((etch-stop ESL) WITH (depth dimension thick thickness) WITH (nm nms angstrom nanometer nanometre)) AND (staircase stairstep stair stair-case stair-step)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/22 06:20 PM
L66	59	(L12 OR L13) AND ((etch-stop ESL) WITH (depth dimension thick thickness))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/22 06:22 PM
L67	38	66 NOT ("2021" "2020" "2019").ay.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/22 06:22 PM
L68	3	("20170148677" "20190013237" "20170117222").pn.	(US-PGPUB; USPAT)	OR	ON	ON	2021/03/22 06:25 PM

L70	5287	(L12 OR L13) AND (WL wordline word-line (word ADJ line)) WITH (silicon si poly-si polysi polysilicon ge germanium)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO)); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/22 07:11 PM
L71	1621	70 AND (remov\$3 WITH sacrificial)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO)); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/22 07:12 PM
L72	530	71 NOT ("2021" "2020" "2019" "2018" "2017").ay.	(US-PGPUB; USPAT)	OR	ON	ON	2021/03/22 07:12 PM
L73	266	71 NOT ("2021" "2020" "2019" "2018" "2017").ay.	(USPAT)	OR	ON	ON	2021/03/22 07:14 PM
L74	1059	70 AND (staircase stairstep stair stair-case stair-step)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO)); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/22 07:15 PM
L75	569	74 AND (remov\$3 WITH sacrificial)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO)); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/03/22 07:15 PM
L76	166	75 NOT ("2021" "2020" "2019" "2018" "2017").ay.	(US-PGPUB; USPAT)	OR	ON	ON	2021/03/22 07:15 PM
L82	5468	(L12 OR L13) AND L23	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO)); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/06/03 01:32 PM
L83	2342	(L12 OR L13) AND L23 AND L21	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO)); FPRS; EPO;	OR	ON	ON	2021/06/03 01:33 PM

			JPO; DERWENT; IBM_TDB)				
L84	498	(L12 OR L13) AND L23 AND L21 AND L9	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO)); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/06/03 01:34 PM
L86	136	L84 NOT ("2021" "2020" "2019" "2018" "2017").ay.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/06/03 01:35 PM
L88	912	(L12 OR L13) AND (((etch ADJ stop) etch- stop ESL) SAME (staircase stairstep stair stair-case stair-step step))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/06/03 01:37 PM
L89	98	L88 AND ((etch ADJ stop) etch-stop ESL) WITH ((hafnium ADJ oxide) (zirconium ADJ oxide) (aluminum ADJ oxide) (tantalum ADJ oxide) (lanthanum ADJ oxide) high-k hi-k (hi ADJ k) (high ADJ k))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/06/03 01:38 PM
L90	35	L89 NOT ("2021" "2020" "2019" "2018" "2017").ay.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/06/03 01:38 PM

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N1		(((etch ADJ stop) etch- stop ESL) WITH ((hafnium ADJ oxide) (zirconium ADJ oxide) (aluminum ADJ oxide) (tantalum ADJ oxide) (lanthanum ADJ oxide) high-k hi-k (hi ADJ k) (high ADJ k))).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2021/06/03 03:39 PM
N2		N1 AND (staircase stairstep stair stair-case stair-step step).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2021/06/03 03:40 PM

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STUDENT ASSOCIATE
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MYANG@STERNEKESSLER.COM



July 22, 2021

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 6601
Attn: Mail Stop Issue Fee

Re: Allowed U.S. Utility Patent Application
Appl. No. 16/865,056; Filed: May 1, 2020
For: **WORD LINE CONTACT STRUCTURE FOR THREE-
DIMENSIONAL MEMORY DEVICES AND FABRICATION
METHODS THEREOF**
First Named Inventor: Jifeng ZHU
Our Ref: 4123.0480003

Commissioner:

In response to the **Notice of Allowance and Fee(s) Due** dated **June 9, 2021**, the following documents are transmitted for appropriate action by the U.S. Patent and Trademark Office:

1. Issue Fee Transmittal (Form PTOL-85);
2. Online Credit Card Payment Authorization for \$1,200.00 to cover:
\$1,200.00 – Issue Fee; and
3. Comments on Statement of Reasons for Allowance.

The above-listed documents are filed electronically.

Fee payment is provided through online credit card payment.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Commissioner for Patents
July 22, 2021
Page 2

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Min Yang/

Min Yang
Agent for Applicant
Registration No. 78,149

M-Y/jcv
Enclosure(s)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26111 7590 06/09/2021
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1100 NEW YORK AVENUE, N.W.
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(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/865,056	05/01/2020	Jifeng ZHU	4123.0480003	6601

TITLE OF INVENTION: WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	09/09/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
GEYER, SCOTT B	2812	257-751000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

Sterne, Kessler, Goldstein
& Fox P.L.L.C.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

Yangtze Memory Technologies Co., Ltd.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Wuhan, Hubei, CHINA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

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☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 19-0036

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Min Yang/ Date 7/22/2021

Typed or printed name Min Yang Registration No. 78,149

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Jifeng ZHU

Confirmation No.: 6601

Applicant: YANGTZE MEMORY
TECHNOLOGIES CO., LTD.

Art Unit: 2812

Application No.: 16/865,056

Examiner: GEYER, SCOTT B.

Filing Date: May 1, 2020

Atty. Docket: 4123.0480003

Title: **WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY
DEVICES AND FABRICATION METHODS THEREOF**

Comments on Statement of Reasons for Allowance

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Mail Stop: Issue Fee

Commissioner:

Applicant thanks the Examiner for indicating the allowability of claims 1-5 and 8-20 in the Notice of Allowance dated June 9, 2021.

Comments on Statement of Reasons for Allowance

Applicant notes the Examiner's Statement of Reasons for Allowance presented on page 2 of the Notice of Allowance. Applicant reserves the right to demonstrate claims 1-5 and 8-20 are allowable over the art made of record for further reasons related to any of their recited features. Applicant further contends that reservation of this right does not give rise to any implication regarding whether the Applicant agrees with or acquiesces in the reasoning provided by the Examiner.

Jifeng ZHU
Application No. 16/865,056

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Min Yang/

Min Yang
Agent for Applicant
Registration No. 78,149

Date: 7/22/2021

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

17084728.1

Atty. Dkt. No. 4123.0480003

Electronic Patent Application Fee Transmittal				
Application Number:		16865056		
Filing Date:		01-May-2020		
Title of Invention:		WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		
First Named Inventor/Applicant Name:		Jifeng ZHU		
Filer:		Min Yang/Julia Vang		
Attorney Docket Number:		4123.0480003		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1200	1200

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1200

Electronic Acknowledgement Receipt	
EFS ID:	43319119
Application Number:	16865056
International Application Number:	
Confirmation Number:	6601
Title of Invention:	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF
First Named Inventor/Applicant Name:	Jifeng ZHU
Customer Number:	26111
Filer:	Min Yang/Julia Vang
Filer Authorized By:	Min Yang
Attorney Docket Number:	4123.0480003
Receipt Date:	22-JUL-2021
Filing Date:	01-MAY-2020
Time Stamp:	15:39:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 1200
RAM confirmation Number	E20217LF40083496
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	2021-07-22-Cover-Letter-4123-0480003.pdf	269293	no	2
			789f9f297330308bf0d045ecc98302a64fa5b6bf		
Warnings:					
Information:					
2	Issue Fee Payment (PTO-85B)	2021-07-22-Issue-Fee-4123-0480003.pdf	842187	no	1
			e36de670f6405a5911351676f0be3ce27c0121b1		
Warnings:					
Information:					
3	Post Allowance Communication - Incoming	2021-07-22-Comments-Statement-Reasons-for-Allowance-4123-0480003.pdf	133638	no	2
			4b31d03e31162aec8bb3cd2d3b956f1aac5f6876		
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30267	no	2
			ae3b18b5ee03204366509470322d2cf11338e151		
Warnings:					
Information:					
Total Files Size (in bytes):			1275385		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/865,056	08/24/2021	11101276	4123.0480003	6601

26111 7590 08/04/2021
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Jifeng ZHU, Wuhan, CHINA;
Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA;
Zhenyu LU, Wuhan, CHINA;
Jun CHEN, Wuhan, CHINA;
Si Ping HU, Wuhan, CHINA;
Xiaowang DAI, Wuhan, CHINA;
Lan YAO, Wuhan, CHINA;
Li Hong XIAO, Wuhan, CHINA;
A Man ZHENG, Wuhan, CHINA;
Kun BAO, Wuhan, CHINA;
Haohao YANG, Wuhan, CHINA;

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IR103 (Rev. 10/09)

Micron Ex. 1002, p. 156
Micron v. YMTC
IPR2025-00228



ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
16/865,056

RECEIPT DATE / TIME
07/03/2024 02:57:49 PM Z ET

ATTORNEY DOCKET #
4123.0480003

Title of Invention

WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND
FABRICATION METHODS THEREOF

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # 11101276

CONFIRMATION # 6601

FILED BY Hillary White

PATENT CENTER # 66231638

FILING DATE 05/01/2020

CUSTOMER # 26111

FIRST NAMED
INVENTOR Jifeng ZHU

CORRESPONDENCE
ADDRESS -

AUTHORIZED BY Mark Zimmerman

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
2017-00285-YMTC-PCT-US-DV1__POA.pdf	3	Power of Attorney	402 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
2017-00285-YMTC-PCT-US-DV1__POA.pdf	3523D9ACFAD7A36841096F612A79FFF90E04CA3BA504801370 C19F1A9509D912588B3A509A548B1C5ACAF39034AB6B3EA42 A4AB5C926B4B2DF502374679AD712

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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA/82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	16865056
Filing Date	May 01, 2020
First Named Inventor	Jifeng ZHU
Title	Word line contact structure for three-dimensional memory devices and fabrication methods thereof
Art Unit	2812
Examiner Name	SCOTT GEYER
Attorney Docket Number	2017-00285-YMTC-PCT-US-DV1

SIGNATURE of Applicant or Patent Practitioner

Signature	/Mark C. Zimmerman /	Date (Optional)	July 3, 2024
Name	Mark C. Zimmerman	Registration Number	44006
Title (if Applicant is a juristic entity)	Attorney for Applicant		
Applicant Name (if Applicant is a juristic entity)	Yangtze Memory Technologies Co., Ltd.		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

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*Total of _____ forms are submitted.

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I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number

Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)



I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

34431

OR



I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

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OR



The address associated with Customer Number:

OR



Firm or
Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Yangtze Memory Technologies Co., Ltd.



Inventor or Joint Inventor (title not required below)



Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)



Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)



Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

Name

Tuenlap Daniel Chan

Title

Deputy General Counsel, Head of Intellectual Property Department

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of

forms are submitted.

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