UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00228
U.S. Patent No. 11,101,276
Issue Date: August 24, 2021

Title: WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF

DECLARATION OF SANJAY BANERJEE, PH.D., IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 11,101,276

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1. [1.PRE] "A method for forming a semiconductor structure, comprising:" 58

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2. [1.A] "forming a staircase structure having a plurality of steps, wherein the forming of each step of the plurality of steps comprises disposing a sacrificial layer over a dielectric layer;" 59

3. [1.B] "disposing an etch-stop layer on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer;" 63

4. [1.C] "disposing an insulating layer on the etch-stop layer;" 65

5. [1.D] "replacing the sacrificial layer of each step with a gate stack, the gate stack comprising a conductive layer and a first high-k dielectric layer;" 67

6. [1.E] "forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer;" 70

7. [1.F] "etching the exposed portions of the etch-stop layer in the plurality of openings and exposing at least a portion of the conductive layer of each step; and" 73

8. [1.G] "forming a plurality of conductive structures in each of the plurality of openings." 76

C. Claim 2: 77

1. [2] "The method of claim 1, wherein the forming the plurality of openings comprises performing an etching process on the insulating layer, wherein an etching rate of the insulating layer is higher than an etching rate of the etch-stop layer." 77

D. Claim 4: 78

1. [4] "The method of claim 1, wherein etching the exposed portions of the etch-stop layer comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer of each step." 78

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E. Claim 5: 80

1. [5] "The method of claim 4, wherein etching the exposed portions of the etch-stop layer further comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the first high-k dielectric layer." 80

F. Claim 9: 82

1. [9] "The method of claim 1, further comprising: after disposing the insulating layer on the etch-stop layer, planarizing the insulating layer and the staircase structure by using chemical-mechanical-polishing (CMP)." 82

G. Claim 10: 84

1. [10] "The method of claim 1, wherein forming the plurality of conductive structures comprises disposing conductive materials inside the plurality of openings, the conductive materials directly on the exposed conductive layer of the each step." 84

H. Claim 11: 85

1. [11] "The method of claim 1, wherein forming the plurality of conductive structures further comprises planarizing the conductive materials and the insulating layer." 85

I. Claim 12: 87

1. [12] "The method of claim 1, wherein forming the staircase structure further comprises performing a repetitive etch-trim process on the sacrificial layers and the dielectric layers." 87

J. Claim 13: 89

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1. [13.PRE] "The method of claim 1, wherein replacing the sacrificial layer of each step with the gate stack comprises:" 89
2. [13.A] "forming a substrate opening through the staircase structure;" 90
3. [13.B] "removing the sacrificial layer of each step through the substrate; and" 91
4. [13.C] "disposing the first high-k dielectric layer and the conductive layer in place of the sacrificial layer." 92

K. Claim 14: 93

1. [14] "The method of claim 13, wherein disposing the first high-k dielectric layer comprises disposing hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide and/or any combination thereof." 93

L. Claim 15: 94

1. [15] "The method of claim 13, wherein disposing the conductive layer comprises disposing tungsten, cobalt, nickel, copper, aluminum, and/or any combination thereof." 94

M. Claim 16: 94

1. [16] "The method of claim 13, wherein disposing the conductive layer comprises disposing poly-crystalline silicon, poly-crystalline germanium, or poly-crystalline germanium-silicon." 94

N. Claim 17: 95

1. [17] "The method of claim 1, further comprising: prior to disposing the etch-stop layer, disposing a barrier layer on each step of the plurality of steps, wherein the barrier layer protects underlying structures during the etching of the exposed portions of the etch-stop layer." 95

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O. Claim 18: 97

1. [18] "The method of claim 17, wherein disposing the barrier layer comprises disposing one or more of silicon oxide, silicon oxynitride, silicon nitride, TEOS, aluminum oxide, and silicon oxide incorporated with F, C, N, or H." 97

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1. [1.B] "disposing an etch-stop layer on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer;" 98

B. Claim 3: 98

1. [3] "The method of claim 2, wherein the etching process comprises anisotropic dry etching." 98

C. Claim 6: 100

1. [6] "The method of claim 1, wherein disposing the etch-stop layer comprises disposing hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, and/or any combination thereof." 100

D. Claim 7: 101

1. [7] "The method of claim 1, wherein disposing the etch-stop layer comprises disposing the etch-stop layer with a thickness in a range between 10 nm to 100 nm." 101

E. Claim 8: 103

1. [8] "The method of claim 1, wherein disposing the etch-stop layer comprises performing chemical vapor deposition (CVD), physical vapor deposition (PVD), sputtering, atomic layer deposition (ALD), spin-coating, or any combination thereof." 103

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A. Claim 1: 111

1. [1.PRE] "A method for forming a semiconductor structure, comprising:" 111
2. [1.A] "forming a staircase structure having a plurality of steps, wherein the forming of each step of the plurality of steps comprises disposing a sacrificial layer over a dielectric layer;" 112
3. [1.B] "disposing an etch-stop layer on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer;" 116
4. [1.C] "disposing an insulating layer on the etch-stop layer;" 118
5. [1.D] "replacing the sacrificial layer of each step with a gate stack, the gate stack comprising a conductive layer and a first high-k dielectric layer;" 121
6. [1.E] "forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer;" 126
7. [1.F] "etching the exposed portions of the etch-stop layer in the plurality of openings and exposing at least a portion of the conductive layer of each step; and" 129
8. [1.G] "forming a plurality of conductive structures in each of the plurality of openings." 131

B. Claim 2: 134

1. [2] "The method of claim 1, wherein the forming the plurality of openings comprises performing an etching process on the insulating layer, wherein an etching rate of the insulating layer is higher than an etching rate of the etch-stop layer." 134

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C. Claim 3: 135

1. [3] "The method of claim 2, wherein the etching process comprises anisotropic dry etching."....135

D. Claim 4: 136

1. [4] "The method of claim 1, wherein etching the exposed portions of the etch-stop layer comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer of each step."....136

E. Claim 5: 139

1. [5] "The method of claim 4, wherein etching the exposed portions of the etch-stop layer further comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the first high-k dielectric layer."....139

F. Claim 6: 140

1. [6] "The method of claim 1, wherein disposing the etch-stop layer comprises disposing hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, and/or any combination thereof." 140

G. Claim 7: 140

1. [7] "The method of claim 1, wherein disposing the etch-stop layer comprises disposing the etch-stop layer with a thickness in a range between 10 nm to 100 nm." 140

H. Claim 8: 141

1. [8] "The method of claim 1, wherein disposing the etch-stop layer comprises performing chemical vapor deposition (CVD), physical vapor deposition (PVD), sputtering, atomic layer deposition (ALD), spin-coating, or any combination thereof." 141

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I. Claim 9: 142

1. [9] "The method of claim 1, further comprising: after disposing the insulating layer on the etch-stop layer, planarizing the insulating layer and the staircase structure by using chemical-mechanical-polishing (CMP)." 142

J. Claim 10: 143

1. [10] "The method of claim 1, wherein forming the plurality of conductive structures comprises disposing conductive materials inside the plurality of openings, the conductive materials directly on the exposed conductive layer of the each step." 143

K. Claim 11: 145

1. [11] "The method of claim 1, wherein forming the plurality of conductive structures further comprises planarizing the conductive materials and the insulating layer." 145

L. Claim 12: 147

1. [12] "The method of claim 1, wherein forming the staircase structure further comprises performing a repetitive etch-trim process on the sacrificial layers and the dielectric layers." 147

M. Claim 13: 148

1. [13.PRE] "The method of claim 1, wherein replacing the sacrificial layer of each step with the gate stack comprises:" 148

2. [13.A] "forming a substrate opening through the staircase structure;" 148

3. [13.B] "removing the sacrificial layer of each step through the substrate; and" 149

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4. [13.C] "disposing the first high-k dielectric layer and the conductive layer in place of the sacrificial layer." 151

N. Claim 14: 152

1. [14] "The method of claim 13, wherein disposing the first high-k dielectric layer comprises disposing hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide and/or any combination thereof." 152

O. Claim 15: 152

1. [15] "The method of claim 13, wherein disposing the conductive layer comprises disposing tungsten, cobalt, nickel, copper, aluminum, and/or any combination thereof."....152

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A. Claim 17: 155

1. [17] "The method of claim 1, further comprising: prior to disposing the etch-stop layer, disposing a barrier layer on each step of the plurality of steps, wherein the barrier layer protects underlying structures during the etching of the exposed portions of the etch-stop layer."....155

B. Claim 18: 157

1. [18] "The method of claim 17, wherein disposing the barrier layer comprises disposing one or more of silicon oxide, silicon oxynitride, silicon nitride, TEOS, aluminum oxide, and silicon oxide incorporated with F, C, N, or H." 157

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I, Sanjay Banerjee, hereby declare as follows:

I. INTRODUCTION

1. My name is Sanjay Banerjee. I have been retained on behalf of Petitioner Micron Technology, Inc. ("Micron") to provide this Declaration concerning technical subject matter relevant to the *inter partes* review petition ("Petition") concerning U.S. Patent No. 11,101,276 (Ex. 1001, the "'276 Patent").

2. In the preparation of this Declaration, I have confined my analysis to the materials and opinions that were available at the time of the preparation of this Declaration. I reserve the right to supplement this Declaration in response to additional evidence that may come to light.

3. If requested, I am prepared to explain (in a deposition or at a trial before the Patent Trial and Appeal Board (the "Board")) the technology disclosed in the '276 Patent—including the state of the art in the relevant timeframe. Similarly, I am prepared to explain the technology disclosed in the Kim (Ex. 1005, U.S. Patent Publication Number 2012/0070944A1), Fang (Ex. 1006, U.S. Patent Publication Number 2019/0067306A1), Han (Ex. 1007, U.S. Patent Publication Number 2017/0062470A1), and Chen (Ex. 1008, U.S. Patent Publication No. 2017/0294384A1) references, and in any other prior art references cited herein. This may include, among other things, background information on 3D NAND technology.

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4. I am over 18 years of age and competent to testify to the matters addressed in this Declaration.

II. QUALIFICATIONS

5. I currently serve as the Cockrell Family Regents Chair Professor of Electrical and Computer Engineering and Director of the Microelectronics Research Center at the University of Texas at Austin ("UT"). Prior to this position, I was first an Assistant Professor (September 1987-August 1990) and later an Associate Professor (September 1990-August 1993) at UT, before being named a Professor in September 1993. Prior to starting my academic work at UT, I was a member of the technical staff at Texas Instruments (Corporate R&D) from the time I completed my doctoral studies in 1983 until August 1987. I worked on vertical 3D Dynamic Random Access Memory (DRAM) cells (see S. Banerjee and M. Bordelon, "A Model for the Trench Transistor," IEEE Trans. Elec. Dev., 34 (12), 2485-2493, December 1987).

6. In addition to my academic work at UT, I was also the Director of the South West Academy of Nanoelectronics, one of three centers created by the Semiconductor Research Corporation Nanoelectronics Research Initiative in 2006 to research and develop a replacement for conventional metal oxide semiconductor field effect transistors ("MOSFETs") during the entire program.

7. I received my Ph.D. in Electrical Engineering from the University of

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Illinois in 1983. I also received an M.S. in Electrical Engineering from the University of Illinois in 1981. I received a B. Tech. in Electronics from the Indian Institute of Technology at Kharagpur in 1979.

8. As described in my CV (Ex. 1004), I have more than 40 years of experience in the field of electrical engineering, including extensive experience in semiconductor development and fabrication including that of 3-Dimensional Dynamic Random Access Memory ("DRAM") cells, MOSFETs, flash memory, and beyond-complementary metal-oxide-semiconductor ("CMOS") transistors. My work in these fields has resulted in thirty-five United States patents related to methods of forming polysilicon and novel transistors, flash memory, and vertical DRAM cells. I have been elected a Fellow of the National Academy of Inventors.

9. Much of my research and experience has related to methods for MOSFET fabrication and design, including deposition of thin films by chemical vapor deposition (CVD), atomic layer deposition (ALD), physical vapor deposition (PVD), patterning using photolithography and etching using plasma-based Reactive Ion Etching (RIE) which are some of the processing techniques used to make 3D NAND flash. I have worked extensively on polysilicon thin film transistors similar to the ones used in the channel of NAND flash memory cells, high-k and other dielectrics used for charge storage, and for tunneling. A number of the sponsored research grants on which I have been a principal or coinvestigator have related to

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chemical deposition methods and/or ultra-shallow source/drain junction technology, including "Transport in MOSFETs" (Motorola, August 1993-August 1994), "Ultra Shallow Junction Technology" (SEMATECH January 1994-December 1996), and "Vertical Si-Ge-C MOSFETS" (Semiconductor Research Corporation September 2000-August 2003). In addition, I am an author on over forty publications relating to flash memory cells, including vertical 3D memory that can be used in NAND flash (e.g., Sarkar J, Dey S, Shahrjerdi D, Banerjee SK, Vertical Flash memory cell with nanocrystal floating gate for ultradense integration and good retention, IEEE ELECTRON DEVICE LETTERS 28 (5): 449-451 MAY 2007.) One of my papers on flash memory was given a Best Paper Award by the SRC.

10. I am a Fellow of the Institute of Electrical and Electronics Engineers ("IEEE"), the American Physical Society ("APS"), and the American Association for the Advancement of Science ("AAAS"). I have served on numerous professional and government committees in the electrical engineering field, including chairing multiple IEEE committees, meetings, and programs, serving on Morgan & Claypool's editorial board, and serving as a member on the International Technology Roadmap for Semiconductors ("ITRS").

11. I have taught courses in Semiconductor Physics, Solid State Electronic Devices, and Microelectronic and VLSI Device Fabrication at UT. In addition, I have delivered many courses to industry on Semiconductor Devices and Memory

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and Semiconductor Processing. I have taught courses that cover 3D memories, such as 3D NAND (Ultra Large Scale Integration Techniques and Solid State Electronic Devices). As a principal investigator, I have been the advisor to over 80 Doctoral and Masters students.

12. I am the co-author of several books and invited book chapters covering the area of electronic and semiconductor devices, including: Dopant Diffusion, Solid State Electronic Devices (three editions), Silicon-germanium Devices, and Novel 3D CMOS. I have authored or co-authored more than 1,000 papers and presentations in the areas of semiconductor devices and electronics development over the course of my career.

13. I have been the recipient of fifty grants to fund my research from a variety of funding agencies including the National Science Foundation ("NSF"), DARPA, the Department of Energy, Semiconductor Research Corporation, the Department of Defense-Multidisciplinary University Research Initiative, and the Office of Naval Research.

14. I have received numerous awards for my work, including the NSF Presidential Young Investigator Award. The NSF Presidential Young Investigator Award was [1] a highly competitive honor and grant bestowed annually upon

[1] The NSF Presidential Young Investigator Award was an award given out by the

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recognized young academic leaders in science and engineering. I have received numerous other awards, including some the highest honors for semiconductor devices such as the Andrew Grove Award from the IEEE, and the Semiconductor Industry Association/Semiconductor Research Corporation University Researcher Award, for my work in semiconductor memory and transistors, which are described in more detail in my CV (Ex. 1004).

III. COMPENSATION

15. I am being compensated for my work in this matter at an hourly rate of $650.00 for consulting services. My compensation is not based on the outcome of this matter or on the substance of my opinions.

IV. MATERIALS CONSIDERED

16. In preparing this declaration, I reviewed and considered the following materials, along with any other materials referenced in the body of my declaration:

EXHIBIT NO.	DESCRIPTION
1001	U.S. Patent No. 11,101,276 to Zhu et al. ("the '276 Patent")
1002	File History of U.S. Patent No. 11,101,276 ("the '276 FH")
1005	U.S. Patent Publication No. 2012/0070944A1 ("Kim")

NSF until 1991, at which time it was replaced with the NSF Young Investigator Awards and Presidential Faculty Fellows Program.

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EXHIBIT NO.	DESCRIPTION
1006	U.S. Patent Publication No. 2019/0067306A1 ("Fang")
1007	U.S. Patent Publication No. 2017/0062470A1 ("Han")
1008	U.S. Patent Publication No. 2017/0294384A1 ("Chen")
1009	U.S. Patent Publication No. 2018/0330985A1 ("Yu")
1010	Aritome, "NAND Flash Memory Technologies" (2016)
1011	Silvagni, "3D NAND Flash Based on Planar Cells," Computers 2017
1012	Micheloni et al., "Inside Solid State Drives (SSDs)" (2nd Ed. 2018)
1013	U.S. Patent Publication No. 2017/0117222A1 to Kim et al.
1014	Chang and Sze, "ULSI Technology" (1996)
1015	Orlowski et al., *Si, SiGe, Ge, and III-V Semiconductor Nanomembranes and Nanowires Enabled by SiGe Epitaxy*, ECS Transactions Vo. 33, No. 6 (2010), 777-89
1016	U.S. Patent No. 9,728,547 ("Ohsaki")
1017	U.S. Patent Publication No. 2017/0148677A1 ("Shin")
1018	U.S. Patent No. 10,672,711 to Zhu et al. ("the '711 patent")
1019	Excerpt from YMTC's Exemplary Infringement Claim Chart for U.S. Patent No. 11,101,276 (Ex. H-1 to Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024) ("YMTC2 Infringement Contentions, Ex. H-1") [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]
1020	Korean Patent Publication Number KR10-2013-0015120 ("Lee")

EXHIBIT NO.	DESCRIPTION
1021	Wolf S., et al., "Silicon Processing for the VLSI Era, Volume 1 – Process Technology, Chapter 15, Multilevel Interconnects for ULSI," (2nd Ed. 2000)
1022	CN Patent Publication No. 107658309 A with certified translation (Priority application to the '276 Patent)
1023	Wang, et al., "Low DC-Bias Silicon Nitride Anisotropic Etching," Journal of Vacuum Science & Technology B, Vol. 33, Issue 6 (Sept. 10, 2015)
1024	U.S. Patent Publication No. 2014/0284661A1 ("Williams")
1025	Shamiryan D., et al., "Selective Removal of High-K Gate Dielectrics," Chemical Engineering Communications (2009)
1026	Morel, et al., "Tungsten metal gate etching in Cl2/O2 inductively coupled high density plasmas," Journal of Vacuum Science and Technology B (Nov. 3, 2008)
1027	Kim, et al., "Dry Etching of High-k Dielectric Thin Films in HBr/Ar Plasma," Journal of the Korean Physical Society, Vol. 54, No. 2, pp. 934-38 (February 2009)
1028	U.S. Patent No. 10,297,543 to Park et al.

V. UNDERSTANDING OF THE GOVERNING LAW

17. I am not an attorney but have been instructed in and applied the law as described in this section.

A. Claim Construction

18. I understand that the first step in determining whether a patent claim would have been anticipated or obvious is to ascertain how a person of ordinary skill

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in the art ("POSITA") would have understood the claim terms.

19. I have been instructed by counsel on the law regarding claim construction and patent claims, and I understand that a patent may include two types of claims: independent claims and dependent claims. An independent claim stands alone and includes only the limitations it recites. A dependent claim can depend from an independent claim, or it can further depend from another dependent claim. I understand that a dependent claim includes all the limitations that it recites, in addition to all the limitations recited in the claim(s) from which it depends.

20. It is my understanding that in proceedings before the USPTO, the claims of a patent are to be construed under what is referred to as the "*Phillips* standard." I understand that this means that claim terms of a patent are given the ordinary and customary meaning they would have to a POSITA in view of the description provided in the patent itself and the patent's file history.

21. I understand that to determine how a person of ordinary skill would understand a claim term, one should look to those sources available that show what a person of skill in the art would have understood the disputed claim language to mean. I understand that, in construing a claim term, one looks primarily to the intrinsic patent evidence, including the words of the claims themselves, the patent specification, and the patent's prosecution history. I understand that extrinsic evidence, which is evidence external to the patent and the prosecution history, may

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also be useful in interpreting patent claims when the intrinsic evidence itself is insufficient.

22. I understand that words or terms should be given their ordinary and accepted meaning unless it clearly appears that the inventors were using them to mean something else. In making this determination, the claims, the remainder of the patent, and the prosecution history are of paramount importance. Additionally, the patent and its prosecution history must be consulted to confirm whether the patentee has acted as its own lexicographer (i.e., provided its own special meaning to any disputed terms) or intentionally disclaimed, disavowed, or surrendered any claim scope.

23. I further understand that in proceedings before the Board, claim terms need only be construed to the extent necessary to resolve any controversy that may arise.

24. In comparing the claims of the ’276 Patent to the prior art, I have considered the ’276 Patent and its file history in light of the understanding of a POSITA at the time of the alleged invention. I address further how a POSITA would have understood the claims of the alleged invention in §X.

B. Obviousness

25. I have been further instructed and understand that a patent claim is unpatentable and invalid as obvious if the subject matter of the claim as a whole

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would have been obvious under 35 U.S.C. §103(a) to a person of ordinary skill in the art of the claimed subject matter as of the time of the invention at issue. I understand that when assessing the obviousness of claimed subject matter, the following factors are evaluated: (1) the scope and content of the prior art; (2) the difference or differences between each claim of the patent and the prior art; and (3) the level of ordinary skill in the art at the time the patent was filed. I also understand that the Board considers certain objective factors if they are present, generally referred to as "secondary considerations" or "objective indicia" of non-obviousness, as further discussed below in this section.

26. I have been informed that there are two ways to determine whether prior art is analogous and thus can be considered prior art: (1) whether the art is from the same field of endeavor, regardless of the problem addressed, and (2) if the reference is not within the field of the patentee's endeavor, whether the reference still is reasonably pertinent to the particular problem with which the patentee is involved. I have also been informed that the field of endeavor of a patent is not limited to the specific point of novelty, the narrowest possible conception of the field, or the particular focus within a given field. I have also been informed that a reference is reasonably pertinent if, even though it may be in a different field from that of the patentee's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to a patentee's attention in considering his

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or her problem.

27. I understand that claimed subject matter may be obvious in view of more than one item of prior art. I understand, however, that it is not enough to show simply that all the limitations of the claimed subject matter are spread throughout the prior art. Instead, for claimed subject matter to be obvious over multiple references, there generally must have been some reason or motivation for one of ordinary skill in the art to combine the teachings of the prior art references to arrive at the claimed subject matter.

28. I have been informed that, in seeking to determine whether an invention that is a combination of known elements would have been obvious to a person of ordinary skill in the art at the time of the invention, one must consider the references in their entirety to ascertain whether the disclosures in those references render the combination obvious to such a person.

29. I have been informed and understand that, while not required, the prior art references themselves may provide a teaching, suggestion, motivation, or reason to combine, but that other times the motivation linking two or more prior art references is common sense to a POSITA at the time of the invention.

30. I understand that a particular combination may be proven obvious merely by showing that it was obvious to try the combination. I have been informed that, if a technique has been used to improve one device, and a person of ordinary

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skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. I have further been informed and understand that a POSITA combines the teachings of the prior art references and does not necessarily combine the embodiments of those teachings physically.

31. I further understand that an obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references also may be supplied by the direction of the marketplace. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

32. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. Thus, where all of the elements of a claim are used in substantially the same manner in devices in the same field of endeavor, the claim is likely obvious.

33. Additionally, I understand that a patent is likely to be invalid for obviousness if a person of ordinary skill can implement a predictable variation or if

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there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. Therefore, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.

34. I further understand that combining embodiments related to each other in a single prior art reference would not ordinarily require a leap of inventiveness.

35. I also understand that one of ordinary skill in the art must have had a reasonable expectation of success when combining references for claimed subject matter to be obvious.

36. I have been informed and I understand that factors referred to as "objective indicia of non-obviousness" or "secondary considerations" are also to be considered when assessing obviousness when such evidence is available. I understand that these factors can include: (1) commercial success; (2) long-felt but unresolved needs; (3) copying of the invention by others in the field; (4) initial expressions of disbelief by experts in the field; (5) failure of others to solve the problem the claimed subject matter solved; and (6) unexpected results.

37. I also understand that evidence of objective indicia of non-obviousness must be commensurate in scope with the claimed subject matter. I further understand that there must be a relationship, sometimes referred to as a "nexus," between any such secondary indicia and the claimed invention. I also have been

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informed that even when they are present, secondary considerations may be unable to overcome primary evidence of obviousness (e.g., motivation to combine with predictable results) that is sufficiently strong.

38. Finally, I have been informed that one cannot use hindsight to determine that an invention was obvious.

39. I provide my opinions in this Declaration based on the guidelines set forth above.

VI. LEVEL OF SKILL IN THE ART

40. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA may have for combining references.

41. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the relevant field. I have been further informed and understand that a POSITA is also a person of ordinary creativity.

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42. In my opinion, a POSITA in the field of the '276 Patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (*e.g.*, researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience). This POSITA would have been aware of and generally knowledgeable about the structure of 3D NAND, how it is manufactured, and its component parts.

43. In view of my educational background and work experience, I am a person of more than the ordinary level of skill in the art of the '276 Patent and was so by August 31, 2017. In forming my opinions, I have drawn on my academic background and professional experiences. In forming my opinions herein, however, I took into account the perspective of a POSITA.

VII. THE '276 PATENT'S EFFECTIVE FILING DATE

44. I understand that the application leading to the '276 Patent was filed on May 1, 2020. I further understand that the patent claims priority to a an earlier-filed PCT publication No. PCT/CN2018/101308, filed on August 20, 2018, and further to a Chinese patent application 201710774754, filed on August 31, 2017. Ex. 1001, Cover.

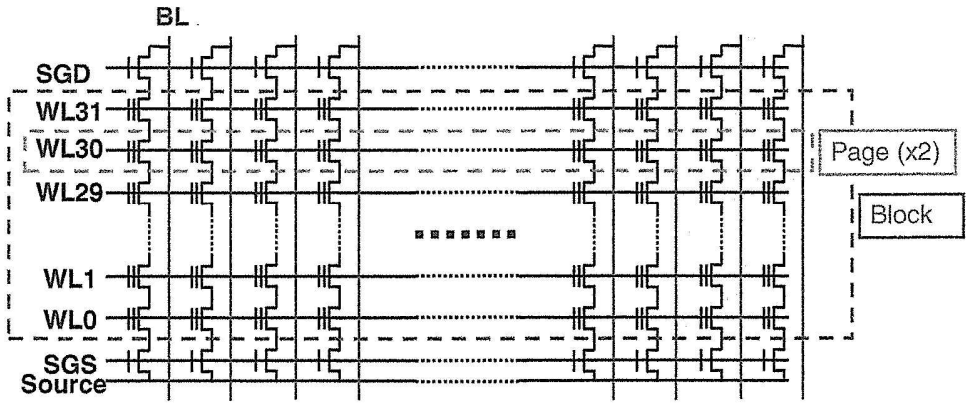
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45. For purposes of this declaration, I have been instructed to use August 31, 2017 as the priority date of the '276 Patent. My opinions in this declaration were formed from the perspective of a POSITA as of August 31, 2017, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the prior art.

VIII. TECHNOLOGY BACKGROUND

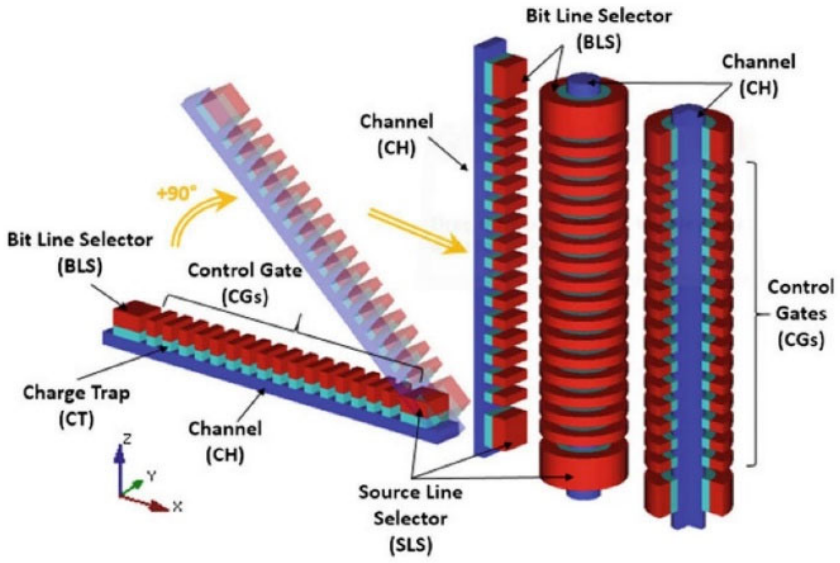
46. The '276 Patent and the prior art references discussed in this Declaration relate to methods of fabricating three-dimensional (3D) memory devices, such as 3D NAND memory devices.

47. Central to NAND memory devices is a "memory cell," which stores information as electrical charge. In these devices, NAND memory cells are arranged in "strings" having multiple cells "connected in series." Ex. 1010, 38. Early NAND memory devices were formed as two-dimensional arrays of cells on a substrate surface. *Id.*, 58.

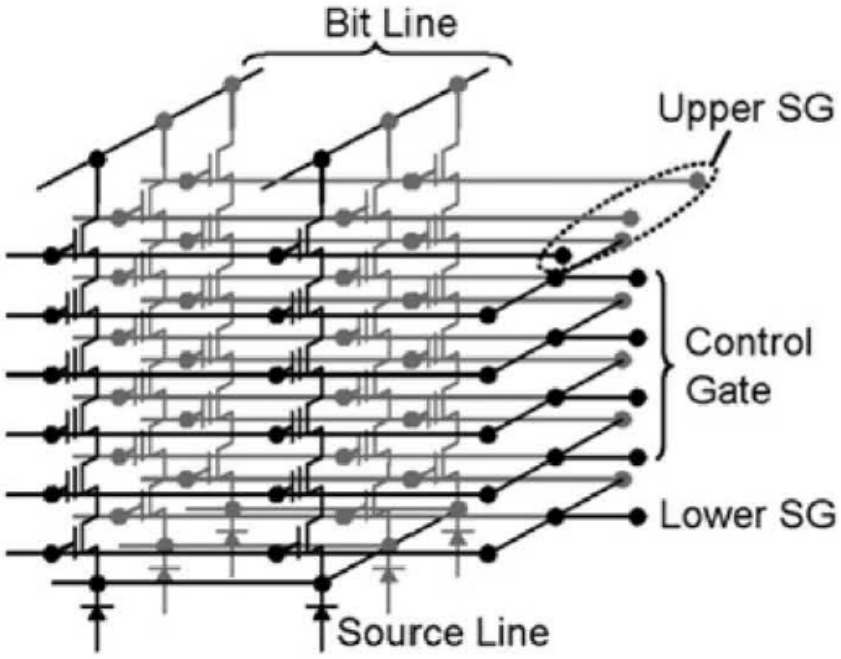


Ex. 1010, 40.

48. "[T]o further scale down the memory cell size," "three-dimensional (3D) NAND flash cells" were developed. *Id.*, 292. "Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block" and "turning the 2D NAND string upside," "resulting" in a "3D structure" with a "vertical channel." Ex. 1011, 3.



Ex. 1012, 122 (colors in the original). Multiple such vertical channels are repeated in a three-dimensional array:

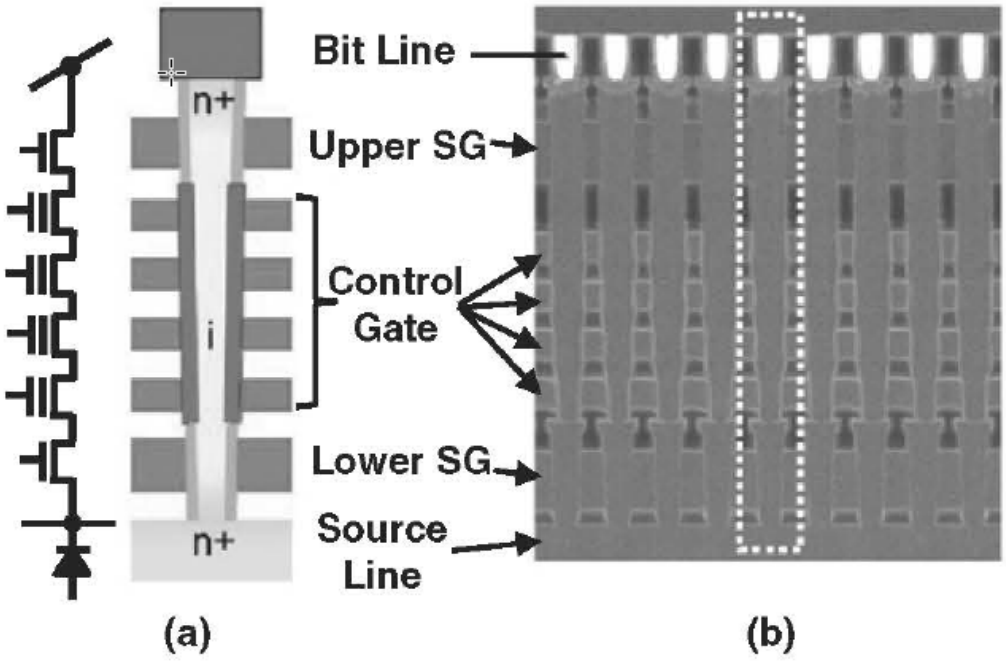


Ex. 1010, 296. A voltage applied on the control gate (which is also known as the word line) of each cell and the information stored in the cell (*e.g.*, binary 0 or 1 for a one-bit memory cell) determine whether the cell turns on or off. Specifically, the electrical charge (representing information) stored in the cell determines a threshold voltage of the cell, and the cell turns on when the control gate voltage is greater than the threshold voltage. Electrical current can only flow through a string when all cells in the string are turned on. Therefore, by applying a control gate voltage sufficient to turn on all but one cell (the selected cell) in a string and applying a suitable voltage to the control gate of the selected cell, the information stored in the selected cell may be determined using the amount of current flow through the string. This process is

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repeated by selecting a different cell to read (as an example operation) in the next cycle, eventually retrieving the requested information from the cells that store it.

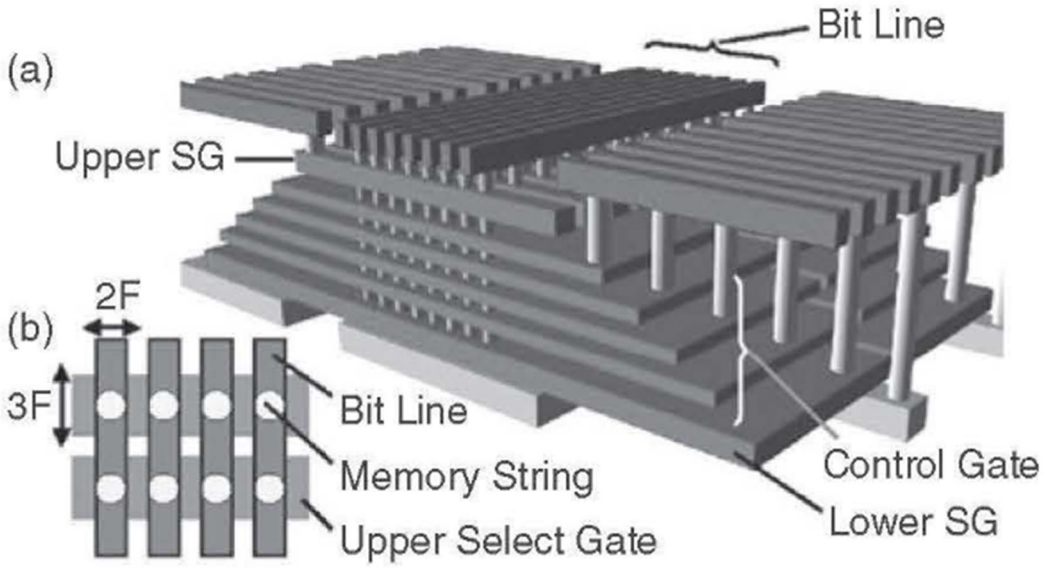
49. A particular vertical memory cell "string is selected by a bit line and an upper select gate (upper SG)." Ex. 1010, 295-96. A memory cell "is located in the intersection of a control gate plate" and the channel of the string. *Id.* The lowest layer is a "select gate (lower SG)," which allows the strings to connect to a lower "common source." *Id.*, 295, 297. An example 3D NAND vertical memory cell string is shown below:



Ex. 1010, 296.

50. 3D NAND memory devices include "multi-stacked layers of [control] gate (plate)" material alternated with "dielectric" (insulator of direct current) in a

"[s]tack." Ex. 1010, 294. A "through-hole[]" channel (which is also known as a channel structure) "filled by memory film … and channel poly-Si" passes through the layers to form a string of vertically arranged memory cells. *Id.*, 295. "Each" layer of "electrode plate acts as a control gate." *Id.* "[T]he control gates … are connected … [in a] stair-like gate structure." *Id.*, 295-97.



Ex. 1010, 296 (Fig. 7.6). Vertical conductive structures couple the control gates to control voltages. The steps of the staircase structure provide landing areas for the vertical conductive structures to contact the control gates. *Id.*, 298.

51. As can be seen in the figure above, the vertical conductive structures contacting the different control gate plates have different lengths because the landing areas of the plates are located at different heights. The '276 Patent and the prior art references relate to the technology of fabricating these vertical conductive structures

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in a reliable and cost-effective manner.

52. The vertical conductive structures are formed by etching holes through an insulating layer above the staircase structure and depositing a conductive material inside the holes. Etching can be done using various techniques and involves an etchant. Different materials react to an etchant differently and an etching rate is used to characterize how fast or slow an etchant etches through a particular material. On the flip side, a material also can react differently to different etchants. For example, a material may have a high etching rate for one etchant and a low etching rate for a different etchant.

53. Because the conductive structures need to have different lengths and so the holes need to be etched to different depths, techniques were developed to etch holes to their respective lengths. The ’276 Patent mentions one such prior art technique. Ex. 1001, 5:58-60. Another prior art technique is to place one or more etch-stop layers above the staircase structure. The etch-stop layers have a lower etching rate than the insulating layer for the etchant used to penetrate the insulating layer. Therefore, when etching reaches the etch-stop layers, etching slows down. This protects the underlying layers and prevents over-etching shallower holes while etching deeper holes. Ex. 1006, [0008], [0028]. One prior art reference illustrates this through the following sequence of figures:

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FIG. 24

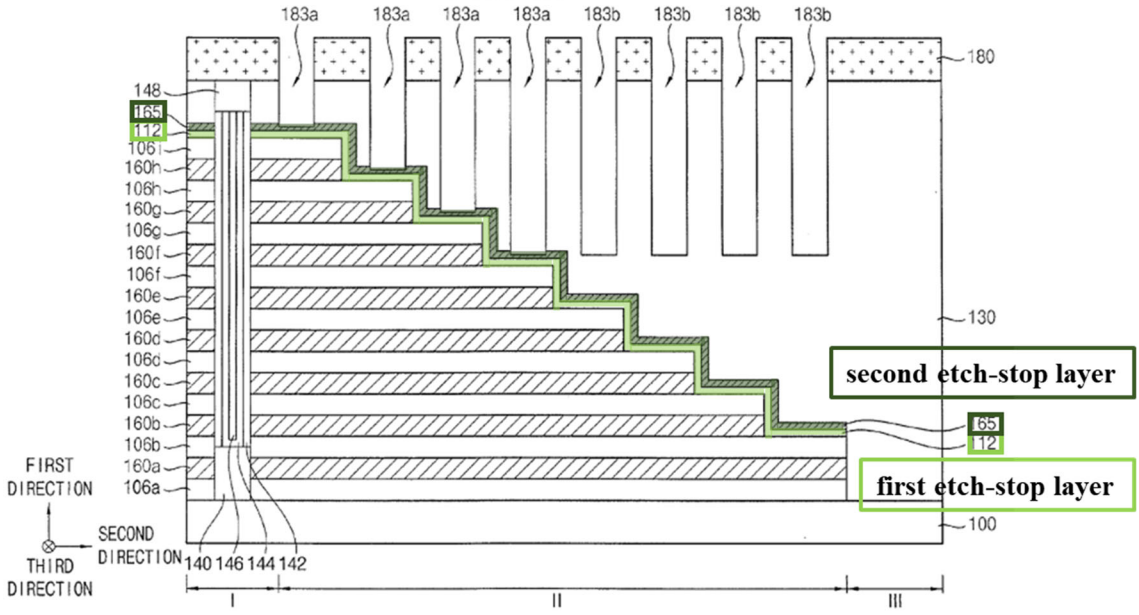
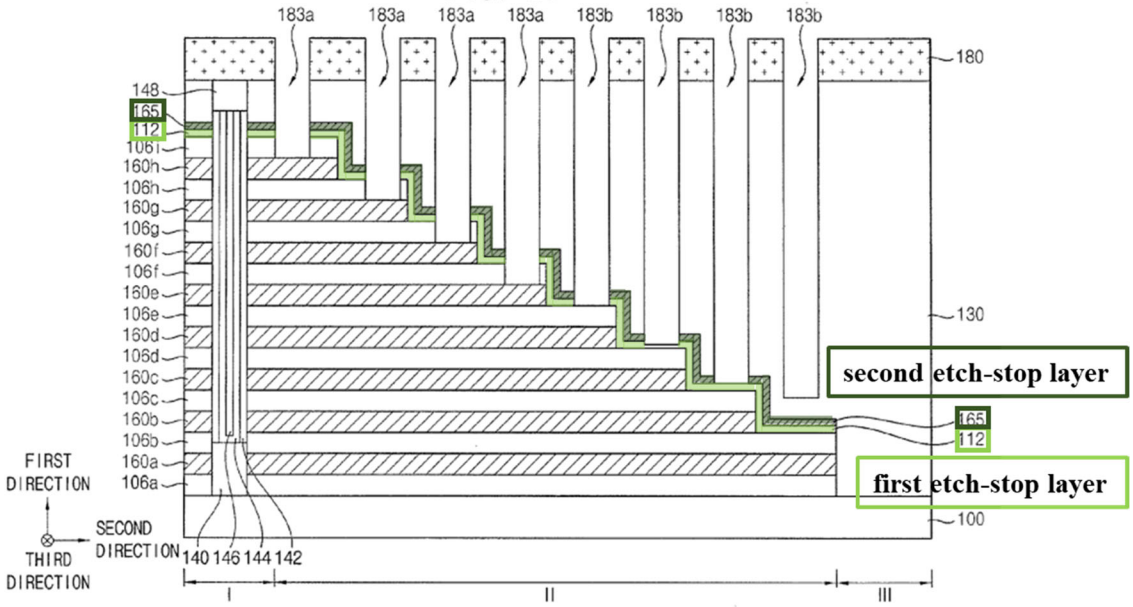
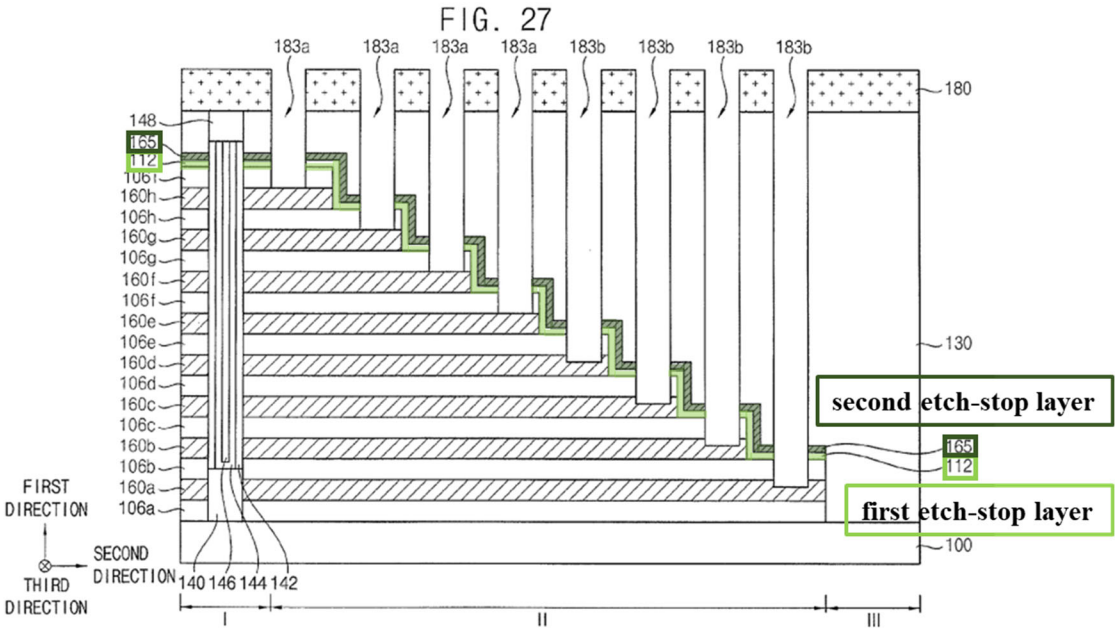

183a
183b
180
148
165
112
160h
106h
160g
106g
160f
106f
160e
106e
160d
106d
160c
106c
160b
106b
160a
106a
130
second etch-stop layer
65
112
first etch-stop layer
100
FIRST DIRECTION
SECOND DIRECTION
THIRD DIRECTION
140 146 144 142
I
II
III

FIG. 26


183a
183b
180
148
165
112
160h
106h
160g
106g
160f
106f
160e
106e
160d
106d
160c
106c
160b
106b
160a
106a
130
second etch-stop layer
165
112
first etch-stop layer
100
FIRST DIRECTION
SECOND DIRECTION
THIRD DIRECTION
140 146 144 142
I
II
III



Ex. 1013, Figs. 24, 26-27.[2] As shown in Figure 24, etching slows down when it reaches an etch-stop layer such that the four contact holes 183a on the left, each having a different depth from the others, do not penetrate the second etch-stop layer 165. *Id.*, [0113]-[0116]. Then a second etching process is used to etch the second etch-stop layer 165. *Id.*, [0117]. This can also increase the depths of the contact holes 183b (on the right). *Id.*, [0118]. Then a third etching process can be used to further increase the lengths of the contact holes, as shown in Figure 26. *Id.*, [0119]-[0121]. Finally, a fourth etching process can further increase the depths of contact holes 183b. *Id.*, [0122]. Using the etch-stop layers allows the contact

[2] From this point forward, all color annotations in this Declaration are added except where noted otherwise.

holes of different depths be formed "without defects such as a punching or a not-open failure of the gate lines." *Id.*, [0124]. Of course, this sequence is merely an example. Other etching sequences can be used as was within the ability of a POSITA.

54. More generally speaking, a layer ("layer 2") functions as an etch-stop layer when its etching rate is lower than the etching rate of the layer immediately above ("layer 1"). This is known as selective etching and is based on the relative etching rates of materials in the layers. Ex. 1014, 220, 390. Etch selectivity (the ratio of etching rates of one layer relative to another layer) implies that layers 1 and 2 cannot be made from the same material if layer 2 is to function as an etch stop because the same material will have the same etching rate. As explained above, etch selectivity is determined by the etchant used. Accordingly, layer 1 may have a higher etching rate than layer 2 when one type of etchant is used, but a lower etching rate than layer 2 when a different type of etchant is used. These conventional processes were known as "selective etching" and "reverse selective etching." Ex. 1015, 4, 6 (internal quotation marks omitted). Using different etchants allows greater flexibility in the choices of materials to use as an etch stop. For example, the materials of two layers may be swapped and using a different etchant can still allow the upper layer to function as an etch stop to the lower layer. Other factors in determining the required selectivity of the etch rates are the thickness variability of

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various layers and the random variability of etching rates of a particular material due to etchant concentration variability in the etching tool, etc. It is necessary to account for the worst-case scenario where in some locations the thinner layers etch faster, while in other locations the thicker layers etch slower. This can lead to unintentional over-etching in certain locations and punching through the word lines, potentially resulting in short circuits, or under-etching in some other locations, potentially resulting in open circuits. The "barrier layer" in the '276 Patent is effectively a second etch-stop layer. The use of two etch-stop layers provides additional flexibility in the process and guards against such problems because each layer can be specifically configured to slow down etching when etching penetrates the respective layer above and reaches each etch-stop layer, thereby protecting the underlying layers.

55. An etch stop may be somewhat of a misnomer because etching slows down (perhaps significantly) but does not truly stop. In other words, etching rate of a material can be very small but is not zero.

IX. THE '276 PATENT AND ITS PROSECUTION HISTORY

56. The '276 Patent describes 3D memory structures and their fabrication. More specifically, it relates to forming "word line contact structures" on a staircase structure. Ex. 1001, Abstract. As shown below, the word line contact structure is the landing area in which a vertical conductive structure 945 makes contact with a

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particular step. The landing area is also commonly referred to as the step, because it is the step in the staircase. And the conductive structure is also commonly referred to as a staircase contact, because it is the contact to the step of the staircase. The '276 Patent discloses a conventional staircase structure 900 with alternating gate stacks 525 and dielectric layers 104:

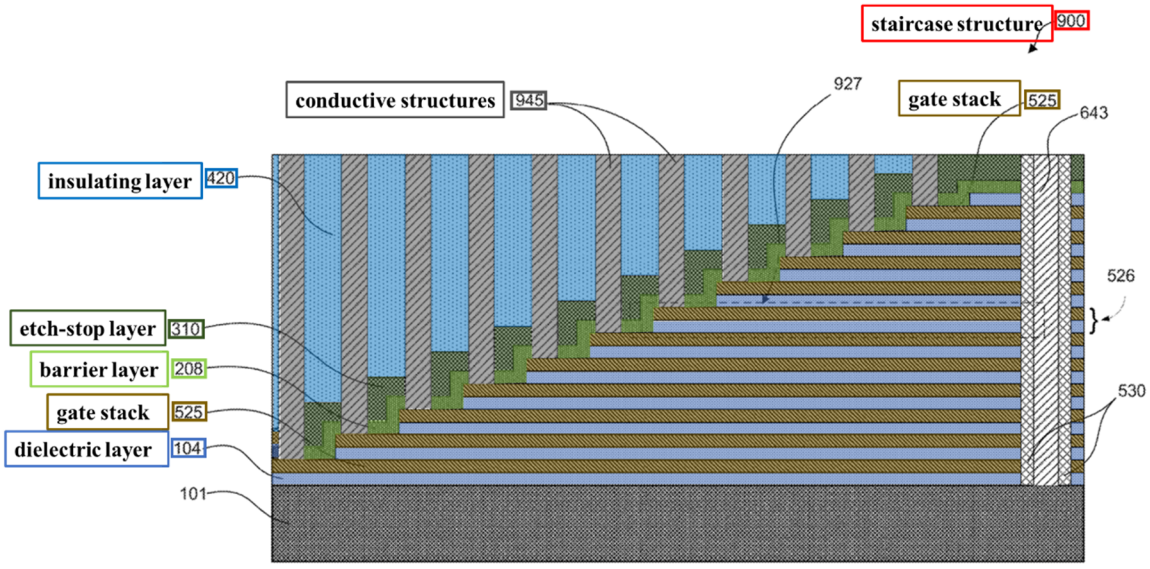


FIG. 9A

Id., Fig. 9A; 8:60-61. As also shown, an optional barrier layer 208 and an etch-stop layer 310 cover the side surface and a portion of the top surface of each step. *Id.*, 5:61-6:5, 7:36-45, 7:62-64, 8:5-9. These coverages are more apparent in Figures 2 and 3, which show the formation of these two layers before the vertical conductive structures are formed. An insulating layer 420 is disposed on the etch-stop layer 310. *Id.*, Fig. 4. Conductive structures 945 (commonly known as staircase contacts) penetrate the insulating layer 420, the etch-stop layer 310, and the barrier

layer 208, and contact the gate stacks 525. *Id.*, 10:60-67, 11:17-22. The function of the staircase contacts is to electrically couple the control gate stacks to a word line control voltage. The penetration of the various layers is necessary for this function.

57. In the context of the ’276 Patent, a barrier layer is simply an etch-stop layer called by another name. Consistent with the well-known principle I explained above in Technology Background (§ VIII), the ’276 Patent states that relative etch selectivity is what enables a layer to “function as an etch-stop layer,” that is, to slow down etching to protect the underlying layers. Ex. 1001, 7:1-6. The only statement in the ’276 Patent regarding the function of the barrier layer is that it serves as an etch stop: “protecting the underlying structure during subsequent *etching* processes.” *Id.*, 7:42-45 (emphasis added). The ’276 Patent further discloses that “the second insulating layer 208 can be used as a barrier layer.” *Id.*, 7:41-45. This statement implies that the second insulating layer 208 is not necessarily (but merely can be) a barrier layer. Setting aside that implication and assuming the descriptions of insulating layer 208 in the ’276 Patent apply to the barrier layer, what the patent discloses regarding the insulating layer 208 confirms the understanding that, for the ’276 Patent, a barrier layer is just another etch-stop layer. To begin, the second insulating layer 208 and the etch-stop layer 310 are formed in sequence to the same step shape. *Id.*, 7:36-40, 7:62-64, 8:9-12, Figs. 3-4. They share the same thickness characteristics. *Id.*, 7:45-51, 8:12-16. Moreover, the barrier layer is optional, and,

when it is absent, the etch-stop layer would take its place in the structure. *Compare id.*, 8:6-12 *with* 7:36-40. When the barrier layer is present, it simply does what an etch-stop layer would do in its absence with respect to protecting the structure during etching. *Id.*, 8:62-9:3 ("In some embodiments, removing the sacrificial layer 106 is also selective to the second insulating layer 208. In some embodiments, the second insulating layer 208 is optional, and removing the sacrificial layer 106 is selective to the etch-stop layer 310."). Both layers comprise an insulating material. *Id.*, 7:57-58 ("the second insulating layer 208 can be made of similar material as the first insulating layer 104."), 8:3-5 ("The etch-stop layer 310 can be made of any suitable insulating material that is different from the second insulating layer 208."). This last statement regarding the two layers having different materials is understandable from my explanation above, that two adjacent layers must have different materials for the lower layer to function as an etch-stop layer with respect to the upper layer. §VIII. Both layers have an etching rate needed to slow down etching, *i.e.*, an etching rate lower than that of the layer immediately above. Ex. 1001, 9:66-10:1 ("the etching rate of the third insulating layer 420 is higher than the etching rate of the etch-stop layer 310"), 10:49-51 ("the etch-stop layer 310 can be etched faster than the second insulating layer 208."); §VIII. Thus, both etch-stop and barrier layers serve the same purpose, *i.e.*, to slow down the etching process to protect the underlying layers from over-etching. Ex. 1001, 6:1-3 ("The etch-stop film protects

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underlying layers during etching processes that form contact VIAs."), 7:42-45 ("the second insulating layer 208 can be used as a barrier layer for protecting the underlying structure during subsequent etching processes."), 10:9-20.

58. In certain embodiments of the '276 Patent, each gate stack 525 comprises a conductive layer 525M at the center, surrounded on three sides by a high-k dielectric layer 525H:

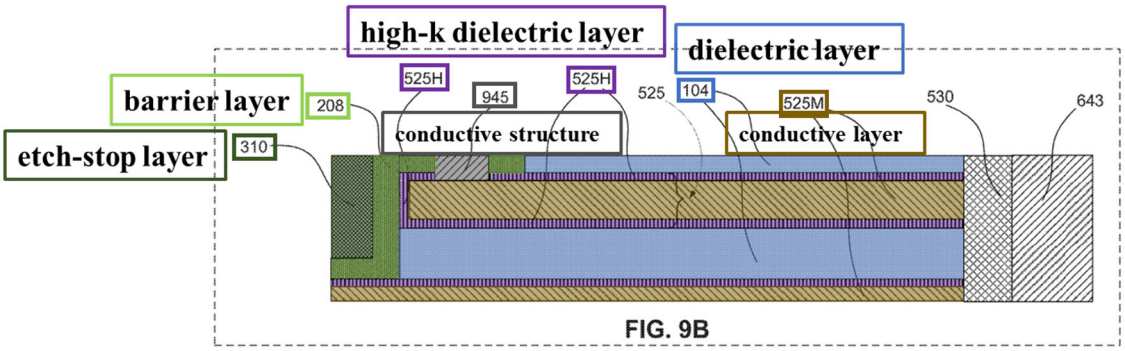


FIG. 9B

Ex. 1001, Fig. 9B, 9:4-10. The conductive structure 945 penetrates the high-k dielectric layer 525H in addition to (as shown above in Figure 9A) the insulating layer 420, the etch-stop layer 310, and the barrier layer 208 and contacts the conductive layer 525M, thereby forming a contact to the control gate. *Id.*, 10:60-67, 11:17-25. This contact, again, is necessary to control the respective gate layers, that is, word lines of the 3D memory device.

59. The '276 Patent asserts that by using an etch-stop layer, the staircase contacts 945 of different lengths may be simultaneously formed using one lithography mask without reducing manufacturing yields due to over-etching the

shallower contact holes. *Id.*, 5:47-6:5. In other words, the '276 Patent alleges that inadvertent punch-through (etching too far and into underlying layers) of shallower holes will not occur. The '276 Patent asserts that its etch-stop layer provides a lower-cost solution than the conventional method using multiple lithography masks. *Id.*, 5:58-60, 6:5-7.

60. During prosecution of the '276 Patent, the Examiner rejected various claims under §103 over Shin, Nam, and Kim '222. Ex. 1002, 90-95. The Examiner found pending claims 4, 7, and 18 allowable if rewritten as independent claims. *Id.*, 95. The Applicant then amended claim 1, adding the allowable features of claim 7, which requires that "the etch-stop layer comprises a second high-k dielectric layer." *Id.*, 114, 118. With Applicant's authorization, the Examiner canceled pending claim 6, which recited "disposing the etch-stop layer comprises disposing one or more of silicon nitride, silicon oxynitride, and silicon oxide," and allowed the remaining claims 1-5 and 8-20. *Id.*, 115, 128. A POSITA would understand the Examiner cancelled the pending claim 6 because silicon nitride, silicon oxynitride, and silicon oxide are not high-k dielectric materials and thus claim 6 cannot depend from claim 1.

61. Every aspect of the alleged invention of the '276 Patent, however, including the second high-k dielectric layer that led to allowance, was conventional by the time of the application was filed, as I will demonstrate below. In particular,

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a second high-k material for an etch-stop layer was a known feature before the priority date of the '276 Patent. Further, Patent Owner's infringement contentions against Petitioner broadens the scope of high-k dielectric to include silicon nitride. While I disagree with that broad scope, silicon nitride was used for etch-stop layers well before the priority date of the '276 Patent.

X. CLAIM CONSTRUCTION

62. I stated my understanding of the law on claim construction above. §V.A. It is my opinion that all terms of the '276 Patent's claims may be understood based on their plain and ordinary meaning. For completeness and based on explanation in §XIII.B.3, the plain and ordinary meaning of "high-k dielectric" as of the priority date of the '276 Patent is a dielectric whose dielectric constant is higher than that of silicon nitride.

XI. SUMMARY OF OPINIONS

63. I have reviewed and analyzed the prior art references and materials listed in §XII below.

64. For the reasons I explain in greater detail below, it is my opinion that before the earliest possible filing date of the '276 Patent on August 31, 2017, a POSITA would have considered claims 1-18 of the '276 Patent to be unpatentable as obvious over the prior art discussed in this declaration. Below is the summary of the grounds detailed in this declaration:

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Ground	Claim(s)	Prior Art Asserted
1	1-2, 4-5, 9-18	Obvious under §103 based on Kim (Ex. 1005) in view of a POSITA's knowledge
2	1-18	Obvious under §103 based on Kim in view of Fang (Ex. 1006)
3	1-15	Obvious under §103 based on Han (Ex. 1007) in view of Fang
4	17-18	Obvious under §103 based on Han in view of Fang and further in view of Chen (Ex. 1008)

XII. THE PRIOR ART

65. The prior art references are analogous art to the '276 Patent. They are in the same field of endeavor of improving 3D memory devices, and more specifically relating to the word line contact structures of such devices.

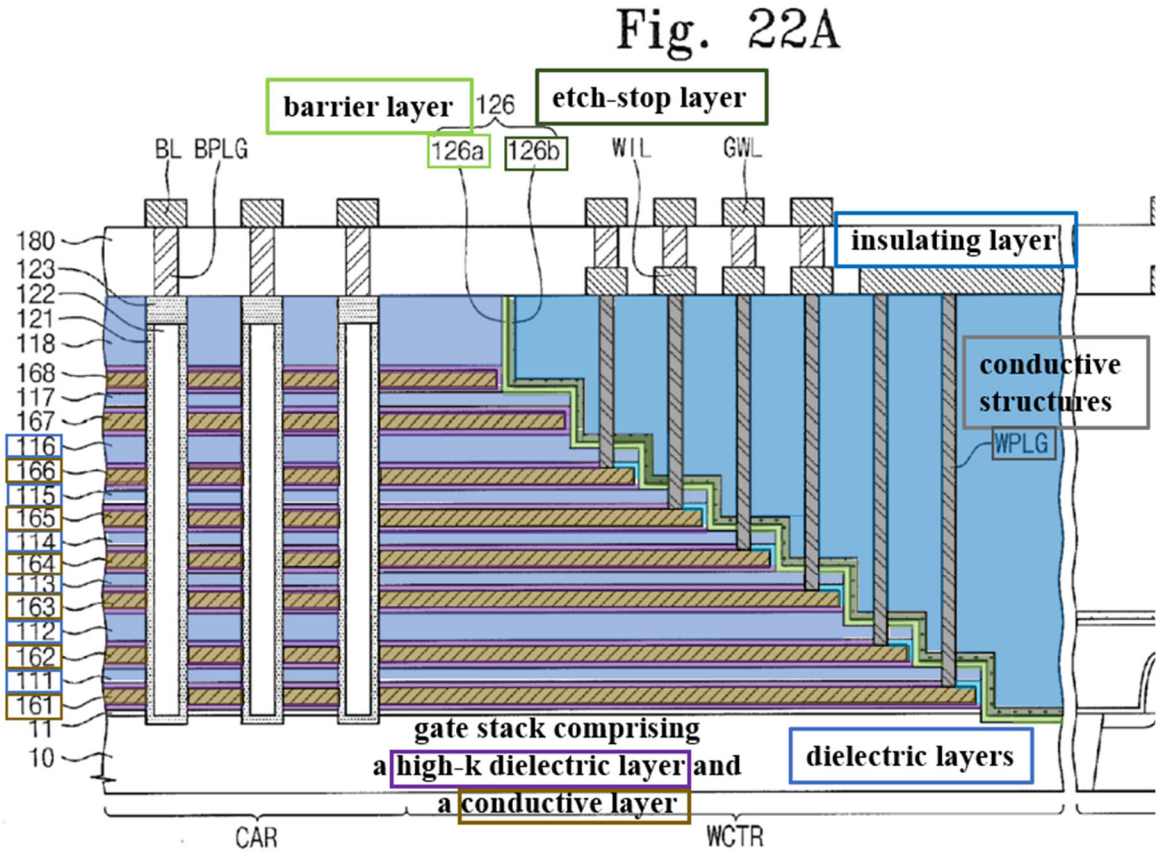
A. Kim

66. U.S. Patent Publication No. 2012/0070944 (Ex. 1005 or Kim). Kim was filed on September 13, 2011 and was published on March 22, 2012. Ex. 1005, Cover. I understand Kim is prior art to the '276 Patent.

67. Kim discloses methods of manufacturing a 3D semiconductor memory device having a cell-array region, a peripheral-circuit region, and a word line contact region WCTR disposed between the cell-array region and the peripheral-circuit region. *Id.*, Abstract, [0037]. Kim focuses on the issue of planarizing the interlayer dielectric (which is analogous to the insulating layer of the '276 Patent) between the regions. *Id.*, [0024]-[0025].

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68. It is my opinion that Kim's descriptions of the method of manufacturing word line contact region WCTR render obvious the alleged invention of the '276 Patent. In advance of the detailed analysis below, this is readily apparent by comparing the devices made from their respective methods: Kim's Figure 22A and Figures 9A-9B of the '276 Patent in §IX above.



Ex. 1005, Fig. 22A.[3]

[3] All cross-sectional images from Kim and Han shown in this Declaration omit the peripheral-circuit region that is irrelevant to this Declaration.

69. Kim discloses a silicon-nitride etch-stop layer. A POSITA would not have considered silicon nitride to be a high-k dielectric material. Patent Owner, however, apparently has a contrary view as shown by its infringement allegations against Petitioner. Ex. 1019, 9.

70. Like Figure 22A above, Kim's figures show embodiments in which a dielectric layer is disposed over a sacrificial layer/gate stack at each step. But Kim also discloses the reverse order, that is, embodiments in which a sacrificial layer/gate stack is disposed over a dielectric layer at each step. For example, after describing the layer ordering in its figures, Kim discloses that "[i]n other embodiments, each of top surfaces of the sacrificial layers SC1 to SC8, not the top surfaces of the insulating layers 111 to 118, may be partially exposed in the word line contact region WCTR." Ex. 1005, [0090]. Sacrificial layers SC1-SC8 are replaced with, and thus positionally correspond to, gate stacks in the fully formed device comprising gate-electrode layers and blocking layers. *Id.*, [0104]-[0105], [0198]-[0200]. This can be seen by comparing Figures 17A and 22A, for example. More specifically, Kim discloses that the edge portions of the sacrificial layers SC1-SC8 (or of the insulating layers 111 to 118) may be exposed as the top surfaces of the steps. *Id.*, [0091] ("the insulating layers 111 to 118 and/or the sacrificial layers SC1 to SC8 thereof may have the edge portions sequentially exposed on the word line contact region WCTR."), [0240] ("the insulating layers 111 to 118 and/or the sacrificial layers SC1

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to SC8 thereof may have the edge portions sequentially exposed on the word line contact region WCTR."). In other words, the edge portions of the sacrificial layers/gate stacks can be positioned directly below the first stop layer 126a. Therefore, Kim discloses disposing a sacrificial layer/gate stack over a dielectric layer at each step.

B. Fang

71. U.S. Patent Publication No. 2019/0067306A1 (Ex. 1006 or Fang) was filed on August 24, 2017 and was published on February 28, 2019. Ex. 1006, Cover. I understand Fang is prior art to the '276 Patent.

72. Like the '276 Patent and the other prior art in §XII, Fang discloses methods of forming a 3D semiconductor memory device having a staircase structure. Ex. 1006, [0001]-[0002]. The structure comprises alternating dielectric layers and conductive layers. *Id.*, Abstract. The structure further comprises a silicon-nitride etch-stop layer and an oxide insulating layer. *Id.* Conductive word line structures contacting the conductive layers are formed in openings through the insulating layer, the etch-stop layer, and the dielectric layers:

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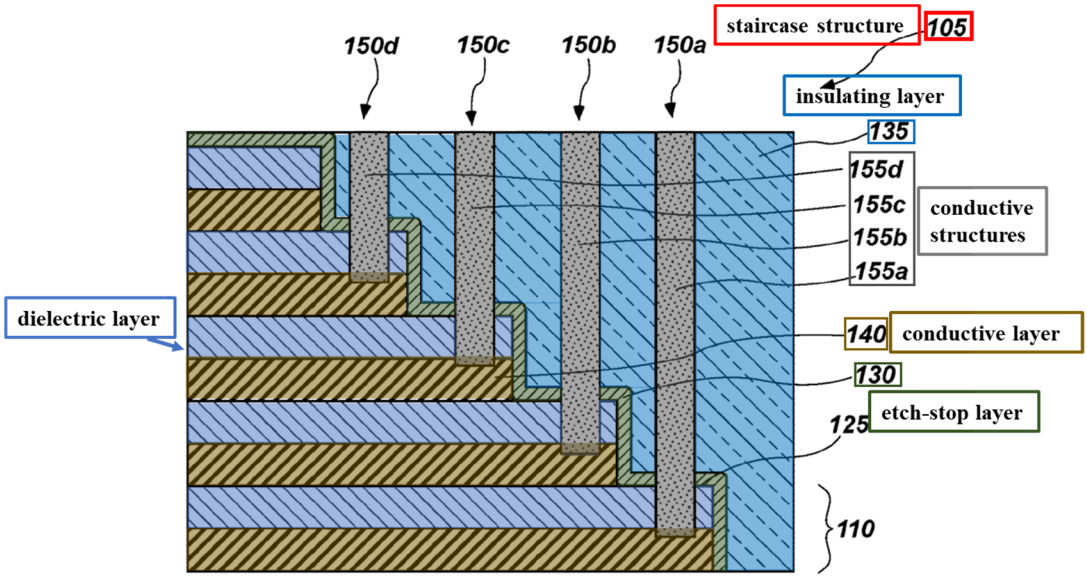


FIG. 6

Ex. 1006, Fig. 6. The word line structures or contacts have "different depths" to reach the "control gates" at various steps of the staircase. *Id.*, [0001]-[0002].

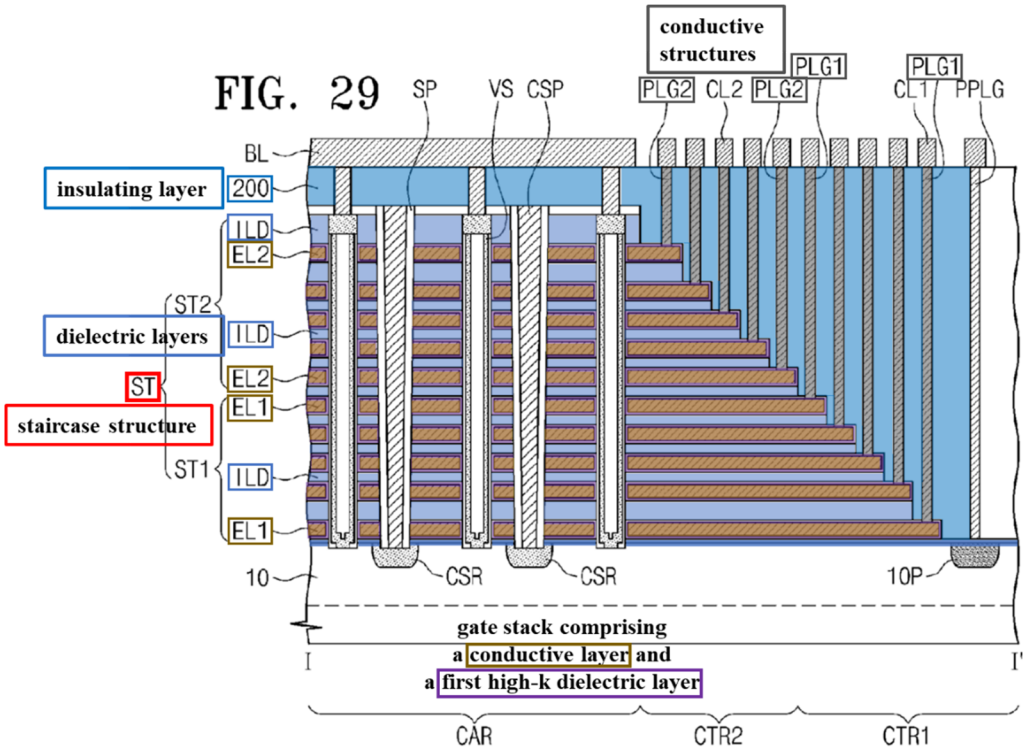
73. Notably, Fang discloses that "the etch stop material … may be a high-k dielectric material, such as hafnium oxide," as an alternative. *Id.*, [0022].

C. Han

74. U.S. Patent Publication No. 2017/0062470A1 (Ex. 1007 or Han) was filed on August 26, 2016 and claims priority to a Korean patent application filed on August 28, 2015. Ex. 1007, Cover. I understand Han is prior art to the '276 Patent.

75. Like the '276 Patent and the other prior art in §XII, Han discloses methods of forming a 3D semiconductor memory device with a staircase structure. Ex. 1007, [0142], [0151]. The staircase comprises alternating dielectric layers and gate stacks comprising high-k dielectric layers surrounding conductive layers. *Id.*,

[0096], [0118]-[0120], [0134]-[0141]. The high-k dielectric layers are called "horizontal insulating layer[s]" and may be the data storage layer surrounding the channel. *Id.*, [0119]. As was conventional by 2017, after sacrificial layers of the staircase stack are removed, the channel region may be coated with dielectric materials to form a data storage layer. Because the recess regions created by the removal of the sacrificial layers are connected to the channel region, the same coating can form in the recess regions. An insulating layer covers the staircase structure. *Id.*, [0131]. Conductive structures contacting the conductive layers are formed in openings through the insulating layer and the high-k dielectric layer:



Id., Fig. 29. Again, these contacts are necessary to couple the conductive gate layer to the control voltages for proper functioning of the memory device. §VIII.

D. Chen

76. U.S. Patent Publication No. 2017/0294384A1 (Ex. 1008 or Chen) was filed on April 12, 2016 and was published on October 12, 2017. Ex. 1008, Cover. I understand Chen is prior art to the '276 Patent.

77. Like the '276 Patent, Kim, and Fang, Chen discloses manufacturing methods of forming 3D memory devices comprising "stack structure, an etching stop layer, and a conductive structure." Ex. 1008, Abstract, [0027]-[0029]. The dielectric layers and conductive layers in the stack structure may be positioned with either type of layer above the other at each step. *Id.*, Figs. 7A-7B, [0045]-[0046]. The etch-stop layer may comprise a single layer or be divided into two layers. *Id.*, [0037]. A two-layer configuration is shown below:

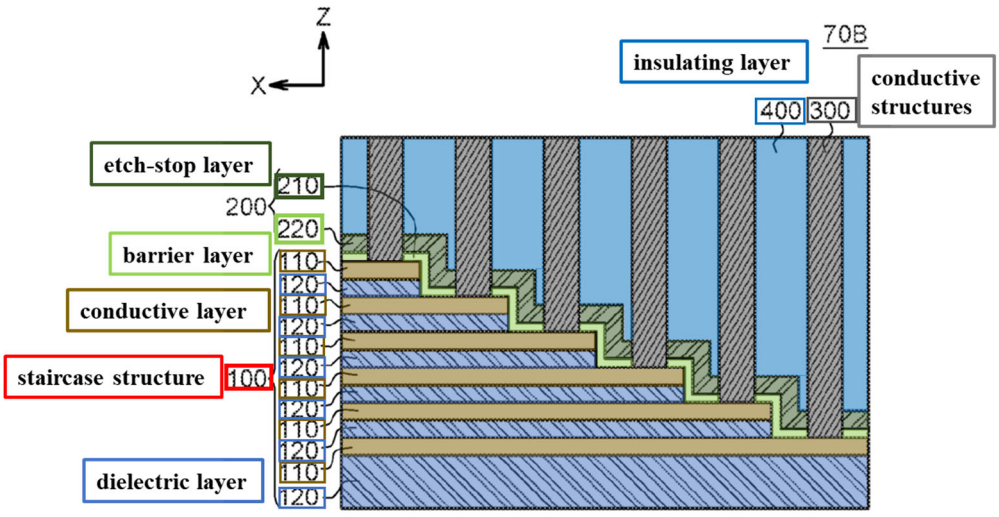


FIG. 7B

Id., Fig. 7B. In this two-layer configuration, the upper layer (*i.e.*, the etch-stop layer) may comprise a high-k dielectric. *Id.*, [0041].

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78. At this point it is necessary to introduce the concept of "tunneling." Tunneling refers to a quantum mechanical phenomenon wherein particles, *e.g.*, electrons carrying electrical charges, can penetrate a potential energy barrier larger than the total energy (potential plus kinetic) of the particles. (This violates the principles of classical mechanics because it implies that the particles must have a negative kinetic energy when they are inside the barrier.) Tunneling can be understood based on the wave-particle duality of nature, as described by quantum mechanics. Particles impinging on the tunnel barrier can be thought of as a wave, with a so-called de Broglie wavelength, with a finite reflection probability and a finite transmission probability (i.e. tunneling). In other words, the tunnel barrier acts as semi-transparent barrier for the electron waves. Undesirable tunneling caused by unintended tunneling of electrical charges may also occur due to electrical weak spots in the tunnel oxide and cause a memory device's storage characteristics to degrade, and make the NAND cell less non-volatile. However, in a NAND memory tunneling is also used beneficially to transfer charges from the polysilicon channel, through the tunnel oxide into the charge storage layer (CTL), which can be the high-k dielectric surrounding the metal word lines. This is the program mechanism. Conversely, electrons can also be removed by tunneling from the CTL into the channel, leading to the erase operation. The tunneling probability decreases with increasing barrier potential height, or increasing barrier thickness. Increasing the

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energy gap of the tunnel oxide increases the tunneling barrier, and increasing the tunnel oxide thickness increases the tunneling length and reduces the probability of tunneling, and vice versa. The high-k dielectric surrounding the word line is generally much thicker than the tunnel oxide, and hence acts as a blocking layer. Chen discloses that an aluminum oxide (a high-k dielectric) etch-stop layer has a larger tunneling length than a silicon nitride etch-stop layer. *Id.*, [0049]. Chen further discloses that having two etch-stop layers increases the total tunneling length of the etch-stop layer(s). *Id.*, [0053]. In both cases, the larger tunnel length results in increased electrical isolation between the conductive layers and increased device stability, *i.e.*, non-volatility of the NAND memory cell. *Id.*, [0004], [0049], [0053].

XIII. GROUND 1: KIM IN VIEW OF A POSITA'S KNOWLEDGE

79. Ground 1 applies Patent Owner's interpretation of "high-k," apparent from Patent Owner's infringement allegations against Petitioner. Ground 2 applies Petitioner's interpretation, which in my opinion is the correct interpretation.

80. This Declaration relies on Kim's Figure 17A-22B embodiment comprising an etch-stop layer and a barrier layer. Kim discloses other embodiments, such as Figures 5A-14B.

81. Even though Kim discloses different embodiments, a POSITA would have understood that descriptions of one of Kim's embodiments apply to other embodiments except where the embodiments differ. Kim discloses closely related

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embodiments having many of the same elements denoted by the same reference numerals. Ex. 1005, [0184]. For example, the embodiments shown in Figures 5A-14B and in Figures 17A-22B are closely related. Accordingly, Kim states that overlapping descriptions of the same elements are omitted in the descriptions of Figures 17A-22B. *Id.* Moreover, the descriptions of Figures 17A-22B extensively reference Figures 9A-14B. *Id.*, [0183]-[0212]. Similarly, as another example, descriptions of Figures 26-27 refer to the two embodiments in Figures 17A-22A and 8A-11A. *Id.*, [0221], [0223]-[0224]. A POSITA would have understood Kim's various embodiments to be variants of each other that share many common elements and characteristics. Kim's approach is common among patent art in the field. A patent publication commonly discloses multiple embodiments with slight variation and typically explains one embodiment in detail and other embodiments where they differ from the one embodiment. Kim is one such publication.

A. Kim Discloses "Disposing a Sacrificial Layer over a Dielectric Layer"

82. First, as a preliminary matter, sacrificial layers of the '276 Patent are replaced with gate stacks in the fully formed claimed semiconductor structure. Ex. 1001, 15:14-15 (limitation [1.D]) ("replacing the sacrificial layer of each step with a gate stack…."). This is what Fang calls a "'replacement gate' process." Ex. 1006, [0025]. Thus, sacrificial layers positionally correspond to gate stacks, and

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"disposing a sacrificial layer over a dielectric layer" create a structure whose gate stack is disposed over a dielectric layer. The two impose the same positional requirement.

83. Even though Kim's figures show the opposite order, it discloses the sacrificial-layer-on-top/gate-stack-on-top layer ordering. §XII.A. A POSITA would have understood that this teaching of the gate-stack-on-top layer ordering applies to the Figure 17A-22B embodiment. As explained above, Kim's descriptions apply to common aspects across embodiments. §XIII. A POSITA would have understood that the reverse layer ordering is compatible with the variations between Kim's embodiments. Kim's teaching at least renders the sacrificial-layer-on-top limitation obvious. In fact, visualizing the reversed layer ordering would have been well within the grasp of a POSITA.

84. In addition to Kim's express teaching, a POSITA would have known that either order was a common alternative in the art. For example, Chen discloses both orders side-by-side:

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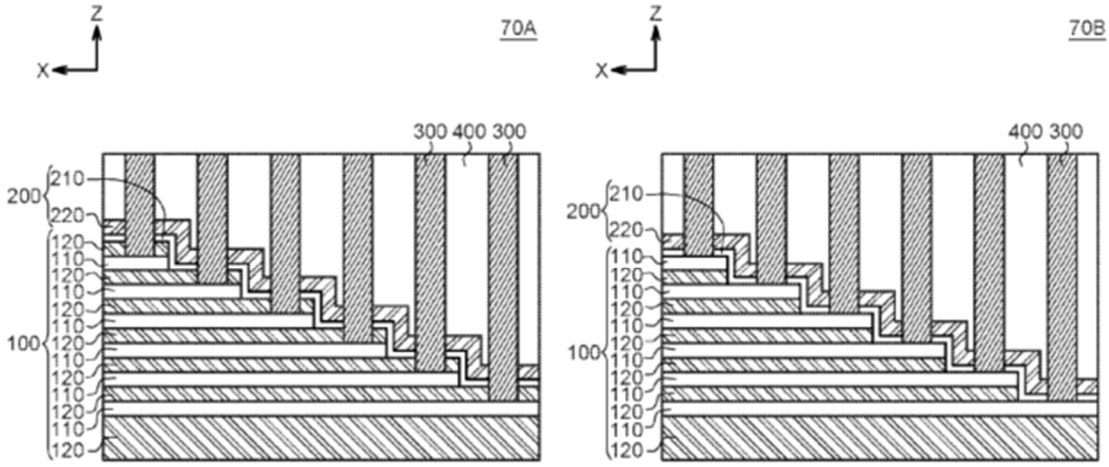


FIG. 7A FIG. 7B

Ex. 1008, Figs. 7A (dielectric layer 120 on top), 7B (conductor layer 110 on top), [0044]-[0046]. Yu also teaches that the layers may be stacked in either order. Ex. 1009, [0034]-[0035]. A POSITA would have known that either order was routine, highly predictable, and would have had a reasonable expectation of success for implementing a gate-stack-on-top embodiment. For example, either order was compatible with common deposition techniques such as CVD or ALD used to deposit these layers. Since the stack that is deposited consists of two types of dielectrics (such as silicon dioxide and silicon nitride), it would have been trivial to alter the sequence of the precursor gas flows (such as silane and oxygen for silicon dioxide, and dichlorosilane and ammonia for silicon nitride) during CVD to achieve either oxide on top, or nitride on top in the staircase. The nitride layers (which is commonly the sacrificial layer) are then selectively etched off and the cavities (or

recess regions) refilled with a high-k gate dielectric such as hafnium dioxide and a word line metal such as tungsten to form the gate stack.

85. At the very least, Kim's teaching on reversing the order represents a known technique that is at least a suitable option for the Figure 17A-22B embodiment. Chen and Yu demonstrate that either order was viable and known to a POSITA.

86. Below in this Declaration, Kim's figures are modified to show this sacrificial-layer-on-top/gate-stack-on-top ordering. Based on Kim's express teaching and a POSITA's knowledge, a POSITA could have easily visualized how the reversed order would be arranged. Doing so was well within the knowledge and skill of a POSITA. Furthermore, prior-art references with gate-stack-on-top configurations (two additional examples below) would have helped a POSITA visualize a Kim embodiment with gate stacks on top:

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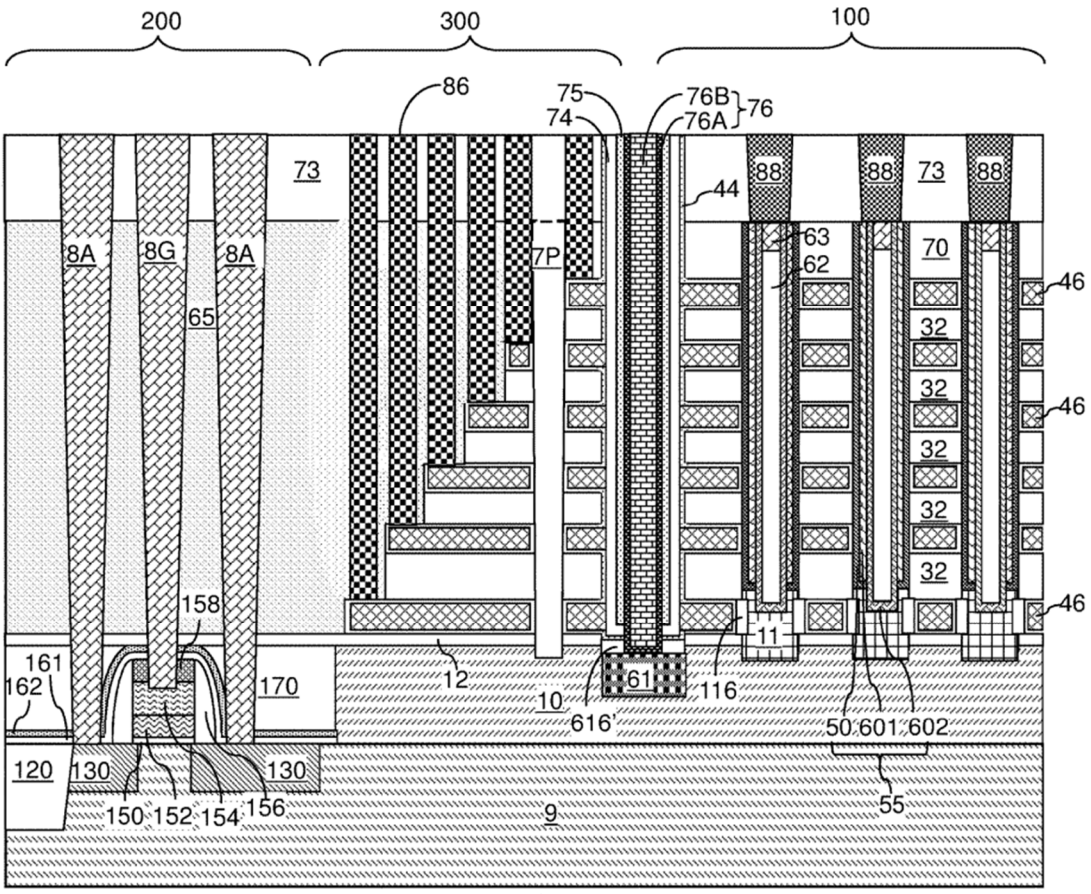
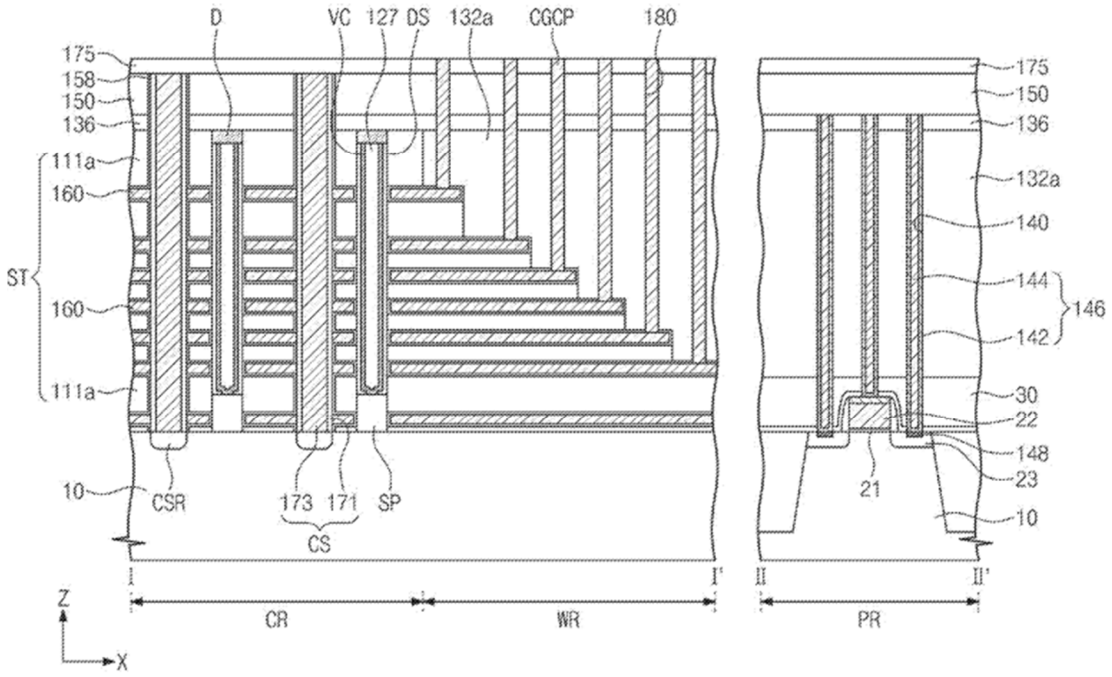


FIG. 13

Ex. 1016, Fig. 13.

FIG. 20



Ex. 1017, Fig. 20.

87. For clarity, the modified Kim figures in this Declaration are annotated with "Gate-Stack-on-Top."

B. Claim 1:

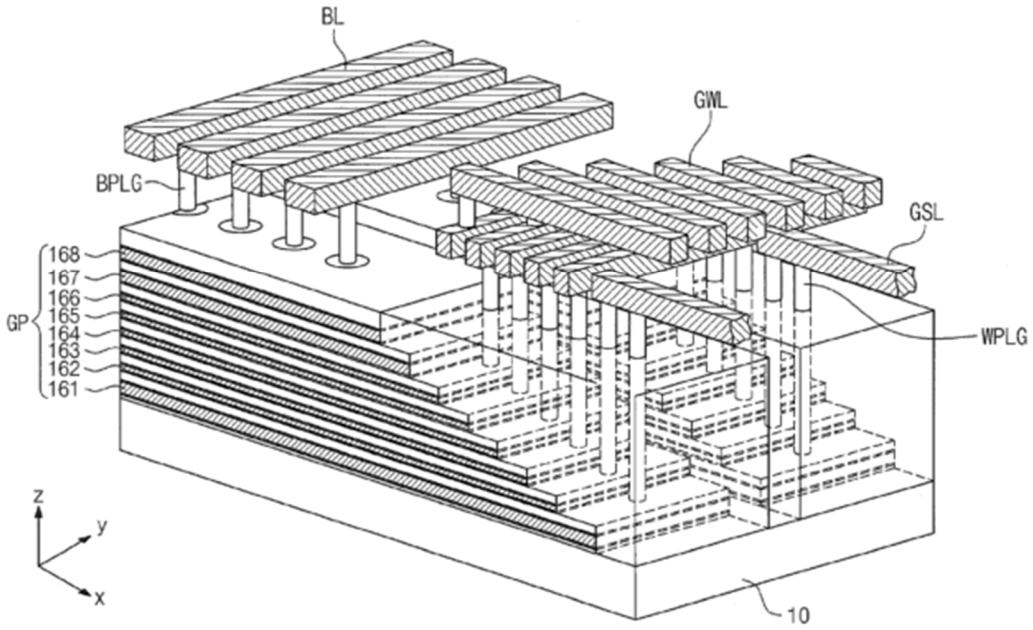
1. [1.PRE] "A method for forming a semiconductor structure, comprising:"

88. Kim discloses *[a] method for forming a semiconductor structure*, *e.g.*, "methods of manufacturing a three dimensional semiconductor device."[4] Ex. 1005, Abstract. Figure 4 shows a perspective view of such a 3D memory device. The

[4] Red italics in the claim-mapping sections denote claim language.

staircase structure and the conductive structure on the landings are clearly illustrated:

Fig. 4



Id., Fig. 4. Kim's Figures 17A-22A shows such a semiconductor structure at successive stages of manufacturing. *Id.*, [0183]. This sequence of figures closely matches the claimed manufacturing steps of Claim 1, as illustrated in the following sections.

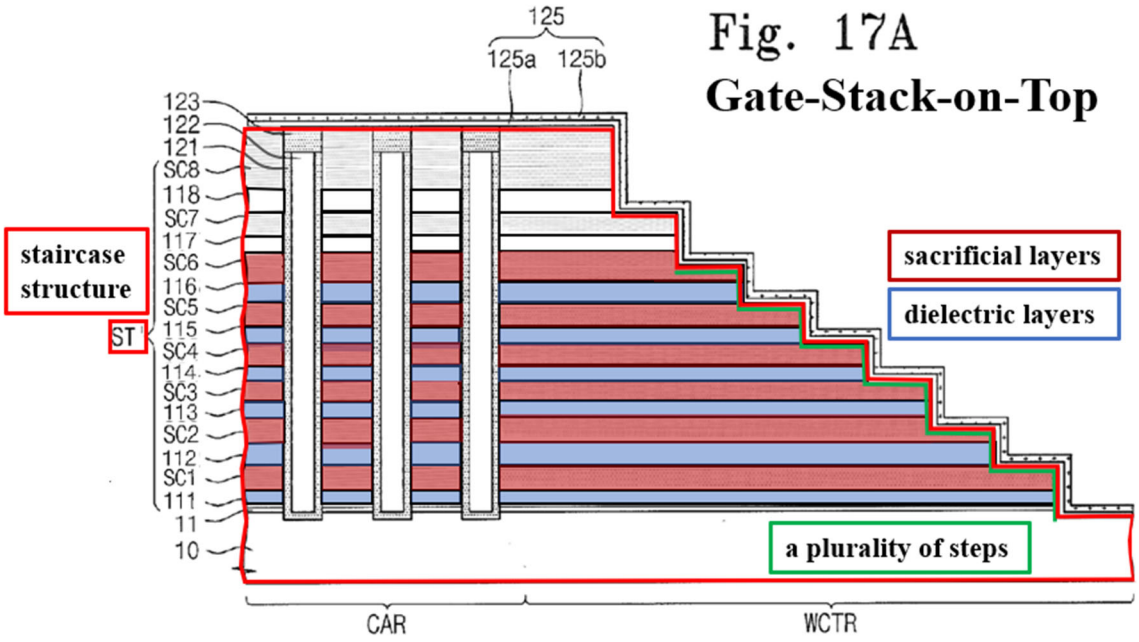
2. [1.A] "forming a staircase structure having a plurality of steps, wherein the forming of each step of the plurality of steps comprises disposing a sacrificial layer over a dielectric layer;"

89. It is my opinion that Kim at least renders limitation [1.A] obvious.

90. Specifically, Kim's method comprises *forming a staircase structure* ("stepwise stacked layer structure ST′") *having a plurality of steps, wherein the*

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forming of each step of the plurality of steps comprises disposing a sacrificial layer (one of "sacrificial layers" SC1-SC6) *over a dielectric layer* (one of "insulating layers" 111-116), as illustrated below:



Ex. 1005, Fig. 17A, [0007]-[0008] ("a stepwise structure"), [0064] (forming "a stacked layer structure ST" including a plurality of insulating layers and sacrificial layers), [0086] ("stepwise stacked layer structure ST′"). As explained above, the description of Figures 5A-14B applies to the Figure 17A-22B embodiment. §XIII.

91. As shown above, the *plurality of steps* may be the bottom six steps, that is, the *plurality of steps* may not include all of the steps of the *staircase structure*. This is relevant to limitation [1.F], because [1.F] requires "exposing … the conductive layer of *each* step" of the plurality of steps to allow contacts between the conductive layers and the conductive structures. The *plurality of steps* need not

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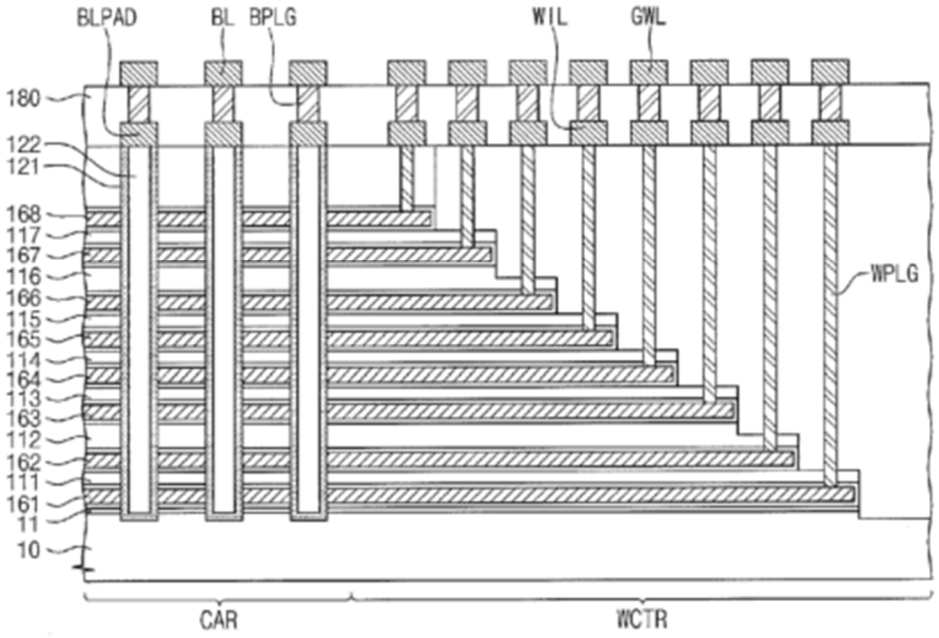
include all steps of the *staircase structure*, because I understand the term *a staircase structure having a plurality of steps* permits additional steps given the use of *having* in patent usage. Relatedly, the parent '711 Patent recites a parallel limitation in claim 13 using another open-ended word *comprising* in patent usage. Ex. 1018, 16:7 ("a staircase structure comprising a plurality of steps"). This further confirms the staircase structure may include additional steps because claim 1 basically recites a manufacturing method for forming the semiconductor structure of the '711 Patent claim 13, except that claim 1 requires the etch-stop layer to be made from a high-k dielectric, which is not relevant to the "steps" requirement.

92. Moreover, a POSITA would have understood, and certainly found obvious, that there are conductive structures that are not shown on the top steps, and the *plurality of steps* would then include all steps of the staircase. This is because the channel structures are effectively a string of memory cells at the interface of the channel and the word lines (which are the conductive layers coupled to the vertical conductive structures), and for various memory cell operations (such as a read operation) targeting a memory cell in the middle of the memory string, it is necessary to turn on all memory cells above and below the target cell by applying a voltage (commonly known as a pass voltage) to the memory cells through the word lines (*i.e.*, gates). §VIII. The memory would not be able properly function without a contact to each gate layer because the pass voltage (for example) is applied through

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that contact to the memory cell at the intersection of the gate layer and the channel. In fact, usually the top gate layer is a select layer to turn on the memory string, typically a drain-select layer. Therefore, it was conventional for a staircase structure to have a conductive structure on every step. Examples abound just within a few references cited in this Declaration. Ex. 1006, Fig. 6; Ex. 1007, Figs. 7A-7B. Indeed, Kim also discloses such an embodiment:

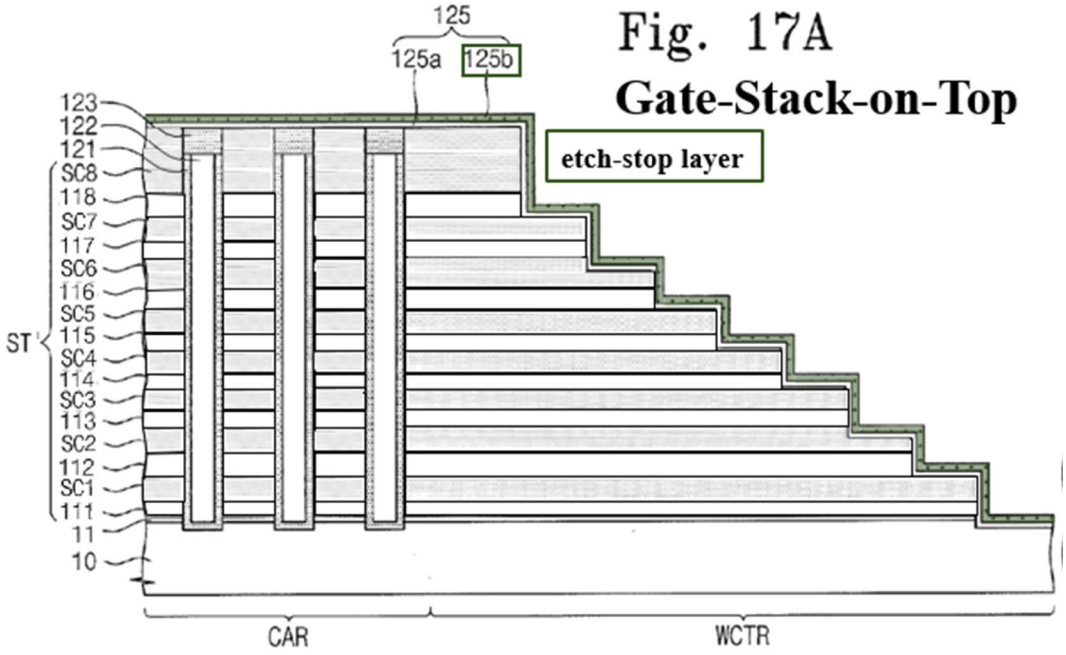
Fig. 30



Ex. 1005, Fig. 30. This further demonstrates that a POSITA would have understood, and found obvious, to include a contact on the top steps. While Kim's figures do not annotate the top steps, Grounds 1-2 equally apply to including contacts on each step of the staircase as just explained.

3. [1.B] "disposing an etch-stop layer on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer;"

93. Kim discloses *disposing an etch-stop layer* ("second stop layer" 125b) *on each step of the plurality of steps*:



Ex. 1005, Fig. 17A, [0185] (forming a conformal etch-stop layer on the substrate after forming the stepwise stacked layer structure ST), [0213] (similar). Although Kim does not expressly state that the second stop layer 125b serves as an etch stop, a POSITA would have understood the etch selectivity of the second stop layer to serve its purpose of protecting underlying structures and preventing punch-through. *Id.*, [0186]-[0187]. An etch stop is what "stop" in "second stop layer" refers to. Also, as explained, as long as the two layers comprise different materials and thus have different etching rates, both can serve the intended purpose of an etch stop.

That is what Kim discloses: the etch-stop layer may be formed of silicon nitride. *Id.*, [0187]. And the interlayer dielectric above it may be formed from a variety of materials other than silicon nitride. *Id.*, [0098].

94. Kim further discloses that *the etch-stop layer comprises a second high-k dielectric layer* under Patent Owner's incorrect interpretation of high-k dielectric. Specifically, Kim's etch-stop layer may comprise silicon nitride. Contrary to the '276 Patent and a POSITA's knowledge at the time of the '276 Patent, Patent Owner apparently considers silicon nitride to be a high-k dielectric material. Ex. 1019, 9 (Patent Owner alleging that "forming the etch-stop layer SiN" satisfies limitation [1.B]). Kim, too, considers silicon nitride a high-k material. Ex. 1005, [0186], [0064]. But the '276 Patent itself does not identify silicon nitride as a high-k dielectric. Ex. 1001, 8:16-20 ("etch-stop layer 310 can be made of silicon nitride, silicon oxynitride, spin-on-dielectric, and/or high-k dielectric films…."). In fact, the CN patent application to which the '276 Patent claims priority expressly excludes silicon nitride as a high-k dielectric: "a high-k film … refers to a film having a dielectric constant (permittivity) higher than that of silicon nitride." Ex. 1022, [0051]. That is consistent with a POSITA's knowledge of the common usage of the term.

95. In the context of semiconductor devices such as 3D NAND memory devices that are the subject matter of the '276 Patent, a POSITA would have known

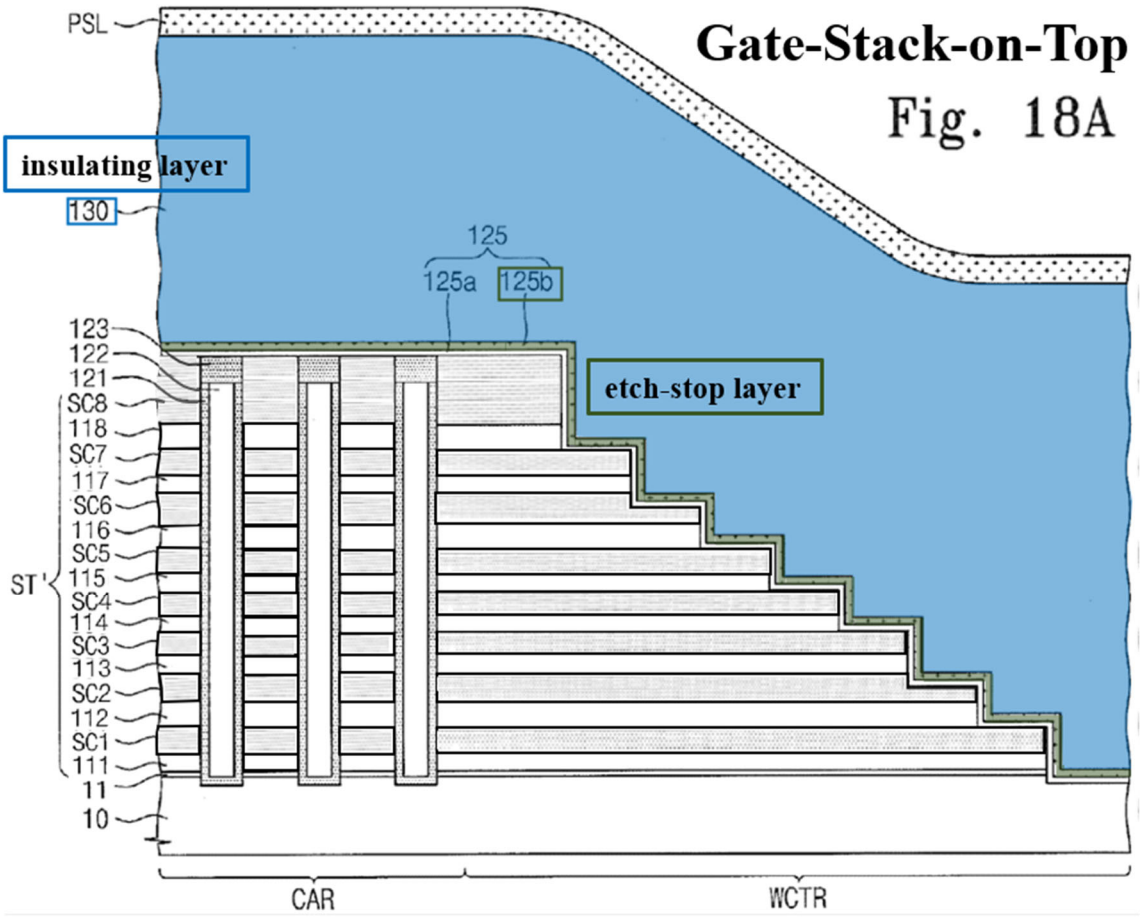
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a high-k dielectric material has a dielectric constant significantly higher than that of silicon dioxide, which has a relative dielectric constant of 3.9. The relative dielectric constant is given by the ratio of the relative dielectric constant and the dielectric constant of free space or vacuum. Silicon nitride (*e.g.*, Si_3N_4) has a relative dielectric constant of 7.5, which, while higher than that of silicon dioxide, is generally not viewed as a high-k dielectric in the context of semiconductor manufacturing. In that context, a POSITA would have typically considered a relative dielectric constant higher than 9 for a high-k dielectric (*e.g.*, aluminum oxide has a relative dielectric constant of approximately 9, and hafnium dioxide, a typical high-k dielectric, has a relative dielectric constant of around 25).

4. [1.C] "disposing an insulating layer on the etch-stop layer;"

96. Kim discloses *disposing an insulating layer* ("interlayer dielectric" 130) *on the etch-stop layer* ("second stop layer" 125b):

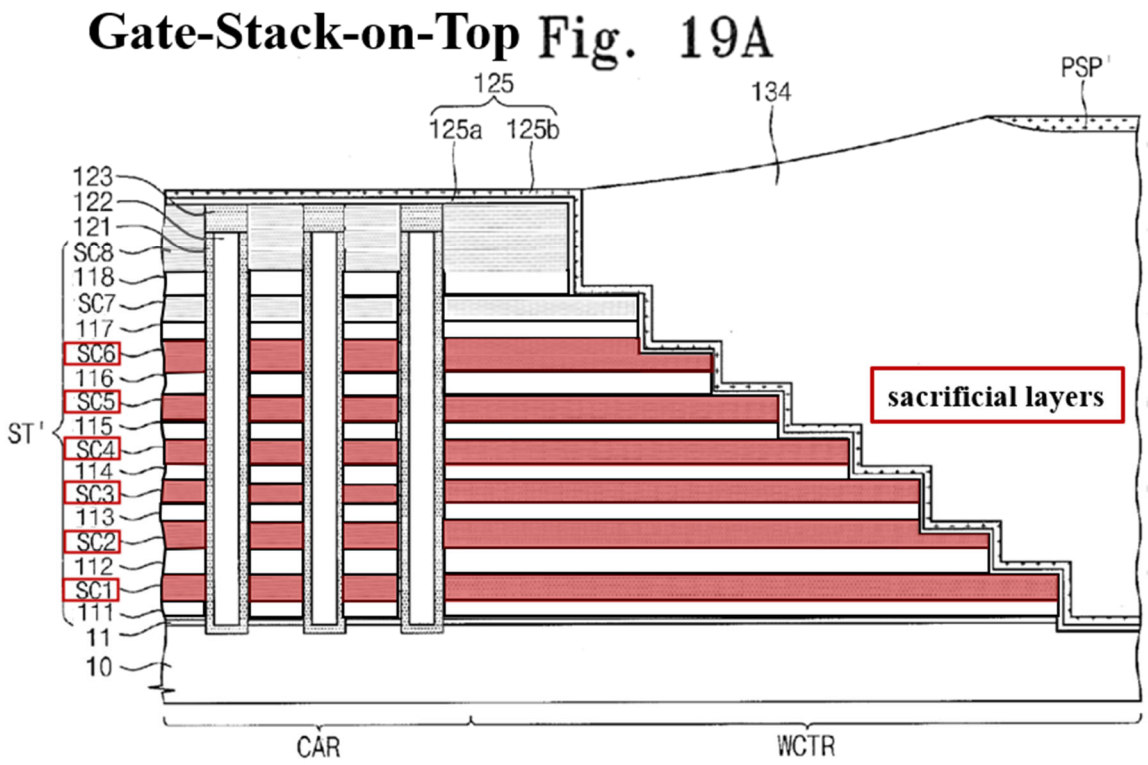
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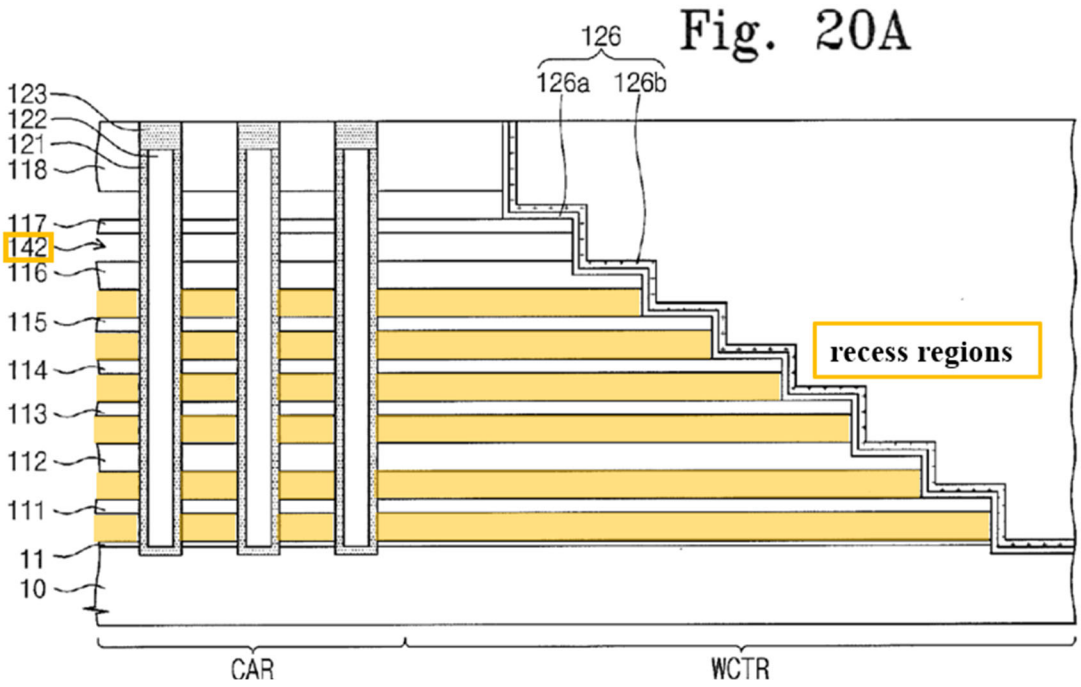
Ex. 1005, Fig. 18A. As the figure clearly shows, "the interlayer dielectric 130 … may be … formed on the etch stop layer 125." *Id.*, [0188]. *id.*, [0007]-[0008], [0094] (covering the stepwise stacked layer structure ST′), [0097]. The insulating layer provides structural support and electrical insulation on top of the staircase structure. Its top surface is conventionally planarized to facilitate depositing additional layers above it. *See id.*, [0213].

5. [1.D] "replacing the sacrificial layer of each step with a gate stack, the gate stack comprising a conductive layer and a first high-k dielectric layer;"

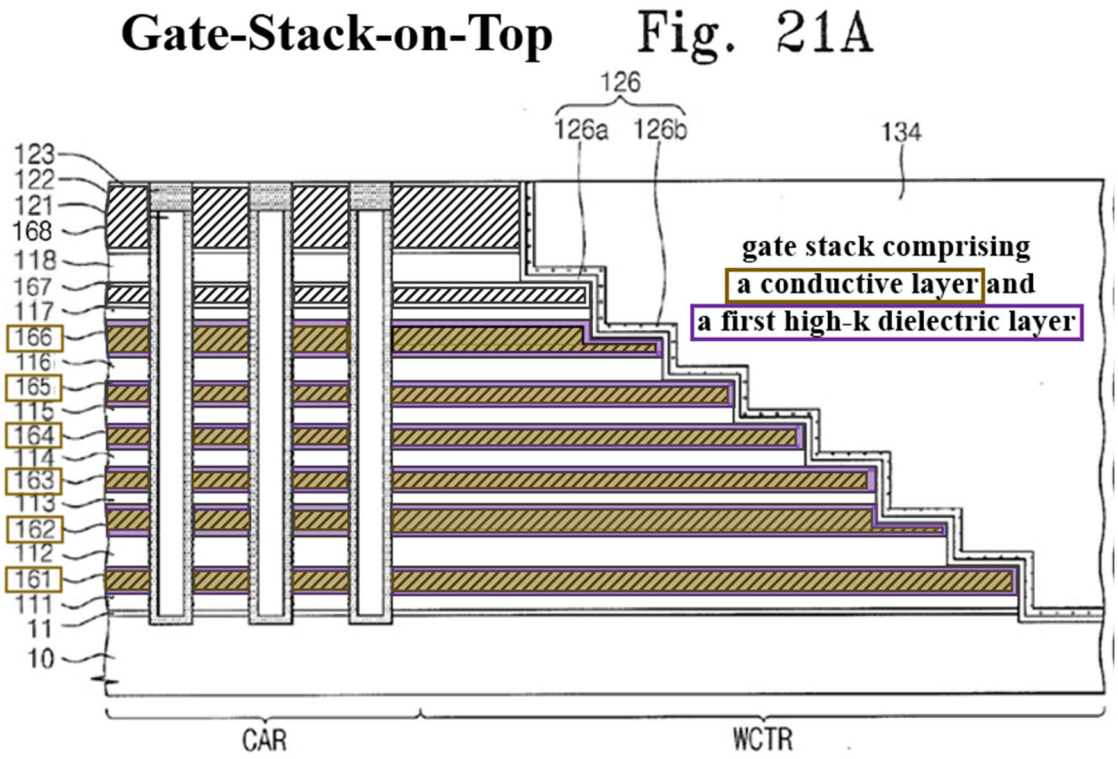
97. Kim discloses *replacing the sacrificial layer* (one of "sacrificial layers" SC1-SC6) *of each step with a gate stack*. This can be seen through the progression from Figure 19A through Figure 21A. Figure 19A shows the sacrificial layers:



Ex. 1005, Fig. 19A. Figure 20A shows sacrificial layers having been removed, creating recess regions:



Id., Fig. 20A, [0198]-[0200] ("selectively removing the sacrificial layers … to form recess regions 142 between the insulating layers…."). Figure 21A shows *gate stack[s] [each] comprising a conductive layer* (one of "gate electrodes" 161-166) *and a first high-k dielectric layer* ("blocking insulating layer" in a "data storing layer") formed in the recess regions, thereby *replacing the sacrificial layer of each step*.



Id., Fig. 21A, [0200]-[0202] ("forming a data storing layer 150 and gate electrodes 161 to 168 in the recess regions 142."), [0134]. As explained, it was conventional to form data-storing layers on the surface of the channel region after removing the sacrificial layers. Therefore, the data-storing layers would form in the recess regions in the staircase stack. The reverse order of the sacrificial layer and the insulating layer at each step does not impact this process. A reverse order may offset the vertical positions of the recess regions but the formation of the recess regions and data-storing layers proceeds identically with either stack order.

98. Kim discloses that *the gate stack compris[es] a conductive layer*, which Kim calls a "gate conductive layer" or "gate electrode." Ex. 1005, [0202].

99. Kim discloses that *the gate stack compris[es] … a first high-k dielectric layer*. Specifically, Kim discloses "forming a data storing layer 150 and gate electrodes 161 to [166]" between insulating layers. *Id.*, [0200]. The data-storing layer forms a conformal covering of the gate electrodes and surrounds them. *Id.*, [0202], Figs. 13A-13B. The data-storing layer may include a blocking insulating layer, which may comprise *a first high-k dielectric* such as aluminum oxide. *Id.*, [0148], [0151], Figs. 15B-15D. In fact, high-k dielectrics were conventional materials for the data-storing layer or charge storage layer (CTL) because they provide better electrical insulation and therefore can better maintain the stored electrical charges than continuous floating gates such as polysilicon, leading to improved non-volatility or retention time of the cell to greater than about 10 years at room temperature. With a continuous floating gate, a single weak spot in the thin tunnel oxide can discharge the stored charges into the polysilicon channel. In contrast, the charges are stored at discontinuous electrical trap sites in the CTL, leading to improved charge retention. As mentioned before, the CTL is made thicker than the tunnel oxide so that the stored charges cannot leak out via tunneling; hence the moniker "blocking layer."

6. [1.E] "forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer;"

100. As a preliminary matter, Kim's disclosures of the second stop layer

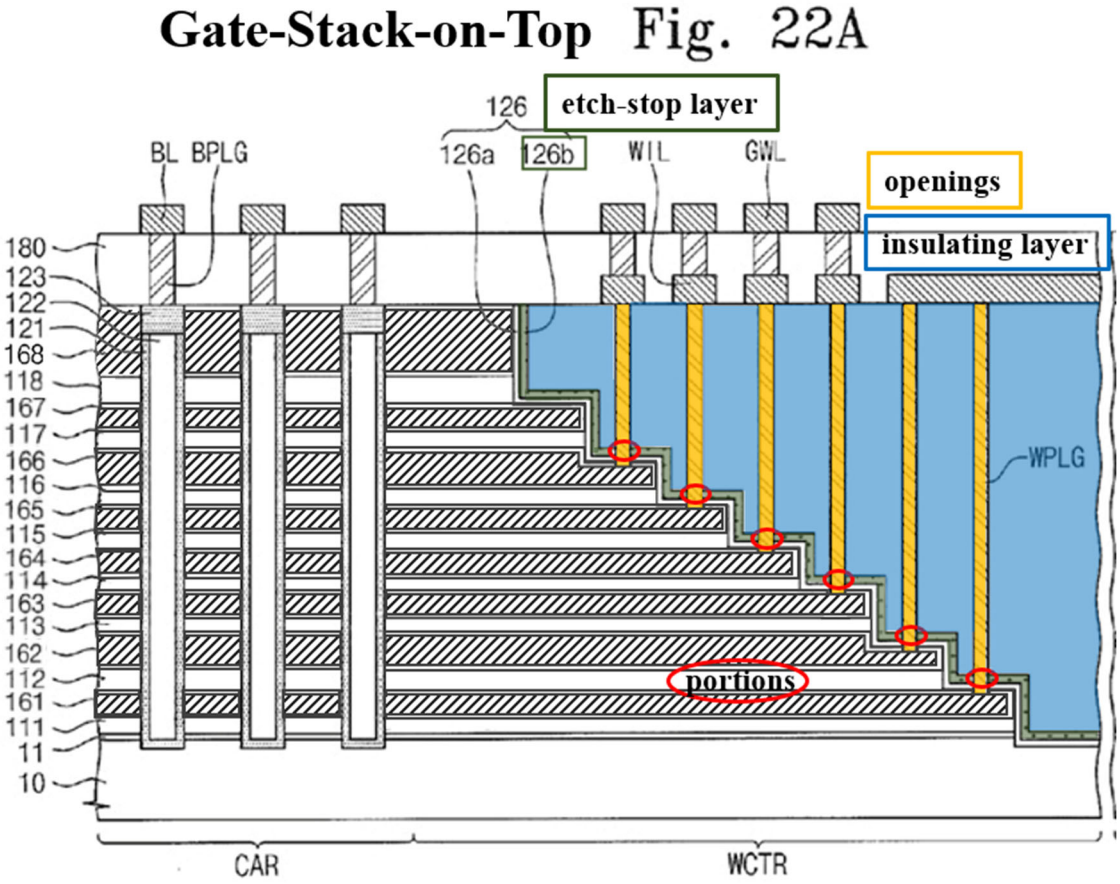
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125b apply to the layer labeled 126b in Figures 20A-22A for purposes of these claims. The "stepwise etch stop pattern 126[b]" simply results from removing the portion of the second stop layer 125b at the top surface of Kim's staircase structure. Ex. 1005, [0201]; *compare id.*, Fig. 19A (showing 125a-125b) *with id.*, Fig. 20A (showing 126a-126b after the removal).

101. Similarly, Kim's descriptions of the interlayer dielectric 130 apply to the interlayer insulating pattern 134 in Figures 19A-22A. The interlayer insulating pattern 134 results from the interlayer dielectric 130 after a planarization process. Ex. 1005, [0193]; *compare id.*, Fig. 18A (pre-planarization interlayer dielectric 130) *with id.*, Fig. 19A (post-planarization pattern 134). Again, a planar top surface facilitates depositing additional components or layers such as interconnection lines WIL above the surface, as shown in Figure 22A. *Id.*, [0209].

102. Kim discloses *forming a plurality of openings* ("contact holes") *in the insulating layer* ("interlayer insulating pattern" 134) *exposing portions of the etch-stop layer* ("etch stop pattern" 126b):

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Ex. 1005, Fig. 22A, [0173]-[0174] ("the formation of word line contact plugs WPLG[s] … include[s] forming contact holes to penetrate the interlayer insulating pattern…."). In a later manufacturing step, these contact holes get filled with a conductive material to become word line contact plugs WPLGs connected to the gate electrodes 161-166 (colored orange above to illustrate the openings). *Id.*, [0173]. Therefore, etching the contact holes involves penetrating the etch-stop layer as shown in Figure 22A.

103. But before the contact holes penetrate the etch-stop layer, they first penetrate *the insulating layer exposing*—but not penetrating—*portions of the etch-*

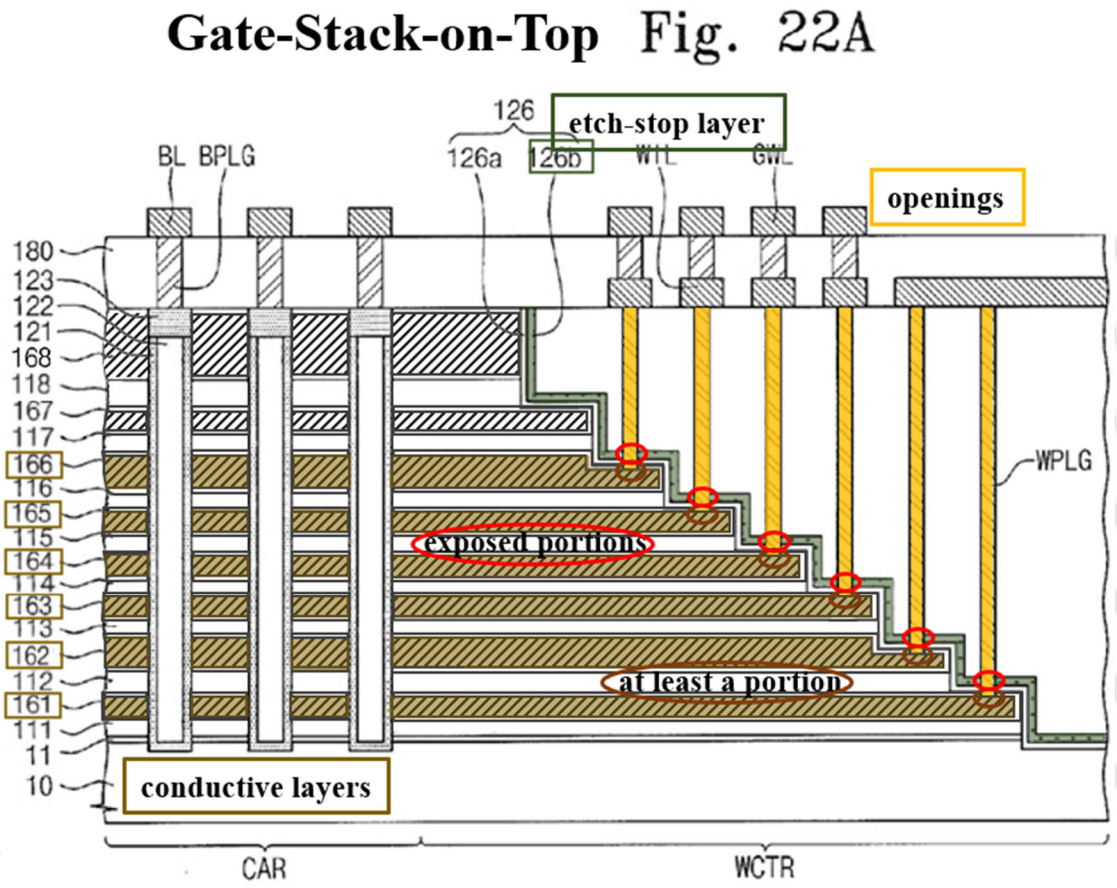
stop layer. This necessarily occurs when the insulating layer is completely removed from any particular contact hole. When that happens, it would have been obvious that *portions of the etch-stop layer* (*i.e.*, its top surface within the contact hole) is *expos[ed]*. Additionally, a POSITA would have recognized this occurrence as the result of a deliberate choice of etch selectivity, with the occurrence happening at the end of an etching stage. Specifically, Kim discloses that "[t]he etch stop layer 125[/126] may be formed of a material having an etch selectivity with respect to the interlayer dielectric 130." *Id.*, [0213]. The relative etch selectivity allow the interlayer dielectric to be etched away while preserving the etch-stop layer. Thus, the etch-stop layer protects the layers beneath and prevents over-etching, especially of shallow openings. Therefore, after the openings reach the etch-stop layer, most of the etch-stop layer would remain, exposing portions of it at the bottom of the openings. After all contact holes reach the etch-stop layer (which involves contact holes of different depths since the etch-stop layer has a stepwise pattern on top of the staircase), etching would continue in a next stage by changing the etchant so that the contact holes may penetrate the etch-stop layer within a reasonable length of time.

7. [1.F] "etching the exposed portions of the etch-stop layer in the plurality of openings and exposing at least a portion of the conductive layer of each step; and"

104. Kim discloses *etching the exposed portions of the etch-stop layer* ("etch

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stop pattern" 126b) *in the plurality of openings* ("contact holes") *and exposing at least a portion of the conductive layer of each step* ("gate electrodes" 161-166):



Ex. 1005, Fig. 22A. After the step of [1.E], etching must continue by penetrating the etch-stop layer because, to form the necessary electrical contact between the conductive structures and the respective conductive layers, the contact holes and the conductive structures to be formed therein must reach the gate electrodes by penetrating the layers above them. *Id.*, [0211] (disclosing contacts between gate electrodes and word line contact plugs WPLGs formed in the contact holes). Therefore, *the exposed portions of the etch-stop layer in the plurality of openings*

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must be etched away and *at least a portion of the conductive layer of each step* must be *expos[ed]*. Such penetration involves successively etching away the etch-stop layer and the layers above the gate electrodes as the contact holes extend to each layer. The successive etching in turn involves choosing relative etch selectivities of the etch-stop layer, the insulating layers, the first high-k dielectric layer (blocking insulating layer in a data-storing layer), and the conductive layers (gate conductive layers 161-166). Kim's disclosures of relative etch selectivities would have confirmed a POSITA's understanding of a successive etch process. *See, e.g.*, Ex. 1005, [0165] (disclosing etch selectivity between data storing layer 150 and gate conductive layers); [0213] (disclosing same between the etch-stop layer and insulating layer).

105. The reverse layer ordering at each step does not materially change Kim's disclosure relevant to this limitation because the function of the WPLGs (formed in the openings) is to electrically connect the gate electrodes with global word lines GWL. *Id.*, [0175], [0210], [0251]-[0252]. I note one difference for completeness. Kim discloses relative etch selectivity between the etch-stop layer and the dielectric layers. *Id.*, [0186]-[0187]. This reflects Kim's default dielectric-layer-on-top configuration in which the dielectric layers are located immediately below the etch-stop layer. For a gate-stack-on-top configuration, a POSITA would have found it obvious that the analogous relative etch selectivity would be between

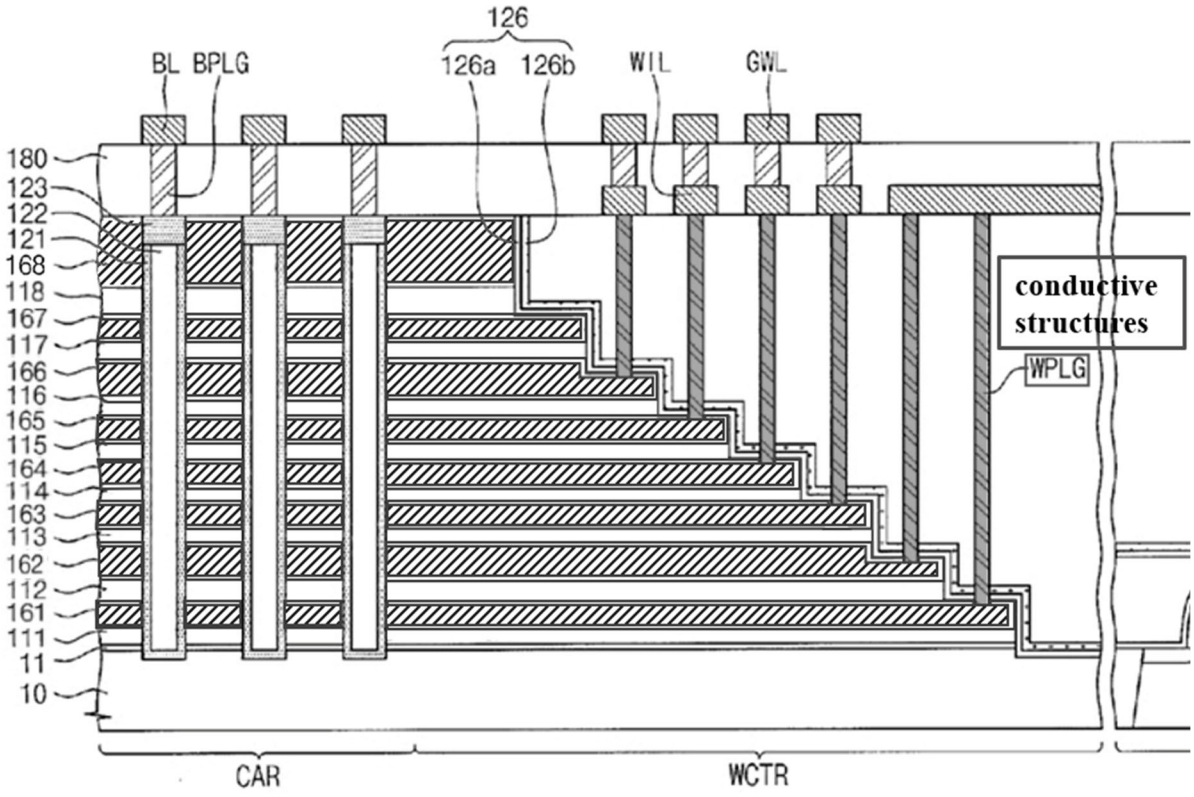
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the etch-stop layer and the first high-k dielectric layer, which is located immediately below the etch-stop layer in the reverse layer order. Given the flexibility in the choices of etchants and layer material (§VIII), choosing an appropriate relative etch selectivity would have been well within the knowledge and skill of a POSITA.

8. [1.G] "forming a plurality of conductive structures in each of the plurality of openings."

106. Kim discloses *forming a plurality of conductive structures* ("WLPG[s]") *in each of the plurality of openings* ("contact holes"):

Gate-Stack-on-Top Fig. 22A



Ex. 1005, Fig. 22A, [0173] ("the formation of word line contact plugs WPLG … may include … filling the contact holes with a conductive material."); *id.*, [0210]-

[0211] (connecting contact plugs with gate electrodes at different heights), [0251]-[0252]. Filling the openings with a conductive material was a common and conventional way to form conductive structures.

C. Claim 2:

1. [2] "The method of claim 1, wherein the forming the plurality of openings comprises performing an etching process on the insulating layer, wherein an etching rate of the insulating layer is higher than an etching rate of the etch-stop layer."

107. Kim discloses the additional limitation of claim 2. Specifically, "[t]he etch stop layer 125[/126] may be formed of a material having an etch selectivity with respect to the interlayer dielectric 130[/134]." Ex. 1005, [0213]. The references to etch selectivity mean *the forming the plurality of openings* ("contact holes") *comprises performing an etching process on the insulating layer* ("interlayer insulating pattern" 134) because that is why etch selectivity is a relevant parameter. Further, a POSITA would have understood that the relative etch selectivity of the etch-stop layer and interlayer dielectric mean that *an etching rate of the insulating layer* ("interlayer insulating pattern" 134) *is higher than an etching rate of the etch-stop layer* ("etch stop pattern" 126b) so that the etch-stop layer 126b would protect its underlying layers and prevent over-etching, especially of shallower openings. §VIII. Indeed, the claimed relation of the two etching rates is the only sensible relation. For example, it would not make sense to have an etch-stop layer with a

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higher etching rate than that of the insulating layer because the former is to protect the underlying layers while the latter is being etched away.

D. Claim 4:

1. [4] "The method of claim 1, wherein etching the exposed portions of the etch-stop layer comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer of each step."

108. It is my opinion that Claim 4 is obvious in view of a POSITA's knowledge. Limitation [1.F] requires that portions of the etch-stop layer in the openings are etched to expose a portion of the conductive layer of each step. §XIII.B.7. One common approach to accomplish this is to extend the etching time to penetrate both the etch-stop layer and the first high-k dielectric layer until the openings reach the conductive layers. Fang, for example, discloses such an approach to etch the etch-stop layer. Ex. 1006, [0029]. Using the same approach to etch the first high-k dielectric layer would have been a suitable option because that layer is typically quite thin and thus can be etched away within a reasonable time even if the etching process does not include a specific step with an etchant chosen to accelerate its etching. But since punch-through of gate electrode layers must be prevented to avoid short circuits, a POSITA would have found it prudent and obvious to slow down etching once it reaches the conductive layer. This means that *the etch-stop layer [has] a higher etching rate than an etching rate of the conductive layer of each*

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step because the etchant is chosen to etch the etch-stop layer. Moreover, because the first high-k dielectric layer is typically quite thin, even when that layer is configured to slow down etching to protect the underlying conductive layer, a POSITA would still have found it desirable to have a conductive layer with low etching rate relative to that of the etch-stop layer. Such relative etch selectivity would have provided additional protection for the conductive layers. Finally, the additional limitation of claim 4 would have been obvious because there are only three possible relationships of one etching rate relative to another: higher, equal, or lower. A POSITA would not have configured the conductive layer to have a higher etching rate than that of the etch-stop layer since the conductive layer should be preserved, an objective calling for a low etching rate. Moreover, since the two layers have different materials, they do not have equal etching rates. Thus, the only remaining possibility is the claimed relationship, *i.e.*, *the etch-stop layer [has] a higher etching rate than an etching rate of the conductive layer of each step*. As an example, a silicon nitride etch-stop layer has a higher etching rate than metal conductive layers relative to SF_6 and C_4F_8. Wang discloses a method of anisotropic dry etching with this chemistry that "achieve[s] vertical etching sidewalls." Ex. 1023, 1.

109. The conductive layer needs to be preserved for word line contacts regardless of the layer ordering at each step. The reverse order of the layers at each

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step, upon which the above analysis is based, makes the additional limitation of Claim 4 more obvious than the other order. In Kim's default dielectric-layer-on-top configuration, a dielectric layer resides between the etch-stop layer and the gate stack and provides additional protection for the gate stack when the etch-stop layer is etched. But in the gate-stack-on-top configuration relevant here, the gate stack resides immediately below the etch-stop layer. Thus, the claimed etch selectivity would have been obvious as discussed above.

E. Claim 5:

1. [5] "The method of claim 4, wherein etching the exposed portions of the etch-stop layer further comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the first high-k dielectric layer."

110. It is my opinion that Claim 5 is obvious in view of a POSITA's knowledge. Since punch-through of gate electrode layers must be prevented (which is the objective of prior art including Kim), a POSITA would have found it desirable to further protect the gate electrode layer in addition to relying on the layers' low etching rate. This further protection would have been prudent because the etching process involves many parameters that cannot be perfectly or completely controlled. As a result, deviations from the intended etching outcome are possible, for example etching might proceed faster than intended, and the further protection could guard against such deviations. Accordingly, the first high-k dielectric layer may be

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advantageously used as an etch stop to protect the conductive layer below. That means that *the etch-stop layer [has] a higher etching rate than an etching rate of the first high-k dielectric layer*. §VIII. Further, as in Claim 4, a POSITA would have recognized that only the claimed relative etching rates have a sensible relationship. The etch-stop and the first high-k dielectric layers do not have equal etching rate since they comprise different materials, silicon nitride for the etch-stop layer and one of many high-k dielectric materials for the blocking insulating layer. Ex. 1005, [0151], [0187]. And it would not have made sense to choose an etchant/etching process such that the etch-stop layer would have a lower etching rate than that of the first high-k dielectric layer because the etch-stop layer is thicker and because it is desirable for the first high-k dielectric layer to serve as an etch stop to protect the gate conductive layer when the etch-stop layer is etched. That leaves only one alternative: *the etch-stop layer [has] a higher etching rate than an etching rate of the first high-k dielectric layer*. As an example, selective etching of silicon nitride relative to aluminum oxide was well known. Williams discloses using "aluminum oxide as an etch-stop interlayer [to] enable[] selective removal of the silicon nitride dielectric layer." Ex. 1024, [0017]. Dry etch may be used, and "the etch process etches away the silicon nitride at a rate significantly greater than that to the aluminum oxide." *Id.*, [0029].

111. The reverse order of the layers at each step renders the additional

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limitation of this claim obvious. In Kim's default dielectric-layer-on-top configuration, a dielectric layer resides between the etch-stop layer and the gate stack and provides the further protection discussed above. Accordingly, Kim discloses relative etch selectivity between the etch-stop layer and the dielectric layers. Ex. 1005, [0186]-[0187]. In the reverse gate-stack-on-top order, the etch-stop layer is positioned directly above the first high-k dielectric layer of the gate stack. Thus, a POSITA would have found it obvious that the analogous relative etch selectivity would be between the etch-stop layer and the first high-k dielectric layer. Given the flexibility in the choices of etchants and layer material (§VIII), choosing an appropriate relative etch selectivity would have been well within the knowledge and skill of a POSITA.

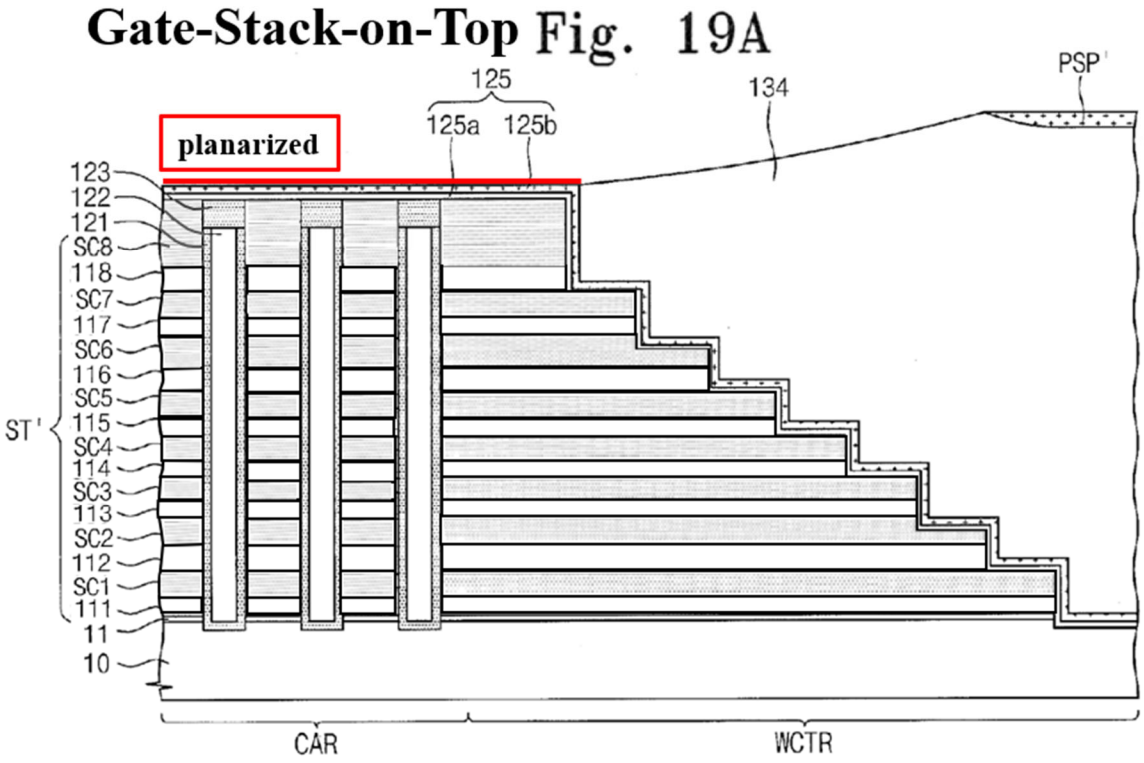
F. Claim 9:

1. [9] "The method of claim 1, further comprising: after disposing the insulating layer on the etch-stop layer, planarizing the insulating layer and the staircase structure by using chemical-mechanical-polishing (CMP)."

112. Kim discloses the additional limitation of claim 9. Specifically, Figures 19A-19B show the word line contact structure *after disposing the insulating layer on the etch-stop layer* (that is, after the step of limitation [1.C], §XIII.B.4). Kim states "[r]eferring to FIGS. 19A and 19B, a planarization process on the interlayer dielectric 130 [*the insulating layer*] may be performed using a *chemical mechanical*

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polishing (CMP) technique." Ex. 1005, [0191], [0104] (similar), [0118] (similar). CMP was conventional for planarizing surfaces by the time of the '276 Patent. *[T]he staircase structure* is *planariz[ed]* as well:



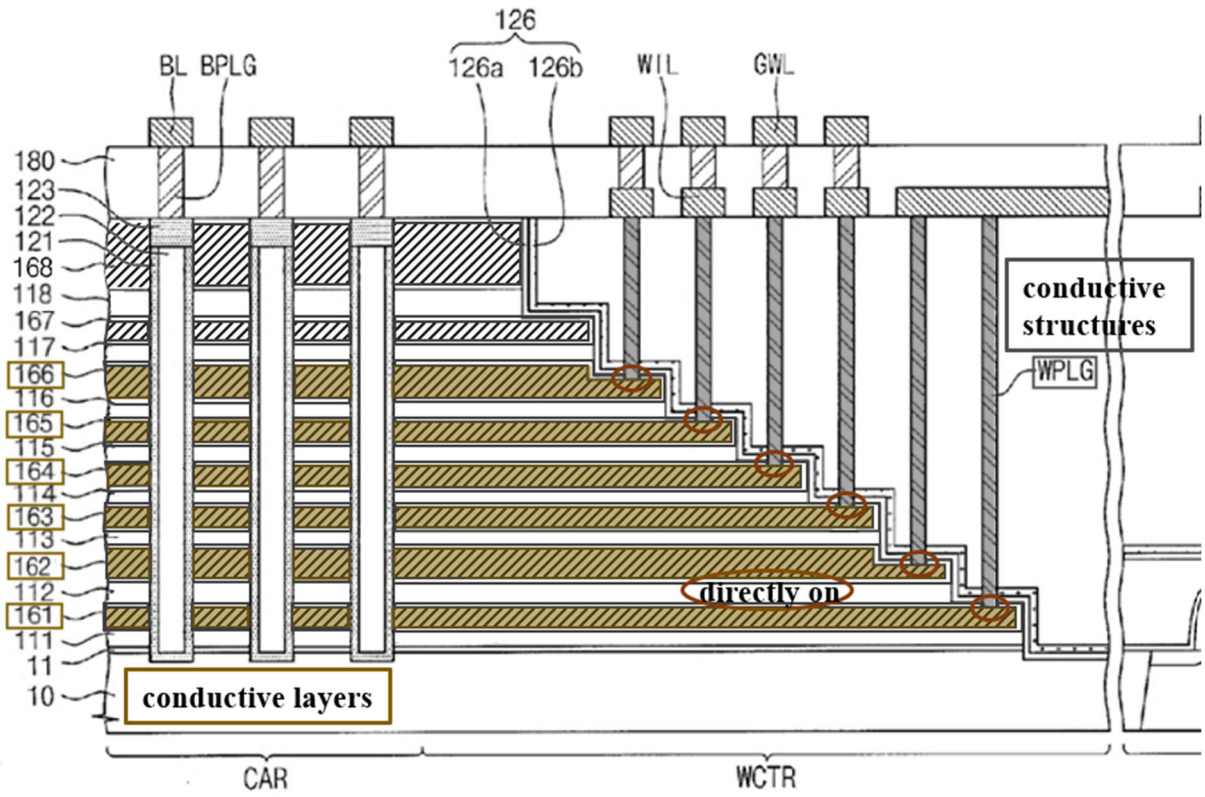
Id., Fig. 19A; *see also* §XIII.H.1 (showing coplanar top surfaces of the etch-stop layer and the insulating layer). A comparison of Figures 18A, 19A, and 20A reveals the extent of the planarization process. A planar top surface is desirable for depositing additional layer on top. For example, as shown in Figure 22A, interconnection lines WIL (Ex. 1005, [0209]) are laid on top of the insulating layer. A planar top surface helps to secure those lines in place.

G. Claim 10:

1. [10] "The method of claim 1, wherein forming the plurality of conductive structures comprises disposing conductive materials inside the plurality of openings, the conductive materials directly on the exposed conductive layer of the each step."

113. Kim discloses *forming the plurality of conductive structures* ("WPLG[s]") *comprises disposing conductive materials inside the plurality of openings* ("contact holes"), *the conductive materials directly on the exposed conductive layer* ("gate electrodes" 161-166) *of the each step*:

Gate-Stack-on-Top Fig. 22A



Ex. 1005, Fig. 22A, [0173] ("filling the contact holes with a conductive material."). The additional limitation of Clam 10 would have been obvious to a POSITA because it is needed for the very purpose of the conductive structure, to connect the gate layers to the control voltage. *Id.*, [0210]-[0211] ("WPLG may be formed to connect the global word lines GWL and the gate electrodes 161 to 168.").

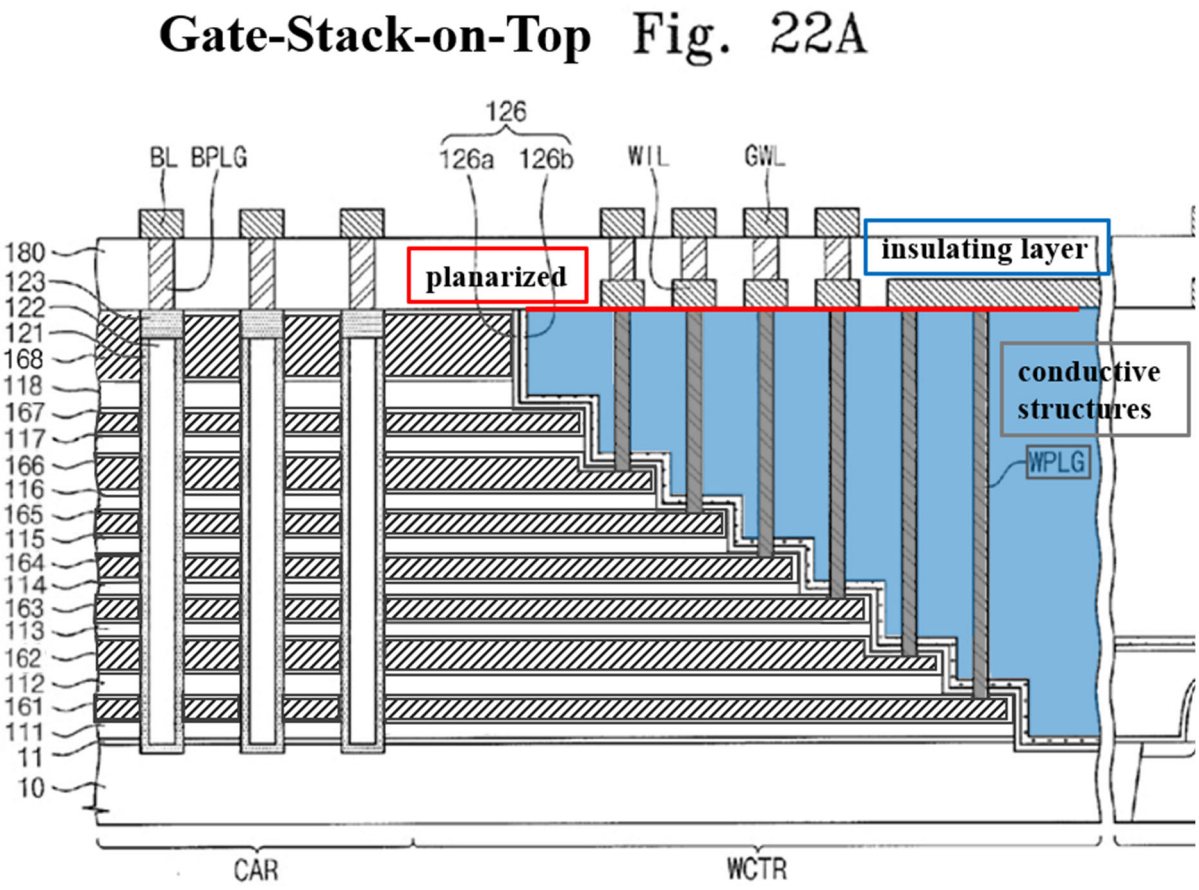
114. The layer ordering at each step does not impact this explanation because direct contacts between WLPGs and the gate electrodes are needed for the word lines to function regardless of the layer ordering. The only difference is whether the WLPGs would penetrate dielectric layers in the stack to reach the gate electrodes, something Claim 10 does not explicit address.

H. Claim 11:

1. [11] "The method of claim 1, wherein forming the plurality of conductive structures further comprises planarizing the conductive materials and the insulating layer."

115. It is my opinion that Kim at least renders obvious *forming the plurality of conductive structures* ("WPLG[s]") *further comprises planarizing the conductive materials* (of "WPLG[s]") *and the insulating layer* ("interlayer insulating pattern" 134). This can be observed in Figure 22A:

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Ex. 1005, Fig. 22A.

116. A POSITA would have understood that a planar top surface is advantageous and required for forming the word line connecting lines (WIL in Figure 22A) on the surface. Ex. 1005, [0209]. This is consistent with Kim's planarizing the top surfaces of other components. Ex. 1005, [0119], [0206]. From a practical standpoint, the top surface above the stack must be planar. This is because the upper-level metal layers must be highly planar, otherwise, there will be challenges patterning them due to depth of focus issues during optical lithography. There will also be challenges etching the metal interconnects on non-planar

topographies. Depending on the layout, there can be residual metal filaments or "stringers" at notches in the underlying topography, leading to electrical shorts. The interface to the metal layers must be planar, and each metal layer itself must be planar. Thus, such filling insulators are understood to surround the stack structures to create a planar surface for the upper-level metal layer. Ex. 1021, 14. 113. Thus, a POSITA would have understood this limitation, or at least found it obvious.

I. Claim 12:

1. [12] "The method of claim 1, wherein forming the staircase structure further comprises performing a repetitive etch-trim process on the sacrificial layers and the dielectric layers."

117. Kim discloses *forming the staircase structure* ("stepwise stacked layer structure ST′") *further comprises performing a repetitive etch-trim process on the sacrificial layers* ("sacrificial layers" SC1-SC6) *and the dielectric layers* ("insulating layers" 111-116).

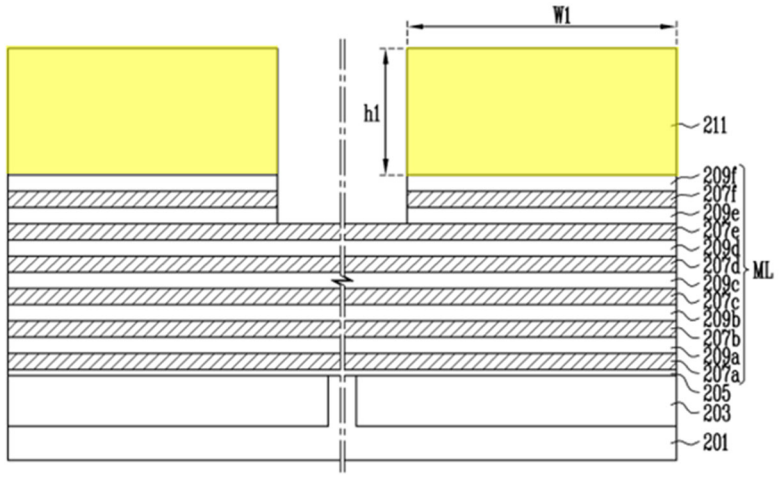
118. Specifically, Kim discloses that "the patterning of the stepwise stacked layer structure ST′ may include steps of reducing a horizontal area occupied by a mask pattern MP and etching the stacked layer structure ST, which are alternately performed." Ex. 1005, [0087], [0182]. That reduction of the horizontal area is a conventional mask trimming process, which the '276 Patent describes as a "lateral pull-back." Ex. 1001, 7:19-28. Thus, the two alternately performed steps constitutes

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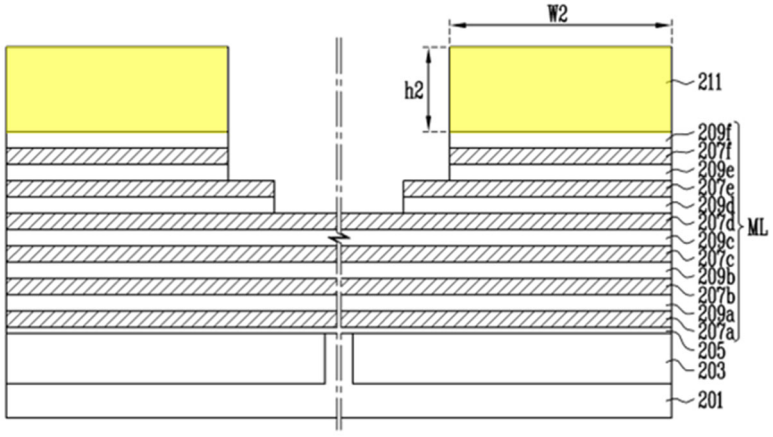
a *repetitive etch-trim process*. Ex. 1005, [0182].

119. In this process, the unmasked portion of the stack is etched, the mask is trimmed, and the process is repeated. This is illustrated in the following sequence of figures:

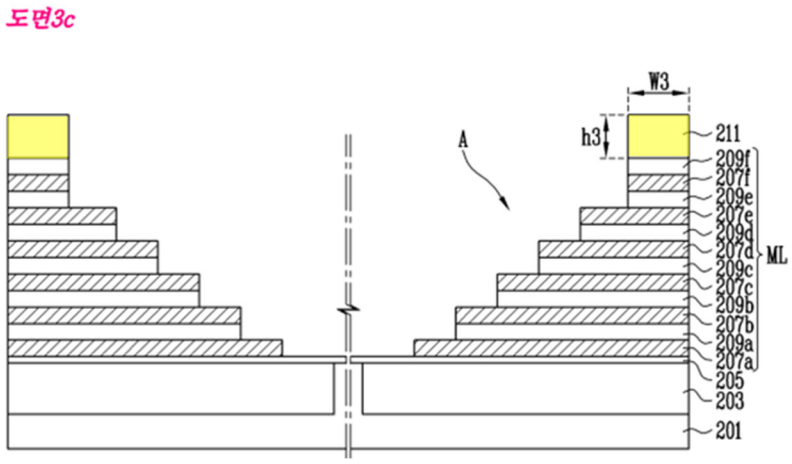
도면3a



도면3b



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Ex. 1020, Figs. 3a-3c. As this reference demonstrates, the process was well known in the art.

120. As illustrated above, the mask pattern protects the area it covers from etching. The area not covered by the mask pattern is etched. After a depth of a *sacrificial layer[]* and a *dielectric layer[]* is etched away in the exposed area, forming a step, the mask-pattern area is reduced or trimmed. Etching is repeated and a larger exposed area is etched away, forming one more step and reducing the heights of existing steps by a predetermined depth. By repeating this process, *the staircase structure* is formed. Ex. 1005, [0089]-[0090]. The layer ordering at each step does not affect this analysis because the same etching process is configured to remove both sacrificial and dielectric layers of the stack. *Id.*

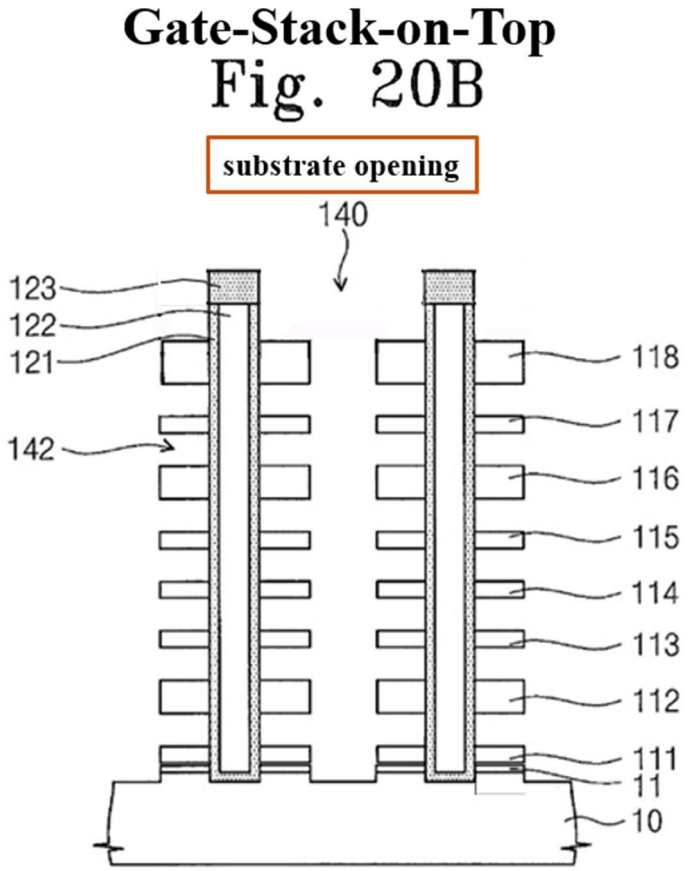
J. Claim 13:

1. [13.PRE] "The method of claim 1, wherein replacing the sacrificial layer of each step with the gate stack comprises:"

121. This preamble simply repeats limitation [1.D]. §XIII.B.5.

2. [13.A] "forming a substrate opening through the staircase structure;"

122. Kim discloses *forming a substrate opening* ("trench" 140) *through the staircase structure*:



Ex. 1005, Fig. 20B, [0198]-[0199] ("The formation of the gate electrodes … may include forming the trenches 140 … and replacing the sacrificial layers…."). Such a replacement process was conventional in the art. The layers in the stack would be chosen such that the dielectric layers are etch resistant to the etchant used to remove the sacrificial layers. *Id.*, [0064] ("The insulating layers 111 to 118 and the

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sacrificial layers SC1 to SC8 may be formed of materials having an etch selectivity with respect to each other in a subsequent wet etching process."). Trench 140 constitutes a substrate opening because its opening extends to the substrate surface. *Id.*, [0199]. That matches the '276 Patent's substrate opening. Ex. 1001, 8:45-53 ("a substrate opening 522 is formed … by etching through the entire film stack …, exposing the surface of the substrate 101."). Additionally, a POSITA would have understood that trench 140 must extend into the substrate, because the structure to be formed in the trench provides a connection to a doped region of the substrate that serves as the common source line. Ex. 1005, [0203]-[0204] ("a vertical conductive pattern 156 may be formed in the trench 140. The vertical conductive pattern 156 may be electrically coupled to the doped region 15" "serving as the common source line").

3. [13.B] "removing the sacrificial layer of each step through the substrate; and"

123. Preliminarily, *the substrate* appears to be an error. The logical and technical antecedent recited in limitation [13.A] recites a *substrate opening*, which matches the description of the specification. §XIII.J.2; Ex. 1001, 8:45-53, 12:29-36. I have been instructed to treat the term as *the substrate opening* for the purpose of this Proceeding.

124. Kim discloses *removing the sacrificial layer* (one of "sacrificial layers"

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SC1-SC6) *of each step through the substrate [opening]* ("trench" 140). Specifically, Kim's process involves "selectively removing the sacrificial layers … exposed by the trenches 140 to form recess regions 142 between the patterned insulating layers…." Ex. 1005, [0140], Figs. 20A-20B; *id.*, [0142], [0200]. A POSITA would have understood that the trenches 140 are formed to expose the sacrificial layers for the purpose of removing those layers through the trenches, as was conventional and well known. The layer ordering at each step does not impact this explanation because the different ordering simply shifts the heights of the sacrificial layers and does not alter their exposure through the trenches.

4. [13.C] "disposing the first high-k dielectric layer and the conductive layer in place of the sacrificial layer."

125. Kim discloses *disposing the first high-k dielectric layer* ("blocking insulating layer" 150c of "data storing layer" 150) *and the conductive layer* (one of "gate electrodes" 161-166) *in place of the sacrificial layer* (corresponding one of "sacrificial layers" SC1-SC6). This is done through "forming a data storing layer 150 and gate electrodes 161 to 168 in the recess regions 142." Ex. 1005, [0200]; §XIII.B.5 (showing sequence of replacing the sacrificial layers with the gate stacks); Ex. 1005, [0202], [0144], [0148] ("the data storing layer 150 may include … a blocking insulating layer 150c…."), [0198]. It was conventional to form the data-storing layer for the memory cells after the recess regions are formed. The data-

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storing layer (or a sub-layer) would also be formed in the stack between the dielectric layers in the same process. Having this high-k dielectric layer around the gate stack can provide an additional protective layer around the gate electrodes. At a minimum, having this high-k dielectric layer does not affect the functioning of the device since the gate electrodes are surrounded by insulators/dielectrics with or without the high-k dielectric layer. The layer ordering at each step does not affect this analysis because a different order merely changes the relative layer positions at each step, which does not matter to this processing stage.

K. Claim 14:

1. [14] "The method of claim 13, wherein disposing the first high-k dielectric layer comprises disposing hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide and/or any combination thereof."

126. Kim discloses that *disposing the first high-k dielectric layer* ("blocking insulating layer" 150c) *comprises disposing hafnium oxide, zirconium oxide, aluminum oxide, [or] tantalum oxide…*. Specifically, "[t]he blocking insulating layer 150c may include … [a] high-k dielectric, … e.g., tantalum oxide, … , hafnium oxide, zirconium oxide, [or] aluminum oxide…." Ex. 1005, [0151]. A high-k dielectric layer for data-storing layer was well known by the time of the '276 Patent.

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L. Claim 15:

1. [15] "The method of claim 13, wherein disposing the conductive layer comprises disposing tungsten, cobalt, nickel, copper, aluminum, and/or any combination thereof."

127. Kim discloses that *disposing the conductive layer* (one of "gate conductive layers" 161-166) *comprises disposing tungsten….* Specifically, "[t]he gate conductive layer may include … tungsten…."). Ex. 1005, [0157]; §XIII (description of Figures 5A-14B applies). Tungsten is a suitable metal because, unlike other metals like copper, it does not easily diffuse and contaminate and degrade surrounding materials.

M. Claim 16:

1. [16] "The method of claim 13, wherein disposing the conductive layer comprises disposing poly-crystalline silicon, poly-crystalline germanium, or poly-crystalline germanium-silicon."

128. Kim discloses that *disposing the conductive layer* ("gate conductive layers" 161-166) *comprises disposing poly-crystalline silicon….* Specifically, "[t]he gate conductive layers 101 to 108 may be a polysilicon…." Ex. 1005, [0230] §XIII (Kim's descriptions apply to common aspects across embodiments). Though less conductive than metal, polysilicon is nonetheless a suitable conductor.

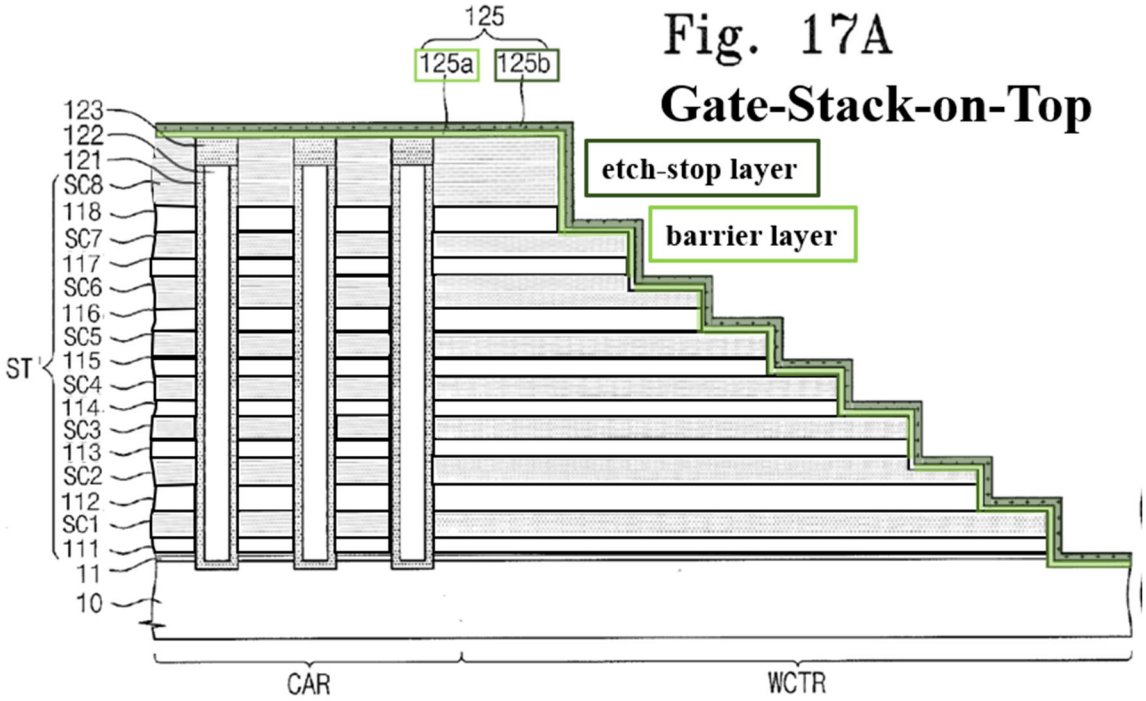
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N. Claim 17:

1. [17] "The method of claim 1, further comprising: prior to disposing the etch-stop layer, disposing a barrier layer on each step of the plurality of steps, wherein the barrier layer protects underlying structures during the etching of the exposed portions of the etch-stop layer."

129. It is my opinion that Kim at least renders claim 17 obvious.

130. Kim discloses that *prior to disposing the etch-stop layer* ("second stop layer" 125b)*, disposing a barrier layer* ("first stop layer" 125a) *on each step of the plurality of steps*. This can be observed in Figure 17A, in which the first stop layer 125a is deposited before and therefore positioned below the second stop layer 125b:



Ex. 1005, Fig. 17A, [0185], [0187] (describing the sequence of forming conformal layers 125a and 125b).

131. Kim renders obvious that *the barrier layer* ("first stop layer" 125a) *protects underlying structures*. I explained above that a barrier layer of the '276 Patent is simply another etch-stop layer. §IX. Kim discloses etching selectivity of its etch-stop layer 125 and etching selectivities of the first stop layer 125a and 125b. Ex. 1005, [0186]-[0187]. Indeed, the etching profiles of the first and second stop layers 125a-125b together match that of the single etch-stop layer 125. *Id.*, [0187]. Accordingly, it would have been obvious that the first stop layer 125a would perform part of the function of the etch-stop layer 125, which includes *protect[ing] underlying structures during ... etching*. Moreover, using the first stop layer 125a as an etch stop would have been prudent and obvious because it is positioned immediately above the gate stack (the punch through of which is to be avoided) in the gate-stack-on-top configuration. Process variations and imperfections would have made it desirable to use the first stop layer 125a as an etch stop as additional guard against inadvertent defects.

132. It would have been also obvious that this protection includes that *during the etching of the exposed portions of the etch-stop layer*. In general, to prevent over-etching, a lower layer has an etching rate lower than the upper layer above it and the two layers cannot have the same material (which would mean the same etching rate). §VIII. Kim discloses exactly that: "the first stop layer 125a may be formed of silicon oxide and the second stop layer 125b may be formed of silicon

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nitride." Ex. 1005, [0187]. The flexibility in the choice of etchants and the availability of selective etching and reverse selective etching (§VIII, citing Ex. 1015) would have rendered it obvious to a POSITA that the first stop layer could have a lower etching rate than the second stop layer, thereby slowing down etching when the second stop layer is penetrated. A POSITA would have further found it obvious that the first stop layer should preferably have a lower etching rate for the reasons I explained in the previous paragraph. Therefore, it would have been obvious that the first stop layer *protects underlying structures during the etching of the exposed portions of the etch-stop layer*.

O. Claim 18:

1. [18] "The method of claim 17, wherein disposing the barrier layer comprises disposing one or more of silicon oxide, silicon oxynitride, silicon nitride, TEOS, aluminum oxide, and silicon oxide incorporated with F, C, N, or H."

133. Kim discloses that *disposing the barrier layer* ("first stop layer" 125a) *comprises disposing … silicon oxide…*. Specifically, "the first stop layer 125a may be formed of silicon oxide." Ex. 1005, [0187]. Again, the material of the barrier layer should be, and is. different from that of the etch-stop layer for the barrier layer to function as an etch stop when the etch-stop layer above is etched.

XIV. GROUND 2: KIM IN VIEW OF FANG

134. In addition to Claims 3 and 6-8 not included in Ground 1, I explain in Ground 2 an alternative combination against all Ground 1 claims. Specifically, Fang

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discloses a high-k dielectric etch-stop layer under what a POSITA would consider to be the correct scope of limitation [1.B]. Explanations of other claims and limitations in Ground 1 are unchanged and so I will not repeat them.

A. Claim 1:

1. [1.B] "disposing an etch-stop layer on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer;"

135. Kim discloses *disposing an etch-stop layer on each step of the plurality of steps*. §XIII.B.3. Fang discloses that *the etch-stop layer comprises a second high-k dielectric layer* under a correct interpretation of high-k dielectric. Specifically, Fang discloses that its etch-stop layer "may be a high-k dielectric material, such as hafnium oxide." Ex. 1006, [0022]. A POSITA would consider high-k dielectric to comprise materials with a dielectric constant higher than that of silicon nitride. Typically such high-k dielectrics have a dielectric constant greater than 9. Hafnium oxide has a dielectric constant greater than 15, *e.g.*, 16-25. Kim in view of Fang thus renders this limitation obvious under its correct scope.

B. Claim 3:

1. [3] "The method of claim 2, wherein the etching process comprises anisotropic dry etching."

136. Kim in view of Fang renders obvious claim 3.

137. *[T]he etching process* is performed on the insulating layer in forming the plurality of openings. §XIII.C. Fang discloses "[o]penings 145 may be formed

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in the another oxide material 135," which is equivalent to the insulating layer of the '276 Patent. Ex. 1006, [0027]-[0028].

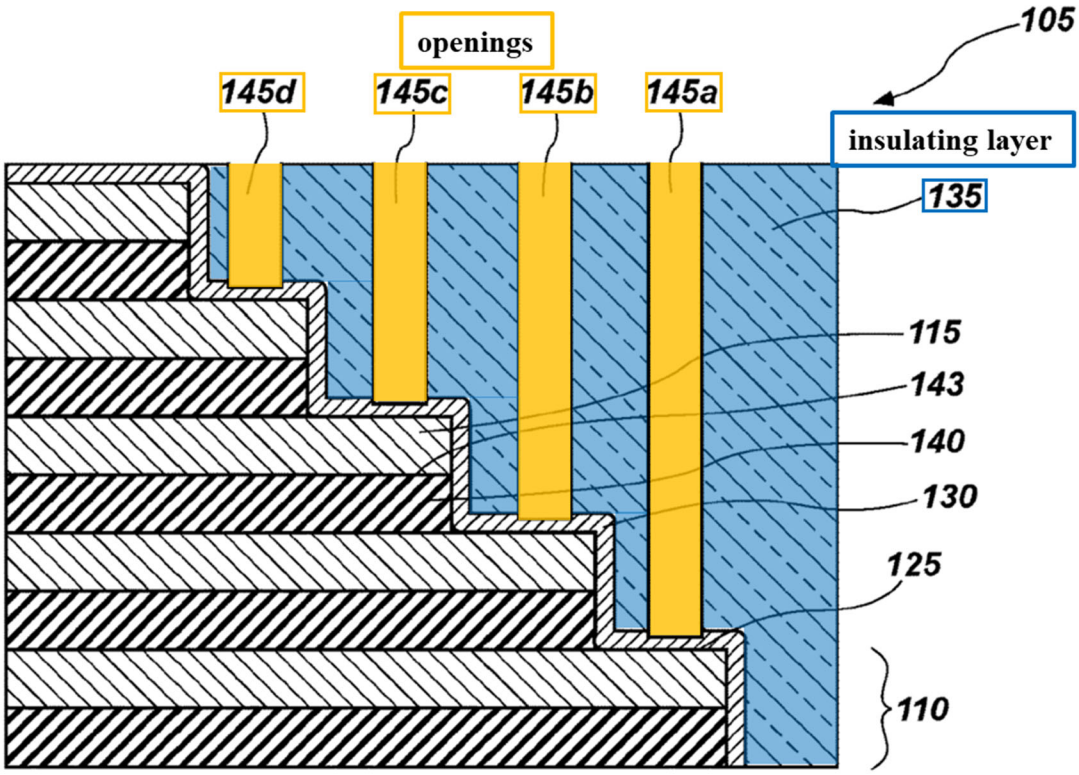


FIG. 5

Ex. 1006, Fig. 5. *Anisotropic dry etching* may be used during this *etching process*. *Id.*, [0028], [0008], [0020]. This etching process was conventional and would have been a suitable process for etching small but deep openings due to its directionality.

138. Kim also uses anisotropic etching. For example, the substrate openings 120 and the trenches 140 may be formed via anisotropic etching. Ex. 1005, [0070], [0199], Figs. 6A, 12B. A POSITA would have understood these disclosures to refer to anisotropic dry etching because of the directionality required to etch small but

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deep vertical holes. Since Kim already uses this process, applying the same process to etch the insulating layer would have been an obvious, suitable choice. Doing so would have been nothing more than applying what Kim already uses on an additional layer. Indeed, the substrate openings, the trenches, and the openings for conductive structures all have similar profiles or aspect ratios. Such similarity would have provided a POSITA a reasonable expectation of success.

C. Claim 6:

1. [6] "The method of claim 1, wherein disposing the etch-stop layer comprises disposing hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, and/or any combination thereof."

139. It is my opinion that Kim in view of Fang renders obvious claim 6. Specifically, Fang discloses that *the etch-stop layer* may comprise silicon nitride or, "[a]lternatively, … a high-k dielectric material, such as *hafnium oxide*." Ex. 1006, [0022]. A POSITA would have understood both materials to meet Fang's criterion of not removing the etch-stop material when removing the sacrificial layer nitride materials. *Id.*, [0025]. Otherwise Kim would not have disclosed them as alternatives. And the flexibility in choice of etchants would have made the various alternatives suitable to function as an etch-stop layer. Like Fang, Kim discloses silicon nitride as a material for the etch-stop layer. Ex. 1005, [0186]. Thus, applying Fang's "alternative[]" to silicon nitride (Ex. 1006, [0022]) represents nothing more

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than applying the same alternative toward Kim's similar device in the same way.

D. Claim 7:

1. [7] "The method of claim 1, wherein disposing the etch-stop layer comprises disposing the etch-stop layer with a thickness in a range between 10 nm to 100 nm."

140. As an initial matter, as the Examiner correctly noted, "the specification … reveals no particular benefit to any particular thickness." Ex. 1002, 92 (citing the equivalent of Ex. 1001, 7:62-8:25). Instead, the patent specification just includes a long list of permissible thicknesses and further states that permissible ranges include "any range defined by any two of these values." Ex. 1001, 7:62-8:3. That translates to hundreds of permissible ranges, with no apparent benefit or advantage to any particular range. And the cited range— *between 10 nm to 100 nm* and spanning orders of magnitude—indicates that no particular thickness "is particularly critical." Ex. 1002, 92-93. Moreover, the '276 Patent provides no guidance on how to choose among the hundreds of permissible ranges, or why one might be more suitable than another for a given scenario. It is my understanding that such a claim to dimensions that have no performance benefits is not patentable.

141. I was asked to nonetheless opine on the obviousness of Claim 7. It is my opinion that Kim in view of Fang renders Claim 7 obvious. Fang discloses an semiconductor structure analogous to Kim's with an etch-stop layer. Ex. 1006, Fig. 6, [0020]. A POSITA would have found it obvious to apply Fang's disclosed

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thickness to Kim's device. To begin, Kim's and Fang's etch-stop layers are similar. For example, both of their etch-stop layers may comprise silicon nitride. Ex. 1005, [0187]; Ex. 1006, [0022]. Fang's alternative of a high-k dielectric etch-stop layer could have been an alternative for Kim. §XIV.C.1. Fang's etch-stop layer "may be formed by conventional techniques…." Ex. 1006, [0020]. It would have been obvious that such conventional techniques could form Kim's etch-stop layer because such techniques were known to be suitable for depositing conformal layers, such as an etch-stop layer over a staircase structure. Additionally, Fang's disclosed thickness range may be adjusted based on Kim's staircase structure. Fang's layer "may be formed over the stairs 125 at a thickness ranging from about 50 Å to about 1000 Å," or about 5 nm to 100 nm. *Id.*, [0021]. This etch-stop-layer thickness withstands etching of contact holes with depths "from about 1 μm to about 15 μm." *Id.*, [0030]. The height of Kim's staircase structure, and thus the approximate depth of its deepest contact hole, ranges from "about 10,000 Å to about 40,000 Å," or about 1 μm to about 4 μm. Ex. 1005, [0068]. Thus, a POSITA would have found it obvious that Fang's disclosed maximum thickness may be decreased proportionally to 26.7 nm (100 nm / 15 μm * 4 μm) to account for the shallower holes required for Kim's staircase structure when applying those teachings to specify Kim's etch-stop thickness. Both Fang's disclosed thickness range and the adjusted thickness range

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overlap with the claimed *range between 10 nm and 100 nm*.[5] And as just demonstrated through the simple scaling computation, such an adjustment would have been well within the knowledge and skill of a POSITA. Thus, Kim in view of Fang renders claim 7 obvious.

E. Claim 8:

1. [8] "The method of claim 1, wherein disposing the etch-stop layer comprises performing chemical vapor deposition (CVD), physical vapor deposition (PVD), sputtering, atomic layer deposition (ALD), spin-coating, or any combination thereof."

142. It is my opinion that Kim in view of Fang renders obvious Claim 8.

143. Fang discloses forming the etch-stop layer using "conventional techniques including, but not limited to, *chemical vapor deposition (CVD), physical vapor deposition (PVD)*, *atomic layer deposition (ALD)*, or a diffusion process." Ex. 1006, [0020].

144. Kim's method also uses at least CVD and ALD processes. *See* Ex. 1005, [0079], [0236]. Thus, applying CVD or ALD toward *disposing the etch-stop layer* represents nothing more than applying a known technique that Kim already

[5] Claim 7 is directed toward a semiconductor structure with only an etch-stop layer and without an optional barrier layer. *See* Ex. 1001, claims 1, 17. A single layer is what Fang discloses. Ex. 1006, Fig. 6.

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uses. Furthermore, these conventional techniques were known to be suitable for depositing conformal layers, such as an etch-stop layer over a staircase structure. Using such a suitable and conventional technique would have provided a POSITA a reasonable expectation of success.

F. Motivation to Combine

145. In addition to the reasons already stated above in this Ground, it is my opinion that a POSITA would have been motivated to combine Fang's disclosure related to the etch-stop layer and contact-hole etching on Kim's word line structure and would have had a reasonable expectation of success in doing so. The reasons stated above include (1) Kim and Fang both use anisotropic dry etching to form openings of similar profiles (§XIV.B.1); (2) Fang's disclosure of an etch-stop material as an alternative to silicon nitride, which both Kim and Fang disclose to be a suitable etch-stop material (§XIV.C.1); (3) the similarities between Kim's and Fang's etch-stop disclosures and their implication on the thickness of the layer (§XIV.D.1); (4) Kim and Fang both use conventional deposition methods including CVD and ALD suitable for depositing a conformal etch-stop layer (§XIV.E.1). I will explain additional reasons that would have motivated a POSITA to combine Kim and Fang and provided a reasonable expectation of success.

146. Kim focuses on the issue of planarizing the interlayer dielectric to reduce the height difference between the cell array region and peripheral circuit

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region. Ex. 1005, [0024]-[0025]. Therefore, Kim does not state in detail certain aspects of the word line contact region WCTR that were well-known in the art. On the other hand, Fang focuses on preventing over-etching shallower openings when etching openings for the word line conductive structures. Ex. 1006, [0004], [0008]. A POSITA would have known that Fang's focus is an important consideration for manufacturing 3D memory devices and dovetails with Kim's focus to "reduce or prevent damage[s]" to the device during manufacturing. Ex. 1005, [0027]. In a sense, Fang can be considered to disclose a building block of Kim's device. Therefore, a POSITA would have considered Fang's teaching in implementing Kim's device. Moreover, a POSITA would have known that the thickness and material of an etch-stop layer are at least necessary (but routine) design parameters and may be important to its purpose of preventing punch-through to underlying layers. Therefore, a POSITA would have been motivated to adapt Kim's etch-stop layer in view of Fang.

147. Along with those parameters, a POSITA would have also considered Fang's techniques for forming the etch-stop layer and etching the insulating layer for a comprehensive treatment of the related subject matter. A POSITA would have understood Fang's techniques are compatible with and suitable for Kim's similar device. Indeed, Fang simply applies techniques that Kim already uses. §§XIV.B.1, XIV.E.1. Therefore, a POSITA would have found adopting Fang's techniques to be

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cost effective because it merely expands the use of Kim's existing techniques to another layer.

148. Furthermore, adopting the techniques that Kim already uses would have increased a POSITA's expectation of success because they are already used in Kim, in addition to being conventional. Additionally, adopting Fang's etching and deposition techniques and alternative material for the etch-stop layer represents applying what is already known to work in Fang's similar device. Thus, a POSITA would have had a reasonable expectation of success in adopting them for Kim. Indeed, all of these techniques and materials were common, routine, and well known, and it would have been a trivial task for a POSITA to employ them on Kim's device.

149. A POSITA would also have had a reasonable expectation of success in applying Fang's etch-stop-layer thickness to Kim because Fang's range (5-100 nm, or 5-26.7 nm adjusted) was reasonable, especially in light of the additional flexibility provided by other process parameters as explained above. Such additional flexibility also makes the required thickness more flexible, increasing the likelihood that some thickness within the wide range claimed by the '276 Patent would work well with Kim's device. Further, a POSITA would have had a reasonable expectation of success because of similarities between Kim's and Fang's disclosures regarding the etch-stop layer. For example, Kim discloses that its "etch stop layer 125 may be formed of a material having an etch selectivity with respect to the interlayer

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dielectric 130." Ex. 1005, [0213]. Fang discloses the same. Ex. 1006, [0020] ("The etch stop material 130 may also be substantially resistant to dry etch chemistries used to form openings 145 [through the insulating layer.]."). Kim discloses that its "second stop layer 125b may be formed of silicon nitride." Ex. 1005, [0187]. So does Fang. Ex. 1006, [0020]. A POSITA would have expected such similarities since Kim's and Fang's devices are analogous.

150. More generally, a POSITA would have had a reasonable expectation of success because both Kim and Fang are directed to similar 3D memory devices with staircase word line structures, for example, both comprising alternating conductive and dielectric layers at each step, an etch-stop layer and an insulating layer on the steps, and conductive structures penetrating various layers to form contacts with the conductive layers. Again, a POSITA would have expected such similarities since Kim's and Park's devices are analogous. These components and the structure itself were routine and conventional, well within the knowledge of a POSITA.

151. Additionally, a POSITA would have been motivated to use Fang's "[a]lternative[]" material, *i.e.*, a high-k dielectric material such as hafnium oxide, for the etch-stop layer. Ex. 1006, [0022]. Prior art Chen discloses increasing the tunneling length of the etch-stop layer to reduce tunneling current, thereby "more effectively electrically isolat[ing] [the conductive layers] from one another." Ex. 1008, [0004]. The opposite effect, that is, reduced electrical isolation between

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conductive layers, is problematic for the operation of the 3D memory device. As explained and using a read operation as an example, the control gate voltage of the target memory cell is chosen relative to a threshold voltage to determine the programmed state of the cell. §VIII. And the target would move from cell to cell in successive cycles to retrieve the information to be read. *Id.* A short circuit between two gate electrodes caused by insufficient electrical isolation would mean that the corresponding cells cannot be read correctly. A high-k dielectric etch-stop layer has a greater tunneling length (L2 in Figure 8B) compared to that of a silicon nitride etch-stop layer (L1 in Figure 8A):

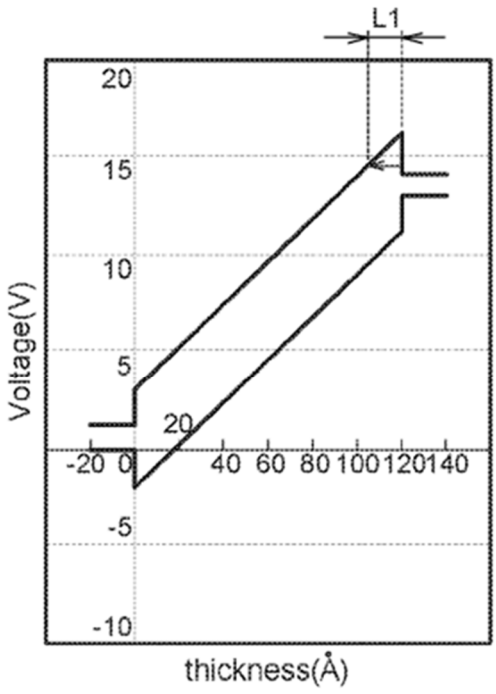


FIG. 8A

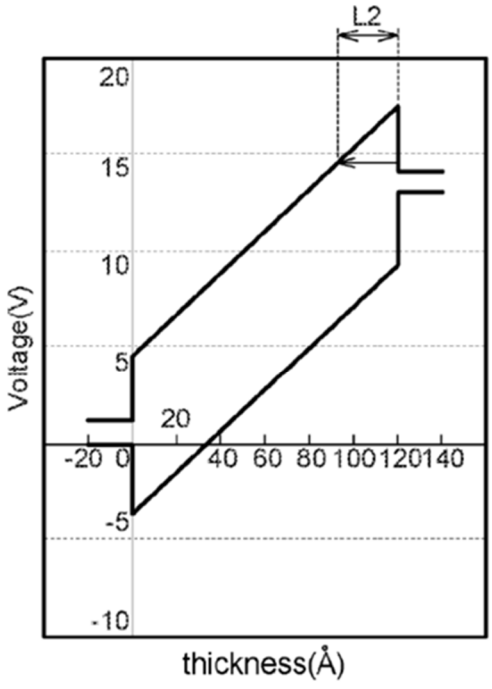


FIG. 8B

Ex. 1008, Figs. 8A-8B, [0047]-[0048] ("It is apparent that the tunneling length L2 is

larger than the tunneling length L1."). Specifically, the energy gap is increased from 4.7-5 eV to greater than 6 eV, improving "the stability" of the device. *Id.*, [0049], [0031].

152. At minimum, Fang presents a high-k dielectric as an alternative for the etch-stop layer. A POSITA would have readily considered such a suitable alternative.

153. If Patent Owner argues against the combination because Kim discloses an additional barrier layer, that argument would be wrong. First, none of claims 1, 3 and 6-8 requires a barrier layer or prohibit it since they are open-ended "comprising" claims. So a barrier layer has no bearing on those claims. Second, like Fang, Kim discloses an embodiment with a single etch-stop layer 125. Ex. 1005, [0256]; §XIII (Kim's descriptions apply to common aspects across embodiments). And Kim does not teach or suggest that the thickness or deposition method of the etch-stop layer would be impacted by the number of etch-stop layers. *See generally* Ex. 1005. And the etch-stop layer in both single- and two-layer configurations may comprise silicon nitride, to which Fang discloses a high-k dielectric as an alternative. *Id.*, [0186]-[0187]; Ex. 1006, [0022]. Therefore, it would have been obvious that Fang's single etch-stop disclosures are applicable to Kim's device. Thus, the presence or absence of a barrier layer does not impact either the motivation to combine or the expectation of success.

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XV. GROUND 3: HAN IN VIEW OF FANG

154. Grounds 3-4 rely on Han's method that forms the word line contact structure, including the insulating layer. The Grounds further rely on Fang's method of forming an etch-stop layer and Chen's method of forming a barrier layer. Although the respective references are not used in the combination beyond these elements, I will describe below elements not used in the combination (for example, Fang's staircase structure and insulating layer) to show the similarities between the disclosures to lay a foundation for motivation to combine and expectation of success.

155. Grounds 3-4 are based on Han's Figure 29 embodiment. Although Han discloses several embodiments, it also makes plain that the descriptions of these other embodiments apply to the method associated with Figure 29. Specifically, Figures 27-29 together illustrate one method of device fabrication. Ex. 1007, [0026], [0142]. Figures 30 and 31 are enlarged partial views of Figure 29. *Id.*, [0027], [0142]. In describing Figures 27-29, Han also discloses that the process illustrated via Figures 15-26 to fabricate the device shown in Figure 14 may be used. *Id.*, [0143], [0150]. More precisely, the stack structure of Figure 29 may be the one described in Figures 14-26. *Id.*, ("the cell array structure may include the stack structures ST and the vertical structures VS described with reference to FIGS. 15 to 26."). Figure 29 embodiment is further linked directly and indirectly to the process illustrated in Figures 1-11, which illustrates methods of forming vertical openings

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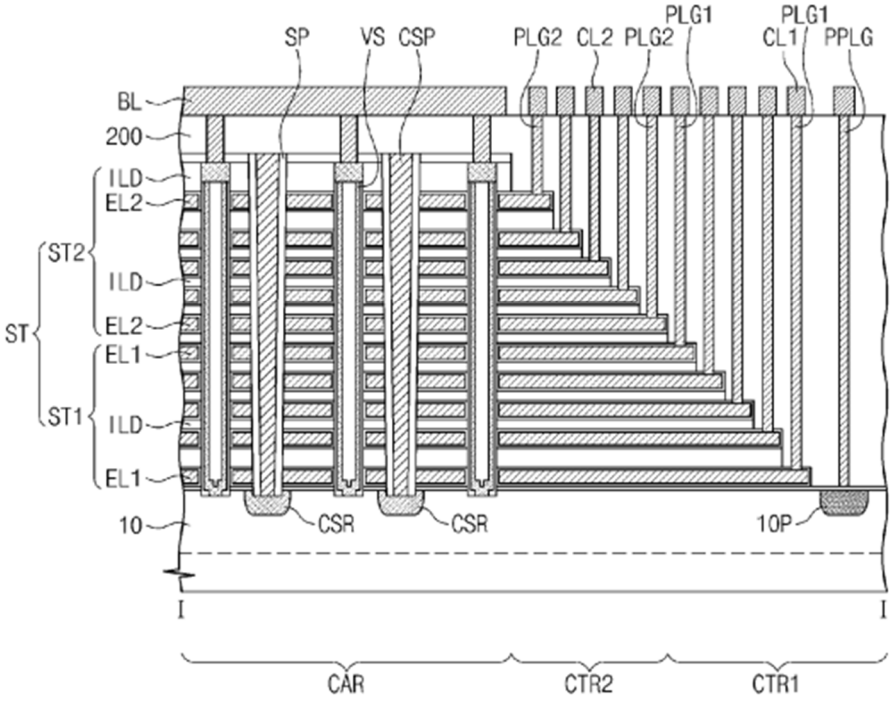
and represent building blocks for a more complete device, such as the embodiment of Figure 29. *Id.*, [0162], [0126]. Therefore, the descriptions of at least Figures 1-11 and 14-31 are all applicable to the method forming the device shown in Figure 29.

A. Claim 1:

1. [1.PRE] "A method for forming a semiconductor structure, comprising:"

156. Han discloses *[a] method for forming a semiconductor structure*, *e.g.*, methods for fabricating semiconductor devices. This is plain from its title. An embodiment is shown below:

FIG. 29



Ex. 1007, Fig. 29.

157. Fang also discloses *[a] method for forming a semiconductor structure*, *e.g.*, "method[s] of forming the semiconductor device structure…." Ex. 1006, Abstract. An embodiment is shown below:

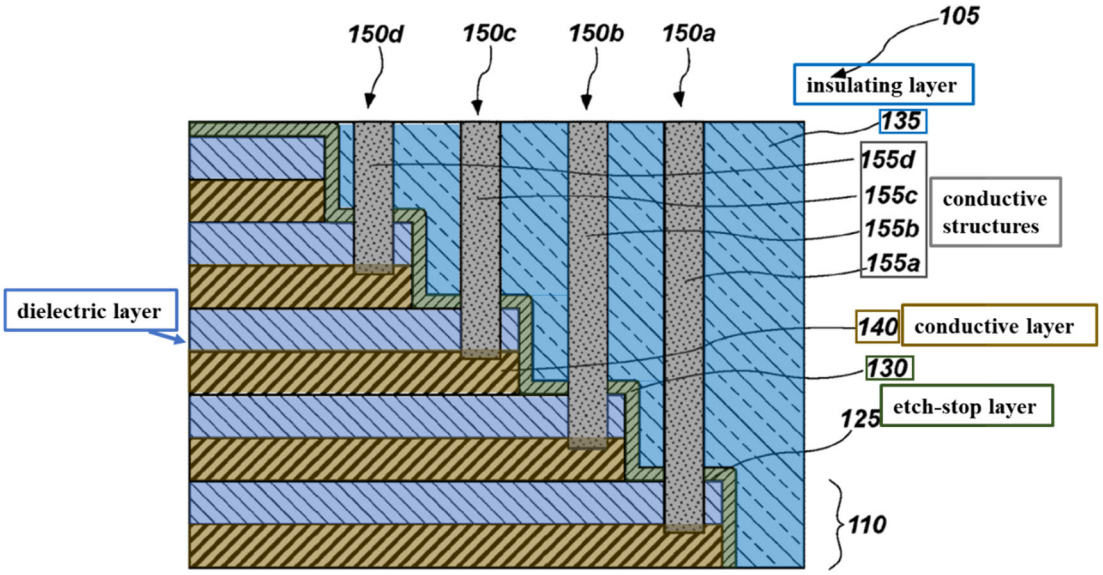


FIG. 6

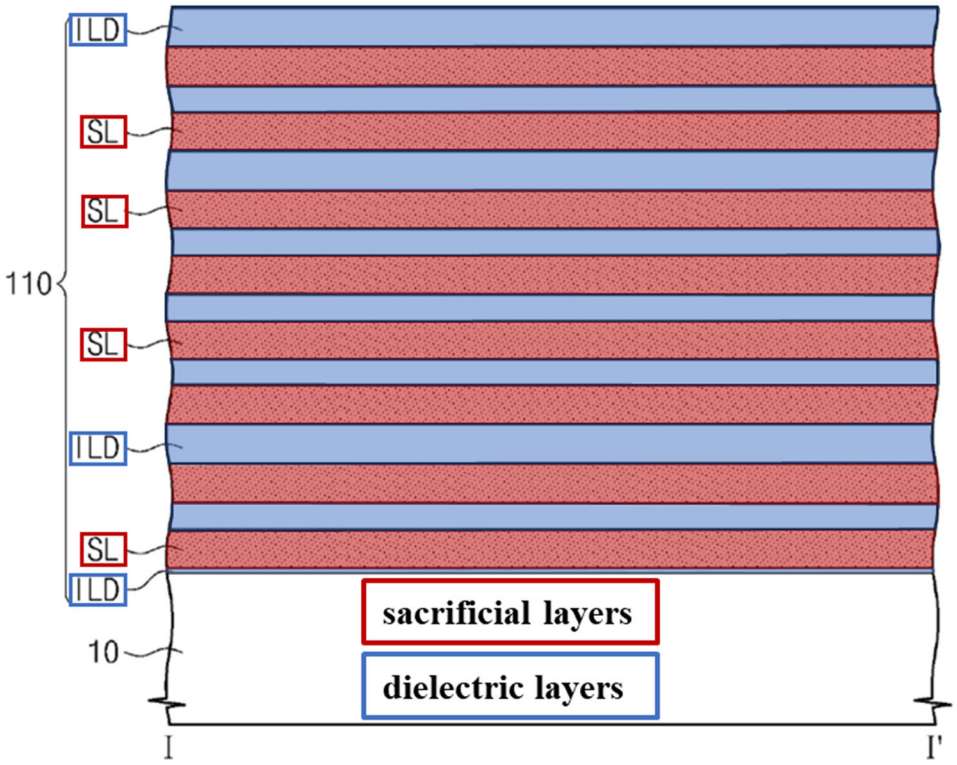
Ex. 1006, Fig. 6.

2. [1.A] "forming a staircase structure having a plurality of steps, wherein the forming of each step of the plurality of steps comprises disposing a sacrificial layer over a dielectric layer;"

158. Han's method comprises *forming a staircase structure* ("stepwise structure" ST) *having a plurality of steps*. Han discloses forming "a stepwise structure" ST wherein "[a]reas of the … electrodes … may decrease as a vertical distance from the top surface of the substrate 10 increases." Ex. 1007, [0151]-[0152]. Those are just different words describing a staircase structure and steps that

become shorter from bottom to top. This structure ST may be formed using the method illustrated via Figure 15-26, which illustrate the stack portion of the Figure 29 embodiment. §XV. Figure 15 shows *wherein the forming of each step of the plurality of steps comprises disposing a sacrificial layer* (one of "sacrificial layers SL") *over a dielectric layer* (one of "insulating layers ILD"):

FIG. 15



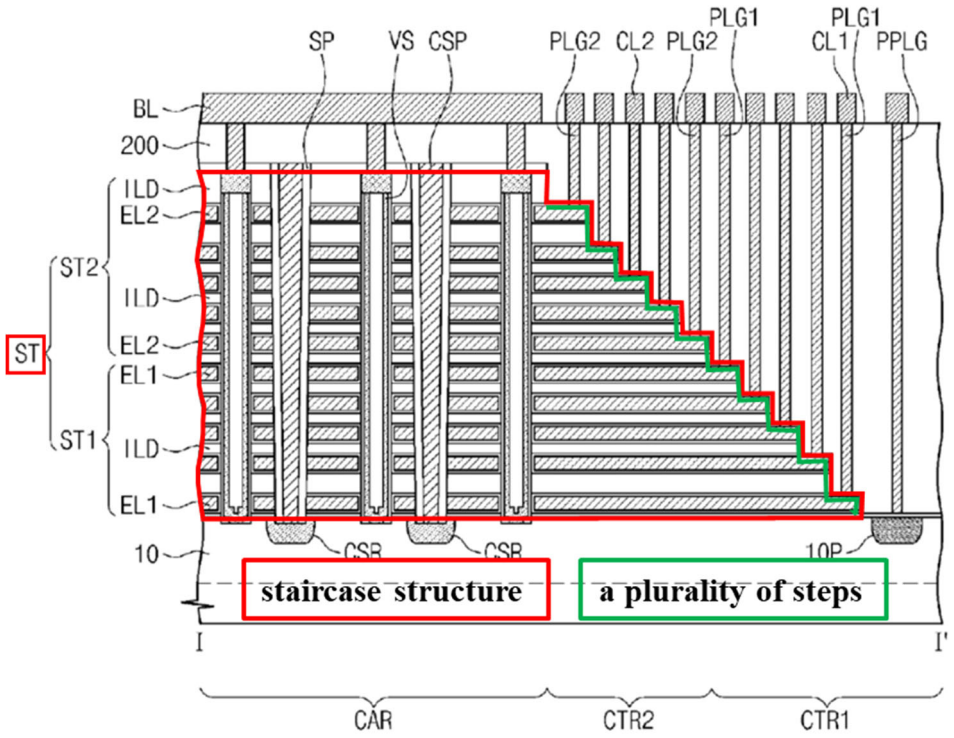
Ex. 1007, Fig. 15, [0096] ("sacrificial layers SL and insulating layers ILD may be alternately and repeatedly stacked on a substrate…."). As shown above in Figure 15, a thin insulating layer ILD resides at the bottom of the thin-layer structure 110 (note that the bracket 110 in the figure specifically extends to include that bottom

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ILD), and the lowest sacrificial layer SL is deposited on top of that bottom ILD layer. This bottom ILD layer is preserved when the sacrificial layer is removed and forms a step with the gate stack above. *Id.*, Figs. 18, 29. It was not uncommon to have dielectric layers (or gate conductive layers) in the staircase word line structure with different thickness between the layers. Ex. 1005, [0066]-[0067] (Kim disclosing varying thickness as an alternative). Han's is such an embodiment.

159. As also shown below, a gate stack (one of the shaded layers in the staircase) is disposed over the corresponding dielectric layer at each step:

FIG. 29



Id., Fig. 29. As will be explained in connection with Claim [1.D] and 13, gate stacks in the fully formed device replace and positionally correspond to the sacrificial

layers. *Id.*, [0115]. Therefore, the gate-stack-on-top configuration results from *disposing a sacrificial layer over a dielectric layer*.

160. Han's sacrificial layers SL and insulating layers ILD may comprise silicon nitride and silicon oxide, respectively. *Id.*, [0099]. These materials match Fang's disclosure.

161. Fang also discloses *forming a staircase structure* ("staircase structure 105") *having a plurality of steps, wherein the forming of each step of the plurality of steps* ("tiers 110") *comprises disposing a sacrificial layer* ("nitride materials 120") *[and] a dielectric layer* ("oxide materials 115"):[6]

[6] Grounds 3 and 4 rely on Han for its staircase structure and Fang for its etch-stop layer. Thus, Fang's layer ordering does not matter. In any event, reversing the order would have been obvious. §§XII.A, XIII.A.

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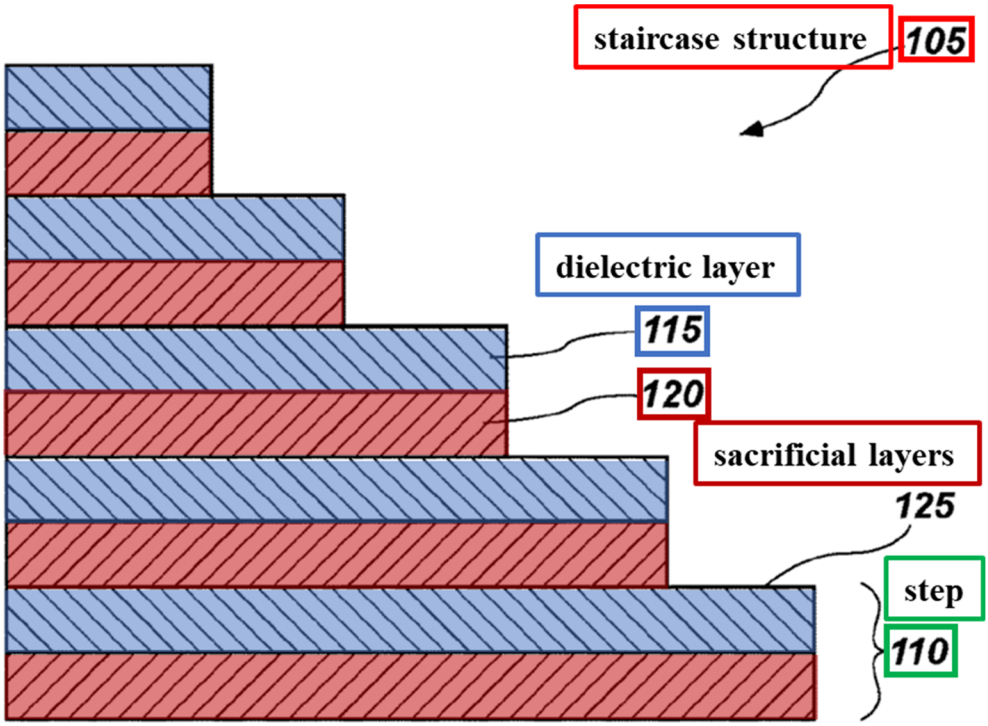


FIG. 1

Ex. 1006, Fig. 1, Abstract, [0015] (defining a "staircase structure"), [0019] (disclosing forming the alternating layers on the substrate and patterning the tiers to form a staircase structure).

3. [1.B] "disposing an etch-stop layer on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer;"

162. Fang discloses *disposing an etch-stop layer* ("etch stop material 130") *on each step of the plurality of steps* ("tiers 110"):

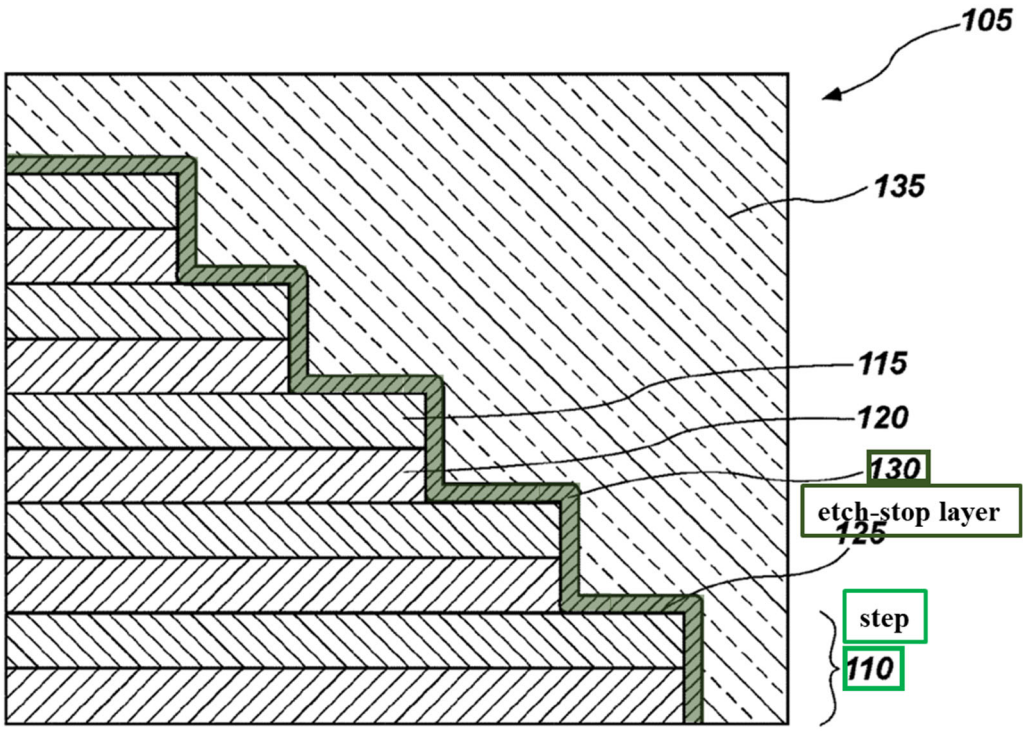


FIG. 2

Ex. 1006, Fig. 2. Fang discloses depositing etch-stop material over exposed horizontal and vertical surfaces of the steps, thereby forming a layer of "a stepped profile over the stairs." *Id.*, [0020]. The "stepped profile" refers to the staircase. *Id.*, [0019].

163. In the combination for this Ground, Fang's etch-stop material is deposited over Han's staircase structure, which may comprise the same materials as Fang's staircase, *e.g.*, silicon-nitride sacrificial layers and silicon-oxide dielectric layers. Ex. 1007, [0099]. While there is a range of materials that are suitable for the layers (for example as disclosed in Han, *id.*), the fact that Han's and Fang's stacks

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may comprise identical materials for the layers would have further bolstered a POSITA's expectation of success.

164. Fang further discloses that *the etch-stop layer* ("etch stop material 130") *comprises a second high-k dielectric layer* under the correct scope of "high-k dielectric." Specifically, the layer "may [comprise] a high-k dielectric material, such as hafnium oxide." Ex. 1006, [0022]. Hafnium oxide has a dielectric constant greater than 15, *e.g.*, 16-25. It is undisputably a high-k dielectric.

4. [1.C] "disposing an insulating layer on the etch-stop layer;"

165. Fang discloses *disposing an insulating layer* ("another oxide material 135") *on the etch-stop layer* ("etch stop material 130"):

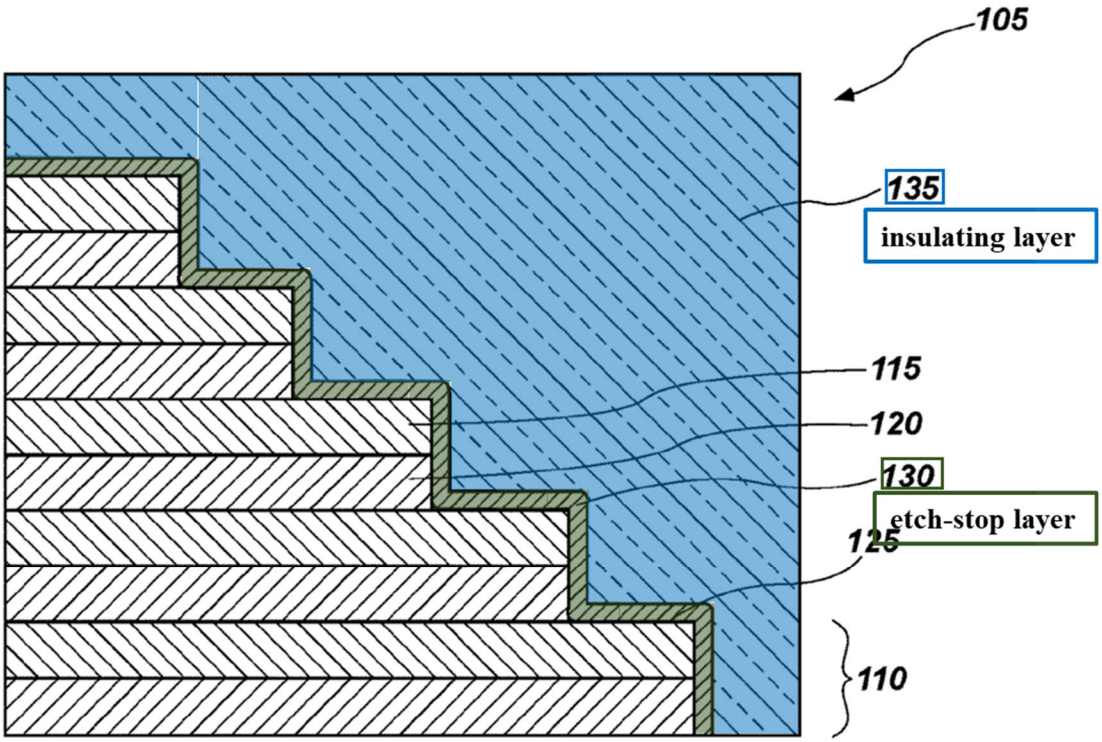


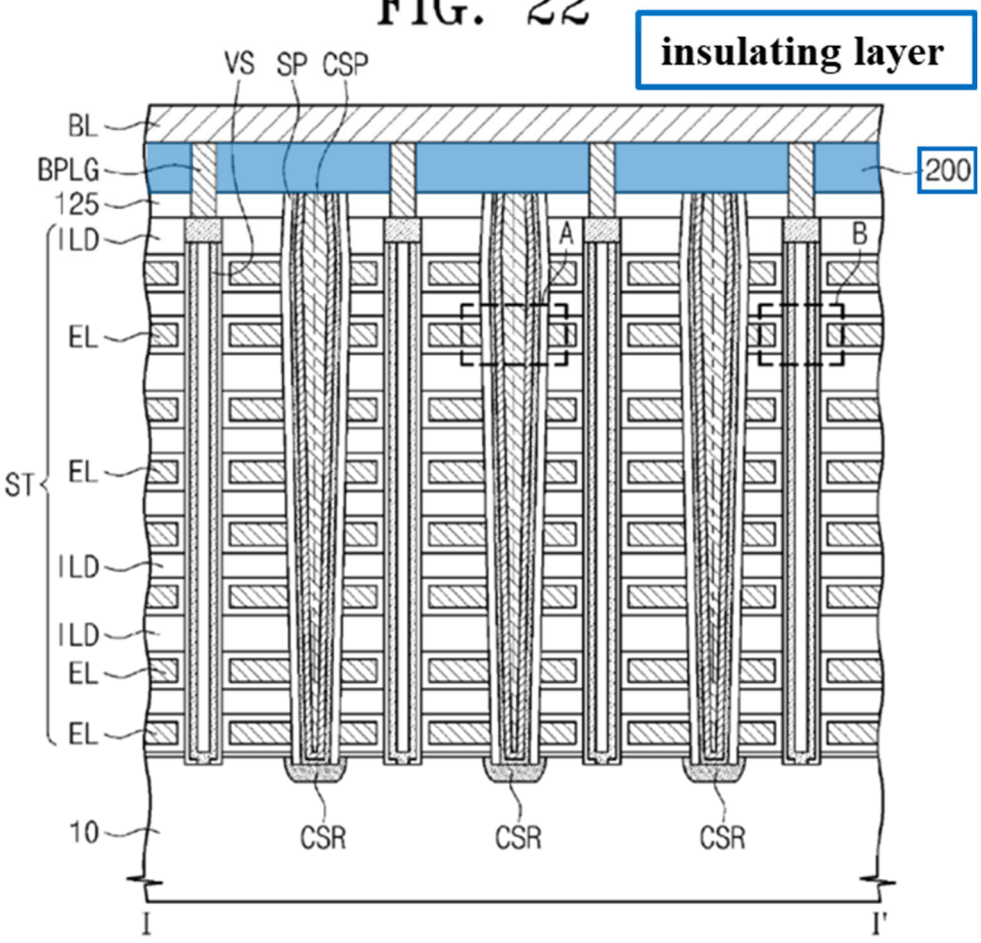
FIG. 2

Ex. 1006, Fig. 2, [0023] ("Another oxide material 135 may be formed over the etch stop material 130….").

166. Han also discloses *disposing an insulating layer* ("upper filling insulation layer 200"):

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FIG. 22



Ex. 1007, Fig. 22, [0131] ("an upper filling insulation layer 200 … may be formed on the stack structures ST."). Although Han does not disclose the material of the upper filling insulation layer, oxide is viable based on Han's disclosures of the characteristics of the layer. For example, the upper filling *insulation* layer obviously should have an insulating material. The material should permit formation of a staircase profile on the bottom surface and planarization of the top surface. *Id.*, [0131]-[0132], [0155], [0161]. The material should be etchable to permit the

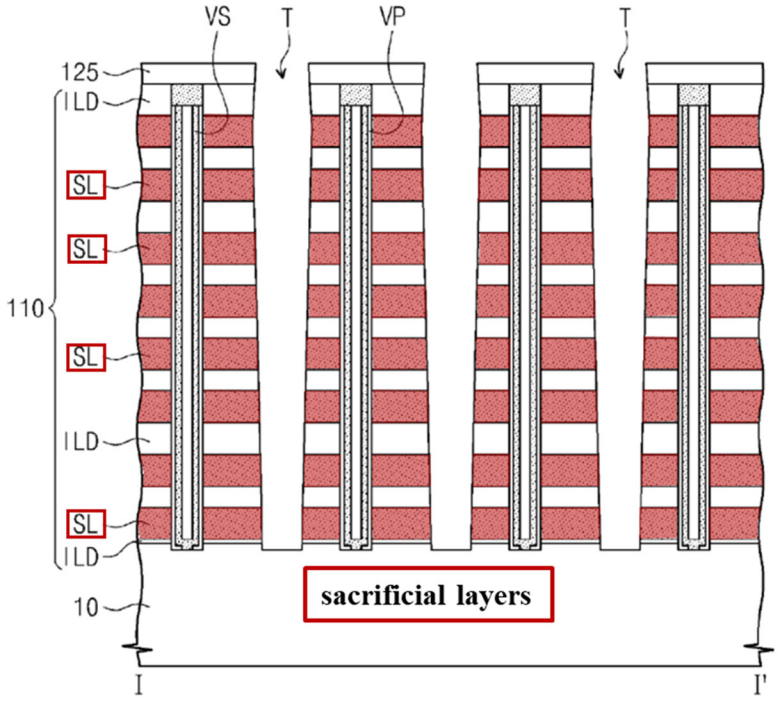
formation of opening through the layer. *Id.*, [0132], [0156]. Oxide, *e.g.*, silicon oxide, has those characteristics.

167. In the combination, Han's upper filling insulation layer is *dispos[ed] on the etch-stop layer* ("etch stop material 130") as taught by Fan.

5. [1.D] "replacing the sacrificial layer of each step with a gate stack, the gate stack comprising a conductive layer and a first high-k dielectric layer;"

168. Han discloses *replacing the sacrificial layer* ("SL") *of each step with a gate stack*. This can be seen through the progression from Figure 17 through Figure 19. Figure 17 shows the sacrificial layers after trenches T have been formed:

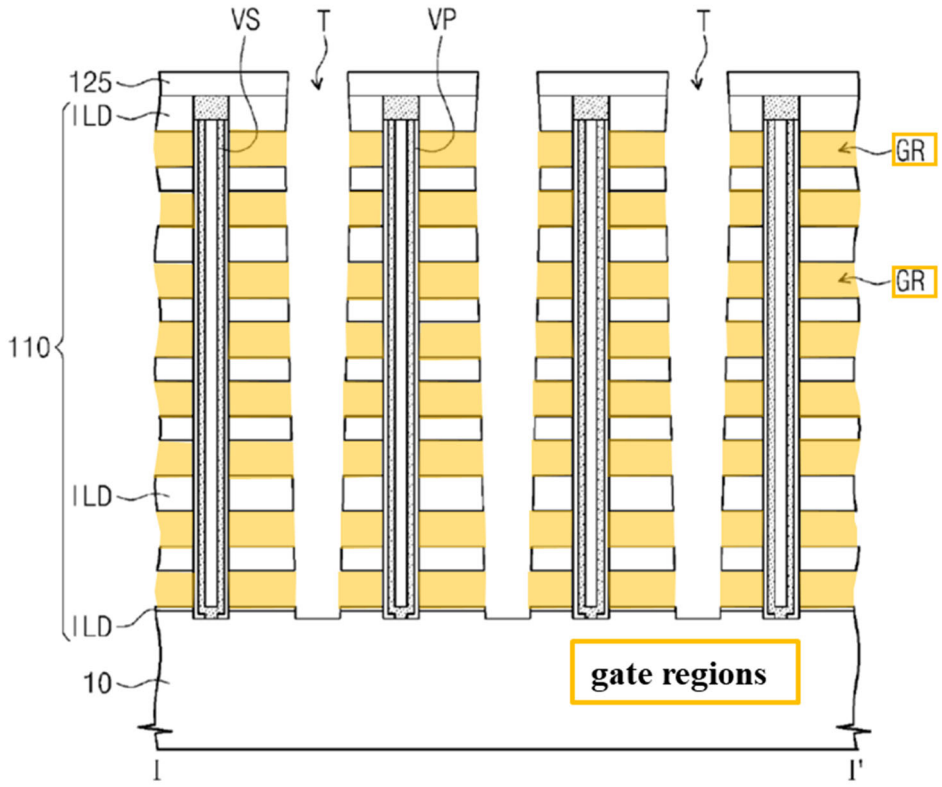
FIG. 17



Ex. 1007, Fig. 17, [0110]. Trenches T will be filled with a conductive material to provide contact to a common source for the memory string. *Id.*, [0119], [0121].

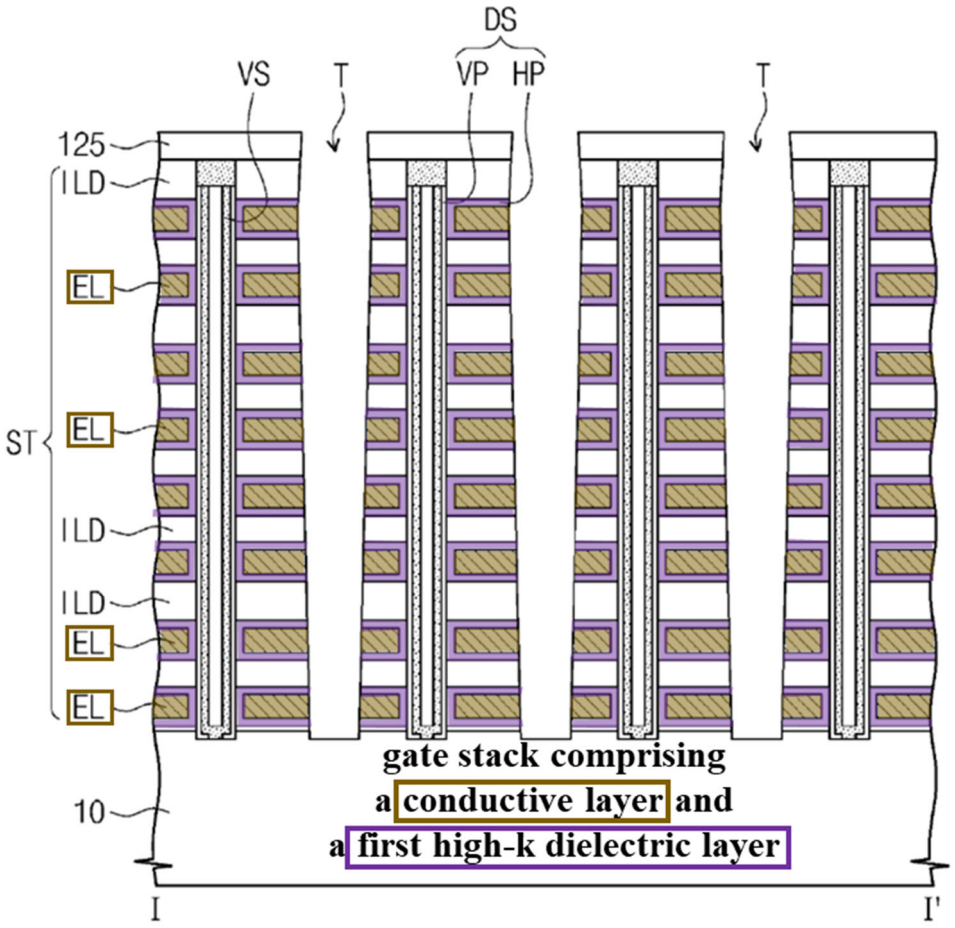
During the manufacturing process, it is used for removal of the sacrificial layer and depositing of the gate stack. *Id.*, [0115]. Figure 18 shows "the sacrificial layers SL exposed by the trenches T [have been] removed to form gate regions GR between the insulating layers ILD." *Id.*:

FIG. 18



Id., Fig. 18. Figure 19 shows *gate stack[s] [each] comprising a conductive layer* (one of "electrodes EL") *and a first high-k dielectric layer* ("horizontal insulating layer") have been formed in the gate regions GR, thereby *replacing the sacrificial layer of each step*.

FIG. 19



Id., Fig. 19. Specifically, Han's method involves "cover[ing] inner surfaces of the gate regions GR" with a conformal horizontal insulating layer and subsequently filling GR with a gate conductive layer. *Id.*, [0118]-[0120]. These same layers also fill the trenches, forming contacts to the common source. *Id.*, [0119], [0121].

169. Han discloses that *the gate stack compris[es] a conductive layer*, *i.e.*, a "gate conductive layer" or "electrodes EL." *Id.*, [0119].

170. Han discloses that *the gate stack compris[es] … a first high-k dielectric layer*. Specifically, "the horizontal insulating layer may be a portion of a data

storage layer of a charge trap-type flash memory transistor." *Id.* "[T]he data storage layer … may include a tunnel insulating layer TIL, a charge storage layer CIL, and a blocking insulating layer BK." *Id.*, [0134]. All three sub-layers may extend into the horizontal gate region in the stack. *Id.*, [0136]-[0138], Figs. 26B-D. The tunnel insulating layer TIL or the blocking insulating layer BK may comprise a high-k dielectric layer. *Id.*, [0140]-[0141]. Therefore, *the gate stack compris[es] … a first high-k dielectric layer*, *e.g.*, the tunnel insulating layer TIL or the blocking insulating layer BK. The formation of a data storage layer in the horizontal gate region is an artifact of the manufacturing process of forming the layer after removing the sacrificial layers and forming empty gate regions. The data storage layer in the horizontal gate region is not necessary for the functioning of the device. Lots of prior art exist that does not have such a dielectric layer around the conductive gate layers. But Han's configuration was also common and well know in the art.

171. Similarly, Fang discloses *replacing the sacrificial layer* ("nitride materials 120") *of each step layer* ("tier 110") *with … a conductive layer* ("conductive materials 140") in "a so-called 'replacement gate' process." Ex. 1006, [0025]. This can be seen through the progression from Figure 3 to 4. Figure 3 shows the sacrificial layers:

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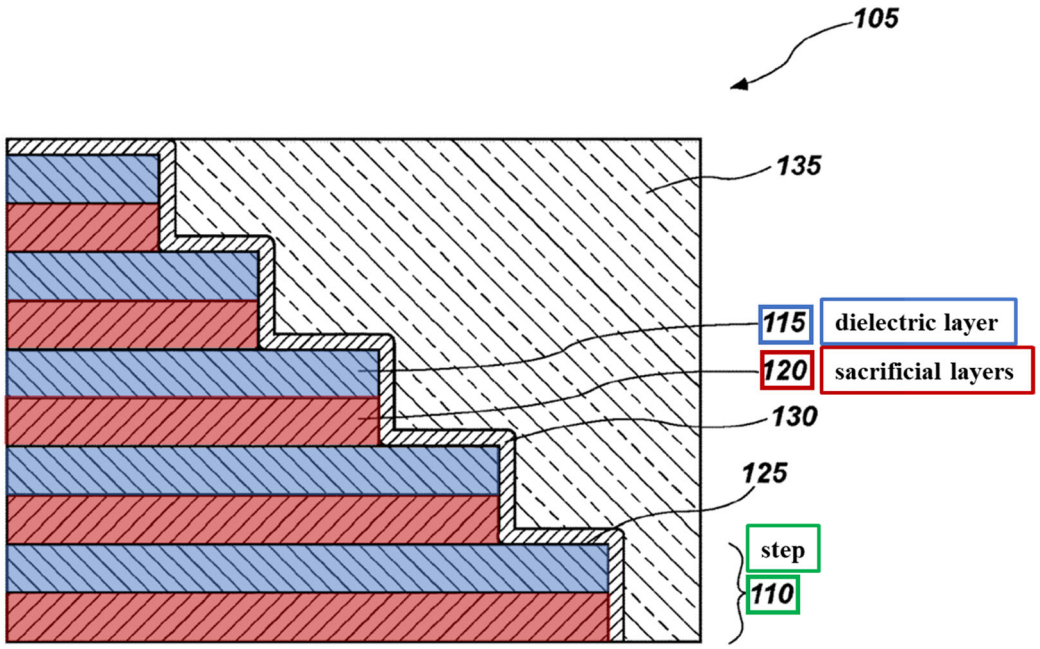


FIG. 3

Id., Fig. 3. Then, "[t]he nitride materials 120 of the staircase structure 105 are removed and conductive materials 140 formed in the resulting spaces…." *Id.*, [0025].

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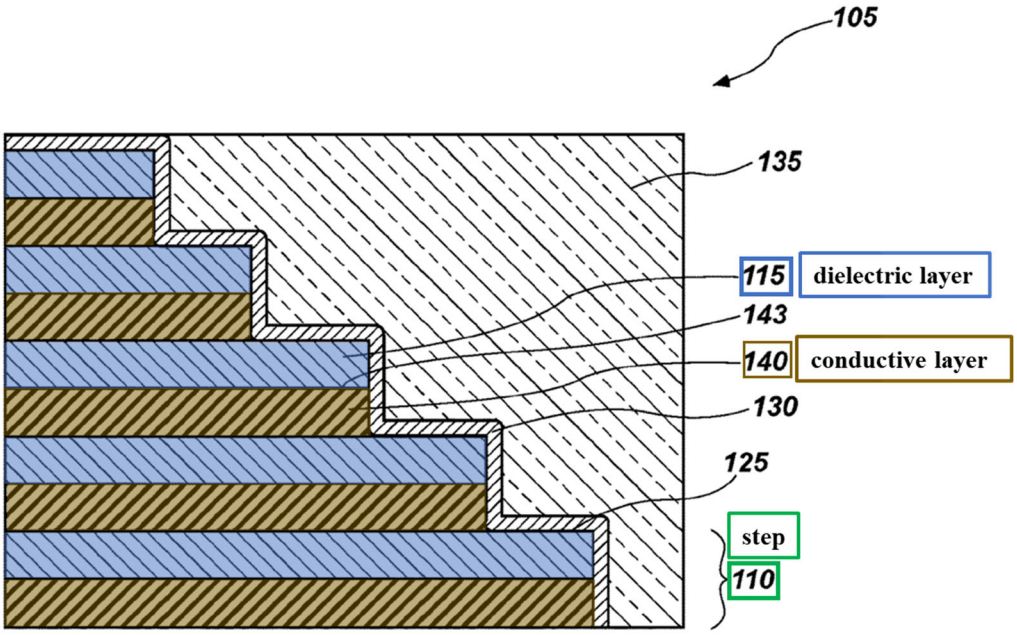


FIG. 4

Id., Fig. 4. Again, the parallel between Fang's replacement gate process and Han's process demonstrates that the process was widely known and commonly used. It also renders the combination obvious and increases a POSITA's expectation of success.

172. For clarity, the combination comprises Han's gate stack including the first high-k dielectric layer.

6. [1.E] "forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer;"

173. Fang discloses *forming a plurality of openings* ("openings 145") *in the insulating layer* ("another oxide material 135") *exposing portions of the etch-stop layer* ("etch stop material 130"):

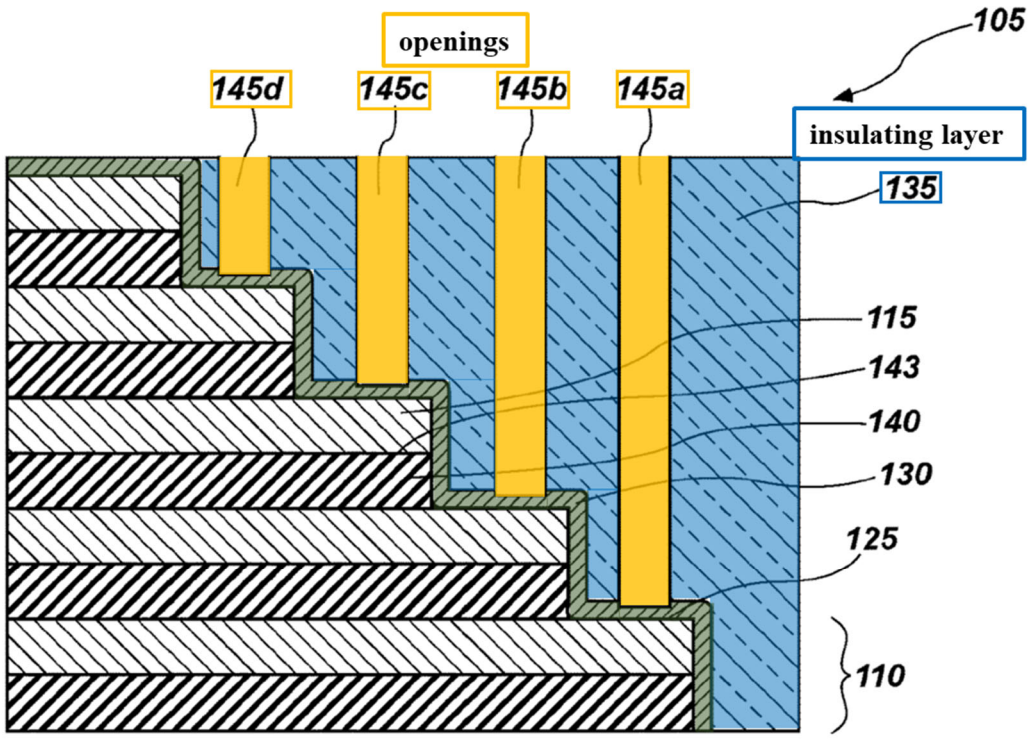
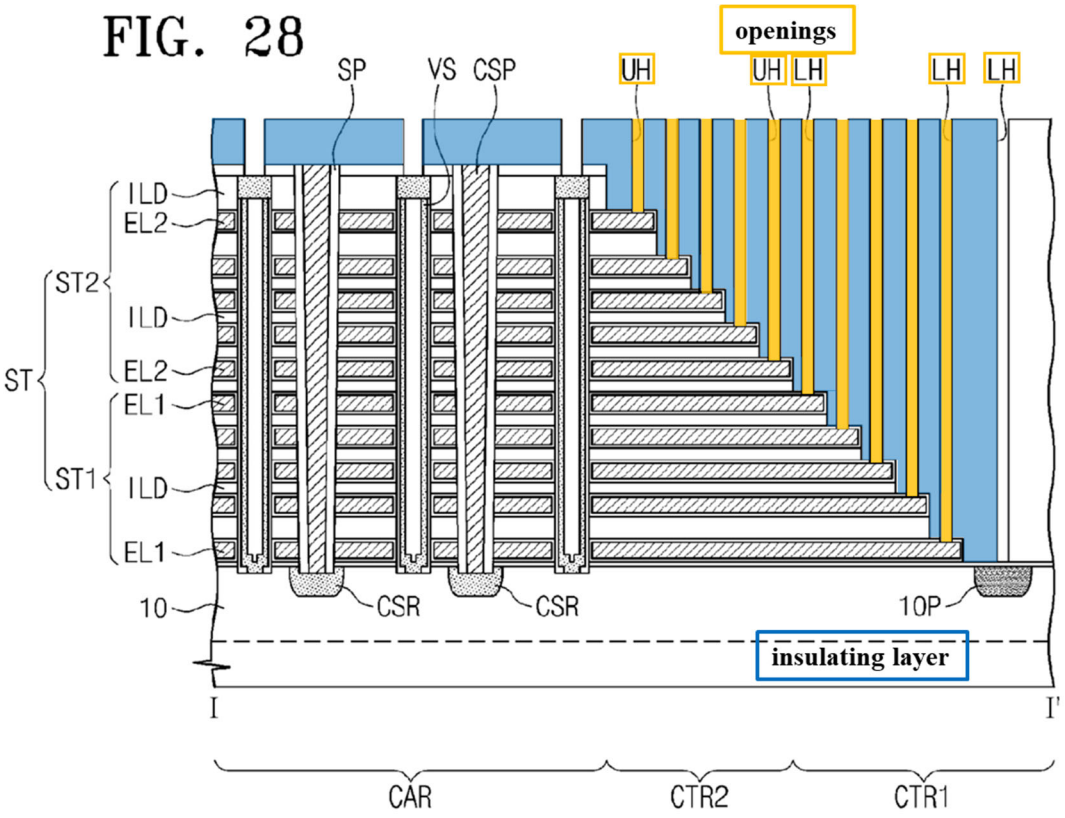


FIG. 5

Ex. 1006, Fig. 5. Fang discloses a discreet manufacturing step that involves etching to the top surface of the etch-stop layer: "Openings 145 may be formed in the another oxide material 135 … [and] extend … to an upper surface of the etch stop material 130 overlying each of the stairs 125." *Id.*, [0027]-[0028]. Having such a discreet step is a common approach, which typically is followed by another step of etching the etch-stop layer using a different etchant. It was also known to simply using one etching step and one etchant to etch both the insulating layer and the etch-stop layer. But even in this approach, there is a point in time when etching reaches the top of the etch-stop layer, *exposing portions of the etch-stop layer*.

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174. Han also discloses *forming a plurality of openings* ("upper contact holes UH" and "lower contact holes LH") *in the insulating layer* ("upper filling insulation layer 200"):



Id., Fig. 28, [0156] ("process may be performed on the upper filling insulation layer 200 to form lower contact holes LH … [and] upper contact holes UH…."). The upper and lower contact holes are distinguished by their lengths and may be formed in two separate stages (which is not relevant to the claim). *Id.*, [0156]. In other respects, the upper and lower contact holes are basically the same and share parallel or identical descriptions. *See, e.g.*, *id.*, [0158]-[0159], [0161]-[0165].

175. In the combination, *forming a plurality of openings* (Han's "upper

contact holes UH" and "lower contact holes LH") *in the insulating layer* (Han's "upper filling insulation layer 200") would *expos[e] portions of the etch-stop layer* (Fang's "etch stop material 130") since Fang's etch-stop layer covers the steps of the staircase structure. Therefore, the openings would necessarily reach the etch-stop layer before reaching the gate conductive layers.

7. [1.F] "etching the exposed portions of the etch-stop layer in the plurality of openings and exposing at least a portion of the conductive layer of each step; and"

176. Fang discloses *etching the exposed portions of the etch-stop layer* ("etch stop material 130") *in the plurality of openings* ("contact holes 150") *and exposing at least a portion of the conductive layer* ("conductive materials 140") *of each step* ("tier 110"):

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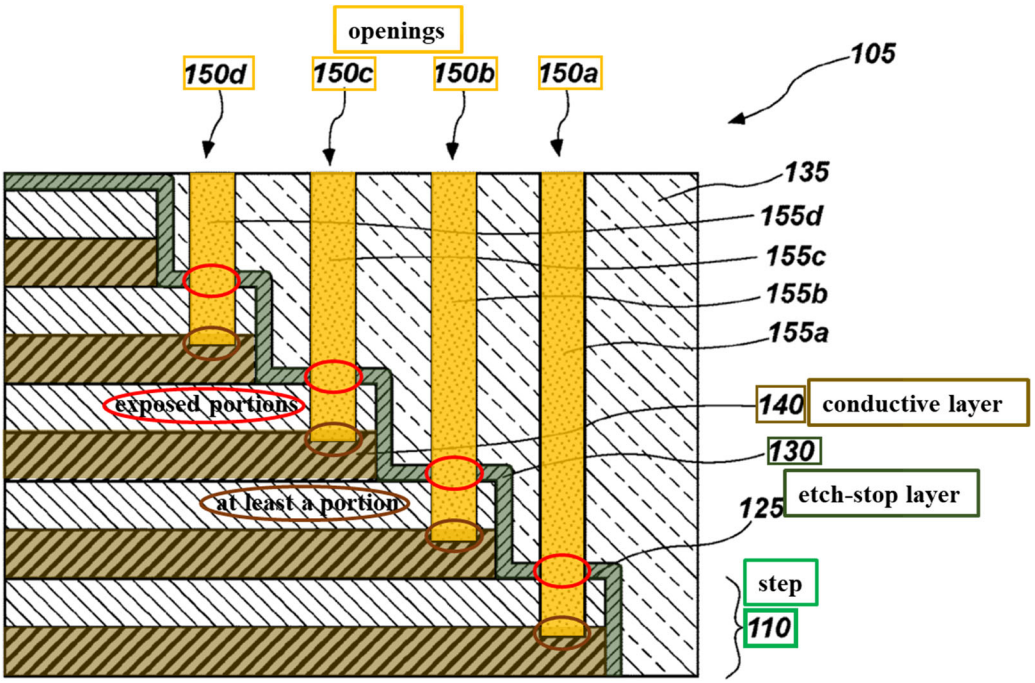


FIG. 6

Ex. 1006, Fig. 6. After the openings 145 are etched to the upper surface of the etch stop material 130, they are "extended through the oxide materials 115 and into the conductive materials 140 to form the contact holes 150." *Id.*, [0027], [0029]. This process involves selective etching. *Id.*, [0023], [0028]. Going through the oxide materials of the dielectric layers is part of Fang's process because those layers are above the conductive gate layers at each step. Again, the contact holes must extend to the conductive gate layers because the gate layers must be electrically coupled to the conductive structures to be formed in the holes for the proper functioning of the device.

177. The combination comprises *etching the exposed portions of the etch-*

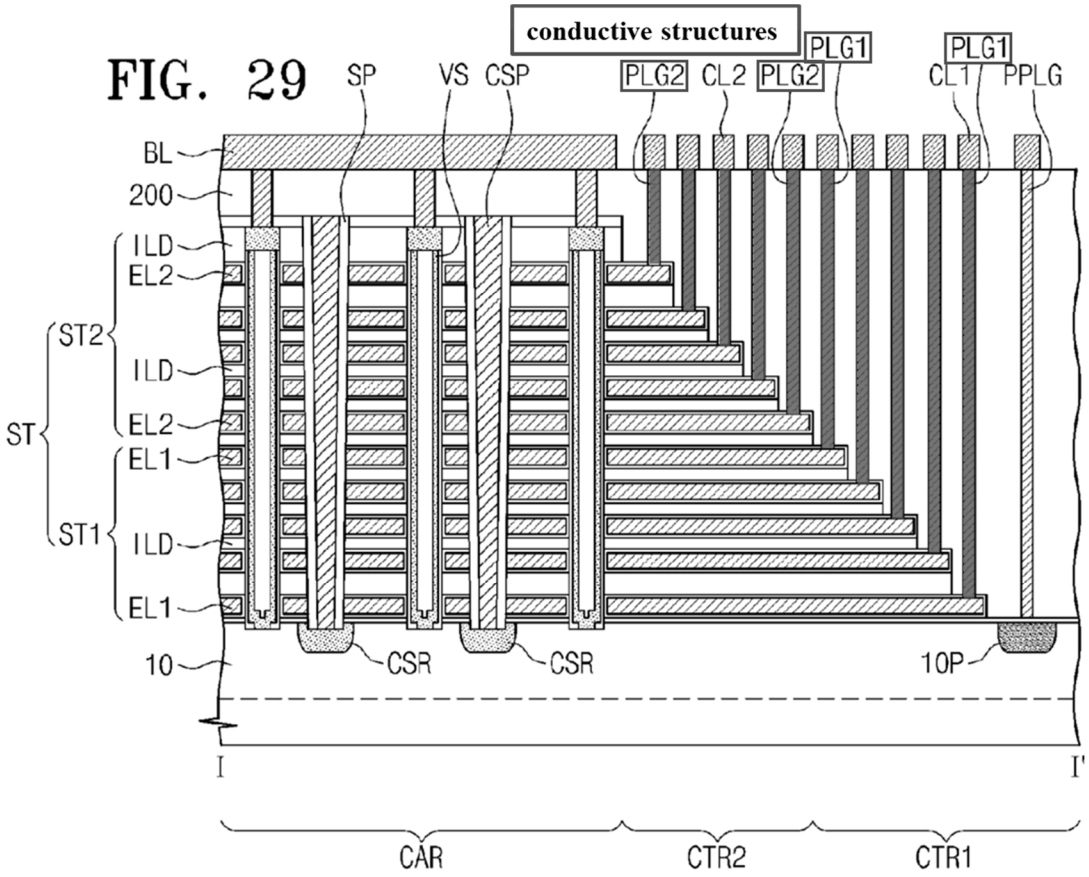
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stop layer (Fang's "etch stop material 130") *in the plurality of openings* (Han's "upper contact holes UH" and "lower contact holes LH") *and exposing at least a portion of the conductive layer of each step* (Han's "electrodes EL"). Han and Fang both disclose *exposing at least a portion of the conductive layer of each step*, which is necessary for the subsequently formed conductive structures to contact the conductive gate layers for electrical connection. In the combination, the openings extend through the first high-k dielectric layer but not the dielectric layer. This would have been obvious to a POSITA because of the required contact between the conductive layers and the conductive structures.

8. [1.G] "forming a plurality of conductive structures in each of the plurality of openings."

178. Han discloses *forming a plurality of conductive structures* ("first contact plugs PLG1" and "second contact plugs PLG2") *in each of the plurality of openings* ("lower contact holes LH" and "upper contact holes UH"):

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Ex. 1007, Fig. 29, [0159], [0161] (forming PLG1 and PLG2 in LH and UH, respectively, by forming a conductive layer filling in the contact holes). Similar to upper and lower contact holes, first and second contact plugs share identical or parallel descriptions. *See, e.g.*, *id.*, [0159], [0161], [0166]-[0167]. They are not distinguishable for purposes of these claims.

179. Similarly, Fang also discloses *forming a plurality of conductive structures* ("contacts 155") *in each of the plurality of openings* ("contact holes 150"):

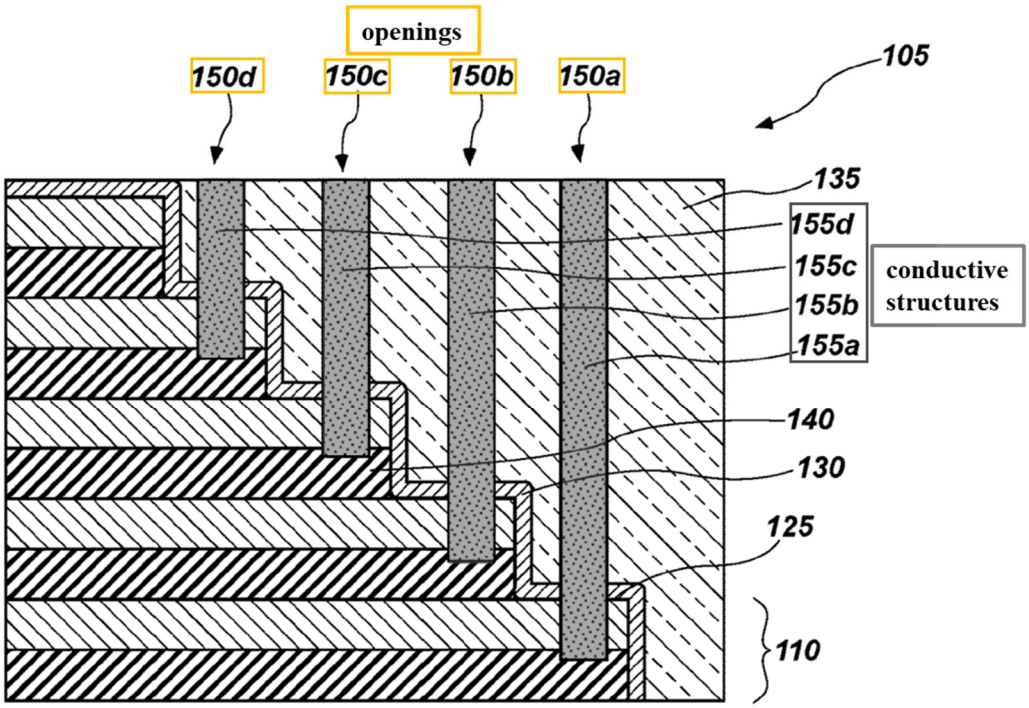


FIG. 6

Ex. 1006, Fig. 6, [0030] (filling contact holes 150 with conductive material to form contacts 155).

180. For completeness (inconsequential since the combination uses Han's staircase structure), although Fang's Figure 6 does not show a conductive structure at the topmost step, a POSITA would have understood that a conductive structure would be present. §XIII.B.2.

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B. Claim 2:

1. [2] "The method of claim 1, wherein the forming the plurality of openings comprises performing an etching process on the insulating layer, wherein an etching rate of the insulating layer is higher than an etching rate of the etch-stop layer."

181. Fang discloses the additional limitation of Claim 2. *[T]he forming the plurality of openings* ("openings 145") *comprises performing an etching process on the insulating layer* ("another oxide material 135"). Specifically, "portions of the another oxide material 135 [*i.e.*, the insulating layer] are removed until the upper surface of the etch stop material 130 is exposed at a bottom portion of the openings 145." Ex. 1006, [0028]. This removal is done using "dry etch chemistries" to which the etch-stop layer is "substantially resistant." *Id.*, [0020]. In other words, *an etching rate of the insulating layer* ("another oxide material 135") *is higher than an etching rate of the etch-stop layer* ("etch stop material 130") such that the etch-stop layer substantially slows down the etching process when it reaches the layer. Fang describes this as "selectively etchable" and discloses that "[t]he another oxide material 135 may be … selectively etchable relative to the etch stop material 130 during formation of the contact holes 150." *Id.*, [0018], [0023]. That disclosure matches the claimed relationship of etching rates. Fang further defines "selectively etchable" to mean "a material that has an etch rate that is at least about two times (2×) greater than the etch rate of another material." *Id.*, [0018]. But the numerical

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value of the ratio is not relevant here since Claim 2 simply requires a higher etching rate.

182. In the combination, Han's upper filling insulation layer 200 comprises oxide material as disclosed in Fang. As explained above, Han does not disclose the material of its insulating layer, and oxide is a suitable material for Han's upper filling insulation layer. §XV.A.4.

C. Claim 3:

1. [3] "The method of claim 2, wherein the etching process comprises anisotropic dry etching."

183. Fang discloses the additional limitation of claim 3.

184. *[T]he etching process* is performed on the insulating layer (e.g., Han's upper filling insulation layer 200, or, equivalently, Fang's another oxide material 135) when forming the openings. §XV.B.1. Fang discloses "[a] *dry etch[]* process (e.g., an *anisotropic* etch process) may be used to form the openings 145." Ex. 1006, [0028]. This etching process was conventional and would have been a suitable process for etching small but deep openings due to its directionality. Fang discloses additional uses of dry etch. *Id.*, [0008], [0020].

185. Han similarly uses anisotropic etching to form openings such as trenches used to remove the sacrificial layers. Ex. 1007, [0041], [0105], [0111]. This would have rendered Fang's anisotropic dry etching an obvious choice for

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Han's method for the same reason that Fang's method would have been an obvious choice for Kim's method. §XIV.B.1. And a POSITA would have had a reasonable expectation of success for the same reason. *Id.*

D. Claim 4:

1. [4] "The method of claim 1, wherein etching the exposed portions of the etch-stop layer comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer of each step."

186. Claim 4 is obvious in view of a POSITA's knowledge. §XIII.D.1. This, in my opinion, is sufficient even without any additional disclosure from Han or Fang.

187. Additionally, it is my opinion that Fang further renders claim 4 obvious. Fang discloses that "[t]he etch stop material is also selectively etchable relative to specific other materials in the semiconductor device structure." Ex. 1006, [0008]. A POSITA would have understood this to be essential to the purpose of the etch-stop layer to slow down etching. Moreover, Fang discloses a multi-stage etching process wherein, after etching reaches the etch-stop layer and exposes a portion of it, "the exposed portions of the etch stop material 130 are removed to expose the underlying [layer]." *Id.*, [0029]. Thereafter, portions of conductive material 140 exposed by the opening are also removed to extend the openings into them. *Id.* The etch-stop-layer removal may use the same or a different etch chemistry compared to

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the etch chemistry used to extend the openings into the conductive layers. *Id.* The flexibility helps achieve the objective of protecting the conductive layer through configuring it with a lower etching rate based on the etch chemistry. Although a high-k dielectric layer is present between the etch-stop and conductive layers in the Han/Fang combination, the flexibility taught by Fang is still advantageous, as I explained above with respect to Kim. §XIII.D.1.

188. Additionally, a POSITA would have found it obvious that the removal of portions of conductive material (which Fang teaches) should be designed such that the opening would penetrate the conductive materials just enough to ensure a solid contact between the conductive layer and the corresponding conductive structure without unnecessarily reaching the dielectric layer underneath in the combined gate-stack-on-top embodiment. Accordingly, a different etch chemistries used to remove the etch-stop layer and to remove portions of the conductive layers makes it viable (and obvious) that *etching the exposed portions of the etch-stop layer* is done *at a higher etching rate than an etching rate of the conductive layer of each step* when *etching the exposed portions of the etch-stop layer* because it is unnecessary to penetrate the conductive layer, and thus a relatively low etching rate would be adequate. Shamiryan discloses dry etching recipes using CHF_3 which etch silicon dioxide (an exemplary material for the insulating layer, *see* Ex. 1006,

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[0023][7]) faster than a high-k dielectric such as hafnium dioxide (an exemplary etch-stop material, *see* Ex. 1006, [0022]). Ex. 1025, 11, 24. Hence, one can etch the word line contact holes through the silicon dioxide using CHF_3, which will essentially stop at the hafnium oxide etch-stop layer. Then, one can switch to Cl_2 to etch through the thin hafnium oxide to stop at the underlying tungsten word lines. Morel discloses that tungsten has a low etching rate relative to hafnium dioxide in Cl_2.

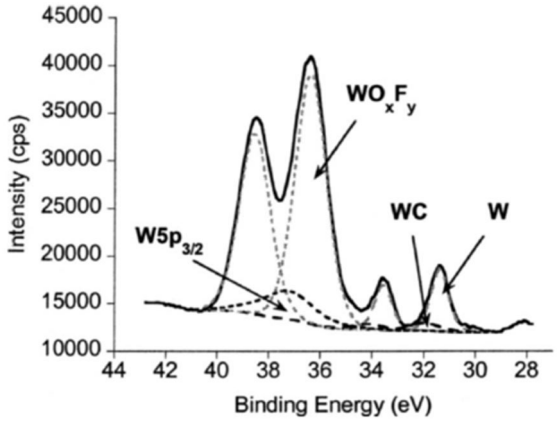


FIG. 12. W 4*f* XPS spectrum obtained after partial etching of W in Cl_2/O_2 60% with fluorine addition.

Ex. 1026, 7.

[7] Han does not disclose the material of its insulating layer.

E. Claim 5:

1. [5] "The method of claim 4, wherein etching the exposed portions of the etch-stop layer further comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the first high-k dielectric layer."

189. Claim 5 is obvious in view of a POSITA's knowledge. §XIII.E.1. As an example, a non-patent publication Kim shows that a high-k Al_2O_3 (an exemplary etch-stop material) has a higher etching rate than high-k HfO_2 (an exemplary dielectric-layer material) relative to argon plasma. Ex. 1027, 2. This is seen in Figure 1, where an HBr/(HBr+Ar) ratio of 0 corresponds to argon plasma.

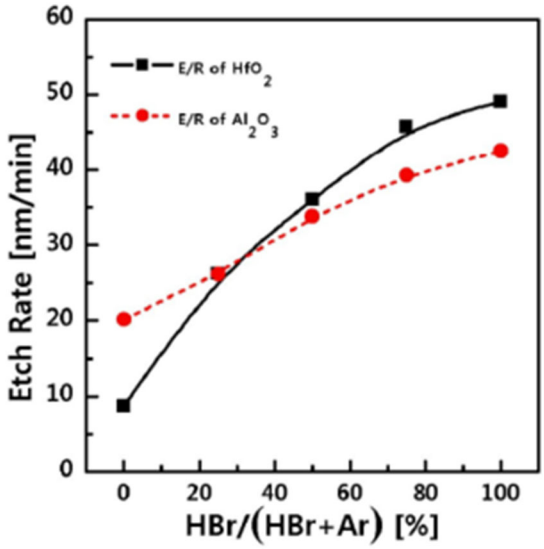


Fig. 1. Etch rate of HfO_2 and Al_2O_3 thin films as a function of HBr mixing ratio in a HBr/Ar plasma.

Id. At that ratio, the etch rate of Al_2O_3 (in red) is more than twice that of HfO_2 (in black).

190. The layer ordering at each step does not impact this analysis as I explained above. *Id.*

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F. Claim 6:

1. [6] "The method of claim 1, wherein disposing the etch-stop layer comprises disposing hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, and/or any combination thereof."

191. Fang discloses the additional limitation of claim 6. Specifically, *the etch-stop layer* may comprise silicon nitride or, "[a]lternatively, … a high-k dielectric material, such as *hafnium oxide*." Ex. 1006, [0022]. As explained above, Chen discloses that using a high-k dielectric material as an etch stop increases electrical isolation between conductive layers. §XIV.F. A POSITA would have found this desirable.

G. Claim 7:

1. [7] "The method of claim 1, wherein disposing the etch-stop layer comprises disposing the etch-stop layer with a thickness in a range between 10 nm to 100 nm."

192. Fang discloses the additional limitation of claim 7.

193. Claim 7 is directed toward a semiconductor structure with only an etch-stop layer and without an optional barrier layer. *See* Ex. 1001, Claims 1, 17. Fang discloses an analogous semiconductor structure with only an etch-stop layer. Ex. 1006, Fig. 6, [0020]. The layer "may be formed over the stairs 125 at a thickness ranging from about 50 Å to about 1000 Å," or about 5 nm to 100 nm. *Id.*, [0021]. Fang's thickness range overlaps with the claimed *range between 10 nm and 100 nm*. To the extent that Fang's etch-stop thickness may need to be adjusted to account for,

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e.g., the height of Han's staircase structure (which Han does not appear to disclose), the claimed range still would have been obvious because etch chemistry may be adjusted, allowing great flexibility in the thickness of the etch-stop layer.

H. Claim 8:

1. [8] "The method of claim 1, wherein disposing the etch-stop layer comprises performing chemical vapor deposition (CVD), physical vapor deposition (PVD), sputtering, atomic layer deposition (ALD), spin-coating, or any combination thereof."

194. Fang discloses the additional limitation of Claim 8, specifically, forming the etch-stop layer using "conventional techniques including … *chemical vapor deposition (CVD), physical vapor deposition (PVD)*, *atomic layer deposition (ALD)*…." Ex. 1006, [0020].

195. Han's method also uses these processes. *See, e.g.*, Ex. 1007, [0046], [0048], [0101], [0139]-[0141]. Thus, in the combination, applying one of these conventional techniques to form etch-stop layer represents nothing more than applying a known technique on a similar device, which would have been well within a POSITA's knowledge and skill. Further, using an existing technique is desirable to keep low the cost of the additional etch-stop layer of the combination. For example, the existing equipment for the deposition method may be used to deposit the etch-stop layer. The cost effectiveness would have motivated a POSITA to do so.

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I. Claim 9:

1. [9] "The method of claim 1, further comprising: after disposing the insulating layer on the etch-stop layer, planarizing the insulating layer and the staircase structure by using chemical-mechanical-polishing (CMP)."

196. Fang discloses the additional limitation of Claim 9.

197. Fang discloses using CMP to planarize the insulating layer and the etch-stop layer to level their top surfaces. Ex. 1006, [0024]. Since the etch-stop layer forms a stepwise covering on the staircase structure, Fang's process *planariz[es] the insulating layer and the staircase structure* (at the top of the etch-stop layer) *by using chemical-mechanical-polishing (CMP)*:

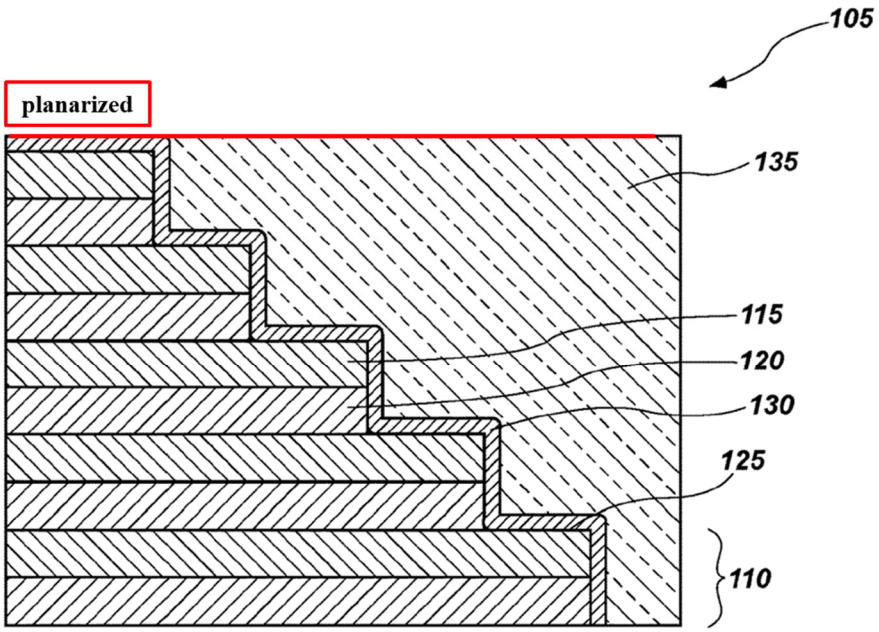


FIG. 3

Id., Fig. 3. Fang's process occurs *after disposing the insulating layer on the etch-stop layer*. This is necessarily true since the insulating layer has to be formed before

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it can be planarized. As explained, it is necessary for the top surface of the staircase structure to be planar. §XIII.H.1. Therefore, a POSITA would have been motivated to apply Fang's planarization process in the combination.

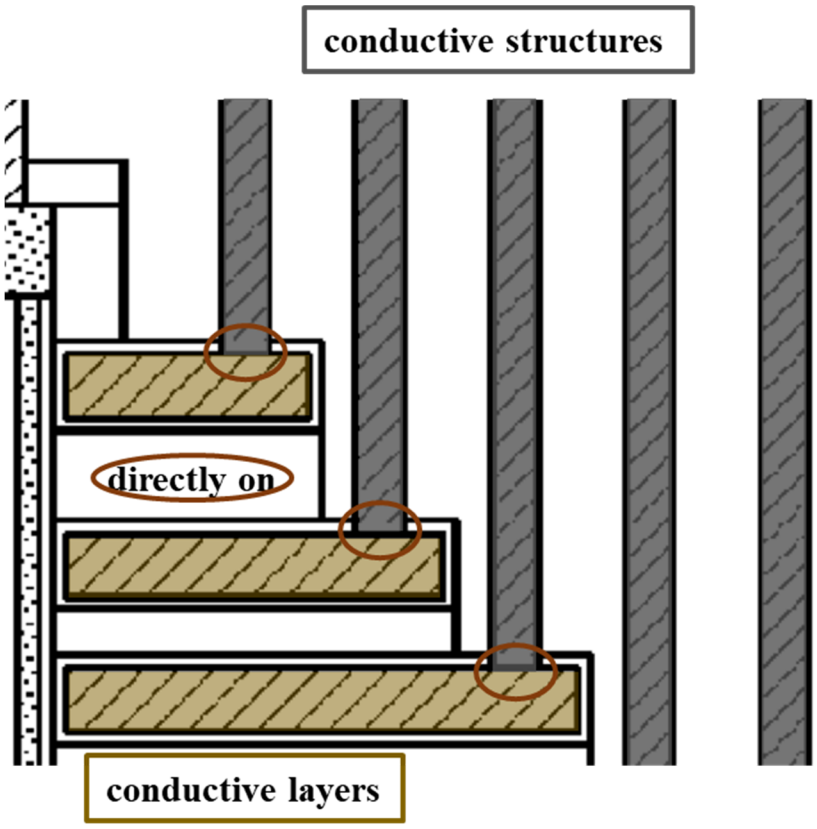
198. Han also discloses using "chemical mechanical polishing (CMP)," to planarize the conductive structures. Ex. 1007, [0065]. Therefore, applying Fang's process in the combination would have been obvious and would have yielded a reasonable expectation of success because it applies a process that both Han and Fang use on a device similar to both of their embodiments.

J. Claim 10:

1. [10] "The method of claim 1, wherein forming the plurality of conductive structures comprises disposing conductive materials inside the plurality of openings, the conductive materials directly on the exposed conductive layer of the each step."

199. Han discloses *forming the plurality of conductive structures* ("first contact plugs PLG1" and "second contact plugs PLG2") *comprises disposing conductive materials inside the plurality of openings* ("lower contact holes LH" and "upper contact holes UH"), *the conductive materials directly on the exposed conductive layer* ("electrodes EL") *of the each step*:

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Ex. 1007, Fig. 29 (partial, enlarged). Specifically, the contact holes LH and UH are etched to expose portion of the electrodes. *Id.*, [0156]. The holes are then filled with a conductive filling to form contact plugs PLG1 and PLG2. *Id.*, [0161]. The claimed direct contacts are necessary for the conductive structures to function as electrical connections to the conductive gate layers. Consistent with that requirement, Han discloses that the contact plugs "electrically connect the electrodes EL1 and EL2 to the peripheral logic structure." *Id.*, [0151].

200. Similarly, Fang discloses *forming the plurality of conductive structures* ("contacts 155") *comprises disposing conductive materials inside the plurality of openings* ("contact holes 150"), *the conductive materials directly on the exposed*

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conductive layer ("conductive materials 140") *of the each step* ("tier 110"):

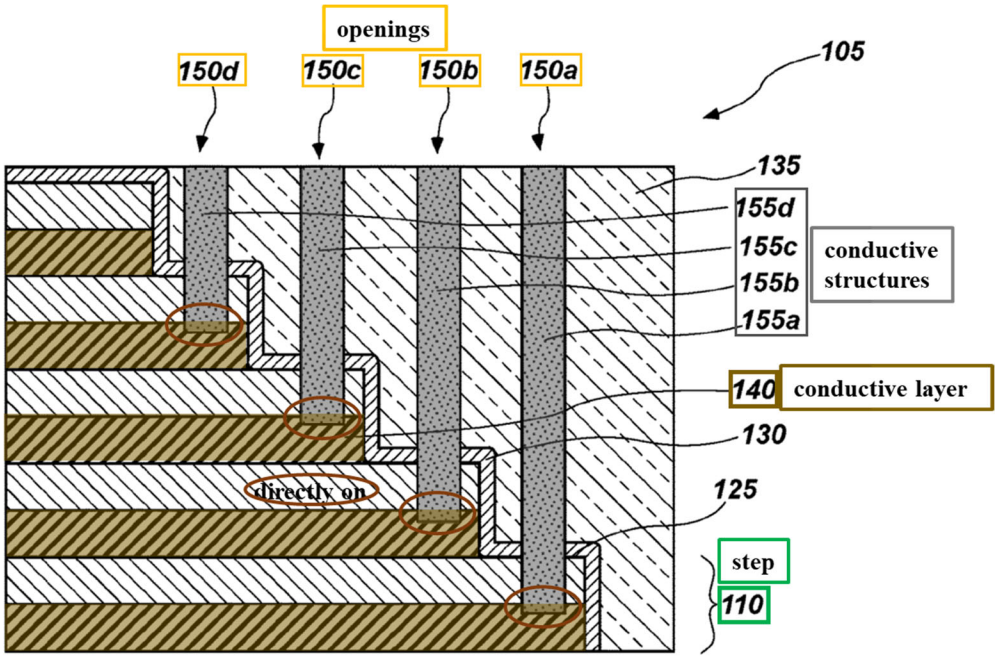


FIG. 6

Ex. 1006, Fig. 6; §§XV.A.7-8 (explaining Fang's relevant disclosures). Again, such direct contacts are necessary for the conductive structures to function as electrical connections to the conductive gate layers. And Han's and Fang's similar disclosures would have made their combination obvious.

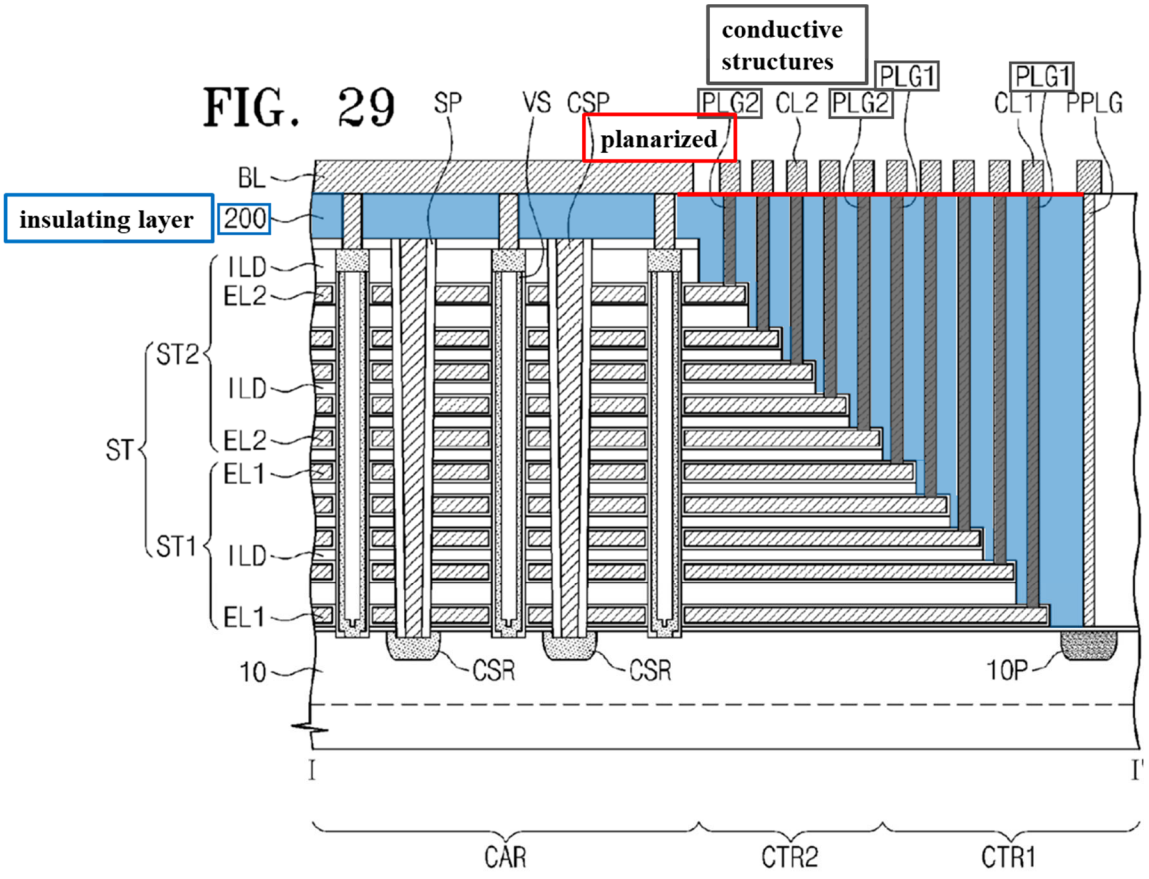
K. Claim 11:

1. [11] "The method of claim 1, wherein forming the plurality of conductive structures further comprises planarizing the conductive materials and the insulating layer."

201. Han discloses *forming the plurality of conductive structures* ("first contact plugs PLG1" and "second contact plugs PLG2") *further comprises planarizing the conductive materials* (of the contact plugs) *and the insulating layer*

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("upper filling insulation layer" 200). Specifically, as a part of forming the contact plugs, Han "perform[s] a planarization process on the conductive layer until a top surface of the upper filling insulation layer 200 is exposed." Ex. 1007, [0161]. Han's "conductive layer" is the conductive structure of the '276 Patent. After planarization, "top surfaces of the first and second contact plugs PLG1 and PLG2 may be substantially coplanar" (*id.*) with other surfaces, including the top surface of the insulating layer:



Id., Fig. 29.

202. Fang also discloses planarizing the insulating layer and the etch-stop

layer. §XV.I.1. A POSITA would have found it obvious that Han's and Fang's planarization processes are at least compatible. Both involve planarizing the insulating layer. Indeed, because the top surface of the staircase structure must be planar (§XIII.H.1), a POSITA would have found it obvious that both would planarize the insulating layer and the conductive structures. This compatibility would have made their combination obvious and yielded a reasonable expectation of success.

L. Claim 12:

1. [12] "The method of claim 1, wherein forming the staircase structure further comprises performing a repetitive etch-trim process on the sacrificial layers and the dielectric layers."

203. Han in view of Fang renders obvious *forming the staircase structure* ("stepwise structure" ST) *further comprises performing a repetitive etch-trim process on the sacrificial layers* ("sacrificial layers SL") *and the dielectric layers* ("insulating layers ILD").

204. Fang discloses that "[t]he stairs are formed by repeatedly trimming and etching exposed regions of the conductive structures." Ex. 1006, [0003]. "By conducting repeated etch and trim acts, the stepped profile (e.g., stairs 125) of the staircase structure 105 is formed." *Id.*, [0019].

205. A POSITA would have understood Fang's *repetitive etch-trim process*

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can be applied on Han's staircase structure, if it is not already implied by Han's disclosure. Specifically, Han discloses that the relative etching selectivities between its sacrificial layers SL and insulating layers ILD "may be relatively great in a wet etching process" but "relatively small in a dry etching process." Ex. 1007, [0098]. The former is needed for removing the sacrificial layers while preserving the insulating layers. *Id.*, [0116] (describing a wet etching process "using an etching solution" to remove sacrificial layers SL). A POSITA would have understood the relative small etching selectivities to be conducive to the etching process to form the staircase structure because when both layers have similar etching rates, they can be etched together, as required to form the staircase structure. A mask-trimming process was a conventional process of forming a staircase structure. §XIII.I.1 (sequence of figures showing the etch-trim process). Therefore, either Han implies the use of a repetitive etch-trim process, or its use would have been obvious in view of Fang.

M. Claim 13:

1. [13.PRE] "The method of claim 1, wherein replacing the sacrificial layer of each step with the gate stack comprises:"

206. This preamble simply repeats limitation [1.D]. §XII.A.5.

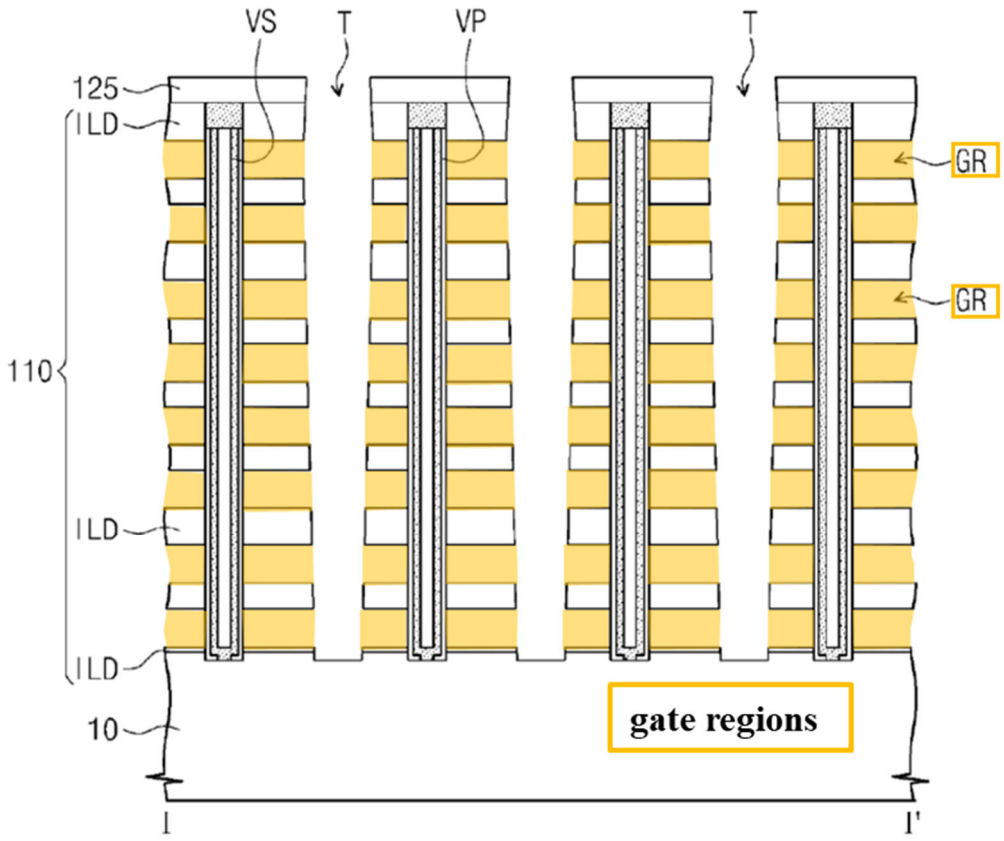
2. [13.A] "forming a substrate opening through the staircase structure;"

207. Han discloses *forming a substrate opening* ("trench T") *through the*

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staircase structure ("stepwise structure" ST):

FIG. 18



Ex. 1007, Fig. 18. Trench T "expos[es] the substrate 10 between the vertical structures VS." *Id.*, [0110], [0112]. Trenches T will be filled with a conductive material to provide contact to a common source for the memory string. *Id.*, [0119], [0121]. The common source is a doped region in the substrate. *Id.*, [0121]. Therefore, trenches T must expose the substrate for the contact to be formed.

3. [13.B] "removing the sacrificial layer of each step through the substrate; and"

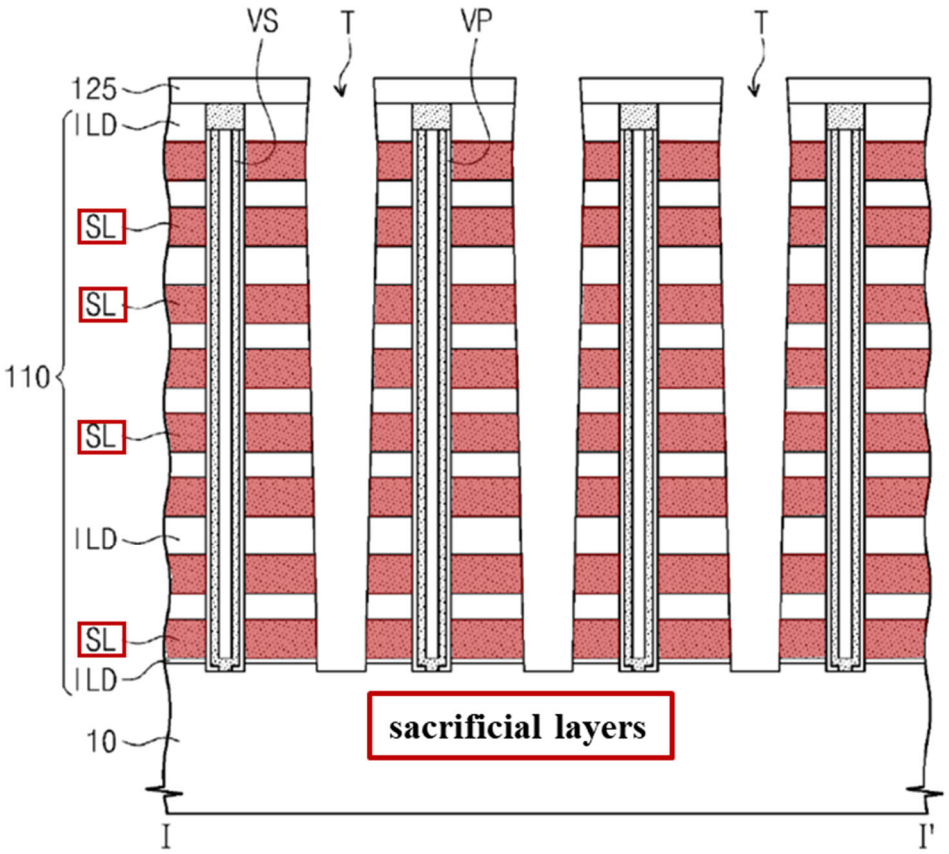
208. Preliminarily, *the substrate* appears to be an error. I have been

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instructed to treat the term as *the substrate opening*. §XIII.J.3.

209. Han discloses *removing the sacrificial layer* ("sacrificial layer SL") *of each step through the substrate [opening]* ("trench T"). Specifically, trenches T "expose sidewalls of the sacrificial layers SL and the insulating layers ILD." Ex. 1007, [0112]:

FIG. 17



Id., Fig. 17. Then, "the sacrificial layers SL exposed by the trenches T may be removed to form gate regions GR between the insulating layers ILD." *Id.*, [0115]-[0116].;

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4. [13.C] "disposing the first high-k dielectric layer and the conductive layer in place of the sacrificial layer."

210. Han discloses *disposing the first high-k dielectric layer* ("horizontal insulating layer") *and the conductive layer* (one of "electrodes EL") *in place of the sacrificial layer* ("sacrificial layer SL"). Specifically, after the sacrificial layers have been removed and the gate regions GR are formed in their place, "a horizontal insulating layer may be formed to conformally cover inner surfaces of the gate regions GR." Ex. 1007, [0118]. "Subsequently, a gate conductive layer may be formed to fill the gate regions GR…." *Id.*, [0119]. I explained above the processing sequence of removing the sacrificial layers and disposing the gate stack layers, and that the formation of a data storage layer in the horizontal gate region is an artifact of the manufacturing process of forming the layer after removing the sacrificial layers. §XV.A.5. Claim 13 simply recites the separate steps of limitation [1.D].

211. Fang discloses a replacement gate process in which the sacrificial layer is replaced with a conductive layer. §XV.A.5. The details of such process were "known in the art and are not described in detail" in Fang. Ex. 1006, [0025]. A POSITA would have found it obvious that Han's process of using a substrate opening to remove the sacrificial layers was at least compatible with Fang's replacement gate process.

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N. Claim 14:

1. [14] "The method of claim 13, wherein disposing the first high-k dielectric layer comprises disposing hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide and/or any combination thereof."

212. Han discloses that *disposing the first high-k dielectric layer* ("horizontal insulating layer") *comprises disposing hafnium oxide … [or] aluminum oxide…*. As explained, the horizontal insulating layer may comprise a tunnel insulating layer TIL and a blocking insulating layer BK. §XV.A.5. Both sublayers may comprise *hafnium oxide* or *aluminum oxide*. Ex. 1007, [0140]-[0141]. Again, a high-k dielectric layer for data-storing layer was well known by the time of the '276 Patent.

O. Claim 15:

1. [15] "The method of claim 13, wherein disposing the conductive layer comprises disposing tungsten, cobalt, nickel, copper, aluminum, and/or any combination thereof."

213. Han discloses that *disposing the conductive layer* (one of "electrodes EL") *comprises disposing tungsten, cobalt, … copper, [or] aluminum…*. Ex. 1007, [0119] ("the metal layer may include a metal material such as W, Al, …, Co, or Cu."). These metals are good conductors and are suitable for gate electrodes.

214. Similarly, Fang discloses that *the conductive layer* ("conductive materials 140") may comprise a metal such as *tungsten, cobalt, nickel, copper, aluminum*, "or combinations thereof." Ex. 1006, [0026].

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P. Motivation to Combine

215. A POSITA would have been motivated to adapt Han's staircase structure by adding Fang's etch-stop layer based on Fang's teaching. It would have been obvious and indeed readily apparent that "the conductive structures [conventionally used for word line contacts of 3D memory devices] include both shallower conductive structures and the deeper conductive structures." Ex. 1006, [0003]. Therefore, it was necessary to etch openings of "various depths." *Id.*, [0004]. But that resulted in an increased likelihood of "overetch[ing] (*e.g.*, punch through) into the conductive structures." *Id.* "Adjustments to etch chemistries …[, however,] ha[d] not sufficiently addressed this problem." *Id.* Using multiple masks to prevent punch-through "add[ed] additional processing acts, complexity, and cost to the overall process." *Id.* Other prior art confirmed this problem and shortcomings of the conventional solutions to be well within a POSITA's knowledge. For example, another reference discloses "depositing an encapsulation layer over a staircase structure … to prevent punchthrough of a wordline." Ex. 1009, Abstract. It similarly describes the nature of the problem and the shortcomings of the conventional solutions. *Id.*, [0042], [0044]. A POSITA would have recognized Han's method suffered from this exact problem and the shortcomings of the conventional solutions and would have been motivated to apply Fang's solution of adding an etch-stop layer to resolve this problem to "reduc[e] the likelihood of punch

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through." Ex. 1006, [0026], [0028].

216. Curiously, this is exactly the problem and purported solution described in the '276 Patent. §VI. But the '276 Patent came later.

217. The combination of this Ground also references Fang for its teaching on dry etching (§XV.C.1), CMP (§XV.I.1), and etch-trim (§XV.L.1). In each of these cases, as explained above in the respective sections, Han discloses using the same method. A POSITA would have been motivated to follow Fang's teaching in the combination because doing so would have been cost efficient for reusing the same tools (such as for etching or polishing), and time efficient for leveraging a POSITA's familiarity with Han, which is the primary reference of this Ground. Other specific factors would have further motivated a POSITA to apply Fang's teaching. Anisotropic dry etching, having good directionality, is well suited for etching small but deep openings. CMP was well-known, routine, and well suited for planarizing a top semiconductor surface. And Han implies the use of an etch-and-trim process (as explained in §XV.L.1), which was also well known and routine for forming a staircase structure. Further, a POSITA would have had a reasonable expectation of success in simply applying a method already disclosed by both Han and Fang to the combined, similar embodiment. Furthermore, since a POSITA would have been motivated to adopt Fang's etch-stop layer into Han's staircase structure, it would have been natural for the POSITA to consider Fang's full

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disclosure and how that might apply to the combination. Having done so, a POSITA would have found these routine processes to be compatible with the combined embodiment.

218. I have noted the similarities and compatibility of Han and Fang throughout this Ground. Moreover, the combination—introducing Fang's etch-stop layer in an additional manufacturing step between formation of a staircase and depositing an insulating layer—would have been straightforward. These factors, a POSITA's knowledge of etch-stop layers (as reflected in, *e.g.*, §V, Kim, Chen) and the well-known and routine processes, and the flexibility of layer materials and etchants all would have provided a POSITA a reasonable expectation of success. Indeed, as indicated by Kim, the techniques had been known for many years before the '276 Patent. A POSITA would have found a combination of Han and Fang to be a certain success.

XVI. GROUND 4: HAN IN VIEW OF FANG IN FURTHER VIEW OF CHEN

A. Claim 17:

1. [17] "The method of claim 1, further comprising: prior to disposing the etch-stop layer, disposing a barrier layer on each step of the plurality of steps, wherein the barrier layer protects underlying structures during the etching of the exposed portions of the etch-stop layer."

219. Chen discloses the additional limitation of claim 17.

220. Chen discloses *prior to disposing the etch-stop layer* ("second stop

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layer 220”), *disposing a barrier layer* (“first stop layer 210”) *on each step of the plurality of steps*:

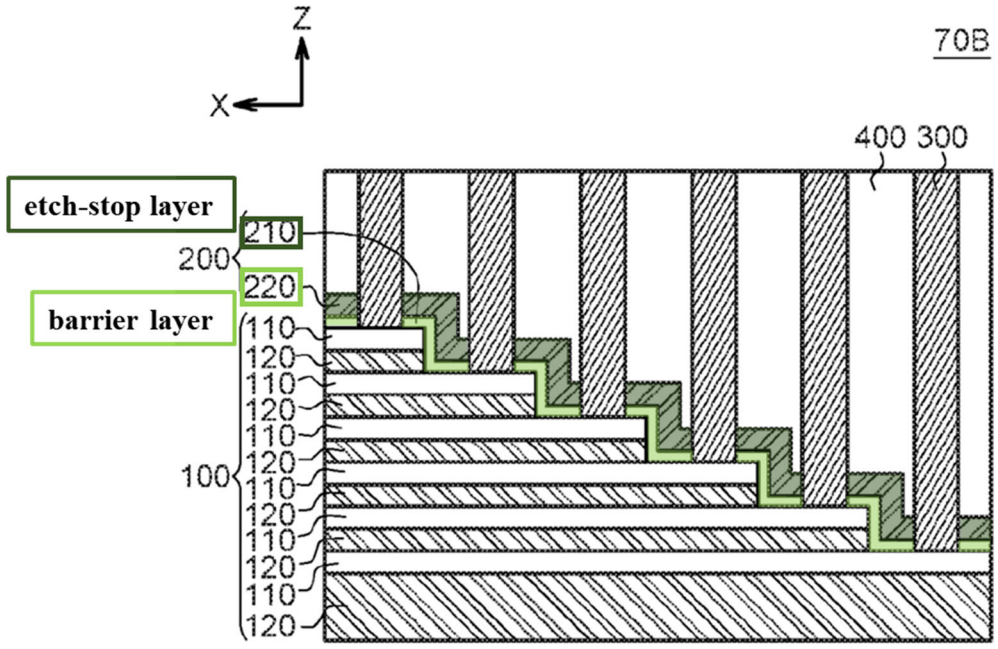


FIG. 7B

Ex. 1008, Fig. 7B, [0046] (“the first stop layer 210 is formed on the surfaces of the conductive layers 110, and the second stop layer 220 is formed on the first stop layer 210.”); [0037], [0039]. Note that Figure 7B is a gate-electrode-on-top configuration, similar to Han and the ’276 Patent.

221. Chen renders obvious that the barrier layer (“first stop layer 210”) protects *underlying structures during the etching of the exposed portions of the etch-stop layer* (“second stop layer 220”). First, these two layers take the place of an *etching stop* layer 200. *Id.*, [0037]. That name indicates that the function of the first (and the second) stop layer is to stop (or, more precisely, slow down) etching when

it reaches the layer, thereby protecting the underlying structures. As explained, for a lower layer to serve as an etch stop, it must have a slower etching rate than the upper layer above it, which also means the two layers must comprise different materials. §VIII. After disclosing a large set of viable materials for the first and second stop layers, Chen specifically notes that the two stop layers have "different" materials. Ex. 1008, [0041]. A POSITA would have understood this to mean that the first stop layer serves as an etch stop to the layer above it, *i.e.*, the second stop layer or *the etch-stop layer*.

B. Claim 18:

1. [18] "The method of claim 17, wherein disposing the barrier layer comprises disposing one or more of silicon oxide, silicon oxynitride, silicon nitride, TEOS, aluminum oxide, and silicon oxide incorporated with F, C, N, or H."

222. Chen discloses that *disposing the barrier layer* ("first stop layer 210") *comprises disposing one or more of silicon oxide, … [and] aluminum oxide…*. Ex. 1008, [0041] ("the first stop layer 210 may include silicon oxide (SiO_2), aluminum oxide (Al_xO_y, *e.g.* Al_2O_3)….").

C. Motivation to Combine

223. It is my opinion that a POSITA would have been motivated to add Chen's barrier layer to Han's staircase structure with Fang's etch-stop layer.

224. Unintended short circuits between circuit components are a basic electrical-engineering problem to be avoided. Indeed, this is more basic than

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engineering 101. A child is usually taught that bad things happen when short circuits are created. The same is true in semiconductor devices, including 3D memory devices. For example, short circuit between conductive layers in a word line staircase was also known to be an issue to be prevented. Ex. 1028, 6:22-28. Chen discloses a short-circuit phenomenon through electron tunneling between conductive layers of a word-line staircase. Ex. 1008, [0049]. A POSITA would have recognized this phenomenon should be avoided.

225. I explained above the concept of "tunneling." §XII.D. Chen discloses increasing the tunneling length of the etch-stop layer(s) to reduce tunneling current, thereby "more effectively electrically isolat[ing] [the conductive layers] from one another." Ex. 1008, [0004]. Adding a first stop layer (the barrier layer of the '276 Patent) to Fang's etch-stop layer increases the tunneling length. Specifically, Fang's etch-stop layer may comprise a high-k dielectric. Ex. 1006, [0022]. A single aluminum-oxide high-k-dielectric etch-stop layer (as in Fang) can have a tunneling length L2 shown in Figure 8B of Chen. Ex. 1008, [0048]. When a silicon-oxide barrier layer is added, the total tunneling length becomes L4 as shown in Figure 8D. *Id.*, [0052]. It is apparent that L4 is larger than L2:

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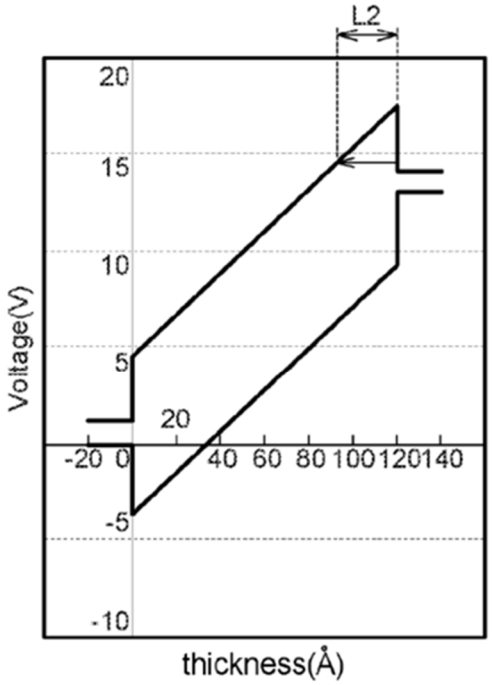


FIG. 8B

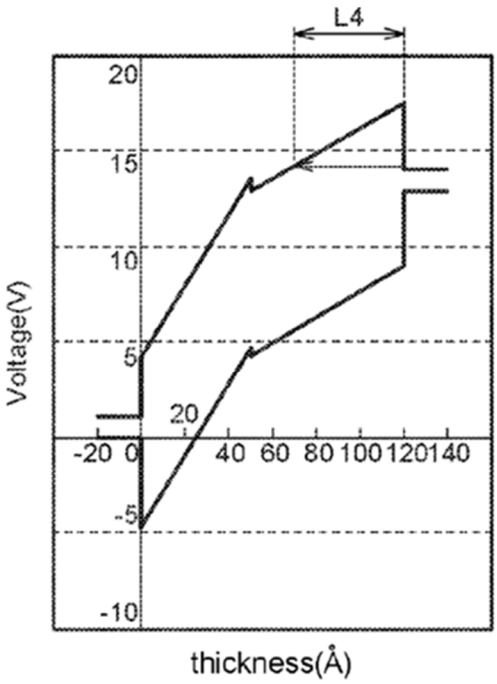


FIG. 8D

Id., Figs. 8B, 8D. Although the thickness shown on the x-axis of Figures 8B and 8D (up to about 120 Å) may be different from Fang's, that does not matter for at least two reasons. First, the concept taught by Chen and the trend revealed by the figures are not limited to specific thicknesses. Second, Claims 17 and 18 do not require any particular etch-stop thickness. And the flexibility of etchants and layer materials permits adjusting etch-stop thickness (which is not necessary because of the first reason). Thus, by adding a barrier layer to a high-k dielectric etch-stop layer, "the overall etching stop layer 200 [including the barrier layer] can further provide a relatively large tunneling length," reducing the "occurrence of short circuit between

different conductive layers" and increasing "the stability of the semiconductor device." *Id.*, [0053].

226. Further, like Fang, Chen discloses an embodiment with only one etch-stop layer 200. Ex. 1008, Fig. 4B, [0035]. The etch-stop layer 200 may comprise two stop layers 210 and 220 as shown in Figure 7B. *Id.*, [0037], [0046]. Thus, a one- or two-stop-layer embodiment represents a design choice, both suitable for word line contact structures. In other words, a POSITA having a single-layer embodiment as taught by either Fang or Chen would have recognized that two etch-stop layers was a suitable alternative, as taught by Chen. Either configuration would have been obvious, and a POSITA would have been motivated to adopt a two-layer configuration to increase the tunneling length as explained above.

227. Chen's manufacturing methods to form two etch-stop layers is simply that one step of forming layer 200 "is divided into two separate steps." *Id.*, [0059]. A POSITA would have had a reasonable expectation of success of performing such a simple division. Indeed, reflecting the knowledge of a POSITA, when disclosing both one- and two-etch-stop-layer embodiments, Kim simply notes "[i]n some embodiments, the etch stop layer 125 may include a first stop layer 125a … and a second stop layer 125b…." Ex. 1005, [0187]. The brevity of both Chen's and Kim's descriptions confirms that implementing a two-layer embodiment was well within the knowledge and skill of a POSITA, leading to a reasonable expectation of success.

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Moreover, although not explained in detail here, it is readily apparent from Chen's Figure 7B that the staircase structure formed by its method is remarkably similar to Han's and Fang's. Such similarities would have bolstered a POSITA's reasonable expectation of success.

XVII. SECONDARY CONSIDERATIONS OF NON-OBVIOUSNESS

228. During my review of the materials discussed herein, I did not become aware of any evidence suggesting the existence of any secondary indicia or considerations of non-obviousness. In the event that Patent Owner proffers any such evidence, I shall provide my opinions on such evidence in a reply declaration.

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XVIII. DECLARATION

229. In signing this declaration, I realize that this declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the USPTO.

230. I am aware that willfully false statements and the like made by me in connection with this declaration are punishable by fine or imprisonment, or both (18 U.S.C. § 1001) and may jeopardize the validity of the Petition. All statements herein made by me of my own knowledge are true and all statements made on information and belief are believed to be true. I declare under penalty of perjury that the foregoing is true and correct.

Executed this 29th day of November 2024 at Austin, Texas.



Sanjay Banerjee, Ph.D.

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