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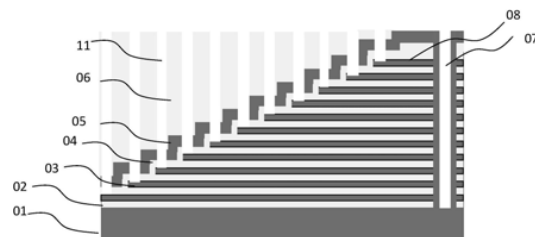
Claims 2 Pages Specification 4 Drawings 5 Pages
Pages

(54) Title of Invention

A Multi-level Contact of Three-dimensional Memory
Array and Manufacturing Method Thereof

(57) Abstract

The present invention provides a multi-level contact of a three-dimensional memory array and a manufacturing method thereof. Through structural adjustment, the contact structure can be prepared in 3D NAND technology with only one layer of photomask. By placing a termination layer for selectivity transition above the staircase silicon/substrate structure, during the etching process, an etching process with a high selectivity is first used to stop the contact channel on the termination layer, and then the reverse direction is used. The selective etching process removes the termination layer, and finally achieves the purpose of uniformly opening the contact channel above the staircase silicon/substrate structure. Through the above mentioned process provided by the present invention, the situation of insufficient etching or over-etching caused by using a layer of photomask for etching in the prior art is avoided. Using this new process can save costs, reduce process complexity, and expand the process window.



1. A method for preparing a three-dimensional memory structure, including:
 In the first step, etching of the staircase structure:
 Provide substrate;
 Form a stacked layer on the surface of the substrate, the stacked layer including a plurality of alternately overlaying oxide layers and nitride layers;
 The stacked layer is then etched to form a stacked layer with a staircase structure;
 In the second step, a second oxide layer with a staircase structure is formed on the stacked layer of the staircase structure:
 In the third step, a termination layer of the staircase structure is formed on the second oxide layer of the staircase structure;
 In the fourth step, the termination layer of the staircase structure is filled to form a third oxide layer with the same height as the uppermost layer of the termination layer of the staircase structure. After the third oxide layer is formed, chemical mechanical polishing (CMP) is used. The process makes the height of the third oxide layer of each stage flush with the uppermost layer of the termination layer of the staircase structure;
 In the fifth step, the uppermost termination layer of the termination layer of the staircase structure is etched to form a contact opening that penetrates each layer until it contacts the substrate, and then the silicon nitride layer is then replaced with a metal layer including the insulating film HK;
 In the sixth step, the third oxide layer is etched and high-selectivity etching is carried out to form contact channels reaching the termination layer of each step of the staircase structure;
 In the seventh step, reverse selectivity etching is used to further etch the contact channel, and through each step of the staircase structure termination layer, a contact channel reaching the second oxide layer is obtained;
 In the eighth step, the contact channel is further etched, and through the second oxide layer and the insulating film HK, a contact channel reaching the metal layer of the insulating film HK is obtained;
 In the ninth step, after the through holes are realized by etching in the previous steps, the metal connection structure is realized by metal filling and grinding.
2. A method for preparing a three-dimensional memory structure according to Claim 1, wherein the termination layer is silicon nitride.
3. A method for preparing a three-dimensional memory structure according to Claim 1, wherein the metal layer of the insulating film HK includes tungsten.
4. A method for preparing a three-dimensional memory structure according to Claim 1 or 3, wherein the insulating film HK is a hafnium oxide film, a zirconium oxide film, an aluminum oxide film, a tantalum oxide film or a lanthanum oxide film.
5. A three-dimensional memory structure prepared by the method described in any one of Claims 1-3.
6. A three-dimensional memory structure including:
 Substrate 01;
 A stacked layer, in a staircase structure, is formed on the surface of the substrate 01. The stacked layer includes a plurality of alternately overlaying first oxide layers 02 and a metal layer including an insulating film HK;
 The second oxide layer 04 has a staircase structure and is located on the stacked layer of the staircase structure;
 The termination layer 05 has a staircase structure and is located on the second oxide layer 04 of the staircase structure;
 The third oxide layer 06 is formed on the termination layer 05; the third oxide layer 06 is flush with the uppermost layer 08 of the termination layer of the staircase structure;
 A contact channel is formed between adjacent third oxide layers 06, passing through the second oxide layer 04 and the insulating film HK to reach the contact channel 11 of the metal layer of the insulating film HK;
 The contact opening 07 is located on the uppermost termination layer 08 of the termination layer of the staircase structure, and penetrates through each layer until it contacts the substrate.
7. A three-dimensional memory structure of Claim 6, wherein the termination layer is nitride.
8. A three-dimensional memory structure of Claim 6 or 7, wherein the metal layer of the insulating film HK includes tungsten.

9. A three-dimensional memory structure according to Claim 6 or 8, wherein the insulating film HK is a hafnium oxide film, a zirconium oxide film, an aluminum oxide film, a tantalum oxide film or a lanthanum oxide film.

A Multi-level Contact for a Three-dimensional Memory Array and its Manufacturing Method

Technical field

[0001] The present invention relates to the field of semiconductor devices, and in particular to multi-contact three-dimensional memory arrays and manufacturing methods thereof.

Background technology

[0002] Prior art methods of fabricating contacts for multi-level memory arrays such as monolithic 3D arrays. The multi-level memory device includes at least one device area in which memory cells (for example, vertical NAND strings) are located and at least one contact area in which the multi-level contacts are located. The far ends of the control gates of the multi-level vertical NAND memory array are arranged in a staircase structure. In this manner, electrical contact to the individual control gates can be achieved by etching an array of openings in the surrounding dielectric layer from the upper surface of the memory array down to the step and depositing contact metal in the opening to contact the step. In the conventional method of making the control gate contacts of a multi-level memory array, when a one-layer photomask process is used, since one type of etchant is used to etch to the bottom, due to the different step heights, the resulting etching depth at different locations is difficult to control, resulting in problems of under-etching or over-etching. Typically two or three layers of masks are required to accomplish process goals. Therefore, the existing three-dimensional memory NAND process uses multi-layer masks to achieve the production of contact structures, making the process complex and costly.

Content of the invention

[0003] The purpose of the present invention is to provide a multi-level contact of a three-dimensional memory array and a manufacturing method thereof. By adjusting the structure, only one layer of photomask is needed to prepare the contact structure in 3D NAND technology. By placing a termination layer for selectivity transition above the staircase silicon/substrate structure, during the etching process, an etching process with a high selectivity is first used to stop the contact channel on the termination layer, and then the termination layer is removed using an etching process with a reverse selectivity ratio, and finally the purpose of uniformly opening the contact channels above the staircase silicon/substrate structure is achieved.

[0004] The present invention uses an etching termination layer. Since the termination layer and its adjacent layers have completely different etching effects with respect to the etchant during the etching process, therefore, through the selection of etchants with different etching selectivity ratios, the first etching can be achieved to accurately stay on the etching termination layer, and then the second etching can be used to achieve the contact via holes to accurately stay on the metal layer. Compared with the original method of only using one type of etchant to etch to the bottom, the etching depth at different positions caused by different step heights is difficult to control, resulting in the problem of under-etching or over-etching, the present invention improves the etching accuracy.

[0005] The object of the present invention is achieved by the following technical scheme.

[0006] By placing a termination layer for selective ratio transition above the staircase silicon/substrate structure, During the etching process, an etching process with a high selectivity ratio is first used to stop the contact channel on the termination layer, and then an etching process with a reverse selectivity ratio is used to remove the termination layer. Finally, the purpose of uniformly opening the contact channel above the staircase silicon/substrate structure is achieved.

[0007] A method of making a three-dimensional memory structure, comprising:

[0008] In the first step, etching of the staircase structure:

[0000] Provide a substrate;

[0010] Form a stacked layer on the surface of the substrate, the stacked layer including a plurality of alternately overlaying oxide layers and nitride layers;

[0011] The stacked layer is then etched to form a stacked layer with a staircase structure;

[0012] In the second step, a second oxide layer with a staircase structure is formed on the stacked layer of the staircase structure:

- [0013] In the third step, a termination layer of the staircase structure is formed on the second oxide layer of the staircase structure;
- [0014] In the fourth step, the termination layer of the staircase structure is filled to form a third oxide layer with the same height as the uppermost layer of the termination layer of the staircase structure. After the third oxide layer is formed, chemical mechanical polishing (CMP) is used. The process makes the height of the third oxide layer of each step flush with the uppermost layer of the termination layer of the staircase structure;
- [0015] In the fifth step, the uppermost termination layer of the termination layer of the staircase structure is etched to form a contact opening that penetrates each layer until it contacts the substrate, and then the silicon nitride layer is then replaced with a metal layer including the insulating film HK;
- [0016] In the sixth step, the third oxide layer is etched and high-selectivity etching is carried out to form contact channels reaching the termination layers of each step of the staircase structure;
- [0017] In the seventh step, reverse selectivity etching is used to further etch the contact channel, and through each staircase structure termination layer, a contact channel reaching the second oxide layer is obtained;
- [0018] In the eighth step, the contact channel is further etched, and through the second oxide layer and the insulating film HK, a contact channel reaching the metal layer of the insulating film HK is obtained;
- [0019] In the ninth step, after the through holes are realized by etching in the previous steps, the metal connection structure is realized by metal filling and grinding.
- [0020] Preferably, the termination layer is silicon nitride.
- [0021] Preferably, the metal layer of the insulating film HK comprises tungsten.
- [0022] Preferably, the insulating film HK is a hafnium oxide film, a zirconium oxide film, an aluminum oxide film, a tantalum oxide film or a lanthanum oxide film.
- [0023] A three-dimensional memory structure prepared by any of the methods described above.
- [0024] A three-dimensional memory structure comprising:
- [0025] Substrate 01;
- [0026] A stacked layer formed on the surface of the substrate 01 in a staircase structure, the stacked layer comprising a plurality of alternately overlaying first oxide layers 02 and metal layers comprising an insulating film HK;
- [0027] A second oxide layer 04, in a staircase structure, on the stacked layer of the staircase structure;
- [0028] A termination layer 05, in a staircase structure, on the second oxide layer 04 of the staircase structure;
- [0029] A third oxide layer 06 formed on the termination layer 05; the third oxide layer 06 is flush with the uppermost layer 08 of the termination layer of the staircase structure;
- [0030] A contact channel formed between the adjacent third oxide layer 06 and through the second oxide layer 04 and the insulating film HK to reach the contact channel 11 of the metal layer of the insulating film HK;
- [0031] The contact opening 07 is located on the uppermost termination layer 08 of the termination layer of the staircase structure and penetrates through the layers until it is in contact with the substrate.
- [0032] Preferably, the termination layer is a nitride.
- [0033] Preferably, the metal layer of the insulating film HK comprises tungsten.
- [0034] Preferably, the insulating film HK is a hafnium oxide film, a zirconium oxide film, an aluminum oxide film, a tantalum oxide film or a lanthanum oxide film.
- [0035] An advantage or benefit of the present invention is that: Through the above process provided by the present invention, the original one-step etch is changed to two-step etch by using the setting of an etching termination layer. The principle is that the termination layer used has different etch effects for different etchants, thereby avoiding under-etching or over-etching produced during the etch process with one layer of photomask in the prior art. The use of this new process can save costs, reduce process complexity, and expand the process window.

Description of Drawings

[0036] Various other advantages and benefits will become apparent to those of ordinary skill in the art by reading the following detailed description of the preferred embodiments. The drawings are for the purpose of illustrating preferred embodiments only and are not to be construed as limiting the invention. Also throughout the drawings, the same reference characters are used to designate the same components. In the drawings:

[0037] Figure 1 shows a three-dimensional peninsula memory structure obtained by using a three-layer mask process in the background technology of the present invention;

[0038] Figure 2 shows a defective three-dimensional peninsula memory structure obtained by using a one-layer mask process in the background technology of the present invention;

[0039] Figures 3-10 show the schematic structural diagram of the structure preparation process flow for a three-dimensional memory according to an embodiment of the present invention.

Specific embodiments

[0040] Example embodiments of the present disclosure will be described in more detail below with reference to the drawings. While example embodiments of the disclosure are shown in the drawings, it should be understood that the disclosure may be implemented in various forms and should not be limited by the embodiments set forth herein. Rather, these embodiments are provided to enable a more thorough understanding of the disclosure and to fully convey the scope of the disclosure to those skilled in the art.

[0041] Referring to Figures 3-10, an embodiment of the present invention provides a structural preparation process for a three-dimensional memory, comprising the following steps:

[0042] A method of making a three-dimensional memory structure, comprising:

[0043] In the first step, etching of the staircase structure:

[0044] Provide a substrate 01;

[0045] Form a stacked layer on the surface of the substrate 01, the stacked layer including a plurality of alternately overlaying first oxide layer 02 and nitride layer 03;

[0046] The stacked layer is then etched to form a stacked layer with a staircase structure;

[0047] In the second step, a second oxide layer 04 with a staircase structure is formed on the stacked layer of the staircase structure:

[0048] In the third step, the termination layer 05 of the staircase structure is formed on the second oxide layer 04 of the staircase structure;

[0049] In the fourth step, the termination layer of the staircase structure is filled to form a third oxide layer 06 with the same height as the uppermost layer of the termination layer of the staircase structure. After the third oxide layer 06 is formed, chemical mechanical polishing (CMP) is used. The process makes the height of the third oxide layer 06 of each step flush with the uppermost layer of the termination layer of the staircase structure;

[0050] In the fifth step, the uppermost termination layer 08 of the termination layer of the staircase structure is etched to form a contact opening 07 that penetrates each layer until it contacts the substrate, and then the silicon nitride layer 03 is then replaced with a metal layer including the insulating film HK;

[0051] The insulating film HK is a film of insulating material having a higher dielectric constant (permittivity) than each of oxide and silicon nitride, that is, a so-called high-k film (high dielectric constant film). In the present application, a high-k film or a high dielectric constant film refers to a film having a dielectric constant (permittivity) higher than that of silicon nitride.

[0052] A metal oxide film may be used as the insulating film HK, such as a hafnium oxide film, a zirconium oxide film, an aluminum oxide film, a tantalum oxide film, or a lanthanum oxide film. Such metal oxide films may also comprise one or both of nitrogen (N) and silicon (Si). The insulating film HK may be formed, for example, by an atomic layer deposition (ALD) process. The insulating film HK has a thickness of, for example, 3 nm. When a high dielectric constant film (here the insulating film HK) is used as a gate insulating film, the physical thickness of the gate insulating film can be increased compared to the case with an oxide film; thus, the leakage current can be reduced.

[0053] In the sixth step, the third oxide layer 06 is etched and high-selectivity etching is carried out to form contact channel 09 reaching the termination layers of each step of the staircase structure;

[0054] In the seventh step, reverse selectivity etching is used to further etch the contact channel, and through each staircase structure termination layer 05, a contact channel reaching the second oxide layer 04 is obtained;

- [0055] In the eighth step, the contact channel is further etched, and through the second oxide layer 04 and the insulating film HK, a contact channel 11 reaching the metal layer of the insulating film HK is obtained;
- [0056] In the ninth step, after the through holes are realized by etching in the previous steps, the metal connection structure is realized by metal filling and grinding.
- [0057] The present invention provides a three-dimensional memory structure prepared by the aforementioned preparation method.
- [0058] Preferably, the termination layer is silicon nitride.
- [0059] Preferably, the insulating film HK is a hafnium oxide film, a zirconium oxide film, an aluminum oxide film, a tantalum oxide film or a lanthanum oxide film.
- [0060] A three-dimensional memory structure comprising:
- [0061] Substrate 01;
- [0062] A stacked layer formed on the surface of the substrate 01 in a staircase structure, the stacked layer comprising a plurality of alternately overlaying first oxide layers 02 and metal layers comprising an insulating film HK;
- [0063] A second oxide layer 04, in a staircase structure, on the stacked layer of the staircase structure;
- [0064] A termination layer 05 in a staircase structure on the second oxide layer 04 of the staircase structure;
- [0065] A third oxide layer 06 formed on the termination layer 05; the third oxide layer 06 is flush with the uppermost layer 08 of the termination layer of the staircase structure;
- [0066] A contact channel formed between adjacent third oxide layer 06 to reach a contact channel 11 of the metal layer of the insulating film HK through the second oxide layer 04 and the insulating film HK;
- [0067] The contact opening 07 is located on the uppermost termination layer 08 of the termination layer of the staircase structure and penetrates through the layers until contact with the substrate.
- [0068] Preferably, the termination layer is silicon nitride.
- [0069] Preferably, the insulating film HK is a hafnium oxide film, a zirconium oxide film, an aluminum oxide film, a tantalum oxide film or a lanthanum oxide film.
- [0070] The above description is only a preferred embodiment of the present invention, but the scope of protection of the present invention is not limited to this. Any readily conceivable change or replacement within the scope of the invention disclosed by any person skilled in the art of the present technology shall be covered by the scope of protection of the present invention. Therefore, the scope of protection of the present invention should be according to the scope of protection of its claims.

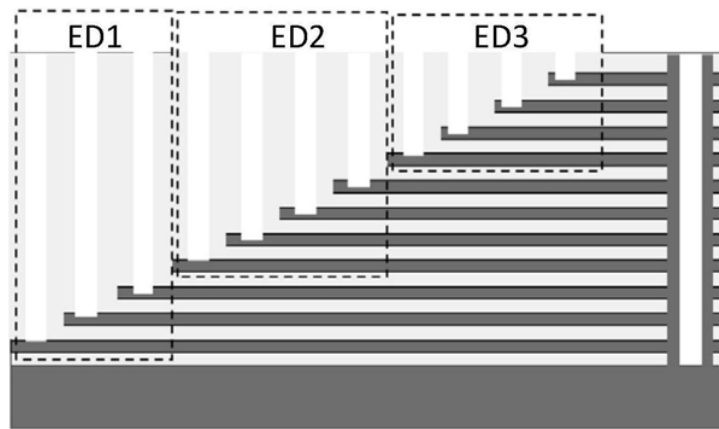


Figure 1

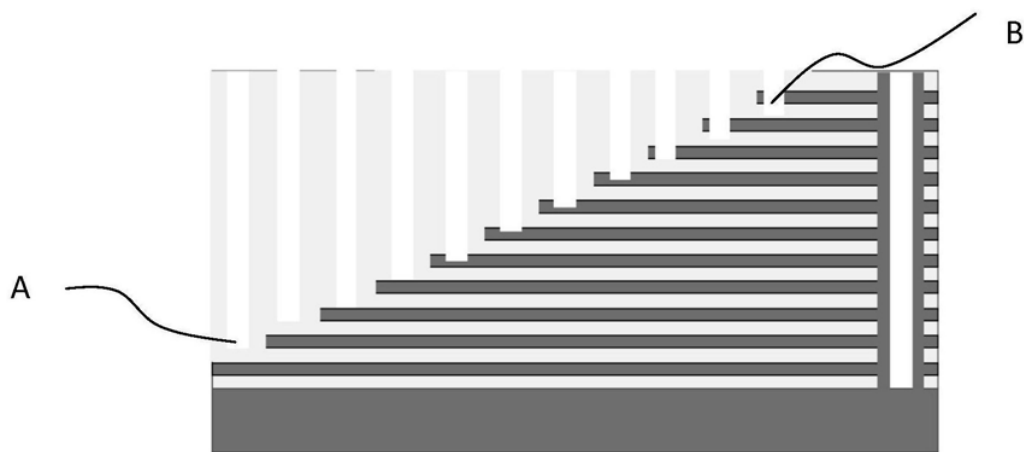


Figure 2

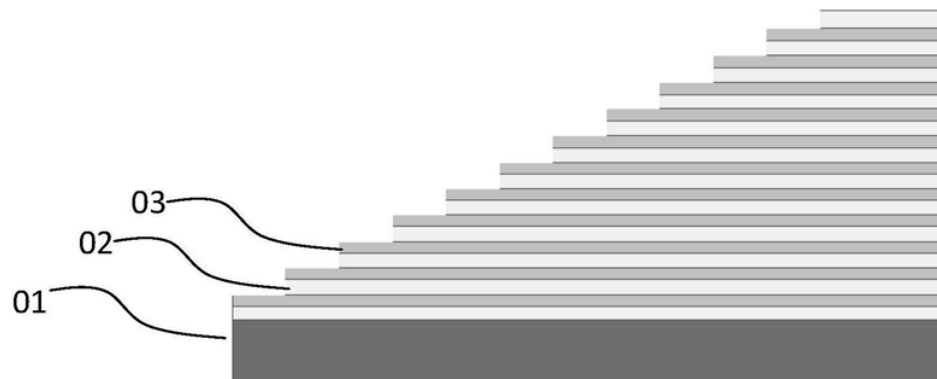


Figure 3

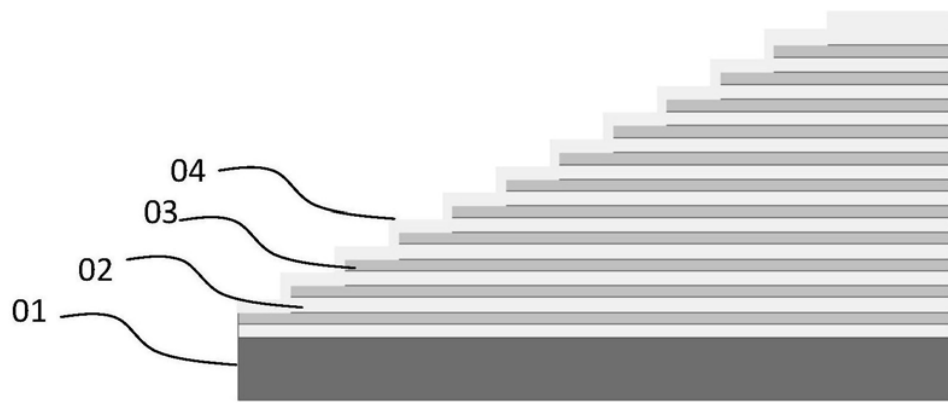


Figure 4

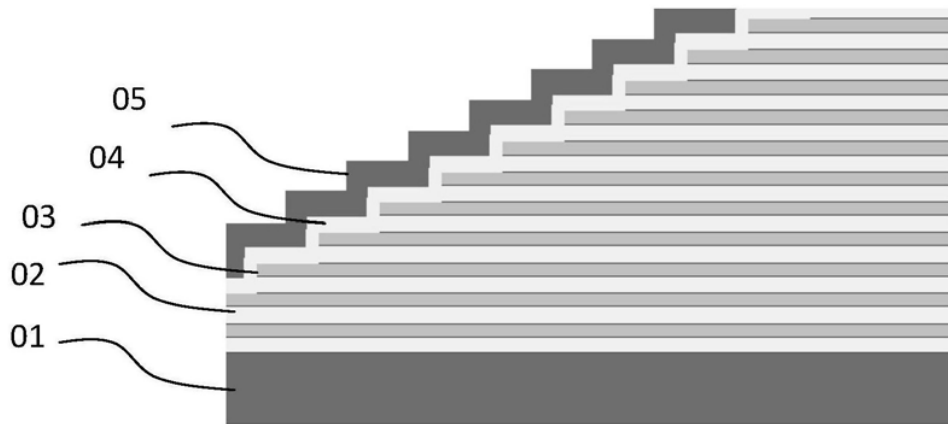


Figure 5

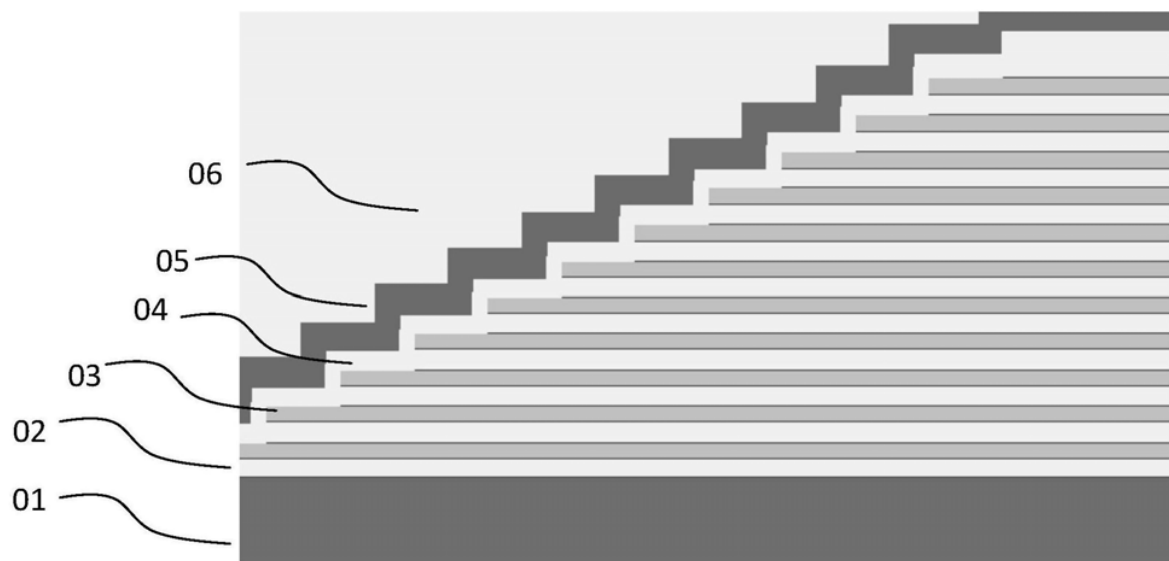


Figure 6

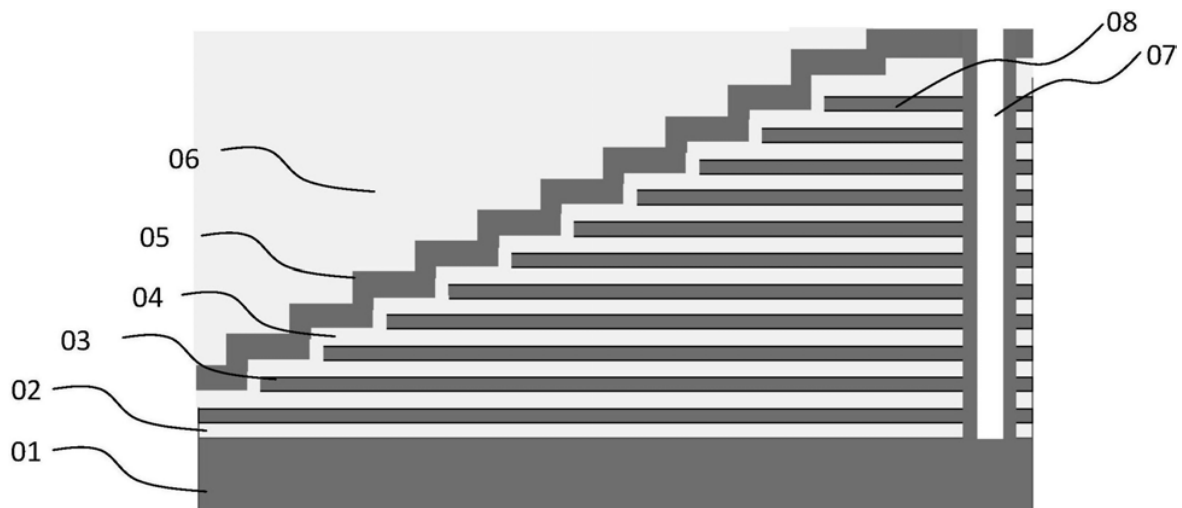


Figure 7

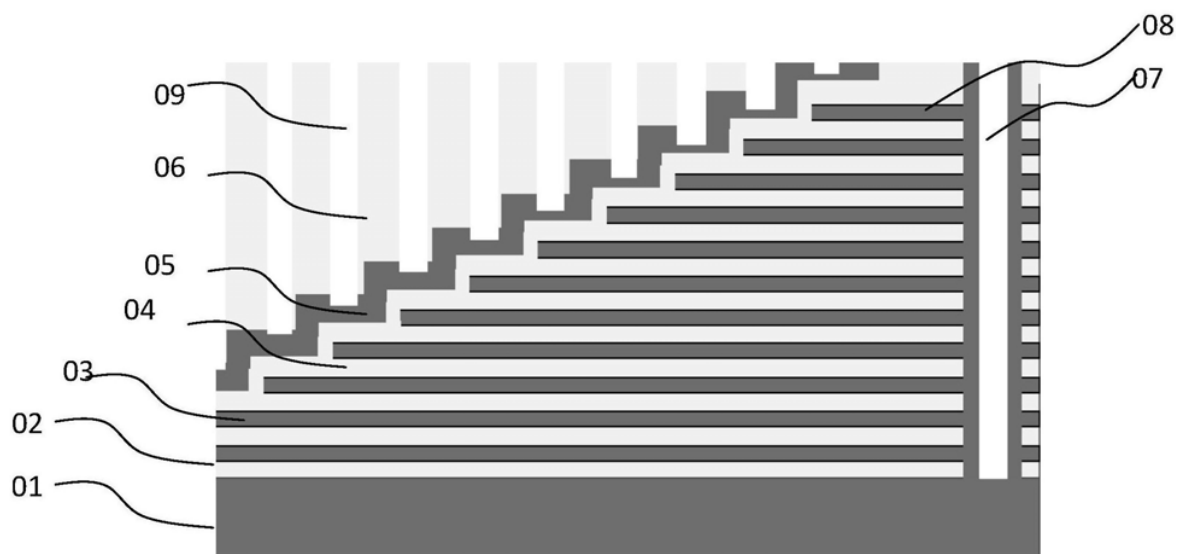


Figure 8

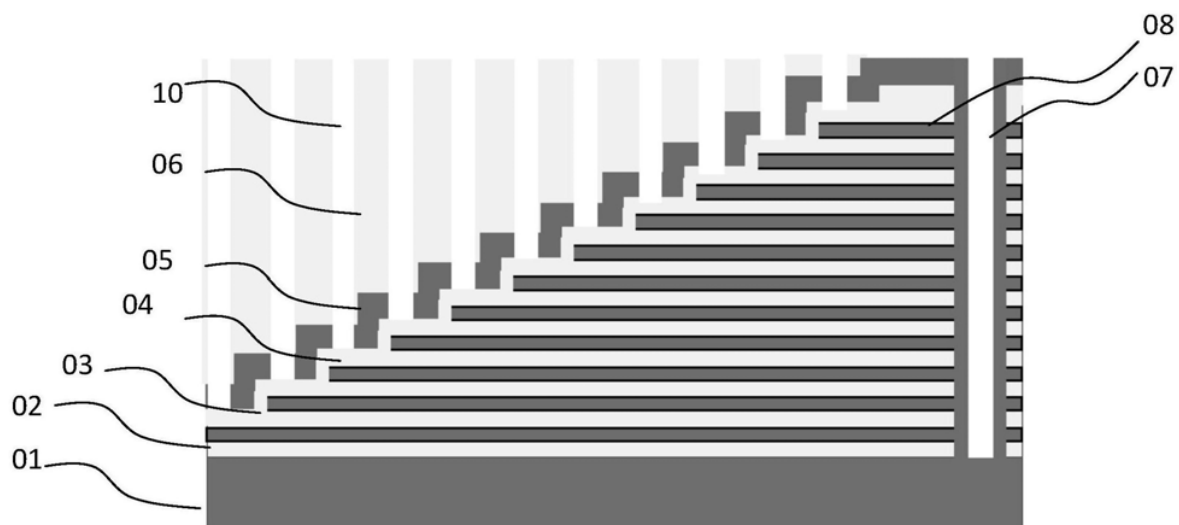


Figure 9

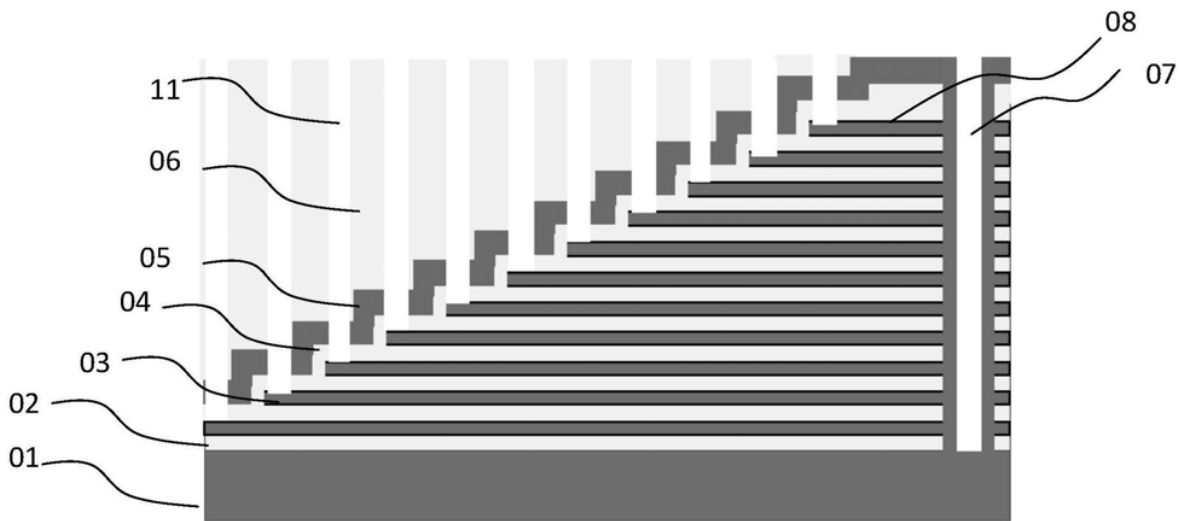


Figure 10

September 10, 2024

Certification

Translator's Declaration:

I, Karen Lee, hereby declare:

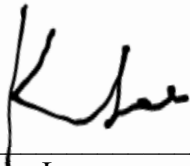
That I possess advanced knowledge of the Chinese and English languages.

My qualifications are as follows: Chinese is my native language; I have completed a Chinese language program at New York University; and I have over 10 years of training and experience in providing professional translation/interpretation.

The attached Chinese into English translation has been translated by me and to the best of my knowledge and belief, it is a true and accurate translation of:

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Karen Lee

Sworn to before me this

10th of September 2024



Signature, Notary Public

Mikhail E. Lezhnev
Notary Public ID No. 02LE6301549
State of New York Qualified in Kings County
Commission Expires on June 1, 2026

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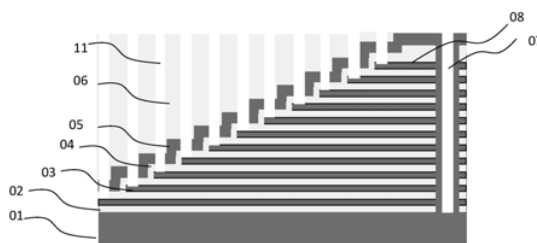
权利要求书2页 说明书4页 附图5页

(54)发明名称

一种三维存储器阵列的多级接触及其制造方法

(57)摘要

本发明提供一种三维存储器阵列的多级接触及其制造方法,可以通过结构的调整,只需要一层光罩就可以在3D NAND技术中实现接触结构的制备。通过在阶梯型硅/衬底结构上方放置用于选择比过渡的终止层,在刻蚀的过程中首先利用具有高选择比的刻蚀工艺,使接触通道停止在终止层上,再利用反向选择比的刻蚀工艺去掉终止层,最终实现均匀的打开台阶型硅/衬底上方的接触通道的目的。通过本发明提供的上述工艺,避免了现有技术中采用一层光罩进行刻蚀的过程中产生的刻蚀不足或过刻蚀的情况,采用这种新的工艺可以节省成本,降低工艺复杂度,扩大工艺窗口。



1. 一种三维存储器结构制备方法,包括:

第一步,阶梯式结构刻蚀:

提供基底;

在所述基底表面形成堆叠层,所述堆叠层包括多个交错叠加的氧化物层和氮化物层;

然后对堆叠层进行刻蚀,形成阶梯式结构的堆叠层;

第二步,在阶梯式结构的堆叠层上形成阶梯式结构的第二氧化物层;

第三步,在阶梯式结构的第二氧化物层上形成阶梯式结构的终止层;

第四步,在阶梯式结构的终止层上进行填充,形成与阶梯式结构的终止层的最高层等高的第三氧化物层,第三氧化物层形成后,采用化学机械抛光(CMP)工艺使得各台阶层的第三氧化物层的高度与阶梯式结构的终止层的最高层齐平;

第五步,蚀刻阶梯式结构的终止层的最高终止层,形成穿透各层直至接触基底的接触开口,然后将氮化硅层取代为包含绝缘膜HK的金属层;

第六步,刻蚀第三氧化物层,进行高选择比的刻蚀,形成达到各阶梯式结构的终止层的接触通道;

第七步,利用反向选择比的刻蚀,进一步刻蚀接触通道,透过各阶梯式结构终止层,得到达到第二氧化物层接触通道;

第八步,进一步刻蚀接触通道,透过第二氧化物层、绝缘膜HK,得到达到绝缘膜HK的金属层的接触通道;

第九步,在前述的步骤中通过刻蚀实现了通孔之后,通过金属填充和研磨实现金属连接结构。

2. 权利要求1所述的三维存储器结构制备方法,所述终止层是氮化硅。

3. 权利要求1所述的三维存储器结构制备方法,所述绝缘膜HK的金属层包括钨。

4. 权利要求1或3所述的三维存储器结构制备方法,所述绝缘膜HK为氧化钪膜、氧化锆膜、氧化铝膜、氧化钽膜或者氧化铌膜。

5. 一种三维存储器结构,其由权利要求1-3任一所述方法制备得到。

6. 一种三维存储器结构,包括:

基底01;

堆叠层,呈阶梯式结构,形成在所述基底01表面,所述堆叠层包括多个交错叠加的第一氧化物层02和包含绝缘膜HK的金属层;

第二氧化物层04,呈阶梯式结构,位于阶梯式结构的堆叠层上;

终止层05,呈阶梯式结构,位于阶梯式结构的第二氧化物层04上;

第三氧化物层06,形成在终止层05上;第三氧化物层06与阶梯式结构的终止层的最高层08齐平;

接触通道,形成在相邻的第三氧化物层06之间,透过第二氧化物层04、绝缘膜HK,达到绝缘膜HK的金属层的接触通道11;

接触开口07,位于阶梯式结构的终止层的最高终止层08上,并穿透各层直至接触基底。

7. 权利要求6所述的三维存储器结构,所述终止层是氮化物。

8. 权利要求6或7所述的三维存储器结构,所述绝缘膜HK的金属层包括钨。

9. 权利要求6或8所述的三维存储器结构,所述绝缘膜HK为氧化钪膜、氧化锆膜、氧化铝

膜、氧化钽膜或者氧化镧膜。

一种三维存储器阵列的多级接触及其制造方法

技术领域

[0001] 本发明涉及半导体装置领域,特别涉及三维存储阵列的多接触及其制造方法。

背景技术

[0002] 现有技术制造例如单片3D阵列的多级存储器阵列的接触的方法。多级存储器装置包括至少一个装置区域和至少一个接触区域,存储器单元(例如垂直NAND串)位于该至少一个装置区域,多级接触位于该至少一个接触区域。多级垂直NAND存储器阵列的控制栅的远端以台阶式构造布置。以此方式,通过从存储器阵列的上表面向下至台阶蚀刻在四周的介电层中的开口的阵列以及在该开口中沉积接触金属以接触该台阶,可以实现到单独控制栅极的电接触。在制作多级存储器阵列的控制栅级的接触的常规方法中,当采用一层光罩工艺时,由于采用通过一种类型的刻蚀剂一刻到底的方式,实际刻蚀过程中由于台阶高低不同引起的不同位置刻蚀深度难于控制造成刻蚀不足或过刻蚀的问题出现。通常需要两层或三层光罩才能完成工艺目标。因此,现有三维存储器NAND工艺通过多层光罩实现接触结构的制作,使得工艺复杂,成本高。

发明内容

[0003] 本发明的目的就是要提供一种三维存储器阵列的多级接触及其制造方法,可以通过结构的调整,只需要一层光罩就可以在3D NAND技术中实现接触结构的制备。通过在阶梯型硅/衬底结构上方放置用于选择比过渡的终止层,在刻蚀的过程中首先利用具有高选择比的刻蚀工艺,使接触通道停止在终止层上,再利用反向选择比的刻蚀工艺去掉终止层,最终实现均匀的打开台阶型硅/衬底上方的接触通道的目的。

[0004] 本发明采用了一个刻蚀终止层,由于该终止层与其相邻的层在刻蚀工艺中对刻蚀剂的刻蚀效果有截然不同的结果,因此,可以通过不同刻蚀选择比的刻蚀剂的选择,实现第一次刻蚀精准的停留在刻蚀停止层,然后再利用第二次刻蚀实现接触通孔准确的停留在金属层上,相比于原来的只是通过一种类型的刻蚀剂一刻到底的方式,由于台阶高低不同引起的不同位置刻蚀深度难于控制产生刻蚀不足或过刻蚀的问题,提高了刻蚀精度。

[0005] 本发明的目的是通过以下技术方案实现的。

[0006] 通过在阶梯型硅/衬底结构上方放置用于选择比过渡的终止层,在刻蚀的过程中首先利用具有高选择比的刻蚀工艺,使接触通道停止在终止层上,再利用反向选择比的刻蚀工艺去掉终止层,最终实现均匀的打开台阶型硅/衬底上方的接触通道的目的。

[0007] 一种三维存储器结构制备方法,包括:

[0008] 第一步,阶梯式结构刻蚀:

[0009] 提供基底;

[0010] 在所述基底表面形成堆叠层,所述堆叠层包括多个交错叠加的氧化物层和氮化物层;

[0011] 然后对堆叠层进行刻蚀,形成阶梯式结构的堆叠层;

- [0012] 第二步,在阶梯式结构的堆叠层上形成阶梯式结构的第二氧化物层;
- [0013] 第三步,在阶梯式结构的第二氧化物层上形成阶梯式结构的终止层;
- [0014] 第四步,在阶梯式结构的终止层上进行填充,形成与阶梯式结构的终止层的最高层等高的第三氧化物层,第三氧化物层形成后,采用化学机械抛光(CMP)工艺使得各台阶层的第三氧化物层的高度与阶梯式结构的终止层的最高层齐平;
- [0015] 第五步,蚀刻阶梯式结构的终止层的最高终止层,形成穿透各层直至接触基底的接触开口,然后将氮化硅层取代为包含绝缘膜HK的金属层;
- [0016] 第六步,刻蚀第三氧化物层,进行高选择比的刻蚀,形成达到各阶梯式结构的终止层的接触通道;
- [0017] 第七步,利用反向选择比的刻蚀,进一步刻蚀接触通道,透过各阶梯式结构终止层,得到达到第二氧化物层接触通道;
- [0018] 第八步,进一步刻蚀接触通道,透过第二氧化物层、绝缘膜HK,得到达到绝缘膜HK的金属层的接触通道;
- [0019] 第九步,在所述的步骤中通过刻蚀实现了通孔之后,通过金属填充和研磨实现金属连接结构。
- [0020] 优选地,所述终止层是氮化硅。
- [0021] 优选地,所述绝缘膜HK的金属层包括钨。
- [0022] 优选地,所述绝缘膜HK为氧化钪膜、氧化锆膜、氧化铝膜、氧化钽膜或者氧化镧膜。
- [0023] 一种三维存储器结构,其由上述任一所述方法制备得到。
- [0024] 一种三维存储器结构,包括:
- [0025] 基底01;
- [0026] 堆叠层,呈阶梯式结构,形成在所述基底01表面,所述堆叠层包括多个交错叠加的第一氧化物层02和包含绝缘膜HK的金属层;
- [0027] 第二氧化物层04,呈阶梯式结构,位于阶梯式结构的堆叠层上;
- [0028] 终止层05,呈阶梯式结构,位于阶梯式结构的第二氧化物层04上;
- [0029] 第三氧化物层06,形成在终止层05上;第三氧化物层06与阶梯式结构的终止层的最高层08齐平;
- [0030] 接触通道,形成在相邻的第三氧化物层06之间,透过第二氧化物层04、绝缘膜HK,达到绝缘膜HK的金属层的接触通道11;
- [0031] 接触开口07,位于阶梯式结构的终止层的最高终止层08上,并穿透各层直至接触基底。
- [0032] 优选地,所述终止层是氮化物。
- [0033] 优选地,所述绝缘膜HK的金属层包括钨。
- [0034] 优选地,所述绝缘膜HK为氧化钪膜、氧化锆膜、氧化铝膜、氧化钽膜或者氧化镧膜。
- [0035] 本发明的优点或有益效果在于:通过本发明提供的上述工艺,将原来的一步刻蚀变为两步刻蚀,利用的是刻蚀停止层的设置,原理是利用的停止层对于不同的刻蚀剂有不同的刻蚀效果来实现,避免了现有技术中采用一层光罩进行刻蚀的过程中产生的刻蚀不足或过刻蚀的情况,采用这种新的工艺可以节省成本,降低工艺复杂度,扩大工艺窗口。

附图说明

[0036] 通过阅读下文优选实施方式的详细描述,各种其他的优点和益处对于本领域普通技术人员将变得清楚明了。附图仅用于示出优选实施方式的目的,而并不认为是对本发明的限制。而且在整个附图中,用相同的参考符号表示相同的部件。在附图中:

[0037] 图1示出了本发明背景技术中采用三层光罩工艺获得的三维半岛器存储器结构;

[0038] 图2示出了本发明背景技术中采用一层光罩工艺获得的具有缺陷的三维半岛器存储器结构;

[0039] 图3-10示出了本发明实施例的用于三维存储器的结构制备工艺流程结构示意图。

具体实施方式

[0040] 下面将参照附图更详细地描述本公开的示例性实施方式。虽然附图中显示了本公开的示例性实施方式,然而应当理解,可以以各种形式实现本公开而不应被这里阐述的实施方式所限制。相反,提供这些实施方式是为了能够更透彻地理解本公开,并且能够将本公开的范围完整的传达给本领域的技术人员。

[0041] 参考图3-10所示,本发明实施例提供一种三维存储器的结构制备工艺,包括以下步骤:

[0042] 一种三维存储器结构制备方法,包括:

[0043] 第一步,阶梯式结构刻蚀:

[0044] 提供基底01;

[0045] 在所述基底01表面形成堆叠层,所述堆叠层包括多个交错叠加的第一氧化物层02和氮化硅层03;

[0046] 然后对堆叠层进行刻蚀,形成阶梯式结构的堆叠层;

[0047] 第二步,在阶梯式结构的堆叠层上形成阶梯式结构的第二氧化物层04:

[0048] 第三步,在阶梯式结构的第二氧化物层04上形成阶梯式结构的终止层05;

[0049] 第四步,在阶梯式结构的终止层上进行填充,形成与阶梯式结构的终止层的最高层等高的第三氧化物层06,第三氧化物层06形成后,采用化学机械抛光(CMP)工艺使得各台阶层的第三氧化物层06的高度与阶梯式结构的终止层的最高层齐平;

[0050] 第五步,蚀刻阶梯式结构的终止层的最高终止层08,形成穿透各层直至接触基底的接触开口07,然后将氮化硅层03取代为包含绝缘膜HK的金属层;

[0051] 绝缘膜HK是具有比氧化物和氮化硅中的每一个更高的介电常数(电容率)的绝缘材料的膜、即所谓高k膜(高介电常数膜)。在本申请中,高k膜或者高介电常数膜是指具有高于氮化硅的介电常数(电容率)的膜。

[0052] 可以使用金属氧化物膜作为绝缘膜HK,金属氧化物膜比如氧化钪膜、氧化锆膜、氧化铝膜、氧化钽膜或者氧化镧膜。这样的金属氧化物膜还可以包含氮(N)和硅(Si)中的一个或者二者。可以例如通过原子层沉积(ALD)工艺形成绝缘膜HK。绝缘膜HK具有例如3nm的厚度。在高介电常数膜(这里为绝缘膜HK)用作栅极绝缘膜时,与使用氧化物膜的情况比较可以增加栅极绝缘膜的物理厚度;因此,可以减少漏电流。

[0053] 第六步,刻蚀第三氧化物层06,进行高选择比的刻蚀,形成达到各阶梯式结构的终

止层的接触通道09;

[0054] 第七步,利用反向选择比的刻蚀,进一步刻蚀接触通道,透过各阶梯式结构终止层05,得到达到第二氧化物层04接触通道;

[0055] 第八步,进一步刻蚀接触通道,透过第二氧化物层04、绝缘膜HK,得到达到绝缘膜HK的金属层的接触通道11;

[0056] 第九步,金属填充和研磨的步骤,即在前述的步骤中通过刻蚀实现了通孔之后,通过金属填充和研磨等方式实现金属连接结构。

[0057] 本发明提供一种三维存储器结构,其由前述制备方法制备得到。

[0058] 优选,所述终止层是氮化硅。

[0059] 优选,所述绝缘膜HK为氧化铅膜、氧化锆膜、氧化铝膜、氧化钽膜或者氧化镧膜。

[0060] 一种三维存储器结构,包括:

[0061] 基底01;

[0062] 堆叠层,呈阶梯式结构,形成在所述基底01表面,所述堆叠层包括多个交错叠加的第一氧化物层02和包含绝缘膜HK的金属层;

[0063] 第二氧化物层04,呈阶梯式结构,位于阶梯式结构的堆叠层上;

[0064] 终止层05,呈阶梯式结构,位于阶梯式结构的第二氧化物层04上;

[0065] 第三氧化物层06,形成在终止层05上;第三氧化物层06与阶梯式结构的终止层的最高层08齐平;

[0066] 接触通道,形成在相邻的第三氧化物层06之间,透过第二氧化物层04、绝缘膜HK,达到绝缘膜HK的金属层的接触通道11;

[0067] 接触开口07,位于阶梯式结构的终止层的最高终止层08上,并穿透各层直至接触基底。

[0068] 优选,所述终止层是氮化硅。

[0069] 优选,所述绝缘膜HK为氧化铅膜、氧化锆膜、氧化铝膜、氧化钽膜或者氧化镧膜。

[0070] 以上所述,仅为本发明较佳的具体实施方式,但本发明的保护范围并不局限于此,任何熟悉本技术领域的技术人员在本发明揭露的技术范围内,可轻易想到的变化或替换,都应涵盖在本发明的保护范围之内。因此,本发明的保护范围应以所述权利要求的保护范围为准。

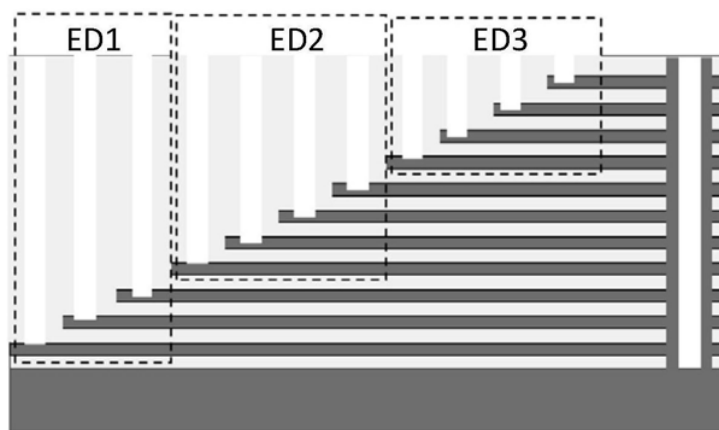


图1

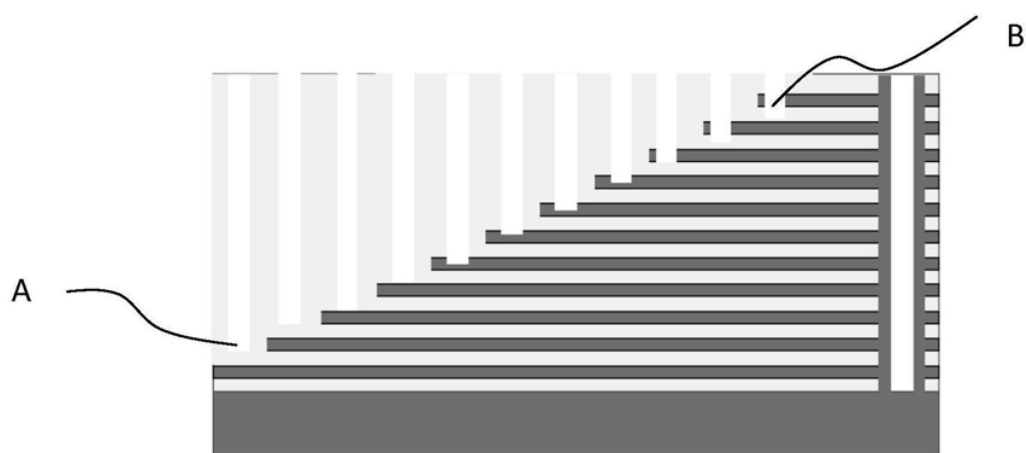


图2

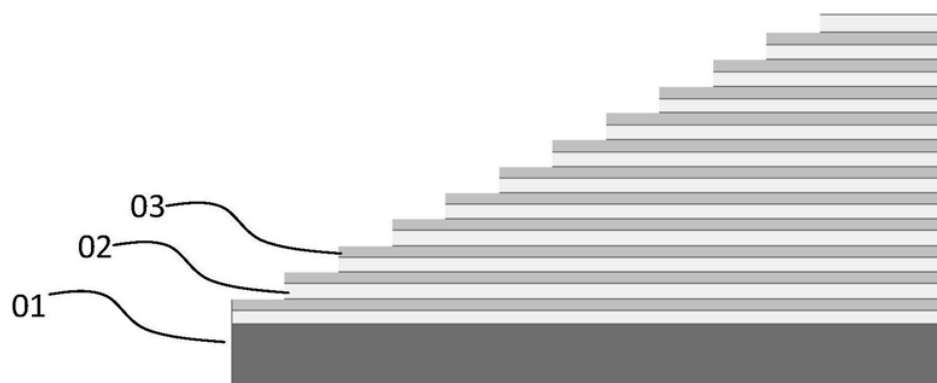


图3

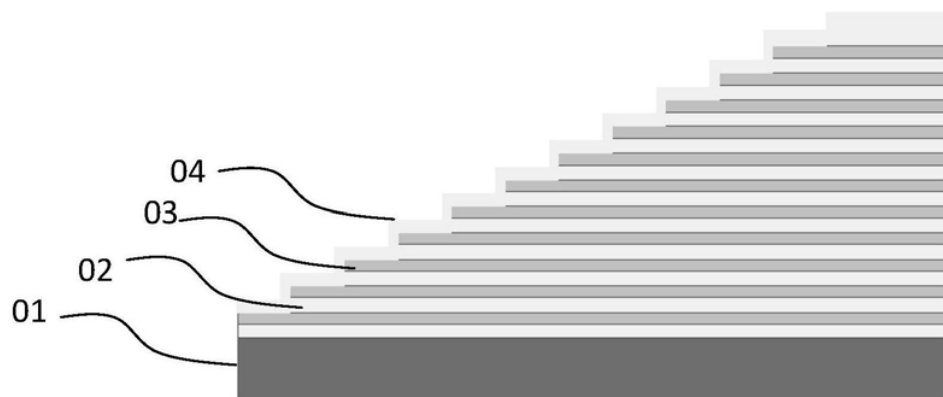


图4

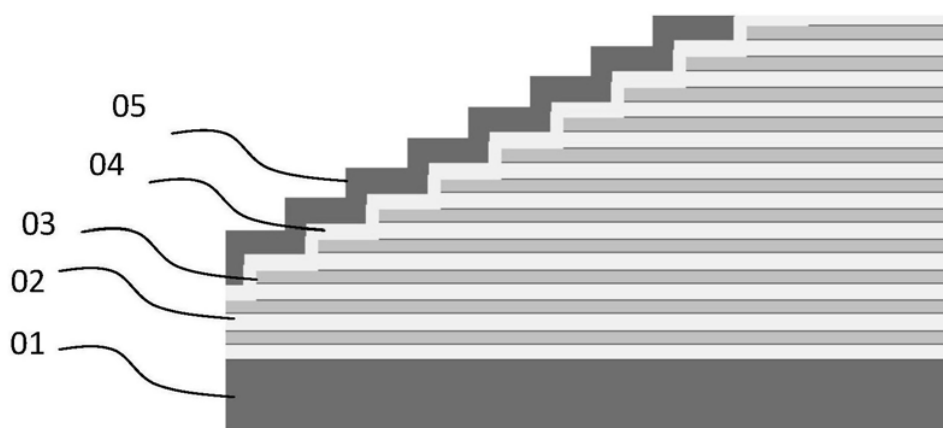


图5

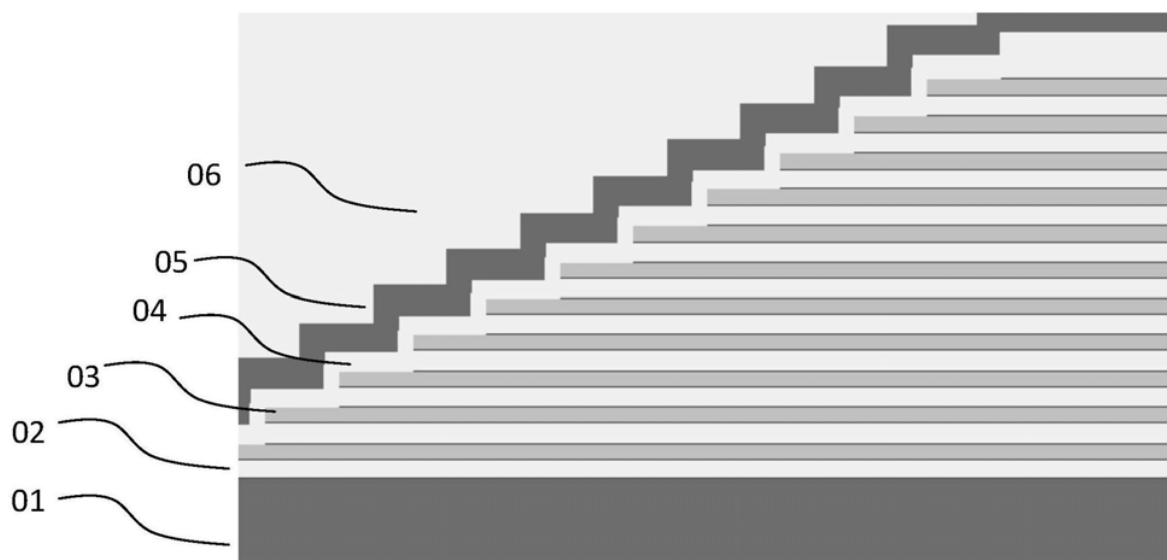


图6

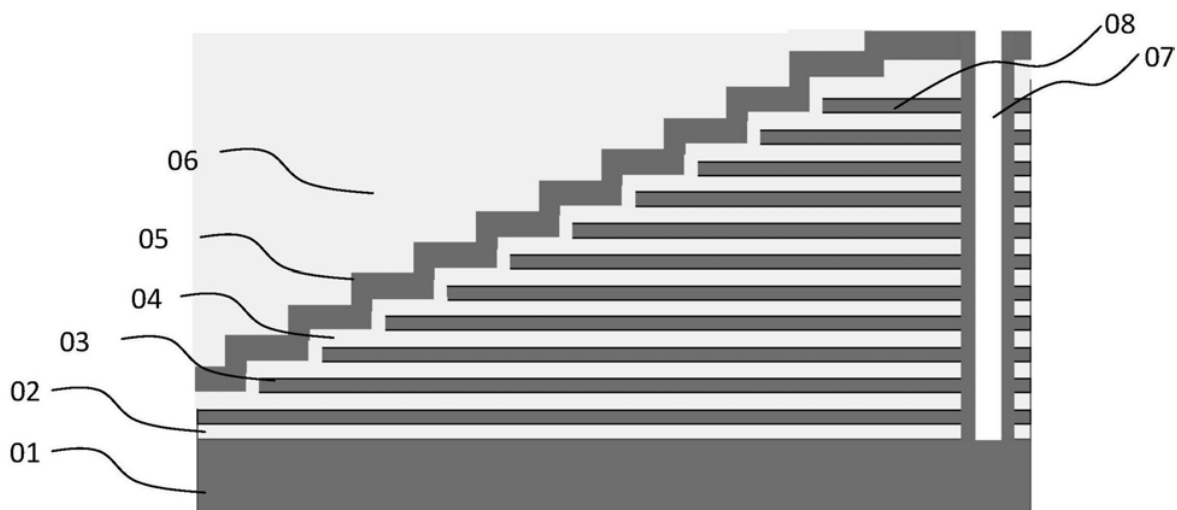


图7

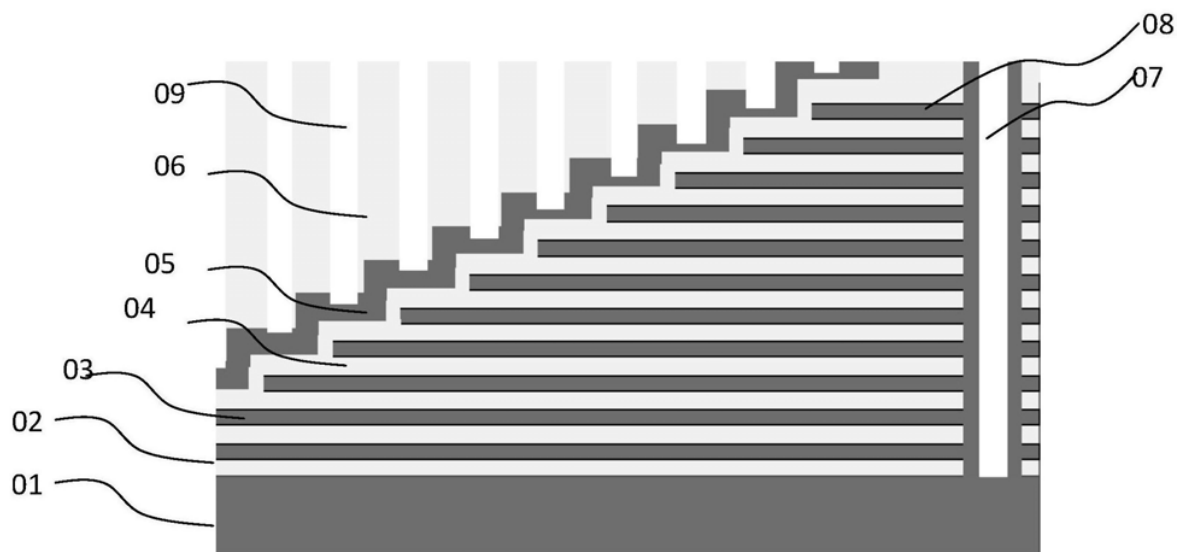


图8

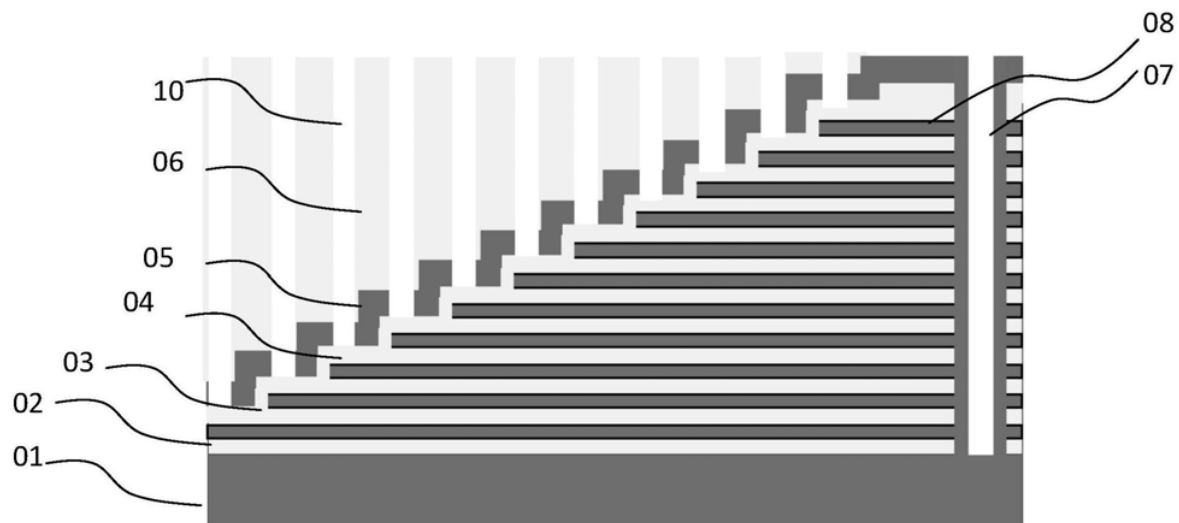


图9

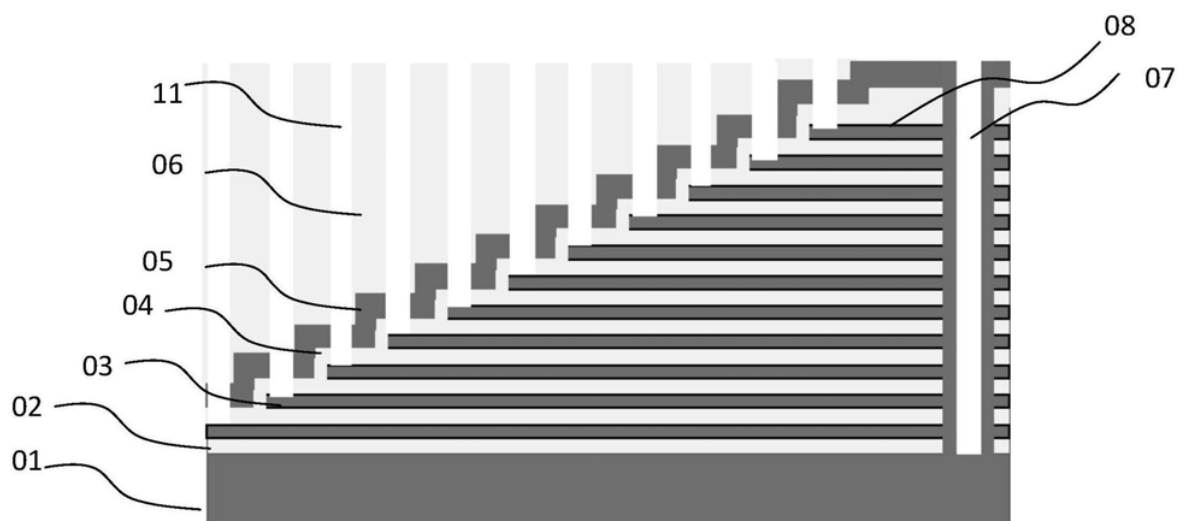


图10