

Low DC-bias silicon nitride anisotropic etching

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This paper presents an effective approach for silicon nitride plasma dry etching, with low DC-bias (self-bias) and vertical sidewalls. Four factors were studied: capacitively coupled radio frequency power, inductively coupled plasma power, pressure in the etching chamber, and the combination of etching gases. By meticulously controlling these factors, the authors successfully achieved low DC-bias silicon nitride anisotropic etching without argon bombardment, with DC-bias of only 34 V and etching rate of 40 nm/min. Our new etching recipe can avoid short-circuits effectively when patterning sub-50 nm thick silicon nitride layer as a dielectric layer between two metal layers. Moreover, “beaklike” structures, which were formed during the etching process due to increasing etching DC-bias at the beginning of the etching process, were discovered, understood, and prevented. © 2015 American Vacuum Society. [<http://dx.doi.org/10.1116/1.4930298>]

I. INTRODUCTION

Silicon nitride is one of the most important materials in micro/nanofabrication and applications, including diffusion barriers, etching mask material, electric insulators, etc. It has not only very excellent chemical inertia but also very high electrical resistivity. Particularly, metal–insulator–metal (MIM) sandwiched-like structures with silicon nitride as a dielectric layer have drawn a great number of attention because of their numerous applications in MEMS switches,¹ optical devices (e.g., metamaterials²), biochemical sensing,³ and nanoelectronics.

However, it is hard to pattern silicon nitride by common reactive ion etch (RIE) without causing short-circuit between the two metal layers^{4,5} in MIM sandwiched-like structures due to metal sputtered out and redeposited onto the sidewall. Commonly used RIE methods usually take advantages of high DC-bias (self-bias) voltage to achieve perfect anisotropic etching profile. However, as shown in Fig. 1, high-energy ions will bombard the top and bottom metal layers during etching process when DC-bias is high, resulting in metal atoms sputtered out everywhere and then redeposited back onto the substrate.^{6–8} In some cases, especially when the silicon nitride layer is very thin, those metal atoms will be unfortunately redeposited onto the sidewall of silicon nitride and form an electrical current path, in other words, short-circuit between two metal layers. Chromium is one of the most widely used materials as metal etching mask. However, theoretical analysis⁹ indicates that the sputtering yield of chromium will be up to 0.3 atoms/ion under bombardment of only 100 eV Argon⁺ ions. Moreover, most other metals have even higher sputtering yield. That is to say, it is very easy to sputter the metal atoms out to get short-circuit during common RIE process. Wet etching of silicon nitride by hot phosphoric acid would not have such problems;

however, it is isotropic and could not be utilized in some cases when vertical sidewalls are desired.

Although researchers have come up with many approaches to try to reduce the sputtering/redeposition during etching processes, such as modified gas combination,^{10,11} geometry and material optimization,^{8,12} and pressure modulation,¹³ there is no report yet applicable for particular etching methods for MIM sandwiched-like structures, especially when dielectric layer is very thin and low DC-bias is

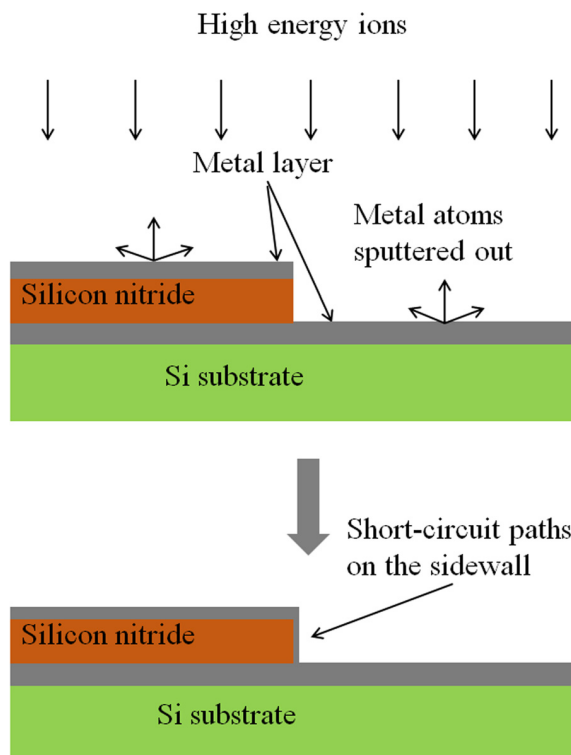


FIG. 1. (Color online) Metal atoms sputtered out and redeposited at high DC-bias etching, leading to short-circuit between two metal layers.

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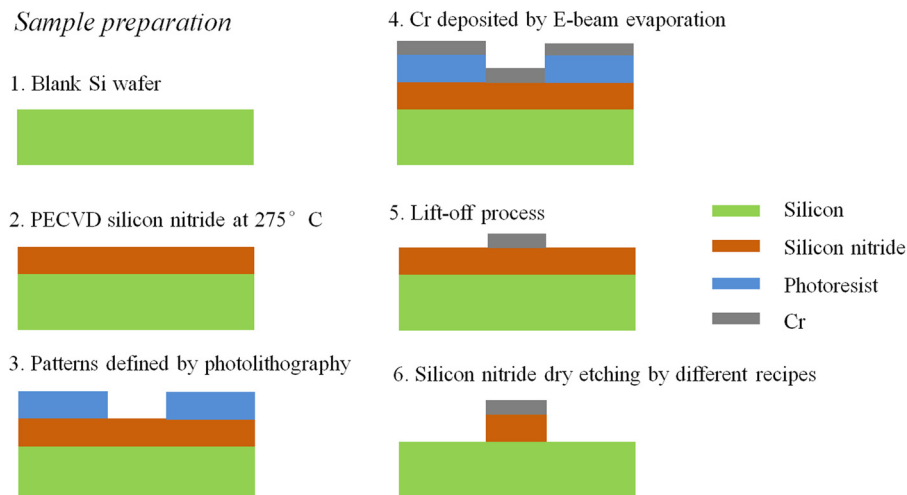


FIG. 2. (Color online) Schematic diagram of sample fabrication processes for etching recipe test.

necessary. Here, we studied four factors that can affect the DC-bias and etching profile significantly: capacitively coupled RF power, inductively coupled plasma (ICP) power, the pressure in the etching chamber, and the combination of etching gases. Finally, we developed an optimal etching recipe for silicon nitride with only SF_6 and C_4F_8 as etching gases. The DC-bias was lowered to only 34 V, and the sidewall is nearly vertical, with etching rate of 40 nm/min. Further study also showed that this recipe could avoid short-circuit between two metal layers effectively.

II. SAMPLE PREPARATION

The samples used to test silicon nitride etching recipes were fabricated by common semiconductor processes. As shown in Fig. 2, first, 400 nm silicon nitride (SiN_x) was deposited onto silicon wafers by plasma-enhanced chemical vapor deposition at 275 °C. Then, photolithography, e-beam evaporation, and lift-off processes were used to define 30 nm thick chromium gratings on top of the deposited SiN_x film, which were used as etching mask to test etching profiles. Figure 3 shows a piece of sample prepared for etching recipe test.

III. ETCHING TEST AND ANALYSIS

In general, both physical etching and chemical etching are exploited during dry etching processes, to keep balance between vertical profile and high selectivity. In experiments, we used only SF_6 and C_4F_8 (and sometimes O_2) as etching gases. SF_6 was mainly used to generate F and SF_x free radicals to etch SiN_x , while C_4F_8 was the source of carbon-based passivation layer to protect the sidewall from etching (sometimes, O_2 was used to adjust the C/F ratio slightly). In order to reduce the physical bombardment etching, and hence the sputtering of metal layer, we did not use argon as etching gas.

Two key points of etching recipes were investigated: first is the DC-bias, which should be low enough to reduce the sputtering yield; second is the etching profile, which should

have vertical sidewalls as desired. There is a trade-off between those two, because it is difficult to generate vertical sidewalls with low DC-bias, in which physical bombardment is very weak; therefore, isotropic chemical etching is dominant. One thing needs to be clarified: due to the collisions and scatterings of the ions from gas molecules (and ions) in the chamber, the kinetic energy of the bombardment ions is not necessarily the same as the DC-bias times the charge. But the kinetic energy is not directly measurable in contrary to the DC-bias, and DC-bias and the bombardment energy are closely correlated, so we studied the DC-bias instead. By carefully controlling the parameters of etching recipes, passivation and etching will be in dynamic equilibrium at the sidewalls, and therefore, vertical sidewalls can be achieved even when DC-bias is very low.

Four factors were studied: capacitively coupled RF power, ICP power, pressure in the etching chamber, and combination of etching gases. Each of them will affect the DC-bias and the etching profile significantly; even sometimes, the effects are coupled and not simply monotonous.

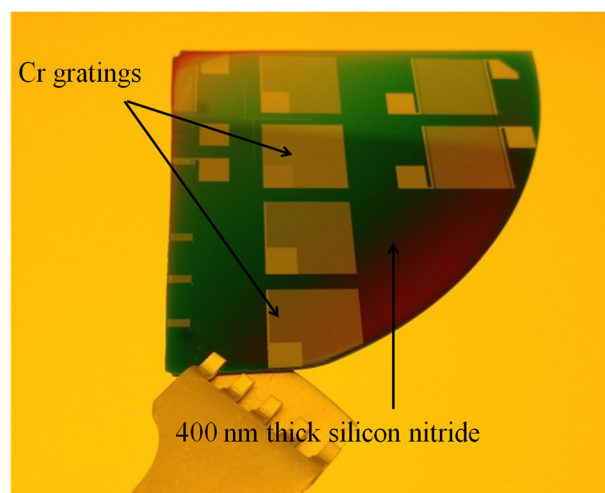


FIG. 3. (Color online) Piece of sample prepared for etching recipe test, with 400 nm silicon nitride and Cr grating patterns on it.

Here, we tried different etching recipes with the same etching time of 5 min, and observed the DC-bias variation and the final etching profiles. The original silicon nitride layer was 400 nm, and the RIE etcher was Oxford Plasmalab system 100.

A. Capacitively coupled RF power

Figure 4 shows the relationship between DC-bias and capacitively coupled RF power (or “RF power” abbreviated in this paper). When RF power increases, DC-bias increases monotonically. However, there is a striking RF power below which the DC-bias keeps at zero. At this striking threshold, DC-bias is not stable and could be either very high or zero. However, once the DC-bias has been activated, it is maintained easily. When the pressure is low enough, it is easier for striking because the mean-free-path gets larger so electrons can accumulate enough energy to excite the gas molecules. And also, when ICP power is higher, the striking RF power needed is smaller because ICP power increases the plasma density.

Moreover, we discovered that it is difficult to find low DC-bias recipe at high pressure. Experiments showed that the minimum DC-bias with struck plasma at high pressure is very large. Figure 4 shows two SEM images at relatively low DC-bias (15 and 25 V, respectively). The one with lower RF power had lower DC-bias, and correspondingly achieved lower etching rate and more isotropic etching profile due to lower ion energy to remove the passivation layer and enhance the chemical etching rate at the bottom.

B. ICP power

The relationship between DC-bias and ICP power is shown in Fig. 5. The circle line shows that DC-bias first turns on suddenly (the plasma strikes) and then decreases slowly along with ICP power increasing. The turn-on points are when the ionization rate is sufficient to compensate the

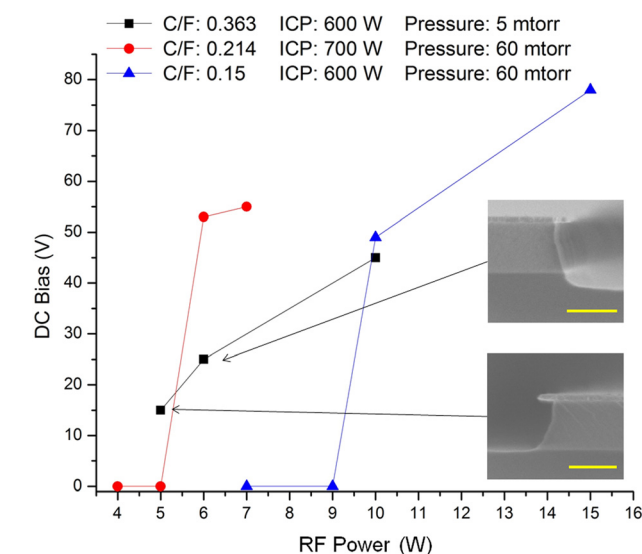


FIG. 4. (Color online) Relationship between DC-bias and capacitively coupled RF power. The scale bar is 400 nm.

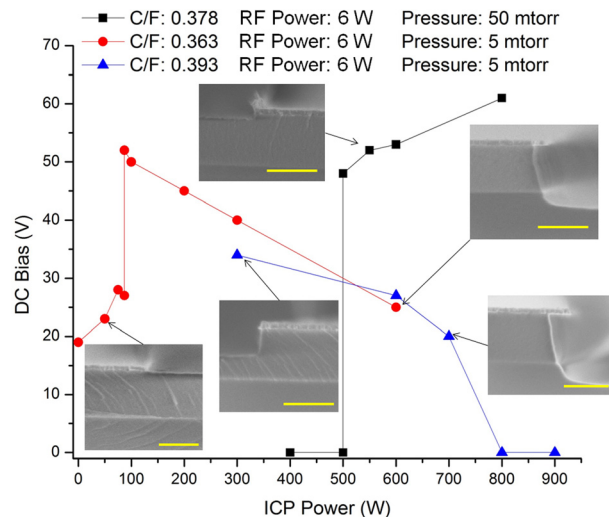


FIG. 5. (Color online) Relationship between DC-bias and ICP power. The scale bar is 400 nm.

electron loss (the triangle line only shows the data after its turn-on point and the square line only shows the data before its turn-on point). The turn-on points increase if the pressure increases, because mean-free-path gets shorter so more power are necessary to generate sufficient ionization rate. After the turn-on points, increasing ICP power results in larger plasma density, so the ion flow current toward the substrate increases. At fixed RF power, the product of ion flow current and bias voltage between two capacitive plates is conserved, therefore larger ICP power will lead to lower DC-bias.

Two SEM images from the circle line and the square line in Fig. 5 show nonetching results when the values of the ICP power are smaller than the turning points. The etching rate is almost zero even at high DC-bias because the plasma density is insufficient to generate enough radicals and to etch efficiently. Comparison within three SEM images from the triangle line indicates that ICP power affects the etching rate significantly: larger ICP power leads to faster etching. However, larger ICP power may not be a good choice even it will decrease the DC-bias, because lateral etching will also become faster so that the profile will become even more isotropic.

C. Pressure

The relationship between DC-bias and the pressure in the chamber is shown in Fig. 6. At low pressure, DC-bias increases as the pressure increases, which may result from increasing amount of charged particles (ions and electrons). However, we also discovered that at high pressure, DC-bias decreases as the pressure increases due to shorter mean-free-path. We also found that at very high pressure, the etching rate is much slower, which results from insufficient kinetic energy of the ions at high pressure with the fixed RF power and ICP power. When the pressure is too high (e.g., 50 mTorr), in fact, the plasma is difficult to be struck and the DC-bias keeps zero when RF power is relatively low. People¹³ have discovered that, low pressure can avoid

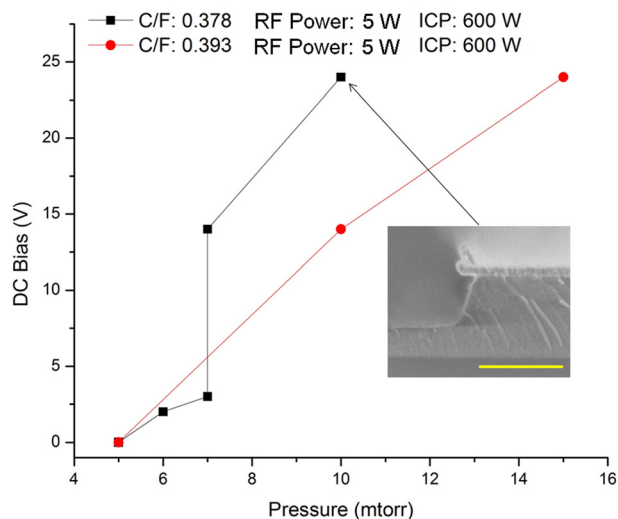


FIG. 6. (Color online) Relationship between DC-bias and the pressure in the chamber. The scale bar is 400 nm.

etching product substrate redeposition and also may reduce the negative taper angle for trench etching. Therefore, here low pressure is our primary selection for low DC-bias etching.

D. Etching gas combinations

When the total flow rate is constant and the pressure is low, DC-bias decreases as C-to-F ratio increases, as shown in Fig. 7. That may be because carbon atoms are easier to be ionized than fluorine atoms;¹⁴ therefore, the gas in the chamber is more conductive with increasing C-to-F ratio. Another reason may be the electronic attachment of fluorine plasma, in which F ions tend to catch electrons to form F^- ions. This leads to less free electron density between the capacitive plates then higher DC-bias voltage. While at high pressure, the DC-bias can either increase or decrease along with the increasing C-to-F ratio, depending on different recipes. The C-to-F ratio only plays a big role on the etching profile, coupled with the effect by DC-bias.

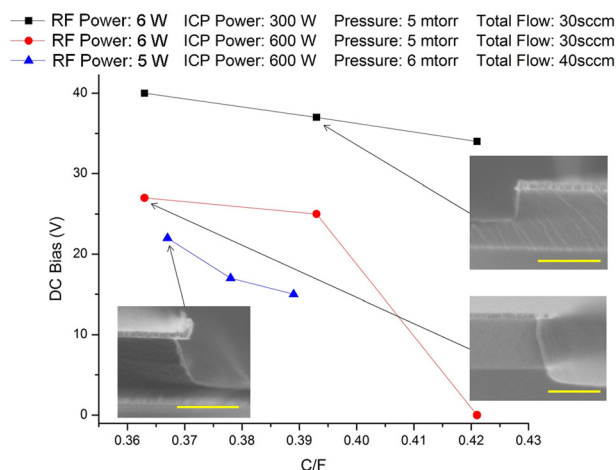


FIG. 7. (Color online) Relationship between DC-bias and etching gas combinations. The scale bar is 400 nm.

E. Beaklike structures

In experiments, we discovered interesting beaklike structures formed at the top edge of silicon nitride at certain conditions, as shown in Fig. 8(b). This is because the RF matching network tuning period sometimes can last up to several tens of seconds. During that time, the etching is mainly isotropic chemical etching because the reflected power is very high so the DC-bias is very low. When the tuning network gets matched, the DC-bias increases very fast to its stable value, after which there is more physical bombardment due to large DC-bias, and the etching profile goes back to normal. Figure 8(a) shows a typical DC-bias matching period versus time.

The beaklike structures only occur when it takes long time to tune the RF matching network. These initial striking periods are related to the etching recipes, and generally higher RF power, lower pressure, and higher final stable DC-bias give shorter initial striking periods. We also discovered that more conductive substrates will reduce the initial striking periods significantly.

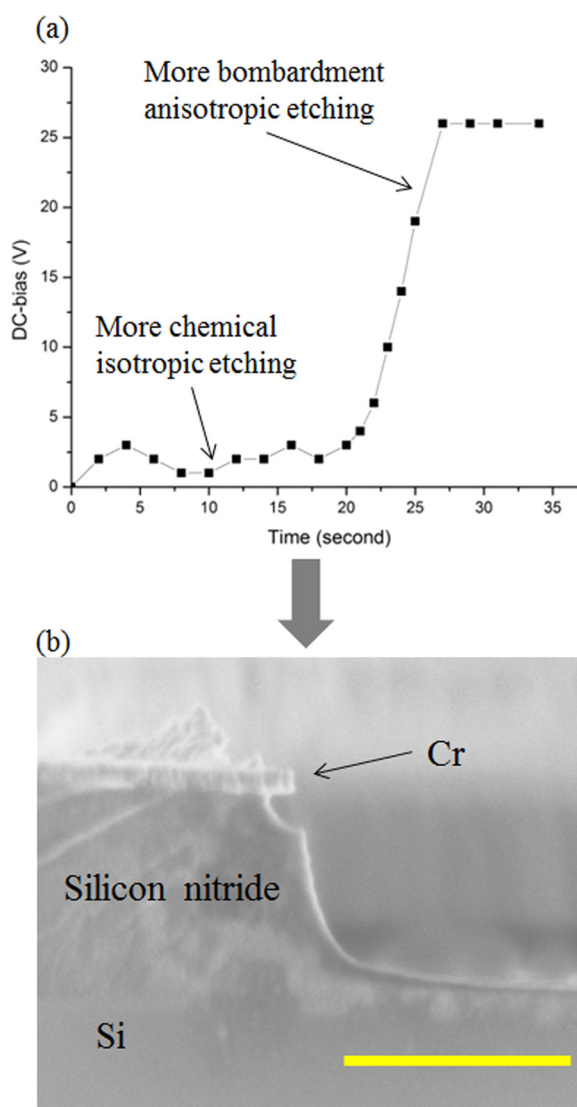


FIG. 8. (Color online) (a) Typical DC-bias matching period vs time. (b) SEM image of a beaklike structure. The scale bar is 500 nm.

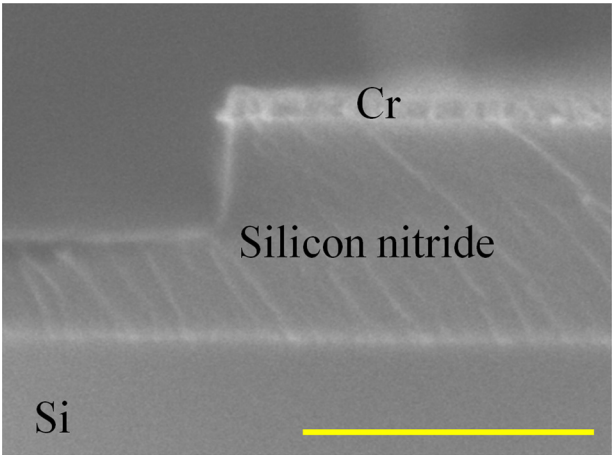


FIG. 9. (Color online) Low DC-bias silicon nitride anisotropic etching based on our optimal recipe. The scale bar is 500 nm.

IV. OPTIMAL ETCHING RECIPE

By meticulously controlling the parameters of etching recipes, we eventually found a recipe with DC-bias of only 34 V and nearly 90° sidewall, as shown in Fig. 9, and the etching rate is 40 nm/min, which is fast enough for etching thin silicon nitride film in nanometer scale. The parameters are shown in Table I. Moreover, further study shows that the selectivity between silicon nitride and chromium based on our optimal recipe is larger than 100:1.

More significantly, our experiments show that this recipe can be used to fabricate MIM sandwiched-like structures without causing short circuit between top and bottom metal layers. The cross section of one of the testing samples is shown in Fig. 10(b), which has two 30 nm thick chromium layers and one 50 nm thick silicon nitride layer in between. The samples were tested under a common silicon nitride dry etching recipe with DC-bias of around 300 V and our optimal recipe with DC-bias of only 34 V for comparison. By measuring the resistances between each top Cr pad electrode and the bottom Cr layer electrode [Fig. 10(a)], we approved that our recipe can avoid short-circuit nearly 100% between two metal layers (resistances out of the range of our multimeter) while the common recipe always leads to short-circuit (smaller than 100 Ω) between almost all the pad electrodes and the bottom metal layer.

TABLE I. Parameters of the optimal recipe for low DC-bias silicon nitride etching.

Etching parameters	Value
SF ₆ (sccm)	8
C ₄ F ₈ (sccm)	22
C/F ratio	0.393
RF power (W)	6
ICP power (W)	300
Pressure (mTorr)	5
DC bias (V)	34
Etching rate (nm/min)	40

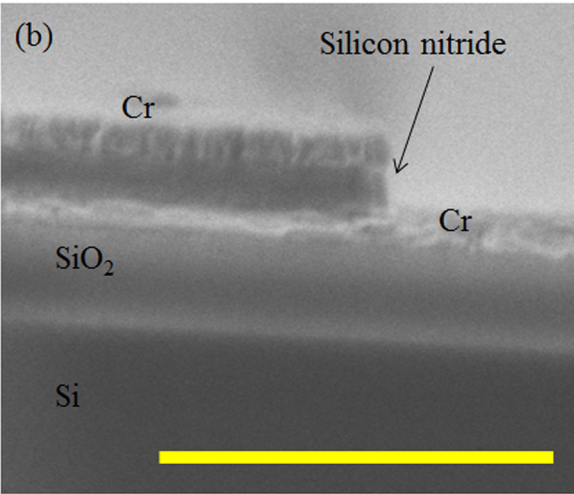
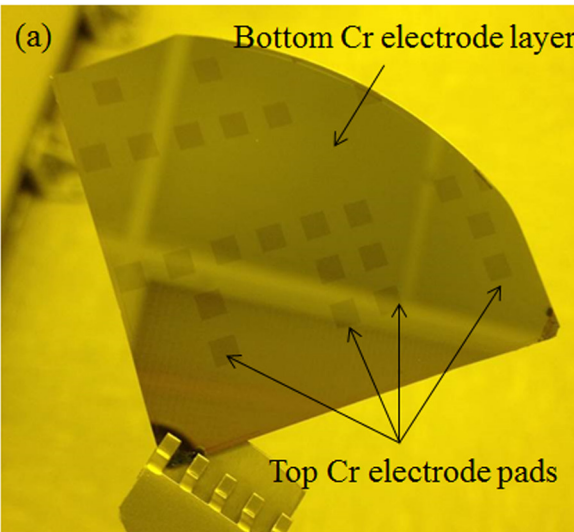


FIG. 10. (Color online) (a) Testing sample with MIM sandwiched-like structures. (b) SEM image of the cross section of a testing sample. The scale bar is 500 nm.

V. SUMMARY AND CONCLUSIONS

In this paper, we provide an optimal recipe for silicon nitride etching, with DC-bias of only 34 V, which prevents short circuits in fabricated MIM structures, and nearly 90° etching sidewalls. The four main factors, capacitively coupled RF power, ICP power, the pressure in the etching chamber, and the combination of etching gases, have been studied to achieve low DC-bias and desired etching profiles. We discovered that the beaklike structures formed on the top edge of silicon nitride layer due to initial striking periods at certain etching conditions, which could be promising functional structures for some applications. The relationships between the four factors and etching results we discussed here can applied not only on silicon nitride, but also many other materials.

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- ¹A. Dogan, "The reliability of the silicon nitride dielectric in capacitive MEMS switches," Ph.D. thesis (PSU, 2005).
- ²W. Wu *et al.*, *Appl. Phys. A* **87**, 143 (2007).
- ³J. Bai *et al.*, *Nanoscale* **6**, 8900 (2014).
- ⁴H. K. Kang *et al.*, *International Electron Devices Meeting on IEDM'94 Technical Digest* (IEEE, San Francisco, CA, 1994).
- ⁵K. H. Rasmussen, "Advanced dry etching studies for micro- and nano-systems," Ph.D. thesis (DTU Nanotech, Kongens Lyngby, 2014).
- ⁶D. Gao, M. B. J. Wijesundara, C. Carraro, R. T. Howe, and R. Maboudian, *IEEE Sens. J.* **4**, 441 (2004).
- ⁷V. Abramova, A. S. Slesarev, and J. M. Tour, *Nano Lett.* **15**, 2933 (2015).
- ⁸H. Hübner, *J. Electrochem. Soc.* **139**, 3302 (1992).
- ⁹N. Laegreid and G. K. Wehner, *J. Appl. Phys.* **32**, 365 (1961).
- ¹⁰D. C. Gray, V. Mohindra, and H. H. Sawin, *J. Vac. Sci. Technol. A* **12**, 354 (1994).
- ¹¹R. M. Ranade, S. S. Ang, and W. D. Brown, *J. Electrochem. Soc.* **140**, 3676 (1993).
- ¹²A. Aydemir and T. Akin, *J. Micromech. Microeng.* **22**, 074004 (2012).
- ¹³W. Chen, K. Sugita, Y. Morikawa, S. Yasunami, T. Hayashi, and T. Uchida, *J. Vac. Sci. Technol. A* **19**, 2936 (2001).
- ¹⁴D. R. Lide, *CRC Handbook of Chemistry and Physics: A Ready-Reference Book of Chemical and Physical Data* (CRC, Boca Raton, FL, 2004).