

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: April 30, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00228
Patent 11,101,276

PATENT OWNER'S PRELIMINARY RESPONSE

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Ex.	Description
2001	Defendants' Preliminary Invalidity Contentions and Document Production Accompanying Invalidity Contentions re YMTC II Asserted Patents (Patent Local Rules 3-3 and 3-4), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Nov. 25, 2024) (excerpts)
2002	Civil Minutes, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Sept. 18, 2024), ECF No. 141
2003	Order Granting Stipulation to Extend Certain Deadlines Pursuant to Patent L.R. 4-2 and the Scheduling Order (ECF No. 141) Pursuant to Civil Local Rule 6-1(b), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Jan. 8, 2025), ECF No. 194
2004	Order Granting Motion to Stay Case Pending <i>Inter Partes</i> Review, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Mar. 14, 2025), ECF No. 243
2005	Plaintiff/Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.'s and Counterclaim Defendant Yangtze Memory Technologies, Inc.'s Opposition to Micron's Motion to Stay Case Pending <i>Inter Partes</i> Review and Post-Grant Proceedings, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Feb. 3, 2025), ECF No. 221
2006	Declaration of Steve Campbell in Support of Patent Owner's Preliminary Response
2007	<i>Curriculum Vitae</i> of Steve Campbell
2008-2017	RESERVED

Ex.	Description
2018	Order Granting Motion to Consolidate, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Aug. 21, 2024), ECF No. 106

I. Introduction

Patent Owner Yangtze Memory Technologies Company, Ltd. (“YMTC” or “Patent Owner”) respectfully submits this Preliminary Response to the Petition for *inter partes* review of U.S. Patent No. 11,101,276 (“’276 Patent”). As explained below, Petitioner fails to carry its burden to show a reasonable likelihood that at least one of the challenged claims is unpatentable. Thus, the Board should deny the Petition, and no IPR proceeding should be instituted.

The ’276 Patent describes and claims an innovative “method for forming a semiconductor structure” including a staircase for a 3D NAND memory. Specifically, the ’276 Patent claims forming staircase structures by disposing an etch-stop layer on each step of the plurality of steps, where formation of each step includes a “disposing sacrificial layer over a dielectric layer.” This specific method allows for a single etching process to form holes of different depths that connect the gate stack with external devices.

The Petition relies on embodiments from two primary references, Kim (Ex.1005) (Grounds 1-2) and Han (Ex.1007) (Grounds 3-4). The Petition acknowledges that Kim discloses a gate stack *under* a dielectric layer. Pet. 27. But the Challenged Claims all require the *opposite* configuration by disposing a “sacrificial layer over a dielectric layer.” Pet. 27. Petitioner resorts to redrawing the figures of Kim to support its arguments.

As explained below, Petitioner has failed to provide any reason a POSITA would have been motivated to make such modifications by combining disparate embodiments in Kim. *In re Stepan Co.*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017) (“combining multiple embodiments from a single reference” requires “a motivation to make the combination”). Petitioner identifies no flaw or problem these modifications would address. Nor does Petitioner identify any benefit that would result from the proposed modifications. And Petitioner does not explain why a POSITA would have had a reasonable expectation of success in making these extensive changes, which would involve conductive gate electrodes becoming non-conductive insulators and vice versa.

Petitioner's Han grounds fare no better. Petitioner acknowledges that Han's staircase structure does not include any etch stop layer. Using hindsight, Petitioner cherry-picks an etch stop layer from Fang (Ex. 1006), and asserts—with no explanation or support—that adding Fang's etch stop layer to Han would address undisclosed problems in Han. Petitioner's lack of support for its motivation to combine shows that Grounds 3-4 are based entirely on hindsight and do not establish a reasonable likelihood of prevailing.

The Board should deny the Petition.

II. Background

A. 3D NAND Memories

3D NAND memory devices are “memory arrays” with memory cells stacked one on top of the other. Memory cells can be written or read by applying a voltage to corresponding conductors that run horizontally across the memory array, called “wordlines.”

An exemplary 3D NAND memory is shown in Figure 5.20 of Petitioner's Exhibit 1012, which depicts a series of vertically stacked memory cells, each controlled by a “Control Gate” (the wordline) shown in red as “CG0” through “CG3.” Ex.1012, 134. In other words, the wordlines serve as the gates of the transistors comprising the memory stack.

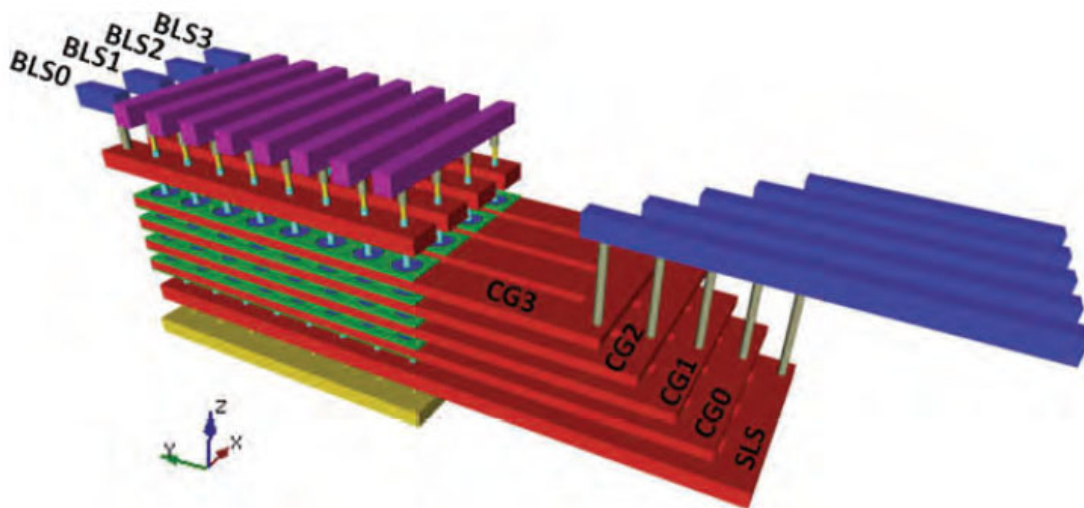


Fig. 5.20 C-FG NAND Flash array with fan-out

The word lines (CG0, CG1, CG2, and CG3) need to be accessed externally from the memory device to control the memory. The word lines extend out of one

memory array in a staggered manner as shown above, which is sometimes referred to as a “staircase structure.” With such a “staircase,” the word lines can then be separately accessed through the vertical vias (shown in tan) connected to external conductive lines (shown in blue). Ex.1012, 134.

B. The '276 Patent (Ex. 1001)

The '276 Patent discloses “a word line contact structure for three-dimensional (3D) memory array and methods for forming the same.” Ex.1001 (“'276 Patent”) 1:40-42; Ex. 2006 (“Campbell”) ¶¶23-25.

To meet the demand for higher storage capacity in 3D NAND memories, manufacturers have tried to increase the number of conductor/dielectric layer pairs in 3D memory devices. '276 Patent 5:42-46. The added layers, however, create challenges in etching holes of differing depths above the staircase structure to create the vertical word line contacts. *Id.* 5:47-54. As the '276 Patent recognizes, “contact holes for lower levels may be deeper than contact holes for upper levels.” *Id.* According to the '276 Patent, “[t]ypically, all of the contact holes are formed with a single lithography mask and etching process.” *Id.* 5:54-55. But “[o]ften, before contact holes to the bottom levels are entirely formed, the materials exposed in contact holes at the upper levels are over-etched and lost.” *Id.* 5:55-58.

The '276 Patent solves the problems of the prior art by disclosing an etch stop layer over the staircase structure, which protects underlying staircase structure

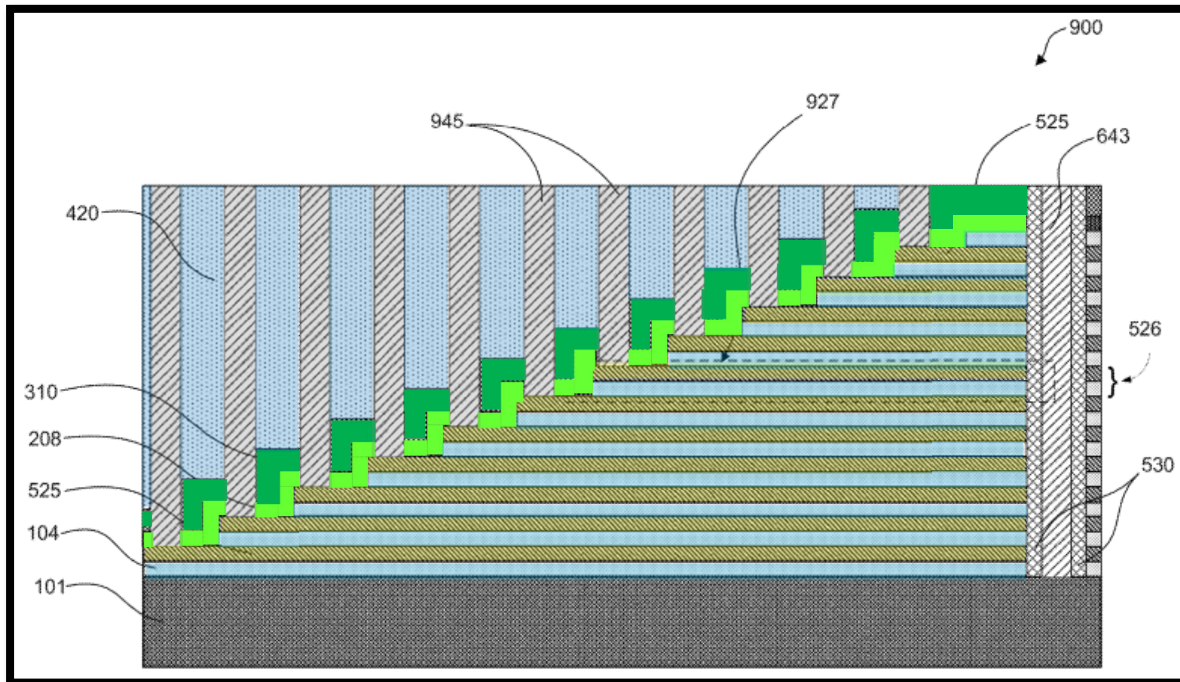
layers during the etching process. '276 Patent 5:61-6:5. This improves fabrication yield and reduces cost. *Id.* 6:5-7.¹ A barrier layer can also be introduced over the staircase structure “for protecting the underlying structure during subsequent etching processes.” *Id.* 7:35-45; Campbell ¶26. To implement these structures, the steps of the staircase are arranged so that the gate stacks of the wordlines are disposed over corresponding dielectric layers. '276 Patent 6:11-12, 8:60-61, 10:34-38.

Below is an annotated version of Figure 9A, showing an exemplary '276 Patent 3D memory device staircase structure. The staircase structure 900 includes alternating layers of gate stacks 525 (yellow) over insulating layers 104 (lighter blue). '276 Patent 6:11-12, 8:60-61, 10:34-38. A second insulating layer 208 (bright green) is formed on the top and side surfaces of each step and an etch-stop layer 310 (dark green) is formed on the second insulating layer. *Id.* 7:36-45, 7:62-64, 8:5-6. A third insulating layer 420 (dark blue) is on the staircase structure 900. *Id.* 8:26-30. Vertical interconnect access (“VIA”) structures 945 (hatched grey) are

¹ The patented solution also allows the formation of semiconductor interconnect structures for inter-connecting components at different layers with an uneven topology. *Id.* 6:7-10; Campbell ¶27.

formed in VIA openings 840 in the third insulating layer 420. *Id.* 11:17-22;

Campbell ¶28.



No.	Structure
525	Gate Stack
104	First Insulating Layer
208	Second Insulating Layer
310	Etch-Stop Layer
420	Third Insulating Layer
945	Vertical Interconnect Access Conductive Structures

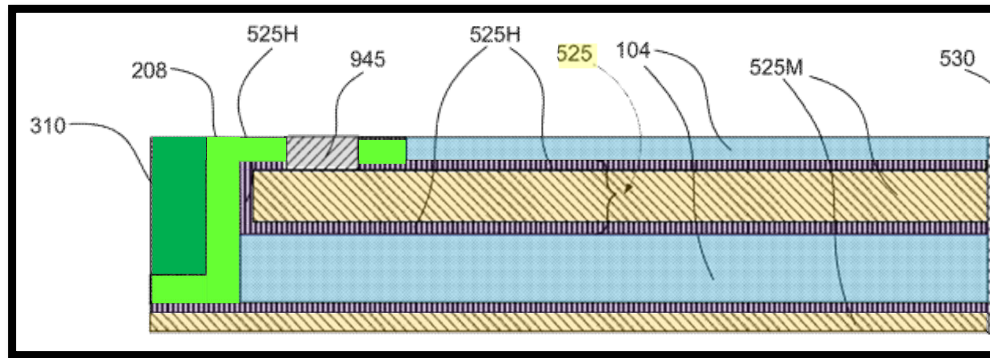
'276 Patent Fig. 9A (annotated) and color key; Campbell ¶28.

Figure 9B shows details of the gate stack 525 of Figure 9A above. The gate stack includes a high-k dielectric layer 525H (purple), which surrounds a gate conductive layer 525M (orange) with one side next to fifth insulating layer 530.

'276 Patent 9:4-10, 9:47-50. The VIA conductive structures 945 (hatched grey)

may be directly disposed on an exposed portion of gate conductive layer 525M.

Id. 11:19-25; Campbell ¶33.



No.	Structure
104	First Insulating Layer
525H	High-k Dielectric Layer
525M	Gate Conductive Layer
208	Second Insulating Layer
310	Etch-Stop Layer
945	Vertical Interconnect Access Conductive Structures

'276 Patent Fig. 9B (cropped and annotated) and color key; Campbell ¶33.

C. Person of Ordinary Skill in the Art

For purposes of this Preliminary Response, YMTC does not dispute Petitioner's proposed level of a person of ordinary skill in the art ("POSITA").²

² YMTC reserves the right to argue an alternative level of a POSITA in other proceedings or if the Board institutes review.

Pet. 26. Regardless of the precise definition of a POSITA, Petitioner's grounds do not render any challenged claims unpatentable. Campbell ¶22.

D. Claim Construction

Petitioner asserts that the terms of the '276 Patent's claims have their plain and ordinary meaning. Pet. 25. For purposes of this Preliminary Response, YMTC agrees because Petitioner fails to show that any Ground has a reasonable likelihood of prevailing under any reasonable construction, including their plain meaning.³

III. Ground 1: Petitioner Fails to Meet Its Burden to Establish Kim in View of a POSITA's Knowledge Renders Obvious Claims 1-2, 4-5, and 9-18

All Challenged Claims require “forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer” and “a plurality of steps” where “the forming of each step... comprises disposing a sacrificial layer over a dielectric layer.” As discussed below, Kim fails to disclose or render obvious these limitations.

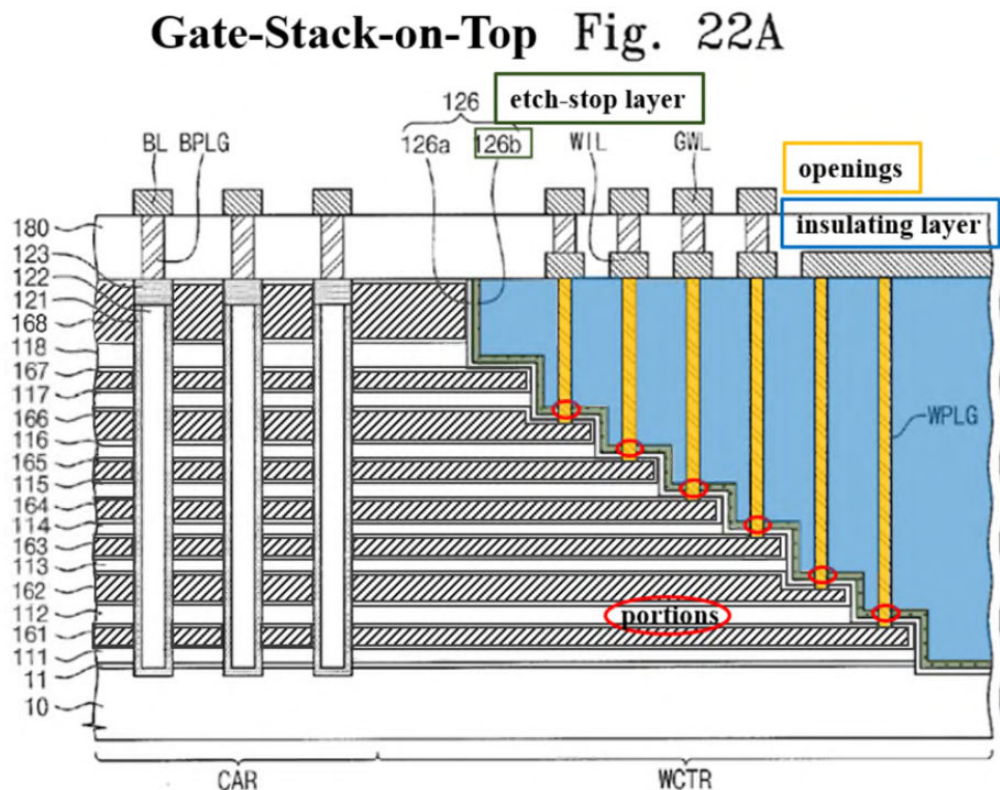
A. Kim Does Not Disclose “forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer”

Petitioner asserts that “Kim discloses” this limitation. Pet. 45. Specifically, Petitioner cites Kim's formation of word line contact plugs WPLG and asserts that

³ YMTC reserves the right to argue alternative constructions in other proceedings or if the Board institutes review.

“Kim’s opening formation comprises a step where etching penetrates the insulating layer exposing—but not penetrating—portions of the etch-stop layer.” Pet. 46.

Petitioner is wrong. Kim does not disclose any method step in forming the word line contact plugs WPLG where “portions of the etch-stop layer” are exposed but not penetrated. Tellingly, Petitioner acknowledges that Kim’s openings *do* penetrate the etch-stop layer rather than exposing a portion of it. For example, Petitioner provides an annotated “Gate-on-Stack” manipulation of Figure 22A, including annotations for what Petitioner calls “openings” (orange) that clearly penetrate, rather than expose, the etch-stop layer 126, as shown by the red circles.



Pet. 46 (annotating Kim Fig. 22A)

Petitioner asserts, however, that these openings are formed in a two-step process: one “step where etching penetrates the insulating layer exposing—but not penetrating—portions of the etch-stop layer” (Pet. 46) and a second step where the “etching must continue by penetrating the etch-stop layer” (Pet. 48).

Kim, however, does ***not*** disclose such two-step contact hole formation for the word line contact plugs. To the contrary, the very passage of Kim that Petitioner cites for support merely discloses forming contact holes. Kim [0173] (“[F]ormation of word line contact plugs WPLG... may include forming contact holes to penetrate the interlayer insulating pattern 134 in the word line contact region WCTR.”); *see* Pet. 46. As a result of this hole formation, the holes ***penetrate***, rather than merely expose, the etch-stop layer so that “the word line contact plugs WPLG can be connected to the gate electrodes” which are below the etch stop layer. Kim [0173]; Campbell ¶¶35-37.

Petitioner acknowledges that Kim does not explicitly disclose a two-step etching for the contact holes, and instead asserts that “[a] POSITA would have recognized” the need for an extra step in contact hole formation due to Kim’s disclosure that the etch stop layer “may be formed of a material having an etch selectivity with respect to the interlayer dielectric 130.” Pet. 46-47 (quoting Kim [0213]). Not so. To the contrary, a POSITA would have understood from this passage that Kim explicitly discloses a two-step etching process when it was

intended. Kim's disclosure of "etch selectivity" relates to two-step device planarizing in the cell-array region. Kim [0213] ("[T]he interlayer dielectric 130 may be formed on the etch stop layer 125 and then planarized until a top surface of the etch stop layer 125 is exposed on the cell array region CAR."); Campbell ¶38. This is an entirely different process from forming word line contact plugs, and occurs in an entirely different part of the device from the word line contact plugs. Campbell ¶38. The etch stop layer has etch selectivity with respect to the planarization process (thus forming a stop point for a first step of planarization)—not for contact hole formation for word line contact plugs. Campbell ¶38; *see, e.g.*, Kim [0196] ("[E]tch stop layer 125... may be used as a planarization stopping point."). The "etch selectivity" of the etch-stop layer for the planarization process does not require or imply etch selectivity for hole formation, as selectivity depends on the "etch recipe" and Kim does not teach or suggest using the same "etch recipe" for these two distinct processes. Campbell ¶38; *see* Kim [0132], [0141] (referring to "etch recipe[s] having an etch selectivity").

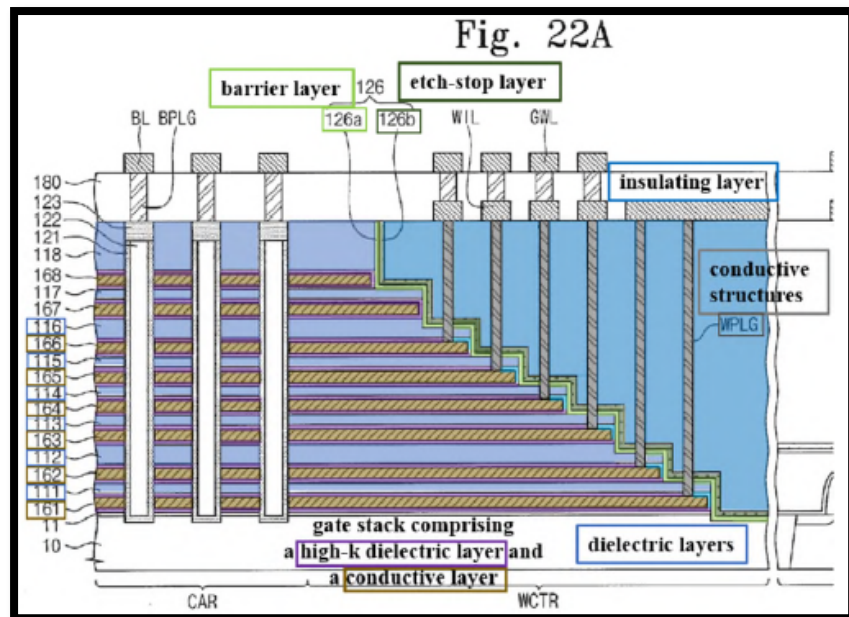
Petitioner uses hindsight to read into Kim an extra step of exposing the etch stop layer during contact hole formation. A POSITA would not have understood this extra step to be implicit or inherent in Kim, and Petitioner does not argue that it is obvious. Campbell ¶38; *see* Pet. 45-47. Consequently, Petitioner fails to establish a reasonable likelihood that Kim discloses "forming a plurality of

openings in the insulating layer exposing portions of the etch-stop layer” as required by the claims.

B. Kim Does Not Disclose “the forming of each step ... comprises disposing a sacrificial layer over a dielectric layer”

According to Petitioner, “Grounds 1 and 2 rely on Kim’s Figures 17A-22B embodiment.” Pet. 31. The Petition alleges that “Kim discloses the sacrificial-layer-on-top/gate-stack-on-top ordering *even though its figures show the opposite order*”—i.e., a dielectric layer disposed over a sacrificial layer (which later is replaced with the conductive gate stack layer). Pet. 32.⁴ Petitioner’s characterization thus contradicts Kim’s explicit disclosure. As Petitioner acknowledges, Figure 22A of the embodiment Petitioner “relies on” shows that each step comprises a conductive layer 161 to 168 (tan) disposed *below* a dielectric layer 111-118 (light purple), and thus does not show “disposing a sacrificial layer *over* a dielectric layer” as claim 1 requires. Campbell ¶¶39-40. Petitioner does not cite anything in Kim’s description of the Figures 17A-22B embodiment that teaches “disposing a sacrificial layer over a dielectric layer.”

⁴ All emphasis added unless noted otherwise.

Original

Pet. 27 (annotating Kim Fig. 22A); Campbell ¶¶39-40. Thus, Kim does not disclose “disposing a sacrificial layer over a dielectric layer” in the embodiment that “Grounds 1 and 2 rely on.” Pet. 31.

C. Kim in View of a POSITA’s Knowledge Does Not Render Obvious “the forming of each step... comprises disposing a sacrificial layer over a dielectric layer”

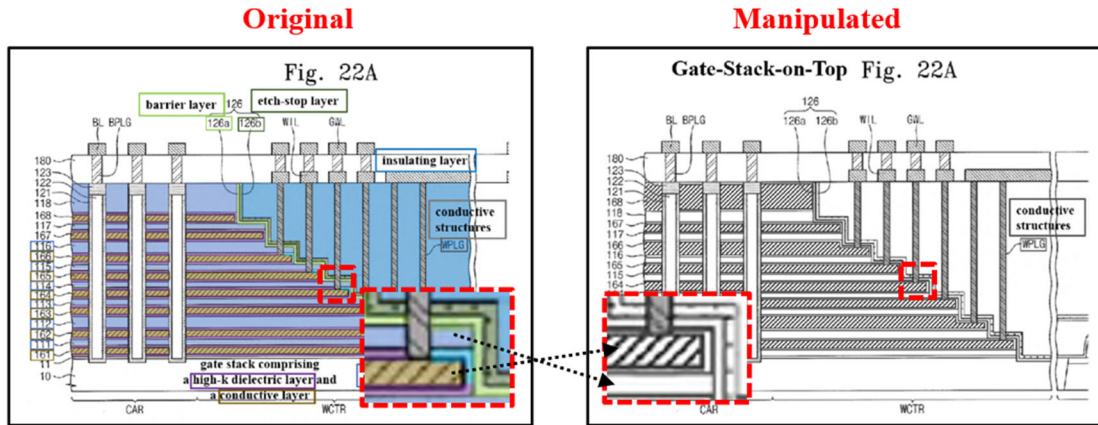
Petitioner asserts that Kim “at least renders the [forming of each step comprises a disposing a sacrificial layer over a dielectric layer] limitation obvious” in the Figures 17A-22B embodiment. Pet. 32-33. According to Petitioner, although “Grounds 1 and 2 rely on Kim’s Figures 17A-22B embodiment,” Kim “discloses other embodiments, *e.g.*, Figures 5A-14B.” Pet. 31. Thus, as Petitioner recognizes, Figures 5A-14B constitute a separate embodiment from the embodiment of Figures 17A-22B. Kim, [014], [017]. Petitioner then cites various

paragraphs about the Figures 5A-14B embodiment to support a wholesale recreation of Figure 22A of the Figures 17A-22B embodiment that reverses the order of the gate stack and dielectric layer. Pet. 27-28 (citing, e.g., Kim [090]).⁵

In the manipulated version of Figure 22A, Petitioner changes the “insulating layers” of Figure 22A to be “gate stacks”⁶ and the “gate stacks” of Figure 22A to be “insulating layers.” In this contorted figure, Petitioner adds hatching to the insulating layers of the original figure (as annotated by Petitioner) to turn them into gate stacks and removes hatching from the gate stacks of the original figure to turn them into insulating layers as shown below.

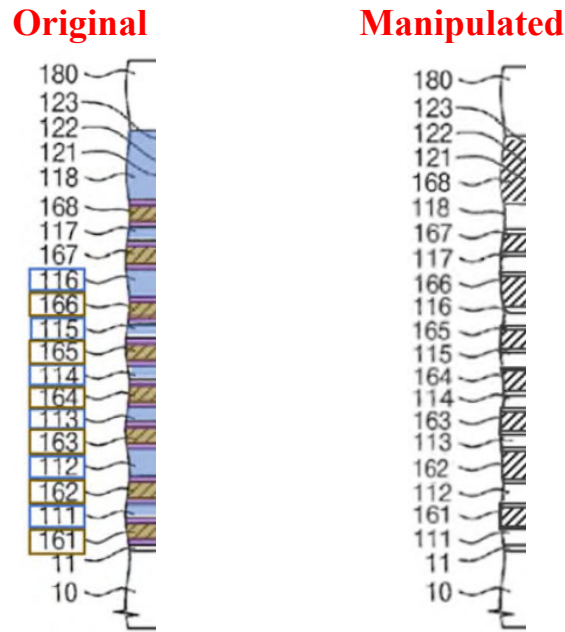
⁵ According to Kim, “FIGS. 5A through 14A and 5B to FIG. 14B are sectional views illustrating a method of fabricating three-dimensional semiconductor memory device of FIG. 4.” Kim [0013]-[0014].

⁶ Petitioner equates the alleged “gate stacks” in Kim’s Figure 22A with the claimed “sacrificial layer”



Pet. 27 (Kim Fig. 22A), 49 (Kim “Gate-Stack-on-Top Fig. 22A”); Campbell ¶42.

Petitioner then rennumbers the labels of Figure 22A so that Kim’s insulating layers are relabeled as gate electrodes and vice versa. For example, Petitioner changes the label “116” (corresponding to an insulating layer) to “166” (corresponding to a gate electrode) and “115” (corresponding to an insulating layer) to “165” (corresponding to a gate electrode), and so on. Campbell ¶¶43-44; Kim [0140] (“gate electrodes 161 to 168”); [0232] (“insulating layers ... 111, 113 to 116, and 118”). Based on this manipulation of Kim’s Figure 22A, Petitioner argues in a vacuum that Kim renders obvious the “disposing a sacrificial layer over a dielectric layer” limitation. Pet. 36-41.



Pet. 27 (Kim Fig. 22A) (cropped), 49 (Kim “Gate-Stack-on-Top Fig. 22A”) (cropped); Campbell ¶43.

But Petitioner fails to proffer any evidence or articulate any reason that a POSITA would have been motivated to combine Kim’s disparate embodiments to arrive at the manipulated figure. Nor has Petitioner shown that a POSITA would have had a reasonable expectation of success in doing so.

1. Petitioner Has Failed to Establish a POSITA Would Have Been Motivated to Combine Disparate Embodiments of Kim to Arrive at the Claimed “forming of each step... comprises disposing a sacrificial layer over a dielectric layer”

Petitioner’s proposed modification of Kim suffers a fundamental flaw:

Petitioner fails to establish that a POSITA would have been motivated to combine

Kim's Figure 17A-22B embodiment with Kim's Figure 5A-14B embodiment as Petitioner proposes. Pet. 27-28, 32.

The Federal Circuit and this Board has consistently held that Petitioners must establish a motivation to combine “disparate embodiments” within a single prior art reference. *Stepan*, 868 F.3d at 1346 n.1 (“combining multiple embodiments from a single reference” requires “a motivation to make the combination”); *In re Kotzab*, 217 F.3d 1365, 1370 (Fed. Cir. 2000) (“Even when obviousness is based on a single prior art reference, there **must be** a showing of a suggestion or motivation to modify the teachings of that reference.”) (citations omitted). As the Federal Circuit has found, the use of “generic statements” to describe features “[i]n other embodiments” “do not establish” the requisite motivation to combine. *BlephEx, LLC v. Myco Indus., Inc.*, 24 F.4th 1391, 1401 (Fed. Cir. 2022) (finding no motivation to combine features based on prior art's teachings of features “[i]n other embodiments”).

Here, Petitioner acknowledges that it is combining features from Kim's Figures 17A-22B embodiment with features from the Figures 5A-14B embodiment. Pet. 27-28 (combining disclosure from Kim [0090] with Figures 17A-22B), 32. But Petitioner fails to provide any reason a POSITA would have been motivated to replace the “gate electrodes” in the memory stack of the Figures 17A-22B embodiment with “insulating layers,” and “insulating layers” with “gate

electrodes.” Petitioner identifies no flaw or problem this modification would address. Nor does Petitioner identify any benefit that would result from the proposed modification. Petitioner provides only conclusory reasons that purport to support its modification of Figures 17A-22B. All fail.

First, Petitioner asserts that “[a] POSITA would have understood that descriptions of one of Kim’s embodiments apply to other embodiments except where the embodiments differ.” Pet. 32. As support, Petitioner cites only its expert, Dr. Banerjee. But Dr. Banerjee only parrots the language of the Petition. Ex.1003 ¶¶80-81. The Board should give Dr. Banerjee’s declaration no weight. *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15-16 (Aug. 24, 2022) (precedential) (expert testimony that is “conclusory and unsupported, [and] adds little to the conclusory assertion for which it is offered to support” is “entitled to little weight”) (citations omitted).

Regardless, Petitioner’s and its expert’s conclusory assertion that Kim’s disparate embodiments can be combined “except where the embodiments differ” falls well short of articulating a proper motivation to combine, as required. *Personal Web. Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993-94 (Fed. Cir. 2017) (rejecting reasoning “that a skilled artisan, once presented with the two references, would have understood that they could be combined” because “that is not enough: it does not imply a motivation to pick out those two references and combine them

to arrive at the claimed invention”) (citations omitted); *In re Nuvasive, Inc.*, 842 F.3d 1376, 1381-85 (Fed. Cir. 2016) (holding that a proper motivation to combine includes “identif[ying] a reason why a PHOSITA would have combined the prior art references—i.e., ‘minimiz[ing] waste’ and ‘allow[ing] for a greater degree of movement’—that had a foundation in the prior art”) (citations omitted). Petitioner provides no reason *why* a POSITA would have been motivated to combine the Figures 17A-22B embodiment with the Figures 5A-14B embodiment to reverse the order of gate electrodes and insulating layers. Pet. 32. The Petition identifies no problem solved and no benefit achieved by this modification.

Second, Petitioner asserts that Kim’s embodiments are “[c]losely related.” Pet. 32. Courts have found that generic assertions of relatedness (like Petitioner’s) insufficient to establish the required motivation to combine. *Securus Techs., Inc. v. Glob. Tel*Link Corp.*, 701 F. App’x 971, 977 (Fed. Cir. 2017) (“a broad characterization of [prior art references] as both falling within the same alleged field ... without more, is not enough for [Petitioner] to meet its burden of presenting a sufficient rationale to support an obviousness conclusion”); *see also Microsoft Corp. v. Enfish, LLC*, 662 F. App’x 981, 990 (Fed. Cir. 2016) (“[The] Board correctly concluded that [the petitioner] did not articulate a sufficient motivation to combine. With respect to [certain challenged claims], [the petitioner] gave no reason for the motivation of a person of ordinary skill to

combine [the two references] except that the references were directed to the same art or same techniques"). Petitioner's conclusory allegation that Kim's embodiments are "closely related" fails to establish a proper motivation to combine. *Cf.* Pet. 32.

Moreover, Petitioner's reasons for alleging the embodiments are "closely related" do not provide a motivation to combine them. Pet. 32. For example, Petitioner alleges that "many of the same elements are denoted by the same reference numerals." Pet. 32. Petitioner cites no authority holding that denoting elements with the "same reference numerals" is sufficient to establish a motivation to combine. None exist. To the contrary, Kim makes clear that the use of the same reference numbers and "previously described" element descriptions is to allow "for *concise description*"—not because Kim contemplates mixing and matching features from disparate embodiments. Kim [0184]. Petitioner also cites paragraph 184 of Kim to allege that the Figures 5A-14B and 17A-22B embodiments are "closely related." Pet. 32. But paragraph 184 of Kim simply acknowledges that, in describing the Figures 17A to 22B embodiment, "overlapping description[s] of elements previously described with reference to FIGS. 5A through 14A and FIGS. 5B through 14B may be omitted." Kim [0184]. It does not provide a motivation to combine the two disparate embodiments, let alone in the particular manner that Petitioner proposes in its manipulated figures described above.

Third, Petitioner asserts that “the descriptions of Figures 17A-22B extensively reference Figures 9A-14B.” Pet. 32. Again, Petitioner fails to establish how or why this would motivate a POSITA to make the proposed modifications to the Figures 17A-22B embodiment. In the cited paragraphs, Kim only states that certain features of the Figures 17-22B embodiment may be “described with reference to” Figures 9A to 14B—for example, the steps of forming “the interlayer dielectric 130 and the polishing stop layer” (Kim [0188]); various “planarization” processes (*id.* [0190], [0193]); forming “trenches” and “replacing the sacrificial layers” (*id.* [0198]) and others. The cited paragraphs say nothing about combining the disclosures about the insulating layers and gate electrodes of the Figures 17A-22B embodiment with disclosures about those structures from the Figures 5A-14B embodiment—let alone disclose that the insulating layers and gate electrodes of the Figure 17A-22B embodiment may be swapped.⁷

⁷ Petitioner also asserts that “descriptions of Figures 26-27 refer to the two embodiments in Figures 17A-22A and 8A-11A.” Pet. 32. But Petitioner does not propose combining the Figures 17A-22A embodiment with anything from Figures 26-27.

Finally, Petitioner cites the Chen (Ex. 1008) reference in passing and asserts that “POSITA would have known that either order was a common alternative.”

Pet. 33. But just because Chen discloses semiconductors with a “dielectric on top” and a “conductor on top” does not mean a POSITA “would have been motivated to make the combinations or modifications” to Kim’s Figures 17A-22B embodiment.

See Belden Inc. v. Berk-Tek LLC, 805 F.3d 1064, 1073 (Fed. Cir. 2015)

(“[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.”) (citations omitted); *Personal Web Techs.*, 848 F.3d at 993-94 (conclusion that a combination “would have allowed for” a claimed limitation “is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention”) (citations omitted).

In short, Petitioner has failed to establish that a POSITA would have been motivated to combine disparate embodiments of Kim as Petitioner proposes to arrive at the claimed invention. Petitioner’s unexplained swap instead reflects impermissible hindsight reconstruction of the claimed invention. *Abbott Labs. v. Sandoz, Inc.*, 544 F.3d 1341, 1348 (Fed. Cir. 2008) (“[I]n addressing the question of obviousness a judge must not pick and choose isolated elements from the prior art and combine them so as to yield the invention in question if such a combination

would not have been obvious at the time of the invention.” (quoting *Dennison Mfg. Co. v. Panduit Corp.*, 475 U.S. 809, 810 (1986)).

2. Petitioner Has Failed to Establish a POSITA Would Have Had a Reasonable Expectation of Success in Modifying Kim to Arrive at the Claimed “forming of each step... comprises disposing a sacrificial layer over a dielectric layer”

Even if Petitioner had established a motivation to combine (it has not), Petitioner has failed to establish that a POSITA would have had a reasonable expectation of success in implementing the proposed combination. The Federal Circuit has “emphasize[d]” the “clear distinction in our case law between a patent challenger’s burden to prove that a skilled artisan would have been motivated to combine prior art references and the additional requirement that the patent challenger also prove that the skilled artisan would have had a reasonable expectation of successfully achieving the claimed invention from the combination.” *Eli Lilly & Co. v. Teva Pharms. Int’l GmbH*, 8 F.4th 1331, 1344 (Fed. Cir. 2021) (citations omitted). “A finding by the Board that a patent challenger has demonstrated a motivation to combine references does not necessarily imply that the challenger has also met its burden of showing a reasonable expectation of success in achieving a claimed method of treatment.” *Id.*

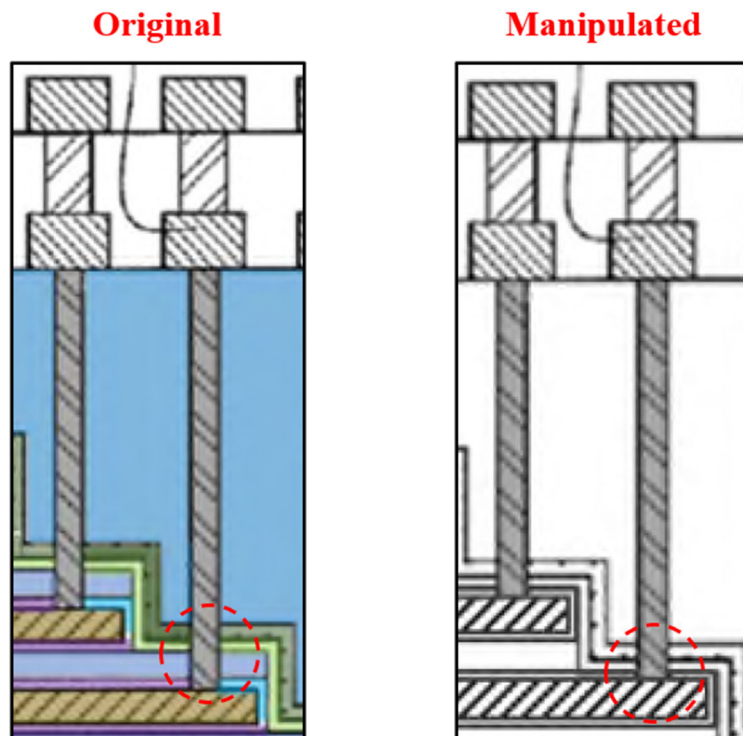
Here, Petitioner asserts that “[a] POSITA would have known that” changing the order of Kim’s insulating layer and gate electrode “was routine, highly predictable, and would have had a reasonable expectation of success for

implementing a gate-stack-on-top embodiment.” Pet. 33. Petitioner cites Dr. Banerjee, who merely parrots the language of the Petition and adds that “common deposition techniques such as CVD or ALD” could be used with the proposed modification. *See* Ex.1003 ¶84; Pet. 33.

Petitioner misses the point. Simply because “common deposition techniques” can be used with the proposed modification does not provide a “clear, evidence-supported account” of “how the combination” would work as required. *Personal Web Techs.*, 848 F.3d at 994. This is especially true where, as here, the proposed combination involves fundamentally changing the memory stack of Kim by replacing insulating materials with conductive gate electrodes and conductive gate electrodes with insulating materials. *See supra* §III.B.1.

While Petitioner tries to trivialize its wholesale modification to Kim, Petitioner’s proposal is far from a trivial change. A POSITA would understand that replacing a functional, gate stack with insulating material and vice versa would require extensive modifications to the manufacturing process and device—all of which Petitioner ignores. Campbell ¶¶46-47. As just one example (and as Petitioner recognized in its modified figure), for Petitioner’s “Gate-Stack-on-Top” modification to work, the process for forming word line contacts (shown in gray below) would also need to be modified to use an entirely different etching process. As can be seen below, the contact opening in the actual Kim embodiment

(Original) penetrates the etch-stop layer, the barrier layer, the dielectric layer, and then through to the conductive layer in the gate stack. However, in Petitioner's manipulated figure (Manipulated), the contact opening penetrates only through the etch-stop layer and the barrier layer before arriving at the conductive layer in the gate stack. through different materials with different depths. Campbell ¶¶46-47. Petitioner does not explain how or why a POSITA could etch such vertical contacts without undue experimentation and with a reasonable expectation of success. Pet. 27 (Kim Fig. 22A) (cropped below), 49 (Kim "Gate-Stack-on-Top Fig. 22A") (cropped below).



Changing how a vertical contact penetrates the layers of a semiconductor device is not a trivial change, but requires fundamental changes to the manufacturing

process and device structure. Campbell ¶¶46-47. Petitioner fails to address this (and other) modifications that would be required. *Id.*

Petitioner further asserts that Kim's using conductors over dielectrics represents a "known technique" or "'a suitable option' for the Figure 17A-22B embodiment." Pet. 33 (quoting *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023)). But Kim does *not* teach that "reversing the order" is "suitable" for the Figure 17A-22B embodiment. Pet. 33. Kim says nothing about "reversing the order," and the passage that Petitioner relies on merely discloses that the sacrificial layers "may be partially exposed in the word line contact region." Pet. 27-28 (quoting Kim [0090]). Kim does not teach that this exposure is "suitable" for the Figure 17A-22B embodiment. Rather, Kim discloses this exposure applies to "other embodiments" that are not Figures 17A-22B. Kim [0090]. As Petitioner admits, the Figure 17A-22B embodiment "show[s] the opposite order" than the claims of the '276 Patent.

In short, Petitioner has failed to identify any motivation to combine disparate embodiments of Kim or that a POSITA would have had a reasonable expectation of success in doing so. The Petition should be denied.

D. Kim in View of a POSITA's Knowledge Does Not Render Obvious the Dependent Claims (Claims 2-9, 11-12, 14-16, 18-19)

Because they depend from independent claim 1, Petitioner fails to establish claims 2, 4, 5, and 9-18 would have been obvious for the reasons described above.

See In re Fine, 837 F.2d 1071, 1076 (Fed. Cir. 1988) (“Dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious.”) (citations omitted); *Tris Pharma, Inc. v. Teva Pharms. USA, Inc.*, No. 20-00212, 2022 WL 4082190, at *18 (D.N.J. Sept. 6, 2022) (“Because I have found that claim 1 of the ’545 patent nonobvious and claim 24 of the ’545 patent is dependent on claim 1, claim 24 must therefore also be nonobvious and valid.”) (citation omitted).

IV. Ground 2: Petitioner Fails to Meet Its Burden to Establish Kim in View of Fang Renders Obvious Claims 1-18

Kim in view of a POSITA's knowledge does not render obvious “forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer” or “the forming of each step... comprises disposing a sacrificial layer over a dielectric layer” as recited in independent claim 1. *See supra* §III.

Petitioner does not rely on Fang to teach these claim limitations. Pet. 64-65. Instead, Petitioner purports to rely on Fang to disclose a “high-k dielectric etch-stop layer.” *Id.* Accordingly, Ground 2 fails for the same reasons as Ground 1 as to claim 1, as well as for dependent claims 2-17. Petitioner has not established a reasonable likelihood that the combination of Kim and Fang renders claims 1-18 obvious.

V. Ground 3: Petitioner Fails to Meet Its Burden to Establish Han in View of Fang Renders Obvious Claims 1-15

Petitioner proposes to combine Han with Fang. For the reasons discussed below, Petitioner has not shown a reasonable likelihood that a combination of Han and Fang renders obvious claims 1-15 of the '276 Patent.

A. A POSITA Would Not Have Been Motivated to Modify the Steps of Han to Render Obvious “disposing an etch-stop layer on each step”

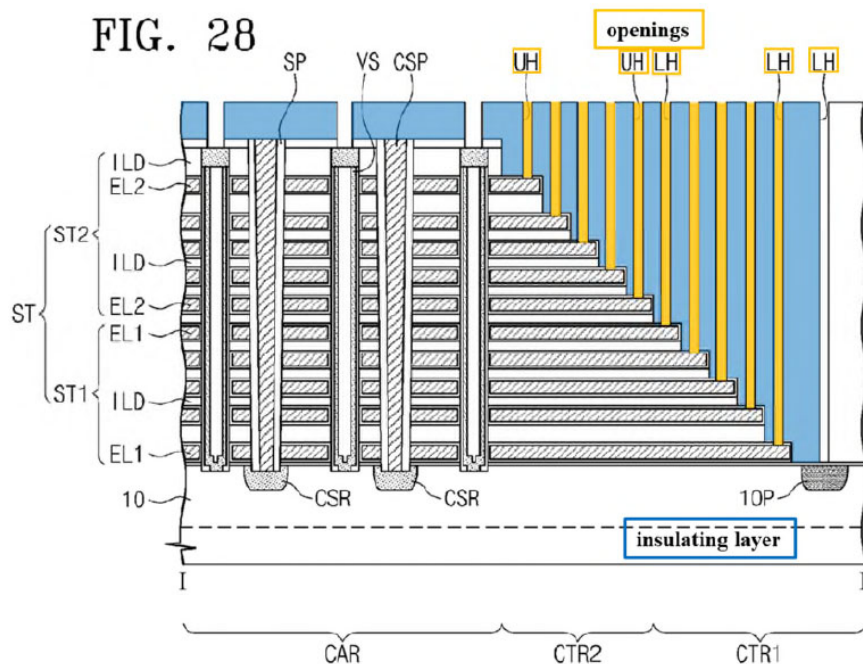
The challenged claims require “disposing an etch-stop layer on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer.”

Petitioner acknowledges that Han does not disclose an etch-stop layer. Pet. 79, 102. Petitioner proposes “adapt[ing] Han’s staircase by adding Fang’s etch-stop layer.” Pet. 102. Attempting to justify this addition, Petitioner cites Fang’s disclosure of “multiple masks” as a solution to punch-through in the prior art and Fang’s disclosure that using multiple masks “add[s] additional processing acts, complexity, and cost to the overall process.” Pet. 102 (quoting Fang [0004]). Petitioner then asserts—with no support or explanation—that “Han’s method suffered from this exact problem.” Pet. 102. But Petitioner fails to cite any disclosure in Han to support its assertion that Han suffers from the problem described in Fang, let alone a disclosure of “multiple masks.” Pet. 102. In fact, Han does not use the term “multiple masks.” Campbell ¶50. Although Han does

disclose the use of a mask pattern, it does not disclose such use for forming openings in the contact region of the circuit. *See* Han [0041] (mask pattern used to etch opening 25, e.g., in Figure 1), [0105] (mask pattern used to etch the thin-layer structure 110, e.g., in Figure 17), [0111] (mask pattern used to form trenches T, e.g., in Figure 17); Campbell ¶50.

Contrary to Petitioner's conclusory assertion, Han discloses that all the contact holes in the contact region can be formed using "[a]t least one patterning process"—which includes a single process. Han [0156]; Campbell ¶51.

Specifically, as shown in Petitioner's annotation of Han's Figure 26, below, Han includes upper holes UH and lower holes LH that are formed by "[a]t least one patterning process." Han [0156].



Pet. 87 (annotating Han Fig. 28)

Han is silent about the use of “multiple masks” in this “[a]t least one patterning process.” Han [0156]. And although Han discloses that the upper holes “may be formed before the formation of the lower contact holes” in “some exemplary embodiments” (*id.*), there is no suggestion that the relative timing of forming these holes requires “multiple masks” or suffers from the problems Petitioner reads into Han. *Cf.* Pet. 102. Nor is Han limited to forming these holes at different times, as this passage relates only to “some exemplary embodiments.” Han [0156]; Campbell ¶52. Thus, a POSITA would not have understood Han to have the problems that Fang describes and that Petitioner attributes to Han. Campbell ¶52.

Nor would a POSITA have viewed Han's process of forming upper holes and lower holes as requiring more “processing acts, complexity, and cost” than Fang's system. Campbell ¶53. Under Han's approach for forming the contact holes (which is not the approach Fang disparages), holes can be formed in “[a]t least one patterning process” and in some embodiments, the upper holes can be formed before the lower holes using the *same* process. Han [0156]; Campbell ¶53. In contrast, Fang requires additional step, and a new process, of forming an etch stop material “over exposed horizontal and exposed vertical surfaces of the oxide materials 115 and nitride materials 120.” Fang [0020]. Petitioner does not address Fang's additional processing steps, complexity, and cost in comparison to Han's

solution and instead assumes—with no support—that Han's solution has the problems that Fan intended to address.

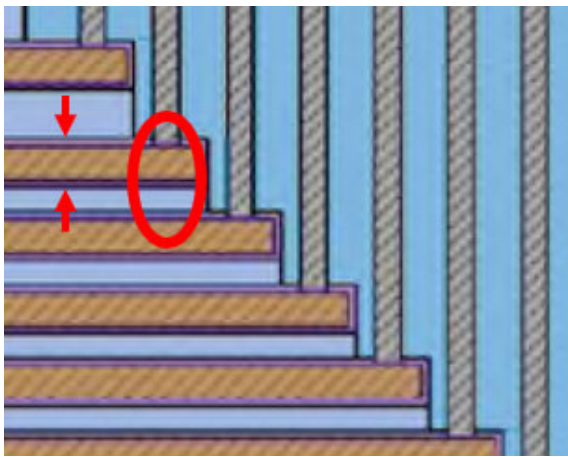
B. A POSITA Would Not Have Been Motivated to Combine Han and Fang

In addition to failing to show that a POSITA would have had a reason to add “disposing an etch-stop layer” to Han, Petitioner has failed to demonstrate that a POSITA would have combined Han and Fang at all. Campbell ¶¶54-55. Han and Fang disclose significantly different structures, and Petitioner's cherry-picking of features from Fang to add to Han is borne out of impermissible hindsight. *Abbott*, 544 F.3d at 1348.

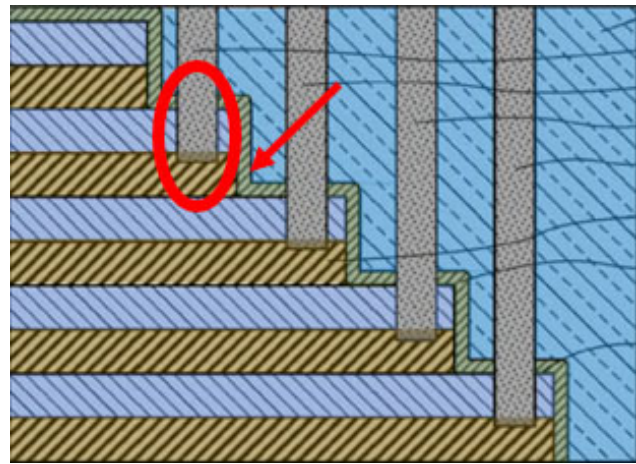
Han and Fang differ particularly in their staircase regions. As shown in the comparison below, Han and Fang differ in three significant ways: (1) they have different gate structures; (2) they have opposite stair step compositions; and (3) they have different layer configurations.

First, Han and Fang employ different gate structures. Han employs a “horizontal insulating layer” that “cover[s] inner surfaces of the gate regions” and a conductive layer filling the remainder. Han [0118]-[0119]. Petitioner maps this two-layer design (shown between red arrows in Han Figure 29, below left) to the claimed “gate stack.” Pet. 84. Fang, however, employs a simple conductive layer as shown highlighted in gold in Fang's Figure 6, below right. Second, Han and Fang employ the *opposite* stair step composition. Specifically, as shown in the

circled portions in both figures below, Han's Figure 29 discloses a stair step with the gate (gold) above the dielectric (lilac), and Fang's Figure 6 discloses a stair step with the gate (gold) below the dielectric (lilac). Third, Han and Fang use different layer configurations for its staircase, and specifically, as shown by the red arrow added to Fang's Figure 6 below, Fang employs an etch stop layer completely absent in Han. Campbell ¶¶56-58.



Han Fig. 29 (cropped)



Fang Fig. 6

Petitioner ignores these differences. But these differences would have influenced a POSITA away from combining Han and Fang. Specifically, by placing the gate on top of the stair, employing a “horizontal insulating layer” as part of the gate, and forming “upper” and “lower” contact holes, Han's structure has no need for an etch stop layer. As shown in the comparison above, Han's contact holes must penetrate the “horizontal insulating layer”—which is not an etch stop layer separate from a gate stack—and thus implicates different process

considerations than Fang's process, which does not include a horizontal insulating layer. Campbell ¶59. Petitioner fails to address these issues. As such, Petitioner's picking and choosing of various features in Fang to incorporate in Han is based on nothing more than hindsight. *Abbott*, 544 F.3d at 1348.

For the above reasons, Petitioner has failed to demonstrate a reasonable likelihood that a POSITA would have combined Han and Fang. Accordingly, Ground 3 fails.

VI. Ground 4: Petitioner Fails to Meet Its Burden to Establish Han in View of Fang and Chen Renders Obvious Claims 17-18

Han in view of Fang does not render obvious independent claim 1. *See supra* §V. Petitioner does not rely on Chen for claim 1. Pet. 103-05. Instead, Petitioner purports to rely on Chen only for limitations recited in claims 17-18, which both depend from claim 1. *Id.* Accordingly, Ground 4 fails for the same reasons as Ground 3. Petitioner has not established a reasonable likelihood that the combination of Han, Fang, and Chen renders claims 17-18 obvious.

VII. Conclusion

For the reasons set forth above, the Board should deny the Petition for *Inter Partes* Review.

Respectfully submitted,

Dated: April 30, 2025

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CERTIFICATE OF COMPLIANCE WITH 37 C.F.R. § 42.24

I hereby certify that this Patent Owner's Preliminary Response complies with the word count limitation of 37 C.F.R. § 42.24(b)(1) because the Patent Owner's Preliminary Response contains 6,232 words using Microsoft Word's counting feature, excluding the cover page, signature block, and the parts of the Patent Owner's Preliminary Response exempted by 37 C.F.R. § 42.24(b)(1).

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 30th day of April, 2025, a true and correct copy of the foregoing **Patent Owner's Preliminary Response and all Exhibits** were served by electronic mail on Petitioner's lead and backup counsel at the following email addresses:

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