

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00228
Patent 11,101,276

**DECLARATION OF STEVE CAMPBELL
IN SUPPORT OF
PATENT OWNER'S PRELIMINARY RESPONSE**

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I. Introduction and Qualifications

1. I have been retained by Yangtze Memory Technologies Company, Ltd. (“YMTC” or “Patent Owner”) to provide my opinion concerning the validity of U.S. Patent No. 11,101,276 (Ex. 1001) (“’276 Patent”).

2. I received my Bachelor’s degree in Physics from the University of St. Thomas (St. Paul, Minnesota) in 1975, and my M.S. and Ph.D. in Physics from Northwestern University (Evanston, Illinois) in 1978 and 1981, respectively. I then joined Sperry, now called Unisys, in 1981 as a CMOS process development engineer. In 1982, I was assigned the lead engineer for the 1.2 μm technology process development effort. In 1984 I was promoted to head of silicon research for the company. This involved a wide variety of process technologies for submicron CMOS.

3. In 1986, I joined the University of Minnesota as an Assistant Professor in the Electrical Engineering Department. My research at the University involved semiconductor processing, materials, and device structures. I raised more than \$100M in various grants and successful submissions to companies and industry consortiums such as the Semiconductor Research Association, as well as State and US government agencies including DARPA and the National Science Foundation. The first ten years of my career at the University concentrated on the development of rapid thermal annealing for 200 mm wafers, particle control in

CVD systems, and the development of high uniformity rapid wafer annealing systems. The next ten years were dedicated to the invention and development of high permittivity (aka high-k) films for use as gate insulators. This is necessary to allow the development of deeply scaled CMOS devices. This technology has been widely adopted for nanoscale CMOS devices. In the last fifteen years at the University, my work involved the development of low-cost tandem photovoltaics and micro electromechanical systems (MEMS). The latter included a chronic deep brain sense/stimulation system and very high-speed mechanical switches. Finally, I developed processes for the fabrication of novel 2D materials such as black arsenic, and fabricated transistors using these materials. I retired from the University in 2021.

4. A brief summary of my work at the University would include:

- Approximately 200 publications
- The leading textbook on semiconductor technology. Currently in its fourth edition, Fabrication Engineering at the Micro and Nanoscale (Oxford 1996, 2000, 2008, 2013) is the dominant text on the topic.
- Honors from outside the University such as being named a Presidential Young Investigator by the National Science

Foundation and a Life Fellow by the Institute of Electrical and Electronic Engineers (IEEE).

- Honors within the University including outstanding service and outstanding teaching.
- As the Director of the University's Nanofabrication Center, I increased lab usage from 30 to more than 300 users, enabling millions of dollars research awards annually by Minnesota faculty, and leading to the construction of a new \$80M building with an expansive cleanroom facility.

5. Since retiring from the University, I have consulted with semiconductor companies including patent litigation.

6. Additional information regarding my education, technical experience and publications, including a list of the U.S. patents of which I am an inventor/coinventor, is included in my *Curriculum Vitae*, which I understand is attached at Exhibit 2007.

II. Summary Of Materials Reviewed And Considered

7. All of the opinions contained in this declaration are based on the documents I reviewed and my knowledge and professional judgment. In forming the opinions expressed in this declaration, while drawing on my experience in the field of semiconductor fabrication, I reviewed the following documents:

Ex.	Description
1001	U.S. Patent No. 11,101,276 to Zhu et al. (“’276 Patent”)
1002	File History of U.S. Patent No. 11,101,276 (“’276 FH”)
1003	Declaration of Dr. Sanjay Banerjee (“Banerjee”)
1004	Curriculum Vitae of Dr. Sanjay Banerjee
1005	U.S. Patent Publication No. 2012/0070944A1 to Kim et al. (“Kim”)
1006	U.S. Patent Publication No. 2019/0067306A1 to Fang et al. (“Fang”)
1007	U.S. Patent Publication No. 2017/0062470A1 to Han et al. (“Han”)
1008	U.S. Patent Publication No. 2017/0294384A1 to Chen (“Chen”)
1010	Aritome, “NAND Flash Memory Technologies” (2016)
1011	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
1012	Michelsoni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)
1013	U.S. Patent Publication No. 2017/0117222A1 to Kim et al.
1014	Chang and Sze, “ULSI Technology” (1996)
1015	Orlowski et al., <i>Si, SiGe, Ge, and III-V Semiconductor Nanomembranes and Nanowires Enabled by SiGe Epitaxy</i> , ECS Transactions Vo. 33, No. 6 (2010), 777-89
1016	U.S. Patent No. 9,728,547 to Ohsaki et al.
1017	U.S. Patent Publication No. 2017/0148677A1 to Shin
1027	Kim et al., <i>Dry Etching of High-k Dielectric Thin Films in HBr/Ar Plasma</i> , Journal of the Korean Physical Society, vol. 54, no. 2, Feb. 2009, pp. 934-938
1028	U.S. Patent No. 10,297,543 to Park et al.

8. My opinions are additionally guided by my appreciation of how a person of ordinary skill in the art (“POSITA”) would have understood the claims

of the '276 Patent at the time of the effective filing date of the patent, which I have been asked to assume is August 31, 2017.

III. Understanding of Legal Standards

9. I am not an attorney, and in this Declaration, I do not opine on matters of law. For the purposes of this Declaration, I have been informed about certain aspects of the law that are relevant to my analysis and opinions. My understanding of these principles is set forth below.

10. I have been informed by Counsel that the validity analysis is a two-step process. First, the patent claims are construed to ascertain their proper scope. Second, the construed claims are compared to the identified prior art to determine if the claims are valid over the prior art.

A. Claim Construction

11. I have been informed by Counsel that the claims of a patent define the limits of the patentee's exclusive rights. I have been informed by Counsel that to determine the scope of the claimed invention, courts typically construe claim terms, the meaning of which the parties may dispute. I have been informed by Counsel that claim terms should generally be given their ordinary and customary meaning as understood by one of ordinary skill in the art at the time of filing of the patent application, after reading the patent and its prosecution history. I also have been informed by Counsel that a basic tenet of claim construction presumes

that different words in a claim have different meanings, unless there is evidence to the contrary.

12. I have been informed by Counsel that claims must be construed in light of, and consistent with, the intrinsic evidence. In this context, I have been informed by Counsel that intrinsic evidence includes the claims themselves, the written disclosure in the specification, and the patent's prosecution history, including prior art that was considered by the United States Patent and Trademark Office ("USPTO"). I have been informed by Counsel that the specification is always highly relevant to the claim construction analysis and often is the single best guide to the meaning of a disputed term. I have been informed by Counsel that extrinsic evidence may also be considered when construing claims and may include, for example, technical dictionaries, technical publications and books, treatises, and expert testimony.

B. Obviousness

13. I have been informed by Counsel that patent claims can be deemed invalid if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. While such conclusions are often based on more than one piece of prior art, only one is required. It is not sufficient that a collection of prior art references merely recites

the various elements of a challenged patent claim. Rather, as I have been informed by Counsel, the prior art must present the elements in a manner that is consistent with their arrangement or use in the challenged claims. I have been informed by Counsel that obviousness cannot be based on the hindsight combination of components selectively culled from the prior art.

14. I have been informed by Counsel that a person having ordinary skill in the art (i.e., a POSITA) is a hypothetical person who is presumed to have known the relevant art at the time the invention was made. I have been informed by Counsel that the condition “at the time the invention was made” is imposed to rule out impermissible hindsight. I also have been informed by Counsel that an expert is to analyze the prior art from the perspective of a person of ordinary skill in the art at the time the invention was made, and not simply to provide his/her own personal conclusions.

15. I also have been informed by Counsel that an obviousness determination includes several factual inquiries, including (1) determining the scope and content of the prior art; (2) ascertaining the differences between the claimed invention and the prior art; (3) resolving the level of ordinary skill in the pertinent art; and (4) taking into consideration any objective indicia of nonobviousness.

16. I have been informed by Counsel that obviousness must be determined as of the date of the invention (i.e., the effective filing date or priority date of the patent). Thus, in considering the reason or motivation to combine references, it is essential to avoid using hindsight. For example, the problem examined when considering obviousness is the general problem that confronted the inventor before the invention was made, not the specific problem solved by the invention. Defining the problem in terms of its solution reveals improper hindsight in the selection of the prior art relevant to obviousness. Further, an overly narrow statement of the problem can represent a form of hindsight, because often the inventive contribution lies in defining the problem in a new revelatory way. Similarly, an assertion that a person of ordinary skill could combine the references, rather than that they would have been motivated to do so, is an impermissible form of hindsight. Moreover, knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references to reach the particular claimed invention.

17. I have been informed by Counsel that a motivation to solve a problem (or issue) is not the same as a motivation to have combined references. I have been informed by Counsel that whether a skilled artisan would be motivated to make a combination includes whether he/she would select particular references in order to combine their elements.

18. I have been informed by Counsel that the analysis of the motivation to combine should be explicit. Additionally, it must include articulated reasoning with rational underpinnings to support the conclusion of obviousness. Providing a full explanation of the motivation to combine the references and the reasonable expectation of success is a necessary component of the obviousness inquiry, as inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known. However, conclusory statements fail to adequately explain why a person of ordinary skill would have a motivation to combine the potential prior art references.

19. I have been informed by Counsel that common sense, common wisdom, and common knowledge may be used to support a motivation to combine, so long as the use of common sense in the analysis is explained with sufficient reasoning. But, common sense can only be used to supply a limitation missing from the prior art where the technology is unusually simple and straightforward.

20. I also have been informed by Counsel that evidence suggesting reasons to combine cannot be viewed apart from evidence suggesting reasons not to combine. In analyzing motivation, both advantages and disadvantages must be considered. Teaching away, for example, is a statement in the prior art that either

(i) discourages one from following the path of the claimed invention, or (ii) encourages one to follow a path that diverges from the path of the claimed invention. The concept of teaching away bears directly on whether there was a reason to combine prior art. Known disadvantages in prior art technology or devices which would naturally discourage a search for new inventions may also be taken into account in determining obviousness.

IV. Level of Ordinary Skill in the Art

21. Dr. Banerjee defines a person of ordinary skill in the art (“POSITA”) as a person having “a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).” Ex. 1003 ¶ 42.

22. For the purposes of this declaration, I have not been asked to provide an opinion on the level of ordinary skill in the art. In view of my educational background and work experience, I surpass Dr. Banerjee definition of a POSITA, and did so before August 31, 2017. Regardless of the precise definition of a POSITA, Grounds 1-4 of the Petition do not show the challenged claims obvious.

I reserve the right to opine as to an alternative level of a POSITA in other proceedings or if the Board institutes review in this proceeding.

V. Overview of the '276 Patent (Ex. 1001)

23. The '276 Patent is titled “Word Line Contact Structure for Three-Dimensional Memory Devices and Fabrication Methods Thereof.” The specification discloses “a word line contact structure for three-dimensional (3D) memory array and methods for forming the same.” '276 Patent 1:40-42.

24. To meet the demand for higher storage capacity, manufacturers have tried to increase the number of conductor/dielectric layer pairs in 3D memory devices, which created challenges of balancing manufacturing throughput and process complexity/cost. '276 Patent at 5:42-46. Lithography and etching processes create holes in the insulating layer above the staircase structure that are then filled with conductive material to create contacts for conductive layers of the staircase. *Id.* 5:47-49. The required hole depth depends on the distance between the top of the insulating layer and the conductive layer of each level, and can vary between steps. *Id.* 5:49-54. This leads to holes for lower levels being deeper than holes for the upper levels. *Id.*

25. Typically, when using a single etching process, the material in the staircase structure in the upper levels is often over-etched (or “punched through”) and lost before holes in the lower levels are formed. *Id.* 5:54-58. Manufacturers

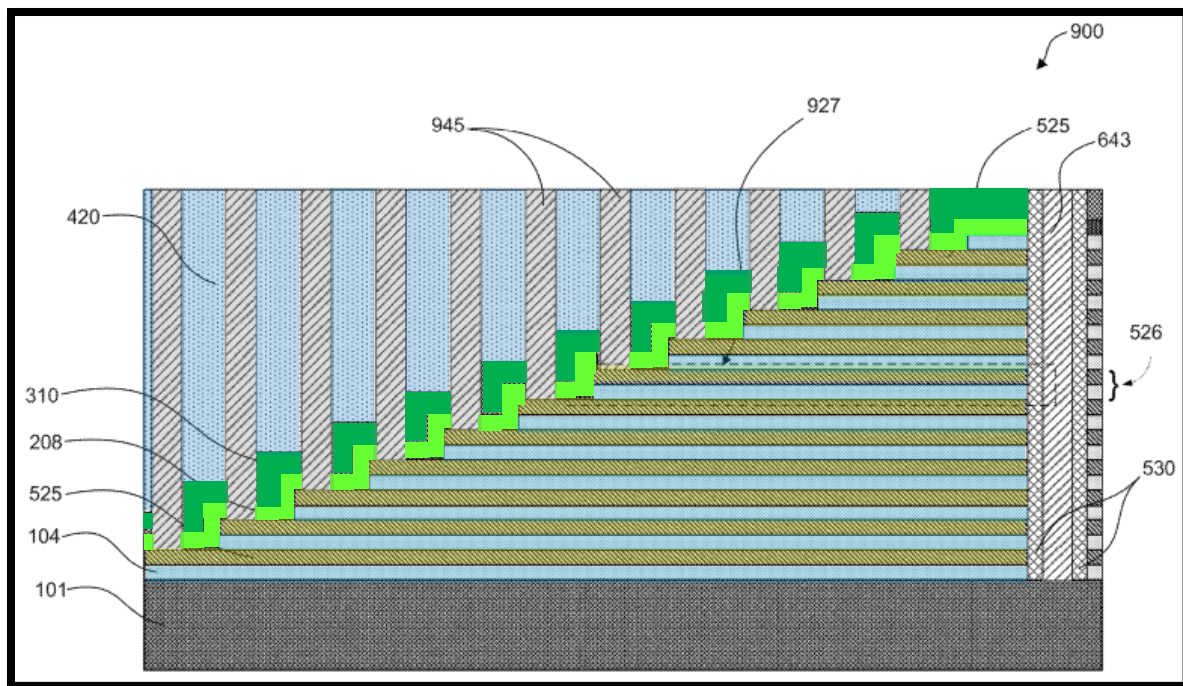
tried to address the problem by using two or more etching processes that would create holes of similar depth at the same time before creating holes at other depths. *Id.* 5:58-60. But this method creates problems of additional fabrication cost and complexity. *Id.*

26. The '276 Patent solves the punch through problem without the drawbacks of separate etching steps for different hole depths. '276 Patent 5:61-6:5. The solution includes an “etch stop layer” over the staircase structure, which protects underlying staircase structure layers during the etching process and permits the simultaneous etching of all word line holes. *Id.* This improves fabrication yield and reduces cost. *Id.* 6:5-7. A barrier layer can also be introduced over the staircase structure “for protecting the underlying structure during subsequent etching processes.” *Id.* 7:41-45.

27. The disclosed solution also allows the formation of semiconductor interconnect structures for inter-connecting components at different layers with an uneven topology. *Id.* 6:7-10.

28. Figure 9A, annotated below, is a cross-sectional view of an exemplary '276 Patent 3D memory device staircase structure. The staircase structure 900 includes a substrate conductive structure 643 oriented vertically on a substrate 101 and extending through alternating layers of gate stacks 525 (yellow) and first insulating layers 104 (lighter blue). *Id.* 6:11-12, 8:60-61, 10:34-38. A second

insulating layer 208 (bright green), which can be a barrier layer, is formed on the staircase structure 900, including on the top and side surfaces of each step. *Id.* 7:36-45. An etch-stop layer 310 (green) is on the staircase structure 900, including on the second insulating layer 208. *Id.* 7:62-64, 8:5-6. A third insulating layer 420 (dark blue) is on the staircase structure 900. *Id.* 8:26-30. Vertical interconnect access (“VIA”) structures 945 (grey) are formed in VIA openings 840 in the third insulating layer 420. *Id.* 11:17-22.

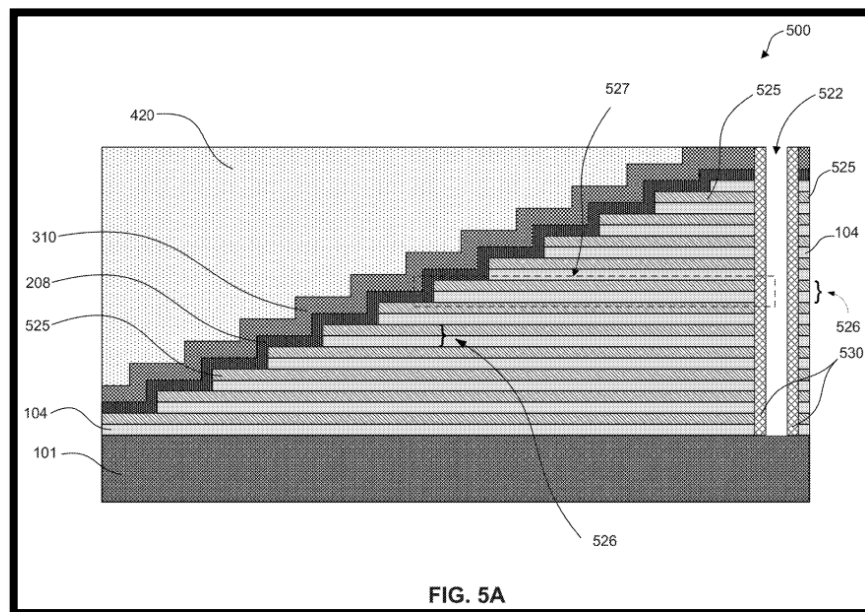


'276 Patent, Figure 9A (annotated)

No.	Structure
525	Gate Stack
104	First Insulating Layer
208	Second Insulating Layer
310	Etch-Stop Layer
420	Third Insulating Layer
945	Vertical Interconnect Access Conductive Structures

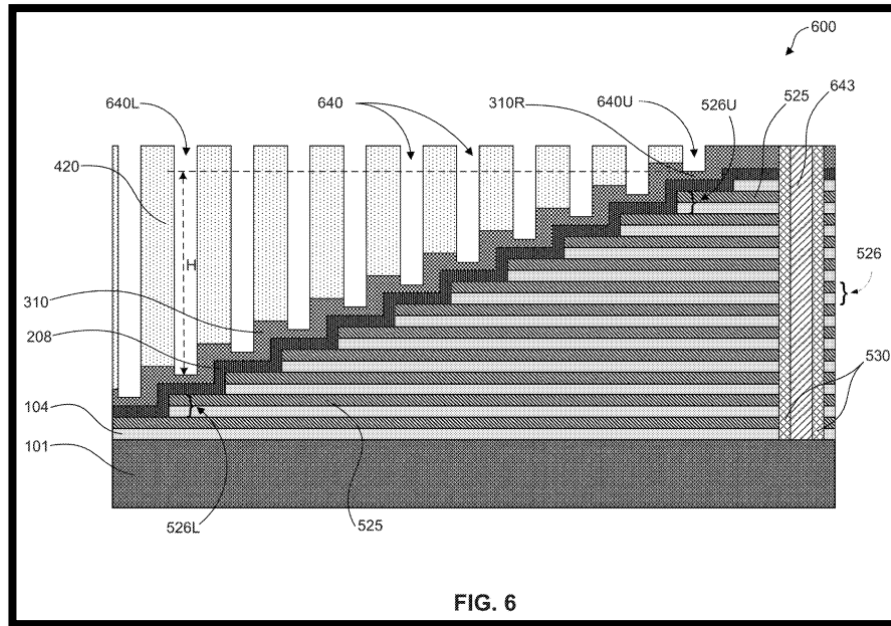
Key for Annotations of Figure 9A

29. The etch-stop layer 310 protects the underlying layers of the staircase structure 900 in the following way. In an earlier step, the third insulating layer 420 is formed on the staircase structure as shown in Figure 5A, below. *Id.* 8:26-30, Fig. 5A.



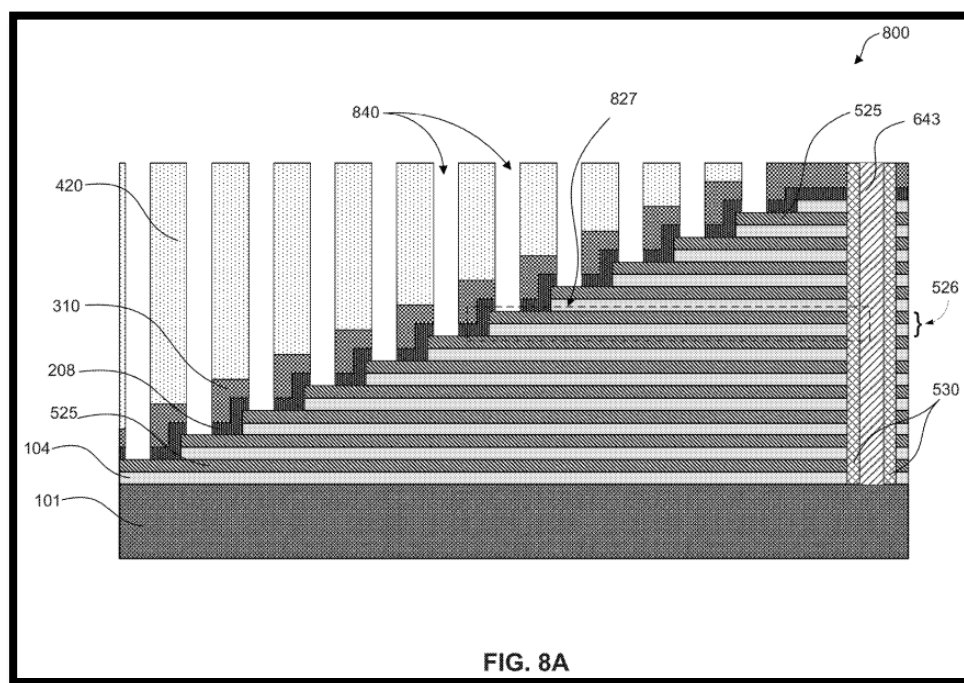
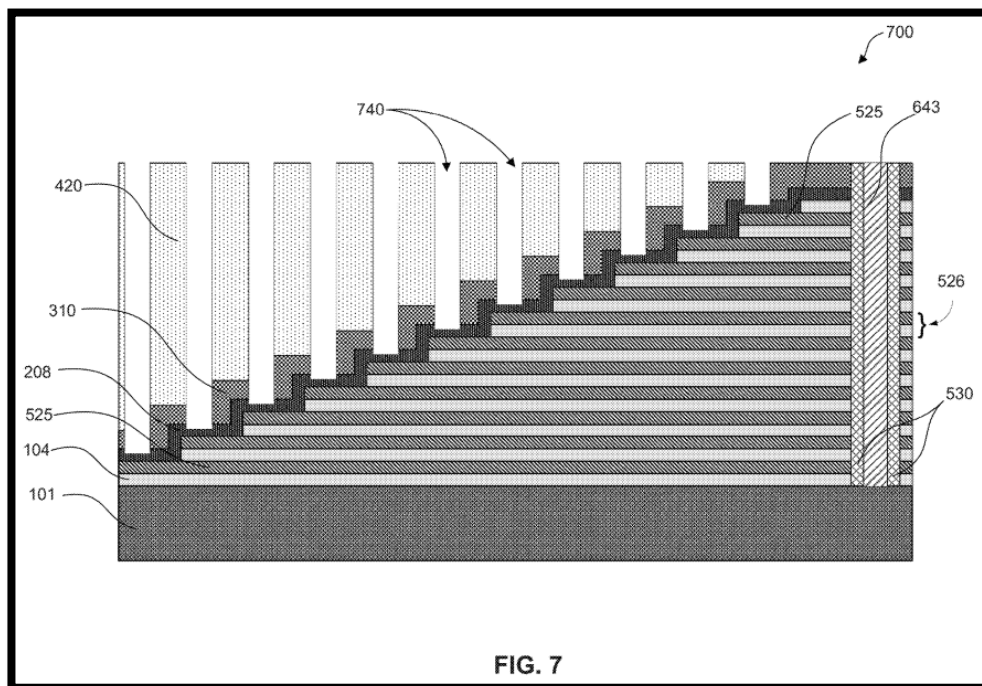
30. Subsequently, as illustrated in Figure 6, below, at least one etching process etches VIA openings 640, where the etch-stop layer 310 “protects the

underlying structure until all the VIA openings 640 are formed throughout the staircase structure 600.” *Id.* 10:2-5, Fig. 6.



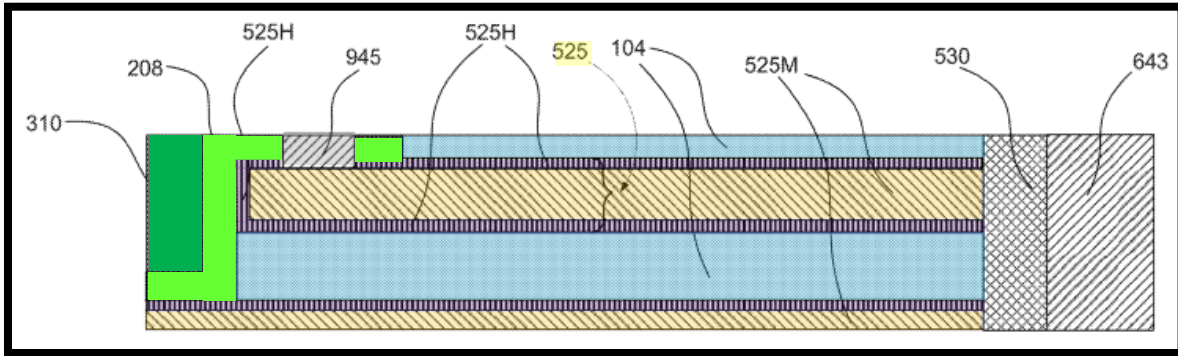
31. As shown in Figure 6, a VIA opening 640L for the lower levels requires a longer etching time than a VIA opening 640U for the upper levels to etch through thickness H of the third insulating material 420—distance from the top of the third insulating material 420 to the etch-stop layer 310. *Id.* 10:5-13. The etch-stop layer 310 protects the upper levels while the VIA openings 640 are formed at the stack lower levels. *Id.* 10:9-13; *see also id.* 10:13-33.

32. Then, as shown in Figures 7 and 8A, below, an etchant etches the etch-stop layer 310 and second insulating layer 208 to expose a gate stack layer 525M of gate stack 525. *Id.* 10:47-11:7, Figs. 7, 8A. This sequence is shown below.



33. Figure 9B, annotated below, shows details about the gate stack 525. The gate stack includes a high-k dielectric layer 525H (purple), which surrounds a gate conductive layer 525M (orange) with one side next to fifth insulating layer

530. *Id.* 9:4-10, 9:47-50. The VIA conductive structures 945 (grey) may be directly disposed on an exposed portion of gate conductive layer 525M. *Id.* 11:19-25.



'276 Patent, Figure 9B (annotated)

No.	Structure
104	First Insulating Layer
525H	High-k Dielectric Layer
525M	Gate Conductive Layer
208	Second Insulating Layer
310	Etch-Stop Layer
945	Vertical Interconnect Access Conductive Structures

Key for Annotation of Figure 9B

VI. Ground 1: Claims 1-2, 4-5, and 9-18 in view of Kim and the Knowledge of a POSITA

34. Claim 1 is the only independent claim in the '276 patent and recites, in part, "forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer" and "a plurality of steps" where "the forming of each step... comprises disposing a sacrificial layer over a dielectric layer." For the

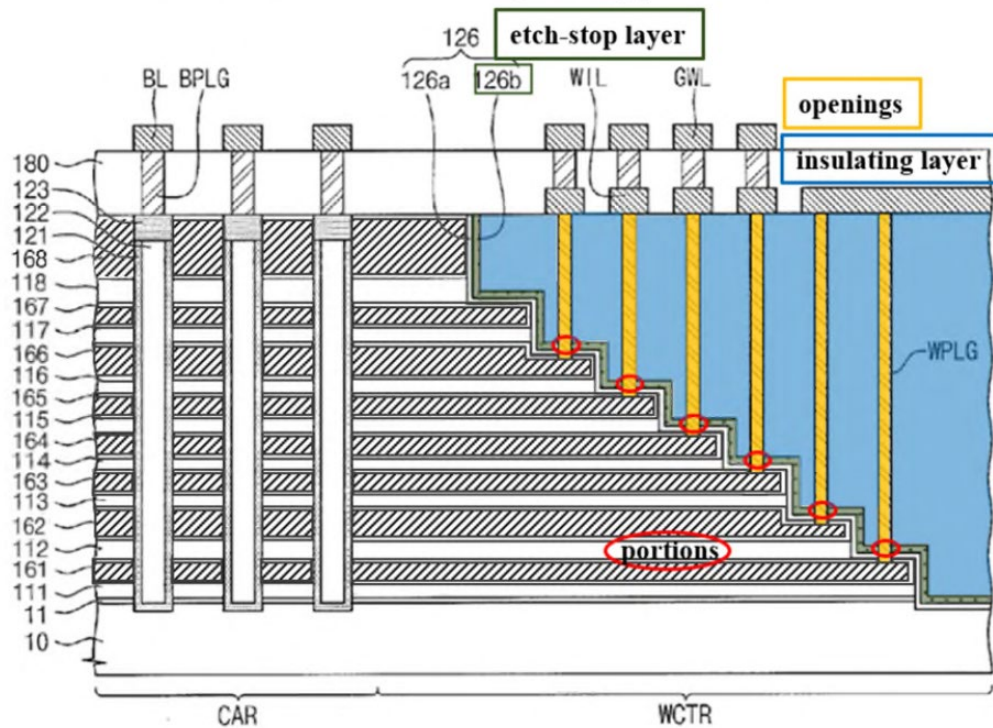
reasons below, it is my opinion that these limitations are not obvious in view of Kim and the knowledge of a POSITA.

A. Kim does not disclose “forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer”

35. Dr. Banerjee asserts that “Kim discloses” this limitation. Ex. 1003

¶102. Dr. Banerjee cites to Kim’s disclosure of forming of openings for word line contact plugs WPLG as disclosing this limitation, and asserts that forming these openings requires a two-step process including a first step where “the contact holes “penetrate the insulating exposing—but not penetrating—portions of the etch-stop layer.” Pet. 72-73. I disagree.

36. Kim does not disclose such a two-step process. And in particular, Kim does not disclose a step in forming the word line contact plugs WPLG where “portions of the etch-stop layer” are exposed but not penetrated. Dr. Banerjee’s annotation of Kim’s Figure 22A shows that Kim’s openings *do* penetrate the etch-stop layer rather than exposing a portion of it as shown by the red circles below.

Gate-Stack-on-Top Fig. 22A**Ex. 1003 ¶ 102 (annotating Kim Fig. 22A)**

37. Dr. Banerjee cites paragraph 173 of Kim, but that paragraph does not mention two steps for formation of these contact holes, but rather just discloses forming these contact holes. Kim [0173] (“[F]ormation of word line contact plugs WPLG... may include forming contact holes to penetrate the interlayer insulating pattern 134 in the word line contact region WCTR.”); see Ex. 1003 ¶ 102. As a result of this formation, the holes *penetrate*, rather than merely expose, the etch-stop layer so that “the word line contact plugs WPLG can be connected to the gate electrodes” which are below the etch stop layer. Kim [0173].

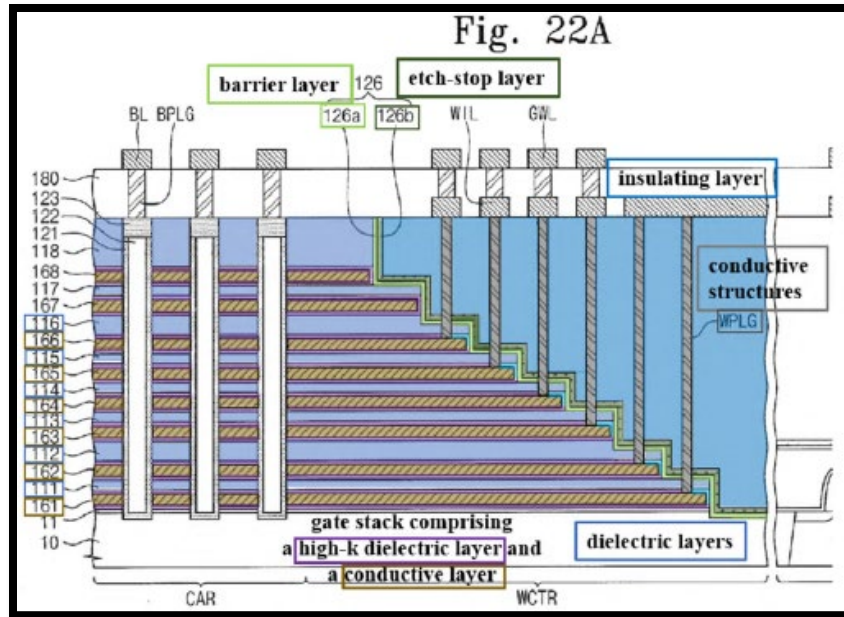
38. Dr. Banerjee asserts that “[a] POSITA would have recognized” the need for an extra step in contact hole formation due to Kim’s disclosure that the etch stop layer “may be formed of a material having an etch selectivity with respect to the interlayer dielectric 130.” Ex. 1003 ¶ 103 (quoting Kim [0213]). I disagree. A POSITA would have understood from this passage that Kim explicitly discloses when a two-step etching process was intended. Specifically, “etch selectivity” in this passage relates to two-step device planarizing in the cell-array region—not formation of contact holes. Kim [0213] (“[T]he interlayer dielectric 130 may be formed on the etch stop layer 125 and then planarized until a top surface of the etch stop layer 125 is exposed on the cell array region CAR.”). This is an entirely different process from forming word line contact plugs, and occurs in an entirely different part of the device (i.e., the cell array region) from the word line contact plugs (e.g., the contact region). The etch stop layer is an “etch stop” because it has etch selectivity with respect to the *planarization process* (in other words, it forms a stopping point for a first step of *planarization* in the cell array region)—not for contact hole formation for word line contact plugs. *See, e.g.*, Kim [0196] (“[E]tch stop layer 125... may be used as a planarization stopping point.”). This is a very commonly used technique when planarizing layers in most applications of semiconductor processing. The “etch selectivity” of the etch-stop layer for the planarization process does not

require or imply the same functionality (including etch selectivity) for hole formation, as selectivity depends on the “etch recipe” and Kim does not teach or suggest using the same “etch recipe” for these two distinct processes. *See* Kim [0132], [0141] (referring to “etch recipe[s] having an etch selectivity”). A POSITA therefore would not have understood this extra step to be implicit or inherent in Kim.

B. Kim does not disclose “the forming of each step ... comprises disposing a sacrificial layer over a dielectric layer”

39. Dr. Banerjee asserts that “[t]his Declaration relies on Kim’s Figure 17A-22B embodiment comprising an etch-stop layer and a barrier layer.” Ex. 1003 ¶ 80. This embodiment of Kim does not disclose that forming each step comprises disposing a sacrificial layer over a dielectric layer as recited in claim 1. To the contrary, as shown in Figure 22A (annotated below), this embodiment shows that each step comprises a gate stack¹ 161 to 168 (tan) disposed *below* a dielectric layer 111-118 (purple).

¹ For the purpose of this declaration, I have accepted for the sake of argument Dr. Banerjee’s assertion that the alleged gate stack replaces the sacrificial layer during the gate replacement process. Thus, I have assumed that the location of the gate stack in Figure 22A indicates the location of the sacrificial layer. Ex. 1003 ¶ 82.



Pet. 27 (annotating Kim Fig. 22A)

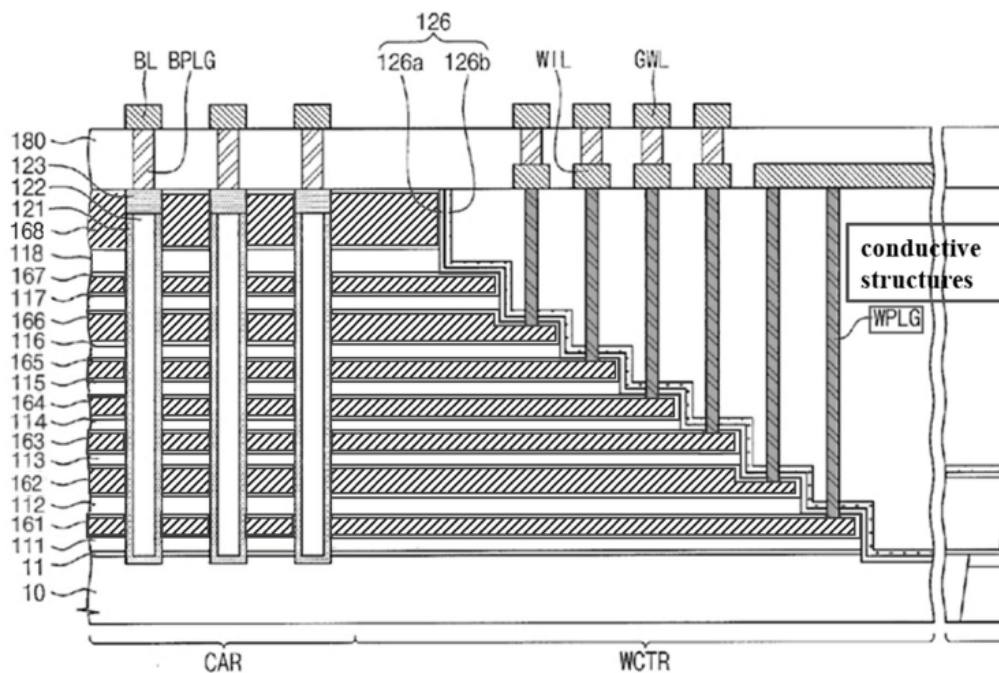
40. Dr. Banerjee acknowledges that Kim’s “figures show the opposite order” of the claims. Ex. 1003 ¶ 83; *see also* ¶ 70 (“Like Figure 22A..., Kim’s figures show embodiments in which a dielectric layer is disposed over a sacrificial layer/gate stack at each step.”). Dr. Banerjee further asserts that “[a] POSITA would have understood that [Kim’s] teaching of the gate-stack-on-top layer ordering applies to the Figure 17A-22B embodiment.” *Id.* ¶ 83. In that paragraph, Dr. Banerjee does not cite to any specific passage of Kim for support. I note that in a previous section, Dr. Banerjee cites to paragraph 90 of Kim, asserting that it describes “embodiments in which a sacrificial layer/gate stack is disposed over a dielectric layer at each step.” Ex. 1003 ¶ 70 (citing Kim [0090]). However, that

passage of Kim specifically relates to Figures 4, 8A, and 8B and not the Figure 17A-22B embodiment the Petition and Dr. Banerjee rely on. *See* Kim [0086].

C. Kim in view of a POSITA's knowledge does not render obvious "the forming of each step... comprises disposing a sacrificial layer over a dielectric layer"

41. Dr. Banerjee further opines that the recited limitation would have been obvious. Specifically, Dr. Banerjee redraws Figure 22A to illustrate what he admits is the "opposite" of what it actually discloses, labeling this new figure "Gate-Stack-On-Top Fig. 22A."

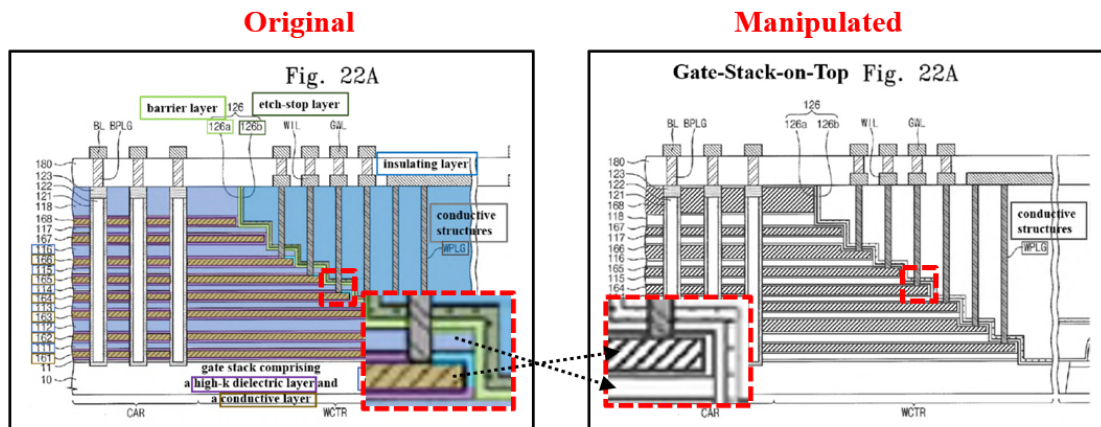
Gate-Stack-on-Top Fig. 22A



Ex. 1003 ¶ 106

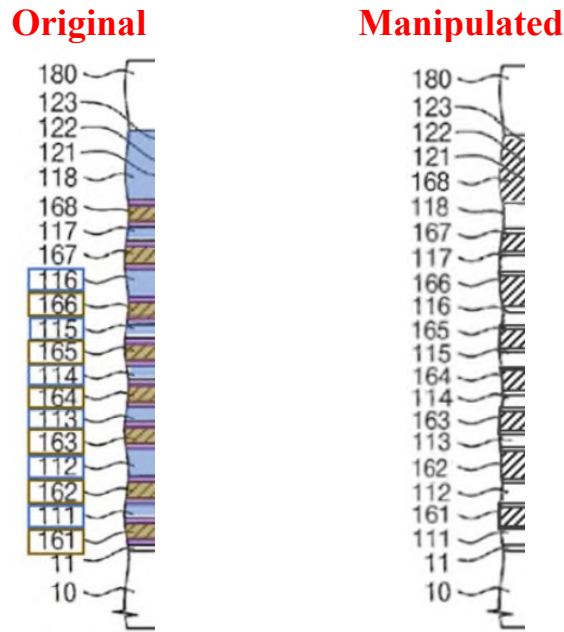
42. In redrawing Figure 22A, Dr. Banerjee changes the insulating layers of Figure 22A to be "gate stacks," and vice versa. As shown in the side-by-side

comparison of the original Fig. 22A (annotated) and Dr. Banerjee's modified Figure 22A, Dr. Banerjee also added hatching to the insulating layers of Figure 22A to make them appear as gate stacks, and removed hatching from the gate stacks of Figure 22A to make them appear as insulating layers.



Ex. 1003 ¶ 68 (left), ¶ 106 (right)

43. Dr. Banerjee also rennumbers labels of Fig. 22A, for example to change label “116” (corresponding to an insulating layer) to “166” (corresponding to a gate electrode) and vice versa.



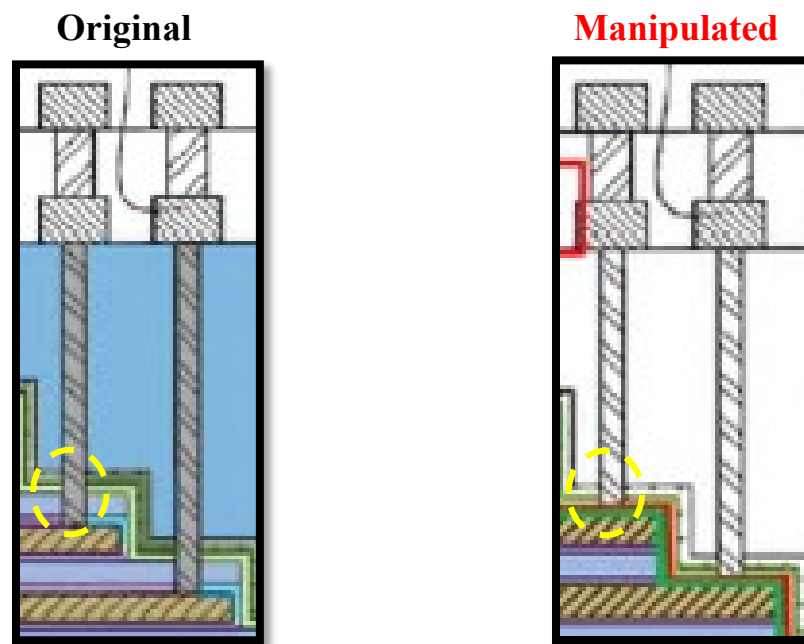
Ex. 1003 ¶68 (left) (excerpted), ¶90 (right) (excerpted).

44. It is my opinion that a POSITA would not have been motivated to modify Kim in the manner proposed by Dr. Banerjee, and would not have had a reasonable expectation of success in doing so.

45. Dr. Banerjee bases his opinion of obviousness on his redrawing of Figure 22A. Ex. 1003 ¶¶ 82-90. For example, Dr. Banerjee asserts that “the reverse layer ordering is compatible with the variations between Kim’s embodiments,” that “Kim’s teaching at least renders the... limitation obvious,” and that a POSITA would have been able to “visualiz[e] the reversed layer ordering.” *Id.* ¶ 83.

46. I disagree. Dr. Banerjee’s extensive modifications to Figure 22A show that the proposed modification—replacing a functional gate stack with insulating material and vice versa—would require extensive modifications to the

manufacturing process and the device's structure. Drawing a figure that moves structures around gives the illusion of simplicity. But the reality of such changes is extremely complicated, and Dr. Banerjee ignores it. For example, Dr. Banerjee's modified Figure 22A not only swaps the layers, but also shortens the contact plugs to terminate within gate electrode layers, as shown below. This is no trivial change to Kim's processes and devices. The switching may also change the etch selectivity between the insulating layer above the sacrificial layers SC1-8 and sacrificial layers themselves such that the first stop layer 126a or the second stop layer 126b is not needed—just like in the Alternative Figs. 4-15D embodiment. A POSITA would not use the stop pattern 126 if its function is not needed because a POSITA would not want to add the time or material to include a non-functional component.



47. Thus, Dr. Banerjee's proposed modification requires significant modification for the processes for forming word line contacts to penetrate through different materials at different depths. Dr. Banerjee makes this modification in the figure but does not address a POSITA's motivation or reasonable expectation of success in making these series of modifications to Figure 22A.

VII. Ground 3: Claims 1-15 in view of Han and Fang.

A. A POSITA would not have been motivated to modify Han to add “disposing an etch-stop layer on each step.”

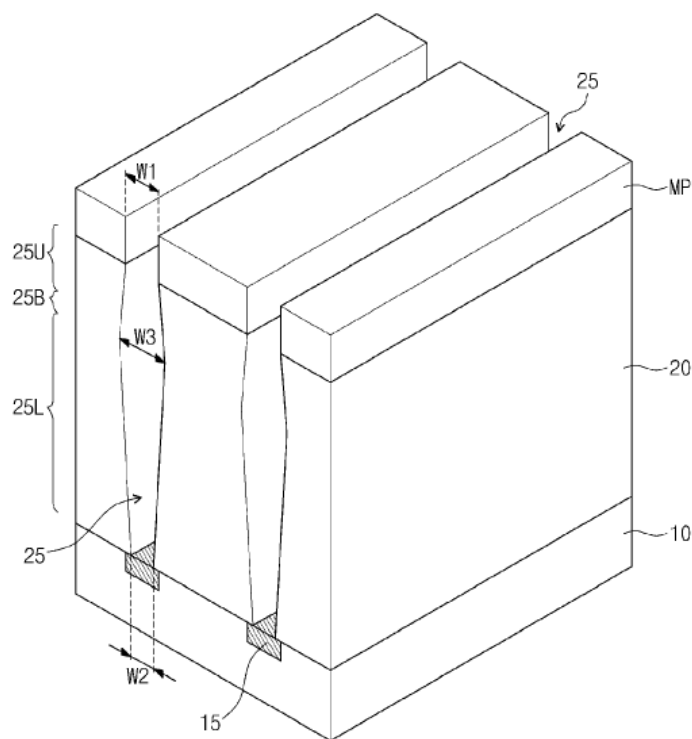
48. Claim 1 recites “disposing an etch-stop layer on each step.” In Ground 3, Dr. Banerjee proposes to “adapt Han's staircase structure by adding Fang's etch-stop layer.” Ex. 1003 ¶ 215. It is my opinion that a POSITA would not have been motivated to do so.

49. Dr. Banerjee cites to Fang's disclosure of “multiple masks” in the prior art as a solution to “punch-through” as requiring “additional processing acts, complexity, and cost to the overall process.” Ex. 1003 ¶ 215 (quoting Fang [0004]). Dr. Banerjee that “[a] POSITA would have recognized Han's method suffered from this exact problem.” Ex. 1003 ¶ 215. Dr. Banerjee does not explain this conclusion or cite to any portion of Han in support. *Id.*

50. I note that Han does not appear to use the term “multiple masks.” Although Han does disclose the use of a mask pattern, it does not disclose such use for forming openings in the contact region of the circuit—i.e., where the

punch-through problem would occur. For example, paragraph 41 of Han discloses a mask pattern used to etch opening 25 as shown below in Figure 1.

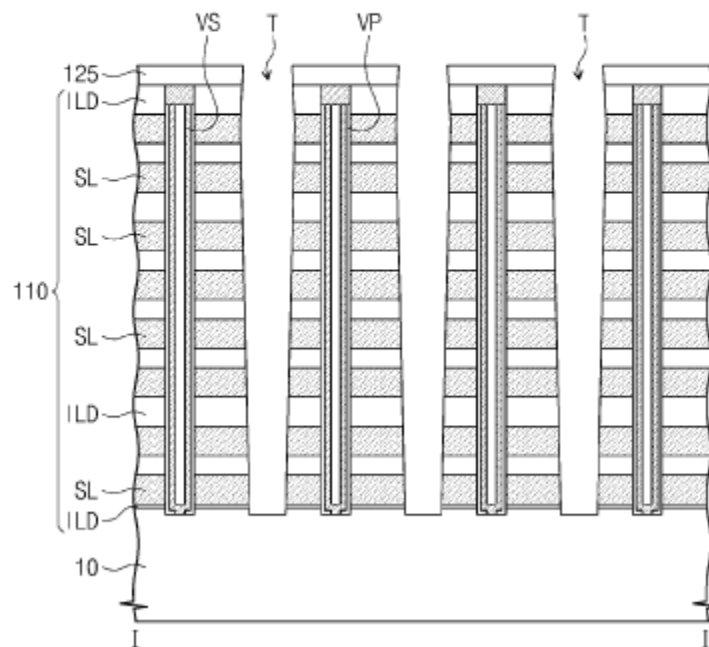
FIG. 1



Han Fig. 1

In paragraph 105, a mask pattern is used to etch the thin-layer structure 110, for example as shown in Figure 17, below.

FIG. 17

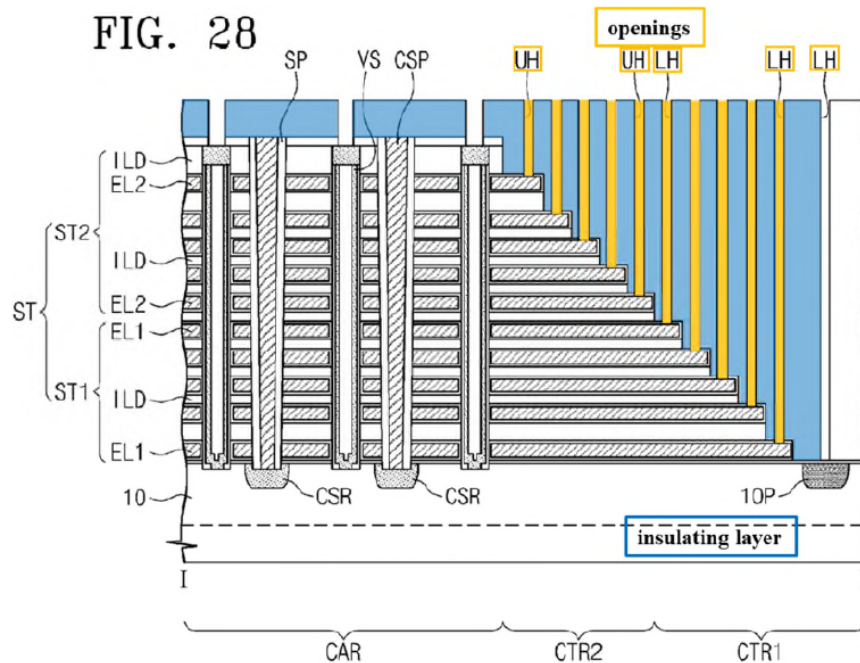


Han Fig. 17

And in paragraph 111, a mask pattern is used to form trenches T in Figure 17, above. These openings are not illustrated for a contact region of a circuit where punch-through would occur—indeed all of the openings above are shown as being of the same depth, rather than the different-depth openings that are used for the contact region.

51. Further, when discussing contact holes in the contact regions, Han discloses that they can all before formed using “[a]t least one patterning process”—e.g., a single patterning process. Han [0156]. As shown in Dr.

Banerjee's annotation of Han's Figure 26, below, Han includes upper holes UH and lower holes LH that are formed by "[a]t least one patterning process." Han [0156].



Ex. 1003 ¶ 174 (annotating Han Fig. 28)

52. Han does not suggest that “multiple masks” are required for this “[a]t least one patterning process.” Han [0156]. And although Han discloses that the upper holes “may be formed before the formation of the lower contact holes” in “some exemplary embodiments” (*id.*), there is no suggestion that the relative timing of forming these holes requires “multiple masks” or suffers from the “additional processing” problems Dr. Banerjee asserts are in Han. I also note that this passage describes forming these holes at different times as relating only to “some exemplary embodiments.” Han [0156]. A POSITA would not have

understood Han to have the “additional processing” problems that Fang describes and that Dr. Banerjee attributes to Han.

53. A POSITA have also not have viewed Fang as simpler or less costly than Han. Specifically, Han’s process of forming upper holes and lower holes does not require more “processing acts, complexity, and cost” than Fang’s system. As I described above, under Han’s approach for forming the contact holes (which is not the approach Fang disparages), holes can be formed in “[a]t least one patterning process” and in some embodiments, the upper holes can be formed before the lower holes using the same process. Han [0156]. Fang, however, requires an additional step, and a new process, of forming an etch stop material “over exposed horizontal and exposed vertical surfaces of the oxide materials 115 and nitride materials 120.” Fang [0020].

B. A POSITA would not have been motivated to combine Han and Fang.

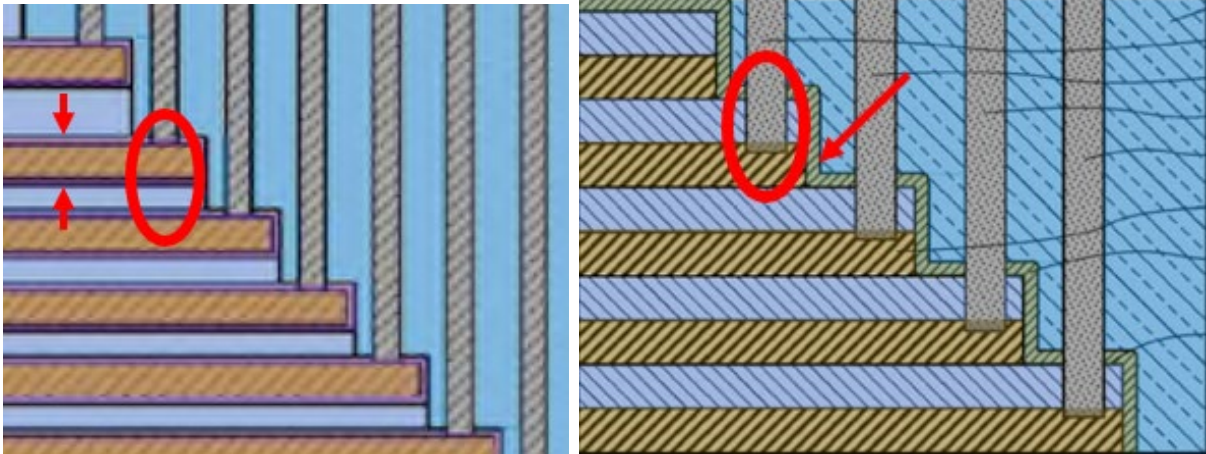
54. It is my opinion that a POSITA also would not have been motivated to combine Han and Fang generally because of the significant differences between the two references.

55. Han and Fang differ particularly in their staircase regions. As shown in the comparison below, Han and Fang differ in three significant ways: (1) they have different gate structures; (2) they have opposite stair step compositions; and (3) they have different layer configurations.

56. First, Han and Fang employ different gate structures. Han discloses what Dr. Banerjee calls a “gate stack” (or, at least, he maps it to the “gate stack” in claim 1), which includes a “horizontal insulating layer” that “cover[s] inner surfaces of the gate regions” and a conductive layer filling the remainder. Han [0118]-[0119]. This two-layer design is shown in annotated Figure 29, below left, between red arrows. Pet. 84. In contrast, Fang illustrates a simple conductive layer as shown highlighted in gold in Fang’s Figure 6, below right.

57. Second, Han and Fang employ opposite compositions for their respective stair steps. Specifically, as shown in the circled portions in both figures below, Han’s Figure 29 (left) discloses a stair step with the gate (gold) above the dielectric (lilac), and Fang’s Figure 6 (right) discloses a stair step with the gate (gold) below the dielectric (lilac).

58. Third, Han and Fang use different layer configurations for its staircase, and specifically, as shown by the red arrow added to Fang’s Figure 6 (right) below, Fang employs an etch stop layer completely absent in Han.

**Han Fig. 29 (cropped)****Fang Fig. 6**

59. Dr. Banerjee ignores these differences, which would have influenced a POSITA against combining Han and Fang. For example, Han's structure has no need for an etch stop layer because the structure uses a "horizontal insulating layer" as part of the gate, puts the gate on top of the stair, and includes "upper" and "lower" contact holes. As shown in the comparison above, Han's contact holes must penetrate the "horizontal insulating layer"—which is not an etch stop layer separate from a gate stack—and thus implicates different process considerations than Fang, which does not include a horizontal insulating layer.

60. Thus, it is my opinion that a POSITA would not have combined Han and Fang in the proposed manner.

VIII. CONCLUSION

All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. Further, I am aware that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001. I declare under penalty of perjury that the foregoing is true and correct.

Executed on April 29, 2025, in Arden Hills, Minnesota.

Stephen Campbell

Stephen Campbell