

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2025-00228
Patent 11,101,276 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

CYGAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

Micron Technology, Inc. (“Petitioner”) filed a Petition requesting an *inter partes* review of claims 1–18 of U.S. Patent No. 11,101,276 B2 (Ex. 1001, “the ’276 patent”). Paper 1 (“Pet.”). The Petition is supported by a Declaration from Dr. Sanjay Banerjee. Ex. 1003 (“Banerjee Declaration”). Yangtze Memory Technologies Company, Ltd. (“Patent Owner”) filed a Preliminary Response to the Petition, supported by a Declaration from Dr. Stephen Campbell. Paper 12 (“Prelim. Resp.”); Ex. 2006 (“Campbell Dec.”).

We have authority to determine whether to institute an *inter partes* review. *See* 35 U.S.C. § 314 (2018); 37 C.F.R. § 42.4(a) (2023). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted “unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” On June 25, 2025, Patent Owner’s Request for Discretionary Denial was denied. Paper 21. For the reasons discussed below, we determine that Petitioner establishes a reasonable likelihood of prevailing with respect to the unpatentability of at least one claim of the ’276 patent. Accordingly, we institute an *inter partes* review of claims 1–18 of the ’276 patent under all grounds presented in the Petition.

B. *Real Parties-in-Interest*

Petitioner identifies itself and its subsidiaries, including Micron Consumer Products Group LLC, as real parties-in-interest. Pet. 7. Patent Owner identifies itself as the real party-in-interest. Paper 5, 1.

C. Related Matters

The parties represent that the '276 patent is involved in *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023). Paper 5, 1; Pet. 7–8. Petitioner also filed IPRs challenging other patents asserted in the district court case. Pet. 8–9.

D. The '276 Patent

The '276 patent is titled “Word Line Contact Structure for Three-Dimensional Memory Devices and Fabrication Methods Thereof.” Ex. 1001, code (54). The '276 patent issued on August 24, 2021, from Application 16/865,056, as a division of Application No. 16/126,947, filed on September 10, 2018, now U.S. Patent No. 10,672,711, which is a continuation of PCT/CN/2018/101308, filed on August 20, 2018. *Id.* at codes (21), (22), (45). The '276 patent relates to a word line contact structure including a staircase structure having a conductor layer disposed over a dielectric layer, with a barrier layer disposed over a portion of the conductive layer on each step of the staircase, and an etch-stop layer disposed on the barrier layer. *Id.* at code (57).

E. Illustrative Claim

Claim 1 is illustrative, and recites as follows:¹

[1.PRE] A method for forming a semiconductor structure, comprising:

[1.A] forming a staircase structure comprising a plurality of steps, wherein the forming of each step of the plurality of steps comprises disposing a sacrificial layer over a dielectric layer;

¹ Bracketed organization added as per the Petition.

[1.B] disposing an etch-stop layer on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer;

[1.C] disposing an insulating layer on the etch-stop layer;

[1.D] replacing the sacrificial layer of each step with a gate stack, the gate stack comprising a conductive layer and a first high-k dielectric layer;

[1.E] forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer;

[1.F] etching the exposed portions of the etch -stop layer in the plurality of openings and exposing at least a portion of the conductive layer of each step, and

[1.G] forming a plurality of conductive structures in each of the plurality of openings.

Ex. 1001, 15:3–23.

F. Evidence

Petitioner relies on the following patent and non-patent document evidence:

Name	Document	Exhibit
Kim et al. “Kim” ²	US 2012/0070944 A1	1005
Fang et al. “Fang” ³	US 2019/0067306 A1	1006
Han et al. “Han” ⁴	US 2017/0062470 A1	1007
Chen ⁵	US 2017/0204384 A1	1008

² Petitioner asserts that Kim is prior art under 35 U.S.C. §§ 102(a)(1)-(a)(2) based on its March 22, 2012 publication date and the August 31, 2017 priority date of the ’276 patent. Pet. 11.

³ Petitioner asserts that Fang is prior art under 35 U.S.C. § 102(a)(2) based on its publication date of February 28, 2019. Pet. 12.

⁴ Petitioner asserts that Han is prior art under 35 U.S.C. §§ 102(a)(1)-(a)(2) based on its filing date of August 26, 2016 and its priority date of August 28, 2015. Pet. 12.

⁵ Petitioner asserts that Chen is prior art under 35 U.S.C. § 102(a)(2) based on its filing date of April 12, 2016 and its publication date of October 12, 2017. Pet. 12.

G. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–19 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2, 4, 5, 9–18	103 ⁶	Kim ⁷
1–18	103	Kim, Fang
1–15	103	Han, Fang
16, 17	103	Han, Fang, Chen

II. ANALYSIS

A. Legal Standards

A claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, “would have been obvious at the time the invention was made to a person having ordinary skill in the art [to which said subject matter pertains].” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level

⁶ We apply AIA 35 U.S.C. § 103 to the ’276 patent because it was filed after, and never claimed the benefit of an effective filing date before, March 16, 2013. Ex. 1001, codes (22), (63); Pet. 11.

⁷ Petitioner styles this ground and the Park ground as also being based on “a POSITA’s [Person of Ordinary Skill In The Art] knowledge.” Pet. 12. However, an *inter partes* review may be requested “only on the basis of prior art consisting of patents or printed publications,” although it may “rely on evidence beyond prior art documents.” 35 U.S.C. § 311(b); *Qualcomm Inc. v. Apple, Inc.*, 24 F.4th 1367, 1374–75 (Fed. Cir. 2022). Patent Owner does not raise a §311(b) challenge.

of ordinary skill in the art; and (4) objective evidence of non-obviousness.⁸
See Graham v. John Deere Co., 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art (“POSITA”) at the critical time “would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (*e.g.*, researching, designing, or teaching) monolithic 3D structures and NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience).” Pet. 26 (citing Ex. 1003 ¶42). Petitioner further asserts that a POSITA “would have been aware of and generally knowledgeable about 3D NAND’s structure, its component parts, how it operates, and how it is controlled.” *Id.* Patent Owner does not provide any such assessment in its Preliminary Response. Prelim. Resp. 7 (reserving the right to argue an alternative level if the Board institutes review). For purposes of this Decision, we adopt Petitioner’s proposed level of ordinary skill, as it appears to be consistent with the specification of the ’276 patent and the prior art of record.

C. Claim Construction

In an *inter partes* review, we construe a patent claim “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b).” 37 C.F.R. § 42.100(b). Under this standard, the words of a claim generally are given their “ordinary and customary meaning,” which is the meaning the term would have to a person

⁸ Neither party presents evidence or arguments regarding objective evidence of non-obviousness. Pet. 107–108; Prelim. Resp.

of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc).

Neither party proposes any express claim construction at this stage of the proceeding. Pet. 25; Prelim. Resp. 8. Based on the record before us, we determine that no claim term requires express construction for purposes of this Decision.

D. Obviousness over Kim

Petitioner asserts that claims 1, 2, 4, 5, and 9–18 are unpatentable under 35 U.S.C. §103 as obvious over Kim in view of the knowledge of a person of ordinary skill in the art. Pet. 31–64. Patent Owner argues against this assertion. Prelim. Resp. 8–27.

Upon consideration of Petitioner’s explanations and the totality of evidence in this current record, we are persuaded that Petitioner demonstrates a reasonable likelihood of prevailing in showing that at least one claim is unpatentable under 35 U.S.C. §103.

1. Kim

Kim is titled “Methods of Manufacturing Three Dimensional Semiconductor Devices.” Ex. 1005, code (54). Kim relates to providing a semiconductor substrate including a peripheral region and a cell array region, with a peripheral structure on the peripheral region and a cell structure in the cell array region that is thicker than the peripheral structure. *Id.* at code (57). Both structures are covered by an interlayer dielectric, on which is formed a polishing stop layer. *Id.* The interlayer dielectric is planarized using the polishing stop layer as a planarization stop. *Id.*

2. *Analysis of Claim 1*

We begin our analysis of Petitioner’s obviousness contentions with Petitioner’s assertions as to claim 1.

[1.PRE] A method for forming a semiconductor structure, comprising: [1.A] forming a staircase structure comprising a plurality of steps, wherein the forming of each step of the plurality of steps comprises disposing a sacrificial layer over a dielectric layer;

Patent Owner contests Petitioner’s assertion that Kim in view of the knowledge of the prior art teaches “disposing a sacrificial layer over a dielectric layer,” as set forth in limitation [1.A]. Prelim. Resp. 12.

To the extent the preamble [1.PRE] is limiting, Petitioner asserts that it is taught by Kim’s description of a 3D semiconductor device at successive stages of manufacturing. Pet. 35 (citing Ex. 1005, code (57), ¶ 183, Figs. 17A–22A). With respect to limitation [1.A], Petitioner asserts that Kim’s “stepwise stacked layer structure ST” teaches a staircase structure comprising a plurality of steps. *Id.* at 36–37 (citing Ex. 1005, Fig. 17A (bottom six steps), ¶¶ 7–8, 64; Ex. 1003 ¶¶ 89–91).

Petitioner further asserts that each of Kim’s steps comprises a sacrificial layer SC1–SC6 over an insulating dielectric layer 111–116. *Id.* at 35–36 (citing Ex. 1005 ¶¶ 64, 86; Ex. 1003 ¶¶ 89–90). Petitioner points to Kim’s description of two embodiments, one in which the sacrificial layer is the top surface and one in which the dielectric layer is the top surface. *Id.* at 27 (citing Ex. 1005 ¶¶ 90, 91, 240). Petitioner asserts that although Kim’s Figures show the lower steps having the insulating layer (e.g., 111) atop the sacrificial layer (e.g., SC1), the order would be reversed in the other embodiment to result in the claimed arrangement at each step. *Id.* at 36–37 (citing Ex. 1005, Fig. 17A; Ex. 1003 ¶¶ 89–90).

Patent Owner argues that Kim’s Figure 22A shows “[a gate stack] 161 to 168 (tan) disposed **below** a dielectric layer 111-118 (light purple)” rather than “disposing a sacrificial layer **over** a dielectric layer” as claimed.

Prelim. Resp. 12.

Petitioner’s assertions are supported by its assertions based upon Kim’s alternate embodiment, in which the bottom-most step has a lower dielectric layer 111 on which the gate stack 161 is disposed. *Compare* Ex. 1005, Fig. 22A (representing the embodiment of the dielectric layer at the top surface) with Pet. 37 (Petitioner’s altered Figure 17A representing the embodiment in which the dielectric layer is at the top surface). It is true that the gate stack 161 may also be below dielectric layer 112; however, Patent Owner’s alternate manner of viewing the arrangement of layers does not contradict Petitioner’s equally valid description based upon Kim’s dual embodiments. Petitioner sufficiently shows that Kim’s lower steps (or even a single step) teaches deposition of a sacrificial layer (e.g., SC1) over a dielectric layer (e.g., 111). Pet. 36–37. Consequently, we agree that Petitioner has sufficiently shown Kim to teach or suggest limitations [1.PRE]⁹ and [1.A].¹⁰

[1.B] disposing an etch-stop layer on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer; [1.C] disposing an insulating layer on the etch-stop layer; [1.D] replacing the sacrificial layer of each step with a gate

⁹ We do not express an opinion on whether the preamble is limiting.

¹⁰ Accordingly, we need not assess Patent Owner’s further arguments as to whether the knowledge in the prior art, or a combination of embodiments of Kim, teaches limitation [1.A]. Prelim. Resp. 12–26.

stack, the gate stack comprising a conductive layer and a first high-k dielectric layer;

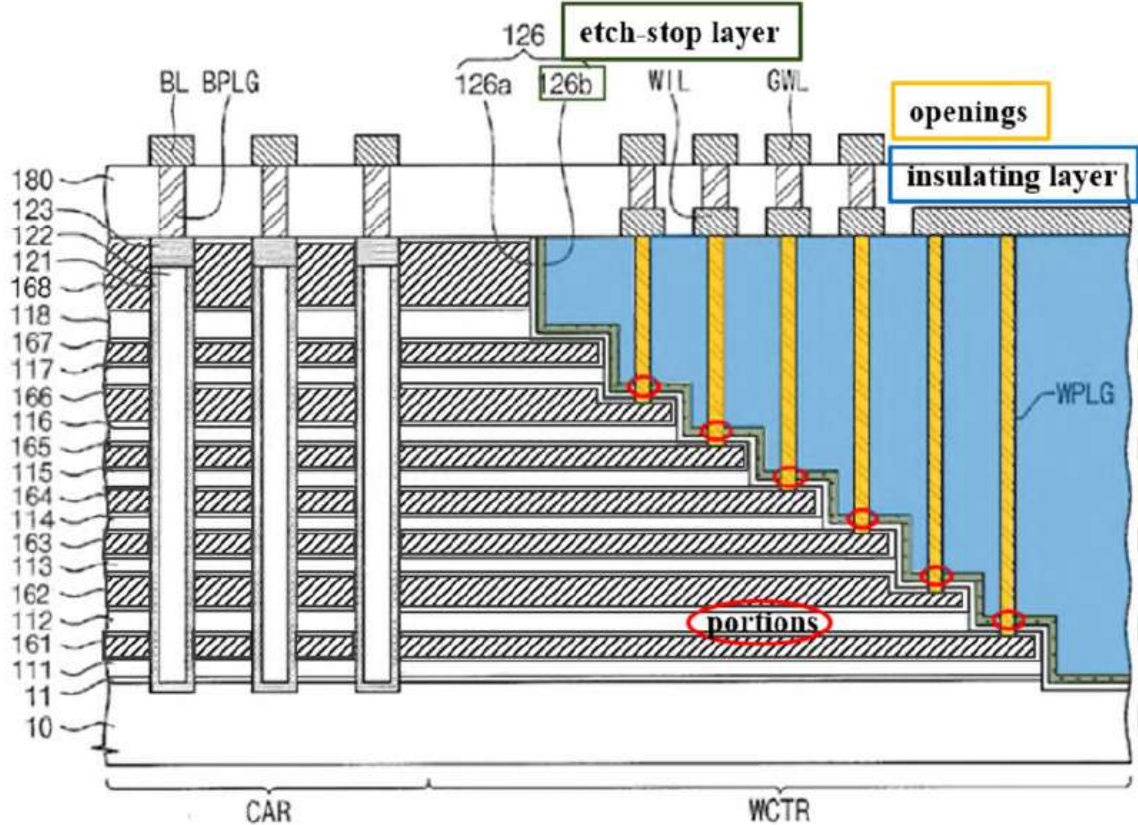
We determine that Petitioner has sufficiently shown Kim to teach uncontested limitations [1.B]–[1.D]. Petitioner has shown that Kim teaches first etch-stop layer 125a, second stop layer 125b (etch stop layer) comprised of high-k dielectric silicon nitride disposed on each step, and interlayer dielectric 130 (insulating layer) disposed on the etch stop layer. Pet. 39–42 (citing Ex. 1005, Figs. 17A, 18A, ¶¶ 94, 185–188, 213; Ex. 1003 ¶¶ 93–96). Petitioner has also shown that Kim teaches replacing the sacrificial layer (e.g., one of SC 1–6) with a gate stack comprising a conductive layer (e.g., one of corresponding gate electrodes 161–166) and a first high-k dielectric layer (data storing layer 150 including a “blocking insulating layer” made of aluminum oxide). *Id.* at 43–44 (citing Ex. 1005 ¶¶ 198–202, Figs. 20A, 21A, Ex. 1003 ¶¶ 97–99).

[1.E] forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer; [1.F] etching the exposed portions of the etch-stop layer in the plurality of openings and exposing at least a portion of the conductive layer of each step; [1.G] forming a plurality of conductive structures in each of the plurality of openings.

Patent Owner argues that Kim does not teach limitation [1.E]. Prelim. Resp. 45.

Petitioner asserts that Kim etches openings through insulating layer 130 to expose portions of the etch-stop layer 126b (which Petitioner asserts to be analogous to etch-stop layer 125b). Pet. 45–46 (citing Ex. 1005 ¶ 173; Ex. 1003 ¶ 102). Petitioner provides an annotated Figure 22A of Kim:

Gate-Stack-on-Top Fig. 22A



Id. at 45–46. Annotated Figure 22A of Kim shows openings (yellow) through insulating layer 130 (blue) extending through etch-stop layer 126b to gate electrodes 161–166. Ex. 1005, Fig. 22A, ¶¶ 185–86; Pet. 45–46. Petitioner asserts that Kim’s openings are “extended to the gate electrodes” and subsequently filled with conductive structures (word line contact plugs (“WPLGs”). Pet. 46–49 (citing Ex. 1005 ¶ 173; Ex. 1003 ¶102). Petitioner further asserts that the etch-stop layer has an etch selectivity that stops etching, i.e., by allowing the interlayer dielectric 130 to be etched away without penetrating the etch-stop layer. *Id.* at 47 (citing Ex. 1005 ¶ 213).

Patent Owner argues that “Kim does not disclose any method step in forming the word line contact plugs WPLG where ‘portions of the etch-stop layer’ are exposed but not penetrated.” Prelim. Resp. 9. Patent Owner

further argues that a person having ordinary skill in the art would not have applied a two-step etching process (exposure, then penetration of the etch-stop layer) to the insulating layer because Kim explicitly provides two-step etching for a different process, and not for forming the word line contact plugs. *Id.* at 10–11 (citing Ex. 2006 ¶ 38).

Patent Owner’s argument is unavailing. Claim 1 does not require different processes to expose and penetrate the etch-stop layer. Nor does claim 1 require that the etching of the etch-stop layer not begin until removal of the insulating layer is complete. Claim 1 may be taught by a single process of etching that first exposes, and through continued etching, then penetrates the etch-stop layer. Because Petitioner has shown etching to the surface of the etch-stop layer and further etching to penetrate the etch-stop layer to the conductive layer of each step, Petitioner has sufficiently shown Kim to teach limitations [1.E] and [1.F].

Additionally, Patent Owner argues that Kim describes the etch selectivity of its etch stop layer with respect to planarization of the dielectric, not for hole formation. Prelim. Resp. 11 (citing Ex. 2006 ¶ 38). Kim, however, describes its etch stop layer 125b as being formed of silicon nitride, the same material that Kim describes as “exhibiting a slower removal rate than the interlayer dielectric 130” during planarization. Ex. 1005 ¶¶ 187, 190.

3. *Claims 2, 4, 5, and 9–18*

Patent Owner does not separately contest the further limitations of challenged dependent claims 2, 4, 5, and 9–18. Prelim. Resp. 26–27. We have reviewed Petitioner’s assertions for these claims and determine that they are supported by the record. Pet. 50–64. Consequently, we determine

that Petitioner has shown a reasonable likelihood that it will prevail on its assertions for claims 1, 2, 4, 5, and 9–18 over Kim.

E. Obviousness over Kim and Fang

Patent Owner does not separately contest Petitioner’s reliance on Fang in its assertions that claims 1–18 would have been obvious over on the combined teachings of Kim and Fang. Prelim. Resp. 27. We have reviewed Petitioner’s assertions for these claims and determine that they are sufficiently supported by the record, including Petitioner’s reasons to combine Kim and Fang. Pet. 64–74. Consequently, we determine that Petitioner has shown a reasonable likelihood that it will prevail on its assertions for claims 1–18 over the combined teachings of Kim and Fang.

F. Obviousness over Han and Fang, or Han, Feng, and Chen

Because we determine Petitioner has made a sufficient showing for at least one claim under its Kim-based assertions, we need not evaluate Petitioner’s assertions based on Han and Fang (Pet. 74–103) or on Han, Feng, and Chen (Pet. 103–107). To the extent that this Decision provides guidance for the parties at trial, Patent Owner’s arguments focus on a lack of a reason to combine Han and Feng.

First, Patent Owner argues that Feng’s use of multiple masks, and any benefits accruing from such use, would not apply to Han’s use of a single patterning process that is not described as using multiple masks. Prelim. Resp. 28–31. However, Petitioner’s asserted benefits are based upon the ability of Fang’s etch-stop layer to prevent punch-through in Han’s system. Pet. 102. Petitioner does not suggest that an etch-stop only prevented punch-through as a replacement for multiple masks, only that Fang described etch-stop as a beneficial punch-through technique, with recognized benefits over other art-recognized techniques such as adjusting

etch chemistries and using multiple masks. *Id.* (citing Ex. 1007 ¶¶ 3–4, 26, 28). Moreover, as admitted by Patent Owner, Han has multiple embodiments, some using a single step of patterning and others using multiple patterning steps. Prelim. Resp. 30 (citing Ex. 1007 ¶ 156 (acknowledging that Han discloses that holes may be formed at different times in “some exemplary embodiments”)); Pet. 74.

Second, Patent Owner argues, “Han and Fang differ in three significant ways: (1) they have different gate structures; (2) they have opposite stair step compositions; and (3) they have different layer configurations.” Prelim. Resp. 31–32. Patent Owner argues that Han’s features such as a horizontal insulating layer as part of the gate, remove the need for an etch stop layer and implicates different process considerations than in Fang. *Id.* at 32–33. However, Petitioner relies on Fang’s minimization of punch-through as a reason (among others) to use an etch stop layer. Pet. 102 (citing Ex. 1007 ¶ 4). Patent Owner does not address at this stage of the proceeding whether such punch-through is moot due to Han’s horizontal insulating layer, and whether one having ordinary skill in the art would have not found it obvious to use Fang’s etch-stop layer as an alternative to Han’s horizontal insulating layer in combining their teachings. *See Honeywell International Inc. v. 3G Licensing, S.A.*, 124 F.4th 1345, 1355 (Fed. Cir. 2025) (stating that “obviousness ‘does not require that a particular combination be preferred, or the most desirable, combination described in the prior art to provide motivation for the current invention’”); *Intel Corp. v. PACT XPP Schweiz AG*, 81 F.4th 1373, 1381 (Fed. Cir. 2023) (finding motivation where a second reference provides a “‘suitable option’ to replace” a feature in a first reference).

III. CONCLUSION

Based on the arguments in the Petition and the Preliminary Response, and the evidence of record, we determine that Petitioner establishes a reasonable likelihood that it will prevail on its challenge to at least one claim of the '276 patent. Our determination at this stage of the proceeding is based on the evidentiary record currently before us. This decision to institute trial is not a final decision as to patentability of any claim for which an *inter partes* review has been instituted. Our final decision will be based on the full record developed during trial.

Accordingly, we institute an *inter partes* review of all the challenged claims on all the challenged grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2, 4, 5, 9–18	103	Kim
1–18	103	Kim, Fang
1–15	103	Han, Fang
16, 17	103	Han, Fang, Chen

IV. ORDER

For the foregoing reasons, it is:

ORDERED that an *inter partes* review is instituted with respect to all of the grounds asserted in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which shall commence on the entry date of this Decision.

IPR2025-00228
Patent 11,101,276 B2

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