

1 UNITED STATES PATENT AND TRADEMARK OFFICE
2 BEFORE THE PATENT TRIAL AND APPEAL BOARD

3 Case No. IPR2025-00228

4 Patent 11,101,276

5 MICRON TECHNOLOGY, INC.,

6 Petitioner,

7 -vs-

8 YANGTZE MEMORY TECHNOLOGIES
9 COMPANY, LTD.,

10 Patent Owner.
_____ /

11
12 DEPOSITION OF
13 SANJAY BANERJEE, PH.D.

14 Thursday, October 2, 2025
15 10:01 a.m. - 11:40 a.m.

16 Remote Location
17 Via Zoom Videoconference
18 All Parties Remote

19 Stenographically reported by:
20 Erica Field, RDR, CRR, CA-CSR, TX-CSR, GA-CSR,
21 WA-CSR, NM-CCR, IL-CSR, NJ-CCR, FL-FPR, OR-CSR, NY
22 Notary, FL Notary,
23 AK Notary, DC Notary
24 Job No. 601323
25

1 REALTIME STENOGRAPHIC DEPOSITION of SANJAY
2 BANERJEE, PH.D., taken in the above-entitled matter
3 before ERICA FIELD, RDR, CRR, California
4 Certified Shorthand Reporter (License No.
5 14515), Texas Certified Shorthand Reporter
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15 5338-8044-2296-7296), Florida Professional
16 Reporter (License No. 1109), New York Notary,
17 Florida Notary, Alaska Notary, DC Notary taken
18 via remote videoconference on Thursday,
19 October 2, 2025, commencing at 10:01 a.m.

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EXHIBIT	EXHIBITS DESCRIPTION	PAGE
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Exhibit 1003	Declaration of Sanjay Banerjee, Ph.D., in Support of Petition For Inter Partes Review of U.S. Patent No. 11,101,276	34
Exhibit 1005	U.S. Patent Application Publication Number 2012/0070944 A1	37
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1 Thereupon,
2 the proceedings began at 10:01 a.m.:

3 DOC TECH: Thank you to everyone for
4 attending this proceeding remotely which we
5 anticipate will run smoothly. Please remember
6 to speak slowly and do your best not to talk
7 over one another.

8 Please be aware that we're recording this
9 proceeding for backup purposes. Any
10 off-the-record discussions should be had away
11 from the computer. Please remember to mute
12 your mic for those conversations.

13 Please have your video enabled to help the
14 reporter identify who is speaking. If you're
15 unable to connect with video and are
16 connecting via phone, please identify yourself
17 each time before speaking.

18 We'll provide a complimentary, unedited
19 recording of this deposition with a purchase
20 of the transcript. I apologize in advance for
21 any technical-related interruptions. Thank
22 you.

23 Whereupon,

24 SANJAY BANERJEE, PH.D.,
25 having been first duly sworn or affirmed, was

1 examined and testified as follows:

2 DIRECT EXAMINATION

3 BY MR. GRABOWSKI:

4 Q Dr. Banerjee, as you may recall from when
5 we did this a few months ago, my name is
6 Alex Grabowski. I'm from Latham here on behalf of
7 the patent owner. If you wouldn't mind just
8 starting off by stating your name and business
9 address for the record, please.

10 A Sanjay Banerjee, University of Texas at
11 Austin. Just so you know, I have unmarked copies
12 of my declaration, the '276 Patent, and portions
13 of the four main prior art that was cited with me.
14 So I can move them if you want me to.

15 Q No, that's fine to have them. I'm sure
16 we'll get them marked over the course of the dep.
17 But thanks for letting me know.

18 I know from the last time we spoke, you
19 have been deposed before, but I will still go over
20 the ground rules quickly just so we're all on the
21 same page.

22 I'm going to ask you questions and you're
23 going to give me answers. Is that all right?

24 A Yes.

25 Q I ask that you give verbal answers only

1 rather than nodding or shaking your head so that
2 the court reporter can take it down. Is that
3 okay?

4 A Yes.

5 Q For that same reason, I would ask that we
6 try not to talk over each other, and I will do the
7 same so we get a clear recording from the
8 transcript, if that's all right?

9 A Yes.

10 Q If you don't understand any of my
11 questions, please feel free to ask for
12 clarifications. Otherwise, I will assume you
13 understood it. Is that fair?

14 A Yes.

15 Q You understand that your lawyer may make
16 objections from time to time, but that unless he
17 instructs you not to answer, you will still have
18 to answer the question?

19 A Yes.

20 Q You will have an opportunity to take
21 breaks. We'll try to do one about every hour. If
22 you need a break, feel free to just ask for one.
23 The only thing I ask is that if there's a question
24 pending, you answer it before we go on the break.
25 Is that all right?

1 A Yes.

2 Q All right. And then just a couple of
3 questions that I have to ask everyone.

4 Are there any medications you are taking
5 today that would impact your ability to give
6 complete, truthful, and accurate testimony?

7 A No.

8 Q Are there any other reasons you cannot
9 give complete, accurate, and truthful testimony
10 today?

11 A No.

12 Q All right. And then because this is a
13 remote deposition, I just have a few other
14 questions about how you're set up.

15 Is there anyone else in the room with you?

16 A No.

17 Q Other than the papers you mentioned
18 before, do you have any notes in front of you?

19 A No.

20 Q The declaration, the patent, the prior
21 art, are those all clean copies of those?

22 A Yes.

23 Q Other than the computer you have in front
24 of you connected to the Zoom, do you have any
25 other computers, phones, tablets, devices in front

1 of you?

2 A I have my cell phone. It's on mute.

3 Q Okay. And I would just ask that you
4 refrain from messaging with anyone over the course
5 of deposition while we're on the record, if that's
6 all right?

7 A Of course.

8 Q And then other than the Zoom to connect
9 here, are you -- are there any other applications
10 open on your computer?

11 A No.

12 Q Perfect. All right. What --

13 A I have my e-mail open. So I can close
14 that if you want me to.

15 Q Yes, please. Thank you.

16 All right. What did you do to prepare for
17 your deposition today?

18 A I reviewed my declaration, the
19 '276 Patent, and I did prior art, but I focused
20 mostly on the four main prior art: Kim, Fang,
21 Han, and Chen. I also met briefly with counsel.

22 Q How many times did you meet with counsel?

23 A Twice.

24 Q When were those meetings?

25 A I met earlier this week for about an hour

1 to maybe an hour and a half. And then I met
2 briefly last week for, I think, maybe half an hour
3 to an hour.

4 Q And who was present at those meetings?

5 A Mr. Hsu.

6 Q Anyone else?

7 A No.

8 Q Did you speak to any non-attorneys about
9 your deposition today?

10 A No.

11 Q When were you first contacted about this
12 petition?

13 A It's been a while. Let me look at the
14 date of my -- I'm looking at my declaration, and I
15 signed it on the 29th of November 2024. So I
16 suspect I started working on this maybe six months
17 before that perhaps, but I don't remember exactly.

18 Q And who wrote your declaration for the
19 IPR?

20 A It's my report. These opinions are mine,
21 but as you know, you write this collaboratively
22 with counsel.

23 Q About how many hours did you spend working
24 on your declaration, if you know?

25 A I don't recall exactly, but I suspect

1 maybe 20 to 40 hours. It didn't take quite as
2 long, because, as you know, there's a very similar
3 patent, '711, so you sort of amortize the time
4 between the two in some sense.

5 Q Makes sense. You mentioned four primary
6 references -- or excuse me, four main references
7 earlier: Kim, Han, Fang, and Chen. Is that
8 right?

9 A Yes.

10 Q Were those references you found or were
11 they provided to you by counsel?

12 A I don't recall exactly, but I believe
13 these were provided by counsel. I think I found
14 some of the other references that we cited.

15 Q And I know I asked this question about
16 preparation for your deposition. Did you talk to
17 any non-lawyers during the preparation of your
18 declaration?

19 A No.

20 MR. GRABOWSKI: Okay. Then I think with
21 that, we can start marking exhibits. Can we
22 please have the '276 Patent, that's
23 Exhibit 1001.

24 DOC TECH: Please stand by. It is in the
25 chat.

1 (Exhibit 1001 was marked for
2 identification.)

3 DOC TECH: It should be on the screen.

4 BY MR. GRABOWSKI:

5 Q Can you see it all right, Dr. Banerjee, or
6 would it help to make it a little bigger?

7 A I can see it. I can see it.

8 Q Perfect. Okay. You recognize
9 Exhibit 1001 as U.S. Patent Number 11,101,276
10 that's at issue in this IPR proceeding?

11 A Yes.

12 Q And if I refer to it as the '276 Patent,
13 you will understand what I mean by that?

14 A Yes.

15 Q All right. The '276 Patent generally
16 discusses three-dimensional memory devices and
17 fabrication methods for the same, right?

18 A Yes.

19 Q As part of these fabrication methods,
20 various etching steps are performed, right?

21 A Yes.

22 Q Can you just give me a high-level
23 explanation of how an etching process works?

24 A Sure. So when you build chips, including
25 memory chips, it involves deposition of different

1 kinds of layers, such as insulators, conductors,
2 semiconductors, and these can be deposited by
3 various techniques, as discussed in the patent.

4 And then you'll pattern then. Those steps
5 are known as lithography. And using those
6 patterns, you etch unwanted regions of the flumes
7 that are deposited or grown and, generally
8 speaking, that's what's meant by etching.

9 In broad terms, etching can be done using
10 wet chemical etches or dry plasma-based etches.
11 For making complex geometries, it's preferable to
12 use dry etches if you want very high degree of
13 anisotropy. But if you want a high degree of
14 selectivity, very often, wet etches are used.

15 Q And from a technical standpoint, what's
16 the difference between a wet etch and a dry etch?

17 A A wet etch will use liquids, such as
18 different kinds of acids perhaps, while a dry etch
19 will involve flowing in appropriate gases into a
20 reactor and then you strike a plasma.

21 And then there's different flavors of dry
22 etches. But the most common one is something
23 called reactive-ion etching, where you
24 disassociate the gases that flow in, create a
25 plasma, and you get an etch which is partly

1 physical in nature because of iron bombardment of
2 the surface. And that's what gives the etch the
3 anisotropy.

4 The term "anisotropy," as you know, means
5 you etch primarily in the vertical direction and
6 not that much in the lateral direction. But then
7 you also have radicals or molecular fragments that
8 are created in the plasma that provides a chemical
9 component to the etch, which is generally not that
10 anisotropic, but it's more selective than a
11 physical component of the etch.

12 Q So the etching process occurs at the
13 exposed surface; is that right?

14 A In broad sense, yes, but we have to look
15 at the context. So very often, the parts that you
16 don't want to etch might be covered by
17 photoresist, and then you only etch through the
18 windows in the photoresist. But in other
19 structures, it may be covered by other materials.
20 And we have openings in those materials and would
21 be etching through the windows. So you have to
22 give more context to answer precisely. But in
23 broad sense, you're correct.

24 Q Okay. So you're not necessarily etching
25 every exposed surface at the same time, but you

1 have to expose the surface before you can etch it;
2 is that fair?

3 A It may not be etching every exposed
4 surface at the same time because different regions
5 may be made up of different materials, and the
6 etches, as I mentioned, can be selective to
7 certain materials versus others. So it could etch
8 certain regions that were, quote/unquote, exposed,
9 but not the other regions.

10 Q But I guess the question I'm trying to ask
11 is you can't etch a region that hasn't been
12 exposed to the surface; is that fair?

13 A Yeah, you can't etch a region that's not
14 exposed to the etchant.

15 Q And are you familiar with the concept of
16 an etch-stop layer?

17 A Yes.

18 Q What's your understanding of an etch-stop
19 layer?

20 A The etch-stop layer is used to have better
21 control over unintentional overetching of certain
22 layers. So the layers that I'm trying to etch
23 might be covered with a thin layer of a different
24 material which will have a slower etch rate than
25 the underlying layer that I'm ultimately trying to

1 etch.

2 So you choose a chemistry, the etchant
3 chemistry such that when I'm etching the layers
4 above the etch-stop layer, you etch the layers
5 above the etch-stop layer very, very fast. But
6 then once the etchant reaches the etch-stop layer,
7 the etch rate will slow down dramatically. And
8 the ratio of the two etch rates is what's called
9 "etch selectivity," and then it can switch the
10 etching gas in some cases.

11 But now the etch-stop layer will etch
12 faster than the layer underneath. So this gives
13 the insurance policy for about not overetching the
14 layers underneath the etch-stop layer which I'm
15 trying to protect.

16 Q Okay. So the purpose of the etch-stop
17 layer is to protect the layer beneath it from
18 being overetched; is that right?

19 A Once again, it may depend on the context,
20 but in general sense, yes.

21 Q All right. And holding the material of
22 any given etch-stop layer constant, a thicker
23 etch-stop layer is going to provide more
24 protection than a thinner etch-stop layer, right?

25 MR. HSU: Objection. Form.

1 A Yes. I mean, if you get everything about
2 the etching rate the same in terms of the etch
3 chemistry, its parameters, and only thing that was
4 changed was the thickness of the etch-stop layer,
5 it will require a lot longer time to
6 unintentionally etch to the etch-stop layer. In
7 that sense, a thicker etch-stop layer will provide
8 more of an insurance policy, if you will.

9 BY MR. GRABOWSKI:

10 Q And it's possible to use multiple
11 etch-stop layers; is that right?

12 A Yes.

13 Q And in general, if you're using thicker
14 etch-stop layers, does that mean you're going to
15 be using fewer layers than if you're using more
16 thin layers?

17 MR. HSU: Objection. Incomplete
18 hypothetical.

19 A And that very much depends on the context
20 because if you have two different etch-stop layers
21 in a certain etch chemistry, in general, they'll
22 have different etch rates.

23 So you may etch through the first -- the
24 top etch-stop layer, and then once it reaches the
25 lower etch-stop layer, presumably the etch rate

1 would slow down dramatically, so you have a
2 selectivity between the top and the lower
3 etch-stop layers. And then you switch on the
4 chemistry, then you figure out the lower etch-stop
5 layer.

6 By contrast, if you just have a single
7 etch-stop layer, you're stuck with a certain etch
8 rate, unintentional etch rate of the etch-stop
9 layer, so then thickness becomes the main
10 parameter that you can control in terms of how
11 long it would take to go through the etch-stop
12 layer. But you have to give me more specific
13 details to answer this.

14 BY MR. GRABOWSKI:

15 Q Could we go to Claim 1 of the '276 Patent?
16 It's the final PDF page.

17 And, Dr. Banerjee, am I correct that
18 Claim 1 of the '276 Patent describes a method for
19 forming a semiconductor structure?

20 A Yes.

21 Q And the method involves first forming a
22 staircase structure with a plurality of steps; is
23 that right?

24 A Yeah, that's the first claim element.

25 Q And each step of the staircase structure

1 has a sacrificial layer over a dielectric layer;
2 is that right?

3 A I see that.

4 Q So what that means is you first form a
5 dielectric layer and then you form a sacrificial
6 layer on top of it; is that right?

7 MR. HSU: Objection to form.

8 A Well, you deposit a dielectric --
9 sacrificial layer over a dielectric layer, but
10 then you continue the sequence so you don't have
11 just one pair. You've a plurality of them.

12 So the next step in the sequence would be
13 you deposit a dielectric layer over the
14 sacrificial layer and so on and so forth, right.

15 BY MR. GRABOWSKI:

16 Q Okay. Perfect. That's actually where I
17 was going next. So there's a plurality of these
18 sacrificial layers, dielectric layer pairs,
19 stacked on top of each other like a staircase; is
20 that right?

21 A When they first do the deposition, they'll
22 just form the stack. It's not going to be a
23 staircase to begin with. You have to do this etch
24 stream -- etch trim processes, to make a staircase
25 out of the stack.

1 Q Okay. So you form the stack of these
2 sacrificial layer, dielectric layer pairs, and
3 then you do the etch-trim process to make that
4 stack into a staircase; is that right?

5 A Yes.

6 Q And how many of these sacrificial,
7 dielectric layer pairs could be stacked on top of
8 each other? Dozens?

9 A Well, the number of those pairs would
10 correspond to the number of memory cells you want
11 in a NAND memory string. So -- and that number
12 keeps going up every year. So -- maybe every
13 other year. So I haven't kept up with the latest
14 products on the market, but I believe it's on the
15 order of 512 or 256. Pretty large numbers.

16 Q Okay. So fair to say you could have
17 hundreds of pairs of these layers?

18 A In the most advanced NAND, 3D NAND, yes.

19 Q Okay. And once it's been etched into a
20 staircase, the surface of the steps has an
21 etch-stop layer deposited over them; is that
22 right?

23 MR. HSU: Objection. Form.

24 A I mean, that's the next claim element of
25 independent Claim 1, the disposing an etch-stop

1 layer on each step of the plurality of steps.

2 BY MR. GRABOWSKI:

3 Q And then on top of that etch-stop layer,
4 there's an insulating layer deposited?

5 A Yes, that's the next claim element.

6 Q Going back to the sacrificial layer, it's
7 a sacrificial layer because eventually it gets
8 removed, right?

9 A Yes.

10 Q And when it's removed, that leaves a
11 cavity that's later filled by conductive materials
12 to form the gate stack, right?

13 A Well, the cavity gets filled with the
14 first high-k dielectric layer and then the
15 conductive layer which is going to be the wordline
16 metal.

17 Q And the wordline and the high-k,
18 collectively, form the gate stack; is that right?

19 A Yes, that's very often the term that's
20 used.

21 Q And that's the term that's used in
22 Claim 1, right?

23 A Yes.

24 Q How is the sacrificial layer removed?

25 A Well, you want etch chemistry that's going

1 to be selective with respect to the dielectric
2 layers in the stack. So what one does is,
3 generally speaking -- I mean, you could do that,
4 in principle, with a wet chemistry also because
5 here anisotropy is not really required.

6 But in general, people prefer to use dry
7 plasma-based processes because, you know, the
8 trend in the industry -- in general -- I mean,
9 there's always pathological counter-examples. In
10 general, if you have large volumes of wet acids
11 that are used, you have to dispose of them. In
12 typical fabs, that's an environmental hazard.
13 Plus, with wet acids, you etch out the cavities
14 and then ultimately to dry them. That creates all
15 kinds of manufacturing problems. You get collapse
16 of these cantilever structures and things like
17 that because of capillary forces.

18 I don't know exactly what different
19 companies necessarily use, and, in principle, both
20 could be used, wet and dry. But I believe dry is
21 the preferred option in most cases. But I haven't
22 researched that in a lot of detail.

23 Q Assuming it is a more common dry-etch
24 process, the way that would work is the
25 sacrificial material is exposed to gases that

1 break it down. Is that a fair description?

2 A Yeah, the sacrificial layer -- first of
3 all, you have to create this opening in the
4 substrate. That is in one of the later claims.
5 In Claim 13, the dependent Claim 13 mentioned
6 that.

7 Anyway, you create an opening and then you
8 laterally etch out the sacrificial layers. And
9 assuming you're doing a dry etch, the reactant
10 gases will react with the material of the
11 sacrificial layer radiating from that silicon
12 nitride and create gaseous byproducts which will
13 then escape. That's how you create the cavity.

14 Q When you say "escape," those gaseous
15 byproducts will flow out that opening you were
16 talking about; is that right?

17 A Yes.

18 Q And once they flow out, that leaves an
19 open cavity where the sacrificial layer used to
20 be, right?

21 A Yeah, after you're done with the etch of
22 the sacrificial layers.

23 Q Now, am I right that the thinner you can
24 make these layers of the staircase, the more steps
25 the device can have and the more capacity the

1 memory can have in the same physical space?

2 A Not necessarily. In a sense that you're
3 not constrained to a certain maximum thickness
4 when you make these memory cells because if you
5 keep the relative scales in mind, the starting
6 silicon substrate is in the order -- it's going to
7 be on the order of 6-, 700 microns, and the layers
8 that you add collectively may only be a few tens
9 of microns.

10 So in terms of the overall scheme of
11 things, 90 percent of overall thickness of the
12 chip is the starting silicon wafer thickness. And
13 you're not limited to a certain maximum thickness.
14 I don't think that's the right way of looking at
15 it.

16 What you have to worry about is how long
17 does it take to deposit those layers, and what are
18 the electrical ramifications. And by that, I mean
19 we have horizontal wordlines, and if the oxide in
20 between is very, very thin, you may get
21 unintentional wordline coupling --

22 (Reporter clarification.)

23 A Coupling capacitances.

24 BY MR. GRABOWSKI:

25 Q Okay. So if you make the sacrificial

1 layer and, thus, the later gate stack layer too
2 thin, that can cause problems? Is that fair to
3 say?

4 A If you make the sacrificial layer too
5 thin, then the wordline thickness will be very
6 thin. And that, in turn, will increase the
7 wordline resistance, and that will slow down the
8 chip. Because these wordlines basically work as
9 transmission lines, if you will. When you apply
10 the wordline voltages, those signals have to
11 propagate laterally to the vertical memory
12 strength. So a very thin sacrificial layer would
13 imply a very thin wordline thickness, a high
14 wordline resistance, larger RC time constant, and
15 a slower chip.

16 I was talking earlier about the thickness
17 of the oxide layers. If you made that too thin,
18 adjacent wordlines would be closed, and then the
19 coupling capacitance would be high and you'd get
20 crossed up.

21 Q I just want to make sure I understand. By
22 "wordlines," you're referring to the conductive
23 portion of what the patent refers to as "gate
24 stacks"; is that right?

25 A That's correct.

1 Q Okay. Are there manufacturing issues that
2 can arise if the sacrificial layer is made too
3 thin?

4 A Sure. I mean, generally, the thinner the
5 better in the sense that it's going to take less
6 time, you're going to consume less chemicals.

7 But the problem is when you do these
8 deposition, you'll always have manufacturing
9 variabilities in the way of thicknesses or
10 uniformity of the thickness across the wafer and
11 things like that.

12 So if you try to make it too thin, in
13 addition to the problems of these parasitic
14 coupling capacitance that I mentioned, you could
15 have situations where in certain regions maybe the
16 layer wasn't even completely formed. We have thin
17 holes, for example. And that would be
18 catastrophic because that would then mean you have
19 a short-circuit between adjacent wordlines.

20 So in general, you do want to make it
21 thin. But if you push your luck too much, you can
22 have other problems.

23 Q Understood. Is one of those problems that
24 the gaseous byproducts of the sacrificial layer
25 etch process may not be able to fully escape?

1 A That's certainly a possibility, yes.

2 Q I think you also mentioned this in the
3 process of the wet etch. I think you described it
4 as a capillary collapse. Did I hear that
5 correctly?

6 A Yes.

7 Q Can you explain a little more about what
8 that is?

9 A Right. So if you're using wet etches
10 using some sort of acid that's going to go into
11 those cavities as the sacrificial layers are being
12 etched off. But then ultimately, of course, you
13 have to get rid of those wet acids, and that -- as
14 the liquids are retracting, you have surface
15 tension forces between the liquid and the two
16 solid cantilevered surfaces. And those surface
17 tension forces can very often cause these
18 cantilevered horizontal structures to collapse
19 towards each other. And that's a well-known
20 problem in something called MEMS technology. It's
21 a problem called stiction. Okay? Where you have
22 basically electrostatic forces and capillary
23 forces which cause the stiction.

24 (Reporter clarification.)

25 A It's not gravity. Gravity is irrelevant

1 because the structures are so light.

2 My apologies.

3 BY MR. GRABOWSKI:

4 Q Is -- if you make the sacrificial layer
5 too thin, and you're using a dry etch process, is
6 there still a point where cavity collapse becomes
7 a risk?

8 A It could. It could. But I think it would
9 be less of an issue than with wet etches.

10 Q All right. You mentioned another problem
11 might be that the layer doesn't fully form and
12 could have pinholes. Do you mean that the
13 conductive material may not fully fill the cavity?

14 A I think you're talking about the insulator
15 in the stack. So if the insulator did not fully
16 form and you had gaps in that, that's what I meant
17 by a pinhole, and then the conductor above and
18 below that pinhole might get shorted out.

19 Q Got it. Okay. If your cavity that's left
20 by the sacrificial layer is too thin, is there a
21 risk you can't completely fill it with conductive
22 material?

23 A Yes, that's also a possibility. And if
24 you did not fill it up completely, and you had
25 voids, that would also be catastrophic. It could

1 lead to an open circuit or a very high wordline
2 resistance.

3 Q Are you familiar with the term
4 "punch-through" in the context of memory cell
5 manufacturing?

6 A Yes.

7 Q What's your understanding of the term
8 "punch-through"?

9 A So after you have made these staircase
10 structure and refilled the sacrificial layer with
11 the wordline, the gate stack of the wordline, and
12 all these are separated by insulators, you
13 ultimately have to -- and then you fill the rest
14 of the staircase with what's called -- I think we
15 call it the third insulator layer. Let me
16 double-check. Well, they deposit an insulator to
17 fill up the cavity in the staircase. And you
18 planarize it, and then you have to punch vertical
19 holes in that insulator and refill that with a
20 conductor. And you have a plurality of these
21 vertical conductors connected to these horizontal
22 wordlines because ultimately you have to access
23 them on the top surface of the memory chip.

24 So when I'm etching these vertical holes
25 in the insulator, if I'm not careful, it might

1 punch through or etch through the intended
2 horizontal layer in the stack and then etch right
3 through the next layer perhaps. So that when I
4 refill that cavity with a conductive material, the
5 vertical conductors, that might cause shorting
6 between two horizontal wordlines.

7 Q Got it. And so punch-through is something
8 undesirable and to be avoided, right?

9 A Yes.

10 Q The risk that punch-through occurs is
11 going to be greater the thinner the layer gets,
12 right?

13 MR. HSU: Objection. Form.

14 A You may have to give me more specific
15 details. You may be using different types of etch
16 stops and things like that.

17 BY MR. GRABOWSKI:

18 Q Fair. Holding the composition of the
19 staircase and the etch chemistry and parameters
20 constant, and the only thing that varies is the
21 thickness of the layers, you're going to be at
22 more risk of punch-through the thinner the layer
23 gets, right?

24 A Yeah. And, hypothetically, if you kept
25 every other parameter constant and you only reduce

1 the thickness, punch-through is more likely to
2 happen.

3 Q Okay. Are there techniques for mitigating
4 the risk of punch-through?

5 A Yes.

6 Q What are those techniques?

7 A Well, the etch-stop layers that we are
8 talking about would be one example.

9 Q And I guess I should clarify this
10 question. The -- as of the priority date of these
11 patents, what techniques would have been available
12 to mitigate?

13 MR. HSU: Objection. Form.

14 A Well, we have cited several pieces of
15 prior art, which, in my opinion, invalidate the
16 '276 Patent, and several of those disclose various
17 types of etch-stop layers, single etch stops, or
18 two etch stops, and that's a classic way of
19 mitigating the punch-through problem.

20 BY MR. GRABOWSKI:

21 Q Are there any other ways in that time
22 period that would have been known to mitigate the
23 punch-through problem?

24 A I haven't looked into that, but
25 hypothetically, one could choose an etch process

1 which is very, very slow, and one could choose the
2 thicknesses of these insulators and these
3 sacrificial layers to be quite thick. So it takes
4 a long time to etch through one of those stacks,
5 and that would then give you enough safety margin
6 where you would not have a punch-through problem.

7 But then the down side would be the time
8 required for manufacturing would go up, and that
9 would not be a desirable pathway.

10 So the only thing that I'm aware of in
11 that time frame is to use -- not the only thing.
12 One of the main ways is to use etch-stop layers.

13 There could be other ways also. You could
14 use multiple masks and things like that to etch
15 the shallow region separately from the deeper
16 regions. But etch-stop layers are a very elegant
17 way of solving the punch-through problem.

18 Q Other than multiple masks and etch stops
19 and altering the thickness, are there any other
20 ways you're aware of as that period to mitigate
21 the risk of punch-through?

22 A I can't think of any, sitting here.

23 Q Would using a high-k dielectric around the
24 wordline contact as part of the gate stop mitigate
25 the risk of punch-through?

1 MR. HSU: Objection. Form.

2 A If you have a high-k dielectric, that
3 could, in some cases, serve the role of an
4 etch-stop layer because, as I've told you, the way
5 an etch-stop layer works is it has a slower etch
6 rate than the layers above.

7 And if you had a high-k dielectric
8 composition which is different from the insulator
9 used to fill up the opening in the staircase, very
10 often that's going to be silicon dioxide, the
11 high-k dielectric itself could serve the role of
12 an etch-stop layer.

13 BY MR. GRABOWSKI:

14 Q So if you had a high-k dielectric layer as
15 part of what the patent refers to as a gate stack,
16 that would be a sort of belt-and-suspenders
17 approach with an etch stop over the top of it; is
18 that fair?

19 MR. HSU: Objection. Form.

20 A I mean, it could serve the role of an
21 etch-stop layer, absent other etch-stop layers.
22 However, the caveat is no etch stop is going to
23 have zero unintentional etch rate. Meaning that
24 you never have infinite etch selectivity between
25 the etch-stop layer and the layers above.

1 So you need a certain minimum thickness of
2 the etch-stop layer typically to serve the
3 function of an etch stop. The high-k dielectric
4 and the gate stack may not necessarily be thick
5 enough because there's other requirements in terms
6 of the thickness of high-k dielectric.
7 Specifically, you want a good coupling capacitance
8 between the wordline and the memory cells.

9 So while the high-k dielectric and the
10 gate stack may serve the role of an etch-stop
11 layer, in some cases, it may not be thick enough
12 to be an adequate etch-stop layer. But absent
13 other etch-stop layers, that could be a poor man's
14 solution to the punch-through problem.

15 MR. GRABOWSKI: All right. Could we have
16 the Banerjee Decl (EX1003).

17 (Exhibit 1003 was marked for
18 identification.)

19 DOC TECH: It is also in the chat.

20 BY MR. GRABOWSKI:

21 Q Dr. Banerjee, do you recognize
22 Exhibit 1003 here?

23 A Yes.

24 Q All right. And this is the declaration
25 you submitted in connection with this IPR

1 proceeding, right?

2 A Yes.

3 Q This declaration contains your complete
4 opinions regarding the '276 Patent; is that fair?

5 A Yes, it does, but if you look at
6 Paragraph 228 of my declaration, I state that I
7 did not become aware of any secondary
8 considerations. If YMTC prefers any such
9 evidence, I shall provide my opinions on such
10 evidence in a reply declaration. So I reserve the
11 right to add to my declaration, if necessary.

12 Q Understood. As you sit here today, are
13 you aware of any mistakes in this declaration?

14 A I did see a few typos, but nothing
15 substantive.

16 Q So why don't we walk through those typos
17 just to make sure, if you happen to know them.

18 A So, I think, in one place referred to some
19 of these dependent claims as independent claims.
20 That was an obvious typo. I can't remember where
21 that was. I think I referred to Claims 13 and 14
22 as independent claims. It should be dependent
23 claims. But I can't remember exactly. So that's
24 one thing I remember reading through the
25 declaration last night.

1 Q All right. And any other typos you're
2 aware of?

3 A I can't think of any.

4 Q Do you have an understanding of the term
5 "obviousness" in the context of patent law?

6 A I have a layman's understanding.

7 Q What is your layman's understanding of
8 obviousness in the context of patent law?

9 A As I described in Paragraph 25 on in my
10 report, the patent is going to be obvious if the
11 subject matter of the claim as a whole would have
12 been obvious under 103 to a person of ordinary
13 skill in the art at the time of the invention.

14 I mean, I can read through the paragraphs
15 if you want me to. But my understanding of
16 obviousness as explained to me by my counsel is
17 described in Paragraphs 25 through 38.

18 But at a very high level, if all the claim
19 elements are not disclosed by a single piece of
20 prior art, you have to invoke obviousness. But if
21 it's all disclosed by a single piece of prior art,
22 that's anticipation one or two. That's my
23 non-lawyer's understanding.

24 Q All right. And your opinion relates to
25 four grounds of invalidity; is that correct?

1 A Yes.

2 Q And it's your understanding that all four
3 of those grounds are based on obviousness; is that
4 right?

5 A Yes.

6 Q You mentioned the term "anticipation" just
7 a moment ago. Did I hear that correctly?

8 A Yes.

9 Q And it sounded like you have at least a
10 lay understanding of the concept of anticipation;
11 is that fair?

12 A Yes.

13 Q You don't offer any opinion in your
14 declaration that any of the claims of the
15 '276 Patent are anticipated, right?

16 A No, I do not.

17 MR. GRABOWSKI: Could we pull up Kim 1005,
18 please?

19 (Exhibit 1005 was marked for
20 identification.)

21 BY MR. GRABOWSKI:

22 Q Can you see that, Dr. Banerjee?

23 A Yes.

24 Q And do you recognize Exhibit 1005?

25 A Yes.

1 Q Exhibit 1005 is the Kim reference you
2 relied on in forming some of your opinions in this
3 case?

4 A Yes.

5 Q It's your opinion that Kim discloses a
6 plurality of steps, correct?

7 A Yes.

8 Q And, further, it's your opinion that Kim
9 discloses having each step comprise a gate stack
10 disposed over a dielectric layer, correct?

11 A Yes.

12 Q Could we please take a look at Kim
13 Figure 22A? It's on PDF Page 39. Figure 22A is
14 one of the figures showing the embodiment from Kim
15 that you relied on for your opinions on
16 obviousness in Grounds 1 and 2, correct?

17 A Yes.

18 Q Kim's Figure 22A shows a staircase
19 structure for a 3D semiconductor memory device,
20 right?

21 A Yes.

22 Q The staircase shown in Kim's Figure 22A
23 has a series of alternating insulating layers and
24 gate stack layers, right?

25 A Yes.

1 Q And each one of those pairs of insulating
2 layers and gate stack layers makes up a step of
3 the staircase; is that right?

4 A Yes.

5 Q There's no dispute that the actual
6 Figure 22A as it appears in Kim shows the gate
7 stack layers on the bottom of each step, correct?

8 A That's correct. But if I read the
9 specifications of Kim, it clearly describes the
10 alternative stacking arrangement that the gate
11 stack would be on top of the insulator.

12 Q Understood. And you prepared a modified
13 version of Figure 22A showing a reversed order
14 with the gate stacks on top, correct?

15 A Yes.

16 Q And that appears at Page 76 of your
17 declaration, for instance?

18 A Yes.

19 Q And versions of this gate stack on top
20 Figure 22A appear in several places throughout
21 your report, right?

22 A Yes.

23 Q Am I correct that they're all the same
24 underlying figure except that you have annotated
25 them differently in different places?

1 A I think so.

2 MR. GRABOWSKI: Could we please pull up
3 Dr. Banerjee's declaration from the '711 case.
4 It's the file name "Exhibit 1003 Banerjee."
5 They're unfortunately the same exhibit number
6 in two different proceedings, so we will only
7 be using this briefly.

8 Could we scroll down just a little to see
9 the patent number at issue? This is the other
10 1003. The file name is "Ex. 1003 Banerjee."
11 There we go.

12 BY MR. GRABOWSKI:

13 Q And, Dr. Banerjee, you recognize this as
14 your declaration from other IPR concerning
15 U.S. Patent Number 10,672,711?

16 A Yes.

17 Q And you recall I deposed you about this
18 declaration a few months ago?

19 A Yes.

20 Q Could we look at Page 72 of this
21 declaration from the '711 proceeding?

22 Do you see the gate stack on top
23 Figure 22A there?

24 A Yes.

25 Q Other than the annotations, can you just

1 confirm for me that this is the same gate stack on
2 top Figure 22A that appears in your declaration in
3 the '276 proceeding?

4 A I believe so.

5 Q Okay.

6 MR. GRABOWSKI: Then we can take down the
7 '711 declaration. Thank you.

8 BY MR. GRABOWSKI:

9 Q All right. Dr. Banerjee, are you familiar
10 with the term "planarization"?

11 A Yes.

12 Q What does planarization mean?

13 A As you build up structures in an
14 integrated circuit through the steps of deposition
15 of different kinds of layers, patterning using
16 lithography and etching, you get non-planar
17 surfaces. You get a topography with hills and
18 valleys, and then as you proceed with the
19 fabrication, these hills and valleys in the
20 underlying layers can create problems. And we
21 talk about some of those in my report.

22 So as you proceed, you periodically want
23 to make the top surface flat or horizontal.
24 That's what planarization refers to.

25 Q Are there any techniques that are

1 typically used to perform planarization? And,
2 again, I'm speaking as of the priority date of the
3 '276 Patent.

4 A Yes. I mean, I teach this in my undergrad
5 class. So there are different techniques, but the
6 one that's most popular these days is called
7 chemical-mechanical polishing.

8 Q You mentioned there were other techniques
9 as well. Can you tell me what those are?

10 A Yes. So we could deposit oxide layers,
11 and these oxides will be heavily chemically doped
12 with boron and phosphorus. These are known as
13 BPSG. And when you dope them chemically with
14 boron and phosphorus, these oxides can reflow at a
15 lower temperature.

16 So oxides are a funny kind of a solid.
17 They're not true solids. They're so-called glassy
18 materials. Higher the temperature, lower the
19 viscosity. And with boron and phosphorus,
20 chemical doping of these oxides, the viscosity
21 drops. So as you heat it up, the oxide can reflow
22 and planarize it.

23 Another technique prior to CMP was to
24 deposit resist. Where the idea of this resist is
25 not to do patterning, but the resist liquid fills

1 up these cavities, then you do the resist etch
2 back. And that was another way that was used to
3 do planarization.

4 Q So the use of a resist is a form of
5 etching to do planarization; is that right?

6 A So the resist is liquid, and when you
7 cover the surface of a wafer which has these hills
8 and valleys, the top layer may be an oxide having
9 these hills and valleys. You spin on the resist,
10 and the resist will fill up the valleys.

11 And then you use an etch chemistry, which
12 will etch the photoresist that I've spun on as
13 well as the top oxide layer which makes up the
14 hills and valleys. So when you do the so-called
15 resist etch back, it will etch back the
16 photoresist as well as these oxides more or less
17 at the same rate. So as a result, you can get rid
18 of the hills in this oxide layer underneath the
19 full resist.

20 Q Okay. So you can use etching as a form of
21 planarization; is that right?

22 MR. HSU: Objection. Form.

23 A Yeah, you can use etching with a chemistry
24 which has a similar etch rate of the topmost oxide
25 layer. And resist that was used in this resist

1 etch back process. So this resist is not used for
2 patterning. It's to help planarize the structure.
3 These were all the techniques most of them have
4 been supplanted by chemical-mechanical polishing.

5 BY MR. GRABOWSKI:

6 Q So I think we mentioned etching. We
7 mentioned CMP. You mentioned the use of oxides.
8 Are there any other planarization techniques that
9 you're familiar with as of the priority date of
10 the '276?

11 A I can't think of any, sitting here.

12 Q All right. Let's start with
13 chemical-mechanical polishing. I know you said
14 you taught this to undergrads. Can you just give
15 an explanation of, like, an undergrad level of
16 what chemical-mechanical polishing is?

17 A Sure. So as the term states, this
18 polishing is partly chemical in nature and partly
19 mechanical in nature. And what you do is you
20 place the wafer which has these hills and valleys
21 facedown on the surface of a platen which has
22 bristles on it, kind of like a toothbrush.

23 And then you add a slurry which has
24 these -- it's got some etch chemistry, very often
25 a basic solution with a high pH, and mixed in with

1 that, you will have a grit, very often silicon
2 dioxide particles. And what you do is you move
3 the wafer across this brush in the CMP tool, which
4 also has a slurry, and the main result is these
5 protrusions on the wafer get ground down faster
6 and they get etched down faster than the
7 non-protruding parts of the wafer. That's how you
8 end up getting planarization.

9 Q And can you explain how -- first ask,
10 I guess, the baseline question. Strike that.

11 CMP is a different process than etching,
12 correct?

13 A I mean, if you use the term "etching" as a
14 removal process, CMP also does remove material.
15 But when I was using the term "etching" before in
16 the context of resist etch-back, I was talking
17 about more of a plasma-based etch chemistry which
18 should have similar etch rates of the resist and
19 the oxide at the topmost layer of the structure.

20 CMP also does involve removal through
21 chemical and mechanical etching in some sense, but
22 we call that polishing in this particular context.

23 Q Okay. So CMP and etching both remove
24 material, but they do it in a different manner; is
25 that fair?

1 A Yeah, in a broad sense, that's fair.

2 Q How do they differ in the way they remove
3 material?

4 A In the case of etching, as I mentioned, it
5 involves chemical reactions between the etchant
6 gas and the material that I'm trying to etch. And
7 you choose a process where the etch byproducts are
8 volatile so that it can be pumped out of the etch
9 reactor.

10 In CMP, on the other hand, you grind down
11 the regions that stick out, partly mechanically
12 using this -- these colloidal -- colloidal
13 suspension of various oxide particles, but then
14 you also etch these protrusions faster using the
15 chemical component of the etch.

16 And then once a planarized surface, you
17 move the wafer and then you, of course, have to
18 clean the wafer surface.

19 So in the case of CMP, the removal rate is
20 governed by something known as the Preston
21 equation. It's very straightforward. The removal
22 rate is going to be proportional to the pressure
23 between the wafer and the CMP pad, and the
24 relative velocity between the wafer and the CMP
25 pad, and the proportionality constant is known as

1 a Preston --

2 (Reporter clarification.)

3 A The proportionality constant is known as
4 the Preston coefficient. P-R-E-S-T-O-N.

5 BY MR. GRABOWSKI:

6 Q Can chemical-mechanical polishing be used
7 to etch contact holes?

8 A No.

9 Q And I think you were just getting into
10 this at the end there. Are there various
11 parameters you can adjust that impact how the
12 chemical-mechanical polishing process operates?

13 A Yes. So the main parameters are the
14 pressure between the wafer and the pad and the
15 relative speed with which they move. Okay. And
16 then it depends on the details of the CMP slurry.
17 And those, frankly, are closely-guarded secrets by
18 these CMP slurry vendors. And that will impact
19 this Preston coefficient.

20 Q So not looking for any closely-guarded
21 secrets, but, generally, what parameters of the
22 slurry are going to impact how the CMP process
23 operates?

24 A It will depend on the pH of the solution.
25 Generally speaking, they are alkaline mixtures,

1 and I believe in many cases they use sodium
2 hydroxide diluted in water mixed in with these
3 tiny particles of silicon dioxide.

4 So the density of those particles and the
5 size of those particles would be a factor. But
6 I've not done a detailed study of the slurry
7 chemistries. Most of those are not public
8 knowledge.

9 Q Would what those particles are made up of
10 also have an impact on the function of the
11 chemical-mechanical polishing process?

12 A I haven't looked into those aspects, but,
13 presumably, yes.

14 MR. HSU: Counsel, we have been going over
15 an hour, so maybe it's a good time to stop.

16 MR. GRABOWSKI: I just have a couple of
17 more questions on this topic and then --

18 MR. HSU: Certainly.

19 BY MR. GRABOWSKI:

20 Q I think just one more. The material
21 that's being planarized obviously would also have
22 an impact on the function of the
23 chemical-mechanical polishing process, correct?

24 MR. HSU: Objection. Form.

25 A Yes, the material impacts it in terms of

1 if it's a softer material, it will polish faster,
2 if it's a harder material, it will polish slower.

3 MR. GRABOWSKI: All right. Then with
4 that, I'm happy to take a break.

5 THE WITNESS: How long?

6 MR. GRABOWSKI: Ten minutes.

7 THE WITNESS: Ten minutes is perfect.

8 (A brief recess was held from 11:08 a.m.
9 to 11:20 a.m.)

10 BY MR. GRABOWSKI:

11 Q Dr. Banerjee, before the break, we were
12 talking about the parameters that impacted
13 chemical-mechanical polishing. I just had a
14 couple of follow-ups on that.

15 You mentioned that the hardness or the
16 softness of the material being polished could have
17 an impact. Is that right?

18 A Yes.

19 Q Is there an element of chemical
20 selectivity between the material being polished
21 and the slurry being used as well?

22 MR. HSU: Objection to form.

23 A I mean, the chemical etch selectivity
24 between the slurry and the material being removed
25 does matter in terms of the removal rate.

1 BY MR. GRABOWSKI:

2 Q And holding the material being removed
3 constant, the CMP process would have a different
4 etch selectivity versus a wet etch process or a
5 dry etch process, right?

6 A That's a very broad question, but in
7 general, yes. I mean, you're comparing apples to
8 oranges in some sense.

9 Q Fair to say unless you were working very
10 hard to make the selectivity the same, you have no
11 reason to believe the selectivity would be the
12 same between a CMP process and a wet or dry
13 etching?

14 MR. HSU: Objection. Form.

15 A Once again, that's very broad and you have
16 to give me specifics. But in a broad sense, yes.

17 MR. GRABOWSKI: Could we bring up Han
18 Exhibit 1007, please?

19 (Exhibit 1007 was marked for
20 identification.)

21 BY MR. GRABOWSKI:

22 Q Dr. Banerjee, you recognize Exhibit 1007,
23 right?

24 A Yes.

25 Q This is the Han reference you relied on in

1 forming your opinions, right?

2 A Yes.

3 Q You don't offer the opinion in your
4 declaration that Han discloses an etch-stop layer,
5 right?

6 A I don't think I do, but I can confirm.

7 Q Take your time.

8 A Yes, we do not say that Han discloses an
9 etch-stop layer. That's why we brought in Fang.

10 Q And you don't offer the opinion in your
11 declaration that Han explicitly discusses any
12 issues with short-circuiting, correct?

13 A By "short-circuiting," do you mean the
14 punch-through problem?

15 Q So punch-through or any other form of
16 short-circuiting.

17 A I did talk about the need to avoid
18 short-circuiting. I can't remember exactly where
19 that was.

20 Q I appreciate you talked about
21 short-circuiting in your declaration. I'm asking,
22 you don't offer the opinion in your declaration
23 that Han talks about short-circuiting, right?

24 A Yeah, I don't think Han explicitly talks
25 about that, but short-circuiting would be a bad

1 thing in general.

2 Q And Han also doesn't discuss
3 punch-through, correct?

4 A Yeah, I don't think that Han does.

5 Q And looking at Han Paragraph 149, it does
6 teach the use of a high-k dielectric surrounding
7 its wordline context, right?

8 A Can you show me that paragraph, please?

9 Q It's 149.

10 A I don't have a hard copy.

11 Q I was just helping the tech out. It's on
12 PDF Page 50.

13 Just so I've got a clear question on the
14 record, Han does teach the use of a high-k
15 dielectric in its gate stack layers, correct?

16 A Yes.

17 MR. GRABOWSKI: Could we pull up Fang
18 1006, please?

19 (Exhibit 1006 was marked for
20 identification.)

21 BY MR. GRABOWSKI:

22 Q And you recognize Exhibit 1006, correct?

23 A Yes.

24 Q This is the Fang reference you relied on
25 in forming your opinions, correct?

1 A Yes.

2 Q Fang generally discloses 3D memory devices
3 with staircase structures, correct?

4 A Yes.

5 Q You don't offer the opinion that Fang
6 discloses a staircase structure with the gate
7 stack on top, right?

8 A That's correct.

9 Q I would like to look at Ground 3 in your
10 declaration which starts on Page 110. Are you
11 there?

12 A Yes.

13 Q Okay. That combination -- strike that.

14 That ground relies on a combination of Han
15 and Fang, right?

16 A Yes.

17 Q And in that ground, the only limitation
18 you rely on Fang for is the presence of an etch
19 stop, correct?

20 A Yeah, we bring in Fang to bring in the
21 etch-stop layer.

22 MR. GRABOWSKI: Could we please bring up
23 Chen Exhibit 1008?

24 (Exhibit 1008 was marked for
25 identification.)

1 BY MR. GRABOWSKI:

2 Q And do you recognize Exhibit 1008?

3 A Yes.

4 Q Exhibit 1008 is the Chen reference you
5 relied on in Ground 4 of your opinions, correct?

6 A Yes.

7 Q Chen is directed to addressing the problem
8 of short-circuits as a result of electron
9 tunneling; is that fair?

10 (Reporter clarification.)

11 A Chen discloses the electron tunneling
12 problem. Now, electron tunneling did not
13 necessarily lead to a short-circuit because the
14 tunneling depends on parameters such as the width
15 of the tunneling barrier, height of the barrier.
16 So thinner the barrier, the more tunneling leakage
17 you have. But it did not necessarily mean a dead
18 short-circuit.

19 BY MR. GRABOWSKI:

20 Q Okay. So just because you're experiencing
21 electron tunneling doesn't mean you're necessarily
22 going to actually see short-circuits in any given
23 memory device; is that fair?

24 A That's correct. Depending on the extent
25 of the tunneling, it can lead to tunneling leakage

1 which can be bad in this context. But the leakage
2 may not be so high that it constitutes a
3 short-circuit, which is almost zero resistance.

4 Q It's your opinion that Chen discloses
5 disposing a barrier layer on each step of the
6 plurality of steps of the staircase structure; is
7 that right?

8 A Yes. I discuss that in Page 50 of my
9 report, for example, where I cite Figure 7B. It's
10 nicely annotated.

11 Q That view is based on Chen's discussion of
12 its first stop layer, right?

13 A I can't remember. Is that the terminology
14 that Chen used?

15 Q Yeah. If you look at Paragraph 220 of
16 your report, that might help.

17 A Yes, I see that now.

18 Q Okay. Chen doesn't mention any processing
19 function for its first stop layer, right?

20 MR. HSU: Objection. Form.

21 A I have to respectfully disagree. If you
22 look at Paragraph 221, I state that the very use
23 of term "stop" has a connotation of stopping
24 unintended etching processes. So that's like an
25 etch-stop layer. And that has an implication for

1 processing.

2

3 BY MR. GRABOWSKI:

4 Q But Chen doesn't actually say that that's
5 what the stop layer is for beyond, in your view,
6 the name "stop layer," correct?

7 A I don't recall. I would have to review
8 Chen in detail for that purpose. But for me, the
9 use of the term "first stop" and "second stop"
10 clearly indicated the functionalities of those
11 layers.

12 Q And I guess I'm just asking, beyond the
13 names, there's no functionality -- strike that.

14 Beyond the names, there's no functionality
15 attributed to those layers in Chen, right?

16 MR. HSU: Objection --

17 (Simultaneous unreportable crosstalk
18 occurs among parties.)

19 A I don't recall. I would have to maybe
20 scroll through Chen, if you want me to.

21 MR. GRABOWSKI: Could we give Dr. Banerjee
22 control of the screen?

23 DOC TECH: Sure. Okay, sir, just click
24 anywhere, and you should have control.

25 A I did a quick search of the word "etch."

1 Right in the title, it says: Semiconductor
2 structure having an etching stop layer and
3 manufacturing method of the same."

4 And etching comes up again and again. So
5 I think, clearly, Figure 8A and 8D, various
6 etching stop layers. Literally, I see dozens of
7 places where the word "etching stop layer"
8 appears. So that's a process term.

9 BY MR. GRABOWSKI:

10 Q All right. And it's your opinion that a
11 POSA would incorporate this stop layer of Chen
12 into the combination of Han and Fang as an
13 additional barrier layer; is that right?

14 A A POSITA would include the teaching of
15 Fang to provide etch stopping capability in Han.
16 However, Han, although it does not explicitly talk
17 about an etch-stop layer, Han does disclose these
18 high-k gate dielectrics. I think they talk about
19 that as a horizontal layer of some form.

20 And as we were discussing before the
21 break, the high-k dielectric also has additional
22 benefits of acting as an etch-stop layer, a poor
23 man's etch-stop layer.

24 Q But, nevertheless, it's your opinion that
25 the POSA would want to include a redundant

1 etch-stop layer that's taught by Chen as well?

2 MR. HSU: Objection. Form.

3 A It depends on what you mean by
4 "redundant." As I told you, a high-k gate
5 dielectric may not be thick enough to provide
6 adequate etch stopping, so that's why we brought
7 in Fang's etch-stop layer.

8 BY MR. GRABOWSKI:

9 Q And in your view, in addition to Fang's
10 etch-stop layer, you would also incorporate the
11 additional barrier layer that functions as an
12 etch-stop layer from Chen; is that right?

13 A I mean, it could work with a single
14 etch-stop layer as disclosed in Claims 1 through
15 16 of the '276 Patent, but having a second
16 etch-stop layer as discussed in dependent Claim 17
17 and 18 of '276 gives you additional insurance
18 policy against punch-through.

19 Q Fang doesn't suggest that it needs an
20 additional etch-stop layer to provide that
21 protection, right?

22 MR. HSU: Objection.

23 A Fang, I believe, only has one etch-stop
24 layer, but Chen has two etch-stop layers. Kim has
25 two etch-stop layers.

1 BY MR. GRABOWSKI:

2 Q And adding that second etch-stop layer
3 would increase the complexity of the etching
4 process, right?

5 A Depends on what you mean by "added
6 complexity." Yeah, it's one more layer of
7 deposition and one more step in the etch process,
8 if you will, because you have to change something
9 between the etch process of etch-stop layer one
10 versus etch-stop two. But you do have additional
11 benefits of doing that. So it does come with a
12 cost, yes.

13 MR. GRABOWSKI: All right. I think we're
14 winding down here. If you don't mind, let me
15 take a five-minute break and look at my notes
16 and touch base with my team.

17 THE WITNESS: Okay. Thank you.

18 (A brief recess was held from 11:38 a.m.
19 to 11:40 a.m.)

20 MR. GRABOWSKI: Thank you, Dr. Banerjee.
21 I have no further questions. I'm going to
22 pass the witness.

23 THE WITNESS: Thank you.

24 MR. HSU: I don't have any questions
25 either. Thank you.

1 MR. GRABOWSKI: Thank you for your time.

2 THE WITNESS: Thank you.

3 (Thereupon, the proceedings concluded at
4 11:40 a.m.)

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CERTIFICATE OF REPORTER

I, the undersigned, do hereby certify:

That Sanjay Banerjee, PH.D., the witness whose Deposition
is hereinbefore set forth, was duly sworn by me
before the commencement of such deposition
and that such deposition was taken virtually and
is a true record of the testimony given by such
witness.

I further certify that the adverse party,
MICRON TECHNOLOGY, INC., was represented by
counsel at the deposition.

I further certify that the deposition of
Sanjay Banerjee, PH.D., occurred virtually, on Thursday,
October 2, 2025, from 10:01 a.m. to 11:40 a.m.

1 I further certify that I am not related to
2 any of the parties to this action by blood or
3 marriage, I am not employed by or an attorney to
4 any of the parties to this action, and that I am
5 in no way interested financially or otherwise, in
6 the outcome of this matter.

7
8
9 IN WITNESS WHEREOF, I have hereunto set
10 my hand this 4th day of October, 2025.

11
12 *Erica Field*
13 _____

14 Erica Field, RDR, CRR
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