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AT THE MICRO-
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11

CHAPTER

ETCHING



After a photoresist image has been formed on the surface of a wafer, the next process often involves transferring that image into a layer under the resist by etching. The chapter will begin with simple wet chemical etching processes where the wafer is immersed in a solution that reacts with the exposed film to form soluble by-products. Ideally, the photoresist mask is highly resistant to attack by the etching solution. Although still used for noncritical processes, wet chemical etching is difficult to control, is prone to high defect levels due to solution particulate contamination, cannot be used for small features, and produces large volumes of chemical waste. The chapter will therefore go on to discuss dry, or plasma, etch processes.

It is useful to begin the discussion of etching by identifying the appropriate figures of merit. The primary one is the etch rate, which has dimensions of thickness per unit time. A high etch rate is generally desirable in a manufacturing environment. Too high of an etch rate, however, may render a process difficult to control. Common desired etch rates are tens or hundreds of nanometers per minute. Several related figures are equally important. Etch rate uniformity is measured in terms of percentage variation of the etch rate. It is quoted across a wafer and from wafer to wafer. Selectivity is the ratio of the etch rates of various materials, such as the photoresist or the underlying layer, referenced to the etch rate of the film being patterned. A particular process may be quoted as having a selectivity of 20 to 1 for polysilicon over oxide, meaning that polysilicon etches 20 times faster than oxide.

Undercut is the lateral extent of the etch under the photoresist mask. It can be quoted in two forms. The first is an undercut distance per side. For example, a particular etching process may be found to produce 0.8- μm lines when the patterned photoresist line is 1.0 μm wide. The process bias is 0.1 μm per side. As shown in Figure 11.1, the etched sidewalls are not always vertical. The amount of undercut therefore depends on how it is

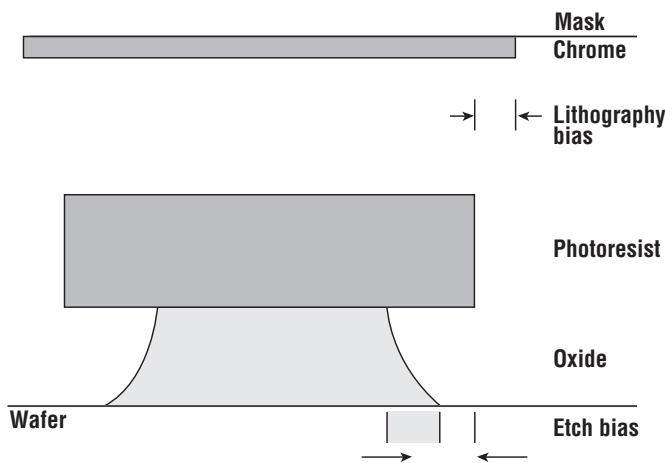


Figure 11.1 Typical isotropic etch process showing the etch bias.

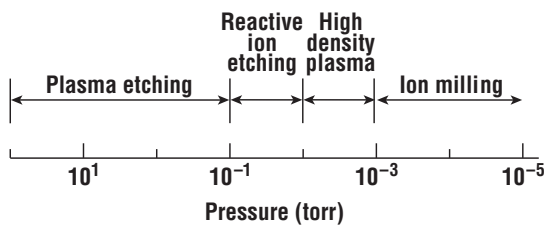


Figure 11.2 Types of etch processes on a chamber pressure scale.

measured. Most electrical measurements of the line are sensitive to its cross-sectional area, providing an average undercut. If the etch process attacks the resist pattern, this attack will also produce an etch bias. Some processes are designed to intentionally do this. For now, however, assume that the resist mask does not change during the etching.

The second method of describing undercut is to quote the etch rate anisotropy. Anisotropy is given by

$$A = 1 - \frac{R_L}{R_V} \quad (11.1)$$

where R_L and R_V are the lateral and vertical etch rates. A process is said to be perfectly anisotropic ($A = 1$) if the lateral etch rate is zero. On the other hand, $A = 0$ would imply that the lateral and vertical etch rates are identical.

All of the preceding metrics can be expressed quantitatively. There are several other metrics that are somewhat more difficult to quantify. The first is the substrate damage. As an example, p-n junctions have been shown to degrade under certain types of plasma etching. The amount of degradation depends not only on the etch process, but on the depth and type of the junction. Finally, the process must be safe, both to the operator and to the environment.

Chlorine plasmas, in particular, are known to produce hazardous by-products that must be neutralized before they are exhausted into the air. Many plasma etch processes are based on Freon chemistries that are known to degrade the environment. Replacing these etches is a continuing area of research.

Etching can be done by physical damage, chemical attack, or some combination of the two. One can define a scale of the etch mechanism that describes the range of etch processes (Figure 11.2). Ion milling, for example, is done with an energetic beam of chemically inert atoms in a very low pressure chamber, such that the length of the mean free path of ions is much greater than the chamber diameter. It is at the extreme of purely physical etching. This process does not volatilize the film; instead it creates an aerosol of atoms and small clusters. These processes are characterized by a high degree of anisotropy, but the etch rate is nearly independent of the substrate material. The selectivity of ion beam milling, therefore, is close to 1. Wet etching is at the other extreme of the spectrum with no physical attack. This type of process is usually characterized by low anisotropy, but it may have high selectivity.

11.1 WET ETCHING

Wet etching is a purely chemical process. Serious drawbacks include a lack of anisotropy, poor process control, and excessive particle contamination. However, wet etching can be highly selective and often does not damage the substrate. As a result, although the process

is much less popular than it once was, it continues to be used for a wide range of “non-critical” tasks. Comprehensive reviews of wet etching can be found elsewhere [1].

Since the reactive species is normally present in the etchant solution, wet chemical etching consists of three processes: movement of the etchant species to the surface of the wafer, a chemical reaction with the exposed film that produces soluble by-products, and movement of the reaction products away from the surface of the wafer. Reactions in the solution may also be required to supply more of the reactive species once the etching starts. Since each step must occur in sequence, the slowest one, called the *rate-limiting step*, determines the etch rate. Since it is generally desirable to have a large, uniform, well-controlled etch rate, the wet etch solution is often agitated in some manner to assist in the movement of etchant to the surface and the removal of the etch product. Some wet etch processes use a continuous acid spray to ensure a fresh supply of etchant, but this comes at the cost of the production of significant amounts of chemical waste.

For most wet etch processes, the film to be etched is not directly soluble in the etchant solution. It is usually necessary to use a chemical reaction to change the material to be etched from a solid to a liquid or a gas. If the etching process produces a gas, this gas can form bubbles that can prevent the movement of fresh etchant to the surface. This is an extremely serious problem, since the occurrence of the bubbles is difficult to predict. The problem is most pronounced near pattern edges, where bubbles can attach to surface topography. In addition to assisting the movement of fresh etchant chemicals to the surface of the wafer, agitation in the wet chemical bath or the use of surfactants will reduce the ability of the bubbles to adhere to the wafer. Even in the absence of bubbles, however, small geometry features may etch more slowly, due to the difficulty in removing all of the etch products. This phenomenon has been shown to be related to microscopic bubbles of trapped gas [2]. Another common problem for wet etch processes is undetected resist scumming. This occurs when some of the exposed photoresist is not removed in the develop process (Figure 11.3). Common causes are incorrect or incomplete exposures and insufficient developing of the pattern. Due to the high selectivity of wet etch processes, even a very thin layer of resist residue is sufficient to completely block the wet etch process.

In the 1990s, wet etching enjoyed something of a resurgence. Automated wet etch benches were developed that allow the operator to control precisely the etch time, bath temperature, degree of agitation, bath composition, degree of misting in spray etches [3], and single-sided etching [4]. Increased use of filtration, even in hot, very aggressive, compounds, has helped control particle deposition concerns. Even with these improvements, however, wet etching is still not regarded as practical for most features smaller than 2 μm . A variety of recipes are available [5].

One of the most common etching processes is the wet etching of SiO_2 in dilute solutions of hydrofluoric acid (HF) [6]. Common etchants are 6:1, 10:1, and 50:1, meaning 6, 10, or 50 parts (by volume) of water to one part HF. A 6:1 HF solution will etch thermal silicon dioxide at about 120 nm/min. Deposited oxides tend to etch much faster. The ratio of the deposited film etch rate in HF to that of thermal oxides is often taken as a measure of its density. Doped oxides such as phosphosilicate glass and borophosphosilicate glass etch faster yet, as the etch rate increases with impurity concentration. Solutions of HF are extremely selective of oxide over silicon [7]. Some etching of silicon does occur, since the water will slowly oxidize the surface of the silicon and HF will etch

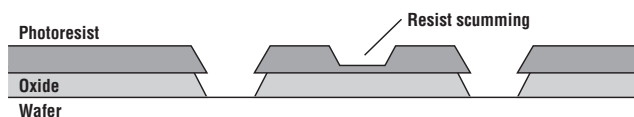


Figure 11.3 Resist scumming occurs when the photoresist is incompletely developed. The residual resist may serve as an etch mask to prevent a complete etch process.

this oxide. Selectivities at room temperature are commonly better than 100:1. Wet etching of oxide in HF solutions is, however, completely isotropic.

The exact reaction pathway is complex and depends on the ionic strength, the solution pH, and the etchant solution [8]. The overall reaction for etching SiO₂ is



One of the important aspects of nearly all chemical etching associated with micro- and nanofabrication is the role of charge transfer. In the case of HF etch of silicon, the adsorption of hydrogen atoms, which react with SiO₂ to form hydroxyls, pulls an electron from the Si–O bond, since OH is extremely electronegative [9]. This reduces the strength of the Si–O bond, leaving Si⁺, which reacts with F. This basic mechanism is one of the reasons that virtually all etching processes, wet or dry, use halides. These are the column VII elements: F, Cl, Br, and I.

Since the reaction consumes HF, the reaction rate will decrease with time. To avoid this, it is common to use HF with a buffering agent (BHF) such as ammonium fluoride (NH₄F), which maintains a constant concentration of HF through the dissolution reaction



where NH₃ (ammonia) is a gas. Buffering also controls the pH of the etchant, which minimizes photoresist attack.

Silicon nitride is etched very slowly by HF solutions at room temperature. A 20:1 BHF solution at room temperature, for example, etches thermal oxide at about 30 nm/min, but the etch rate for Si₃N₄ is less than 1 nm/min [10]. More practical etch rates of silicon nitride can be obtained in H₃PO₄ at 140 to 200°C [11]. A 3:10 mixture of 49% HF (in H₂O) and 70% HNO₃ at 70°C can also be used, but is much less common. Typical selectivities in the phosphoric etch are 10:1 for nitride over oxide and 30:1 for nitride over silicon. If the nitride layer is exposed to a high temperature oxidizing ambient, therefore, a dip in BHF is often done before the nitride wet etch to strip any surface oxide that may have grown on top of the nitride.

Wet etching has also been widely used to pattern metal lines. Since the metal layers used in ICs are often polycrystalline, the lines produced by wet etching sometimes have ragged edges. A common aluminum etchant is (by volume) 20% acetic acid, 77% phosphoric acid, and 3% nitric acid. Some of the metal interconnect is not elemental but, rather, dilute alloys. In many cases, these impurities are much less volatile in the bath than the base material. In particular, silicon and copper additions to aluminum are often difficult to completely remove in standard aluminum wet etch solutions.

Although several techniques have been used for wet etching silicon, most of them use a strong oxidant to chemically oxidize the silicon and HF to etch the oxide. A common etchant solution is a combination of HF and nitric acid (HNO₃) in water. The overall reaction is given by



Often acetic acid (CH₃COOH) is used as a diluent rather than water. Figure 11.4 diagrams the etch rate of silicon in HF and HNO₃ [12]. Notice that the three axes are not independent. To find the etch rate, draw lines from the percentages of HNO₃ and HF. They should intersect at a point on the line corresponding to the remaining percentage of diluent. At low HNO₃ concentrations, the etch rate is controlled by the oxidant concentration.

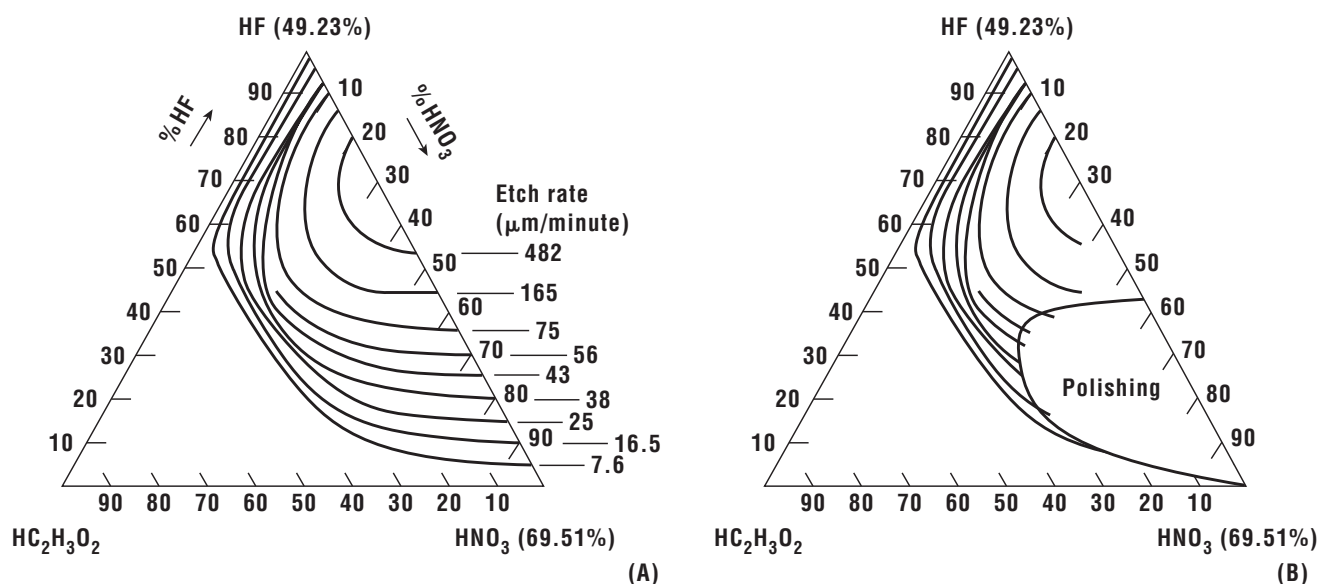


Figure 11.4 The etch rate of silicon in HF and HNO₃ (after Schwarz and Robbins, reprinted by permission of the publisher, The Electrochemical Society Inc.).

At low HF concentrations, the etch rate is controlled by the HF concentration. The maximum etch rate for this solution is 470 $\mu\text{m}/\text{min}$. A hole can be etched completely through a typical wafer at this rate in about 90 sec.

EXAMPLE 11.1

A solution contains two parts of $\sim 70\%$ HNO₃, six parts of $\sim 49\%$ HF, and two parts of acetic acid. Find the etch rate of silicon in this solution.

Solution

Drawing the intersecting lines (as shown in Figure 11.5) produces an etch rate of about 165 $\mu\text{m}/\text{min}$. Note that all three lines intersect at a single point.

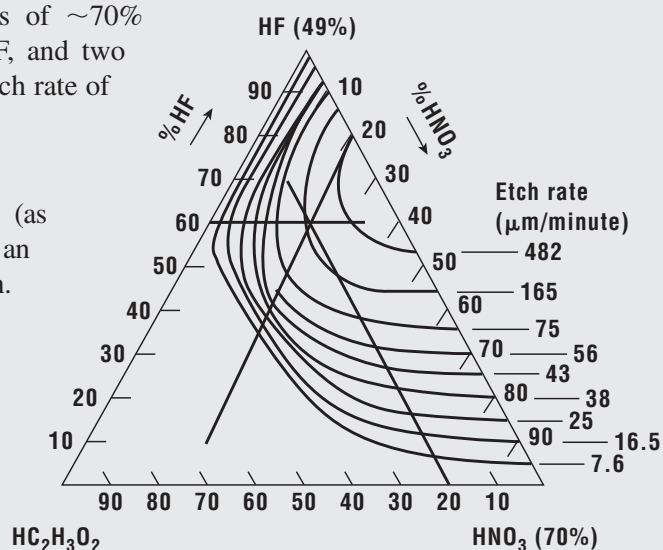


Figure 11.5 Intersection lines imposed on Figure 11.4A to show etch rate.

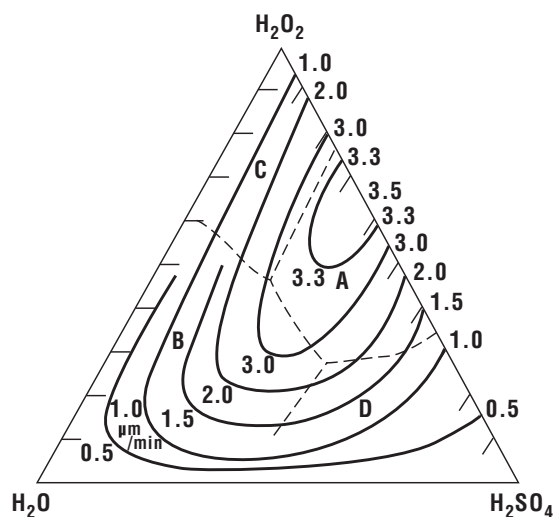


Figure 11.6 The etch rate of GaAs in H_2SO_4 , H_2O_2 , and H_2O . The right leg is the concentration of H_2SO_4 , the bottom leg is H_2O , and the left leg is H_2O_2 . All scales increase in the clockwise direction (after Iida and Ito, reprinted by permission of the publisher, The Electrochemical Society Inc.).

The most common wet etchants for GaAs [13, 14] are H_2SO_4 – H_2O_2 – H_2O [15], Br_2 – CH_3OH [16], NaOH – H_2O_2 [17], and NH_4OH – H_2O_2 – H_2O [18]. Figure 11.6 shows the etch contours for the H_2SO_4 – H_2O_2 – H_2O system [19]. The curves are qualitatively similar to those of Figure 11.4. At high sulfuric acid concentrations, the solution is quite viscous, and so the etch may be limited by diffusion of fresh etchant to the wafer. Etches are uneven in these solutions. As a result, the acid content is usually kept to less than 30%. As with all etching solutions using H_2O_2 , the etch rate decreases with time.

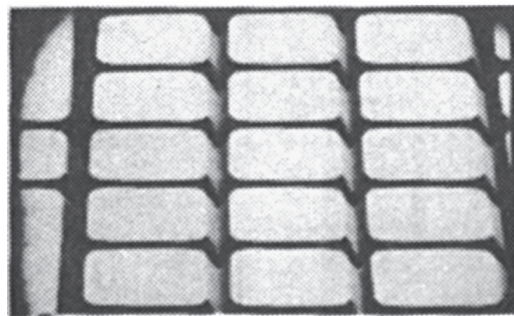
Gallium arsenide etches that are selective to $\text{Al}_x\text{Ga}_{1-x}\text{As}$ are often required since many advanced devices consist of very thin layers of one material on top of the other. Selective etches are needed to make electrical contact to the various layers. The first reports of a selective etch used a 30% solution of H_2O_2 diluted with NH_4OH or H_3PO_4 to control the pH [20]. Selectivities as large as 30:1 have been reported in this system [21]. Redox solutions such as I_2 – KI , $\text{K}_3\text{Fe}(\text{CN})_6$ – $\text{K}_4\text{Fe}(\text{CN})_6$, and $\text{C}_6\text{H}_4\text{O}_2$ – $\text{C}_4\text{H}_6\text{O}_2$ are now more commonly used due to their high etch rates and good selectivities. Tijburg and van Dongen [22] reported selec-

tive etching of GaAs over AlGaAs for $\text{K}_3\text{Fe}(\text{CN})_6$ – $\text{K}_4\text{Fe}(\text{CN})_6$ solutions with pH values greater than 9 and selective etching of AlGaAs over GaAs for the same solutions with pH values between 5 and 9. In addition, NH_4OH – H_2O_2 – H_2O and $\text{K}_3\text{Fe}(\text{CN})_6$ – $\text{K}_4\text{Fe}(\text{CN})_6$ have been found to be highly selective etches for GaAs and AlGaAs over InGaAs [23].

A wide variety of wet etches exist for GaN [24], ranging from phosphoric acid, which etches at 13 to 32 nm/min [25], to a mixture of citrus acid and hydrogen peroxide, which etches at 570 nm/min [26]. As with silicon, most recipes require an oxidizer and a reducing agent. Surface roughness can vary significantly. Interested readers are referred to Ma *et al.* [24] for more information.

It is sometimes useful to be able to etch deep patterns in semiconductor substrates with directional control. Wet etching can be directional if a crystalline material is etched. Directional wet etching will be discussed in more detail in Chapter 19. Briefly, because some solutions etch much faster along certain crystal directions, they produce sharp facets with well-controlled angles in the single-crystal substrates [27]. In the zincblende structure, the density of bonds in the (111) directions is much larger than in the (100) or (110) directions. Some etchants will therefore etch more slowly in the (111) directions.

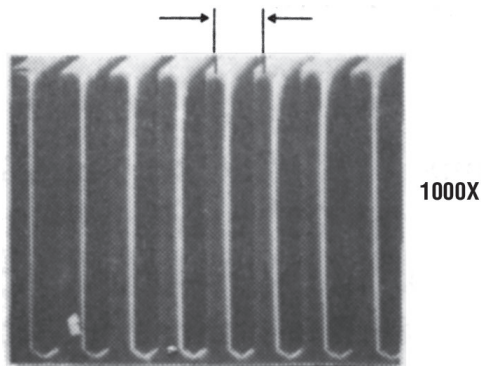
Common directional wet etchants for silicon are mixtures of KOH, isopropyl alcohol, and water. A 23.4:13.5:63 mixture etches 100 times faster in the (100) directions than in the (111) [28], although some researchers have reported etch rate ratios up to 200:1 [29]. Since this etchant contains no HF, a thermal oxide can be used as the masking layer. Figure 11.7 shows a cross-sectional view of (100) wafers after directional etching. Closely spaced features will result in a characteristic V shape with sidewalls at 54.77° to the surface normal. More widely spaced features will etch deeper into the substrate, exposing more of the (111) surface. If the wafers are etched long enough, these facets can extend completely through the wafer. A common directional etchant for GaAs is Br_2 – CH_3OH [30]. Directional etches for GaN include H_3PO_4 , molten KOH, KOH dissolved in ethylene glycol, and NaOH dissolved in ethylene glycol [25].



SEM TOP VIEW (100) DI ETCH



SEM CROSS-SECTIONAL VIEW (100) DI ETCH



1000X

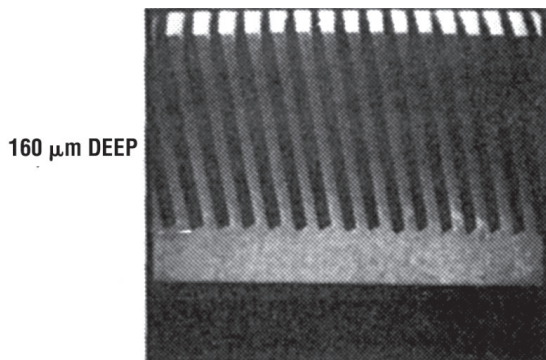
160 μm DEEP

Figure 11.7 (100) silicon wafers after directional etching in KOH, isopropyl alcohol, and water. The upper photo shows a 50- μm -deep etch. The lower photographs are of 80- μm -deep trenches etched at 10- μm pitch on (110) and 10° off (110) (after Bean [27], ©1978 IEEE).

A variety of special-purpose wet etches have also been developed for selectively etching certain regions of the wafers. This section will review two: doping selective and defect selective. Doping-selective etches were developed primarily for junction staining, providing steps that can be used to show the depth of a deep p-n junction (see Section 3.5). These techniques have also been applied to the fabrication of etch stop layers for sensors, silicon on insulator, freestanding membranes, and other special structures. One of the most common doping-selective etches is a 1:3:8 mixture of $\text{HF}/\text{HNO}_3/\text{CH}_3\text{COOH}$. The etch rate of either type of heavily doped ($>10^{19}\text{ cm}^{-3}$) layers of silicon is about 15 times larger than the etch rate of lightly doped layers [35]. An ethylenediamine/pyrocatechol/water mixture, however, etches lightly doped silicon but does not attack heavily doped p-type layers [36].

Defect-selective etching is done to decorate (highlight) defects in the wafer. Defects that may be invisible before etching are often readily observable by simple optical microscopy after preferential defect staining. By counting the defects after staining, a defect density can be derived. Although some defect stain etches have been developed for GaAs, the most common (summarized in Table 11.1) have been used in silicon.

11.2 CHEMICAL MECHANICAL POLISHING

The chemical mechanical polishing (CMP) process is designed to produce a globally flat surface, free of scratches and contamination. Due to the need for high NA lens with a small depth of field and for many layers of metal interconnect, CMP usage has increased dramatically, with a total market exceeding \$2.5 billion by 2013. Interestingly, the consumables market for CMP exceeds the systems market [37]. Although originally developed for interconnect planarization, it is now also being applied to front-end processes such as device isolation as well. A simple process schematic is shown in Figure 11.8. The wafer is mounted on a rotating carrier, which is placed into contact with a rotating pad. A slurry of chemicals and particles is put on the pad and is transported under the wafer. The pad has small asperities on the surface to provide fresh slurry to the wafer and to remove the by-products.

The simplest equation for the removal rate is Preston's equation [38]

$$RR = k_p P v$$

where k_p is Preston's coefficient, P is the downward pressure, and v is the relative velocity between the pad and the wafer.

TABLE 11.1 / WET CHEMICAL ETCH SOLUTIONS USED TO DELINEATE DEFECTS IN (100) AND (111) SILICON

(100)	Schimmel [31]	2:1; HF/CrO ₃ (1 molar)	Works well on lightly doped layers (>0.6 Ω-cm)
	Modified Schimmel [31]	4:3:2; HF/H ₂ O/CrO ₃ (1 molar)	Works well on heavily doped layers
	Secco d'Aragona [32]	2:1; HF/K ₂ Cr ₂ O ₇ (0.15 molar)	Delineates oxidation-induced stacking faults
(111)	Sirtl and Adler [33]	1:1; HF/CrO ₃ (5 molar)	Requires agitation
	Dash [34]	1:3:10; HF/HNO ₃ /CH ₃ COOH	Etch rates are slow and concentration dependent

Typical removal rates are several hundred nanometers per minute [39]. For many processes the removal mechanism is believed to be the formation of a hydrated surface layer that is abraded away by contact with the particles in the slurry. The formation and depth of this layer are increased by pressure. Some typical CMP process parameters are given in Table 11.2 [40]. Increasing the pad pressure increases the removal rate linearly, but often increases the step height ratio of the polished features [41] as well as increasing the residual oxide damage and metal contamination of the surface layer [42].

Gross mechanical damage is prevented by the fact that the particles chosen for the slurry are not harder than the film that is being polished [43]. Surface angles on CMP wafers are approximately 1° compared to 10° on reflow glass polished over abrupt metal steps. Due to the flat surface that is formed, CMP wafers can have far fewer defects, such as metal stringers and opens, both of which commonly occur near the edges of severe topology. The smoothness that can be attained after CMP can be approximated by the Hertzian penetration depth

$$R_s = \sqrt[3]{\frac{\phi P}{2K_p E}}$$

where ϕ is the diameter of the abrasive particle, E is the Young's modulus of the material being polished, and K_p is a constant related to the density of the particle. For a closely packed material, $K_p = 1$. For the case of polishing silicon with silica particles with $\phi = 100$ nm, $K_p = 0.5$, and a pressure of 1.5 MPa, giving $R_s \sim 0.3$ nm, indicating that an essentially smooth surface can be attained for this system.

In the earliest and most common CMP processes, a thick spin-on or deposited layer of SiO₂ is first applied. The wafer is polished in an alkaline slurry containing colloidal silica (a suspension of abrasive SiO₂ particles) and an etching agent [44] such as a dilute HF (see Figure 11.8 for a simplified schematic). Common matrix solutions for the suspension are KOH and NH₄OH. The pH, which is typically around 10, is

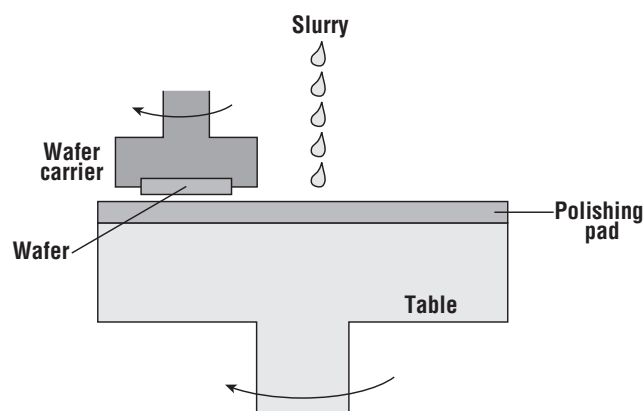


Figure 11.8 Chemical mechanical polishing of the surface of a partially processed wafer done to achieve a high degree of global planarization.

TABLE 11.2 / TYPICAL CMP PROCESS PARAMETERS AND RESULTS FOR OXIDE PLANARIZATION

Thermal oxide removal rate	(nm/min)	60–80
Deposited oxide removal rate	(nm/min)	100–150
Polishing time	(min)	~10
Pad pressure	(psi)	6
Pad rotation	(rpm)	10
Wafer rotation	(rpm)	12

After Nanz and Camilletti [40].

maintained, to keep the silica particles charged to repel each other and so avoid the formation of a large gel network. A pH buffering agent is sometimes used to ensure the stability of the process. The size of the particles that are used depends on the desired removal rate, with literature reports ranging from 0.03 to 0.14 μm . Typically sized particles ($\sim 0.05 \mu\text{m}$) can agglomerate to form clusters about 0.25 μm in diameter [45]. The solids content in the slurry is kept to 12–30%.

CMP has also been extended to the planarization of metals such as copper [46, 47] and tungsten. For metal planarization, acidic ($\text{pH} < 3$) slurries are used. These slurries do not form colloidal suspensions, and so some agitation must be used to maintain uniformity [48]. Alumina is the most commonly used abrasive for tungsten CMP because it is closer in hardness to tungsten than most other abrasives. Tungsten is removed by continuous, self-limiting oxidation of the tungsten surface and subsequent mechanical abrasion [49, 50]. The slurry forms a hydrated tungsten oxide that is selectively removed by alumina particles of order 200 nm. It has been shown that for typical CVD tungsten, the removal rate increases as the film gets thinner. This has been related to the change in tungsten grain size [51]. Generally the tungsten CMP process is optimized to obtain a large selectivity for W over SiO_2 . Selectivities approaching 30 are commonly achieved.

Chemical mechanical polishing of copper is particularly interesting due to the low resistivity of copper and because copper is extremely difficult to etch in a plasma. Thus copper can be patterned by a CMP technique called damascene processing. This will be discussed in Chapter 15. Copper is polished in an aqueous solution containing particles several hundred nanometers in diameter. The slurry must meet two basic requirements: any copper mechanically abraded must be dissolved by the slurry, and the polishing rate of the surfaces that come into contact with the pad must be higher than the removal rate of the low-lying copper. Typical slurries include ammonium hydroxide (NH_4OH), nitric acid (HNO_3), and hydrogen peroxide (H_2O_2) [52]. The oxidizing agents form copper oxide on the surface, which greatly inhibits removal unless the abrasives can remove the oxides. Polish rates up to 1600 nm/min have been achieved [53]. Unlike tungsten, copper is a soft metal. Mechanical effects have a significant effect on the polish process. The polish rate has been found to be proportional to applied pressure and relative linear velocity. The pad condition and pressure application mechanism are found to be particularly important for copper CMP.

To minimize overpolish, one must develop processes with a high selectivity or strive for very reproducible removal rates. Polish rate drift is a serious problem. The condition of the polishing pad is a key determinant of the removal rate, since the porosity of the pad

determines the slurry arrival rate at the surface of the wafer. Glazing of the pad tends to occur after several runs and slows the polishing rate [54]. The solution to this problem is frequent conditioning of the pad to obtain a consistent roughness. Pad glazing is removed by contacting the pad with a diamond-impregnated workpiece. This can be done either during the wafer polish (*in situ*) or between wafer polishing (*ex situ*) [55]. This must be traded off against defect density, however, since post-CMP wafers often show greatly increased particle counts if polished immediately after pad conditioning [41].

Dishing is a common problem in CMP. This refers to the tendency to continue removing material in the spaces between etch stop features. The amount of material removed goes smoothly from zero near the etch stop to a maximum halfway between the features. Dishing is a result of the flexing of the polishing pad and can lead to short circuits in the copper damascene process. The degree of dishing depends on the spacing between the polish stop features—lower spacing results in less dishing. Therefore, it is common to impose design rules on the maximum spacing allowed. Dummy features that have no circuit use may be inserted in the design to control dishing.

Postpolish cleaning is an important step in the CMP unit process. Generally one must trade off polishing goals (uniformity planarity, throughput) against cleaning goals (particles, scratches, and other surface damage; residual ionic and metallic contaminants). Megasonic agitation may be used in combination with a soft pad scrubber or a cleaning solution to assist in the removal of the colloidal suspension from the wafer [56]. Usually the wafer is transferred to a second pad that is reserved for cleaning. This transfer should be timed to prevent the drying of the suspension on the surface of the wafer, after which residue removal is considerably more difficult. Furthermore, scratches left behind after CMP may collect metal that is hard to remove in standard plasma etches. These embedded metal-filled scratches are sometimes called rails and will short out subsequent metal lines. Rails are commonly produced in tungsten CMP processes in which the surface tungsten is removed down to an interlayer oxide, leaving tungsten only in the through holes. Such a process is done instead of the selective tungsten and the deposition and etchback processes described in Section 15.7. The hard alumina particles often severely scratch the oxide surface once all of the tungsten has been removed. Cleanup after tungsten CMP may also be significantly more difficult due to the large electrostatic potential of tungsten particles under typical process conditions [57]. A dilute (100:1) HF step may be included to lift off many of the smaller metal particles and to reduce residual surface damage.

11.3 BASIC REGIMES OF PLASMA ETCHING

Etching in a plasma environment has several significant advantages when compared with wet etching. Plasmas are much easier to start and stop than simple immersion wet etching. Furthermore, plasma etch processes are much less sensitive to small changes in the temperature of the wafer. These two factors make plasma etching more repeatable than wet etching. Most important for small features, plasma etches may have high anisotropies. Plasma environments may also have far fewer particles than liquid media. Finally, a plasma etch process produces less chemical waste than wet etching.

As shown in Figure 11.2, there is a wide variety of dry etch processes with differing amounts of physical and chemical attack. Overlaid on this is the variety of etch chemistries that is used in each type of etch system. Table 11.3 lists some of the most common [58]. Clearly, a complete review of this topic would be complicated and lengthy. The remainder of the chapter will review a representative sample of these processes. A few of the typical

TABLE 11.3 / TYPICAL ETCH CHEMISTRIES

Si	CF ₄ /O ₂ , CF ₂ Cl ₂ , CF ₃ Cl, SF ₆ /O ₂ /Cl ₂ , Cl ₂ /H ₂ /C ₂ F ₆ /CCl ₄ , C ₂ ClF ₅ /O ₂ , Br ₂ , SiF ₄ /O ₂ , NF ₃ , ClF ₃ , CCl ₄ , CCl ₃ F ₅ , C ₂ ClF ₅ /SF ₆ , C ₂ F ₆ /CF ₃ Cl, CF ₃ Cl/Br ₂
SiO ₂	CF ₄ /H ₂ , C ₂ F ₆ , C ₃ F ₈ , CHF ₃ /O ₂
Si ₃ N ₄	CF ₄ /O ₂ /H ₂ , C ₂ F ₆ , C ₃ F ₈ , CHF ₃
Organics	O ₂ , CF ₄ /O ₂ , SF ₆ /O ₂
Al	BCl ₃ , BCl ₃ /Cl ₂ , CCl ₄ /Cl ₂ /BCl ₃ , SiCl ₄ /Cl ₂
Silicides	CF ₄ /O ₂ , NF ₃ , SF ₆ /Cl ₂ , CF ₄ /Cl ₂
Refractories	CF ₄ /O ₂ , NF ₃ /H ₂ , SF ₆ /O ₂
GaAs	BCl ₃ /Ar, Cl ₂ /O ₂ /H ₂ , CCl ₂ F ₂ /O ₂ /Ar/He, H ₂ , CH ₄ /H ₂ , CClH ₃ /H ₂
InP	CH ₄ /H ₂ , C ₂ H ₆ /H ₂ , Cl ₂ /Ar
Au	C ₂ Cl ₂ F ₄ , Cl ₂ , CClF ₃

Cotler and Elta [58].

etch chemistries for the most common etch process will also be presented. For further information on plasma etching, the reader is referred to any of several references [59–61].

The preceding chapter introduced the concept of a glow discharge. For a plasma etch process to proceed, six steps must occur. A feed gas introduced into the chamber must be cracked into chemically reactive species by the plasma. These species must diffuse to the surface of the wafer and be adsorbed. Once on the surface, they may move about (surface diffusion) until they react with the exposed film. The reaction product must be desorbed, diffused away from the wafer, and transported by the gas stream out of the etch chamber. As with wet etching, the etch rate is determined by the slowest of these steps.

In a typical plasma etch processes, the surface of the film to be etched is subjected to an incident flux of ions, radicals, electrons, and neutrals. Although the neutral flux is by far the largest, physical damage is related to the ion flux. Chemical attack depends on both ion flux and the radical flux. Often this bombardment sets up a modified surface layer that is many atomic layers thick.

11.4 HIGH PRESSURE PLASMA ETCHING

The earliest plasma etch equipment, introduced into IC fabrication facilities in the early 1970s, was based on high pressure, low power plasmas, where the mean free path of the species in the plasma is much less than the chamber size. The plasma in such a process is used to start and stop the chemical reaction of etching. It does this by producing a reactive species from an inert precursor. Since the energy of ions in the plasma is quite low, the etching process depends primarily on the chemistry of the plasma.

Plasma chemistry is extremely complex. To begin to understand the chemistry of the glow discharge, it is useful to start from a prototype system. The most widely studied plasma etch chemistry is that produced by carbon tetrafluoride (CF₄). Assume that a flow of CF₄ gas is established in a chamber, where a high pressure plasma ($\lambda \ll$ the electrode spacing) is maintained. Silicon wafers with a photoresist mask are in contact with the plasma. The process intent is to etch the substrate silicon. This choice does not mean that only CF₄ or even fluorinated plasmas are run at high pressure. Chlorine and other species may also

be used in high pressure plasmas. By the same token, fluorinated species are sometimes used for lower etch processes.

One can begin with a simple energy balance argument as discussed in Morgan [60]. This model suggests that etching can occur if a chemical reaction that produces a gaseous or high vapor pressure liquid or solid is energetically favored. Applied to the etching of silicon, the basic idea is that volatilizing silicon with a halogen requires the replacement of Si–Si bonds with Si–halogen bonds. The amount of energy necessary to break a C–F bond in CF_4 is 105 kcal/mole. The amount of energy required to break an Si–Si bond is 42.2 kcal/mole. For CF_4 to etch silicon, the sum of these two energies (147 kcal/mole) must be less than the energy of the Si–F bond (130 kcal/mole)



where $\searrow$ represents a bond-breaking event. Since there is a net positive energy required for the reaction, CF_4 will not etch silicon directly. However, we have not taken into account the effect of the adsorption of a highly negative species like F, as mentioned in Section 11.1. This will lower the Si–Si bond strength by localizing an electron previously participating in a covalent bond. Yet, even if this results in a net negative energy for Reaction 11.5, the bond breaking on the left side still imposes a large kinetic barrier that can make the process unworkably slow. In a plasma, however, collisions with high energy electrons will dissociate some of the CF_4 molecules, producing free fluorine atoms and molecular radicals. The first term of Equation 11.5 is now ignored from an energy balance point of view. The formation of SiF compounds is then energetically favored. Furthermore, by choosing the feed gas, chamber pressure, and plasma power, one can increase the density of species that are energetically favored to etch the film.

In a typical plasma, most of the species are unreacted gas molecules. The density of these molecules at 500 mtorr is about $3 \times 10^{16} \text{ cm}^{-3}$. After the unreacted feed gas, the next most common (5 to 10%) species in the plasma are neutral radicals from the precursor: CF_3 , CF_2 , C, and F. These radical species are extremely reactive. Assuming a simple kinetic theory gas, one can use Equation 10.10 to estimate roughly the flux of radicals striking the surface:

$$J_n = \sqrt{\frac{n^2 kT}{2\pi M}} \quad (11.6)$$

Assuming a radical species temperature of 500 K, the radical bombardment rate due to simple diffusion is of order $10^{23} \text{ m}^{-2} \text{ sec}^{-1}$. Also assuming that every radical that strikes the surface etches one silicon atom, and that the radical flux is the rate-limiting step, the resultant etch rate would be about 2000 nm/min. Thus, one could conceive of such a purely chemical process that would provide ample etch rates. In practice, not all of the radical species will etch all of the substrate materials. Some of the reaction by-products such as carbon do not react with silicon or do not form volatile species. As these materials coat the surface of the wafer, they slow the etching reaction. Furthermore, not all reactant species that strike the surface of the wafer will stick.

Typical plasma power densities in this prototype reactor also create an ion concentration of order 10^{10} cm^{-3} . In a CF_4 plasma, the most abundant ion species is CF_3^+ . Because of the small ion concentration, most of the etching will not be directly due to ions in the plasma. Rather, the constant bombardment of ions incident on the surface creates damage

in the form of unsatisfied bonds that are exposed to the reactive radicals. The neutral radicals diffuse to the surface due to the concentration gradient in the plasma. On the surface they quickly react, form volatile products, and are pumped away. Referring back to Reaction 11.5, we see that ion bombardment of the surface eliminates most of the energy penalty associated with the Si–Si bond breaking event. This makes the forward reaction even more energetically favored. A classical paper by Coburn and Winters [62] demonstrated vividly that a combination of chemical and physical attack etches much faster than either mechanism alone.

The CF_4 plasmas can be used to selectively etch silicon on silicon dioxide or silicon dioxide on silicon. To understand how, start with a picture of what happens at the surface

of the wafer. It is believed that in a fluorine plasma, the surface silicon atoms are bonded to two F atoms, forming a fluorinated skin that may be several atoms thick. Both SiF_2 and SiF_4 are volatile species, but SiF_2 will not readily desorb since it is still weakly bonded to the wafer. As shown in Figure 11.9, the arrival of additional F atoms will reduce the number of bonds between the surface silicon atom and the substrate until eventually the silicon fluoride molecule can be released at a minimum of energy. The primary sources of these atoms are atomic fluorine, F_2 , and radicals of the form CF_x , where $x \leq 3$.

Without ion bombardment, F_2 radicals will etch SiO_2 very slowly, since there is a net energy loss in the reaction



while CF_3 radicals will etch SiO_2 much more aggressively because the C—O bond energy compensates for the Si—O bond breaking. In a pure fluorine beam at low energy, the selectivity of Si of SiO_2 is almost 50:1 when the wafer is held at room temperature and about 100:1 at -30°C . As a result, one type of plasma process for etching silicon selectively over silicon dioxide produces high atomic fluorine concentrations. Although it is possible to use F_2 as the feed gas, this is not desirable due to the toxicity of the gas. The preferred species are CF_4 , C_2F_6 , SF_6 , and NF_3 , all of which produce very large concentrations of free F in a plasma. It is found experimentally that the addition of small concentrations of oxygen to a CF_4 feed gas will increase the etch rate of both silicon and silicon dioxide [63]. It is believed that the oxygen reacts with the carbon atoms to produce CO and CO_2 . This removes (scavenges) some of the carbon from the plasma, thereby increasing the F concentration. These plasmas are called fluorine rich. Figure 11.10 shows plots of some of the species concentrations in a CF_4 plasma

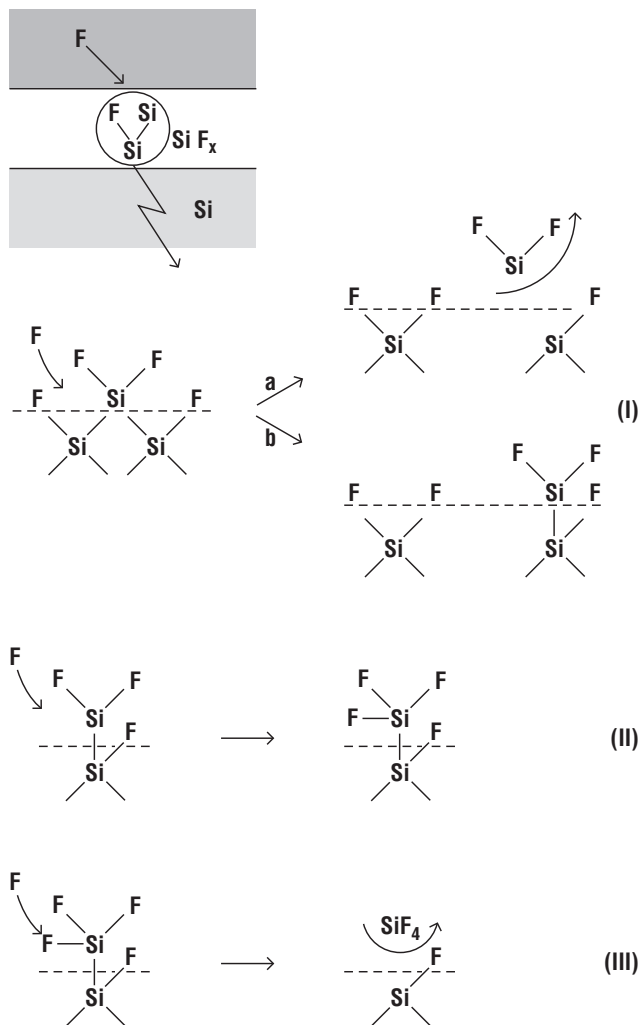


Figure 11.9 Proposed mechanism of plasma etching of silicon in CF_4 . A 1- to 5-atom-thick SiF_x layer forms on the surface. A silicon atom on the upper level is bonded to two fluorine atoms. An additional fluorine atom may remove the silicon as SiF_2 . It is more likely, however, that additional fluorine atoms bond to the silicon atom until SiF_4 forms and desorbs (after Manos and Flamm, reprinted by permission, Academic Press).

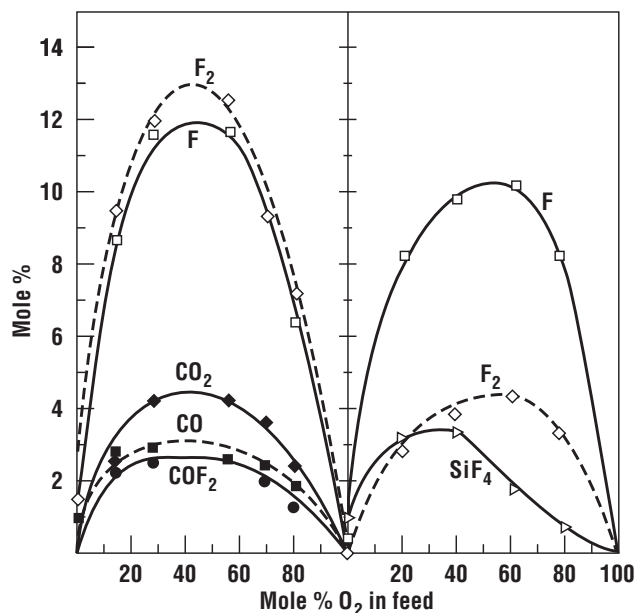


Figure 11.10 Species concentration in a 500-mtorr, 50-W CF_4 plasma as a function of the amount of oxygen in the feed gas in the absence (left) and presence (right) of silicon (after Smolinsky and Flamm, reprinted by permission, AIP).

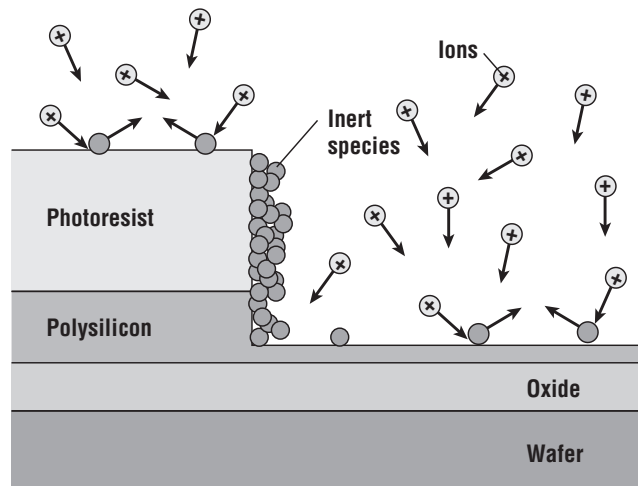


Figure 11.11 Schematic diagram of a high pressure anisotropic etch showing the formation of sidewall passivating films.

as a function of the amount of oxygen in the feed gas [64]. The F concentration can be increased by an order of magnitude by the addition of 12% O_2 to a CF_4 plasma producing about an order of magnitude increase in the Si etch rate, while the increase in the etch rate of SiO_2 is considerably less. At higher oxygen concentrations, the selectivity of silicon to oxide drops sharply as the molecular and atomic oxygen chemisorb on the silicon surface, making it appear more like SiO_2 [65].

A traditional application of a selective etch of Si to SiO_2 is patterning a polysilicon gate for an MOS transistor over a thin gate oxide. Although the addition of O_2 to CF_4 can increase the selectivity of the etch, the processes are not necessarily anisotropic. It is possible to etch silicon anisotropically in a high pressure fluorine plasma by encouraging the formation of nonvolatile fluorocarbons that deposit on the surface of the wafer. The deposit can only be removed by physical collisions with incident ions. Figure 11.11 shows a schematic of an anisotropic high pressure plasma etch process. Fluorocarbon films deposit on all surfaces [66], but the ion velocity, which follows the electric field, is nearly vertical. As a result, as the etching proceeds there is little ion bombardment of the sidewalls and the fluorocarbon film accumulates. (Due to collisions with the ions, neutral species may also strike the surface of the wafer, but they are not shown in Figure 11.11.) The nature of the film is a sensitive function of plasma conditions [67]. If it is not reactive, ion bombardment of the horizontal surfaces drives reactions with the underlying substrate [68, 69]. Under steady-state conditions an approximately 1.5-nm layer of fluorinated silicon is formed under the fluorocarbon [70]. The process of producing nonvolatile species that reduce the etch rate is known as *polymerization*. The film is said to passivate the sidewall, preventing lateral etching. This is one of two techniques for producing anisotropy. The composition of this film has been studied for a variety of chemistries [71–75].

One way to encourage sidewall polymerization is to add hydrogen to the plasma. The hydrogen scavenges fluorine, creating a carbon-rich plasma. The excess carbon can then form these nonvolatile products. The same thing happens if C_2F_6 is used as the feed gas instead of CF_4 . In many cases, the etch products from the resist, which are also hydrocarbons, may also participate in the polymer formation process. Scavenging fluorine, however, does the opposite of what was done when oxygen was added to the plasma. As a result, the silicon-to-oxide selectivity drops in such an etch process. One can therefore obtain anisotropy or selectivity of Si to SiO_2 in such a plasma, but not both simultaneously.

The gases in a plasma reactor, however, can be changed during the etch process. In the case of MOS technologies, to obtain good dimensional control of polysilicon gate electrodes in a simple process, one might start the etch in a CF_4 plasma with H_2 . When the etch is most of the way through the polysilicon, one could shut off the H_2 and instead add O_2 . There may be some undercutting during this part of the process, but before undercutting can begin, the plasma must first erode the accumulated polymer. As a result, these hybrid etch processes, while using very simple equipment and relatively innocuous feed gases, can produce adequate etch profiles for features down to about 1 μm .

An example of this kind of approach is Bosch etching [76]. In this technique two steps are run repeatedly in a cycle. In the first part of the cycle an isotropic plasma etch is done. This might be SF_6 etching of undoped silicon. Next the gas is purged, and a heavy sidewall polymerization mix of gases is used, such as H_2/CF_4 . This coats all surfaces, stopping the etch process. The thickness of the coating is limited by the step time. When the SF_6 is reintroduced, ion bombardment removes the polymer from all horizontal surfaces, but vertical surfaces remain protected. Once again, an isotropic etch starts from the bottom of the first etch cycle. An etch process may require dozens of cycles. Bosch profiles show a very characteristic scallop along the edge. It is commonly used for MEMS (Chapter 19).

As just described, adding a small amount H_2 to a CF_4 plasma causes the etch rate of both silicon and silicon dioxide to decrease, in good agreement with our nonvolatile species model. At moderate H_2 concentrations, the etch rate of SiO_2 exceeds that of Si. The chemistry can therefore be used to selectively etch SiO_2 over Si. In this case, the hydrogen reacts with the fluorine radicals to form HF, which etches silicon dioxide but not silicon [77]. The plasma in this situation is said to be fluorine deficient. At moderate H_2 concentrations, the nonvolatile fluorocarbon film deposition process that increases anisotropy further increases the selectivity. On the surface of the SiO_2 , the oxygen produced during the ion bombardment will react with the carbon to form CO and CO_2 , both of which are volatile and so are pumped away. No such reaction occurs over the silicon, and so the etch selectivity of SiO_2 over Si increases sharply with the addition of H_2 to the plasma (Figure 11.12). Eventually, the carbon deposition rate swamps the ability of the plasma etch process to remove it, and instead of etching, there may be a net deposition.

Coburn and Kay recognized that for fluorocarbon systems the onset of polymerization depends on the fluorine to carbon ratio [78, 79]. After taking into account the formation of HF, CO, CO_2 , and other scavenging compounds, polymerization proceeds when the remaining carbon concentration in the feed gas mixture is greater than half of the fluorine concentration. Examples of gases at the point of polymerization include C_2F_4 , CHF_3 , and a 1:1 mixture of CF_4 and H_2 . Highly selective plasma etch processes operate close to this point and can achieve etch selectivities of over 20:1 for etching SiO_2 over Si. The hydrogen can be supplied as H_2 gas. It can also be incorporated into the fluorinated precursor as CHF_3

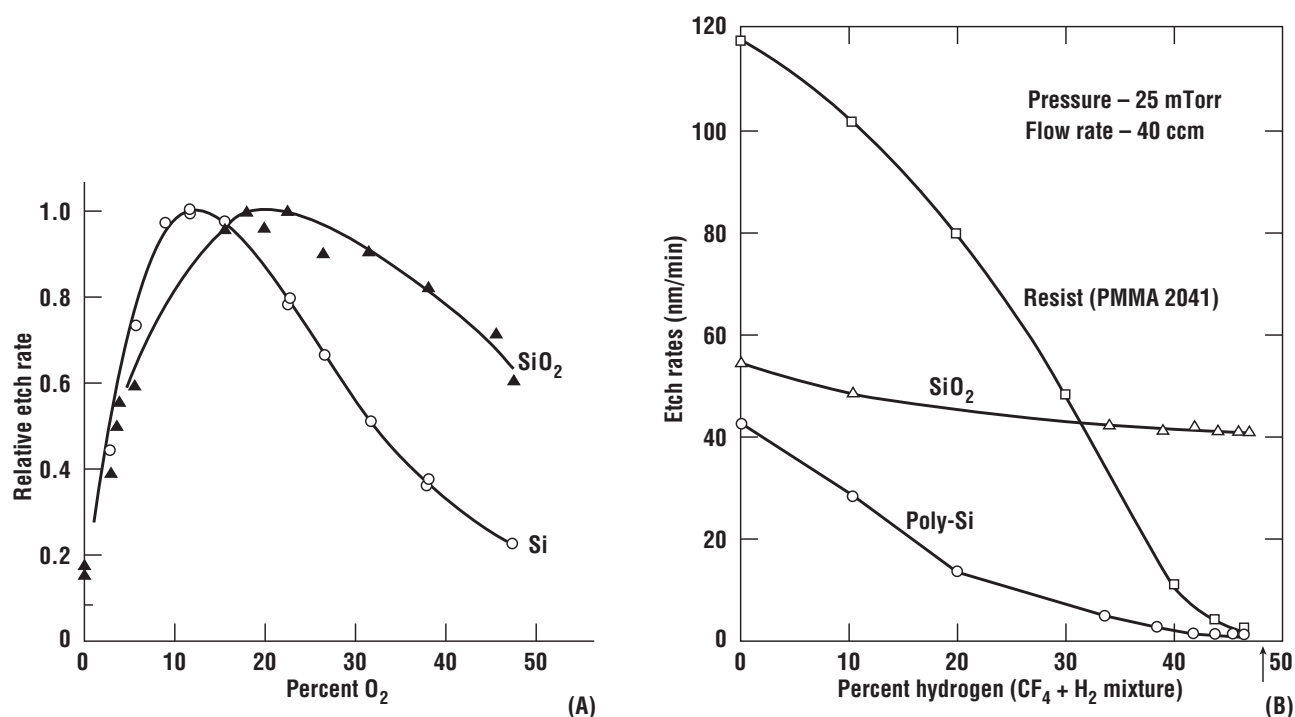


Figure 11.12 Etch rate of Si and SiO₂ in (A) CF₄/O₂ plasma (after Mogab et al. [65], reprinted by permission, AIP), and (B) CF₄/H₂ plasma (after Ephrath and Petrillo [107], reprinted by permission of the publisher, The Electrochemical Society Inc.).

or CH₂F₂. It can also be added in the form of methane (CH₄), ethane (C₂H₆), or other simple hydrocarbons. In the latter case, one must take into account that this not only adds hydrogen to the plasma, but carbon as well.

As was just pointed out, the concept of depositing a nonvolatile polymeric film during the plasma etch process has an important application in producing etch selectivity. As was the case for silicon etching, sidewall passivation can produce highly anisotropic etch profiles when one is etching SiO₂; however, there is no trade-off of selectivity required. As a result, it is relatively easy to use fluorinated plasmas to produce nearly vertical etching of SiO₂ over Si. Figure 11.13 shows etch profiles of SiO₂ with increasing concentrations of NF₃ [80]. At the highest concentrations, there is a large etch rate, but the polymeric formation is suppressed and the etch is isotropic with substantial undercut of the mask.

Selective etching of silicon nitride to both silicon dioxide and silicon cannot be achieved simultaneously due to its intermediate position in terms of bond strength and electronegativity. For selectivity of nitride to oxide, silicon nitride can be etched in plasma processes similar to those used to etch silicon, that is, plasmas rich in atomic fluorine. A typical example is a CF₄-O₂ plasma [81]. Etching of silicon nitride selectively to silicon is uncommon, but it can be done in a typical silicon dioxide etching process, such as a CF₄-H₂ plasma.

In some applications, the plasma etch rate for a process is measured for a given set of process conditions, and the time to etch is inferred. Such etches provide poor reproducibility, since subtle changes in the etch process or in the film properties can result in unacceptable under- or overetch. One such subtlety is loading effect, the tendency for the

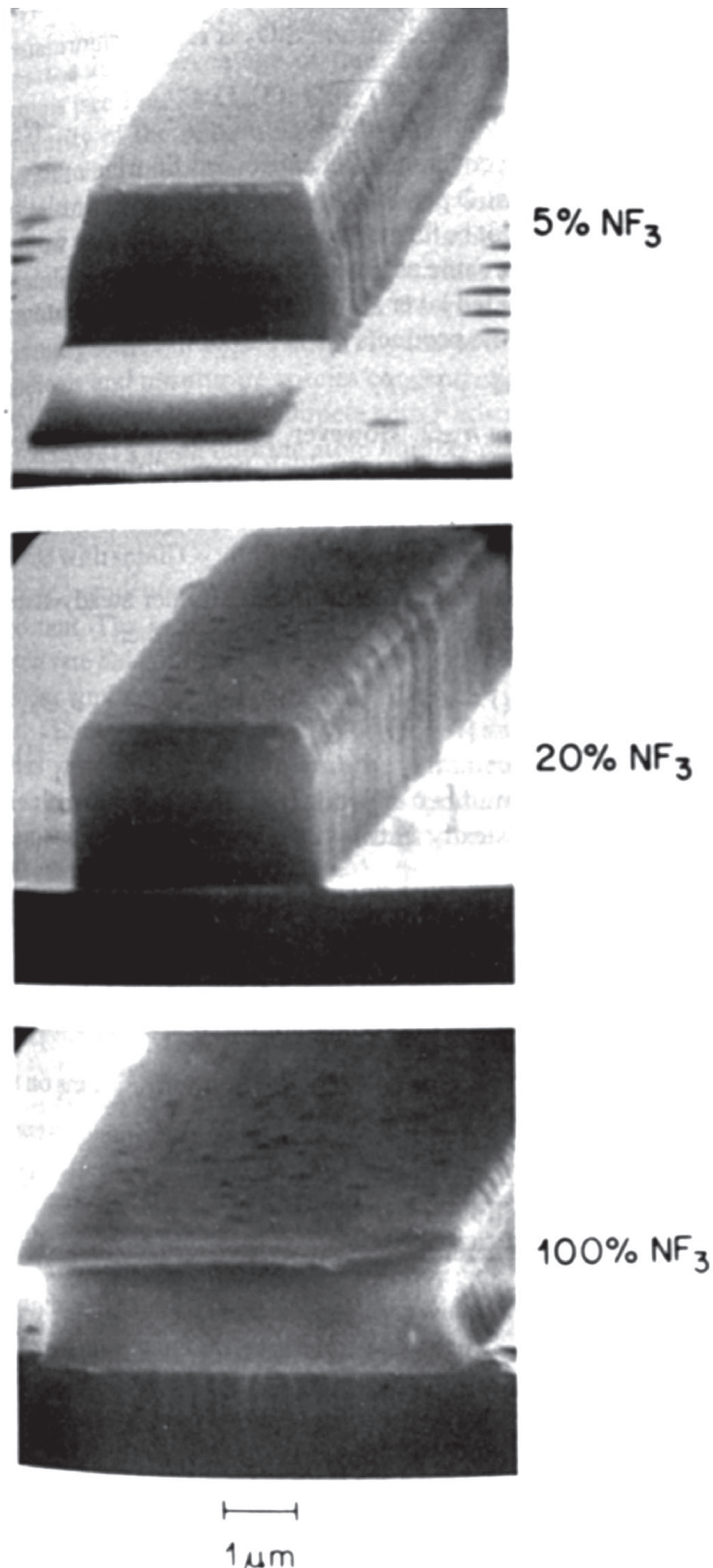


Figure 11.13 Etch profiles of SiO_2 with increasing concentration of NF_3 (after Donnelly et al., reprinted by permission, AIP).

etch rate in many plasma etches to decrease with an increase in the area of the exposed film being etched. Usually, this is caused by a depletion of the reactive species in the plasma. Loading effect can be described by the equation

$$R = \frac{R_o}{1 + kA} \quad (11.8)$$

where R_o is the empty chamber etch rate, A is the area of the exposed film to be etched, and k is a constant [82]. Often k can be reduced by fixing the reactor pressure and increasing the flow of the etch gases, but this approach is subject to pumping limitations. A related problem is aspect ratio dependent etching. For small features with aspect ratios larger than one, the etch rate may slow down as small features are etched. This may be due to consumption of etch species or to gas transport limitations. The result is that small holes or spaces may be underetched, while large open areas are overetched.

If a more repeatable process is required, some method of detecting either the thickness of the film remaining to be etched or the presence of etch by-product in the plasma can be used to determine the etch end point. If the film being etched is transparent, it is possible to use the same constructive and destructive interference effect described in Chapter 4 for measuring oxide thickness. The sum of the reflected and transmitted optical beams will oscillate with film thickness until the transparent layer is removed. This end point method, however, requires a substantial area of unpatterned film to focus and align the laser beam.

Alternatively, one can monitor the chemistry of the plasma either by using mass spectrometry of the etch effluent or by using the peaks of the optical emission spectra. In either case one can look for the extinction of the etch product of the desired film or the emergence of an etch product of the substrate. It is also possible to detect changes in the reactive species. If a substantial part of

EXAMPLE 11.2

A plasma etch process is found to produce an etch rate of 30 nm/min when it is used to etch a single wafer. When a second wafer is added to the reactor, the etch rate falls to 24 nm/min. What etch rates would you expect for three and four wafers?

Solution

Denote the area to be etched on each wafer as A_o and the etch rates as R_n , where n is the number of wafers. Then from Equation 11.8,

$$\frac{R_1}{R_2} = 1.25 = \frac{1 + 2kA_o}{1 + kA_o} \quad (11.9)$$

Solving this equation for the kA_o product gives a value of 1/3. Then, inserting back into Equation 11.8 using either of the two known etch rates gives $R_o = 40$ nm/min. Finally, for three and four wafers, $R_3 = 20$ nm/min, and $R_4 = 17.1$ nm/min.

the gas is consumed by the reaction, the end point will be seen as a sudden increase in the concentration of the etchant. Table 11.4 lists some of the most common etch processes and the associated detection wavelengths. Figure 11.14 shows a commercial research-grade parallel-plate plasma etcher. The system contains two etch chambers fed by a central load lock and robot. Windows are provided at the front of each chamber for possible spectral analysis of the glow discharge.

TABLE 11.4 / CHARACTERISTIC OPTICAL EMISSION WAVELENGTHS USED FOR END POINT DETECTION OF PLASMA ETCH PROCESSES

Film	Etchant	Wavelength (nm)	Emitter
Al	CCl ₄	261.4	AlCl
		396.2	Al
Resist	O ₂	297.7	CO
		308.9	OH
		656.3	H
		615.6	O
Si	CF ₄ /O ₂	703.7	Fl
		777.0	SiF
		288.2	Si
Si ₃ N ₄	CF ₄ /O ₂	337.0	N ₂
		703.7	F
		674.0	N
		184.0	CO
SiO ₂	CHF ₃	184.0	CO
W	CF ₄ /O ₂	703.7	F

After Manos and Flamm [59].

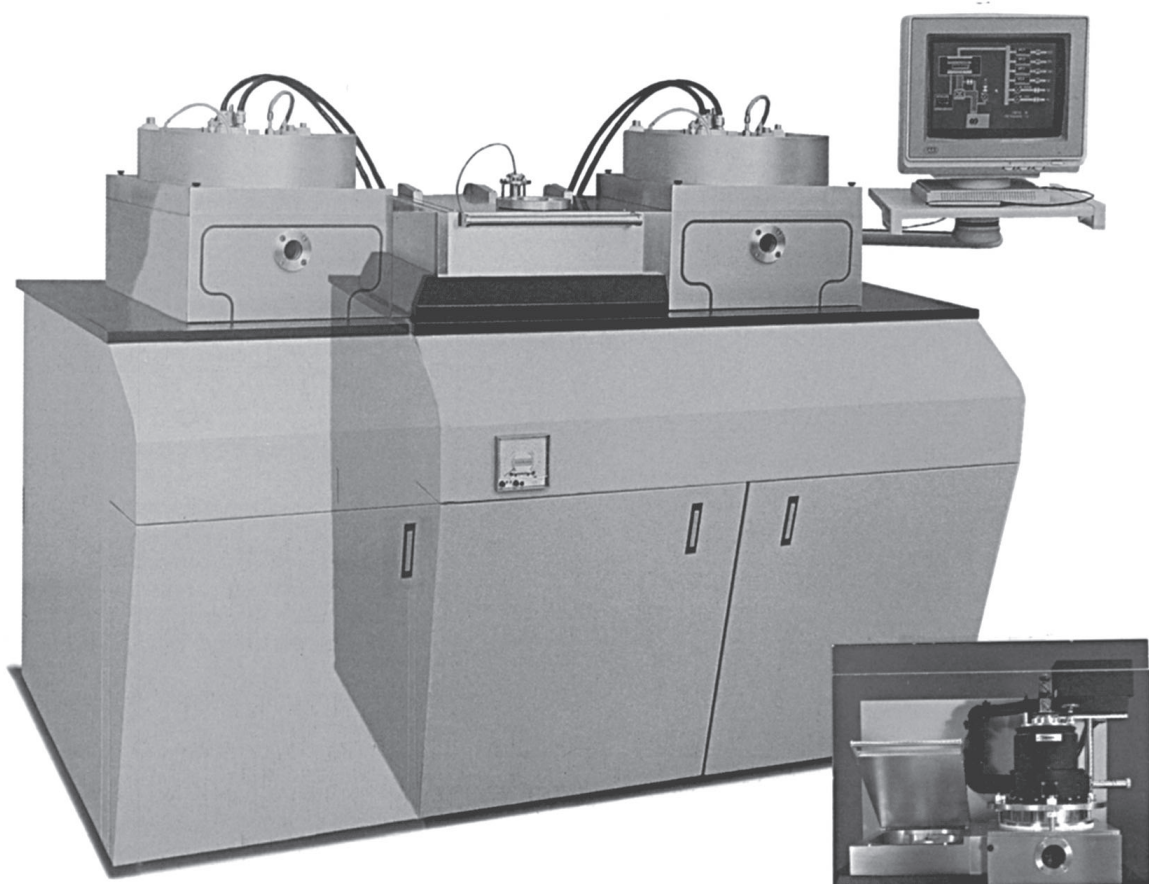


Figure 11.14 A computer-controlled, dual-chamber, parallel-plate plasma etch system (*courtesy of Plasma Therm*).

11.5 ION MILLING

Ion milling is at the opposite extreme of the spectrum of etch processes from high pressure plasma etches. Pure ion milling or ion-beam etching involves no chemical reactions with the etch species, since it uses noble gases such as argon. It is a strictly mechanical process, sometimes called the micromechanical analog of sandblasting. The physics of the etch process is analogous to sputtering. The reader is referred to Sections 12.7 and 12.8 for a review of the physical interactions between incident ions and solid targets. Ion milling has two significant advantages compared to high pressure plasmas: directionality and applicability. The directionality of the erosion is due to the fact that the ions in the beam are accelerated by a strong vertical electric field, and the chamber pressure is so low that atomic collisions are extremely unlikely. As a result, the ions' velocity as they impinge on the surface of the wafer is almost completely vertical. Anisotropic etching is possible for any material because it is chemistry independent, although the sputter yield will vary from one material to another. The second advantage of ion milling is that it can be used to pattern a wide variety of materials including compounds and alloys even if there are no suitable volatile etch products. The erosion rate of the target does not vary by much more than a factor of 3 from material to material. Thus, ion milling is popular for patterning YBaCuO, InAlGaAs, and other ternary and quaternary systems.

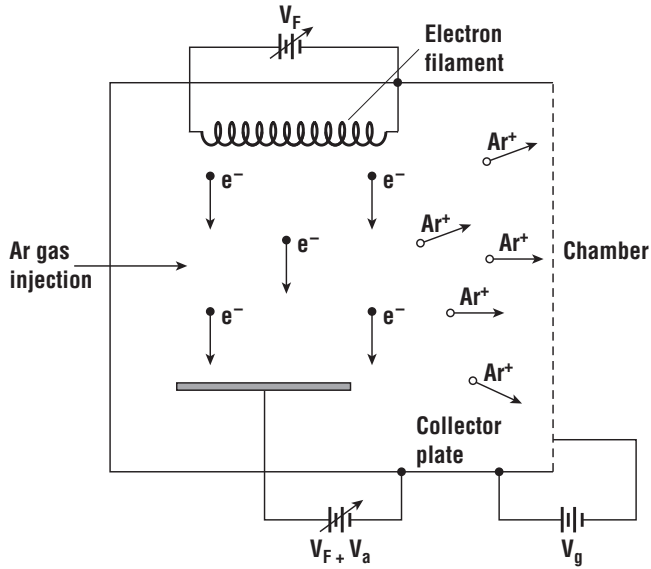


Figure 11.15 Cross section schematic of a Kaufman ion source.

The ability of ion milling to pattern a wide range of materials is also one of its most serious liabilities. The process selectivity to photoresist and underlying layers is generally close to 1:1 unless a chemical component is added to the process. The other drawback with ion milling is throughput. For large silicon wafers, ion milling is normally a single-wafer process. Combined with the low erosion rates and the need for high vacuums, this makes ion milling impractical for high volume manufacturing in silicon-based technologies. For III-V technologies, however, the smaller wafer sizes and reduced number of wafers per lot make ion milling viable.

The most popular source for ion milling is the Kaufman source (Figure 11.15). This basic source was originally developed as a space-based rocket engine [83]. Unlike simple plasma processes, it has direct and independent control over both the ion bombardment energy and ion flux [84, 85]. A Kaufman source has an electron filament heated using the supply V_F . The filament is held at a voltage V_a below the anode potential.

Electrons boil off the filament and are accelerated toward the anode grid. The voltage V_a must be large enough to ensure that the accelerated electrons impact the neutral gas atoms with enough energy to ionize them. Typically, this is about 40 V. Much higher voltages are not desirable, since high energy ions that strike the inside of the chamber walls will erode the chamber and so contaminate the system. To maintain the plasma, the source is held at about 10^{-3} torr.

The source body is perforated on one side. A grid held at a voltage V_g below the target just below this side of the source body accelerates the ejected ions toward the target. Typical accelerating potentials are 500 to 1000 V. Ions arrive at the target surface with an energy given by

$$E_{\text{ion}} = q|V_p - V_g| = q|V_a + V_{pa} - V_g| \quad (11.10)$$

where V_p is the plasma voltage with respect to ground, and V_{pa} is the plasma voltage with respect to the anode. This latter number is determined by the ion flux and the geometry of the discharge. As discussed in Chapter 10, V_{pa} is positive. Because of the large anode area, however, it is only a few volts. The extracted ion energy then is simply controlled by changing V_a or V_g .

To increase the ion density, a magnetic field can be applied to the source as well. Field strengths are about 100 G [86]. (The use of magnetic fields to enhance the ion density in a plasma was discussed in Section 10.7.) Typical Kaufman sources can produce ion currents of almost an ampere over areas as large as 300 mm in diameter. This maximum current is limited by the electric field produced by a high density ion stream. The maximum current is approximately

$$j_{\text{max}} \approx K \sqrt{\frac{q}{m}} \frac{V_t^{3/2}}{I_g^2} \quad (11.11)$$

EXAMPLE 11.3

Calculate the maximum flux from a Kaufman argon source when the potential difference between the grids is 500 V, the grid spacing is 1 mm, and $K = 2 \times 10^{-15}$ F/m. Assume singly ionized argon.

Solution

Substituting $q = 1.6 \times 10^{-19}$ C and $m = 40 \times 1.67 \times 10^{-27}$ kg into Equation 11.11, $j_{\max}$ is directly calculated as 35 mA/m². This corresponds to 2.2×10^{17} ions/m²-sec.

where K is a constant for a given chamber, q/m is the charge-to-mass ratio of the ions, V_t is the potential difference between the screen and accelerator grids, and I_g is the distance between the grids [87]. Typical values of I_g are 1 to 2 mm. These systems produce beams with divergences of 5 to 7°.

Electron cyclotron resonance (ECR) and other advanced plasma sources have now been developed for etching. The basic operation of an ECR plasma is described in Section 10.7. An advantage of such a source for ion milling is the elimination of the filament [88]. This reduces source heating and therefore contamination, and improves system reliability. This advantage is most notable if a reactive species is used rather than argon (see CAIBE, later in this section). By using a large flux at a low energy, such a system may have less substrate damage than reactive ion etchers [89]. The disadvantages of these systems include increased cost and complexity for the source and the need for more expensive pumping systems. Since the flux density in an ion mill is limited by Equation 11.11, substantially higher erosion rates are not obtained with these sources [90] unless modified extraction methods are used.

The ions that are ejected from the source enter the target chamber. To maintain a highly directional etch, the target chamber is pumped to the lowest pressure the incident flux and the pumping speed will allow. This minimizes collisions between the ions and residual gas molecules. Cryopumps or turbomolecular pumps are typically used to evacuate the target chamber. It is normally maintained at a pressure 10 to 100 times lower than the source. Neglecting space charge effects, ions travel in a straight line to the target electrode, which contains the wafers to be milled. Since the ions are positively charged, a voltage will build up on the surface unless the wafer and the film being etched are conductive. To avoid charging effects, an electron flood gun is used. A similar principle is used for maintaining accurate dosimetry in ion implantation (Chapter 5).

Figure 11.16 shows some of the problems that may occur during ion milling. Since the process erodes the mask, any taper in the masking layer will be transferred to the pattern. After the etch is done and the photoresist mask has been removed, the resultant pattern is broadened and appears very similar to an undercut. Since the eroded material from the target is not volatile, some of it will redeposit on the surface of the wafer. This can lead to an uneven etch and a considerable amount of organic residue from the photoresist

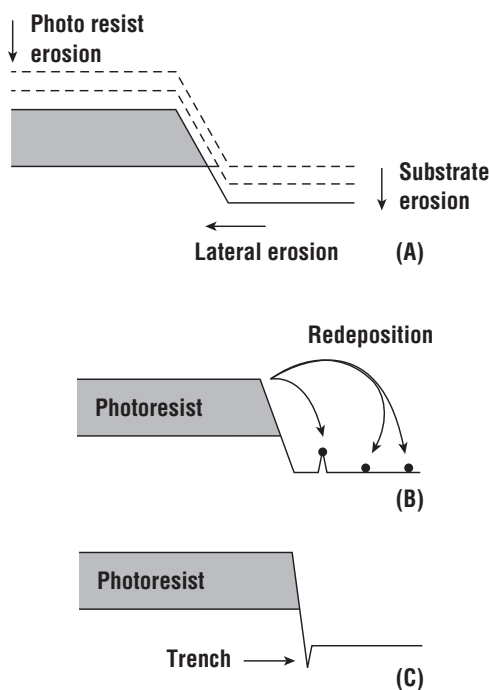


Figure 11.16 Problems that may occur during ion milling: (A) mask taper transfer, (B) redeposition from the mask, and (C) trenching.

mask. The latter problem is particularly pronounced on the sidewalls of the features. Finally, some milling cross sections show an enhanced erosion rate at the edges of the pattern. This problem, called *trenching*, most often occurs when mask erosion causes the sidewalls of the pattern to be tapered at a steep angle. Some of the low angle ions will reflect off the tapered surface toward the pattern edge, where they cause trenches. Commercial ion beam systems often allow the target to be tilted and rotated with respect to the incident beam during milling to minimize these effects [91].

It is necessary to use reactive species to increase selectivity in ion milling. The mixture of ions producing physical damage along with chemical attack provides the second approach to anisotropic etching, since the physical damage occurs primarily on horizontal surfaces. It will be exploited in reactive ion etching, but the name *chemically assisted ion-beam etching* (CAIBE, pronounced kay-bee) or reactive ion milling will be reserved for those processes in which the wafer is in a broad-area, well-collimated ion beam, but not in the plasma chamber itself. An inert species such as argon can be mixed with small amounts of oxygen to reduce the erosion rate of many metals in an ion mill. This has particular applications in the etching of GaAs over $\text{Al}_x\text{Ga}_{1-x}\text{As}$. It has been shown that a 2% O_2 dilution in Ar at 100 eV etches GaAs at hundreds of angstroms per minute, while the etch rate of $\text{Al}_{0.5}\text{Ga}_{0.5}\text{As}$ is not measurable [92].

The difficulty with introducing some reactive species, of course, is that they will tend to attack the source components. In particular, the hot filament is readily attacked. Oxygen is known to simply shorten filament life, but more aggressive precursors such as the halogens may be completely unusable for this reason. Some species may also have problems with gas phase polymerization that leads to coating of the inside of the source. It is therefore necessary to design ion source to accommodate a very reactive plasma. As previously discussed, ECR sources are desirable for this application.

Another way to avoid this problem is to add a reactive bleed near the wafer surface in a conventional ion mill (Figure 11.17). This type of etch, sometimes called an ion-assisted

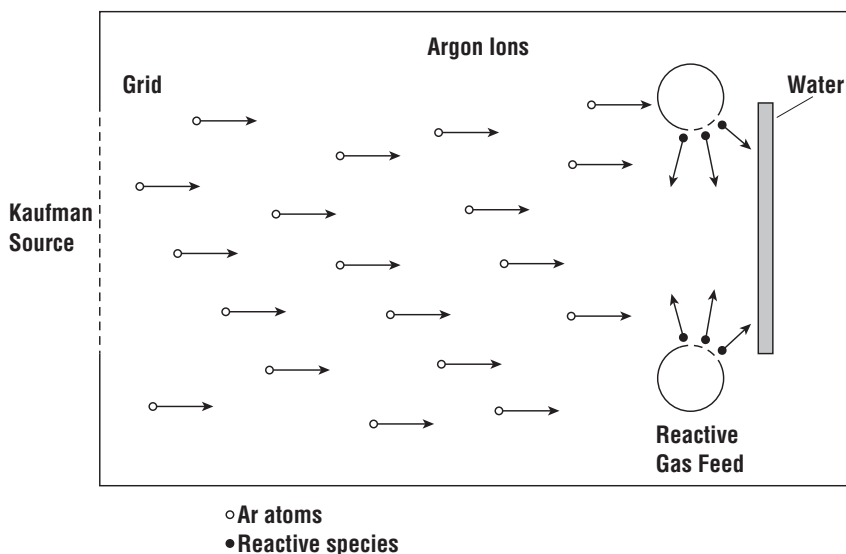


Figure 11.17 The use of a reactive bleed near the wafer surface in a conventional ion mill to introduce a chemical component to the etch process.

chemical etch, proceeds primarily by adsorption of the precursor gas on the wafer surface, simultaneously with ion bombardment. The ion stream leads to both adsorbed species decomposition and substrate damage to drive a chemical reaction. Since the chemical process depends on ion bombardment, however, this type of process cannot achieve the level of selectivity that can be obtained in a purely chemical process.

11.6 REACTIVE ION ETCHING

Reactive ion etching (RIE) was developed because there was a very strong need for an anisotropic etch with much higher selectivity than can be achieved in ion milling. The name is something of a misnomer, since the ions are not the primary etching species in this process. A more appropriate name that is sometimes used is ion-assisted etching, although RIE (pronounced as either R I E or rye) is far more common.

Two common systems for RIE are shown in Figure 11.18. Unlike high pressure plasma etchers, the wafers rest on the powered electrode. In the parallel-plate reactor, the ground electrode is attached to the chamber wall to enlarge its effective area. In the hexode, the ground electrode is the chamber wall. As discussed in Chapter 10, the effect of this arrangement is to increase the potential difference from the plasma to the powered

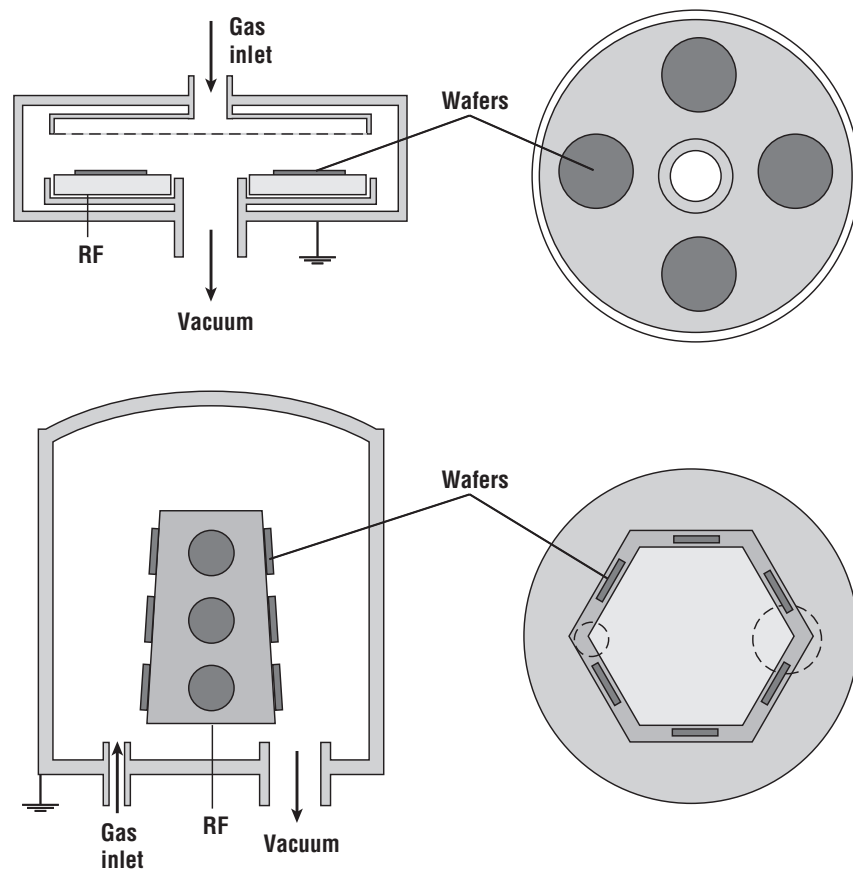


Figure 11.18 Top and side views of parallel-plate and hexode batch RIE systems. Typical conditions for either are 50 mtorr and 5 kW/m². For larger wafers the exhaust in the upper figure is drawn from the periphery rather than the center.

electrode and so the energy of the ion bombardment. For the parallel-plate arrangement to be effective, the plasma must make significant contact with the chamber walls. As pressures increase (>1 torr), the plasma contracts and loses contact with the walls. RIE, however, is done in low pressure plasmas, where the mean free path in the plasma is at least of order millimeters. In this region, the plasma remains in good contact with the walls, and a large potential appears between the plasma and the powered electrode.

Chlorine-based plasmas are commonly used to anisotropically etch silicon, GaAs, and aluminum-based metallizations. Although corrosive, chlorinated precursors such as CCl_4 , BCl_3 , and Cl_2 have high vapor pressures, and both the precursors and etch products are easier to deal with than the comparable bromides or iodides. Fluorine, iodine, and bromine plasmas can also be used under RIE conditions, but the chlorine system will serve as a model for this section.

It is relatively easy to develop a basic understanding of the anisotropic etching of silicon in a chlorine RIE. Undoped silicon etches very slowly in a Cl or Cl_2 ambient without the addition of ion bombardment. Heavily n-type doped silicon or polysilicon, however, spontaneously etches at high rates without bombardment in the presence of Cl , but not in the presence of Cl_2 . The doping enhancement, which can be as much as a factor of 25, depends on the carrier concentration in the film rather than the chemical identity of the dopant [93, 94].

This very pronounced doping effect implies that the chlorine etching process involves electron transfer from the substrate. The model that has developed postulates that in a chlorine plasma, atomic chlorine chemisorbs on the silicon but does not damage the underlying Si–Si bonds. The absorption of more chlorine atoms is impeded by steric hindrance, the repulsion of Cl once a monolayer coverage has been achieved (Figure 11.19). Once the surface chlorine becomes negatively charged, however, it can bond ionically with the substrate. This frees additional chemisorption sites and greatly increases the probability that the chlorine atoms will penetrate the surface and produce volatile silicon chlorides.

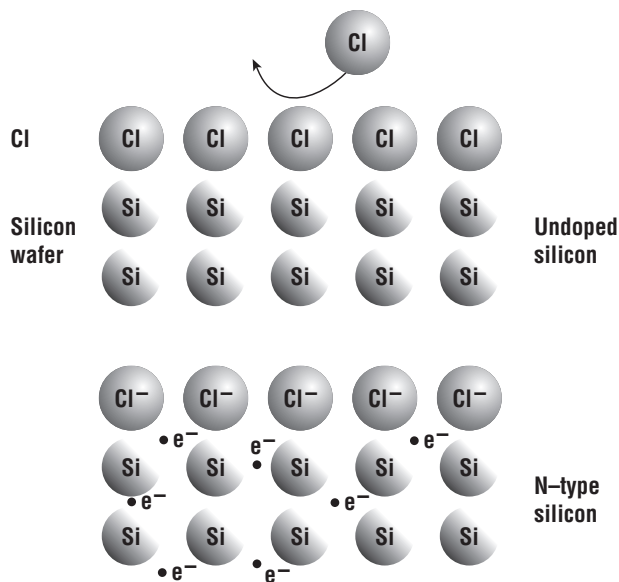


Figure 11.19 Once a monolayer of chlorine atoms has built on the surface, it impedes any chlorine addition.

Chlorine penetration of the surface is also dramatically increased by ion bombardment. As a result, those surfaces subject to ion bombardment etch much more rapidly than those that are not. In particular, the vertical sidewalls receive very little ion bombardment. Because of these effects, the etch profile of undoped polysilicon or single-crystal silicon in a Cl_2 RIE is almost completely anisotropic. Unfortunately, the charge transfer mechanism described earlier produces isotropic etch profiles in heavily doped layers such as N^+ polysilicon gates [95] and aluminum metallizations. In these structures, it is necessary to obtain anisotropic etch profiles through sidewall polymerization schemes. This is commonly done by adjusting the relative concentrations of Cl_2 and an inhibitor-forming gas such as BCl_3 , CCl_4 , or SiCl_4 . It can also be done by combining fluorinated precursors and Cl_2 . A common mixture is 90% C_2F_6 with 10% Cl_2 . By controlling the ratio of Cl to F , one can control the degree of undercut and obtain a range of etch profiles [96]. This is particularly useful in etching multiple layer films such as silicides on

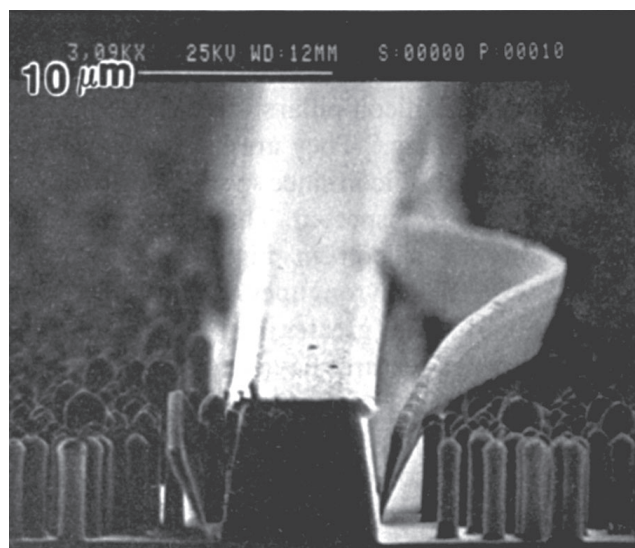
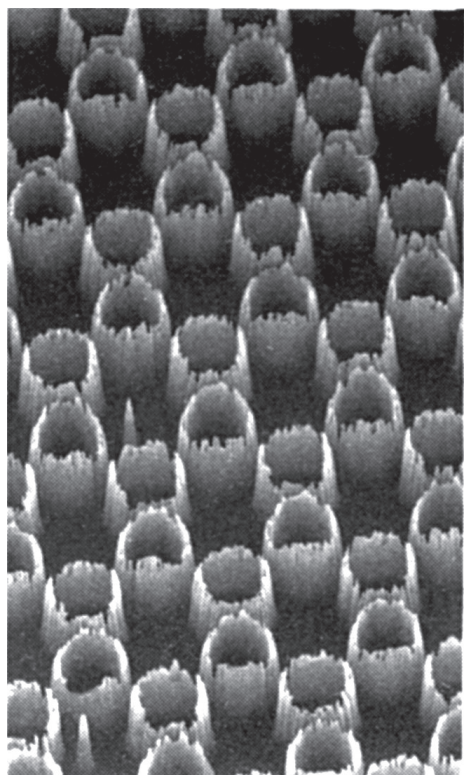


Figure 11.20 Scanning electron micrographs of sidewall passivation films created in a $\text{HCl}/\text{O}_2/\text{BCl}_3$ plasma. In the upper micrograph, the photoresist and silicon posts have been removed by subsequent wet etching. The lower photo shows the sidewall film partially peeled from the etched pattern (after Oehrlein et al., reprinted by permission, AIP).

polysilicon with acceptable profiles [97]. As with many other passivation schemes, the etch rate must be traded off against the etch selectivity.

The lower half of Figure 11.20 shows a silicon line etched with BCl_3 , Cl_2 , and O_2 in a sidewall passivation technique [98]. In this micrograph the sidewall film has begun to peel off the line. Notice that the top of the sidewall film is thicker than the bottom because of the difference in the deposition time. This produces a slight taper in the etch profile. This effect is a serious concern at very small dimensions, where the thickness of the sidewall coating becomes a substantial fraction of the feature size. The sidewall film, which is more clearly shown in the upper film, is almost pure SiO_2 for this etch. The other features in the lower micrograph are sometimes called grass or black silicon [99]. They are due to the unintentional deposition of nonvolatile species and incomplete removal by ion bombardment. Grass appears in a microscope as a darkened area and often occurs when operating a sidewall passivation RIE process under heavy deposition conditions. Grass formation is suppressed by reducing the polymer formation by decreasing the flow of BCl_3 , increasing the O_2 concentration, or by increasing the ion bombardment by reducing the pressure or increasing the power.

Reliable and repeatable etching of aluminum and aluminum-based compounds requires considerable attention to detail. Aluminum readily oxidizes to form Al_2O_3 , which etches very slowly in most Cl plasmas. To avoid problems with etch uniformity and to maintain proper etch timing, a short sputter etch in Ar or an appropriate chemical RIE can be used before beginning the Cl -based RIE. At the end of the etch, it is also necessary to remove any adsorbed chlorinated species from the surface of the wafer. When the wafers are removed from the vacuum chamber, these compounds can react with moisture in the air to form hydrochloric acid, leading to metal corrosion. Several methods have been developed to avoid this problem. The simplest is a dip in deionized water immediately after the etch. Other postetch treatments can be done inside the vacuum chamber. These include an inert sputter etch, an oxygen plasma, or a fluorinated plasma to displace the

adsorbed chlorine atoms [100]. If an insufficient clean is carried out, metal lines will have small voids, called mouse bites, along the line edges.

A problem related to etching aluminum compounds is the volatilization of silicon and/or copper additives to the metal. Copper residues are especially difficult to remove due to the low vapor pressures of these copper chlorides at room temperature. Furthermore, the copper residues are even more prone to corrosion than their aluminum counterparts. Etching compounds with greater than 2% copper generally require increased ion bombardment and/or heated substrates. Another way to etch these compounds is the use of sacrificial aluminum in the etch chamber to provide a sufficient amount of AlCl_3 , an etch product that helps volatilize copper chlorides.

Finally, a serious problem in chlorinated RIE is resist erosion due to Cl attack. This is particularly aggravated in aluminum RIE because of the thickness of typical interconnect layers, the topology that may exist, the presence of the etch product AlCl_3 , which also accelerates resist attack, and the tendency for elevated substrate temperatures that increase the resist erosion rate. Some resist vendors supply chlorine-resistant resists to address this problem, but even with these resists, erosion remains a concern.

Most anisotropic etching of GaAs is also done in chlorinated reactive ion etchers. Purely chemical, isotropic etching occurs in high pressure plasmas, while anisotropic etching occurs for chamber pressures of less than 10 mtorr under strong ion bombardment [101]. It is believed that the primary group III by-product, GaCl_3 , accumulates on the surface of the wafer [102], even though the compound is reported to have a high vapor pressure. Due to differences in the etch rates of group III and group V halides, GaAs etches more rapidly along some crystal planes than in others. In low power, high pressure Cl_2 plasmas, significant faceting can occur. To avoid this problem, compounds may be added to form polymers in the plasma and passivate the sidewalls.

Another chemistry that can be used for anisotropically etching GaAs is hydrogen based. Arsenic, of course, forms several hydrides, the most stable of which is AsH_3 . Given the toxicity of AsH_3 , great care must be taken in treating the effluent. To volatilize gallium, 5 to 25% methane must be added [103]. The maximum etch rate occurs at about 500 K [104]. As will be discussed in Section 14.9, both the long-lived radical monomethyl gallium and the stable compound trimethyl gallium [$\text{Ga}(\text{CH}_3)_3$] are volatile products. At high methane concentrations, however, excessive polymerization occurs and etching stops. Anisotropic etching with very high etch rates has also been demonstrated with chloromethanes [105].

In fluorinated RIE, as in chlorinated RIE, etch anisotropy may be due to either sidewall passivation, physical damage of the horizontal surfaces, or some combination of the two. The physical damage mechanism is believed to be described by the chemical sputtering model [106]. In this model, the ion bombardment supplies energy, increasing the mobility and reactivity of surface species. The development of anisotropic etch profiles due to sidewall passivation was discussed in a previous section. In such a process, some ion bombardment of the surfaces is required to allow any etching at all [107]. In reactive ion etching, there is a substantial ion bombardment, suggesting that these tools may also be used with fluorinated chemistries. The high energy bombardment in RIE, however, damages the substrate, particularly when etching SiO_2 over Si. This will be discussed in the next section.

11.7 DAMAGE IN REACTIVE ION ETCHING⁺

One of the limitations of reactive ion etching is residual damage left in the substrate after the etch. Typical ion fluences of 10^{15} ions/cm² are delivered at energies of 300 to 700 eV in

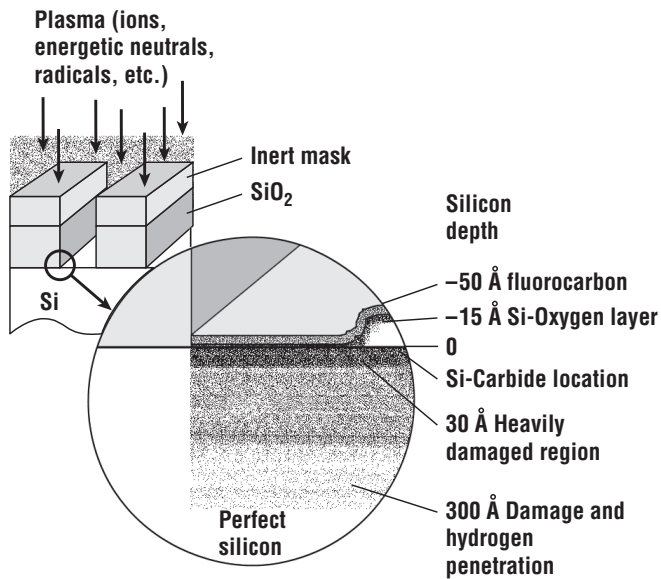


Figure 11.21 A cross section schematic of the results of a typical etch of SiO_2 down to Si using CF_4/H_2 (after Oehrlein, Rembetski, and Payne, reprinted by permission, AIP).

a RIE. Both substrate damage [108] and chemical contamination are serious issues. The latter is a particular concern in polymerization etches, which are known to leave behind residual films. Gas phase particle deposition is also a significant problem [109]. Furthermore, one can often find metallic impurities, including Fe, Ni, Na, Cr, K, and Zn, on the surface of the wafer after the etch [110] due to sputtering of the electrodes, chamber, and fixtures in contact with the plasma. Techniques developed for the removal of these impurities include O_2 plasma treatments followed by wet acid cleaning [111, 112] and H_2 plasma treatments [113]. The drawback of these postetch treatments is the increased complexity of the process.

Physical damage and drive-in of impurities are a second class of problem with RIE. After a typical etch in a carbon-containing RIE, the top 3 nm is heavily damaged with an extensive concentration of Si–C bonds, while significant damage is as deep as 30 nm [114]. RIE processes done in a hydrogen-containing ambient also have Si–H defects that can be observed electrically as deep as 40 nm [115] and

are very difficult to remove [116]. Hydrogen may actually penetrate several microns into the surface, where it can deactivate dopants in the substrate [117]. Figure 11.21 shows a cross section schematic of the results of a typical etch of SiO_2 down to Si [98]. Removal of this damage requires an initial clean followed by annealing at temperatures of over 800°C [118]. It is also possible to design RIE processes without hydrogenated species [119].

EXAMPLE 11.4 / ETCHING A 0.5-MICRON-WIDE TRENCH USING ATHENA ELITE

Use the following deck:

Go Athena

```
#TITLE: Trench etch using rie model
```

```
#
```

```
line x loc=0.00 spac=0.05
```

```
line x loc=2.00 spac=0.05
```

```
line y loc=0.00 spac=0.05
```

```
line y loc=0.00 spac=0.05
```

```
init orientation=100 space.m=1
```

```
# Deposit oxide to serve as an etch mask
```

```
deposit oxide thick=0.10 div=5
```

```
# Remove oxide in 0.5 um area to be etched by defining the  
four corners of the removal area
```

```
etch oxide start x=0.75 y=-10
```

```

etch cont x=0.75 y=10
etch cont x=1.25 y=10
etch done x=1.25 y=-10
# Define how the etch machine 11_3 etches silicon and
oxide.
# Chemical is a uniform etch rate in nm/min directional
is the etch rate in the ion direction in nm/min
# Divergence is the angular divergence of the ions
rate.etch machine=11_3 rie silicon n.m chemical=35
directional=90 divergence=40
rate.etch machine=11_3 rie oxide n.m chemical=3.0
directional=15 divergence=40
#
etch mach=11_3 time=5.0 minutes dx.mult=.5
structure outfile=anelex 18.str
tonyplot anelex 18.str
quit

```

Solution

In this example, which uses the ELITE routine from Silvaco's Athena code, SiO_2 is used as a hard mask for the etch. Comparing the final profile (Figure 11.22) with the input deck, you can see that some of the oxide was lost during the etch. Also note that the beam is not perfectly normal to the surface. This leads to a shaped profile in the final trench. You can try adjusting the divergence parameter or the ratio of the nondirectional (chemical) etch rate to the directional etch rate to get a flavor for what happens.

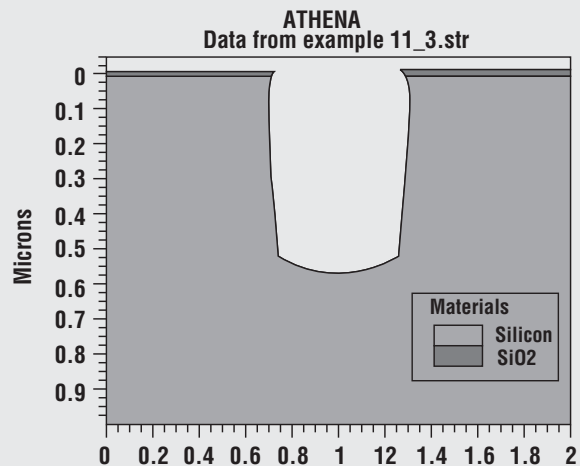


Figure 11.22 Etching a trench 0.5 μm wide.

11.8 HIGH DENSITY PLASMA (HDP) ETCHING

Some of the first uses of high density plasma systems, introduced in Chapter 10, were for etching. Perhaps this is because the benefits of using an HDP system were more obvious than were those for other plasma processes. High density sources use crossed magnetic and electric fields to dramatically increase the distance that free electrons in the plasma travel. This, in turn, increases the rate of dissociation and ionization as compared to a simple diode plasma operating at the same pressure. This high density of ions and radicals can be used to increase

the etch rate, or they can be traded off against other parameters. For example, one can obtain acceptable ion and radical densities at very low pressures in an HDP. This allows one to decouple the bias on the wafer-containing electrode from the ion density. Often this is done in HDP etch systems by attaching the wafer-containing electrode to a second RF source. The dc bias is set by the RF power of this second source. Because of the long mean free path in the system at low pressure, substrate biases of 10–30 V are often enough to produce anisotropic etching. This low energy can provide large selectivities and produce little residual damage. This is extremely useful for etching down to very thin layers (as in the gate etch for CMOS) or for etching contacts down to very thin junctions, or for etching down to active layers such as the poly etch process for a double-poly bipolar process. Furthermore, etching at lower pressures ensures more vertical incidence of the ions and therefore less reduction of the etch rate for high aspect ratio features [120], an effect that is sometimes called *microloading* [121]. The HDP source provides a high concentration of these low energy ions, ensuring acceptable etch rates. One disadvantage of HDP etching is that the high ion fluence can charge floating structures, like MOS gates, excessively. This can lead to excess leakage in the gate insulator due to residual etch damage [122]. An overview of conventional and HDP etching is given by Sugawara [123].

When sidewall passivation is used to produce an anisotropic etch, the low pressure used in most HDP etchers severely restricts the production of the nonvolatile species. This may simply be a matter of increasing the flow ratio of the BCl_3 to Cl_2 or CH_2F_2 to CF_4 , for example. At these high ratios of polymer formation, however, nonvolatile species will build up on the chamber walls. Eventually this buildup flakes off, depositing dust on the wafers. Commonly, O_2 plasma cleans

along with wall heating are used to control polymeric buildup in HDP systems [124]. Wall temperature can also be used to fine-tune the etch selectivities and/or the etch rate uniformity. Alternatively, some geometries can be employed that prevent the plasma from reaching the walls of the chamber to minimize contamination.

The first HDP sources applied to etching were electron cyclotron resonance (ECR) systems [125]. Both magnetic coil and permanent magnets [126] have been used on the walls of the reactor to achieve the resonance condition. The critical concern is obtaining sufficient uniformity over a broad area to get uniform etch rates. Coil systems allow real-time changes in the magnetic field, while permanent magnets often provide more localized fields. Typical ECR etch systems use a 2.45-GHz source. This requires a field of 875 G to achieve resonance. The plasma products are transported to the surface of the wafer with a divergent magnetic field [127]. Typical ECR etch pressures are 0.1 to 10 mtorr. Typical plasma powers are 10 to 100 W.

As an example of the use of an ECR plasma, consider a gate etch. This requires etching 300 nm of polysilicon down to 1.5 nm of SiO_2 . Obviously, a very



Figure 11.23 The Applied Materials high density plasma silicon etch system (photo courtesy of Applied Materials).

high selectivity will be required for etching silicon over oxide. A high selectivity to the resist is also desirable to improve the linewidth control. From the previous discussion we know that Cl can be used to selectively etch silicon over SiO₂, but anisotropy can be achieved only in undoped films or with a sidewall passivation technique. Since silicon dioxide does not react chemically with Cl radicals, the etch rate is negligible if no sputtering of the film occurs. The Cl⁺ sputter threshold for Si is about 20 eV, while that of SiO₂ is about 50 eV [128]. Thus an ECR operating with chlorine ion energies between 20 and 50 eV should obtain extremely high selectivities for Si over SiO₂. Kanai *et al.* demonstrated a selectivity of 200:1 at low power in such a system [129].

Perhaps one of the most popular types of HDP etch systems is the inductively coupled reactor. HDP systems can be divided into the cylindrical coil or vertical barrel type of system, and the planar coil system. The former is shown in Figure 11.23. One of the challenges of designing a planar coil system is ensuring a uniform plasma density, since the reactor tends to have a peak under the center of the coil. This problem gets progressively more difficult as the wafer size increases. The typical coil-to-wafer spacing is 3 to 8 cm. Inductively coupled systems do not use an externally applied magnetic field. Instead, RF current through the coil produces an oscillating magnetic field that creates an electric field as described by Faraday's law. This induced magnetic field alters the path of the electrons in the plasma, increasing the plasma density.

ICP systems are widely used for gate etching due to their ability to obtain high silicon-to-oxide selectivity at low power. Typical ICP power for gate etching is approximately 50 W. For silicon trench etching higher etch rates are desirable since trench depths can be of the order of 10 μm for DRAM technologies. At 200 to 800 W the selectivity of silicon over oxide decreases significantly [130]; however, selectivity is not a concern in this type of etch. At high power densities the anisotropy can decrease due to the high concentration of reactive radicals. This can be countered by increasing the substrate bias and/or using sidewall passivation.

GaN is generally etched in chlorine chemistries in ICP and RIE. The most common is BCl₃/Cl₂ [131]. In general, increasing the Cl₂ concentration leads to increased etch rates. Adding N₂ and SF₆ to Cl₂ decreases the etch rate; however, adding N₂ and SF₆ to BCl₃ improves the GaN etch rate to a point [132]. This tendency is similar to that observed in ICP etching of GaAs, GaP, and In-containing materials. Simply adding N₂ to BCl₃ can increase the etch rate by as much as a factor of 5. This was found to be due to scavenging of B with N, creating higher Cl radical concentrations [133]. High etch rates (up to 700 nm/min) can also be obtained in a Cl₂/H₂/Ar mixture [134]. Residual damage is a concern in these materials [135]. Electrical transport and contact resistance can degrade after etching.

All three types of high density sources have been applied to etching. All three produce similar etch rates and etch profiles for similar etch chemistries [136]. Often the choice comes down to parameters such as uniformity, repeatability, ease of use, starting effects, and source compatibility with the etcher geometry.

11.9 LIFTOFF

Most GaAs technologies were developed around liftoff rather than etching. The process is still popular as an alternative to ion milling for patterning difficult to etch materials. The

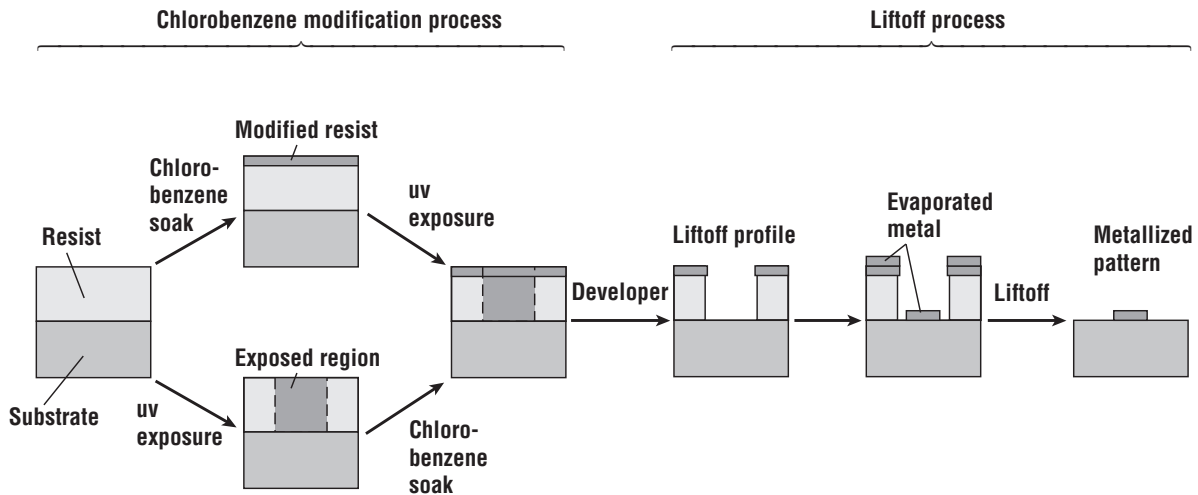


Figure 11.24 Process sequence for a liftoff operation (after Hatzakis et al., © 1980 International Business Machines Corporation).

sequence for liftoff is shown in Figure 11.24. A thick layer of resist is spun and patterned. Next, a thin layer of metal is deposited using evaporation (Chapter 12). One characteristic of evaporation is its difficulty in covering high aspect ratio features. If a reentrant profile is obtained in the resist, a break in the metal is virtually assured. Next, the wafer is immersed in a solution capable of dissolving the photoresist. The metal lines that were deposited directly on the semiconductor remain, while the metal deposited on the resist lifts off of the wafer as the resist dissolves. Etch damage to the substrate is avoided and the lines patterned with infinite selectivity with no undercut. Since the process in its simplest form requires only a wet bench and perhaps ultrasonic agitation, it is widely used in research laboratories.

Methods that have been used to form a reentrant resist profile generally harden the surface of the resist. This can be done to some extent by promoting cross-linking by deep UV exposure, in a suitable plasma environment, or by ion implantation. Another solution is the use of multiple layers of resist such as a DQN resist on PMMA. After PMMA coating, the upper layer of resist is spun, baked, exposed, and developed as normal with a UV source. The patterned upper layer can then be used as a mask for a deep UV exposure of the PMMA, which is then overdeveloped using a solution that does not attack the upper resist. The result is a pronounced ledge that is very difficult to cover. Due to the complexity of multilayer resist processing, the most popular method of producing reentrant profiles is soaking a single-layer DQN resist after softbake in chlorobenzene [137, 138] or similar compounds. Typical soak times are 5 to 15 min. The soak process reduces the dissolution rate of the upper surface of the resist [139]. After developing the pattern, therefore, a ledge appears (Figure 11.25). The thickness of the ledge depends on the soak time, the temperature of the soak bath, and the resist prebake cycle [140].

Liftoff processes have several shortcomings. The first is that the surface topology must be very smooth, since the metal deposition step is designed to have poor step coverage. Therefore, either the technology must be limited to one layer of metallization, or each layer must be planarized before liftoff patterning. This effectively prevents the use

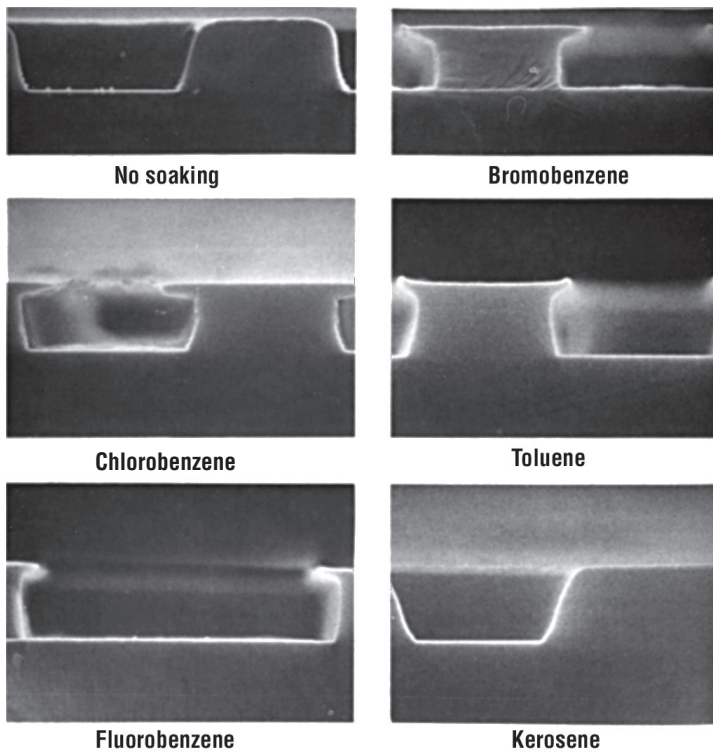


Figure 11.25 Liftoff profiles after various resist treatments (after Hatzakis et al., © 1980 International Business Machines Corporation).

of sputtering. Even if the layer is planarized, contact holes must have a low aspect ratio. The other serious problem is that the metal lifted off remains solid and floats in the bath. Pieces of it are very likely to redeposit on the surface of the wafer. Unless the patterns are very simple, liftoff has serious yield impacts.

11.10 SUMMARY

This chapter reviewed a variety of etch techniques that ranged from the purely physical (ion milling) to the purely chemical (wet etching). In between the two extremes are chemically assisted ion-beam etching, reactive ion etching, and high pressure plasma etching. Generally, the greater the degree of ion bombardment, the higher the etch anisotropy, but the lower the selectivity. Sidewall passivation was introduced as a technique for retaining high etch anisotropy with good selectivity. A wide variety of etches is used. Two of the most common, fluorine and chlorine plasma, have been described in some detail. Liftoff processes were developed to avoid the need for etching altogether. In these processes, the resist is patterned before metal deposition.

Problems

1. A solution consisting of four parts 70% HNO_3 , four parts 49% HF , and two parts $\text{HC}_2\text{H}_3\text{O}_2$ is used to etch silicon. If the solution is held at room temperature, what etch rate would you expect? If the compound is to remain at two parts $\text{HC}_2\text{H}_3\text{O}_2$, what mixture of these same chemicals would be suitable to etch silicon at a rate of approximately $10 \mu\text{m}/\text{min}$?
2. A hole must be wet-etched through a silicon wafer that is $700 \mu\text{m}$ thick. A mixture of two parts of $\text{HC}_2\text{H}_3\text{O}_2$, two parts of 49.2% HF , and six parts of 69.5% HNO_3 is mixed together to do the etch.
 - (a) How long should the etch take?
 - (b) The etch is found to take nearly twice as long as predicted. Assuming that the initial concentrations of the proper chemicals are used, list three things that might have caused the reduction in the apparent etch rate and what you would do to solve each one.
3. Consider the GaAs etch diagram (Figure 11.6). The left axis is for H_2O_2 , the right axis is for H_2SO_4 , and the bottom axis is for water. A solution of 30% H_2O_2 , 50% H_2SO_4 , and 20% water is made up and used for etching a GaAs wafer.

- (a) Estimate the etch rate.
 - (b) In practice it is found that the deposition rate slows with time. Suggest two possible mechanisms for this slowdown.
 - (c) Would you expect this etch to be isotropic or anisotropic? Justify your answer. Remember that not all wet etches are isotropic.
4. One can etch SiO_2 using HF vapor. In this technique, the wafer is suspended above a bath of HF and the vapor comes off of the surface of the liquid and then diffuses through the air to the surface of the wafer, where it reacts with the oxide.
- (a) Assume that the process is limited by the flux of HF molecules to the surface of the wafer, and that, for the conditions used, the partial pressure of HF near the wafer is 100 torr. If it takes four HF molecules to be incident on the surface to remove a single silicon atom from the SiO_2 , and the density of silicon atoms in SiO_2 is $2 \times 10^{22} \text{ cm}^{-3}$, determine the expected etch rate at room temperature. (You can assume that the oxygen immediately volatilizes once the silicon is removed.)
 - (b) The measured etch rate is many orders of magnitude less than the answer from part (a). It is found to be a sensitive function of the wafer temperature, with higher wafer temperatures resulting in higher etch rates. List two possible explanations for the lower etch rates that would be consistent with the observed temperature dependence.
5. An etch engineer has only a high pressure plasma etch and an ion mill available. Select which you would use in the following applications. Be sure to justify your answer.
- (a) Etching a 500-nm polysilicon layer that serves as the upper electrode of a large square capacitor. The capacitor dielectric is 5 nm of SiO_2 .
 - (b) Recessing the channel of a GaAs FET. For this application, the residual etch damage must be minimized.
 - (c) Anisotropic patterning of a thin layer of $\text{YBa}_2\text{Cu}_3\text{O}_7$ on a thick insulating layer.
6. An ion mill is used to etch a feature into a silicon wafer. The mill uses the ion source and conditions described in Example 11.3.
- (a) What etch rate of silicon would you expect?
Hints: (1) The sputter yield for Ar^+ is given in Figure 12.14; (2) the number density of an elemental solid is the mass density divided by the atomic weight.
 - (b) The process is found to have a poor selectivity to the photoresist. What could you do to increase the silicon removal rate to try to obtain a better selectivity?
 - (c) Would you expect the process to be nearly isotropic or nearly anisotropic? Assume vertical resist walls.
7. A cylindrical parallel-plate RF etch chamber is constructed with 12-in.-diameter electrodes. The chamber diameter is 18 in. and the height of the chamber is 6 in. One of the electrodes is attached to ground. The dc voltage between the electrodes is measured to be 20 V when a plasma is established. Assuming that the plasma is in contact with the chamber walls, calculate the potential difference between the plasma and each electrode. Explain the significance of the result.
8. Describe the differences between high pressure plasmas and reactive ion-etch systems. Explain when each is the preferred process.
9. Describe the difference between chemically assisted ion beam etching (CAIBE) and ion-assisted chemical etching.

References

1. W. A. Kern and C. A. Deckert, "Chemical Etching," in *Thin Film Processing*, J. L. Vossen, ed., Academic Press, New York, 1978.
2. K. McAndrews and P. C. Subanek, "Nonuniform Wet Etching of Silicon Dioxide," *J. Electrochem. Soc.* **138**:863 (1991).
3. P. Burggraaf, "Wet Etching: Alive, Well, and Futuristic," *Semicond. Int.* **58** (July 1990).
4. www.matech.com
5. K. R. Williams and R. S. Muller, "Etch Rates for Micromachining Processes," *J. Microelectromech.* **5**(4) (1996).
6. W. Kern, "Chemical Etching of Dielectrics," in *Etching for Pattern Definition*, H. G. Hughes and M. J. Rand, eds., The Electrochemical Society, Pennington, NJ, 1976.
7. S. M. Hu and D. R. Kerf, "Observation of Etching of n-Type Silicon in Aqueous HF Solutions," *J. Electrochem. Soc.* **114**:414 (1967).
8. J. S. Judge, in *Etching for Pattern Definition*, H. G. Hughes and M. J. Rand, eds., The Electrochemical Society, Princeton, NJ, 1976.
9. M. Prigogine, and J. J. Fripiat, *J. Chem. Phys.* **76**:26 (1979).
10. L. M. Loewenstein and C. M. Tipton, "Chemical Etching of Thermally Oxidized Silicon Nitride: Comparison of Wet and Dry Etching Methods," *J. Electrochem. Soc.* **138**:1389 (1991).
11. J. T. Milek, *Silicon Nitride for Microelectronic Applications, Part 1—Preparation and Properties*, IFI/Plenum, New York, 1971, p. 1.
12. B. Schwartz and H. Robbins, "Chemical Etching of Silicon: Etching Technology," *J. Electrochem. Soc.* **123**:1903 (1976).
13. For a comprehensive listing of etching solutions for groups III–V, see Kern and Deckert [1] and references therein.
14. R. E. Williams, *Gallium Arsenide Processing Techniques*, Artech, Dedham, MA, 1984.
15. S. Adache and K. Oe, "Chemical Etching Characteristics of (001) GaAs," *J. Electrochem. Soc.* **130**:2427 (1983).
16. Y. Tarui, Y. Komiya, and Y. Harada, "Preferential Etching and Etched Profiles of GaAs," *J. Electrochem. Soc.* **118**:118 (1971).
17. D. W. Shaw, "Enhanced GaAs Etch Rates Near the Edges of a Patterned Mask," *J. Electrochem. Soc.* **113**:958 (1966).
18. J. J. Gannon and C. J. Nuese, "A Chemical Etchant for the Selective Removal of GaAs Through SiO₂ Masks," *J. Electrochem. Soc.* **121**:1215 (1974).
19. S. Iida and K. Ito, "Selective Etching of Gallium Arsenide Crystals in the H₂SO₄-H₂O₂-H₂O System," *J. Electrochem. Soc.* **118**:768 (1971).
20. R. A. Logan and F. K. Reinhart, "Optical Waveguides in GaAs-AlGaAs Epitaxial Layers," *J. Appl. Phys.* **44**:4172 (1973).
21. J. J. LePore, "Improved Technique for Selective Etching of GaAs and Ga_{1-x}Al_xAs," *J. Appl. Phys.* **51**:6441 (1980).
22. R. P. Tijburg and T. van Dongen, "Selective Etching of III–V Compounds with Redox Systems," *J. Electrochem. Soc.* **123**:687 (1976).
23. D. G. Hill, K. L. Lear, and J. S. Harris, Jr., "Two Selective Etching Solutions for GaAs on InGaAs and GaAs/AlGaAs on InGaAs," *J. Electrochem. Soc.* **137**:2912 (1990).
24. L. Ma, K. Fareen Adeni, C. Zeng, Y. Jin, K. Dandu, Y. Saripalli, M. Johnson, and D. Barlage, "Comparison of Different GaN Etching Techniques," *CS MANTECH Conference*, pp. 105–108, April 24–27, 2006.

25. D. A. Stocker, E. F. Schubert, and J. M. Redwing, "Crystallographic wet chemical etching of GaN," *Appl. Phys. Lett.* **71**(15) (1997).
26. G. C. DeSalvo *et al.* "Wet Chemical Etching of GaAs at Room Temperature," *J. Electrochem. Soc.* **143**(11) pp. 3652–3656 (1996).
27. K. E. Bean, "Anisotropic Etching of Si," *IEEE Trans. Electron Dev.* **ED-25**:1185 (1978).
28. S. Wolf and R. N. Tauber, *Silicon Processing for the VLSI Era*, Vol. 1, Lattice Press, Sunset Beach, CA, 1986.
29. D. L. Kendall and G. R. de Guel, in *Orientation of the Third Kind: The Coming Age of (110) Silicon Micromachining and Micropackaging of Transducers*, C. D. Fung, P. W. Cheung, W. H. Ko, and D. G. Fleming, eds., Elsevier, Amsterdam, 1985, p. 107.
30. P. D. Greene, "Selective Etching of Semi-Insulating Gallium Arsenide," *Solid-State Electron.* **19**:815 (1976).
31. D. G. Schimmel, "Dry Etch for <100> Silicon Evaluation," *J. Electrochem. Soc.* **126**:479 (1979).
32. F. Secco d'Aragona, "Dislocation Etch for (100) Planes in Silicon," *J. Electrochem. Soc.* **119**:948 (1972).
33. E. Sirtl and A. Adler, *Z. Metallk.* **52**:529 (1961).
34. W. C. Dash, "Copper Precipitation on Dislocations in Silicon," *J. Appl. Phys.* **27**:1193 (1956).
35. H. Muraoka *et al.*, "Controlled Preferential Etching Technology," in H. R. Huff and R. R. Burgess, eds., *Semiconductor Silicon 73*, The Electrochemical Society, Pennington, NJ, 1973, p. 327.
36. J. C. Greenwood, "Ethylene Diamine-Catechol-Water Mixture Shows Preferential Etching of p-n Junction," *J. Electrochem. Soc.* **116**:1325 (1969).
37. *Chemical Mechanical Polishing Equipment and Materials* (AVM047B) from BCC Research (2008).
38. R. Jairath, D. Mukesh, M. Stell, and R. Tolles, "Role of Consumables in the Chemical-Mechanical Polishing (CMP) of Silicon Oxide Films," *Proc. 1993 ULSI Symp.* (October 1993).
39. M. A. Fury, "Emerging Developments in CMP for Semiconductor Planarization," *Solid State Technol.* **47** (April 1995).
40. G. Nanz and L. E. Camilletti, "Modeling of Chemical-Mechanical Polishing: A Review," *IEEE Trans. Semicond. Manuf.* **8**:382 (1995).
41. F. Malik and M. Hasan, "Manufacturability of the CMP Process," *Thin Solid Films* **270**:612 (1995).
42. F. Kaufman, S. Cohen, and M. Jaso, "Characterization of Defects Produced in TEOS Thin Films Due to Chemical Mechanical Polishing (CMP)," in *Ultraclean Semiconductor Processing Technology and Surface Chemical Cleaning and Passivation*, MRS 386, Materials Research Society, Pittsburgh, 1995, p. 85.
43. W. L. Patrick, W. L. Guthrie, C. L. Standley, and P. M. Schiabile, "Application of Chemical-Mechanical Polishing to the Fabrication of VLSI Circuit Interconnections," *J. Electrochem. Soc.* **138**(6):1778 (1991).
44. B. Davari, C. W. Koburger, R. Schulz, J. D. Warnock, T. Furukawa, M. Jost, Y. Taur, W. G. Schwittek, J. K. DeBrosse, M. L. Kerbaugh, and J. L. Mauer, "A New Planarization Technique Using a Combination of RIE and Chemical Mechanical Polish (CMP)," *IEDM Tech. Digest*, 1989, p. 61.
45. P. Singer, "Chemical-Mechanical Polishing: A New Focus on Consumables," *Semiconductor Int.* **48** (February 1994).

46. J. M. Steigerwald, R. Zirpoli, S. P. Murarka, D. Price, and R. J. Gutmann, "Pattern Geometry Effects in the Chemical-Mechanical Polishing of Inlaid Copper Structures," *J. Electrochem. Soc.* **141**(10):2842 (1994).
47. R. Capio, J. Farkas, and R. Jairath, "Initial Study on Copper CMP Slurry Chemistries," *Thin Solid Films* **266**(2):238 (1995).
48. E. Ferri, "CMP Chemical Distribution Management," *Proc. Semicond. West: Planarization Technology: Chemical Mechanical Polishing (CMP)*, July 1994.
49. F. B. Kaufman, D. B. Thompson, R. E. Broadie, M. A. Jaso, W. L. Guthrie, D. J. Pearson, and M. B. Small, "Chemical-Mechanical Polishing for Fabricating Patterned W Metal Features as Chip Interconnects," *J. Electrochem. Soc.* **138**:3460 (1991).
50. C.-W. Liu, W.-T. Tseng, B.-T. Dai, C.-Y. Lee, and C.-F. Yeh, "Perspectives on the Wear Mechanism During CMP of Tungsten Thin Films," *Proc. CMP VLSI/ULSI Multilevel Interconnection Conf.*, Santa Clara, CA, 1996.
51. I. Kim, K. Murella, J. Schlueter, E. Nikkel, J. Traut, and G. Castleman, "Optimized Process for CMP," *Semicond. Int.*, **9**:119 (November 1996).
52. R. Capio, J. Farkas, and R. Jairath, "Initial Study on Copper CMP Slurry Chemistries," *Thin Solid Films* **266**:238 (1995).
53. C. Sainio, D. Duquette, J. Steigerwald, and S. Muraka, "Electrochemical Effects in the Chemical-Mechanical Polishing of Copper for Integrated Circuits," *J. Elect. Mater.* **25**(10):1593 (1996).
54. I. Ali, S. R. Roy, and G. Shinn, "Chemical-Mechanical Polishing of Interlayer Dielectric: A Review," *Solid State Technol.* **37**(10):63 (1994).
55. L. Borucki *et al.*, "A Theory of Pad Conditioning for Chemical-Mechanical Polishing," *J. Eng. Math.* **50**(1):1–24 (2004).
56. J. M. de Larios, M. Ravkin, D. L. Hetherington, and J. D. Doyle, "Post-CMP Cleaning for Oxide and Tungsten Applications," *Semicond. Int.* 121 (May 1996).
57. I. Malik, J. Zhang, A. J. Jensen, J. J. Farber, W. C. Krusell, S. Raghavan, and C. Rajhunnath, "Post-CMP Cleaning of W and SiO₂: A Model Study," in *Ultraclean Semiconductor Processing Technology and Surface Chemical Cleaning and Passivation*, MRS 386, Materials Research Society, Pittsburgh, 1995, p. 109.
58. T. J. Cotler and M. Elta, "Plasma-Etch Technology," *IEEE Circuits, Dev. Mag.* **38** (July 1990).
59. D. M. Manos and D. L. Flamm, *Plasma Etching, An Introduction*, Academic Press, Boston, 1989.
60. R. A. Morgan, *Plasma Etching in Semiconductor Fabrication*, Elsevier, Amsterdam, 1985.
61. A. J. van Roosmalen, J. A. G. Baggerman, and S. J. H. Brader, *Dry Etching for VLSI*, Plenum, New York, 1991.
62. J. W. Coburn and H. F. Winters, "Ion and Electron Assisted Gas Surface Chemistry," *J. Appl. Phys.* **50**(5): 3189–3196 (1979).
63. V. M. Donnelly, D. I. Flamm, W. C. Dautremont-Smith, and D. J. Werder, "Anisotropic Etching of SiO₂ in Low-Frequency CF₄/O₂ and NF₃/Ar Plasmas," *J. Appl. Phys.* **55**:242 (1984).
64. G. Smolinsky and D. L. Flamm, "The Plasma Oxidation of CF₄ in a Tubular, Alumina, Fast-Flow Reactor," *J. Appl. Phys.* **50**:4982 (1979).
65. C. J. Mogab, A. C. Adams, and D. L. Flamm, "Plasma Etching of Si and SiO₂—The Effect of Oxygen Additions to CF₄ Plasmas," *J. Appl. Phys.* **49**:3796 (1978).

66. J. W. Coburn, "In-situ Auger Spectroscopy of Si and SiO₂ Surfaces Plasma Etched in CF₄-H₂ Glow Discharges," *J. Appl. Phys.* **50**:5210 (1979).
67. R. d'Agostino, F. Cramarossa, F. Fracassi, E. Desimoni, L. Sabbatini, P. G. Zambonin, and G. Caporiccio, "Polymer Film Formation in C₂F₆-H₂ Discharges," *Thin Solid Films* **143**:163 (1986).
68. M. Shima, "A Study of Dry-Etching Related Contaminations of Si and SiO₂," *Surf. Sci.* **86**:858 (1979).
69. S. Joyce, J. G. Langan, and J. I. Steinfeld, "Chemisorption of Fluorocarbon Free Radicals on Si and SiO₂," *J. Chem. Phys.* **88**:2027 (1988).
70. C. Cardinaud and G. Turban, "Mechanistic Studies of the Initial Stages of Si and SiO₂ in a CHF₃ Plasma," *Appl. Surf. Sci.* **45**:109 (1990).
71. G. S. Oehrlein, K. K. Chan, and G. W. Rubloff, "Surface Analysis of Realistic Semiconductor Microstructures," *J. Vacuum. Sci. Technol. A* **7**:1030 (1989).
72. G. S. Oehrlein and J. F. Rembetski, "Study of Sidewall Passivation and Microscopic Silicon Roughness Phenomena in Chlorine-based Reactive Ion Etching of Silicon Trenches," *J. Vacuum Sci. Technol. B* **8**:1199 (1990).
73. K. V. Guinn and C. C. Chang, "Quantitative Chemical Topography of Polycrystalline Si Anisotropically Etched in Cl₂/O₂ High Density Plasmas," *J. Vacuum Sci. Technol. B* **13**:214 (1995).
74. K. V. Guinn and V. M. Donnelly, "Chemical Topography of Anisotropic Etching of Polycrystalline Si Masked with Photoresist," *J. Appl. Phys.* **75**:2227 (1994).
75. F. H. Bell and O. Joubert, "Polycrystalline Gate Etching in High Density Plasmas. II. X-Ray Photoelectron Spectroscopy Investigation of Silicon Trenches Etched Using a Chlorine-based Chemistry," *J. Vacuum Sci. Technol. B* **14**:1796 (1996).
76. F. Laermer and A. Schilp of Robert Bosch GmbH, "Method of Anisotropically Etching Silicon," U.S. Patent 5,501,893 (2003).
77. M. M. Millard and E. Kay, "Difluorocarbene Emission Spectra from Fluorocarbon Plasmas and Its Relationship to Fluorocarbon Polymer Formation," *J. Electrochem. Soc.* **129**:160 (1982).
78. J. W. Coburn and E. Kay, "Some Chemical Aspects of Fluorocarbon Plasma Etching of Silicon and Its Compounds," *IBM J. Res. Dev.* **23**:33 (1979).
79. J. W. Coburn and E. Kay, "Some Chemical Aspects of Fluorocarbon Plasma Etching of Silicon and Its Compounds," *Solid State Technol.* **22**:117 (1979).
80. V. M. Donnelly, D. E. Ibbotson, and D. L. Flamm, in *Ion Bombardment Modification of Surfaces: Fundamentals and Applications*, O. Auciello and R. Kelly, eds., Elsevier, New York, 1984.
81. F. H. M. Sanders, J. Dieleman, H. J. B. Peters, and J. A. M. Sanders, "Selective Isotropic Dry Etching of Si₃N₄ over SiO₂," *J. Electrochem. Soc.* **129**:2559 (1982).
82. C. J. Mogab, "The Loading Effect in Plasma Etching," *J. Electrochem. Soc.* **124**:1262 (1977).
83. B. A. Heath and T. M. Mayer, in *VLSI Electronics Microstructure Science 8, Plasma Processing for VLSI*, N. G. Einspruch and D. M. Brown, eds., Academic Press, New York, 1984.
84. J. M. E. Harper, "Ion Beam Techniques in Thin Film Deposition," *Solid State Technol.* **30**:129 (1987).
85. R. E. Lee, "Ion-Beam Etching (Milling)," in *VLSI Electronics Microstructure Science 8, Plasma Processing for VLSI*, N. G. Einspruch and D. M. Brown, eds., Academic Press, New York, 1984.

86. H. R. Kaufman, J. J. Cuomo, and J. M. E. Harper, "Techniques and Applications of Broad-Beam Ion Sources Used in Sputtering—Part 1. Ion Source Technology," *J. Vacuum Sci. Technol.* **21**:725 (1982).
87. J. M. E. Harper, "Ion Beam Etching," in *Plasma Etching: An Introduction*, D. M. Manos and D. L. Flamm, eds., Academic Press, New York, 1989.
88. S. Matsup and Y. Adachi, "Reactive Ion Beam Etching Using a Broad Beam ECR Ion Source," *Jpn. J. Appl. Phys.* **21**:L4 (1982).
89. A. S. Yapsir, G. S. Oehrlein, F. Wiltshire, and J. C. Tsang, "X-ray Photoemission and Raman Scattering Spectroscopic Study of Surface Modifications of Silicon Induced by Electron Cyclotron Resonance Etching," *Appl. Phys. Lett.* **57**:590 (1990).
90. C. Keqiang, A. Erli, W. Jinfa, Z. Hansheng, G. Zuoyao, and Z. Bangwei, "Microwave Electron Cyclotron Resonance Plasma for Chemical Vapor Deposition and Etching," *J. Vacuum Sci. Technol. A* **4**:828 (1986).
91. R. E. Lee, "Microfabrication by Ion-Beam Etching," *J. Vacuum Sci. Technol.* **16**:164 (1979).
92. H. Kinoshita, T. Ishida, and K. Kaminishi, "Surface Oxidation of GaAs and AlGaAs in Low-Energy Ar/O₂ Reactive Ion Beam Etching," *Appl. Phys. Lett.* **49**:204 (1986).
93. S. Berg, N. Nender, R. Buchta, and H. Norstrom, "Dry Etching of n-Type and p-Type Polysilicon: Parameters Affecting the Etch Rate," *J. Vacuum Sci. Technol. A* **5**:1600 (1987).
94. H. Okano, Y. Horiike, and M. Sekine, "Photo-Excited Etching of Poly-Crystalline and Single-Crystalline Silicon in Cl₂ Atmospheres," *Jpn. J. Appl. Phys.* **24**:68 (1985).
95. G. C. Schwartz and P. M. Schaible, "Reactive Ion Etching of Silicon," *J. Vacuum Sci. Technol.* **16**:410 (1979).
96. D. L. Flamm, D. N. K. Wang, and D. Maydan, "Multiple-Etchant Loading Effects and Silicon Etching in CClF₃ and Related Mixtures," *J. Electrochem. Soc.* **129**:2755 (1982).
97. L. Peters, "Plasma Etch Chemistry: The Untold Story," *Semicond. Int.* **67** (May 1992).
98. G. S. Oehrlein, J. F. Rembetski, and E. H. Payne, "Study of Sidewall Passivated and Microscopic Silicon Roughness Phenomena in Chlorine-Based Reactive Ion Etching of Silicon Trenches," *J. Vacuum Sci. Technol. B* **8**:1199 (1990).
99. G. K. Herb, D. J. Rieger, and K. Shields, "Silicon Trench Etching in a Hex Reactor," *Solid State Technol.* **30**:109 (1987).
100. Y. T. Fok, *Electrochem. Soc. Proc.* **80**:301, The Electrochemical Society, Pennington, NJ, 1980.
101. D. E. Ibbotson and D. L. Flamm, "Plasma Etching for III–V Compound Devices: Part 1," *Solid State Technol.* **31**:77 (October 1988).
102. M. Balooch, D. R. Orlander, and W. J. Siekhaus, "The Thermal and Ion-Assisted Reactions of GaAs (100) with Molecular Cl," *J. Vacuum Sci. Technol. B* **4**:794 (1986).
103. R. Cheung, S. Thomas, S. P. Beamont, G. Doughty, V. Law, and C. D. W. Wilkinson, "Reactive Ion Etching of GaAs Using a Mixture of Methane and Hydrogen," *Electronics Lett.* **23**:16 (1987).
104. J. M. Villalvilla, C. Santos, and J. A. Vallés-Abarca, "Temperature Dependence of Reactive Ion Beam Etching of GaAs with CH₄/H₂," *Vacuum* **43**:591 (1992).
105. V. J. Law and G. A. C. Jones, "Chloromethane-Based Reactive Ion Etching of GaAs and InP," *Semicond. Sci. Technol.* **7**:281 (1992).
106. T. J. Tu, T. J. Chang, and H. F. Winters, "Chemical Sputtering of Fluorinated Silicon," *Phys. Rev. B* **23**:823 (1981).

107. L. M. Ephrath and E. J. Petrillo, "Parameter and Reactor Dependence of Selective Oxide RIE in CF_4 and H_2 ," *J. Electrochem. Soc.* **129**:2282 (1982).
108. G. S. Oehrlein, "Dry Etching Damage of Silicon: A Review," *Mater. Sci. Eng. B* **4**:441 (1989).
109. G. S. Selwyn, J. Singh, and R. S. Bennett, "In-situ Laser Diagnostic Studies of Plasma-generated Particulate Contamination," *J. Vacuum. Sci. Technol. A* **7**:2758 (1989).
110. S. J. Fonash, "Overview of Dry Etching Damage and Contamination Effects," *J. Electrochem. Soc.* **137**:3885 (1990).
111. X.-C. Mu, S. J. Fonash, G. S. Oehrlein, S. N. Chakravarti, C. Parks, and J. Keller, "A Study of CClF_3/H_2 Reactive Ion Etch Damage and Contamination Effects in Silicon," *J. Appl. Phys.* **59**:2958 (1986).
112. J. P. Gambino, M. D. Monkowski, J. F. Shepard, and C. C. Parks, "Junction Leakage Due to RIE—Induced Metallic Contamination," *J. Electrochem. Soc.* **137**:976 (1990).
113. J. P. Simko, G. S. Oehrlein, and T. M. Mayer, "Removal of Fluorocarbon Residues on CF_4/H_2 Reactive Ion Etched Silicon Surfaces with a Hydrogen Plasma," *J. Electrochem. Soc.* **138**:277 (1991).
114. G. J. Coyle and G. S. Oehrlein, "Formation of a Silicon-Carbide Layer During CF_4/H_2 Dry Etching of Silicon," *Appl. Phys. Lett.* **47**:604 (1985).
115. G. S. Oehrlein, R. M. Tromp, Y. H. Lee, and E. J. Petrillo, "Study of Silicon Contamination and Near-surface Damage Caused by CF_4/H_2 Reactive Ion Etching," *Appl. Phys. Lett.* **45**:420 (1984).
116. G. S. Oehrlein, J. G. Clabes, and P. Spirito, "Investigation of Reactive Ion Etching Related Fluorocarbon Film Deposition onto Silicon and a New Method for Surface Residue Removal," *J. Electrochem. Soc.* **133**:1002 (1986).
117. J. M. Heddleson, M. W. Horn, and S. J. Fonash, "Evolution of Damage, Dopant Deactivation, and Hydrogen Related Effects in Dry Etched Silicon as a Function of Annealing History," *J. Electrochem. Soc.* **137**:1960 (1990).
118. S. J. Fonash, X.-C. Mu, S. Chakravarti, and L. C. Rathbun, "Recovery of Silicon Surfaces Subjected to Reactive Ion Etching Using Rapid Thermal Annealing," *J. Electrochem. Soc.* **135**:1037 (1988).
119. J. P. Simko and G. S. Oehrlein, "Reactive Ion Etching of Silicon and Silicon Dioxide in CF_4 Plasmas Containing H_2 and C_2F_4 Additives," *J. Electrochem. Soc.* **138**:2748 (1991).
120. K. Norjiri, E. Iguchi, K. Kawamura, and K. Kadota, "Microwave Plasma Etching of Silicon Dioxide for Half-Micron ULSIs," *Ext. Abstr. 21st Conf. Solid State Devices*, 1989, p. 153.
121. P. Singer, "New Frontiers in Plasma Etching," *Semicond. Int.* **19**:152 (July 1996).
122. M. Okandan, S. J. Fonash, O. O. Awadelkarim, T. D. Chan, and F. Preuninger, "Soft-Breakdown Damage in MOSFET's Due to High-Density Plasma Etching Exposure," *IEEE Electron Dev. Lett.* **17**(8):388 (1996).
123. M. Sugawara, *Plasma Etching Fundamentals and Applications*, Oxford Science, New York, 1998.
124. S. Wantanabe, "Plasma Cleaning and Etching Using a Quartz Bell Jar with SnO_2 Transparent Thin Film Heater in a CHF_3 - SiO_2 Microwave Etching System," *Jpn. J. Appl. Phys.* **33**:3608 (1994).
125. K. Suzuki, S. Okudaira, N. Sakudo, and I. Kanomata, "Microwave Plasma Etching," *Jpn. J. Appl. Phys.* **16**:1979 (1977).

126. A. Hatta, M. Kubo, Y. Yasaka, and R. Itatani, "Performance of Electron Cyclotron Resonance Plasma Produced by a New Microwave Launching System in a Multicusp Magnetic Field with Permanent Magnets," *Jpn. J. Appl. Phys.* **31**:1473 (1992).
127. S. Wantanabe, "ECR Plasma Etchers," in M. Sugawara, ed., *Plasma Etching Fundamentals and Applications*, Oxford Science, New York, 1998.
128. W. M. Holber and J. Forster, "The Effect of Operating Parameters and RF Bias on Ion Energies in an ECR Reactor," *Proc. 11th Symp. Dry Processes*, IEE Japan, 1989, p. 9.
129. S. Kanai, K. Nojiri, and M. Nawata, "Microwave Plasma Etching System," *Hitachi Rev.* **40**:383 (1991).
130. J. H. Lee, Yeom, J. W. Lee, and J. Y. Lee, "Study of Shallow Silicon Trench Etch Process Using Planar Inductively Coupled Plasmas," *J. Vacuum Sci. Technol. A* **15**(3):573 (1997).
131. Y. H. Lee, S. H. Kim, G. Y. Yeom, J. W. Lee, M. C. You, and T. I. Kim, *J. Vac. Sci. Technol. A* **16**:1478 (1998).
132. R. J. Shul, C. G. Willon, M. M. Bridges, J. Han, J. W. Lee, S. J. Pearton, C. R. Abernathy, J. D. MacKenzie, S. M. Donovan, L. Zhang, and L. F. Lester, *J. Vac. Sci. Technol. A* **16**:1621 (1998).
133. C. S. Oh, T. H. Kim, K. Y. Lim, and J. W. Yang, "GaN Etch Enhancement in Inductively Coupled BCl₃ Plasma with the Addition of N₂ and SF₆ Gas," *Semicond. Sci. Tech.* **19**(2):172 (2004).
134. M. E. Ryan, A. C. Camacho, and J. K. Bhardwaj, "High Etch Rate Gallium Nitride Processing Using an Inductively Coupled Plasma," *Phys. Stat. Sol.* **176**(1):743 (1999).
135. Y. Han, S. Xue, W. Guo, Z. Hao, C. Sun, and Y. Luo, "Characteristics of n-GaN after ICP etching," *Proceedings of the SPIE—The International Society for Optical Engineering* **4918**:193 (2002); *Materials, Devices, and Systems for Display and Lighting Conference*, 15–17 Oct. 2002, Shanghai, China.
136. J. T. C. Lee, "A Comparison of HDP Sources for Polysilicon Etching," *Solid State Technol.* **39**:63 (August 1996).
137. B. J. Canavello, M. Hatzakis, and J. M. Shaw, "Single Step Optical Lift-off Processes," *IBM Technol. Disc. Bull.* **19**:4048 (1977).
138. M. Hatzakis, B. J. Canavello, and J. M. Shaw, "Single-Step Optical Lift-off Process," *IBM J. Res. Dev.* **24**:452 (1980).
139. R. M. Halverson, M. W. MacIntyre, and W. T. Motsiff, "The Mechanism of Single-Step Lift-off with Chlorobenzene in a Diazo-Type Resist," *IBM J. Res. Dev.* **26**:590 (1982).
140. G. G. Collins and G. W. Halsted, "Process Control of the Chlorobenzene Single-step Liff-off Process with a Diazo-type Resist," *IBM J. Res. Dev.* **26**:596 (1982).