

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: October 27, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00228
Patent 11,101,276

PATENT OWNER'S RESPONSE

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EXHIBIT LIST

Ex.	Description
2001	Defendants' Preliminary Invalidity Contentions and Document Production Accompanying Invalidity Contentions re YMTC II Asserted Patents (Patent Local Rules 3-3 and 3-4), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Nov. 25, 2024) (excerpts)
2002	Civil Minutes, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Sept. 18, 2024), ECF No. 141
2003	Order Granting Stipulation to Extend Certain Deadlines Pursuant to Patent L.R. 4-2 and the Scheduling Order (ECF No. 141) Pursuant to Civil Local Rule 6-1(b), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Jan. 8, 2025), ECF No. 194
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2005	Plaintiff/Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.'s and Counterclaim Defendant Yangtze Memory Technologies, Inc.'s Opposition to Micron's Motion to Stay Case Pending <i>Inter Partes</i> Review and Post-Grant Proceedings, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Feb. 3, 2025), ECF No. 221
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2022	<i>3D Flash Memories</i> (Rino Micheloni ed., 2016)
2023	Harmeet Singh, <i>Overcoming Challenges in 3D NAND Volume Manufacturing</i> , 60 Solid State Tech. 18 (July 2017) (excerpt)
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I. Introduction

Patent Owner Yangtze Memory Technologies Company, Ltd. (“YMTC” or “Patent Owner”) submits this Patent Owner’s Response in the *inter partes* review of U.S. Patent No. 11,101,276 (“’276 patent,” Ex.1001). As explained below, Petitioner has not met its burden to show that any of the challenged claims are unpatentable.

The ’276 patent is directed to methods of forming an innovative “staircase structure” for a 3D NAND memory. The ’276 patent addresses the challenges of forming vertical word line contacts in memory devices with increased storage capacity. The independent claim of the ’276 patent requires forming the staircase structure to have steps where the gate stack is “disposed over” a dielectric layer within each step, a process that enhances fabrication yield and reduces costs.

The Petition relies on embodiments from two primary references: Kim (Ex.1005) and Han (Ex.1007). However, both fail to disclose or render obvious limitations in the independent claim. Kim does not disclose “the plurality of steps comprises disposing a sacrificial layer over a dielectric layer.” Han does not disclose “disposing an etch-stop layer on each step.” Furthermore, both Kim and Han fail to disclose the other limitations of the independent claim and certain dependent claims.

The Petition relies on a patchwork of prior art references—including manipulating the disclosures in Kim—and assertions that fail to account for the technical complexity and specific claim requirements of the ’276 patent. The Petition

also attempts to fill critical gaps in the prior art by invoking the general knowledge of a person of ordinary skill in the art (“POSITA”). But under Federal Circuit law and the Board’s decisions, invoking the general knowledge of a POSITA is only permissible for “unusually simple” limitations in “particularly straightforward” technologies. This is no such case. The manufacture of 3D NAND memory is neither simple nor straightforward.

Moreover, the Petition fails to provide any motivation to combine these references with Kim and Han or a reasoned analysis or evidentiary support for such combinations. Consequently, Petitioner did not meet its burden to demonstrate the unpatentability of the challenged claims.

II. Background

A. The '276 Patent (Ex.1001)

The '276 patent issued from U.S. Patent Application No. 16/865,056, filed May 1, 2020, as a divisional application of U.S. Patent Application No. 16/126,947, filed September 10, 2018. '276 patent Cover. The '276 patent claims priority to a PCT application (PCT/CN2018/101308), filed August 18, 2018, which claims priority to a Chinese application (CN 2017/10774754), filed August 31, 2017. *Id.* Cover, 1:1-11.

The '276 patent discloses “a word line contact structure for three-dimensional (3D) memory array and methods for forming the same.” *Id.* 1:40-42; Ex.2006 (“Campbell”) ¶¶23-25.

To meet the demand for higher storage capacity in 3D NAND memories, manufacturers have tried to increase the number of conductor/dielectric layer pairs in such devices. '276 patent 5:42-46. Additional layers, however, create challenges in etching holes of differing depths above the staircase structure to create the vertical word line contacts. *Id.* 5:47-54. The '276 patent recognizes “contact holes for lower levels may be deeper than contact holes for upper levels.” *Id.* And “[t]ypically, all of the contact holes are formed with a single lithography mask and etching process.” *Id.* 5:54-55. But “[o]ften, before contact holes to the bottom levels are entirely formed, the materials exposed in contact holes at the upper levels are over-etched and lost.” *Id.* 5:55-58.

The '276 patent solves this problem with an etch-stop layer over the staircase structure protecting underlying layers during etching. *Id.* 5:61-6:5. This improves yield and reduces cost. *Id.* 6:5-7. A barrier layer can also be introduced over the staircase structure “for protecting the underlying structure during subsequent etching processes.” *Id.* 7:35-45; Campbell ¶26. To implement these structures, the staircase steps are arranged so that the gate stacks of the word lines are disposed over corresponding dielectric layers. '276 patent 6:11-12, 8:60-61, 10:34-38.

The '276 patent describes the process for forming contact openings and addresses the timing of exposing the etch-stop layer. The patent explains that after forming the staircase structure and depositing the etch-stop and insulating layers, a plurality of openings are formed in the third insulating layer 420 to expose portions of the etch-stop layer 310. *Id.* 10:2-5, 22-24. Importantly, at this stage, the etch-stop layer itself is not yet penetrated: “The etch-stop layer 310 protects the underlying structure until all the VIA openings 640 are formed throughout.” *Id.* 10:3-6.

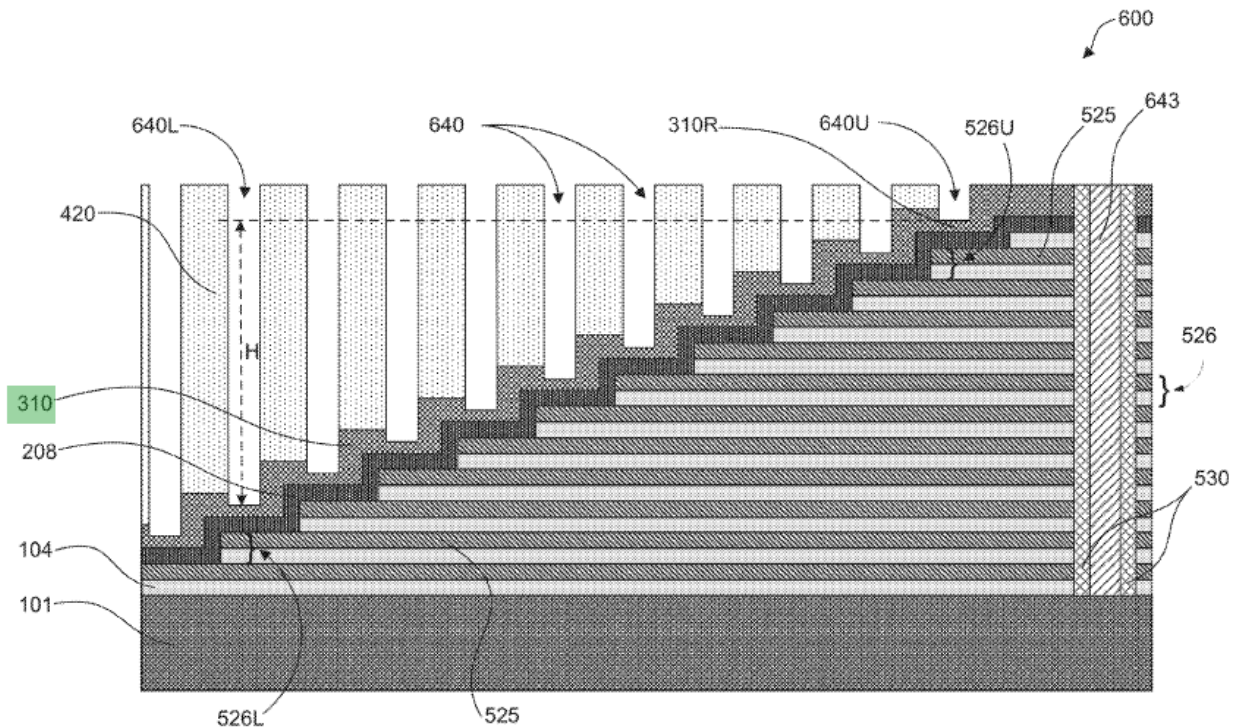
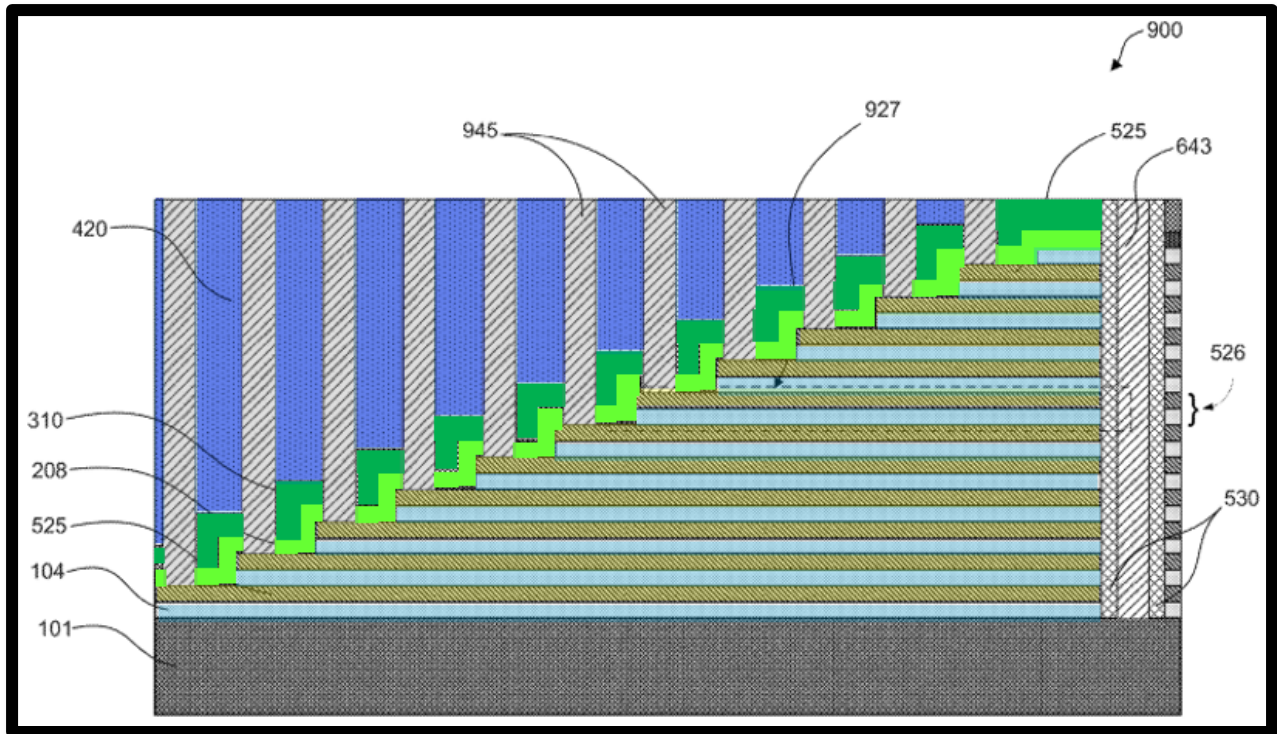


FIG. 6

'276 patent Fig. 6 (annotated).

The '276 patent further describes the purpose of this sequence: “[T]he etch-stop layer 310 protects the underlying” gate stack 525 and other structures from being over-etched or damaged during the formation of the openings in the third insulating layer 420. *Id.* 10:3-5. Only after all the openings have been defined, and the risk of over-etching the upper steps has been mitigated, does the process proceed to etch through the etch-stop layer: “The etch-stop film protects underlying layers during etching processes that form contact VIAs. The etch-stop film is exposed on each level of the staircase structure by a selective etching process, **and then** removed by reverse selective etching.” *Id.* 6:1-5, Figs. 6-7.

Below is an annotated version of Figure 9A, showing an exemplary embodiment of the '276 patent staircase structure. The staircase structure 900 includes alternating layers of gate stacks 525 (yellow) over insulating layers 104 (lighter blue). *Id.* 6:11-12, 8:60-61, 10:34-38. A second insulating layer 208 (bright green) is formed on the top and side surfaces of each step and an etch-stop layer 310 (dark green) is formed on the second insulating layer. *Id.* 7:36-45, 7:62-64, 8:5-6. A third insulating layer 420 (dark blue) is on the staircase structure 900. *Id.* 8:26-30. Vertical interconnect access (“VIA”) structures 945 (hatched grey) are formed in VIA openings 840 in the third insulating layer 420. *Id.* 11:17-22; Campbell ¶28.

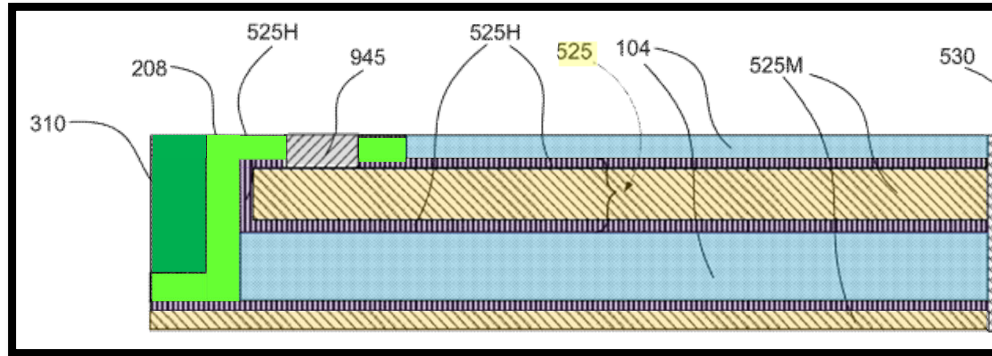


No.	Structure
525	Gate Stack
104	First Insulating Layer
208	Second Insulating Layer
310	Etch-Stop Layer
420	Third Insulating Layer
945	Vertical Interconnect Access Conductive Structures

'276 patent Fig. 9A (annotated), color key; Campbell ¶28.

Figure 9B shows details of the gate stack 525 of Figure 9A above. The gate stack includes a high-k dielectric layer 525H (purple), which surrounds a gate conductive layer 525M (orange) with one side next to fifth insulating layer 530. '276 patent 9:4-10, 9:47-50. The VIA conductive structures 945 (hatched grey) may be

directly disposed on an exposed portion of gate conductive layer 525M. *Id.* 11:19-25; Campbell ¶33.



No.	Structure
104	First Insulating Layer
525H	High-k Dielectric Layer
525M	Gate Conductive Layer
208	Second Insulating Layer
310	Etch-Stop Layer
945	Vertical Interconnect Access Conductive Structures

'276 patent Fig. 9B (trimmed; annotated), color key; Campbell ¶33.

B. Person of Ordinary Skill in the Art

Petitioner proposes a

“POSITA in the field of the '276 Patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (*e.g.*, researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience).”

Pet. 26. Petitioner further proposes that the “POSITA would have been aware of and generally knowledgeable about 3D NAND’s structure, how it is manufactured, and its component parts.” *Id.* YMTC does not dispute this definition of a POSITA for purposes of these proceedings.

C. Claim Construction

The prior art Petitioner relies on fails to disclose the subject matter of the challenged claims under any reasonable construction, including their plain meaning.

Claim 1 recites, among other things, two process steps: first, “forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer” (the exposure step), and, second, “etching the exposed portions of the etch-stop layer in the plurality of openings and exposing at least a portion of the conductive layer of each step” (the etch step). Contrary to the plain language of claim 1, Petitioner suggests that the “etch-stop layer” could be penetrated through or completely etched away in the exposure step, collapsing these two process steps into one. Pet. 45. Petitioner’s interpretation of claim 1 is wrong because it: (a) ignores the difference in plain meaning between the terms “exposing” and “etching”; (b) improperly combines two claimed steps into one; and (c) contradicts the written description in such a way that would defeat the purpose of the claimed subject matter.

Claim 1’s plain language establishes that the exposure and etch steps are distinct. It is well established “[d]ifferent claim terms are presumed to have different

meanings.” *Bd. of Regents of the Univ. of Texas Sys. v. BENQ Am. Corp.*, 533 F.3d 1362, 1371 (Fed. Cir. 2008).¹ The exposure step recites “forming *a plurality of openings* in the insulating layer *exposing portions* of the etch-stop layer.” ’276 patent cl. 1. The etch step operates on the product of the exposure step, i.e., the exposed portions of the etch-stop layer, and recites “*etching the exposed portions* of the etch-stop layer *in the plurality of openings* and exposing at least a portion of the conductive layer of each step.” *Id.* Thus, “etching” and “exposing” have distinct meanings in separate method steps, each serving a different purpose.

Because the etch step must etch “the exposed portions” formed in the exposure step, the etch step cannot occur until after the exposure step as a matter of the grammar and structure of the claims. *See Altiris, Inc. v. Symantec Corp.*, 318 F.3d 1363, 1369 (Fed. Cir. 2003) (stating claims must be performed in the recited order if confirmed “as a matter of logic or grammar”); *E-Pass Techs., Inc. v. 3Com Corp.*, 473 F.3d 1213, 1222 (Fed. Cir. 2007) (“[B]ecause the language of most of the steps of its method claim refer to the completed results of the prior step, E-Pass must show that all of those steps were performed in order.”). Etching the “exposed portions of

¹ All emphases are added and internal quotation marks and citations omitted unless otherwise noted.

the etch-stop layer” cannot occur until those portions are actually “exposed.” In other words, the “exposed portions” of the openings must exist to be etched.

By that same token, combining the exposure step forming a plurality of openings and the etch step, which exposes the conductive structure, would render the etch step superfluous. *See Mformation Techs., Inc. v. Rsch. in Motion Ltd.*, 764 F.3d 1392, 1399 (Fed. Cir. 2014) (holding process step would be rendered “superfluous” if the claim were construed such that a second step would include in it the first step).

Moreover, the '276 patent's written description confirms the exposure step does not penetrate through the etch-stop layer prior to forming the plurality of openings and their “exposed portions.” Every embodiment in the patent is consistent with the plain language of the claims—the exposure step is a separate step that occurs before the etch step. *See, e.g., Hytera Commc'ns Co. v. Motorola Sols., Inc.*, 841 F. App'x 210, 219 (Fed. Cir. 2021) (affirming Board's construction method steps were to be performed in recited order: “[t]he only embodiments are consistent with the plain meaning of the claim in the order that is written”); '276 patent 6:1-5 (describing the invention generally with respect to the etch and exposure steps). The written description states that the etch-stop layer “protects the underlying structure ***until all the VIA openings 640 are formed*** throughout the staircase structure 600.” '276 patent 10:2-5; *see* Ex.2019 (“Campbell2”) ¶30. The stepped-nature of the

claimed staircase structure means “a VIA opening 640L for a lower replacement SC layer 526L requires *longer etch time* than a VIA opening 640U for an upper replacement SC layer 526U” because “[a]n additional thickness” of the insulating layer “must be removed.” ’276 patent 10:6-13; see Campbell2 ¶31.

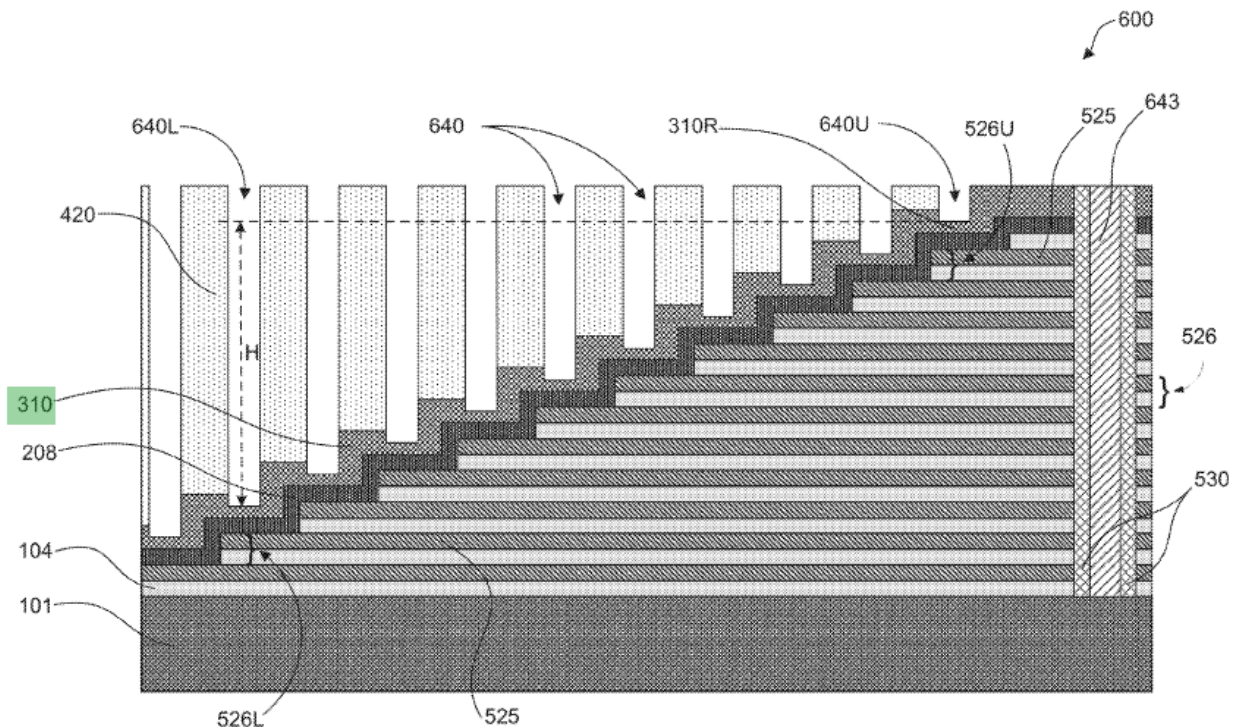


FIG. 6

As shown above in Figure 6, “during the removal process length of the extra thickness H” corresponding to the VIA opening 640L, “the etch-stop layer 310 [green] on top of the upper replacement SC layer 526U ***is not etched through***, with a remaining etch stop layer 310R.” ’276 patent 10:15-17. As a result, “[t]he remaining etch-stop layer 310R provides protection for the replacement SC layers

526U, where the VIA openings 640U are already formed.” *Id.* 10:17-19; *see id.* 7:41-42 (describing the “second insulating layer 208” as optional). Thus, the written description confirms the exposure step is a distinct process that forms a “plurality of openings” separate from the etch step.

Thus, the specification’s description that the exposure step cannot penetrate through the etch-stop layer prior to the etch step confirms the claim’s plain language.² *Campbell* 2 ¶31; *see Mformation Techs.*, 764 F.3d at 1398 (requiring a specific ordering of steps if “the specification directly or implicitly requires” it).

A contrary construction would “defy the invention’s goal” because the “etch-stop layer protects the underlying layers” during the forming of the plurality of openings in a staircase structure, where each plurality of openings has a different length and can take longer to form. ’276 patent 6:1-3, 10:2-16; *Trading Techs. Int’l, Inc. v. eSpeed, Inc.*, 595 F.3d 1340, 1354 (Fed. Cir. 2010) (rejecting claim construction argument that would “present the same problem as the prior

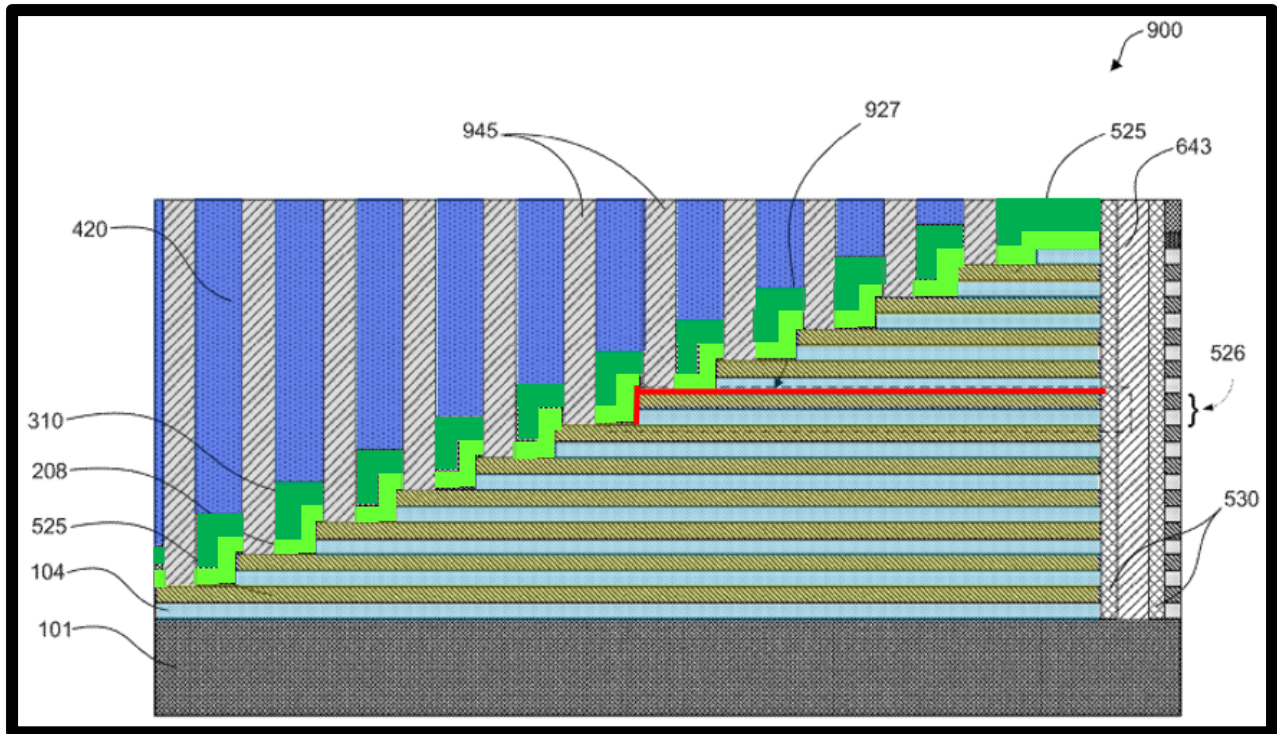
² The specification’s description that “[i]n some embodiments, the etch-stop layer 310 can be *partially etched* in some VIA openings 640” or in other “embodiments ... remains substantially the same during the one or more etching processes that form the VIA openings 640” confirms that the exposure step does not include penetrating through the etch-stop layer prior to forming the openings. ’276 patent 10:24-26.

inventions”). But the etch-stop layer cannot protect the underlying structures during the forming of the plurality of openings if it has already been penetrated. *See* '276 patent 10:13-19. Thus, the plain language of claim 1, in light of the specification, recites two distinct steps: the exposure step and the etch step, where the exposure step does not penetrate through the etch-stop layer prior to forming the plurality of openings.

III. Ground I: Petitioner Failed to Demonstrate Kim in View of a POSITA's Knowledge Renders Obvious Claims 1-2, 4-5, and 9-18.

A. Kim does not disclose “each step of the plurality of steps comprises disposing a sacrificial layer over a dielectric layer” of claim 1.

Claim 1 of the '276 patent requires forming a staircase structure, where “the forming of each [stair] step ... comprises disposing a sacrificial layer over a dielectric layer.” '276 patent cl. 1. Sacrificial layers are later replaced with a “gate stack.” Thus, the '276 patent claims a staircase structure, where each step includes a bottom dielectric layer and a top gate stack layer and methods of forming the same. This can be seen in annotated Figure 9A below, which shows alternating layers on each step with the yellow gate stacks disposed over the blue dielectric layers. An exemplary step has been outlined in red.



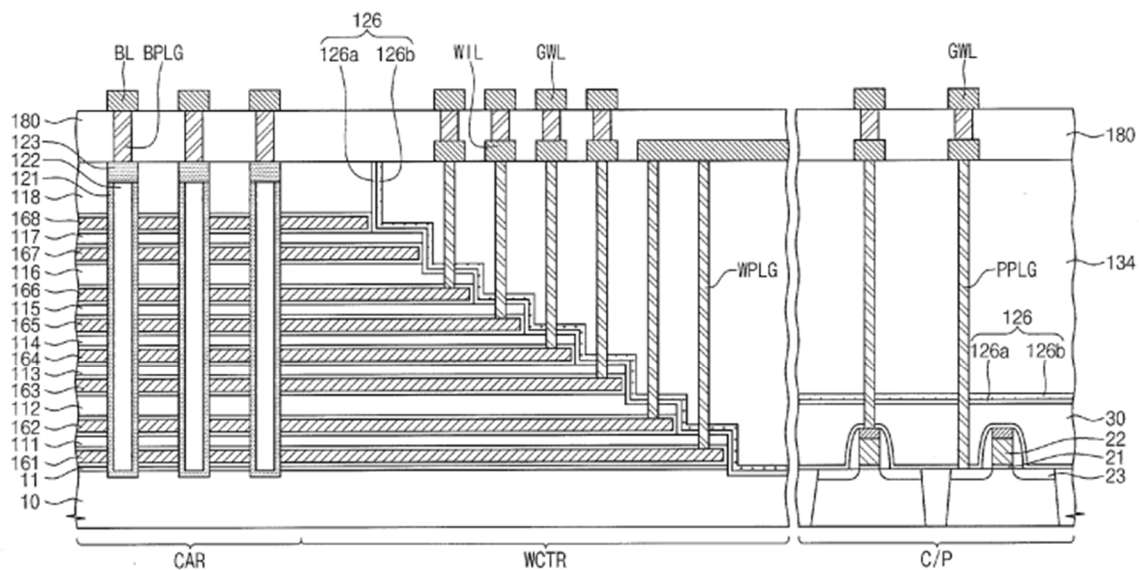
No.	Structure
525	Gate Stack
104	First Insulating Layer
208	Second Insulating Layer
310	Etch-Stop Layer
420	Third Insulating Layer
945	Vertical Interconnect Access Conductive Structures

'276 patent Fig. 9A (annotated), color key; Campbell2 ¶28.

Petitioner admits Grounds 1 and 2 rely on Kim's embodiment in Figures 17A-22B. Pet. 29; Ex.2020 ("Banerjee Dep.") 38:12-17. Yet as shown in the below figure, this embodiment **does not** disclose a gate-stack-on-top arrangement within a single

step, and the cited figures disclose the *opposite*—white dielectric layers disposed over cross-hatched gate stacks.

Fig. 22A



Kim Fig. 22A; Campbell2 ¶34; Banerjee Dep. 39:5-11.

- Petitioner improperly relies on multiple embodiments from Kim but fails to establish a motivation to combine or a reasonable expectation of success in combining embodiments.**

Petitioner relies on multiple embodiments from Kim, but fails to perform the necessary analysis to justify that reliance by neglecting to establish a motivation to combine such embodiments or a reasonable expectation of successfully doing so.

a. Kim does not support freely combining its embodiments or establish a motivation to do so.

Petitioner admits Kim's "figures show the opposite order" of the claims. *See* Pet. 27-28, 32; Ex.1003 ¶54; Campbell2 ¶34; Banerjee Dep. 39:5-11. Nevertheless, in its effort to force the prior art to fit the claims, Petitioner inverts the order of the dielectric and gate stack layers and argues that other embodiments from Kim support that inversion. Pet. 27-28, 32 (citing Kim Figs. 5A-14B); *see, e.g.*, Campbell2 ¶¶35-43; Banerjee Dep. 39:12-15. However, Petitioner fails to show that a POSITA would have been motivated to combine Kim's various embodiments as it proposes.

Petitioner's argument relies on manipulating Figures 17A, 18A, 19A, 21A, and 22A, reversing the order of the "insulating layers" and "sacrificial layers" or corresponding "gate stacks," and changing the shading and labels of the original figures to match its position. *See, e.g.*, Pet. 37-49; Campbell2 ¶¶35-43. For example, in Figure 21A, Petitioner changes the label "116" (corresponding to an insulating layer) to "166" (corresponding to a gate electrode) and "115" (corresponding to an insulating layer) to "165" (corresponding to a gate electrode), and so on. *See, e.g.*, Pet. 44; Campbell2 ¶¶35-37. However, Petitioner does not identify *any* benefit to inverting Kim's layers, any problem that would be solved by doing so, or any reason aside from hindsight that would motivate a POSITA to make the changes it proposes. Campbell2 ¶38. Petitioner makes no effort to provide any motivation to combine Kim's various embodiments as it proposes, which is required even for single-

reference obviousness.³ *See In re Stepan Co.*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017) (“[C]ombining multiple embodiments from a single reference” requires “a motivation to make the combination.”).

Instead of providing an actual motivation to combine, Petitioner argues Kim allows mixing elements across embodiments so long as Kim's description does not explicitly prohibit it. *See* Pet. 32. But that is wrong. Petitioner's basis for this argument is Kim's general statement that “overlapping descriptions of elements previously described with reference to [Figures 5A-14B] may be omitted.” *Id.* (citing Kim [0184]). In context, this is just a statement that Kim uses the same reference numbers for the same elements across embodiments; it does not suggest Petitioner's cherry-picking from Kim's various embodiments. Kim [0184]. Further, even if

³ It is unclear whether Petitioner bases this argument on anticipation or obviousness. While styled as obviousness, Petitioner contends that “a reference invalidates if it enables a POSITA to ‘at once envisage’ ‘the claimed arrangement.’” Pet. 33-34 (citing *Chamberlain Grp., Inc. v. Techtronic Indus. Co.*, 935 F.3d 1341, 1350 (Fed. Cir. 2019)). That is the anticipation standard. *Id.* The Petitioner does not argue anticipation. And Petitioner's expert offers no opinion on anticipation. Banerjee Dep. 37:13-16 (“Q. You don't offer any opinion in your declaration that any of the claims of the '276 patent are anticipated, right? A. No, I do not.”).

arguendo Petitioner were correct, Kim's broad statement would still fail to demonstrate a motivation to combine its embodiments in the way Petitioner proposes. *InTouch Techs., Inc. v. VGO Commc'ns, Inc.*, 751 F.3d 1327, 1351-52 (Fed. Cir. 2014) (describing "conclusory" testimony that a POSITA "*could* combine" prior art references, "not that they *would* have been motivated to do so" as "fraught with hindsight bias") (original emphasis); Campbell2 ¶39.

A POSITA would not have been motivated to combine Kim's embodiments as Petitioner proposes because those embodiments differ materially. Campbell2 ¶¶40-43. Petitioner claims it "rel[ies] on Kim's Figures 17A-22B" embodiment (Pet. 31), but Petitioner cites to the embodiment in Figures 4, 8a and 8B as purportedly disclosing the gate-stack-on-top arrangement (*id.* 27-28 (citing Kim [0090]-[0091], and [0240])). For Figures 4, 8A and 8B, Kim discloses that in some embodiments "each of the top surfaces of the sacrificial layers SC1 to SC8, not the top surfaces of the insulating layers 111 to 118, may be partially exposed in the word line contact region WCTR." Kim [0090]-[0091]. According to Petitioner, this means the sacrificial layer (and thus the gate stack layer) sits on top of the insulating layers in those embodiments. Pet. 27-28, 32. Even though this language is *absent* from the description of Figures 17A-22B, Petitioner concludes it still applies and was simply omitted as an "overlapping description." *Id.* This is wrong.

The embodiment of Figures 17A-22B not only excludes the language from paragraphs [0090]-[0091] but actually *replaces it* with a description requiring a gate-stack-on-*bottom* ordering. Campbell2 ¶¶40-41. Kim explains the etch-stop layer 125a “conformally covers an exposed surface of the stacked layer structure” but covers only “end portions” or “*sidewalls* of the sacrificial layers SC1 to SC8 in the contact region WCTR.” Kim [0185]-[0187]. Thus the sacrificial layer is underneath the dielectric layer in each step, because only the “sidewalls” (not the top surfaces) of the sacrificial layers are exposed and covered by the etch-stop layer 125a. *Id.* [0185]-[0186]; Campbell2 ¶41. Thus, the layer-switching disclosure of Figures 4, 8A and 8B does not apply to the Figures 17A-22B embodiments. Campbell2 ¶¶40-41.

Further, the embodiments Petitioner relies upon are also missing relevant elements disclosed in Figures 17A-22B, including etch-stop and barrier layers. Campbell2 ¶42. Petitioner's combination of disparate embodiments from Figures 4, 8A-8B and 31 with Figures 17A-22B is rank hindsight. A POSITA would not have been motivated to combine the embodiments of Figures 17A-22B with the embodiments of Figures 4, 8A and 8B or 31 as Petitioner proposes. *Id.* Petitioner's many manipulations of Kim's figures are unjustified.

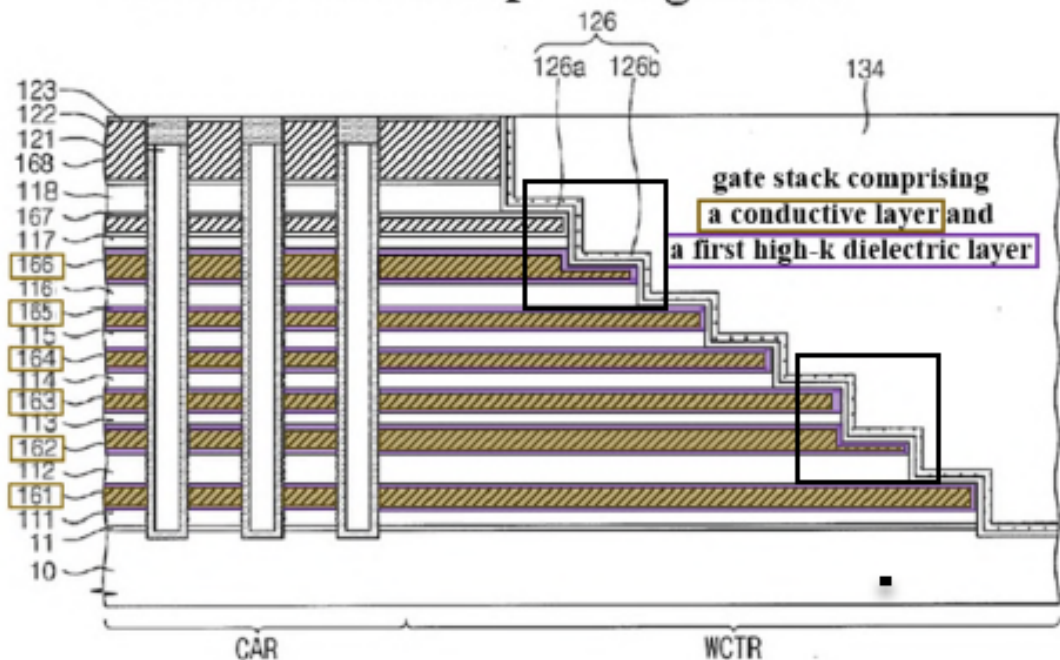
b. Inverting the layers of the relevant embodiment would present technical issues that prevent a reasonable expectation of successfully combining the references.

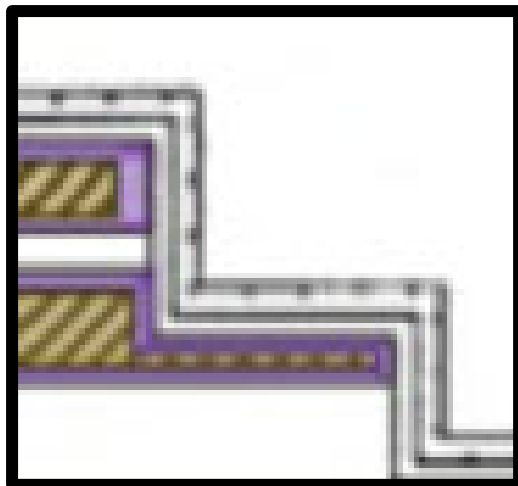
In addition to not being supported by Kim's disclosure, inverting the layers of the embodiment in Figures 17A-22B would present two technical issues. Campbell ¶¶43-46.

First, Petitioner's modification of Kim's figures splits certain gate stacks between two steps, like conductive layers 162 and 166 of the modified Figure 21A below. *Id.* ¶45. The modification leaves some steps with *two* gate conductive layers—one on the top and another on the bottom of the step—while leaving the neighboring step with a thinner gate conductive layer than needed to safely form a word-line contact region. *Id.* This modification is problematic for multiple reasons that could lead to a defective device. First, the thinner conductive layers will be more susceptible to punch-through during the etching process of the vias. *See Banerjee Dep. 30:18-31:2*. Second, thinner conductive layers have higher electrical resistance, which can harm performance. *Id.* 24:25-25:20. Third, if the sacrificial layers are too thin, the gasses or byproducts left over from the sacrificial etching process are unable to flow out of the cavity. *Id.* 26:23-27:1. Fourth, if sacrificial layers are too thin, the cavity created by removing them risks collapse before it can fill with conductive material. *Id.* 28:4-9. Fifth, if the sacrificial layers are too thin, the conductive material will be difficult to deposit in into the recesses of the cavity without leaving

holes, leading to open circuits. *Id.* 28:19-29:2. Sixth, certain steps will have a thin insulator sandwiched between two conductive layers and, because high voltage is used to store data in 3D NAND devices, the high voltage between the two gate stacks can damage the insulator separating the gate stacks causing leakage. Campbell2 ¶45. These issues alone would counsel a POSITA against the combination and undercut any reasonable expectation of successfully achieving it.

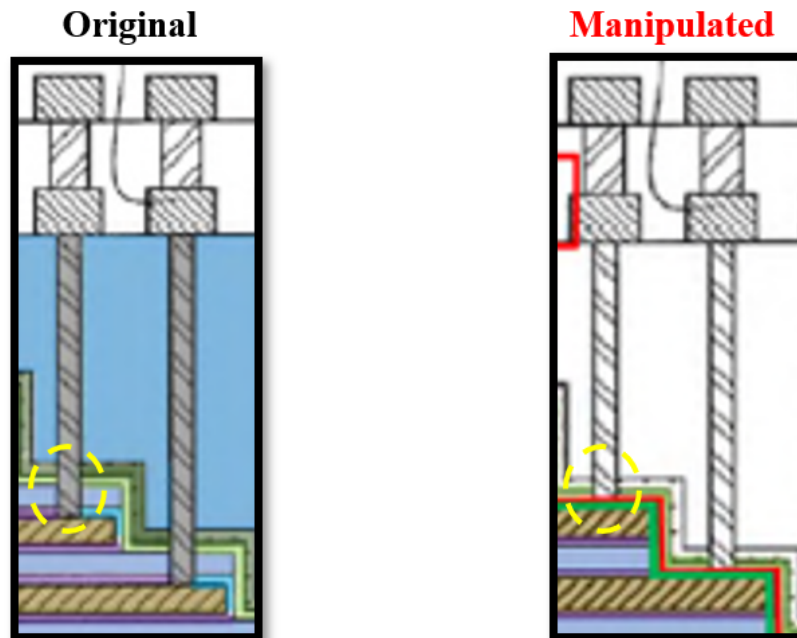
Gate-Stack-on-Top Fig. 21A





(Annotated)

Second, Petitioner's modified Figures also shorten the contact plugs to terminate within gate electrode layers, as shown below in Figure 22A. Campbell2 ¶46. This change is not trivial. Shortening contact plugs requires altering the etching steps and processes that are used to create contact via openings to accommodate a different order of layers. *Id.* As described below in Section III.A.2, these etch processes are complex and sensitive to even minor adjustments. Swapping layers may also change the etch selectivity between the insulating layer above the sacrificial layers SC1-8 and sacrificial layers themselves such that the first stop layer 126a or the second stop layer 126b is not needed—just like in the alternative Figures 4-15D embodiment. *Id.* A POSITA would not use the stop pattern 126 if it is not needed because a POSITA would not want to spend time or material adding an unnecessary component. *Id.*



Even if a POSITA were to ignore the above technical issues, there would still be no reasonable expectation of success in combining the disparate embodiments of Kim because of key differences between these embodiments, as described above, and the impact on the design and manufacturing process, as discussed further below. *Eli Lilly & Co. v. Teva Pharms. Int'l GmbH*, 8 F.4th 1331, 1344 (Fed. Cir. 2021) (“A finding by the Board that a patent challenger has demonstrated a motivation to combine references does not necessarily imply that the challenger has also met its burden of showing a reasonable expectation of success in achieving a claimed method of treatment.”); Campbell² ¶47.

Petitioner argues that “either order was routine, highly predictable, and would have had a reasonable expectation of success.” Pet. 33; Ex.1003 ¶84. But, Petitioner

ignores myriad problems discussed above and in Section III.A.2 that a POSITA must consider when reversing Kim's layer order. For example, Petitioner never addresses the problems resulting from gate stacks spanning two steps, thin conductive layers, and the shortening of conductive structures. Nor does Petitioner address necessary modifications to etch processes and risks of short-circuits associated with reducing the number of protective layers over the gate stack. *See* Campbell2 ¶¶50-52; *see* Ex.2021 (Banerjee '711 Dep.) 48:20-49:8 (explaining that "the more different materials that you have that the etch has to go through, in general, that provides additional safety margin"). Thus, even if a gate-stack-on-top ordering were known, a POSITA would not have a reasonable expectation of success applying it on that basis alone.

2. Petitioner improperly relies on additional background references and improperly invokes common knowledge.

Faced with Kim's deficient disclosures, Petitioner improperly relies on a POSITA's knowledge to supplement the missing limitations. Such argument is improper. A Petitioner "must specify where each element of the claim is found *in the prior art patents or printed publications relied upon*." 37 C.F.R. § 42.104(b)(4). Reference to a POSITA's general knowledge does not meet this standard, according

to the Director's clarification of § 42.104(b)(4), and Petitioner is not entitled to rely on it to supply missing limitations.⁴

Indeed, even in the context of invalidity broadly, general knowledge may only supply a missing claim limitation when “the missing limitation in question [is] *unusually simple* and the technology *particularly straightforward*.” *Motorola Mobility LLC v. Largan Precision Co.*, IPR2024-00688, Paper 7 at 29 (P.T.A.B. Oct. 28, 2024) (original alteration and emphases) (quoting *Koninklijke Philips N.V. v.*

⁴ The Acting Director of the USPTO issued a memorandum that went into effect for petitions filed in September 2025 clarifying as much, explaining that “enforcement of Rule 104(b)(4) means that applicant admitted prior art (AAPA), expert testimony, common sense, and other evidence that is not ‘prior art consisting of patents or printed publications’ (collectively ‘general knowledge’) may not be used to supply a missing claim limitation.” See USPTO Memorandum, Enforcement and Non-Waiver of 37 C.F.R. § 42.104(b)(4) and Permissible Uses of General Knowledge in Inter Partes Reviews at 1 (July 31, 2025). While this Petition was filed before September 1, 2025, the Board should reject Petitioner's effort to use “common knowledge” to fill in missing claim limitations here because, as the Director stated, “enforcement of Rule 104(b)(4) means that ... ‘general knowledge’ may not be used to supply a missing claim limitation.” *Id.*

Google LLC, 948 F.3d 1330, 1337-38 (Fed. Cir. 2020)). But even then, it “cannot be used as a wholesale substitute for reasoned analysis and evidentiary support.” *Google*, 948 F.3d at 1337-38.

Moreover, Petitioner carries the burden of showing the claims are obvious, which “never shifts” to the patent owner. *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378-79 (Fed. Cir. 2015). “Failure to prove the matter ***as required by the applicable standard*** means that the party with the burden of persuasion,” i.e., Petitioner, “loses.” *Motorola Mobility, LLC v. Int’l Trade Comm’n*, 737 F.3d 1345, 1350 (Fed. Cir. 2013) (“At all times, the burden of persuasion rests on the party challenging the patent.”). Thus, the burden of showing a limitation is unusually simple and the technology straightforward falls on ***Petitioner***.

Here, Petitioner provides no argument that the limitations it supplies based on a POSITA’s general knowledge⁵ are unusually simple or that 3D NAND technology is particularly straightforward. Therefore, all four grounds fail on that basis alone.

⁵ To the extent Petitioner argues that it relied on background references such as Chen, Yu, Ohsaki, and Shin (*see, e.g.*, Pet. 33-35), such an argument is equally improper. Petitioner is not entitled to make an end-run around establishing a motivation to combine and reasonable expectation of success for these references by not including them in the relevant ground, but still using them to supply a missing

a. 3D NAND technology is complex.

Highly technical electronic inventions, such as 3D NAND, are not “particularly straightforward.” *See DSS Tech. Mgmt. Inc. v. Apple Inc.*, 885 F.3d 1367, 1374 (Fed. Cir. 2018) (rejecting Board’s reliance on “common knowledge” to “supply a missing claim limitation” because wireless communications are not “particularly straightforward” technology); *see, e.g.*, Pet. 31-35; Campbell² ¶¶48-49. Indeed, the literature describes 3D NAND as “*very complex*” and including “complex device structures.” Ex.2022 293; Ex.2023 3; Ex.2022 212 (“3D NAND architectures need to be proved cost effective in terms of process costs and product yield because the process complexity is not trivial if compared to 2D NAND.”); Ex.2023 4 (“[T]he overall complexity and capital intensity of 3D NAND manufacturing add significantly to the challenges fabs are facing in terms of process

limitation. If Petitioner intended to rely on these or other references to supply a missing limitation, it was required to make them part of the applicable obviousness combination and conduct the proper analysis. It failed to do so here, especially given the structural and compositional differences between the references and their differing focuses.

control, yield, and economics.”); Campbell2 ¶¶48-49; *see also* Ex.2024 5 (“With each generation, the fabrication of 3D NAND becomes more complex.”).

Fabrication of 3D NAND is as complex as the devices themselves and “involves a number of new and ***complex process steps***.” Ex.2025 4; Ex.2023 4-5 (recognizing “[a]n incredible level of precision and repetition is required in defining complex 3D structures with extremely high aspect ratio (HAR) features,” including “alternating film deposition” and formation of “staircase,” “wordline,” “contact,” and “channel” features), Fig. 1; Ex.2026 1 (“3D NAND has led to complex deposition and etch with angstrom-level precision requirements.”); Ex.2028 8, 31 (describing removal of nitride layers and forming a wordline as a “complex process”); Campbell2 ¶¶48-49; *see also* Ex.2028 3 (“[M]aking 3D NAND is a complex process”); *id.* 2 (“The big challenge is to characterize the inner portions of a 3D NAND device, which consists of complex materials, multiple layers and tiny channel holes.”); Ex.2029 5 (“3D NAND is a complex technology”); *id.* 6 (“In all cases, the 3D NAND process flow is complex.”).

Thus, 3D semiconductor design and manufacturing employs concepts of chemical, mechanical, and electrical engineering on a microscopic scale and is not “particularly straightforward” technology. Campbell2 ¶¶48-49.

b. Re-ordering sacrificial and insulating layer is a complex process.

Nor is the missing limitation of “disposing a sacrificial layer over a dielectric layer” “unusually simple” such that Petitioner may rely on a POSITA’s knowledge. Campbell2 ¶¶50-53. Rearranging the layers and adjusting etch-stop characteristics requires changes in both device design and manufacturing processes, including changes to etching processes. *Id.*

Etch processes depend on multiple parameters optimized to achieve desired etch characteristics for a specific device design. *Id.* ¶50. These parameters include the combination of gases used as the etchant, plasma power, bias voltage, chamber pressure, temperature, and etch time. *Id.*; Ex.2021 37:9-41:8 (identifying these various etch parameters); *see, e.g., id.* 61:21-64:10 (confirming that any one of these parameters can effect etch-depth). When the design or manufacturing process changes, various etching parameters must be re-optimized to design a new etching process. Even small changes in these parameters can have significant effects. “[S]pecifics matter” and “details matter,” as Dr. Banerjee repeatedly affirmed in deposition. *See* Ex.2021 40:20-22, 41:5-8, 45:12, 46:18, 57:2-3, 61:18-19. As Dr. Banerjee admitted, such changes can also affect the number and sequence of steps in the etching processes. *Id.* 37:9-41:8, 47:8-48:1, 61:21-64:10.

Etch processes also depend on the materials used in the structure, etch-stop, and mask (e.g., whether it is photoresist or a hard mask), as well as the depth and

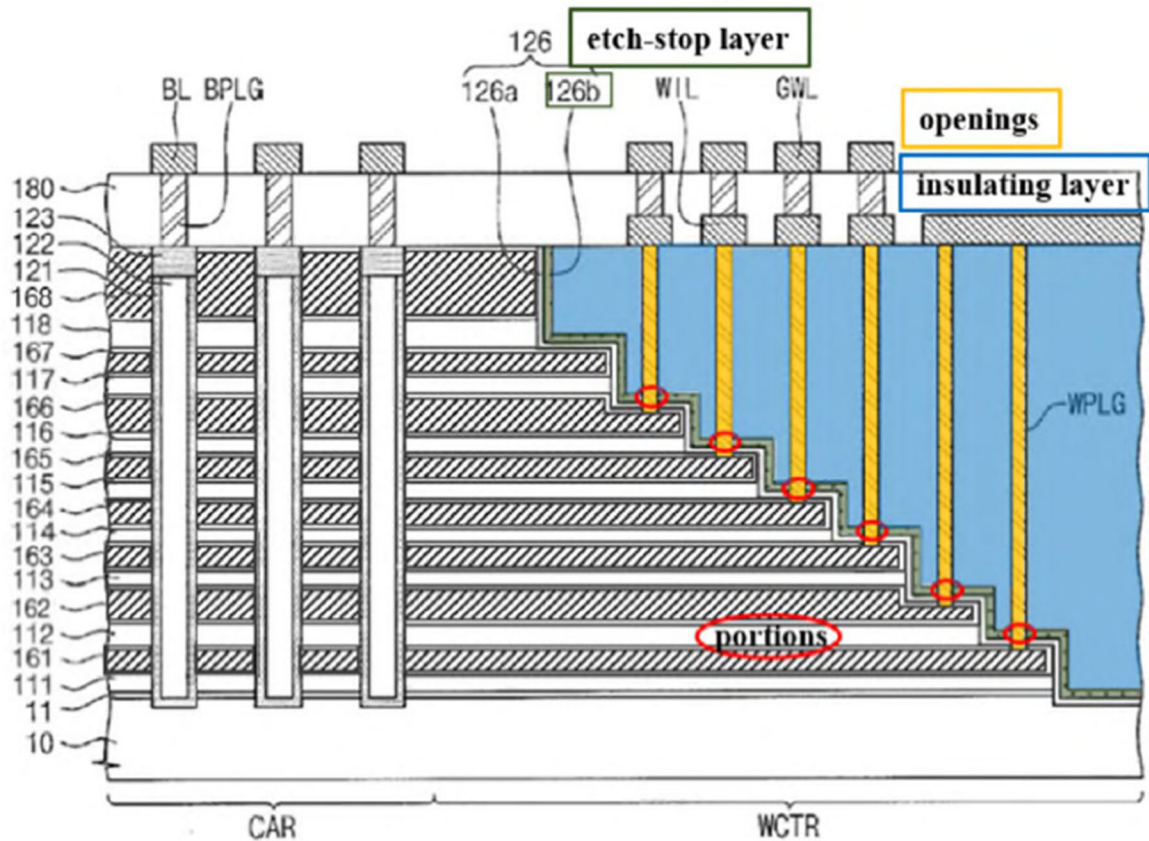
aspect ratio of the desired etch and the order of the layers. Campbell2 ¶51. Thus, drawing a figure that moves structures around, as Petitioner does here, is not only misleading but gives the illusion of simplicity. The reality of such changes is extremely complicated, as discussed above. *Id.*; see Section III.A.1.b. Petitioner ignores their implications here.

As further evidence of this technology's complexity, Petitioner appears to have made a mistake in altering Kim's Figure 22A. Campbell2 ¶52. As Dr. Banerjee acknowledged, Figure 22A required other modifications once the order of the layers was changed. For instance, Petitioner also altered the depth of the word line contacts, which would have required changes to the etch-parameters as described above. *Id.*; Ex.2021 36:9-41:8. However, Kim's Figure 22A also includes a lower gate insulating layer labeled as element 11. *See, e.g.*, Kim [0061], [0064], [0071], [0142]. The purpose of that layer is to prevent "electrical crosstalk" between the lowermost gate and the substrate. Ex.2021 30:21-31:22; see Campbell2 ¶52. Yet when Petitioner altered the layer order, it placed an insulating layer in contact with the substrate, rather than a gate stack. *See, e.g.*, Ex.1003 ¶106, Fig. 22A (modified). This made lower gate insulating layer 11 unnecessary, but Petitioner failed to recognize or account for this change. Campbell2 ¶52.

B. Kim does not disclose “forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer” of claim 1.

Claim 1 recites “forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer.” ’276 patent cl. 1. As discussed above, the exposure step does not penetrate through the etch-stop layer. Section II.C. Petitioner argues that Kim discloses “a step where etching penetrates the insulating layer exposing—but not penetrating—portions of the etch-stop layer.” Pet. 45. Petitioner is wrong. Campbell2 ¶¶54-61.

Kim teaches completely penetrating through the etch-stop layer, such that the etch-stop layer is removed entirely, not exposed. Petitioner does not, and cannot, repudiate this teaching. Pet. 46-47 (citing Kim Fig. 22A) (showing only contact hole penetrating through etch-stop layer). Inevitably, the portion of Kim Petitioner relies on does not teach exposing the etch-stop layer, but rather only connecting the “word line contact plugs WPLG ... to the gate electrodes,” where the openings penetrate Kim’s etch-stop layer, as shown in its modified Figure 22A below. *Id.* 46; Kim [0173]; Campbell2 ¶55.

Gate-Stack-on-Top Fig. 22A**Pet. 46 (annotating Kim Fig. 22A)**

Kim does not teach “exposing portions of the etch-stop layer” as claimed—instead, it only discloses creating “word line contact plugs WPLG” without any disclosure regarding how the contact openings are formed. Nowhere does Kim disclose a process where its contact holes are formed by first forming a plurality of openings exposing the etch-stop layer, prior to etching the “exposed portions” of the plurality of openings exposing the conductive layer (i.e., not penetrating through the etch-stop layer), as required by claim 1. *See* Section II.C; Campbell2 ¶56.

In attempting to cure Kim's deficiencies, Petitioner asserts that a POSITA would have understood Kim's differences in etch selectivity between the interlayer dielectric and the etch-stop layer in *planarization* to teach etching that interlayer dielectric layer without penetrating the etch-stop layer during Kim's *forming contact holes*. Pet. 47 (citing Kim [0213]). The Board accepted Petitioner's argument, reasoning Kim "describes the etch stop layer 125b as being formed of silicon nitride, the same material that Kim describes 'exhibiting a slower *removal* rate than the interlayer dielectric layer' *during planarization*." ID 12.

But that finding is based on a flaw in Petitioner's argument because "planarization" differs from the process for forming contact holes. A POSITA would not have understood Kim's disclosure for purposes of planarizing to apply to forming contact holes in a staircase structure because those processes have different goals, methods, and complexities. Campbell2 ¶¶57-60. More specifically, Kim discloses its planarization step (i.e., creating a flat surface) uses a chemical and mechanical polishing process ("CMP") that does not form openings (i.e., digging from a flat surface) in the etch-stop layer. *Id.* ¶¶58-60 (citing Kim [0141], [0192]-[0194]). Indeed, the "removal rate" the Board refers to is the specific "removal rate ... *during* the planarization," not the specific "etch recipe" used during an etching process for forming an opening. *Id.* ¶60; *see* Kim [0104] ("A removal rate of the interlayer dielectric 130 in the planarization process may be affected by

various factors, such as a slurry type, a configuration of the polishing pad, a structure and type of a polishing head, a rotating speed of the polishing pad relative to the substrate 10, a pressure applied by the polishing pad to the substrate 10, and a material and shape of the interlayer dielectric 130.”), [0132], [0141]. Even Dr. Banerjee agrees that CMP cannot be used to form contact holes (Banerjee Dep. 47:6-8), and that comparing etch selectivities for CMP and for forming contact holes was “comparing apples to oranges.” *Id.* 50:2-8.

Regardless of whether Kim's disclosure regarding planarization applies to forming holes for the WPLGs, Kim does not teach that such a process forms a plurality of openings exposing the etch-stop layer without etching through the etch-stop layer. Neither Petitioner nor its expert assert otherwise. Petitioner only states, without support, that “relative etch selectivity allows the interlayer dielectric to be etched away without penetrating the etch-stop layer.” Pet. 47. Likewise, Petitioner's expert merely states Kim's etch selectivity disclosure “allow[s] the interlayer dielectric to be etched away while preserving the etch-stop layer” without explaining where Kim teaches that. Ex.1003 ¶103.

Thus, Kim does not disclose forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer.

C. Kim does not disclose “etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer” of claim 4.

Petitioner fails to show claim 4 is obvious over Kim. Claim 4 recites “[t]he method of claim 1, wherein etching the exposed portions of the etch-stop layer comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer of each step.”

Kim does not disclose this limitation. Petitioner improperly relies on a POSITA's knowledge to fill in the disclosure. Petitioner's arguments fail for the reasons described in Section III.A.2. To the extent Petitioner argues that it relied on background references such as Fang (Ex.1006) and Wang (Ex.1023) (*see, e.g.*, Pet. 50-51), this argument is improper for the reasons described in Section III.A.2.

Further, “etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer of each step” is not “unusually simple” for the reasons described previously regarding etch-processes, nor is 3D NAND memory array manufacturing and design a “particularly straightforward” technology. *See* Campbell2 ¶¶62-63; Section III.A.2.

D. Kim does not disclose “etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the first high-k dielectric layer” of claim 5.

1. Petitioner improperly relies on additional background references and a POSITA's knowledge.

Petitioner fails to show claim 5 is obvious over Kim. Claim 5 recites “[t]he method of claim 4, wherein etching the exposed portions of the etch-stop layer further comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the first high-k dielectric layer.”

Kim does not disclose this limitation. Petitioner improperly relies on a POSITA's knowledge to fill in the disclosure. Petitioner's arguments fail for the reasons described in Section III.A.2. To the extent Petitioner argues that it relied on background references such as Williams (Ex.1024) (*see, e.g.*, Pet. 52-53), this argument is improper for the reasons described in Section III.A.2.

Further, “etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the first high-k dielectric layer” is not “unusually simple” for the reasons described previously regarding etch-processes, nor is 3D NAND memory array manufacturing and design a “particularly straightforward” technology. *See* Campbell² ¶64; Section III.A.2.

2. Petitioner fails to establish a motivation to combine Kim in view of a POSITA's knowledge to render claim 5 obvious, or a reasonable expectation of successfully doing so.

Petitioner argues that because “punch-through of gate-electrode layers must be prevented,” a POSITA would have wanted to “further protect the gate electrode” by using the first high-k dielectric layer as an etch-stop. Pet. 52. But Kim already protects against punch-through using multiple etch-stop layers. Campbell2 ¶¶65-68. Petitioner provides no reason why a POSITA would consider further etch-stop protection necessary or “advantageous,” especially where doing so would require an additional etch process and etch chemistry during manufacturing.

Even if a POSITA believed additional protection was necessary, Petitioner is wrong that “only the claimed relative etching rates have a sensible relationship.” *Id.* ¶67. Petitioner argues that the “only ... sensible relationship” between the two layers is for the first high-k dielectric layer to function as an etch-stop, meaning it has a lower etching rate than the etch-stop layer above it, because “punch-through ... must be prevented.” Pet. 52. But, instead of using the first high-k dielectric as an etch-stop, a POSITA could have chosen to make the etch-stop and first high-k dielectric layers out of the same material, effectively increasing the thickness of the etch-stop layer. Campbell2 ¶67. In that case, the etch-stop and first high-k dielectric layers would have the *same* etch rate, while accomplishing the same goal of protecting against punch-through. *Id.*

The '276 patent contemplates such an embodiment. *See* '276 patent cls. 6, 14 (dependent claims listing overlapping etch-stop and first high-k dielectric layer materials, where neither claims depends on the method of claim 5). Further, a POSITA would know that the first high-k dielectric's purpose to protect the surrounding oxide layers during formation of the conductive gate layer could still be accomplished regardless of selectivity with the etch-stop layer. Campbell2 ¶68.

E. Kim does not disclose “forming the ... conductive structures further comprises planarizing the conductive materials and the insulating layer” of claim 11.

1. Petitioner improperly relies on additional background references and a POSITA's knowledge.

Petitioner fails to show claim 11 is obvious over Kim. Dependent claim 11 claims “[t]he method of claim 1, wherein forming the plurality of conductive structures further comprises planarizing the conductive materials and the insulating layer.”

Kim does not disclose “planarizing the conductive materials,” as required by Claim 11. Campbell2 ¶69. Instead, Petitioner improperly relies on a POSITA's knowledge to gap-fill this missing limitation. Petitioner's arguments fail for the reasons described in Section III.A.2. To the extent Petitioner argues it relied on background references such as Wolf (Ex.1021) (*see, e.g.*, Pet. 56-57), this argument is improper for the reasons described in Section III.A.2.

Further, the missing limitation of “planarizing the conductive materials” is not “unusually simple” given the variety of factors relevant to designing a CMP process, and how these factors vary across materials and applications. Campbell² ¶70. Nor is 3D NAND memory array manufacturing and design a “particularly straightforward” technology. *See* Section III.A.2.

IV. Ground II: Petitioner Failed to Demonstrate Kim in View of Fang Renders Obvious Claims 1, 3, 6-8.

Petitioner states that the Ground II combination applies to “all Challenged Claims,” referring to claims 1-18. Pet. 64. However, Petitioner only identifies Fang as supplying missing limitations in Kim for Claims 1.B, 3, 6, 7, and 8. Thus, for the remaining claim 1 limitations and for claims 2, 4-5, and 9-18, Ground II fails for at least the reasons described above for Ground I.⁶ Ground II also fails for the reasons below.

⁶ Petitioner waived any argument Fang discloses any other limitation because it was not included in the Petition. *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) (finding waiver where the petition did not “identify ‘with particularity’ the ‘evidence that supports the grounds for the challenge to each claim’”).

A. Like Kim, Fang does not disclose “each step ... comprises disposing a sacrificial layer over a dielectric layer” of claim 1.

Like Kim, Fang does not disclose a gate-stack-on-top ordering for conductive and dielectric layers within each step and, accordingly, does not disclose a sacrificial layer over a dielectric layer in each step. *See, e.g.*, Fang Figs. 1-4. Petitioner does not identify any disclosure in Fang for this limitation. As neither Kim nor Fang disclose this limitation, the combination of Kim and Fang fails to render claim 1 obvious.

B. Petitioner fails to establish a motivation to combine Kim in view of Fang or a reasonable expectation of success in doing so.

Petitioner fails to establish a motivation to combine the Kim and Fang references to render obvious claims 1.B, 3, and 6-8. Petitioner admits that Kim “does not detail certain aspects of the word-line contact region WCTR” but argues a POSITA would have been motivated to combine “Fang’s disclosures related to the etch-stop layer and contact-hole etching on Kim’s word-line structure.” Pet. 70. Petitioner is wrong and ignores fundamental differences between Kim and Fang with respect to the problems they are trying to solve, the materials they use, and their structural design elements. Campbell2 ¶¶72-90.

1. POSITAs would not have been motivated to adapt Fang’s etch-stop characteristics or contact-hole etching to Kim.

A POSITA would not have been motivated combine Fang’s disclosures, including its etch-stop layer and contact-hole etching, with Kim. Nor would a

POSITA have a reasonable expectation of successfully achieving such a combination for the reason described below. See *Adidas AG v. Nike, Inc.*, 963 F.3d 1355, 1359 (Fed. Cir. 2020) (“Fundamental differences between the references are central to th[e] motivation to combine inquiry.”).

a. Kim and Fang are directed towards solving different problems.

Petitioner suggests a POSITA would have been motivated to combine Fang with Kim because Fang's focus on “preventing over-etching shallower openings when etching openings for the word-line conductive structures” is an important consideration for manufacturing 3D memory devices and “dovetails” with Kim's putative focus “to reduce or prevent damage to the device during manufacturing.” Pet. 70. But Fang and Kim are focused on *different* problems. Campbell² ¶¶73-75. Kim focuses on preventing damage during CMP planarization, while Fang focuses on preventing damage from over-etching contact vias. *Id.* Given their disparate focuses, POSITAs would not have been motivated to combine these references. *Id.*

Kim focuses on preventing damage during CMP planarization. *Id.* ¶¶73-74. First, Kim describes preventing “dishing”⁷ that can occur during CMP planarization

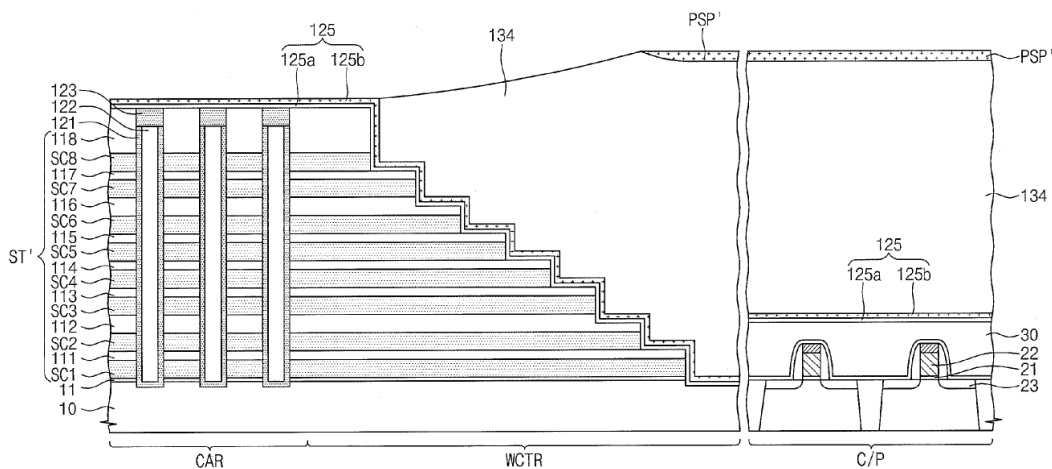
⁷ “Dishing” is an unintentional recess in the interlayer dielectric over the WCTR and C/P regions that occurs because the contact pads 123 of the cell array region (CAR) may have a different removal rate from the interlayer dielectric, meaning the

of the interlayer dielectric in the upper area of the peripheral circuit region (C/P) and word-line contact region (WCTR).⁸ Kim [0025]-[0026], [0104], [0190]-[0197]; Campbell2 ¶74. These regions can be seen below in Figure 19A. Second, Kim also describes preventing damage from CMP to the contact pads 123 in the CAR region by forming a “polishing stop layer PSL” over the interlayer dielectric and “etch stop layer 125” over the contact pads 123. Kim [0027], [0105], [0190]-[0197]; Campbell2 ¶74. Thus, Kim focuses on preventing damage to specific components (contact pads 123 and interlayer dielectric 134), in specific regions of the device (CAR and upper areas of the WCTR and C/P), during a specific process (CMP). Campbell2 ¶74.

interlayer dielectric on the WCTR and C/P regions “may be etched faster than the contact pads 123 of the cell array region.” Kim [0105], [0190]-[0197].

⁸ Figure 19A shows interlayer insulating pattern 134 instead of interlayer dielectric 130 because Figure 19A is post-planarization, but they refer to the same component. For example, Figure 18A shows the interlayer dielectric 130 before planarization. In later Figures, such as Figure 19A, the planarized interlayer dielectric is referred to as interlayer insulating pattern 134. *See* Kim [0193]. The same is true of the polishing stop layer PSL before planarization and the polishing stop pattern PSP afterwards. *See id.* [0196]-[0197].

Fig. 19A



Fang addresses a different problem, resulting from a different process, in a different location. Campbell2 ¶75. Specifically, Fang addresses over-etching, or “punch through,” of shallow openings for word-line conductive structures in the lower part of the WCTR region where the etch-stop layer covers the underlying structures of the staircase steps. Fang [0004], [0008]; Campbell2 ¶75. Fang discloses using a single etch-stop layer directly on the staircase structure to prevent “punch through” into the conductive material during the etching processes used to create openings for the word-line conductive structures. Fang [0004], [0008]; Campbell2 ¶75.

This differs from avoiding damage during CMP planarization, as Kim discloses, because here the damage occurs on the staircase steps and results from the

via-etching process. Given these disparate focuses, a POSITA would not be motivated to combine Fang and Kim. Campbell2 ¶¶74-75.

b. Fang is directed towards carbon-doped silicon nitride etch-stop material, which Kim does not use.

A POSITA would also not have been motivated to combine Kim and Fang because they concern different etch-stop materials. Campbell2 ¶¶76-80. Fang is directed to a carbon-doped silicon nitride (“CDSN”) etch-stop material, which Kim does not use. *See* Fang Title, Abstract, [0020], [0022] (identifying CDSN as the primary example of “etch[-]stop material 130”); *see also e.g., id.* cls. 1-27 (*all claims* explicitly using CDSN); Kim [0186], [0187]; Campbell2 ¶¶76-77; *see* Ex.2021 51:8-15. A POSITA would not apply the etch-stop material and associated thicknesses specified in Fang to Kim for several reasons.

First, a POSITA would know that etch-stop-layer characteristics, such as thickness, are not fungible across different materials. Campbell2 ¶76. Different materials have different etch chemistries, and a POSITA would not be motivated to use Fang’s CDSN etch-stop layer thicknesses in Kim where Kim never uses that material. *Id.*; *see* Pet. 68, 71; Kim [0186], [0187] (disclosing only silicon oxide, silicon carbide, silicon nitride (without carbon doping), silicon oxynitride, and silicon oxycarbide as possible etch-stop materials). Even Petitioner’s expert explains that “[d]ifferent materials react to an etchant differently and an etching rate is used to characterize how fast or slow an etchant etches through a particular material” and

that “a material also can react differently to different etchants. For example, a material may have a high etching rate for one etchant and a low etching rate for a different etchant.” Ex.1003 ¶52; Campbell2 ¶76. Kim does not disclose an etch-stop layer thickness and Petitioner relies on Fang for that element. Pet.68-69. But Fang’s etch-stop-layer thicknesses are specific to CDSN. *See* Fang [0020], [0022], cls. 1-27; Campbell2 ¶76. A POSITA would not ignore the differences in their etch-stop materials and be motivated to adapt Fang’s etch-stop thickness to Kim simply because Kim does not disclose a thickness. *See* Pet. 70; Campbell2 ¶76.

Further, Petitioner’s argument that Kim’s and Fang’s etch-stop-layers are similar because both disclose a “silicon nitride” etch-stop layer is wrong and would provide neither a motivation to combine nor a reasonable expectation of success. Pet. 67-68, 71; Campbell2 ¶¶76, 79.⁹ Kim discloses an etch-stop material of *undoped* silicon nitride, which is different than Fang’s *carbon-doped* silicon nitride. Campbell2 ¶¶76, 79. Indeed, Fang teaches away from the combination of Fang and Kim by explicitly *prohibiting* Kim’s etch-stop layer material of undoped silicon nitride. *Bradium Techs. LLC v. Iancu*, 923 F.3d 1032, 1047 (Fed. Cir. 2019) (“A

⁹ Petitioner makes the same incorrect statements regarding Fang disclosing a silicon nitride etch-stop layer in support of multiple arguments in Grounds II and III. Those arguments should be disregarded for the same reasons discussed here.

prior art reference teaches away if it ‘criticizes, discredits, or otherwise discourages the solution claimed.’”) (citing *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004)); see Kim [0187]; Fang [0020]; Campbell2 ¶79. Fang states that the etch-stop material may be “**any material that is not substantially removed (e.g., etched) during removal and replacement of the nitride materials 120** of the staircase structure,” where “the nitride material 120 is silicon nitride (SiN).” Fang [0019]-[0020]. In other words, Fang **does not allow** for a silicon nitride etch stop and specifies an etch-stop material of CDSN because of its different etch chemistry than silicon nitride. *Id.*; see Ex.2021 55:4-9; Campbell2 ¶¶76, 79.

Second, a POSITA would know that Fang’s etch-stop-layer thicknesses are specific to a **combination** of CDSN etch-stop material and a silicon nitride sacrificial layer. See Fang [0019]-[0022] (identifying **only** silicon nitride as the “nitride material 120” and CDSN as the primary “etch stop material 130”); see also e.g., *id.* [0015], [0019], [0025], cls. 21-22; Campbell2 ¶77. For example, Fang states that “[s]ince the etch stop material 130 [i.e., CDSN] is not substantially removed by the etch chemistry used to remove the nitride materials 120 [i.e., silicon nitride] ..., **the thickness of the etch stop material 130 may be minimal and yet still provide desired etch stop properties.**” Fang [0021]. Kim discloses an undoped silicon nitride sacrificial layer but never contemplates a CDSN etch-stop material. Thus, Kim never uses the combination of etch-stop and sacrificial layer materials for which Fang’s

etch-stop thickness is designed. Campbell2 ¶¶77. Further, Kim uses a second etch-stop layer, where the thickness of one etch-stop layer may impact the thickness of the other etch-stop layer. *Id.* Kim's etch-stop layer 125a can also protect etch-stop layer 125b during removal of the sacrificial layer. *Id.* Finally, as discussed below, Kim also uses a high-k dielectric surrounding the conductive layer of each step providing yet more added protection. *Id.* Each of these features are specific to Kim and may further influence etch-stop layer thickness. *Id.* Thus, Petitioner is incorrect that a POSITA would look to Fang for exemplary etch-stop thicknesses for use in Kim where Kim uses a different etch-stop material and sacrificial layer combination, and adds a high-k dielectric layer surrounding the gate stack. *Id.*

c. Structural design differences between Fang and Kim counsel a POSITA against applying Fang's etch-stop-layer and contact-hole-etching characteristics to Kim.

In addition to the important differences between Fang and Kim's materials, Petitioner also ignores significant structural design differences that would counsel a POSITA against combining Fang's disclosures related to the etch-stop layer and contact-hole etching to Kim. *See* Campbell2 ¶¶81-82.

A POSITA would understand that the purpose of the etch-stop layer is to protect underlying structures during the etching process, making certain structural characteristics, such as the number and type of protective layers used, important to determining the necessary etching processes and etch-stop layer design. *Id.*; *see, e.g.,*

Fang [0026] (“[U]sing the etch stop material 130 according to embodiments of the disclosure prevents or reduces punch through into the conductive materials 140.”); Ex.1003 ¶93 (“[A]lthough Kim does not expressly state that the second stop layer 126b serves as an etch stop, a POSITA would have understood the etch selectivity of the second stop layer to serve the purpose of preventing punch-through and protecting underlying structures.”) (citing Kim [0186]-[0187]).

First, Kim discloses using a high-k dielectric layer around the conductive layer of each step while Fang does not. *See, e.g.*, Kim [0148], [0151], Fig. 22A. A POSITA would know that use of a high-k dielectric layer surrounding the conductive layer provides added protection to the gate stack layer. Campbell2 ¶82. It also affects the necessary etch processes and etch-stop layer characteristics (e.g., material, thickness) that must be considered when forming contact vias. *See, e.g.*, Campbell2 ¶¶50-51, 82; *see* Ex.2021 49:5-8 (“[T]he more different materials that you have that the etch has to go through, in general, that provides additional safety margins.”). Because Fang’s etch-stop layer is designed for a device that does *not* use a high-k dielectric layer surrounding the gate stack, a POSITA would not be motivated to apply Fang’s etch-stop layer characteristics and etching processes to Kim’s different design. Campbell2 ¶¶81-82.

Second, Kim discloses using two etch-stop layers while Fang discloses only a single etch-stop layer. Petitioner claims that arguing against the combination of

Fang and Kim on these grounds “would be wrong” because, according to Petitioner, presence or absence of a barrier layer does not impact the motivation to combine or the expectation of success. Pet. 73. But Petitioner is wrong. Kim’s two etch-stop layers generally provide further protection to underlying structures compared to Fang’s single-layer design and would require different etch processes and etch-stop characteristics than a single-layer design. *See* Kim Fig. 22A; Campbell2 ¶82; Ex.2021 49:5-8. For example, in a single-layer design thickness becomes more important to control etch times compared to a multi-layer design where etch selectivities between layers can be used. Banerjee Dep. 17:13-18:13; Campbell2 ¶82. Thus, a POSITA would not be motivated to apply thicknesses from a single-layer design like Fang to a multi-layer design like Kim. Campbell2 ¶82. Similarly, every time an additional layer is added, etch process must be altered and additional etch-chemistries considered depending on the materials and relationship between the layers. *Id.* Given these and other material differences, Petitioner has not shown a POSITA would have a reasonable expectation of success, especially where Kim does not use the same etch-stop materials as Fang.

Petitioner further argues that “none of claims 1, 3, and 6-8 requires or prohibits a barrier layer.” Pet. 73. Petitioner misses the point. These claims are directed towards etch processes and/or etch-stop layer characteristics such as etching steps, etch-stop materials, etch-stop thicknesses, and etch-stop layer formation,

which are impacted by the number and type of protective layers used in the device. Campbell2 ¶¶50-51, 81-82.

Petitioner also argues that Kim itself “discloses an embodiment with a single etch-stop layer 125.” Pet. 73. Kim’s sole embodiment disclosing a single etch-stop layer is from a separate embodiment than Figures 17A-22B upon which Petitioner bases Grounds 1 and 2, and Kim fails to provide any analysis to show a motivation to combine these disparate embodiments, nor a reasonable expectation of successfully doing so. *See* Kim Fig. 34; Section III.A.1. Further, the Figure 34 embodiment differs in material ways from the Figures 17A-22B embodiment, such as not having a high-k dielectric surrounding its conductive layers. *See* Campbell2 ¶82.

Petitioner also argues that “Kim does not teach or suggest that the thickness or deposition method of the etch-stop layer would be impacted by the number of etch-stop layers.” Pet. 73-74. A POSITA would not expect Kim to disclose such information where Kim’s focus is on reducing or preventing damage from CMP on the top of the device, and not on damage from etching contact holes at the etch-stop layer on the surface of the steps. *See* Section IV.B.1.a; Campbell2 ¶74. Further, a POSITA would know that the number of etch-stop layers may impact many etch-stop layer characteristics, such as the necessary thickness of the layers and the materials used. *See* Campbell2 ¶¶50-51, 81-82.

Third, to the extent Petitioner suggests a POSITA would be motivated to apply Fang's gate-stack-on-bottom etch-stop layer and contact-hole etching characteristics to Petitioner's modified, gate-stack-on-top version of Kim, Petitioner fails to account for the resulting differences. As described above in Ground 1, reordering layers requires changes in manufacturing and etch processes. *See, e.g., Campbell*2 ¶¶50-51, 81-82. A POSITA would know that etch-stop-layer and contact-hole-etching characteristics in Fang correspond to a gate-stack-on-bottom structure and would not apply the same to the gate-stack-on-top structure Petitioner argues is present in Kim. *Id.*

2. Petitioner fails to establish a motivation to combine Kim and Fang to render independent claim 1 obvious.

Petitioner fails to establish a motivation to combine the Kim and Fang references to render obvious claim 1's limitation of "disposing an etch-stop layer on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer" for the reasons described above.

Petitioner argues that a POSITA would have been motivated to use Fang's "alternative"¹⁰ etch-stop material, hafnium oxide, as the etch-stop material in the

¹⁰ While Fang includes a single mention of hafnium oxide as an "alternative" etch-stop material, in all other respects Fang is directed exclusively towards CDSN. *See*

combination because, according to Petitioner, it is a “suitable alternative” to silicon nitride, and because it has a greater tunneling length compared to a silicon nitride etch-stop layer. Pet. 67-68, 72-73. But Petitioner’s argument is based on its incorrect understanding of Fang. Campbell² ¶86. Fang discloses hafnium oxide as an alternative to *CDSN* and not to the undoped silicon nitride etch-stop used in Kim. Fang [0022]. Nor does Kim identify any tunneling problems that would motivate a POSITA to adopt Fang’s etch-stop to Kim. Pet. 72. Even if it did, Kim uses a two-etch-stop-layer design that provides added protection against tunneling. *See* Section VI.A.2. Thus, a POSITA would not be motivated to use Fang’s alternative hafnium oxide etch-stop material with Kim or have a reasonable expectation of successfully doing so.

Petitioner also argues a POSITA would have a reasonable expectation of success doing so because adopting Fang’s alternative material “represents applying what is already known to work in a similar device.” Pet. 67-68, 71. Each of Petitioner’s arguments fail.

First, a POSITA would not be motivated to apply Fang’s hafnium oxide etch-stop material to Kim to reduce tunneling. Kim makes no mention of the tunneling

Fang Title, Abstract, [0020], [0022] (identifying CDSN as the primary example of “etch stop material 130”), cls. 1-27 (*all claims* explicitly using CDSN).

problem, which was identified in Chen (Ex.1008), a reference that is not even part of this obviousness combination. Campbell2 ¶¶78, 85-87. Kim already includes a high-k dielectric layer surrounding the conductive layer of the gate stack. Chen's gate stack does not have this feature, and its experiments never take into account how this would impact tunneling length. Moreover, Kim already employs a two etch-stop-layer design, providing protection against the tunneling effect described by Chen and making further modification unnecessary. Kim does not suggest that it suffers from any tunneling issues or would benefit from further protection against the same. *Id.* Thus, a POSITA would not have been motivated to modify Kim as Petitioner suggests.

Second, a POSITA would not have a reasonable expectation of success adapting Fang's hafnium oxide etch-stop material to Kim's silicon nitride etch-stop because the prior art provides no guidance or disclosure for such an etch-stop with Kim's disclosure. *Id.* ¶¶76, 79, 86. Fang does **not** disclose hafnium oxide as an alternative to an undoped silicon nitride etch-stop, and neither reference provides guidance regarding the etch process parameters or design considerations related to using hafnium oxide as an etch-stop with Kim's materials. *See* Fang [0022]. Petitioner contends that there is a reasonable expectation of success because the etch-stop layer is selective to the insulating layer. Pet. 71. Yet, that argument does nothing more than describe why an etch-stop layer is an etch-stop layer. Campbell2 ¶86.

Further, etch-selectivity between the etch-stop layer and the connecting region insulating layer above it is dependent on, among other things, the materials used. *See id.* ¶¶51-52, 76. Nor would a POSITA consider Fang a “similar device” to Kim for purposes of these limitations for the additional reasons explained previously in Section IV.B.1. *Id.* ¶86. Thus, in the absence of any guidance specific to Kim’s device, Petitioner has failed to demonstrate a reasonable expectation of successfully incorporating Fang’s etch stop.

3. Petitioner fails to establish a motivation to combine the Kim and Fang references to render dependent claim 6 obvious.

Petitioner fails to establish a motivation to combine the Kim and Fang references to render claim 6 obvious, nor a reasonable expectation of successfully doing so. Claim 6 claims “[t]he method of claim 1, wherein disposing the etch-stop layer comprises disposing hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, and/or any combination thereof.” Petitioner fails to make this showing for at least the same reasons described above in Section IV.

In addition, Petitioner’s argument is based on its patently incorrect understanding of Fang’s etch-stop layer. *See* Pet. 67; Campbell2 ¶¶89-90. As discussed above, Fang specifically prohibits the use of a silicon nitride etch-stop layer. Campbell2 ¶¶76, 79, 86, 89-90. Yet Petitioner repeatedly affirms that Fang *discloses* a silicon nitride etch-stop layer. *See, e.g.,* Pet. 67-68, 71. And that Fang

discloses hafnium oxide as an alternative to this silicon nitride etch-stop layer.¹¹ *See, e.g.,* Pet. 67. Petitioner's arguments here and elsewhere are based on its misunderstanding of Fang. Campbell2 ¶¶89-90. Even Dr. Banerjee opines (incorrectly) that because Fang is proposing hafnium oxide as an alternative to a silicon nitride etch-stop material, a POSITA would be motivated to do the same in Kim and use hafnium oxide as an alternative to Kim's silicon nitride etch-stop. *Id.*; Ex.1003 ¶139. But Fang is referencing hafnium oxide as an alternative to *CDSN*, which has significantly different etch properties than silicon nitride. *See* Fang [0022], [0025] ("Since both [materials] are silicon nitride based, ... [i]t was ... surprising that the [CDSN] etch[-]stop material 130 is not removed by conventional etch chemistries used to remove nitride materials."); Campbell2 ¶¶76, 79, 86, 89-90.

Thus, applying Fang's hafnium oxide etch-stop layer to Kim is not applying "the same alternative [to a] similar device in the same way," as Petitioner contends, and a POSITA would not be motivated to make this combination, or have a reasonable expectation of success in doing so. Campbell2 ¶¶86, 89-90.

¹¹ Petitioner also states, incorrectly, that both of these materials would "meet Fang's criterion of not removing the etch-stop material when removing the sacrificial layers." Pet. 67. This is false because Fang's sacrificial layer is also made of silicon nitride. Fang [0019].

V. Ground III: Petitioner Failed to Demonstrate Han in View of Fang Renders Obvious Claims 1-15.

Petitioner fails to establish that it would have been obvious to combine the purported disclosures of Han's 3D NAND device with Fang's etch-stop to invalidate claims 1-15. Han fails to disclose, among other things, an etch-stop layer disposed on the staircase steps, an insulator disposed on the etch-stop layer, and contact-hole etching details for these layers. Campbell² ¶¶91. Petitioner relies on Fang to supply these and other deficiencies. But Petitioner ignores meaningful differences of Fang's device from Han's methods and structural design. These differences undermine Petitioner's proffered motivation to combine the two references disclosures, as well as a POSITA's reasonable expectation of successfully achieving such a combination. *Id.* ¶¶91-97.

A. Petitioner fails to establish a motivation to combine Han and Fang or a reasonable expectation of success in doing so.

1. POSITAs would not have been motivated to adapt Fang's etch-stop layer to Han.

Fundamental differences in Han and Fang's structural designs and manufacturing processes would counsel a POSITA against combining Han and Fang. These fundamental differences outweigh any purported motivation based on their both using well-known manufacturing methods and render Fang's etch-stop layer unnecessary and redundant. *See* Pet. 102-03 (arguing motivation based on both references using certain well-known manufacturing methods). For at least the

following three reasons, a POSITA would not have been motivated to adapt Fang, including etch-stop layer characteristics and contact-hole etching, to Han. Campbell2 ¶¶91-97.

First, Han's gate stacks differ significantly from Fang's and render Fang's etch-stop layer unnecessary. *Id.* ¶92. Han's gate stacks have multiple high-k dielectric layers surrounding the conductive layer of each step. Han [0141]. These layers provide protection both during deposition of the conductive layer and against punch-through during the etching of contact holes. Campbell2 ¶92. Fang's gate stacks, however, do not have this feature and thus require an etch-stop layer to protect against punch-through. *Id.* A POSITA would know that each additional protective layer requires changes to the etch parameters, additional etch steps, and different etch chemistries. *Id.* ¶¶92-96. These changes increase manufacturing cost, time, and complexity. *Id.* Thus, as Han's current design provides adequate protection to underlying structures, a POSITA would not be motivated to add an additional etch-stop layer from Fang. *Id.*; see Section III.A.2; *Provisur Techs., Inc. v. Weber, Inc.*, 2022 WL 17688071, at *5 (Fed. Cir. Dec. 15, 2022) (affirming Board's finding that "because of this increased complexity [of the proposed combination], a person of ordinary skill in the art would have lacked motivation to combine the references and modify them to obtain" the claimed arrangement); Banerjee Dep. 58:8-59:12 (admitting that additional etch-steps add cost and complexity).

Second, Han's manufacturing provides for a staged etching process, further rendering Fang's etch-stop layer unnecessary. Campbell2 ¶93. Unlike Fang, Han delineates upper and lower contact holes and allows forming these contact hole openings at different times—for example, forming the upper holes before the lower holes. Han [0156]; Campbell2 ¶93. This mitigates the risk of punch-through in the upper holes because they are not continuing to etch while waiting for lower, deeper holes to finish. Campbell2 ¶93. Further, a POSITA would have understood that this staged etching approach is beneficial because it can use a single etch chemistry and eliminates having to deposit an additional etch-stop layer on the staircase steps, avoiding the cost, time, and complexity of disposing an additional layer on the structure and requiring another etch process and chemistry during manufacturing. *Id.* A POSITA would not have found an additional layer helpful and would not have been motivated to add it where Han already provided adequate protection against punch-through in other ways. *Id.*

Third, Han and Fang also have different staircase ordering and compositions. Han employs a gate-stack-on-top model and Fang does not. *Id.* ¶94. These structural design differences would motivate a POSITA against combination and defeat a reasonable expectation of success, for the same reasons discussed above in Section III.A.2 regarding the challenges of reordering layers in the staircase structure. *Id.*

For each of these reasons, a POSITA would not be motivated to combine the Han and Fang references. These same differences undermine Petitioner's contention that "similar materials" in Han's and Fang's staircase structures would bolster a reasonable expectation of success (Pet. 79; Ex.1003 ¶163; Campbell2 ¶95), because similarity in staircase materials does not remove the necessary adjustments to etch parameters and etch chemistries required by an additional etch-stop layer during the manufacturing process. Campbell2 ¶95.

Petitioner's primary argument is that a POSITA would have been motivated to adapt Fang's etch-stop layer to Han to protect against "punch-through." But as described above, Han already addressed this problem in at least two ways. *Id.* ¶96. Thus, a POSITA would not have been motivated to add Fang's redundant etch-stop layer to Han. *Id.*; see *S.-Tek Sys., LLC v. Engineered Corrosion Sols., LLC*, 748 F. App'x 1003, 1007 (Fed. Cir. 2018) (affirming Board's finding that a POSITA would not be motivated to combine a reference that provided "redundant function").

Relatedly, Petitioner argues, without support, that Han would have suffered from the "shortcomings of the conventional solutions [to over etching]," and so a POSITA would have been further motivated to adapt Fang's etch-stop layer to Han's staircase structure. Pet. 102. Petitioner again ignores the fundamental differences between Han's and Fang's design described above. Campbell2 ¶97. Petitioner relies only on purported shortcomings described in Fang's device to argue Han would

suffer from the same issues. *Id.* But Han's design differs from Fang's, for example, by using multiple high-k dielectric layers surrounding its conductive layer, which protect against punch-through. *Id.* Petitioner fails to cite to any disclosures in Han to support its assertion that Han suffers from the same problems described in Fang. *Id.* Petitioner is not permitted to "create a problem with the prior art in hopes of creating a motivation to combine references." *See Arctic Cat Inc. v. Polaris Indus., Inc.*, 795 F. App'x 827, 833 (Fed. Cir. 2019).

B. Han in view of Fang does not disclose "etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer of each step" in claim 4.

1. Petitioner improperly relies on additional background references and a POSITA's knowledge.

Petitioner fails to show claim 4 is obvious over Han in view of Fang. Dependent claim 4 claims "[t]he method of claim 1, wherein etching the exposed portions of the etch-stop layer comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer of each step."

Neither Han nor Fang disclose this limitation. To cure their deficient disclosures, Petitioner improperly relies on a POSITA's knowledge to gap-fill this missing limitation. Petitioner's arguments fail for the same reasons described in Section III.A.2. To the extent Petitioner argues that it relied on background

references such as Shamiryan (Ex.1025) and Morel (Ex.1026) (*see, e.g.*, Pet. 91-92), this argument is equally improper for the same reasons described in Section III.A.2.

Further, the missing limitation of “etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer of each step” is not “unusually simple” for the reasons described previously regarding etch-processes, nor is 3D NAND memory array manufacturing and design a “particularly straightforward” technology. *See* Campbell2 ¶¶62-63, 98; Section III.A.2. Further, Fang is a gate-stack-on-bottom structure, meaning its etch-stop layer is separated from its gate stack by a dielectric insulating layer. Campbell2 ¶99.

C. Han in view of Fang does not disclose “etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the first high-k dielectric layer” of claim 5.

1. Petitioner improperly relies on additional background references and a POSITA's knowledge.

Petitioner fails to show claim 5 is obvious over Han in view of Fang. Dependent claim 5 claims “[t]he method of claim 4, wherein etching the exposed portions of the etch-stop layer further comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the first high-k dielectric layer.”

Neither Han nor Fang disclose this limitation. To cure their deficient disclosures, Petitioner improperly relies on a POSITA's knowledge to gap-fill this missing limitation. Petitioner's arguments fail for the same reasons described in

Section III.A.2. To the extent Petitioner argues that it relied on background references such as Kim, et al. (Ex.1027) (*see, e.g.*, Pet. 92), this argument is equally improper for the same reasons described in Section III.A.2.

Further, the missing limitation of “etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the first high-k dielectric layer” is not “unusually simple” for the reasons described previously regarding etch-processes, nor is 3D NAND memory array manufacturing and design a “particularly straightforward” technology. *See* Campbell2 ¶100; Section III.A.2.

2. Petitioner fails to establish a motivation to combine Kim in view of a POSITA's knowledge to render claim 5 obvious, or a reasonable expectation of successfully doing so.

Petitioner's arguments also fail for the reasons described above in Sections III.D.2 and V.A—specifically as they relate to Han's use of a high-k dielectric layer surrounding conductive layers, whether Han requires additional protection during contact hole etching, and if so, whether the claimed etch-rate relationship is the “only ... sensible relationship” between the etch-stop and first high-k dielectric layers. *See, e.g.*, Pet. 92, 102-03; Campbell2 ¶¶100-103. Further, a POSITA would not have a reasonable expectation of success achieving the claimed arrangement combining Han in view of Fang where neither device itself is designed to include both an etch-stop layer and a first high-k dielectric layer. Campbell2 ¶¶100-103.

Petitioner's argument also fails because the background reference Petitioner cites to is irrelevant and does not actually support its argument. Pet. 92 (citing Ex.1027). This reference shows that an aluminum oxide etch-stop layer has a higher etching rate than a hafnium oxide insulating layer relative to argon plasma etchant. *See id.* But a POSITA would not use a simple argon plasma for the complex silicon technology at issue. Campbell2 ¶102. Further, Fang is directed towards a CDSN etch-stop material and does not mention or use an aluminum oxide etch-stop material. Campbell2 ¶102. And as Dr. Banerjee has stated, etch rates depend on both the material and the etch chemistry used. Ex.1003 ¶52. Thus, Petitioner cannot generalize a single example using different materials to render claim 5 obvious.

VI. Ground IV: Petitioner Failed to Demonstrate Han in View of Fang and Chen Renders Obvious Claims 17 and 18.¹²

This Ground includes the same references as Ground III, with the addition of Chen. Petitioner does not assert Chen discloses or renders obvious any limitation of claim 1. Pet. 12, 103-05; ID 4. Instead, it argues Chen's "first stop layer 210" along with Han's staircase structure and Fang's etch-stop layer renders obvious claims 17 and 18. Pet. 103-05. Because Han in view of Fang does not render obvious claim 1,

¹² The Board stated it instituted Petitioner's challenges to claims 16 and 17 based on Han, Fang, and Chen. ID 15. But the Petition relies on that combination only to challenge claims 17 and 18. Pet. 103, 105.

Ground IV fails for the same reason. Regardless, Han in view of Fang and Chen, does not render obvious claims 17 and 18.¹³

Claim 17 recites “prior to disposing the etch-stop layer, disposing a barrier layer on each step of the plurality of steps, wherein the barrier layer protects underlying structures during the etching of the exposed portions of the etch-stop layer.” ’276 patent cl. 17. Claim 17 depends from claim 1. *Id.* Claim 18 depends from claim 17 and further recites “wherein disposing the barrier layer comprises disposing one or more of silicon oxide, silicon oxynitride, silicon nitride, TEOS, aluminum oxide, and silicon oxide incorporated with F, C, N, or H.” *Id.* cl. 18.

A. Petitioner fails to establish a motivation to combine Chen with Han and Fang, or a reasonable expectation of success in doing so.

Petitioner argues a POSITA would be motivated to add Chen’s teaching of depositing a “first stop layer 210” to the Han and Fang combination. Pet. 103-05. For the reasons discussed above, a POSITA would not be motivated to combine Fang’s etch-stop layer to Han’s staircase structure. *See* Section V.A. Thus, Petitioner has not established a motivation to combine Han, Fang, and Chen.

Regardless, Petitioner asserts a POSITA would have been motivated to add a barrier layer between Han’s staircase structure and Fang’s etch-stop layer to prevent

¹³ Because claim 18 depends from claim 17, Petitioner failed to prove claim 18 is unpatentable for the same reasons as claim 17.

“[u]intended short circuits.” Pet. 105. According to Petitioner, Chen “discloses a solution: increasing the tunneling length of the etch-stop layer(s) to reduce tunneling current” by “adding a barrier layer to a high-k dielectric etch-stop layer.” *Id.* 105-06. Similar to Ground III—and even more so when all three references are combined—Petitioner overlooks significant differences between the three references by oversimplifying structural and manufacturing differences that counsel away from combining the three asserted references. Thus, a POSITA would not have been motivated to combine Chen to the Han and Fang combination.

1. Neither Han Nor Han and Fang benefit from an additional etch-protecting barrier.

As explained regarding Ground III, Fang's etch-stop layer does not provide additional benefits to Han because Han prevents punch-through during etching. Section V.A.1; Campbell2 ¶92. As a result, a POSITA would have considered Fang's etch-stop layer to be redundant and would not motivate him to combine Han and Fang. Section V.A.1; Campbell2 ¶¶91-96; *see S.-Tek Sys.*, 748 F. App'x at 1007 (affirming Board's finding that a POSITA would not be motivated to combine a reference that provided “redundant function”).

Petitioner's asserted combination of Han, Fang, and Chen exacerbates the redundancy, and a POSITA would not be motivated to combine all three. Campbell2 ¶¶105-106. To the extent Petitioner is correct that a POSITA would have been motivated to add Fang's etch-stop layer to Han despite Han teaching that its methods

already protect the underlying structures, a POSITA would certainly not have then been motivated to provide an additional etch-protection layer from an additional reference in combination with Fang's etch-stop layer. *Id.*

2. Chen's tunneling length would not motivate a POSITA to add Fang's first stop layer to the Han and Fang combination.

Petitioner argues that a POSITA would have been motivated to implement Chen's first stop layer in Han and Fang because it would increase the tunneling length, reducing the risk of short circuits. Pet. 105. This ignores, however, that unlike Chen, Han *already* has at least a single, and potentially a second, high-k dielectric layer, including aluminum oxide. Section V.A; Campbell2 ¶107; Han [0141]. And when combined with Fang's etch-stop layer (which a POSITA would not do for the reasons discussed above), the combination would have a third layer also comprising materials with the same preferred energy gap properties listed in Chen. Campbell2 ¶107; Chen [0053]; Fang [0020]. Thus, adding a fourth layer would be entirely redundant and is not suggested by Chen. Sections V.A.1, VI.A.1. Moreover, as explained above, a POSITA would not be motivated to add layers where they can be avoided, which would increase process complexity, cost, and time. Sections III.A.2, V.A.1.

3. A POSITA would be dissuaded from adding Chen's first stop layer to Han and Fang because of structural design and process differences.

As explained in Ground III, adding additional etch-protecting layers to Han creates design and process difficulties. Adding Chen compounds these difficulties and would have motivated a POSITA against combining Han, Fang, and Chen. Like adding Fang to Han, adding a third or fourth layer with structural differences between Han, Fang, and Chen necessitates new manufacturing and etch processes, specifically, additional etch steps that can add cost and complexity as discussed above. Sections III.A.2, V.A.1; Campbell2 ¶109; *Provisur Techs.*, 2022 WL 17688071, at *5 (affirming Board's finding that "because of this increased complexity [of the combination], a person of ordinary skill in the art would have lacked motivation to combine the references and modify them to obtain" the claimed arrangement).

Petitioner argues that adding an additional layer is "simply that one step of forming layer 200 [i.e., one layer] 'is divided into two steps'" and is also a "design choice." Pet. 106-07 (citing Chen [0053]; *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023)). But Chen not only recognizes that the order of the layers matter, but that the materials used and the device design, including tunneling length properties, are also interrelated choices that a POSITA must make. Chen [0041], [0048]-[0052]. Indeed, Dr. Banerjee admitted the combining Chen's

first stop layer would *further* increase the complexity and quantity of etching processes. Banerjee Dep. 58:9-59:12; Campbell2 ¶109; Sections V.A.1, III.A.2. Moreover, a POSITA still must have a reason to modify the references, even if the modification was well-known as Petitioner asserts. *See Forest Laboratories, LLC v. Sigmapharm Laboratories, LLC*, 918 F.3d 928, 934 (Fed. Cir. 2019) (“An invention is not obvious simply because all of the claimed limitations were known in the prior art at the time of the invention.”).

Moreover, to the extent Petitioner invokes the “known-technique” doctrine in arguing a POSITA would employ a two-etch stop layer design to solve a purported “known problem” with the one etch-stop layer in Fang (Pet. 107 (citing *Intel*, 61 F.4th at 1380)), the Petitioner fails to establish Chen would address the problem of punch-through to “improve” the claimed combination “in the same way” (*see Intel*, 61 F.4th at 1381). Rather, Petitioner asserts merely that Chen’s etching stop layer 200 can be “divided into two separate steps.” Pet. 107. But, as explained above, Chen’s two-layer solution is, at most, directed to solving problems related to tunneling length and does not provide any known solution to limiting punch-through. Thus, a POSITA would not be motivated to combine Chen with Fang and Han.

VII. Conclusion

For the reasons set forth above, the Board should deny the Petition for Inter Partes Review.

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE WITH 37 C.F.R. § 42.24

I hereby certify that this Patent Owner's Response complies with the word count limitation of 37 C.F.R. § 42.24(b)(2) because the Patent Owner's Response contains a total of 13,972 words, which is the sum of 13,853 words calculated by Microsoft Word's word-count feature and 119 words hand counted in the figures. This total excludes the cover page, signature block, and the parts of the Patent Owner's Response exempted by 37 C.F.R. § 42.24(b)(2).

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 27th day of October, 2025, a true and correct copy of the foregoing **Patent Owner's Response and all Exhibits** were served by electronic mail on Petitioner's lead and backup counsel at the following email addresses:

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