

Filed on Behalf of: Yangtze Memory Technologies Company, Ltd.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00228
Patent 11,101,276

**DECLARATION OF STEPHEN CAMPBELL
IN SUPPORT OF
PATENT OWNER'S RESPONSE**

Table of Contents

I.	Introduction and Qualifications	1
II.	Summary of Materials Reviewed and Considered	3
III.	Understanding of Legal Standards.....	7
A.	Claim Construction.....	8
B.	Obviousness.....	9
IV.	Level of Ordinary Skill in the Art.....	12
V.	Overview of the '276 patent (Ex.1001)	13
VI.	Ground I: Claims 1-2, 4-5, and 9-18 in View of Kim and the Knowledge of a POSITA.	21
A.	Kim does not disclose “each step of the plurality of steps comprises disposing a sacrificial layer over a dielectric layer.” 21	
1.	3D NAND is complex technology.	34
2.	Re-ordering sacrificial and insulating layers is a complex process.	35
B.	Kim does not disclose “forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer” of claim 1.....	38
C.	Kim in view of a POSITA’s knowledge does not render obvious “etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer” of claim 4.....	42
D.	Kim does not disclose “etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the first high-k dielectric layer” of claim 5.....	44
1.	Petitioner fails to establish a motivation to combine Kim in view of a POSITA’s knowledge to render claim 5 obvious, or a reasonable expectation of successfully doing so.....	44
E.	Kim does not disclose “forming the ... conductive structures further comprises planarizing the conductive materials and the insulating layer” of claim 11.....	46

VII.	Ground II: Claims 1, 3, 6-8 over Kim in View of Fang.	47
A.	Fang does not disclose “each step ... comprises disposing a sacrificial layer over a dielectric layer” of claim 1.....	47
B.	There is no motivation to combine Kim in view of Fang or a reasonable expectation of successfully doing so.	47
1.	A POSITA would not have been motivated to combine Fang’s etch-stop characteristics and contact-hole etching to Kim.	48
2.	There is no motivation to combine the Kim and Fang references to render independent claim 1 obvious.	56
3.	There is no motivation to combine Kim and Fang to render claim 6 obvious.	59
VIII.	Ground III: Petitioner Failed to Demonstrate Han in View of Fang Renders Obvious Claims 1-15.	60
A.	There is no motivation to combine Han in view of Fang or a reasonable expectation of successfully doing so.	60
B.	Han in view of Fang does not disclose “etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer of each step” of claim 4. ...	65
C.	Han in view of Fang does not disclose “etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the first high-k dielectric layer” of claim 5.	65
IX.	Ground IV: Claims 17 and 18 over Han in View of Fang and Chen....	68
A.	There is no motivation to combine the Han, Fang, and Chen references to render claim 17 obvious.	68
X.	CONCLUSION	71

I. Introduction and Qualifications

1. I have been retained by Yangtze Memory Technologies Company, Ltd. (“YMTC” or “Patent Owner”) to provide my opinion concerning the validity of U.S. Patent No. 11,101,276 (Ex.1001) (“’276 patent”).

2. I received my Bachelor’s degree in Physics from the University of St. Thomas (St. Paul, Minnesota) in 1975, and my M.S. and Ph.D. in Physics from Northwestern University (Evanston, Illinois) in 1978 and 1981, respectively. I then joined Sperry, now called Unisys, in 1981 as a CMOS process development engineer. In 1982, I was assigned the lead engineer for the 1.2 μm technology process development effort. In 1984 I was promoted to head of silicon research for the company. This involved a wide variety of process technologies for submicron CMOS.

3. In 1986, I joined the University of Minnesota as an Assistant Professor in the Electrical Engineering Department. My research at the University involved semiconductor processing, materials, and device structures. I raised more than \$100M in various grants and successful submissions to companies and industry consortiums such as the Semiconductor Research Association, as well as State and US government agencies including DARPA and the National Science Foundation. The first ten years of my career at the University concentrated on the development of rapid thermal annealing for 200 mm wafers, particle control in

CVD systems, and the development of high uniformity rapid wafer annealing systems. The next ten years were dedicated to the invention and development of high permittivity (aka high-k) films for use as gate insulators. This is necessary to allow the development of deeply scaled CMOS devices. This technology has been widely adopted for nanoscale CMOS devices. In the last fifteen years at the University, my work involved the development of low-cost tandem photovoltaics and micro electromechanical systems (MEMS). The latter included a chronic deep brain sense/stimulation system and very high-speed mechanical switches. Finally, I developed processes for the fabrication of novel 2D materials such as black arsenic, and fabricated transistors using these materials. I retired from the University in 2021.

4. A brief summary of my work at the University would include:

- Approximately 200 publications
- The leading textbook on semiconductor technology. Currently in its fourth edition, Fabrication Engineering at the Micro and Nanoscale (Oxford 1996, 2000, 2008, 2013) is the dominant text on the topic.
- Honors from outside the University such as being named a Presidential Young Investigator by the National Science

Foundation and a Life Fellow by the Institute of Electrical and Electronic Engineers (IEEE).

- Honors within the University including outstanding service and outstanding teaching.
- As the Director of the University's Nanofabrication Center, I increased lab usage from 30 to more than 300 users, enabling millions of dollars research awards annually by Minnesota faculty, and leading to the construction of a new \$80M building with an expansive cleanroom facility.

5. Since retiring from the University, I have consulted with multiple semiconductor companies including patent litigation and have taught process technology short courses in industry.

6. Additional information regarding my education, technical experience and publications, including a list of the U.S. patents of which I am an inventor/coinventor, is included in my *Curriculum Vitae*, which I understand is provided at Exhibit 2007.

II. Summary of Materials Reviewed and Considered

7. All of the opinions contained in this Declaration are based on the documents I reviewed and my knowledge and professional judgment. In forming

the opinions expressed in this Declaration, while drawing on my experience in the field of semiconductor fabrication, I reviewed the following documents:

Ex.	Description
1001	U.S. Patent No. 11,101,276 to Zhu et al. (“’276 patent”)
1002	File History of U.S. Patent No. 11,101,276 (“’276 FH”)
1003	Declaration of Dr. Sanjay Banerjee
1004	Curriculum Vitae of Dr. Sanjay Banerjee
1005	U.S. Patent Publication No. 2012/0070944A1 to Kim et al. (“Kim”)
1006	U.S. Patent Publication No. 2019/0067306A1 to Fang et al. (“Fang”)
1006	Korean Patent No. 10-2015-0051841 to Park et al. (“Park”) including certified translation
1007	U.S. Patent Publication No. 2017/0062470A1 to Han (“Han”)
1008	U.S. Patent Publication No. 2017/0294384A1 to Chen (“Chen”)
1010	Aritome, “NAND Flash Memory Technologies” (2016)
1011	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
1012	Michelsoni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)
1013	U.S. Patent Publication No. 2017/0117222A1 to Kim et al.
1014	Chang and Sze, “ULSI Technology” (1996)
1015	Orlowski et al., <i>Si, SiGe, Ge, and III-V Semiconductor Nanomembranes and Nanowires Enabled by SiGe Epitaxy</i> , ECS Transactions Vo. 33, No. 6 (2010), 777-89
1016	U.S. Patent No. 9,728,547 to Ohsaki et al.
1017	U.S. Patent Publication No. 2017/0148677A1 to Shin
1020	Korean Patent Publication No. KR10-2013-0015120 (“Lee”) with machine translation

Ex.	Description
2001	Defendants' Preliminary Invalidity Contentions and Document Production Accompanying Invalidity Contentions re YMTC II Asserted Patents (Patent Local Rules 3-3 and 3-4), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Nov. 25, 2024) (excerpts)
2002	Civil Minutes, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Sept. 18, 2024), ECF No. 141
2003	Order Granting Stipulation to Extend Certain Deadlines Pursuant to Patent L.R. 4-2 and the Scheduling Order (ECF No. 141) Pursuant to Civil Local Rule 6-1(b), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Jan. 8, 2025), ECF No. 194
2004	Order Granting Motion to Stay Case Pending <i>Inter Partes</i> Review, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Mar. 14, 2025), ECF No. 243
2005	Plaintiff/Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.'s and Counterclaim Defendant Yangtze Memory Technologies, Inc.'s Opposition to Micron's Motion to Stay Case Pending <i>Inter Partes</i> Review and Post-Grant Proceedings, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Feb. 3, 2025), ECF No. 221
2006	Declaration of Stephen Campbell in Support of Patent Owner's Preliminary Response ("Campbell")
2007	<i>Curriculum Vitae</i> of Stephen Campbell
2018	Order Granting Motion to Consolidate, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Aug. 21, 2024), ECF No. 106
2020	Transcript of the Deposition of Sanjay Banerjee, Ph.D., taken October 2, 2025, <i>Micron Tech., Inc. v. Yangtze Memory Techs. Co.</i> , IPR2025-00228 (Patent No. 11,101,276)

Ex.	Description
2021	Transcript of the Deposition of Sanjay Banerjee, Ph.D., taken August 13, 2025, <i>Micron Tech., Inc. v. Yangtze Memory Techs. Co.</i> , IPR2025-00117 (Patent No. 10,672,711)
2022	<i>3D Flash Memories</i> (Rino Micheloni ed., 2016)
2023	Harmeet Singh, <i>Overcoming Challenges in 3D NAND Volume Manufacturing</i> , 60 Solid State Tech. 18 (July 2017) (excerpt)
2024	Thermo Fisher Scientific, <i>White Paper: The Challenge of Measuring Buried Critical Dimensions in High-Aspect-Ratio Structures: How Busy Fab Process Owners Can Reduce Time-to-Data in 3D NAND Metrology</i> , https://assets.thermofisher.com/TFS-Assets/MSD/Reference-Materials/helios-5-pxl-3d-nand-whitepaper-wp0025.pdf (last visited Aug. 5, 2025)
2025	Mark Lapedus, <i>What's Next for NAND?: Vendors Pin Hopes on 3D Memory, Raising Specter of 2D NAND Shortages; Other Memory Types Add to Uncertainty</i> , Semiconductor Eng'g (May 19, 2016), https://web.archive.org/web/20161127122539/https://semiengineering.com/whats-next-for-nand/ (last visited Aug. 15, 2025)
2026	Mark Shirey & Janay Camp, <i>Digging Deep Into High Aspect Ratio Process Control for Memory Technology</i> , Semiconductor Eng'g (Oct. 18, 2018), https://web.archive.org/web/20250621011306/https://semiengineering.com/digging-deep-into-high-aspect-ratio-process-control-formemory-technology/ (last visited Aug. 15, 2025)
2027	Mark Lapedus, <i>3D NAND Flash Wars Begin: Market Overcrowding, More Efficient Manufacturing, and Growing List of Scaling Issues Create a Challenging Competitive Landscape</i> , Semiconductor Eng'g (Aug. 20, 2018), https://web.archive.org/web/20180822030129/https://semiengineering.com/3d-nand-flash-wars-begin/ (last visited Aug. 15, 2025)
2028	Mark Lapedus, <i>3D NAND Metrology Challenges Growing: Rising Costs and Gaps in Equipment Emerge as Technology Scales; New Tools Under Development</i> , Semiconductor Eng'g (Apr. 9, 2019), https://semiengineering.com/3d-nand-metrology-challenges-growing/

Ex.	Description
2029	Mark Lapedus, <i>3D NAND's Vertical Scaling Race: More Competition, Business Uncertainty, and Much More Difficult Manufacturing Processes</i> , Semiconductor Eng'g (Dec. 17, 2020), https://semiengineering.com/3d-nands-vertical-scaling-race/
2030	Stephen A. Campbell, <i>Fabrication Engineering at the Micro- and Nanoscale</i> 297 (Adel S. Sedra ed., 4th ed. 2013) (excerpt)

8. My opinions are additionally guided by my appreciation of how a person of ordinary skill in the art would have understood the claims of the '276 patent at the time of the alleged invention, which I have been asked to assume is August 31, 2017.

III. Understanding of Legal Standards

9. I am not an attorney, and in this Declaration, I do not opine on matters of law. For the purposes of this Declaration, I have been informed about certain aspects of the law that are relevant to my analysis and opinions. My understanding of these principles is set forth below.

10. I have been informed by Counsel that the validity analysis is a two-step process. First, the patent claims are construed to ascertain their proper scope. Second, the construed claims are compared to the identified prior art to determine if the claims are valid over the prior art.

A. Claim Construction

11. I have been informed by Counsel that the claims of a patent define the limits of the patentee's exclusive rights. I have been informed by Counsel that to determine the scope of the claimed invention, courts typically construe claim terms, the meaning of which the parties may dispute. I have been informed by Counsel that claim terms should generally be given their ordinary and customary meaning as understood by one of ordinary skill in the art at the time of filing of the patent application, after reading the patent and its prosecution history. I also have been informed by Counsel that a basic tenet of claim construction presumes that different words in a claim have different meanings, unless there is evidence to the contrary.

12. I have been informed by Counsel that claims must be construed in light of, and consistent with, the intrinsic evidence. In this context, I have been informed by Counsel that intrinsic evidence includes the claims themselves, the written disclosure in the specification, and the patent's prosecution history, including prior art that was considered by the United States Patent and Trademark Office ("USPTO"). I have been informed by Counsel that the specification is always highly relevant to the claim construction analysis and often is the single best guide to the meaning of a disputed term. I have been informed by Counsel that extrinsic evidence may also be considered when construing claims and may

include, for example, technical dictionaries, technical publications and books, treatises, and expert testimony.

B. Obviousness

13. I have been informed by Counsel that patent claims can be deemed invalid if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. While such conclusions are often based on more than one piece of prior art, only one is required. It is not sufficient that a collection of prior art references merely recites the various elements of a challenged patent claim. Rather, as I have been informed by Counsel, the prior art must present the elements in a manner that is consistent with their arrangement or use in the challenged claims. I have been informed by Counsel that obviousness cannot be based on the hindsight combination of components selectively culled from the prior art.

14. I have been informed by Counsel that a person having ordinary skill in the art (i.e., a POSITA), is a hypothetical person who is presumed to have known the relevant art at the time the invention was made. I have been informed by Counsel that the condition “at the time the invention was made” is imposed to rule out impermissible hindsight. I also have been informed by Counsel that an expert is to analyze the prior art from the perspective of a person of ordinary skill in the

art at the time the invention was made, and not simply to provide his/her own personal conclusions.

15. I also have been informed by Counsel that an obviousness determination includes several factual inquiries, including (1) determining the scope and content of the prior art; (2) ascertaining the differences between the claimed invention and the prior art; (3) resolving the level of ordinary skill in the pertinent art; and (4) taking into consideration any objective indicia of nonobviousness.

16. I have been informed by Counsel that obviousness must be determined as of the date of the invention (i.e., the effective filing date or priority date of the patent). Thus, in considering the reason or motivation to combine references, it is essential to avoid using hindsight. For example, the problem examined when considering obviousness is the general problem that confronted the inventor before the invention was made, not the specific problem solved by the invention. Defining the problem in terms of its solution reveals improper hindsight in the selection of the prior art relevant to obviousness. Further, an overly narrow statement of the problem can represent a form of hindsight, because often the inventive contribution lies in defining the problem in a new revelatory way. Similarly, an assertion that a person of ordinary skill could combine the references, rather than that they would have been motivated to do so, is an impermissible form

of hindsight. Moreover, knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references to reach the particular claimed invention.

17. I have been informed by Counsel that a motivation to solve a problem (or issue) is not the same as a motivation to have combined references. I have been informed by Counsel that whether a skilled artisan would be motivated to make a combination includes whether he/she would select particular references in order to combine their elements.

18. I have been informed by Counsel that the analysis of the motivation to combine should be explicit. Additionally, it must include articulated reasoning with rational underpinnings to support the conclusion of obviousness. Providing a full explanation of the motivation to combine the references and the reasonable expectation of success is a necessary component of the obviousness inquiry, as inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known. However, conclusory statements fail to adequately explain why a person of ordinary skill would have a motivation to combine the potential prior art references.

19. I have been informed by Counsel that common sense, common wisdom, and common knowledge may be used to support a motivation to combine,

so long as the use of common sense in the analysis is explained with sufficient reasoning. But, common sense can only be used to supply a limitation missing from the prior art where the technology is unusually simple and straightforward.

20. I also have been informed by Counsel that evidence suggesting reasons to combine cannot be viewed apart from evidence suggesting reasons not to combine. In analyzing motivation, both advantages and disadvantages must be considered. Teaching away, for example, is a statement in the prior art that either (i) discourages one from following the path of the claimed invention, or (ii) encourages one to follow a path that diverges from the path of the claimed invention. The concept of teaching away bears directly on whether there was a reason to combine prior art. Known disadvantages in prior art technology or devices which would naturally discourage a search for new inventions may also be taken into account in determining obviousness.

IV. Level of Ordinary Skill in the Art

21. Dr. Banerjee defines a person of ordinary skill in the art (“POSITA”) as a person having “a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (e.g.,

an advanced degree may replace some of the professional experience).” Ex.1003 (Banerjee Decl.) ¶42.

22. For the purposes of this declaration, I have not been asked to provide an opinion on the level of ordinary skill in the art. In view of my educational background and work experience, I surpass Dr. Banerjee’s definition of a POSITA, and did so before August 31, 2017. I have adopted the point of view of a POSITA for purposes of my opinions in this declaration. Regardless of the precise definition of a POSITA, Grounds I-IV of the Petition do not show the challenged claims obvious.

V. Overview of the ’276 patent (Ex.1001)

23. The ’276 patent is titled “Word Line Contact Structure for Three-Dimensional Memory Devices and Fabrication Methods Thereof.” Such design and manufacturing involves concepts from chemical, mechanical, and electrical engineering and applies them at a microscopic scale. In my opinion, such technologies are not straightforward. More specifically, the specification discloses “a word line contact structure for three-dimensional (3D) memory array and methods for forming the same.” ’276 patent 1:40-42.

24. To meet the demand for higher storage capacity, manufacturers have tried to increase the number of conductor/dielectric layer pairs in 3D memory devices, which created challenges of balancing manufacturing throughput and

process complexity/cost. *Id.* 5:42-46. Lithography and etching processes create holes in the insulating layer above the staircase structure that are then filled with conductive material to create contacts for conductive layers of the staircase. *Id.* 5:47-49. The required hole depth depends on the distance between the top of the insulating layer and the conductive layer of each level, and can vary between steps. *Id.* 5:49-54. This leads to holes for lower levels being deeper than holes for the upper levels. *Id.*

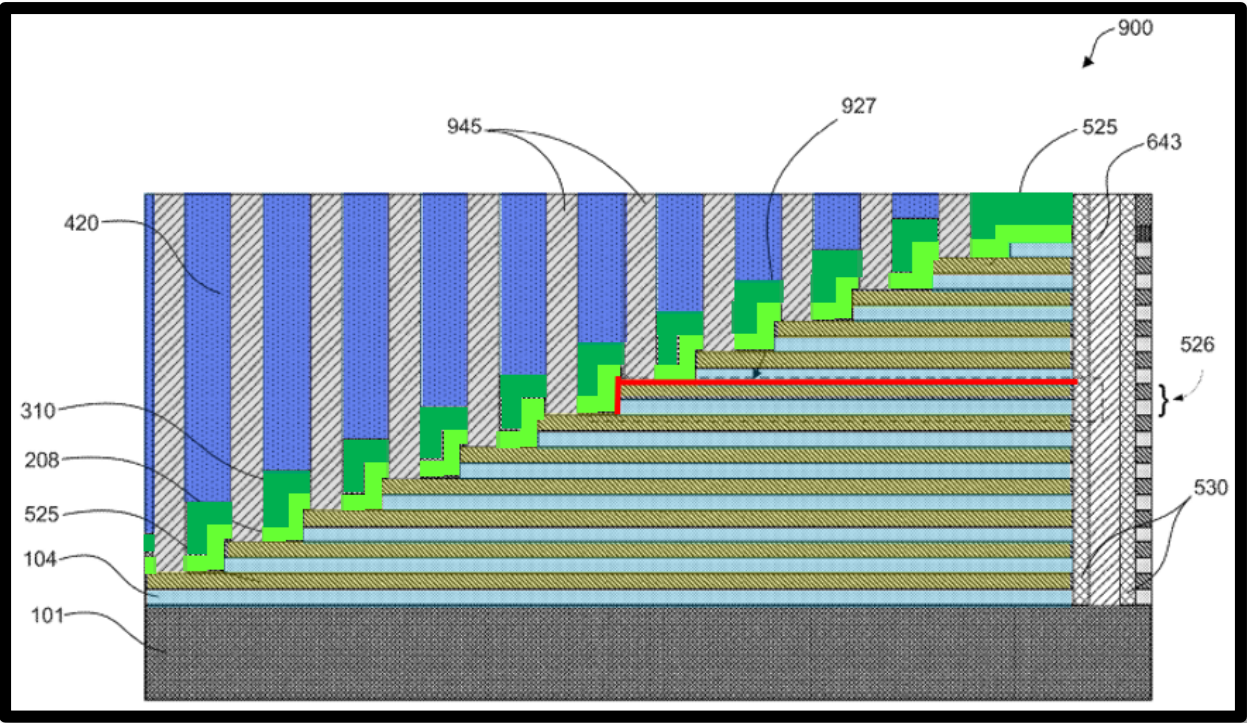
25. Typically, when using a single etching process, the material in the staircase structure in the upper levels is often over-etched (or “punched through”) and lost before VIA openings in the lower levels are fully formed. *Id.* 5:54-58. Manufacturers tried to address the problem by using two or more etching processes that would create holes of similar depth at the same time before creating holes at other depths. *Id.* 5:58-60. But this method creates problems of additional fabrication cost and complexity. *Id.*

26. The '276 patent solves the punch through problem without the drawbacks of separate etching steps for different hole depths. *Id.* 5:61-6:5. The solution includes an “etch stop layer” over the staircase structure, which protects underlying staircase structure layers during the forming of VIA openings and permits the simultaneous etching of all word line holes. *Id.* This improves fabrication yield and reduces cost. *Id.* 6:5-7. A barrier layer can also be introduced

over the staircase structure “for protecting the underlying structure during subsequent etching processes.” *Id.* 7:41-45.

27. The disclosed solution also allows the formation of semiconductor interconnect structures for inter-connecting components at different layers with an uneven topology. *Id.* 6:7-10.

28. Figure 9A, annotated below, is a cross-sectional view of an exemplary '276 patent 3D memory device staircase structure. The staircase structure 900 includes a substrate conductive structure 643 oriented vertically on a substrate 101 and extending through alternating layers of gate stacks 525 (yellow) and first insulating layers 104 (lighter blue). *Id.* 6:11-12, 8:60-61, 10:34-38. A second insulating layer 208 (bright green), which can be a barrier layer, is formed on the staircase structure 900, including on the top and side surfaces of each step. *Id.* 7:36-45. An exemplary step is shown below in red. An etch-stop layer 310 (green) is on the staircase structure 900, including on the second insulating layer 208. *Id.* 7:62-64, 8:5-6. A third insulating layer 420 (dark blue) is on the staircase structure 900. *Id.* 8:26-30. Vertical interconnect access (“VIA”) structures 945 (grey) are formed in VIA openings 840 in the third insulating layer 420. *Id.* 11:17-22.

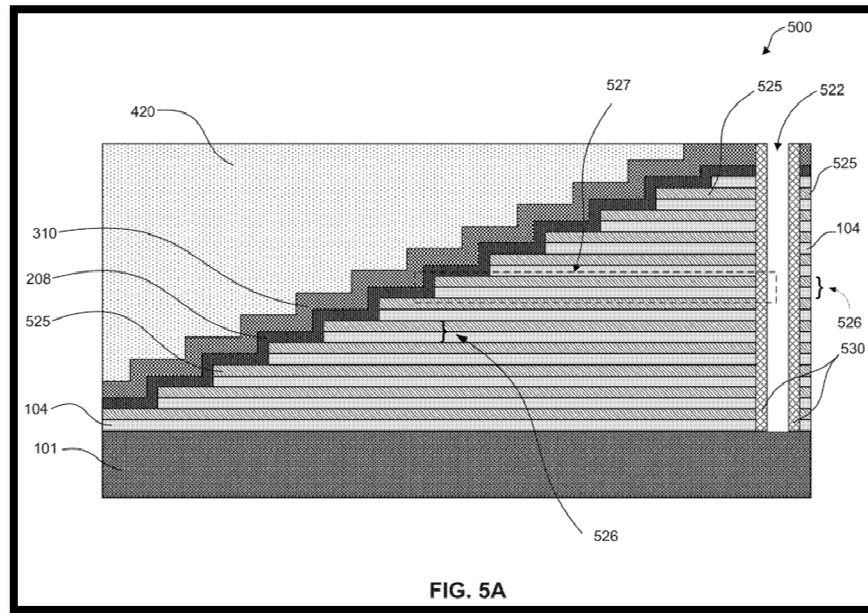


'276 patent, Figure 9A (annotated)

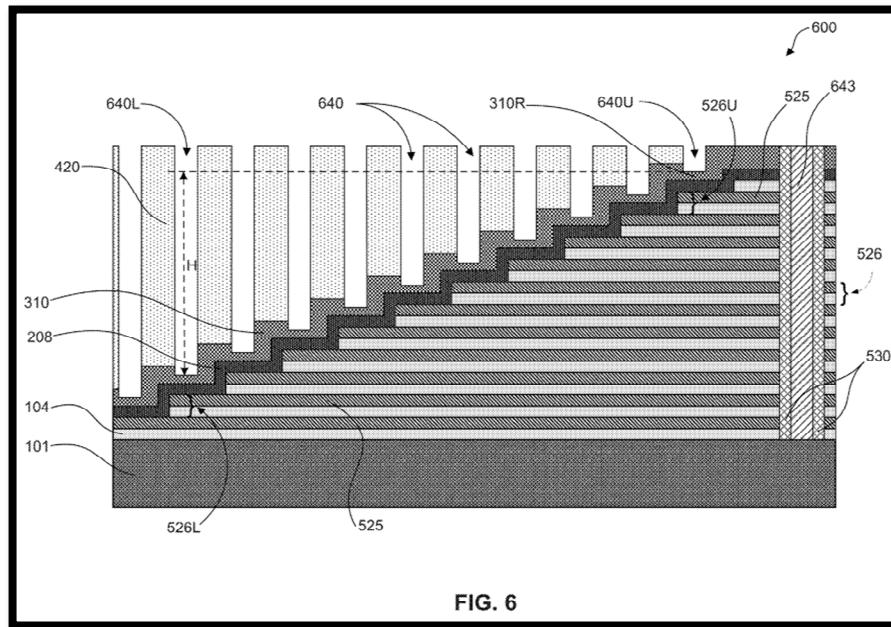
No.	Structure
525	Gate Stack
104	First Insulating Layer
208	Second Insulating Layer
310	Etch-Stop Layer
420	Third Insulating Layer
945	Vertical Interconnect Access Conductive Structures

Key for Annotations of Figure 9A

29. The etch-stop layer 310 protects the underlying layers of the staircase structure 900 in the following way. In an earlier step, the third insulating layer 420 is formed on the staircase structure as shown in Figure 5A, below. *Id.* 8:26-30, Fig. 5A.



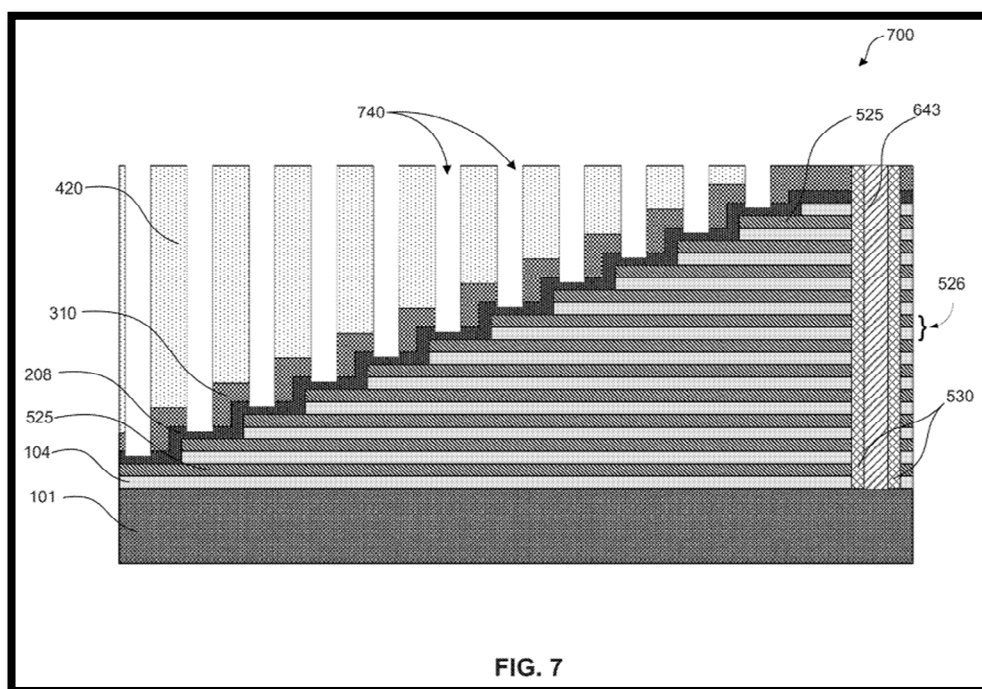
30. Subsequently, as illustrated in Figure 6, below, at least one etching process etches VIA openings 640 exposing portions of the etch-stop layer 310, where the etch-stop layer 310 “protects the underlying structure until all the VIA openings 640 are formed throughout the staircase structure 600.” *Id.* 10:2-5, Fig. 6; *see also id.* 5:65-6:3.



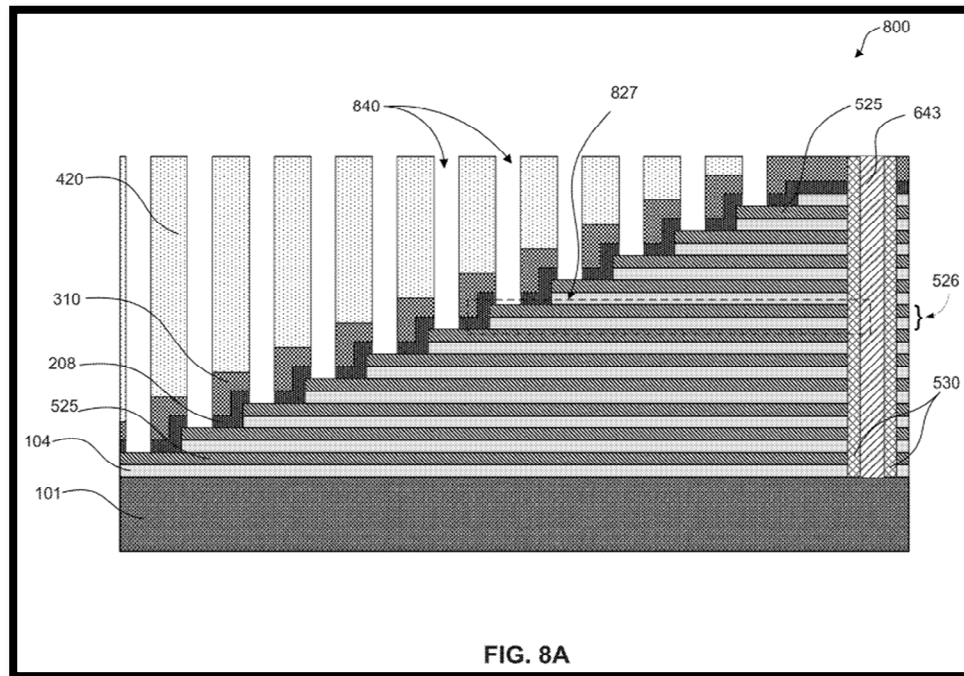
31. As shown in Figure 6, a VIA opening 640L for the lower levels requires a longer etching time than a VIA opening 640U for the upper levels to etch through extra thickness H of the third insulating material 420. *Id.* 10:5-13. Because the portion of “the etch-stop layer 310R on top of the upper replacement SC layer 526U is not etched through” while the VIA opening 640L is being formed, the, “[t]he remaining etch-stop layer 310R provides protection for the replacement SC layers 526U, where the VIA openings 640U are already formed.” *Id.* 10:15-19. Thus, the etch-stop layer 310 protects the upper levels while the VIA openings 640 are formed at the stack lower levels. *Id.* 10:9-13; *see also id.* 10:13-33. That is, a POSITA would have understood that in the claimed method, the VIA openings must be formed to expose portions of the etch-stop layer 310 prior to etching

through (i.e., penetrating) the etch-stop layer 310 exposing the gate stack, as discussed below.

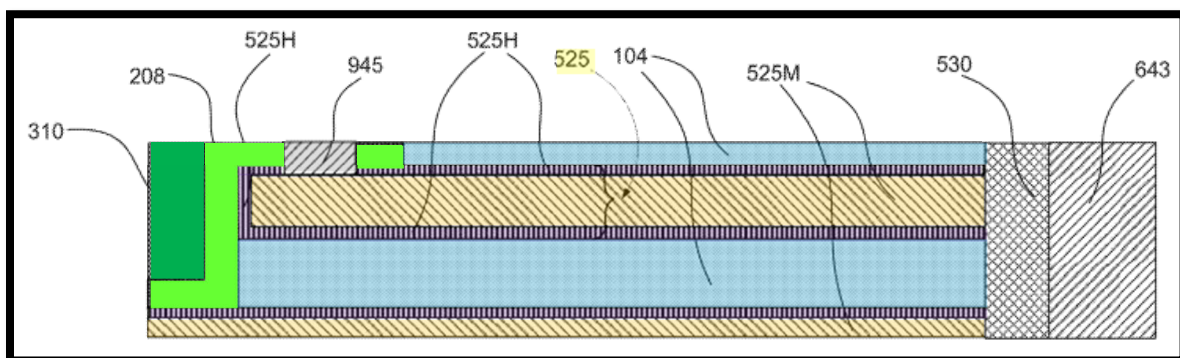
32. Then, as shown in Figures 7 and 8A, below, an etchant etches the etch-stop layer 310 and second insulating layer 208 to expose a gate stack layer 525M of gate stack 525. *Id.* 10:47-11:7, Figs. 7, 8A.¹ This sequence is shown below.



¹ The '276 patent describes that in some embodiments, there is no second insulating layer 208, but only an etch-stop layer 310 disposed on the staircase structure. *See* '276 patent 8:6-9.



33. Figure 9B, annotated below, shows details about the gate stack 525. The gate stack includes a high-k dielectric layer 525H (purple), which surrounds a gate conductive layer 525M (orange) with one side next to fifth insulating layer 530. '276 patent 9:4-10, 9:47-50. The VIA conductive structures 945 (grey) may be directly disposed on an exposed portion of gate conductive layer 525M. *Id.* 11:19-25.



'276 patent, Figure 9B (annotated)

No.	Structure
104	First Insulating Layer
525H	High-k Dielectric Layer
525M	Gate Conductive Layer
208	Second Insulating Layer
310	Etch-Stop Layer
945	Vertical Interconnect Access Conductive Structures

Key for Annotation of Figure 9B

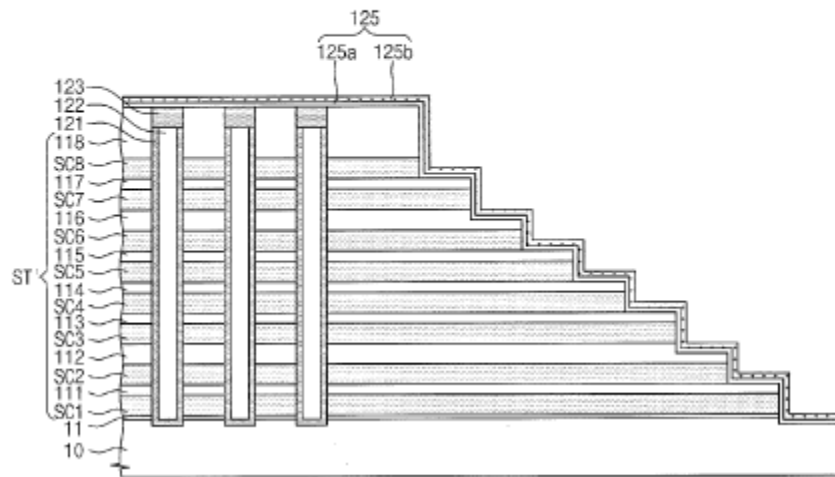
VI. Ground I: Claims 1-2, 4-5, and 9-18 in View of Kim and the Knowledge of a POSITA.

A. Kim does not disclose “each step of the plurality of steps comprises disposing a sacrificial layer over a dielectric layer.”

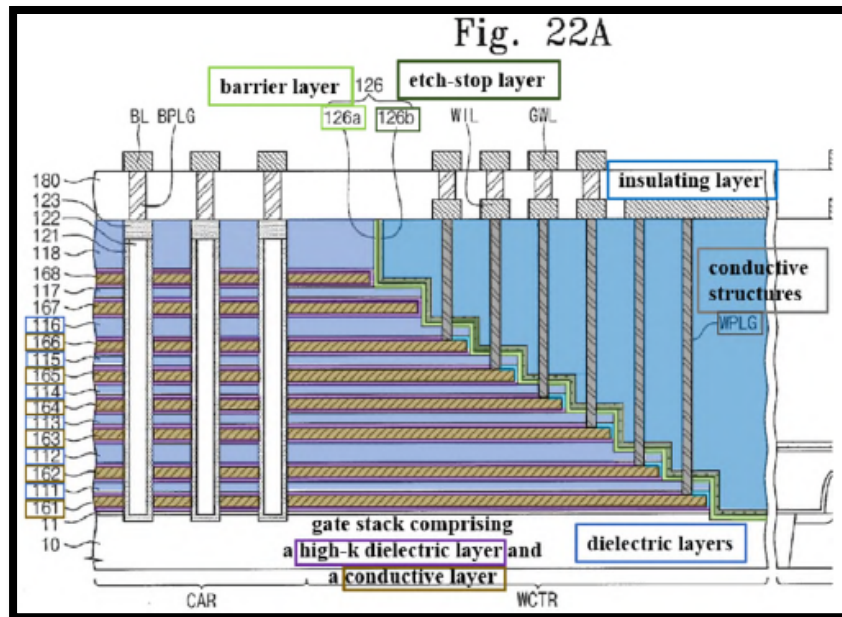
34. Claim 1 is the only independent claim in the '276 patent and recites, in part, “the forming of each step ... comprises disposing a sacrificial layer over a dielectric layer.” '276 patent cl. 1. However, Dr. Banerjee acknowledges that Kim’s “figures show the opposite order” of the claims. Ex.1003 ¶¶70-83; Ex.2020 (“Banerjee Dep.”) 39:5-11; *see also* Ex.1003 ¶70 (“Kim’s figures show embodiments in which a dielectric layer is disposed over a sacrificial layer/gate stack at each step.”). This can be plainly seen in Figures 17A and 22A as examples. In Figures 17A, each step comprises sacrificial layers SC1 to SC8 disposed *below* a dielectric layer 11-118. Sacrificial layers are later replaced with gate stacks, as

seen in Figure 22A (annotated below).² In Figure 22A, a gate stack 161 to 168 (tan) is disposed below a dielectric layer 11-118 (purple).

Fig. 17A

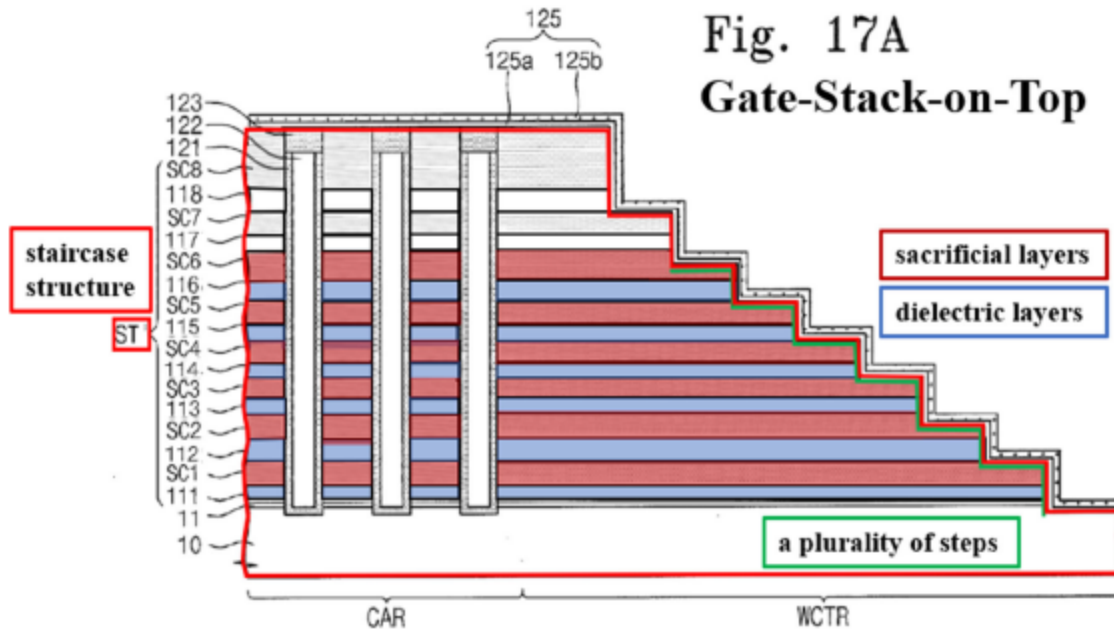


² For the purpose of this declaration, I have accepted for the sake of argument Dr. Banerjee's assertion that the alleged gate stack replaces the sacrificial layer during the gate replacement process. Thus, I have assumed that the location of the gate stack in Figure 22A indicates the location of the sacrificial layer. Ex.1003 ¶82.

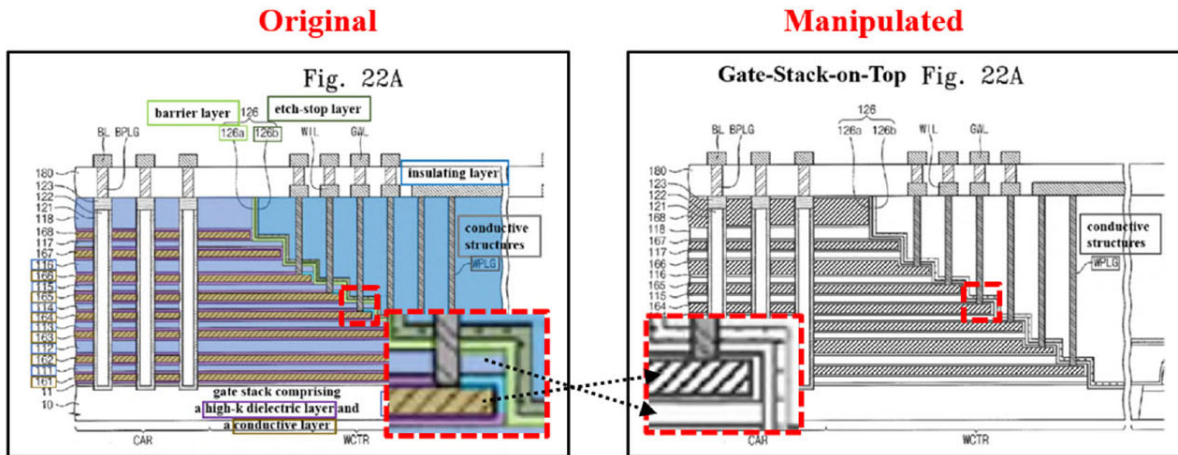


Pet. 27 (annotating Kim (Ex.1005) Fig. 22A)

35. To support his opinions, Dr. Banerjee redraws Kim's Figures 17A, 18A, 19A, 21A, and 22A to show the sacrificial/gate stack layers *over* the dielectric layers, and argues that other embodiments from Kim support inverting the order of these layers. Banerjee Dep. 39:12-15. He labels these as "Gate-Stack-On-Top" figures, as seen in the modified Figure 17A below.

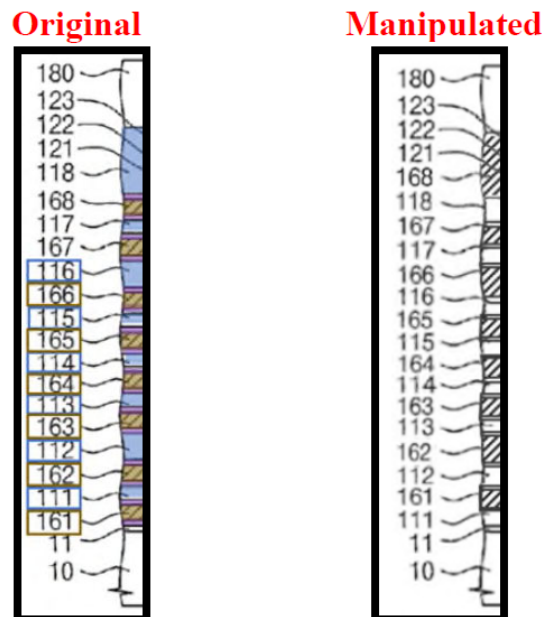


36. These redrawn figures have several modifications, only some of which are identified by Dr. Banerjee. For example, Dr. Banerjee changes the insulating layers of Figure 17A to be sacrificial layers, and vice versa, with corresponding modifications of the gate stacks in later figures. As shown in the side-by-side comparison of the original Figure 22A (annotated) and Dr. Banerjee's modified Figure 22A, Dr. Banerjee also added hatching to the insulating layers of Figure 22A to make them appear as gate stacks, and removed hatching from the gate stacks of Figure 22A to make them appear as insulating layers.



Ex.1003 ¶68 (left), ¶106 (right), both with additional annotation

37. Dr. Banerjee also renumbers labels of Figure 22A, for example to change label “116” (corresponding to an insulating layer) to “166” (corresponding to a gate electrode) and vice versa.



Ex.1003 ¶68 (left) (excerpted), ¶90 (right) (excerpted).

38. Dr. Banerjee does not identify any benefit to inverting Kim's layers or any problem that would be solved by doing so. '711 Banerjee Dep. (Ex.2021) 35:12-36:1 ("Q. [I]n your declaration you don't list any benefits to reversing the order of the layers; right? A. I don't think so. Q. It's a matter of simple choice, but there's no reason you give to go one way or the other; right? A. No, I did not."). The Petition also does not address these issues. *See* Pet. 32-35. In fact, Dr. Banerjee does not articulate any motivation to combine multiple embodiments from Kim to invert the order of the sacrificial/gate stack and dielectric layers.

39. Dr. Banerjee appears to justify combining embodiments in Kim based on Kim stating that "overlapping description of elements previously described with reference to [Figures 5A-14B] may be omitted." Ex.1003 ¶81 (citing Kim [0184]). I disagree that Kim's statement is permitting the kind of mixing and matching of embodiments that Dr. Banerjee believes it does. Even if it did, it still does not articulate any motivation to combine embodiments. The statement is provided in the context of using the same reference numbers for the same elements across embodiments. Specifically, it states that "the same elements as in the embodiments previously described with reference to [Figures 5A-14B] will be denoted by the same references numbers therein, and for concise description, overlapping description of elements previously described with reference to [Figures 5A-14B] may be omitted." Kim [0184]. This statement does not permit the kind of mixing

and matching of elements across embodiments that Dr. Banerjee suggests. Nor does it support the modifications to Kim's figures that Dr. Banerjee engages in.

40. The embodiments Dr. Banerjee seeks to combine differ in material ways such that a POSITA would not have been motivated to combine them. Dr. Banerjee asserts that his declaration "relies on Kim's Figure 17A-22B embodiment comprising an etch-stop layer and a barrier layer." Ex.1003 ¶80; Banerjee Dep. 38:12-17. However, Dr. Banerjee relies on the embodiment in Figures 4, 8A and 8B as purportedly disclosing a gate-stack-on-top arrangement. Ex.1003 ¶70 (citing Kim [0090]-[0091], [0240]). Specifically, Kim's disclosure for these figures states that in some embodiments "each of the top surfaces of the sacrificial layers SC1 to SC8, not the top surfaces of the insulating layers 111 to 118, may be partially exposed in the word line contact region WCTR." Kim [0090]-[0091]. Dr. Banerjee argues this means the sacrificial/gate stack layer is disposed on top of the dielectric layer in this embodiment. Ex.1003 ¶83. Dr. Banerjee then concludes that because this language is absent from the description of the embodiment in Figures 17A-22B it must still apply and was simply omitted as an "overlapping description." *Id.* ¶¶80, 83. I disagree.

41. Notably, the embodiment in Figures 17A-22B does not only exclude the language from Kim paragraphs [0090]-[0091] but actually replaces it with a description demonstrating a gate-stack-on-bottom ordering for the sacrificial/gate

stack and dielectric layers. Kim explains, the etch-stop layer 125a “conformally cover[s] an exposed surface of the stacked layer structure” but covers only “end portions” or “*sidewalls* of the sacrificial layers SC1 to SC8 in the contact region WCTR.” Kim [0185]-[0187]. By explaining that the etch-stop covers only the end portions, or “sidewalls” of the sacrificial layers, Kim demonstrates the sacrificial layer is underneath the dielectric layer within the step such that only the side walls (and not the top surfaces) of the sacrificial layers are exposed. Thus, it is my opinion the embodiment described in paragraphs [0090]-[0091], and also [0240], upon which Dr. Banerjee relies for the gate-stack-on-top disclosure, does not apply to the embodiment in Figures 17A-22B.

42. I also note that the Figures 4, 8A and 8B embodiment Dr. Banerjee seeks to combine with the embodiment in Figures 17A-22B is missing elements disclosed only in Figures 17A-22B, such as an etch-stop layer and a barrier layer. Dr. Banerjee fails to account for these material differences or explain how these elements could be successfully combined into a single embodiment. Attempting such a combination would be complex and costly and a POSITA would not be motivated to do it. For example, it would require redesigning and testing both a new staircase structure and corresponding etch processes for forming openings for conductive vias within each step.

43. Dr. Banerjee bases his opinions on his modified versions of Kim's Figures. Ex.1003 ¶¶90-106. But for the reasons I have described above, it is my opinion that these modified versions are improper and do not accurately reflect Kim's disclosures.

44. Further, Dr. Banerjee's proposed modifications to Kim's device, as seen in Dr. Banerjee's modified figures, creates technical problems that Dr. Banerjee fails to address and that would prevent a POSITA from having a reasonable expectation of successfully combining these references. Further, Dr. Banerjee's proposed modifications to Kim's device, as seen in Dr. Banerjee's modified figures, creates technical problems that Dr. Banerjee fails to address. In my 40 years of experience in developing process flows in industry and academic labs, I have observed that minor alterations in one process step usually changes the outcome of other process steps. This is why leading semiconductor fabricators such as TSMC, rigidly require that transfer of a process flow to another facility must be exactly the same: tools, recipes, step sequence, and even water and air treatment systems. The reversal of the gate stack suggested by Dr. Banerjee would most likely require a POSITA to work with a team of engineers on such a project for at least a year to possibly combine these references. Even if it were successful, the money loss and more importantly, the delays in taking it to market, would prevent the fabricator from being competitive.

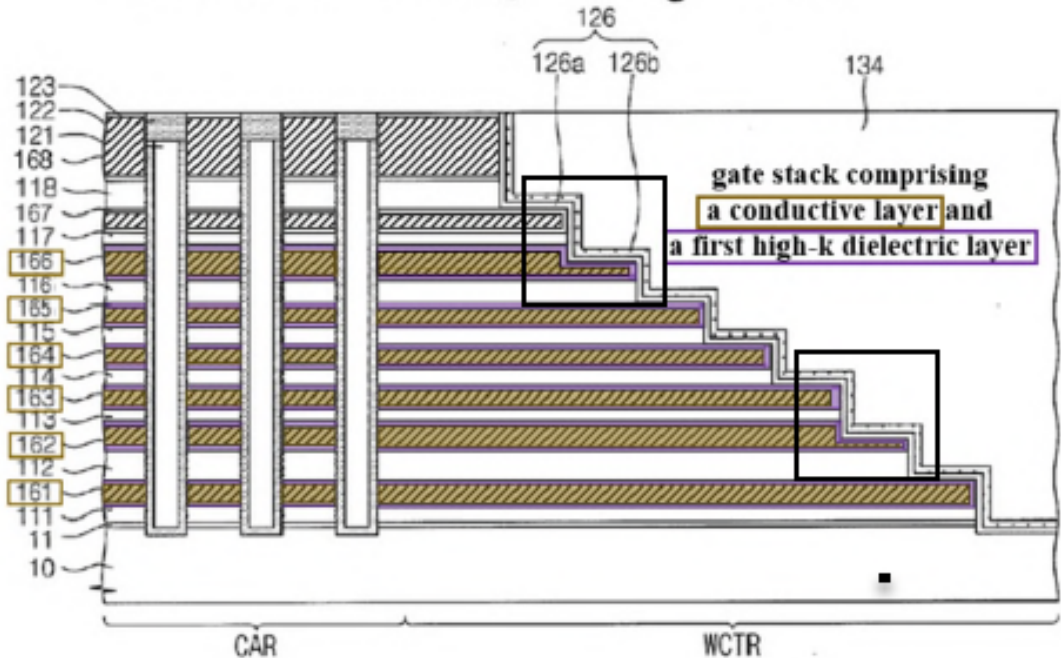
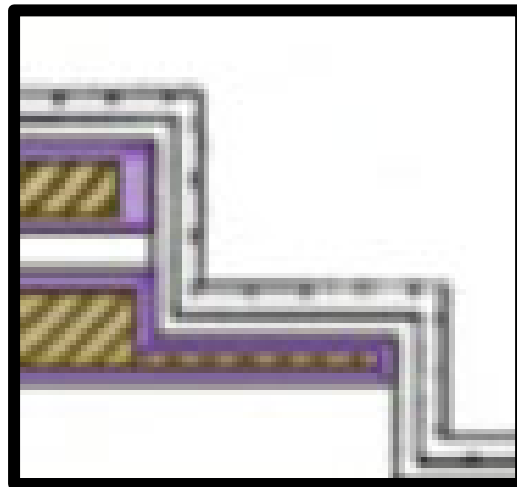
45. For example, first, Dr. Banerjee's modified Figures result in gate stacks being split between two steps, as seen below in conductive layers 162 and 166 of the modified Figure 21A. This results in some steps having *two* gate conductive layers—one on the top and another on the bottom of the step—leaving the neighboring step having a much thinner gate conductive layer than what is needed to safely form a word-line contact region. This modification is problematic for a number of reasons and would strongly counsel a POSITA against combining these embodiments. Any of these problems, individually or collectively, could lead to a defective device. Dr. Banerjee did not address any of these problem in his declaration, but acknowledges in his deposition that they exist: First, the thinner conductive layers on certain steps will be much more susceptible to punch-through during the etching process of the vias, *see* Banerjee Dep. 30:18-31:2 (“[H]ypothetically, if you kept every other parameter constant and you only reduce the thickness, punch-through is more likely to happen.”). Second, thinner conductive layers have higher electrical resistance and can harm performance, *id.* 24:25-25:20 (explaining that “a very thin sacrificial layer would imply a very thin wordline thickness, a high wordline resistance, larger RC time constant, and a

slower chip.”).³ Third, if the sacrificial layers are too thin, the gasses or molecular products left over from the sacrificial etching process are unable to exit or flow out of the cavity, *id.* 26:23-27:1 (“Q. Is one of those problems that the gaseous byproducts of the sacrificial etch process may not be able to full escape? A. That’s certainly a possibility, yes.”). Fourth, if sacrificial layers are made to be too thin, the cavity created from removing the sacrificial material risks collapse before it can be fill with conductive material, *id.* 28:4-9 (Q. If you make the sacrificial layer too thin, and you’re using a dry etch process, is there still a point where the cavity collapse becomes a risk? A. It could. It could. But I think it would be less of an issue than with wet etches.”). Fifth, if the sacrificial layers are too thin, the conductive material will be difficult to deposit into the recesses of the cavity without leaving holes, *id.* 28:19-29:2 (Q. If your cavity that’s left by the sacrificial layer is too thin, is there a risk you can’t completely fill it with conductive material? A. Yes, that’s also a possibility. And if you did not fill it up completely, and you had voids, that would also be catastrophic. It could lead to an open circuit or a very high wordline resistance.”). Sixth, certain steps will have a thin insulator sandwiched between two conductive layers and, because of the high voltage used

³ Dr. Banerjee uses “wordline” as another term for the conductive portion of the gate stack.” Banerjee Dep. 25:21-25.

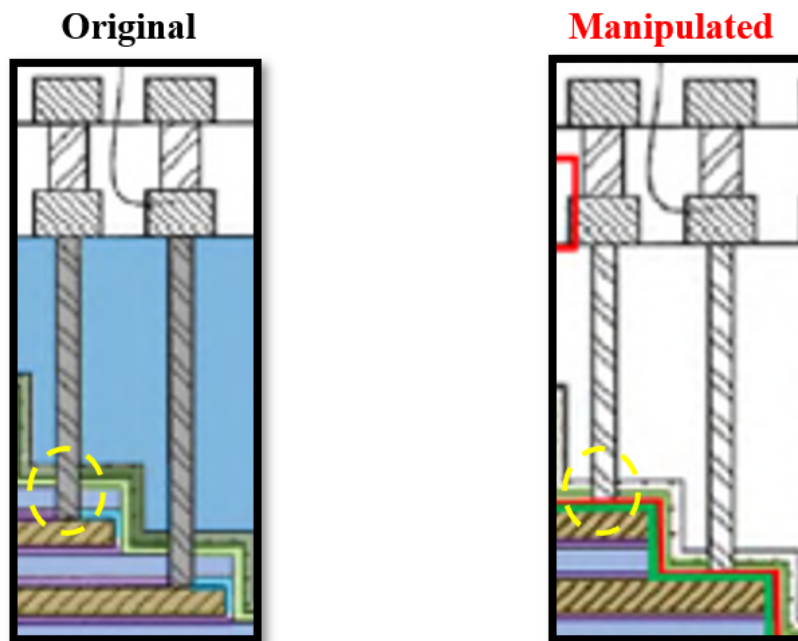
to store data in 3D NAND devices, the high voltage between the two gate stacks can damage the insulator separating the gate stacks and cause leakage.

Gate-Stack-on-Top Fig. 21A



46. Second, Dr. Banerjee's modified Figure 22A not only swaps the layers, but also shortens the contact plugs to terminate within gate electrode layers, as shown below. This is no trivial change to Kim's processes and devices. To

accommodate the shortening of the contact plugs, it would require alteration of the etch steps and processes used to etch the openings for the word-line contacts. As I discuss below, these etch processes are very complex and are sensitive to even small adjustments. The switching may also change the etch selectivity between the insulating layer above the sacrificial layers SC1-8 and sacrificial layers themselves such that the first stop layer 126a or the second stop layer 126b is not needed—just like in the Alternative Figures 4-15D embodiment. A POSITA would not use the stop pattern 126 if its function is not needed because a POSITA would not want to add the time or material to include a non-functional component.



47. For these reasons, it is also my opinion that a POSITA would not have a reasonable expectation of successfully combining these embodiments of Kim.

3D NAND technology is extremely complex, and inverting the order of layers in a device is not a simple change. As described further below, the proposed combination would require material changes to the design and manufacturing process.

1. 3D NAND is complex technology.

48. A POSITA would understand that 3D NAND technology, including manufacturing relevant components, is not particularly straightforward. Instead, a POSITA would understand that 3D NAND is described as “**very complex**” and including “complex device structures.” Ex.2022 293; Ex.2023 3; Ex.2022 212 (“3D NAND architectures need to be proved cost effective in terms of process costs and product yield because the process complexity is not trivial if compared to 2D NAND.”); Ex.2023 4 (“[T]he overall complexity and capital intensity of 3D NAND manufacturing add significantly to the challenges fabs are facing in terms of process control, yield, and economics.”); *see also* Ex.2024 5 (“With each generation, the fabrication of 3D NAND becomes more complex.”).

49. In my opinion, a POSITA would also understand that manufacturing 3D NAND “involves a number of new and **complex process steps**.” Ex.2025 4; Ex.2023 4-5 (recognizing “[a]n incredible level of precision and repetition is required in defining complex 3D structures with extremely high aspect ratio (HAR) features,” including “alternating film deposition” and formation of “staircase,”

“wordline,” “contact,” and “channel” features), Fig. 1; Ex.2026 1 (“3D NAND has led to complex deposition and etch with angstrom-level precision requirements.”); Ex.2028 8, 31 (describing removal of nitride layers and forming a wordline as a “complex process”); *see also id.* 3 (“[M]aking 3D NAND is a complex process” that requires “using a deposition tool” to deposit layers of material on a substrate); *id.* 2 (“The big challenge is to characterize the inner portions of a 3D NAND device, which consists of complex materials, multiple layers and tiny channel holes.”); Ex.2029 5 (“3D NAND is a complex technology”); *id.* 6 (“In all cases, the 3D NAND process flow is complex.”).

2. Re-ordering sacrificial and insulating layers is a complex process.

50. Specifically, Dr. Banerjee’s extensive modifications to Figure 22A show that the proposed modification—replacing a functional gate stack with insulating material and vice versa, including altering corresponding depths of word line contacts—would require extensive modifications to the device’s structure and manufacturing process, including etch processes, none of which are simple or straightforward. For example, etch processes depend on multiple parameters that are optimized to achieve desired etch characteristics for a specific design. When the design changes, these parameters must be reoptimized. These parameters include at least etch chemistry, or the composition of gases used in the etchant, plasma power, bias voltage, chamber pressure, temperature, and etch time.

Ex.2021 37:9-41:8; 61:21-64:10. Even small changes in these parameters can have significant effects. “[S]pecifics matter” and “details matter,” as Dr. Banerjee has repeatedly affirmed in deposition. *See id.* 40:20-22, 41:5-8, 45:12, 46:18, 57:2-3, 61:18-19.

51. Changes in design can also affect the number and sequence of steps in the etching processes. Further, etch processes are highly dependent on the materials used, the depth and aspect ratio of the desired etch, the material to be deposited on the sidewalls, the material on which the etch is stopped, the material used as the mask which can be simple photoresist or a hard mask using other materials such as carbon, and the order of the layers. Thus, drawing a figure that moves structures around gives the illusion of simplicity. The reality of such changes is extremely complicated, as I explained previously.

52. The complexity of this technology can be further illustrated by mistakes Dr. Banerjee appears to make in attempting to modify Kim’s Figure 22A. As I mentioned, changes to the order of layering necessarily implicates other, cascading changes to the design and manufacture. For example, Dr. Banerjee also modified the depth of the word-line contacts in Figure 22A, which in turn would have required even further changes to etch parameters described above. *See, e.g.*, Banerjee Dep. 36:9-41:7. Kim’s Figure 22A additionally includes a lower gate insulating layer 11. *See, e.g.*, Kim [0061], [0064], [0071], [0142]. The purpose of

this layer is to prevent “electrical crosstalk” between the lowermost gate and the substrate 10. *See* Ex.2021 30:21-31:22. When Dr. Banerjee altered the order of layers in Figure 22A, he replaced the lower gate electrode 161 with an insulating layer 111, such that an insulating layer was in contact with the substrate 10 rather than a gate electrode. *See* Ex.1003 ¶90, Modified Figure 22A. This makes lower gate insulating layer 11 unnecessary because, unlike a gate electrode, an insulating layer such as 111 does not need to be insulated from the substrate 10. Dr. Banerjee failed to modify the placement of the lower gate insulating layer 11 to account for this change.

53. Thus, Dr. Banerjee’s proposed combination requires significant modifications to both the processes for forming word line contacts to penetrate through different materials at different depths, as well as structural changes that themselves create other issues that could counsel a POSITA against make such a modification to Kim’s design. For these reasons, Dr. Banerjee’s position that a POSITA would have a reasonable expectation of success because “either order was compatible with common deposition techniques” and deals only with two layers is inconsequential. *Id.* ¶84. The reality is that a POSITA, with two to three years of experience, would inevitably run into processing problems, such as the ones that we have enumerated here. In my opinion, after long experience in semiconductor processing, I can say that even a processing expert with decades of experience and

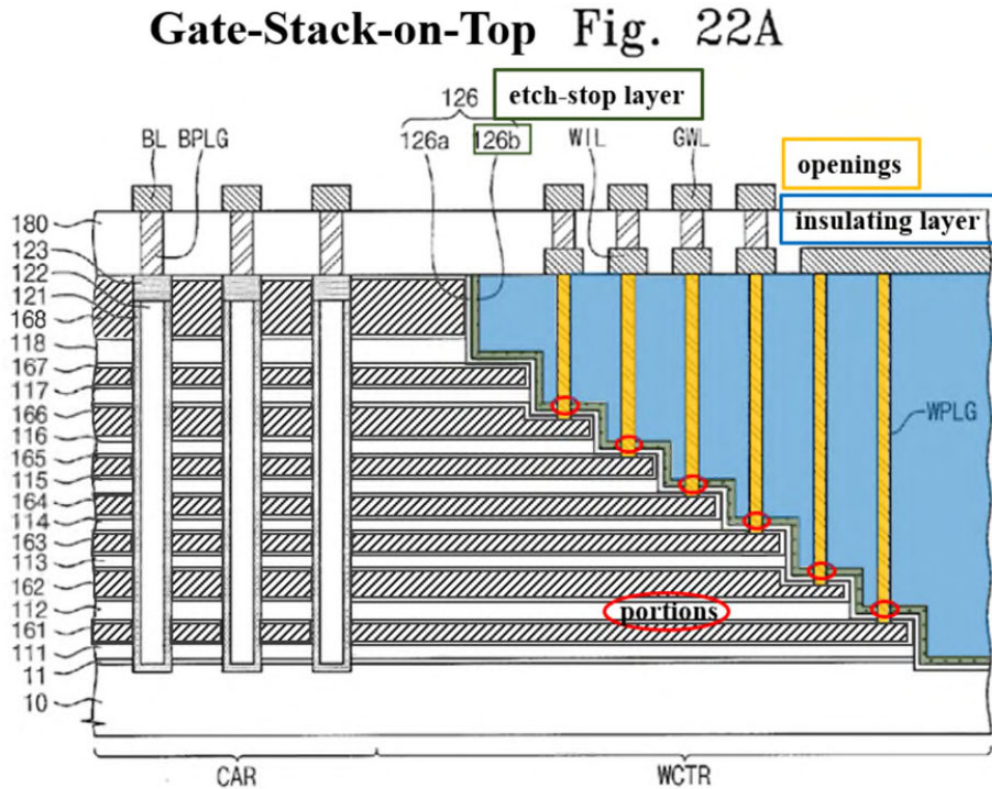
backed up with a team of experienced staff in processing, device physics, device reliability, process simulation, and chemical and TEM characterization would require many months of process runs and many millions of dollars to reacquire the yield seen before the modifications.

B. Kim does not disclose “forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer” of claim 1.

54. Dr. Banerjee asserts that “Kim discloses” this limitation. Ex.1003 ¶102. Dr. Banerjee cites to Kim’s disclosure of forming of openings for word line contact plugs WPLG as disclosing this limitation, and asserts that forming these openings requires a two-step process including a first step where the contact holes “penetrate the insulating layer exposing—but not penetrating—portions of the etch-stop layer.” *Id.* ¶¶102-103. I disagree.

55. Kim discloses only openings that penetrate through its etch-stop layer without first forming a plurality of openings exposing portions of the etch-stop layer. And in particular, Kim does not disclose a step in forming the word line contact plugs WPLG where “portions of the etch-stop layer” are exposed by forming the claimed openings, but not penetrating through the etch-stop layer. Kim discloses only connecting the “word line contact plugs WPLG ... to the gate electrodes,” where the openings penetrate Kim’s etch-stop layer. Dr. Banerjee’s annotation of Kim’s Figure 22A shows that Kim’s openings *do* penetrate through

the etch-stop layer rather than exposing a portion of it as shown by the red circles below. In other words, Kim's Figure 22A does not disclose anything about how the contact holes are formed.



Ex.1003 ¶102 (annotating Kim Fig. 22A)

56. Dr. Banerjee cites paragraph 173 of Kim, but that paragraph does not mention two steps for formation of these contact holes, where the openings in the insulating layers are formed prior to exposing the underlying gate electrodes (e.g., 166), but rather just discloses forming these contact holes. Kim [0173] (“[F]ormation of word line contact plugs WPLG ... may include forming contact holes to penetrate the interlayer insulating pattern 134 in the word line contact

region WCTR.”); *see* Ex.1003 ¶102. As a result of this formation, the holes *penetrate*, rather than merely expose, the etch-stop layer so that “the word line contact plugs WPLG can be connected to the gate electrodes” which are below the etch stop layer. Kim [0173].

57. Dr. Banerjee asserts that “[a] POSITA would have recognized” the need for an extra step in contact hole formation due to Kim’s disclosure that the etch stop layer “may be formed of a material having an etch selectivity with respect to the interlayer dielectric 130.” Ex.1003 ¶103 (quoting Kim [0213]). I disagree. A POSITA would have understood from this passage that Kim explicitly discloses when a two-step etching process was intended. Specifically, “etch selectivity” in this passage relates to two-step device planarizing in the cell-array region—not formation of contact holes. Kim [0213] (“[T]he interlayer dielectric 130 may be formed on the etch stop layer 125 and then planarized until a top surface of the etch stop layer 125 is exposed on the cell array region CAR.”).

58. A POSITA would not have understood Kim as disclosing the etch selectivity between the interlayer dielectric 130 and the etch-stop layer 125 for planarization discloses a process for forming contact holes where the etch stop layer is exposed but not penetrated through. A POSITA would not have understood Kim’s planarization process to be used for forming contact holes. Kim’s planarization process discussed above uses chemical mechanical polishing

(“CMP”) to create a flat, polished surface, not contact holes. *Id.* [0191]. As Dr. Banerjee correctly admitted, CMP **cannot** form contact holes. Banerjee Depo. 47:6-8 (“Q: Can chemical-mechanical polishing be used to etch contact holes? A: No.”).

59. Indeed, paragraph 213 in Kim refers to the interlayer dielectric 130, which is shown in Figure 18A (prior to planarization), not the interlayer insulating pattern 134 in Figures 20A or 22A (after planarization). *See* Kim [0191]-[0193] (“The interlayer insulating pattern 134 may be formed to expose the top surface of the etch stop layer 125.”). The result of the planarization process produces a “insulating pattern 134 having a flat top surface,” not any contact holes. *Id.* [0193].

60. Moreover, the etch selectivity between two materials for planarization, including CMP, does not disclose an etch selectivity for etch processes for forming contact holes. CMP processes have specific recipes, where the etch rate (and therefore the etch selectivity between materials) is affected by slurry, a slurry type including the acid or base solution, buffer chemicals, and the size and composition of the particles, the type, mechanical shape, and properties of a polishing pad, the speed and pressure a polishing pad applies to the surface of the material, and the material itself. *Id.* [0104] (“A removal rate of the interlayer dielectric 130 in the planarization process may be affected by various factors, such as a slurry type, a configuration of the polishing pad, a structure and type of a

polishing head, a rotating speed of the polishing pad relative to the substrate 10, a pressure applied by the polishing pad to the substrate 10, and a material and shape of the interlayer dielectric 130.”), [0132], [0141] (referring to “etch recipe[s] having an etch selectivity”). For the same reason, a POSITA would not have understood Kim’s disclosure of the “removal rate ... during the planarization” of a polishing stop layer (or etch stop layer) to disclose an etch selectivity for purposes of forming a contact hole. *Id.* [0190]. Thus, for the same materials, an etch selectivity for a CMP planarization process is not the etch selectivity for forming contact holes with an entirely different etching process for forming contact holes, most commonly dry or wet etch processes. I agree with Dr. Banerjee that comparing the etching processes for forming contact holes, CMP processing for planarization, and the etch selectivities for materials in those processes is like “comparing apples to oranges.” Banerjee Dep. 50:2-8.

61. A POSITA therefore would not have understood this extra step to be implicit or inherent in Kim.

C. Kim in view of a POSITA’s knowledge does not render obvious “etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer” of claim 4.

62. Dependent claim 4 claims “[t]he method of claim 1, wherein etching the exposed portions of the etch-stop layer comprises etching the exposed portions

of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer of each step.” Kim does not disclose this limitation. Further, achieving the claimed etch relationships are highly dependent upon the specific materials used. Further, 3D NAND technology and development of proper etch processes to achieve the claimed etch relationships is highly complex and not simple or unusually straightforward for the reasons I described previously in Section VI.A.

63. For example, etch processes depend on multiple parameters that are optimized to achieve desired etch characteristics for a specific design. These parameters include at least etch chemistry, or the composition of gases used in the etchant, noble gasses such as Helium, Argon, and Xenon, plasma power, bias voltage, chamber pressure, temperature, and etch time. Even small changes in these parameters can have significant effects. *See* Ex.2021 40:20-22, 41:5-8, 45:12, 46:18, 57:2-3, 61:18-19 (testifying that “details matter” and “specifics matter”). Further, changes in design, such as the modifications proposed by Dr Banerjee, can also affect the number and sequence of steps in the etching processes. In addition, etch processes are highly dependent on the materials used, the depth and aspect ratio of the desired etch, the material to be deposited on the sidewalls, the material on which the etch is stopped, the material used as the mask which can be simple photoresist or a hard mask using other materials such as carbon, and the order of the layers.

D. Kim does not disclose “etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the first high-k dielectric layer” of claim 5.

1. Petitioner fails to establish a motivation to combine Kim in view of a POSITA’s knowledge to render claim 5 obvious, or a reasonable expectation of successfully doing so.

64. Dependent claim 5 claims “[t]he method of claim 4, wherein etching the exposed portions of the etch-stop layer further comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the first high-k dielectric layer.” Kim does not disclose this limitation. And achieving the claimed etch relationships are highly dependent upon the specific materials used. Further, development of proper etch processes to achieve the claimed etch relationships is highly complex and not a simple or unusually straightforward for the reasons I described previously in Section VI.A.

65. Kim discloses two etch-stop layers to protect underlying structures during the etch-stop process. Yet Dr. Banerjee opines that a POSITA would have still “found it desirable to further protect the gate electrode layer” and that “the first high-k dielectric layer may be advantageously used as an etch stop” to provide this added protection. Ex.1003 ¶110. Dr. Banerjee then opines that to achieve this added protection “only the claimed relative etching rates have a sensible relationship.” *Id.* I disagree with Dr. Banerjee for multiple reasons.

66. Kim already protects against punch-through by using two etch-stop layers that can themselves be selective to one another. Kim [0186]-[0187]. A POSITA would not be motivated to add a third effective etch-stop layer in the manner Dr. Banerjee suggests—namely, by adapting the etch-rate relationship of claim 5 to the first high-k dielectric—because it would unnecessarily complicate the manufacturing process by requiring an additional etching step and etch chemistry.

67. Further, Dr. Banerjee is incorrect that the claimed relationship is obvious because “only the claimed relative etching rates have a sensible relationship.” Ex.1003 ¶110. In the event that a POSITA wanted additional protection, a POSITA may be motivated instead to make the etch-stop and first high-k dielectric layers out of the same material, ensuring they have *the same etch-rate* to effectively increase the thickness of the etch-stop layer. A POSITA may find this to be more advantageous than the claimed arrangement because it would simplify the manufacturing process by decreasing the etch-steps and chemistries needed.

68. Finally, while the first high-k dielectric may be used for etch-stop protection, it also serves the purpose to protect the surrounding oxide layer during deposition of the conductive gate layer. This can be accomplished whether or not the relative etch-rates match the claimed arrangement.

E. Kim does not disclose “forming the ... conductive structures further comprises planarizing the conductive materials and the insulating layer” of claim 11.

69. Petitioner fails to establish a motivation to combine Kim in view of a POSITA's knowledge to render claim 11 obvious, or a reasonable expectation of successfully doing so. Dependent claim 11 claims “[t]he method of claim 1, wherein forming the plurality of conductive structures further comprises planarizing the conductive materials and the insulating layer.” Kim discloses planarization *before* the conductive structures are formed, *see* Kim [0119], [0206], and well after they are formed and with respect to a different surface, [0176] (planarizing an upper insulating layer that covers the global word line, GWL in Figure 22A). However, Kim does not disclose “planarizing the conductive materials” as disclosed in claim 11.

70. Moreover, chemical mechanical polishing is not a simple or a straightforward technology. There are numerous factors a POSITA must consider with any CMP process, meaning a POSITA cannot indiscriminately adapt one planarization process to another, as Dr. Banerjee suggests by pointing to Kim's “planarizing the top surfaces of other components” as justification for why Kim discloses planarization in relation to the claimed application. Ex.1003 ¶116. While planarizing conductive materials using CMP is widely used in the CMOS industry, the necessary factors a POSITA must consider vary widely across different

materials and applications. For example, for each CMP process, a POSITA must select the appropriate reactive chemicals, the particle composition and size, the downward force, the relative sliding velocity, how to condition the pad in real time, and how to determine the proper end point. A POSITA may also need to consider what material the process is planarizing down to, how it will react to the slurry, whether the mechanical process will leave scratches, and whether the adhesion between the metal and the layer beneath it is large enough to prevent damage to the patterned structures. All of these considerations are complicated even further if the conductive layer material being used is less common.

VII. Ground II: Claims 1, 3, 6-8 over Kim in View of Fang.

A. Fang does not disclose “each step ... comprises disposing a sacrificial layer over a dielectric layer” of claim 1.

71. Like Kim, Fang does not disclose a gate-stack-on-top ordering, or in other words Fang does not disclose “each step ... comprises disposing a sacrificial layer over a dielectric layer.”

B. There is no motivation to combine Kim in view of Fang or a reasonable expectation of successfully doing so.

72. Dr. Banerjee asserts that a POSITA would be motivated to combine Fang’s (Ex.1006), disclosures related to the etch-stop layer and contact-hole etching on Kim’s word-line structure and would have had a reasonable expectation of success in doing so. Ex.1003 ¶145. Dr. Banerjee provides several reasons in support of his opinion, including Fang’s etch-stop material alternatives, purported

similarities between Fang's and Kim's etch-stop disclosures, and Kim's and Fang's use of conventional deposition methods and anisotropic dry etching. *Id.* Dr. Banerjee also points to other reasons such as the focus of the references, tunneling concerns, and other purported similarities. *Id.* ¶¶145-153. I disagree that any of these reasons, individually or collectively, would motivate a POSITA to combine these references or do so with any reasonable expectation of success. Dr. Banerjee ignores fundamental differences between Kim and Fang described below that undermine his stated reasons and would counsel a POSITA *against* their combination.

1. A POSITA would not have been motivated to combine Fang's etch-stop characteristics and contact-hole etching to Kim.

a. **Kim and Fang are directed towards solving different problems.**

73. First, a POSITA would not be motivated to combine Fang with the Kim reference because they are directed toward solving different problems. Dr. Banerjee claims that Fang's focus on "preventing over-etching shallower openings" when etching openings for the word-line conductive structures "dovetails" with Kim's focus to "reduce or prevent damage to the device during manufacturing." Ex.1003 ¶146. I disagree. Fang and Kim are directed towards solving different problems. Specifically, Kim is directed to preventing damage from CMP planarization, while Fang is directed to preventing punch through

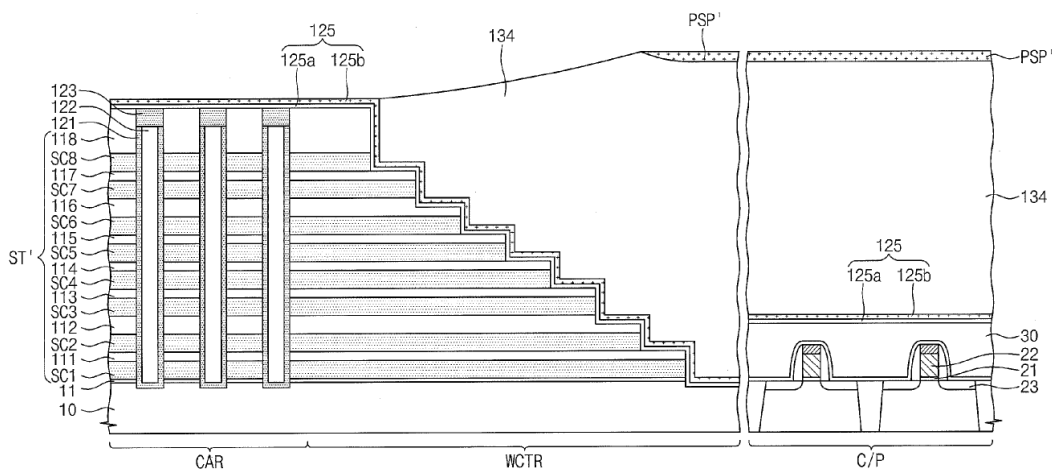
damage during the etching process. Thus, these references are directed towards a different type of damage resulting from different processes in different areas of the device.

74. As seen in Figure 19A below, Kim's device is separated into three distinct regions: a cell array region (CAR), a word line contact region (WCTR), and a peripheral circuit region (C/P). Kim [0036]. Kim is directed to solving the problem of "dishing" that can occur on the interlayer dielectric in the upper areas of the peripheral circuit (C/P) and word-line contact regions (WCTR) during CMP planarization. *Id.* [0025]-[0026], [0104]-[0105], [0190]-[0197]. Dishing is the creation of a recess in the interlayer dielectric over the WCTR and C/P regions. It happens because the contact pads of the cell array region may have a different removal rate from the interlayer dielectric. Ex.2030 306. Thus, the interlayer dielectric on the WCTR and C/P regions "may be etched faster than the contact pads 123 of the cell array region CAR." Kim [0105]. Kim also focuses on reducing or preventing damage to the contact pads 123 in the CAR region that can also occur from the CMP process. *Id.* [0027], [0105], [0190]-[0197]. Kim discloses addressing these problems by forming a "polishing stop layer PSL"⁴ over the

⁴ The portion of the polishing stop layer PSL that remains after planarizing is referred to as the "polishing stop pattern PSP." *See* Kim [0196]-[0197].

interlayer dielectric and “etch stop layer 125” over the contact pads 123. Because of their etch selectivity, these can reduce or prevent damage to the contact pads 123 in the CAR region and the dishing phenomenon elsewhere. Kim [0027], [0105], [0190]-[0197]. Kim is not directed to the general idea of reducing or preventing damage to the device during manufacturing. Rather, it is specifically targeted to preventing CMP damage on the top of the device, and specifically to the contact pads in the CAR region and interlayer dielectric in the WCTR and C/P regions. Based on this focus, a POSITA would not expect Kim to disclose information such as specific etch-stop layer thicknesses.

Fig. 19A



75. Fang addresses a different problem resulting from the etching process on the staircase steps. Fang discloses a purported solution to over-etching of shallow openings for word-line conductive structures, also referred to as “punch-

through,” which occurs in the lower part of the WCTR region where the etch-stop layer meets the underlying structures of the staircase steps. Fang proposes preventing this punch through using a single-etch stop layer. That layer is formed directly on the insulating and conductive layers of the staircase structure to prevent “punch though” into the conductive material while the word-line conductive structures are being etched. Thus, Fang is describing a different solution to a different problem than what is described in Kim, because the damage Fang seeks to prevent occurs in a different region of the device and from a different source. Therefore, a POSITA would not be motivated to combine Fang and Kim on this basis.

b. **Fang is directed towards carbon-doped silicon nitride, which Kim does not use.**

76. Second, the etch-stop materials and characteristics used in Kim and Fang are significantly different and would counsel a POSITA against their combination. Fang is directed towards carbon-doped silicon nitride. *See* Fang Title, Abstract, [0020], [0022], cls. 1-27 (all claims specifically recite carbon-doped silicon nitride). While Fang discloses a single mention of an “alternative[]” etch-stop material of “a high-k dielectric material, such as hafnium oxide,” the specification and claims are still *directed towards* carbon-doped silicon nitride. *See id.* [0022]. Kim does not use or disclose carbon-doped silicon nitride. *See* Kim [0186], [0187]. Nor does it disclose hafnium oxide etch-stop. *Id.* This matters

significantly because different materials respond dramatically differently to etching, and etch-stop characteristics are not fungible across different materials. Different materials require different etch chemistries, or combinations of gases, needed to effectively etch the material. The etch chemistry used will affect the rate at which different materials etch. Etch rate can also be impacted by the specific etchant used, along with the flux and energy of the impinging ions, with different materials reacting differently to different etchants and bombardment. These specifics may impact design decisions and etch-stop layer characteristics, such as altering the requisite thickness of the etch-stop layer, among other things. For example, a POSITA would not be motivated to use Fang's carbon-doped silicon nitride etch-stop layer thicknesses or other characteristics in Kim where Kim never uses that same material. Nor would a POSITA be motivated to apply Fang's etch-stop thicknesses to Kim simply because Kim does not disclose any, as Dr. Banerjee suggests, much less have a reasonable expectation of successfully doing so. *See* Ex.1003 ¶146.

77. Relatedly, etch-stop layer characteristics, including thicknesses, are also specific to the combination of etch-stop material and sacrificial layer material. Fang's sacrificial layer is silicon nitride. *See* Fang [0019]-[0022] (identifying *only* silicon nitride as the "nitride material 120" and carbon-doped silicon nitride as the primary "etch stop material 130"); *see also e.g., id.* [0015], [0019], [0025], cls. 21-

22. Thus, Fang's etch-stop characteristics are specific to the combination of a carbon-doped silicon nitride etch-stop layer and a silicon nitride sacrificial layer. Kim discloses an undoped silicon nitride sacrificial layer, but does not disclose a carbon-doped silicon nitride etch-stop layer. This means Kim does not use the combination of etch-stop and sacrificial layer materials that Fang's etch-stop thickness is designed for. Kim also uses a second etch-stop layer, and the thickness of one etch-stop layer may impact the thickness of the other etch-stop layer. I also note that Kim's etch-stop layer 125a can protect etch-stop layer 125b during removal of the sacrificial layer. Kim also uses a high-k dielectric surrounding the conductive layer of each step for added protection, which Fang does not use, and which could further impact etch processes, etch rates, etch chemistries, and etch-stop layer thicknesses.

78. Dr. Banerjee opines that a POSITA would have been motivated to use Fang's "alternative" etch-stop material of high-k dielectric such as hafnium oxide to reduce potential tunneling effects. Dr. Banerjee relies on the tunneling shortcoming in the Chen reference for this motivation. Chen is not part of the Ground II combination. Further, Kim does not identify tunneling as a problem in its design, as discussed below, so a POSITA would not be motivated to use Fang's alternative etch-stop material for this purpose.

79. Dr. Banerjee repeatedly states, incorrectly, that both Kim and Fang disclose “silicon nitride” as a suitable etch-stop material. *See, e.g.*, Ex.1003 ¶¶141, 145. To be clear, “carbon-doped silicon nitride” is materially different than undoped “silicon nitride.” Kim discloses silicon nitride as an etch-stop material, but Fang actually *prohibits* the use of silicon nitride as an etch stop material. Specifically, Fang explains that the etch stop may be made of “any material that is not substantially removed (e.g., etched) during removal and replacement of the nitride materials 120 of the staircase structure,” where “the nitride material 120 is silicon nitride (SiN).” Fang [0019]-[0020]. Because the sacrificial layer is silicon nitride, a silicon nitride etch stop layer would be removed at the same rate as the silicon nitride sacrificial layer. In contrast, carbon-doped silicon nitride has a high level of etch selectivity with silicon nitride and does not raise the same problem.

80. Because Fang’s etch-stop layer characteristics, including thicknesses, are specific to carbon-doped silicon nitride, and Kim does not use carbon-doped silicon nitride, a POSITA would not be motivated to use Fang’s etch-stop characteristics in Kim’s structure.

c. **Structural differences between Kim and Fang counsel a POSITA against applying Fang’s etch-stop layer characteristics and methods to Kim.**

81. Beyond those differences in purpose and material, Kim and Fang also have significant structural differences. A POSITA would know that an etch-stop

layer is included to protect underlying structures during the etching process. *See* Ex.2021 48:20-49:8 (“[I]n general, the more different materials that you have that the etch has to go through, in general, that provides additional safety margins.”). Thus, differences in the underlying structure, such as the number and type of protective layers used would be important to determining the necessary etching processes and etch-stop layer design. This may include etch process such as forming vias for the conductive structures, and etch-stop layer design such as thicknesses and other characteristics, among other things.

82. Kim and Fang have three important structural differences. First, as mentioned previously, Kim discloses the use of a high-k dielectric layer surrounding the conductive layer of each step while Fang does not. *See, e.g.*, Kim [0148], [0151], Fig. 22A. This high-k dielectric layer provides additional protection to the conductive layer during the etching of the vias and can affect the necessary etch stop layer characteristics and design, such as thickness, material, and number of protective layers. Second, Kim also discloses the use of two etch-stop layers while Fang discloses only one. Kim’s high-k dielectric and two etch-stop layers would provide additional protection compared to Fang’s single layer. Further, the use of multiple etch-stop layers would require a different etch process than Fang’s single layer design. Dr. Banerjee argues that Kim does not “teach or suggest that the thickness ... of the etch-stop layer would be impacted by the

number of etch-stop layers,” and so “argu[ing] against the combination because Kim discloses an additional barrier layer ... would be wrong.” Ex.1003 ¶153. I disagree. The number of etch-stop layers may impact many etch-stop layer characteristics, such as the necessary thickness of the layers and the materials used. Dr. Banerjee admits this, including that thickness is the “main parameter” to control etch times in single layer designs compared to multi-layered designs where etch selectivity can be used. Banerjee Dep. 17:13-18:13; *see also* Ex.2021 49:5-8. Finally, Petitioner’s modifications Kim, such as inverting the gate stack and dielectric layers, and other resulting changes, would also impact manufacturing and etch-processes required. I discuss some of these above in Section VI.A.2. Fang’s etch-stop layer is designed for a device without any of these features. Thus, a POSITA would not be motivated to combine Fang and Kim for these additional reasons, or have a reasonable expectation of successfully doing so.

2. There is no motivation to combine the Kim and Fang references to render independent claim 1 obvious.

83. Claim 1 of the '276 patent claims “disposing an etch-stop layer on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer.” There is no motivation to combine Kim and Fang to render this limitation of claim 1 obvious for the same reasons I described above in Section VII.B.1.

84. Further, I disagree with Dr. Banerjee's opinion that a POSITA would have been motivated to use Fang's "alternative" etch-stop material of high-k dielectric such as hafnium oxide in Kim. Kim does not disclose any concern with the tunneling problems described in Chen that would motivate a POSITA to adapt Fang's etch-stop characteristics to Kim on that basis. Further, Dr. Banerjee is wrong that a POSITA would have a reasonable expectation of success doing so based on hafnium oxide being "already known" as an alternative to a silicon nitride etch-stop layer. Ex.1003 ¶148.

85. First, Kim does not disclose any concern with tunneling problems. Nor would a POSITA expect Kim to do so. Figures 17-22 of Kim disclose a two-layer etch-stop embodiment. Chen discloses that a two-layer etch-stop reduces tunneling compared to a single etch-stop layer. Specifically, Figure 8C of Chen shows that a two-layer design using "silicon oxide as the first stop layer 210 and silicon nitride as the second stop layer 220" has a larger tunneling length than Figure 8A's "single-layer silicon nitride etching stop layer." Chen (Ex.1008) [0048], [0050]. Notably, Kim discloses its etch-stop layers also have a first silicon oxide layer and a second silicon nitride layer, like the example in Chen, and does not describe any issues with tunneling current. Kim [0187] ("In some embodiments, the first stop layer 125a may be formed of silicon oxide and the second stop layer 125b may be formed of silicon nitride."). A POSITA reading

Chen in view of Kim would therefore be dissuaded in view of Chen to modify Kim's etch-stop layers as Petitioner argues. Pet. 71. Thus, Kim would not be motivated to adapt Fang's alternative single hafnium oxide etch stop layer to resolve tunneling concerns.

86. Second, Fang does *not* disclose hafnium oxide as an alternative to a silicon nitride etch-stop material, as Dr. Banerjee suggests. Dr. Banerjee's opinion that hafnium oxide was "already known" as an alternative to silicon nitride based on Fang's disclosure appears to stem from a basic misunderstanding of Fang. Fang includes a single mention of hafnium oxide as an alternative its *carbon-doped* silicon nitride etch stop material and not to undoped silicon nitride, such as the silicon nitride used in Kim. Further, neither reference provides guidance regarding etch processes, parameters, or other design considerations related to using hafnium oxide as an etch-stop with Kim's materials or device. The Petitioner suggests a POSITA would have a reasonable expectation of success because both devices disclose an etch-stop layer that is selective with the interlayer dielectric above it. *Id.* That is simply a description of how an etch-stop layer functions, and I disagree this would provide a POSITA with any reasonable expectation of success. Fang and Kim are not similar devices when it comes to etch-stop characteristics and processes. Thus, a POSITA would not have a motivation or reasonable expectation

of success in adapting Fang's alternative hafnium oxide etch-stop material to Kim's silicon nitride etch-stop layer based on Fang's teaching.

87. Finally, I note that Chen is not part of the Ground 2 obviousness combination.

3. There is no motivation to combine Kim and Fang to render claim 6 obvious.

88. Claim 6 claims "[t]he method of claim 1, wherein disposing the etch-stop layer comprises disposing hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, and/or any combination thereof." There is no motivation to combine Kim and Fang to render this limitation of claim 1 obvious for the same reasons I described above in Sections VII.B.1-2.

89. Dr. Banerjee asserts that "Fang discloses that the etch-stop layer may comprise silicon nitride," and that "[l]ike Fang, Kim discloses silicon nitride as a material for the etch-stop layer." Ex.1003 ¶139. He then states that "A POSITA would have understood [silicon nitride] to meet Fang's criterion of not removing the etch-stop material when removing the sacrificial layer nitride materials." *Id.* Again, Dr. Banerjee is wrong and, as discussed previously, appears to mistake Fang's disclosure of carbon-doped silicon nitride for silicon nitride. Fang *does not* disclose an undoped silicon nitride etch-stop material, and specifically prohibits it by requiring that the etch-stop material "not [be] substantially removed (e.g., etched) during removal and replacement of the nitride materials." Fang [0020].

Fang's "nitride material" is disclosed as silicon nitride, meaning a silicon nitride etch-stop material would in fact be "substantially removed" during removal and replacement of the sacrificial nitride materials.

90. Further, Dr. Banerjee's opinion that a POSITA would be motivated to use Fang's hafnium oxide as an alternative to Kim's silicon nitride etch-stop appears to be based on the same misunderstanding that Fang is using hafnium oxide as an alternative to a silicon nitride etch stop. *But Fang is not.* Fang references hafnium oxide as an alternative to *carbon-doped silicon nitride*, which has significantly different etch properties than silicon nitride. *See id.* [0025] ("Since both [materials] are silicon nitride-based, it was surprising that the [carbon-doped silicon nitride] etch stop material 130 is not removed by ... conventional etch chemistries used to remove nitride materials.").

VIII. Ground III: Petitioner Failed to Demonstrate Han in View of Fang Renders Obvious Claims 1-15.

A. There is no motivation to combine Han in view of Fang or a reasonable expectation of successfully doing so.

91. Han fails to disclose multiple claimed elements, such as an etch-stop layer disposed on the staircase steps, an insulator disposed on the etch-stop layer, and contact hole etching details for these layers. Dr. Banerjee argues that a POSITA would have been motivated to "adapt Han's staircase structure by adding Fang's etch-stop layer based on Fang's teaching." Ex.1003 ¶¶215-218. I disagree

for multiple reasons, and it is my opinion that Fang's etch-stop layer would be unnecessary and redundant in Han's design. Dr. Banerjee ignores significant difference of Fang's device compared to Han's structural design and manufacturing methods. These differences outweigh the motivations Dr. Banerjee puts forth, such as those related to structural design, purported challenges, and well-known manufacturing methods. A POSITA would not have been motivated to combine these references or have had a reasonable expectation of successfully doing so.

92. First, Han discloses a gate stack with multiple high-k dielectric layers covering the inner surface of the gate regions and surrounding the conductive layers within each step. Han [0141]. These high-k dielectric layers protect both during the deposition of the conductive layer and during etching the contact holes by acting as an etch-stop to protect the conductive layer, as Dr. Banerjee has repeatedly confirmed. Ex.1003 ¶110 (“[T]he high-k dielectric layer may be advantageously used as an etch stop to protect the conductive layer.”); Banerjee Dep. 32:23-33:12:57:10-23. For example, the high-k dielectric layer is a different material than the insulating layer above it, and by using a material with a lower etch-rate for the high-k dielectric material, it can provide the protective etch-stop function. This protective function of Han can be heightened even further by utilizing its multiple high-k dielectric layers as multiple etch-stops, and having

each act as an etch-stop for the layer above. Further, a POSITA may also adjust the thickness of the protective high-k dielectric layers as needed to provide additional protection to the conductive layer during etching. Banerjee Dep. 16:21-17:8 (“[A] thicker etch-stop layer will provide more of an insurance policy, if you will.”). Fang does not use any high-k dielectric layers surrounding the conductive layers of each step and thus requires a etch-stop layer to provide protection from punch through. Thus, Han’s gate stacks are very different from Fang’s, and require different manufacturing and design steps that Fang does not use.

93. Second, as described further below, Han’s design delineates upper and lower contact holes of the staircase structure, providing for forming the contact holes at different times. This reduces the risk of punch-through in the upper holes by not continuing to etch them while waiting for the lower, deeper holes to finish etching. Further, this staged etching approach provides protection against punch-through while providing significant benefits. For example, this approach avoids added cost and complexity by using a single etch chemistry and not having to deposit an additional layer on the structure, requiring another etch process and chemistry during manufacturing. Still, Han discloses that its contact holes can still be formed using “[a]t least one patterning process,” which includes a single process. Ex.1007 (“Han”) [0156]. Where utilizing Han’s methods already

adequately protected against punch-through, a POSITA would not have been motivated to add an additional layer to the device.

94. Third, Han and Fang have different staircase orderings and compositions. Han discloses a gate-stack-on-top model while Fang uses a gate-stack-on-bottom model. Such structural differences necessitate different manufacturing processes and design considerations, all of which Petitioner ignores. For example, moving layers in that manner requires changes to etch processes, etch chemistries, and contact hole depths. This can be seen in Fang, where the word line contacts must penetrate a full dielectric layer to reach the stack, but Han's design does not include this processing step because the gate stack is on top. These and other proposed adaptations are not trivial modifications and add additional complexities to an already complicated process. I discuss this in detail previously. *See, e.g.,* Section VI.A.2.

95. For at least these reasons a POSITA would not be motivated to combine the Han and Fang references. Nor would a POSITA have a reasonable expectation of successfully doing so for these reasons. For example, the fact that Han's and Fang's staircase structures may have "similar materials" does nothing to increase a reasonable expectation of success because it does nothing to resolve the changes to etch parameters, chemistries, and manufacturing process that would result from adding Fang's additional etch-stop to Han. *See* Ex.1003 ¶163.

96. Dr. Banerjee's primary motivation to combine the Han and Fang references is to protect against punch-through or over-etching. Han already employs at least two methods that would protect against the risk of punch through such that a POSITA would not be motivated to adapt Fang's etch-stop layer to Han, especially given that an additional etch-stop layer adds unnecessary cost and complexity to Han's manufacturing and design. Dr. Banerjee does not identify anywhere Han indicates it is concerned with or suffers from punch through. Adding Fang's etch-stop would be redundant and undesirable.

97. Dr. Banerjee also projects shortcomings identified in Fang on Han, suggesting that Han would have "suffered from the 'shortcomings of the conventional solutions to over etching.'" For example, Dr. Banerjee cites to Fang's disclosure of "multiple masks" in the prior art as one such "conventional solution" to punch-through that requires "additional processing acts, complexity, and cost to the overall process." Ex.1003 ¶215 (quoting Fang [0004]). Dr. Banerjee then asserts that "[a] POSITA would have recognized Han's method suffered from this exact problem." *Id.* I disagree. Dr. Banerjee relies only on purported shortcomings described in Fang and ignores the fundamental differences described above. For example, Han's design differs from Fang's by using multiple high-k dielectric layers surrounding its conductive layer. Dr. Banerjee fails to support his opinion

with Han's own disclosures and fails to show how Han still suffers from the punch-through problems described in Fang given the differences discussed above. *Id.*

B. Han in view of Fang does not disclose “etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer of each step” of claim 4.

98. Claim 4 claims “[t]he method of claim 1, wherein etching the exposed portions of the etch-stop layer comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer of each step.” Han in view of Fang does not disclose this limitation. Further, achieving the claimed etch relationships are highly dependent upon the specific materials used. Further, 3D NAND technology and development of proper etch processes to achieve the claimed etch relationships is highly complex and not a simple or unusually straightforward for the reasons I described previously in Section VI.A.

99. Further I note that Han is a gate-stack-on-top structure, unlike Fang which is a gate-stack-on-bottom structure. This means Fang has an additional dielectric insulating layer separating its etch-stop layer from the gate stack.

C. Han in view of Fang does not disclose “etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the first high-k dielectric layer” of claim 5.

100. Dependent claim 5 claims “[t]he method of claim 4, wherein etching the exposed portions of the etch-stop layer further comprises etching the exposed

portions of the etch-stop layer at a higher etching rate than an etching rate of the first high-k dielectric layer.” Han in view of Fang does not disclose this limitation. And achieving the claimed etch relationships are highly dependent upon the specific materials used. Further, 3D NAND technology and development of proper etch processes to achieve the claimed etch relationships is highly complex and not a simple or unusually straightforward for the reasons I described previously in Section VI.A.

101. This proposed combination also fails for the reasons I described above in Sections VI.C and VIII.A. In particular, where these sections discuss Han’s use of multiple high-k dielectric layers surrounding conductive layers, whether Han requires additional protection during contact hold etching, and whether the claimed relationship here is the “only ... sensible relationship” between the etch-stop and first high-k dielectric layers, which it is not. In addition, a POSITA would not have a reasonable expectation of successfully achieving the combination where neither Han nor Fang are designed to include *both* an etch-stop layer over the staircase steps *and* a high-k dielectric layer surrounding the conductive layers.

102. Neither Han nor Fang disclose this limitation and Dr. Banerjee’s opinion rests on a background reference showing that aluminum oxide has a higher etching rate than hafnium oxide relative to argon plasma etchant. Ex.1003 ¶189. But the reference Dr. Banerjee relies upon is *not* relevant to the technology at issue

here. A POSITA would not use a simple argon plasma for almost any complex silicon technology. Argon is an inert gas that does not react chemically. As such, it only provides a physical bombardment. Physical bombardment has very little selectivity, and selectivity is needed to processes such as those discussed here. Further, Fang is directed towards carbon-doped silicon nitride etch-stop material, and this reference makes no mention of how carbon-doped silicon nitride would react compared to any other relevant materials at issue in Han.

103. Further, Dr. Banerjee cites back to his related opinion in Ground 1. *Id.* To the extent Dr. Banerjee relies on the same rationale there, that “only the claimed relative etching rates have a sensible relationship,” that opinion fails for the same reason I described previously. *See* Section VI.D. A POSITA may be motivated to make the etch-stop and first high-k dielectric layers out of the same material, ensuring they have *the same etch-rate* to effectively increase the thickness of the etch-stop layer. A POSITA may find this to be more advantageous than the claimed arrangement because it would simplify the manufacturing process by decreasing the etch-steps and chemistries needed. Moreover, this arrangement would still be consistent with the purpose of a high-k dielectric layer to protect surrounding oxide layers during deposition of the conductive layer material.

IX. Ground IV: Claims 17 and 18 over Han in View of Fang and Chen.

104. Claim 17 claims “prior to disposing the etch-stop layer, disposing a barrier layer on each step of the plurality of steps, wherein the barrier layer protects underlying structures during the etching of the exposed portions of the etch-stop layer.” ’276 patent cl. 17.

A. There is no motivation to combine the Han, Fang, and Chen references to render claim 17 obvious.

105. As stated previously in Ground 3, a POSITA would not be motivated to combine the Han and Fang references. For many of those same reasons, and for the additional reasons stated below, a POSITA would not be motivated to combine the three references, and specifically Chen’s barrier layer, to the Han and Fang combination. Specifically, significant structural and manufacturing differences would counsel a POSITA against the combination.

106. Similar to the way Fang’s etch-stop layer adds redundancy to Han’s high-k dielectric layer and staged etching process, and does so at the expense of a simpler manufacturing process and design, adding Chen’s barrier layer to either Han or Fang or both does the same. As I explained previously, Han already employs two methods that would protect against short circuits resulting from punch through. Fang as well employs an etch-stop layer to accomplish the same purpose.

107. Further, Petitioner cites Chen’s Figure. 8B to argue adding Chen’s “single aluminum-oxide high-k-dielectric etch-stop layer can have a tunneling

length L2 shown in Figure 8B,” and adding another barrier layer can increase the tunneling length further. Pet. 106 (citing Chen [0048]). But Han already has at least a single, and potentially a second, high-k dielectric layer that a POSITA would have understood provides the tunneling length benefits described in Chen, for example, aluminum oxide. Han [0141]. According to Chen, aluminum oxide has a “energy gap ... larger than 6 eV,” which “provide[s] a relatively large tunneling length” that Chen says is preferred. Chen [0049]. And when combined with Fang’s etch-stop layer (which a POSITA would not do), the combination would have a third stop layer with similar “energy gap” larger than “6 eV,” which Chen discloses is preferable. *Id.* [0053]. Fang’s carbon-doped silicon nitride has an energy gap of 6.5 eV, and Chen mentions silicon nitride is an acceptable second stop layer (i.e., Fang’s etch-stop layer in Petitioner’s combination). Fang [0020]. Chen teaches that when a first and second stop layer both have energy gaps “larger than 6eV,” then the device provides the preferable tunneling length properties. Chen [0053]. In other words, the Han/Fang combination, as asserted in the Petition, already provides the tunneling length benefits disclosed in Chen. So a POSITA would not be motivated to modify that combination. Thus, adding Chen’s barrier layer only exacerbates the redundancy and complexity of the manufacturing and design by adding even further materials, etch steps, and required etch-chemistries. A POSITA would have recognized that forming contact holes through multiple layers

is one of the more complex processes in 3D NAND manufacturing. The more layers that are added, the more time consuming, expensive, and more difficult it is to reliably form the contact holes.

108. Specifically, a POSITA viewing the punch-through protections of Han alone, and certainly with the additional etch-stop layer disclosed in Fang, would not have been motivated to add Chen's first stop layer 210 to the Han/Fang combination because of processing difficulties and the potential for defects. For example, Chen discloses the first stop layer 210 may be made of silicon zirconium oxide (ZrSiO_2) and silicon hafnium oxide (HfSiO_2). *Id.* [0041]. Forming layers of those materials are slow, expensive, and would leave in the contact hole Zr and Hf residue that could leave to defects.

109. Additionally, regardless of the material used, as described above, adding an additional barrier layer to the Han/Fang combination would require a different etch process than Fang's single layer design. Dr. Banerjee incorrect in suggesting that the choice between a one- or two-stop layer is merely a binary choice. Ex.1003 ¶226. Dr. Banerjee again understates the choice a POSITA would have to make when designing a 3D NAND device. Providing protection for the underlying structures during etching is not as simple as choosing the number of layers. As already discussed, the use of multiple etch-stop layers would require a different etch process than Fang's single layer design. As Dr. Banerjee admitted,

adding layers of different materials requires changing etch chemistry. Ex.2021 43:5-48:1. To choose between a single and double etch-stop structure requires modifying existing etch processes and adding an additional process. As described above regarding Petitioner's proposed modification of Kim, etch processes depend on multiple parameters that are optimized to achieve desired etch characteristics for a specific design. *See* Section VI.A.2. When the design changes, these parameters must be reoptimized. These parameters include at least etch chemistry, or the composition of gases used in the etchant, plasma power, bias voltage, chamber pressure, temperature, and etch time. Even small changes in these parameters can have significant effects. "[S]pecifics matter" and "details matter," as Dr. Banerjee has repeatedly affirmed in deposition. *See* Ex.2020 40:20-22, 41:5-8, 45:12, 46:18, 57:2-3, 61:18-19.

X. CONCLUSION

All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. Further, I am aware that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001. I declare under penalty of perjury that the foregoing is true and correct.

Executed on October 27, 2025, in Arden Hills, Minnesota.

Stephen Campbell

Stephen Campbell