

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00228
U.S. Patent No. 11,101,276

PETITIONER'S REPLY BRIEF

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LISTING OF EXHIBITS

EXHIBIT NO.	DESCRIPTION
1001	U.S. Patent No. 11,101,276 to Zhu et al. (“the ’276 patent”)
1002	File History of U.S. Patent No. 11,101,276 (“the ’276 FH”)
1003	Declaration of Dr. Sanjay Banerjee (“Banerjee”)
1004	<i>Curriculum Vitae</i> of Dr. Sanjay Banerjee
1005	U.S. Patent Publication No. 2012/0070944A1 (“Kim”)
1006	U.S. Patent Publication No. 2019/0067306A1 (“Fang”)
1007	U.S. Patent Publication No. 2017/0062470A1 (“Han”)
1008	U.S. Patent Publication No. 2017/0294384A1 (“Chen”)
1009	U.S. Patent Publication No. 2018/0330985A1 (“Yu”)
1010	Aritome, “NAND Flash Memory Technologies” (2016)
1011	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
1012	Micheloni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)
1013	U.S. Patent Publication No. 2017/0117222A1 to Kim et al.
1014	Chang and Sze, “ULSI Technology” (1996)
1015	Orlowski et al., <i>Si, SiGe, Ge, and III-V Semiconductor Nanomembranes and Nanowires Enabled by SiGe Epitaxy</i> , ECS Transactions Vo. 33, No. 6 (2010), 777-89
1016	U.S. Patent No. 9,728,547 (“Ohsaki”)
1017	U.S. Patent Publication No. 2017/0148677A1 (“Shin”)
1018	U.S. Patent No. 10,672,711 to Zhu et al. (“the ’711 patent”)

EXHIBIT NO.	DESCRIPTION
1019	Excerpt from YMTC’s Exemplary Infringement Claim Chart for U.S. Patent No. 11,101,276 (Ex. H-1 to Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024) (“YMTC2 Infringement Contentions, Ex. H-1”) [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]
1020	Korean Patent Publication No. KR10-2013-0015120 (“Lee”) with machine translation
1021	Wolf S., et al., “Silicon Processing for the VLSI Era, Volume 1 – Process Technology, Chapter 15, Multilevel Interconnects for ULSI” (2nd Ed. 2000)
1022	CN Patent Publication No. 107658309 A with certified translation (Priority application to the ’276 patent)
1023	Wang, et al., “Low DC-Bias Silicon Nitride Anisotropic Etching,” Journal of Vacuum Science & Technology B, Vol. 33, Issue 6 (Sept. 10, 2015)
1024	U.S. Patent Publication No. 2014/0284661A1 (“Williams”)
1025	Shamiryan D., et al., “Selective Removal of High-K Gate Dielectrics,” Chemical Engineering Communications (2009)
1026	Morel, et al., “Tungsten metal gate etching in Cl ₂ /O ₂ inductively coupled high density plasmas,” Journal of Vacuum Science and Technology B (Nov. 3, 2008)
1027	Kim, et al., “Dry Etching of High-k Dielectric Thin Films in HBr/Ar Plasma,” Journal of the Korean Physical Society, Vol. 54, No. 2, pp. 934-38 (February 2009)
1028	U.S. Patent No. 10,297,543 to Park et al.

EXHIBIT NO.	DESCRIPTION
1029	Minute Order (case schedule), Dkt. No. 141, dated September 18, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1030	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1031	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, LTD.’s Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1032	Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:24-cv-04223-RFL which has been consolidated with Case No. 3:23-cv-05792-RFL
1033	Declaration of Jared Bobrow in Support of Petitioner’s Motion for Admission Pro Hac Vice
1034	Alex He, <i>Case Study: From Paper Tiger to Real Tiger? The Development of China’s Semiconductor Industry</i> , CENTRE FOR INT’L GOVERNANCE INNOVATION 14 (2021)
1035	State-Owned Assets Supervision and Administration Commission of the State Council (SASAC), <i>Definition of “State-Owned Enterprise”</i> (July 4, 2019) (https://www.sasac.gov.cn/n2588040/n2590387/n9854212/c11647665/content.html) (“SASAC Definition”)
1036	Certified English Translation of Ex. 1035 (SASAC Definition)

EXHIBIT NO.	DESCRIPTION
1037	China's State Council, <i>Notice of the State Council on Issuing "Made in China 2025"</i> (May 19, 2015) (https://www.gov.cn/zhengce/content/2015-05/19/content_9784.htm) ("Made in China 2025")
1038	Certified English Translation of Ex. 1037 (Made in China 2025)
1039	Karen M. Sutter, Cong. Rsch. Serv., R46767, <i>China's New Semiconductor Policies: Issues for Congress</i> (2021)
1040	Liu Yuanchun et al., <i>Accelerating the Realization of High-Level Scientific and Technological Self-Reliance</i> , PEOPLE (July 15, 2024) (http://paper.people.com.cn/zgjzk/html/2024-07/15/nw.zgjzk_20240715_1-05.htm) ("People's Paper Article")
1041	Certified English Translation of Ex. 1040 (People's Paper Article)
1042	YMTC, <i>Yangtze Memory Technologies Co. Ltd. Officially Established</i> (Aug. 1, 2016) (https://www.ymtc.com/cn/news/28.html) ("YMTC Press Release")
1043	Certified English Translation of Ex. 1042 (YMTC Press Release)
1044	Testimony of Stephen Ezell (VP, Global Innovation Policy – Information Technology & Innovation Foundation) Before the U.S.-China Economic and Security Review Commission (Apr. 14, 2022)
1045	Yahoo! Finance, South China Morning Post, Tech War: China's Top Memory Chip Maker YMTC Gets US\$7 Billion From State-Backed Investors (Mar. 2, 2023) ("Yahoo! Article")
1046	Baidu, <i>Yangtze Memory Increases Capital and Expands Capacity to RMB 100 Billion, Big Fund Phase II Forms a Partnership with Local Hubei State-owned Assets</i> (Mar. 2, 2023) (https://baijiahao.baidu.com/s?id=1759256650733024656&wfr=spider&for=pc) ("Baidu Article")
1047	Certified English Translation of Ex. 1046 (Baidu Article)

EXHIBIT NO.	DESCRIPTION
1048	YMTC's Rule 7.1 Corporate Disclosure Statement, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , Case No. 5:23-cv-05792-VKD (N.D. Cal. Nov. 9, 2023)
1049	Lianhe Credit Rating Co., Ltd., Wuhan Optics Valley Financial Holding Group Co., Ltd., 2024 Tracking Rating Report (Jun. 28, 2024) ("2024 Tracking Rating Report")
1050	Certified English Translation of Ex. 1049 (2024 Tracking Rating Report)
1051	State-Owned Assets Supervision and Administration Commission of the State Council (SASAC), <i>Focusing on Key Points and Making Breakthroughs in Innovation, Hubei Solidly Promotes the Deepening and Improvement Actions to Go Deeper and More Concrete</i> (Mar. 25, 2024) (www.sasac.gov.cn/n4470048/n29955503/n30329277/n30329358/c30380577/content.html) ("Statement of China's State Council")
1052	Certified English Translation of Ex. 1051 (Statement of China's State Council)
1053	Sina Finance, <i>Yangtze Memory's "Double 11 Performance" Surpassed Samsung's for the First Time</i> (Nov. 12, 2024) (https://finance.sina.com.cn/roll/2024-11-12/doc-incvupap6483110.shtml) (" <i>Sina Finance Article</i> ")
1054	Certified English Translation of Ex. 1053 (<i>Sina Finance Article</i>)
1055	Southeast University, <i>Yangtze Memory Technologies Co., Ltd. 2024 Campus Recruitment</i> (Mar. 13, 2024) (https://seu.91job.org.cn/substation/lectureDetail?xjhid=1000000000301932&xxdm=10286) ("Southeast Univ., YMTC 2024 Campus Recruitment")
1056	Certified English Translation of Ex. 1055 (Southeast Univ., YMTC 2024 Campus Recruitment)

EXHIBIT NO.	DESCRIPTION
1057	Wuhan University of Science and Technology, <i>Yangtze Memory Technologies Co., Ltd.</i> 2020 Campus Recruitment Introduction (Sept. 10, 2019) (https://wust.91wllm.cn/teachin/view/id/97310) (“Wuhan Univ. of Sci. and Tech., YMTC 2020 Campus Recruitment Introduction”)
1058	Certified English Translation of Ex. 1057 (Wuhan Univ. of Sci. and Tech., YMTC 2020 Campus Recruitment Introduction)
1059	China University of Petroleum, <i>Yangtze Memory 2025 Campus Recruitment</i> (Feb. 20, 2025) (https://career.cup.edu.cn/job/view/id/618140) (“China Univ. Of Petroleum, YMTC 2025 Campus Recruitment”)
1060	Certified English Translation of Ex. 1059 (China Univ. Of Petroleum, YMTC 2025 Campus Recruitment)
1061	Yoko Kubota et al., <i>U.S. Chip Equipment Suppliers Suspend Business Activities at Yangtze Memory</i> , WALL STREET JOURNAL CHINA (Oct. 13, 2022) (https://cn.wsj.com/articles/美国供应商暂停在中国长江存储科技的业务活动-11665617406) (“ <i>WSJ China Article</i> ”)
1062	Certified English Translation of Ex. 1061 (<i>WSJ China Article</i>)
1063	Letter from Michael T. McCaul, Member of Congress, and Bill Hagerty, U.S. Senator, to the Honorable Gina Raimondo, U.S. Commerce Secretary (July 12, 2021)
1064	Demetri Sevastopulo, <i>Bipartisan Group Urges US Blacklist for “Beijing-Directed” Chipmaker</i> , FINANCIAL TIMES (Sept. 20, 2022) (https://www.ft.com/content/173eb5b7-c211-4fa8-af8e-93382ed12836) (“ <i>Financial Times Article</i> ”)

EXHIBIT NO.	DESCRIPTION
1065	U.S. Senator Charles E. Schumer, <i>With Chinese Chip Companies Threatening National Security And Jobs, Schumer Announces President Has Heeded His Call And Will Add YMTC - One Of China's Leading Chip Makers - To A Trade Blacklist; Administration Action Will Strengthen National Security And Protect The Domestic Chip Industry</i> (Dec. 16, 2022) (“Schumer Statement”)
1066	U.S. Department of Defense, <i>DOD Releases List of People's Republic of China (PRC) Military Companies in Accordance with Section 1260H of the National Defense Authorization Act for Fiscal Year 2021</i> (Jan. 31, 2024) (https://www.defense.gov/News/Releases/Release/article/3661985/dod-releases-list-of-peoples-republic-of-china-prc-military-companies-in-accord/)
1067	U.S. Department of Defense, <i>Entities Identified as Chinese Military Companies Operating in the United States in accordance with Section 1260H of the William M. (“Mac”) Thornberry National Defense Authorization Act for Fiscal Year 2021 (Public Law 116-283)</i> (https://media.defense.gov/2024/Jan/31/2003384819/-1/-1/0/1260H-LIST.PDF)
1068	<i>Oversight of the USPTO: Hearing Before the Subcomm. On Intellectual Property</i> , 118th Cong. (2023) (Testimony of Katherine Vidal, Undersecretary of Commerce for IP and Director of USPTO)
1069	China's State Council, <i>Notice of the State Council on Issuing Policies to Promote the High-quality Development of the Integrated Circuit Industry and Software Industry in the New Era</i> (Aug. 4, 2020) (https://www.gov.cn/zhengce/content/2020-08/04/content_5532370.htm) (“State Council Notice on Policies to Promote Development of IC”)
1070	Certified English Translation of Ex. 1069 (State Council Notice on Policies to Promote Development of IC)
1071	Declaration of Karen Lee, Translator (Mar. 10, 2025)

EXHIBIT NO.	DESCRIPTION
1072	Declaration of Fei-Xue Qian, Translator (Mar. 10, 2025)
1073	Order Granting Motion to Stay Case Pending <i>Inter Partes</i> Review, <i>Yangtze Memory Techs. Co., Ltd. v. Micron Tech., Inc. et al.</i> , Case No. 23-cv-05792-RFL, Docket No. 243 (N.D. Cal. Mar. 14, 2025)
1074	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.’s Disclosure of YMTC I Asserted Claims and Infringement Contentions, <i>Yangtze Memory Techs. Co., Ltd. v. Micron Tech., Inc. et al.</i> , Case No. 23-cv-05792-RFL (N.D. Cal. May 6, 2024)
1075	Press Release, Micron, Micron and Intel Unveil New 3D NAND Flash Memory (Mar. 26, 2015) (“Micron ‘3D NAND Flash Memory’ Press Release”)
1076	Press Release, Micron, <i>Micron and WekaIO Win Best of Show Award at the Flash Memory Summit 2019</i> (Aug. 29, 2019) (“Micron ‘Best of Show Award’”)
1077	Micron Technology, Inc., Annual Report (Form 10-K) (Oct. 4, 2024)
1078	Ministry of Industry and Information Technology, The Ministry of Industry and Information Technology Officially Announced the “National Integrated Circuit Industry Development Promotion Outline” (Jun. 26, 2014) (https://www.cac.gov.cn/2014-06/26/c_1111325916.htm) (“National IC Development Promotion Outline”)
1079	Certified English Translation of Ex. 1078 (National IC Development Promotion Outline)
1080	Karen M. Sutter et al., Cong. Rsch. Serv., R47558, <i>Semiconductors and the CHIPS Act: The Global Context</i> (2023)
1081	Declaration from Mel DeSart, University of Washington

EXHIBIT NO.	DESCRIPTION
1082	Accession Confirmation from German National Library
1083	Declaration of Jeremy Jason Lang
1084	Affidavit of Mina Ching
1085	Declaration of Dr. Sanjay Banerjee in Support of Petitioner’s Reply Brief (“Banerjee2”)
1086	Transcript of January 16, 2026 deposition of Stephen Campbell, Ph.D.
1087	USPTO Memorandum, Enforcement and Non-Waiver of 37 C.F.R. §42.104(b)(4) and Permissible Uses of General Knowledge in <i>Inter Partes</i> Reviews (July 31, 2025)
1088	Korean Patent No. 10-2015-0051841 to Park et al. (“Park”) including certified translation
1089	U.S. Patent Publication No. 2013/0228837A1 to Sukekawa et al. (“Sukekawa”)
1090	Dhungana et al., <i>Combinatorial Survey of Fluorinated Plasma Etching in the Silicon-Oxygen-Carbon-Nitrogen-Hydrogen System</i> , Journal of Vacuum Science and Technology A (2016), 061302-1–18
1091	Transcript of November 7, 2025 deposition of Stephen Campbell, Ph.D., <i>Micron Tech., Inc. v. Yangtze Memory Techs. Co., Ltd.</i> , IPR2025-00117 (Patent No. 10,672,711)
1092	Reyes-Betanzo et al., <i>Silicon nitride etching in high- and low-density plasmas using SF₆/O₂/N₂ mixtures</i> , Journal of Vacuum Science and Technology A21, 461–469 (2003)
1093	Declaration of Sylvia D. Hall-Ellis regarding Ex. 1090, Dhungana et al., <i>Combinatorial Survey of Fluorinated Plasma Etching in the Silicon-Oxygen-Carbon-Nitrogen-Hydrogen System</i> , Journal of Vacuum Science and Technology A (2016), 061302-1–18 originally served in Case No. IPR2025-00117

EXHIBIT NO.	DESCRIPTION
1094	Accession Confirmation from German National Library regarding Journal of Vacuum Science and Technology A21 (2003)

TABLE OF ABBREVIATIONS

ABBREVIATION	TERM
'276 patent	U.S. Patent No. 11,101,276 (Ex. 1001)
Banerjee2	Declaration of Dr. Sanjay Banerjee in Support of Petitioner's Reply Brief (Ex. 1085)
Campbell2	Declaration of Steve Campbell in Support of Patent Owner's Response (Ex. 2019)
Chen	U.S. Patent Publication No. 2017/0294384A1 (Ex. 1008)
Fang	U.S. Patent Publication No. 2019/0067306A1 (Ex. 1006)
Han	U.S. Patent Publication No. 2017/0062470A1 (Ex. 1007)
Kim	U.S. Patent Publication No. 2012/0070944A1 (Ex. 1005)
Park	Korean Patent No. 10-2015-0051841 including certified translation (Ex. 1088)
Yu	U.S. Patent Publication No. 2018/0330985A1 (Ex. 1009)
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 11,101,276 (IPR2025-00228, Paper 1)
POR	Patent Owner's Response (IPR2025-00228, Paper 31)
PO or Patent Owner	Yangtze Memory Technologies Co. Ltd.
Petitioner	Micron Technology, Inc.

I. INTRODUCTION

Patent Owner's ("PO's") arguments fail to overcome Petitioner's showing that the '276 patent's claims are unpatentable. PO first argues that it wouldn't have been obvious to reverse the alternating-layer ordering. But the record demonstrates that both orders were well-known, suitable, and routine to implement. PO next argues that Kim doesn't disclose "exposing portions of the etch-stop layer" of claim 1. But this contradicts the testimony of PO's expert (Dr. Campbell) that exposing must occur before penetrating the etch-stop layer. Regarding Grounds 2–4, PO's arguments against combining references fail, because they misread the references and rely on irrelevant technical differences. While PO argues that Grounds 1 and 3 do not render obvious the relative etch rates of claims 4–5, PO fails to rebut that the need to prevent punch-through makes lower etch rates the obvious choice.

At bottom, the record demonstrates that the '276 patent claims nothing but combining well-known elements in conventional, predictable manners. That is the epitome of obviousness.

II. CLAIM CONSTRUCTION

PO contends that claim 1's limitations "exposing portions of the etch-stop layer" and "etching the exposed portions" are distinct. POR, 8–13. Petitioner never suggested otherwise, but instead explained how Kim discloses these two distinct

steps. Pet., 46–49; Banerjee2 ¶¶11–12. Because there is no dispute, no construction is necessary. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019).

III. GROUND 1

A. Kim Renders Obvious “Disposing a Sacrificial Layer over a Dielectric Layer”

1. Kim’s gate-stack-on-top disclosure applies to Figures 17A–22B

Despite later making a “missing-limitation” argument (*infra*, §III.A.2), PO doesn’t dispute that Kim itself discloses staircases having the alternating layers in both orders. POR, 16; Campbell2 ¶40; Ex. 1086, 108:12–18. Nor does PO dispute additional references demonstrate that both orders were well-known, suitable options. Pet., 33. PO merely disputes whether there was motivation to invert the order in the Petition’s chosen embodiment with a reasonable expectation of success. POR, 15. PO is wrong on the law and the facts.

a. The inverted order is a suitable alternative, which provides motivation

To start, PO’s “motivation” argument fails because it requires a showing that the gate-stack-on-top alternative provides a “benefit.” POR, 16. Not so. In *Intel Corp. v. PACT XPP Schweiz AG*, the petitioner suggested that a POSITA would have substituted a prior-art element with another from a secondary reference that “address[ed] the same problem”—“just through a different mechanism.” 61 F.4th 1373, 1380 (Fed. Cir. 2023). The Board opined that no motivation existed because

the substitution produced no “obvious improvement.” *Id.* The Federal Circuit reversed, explaining the fact that the secondary reference provided a “known way to address [the same] problem is precisely [why] there’s a motivation to combine under *KSR*....” *Id.* The petitioner “never had to show that replacing” one known mechanism with another for addressing the same problem “was an ‘improvement’ in a categorical sense”; showing that it was a “suitable option” sufficed. *Id.* at 1381.

Here, the motivation is stronger than in *Intel*. 3D staircases in either layer order provide isolated gate stacks, meeting the demand for higher-density memories. Multiple references independently demonstrate that both orders were well-known, predictable variations, and thus obvious. *Smith & Nephew, Inc. v. Hologic, Inc.*, 721 F. App’x 943, 948 (Fed. Cir. 2018) (substituting a predictable variation with another provided motivation); *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) (obvious to simply arrange old elements to perform the conventional function and yield expected results). Moreover, the same primary reference (Kim) undisputedly shows both suitable options, along with all other limitations. Banerjee2 ¶¶13–15.

Kim’s disclosure of both orders in a closely related embodiment further supports obviousness. In *Boston Sci. Scimed, Inc. v. Cordis Corp.*, the Wolff reference disclosed two different stents having components designated with identical numerals, but an optional coating for **only one** stent. 554 F.3d 982, 990–92 (Fed. Cir. 2009). Finding it obvious to apply that optional coating to the other stent,

Boston Sci. recognized that obviousness doesn't require the reference itself to "have recognized" the benefits, highlighting the "predictable variation" based on identical numerals. *Id.* at 991. Indeed, "[c]ombining two embodiments disclosed adjacent to each other ... does not require a leap of inventiveness." *Id.* Like Wolff, Kim discloses closely related embodiments with identical numerals. Banerjee2 ¶¶16–17; *Paice LLC v. Ford Motor Co.*, 681 F. App'x 904, 917 (Fed. Cir. 2017) (finding a "predictable variation" on similar facts).

PO cites inapposite cases because, unlike here, none involves primary and background references all disclosing the same well-known, predictable variations. Indeed, Chen discloses both embodiments side-by-side and doesn't bother to explain their well-known implementation details. Banerjee2 ¶15; *Epistar Corp. v. ITC*, 566 F.3d 1321, 1336 (Fed. Cir. 2009) ("[a] patent ... preferably omits[] what is well known in the art"). Further, unlike *In re Stepan Co.*, Kim, Chen, and Yu demonstrate that both orderings were well-known alternatives and thus "explain[] why a [POSITA] would have arrived at the claimed invention..." 868 F.3d 1342, 1346 (Fed. Cir. 2017). *InTouch Techs., Inc. v. VGO Commc'ns, Inc.*, unlike the Petition here, involved combining two "disparate" secondary references. 751 F.3d 1327, 1332–33, 1351–52 (Fed. Cir. 2014).

Next, PO alleges that Kim discloses that its etch-stop layer, *e.g.*, "covers only 'end portions'," thereby "requiring a gate-stack-on-bottom ordering" for the Figures

17A–22B embodiment. POR, 19. That makes no sense—Kim is simply describing the gate-stack-on-bottom embodiment. Kim would say the reverse if it was describing the opposite ordering. Banerjee2 ¶18.

b. Inverting the layers was routine, which provides a reasonable expectation of success

To start, PO’s arguments all fail, because Chen alone demonstrates an expectation of success by describing both orderings *without mentioning the minor implementation changes* in fabricating either ordering. Banerjee2 ¶15. Chen’s silence demonstrates that a POSITA “was more than capable of selecting between the[se] known methods....” *Uber Techs., Inc. v. X One, Inc.*, 957 F.3d 1334, 1339 (Fed. Cir. 2020). Notably, Dr. Campbell concedes that inverting Kim’s layers isn’t more complicated than inverting Chen’s. Ex. 1086, 117:24–119:5. Reversing the order primarily involves changing the layers’ deposition order. Yu, [0034]; Ex. 1086, 42:24–43:10; Ex. 1091, 92:5–93:5; Banerjee2 ¶¶19–27.

Regardless, PO incorrectly advances two alleged “technical issues that prevent a reasonable expectation of successfully combining [sic] the references¹.” POR, 20.

First, PO argues that replacing Kim’s thicker, step-shaped insulating layers creates problematic step-shaped gate-stack layers. POR, 20–22. But these thicker

¹ “References” is incorrect. Only Kim is at issue.

layers are optional. Kim, [0232]. Without them, inverting the layers does not create step-shaped gate-stack layers, mooting PO's argument.

Even if the thicker layers were mandatory, Kim contradicts PO's argument. Kim undisputedly discloses layer-ordering inversion for the Figure 5A–14B embodiment—and Figure 12B, like Figure 20B, shows the optional thicker insulating layers. Thus, the gate-stack-on-top order is suitable even with the thicker layers. For example, a POSITA would have known to adjust layer thicknesses to avoid PO's alleged problems, which all stem from the gate-stack layers being “too thin.” POR, 20–21; Banerjee2 ¶¶28–29. Moreover, obviousness does not require bodily incorporating the features of one embodiment into another. *Qualcomm Inc. v. Intel Corp.*, 2024 WL 4258364, at *4 (Fed. Cir. Sept. 23, 2024).

Second, PO argues that a gate-stack-on-top configuration requires forming shorter conductive structures and additional adjustments and is thus nonobvious. POR, 22. But “changing one component often requires the others to be modified” and does not render the change nonobvious. *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 800 (Fed. Cir. 2021). Such interrelated changes are what PO alleges. Ex. 1086, 137:14–138:2. Moreover, such changes were routine, as Kim's, Yu's, and Park's (Ex. 1088) layer-ordering-reversal disclosures demonstrate. Kim, [0090], Yu, [0034]; Park, [0102]; Banerjee2 ¶30.

Third, PO argues that a gate-stack-on-top configuration “*may*” render the etch-stop layer unnecessary (like “the alternative Figures 4–15D embodiment”), due to altered etch selectivity between the sacrificial layers and the overlying insulating layer. POR, 22 (“*if* it is not needed”).² This argument fails legally and technically. Legally, “[t]he *mere possibility* that such combination would [achieve a] result [contrary to the invention’s] does not render its successful use unobvious [because] [o]bviousness does not require absolute predictability.” *Application of Passal*, 426 F.2d 409, 412 (C.C.P.A. 1970). Technically, first, Kim’s etch-stop layer undisputedly facilitates preventing punch-through in the gate-stack-on-top configuration and is thus desirable. Ex. 1086, 117:6–10, 131:14–132:12. Second, inverting the layers does not change the etch-selectivity considerations because the sacrificial layers directly contact the overlying insulating layer in either layer order. Banerjee2 ¶31.

Fundamentally, in light of Kim, Yu, and Chen, PO cannot credibly dispute that both orders were routine. POR, 23–24. Consistent with that, Dr. Campbell testified that “every time you do any deposition and etching, you have to” “experiment to make [it] work.” Ex. 1091, 106:23–107:10. “[A] POSITA would

² All emphases are added and internal quotation marks and citations omitted unless otherwise noted.

certainly know that’s what you have to do. [There is] not[hing] unique to this process.” *Id.*; Banerjee2 ¶¶19–27. A reasonable expectation of success exists for that which involves “routine, conventional methods and skill.” *Salix Pharms., Ltd. v. Norwich Pharms. Inc.*, 98 F.4th 1056, 1066 (Fed. Cir. 2024).

2. Kim has no missing limitations

PO argues that Petitioner improperly relied on references to supply “missing limitations” and “motivation” (POR, 24–26). That is an incorrect attorney argument.³ Banerjee2 ¶32. First, there are no “missing limitations”: Kim discloses both orders. Second, Petitioner’s reliance is proper because “the motivation to combine ... need not come from the references themselves.” *LKQ Corp. v. GM Glob. Tech. Operations LLC*, 102 F.4th 1280, 1299 (Fed. Cir. 2024).

That Kim discloses all limitations moots PO’s remaining arguments, which presume **missing** limitations. POR, 22–26. Specifically, the “unusually simple” and “particularly straightforward” inquiry applies when “invok[ing] common sense to fill in a **missing** limitation.” *DSS Tech. Mgmt., Inc. v. Apple Inc.*, 885 F.3d 1367, 1374 (Fed. Cir. 2018) (italics in original).

³ PO alleges “all four grounds fail on [this] basis alone.” POR, 26. But Grounds 3–4 do not involve layer-order inversion.

Even if Kim were missing claim limitations, PO misapplies the law. First, the claimed sacrificial-layer-on-top order is a “peripheral” limitation to which the inquiry does not apply. *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1363 (Fed. Cir. 2016). The alleged invention is the etch-stop layer, not the gate-stack-on-top configuration. Ex. 1001, 5:47–6:10; POR, 12 (characterizing the etch-stop protection as “the invention’s goal”). Second, PO ignores a “skilled artisan[’s]” perspective in assessing “unusually simple” missing limitations. *FullView, Inc. v. Polycom, Inc.*, 2024 WL 1843686, at *5 (Fed. Cir. Apr. 29, 2024). The record demonstrates that the gate-stack-on-top embodiment was straightforward to a POSITA. *Supra* §III.A.1.

Notably, the record contradicts PO’s assertion that inverting the layers is a complex process. POR, 29–30. Chen’s side-by-side depiction of both layer orders—without further explanation—demonstrates that either order was unusually simple. *Supra* §III.A.1; Banerjee2 ¶15. The Board “must disregard [expert] testimony ... that is plainly inconsistent with the record.” *Homeland Housewares, LLC v. Whirlpool Corp.*, 865 F.3d 1372, 1378 (Fed. Cir. 2017). Here, the record contradicts Dr. Campbell. His conclusory argument that layer-order inversion would cascade into many other changes contradicts his own testimony that such changes were routine to implement and have been dealt with for decades. POR, 29–30; Ex.

1091, 37:20–38:12, 40:12–22. Regardless, ripple-effect changes do not render the inverted order nonobvious. *Intel*, 21 F.4th at 800.⁴

Further, the alleged complexities do not render the claims nonobvious because they are ***unclaimed*** etch-process details that none of the patents—including the ’276 patent—address. Ex. 1086, 78:5–81:7; 83:15–84:4, 122:12–124:13; Banerjee2 ¶¶34–35; *Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1570 (Fed. Cir. 1997) (claims obvious over prior art not disclosing unclaimed aspects that the patent itself doesn’t disclose).

Finally, PO’s broad assertion that 3D NAND technology is complex misses the mark. POR, 27–28. Before the priority date, the technology at issue (alternating-layer ordering) was well known and straightforward according to ***PO’s own evidence***: “Many 3D NAND companies use the same process steps. The general fab techniques are known.” Ex. 2028, 8; Ex. 2027, 6 (“mature” “48-layer alternating stack deposition process”); *id.*, 7 (“conventional etching tools”); Banerjee2 ¶33.

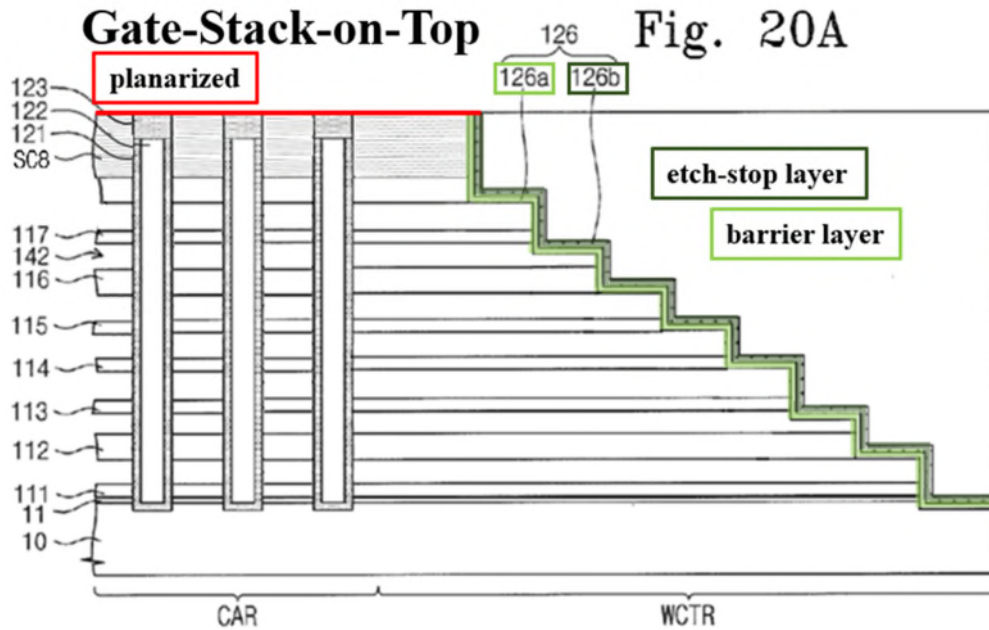
⁴ PO alleges the gate-stack-on-top configuration renders Kim’s lower-gate-insulating layer unnecessary, and its inclusion in the modified Kim figures shows technical complexity. POR, 30. PO is wrong because Chen shows that extra insulation is simply a design choice. Banerjee2 ¶36.

B. Kim Discloses “Exposing Portions of the Etch-Stop Layer”

PO contends that Kim does not disclose “a step where etching penetrates the insulating layer exposing—but not penetrating—portions of the etch-stop layer.” POR, 31–34. PO’s argument ignores the etch-stop layer’s essence and contradicts the record.

The essence of an *etch-stop* layer dictates that contact-hole etching stops or slows down upon contact, *i.e.*, exposing without penetrating it. The etch selectivity of the interlayer dielectric relative to the etch-stop layer ensures that this occurs. Pet. 46–47; POR, 53 (recognizing this selectivity is “why an etch-stop layer is an etch-stop layer”). Dr. Campbell agrees that Kim’s etch “*stop*” layer functions as an etch *stop* for contact-hole etching. Ex. 1086, 117:6–10, 131:14–132:12. To penetrate it, etch chemistry must first be changed. *E.g., id.*, 93:24–94:5, 62:10–15, 70:17–20; Banerjee2 ¶¶37–39.

PO argues that Kim’s etch selectivity relative to the etch-stop layer is only for planarizing the interlayer dielectric. POR, 33–34. But Dr. Campbell conceded that Kim’s etch-stop layer prevents punch-through. Ex. 1086, 117:6–10, 131:14–132:12. Further, PO’s argument implies that the post-planarization etch-stop layer (shown below) is useless, because planarization doesn’t impact anything below the top surface. POR, 33; Ex. 1086, 135:22–136:8.



Kim, Fig. 20A. So if PO were right, Kim’s etch-stop layer would have covered only the staircase’s top layer to avoid “includ[ing] a non-functional component.” Campbell2 ¶¶46; Banerjee2 ¶¶40–41.

C. Kim in View of a POSITA’s Knowledge Renders Claim 4 Obvious

PO does not dispute claim 4’s relative-etching-rate limitation represents one of three relationships, and common knowledge demonstrates that only the claimed relationship is realistic. Instead, PO argues that Petitioner improperly relied on a POSITA’s knowledge and background references to show that the limitation is obvious. POR, 35. But PO merely cross-references its claim 1 arguments without addressing why claim 4’s limitation is unusually simple. Petitioner’s “reasoned analysis and evidentiary support” using background references, however, are proper. *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1338 (Fed. Cir. 2020). In

contrast, PO relies on a conclusory expert declaration that is inconsistent with the record. Banerjee2 ¶¶42–45. Additionally, Dr. Campbell admits the well-known need to prevent punch-through, further confirming claim 4’s obviousness. Ex. 1086, 92:12–25.

D. Kim in View of a POSITA’s Knowledge Renders Claim 5 Obvious

PO’s arguments in subsection III.D.1 are identical to those asserted regarding claim 4. They likewise fail. *Supra* §III.C.

In subsection III.D.2, PO incorrectly argues against a motivation to combine Kim with a POSITA’s knowledge to render claim 5 obvious. POR, 37–38.⁵ PO first argues that, because Kim already has two etch-stop layers, a lower etch rate for the underlying first high-k dielectric layer would provide no benefit. *Id.*, 37. But Dr. Campbell admits that, by applying well-known etchants, Kim discloses this exact configuration. Banerjee2 ¶¶46–48.⁶ PO next argues that claims 6 and 14 permit the same material for the etch-stop and first high-k dielectric layers. POR, 38. But claim

⁵ Subsection III.D.2’s heading includes “a reasonable expectation of success[],” but PO waived the argument by not discussing it.

⁶ PO argues that the etch-stop and first high-k dielectric layers *could be* the same material and thus have equal etching rates. POR, 37. But Kim discloses different materials for these layers. Banerjee2 ¶48 n.12.

5 *requires* different etch rates and thus different materials. Ex. 1086, 148:22–149:1. Lastly, PO points to the additional and therefore irrelevant purpose of the high-k dielectric layer during gate-stack formation. Banerjee2 ¶49.

E. Kim in View of a POSITA’s Knowledge Renders Claim 11 Obvious

PO’s arguments are identical to those asserted regarding claim 4. *Compare* POR, 38–39 *with id.*, 35. They likewise fail. *Supra* §III.C; Banerjee2 ¶¶50–51.

IV. GROUND 2

PO doesn’t dispute that Kim and Fang together disclose all of the Ground 2 limitations. PO only disputes the motivation to combine them. POR, 39–55. But the record shows that Fang’s etch-stop characteristics are applicable to Kim. Pet., 64–74; Banerjee2 ¶52.

A. A POSITA Would Have Been Motivated to Combine Kim and Fang with a Reasonable Expectation of Success

1. Etch-Stop Characteristics

a. Punch-through was Kim and Fang’s shared concern

PO points to the different problems that Kim and Fang address to allege a lack of motivation to combine. POR, 41–44. But that is irrelevant because “the problem motivating [Kim] may be only one of many addressed by [Kim’s] subject matter.” *KSR*, 550 U.S. at 420. That is, Kim need not expressly address contact-hole etch stops to demonstrate their necessity. Indeed, Kim’s etch-stop coverage of the entire staircase demonstrates that Kim, like Fang, sought to prevent punch-through. *Supra*

§III.B. And Dr. Campbell contradicts PO's apparent, senseless argument that Kim employs an etch *stop* over the steps, but not to *stop* etching and avoid punch-through because Kim doesn't expressly say so. Banerjee2 ¶¶53–54.

Even if preventing over-etching did not motivate Kim, a claim reciting an obvious solution to a known problem, regardless of Kim's individual motivations, is obvious. *KSR*, 550 U.S. at 419–20. Thus, Fang's solution motivates the combination.

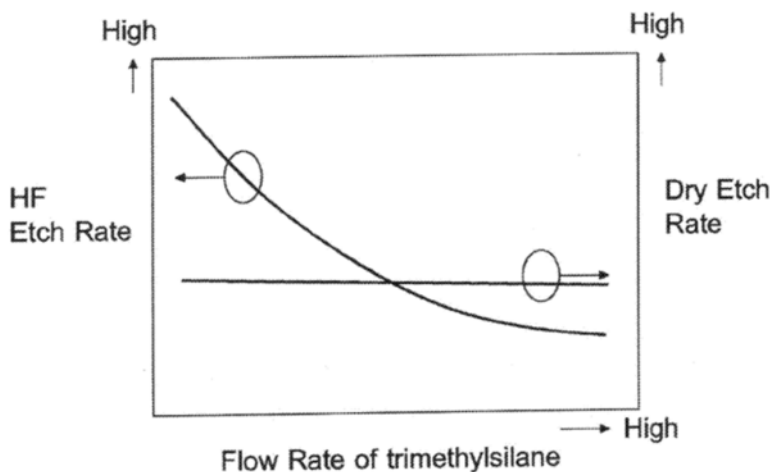
b. Fang's carbon doping is optional and immaterial to obviousness

PO argues against a motivation to combine Kim and Fang because they use different etch-stop materials. POR, 44–47. But the prior art of record and Dr. Campbell contradict PO's arguments. Banerjee2 ¶¶55–56.

Notably, Dr. Campbell himself equates silicon nitride and carbon-doped silicon nitride ("CDSN"). Campbell2 ¶107 ("Chen mentions silicon nitride is an acceptable second stop layer (i.e., Fang's [CDSN] etch-stop layer in Petitioner's combination).") That moots PO's arguments.

Moreover, first, Fang discloses the etch-stop thickness range after disclosing the etch-stop material "[b]y way of example only." Fang, [0020]. Plainly, then, the disclosed etch-stop characteristics are not limited to a specific material. Fang's disclosure applies broadly to any suitable etch-stop material. Banerjee2 ¶58.

Second, even if Fang's disclosure were specific to CDSN, that is irrelevant. Both Kim and Fang etch contact holes using a dry-etching process. Pet., 66. Thus, the etch-stop layer's dry-etch rate (and thus the appropriate thickness for a given margin against over-etching) is what matters. Banerjee2 ¶57. As the flat line below shows, dry-etch rates of silicon nitride (as PO alleges Kim only discloses) are constant across varying carbon-doping levels (as PO alleges Fang only discloses):



Ex. 1089, Fig. 19, [0035] (trimethylsilane flow rate representing carbon-doping level). Thus, even assuming Fang's etch-stop layer must be carbon-doped, its thickness applies to Kim because doping doesn't affect the dry-etch rate. Banerjee2 ¶¶60–61.

PO argues that because Fang's gate-replacement process "does not allow for a silicon nitride etch stop" (*i.e.*, Kim's etch stop material), Fang teaches away from the combination. POR, 45–46 (emphasis omitted). Not so. Fang broadly teaches that an etch-stop layer may be, *e.g.*, a high-k material. Pet., 65. That Fang's gate-

replacement process doesn't allow for a silicon-nitride etch stop does not negate Fang's broader teaching that, in general, an etch stop may be a high-k material. Moreover, Fang's prohibition against using silicon nitride for ***both*** the etch-stop and sacrificial layers (*i.e.*, nitride materials 120) to avoid removing them together is irrelevant because Kim's silicon-oxide barrier layer separates them, preventing their simultaneous removal. Banerjee2 ¶59, 63.

c. Kim and Fang's structural differences are immaterial

PO incorrectly argues that structural differences below the etch-stop layer, *i.e.*, Kim's high-k dielectric layer, barrier layer, and gate-stack-on-top configuration, would have discouraged the combination. POR, 47–51.

Fundamentally, structural differences below the etch-stop layer are irrelevant to etching the overlying insulating layer and thus to the etch-stop characteristics when the etch-stop layer works as intended. As PO recognizes, “the etch-stop layer is to protect underlying structures during the etching process” (*i.e.*, what PO calls the “exposure step,” POR, 8) and it “cannot” serve this purpose “if it has already been penetrated.” *Id.*, 47, 13; Ex. 1086, 53:22–54:2. Hence, a properly designed etch-stop layer is not penetrated, and the underlying structure is not exposed, during the exposure step. Ex. 1086, 52:23–53:1. An unexposed structure is beyond the etchants' reach and does not function as an etch stop. *Id.*, 85:15–20; Ex. 1091, 56:2–14. Therefore, the underlying layers are “irrelevant” in preventing over-etching

during the exposure step. Ex. 1086, 98:19–99:1, 99:11–16. If PO argues that underlying layers can serve as back-up etch stops in case the etch-stop layer is prematurely penetrated at shallow holes, that is a made-up issue because a POSITA would have designed an etch-stop layer to prevent it. *Id.*, 90:11–18. Indeed, a POSITA would have desired to preserve as much of the etch-stop layer as possible so that etching after the exposure step proceeds across all contact holes in “lockstep, in a uniform manner.” *Id.*, 94:14–22, 97:7–14; Banerjee2 ¶¶64–70.

2. A High-K Dielectric Etch-Stop Layer

PO incorrectly argues against motivation and a reasonable expectation of success in having a high-k dielectric etch-stop layer. POR, 51–54. To start, Petitioner cited hafnium oxide as merely an exemplary high-k material for the combination, and PO argues against only hafnium oxide, not any other high-k material. Pet., 65; POR, 51–54. Thus, PO’s arguments fail, because they address only a subset of Petitioner’s position.

PO’s arguments against hafnium oxide also fail. Banerjee2 ¶71.

First, PO argues that Fang discloses hafnium oxide only as a possible alternative to Fang’s CDSN, and thus it is not a suitable alternative to Kim’s undoped silicon nitride. POR, 51–52. PO is wrong because Fang discloses high-k dielectrics (e.g., hafnium oxide) and CDSN equally as alternative etch-stop materials, not high-k dielectrics as alternatives *to* CDSN. Fang, [0022]. Regardless, in relevant respects

(i.e., etch rate),⁷ hafnium oxide is a suitable alternative to both CDSN and silicon nitride, because both have the same dry-etch rate. *Supra* §IV.A.1.b.

Second, PO argues that hafnium oxide’s greater tunneling length would not have provided motivation because Kim doesn’t identify inadequate tunneling lengths. POR, 51–52. But a POSITA “need not see the identical problem addressed in a prior art reference to be motivated to apply its teachings.” *Cross Med. Prods., Inc. v. Medtronic Sofamor Danek, Inc.*, 424 F.3d 1293, 1323 (Fed. Cir. 2005).

Third, PO argues that Kim’s two-etch-stop configuration already “protect[s] against tunneling,” such that a high-k etch-stop layer provides no additional benefit. POR, 52. But replacing a silicon-nitride etch-stop layer with a high-k dielectric in a two-etch-stop configuration, as Chen shows in Figures 8C–8D, **increases** the tunneling length. Ex. 1086, 110:20–111:5. And Chen teaches that a **greater** tunneling length is “**more** effective” to electrically isolate conductive layers. Chen, [0004], [0020]. So is replacing Kim’s silicon nitride with a high-k dielectric. Banerjee2 ¶62.

⁷ Only two factors—etch rate and thickness—determine whether an etch-stop layer would function as needed. Banerjee2 ¶57. Claim 1 does not recite a thickness, which in any event is adjustable based on the etch rate. Thus, only the etch rate is relevant.

PO next makes two arguments against an expectation of success. POR, 52–54. The first, a tunneling-length argument, repeats PO’s argument against motivation and likewise fails. *Id.*, 52–53. Next, PO alleges that using hafnium oxide for Kim’s etch-stop layer lacks prior-art guidance and dooms the expectation of success. Not so. Fang provides no guidance on using hafnium oxide in its own embodiments. This silence shows that using hafnium oxide as an etch stop was routine with a reasonable expectation of success. *Epistar*, 566 F.3d at 1336; *Salix Pharms.*, 98 F.4th at 1066. Moreover, Dr. Campbell testified that “every time you do any deposition and etching, you have to” “experiment to make [it] work.” Ex. 1091, 106:23–107:10. “[A] POSITA would certainly know that’s what you have to do. [There is] not[hing] unique to this process.” *Id.*

3. A Hafnium-Oxide Etch-Stop Layer

PO argues against motivation and a reasonable expectation of success in using hafnium oxide for the etch-stop layer. POR, 54–55. PO cross-references its failed arguments against claim limitation [1.B]. *Supra* §IV.A.2. Further, PO again incorrectly argues that Fang’s sacrificial-layer removal precludes substituting Kim’s silicon nitride with hafnium oxide. POR, 55; *supra* §IV.A.1.b; Banerjee2 ¶¶72–74.

V. GROUND 3

PO doesn't dispute that Han and Fang together satisfy all of the Challenged Claims' limitations. PO only incorrectly argues that there was no motivation to combine them. POR, 56.

A. A POSITA Would Have Been Motivated to Adapt Fang's Etch-Stop Layer to Han with a Reasonable Expectation of Success

Respecting claim 1, PO argues against a motivation to combine Han with Fang's etch-stop layer with a reasonable expectation of success for three incorrect reasons. POR, 56–59.

First, PO argues that Han's gate stacks—with their high-k layers functioning as etch stops—render Fang's etch-stop layer unnecessary. POR, 57. But both Kim and Park disclose etch-stop layers over staircases comprising high-k-dielectric gate-stack layers—the exact configuration in which PO alleges such etch stops are unnecessary. Kim, Fig. 22A, Park, Fig. 9j. Should PO attempt to distinguish Han's multi-high-k-dielectric-layer configuration from Kim's and Park's single-high-k-dielectric-layer configuration, PO would be misguided because Han and Park disclose both configurations. Han, Figs. 26B–26D; Park, Figs. 7a–7c. And Petitioner didn't rely on Han's multi-high-k-dielectric embodiments. Pet., 85 (TIL “*or*” BK layer). Moreover, Kim and Park also disclose insulator-over-gate-stack staircases (the insulator being much thicker than the high-k dielectric layers), which

provide *more* punch-through protection and would render an etch-stop layer *more* unnecessary under PO's (incorrect) theory.⁸ POR, 24; Banerjee2 ¶¶75–76.

Second, PO alleges that Han's staged-etching process renders an etch-stop layer unnecessary. POR, 58. Initially, even Dr. Campbell's conclusory say-so only states that staged etching "mitigates," not solves, the punch-through issue that the etch-stop layer undisputedly solves. *Id.* Next, Dr. Campbell admitted that the staged-etching process involves multiple masks. Ex. 1086, 144:18–145:24. Fang teaches that using multiple masks incurs "additional processing acts, complexity, and cost." Pet., 102.⁹ Therefore, a POSITA would have been motivated to apply Fang's etch stop to Han, thereby obviating the costly masks. Banerjee2 ¶¶77–78.

⁸ *Provisur Techs., Inc. v. Weber, Inc.* is inapposite. 2022 WL 17688071 (Fed. Cir. Dec. 15, 2022). There, the combination "would *double* the number of steps..., adding *needless* complexity *and increasing the likelihood of malfunction.*" *Id.* at *5. Here, the *alleged incremental* complexity of adding an etch-stop layer provides *increased over-etch protection.*

⁹ Fang contradicts PO's argument that an etch-stop layer *adds* "cost, time, and complexity." POR, 58.

Third, PO’s recycled layer-inversion arguments are irrelevant because Han discloses the gate-stack-on-top configuration—no “reordering” is needed. POR, 58. These arguments further likewise fail. *Supra* §III.A.2; Banerjee2 ¶¶79–80.

Lastly, PO additionally argues that Han does not disclose an over-etching problem, and thus provides no motivation for an etch stop. POR, 59–60. But a motivation need not come expressly from the primary reference. *Cross Med. Prods.*, 424 F.3d at 1323. Further, Han’s staged-etching process indicates a concern for over-etching. Banerjee2 ¶81.

B. Han in View of Fang Undisputedly Renders Claim 4 Obvious

Claim 4 is obvious in view of a POSITA’s knowledge *and additionally* in view of Fang. Pet., 91–92. PO only argues against combining a POSITA’s knowledge. POR, 60–61. Thus, Han and Fang undisputedly render claim 4 obvious.

C. Petitioner Properly Relied on a POSITA’s Knowledge for Claims 4–5

PO makes virtually verbatim arguments regarding both claims 4–5’s obviousness in view of a POSITA’s knowledge. POR, 60–62. These arguments merely cross-reference PO’s earlier arguments against applying background knowledge and likewise fail. *Supra* §III.A.2. For example, PO fails to analyze claims 4–5. POR, 61–62. That is insufficient to show that these allegedly missing limitations of relative etch rates are not unusually simple. *Supra* §III.A.2; Banerjee2 ¶¶82–84.

D. A POSITA Would Have Had a Motivation to Apply the Relative Etch Rates with a Reasonable Expectation of Success

For claim 5, PO relies on its earlier arguments respecting Kim's and Han's first high-k dielectric layers to argue against motivation and a reasonable expectation of success in adopting the relative etch rates. POR, 62. PO does not explain why its arguments respecting Kim are applicable. Even if they were, those arguments likewise fail with respect to claim 5. *Supra* §§III.D, V.A.

PO next argues against a reasonable expectation of success because neither Han nor Fang alone discloses all claim limitations. But “[n]on-obviousness cannot be established by attacking references individually....” *In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986). Moreover, Kim and Park show that such a combination were within a POSITA's knowledge and skill. *Supra* §V.A.

PO alleges that “the background reference Petitioner cite[d]” to show an exemplary material combination having the claimed relative etching rates “is irrelevant” because it shows a simple argon plasma. POR, 63. But the reference also shows the claimed relative etch rates in “HBr+Ar,” a hydrogen-bromide-and-argon mixture, at various HBr levels. Ex. 1086, 84:12–20.

Lastly, PO argues that Fang does not disclose an aluminum-oxide etch stop and thus Petitioner's example involving such an etch stop does not render claim 5 obvious. POR, 63. But Fang's etch-stop material “may be a high-k dielectric

material,” which includes aluminum oxide. Fang, [0022]. And Petitioner’s example undisputedly shows the claimed relative etch rates. Banerjee2 ¶¶85–90.

VI. GROUND 4

PO doesn’t dispute that Han, Fang, and Chen together disclose all claims 17–18’s limitations, including Chen’s barrier layer. PO only incorrectly argues against motivation to combine them based on their alleged differences. POR, 63–68.¹⁰

A. Han and Fang Would Benefit from a Barrier Layer

Cross-referencing its earlier arguments, PO incorrectly argues that Han’s staircase would not benefit from Fang’s etch-stop layer. POR, 65; *supra* §V.A. PO then extrapolates that same argument to Chen’s barrier layer. POR, 65–66. PO’s conclusory argument likewise fails. *Supra* §V.A; Banerjee2 ¶¶91.

B. Chen Would Have Motivated a POSITA to Add a Barrier Layer

PO argues that Han’s high-k dielectric layer would have rendered a barrier layer redundant because Han together with Fang has adequate tunneling length. POR, 66. PO, however, ignores Chen’s teaching that a **greater** tunneling length is **more** effective at electrically isolating conductive layers. *Supra* §IV.A.2; Banerjee2 ¶¶92–93.

¹⁰ The title of subsection VI.A notwithstanding, PO makes no argument against a reasonable expectation of success. POR, 64–68.

C. The Alleged Differences Are Irrelevant to Adding a Barrier Layer

PO argues against adding Chen’s barrier layer to the Han-Fang combination for the same reason against adding Fang’s etch-stop layer to Han. POR, 67. That conclusory argument likewise fails. *Supra* §V.A; Banerjee2 ¶94.

PO further argues that adding a barrier layer is not a design choice, alleging that Chen teaches complex “interrelated choices.” POR, 67. But Dr. Campbell agreed that a “barrier layer provides flexibility in terms of processing parameters,” and the choice between one or two etch stops represents a “common tradeoff in engineering.” Ex. 1091, 46:13–47:21. By suggesting a lack of reason to combine, PO ignores the benefit of increased tunneling length and that a suitable alternative itself provides a reason. Pet., 105–107; Banerjee2 ¶¶92–93. Further, Chen’s side-by-side disclosure of insulator-on-top and gate-on-top embodiments contradicts PO’s assertion that Chen “recognizes that the order of the layers matter [sic].” POR, 67; Banerjee2 ¶15.

Finally, PO argues that the “known-technique” doctrine does not provide motivation because Chen does not disclose that its etch-stop layer would prevent punch-through. POR, 68. That argument incorrectly presumes that Chen’s “etching stop layer” doesn’t do what its name says it does. Chen, title.

VII. DR. CAMPBELL IS NOT A POSITA AND HIS TESTIMONY IS UNSUPPORTED BY EVIDENCE OR KNOWLEDGE OF DISPUTED ISSUES

PO did not dispute the qualifications of a POSITA, which require “2-3 years of professional experience working with (*e.g.*, researching, designing, or teaching) monolithic 3D structures and NAND memory devices....” POR, 7–8. Dr. Campbell admitted that he did not have experience in 3D memories as of the priority date. Ex. 1091, 33:5–8, 19:17–22. He admitted that he is not a semiconductor designer and could not testify as such. *Id.*, 32:1–13, 32:23–25, 33:22, 134:9–16, 149:5–10. This is fatal to PO. *In re Ona*, 62 F.3d 1433 (Fed. Cir. 1995).

Moreover, other than citing references for his generalization that 3D NAND is a complex technology, Dr. Campbell’s testimony is virtually unsupported by any evidence. Campbell2 ¶¶48–49 (citing Exs. 2022–26, 2028–29); Banerjee2 ¶33 n.6. “[A]n unsupported [expert] opinion is not substantial evidence,” and the Board may not credit an expert opinion that “contradict[s] a [prior-art] reference.” *Ericsson Inc. v. Intellectual Ventures LLC*, 890 F.3d 1336, 1346 (Fed. Cir. 2018).

Further, Dr. Campbell’s deposition exposes his lack of familiarity with disputed issues. He could not even explain his own declaration. Ex. 1086, 133:21–134:20. This is unsurprising, considering Dr. Campbell’s lack of POSITA qualification and given that his declaration merely parrots PO’s arguments. *Compare, e.g.*, Campbell2 ¶¶40–41, 45–46 with POR, 18–19, 20–22. His testimony

on disputed issues is not entitled to any weight. *Garmin Int'l, Inc. v. LoganTree, LP*, 825 F. App'x 894, 898 n.5 (Fed. Cir. 2020).

VIII. CONCLUSION

Petitioner respectfully requests a final written decision finding the Challenged Claims unpatentable.

Respectfully submitted,

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Dated: January 30, 2026

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing Petitioner's Reply Brief complies with the word count limits set forth in 37 C.F.R. §42.24(a)(1)(i). Excluding the parts of the Petition exempted by 37 C.F.R. §42.24(a)(1), this Reply contains 5,596 words as determined using the word count feature in Microsoft Word, which was used to prepare this Reply.

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CERTIFICATE OF SERVICE

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