

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No. IPR2025-00228
U.S. Patent No. 11,101,276

**DECLARATION OF SANJAY BANERJEE, PH.D.,
IN SUPPORT OF PETITIONER'S REPLY BRIEF**

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I, Sanjay Banerjee, hereby declare as follows:

I. INTRODUCTION

1. My name is Sanjay Banerjee. I have been retained on behalf of Petitioner Micron Technology, Inc. (“Petitioner” or “Micron”) as an independent consultant in this proceeding before the United States Patent and Trademark Office (“USPTO”).

2. I have already submitted a declaration in this proceeding concerning technical subject matter relevant to the above-captioned *inter partes* review petition (“Petition”) of U.S. Patent No. 11,101,276 (Ex. 1001, the “’276 Patent”). My “Initial Declaration” is Ex. 1003.

3. A summary of my education, professional experience, and other qualifications is included within Paragraphs 5 to 14 in Ex. 1003 and in my CV (Ex. 1004).

4. I have been asked to review the Patent Trial and Appeal Board’s (the “Board’s”) Institution Decision, issued on July 25, 2025. I have also been asked to review Yangtze Memory Technologies Co., Ltd.’s (“Patent Owner” or “YMTC”) Patent Owner Response (“POR”), the accompanying exhibits, including the supporting Declaration of Stephen Campbell (Ex. 2019), the transcript from Dr. Campbell’s deposition, taken on January 16, 2026 (Ex. 1086), and the transcript from his deposition in the IPR proceeding for the related U.S. Patent No. 10,672,711,

taken on November 7, 2025 (Ex. 1091), and to provide my opinions on certain statements and arguments presented in YMTC's materials.

5. In this "Reply Declaration," I do not address every argument or opinion that appears in YMTC's Patent Owner Response or Dr. Campbell's declaration with which I disagree. Instead, I focus on arguments and opinions that seem likely to be relevant to the determination of obviousness. For this reason, the opinions that I express in this Reply Declaration are not exhaustive of my opinions regarding the unpatentability of claims 1-18 of the '276 Patent. Importantly, the fact that I do not address a particular point or argument should not be understood to indicate an agreement or concession on my part. And, unless I state otherwise, the opinions I provide below apply equally to both YMTC's Patent Owner Response and Dr. Campbell's declaration, such that any opinions concerning the Patent Owner Response apply to the corresponding section of Dr. Campbell's declaration, and vice versa.

6. I have confined my analysis to the materials that were available when I prepared this Reply Declaration. I reserve the right to supplement my Initial Declaration and this Reply Declaration in response to additional evidence that may come to light.

II. COMPENSATION

7. I am being compensated for my work in this matter at an hourly rate of \$650.00 for consulting services. My compensation is not based on the outcome of this matter or on the substance of my opinions.

III. MATERIALS CONSIDERED

8. In preparing this Reply Declaration, I considered the following materials, along with any other materials referenced in the body of my Initial Declaration and this Reply Declaration:

EXHIBIT NO.	DESCRIPTION
1001	U.S. Patent No. 11,101,276 to Zhu et al. (“the ’276 patent”)
1002	File History of U.S. Patent No. 11,101,276 (“the ’276 FH”)
1003	Declaration of Dr. Sanjay Banerjee (“Banerjee”)
1004	Intentionally left blank
1005	U.S. Patent Publication No. 2012/0070944A1 (“Kim”)
1006	U.S. Patent Publication No. 2019/0067306A1 (“Fang”)
1007	U.S. Patent Publication No. 2017/0062470A1 (“Han”)
1008	U.S. Patent Publication No. 2017/0294384A1 (“Chen”)
1009	U.S. Patent Publication No. 2018/0330985A1 (“Yu”)
1010	Aritome, “NAND Flash Memory Technologies” (2016)
1011	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017

EXHIBIT NO.	DESCRIPTION
1012	Micheloni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)
1013	U.S. Patent Publication No. 2017/0117222A1 to Kim et al.
1014	Chang and Sze, “ULSI Technology” (1996)
1015	Orlowski et al., <i>Si, SiGe, Ge, and III-V Semiconductor Nanomembranes and Nanowires Enabled by SiGe Epitaxy</i> , ECS Transactions Vo. 33, No. 6 (2010), 777-89
1016	U.S. Patent No. 9,728,547 (“Ohsaki”)
1017	U.S. Patent Publication No. 2017/0148677A1 (“Shin”)
1018	U.S. Patent No. 10,672,711 to Zhu et al. (“the ’711 patent”)
1019	Excerpt from YMTC’s Exemplary Infringement Claim Chart for U.S. Patent No. 11,101,276 (Ex. H-1 to Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024) (“YMTC2 Infringement Contentions, Ex. H-1”) [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]
1020	Korean Patent Publication No. KR10-2013-0015120 (“Lee”) with machine translation
1021	Wolf S., et al., “Silicon Processing for the VLSI Era, Volume 1 – Process Technology, Chapter 15, Multilevel Interconnects for ULSI” (2nd Ed. 2000)
1022	CN Patent Publication No. 107658309 A with certified translation (Priority application to the ’276 patent)
1023	Wang, et al., “Low DC-Bias Silicon Nitride Anisotropic Etching,” <i>Journal of Vacuum Science & Technology B</i> , Vol. 33, Issue 6 (Sept. 10, 2015)
1024	U.S. Patent Publication No. 2014/0284661A1 (“Williams”)

EXHIBIT NO.	DESCRIPTION
1025	Shamiryan D., et al., “Selective Removal of High-K Gate Dielectrics,” Chemical Engineering Communications (2009)
1026	Morel, et al., “Tungsten metal gate etching in Cl ₂ /O ₂ inductively coupled high density plasmas,” Journal of Vacuum Science and Technology B (Nov. 3, 2008)
1027	Kim, et al., “Dry Etching of High-k Dielectric Thin Films in HBr/Ar Plasma,” Journal of the Korean Physical Society, Vol. 54, No. 2, pp. 934-38 (February 2009)
1028	U.S. Patent No. 10,297,543 to Park et al.
1029-1085	Intentionally left blank
1086	Transcript of January 16, 2026 deposition of Stephen Campbell, Ph.D.
1087	Intentionally left blank
1088	Korean Patent No. 10-2015-0051841 to Park et al. (“Park”) including certified translation
1089	U.S. Patent Publication No. 2013/0228837A1 to Sukekawa et al. (“Sukekawa”)
1090	Dhungana et al., <i>Combinatorial Survey of Fluorinated Plasma Etching in the Silicon-Oxygen-Carbon-Nitrogen-Hydrogen System</i> , Journal of Vacuum Science and Technology A (2016), 061302-1–18
1091	Transcript of November 7, 2025 deposition of Stephen Campbell, Ph.D., <i>Micron Tech., Inc. v. Yangtze Memory Techs. Co., Ltd.</i> , IPR2025-00117 (Patent No. 10,672,711)
1092	Reyes-Betanzo et al., <i>Silicon nitride etching in high- and low-density plasmas using SF₆/O₂/N₂ mixtures</i> , Journal of Vacuum Science and Technology A21, 461–469 (2003)

9. As stated above, I also reviewed and considered the Board's Institution Decision (Paper 22), issued on July 25, 2025; YMTC's Patent Owner Response (Paper 31), filed on October 27, 2025; and the exhibits that YMTC submitted with its Patent Owner Response, including Dr. Campbell's declaration (Ex. 2019).

IV. UNDERSTANDING OF THE GOVERNING LAW

10. I am not an attorney but have been instructed on and applied the law as described in my Initial Declaration.

V. CLAIM CONSTRUCTION

11. In my Initial Declaration, I opined that "all terms of the '276 Patent's claims may be understood based on their plain and ordinary meaning." Ex. 1003 ¶ 62. I further explained that "the plain and ordinary meaning of 'high-k dielectric' as of the priority date of the '276 Patent is a dielectric whose dielectric constant is higher than that of silicon nitride." Dr. Campbell does not dispute that.

12. Patent Owner advances a claim construction that requires the step of claim limitation [1.E] ("forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer") to "not penetrate through the etch-stop layer prior to" the step of claim limitation [1.F] ("etching the exposed portions of the etch-stop layer..."). POR, 13. My opinion is consistent with that claim construction. Ex. 1003 ¶¶ 103-104. In fact, etching through the insulating layer, the etch-stop layer, and any layers below the etch-stop layer and above the gate

electrodes “involves choosing relative etch selectivities of the etch-stop layer, the insulating layer[], the first high-k dielectric layer [*i.e.*, an intermediate layer], and the conductive layers.” *Id.* ¶ 104. In other words, etch chemistry (corresponding to an etch selectivity) needs to be changed to penetrate the etch-stop layer because the etch chemistry penetrating the insulating layer does not effectively etch the etch-stop layer. This is because the etch-stop layer is designed to slow down the etch through the insulating layer to protect the underlying structure. Patent Owner agrees, stating that saying “the etch-stop layer is selective to the insulating layer ... does nothing more than describe why an etch-stop layer is an etch-stop layer.” POR, 53; Ex. 2019 ¶ 86 (“That is simply a description of how an etch-stop layer functions.”).

VI. GROUND 1

A. Kim Renders Obvious “Disposing a Sacrificial Layer over a Dielectric Layer”

1. Kim’s gate-stack-on-top disclosure applies to Figures 17A–22B

a. The inverted order is a suitable alternative, which provides motivation

13. In my Initial Declaration, I explained that while Kim illustrates a staircase structure with a dielectric layer at the top of each step, Kim also discloses the opposite order, *i.e.*, a staircase structure with a gate stack at the top of each step.

Ex. 1003 ¶ 70.¹ I also explained that, although the disclosure of the opposite order is made in the context of other embodiments, a POSITA would have understood that it was also applicable to the Figure 17A-22B embodiment. *Id.* ¶ 81. I further cited additional references to explain that both configurations were well known in the art. *Id.* ¶¶ 82-86. In particular, prior art reference Chen discloses both configurations side-by-side with only short descriptions. *Id.* ¶ 84 (citing Ex. 1008, Figs. 7A-7B, [0044]-[0046]). Kim's disclosure, along with these other references, demonstrates that both layer orders were well known and routine to implement.

14. The gate-layer-on-top and the dielectric-layer-on-top configurations were common, well understood, and predictable variations of a 3D staircase structure, which was created to meet the demand for ever increasing memory sizes. Kim, [0003]–[0004]; Chen, [0002]–[0003]; Yu, [0002]. In both, the alternating layers perform their typical functions: the gate layers serve as word lines connecting the vertical conductive structures to the gate terminals of memory cells, and the dielectric layers provide insulation and structural support between the gate layers. The order of the alternating layers of each step of the staircase does not change or impact their function in a meaningful way, as Dr. Campbell agrees. Ex. 1086, 28:16-

¹ Dr. Campbell does not dispute that Kim discloses the opposite order. Ex. 2019 ¶ 40; Ex. 1086, 108:12-18.

24. Selecting one of the two orders was a simple design choice, as I testified in my deposition in the IPR proceeding for the related U.S. Patent No. 10,672,711 (the “711 Patent”). Ex. 2021, 35:12-36:1. The two orders are functionally equivalent, predictable variations of each other. Both make good staircase designs. Each provides alternating dielectric and conductive layers, and in both orderings, the staircase contacts extend into or on respective conductive layers, thereby providing contacts to the word lines in a 3D NAND design. Either one may substitute for the other. Because both configurations were routinely used and well understood, Kim simply mentions the opposite gate-stack-on-top configuration in passing.

15. Chen illustrates this conclusion well. Chen’s Figures 9A-11B illustrate a manufacturing process for a 3D memory staircase comprising an etch-stop layer and conductive structures. Chen, Figs. 9A-11B, [0018]. The two side-by-side figures in each pair (*e.g.*, 9A and 9B, 10A and 10B) respectively show a dielectric-layer-on-top configuration and a gate-layer-on-top configuration. Figures 9A and 9B show the formation of the steps of the staircase. The two opposite orders are simply described together in one short paragraph. *Id.*, [0055]. Figures 10A and 10B show the formation of the etch-stop layer on top of the staircase. Again, the two figures are described together in one short paragraph. *Id.*, [0056]. Figures 11A and 11B show the formation of the dielectric layer and the conductive structures above the staircase. Again, the two figures are described together in one short paragraph.

Id., [0057]. Chen simply does not distinguish these two opposite orders in its descriptions. Chen shows that these two opposite orders are simply a design choice, a suitable substitute for each other, and do not make a difference for purposes of constructing a 3D memory staircase. Importantly, Chen does not discuss differentiating implementation details between the two orders, because these implementation details were well known to a POSITA.

16. Dr. Campbell disagrees with my opinion that a POSITA would have understood Kim's description of the closely related Figures 5A-14B embodiment applies to the Figures 17A-22B embodiment. Ex. 2019 ¶ 39. But he agrees that the two embodiments "us[e] the same reference numbers for the same elements." *Id.* And he only identifies an etch-stop layer and a barrier layer as the difference between the two embodiments. *Id.* ¶ 42. I agree that those are the only relevant differences between them. The fact that all other relevant components are identical between the two embodiments supports my opinion that a POSITA would have understood Kim's description of the closely related Figures 5A-14B embodiment applies to the Figures 17A-22B embodiment. Ex. 1003 ¶ 81. Dr. Campbell also mischaracterizes the proposed layer order reversal as "mixing and matching of elements across embodiments." Ex. 2019 ¶ 39. There is no such mixing and matching.

17. Similarly, Dr. Campbell opines that the Figures 5A-14B embodiment lacks elements disclosed only in the Figure 17A-22B embodiment, such that the

layer order reversal would be “complex and costly.” *Id.* ¶ 42. But as Dr. Campbell himself agreed, all that is required is changing the order in which the alternating layers are deposited. Ex. 1086, 42:24-43:10; Ex. 1091, 92:5-93:5. The only two elements that Dr. Campbell identified as missing from the Figures 5A-14B embodiment are an etch-stop layer and a barrier layer, which are deposited **after** the staircase with the alternating layers is formed and therefore do not affect the staircase formation. Again, Chen’s side-by-side depiction of both layer orders with an etch-stop layer and a barrier layer, the elements that Dr. Campbell alleges would add complexity and cost, disproves Dr. Campbell’s conclusion. The alternating layers in the reversed order provide the same, predictable functionality as explained above. The reversal requires some additional changes such as shortening the vertical contact holes. But those are changes well within a POSITA’s skill and knowledge. As I testified, even my undergrad students could have made such changes. Ex. 2021, 48:2-19, 73:12-74:5.

18. Dr. Campbell argues that Kim’s disclosure regarding the etch-stop coverage should be understood to limit its Figures 17A-22B embodiment to a gate-stack-on-bottom ordering. Ex. 2019 ¶ 41. That is incorrect. The description that Dr. Campbell relies on is describing Kim’s **illustrated** gate-stack-on-bottom Figures 17A-22B embodiment. Kim, [0185]-[0187]. So it is expected that the description fits the gate-stack-on-bottom configuration. But that description does not teach or

suggest a gate-stack-on-top embodiment is prohibited. Contrary to Dr. Campbell's statement, the description does not say the etch-stop layer "covers *only*" the sidewalls of the sacrificial layers. Ex. 2019 ¶ 41.² Rather, the description is permissive rather than restrictive. Kim, [0185] ("The etch stop layer 125 *may* cover top surfaces of the contact pads 123 in the cell array region CAR and end portions of the sacrificial layers SC1 to SC8 in the word line contact region WCTR."); *id.*, [0187] ("***In some embodiments***, the first stop layer 125a may cover sidewalls of the sacrificial layers SC1 to SC8 in the contact region WCTR."). If Kim had made a point to describe the gate-stack-on-top configuration (which Kim evidently didn't think necessary because a POSITA would have been able to infer it), the description would have fit the gate-stack-on-top configuration.

b. Inverting the layers was routine, which provides a reasonable expectation of success

19. Dr. Campbell opined that a POSITA would not have had a reasonable expectation of success in reversing the layer order (which he calls "modifications") due to technical problems. Ex. 2019 ¶ 44. But the record does not support his opinion.

² All emphases are added and internal quotation marks and citations omitted unless otherwise noted.

20. At the outset, it may be helpful to clarify that the so-called “modifications” refers to fabricating a gate-stack-on-top staircase instead of a dielectric-layer-on-top staircase starting from the bottom, not “modifying” a dielectric-layer-on-top staircase that has already been fabricated. As I discussed above, for example, Chen demonstrates each option by **starting** with a staircase with each ordering. Thus, using “modifications” to refer to the implementation or embodiments is misleading.³ As explained in the previous section, these two configurations are simply predictable variations of a staircase structure. The “extensive modifications” that Dr. Campbell referred to are merely obvious adjustments to the structure or process that follow from putting the gate stack instead

³ Dr. Campbell also describes implementing the alternative order as “**replacing** a functional gate stack with insulating material and vice versa.” Ex. 2019 ¶ 50. That is similarly a misleading description for the same reason. Unlike replacing sacrificial layers with gate-stack layers, there is no replacement of one layer with the other layer to invert the order of the alternating layers. It is simply structuring the staircase in the opposite order starting from the substrate. Indeed, Dr. Campbell testified that forming a gate-stack-on-top staircase simply means “start[ing] with the insulator rather than the sacrificial layer” and proceeding through the steps. Ex. 1091, 92:5-93:18.

of the dielectric layer on the top of each step. Ex. 2019 ¶ 50. These adjustments represent differences between the structure in the two configurations or the process used to fabricate them. Both layer-ordering configurations and their design and manufacturing were well known. Chen, for example, shows that a POSITA would have known how to build a staircase using either layer ordering from the substrate up by omitting differentiating implementation details between the two orders.

21. The '276 Patent similarly omits many details of its implementation, an observation with which Dr. Campbell agrees. When asked about the numerous etch-stop thickness ranges disclosed by the parent '711 Patent (which shares an identical specification with the '276 Patent), and how any particular thickness or thickness range is appropriate for the numerous combinations of materials for the sacrificial layer and the etch-stop layer, he first acknowledged that the '711 Patent does not identify any particular thickness range as suitable for a particular material combination, and that a POSITA would have to experiment to make it work. Ex. 1091, 105:23-107:6. But he further testified that “**every time** you do **any** deposition and etching, you have to” “experiment to make [it] work.” *Id.*, 106:23–107:10. “[A] POSITA would certainly know that’s what you have to do. This is not unique to this process.” *Id.* In other words, given the disclosure of the '276 Patent (or Chen, for example), a POSITA would have to run routine experimentation to implement any disclosed embodiment, using implementation details known to a POSITA and

therefore not disclosed in the patent. *Id.*, 110:14-111:5. Such experimentation includes details of etching, for example, such as the “kind of machine” or the type of plasma to use, which is for the engineers to “figure out.” *Id.*, 58:20-59:11.

22. Implementing either layer ordering was well within the knowledge and skill of a POSITA. As I testified, even my undergraduate students would have known how to implement either order. Ex. 2021, 72:4-74:9. One straightforward method of forming a staircase structure with the opposite layer order is simply to reverse the order of depositing a sacrificial layer (which will be replaced by a gate stack) and a dielectric layer. For example, depositing a dielectric layer first on the substrate, followed by a sacrificial layer on top, and repeating in the same order for the desired number of times, can form a gate-stack-on-top staircase when the steps are completed. To form a dielectric-layer-on-top staircase, one can deposit a sacrificial layer first on the substrate, followed by a dielectric layer on top, and repeat in the same order for the desired number of times. Dr. Campbell agrees that this simple change in the order of deposition will change the layer order of the staircase structure. Ex. 1091, 93:12-18, 95:13-25.

23. Even if layer ordering reversal involves some “modifications” in the normal sense of that word, because a POSITA would have known what is involved in building a staircase in either layer ordering from the substrate up, in the scenario where a POSITA starts with a dielectric-layer-on-top design and seeks to “modify”

it to a gate-stack-on-top design (an artificial scenario that Patent Owner and Dr. Campbell seem to construct), a POSITA would also know how to adjust the structure and the process to achieve the “modifications.” In fact, Dr. Campbell testified that, after implementing a gate-stack-on-bottom embodiment, implementing a gate-stack-on-top embodiment “is not as intensive.” Ex. 1091, 111:1-16. In other words, given Kim’s disclosure of gate-stack-on-bottom embodiments, it would have been easier and obvious to implement a gate-stack-on-top embodiment.

24. While the high-level changes involved in reversing the layer order that I briefly describe would involve changes in implementation details, such as deposition or etch parameters, such changes, in the words of Dr. Campbell, “[are] not unique to this process.” Ex. 1091, 106:23–107:10. “[A] POSITA would certainly know that’s what you have to do.” *Id.*

25. Next, I explain how the record does not support Dr. Campbell’s specific opinions in his declaration.

26. Initially, Dr. Campbell cites changes to the process flows that would result from the layer order reversal. Ex. 2019 ¶ 44. But those changes do not make the alleged invention of the ’276 patent nonobvious. None of the references nor the ’276 patent discuss such process flows, as Dr. Campbell himself acknowledged. Ex. 1086, 124:10-13. That confirms my opinion that a POSITA would have known how to change whatever process flows might need to be changed to implement the

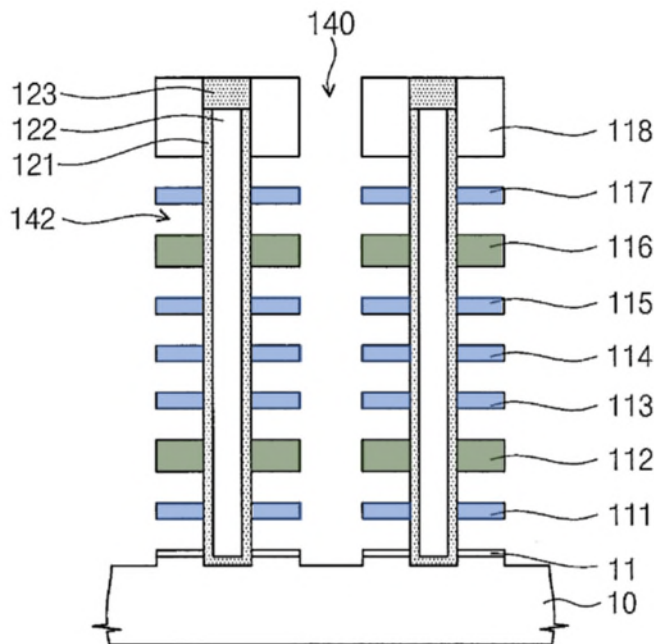
reversed layer order, and therefore the patents need not discuss it. In fact, Dr. Campbell testified that the process flow such as etch recipes cannot be disclosed in patents due to confidentiality provisions from equipment suppliers like Applied Materials. *Id.*, 80:22-81:7. Instead, a POSITA would have known to simply tweak the process flow provided by equipment suppliers. *Id.*, 123:21-124:9. As Dr. Campbell also testified, “**every time** you do **any** deposition and etching, you have to” “experiment to make [it] work.” Ex. 1091, 106:23–107:10. “[A] POSITA would certainly know that’s what you have to do. This is not unique to this process.” *Id.*

27. Dr. Campbell also seems to exaggerate the effort and the impact of layer ordering reversal, which in any event are not relevant to the factors determining obviousness as I understand them. See Ex. 2019 ¶ 44. As Dr. Campbell himself testified, with the knowledge for the gate-stack-on-bottom embodiment (like Chen’s Figure 7A or Kim’s Figure 22A), implementing the gate-stack-on-top embodiment does not involve “as much work.” Ex. 1086, 136:13-137:8. So the alleged delay to market and money loss are not bona fide concerns. In any event, I understand that the obviousness analysis is based on specific factors. See Ex. 1003 ¶ 25. And the amount of time and money it might take to go from the prior art to the alleged invention has no bearing on those factors. Semiconductor fabrication, by its very

nature, is a labor- and capital-intensive undertaking. That doesn't make everything in the field nonobvious.⁴

28. Next, Dr. Campbell opines that the layer order reversal creates step-shaped gate stacks, which allegedly would be problematic for several reasons. Ex. 2019 ¶ 45. But Dr. Campbell's opinion is based on an incomplete reading of Kim. With respect to both the Figures 5A-14B and Figures 17A-22B embodiments, Kim discloses thicker insulating layers. This is shown in Figures 12B and 20B, which are identical:

⁴ Dr. Campbell appears mistaken about the starting point of the proposed "modification." He references "combining[/combine] these references." Ex. 2019 ¶ 44. But the layer ordering reversal is based on Kim alone. There are no multiple references to combine.



Kim, Fig. 20B. Kim discloses that the thicker insulating layers are an optional feature. *Id.*, [0232] (“Some of the insulating layers (e.g., 112 and 117) **may** be thicker than other insulating layers (e.g., 111, 113 to 116, and 118).”); *id.*, [0067] (similar).⁵ Dr. Campbell was not aware that this is an optional feature and opined as though it were required. Ex. 1086, 122:4-7. So his opinion is based on the wrong starting point. A POSITA would have understood to exclude this optional feature when reversing the layer ordering and to not create step-shaped gate stacks.

29. But even if the thicker insulating layers were required, as Dr. Campbell appears to have mistakenly thought, Kim’s disclosure of layer order reversal in the

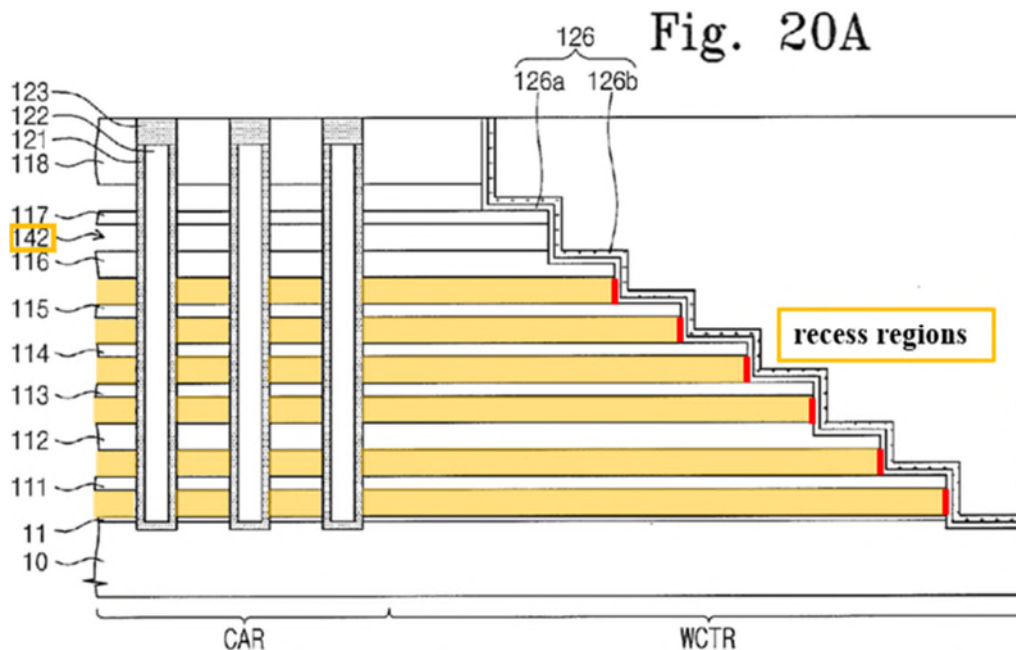
⁵ The figures show layers 112 and 116 to be thicker while the text identifies layers 112 and 117. That discrepancy is irrelevant to the issue at hand.

same Figures 5A-14B embodiment with the feature of thicker insulating layers (shown in Figure 12B) demonstrates that a POSITA would have been able to implement the two features together. A POSITA would have known to adjust the thickness of the step-shaped gate stacks to not encounter the problems Dr. Campbell described, which are due to the gate stack being “too thin.” Ex. 2019, ¶ 45. Dr. Campbell contends that a POSITA would know how to “adjust the thickness of the protective high-k dielectric layers as needed.” *Id.* ¶ 92. The same is true of the sacrificial and gate-stack layers.

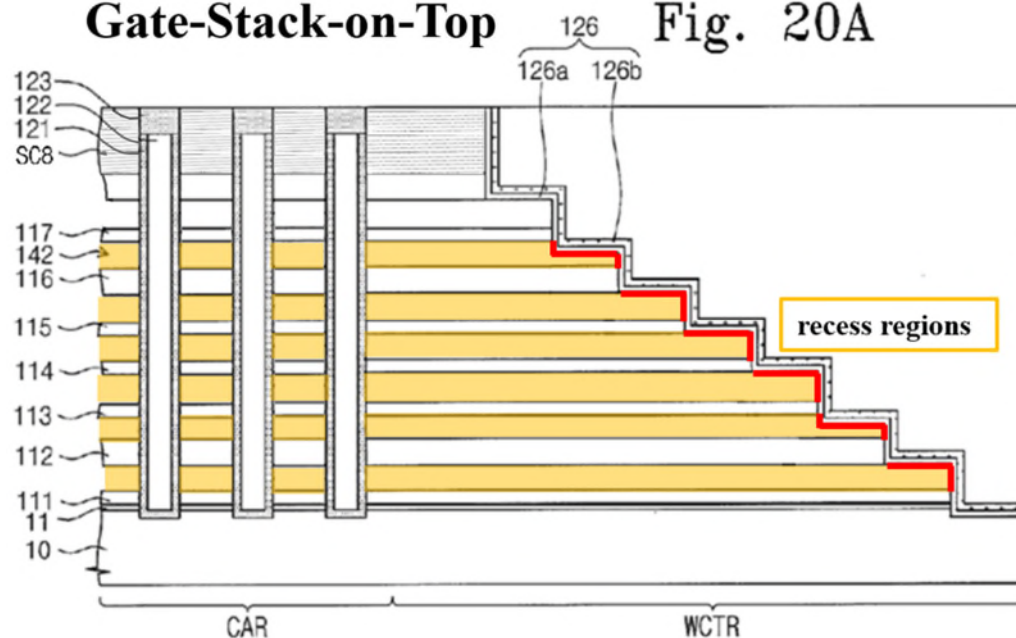
30. Next, Dr. Campbell opines that the layer ordering reversal shortens the contact plugs and is “no trivial change to Kim’s processes and devices.” Ex. 2019, ¶ 46. The record contradicts that as well. The word line contacts have different depths (or heights) between the two layer orderings because the word line contacts need to reach their corresponding gate conductive layers, which occupy a different layer of the steps in the two orderings. The shortened contact plugs are merely one of the interrelated changes resulting from reversing the layer ordering. It would occur when reversing the order in Kim’s Figures 5A-14B embodiment as well. But Kim doesn’t explain how that can be achieved because a POSITA would have known how to implement it. For example, the differences in depths can be easily accomplished by adjusting the etching and deposition time as required, resulting in holes and conductive structures of the appropriate depths. The adjustment to the

etch time may simply be achieved by knowing the etch rate and the depth to which the holes are to be etched. Dr. Campbell's testimony supports this understanding. Ex. 1091, 56:15-21 ("Q. How does one determine when to end an etching process - a particular etching step? A. Well, the simplest scenario of sequences of this, the simple one is just to know your etch rate and time it, know the thickness.").

31. Next, Dr. Campbell speculates that reversing the layers "**may**" change the etch selectivity between the sacrificial layers and the insulating layer above such that an etch-stop layer would not be needed. Ex. 2019 ¶ 46. Kim disproves this speculation. At the outset, it's important to understand that, regardless of the layer ordering, the sacrificial layer is in direct contact with the same layer covering the staircase, just to a different extent as shown below in red:



Gate-Stack-on-Top **Fig. 20A**



Kim, Fig. 20A (original and modified). As shown in these figures, the recess regions created by the removal of the sacrificial layers expose the first stop layer 126a in both layer orderings, just to a different extent. Thus, in either order, the first stop layer 126a still must be formed of a material different from that of the sacrificial

layer so that the first stop layer 126a is not etched at the exposed surfaces when the sacrificial layers are removed. *Id.*, [0187] (“a first stop layer 125a having an etch selectivity with respect to the sacrificial layers SC1 to SC8....”). The same is true for the Figures 5A-14B embodiment without the etch-stop layers, except that it is the materials of the interlayer dielectric and the sacrificial layer that are relevant because they are the two layers in direct contact. *Id.*, [0095] (“The interlayer dielectric 130 may be formed of a material having an etch selectivity with respect to the sacrificial layers SC1 to SC8 during a subsequent process of removing the sacrificial layers SC1 to SC8....”). And Kim’s disclosure allows different materials (and thus different etch selectivities) for the relevant layers: the first stop layer may be formed of silicon oxide (Ex. 1003 ¶ 133), the sacrificial layers may be formed of a variety of materials such as silicon nitride, not limited to silicon oxide (Kim, [0064]), and the interlayer dielectric may be formed of a variety of materials not limited to silicon nitride (*id.*, [0098]). In short, contrary to Dr. Campbell’s speculation, the etch selectivity between the sacrificial layers SC1-SC8 and the insulating layer above requires that the two layers be made from different materials regardless of the order of the layers, Kim already teaches choosing the proper selectivity for the relevant layers with or without an etch stop, and Kim discloses a range of materials to enable the proper selectivity with or without an etch stop. Or consider: the fact that Kim teaches implementing the Figures 5A-14B embodiment

in both the sacrificial-layer-on-top and sacrificial-layer-on-bottom orders shows that the layer ordering is independent of the etch-stop layers. The preceding discussion explains why.

2. Kim has no missing limitations

32. As a preliminary matter, I note that Patent Owner alleges Kim to be “missing” the claim limitation “disposing a sacrificial layer over a dielectric layer.” POR, 29. Patent Owner also alleges that Petitioner may argue that “it relied on background references such as Chen, Yu, Ohsaki, and Shin” “to supply [that] missing limitation.” *Id.*, 26 n.5.⁶ By referring to Chen, Yu, Ohsaki, and Shin, Patent Owner indicates that it uses “missing limitation” to refer to a feature that is missing from the reference the Ground expressly includes, *i.e.*, Kim. I disagree that the sacrificial-layer-on-top limitation is missing from Kim, as explained in my Initial Declaration and in the section above. Further, Dr. Campbell does not dispute that Kim discloses layer ordering reversal. Ex. 2019 ¶¶ 40-41; Ex. 1086, 108:9-18. More generally, “missing” limitation only appears once in Dr. Campbell’s declaration—in the section on his understanding of the law of obviousness. Ex. 2019, ¶ 19. Thus,

⁶ This is not the case. As my Initial Declaration shows, Chen, Yu, Ohsaki, and Shin show that a gate-layer-on-top configuration was common. Ex. 1003 ¶¶ 84-86.

Patent Owner's argument that the gate-stack-on-top limitation is missing from Kim appears to be an erroneous attorney argument.

33. Dr. Campbell cites several exhibits to support his opinion that 3D NAND is a complex technology. Ex. 2019 ¶¶ 48-49.⁷ But this opinion is flawed for two reasons. First, Dr. Campbell ignored the entirety of his own evidence. For example, the author of four exhibits Dr. Campbell relied on, Mark LaPedus, commented that “[m]any 3D NAND companies use the same process steps. The general fab techniques are known.” Ex. 2028, 8. Mr. LaPedus referred to “a 48-layer alternating stack deposition process” as “[g]enerally” “mature.” Ex. 2027, 6. Mr. LaPedus further quoted a TechInsights analyst that “[t]he 32-, 48- and 64-layer

⁷ I note that almost all of the evidence Dr. Campbell cited in his declaration is for this opinion that 3D NAND is a complex technology. Other cites typically do not support the proposition he was making but rather merely supply a context. The cite to Chen in paragraph 85 is an example. When not used to supply a context, Dr. Campbell's cites to my testimony distort its meaning. For example, Dr. Campbell cites my testimony that “details matter” and “specifics matter” several times without citing the context of my testimony. Ex. 2019, ¶¶ 50, 63, 109. But as my Initial Declaration and this Declaration make clear, those details and specifics are not relevant to the obviousness analysis at issue here.

devices use conventional etching tools for the HAR channel hole.” *Id.*, 7.⁸ “HAR” stands for high aspect ratio. Etching contact holes at issue here involves high aspect ratio holes. Ex. 1086, 62:16-19. So, according to TechInsights, conventional etching tools were available for etching the contact holes by the time of the ’276 Patent. Second, even if 3D NAND was a complex technology, that doesn’t mean everything associated with 3D NAND was nonobvious. For example, certainly everything disclosed in Kim, Chen, Yu, Ohsaki, and Shin was obvious by the time of the ’276 Patent.

34. Dr. Campbell opined that layer ordering reversal is a complex process. Ex. 2019 ¶¶ 50-53. Once again, Kim, Park, and Chen all contradict that opinion. Dr. Campbell’s reasoning is incorrect as I explain below.

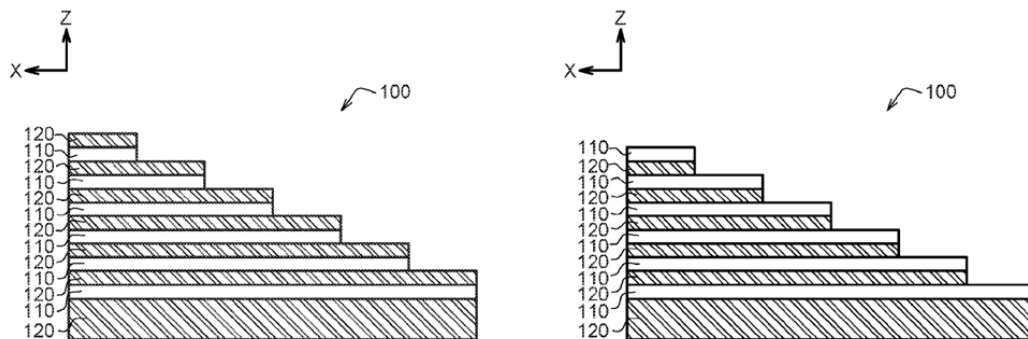
35. Dr. Campbell includes “etch processes” such as “reoptimiz[ation]” of etch parameters in the alleged “extensive modifications.” Ex. 2019 ¶¶ 50-52. But etching contact holes in the gate-layer-on-top configuration is actually simpler

⁸ TechInsights calls itself “The Trusted Source for Semiconductor Insights.” <https://www.techinsights.com/> (last visited January 23, 2026). Patent Owner relied on TechInsights for reverse engineering reports used in its infringement contentions against Petitioner. See Ex. 1029 (“TI 232L Report,” where “TI” is short for TechInsights).

because it does not require one more etch step to etch through the dielectric layer at the top of each step in the dielectric-layer-on-top configuration. Further, as Dr. Campbell himself testified, making adjustments to etch processes was routine to a POSITA. Ex. 1091, 106:23-107:10 (“**every time** you do **any** deposition and etching, you have to” “experiment to make [it] work.”). Reoptimization may involve many interacting or interrelated parameters that need to be adjusted to fabricate a staircase of the opposite layer order. But these are knobs that a POSITA would have known how to adjust. Dr. Campbell testified that a POSITA would “tweak[]” the parameters to make the necessary adjustments. Ex. 1086, 123:5-124:9. Moreover, Dr. Campbell testified that the parameters needing reoptimization, “etch chemistry, ... plasma power, bias voltage, chamber pressure, temperature, and etch time” are parameters that none of the patents, including the ’276 Patent, discuss. *Id.*, 78:5-80:21, 83:15-84:4, 122:12-124:13. So if Dr. Campbell were right that such reoptimization were beyond the skill and knowledge of a POSITA, a POSITA would not be able to practice the ’276 Patent or other patents in this proceeding.

36. Dr. Campbell alleges that I made a mistake by including the lower gate insulating layer 11 in the modified Figure 22A because he asserts that the layer is “unnecessary” in the gate-stack-on-top embodiment. Ex. 2019 ¶ 52. I disagree. Dr. Campbell’s premise seems to be that a POSITA would not want to include an unnecessary layer due to the extra process and materials involved. But the lower

gate insulating layer is not useless or unnecessary. Including the lower gate insulating layer 11 in the gate-stack-on-top embodiment is a suitable choice. Dr. Campbell asserts that lower gate insulating layer 11 “prevent[s] ‘electrical crosstalk’ between the lowermost gate and the substrate 10.” *Id.* The level of reduction in electrical crosstalk is determined by, among other things, the distance and the material between the two components involved in the crosstalk, here, based on Dr. Campbell’s description, the distance and the material between the lowermost gate and the substrate. Adding a thin insulating layer between the two increases the distance and the amount of insulating material between them and thus improves the attenuation of crosstalk. Chen confirms this by showing an extra thick insulating layer 120 below the bottommost gate conductive layer 110:



Chen, Figs. 9A-9B.⁹ This extra thick insulating layer reduces crosstalk to a greater extent than a thin insulating layer. Similarly, it is suitable to include that optional

⁹ This bottommost layer is an insulating layer 120. Chen, [0055]. It is not a substrate, which Chen omits from its disclosure. *See generally* Chen.

layer in the gate-stack-on-top embodiment to reduce electrical crosstalk to a greater extent. And whether this layer is present in a gate-stack-on-top embodiment, the staircase functions in a predictable manner.

B. Kim Discloses “Exposing Portions of the Etch-Stop Layer”

37. Dr. Campbell asserts that Kim does not disclose contact hole etching that “penetrate[s] the insulating layer exposing—but not penetrating—portions of the etch-stop layer.” Ex. 2019 ¶ 54. But his own testimony contradicts that assertion.

38. The very name of etch-stop layer indicates that it functions to stop (or, realistically, slow down) etching when etching reaches the layer. This is achieved through an etch selectivity that etches through the relatively thick upper insulating layer (Kim’s interlayer insulating pattern 134) at a high etch rate but etches the etch-stop layer at a low etch rate. Dr. Campbell agrees. Ex. 1086, 56:19-24. Patent Owner recognizes this selectivity is “why an etch-stop layer is an etch-stop layer.” POR, 53; Ex. 2019 ¶ 86 (“That is simply a description of how an etch-stop layer functions.”). Because the etch chemistry used to etch the upper insulating layer etches the etch-stop layer very slowly, after all of the contact holes (or the deepest hole) have penetrated the upper insulating layer, etch chemistry needs to be changed to penetrate the etch-stop layer at a higher etch rate to save fabrication time. Dr. Campbell repeatedly agreed in his deposition. Ex. 1086, 62:10-15 (“Exactly so.”),

67:25-68:8, 69:23-70:3, 70:17-20, 93:24-94:5. Before the etch chemistry is changed, the etch-stop layer is exposed but not penetrated. And Dr. Campbell admits that Kim's etch-stop layer 126b functions as an etch stop, *i.e.*, it slows down the etching of the contact holes. *Id.*, 117:6-10, 131:14-132:12. Putting it together, Dr. Campbell's testimony confirms that Kim's etch-stop layer 126b is exposed but not penetrated after the interlayer insulating pattern 134 is penetrated, and is afterwards penetrated after a change in etch chemistry. As a specific example of changing etch chemistry, Dr. Campbell testified that etching an upper insulating layer is "done in a fluorine plasma." Ex. 1091, 52:5-7. Then "you have to switch to a chlorine plasma" to etch a high-k etch-stop layer.¹⁰ *Id.*, 52:8-10. Before and at the time of the switch, the etch-stop layer is "exposed" and experiences "some erosion." *Id.*, 52:21-25. Thus, Dr. Campbell himself recognized "the need for an extra step in contact hole formation" and contradicts his disagreement with my opinion. Ex. 2019 ¶ 57.

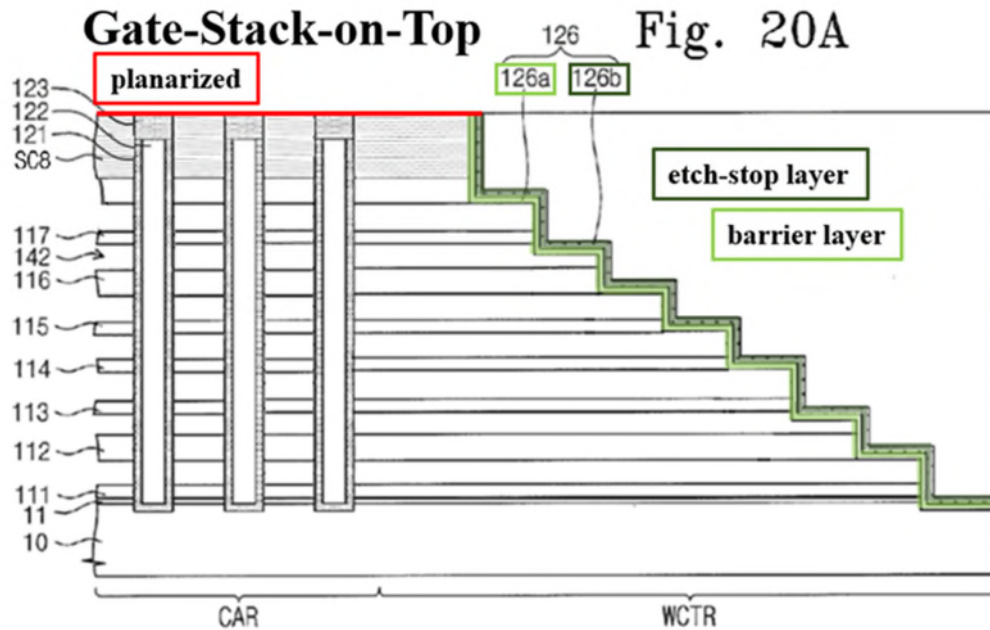
39. Dr. Campbell's self-contradicting opinion that "Kim discloses only openings that penetrate through its etch-stop layer without first forming a plurality

¹⁰ Ground 1 relies on Kim's silicon nitride etch-stop layer, which is not a high-k dielectric. Ex. 1003 ¶ 94. But Dr. Campbell's testimony describes the change in etch chemistry that needs to occur regardless of the etch-stop material.

of openings exposing portions of the etch-stop layer” appears to be based on the fact that Kim does not expressly illustrate such a step. Ex. 2019 ¶ 55 (citing Kim Fig. 22A, which shows the etch-stop layer having been penetrated). But a POSITA would have understood such a step to be part of Kim’s contact hole etching process. As explained in the paragraph above, that is how an etch-stop layer functions. And as Dr. Campbell testified, a POSITA would design an etch-stop layer to function properly. Ex. 1086, 90:11-18.

40. Dr. Campbell asserts that “the etch selectivity between the interlayer dielectric 130 and the etch-stop layer 125” disclosed in Kim is for planarization of the top surface, not for contact hole etch stop. Ex. 2019 ¶¶ 57-60. Once again, his own testimony contradicts his assertion. The planarization is done via a chemical mechanical polishing (“CMP”) process. Dr. Campbell testified that “CMP has no impact on materials underneath the top surface,” including the alternating layers of the staircase. Ex. 1086, 135:18-136:8; Ex. 1091, 61:23-62:2; Ex. 2019 ¶ 74 (“preventing CMP damage on the top of the device”). Therefore, if the etch selectivity between the interlayer dielectric and the etch-stop layer is only for CMP planarization as Dr. Campbell asserts, the etch-stop layer only needs to cover the top surface of the 3D memory staircase because CMP does not damage any materials underneath the surface. In other words, based on Dr. Campbell’s assertion, the

portion of the etch-stop layer that remains after planarization (shown below) is useless.



Kim, Fig. 20A. But that contradicts Dr. Campbell’s opinion that “a POSITA would not want to add the time or material to include a non-functional component.” Ex. 2019 ¶ 46. That also contradicts Dr. Campbell’s testimony that Kim’s etch-stop layer functions as an etch stop for contact hole etching.¹¹ Ex. 1086, 117:6-10, 131:14-132:12.

¹¹ Because Kim’s etch-stop layer functions as an etch stop for contact hole etching, a POSITA would have understood Kim’s disclosure that “[t]he etch stop layer 125 may be formed of a material having an etch selectivity with respect to the interlayer dielectric 130” to include an etch selectivity for contact hole etching. Kim, [0213].

41. If Dr. Campbell were right Kim's etch selectivity is only for planarization, Kim could have limited its etch-stop coverage to only the top surface of the staircase region. Prior art demonstrates this is possible by disclosing etch-stop coverage that is not uniform across the entire staircase. See Ex. 1088, Figs. 11, 13, [0127], [0130] (varying etch-stop coverage on different steps of the staircase).

C. Kim in View of a POSITA's Knowledge Renders Claim 4 Obvious

42. Dr. Campbell disagrees that it would have been obvious to etch the etch-stop layer at a higher etch rate than an etch rate of the conductive layer as required by claim 4. Ex. 2019 ¶ 62. But Dr. Campbell's reasoning does not support his opinion.

43. Dr. Campbell first asserts that "achieving the claimed etch relationships are highly dependent upon the specific materials used." *Id.* But I provided example materials achieving the claimed etch relationships. Ex. 1003 ¶ 108. Dr. Campbell does not refute it.

44. Dr. Campbell next repeats his argument that 3D NAND technology is complex. Ex. 2019 ¶ 62. But as I explain above, his opinion ignores his own evidence and, in any event, that doesn't mean everything associated with 3D NAND technology is nonobvious. *Supra* § VI.A.2. Here, the claimed etch relationship is one of only three possibilities and the only sensible one. Ex. 1003 ¶ 108. Dr. Campbell neither refutes my analysis nor provides his own analysis specific to the

claimed etch relationship. To the contrary, he agrees that punch-through represents a failure of the etch-stop layer. Ex. 1086, 92:12-25, 93:14-19. A POSITA would have known to prevent such a failure by designing the etch-stop layer to function as intended. *See id.*, 90:11-18. That means to allow the etch-stop layer to be penetrated at the intended time but slow down the etch as it approaches the conductive layers.

45. Dr. Campbell then parades a list of etch parameters and materials to allege the complexity due to their interrelationships. Ex. 2019 ¶ 63. But he doesn't explain why the parameters and materials matter to the claimed etch relationship. To the contrary, he testified that these parameters, "etch chemistry, ... plasma power, bias voltage, chamber pressure, temperature, and etch time," are parameters that none of the patents, including the '276 Patent, discuss. Ex. 1086, 78:5-80:21, 123:5-124:13. If these parameters matter to the claimed relationship, a POSITA would have expected the '276 Patent to discuss them. Further, he asserts the proposed modification "can" affect the etch processes. Ex. 2019 ¶ 63. But he doesn't explain how or why such effects would render the claimed etch relationship nonobvious. Further, I explained in my Initial Declaration that the claimed etch relationship would have been even more obvious in the gate-stack-on-top configuration because the gate conductor layers are not protected by an overlying alternating dielectric layer, as they are in the gate-stack-on-bottom configuration. Ex. 1003 ¶ 109. Dr. Campbell did not refute it. On the contrary, both Patent Owner and Dr. Campbell

approvingly cite my testimony that supports this. POR, 24, Ex. 2019 ¶ 81 (both citing Ex. 2021, 48:20-49:8).

D. Kim in View of a POSITA's Knowledge Renders Claim 5 Obvious

46. Dr. Campbell disagrees that it would have been obvious to etch the etch-stop layer at a higher etch rate than an etch rate of the first high-k dielectric layer as required by claim 5. Ex. 2019 ¶ 64. The record does not support Dr. Campbell's opinion.

47. Dr. Campbell first repeats his argument that the etch process is complex with various dependencies. That argument is incorrect as I explain above. *Supra* § VI.C. Furthermore, Dr. Campbell's argument is belied by his contention elsewhere that a high-k dielectric layer having a lower etch rate is readily achievable and would have been obvious to a POSITA. Ex. 2019 ¶ 92 ("For example, the high-k dielectric layer is a different material than the insulating layer above it, and by using a material with a lower etch-rate for the high-k dielectric material, it can provide the protective etch-stop function.").

48. Dr. Campbell argues that a POSITA would not have been motivated to make the first high-k layer effectively another etch stop because Kim already has two etch-stop layers. Ex. 2019 ¶ 66. But Kim's material composition and Dr. Campbell's own testimony of the etch properties contradict his argument. Kim discloses that "the first stop layer 125a may be formed of silicon oxide and the

second stop layer 125b may be formed of silicon nitride.” Kim, [0187]. The first high-k dielectric may comprise aluminum oxide.¹² Ex. 1003 ¶ 99 (citing Kim, [0148], [0151]). Dr. Campbell testified that a fluorine plasma etches well both silicon nitride and silicon oxide.¹³ Ex. 1086, 87:22-88:14.¹⁴ In other words, Kim’s

¹² Kim’s disclosure of the materials contradicts Dr. Campbell’s assertion “to make the etch-stop and first high-k dielectric layers out of the same material[.]” Ex. 2019 ¶ 67.

¹³ Kim discloses a variety of materials that may be used for the interlayer dielectric. Kim, [0098]. The flexibility allows the use of a fluorine plasma to etch the etch-stop layers 125a and 125b.

¹⁴ Incidentally, etching through both the etch-stop layer and the barrier layer using the same etch chemistry would, to use Dr. Campbell’s words, “simplify the manufacturing process by decreasing the etch[]steps and chemistries needed.” Ex. 2019 ¶ 67. Further, this etch chemistry does not impact claim 17, which depends directly from claim 1. As I explained in my Initial Declaration, the flexibility of etch chemistry would have rendered claim 17 obvious. Ex. 1003 ¶ 132. For example, Reyes-Betanzo shows approximately equal etch rates for silicon nitride and silicon oxide under certain etch conditions using a fluorine plasma. Ex. 1092, Figs. 1-2. This is what Dr. Campbell described in his deposition. Reyes-Betanzo also shows

first stop layer 125a (the barrier layer) does not function as an etch stop to the second stop layer 125b (the etch-stop layer) because they both etch well in a fluorine plasma. Additionally, a fluorine plasma does not etch well a high-k dielectric. *Id.*, 88:15-89:1. Therefore, Kim’s etch-stop layer has a higher etching rate than an etching rate of Kim’s first high-k dielectric layer.

49. Lastly, Dr. Campbell argues that the first high-k dielectric serves another purpose, *i.e.*, “to protect the surrounding oxide layer during deposition of the conductive gate layer[, which] can be accomplished whether or not the relative etch-rates match the claimed arrangement.” Ex. 2019 ¶ 68. But whether the high-k dielectric layers may serve another “purpose” during conductive layer formation is irrelevant, because they also function as an etch stop (after the etch-stop layer has been penetrated) with a lower etch rate, as I explain above.

E. Kim in View of a POSITA’s Knowledge Renders Claim 11 Obvious

50. Dr. Campbell first argues that “Kim does not *disclose* ‘planarizing the conductive materials’ as disclosed in claim 11.” Ex. 2019 ¶ 69. But I didn’t opine otherwise. Instead, I opined that Kim “renders obvious” claim 11. Ex. 1003 ¶ 115. Dr. Campbell does not refute my actual opinion.

that silicon oxide has lower etch rates than silicon nitride under other etch conditions.

Id. This satisfies claim 17. Argon may be used in the plasma. *Id.*, 4, 6, 7.

51. Dr. Campbell next argues that the CMP process is complex. Ex. 2019 ¶ 70. His argument is similar to his argument that the etch process is complex and fails for the same reasons. Ex. 1086, 139:4-13 (both involve interrelated parameters); *supra* §§ VI.A.2, VI.C. In fact, he testified that CMP had been widely used in the industry and “is much less complicated than high aspect ratio etching.” Ex. 1086, 139:4-22.

VII. GROUND 2

A. A POSITA Would Have Been Motivated to Combine Kim and Fang with a Reasonable Expectation of Success

52. Dr. Campbell opines that a POSITA would not have been motivated to apply Fang’s etch-stop characteristics and contact-hole etching to Kim with a reasonable expectation of success. Ex. 2019 ¶ 72. But his opinions are not consistent with the record.

1. Etch-Stop Characteristics

a. Punch-through was Kim and Fang’s shared concern

53. First, Dr. Campbell alleges that Kim and Fang’s different focuses would not have provided motivation for a POSITA to apply Fang’s etch-stop disclosures to Kim. Ex. 2019 ¶¶ 73-75. But his allegation mischaracterizes Kim. Dr. Campbell incorrectly characterizes the use of Kim’s etch-stop layer 125 as protecting only the contact pads. *Id.* ¶ 74. If that were the case, the etch-stop layer simply needs to be formed over the top level surface of the staircase because

chemical mechanical polishing (“CMP”) only polishes the top surface and cannot damage materials below the surface, as I explain above. *Supra* § VI.B. It also contradicts Dr. Campbell’s own admission that Kim’s etch-stop layer functions as an etch stop for contact hole etching. *Supra* § VI.B.

54. I explained in my Initial Declaration that because “Kim focuses on the issue of planarizing the interlayer dielectric[,]” “Kim does not state in detail certain aspects of the word line contact region WCTR that were well-known in the art.” Ex. 1003 ¶ 146. Dr. Campbell agrees. Ex. 2019 ¶ 74 (“Based on [Kim’s] focus, a POSITA would not expect Kim to disclose information such as specific etch-stop layer thicknesses.”). That agreement supports applying Fang’s well-known etch-stop characteristics and contact hole etching to Kim.

b. Fang’s carbon doping is optional and immaterial to obviousness

55. Dr. Campbell opines that the difference in the etch-stop materials between Kim and Fang would not have motivated a POSITA to apply Fang’s etch-stop characteristics to Kim. Ex. 2019 ¶ 76. The differences he alleges are based on his assertion that Fang uses carbon-doped silicon nitride, and Kim does not. *Id.* ¶¶ 76-77. But that is not a necessary or material difference.

56. Importantly, Dr. Campbell himself does not distinguish silicon nitride and carbon-doped silicon nitride. He equated Fang’s carbon-doped silicon nitride with Chen’s (undoped) silicon nitride: “Fang’s carbon-doped silicon nitride has an

energy gap of 6.5 eV, and Chen mentions silicon nitride is an acceptable second stop layer (i.e., Fang’s etch-stop layer in Petitioner’s combination).” Ex. 2019 ¶ 107. His testimony is self-contradictory.

57. Next, as a preliminary matter, I note that Dr. Campbell identified only two etch-stop characteristics, etch selectivity and thickness, needed to ensure an etch-stop layer adequately protects the underlying structure. Ex. 1086, 53:2-6; 58:2-7, 90:11-18. This is consistent with his declaration, where he referred to “etch-stop characteristics” across “different materials.” Ex. 2019 ¶ 76. Besides thickness and etch rate, he does not identify any other etch-stop characteristics. *See id.* (“thicknesses or other characteristics”); *id.* ¶ 77 (“etch-stop layer characteristics, including thicknesses”); *id.* ¶ 80 (“etch-stop layer characteristics, including thicknesses”). While he refers to etch chemistry, etchant and ion bombardment, these (and the material) are relevant for their effects on the etch rate. *See id.* ¶ 76 (“The etch chemistry used will affect the rate at which different materials etch. Etch rate can also be impacted by the specific etchant used, along with the flux and energy of the impinging ions, with different materials reacting differently to different etchants and bombardment.”). Dr. Campbell has also testified that thickness and etch rate together achieve the level of etch-stop protection. Ex. 1091, 56:15-21. In other words, thickness may be adjusted based on the etch rate, or vice versa.

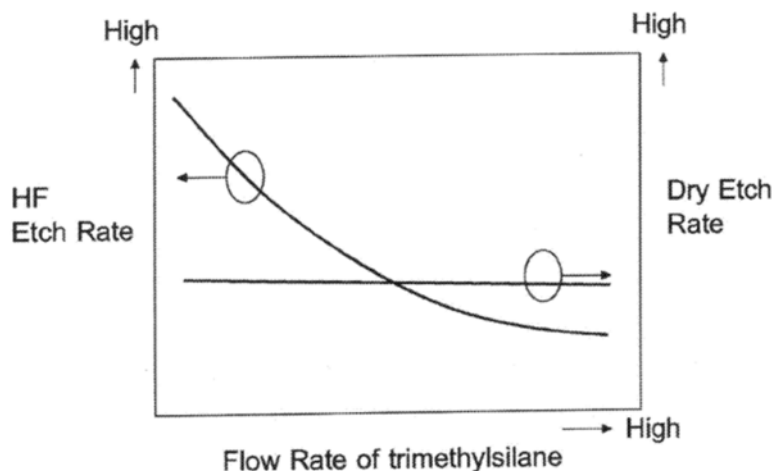
58. Kim and Fang can use the same or similar material for the etch-stop layer. Kim teaches “a second stop layer 125b having an etch selectivity with respect to the insulating layers 111 to 118.” Kim, [0187]. Fang similarly permits “any material that is not substantially removed (e.g., etched) during removal and replacement of the nitride materials of the staircase structure.” Fang, [0020] (numerals omitted). Fang discloses carbon-doped silicon nitride “[b]y way of example only.” *Id.* It discloses a thickness range for the etch-stop layer in the paragraph immediately after that statement. *Id.*, [0020]-[0021]. The specified thickness range makes no reference to carbon doping. *Id.*, [0021]. Accordingly, a POSITA would have understood that the range and other etch-stop characteristics apply to the “any [suitable] material,” not just carbon-doped silicon nitride. *Id.*, [0020]. Fang’s wide thickness range, spanning a factor of 20, confirms it is not specific to “carbon-doped silicon nitride” and makes it appropriate for any suitable materials that can be used for the etch-stop layer in light of the flexibility of etch chemistry and methodology.

59. Dr. Campbell’s assertion about the combination of materials is based on his mistaken understanding that Fang’s thickness is only for carbon-doped silicon nitride. Ex. 2019 ¶ 77. Additionally, the sacrificial layer material is irrelevant to the etch-stop characteristics because of the intervening barrier layer. As Dr. Campbell testified, an etch stop protects the immediately adjacent layer from the etchant (in

the forward direction of etchant flow). Ex. 1091, 23:4-8. Thus, when a barrier layer is present between the sacrificial layer and the etch-stop layer, it is the combination of materials of the barrier layer and the sacrificial layer that matters. *See id.*, 97:2-10. That is why, for the configuration having only one etch-stop layer, Kim discloses etch selectivity between the sacrificial layer and the etch-stop layer. Kim, [0187] (“In other embodiments, the etch stop layer 125 may be a single layer, which is formed of a material having an etch selectivity with respect to the sacrificial layers SC1 to SC8 and the insulating layers 111 to 118.”). But for the configuration with two etch-stop layers, Kim discloses etch selectivity between the sacrificial layer and the first (lower) etch-stop layer 125a, *i.e.*, the barrier layer. *Id.* (“the etch stop layer 125 may include a first stop layer 125a having an etch selectivity with respect to the sacrificial layers SC1 to SC8 and a second stop layer 125b having an etch selectivity with respect to the insulating layers 111 to 118.”).

60. Even if Fang required carbon-doped silicon nitride as Dr. Campbell incorrectly opines, the carbon doping does not affect the etch-stop thickness. Importantly, Dr. Campbell himself takes for granted that Fang’s carbon-doped silicon nitride and Chen’s (undoped) silicon nitride have the same property, energy gap. Ex. 2019 ¶ 107 (“Fang’s carbon-doped silicon nitride has an energy gap of 6.5 eV, and Chen mentions silicon nitride is an acceptable second stop layer (*i.e.*, Fang’s etch-stop layer in Petitioner’s combination).”). Thus, his criticism here rings hollow.

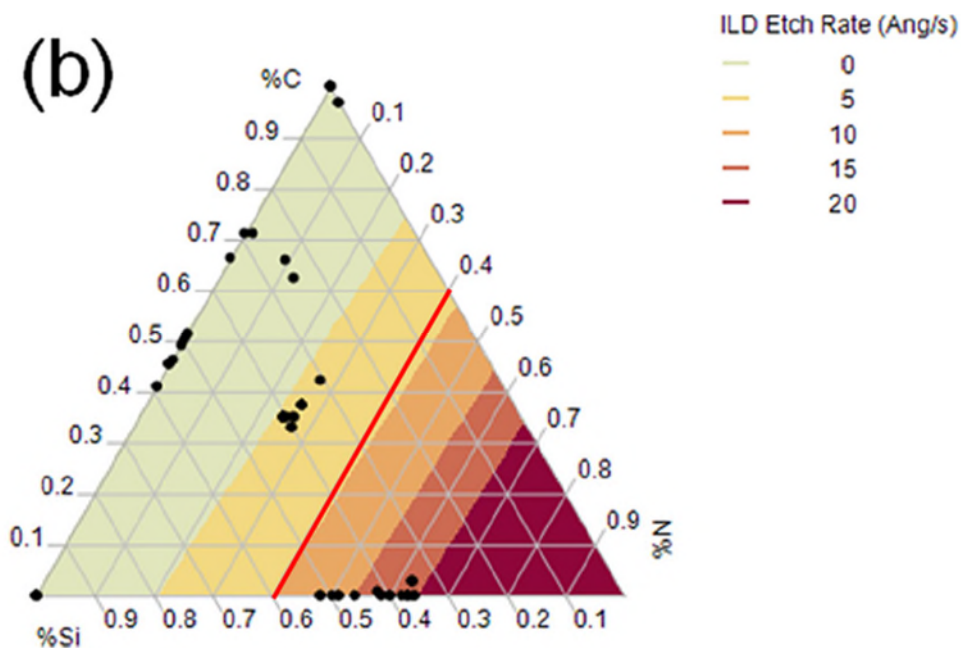
That aside, as he testified, it is the relative etch rates or etch selectivity between the etch-stop layer and the insulator layer above it that matters. Ex. 1091, 23:9-17, 97:2-10. As Fang discloses, the contact holes through the insulator layer are formed using a dry etch chemistry. Fang, [0020]. This is because dry etch can be highly directional (known as “an anisotropic etch process”), which is needed for etching holes with high aspect ratios. *Id.*, [0028]; Kim, [0070], Ex. 1091, 24:2-25:18. Thus, the dry etch rate of the etch-stop layer affects the thickness that is appropriate to protect the staircase from over-etching. But as this figure below shows, the dry etch rate is constant for varying amounts of carbon doping. This figure “is a chart showing the relationships between a carbon-doped amount in a silicon nitride film (the flow rate of trimethylsilane) and etch rates (wet and dry).” Ex. 1089, [0035]. The changing level of carbon doping indicates a nonstoichiometric silicon carbon nitride. *Id.*, [0064]; Fang, [0017] (“The carbon-doped silicon nitride differs from silicon carbon nitride (SiCN), which includes a stoichiometric amount of carbon, such as $\text{Si}_{1.5}\text{C}_{1.5}\text{N}_4$.”).



Ex. 1089, Fig. 19. The figure shows level of carbon doping on the horizontal axis. The dry etch rate is represented by the right vertical axis. The horizontal line across the plot, indicating a constant, shows the dry etch rate of silicon nitride at different levels of carbon doping (the oval with an arrow to the right confirms that the horizontal line represents the dry etch rate). *Id.*, [0074] (“The silicon nitride films have substantially the same dry etch rates, regardless of their ratios of the flow rate of trimethylsilane.”). Thus, even assuming the addition of carbon doping to Fang’s etch-stop layer is mandatory, the thickness of Fang’s etch stop and the corresponding over-etch protection it provides is directly applicable to Kim’s silicon nitride etch-stop because the carbon doping has no impact on the dry etch rate.

61. This phenomenon was well known in the art for silicon-nitride-based materials. For example, Dhungana shows a constant etch rate for ILD (interlayer dielectric above an etch-stop layer) for nonstoichiometric silicon carbon nitride ($\text{SiC}_x\text{N}_y\text{H}$) across different levels of carbon doping, as shown via diagonal lines

connecting constant Si and N levels. The red diagonal line represents 40% nitrogen and 60% silicon, the approximate weight composition of silicon nitride Si_3N_4 :



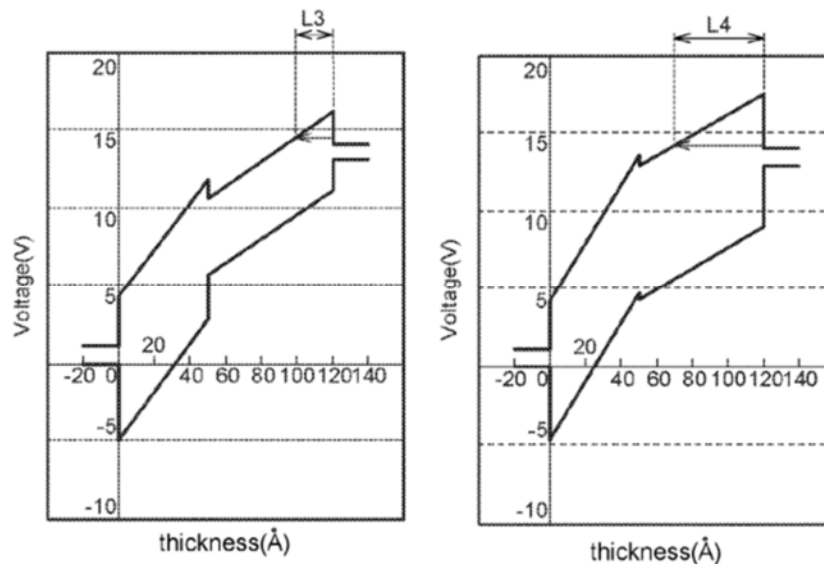
Ex. 1090, Fig. 12(b).¹⁵ As shown, the ILD etch rate is yellow (5 angstroms per second) along the Si_3N_4 tie line, showing that the etch rate remains constant across different carbon doping levels (represented by the axis on the left side of the

¹⁵ “Doping” an insulator such as silicon nitride or oxide refers to chemically adding the dopant to form an alloy. For example, silicon oxide “doped” with boron or phosphorus is called BPSG as a shorthand. Dhungana discusses forming carbon-doped silicon nitride using plasma enhanced chemical vapor deposition (“PECVD”) and suitable precursors.

triangle).¹⁶ This etch rate is based on a CHF₃ plasma, i.e., a dry etch. *Id.* at 2, 4; *see also* '276 Patent, 10:26-28 (“the selective etching includes anisotropic dry etching using chemical etchant such as, for example, ... CHF₃ ... and/or other suitable etchants.”).

62. Dr. Campbell disagrees that “a POSITA would have been motivated to use Fang’s ‘alternative’ etch-stop material of high-k dielectric such as hafnium oxide to reduce potential tunneling effects.” Ex. 2019 ¶ 78. But his opinion is inconsistent with Chen’s disclosure, which a POSITA would have known. Specifically, Chen teaches that a greater tunneling length is “more effective” to electrically isolate conductive layers. Chen, [0004], [0020]. Consistent with that teaching, Chen discloses changing an etch-stop material to a high-k dielectric for an embodiment with one etch-stop layer (*id.*, Figs. 8A-8B, [0048]) as well as an embodiment with two etch-stop layers (*id.*, Fig. 8C-8D, [0050], [0052]). Relevant to Kim, Chen discloses tunneling length with two low-k dielectric etch-stop layers in Figure 8C, and also tunneling length with one high-k and one low-k dielectric etch-stop layers in Figure 8D, which has a greater tunneling length:

¹⁶ The weight composition of silicon and nitrogen in the composite material decreases with increasing amount of carbon doping. But the dry etch rate remains constant across the level of carbon doping as the color-coded areas indicate.



Chen, Figs. 8C–8D, [0050]–[0053]; Ex. 1086, 109:23-111:5 (Dr. Campbell agreeing that the configuration of Figure 8D has a greater tunneling length). A POSITA would have understood Chen to teach that it was desirable to use a high-k dielectric to increase tunneling length even for 3D staircase embodiments that have two etch-stop layers.

63. Dr. Campbell asserts that “Fang **actually** prohibits the use of silicon nitride as an etch stop material” because a silicon nitride etch stop “would be removed at the same rate as the silicon nitride sacrificial layer.” Ex. 2019 ¶ 79 (emphasis in original). But this does not present a problem in Kim’s configuration because Kim has a barrier layer (first stop layer 125a) separating the etch-stop layer and the sacrificial layer. *See, e.g.*, Kim, Fig. 20A. For that reason, Kim does not specify an etch selectivity between the etch-stop layer (second stop layer 125b) and the sacrificial layers. *Id.*, [0187] (“the etch stop layer 125 may include a first stop

layer 125a having an etch selectivity with respect to the sacrificial layers SC1 to SC8 and a second stop layer 125b having an etch selectivity with respect to the insulating layers 111 to 118.”).

c. Kim and Fang’s structural differences are immaterial

64. Dr. Campbell alleges that the structural differences between Kim’s and Fang’s embodiments would have dissuaded a POSITA from applying Fang’s etch-stop characteristics and contact hole etching to Kim. Ex. 2019 ¶ 81. But the structural differences he identified are all irrelevant to the etch-stop functionality and therefore have no impact on etch-stop characteristics and contact hole etching.

65. Dr. Campbell identifies three structural differences, namely, Kim’s embodiment has a high-k dielectric layer around the gate conductors, a barrier layer underneath the etch-stop layer, and (in the modified gate-stack-on-top configuration) no dielectric layer above the gate stack of each step. Ex. 2019 ¶ 82. All three differences are located below the etch-stop layer and thus have no impact on etch-stop characteristics and contact hole etching, as I explain next.

66. An etch-stop layer protects the underlying structure when the layer immediately above it is etched. As Dr. Campbell testified, an etch-stop layer “provides its protective function relative to the etching of the layer that’s immediately above it.” Ex. 1091, 23:4-8; *see also id.*, 41:2-6 (similar); Ex. 2019 ¶ 86 (“an etch-stop layer that is selective with the interlayer dielectric above it ... is

simply a description of how an etch-stop layer functions.”). Based on that function, the position of the etch-stop layers of Kim and Fang makes clear that they provide protection during the etching of the upper insulating layer, *i.e.*, Kim’s interlayer insulating pattern 134 or Fang’s oxide material 135. This is consistent with the goal of preventing over-etching of the shallower contact holes. *See* Fang, [0004], [0031].

When the etch-stop layer works as intended, contact hole etching through the upper insulating layer does not penetrate it, including at the shortest holes where the protection is needed the most. Ex. 1086, 56:19-57:11. And, as Dr. Campbell testified, a POSITA would have designed an etch-stop layer to prevent premature penetration before the deepest contact hole is formed. *Id.*, 90:11-18. Under that scenario, any layers below the etch-stop layer do not serve an etch-stop function during the etching of the upper insulating layer because they are not exposed to the etch. *Id.*, 85:15-20. Therefore, the underlying structure is simply irrelevant to preventing over-etching of the contact holes during the etching of the upper insulating layer when the etch-stop layer is functioning as an etch stop. *See id.*, 99:22-100:24. In other words, the additional barrier and high-k dielectric layers in Kim that are not in Fang, or the dielectric layer above the gate stack in Kim’s gate-stack-on-bottom configuration, do not function as an etch stop when the upper insulating layer above the etch-stop layer is etched. Therefore, the structural differences Dr. Campbell identified have no bearing on the etch-stop characteristic,

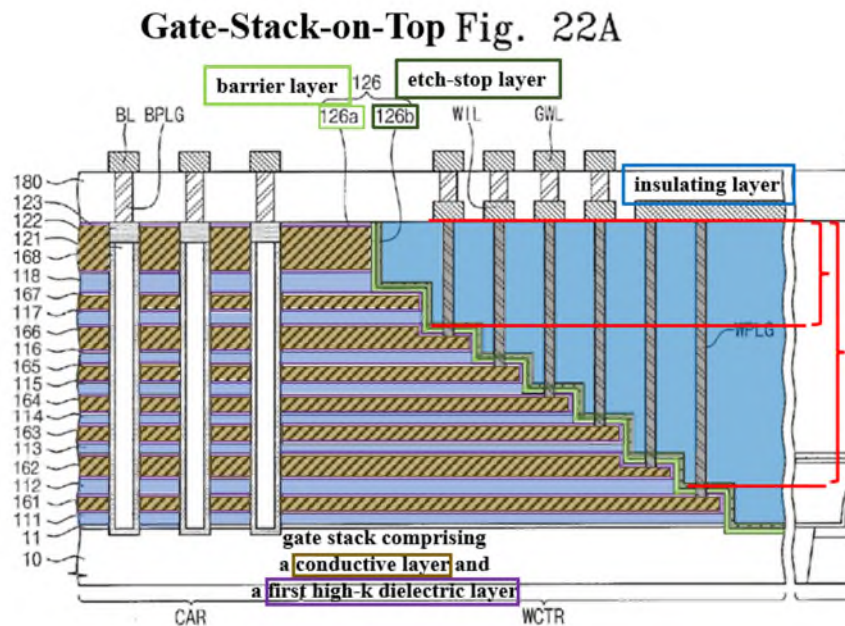
which is set to protect the underlying structure regardless of the actual composition of that structure. So, for example, Dr. Campbell agreed that the high-k dielectric layers surrounding the gate conductors do not serve as an etch stop during the etch of the etch-stop layer when a barrier layer is present between the two, because in that case the high-k dielectric layer is “covered” and “isn’t exposed to the plasma.” Ex. 1091, 56:2-14.

67. Although these additional layers can serve as an etch stop during the etching of the upper insulating layer if over-etching occurs and the etch-stop layer is prematurely penetrated, they merely provide a backup safety margin that a POSITA would not rely on to reduce the etch-stop thickness or otherwise change the etch-stop characteristic, as Dr. Campbell alleges. On the contrary, a POSITA would have designed an etch-stop layer to prevent premature penetration before the deepest contact hole is formed. Ex. 1086, 90:11-18.

68. Moreover, for manufacturing simplicity, it would have been desirable to preserve as much of the etch-stop layer as possible until all the openings have penetrated through the upper insulating layer. This would then enable etching through the etch-stop layer to the first high-k dielectric layer to proceed “in lockstep, in a uniform manner,” as Dr. Campbell agreed. Ex. 1086, 94:14-22. This uniformity is achieved through a high etch selectivity between the upper insulating layer and the etch-stop layer and a suitable etch-stop thickness. The underlying structure has

no impact on these characteristics. That is why, for example, the barrier layer's presence or absence has no impact on the etch-stop thickness. Ex. 1018, cls. 10, 17.

69. To illustrate this uniformity, consider the following. The contact-hole etching process may be divided into two steps: the first step to penetrate the upper insulating layer and a second step (itself comprising multiple steps) to reach the gate conductor layers. A large difference in the etching depth exists during the first step, as illustrated between the shortest and longest openings:



Kim, Fig. 22A.

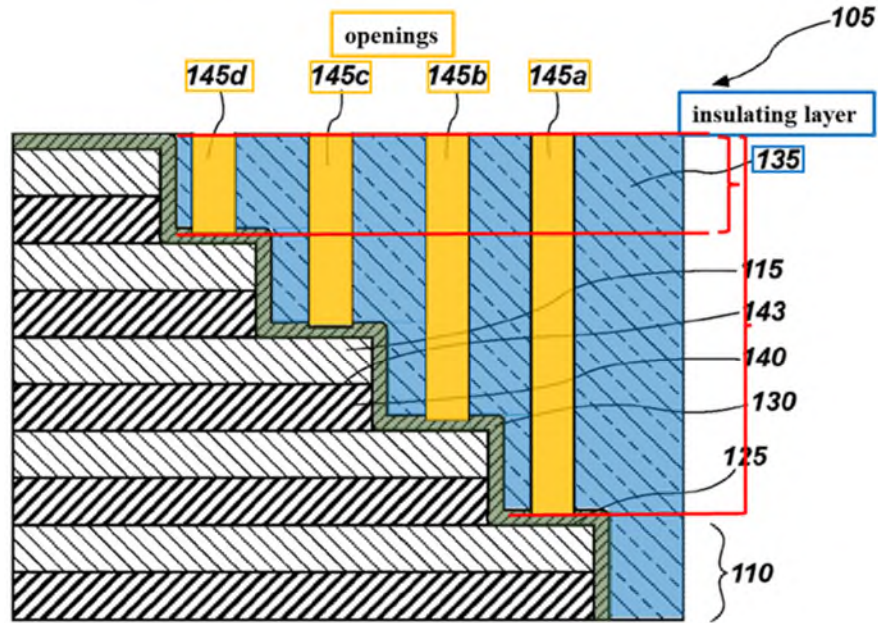
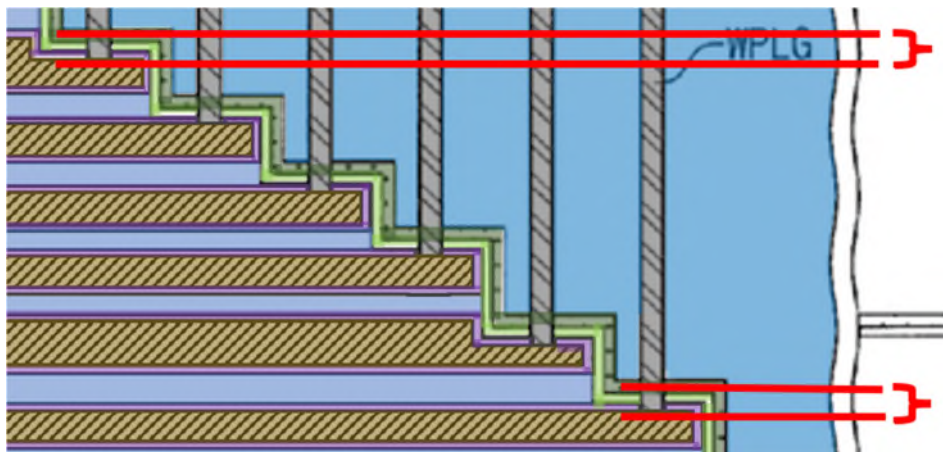


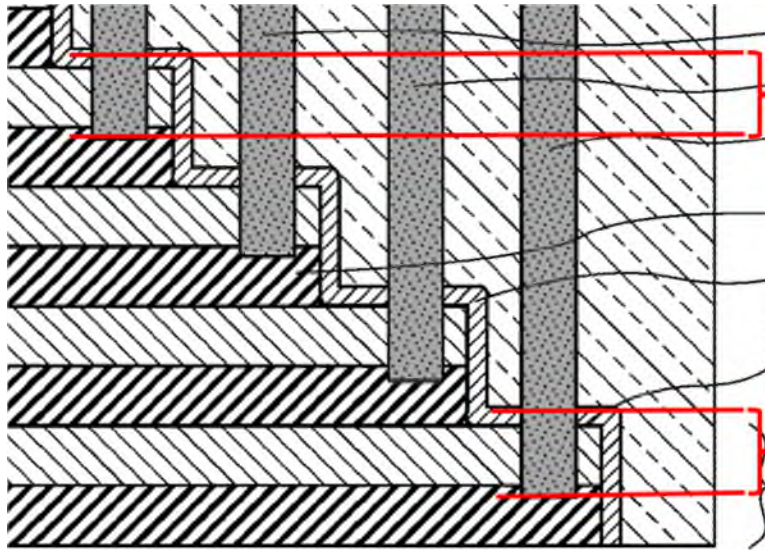
FIG. 5

Fang, Fig. 5.

70. Next, the second step can be uniform across the steps of the staircase independent of underlying structures, as illustrated using the shortest and longest openings:



Kim, Fig. 22A (partial, modified layer order).



Fang, Fig. 6 (partial, original layer order). For manufacturing simplicity, it would have been desirable to keep this second step uniform across the staircase, as Dr. Campbell agreed. Ex. 1086, 94:14-22. Uniformity is achieved when the height of etch-stop layer to remove is the same across all staircase steps. This, in turn, is best accomplished by having a high etch selectivity between the upper insulating layer and the etch-stop layer for what PO calls the “exposure step” (POR, 8) such that an insignificant height of the etch-stop layer is removed during the first step for both the shortest and the longest openings. Once again, the relevant characteristics are those for the first step and have nothing to do with the underlying structure.

2. A High-K Dielectric Etch-Stop Layer

71. Dr. Campbell disagrees that a POSITA would have been motivated to use a high-k dielectric material for Kim’s etch-stop layer. Ex. 2019 ¶ 83. Besides cross-referencing his earlier arguments (which I address above, *supra* § VII.A), he

asserts that Chen's disclosure of tunneling length would not have provided a motivation. Ex. 2019 ¶ 84-85. I explain why Dr. Campbell is wrong above. *Supra* § VII.A.1.b. Finally, Dr. Campbell asserts that Fang only discloses hafnium oxide as an alternative to carbon-doped silicon nitride, and that hafnium oxide is unsuitable for Kim. Ex. 2019 ¶ 86. I explain why Dr. Campbell is wrong above. *Supra* § VII.A.1.b.

3. A Hafnium-Oxide Etch-Stop Layer

72. Dr. Campbell disagrees that a POSITA would have been motivated to use hafnium oxide for Kim's etch-stop layer. Ex. 2019 ¶ 88. Dr. Campbell basically repeats his arguments from earlier sections. His arguments are incorrect as I explain below.

73. First, Dr. Campbell asserts that Fang requires an etch-stop material that is not removed when the sacrificial layers are removed. Ex. 2019 ¶ 89. This is irrelevant to Kim because Kim's barrier layer protects the etch-stop layer from the etchant used to remove the sacrificial layers. *Supra* § VII.A.1.b.

74. Further, Dr. Campbell asserts that I misunderstood Fang to disclose a silicon nitride etch-stop layer, and thus opined that hafnium is a suitable alternative to Kim's silicon nitride etch-stop layer. Ex. 2019 ¶ 90. This is irrelevant because, as I explain above, a POSITA would have been motivated to use hafnium oxide as Kim's etch-stop material with a reasonable expectation of success. Notably, Dr.

Campbell himself refers to Fang’s etch-stop material as silicon nitride: “Chen mentions silicon nitride is an acceptable second stop layer (i.e., Fang’s etch-stop layer in Petitioner’s combination).” *Id.* ¶ 107. Further, my statement is correct in context. Fang itself refers to the etch-stop layer as silicon nitride: “the etch stop material is a silicon nitride material, such as a carbon-doped silicon nitride material.” Fang, [0008]; *id.*, [0025] (“both the nitride materials 120 of the staircase structure 105 and the etch stop material 130 are silicon nitride-based”). My Initial Declaration simply made the point that “Kim’s and Fang’s etch-stop layers are similar.” Ex. 1003 ¶ 141. In that context, “small percentages” of carbon doping do not make a meaningful difference. Ex. 2021, 52:18-54:2. The above discussion on the dry etch rate, for example, demonstrates this. *Supra* § VII.A.1.b.

VIII. GROUND 3

A. A POSITA Would Have Been Motivated to Adapt Fang’s Etch-Stop Layer to Han with a Reasonable Expectation of Success

75. Dr. Campbell disputes that a POSITA would have been motivated to combine Fang’s etch-stop layer with Han’s 3D NAND staircase. Ex. 2019 ¶ 91. But his opinions are not supported by the record.

76. First, Dr. Campbell alleges that Han’s multiple high-k dielectric layers provide additional protection around the gate conductor, rendering an etch-stop layer unnecessary. Ex. 2019 ¶ 92. In other words, Dr. Campbell opines that a POSITA would not have implemented a 3D NAND staircase with both high-k dielectric and

etch-stop layers. But Kim and Park (Ex. 1088) disclose exactly that. *See, e.g.*, Kim, Fig. 22A; Park, Fig. 9j. And, like Han, Park also discloses multiple high-k dielectric layers around the gate conductors. Park, Fig. 7c. On the flip side, Han also discloses a single high-k dielectric layer around the gate conductors. Han, Fig. 26B; Ex. 2019 ¶ 107 (“Han already has at least a single, and potentially a second, high-k dielectric layer....”). That single layer is a BK or blocking layer, which alone my Initial Declaration identified as meeting the first high-k dielectric layer claim limitation. Ex. 1003 ¶ 170 (“Therefore, *the gate stack compris[es] ... a first high-k dielectric layer*, e.g., the tunnel insulating layer TIL *or* the blocking insulating layer BK.”) (red italicized text in original). Although the high-k dielectric layer(s) may protect the conductive layers because the high-k dielectric layers have a low etch rate, they “tend to be very thin” and do not provide much additional safety margin. Ex. 2021, 48:14-19. Dr. Campbell agrees. Ex. 1086, 77:23-25 (“that liner is very thin.”). Thus, a POSITA would not have relied on the high-k dielectric layers to stop the etch of the upper insulating layer. The fact that Han has to resort to a staged etching process, as Dr. Campbell acknowledges, shows that the high-k dielectric layers are not adequate as an etch stop. Ex. 2019 ¶ 93.

77. Second, Dr. Campbell asserts that Han discloses a staged etching approach, which renders etch-stop protection unnecessary. Ex. 2019 ¶ 93. But the record evidence discredits Dr. Campbell’s assertion. Dr. Campbell admits that

Han’s staged etching approach involves using multiple masks. Ex. 1086, 144:18–145:24. As both Fang and the ’276 Patent recognized, multiple masks lead to “additional processing acts, complexity, and cost to the overall process.” Ex. 1003 ¶ 215 (citing Fang, [0004]; ’276 Patent, 5:58-60 (“two or more lithography masks are used to separate etching processes, which adds cost and complexity to the fabrication process.”); Ex. 2019 ¶ 25 (“[m]anufacturers tried to address the [punch-through] problem by using two or more etching processes that would create holes of similar depth at the same time before creating holes at other depths.... But this method creates problems of additional fabrication cost and complexity.”). Fang and the ’276 Patent squarely contradict Dr. Campbell’s opposite assertion, that Han’s staged etching approach “avoids added cost and complexity....” *Id.* ¶ 93; *see also id.* ¶ 96 (alleging “an additional etch-stop layer adds unnecessary cost and complexity....”).

78. Moreover, Han contemplates a single- **or** multi-staged etching process. Han, [0156] (“**At least one** patterning process may be performed ... to form lower contact holes LH.”). That is, Han’s staged-etching process is optional. Ex. 1086, 145:11-15. So, at the very least, a POSITA would have been motivated to add an etch-stop layer to Han’s single-staged etching process. But as just explained, a POSITA would have been motivated to add an etch-stop layer to Han’s multi-stage etching process to reduce cost and complexity.

79. Third, Dr. Campbell again alleges the order of the alternating layers would have dissuaded a POSITA from combining Han and Fang. Ex. 2019 ¶ 94. As I explain above, that order simply has no impact on the etch-stop layer. Both were well-known and routine and provide isolated gate conductors in a 3D NAND staircase structure. *Supra* § VI.A.1. And as the alternating layers are located below the etch-stop layer, they do not affect the etch-stop characteristics. *Supra* § VII.A.1.c. The only specific difference that Dr. Campbell identifies, that Fang’s “word line contacts must penetrate a full dielectric layer to reach the stack” but Han’s do not, actually means the combination, like Han, uses a simpler etching process that has a reduced number of layers and etch chemistry steps to reach the gate conductors. Ex. 2019 ¶ 94.

80. Dr. Campbell’s argument against the expectation of success in adding Fang’s etch-stop layer to Han’s staircase simply repeats his argument against a motivation to combine. Ex. 2019 ¶ 95. The argument is wrong for the same reasons I explain above.

81. Lastly, Dr. Campbell suggests that my opinion that over-etching/punch-through was a concern for Han’s structure, and that “Han would have ‘suffered from the shortcomings of the conventional solutions to over etching’” is incorrect. Ex. 2019 ¶ 97. This suggestion is self-contradictory. Dr. Campbell himself argues that Han “employs at least two methods that would protect against the risk of punch

through.” *Id.* ¶ 96. That very fact indicates punch-through was indeed a concern of Han. And Fang’s teaching identified Han’s staged-etching approach as a conventional, costly solution, upon which Fang’s etch-stop layer would have improved.

B. Han in View of a POSITA’s Knowledge or Fang Renders Claim 4 Obvious

82. Dr. Campbell disagrees that Han in view of Fang “disclose[s]” the limitation of claim 4. Ex. 2019 ¶ 98. But I opined that claim 4 is **obvious** in view of a POSITA’s knowledge or in view of Fang. Ex. 1013 ¶¶ 186-88. Dr. Campbell doesn’t respond to my actual opinion.

83. Dr. Campbell repeats his arguments about the complexity of 3D NAND technology and etch processes to assert that claim 4 is not obvious. Ex. 2019 ¶ 98. These arguments are incorrect. *Supra* §§ VI.A.2, VI.C. Additionally, Dr. Campbell does not address the actual limitation of claim 4 to show how the limitation itself is complex. *See* Ex. 2019 ¶¶ 98-99. But as I explained in my Initial Declaration, only three possibilities exist for the relationship of the two claimed etch rates, and the claimed relative rates are the only sensible one. Moreover, Dr. Campbell’s argument is belied by his contention elsewhere that a high-k dielectric layer having a lower etch rate is readily achievable and would have been obvious to a POSITA. *Id.* ¶ 92 (“For example, the high-k dielectric layer is a different material than the insulating layer above it, and by using a material with a lower etch-rate for the high-k dielectric

material, it can provide the protective etch-stop function.”). Dr. Campbell’s argument regarding the high-k dielectric material appears to be based on a range of available materials from which to select. *See Ex. Id.* ¶ 98. But Kim discloses a range of available materials for the gate conductive layers as well. Kim, [0119].

84. Dr. Campbell states that “Fang has an additional dielectric insulating layer separating its etch-stop layer from the gate stack.” Ex. 2019 ¶ 99. He doesn’t explain the relevance of this statement to the claim. But the statement actually supports the obviousness of claim 4 because, in the combination, Han, with its gate-stack-on-top configuration, does not have an additional dielectric insulating layer separating its etch-stop layer from the gate stack. *See, e.g.*, Han, Fig. 29. So the need to protect the conductive layers through a lower etch rate is greater, not lesser, as Dr. Campbell appears to suggest.

C. Han in View of Fang and a POSITA’s Knowledge Renders Claim 5 Obvious

85. Dr. Campbell disagrees that Han in view of Fang “disclose[s]” the limitation of claim 5. Ex. 2019 ¶ 100. But I opined that claim 5 is **obvious** in view of a POSITA’s knowledge. Ex. 1013 ¶¶ 189-90. Dr. Campbell doesn’t respond to my actual opinion.

86. Dr. Campbell repeats his arguments about the complexity of 3D NAND technology and etch processes to assert that claim 5 is not obvious. Ex. 2019 ¶ 100. These arguments are incorrect. *Supra* §§ VI.A.2, VI.C. Additionally, Dr. Campbell

does not address the actual limitation of claim 5 to show how the limitation itself is complex. See Ex. 2019 ¶¶ 100-03. Moreover, Dr. Campbell's argument is belied by his contention elsewhere that a high-k dielectric layer having a lower etch rate was readily achievable and would have been obvious to a POSITA. *Id.* ¶ 92 ("For example, the high-k dielectric layer is a different material than the insulating layer above it, and by using a material with a lower etch-rate for the high-k dielectric material, it can provide the protective etch-stop function."). Han discloses using high-k dielectric for the first high-k dielectric layer and identifies exemplary materials without identifying narrow restrictions. Han, [0140]. Thus, a range of materials is available from which to choose an appropriate etch rate, as Dr. Campbell's own testimony supports. Ex. 1086, 148:22-149:1.

87. In fact, my Initial Declaration identified such an example from a reference. Ex. 1003 ¶ 189. Dr. Campbell alleges that "the *reference* ... is not relevant to the technology at issue here" because it includes "a simple argon plasma." Ex. 2019 ¶ 102 (emphasis altered). But the reference shows the claimed relative etch rates for HBr to (HBr+Ar) ratios of up to about 25%. As Dr. Campbell acknowledged, (HBr+Ar) is a hydrogen-bromide-and-argon mixture. Ex. 1086, 84:12-20. It is not "a simple argon plasma." Ex. 2019 ¶ 102.

88. Dr. Campbell's remaining arguments, *i.e.*, Han's structure (Ex. 2019 ¶ 101), Fang's use of carbon-doped silicon nitride (*id.* ¶ 102), the claimed etch rates

not being the only sensible relationship (*id.* ¶ 103), either refer back to his earlier arguments or are conclusory. And the only two specific arguments Dr. Campbell adds are both wrong, as I explain next.

89. First, Dr. Campbell argues that “a POSITA would not have a reasonable expectation of successfully achieving the combination where neither Han nor Fang are designed to include both an etch-stop layer over the staircase steps and a high-k dielectric layer surrounding the conductive layers.” Ex. 2019 ¶ 101. The prior art of record contradicts this argument. Specifically, Kim and Park, among others, disclose both an etch-stop layer over the staircase steps and a high-k dielectric layer surrounding the conductive layers. That shows this configuration was well known and routine.

90. Second, Dr. Campbell asserts that “[a] POSITA may be motivated to make the etch-stop and first high-k dielectric layers out of the same material, ensuring they have the same etch-rate to effectively increase the thickness of the etch-stop layer.” Ex. 2019 ¶ 103 (emphasis omitted). He further asserts that using the same material “would still be consistent with the purpose of a high-k dielectric layer to protect surrounding oxide layers during deposition of the conductive layer material.” *Id.* But that assertion ignores the purpose of the etch-stop layer altogether. And to the extent Dr. Campbell appears to suggest selecting materials for the layers is easily done, he contradicts his own argument elsewhere about the

complexity of the process, *e.g.*, “minor alterations in one process step usually changes the outcome of other process steps.” *Id.* ¶ 44.

IX. GROUND 4

A. Han and Fang Would Benefit from a Barrier Layer

91. Referring back to his arguments in Ground 3, Dr. Campbell argues that a POSITA would not have been motivated to combine Han, Fang, and Chen for the same reasons that a POSITA would not have been motivated to combine Han and Fang. Ex. 2019 ¶¶ 105-106. But Dr. Campbell ignores the clear benefits of using an etch-stop layer to prevent punch-through. *Supra* § VIII.

B. Chen Would Have Motivated a POSITA to Add a Barrier Layer

92. Dr. Campbell asserts that a POSITA would not have been motivated to add Chen’s barrier layer because the Han/Fang combination already provides adequate tunneling length. Ex. 2019 ¶¶ 107. Dr. Campbell’s opinion is unsupported by any evidence and contradicts Chen’s teaching. He asserts that “Fang’s carbon-doped silicon nitride has an energy gap of 6.5 eV” and cites Fang paragraph 20. But Fang doesn’t mention any energy gap, let alone a specific value of 6.5 eV for carbon-doped silicon nitride. *See generally* Fang. Chen doesn’t mention “6.5 eV” either. *See generally* Chen. Thus, Dr. Campbell’s assertion that the Han/Fang combination already provides adequate tunneling length is not supported by any evidence. Dr. Campbell does not dispute that adding a barrier increases tunneling length, as a comparison of Chen’s Figure 8B and Figure 8D clearly shows. Thus, because Chen

teaches that a greater tunneling length is “more effective” to electrically isolate conductive layers, a POSITA would have been motivated to add a barrier layer to more effectively isolate the conductive layers. Chen, [0004], [0020]. Chen’s references to 6 eV would not have dissuaded a POSITA from doing so because Chen itself did not stop at a single high-k dielectric etch-stop with an energy gap larger than 6 eV. *Id.*, [0049]. Instead, Chen also teaches a configuration with two etch-stop layers, including a high-k dielectric layer, that further increases tunneling length. *Id.*, [0052]-[0053]. A POSITA would have been motivated to do the same.

93. Dr. Campbell asserts that certain candidate materials for Chen’s etch-stop layers are slow and expensive to form. Ex. 2009 ¶ 108. This assertion is wrong for two reasons. First, I opined on a silicon oxide or aluminum oxide barrier layer. Ex. 1003 ¶ 222. Silicon zirconium oxide (ZrSiO_2) and silicon hafnium oxide (HfSiO_2) that Dr. Campbell cherry-picked to support his assertion are thus irrelevant. *See also* Chen, [0041] (disclosing a range of materials for the first stop layer). Second, Dr. Campbell doesn’t cite any evidence to support his assertion that silicon zirconium oxide (ZrSiO_2) and silicon hafnium oxide (HfSiO_2) are slow and expensive to form.

C. The Alleged Differences Are Irrelevant to Adding a Barrier Layer

94. Dr. Campbell asserts that adding a barrier layer would require a different etch process and reoptimization of etch parameters. Ex. 2019 ¶ 109. This is the same argument that he repeats several times and it fails for the same reasons above. *Supra* §§ VI.A.2, VI.C.

X. DECLARATION

95. In signing this declaration, I realize that this declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the USPTO.

96. I am aware that willfully false statements and the like made by me in connection with this declaration are punishable by fine or imprisonment, or both (18 U.S.C. § 1001) and may jeopardize the validity of the Petition. All statements herein made by me of my own knowledge are true and all statements made on information and belief are believed to be true. I declare under penalty of perjury that the foregoing is true and correct.

Executed this 30th day of January, 2026 at Austin, Texas.



Sanjay Banerjee, Ph.D.