UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

vs.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case No. IPR2025-00228
U.S. Patent No. 11,101,276

REMOTE DEPOSITION OF STEPHEN CAMPBELL

Friday, January 16, 2026

9:03 a.m. (CT)

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Joan Ferrara, RMR, FCRR

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January 16, 2026

9:03 a.m. (CT)

Deposition of STEPHEN CAMPBELL, held remotely via Zoom, before Joan Ferrara, a Registered Merit Reporter, Certified Realtime Reporter, and Notary Public.

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---------- I N D E X ----------

WITNESS	EXAMINATION BY	PAGE
STEPHEN CAMPBELL		
	MR. HSU	5, 160
	MR. DUNTEMAN	155, 161

------ EXHIBITS REFERENCED ------

EXHIBIT 1008	Chen Patent	26
EXHIBIT 2019	Declaration of Stephen Campbell in Support of Patent Owner's Response	30
EXHIBIT 1005	Kim Patent	41
EXHIBIT 1006	Fang Patent	103
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STEPHEN CAMPBELL,

called as a witness, having been duly sworn by a Notary Public, was examined and testified as follows:

EXAMINATION BY

MR. HSU:

Q Good morning, Doctor.

A Good morning.

Q Good to see you again.

Please state your name and spell it for the record, please.

A My name is Stephen, S-T-E-P-H-E-N, Alan, A-L-A-N, Campbell, C-A-M-P-B-E-L-L.

Q I understand you've been deposed before. So you're aware of what's the protocol, I suppose, but just so that we're on the same page, I'll go over a few things.

So I see you understand I'm going to ask questions and you'll provide answers. I'll do my best not to talk over you and -- but for the court reporter, you do have to give verbal answers and -- so far so good?

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A Yes.
Q Okay. And if there's anything in my questions that's not clear, please ask for a clarification. If you don't and you answer the question, I will assume that you have understood my question.
Is that fair?
A Yes.
Q Now, from time to time you'll hear your attorney raising an objection. And you understand that unless you're specifically instructed not to answer, you will still go ahead and answer the question in spite of the objections, right?
A Yes.
Q And we'll plan on taking a break roughly every hour or so, but if I go past that or if at any time you need a break, just please let us know. All I ask is that you don't ask for a break when a question is pending.
Is that okay?
A Yes.
Q Is there any reason why you would not be able to give competent answers

today, such as a medical condition or anything that may affect your ability to testify?

A No.

Q Do you have any papers in front of you?

A I have the '276 unmarked copy.

Q And you're referring to your declaration, is that right?

A My apologies. Yes, it's my declaration for '276.

Q And that's Exhibit 2019, correct?

A I would have to look that up, I'm sorry.

Q On the bottom right perhaps.

A Yes, 2019, correct.

Q Okay. Anything else do you have in front of you?

A No.

Q Okay. And then, obviously, you're on a computer. What applications are running on the computer?

A Aside from Zoom, I have Adobe, which is, again, running my declaration,

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and nothing else.

Q And the Adobe currently doesn't have any files opened, is that right?

A It has my declaration, the only file open.

Q Okay. And both the paper copies and the electronic copies of your declaration that you have in front of you, are they unmarked clean copies?

A Yes. Yes, they are unmarked clear copies.

Q Now earlier you talked -- you heard the court reporter talking about a realtime link, right?

A Yes, I did.

Q Do you have that open, by any chance?

A I have it in -- I have it in the message area. I haven't clicked the real link.

Q Okay. I appreciate that you don't open it because customarily that's -- the witness don't have that.

A Okay.

Q Now, what did you do to prepare

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for the deposition today?

MR. DUNTEMAN: I just want to remind the witness not to reveal any communications with counsel.

A I reviewed my declaration obviously, comments from Dr. Banerjee, and the patents that are discussed in the declaration.

Q Did you review anything else?

MR. DUNTEMAN: I'll again remind the witness not to reveal any communications with counsel.

A Did I review anything else...

I did have a meeting with counsel to go over the content, but that's all I can say about that.

Q And who was the counsel that you met with?

THE WITNESS: Robert, am I allowed to say who it is?

MR. HSU: I didn't hear counsel objecting.

MR. DUNTEMAN: Objection. You can reveal who was there, but not what we discussed.

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A Mr. Dunteman and Mr. Greenfield would be the primary people there.

Q When did you meet with Mr. Dunteman and Mr. Greenfield?

A Yesterday.

Q And how long was the meeting?

A Roughly, 5 hours.

Q And was that the only time you met with counsel to prepare for this deposition?

A Yes. I did have an email exchange with Mr. Dunteman last evening.

Q Did you review anything that is not already of record, meaning already one of the exhibits as submitted in the proceeding in preparation for this deposition?

A No.

Q Did you speak to anybody else besides counsel to prepare for this deposition?

A No.

Q Do you recall roughly when you started working on this declaration in support of patent owner's response?

MR. DUNTEMAN: Objection.
Again, I remind the witness not to reveal any communications or attorney work product.
A Beginning of last year. So let's say January '25, something like that.
Q Are you saying you began to work on patent owner's response in January of 2025 in this IPR proceeding, is that correct?
A I began having discussions with the attorneys about that timeframe. Exactly when they put it into PR, I don't exactly recall, but that is when I started discussions with them.
Q So you don't recall the time when you actually started working on this declaration in support of patent owner's response, is that correct?
A Yes, I couldn't give you an exact date.
Q Do you remember roughly how much time you spent working on the declaration?
A This is just a rough estimate, but 20 to 30 hours.

Q And you recall you submitted a first declaration in support of patent owner's preliminary response, right?

A Yes.

Q Okay. So just to be clear, when I refer to declaration today, unless I explicitly mention your first declaration or somehow indicate that I'm referring to the very first one, I'm referring to Exhibit 2019 that you have in front of you in support of patent owner's response.

Is that okay?

A Yes.

Q So today we are here for an IPR proceeding regarding U.S. Patent No. 11,101,276, and I'll refer to that patent by the '276 Patent. Okay?

A Yes.

Q Now, would you agree that the '276 Patent is directed to methods of forming a staircase structure for a 3D NAND memory?

A I would phrase it a little differently. The '276 focuses on the contacts for the staircase structure, in

particular the etch-stop concerns.

Q When you said you would phrase it a little differently, is there anything in the way I phrased it that you disagree with?

A It's a question of emphasis. When you say it's forming the staircase, that's not wrong. But aside from the sequence of the staircase, which is discussed in this declaration, the majority of the content that are being discussed is the -- not the deposition of the sacrificial layer and dielectric layer, but rather the -- how you make reliable contacts.

So it's just a matter of emphasis. There's nothing wrong with what you said. It's just not how I would say it.

Q So if I understand you correctly, what you're saying is the '276 Patent focuses on the etch-stop layer and the staircase is more of the contacts.

Would that be fair?

MR. DUNTEMAN: Objection.

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Mischaracterizes testimony.

A Again, you are trying to narrow it down. I did say that it also includes the questions about gate on top or gate on bottom. So that would certainly be part of this declaration. So I would not agree with you that it's just the etch-stop.

Q Now, 3D memory devices were created to meet the demand for a -- for higher storage capacity, right?

A Yes, that's correct.

Q And 3D memory devices have a number of gate stack and dielectric layer pairs in a staircase structure, right?

A Yes.

Q What is the function of the gate stack in the staircase?

A What is a gate stack in the staircase? What is its function? Is that what you said?

Q Yes. Let me -- let me -- strike that. So let me reask it.

What is the function of the gate stack in the staircase?

A The gate stack -- how I will say

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this exactly, in the gate stack -- sorry.

In the staircase as it is deposited, there are sacrificial layers. These sacrificial layers will ultimately be removed and a gate metal will be deposited. And if that's tungsten, there will also be a high-k layer placed, put into the area that used to be the sacrificial layer.

The function of this metal is to act as a gate electrode for the memory devices.

Q I'm sorry, I missed the very last part. You said the function of this metal is to act as what now?

A A gate electrode for the device.

Q And there are multiple of these gate stack layers because there are basically one gate electrode for each memory cell, is that right?

A Yes, that's correct.

Q And what is the function of the dielectric layers in the staircase?

A The dielectric layers provide an insulation between the gate layers.

Q And these gate stack and

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dielectric layers alternate in the staircase structure, right?

A Yes.

Q And why -- or strike that.

What is the reason for using a staircase structure in a 3D memory device?

A It provides a higher density. It allows you to make devices in three dimensions. And staircase allows you to access all of the gates inside the stack.

Q And to the last part of your answer, staircase allows you to access all of the gates inside the stack, can you expand on that a little bit?

MR. DUNTEMAN: Objection. Form.

A What is it that you don't understand?

Q So let me ask it differently.

How does a staircase allow all of the gates inside the staircase stack to be accessed?

A If you don't create a staircase, all of the gates are shadowed by the gates above them.

That is to say, you can't

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make -- it's very, very difficult to make contact to the gates. So the process is done to etch back the layers so that all of the gates are exposed from the surface.

Obviously, as we discussed, there will be an insulator that you have to etch a hole through the insulating film, but you have to access all of the gates. You have to make an electro contact to all of the gates independently.

Q So each layer of the staircase forms a step, correct?

A Each --

Q Strike that. Sorry, strike that. Exactly what I was thinking. Thank you for that clarification.

Each pair of layers of the staircase forms a step, correct?

A Yes.

Q And each pair of the layers refer to a gate stack in a dielectric layer, correct?

A Yes, that's correct.

Q And as you said, the contact conductor, the vertical conductors have to

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reach the gate stack, correct?

A Correct.

Q And it has to penetrate through the insulator that's on top of the gate stack, correct?

A Yes.

Q And that is true whether the gate stack is on the top of each step or on the bottom of each step, correct?

A If you're saying that the contact has to reach the gate metal, the answer is yes.

Q And what is the reason for having the alternating gate stack and dielectric layers?

A As I just described, the insulating layer -- sorry, the dielectric layers provide an electrical insulation between the gates. So if they are not connected -- yeah, they're not connected, unless you connect them elsewhere. They're intended to be separate.

Q So if I look at not just a single step, right, there are many, many steps typically in a staircase structure,

is that fair so far?

A Yes.

Q And so each gate stack has a dielectric layer -- strike that.

With the exception of the very top or the very bottom, which we'll ignore for purposes of this question, each gate stack has a dielectric layer that's on top of it which insulates that particular gate stack from the next gate stack above it, correct?

A Yes, that's correct.

Q And in the downward direction, each gate stack is insulated from the next gate stack below also by the intermediate dielectric layer that is in between them, correct?

A Yes, that's correct.

Q And that insulation function provided by the dielectric layer, or layers plural, is the same whether the dielectric layer is on the top of each step or on the bottom of each step, correct?

A That's a rather vague question. Can you explain more what you mean?

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Q Sure.

We've talked about the fact that the dielectric layers are placed above and below each gate stack to insulate the gate stacks from each other, correct?

A Yes.

Q So the question is that insulation function provided by the dielectric layer -- strike that.

The dielectric layer provide that insulation function to the gate stacks regardless of its position in each step of the staircase, correct?

A I don't understand independent of whether it's on top or the bottom.

Q Okay.

A The insulating layer is separating two gate stacks. It's isolating between two gate stacks.

Q Let me try to ask it a different way, a better question.

So I think we agree that -- or that you testified the dielectric layers provide an insulating function between adjacent gate stacked layers, correct?

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A Yes.

Q Now the -- in a gate-stack-on-top configuration, each step of the staircase would have a gate stack on the top and then a dielectric layer on the bottom, and then the next step down would have the same two layers order in the same order, correct?

A Yes, it would be in the same order. Obviously, it would be a different length.

Q Right.

And the insulation function provided by this dielectric layer extends through the length or basically the coverage of the dielectric layer, right? In other words, the different length that you just referred to doesn't -- strike that.

What you referred to by a different length refers to the fact that these are a staircase, so each pair of layers have a different length because they form a step-shaped staircase structure, right?

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A Yes, that's correct.

Q Now, where a layer below is longer than the upper layer, the dielectric layer doesn't need to provide insulation, right, because there's no longer two adjacent gate stacks that need to be insulated. Is that fair?

A I'm trying to picture what you're saying. Is there a diagram, for example, that we might use from the declaration? Because I don't really understand what you're asking.

Q Let me -- let me try one more time, and then if that doesn't work, I'll see if there's a good picture.

Now, each pair of a dielectric and a gate stack have the same length, correct?

A Yes, that's correct.

Q So the dielectric provides the entire length of that corresponding gate stack, the insulation it needs from the gate stack that's on the other side of the dielectric layer, correct?

A My only hesitation there is on

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one side the gate stack is going to be a different length than the other gate stack, obviously.

The dielectric provides isolation in the area where the two metals are coincident. That is to say, the oxide that goes beyond the recessed gate stack is not very effective in isolation because there's no gate metal above it or below it -- or above it generally, yeah.

Q Can you explain what you meant by the second part of your answer, which was the oxide that goes beyond the recessed gate stack is not effective in isolation?

A In order to provide isolation, you have to have a conductor on both sides.

And so if the oxide extends to the end of the metal underneath it, but the metal above it doesn't extend that far because of the staircase structure, you could say that the oxide that's exposed -- sorry, the dielectric that's exposed beyond the upper gate stack is not really insulating something because there's no metal above it.

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Q Right.

But on the other hand, because there's no metal above it, it doesn't need to provide that insulation function, right --

A Yes, yes.

Q -- for that --

A That's correct.

(Simultaneous crosstalk.)

Q -- amount of space.

So then would you agree that whether the gate stack is on the top or on the bottom of each step, it has a dielectric layer above it and a dielectric layer below it?

A This is a gate stack on top. The dielectric layer will not extend to the full length of the gate stack.

The dielectric layer under the gate stack will extend the entire length.

If it is a gate on the bottom, then the upper dielectric layer will extend all the way to the end of the gate stack.

Q Right.

But as we just discussed and I

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think we agreed that the length of the dielectric layer provides the necessary insulation for the gate stack it is -- or for the gate stacks that the dielectric layer is isolating, correct?

MR. DUNTEMAN: Objection. Form.

A Again, it was kind of broken up. Can we repeat that question?

Q Sure.

In your last answer, you talked about the length of the dielectric layer that is above the gate stack having a different length depending on the order of the alternating layers, correct?

A Yes, that's correct.

Q And we had agreed earlier that whatever the length of the dielectric layer is, the dielectric layer provides the necessary insulation between its two adjacent gate stack, correct?

MR. DUNTEMAN: Objection. Form.

A This, again, as I mentioned previously, the dielectric can only provide an insulating function if there are metal on both sides of the dielectric.

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And so if you're asking is it providing insulation, it only provides insulation to the length that both metal stacks extend.

MR. HSU: I am going to put in the chat Exhibit 1008.

BY MR. HSU:

Q Let me know when you get it.

A All right. This is Chen.

Q Right, this is the Chen reference that is part of this IPR proceeding, correct?

A Yes, it is.

Q Okay. If I may turn your attention to Figures 7A and 7B.

A All right.

Q Do you agree that Figure 7A shows a gate stack on the bottom configuration?

A I have to verify the layer numbers, the 110 and 120. If you'll hold on, I'll do that.

Q Sure. Paragraphs 45, 46 may help.

A I have it on 21, that's fine.

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Okay. So 7A has the gate stack on the bottom and 7B has the gate stack on the top.

Q And layer 120 -- strike that.

Layers 120 are the dielectric layers, correct?

A Yes.

Q And that's the same in both Figures 7A and 7B?

A Yes.

Q And do you agree that layers 120, the dielectric layers provides the insulation function that we discussed in both of these configurations?

MR. DUNTEMAN: Objection. Form.

A The insulation layer -- sorry, the dielectric layer provides insulation where the two metal, the gate stacks are present on both sides of the dielectric.

Q And that insulation the dielectric layers provide is sufficient for the functioning of the staircase structure, correct?

A I didn't catch the last part of it.

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Q Let me ask it differently.

Where the two metal gate stacks are not present on both sides of the dielectric, that insulation function provided by the dielectric layer is not necessary at that space, correct?

MR. DUNTEMAN: Objection. Form.

A Yes.

Q So in both Figure 7A and 7B, the gate-stack-on-bottom and gate-stack-on-top configurations, the dielectric layers provides the necessary insulation function for the staircase structure, correct?

A For the staircase structure to -- explicitly, what are you asking?

Q You had told me that the dielectric layers is to provide insulation between two gate stack, correct?

A Correct.

Q And in both the gate-stack-on-bottom and gate-stack-on-top configurations, the dielectric layers provide that function, correct?

A Yes.

Q Now, do you agree that what Dr.

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Banerjee described as a staircase having the reversed layer order, that is a sacrificial layer on top or equivalently gate stack on top, is formed by starting with the insulator rather than the sacrificial layer during the deposition process?

MR. DUNTEMAN: Objection. Form.

A Say this again, I'm sorry?

Q Do you agree that what Dr. Banerjee -- actually, strike that.

Let's break it down into two parts.

You agree that Dr. Banerjee opined on a staircase having a reversed layer order, that is a sacrificial layer on top or equivalently gate stack on top for the Kim reference, correct?

A Let's go to the declaration. Tell me where this is.

Q Okay. Before we go there, let me just ask you: Do you recall that Kim's figure expressly discloses a gate stack on the bottom configuration?

MR. DUNTEMAN: Objection. Form.

A Again, I'd be happy to answer that question if we go to the declaration. Ground one, let's look at the pictures.

Q Okay. Let's go to your declaration starting at paragraph 34.

MR. DUNTEMAN: Counsel, we're talking about Exhibit 1003 here?

MR. HSU: No, I was referring to Dr. Campbell's declaration.

THE COURT REPORTER: Can you drop that in the chat, counsel?

MR. HSU: Certainly. Let me see. Yes, let me drop that in the chat.

BY MR. HSU:

Q Let me know when you are there, Dr. Campbell.

A So we are at paragraph 34?

Q Yes.

A All right.

Q So first you testified earlier that the sacrificial layer at some point during the fabrication process is replaced by the gate stack, correct?

A Sacrificial layer is substituted

for the gate stack, yes, that's correct.

Q So whether we talked about sacrificial layer on top or a gate stack on top, we're referring to eventually the same memory configuration, correct?

MR. DUNTEMAN: Objection. Form.

A So is the question relating to the modified Kim that Dr. Banerjee provided?

Q Yes. I was simply trying to, I guess, establish an agreed-upon shortcut, that when we refer to sacrificial layer on top or gate stack on top, ultimately they refer to the same configuration because the sacrificial layer there are substituted with the gate stack, as you phrased it.

Would you agree to that?

A Yes. The gate stack and the sacrificial layer are essentially the same except for the possibility of the high-k material that is deposited inside the cavity left by the sacrificial layer.

Q What do you mean by the gate stacks and the sacrificial layer are essentially the same?

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A I mean that they are in the same position.

Q Okay. So the Kim reference discloses a gate stack on the bottom configuration in Figure 17A through 22B embodiment, correct?

A Figure 17A shows the gate stack on the bottom.

Q And you understand that Dr. Banerjee opined on a gate-stack-on-top configuration based on a separate disclosure in Kim with respect to another embodiment, correct?

MR. DUNTEMAN: Objection. Form.

A Again, could I have you repeat that question?

Q Do you agree that -- strike that.

Do you understand that Dr. Banerjee opined on a gate-stack-on-top configuration for the Figure 17A through 22B embodiments based on a disclosure in Kim with respect to another embodiment?

MR. DUNTEMAN: Same objection.

A I understand that Dr. Banerjee

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produced a diagram that purported to be a gate stack on top.

In this case, he changed the insulating layers of 17A to be sacrificial, and vice versa, with corresponding modifications of the gate stacks in the later figures.

As shown in the side-by-side comparison of the original 22A and Dr. Banerjee's modified 22A, Dr. Banerjee also added hatching to the insulating layers to make them appear as gate stacks, and removed hatching.

Dr. Banerjee renumbered the labels of 22A, for example, to change label 116 to 166 and vice versa.

Dr. Banerjee does not identify any benefit to inverting Kim's layers or any problem that would be solved by doing so.

In fact, Dr. Banerjee does not articulate any motivation to combine these multiple embodiments from Kim.

Dr. Banerjee appears to justify combing embodiments in Kim based on Kim

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stating that overlapping descriptions of elements previously described.

I disagree that Kim's statement is permitting the kind of mixing and matching of embodiments that Dr. Banerjee believes it does. Even if it did, it still does not articulate any motivation to combine embodiments.

This statement is provided in the context of using the same reference numbers for the same elements across the embodiments.

Specifically, it states that the same elements as in the embodiments previously described with reference to 5A to 14B will be denoted by the same reference numbers therein, and for concise description, overlapping description of elements previously described with reference to Figures 5A and 14B.

This statement does not permit the kind of mixing and matching of elements that Dr. Banerjee does in support of modifications to Kim figures.

The embodiments that

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Dr. Banerjee seeks to define -- combine, differ in material ways such that a POSITA would not have been motivated to combine them.

Dr. Banerjee asserts that his declaration relies on Kim's Figures 17A to 22B embodiment, comprising an etch-stop and barrier layer.

However, Dr. Banerjee relies on embodiment in Figures 4, 8A and 8B as purportedly disclosing a gate-stack-on-top arrangement.

Specifically, Kim's disclosure for these figures states that in embodiments "each of the top surfaces of the sacrificial SC1 to SC8, not the top surfaces of the insulating layers 111 to 118, may be partially exposed in the word contact region."

Dr. Banerjee argues that this means of sacrificial/gate stack layer is disposed on top of the dielectric layer in this embodiment.

Dr. Banerjee then concludes that because this language is absent from the

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description of the embodiment in Figure 17A to 22B, it must still apply was simply omitted as an "overlapping description."

Notably, the embodiments of 17A to 22B does not only exclude the language from Kim's paragraphs, but actually replaces it with a description demonstrating a gate-stack-on-the-bottom ordering for sacrificial/gate stack and dielectric layers.

Kim explains that the etch-stop layer 125 "conformally covers an exposed surface of the stack layer structure" but covers only the "end portions" or "side walls of the sacrificial layers SC1 and SC8 in the contact region."

By explaining the etch-stop covers only the end of the portions or the side walls of the sacrificial layers, Kim demonstrates a sacrificial layer is underneath the dielectric layer.

Despite how it might be drawn, to be consistent with Kim, the side wall -- the stacked layer structure only covers only the end portions and side walls of the

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sacrificial layers. So the layers in which they are covered by only the side walls have to be the end portions in the sacrificial layers.

Thus, it's my opinion the embodiment described in these paragraphs upon which Dr. Banerjee relies for the gate-stack-on-top disclosure does not apply to the embodiment in Figure 17A to 22B.

And with that, I noticed that we are over an hour. I wonder if we could take a short break.

Q Just a few minutes.

MR. DUNTEMAN: Counsel, are you just thinking like one or two to wrap up this issue?

MR. HSU: Don't worry, Dr. Campbell will get his break very quickly.

MR. DUNTEMAN: Counsel, he asked for a break. I think it's fair. We said an hour at beginning of the --

MR. HSU: Bobby, Bobby, I need to respond to Dr. Campbell's previous answer.

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BY MR. HSU:

Q I'm going to strike that answer as unresponsive. I noticed that you basically read selected portions of paragraphs 36 through 41 and perhaps more, typos included. So I'm going to strike that answer.

MR. HSU: And with that, we can go on a break.

THE COURT REPORTER: Okay. We're off the record at 10:08 a.m.

(Recess taken 10:08 a.m.)

(Resumed 10:20 a.m.)

BY MR. HSU:

Q Welcome back, Dr. Campbell.

A Thank you.

Q You recall right before the break you gave a long answer to my question, correct?

A Yes.

Q Did you read from paragraphs 36 through 41 of your declaration?

A Yes.

Q I am here today to explore what your thinking was behind your declaration.

Reading off your declaration isn't going to help me and isn't going to help you. I just want to make that --

MR. DUNTEMAN: Objection. Argumentative.

BY MR. HSU:

Q Anyway, with that, let me go back to my previous question.

So it sounds like you agree that Dr. Banerjee opined on an embodiment -- strike that.

It sounds like you agree that Dr. Banerjee opined on a configuration that has gate stack on top for Kim's Figure 17A through 22B embodiment, correct?

MR. DUNTEMAN: Objection. Mischaracterizes testimony.

A This is --

MR. DUNTEMAN: Hold on. Objection. Mischaracterizes testimony.

Go ahead, Dr. Campbell.

A This is where we disagree. Dr. Banerjee has drawn a gate-on-top structure, but it's not Kim's structure, as

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I described in paragraph 41.

I know you don't want me to read it again. But if you are, I'd be happy to read it.

Q I don't think we disagree, but let me ask a clearer question.

Do you agree that Dr. Banerjee reversed or inverted the order of layers in each step from Kim's Figure 17A through 22B to opine on a gate-stack-on-top configuration?

A Yes. He started from Kim's gate stack on bottom and changed colors and labels to wind up with a gate stack on top.

But I repeat that this is not Kim's. It directly contradicts what Kim says in his patent.

Q During this deposition, I may variously refer to the reversing of the layers as a layer reversal or layer inversion.

Would you understand what I'm referring to?

A I believe you would mean that you change the positions of the stack, a

gate stack in the dielectric layer.

Q By that, I simply mean whereas Kim's Figure 17A through 22B expressly shows a gate-stack-on-bottom configuration, Dr. Banerjee inverts or reverses that order in each step to show and opine on a gate-stack-on-top configuration.

Is that fair?

A Yes, it is a gate stack on top, but it's not Kim's. I agree it's a gate stack on top. But you can draw that from nothing.

Q Would you agree that the gate stack or sacrificial layer on top configuration is formed by starting with the insulator rather than the sacrificial layer during the deposition process?

A Yes. That's how you do it.

Q So let me drop in Exhibit 1005.

Let me know when you have it.

A One second. Okay, I now have Kim.

Q Okay. And this is the Kim reference that both Dr. Banerjee and you have reviewed, correct, and opined on?

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A Yes, that's correct.
Q Okay. So let's turn to Figure 5A of Kim.
A Yes, I'm there.
Q So in your previous answer, you agreed that the sacrificial layer on top configuration is formed by starting with the insulator rather than the sacrificial layer during the deposition process.
Do you recall that?
A Yes.
Q Okay. So looking at Kim's Figure 5A, what Kim shows is depositing the layer SC1 before -- strike that.
What Kim Figure 5A shows is depositing the sacrificial layer SC1 and then followed by depositing the insulator layer or dielectric layer 111, correct?
A Yes, that's correct.
Q And then it repeats, another sacrificial layer and another dielectric layer, and so on. Correct?
A Yes.
Q So the layer reversal or inversion that Dr. Banerjee opined on would

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mean depositing layer, dielectric layer 111 followed by depositing sacrificial layer SC1, and then repeat that same order, correct?

A Yes, that's correct.

Q Basically reversing the order of deposition of the first two layers and then proceed from there through the steps, correct?

A Yes.

Q Now, going to Kim Figure 17A -- let me know when you're there.

A I'm there.

Q That reversed sequence of deposition that we just discussed would apply to the Figure 17A embodiments if or when Dr. Banerjee reverses the order of the layers, correct?

A If you reverse the sacrificial layers and dielectric layers, you would no longer be in agreement with Kim's structure for where the 125A and B go on the staircase. He's very clear on this.

And I argue that if you do that, it's no longer Kim.

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Q That wasn't my question. I was simply asking --

A All right.

Q No worries. No worries.

I was simply asking, we had agreed earlier that reversing the layers simply means when you're depositing the alternating layers to form the staircase, you start with the dielectric layer as opposed to the sacrificial layer, correct?

MR. DUNTEMAN: Objection.

Hold on. Hold on.

Objection. Mischaracterizes testimony.

Go ahead, Dr. Campbell.

A You didn't give me a designation as to where these layers would be -- or maybe I just missed it.

I'm sorry. Go ahead.

Q No need to apologize.

You testified that reversing the layer orders means instead of depositing the sacrificial layer first followed by the dielectric layer, for example 111, you would start by depositing the dielectric

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layers, for example 111, and then followed by depositing the sacrificial layers. Correct?

A Yes.

MR. DUNTEMAN: Same objection.

BY MR. HSU:

Q And that reversal applies to Figure 17A, correct, if Dr. Banerjee is to reverse the layer, correct?

A Yes.

Q Now, earlier you had testified about replacing the sacrificial layer with a gate stack.

Do you remember that?

A Yes.

Q Now, what is that process of replacing a sacrificial layer with a gate stack?

A As applied to 3D NAND, the sacrificial layer is typically silicon nitride. You etch the silicon nitride in a hot phosphoric acid, which dissolves the silicon nitrate.

Then next step, if you are going to use tungsten for your gate, you use

atomic layer deposition process to coat the surfaces of the dielectric layers with typically hafnium oxide, usually a fairly thin layer, and then fill the remainder of the sacrificial volume with tungsten.

Q You mentioned first there's an etch using phosphoric acid to dissolve the -- what is typically a silicone nitride sacrificial layer, correct?

A Yes.

Q How does a POSITA control that process so that the acid etch away what is -- what is intended to be etch away and not more?

A Well, fortunately, this is a purely chemical etch. There is no ion bombardment. And in wet chemical etches, you can have extremely high selectivity, and selectivity etching nitride over SiO2 is ridiculously large.

So you really don't have to worry about breaking through. You just have to leave it in there long enough to dissolve a nitride and allow the byproducts to come out by diffusion.

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Q Now, the '276 Patent and the references that discuss 3D NAND staircase structures, they have an insulating layer that's on top of the staircase that sort of have an inverted shape of staircase that covers the entire staircase, correct?

MR. DUNTEMAN: Objection.

Vague.

A Sorry, which -- let's start by, where are we? Are you talking about Kim still?

Q I'm talking about generally.

I was trying to establish the fact that there's this upper insulating layer that covers the staircase that rests on either the etch-stop layer or the staircase insulating layer.

Do you -- are you with me so far?

A Yes, I understand that.

Q Okay. So different references call this insulator layer by different names. But just for simplicity, would you understand if I used the term upper insulating layer to refer to that structure

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or layer that we just discussed?

A Yes, that's fine.

Q Okay. So, for example, just to -- just so that we're on the same page, in Kim we were looking at -- well, this is not -- let's look at Kim 32 -- sorry 22A.

A One second. I'm trying to find it. Okay, 22A?

Q Yeah. So just for -- just for clarity, what I'm referring to by the upper insulating layer, for example, corresponds to Kim's interlayering pattern 134.

A Yes.

Q Okay. Now, would you agree that at the time the sacrificial layers are etched away, this upper insulating layer is already formed and in place?

A Yes.

Q So is there a concern over the phosphoric acid eating into the upper insulating layer when the sacrificial layers are etched?

A Typically, the upper layer 134 is silicon dioxide. And as I just testified, phosphoric enters silicon

nitride very effectively, not silicon oxide.

Q How would you define or describe an etch-stop layer?

A An etch-stop layer is a layer of material that etches at a slower rate than the material above that layer in a given etch system, whatever that etch system is.

Q And would you agree that the etch-stop layer is used to protect materials underneath the etch-stop layer?

A There can be multiple reasons, but that's certainly a common one.

Q What are others of the multiple reasons that you have in mind?

A Well, it might be that you are trying to maintain topography under it. It often happens that the breakthrough is not uniform across a structure.

I don't know. I've seen etch-stop layers used in lots of steps. But as I say, most the common is to protect what's underneath.

Q So first let me set the context since you mentioned that you've seen

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etch-stop in lots of -- used in a lot of different ways.

When I'm talking about etch-stop layers today, I'm referring to anything that might function as an etch-stop, but in the context of 3D NAND memory staircase. Okay?

A Understood.

Q All right. Now, how -- strike that.

You mentioned maintaining topology underneath the etch-stop.

Is that different from protecting the structure, from protecting the underlying structure?

A Yeah, it's very similar. It's just a question of, in the application, are you concerned about the electrical behavior of the layer beneath it or in this particular case that I refer to they're more concerned about the optical properties of the structure. And so the non-uniform attack in the other layer, in the lower layer, was a concern.

Like in the end, it comes down

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to etching the underlying layer.

Q Can you explain what you meant by non-uniform attack on the other layers?

A When you have an etched process, it is common for the etch to complete etching at the center of the structure to hold and then goes out to the edges.

If you go to the etch process, it isn't a big effect, but it is an effect.

And so if you were, as we are discussing here for the 3D, you want to make sure that all parts of the etch-stop is sufficiently thick that the etch process does not penetrate anywhere, all the way through the etch-stop anywhere on the pad.

Q And in your previous answer, you ended with "it comes down to etching the underlying layer."

Can you explain what you meant by that?

MR. DUNTEMAN: Objection.

Mischaracterizes testimony.

A Certainly. I'm a little mystified where the confusion lies.

The sacrificial -- sorry -- the

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etch-stop layer is, in the 3D case, intended to prevent unwanted etching of layers underneath the etch-stop layer.

Is that -- I'm not sure I understand the question, I guess, because that's what was intended.

Q And the purpose of the etch-stop layer, as you frame it to prevent unwanted layers of etching underneath the etch-stop layer, is accomplished by the etch-stop layer stopping or as more realistically significantly slowing down the etch process when the etch reaches the etch-stop layer, correct?

A Yes, that's correct. I'd just add to it, again, that the etch process is not completely uniform across the etched area. You have ion bombardment.

Typically, the charge is on the sides and that causes the ions to concentrate more towards the middle than the edges.

So when you say you want it to etch slowly, you would etch slowly enough that no portion of the etch-stop layer is

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going to be penetrated through.

Q And one of the ways of ensuring that the etch-stop layer etches slow enough is through etch selectivity, correct?

A Yes, etch selectivity and the thickness of the etch-stop layer.

Q And a properly designed etch-stop layer should not be penetrated during the etch of the upper insulating layer, correct?

MR. DUNTEMAN: Objection. Vague.

A Referring to layer 134 again?

Q By upper insulating layer as it pertains to Kim, yes, I'm referring to layer 134. But I was more asking a more general question.

MR. DUNTEMAN: Same objection.

A I'm sorry, could you repeat it one more time?

Q Certainly.

A properly designed etch-stop layer should not be penetrated during the etch of the upper insulating layer.

Would you agree?

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MR. DUNTEMAN: Same objection.
A Yes, I agree.
Q Now let's turn to your declaration, Exhibit 2019.
A Paragraph 19?
Q Sorry, I was saying Exhibit 19, paragraph 86, page 58.
A Yes, I'm there.
Q Okay. So towards the bottom of the page, you said that, and I quote here: "An etch-stop layer that is selective with the interlayer dielectric above it is simply a description of how an etch-stop layer functions."
A Sorry, can you tell me where this is exactly?
Q Oh, sure.
A On 86?
Q The fifth line up from the bottom on page 58.
A Okay.
Q It says -- I'm skipping the first part of the sentence, but -- "an etch-stop layer that is selective with the interlayer dielectric above it" -- I'm

skipping a couple of words here -- "is simply a description of how an etch-stop layer functions."

Do you see that?

A Okay. So halfway through, I see "the petitioner suggests a POSITA would have a reasonable expectation of success because both devices disclose an etch-stop layer" -- is this the right content?

Q Yes, that's right.

A Let me just finish reading the rest of it.

Okay, so do I agree with what it says? Yes, this is my testimony, yes.

Q What do you mean by that?

A So we have to refer to both devices. Same as primarily using carbon-doped silicon nitride. And I take it on this that the other device is Kim.

Kim suggested, I think there are four different etch-stop materials, whereas Fang had primarily the carbon-doped silicon nitride.

Now, is it going to work? You can't say because it all depends on your

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etch process -- well, it depends on lots of things, but certainly most importantly the etch process.

Are they both going to work? They both can work. But without knowing more about what the etch process is, what the thickness of these layers are, as we just discussed before, you can't -- you can't say for certain. They can be made to work. That's what I would say.

Q I'm not sure that answers my question, so let me try to ask it differently.

Is it fair that -- I'm omitting a few words, but I want to make sure you agree, first of all, that I'm characterizing your declaration fairly or correctly.

Is it fair to say that you opined that an etch-stop layer that is selective with the interlayer dielectric above it is simply a description of how an etch-stop layer functions?

A Yes, that's correct.

Q So my question is, what does

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that mean?

A It means that the etch-stop, as we described before, it has to not be penetrated under -- and maybe this is where we have to add a bit -- under worst case conditions.

So in the case of 3D, you have different etch steps and the etch-stop has to protect whatever's underneath in the worst-case scenario, which would be the shallowest content.

Q And how does -- strike that.

In the description that I've read from your paragraph 86, the word selective refers to etch selectivity, correct?

A Yes.

Q How does etch selectivity help in achieving this objective of not allowing the etch-stop to be penetrated even when the contact holes to be etched have very different depths?

A Well, you have two important primers. Assuming that the plasma etch is fixed, that isn't necessarily the case.

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You can modify the plasma etch.

But let's assume that's fixed, you have two parameters; one is the etch rate of the material, the etch-stop material, under the plasma conditions; and the other is the thickness of the etch-stop layer.

Q How thick is the etch-stop layer compared to the thickest portion of the upper insulating layer?

MR. DUNTEMAN: Objection.

Vague.

A Of course, it depends on what your etch-stop material is. The selectivity can be dramatically different. It can vary by orders of magnitude.

Usually, you can get one that's a fairly good etch-stop and it would be much thinner than the depth of the shallowest etch hole.

Q And since the etch-stop layer is much thinner than the depth of the shallowest etch hole, the primary mechanism that the etch-stop rely on for -- to perform its function of not allowing

penetration when the contact holes are etched is primarily the etch selectivity rather than the thickness.

Would you agree with that?

A No, I wouldn't. Both are important. One is just as important as the other.

It is a benefit to find one that has a high selectivity. That's certainly true. But there are often tradeoffs that make it difficult to use the highest selectivity materials.

Q I understand that. So let me ask a more clear question.

Now, would you agree that by the time the '276 Patent, for example, a 48-layer staircase was common?

A Yes. According to the Applied Materials roadmap for 3D NAND, it's in the range of -- I think it was -- yeah, it was a little bit higher than you said, but that's -- that's in the range.

Q And would you agree that -- take a 48-layer staircase as an example -- the deepest contact hole is much, much longer

than the shallowest contact hole?

A Yes, certainly that's true.

Q So -- strike that.

And you had testified that the etch-stop layer is much thinner than even the shallowest hole, correct?

A Yes. I explain that. I said that.

Q And so I appreciate the fact that, of course, the thickness of the etch-stop layer is an important factor, but the etch selectivity is a key parameter, correct?

For example, you can't have, possibly have an etch selectivity of even two to one if you're etching a 48-layer staircase.

Would you agree?

MR. DUNTEMAN: Objection. Calls for speculation.

A In general, I would agree.

Certainly, as the 3D technology has evolved, there have been emphasis on highest selectivity etch-stops.

Q In general, the higher the etch

selectivity, the better the etch-stop is in performing its function, correct?

A One would hope it was that simple.

There are many things to consider. You have to -- ultimately, you have to get rid of that etch-stop layer in order to access the layers down below.

Is there an etch that I can use to remove the etch-stop layer when it is no longer needed while preferably not attacking aggressively the layer underneath? You want to go through these layers in a controlled manner.

Or there may be residue being left by the etch. Some things are very hard to volatilize.

So I would say yes, you would like to have a very high -- sorry -- a very high selectivity rate. There are constraints.

Q Now, you talked about removing the etch-stop layer when it is no longer needed.

By that are you referring to the

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fact that the etching of the contact holes after penetrating the upper insulating layer has to penetrate the etch-stop layer?

A Initially, it has to reach the gate, otherwise it's not functional. So yes, it has to go through the etch-stop layer.

Q And in order to penetrate the etch-stop layer, since -- strike that.

In order to penetrate the etch-stop layer, the etch chemistry needs to be changed from the etch chemistry that is used to etch the upper insulating layer, correct?

A Exactly so.

Q And these contact holes, 3D memory structures, they have high aspect ratios. Would you agree?

A Yes.

Q You've mentioned, I think, ion bombardment and such. Is that related to dry etch using plasma?

A Yes, that's one aspect of a dry plasma etch that is commonly used. It typically helps you get high anisotropy.

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Q By high anisotropy, you're referring to a high directionality such that it can achieve the high aspect ratio that's required of the contact holes, is that correct?

A Yes, that's correct.

Q And so from what you have testified, I think you would agree with this, but let me make sure based on your testimony, that the etch-stop layer protects the underlying structure until all of the contact holes or via openings are formed throughout the staircase structure.

MR. DUNTEMAN: Objection.

Vague.

BY MR. HSU:

Q Do you agree?

A The only caveat is in some technologies they will etch in groups and not all at once.

So what you said is right for the batch that's currently being etched.

Q How does that etching in groups happen?

MR. DUNTEMAN: Objection.

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Vague.

A There are a couple of options. One is to etch all of the contacts up to a certain depth so that the shallow ones are open and then either cover up -- that's a common thing, and you can do another masking step that protects the shallow ones and it just opens up the deep ones, and so you etch again on the deeper ones -- yeah.

Q So covering up the shallower contact holes using a mask, is that correct?

A Uh-huh. Well, you're using a mask any time you do etching unless you're etching everything. So yeah. It's just another masking step.

Q You mentioned a couple of options, and you provided one. Is there another option or two?

A Another option for -- I'm sorry, for what exactly?

Q For etching in groups.

A Oh, yeah. In some cases, people will do this by -- same idea, you're going to etch the shallow ones first. But in

that step, you don't etch the deep ones. Then on the second round, you etch the deep ones with a different mask.

The downside is that you have to etch longer for the deep ones. The upside is you don't have to exactly perfectly align the contacts when you do the second round because they are -- they were not etched in the first etch process. So give and take.

Q Give and take, meaning that's an engineering tradeoff?

A Exactly.

Q And in both of these options, additional masks had to be used depending on how many groups you are etching the holes -- strike that. Let me rephrase the question.

In both of these options, to etch additional group of contact holes involves an additional masking step, is that fair?

A That's fair.

MR. HSU: We're almost at an hour. I think this is a good time to

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pause. So why don't we take our break.

MR. DUNTEMAN: Sounds good.

For us, Dr. Campbell, you want to take a half hour to grab lunch at this time?

THE WITNESS: Can we make it 45?

MR. DUNTEMAN: Sure.

THE WITNESS: Say noon?

MR. DUNTEMAN: Sounds good.

We'll reconvene at 1:00 Eastern Time, 12 Central.

THE WITNESS: Thank you very much.

MR. HSU: Thank you.

(Recess taken 11:19 a.m.)

(Resumed 12:00 p.m.)

BY MR. HSU:

Q Dr. Campbell, welcome back.

A Thank you.

Q Before the break, we discussed etching vertical contact holes in multiple groups as a way to address the fact that the contact holes need to be etched to different depth.

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Do you recall that?

A Yes, I do.

Q Now, after the contact holes of different depth have penetrated the upper insulating layer and reached the etch-stop layer, would a POSITA continue to etch in multiple groups to penetrate the etch-stop layer?

A No. Normally that's not what you would do.

Q Why not?

A Well, first of all, the material that you're using in the etch-stop was designed to etch very slowly in that plasma.

I'm -- make sure I'm understanding this -- I'm assuming you're not changing the plasma, you're just continuing the same chemistry?

Q Thank you for clarifying that. No, I did not mean to imply continuing the chemistry.

A Okay.

Q So let me reask it.

I understand from your earlier

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discussion that one would switch the etch chemistry to penetrate the etch-stop layer after the upper insulating layer has been penetrated, correct?

A When the upper insulating layer has been penetrated through all of the holes -- well, the deepest holes that were etched, yes.

Q And we discussed the fact that one way of etching these holes of different depth is to use multiple mask steps to etch the holes in multiple groups, right?

A Yes, that's correct. That can be done. That's an option.

Q So with the changing in etch chemistry that a POSITA would understand should be applied to etch through the etch-stop layer, would the POSITA continue to etch these etch-stop layer to penetrate an etch-stop layer in multiple groups like in that option of penetrating the upper insulating layer?

MR. DUNTEMAN: Objection. Form.

A They wouldn't be -- so if I make -- let me say what happens rather --

make sure I'm not mistaking your question.

If one were to do the etching by groups, you would etch all of the holes all the way down to the etch-stop layer, and that might be two groups or three groups or however you do it. Then you would change the chemistry and etch the etch-stop on all of the holes. There's no reason to not do all of the holes at the same time.

Q Why is there not a reason to not do all the holes at the same time through the etch-stop layer?

Actually, strike that. Let me not ask a double negative.

Why does it make more sense to etch through the etch-stop layers through all the holes at the same time?

A Okay. So I'll rephrase it then slightly.

There's a -- there's a modest advantage to go through all of the etch-stop layers at the same time.

So if your process is such that at the end of etching all of the layers down to the etch-stop layer, it would be

reasonable to continue to etch with the changed chemistry and go through the etch-stop layer.

I wasn't thinking about it in terms of having all those holes open at the same time. But yes, if you get to the point where all the holes are open, you need to switch and do the etch-stop.

Q Let me make sure we're on the same page because I may not have understood your previous answer the way you intended.

Maybe let me ask it differently.

You mentioned an option to etch through the upper insulating layer in multiple groups, right?

A Yes.

Q And we agree that change in etch chemistry will be required to etch through the etch-stop layer, right?

A Yes, right.

Q Does it make sense to -- in a situation where all the holes have reached the etch-stop layer, but have not penetrated the etch-stop layer, does it make sense to etch through and penetrate

the etch-stop layer in the changed etch chemistry by etching through them in multiple groups?

MR. DUNTEMAN: Objection. Vague.

And counsel, we've been kind of going for a while just talking in these general terms. What reference or part of the declaration are we talking about here?

MR. HSU: I think the question should be clear. I'm talking general terms.

MR. DUNTEMAN: You can answer, Dr. Campbell, but the objection stands.

A Well, when we talked about this possibility, this option for etching the contact holes, we said that there are two ways of doing it, one where you etch the shallow holes just by themselves and then cover them up, and the second group etch the deep holes.

At that point, the shallow holes are masked. And so you can't just put it

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into the etch tool for the etch-stop because they're masked.

On the other hand, if you do it where you etch shallow ones -- sorry, you etch all of them and then -- yeah, you have to make sure that the shallow ones are not covered. That's the issue.

Q I might not have been clear.

So I'm talking about a situation where -- actually, strike that.

Do you agree that the etch-stop layer is intended to make it unnecessary to apply multiple masks in doing the etching of the contact holes?

A I would say that the higher the selectivity of the etch-stop layer, the less need there is for doing etching in groups.

Q And do you agree that a POSITA would want to ensure the selectivity of the etch-stop layer is sufficiently high so that etching in groups would not be necessary?

A A POSITA would recognize the advantage from a manufacturing perspective

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of avoiding having to etch holes in groups.

However, as you said before, engineering tradeoffs, what is the tradeoff that you have to endure with some particular etch-stop layer. I could ask what material it is, what kind of etching you have to do. It's a very complicated structure.

But yes, if you can make it happen in a way that is realistic, that is to say you can yield it and it's not going to cause other problems and you have the tools for depositing this material and you have the tools for etching it, then yes, it's better to do it that way.

Q It's better to do it that way refers to ensuring the selectivity of the etch-stop layer is sufficiently high so that etching in groups would not be necessary, is that fair?

A The etch-stop selectivity is high enough and the thickness is large enough, yes.

Q So that all of the contact holes can be etched together as opposed to etched

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in multiple groups, right?

A Yes, that's correct.

Q And you're not suggesting that this cannot be done, correct?

A By this, you mean not doing end-to-end groups?

Q Right. Doing it all together.

A I would characterize this as one of the challenges in modern 3D. It can be done, but it is by no means simple.

Q For example, Kim doesn't etch its contact holes in multiple groups, correct?

A I'm sorry, what did you say, Kim?

Q Kim, correct.

A I would have to go back and look at Kim. That's not something I really studied. If you'd like, I could take the time to take a look at that.

Q But sitting here, you don't know one way or the other that Kim teaches etching the contact holes in multiple groups, correct?

A I don't have sufficient

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certainty in my response when I am -- where I could be labeled with perjury. I don't have that certainty, put it that way.

I don't think Kim did it in groups, but I would have to look to make sure.

Q Okay. That's sufficient.

Will your answer be the same for Fang, the Fang reference?

A Yes.

Q Will your answer be the same for the Chen reference?

A I know that one of them suggested that this was an alternative. They didn't say they did it. They just said it was an alternative. But I'm sorry, I don't remember which one.

Q Okay. Will your answer be the same for the '276 Patent?

A Yes. I don't recall doing it in groups in '276.

Q Do you have sufficient certainty in that answer?

A It's the same. I don't think of it, but again, I didn't really study this.

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Just to make a correction to what I had just said, I mentioned that one of the four references suggested the possibility of etching the groups, and I'm fairly certain that was Fang.

Q Now, you testified earlier that it would be better to penetrate all of the -- strike that.

You testified earlier that it would be better to penetrate the etch-stop layer across the entire staircase together as opposed to in multiple groups, right?

A Yes.

Q In the case where there is a barrier layer underneath the etch-stop layer, is the answer the same for penetrating the barrier layer?

MR. DUNTEMAN: Objection. Vague.

A Yes.

Q And in the case where there's a high-k dielectric around the gate conductor, is the answer also the same for penetrating that high-k dielectric layer?

A This gets into -- this is a

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question that is -- I don't have the information to answer.

I don't know what the etch chemistry is going to be, what the -- I haven't confirmed what it's going to be, how thick the layer is. There's just a lot of variables that go into that.

So I can't really say for sure. I don't have the information.

Q Under what parametric condition would a POSITA find it desirable to etch through the high-k dielectric around the gate conductor in multiple groups?

MR. DUNTEMAN: Objection. Vague. Unless you weren't done with your question, counsel.

A Again, are you asking what should this parameter be in order to make a decision? There's 20 parameters. It's -- there is no single parameter to say if this pressure is that, then it's good. But etch process is very complex.

I will say, however, just to point out that that liner is very thin. We're talking a few nanometers. I would be

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surprised if it was ever more than 5 centimeters. But still, I don't -- I'm not sure who they would go about etching it in the best process.

Q You mentioned 20 parameters. I take that to be an approximate number. Would that be fair?

A It might be a slight exaggeration, but it's certainly more than 10.

Q Is plasma power one of those parameters?

A Definitely. Yes, absolutely.

Q Is bias voltage one of those parameters?

A Yes, the bias voltage is a plasma parameter. You have two plasmas in a system typically, but yeah.

Q Is chamber pressure one of those parameters?

A Yes.

Q Is temperature one of those parameters?

A Yes, a very important one.

Q And is etch time one of those

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parameters?

A Sure, of course.

Q And is etch chemistry one of those parameters?

A Sure, but you got multiple things that are in the chemistry. I mean you probably have at least three different reactive species and inert species.

Q Are there additional parameters that come to mind?

A Before doing the etch, during a breakthrough, at the beginning of the etch -- what else...

You almost certainly want some etch-stop measurements. Yeah.

So those come to mind. If I were to sit here for a while, I might figure out a few more. But yeah, I said 10 and that's about right.

Q I missed the very first word you said in your answer, something and then chamber before doing the etch.

A You have to condition the chamber. You have to make sure that what's on the walls is the same as what you want

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to have on the walls rather than let's say air residue, water vapor, whatnot.

So yeah, you have to condition it if you want it to be repeatable.

Q Does the '276 Patent discuss conditioning the chamber?

A None of the patents that I've seen go on to that kind of specificity, not Kim, not Chen, not anybody.

Q Including the '276 Patent?

A Including the '276.

Q Is the answer the same if it's plasma power?

A Yes. You won't get any of those parameters.

Q Is your answer the same with respect to bias voltage?

A Yes.

Q Is the answer the same with respect to chamber pressure?

A Yes to all these things.

Let's point out here what's going on. These companies, Micron or YMTC, they buy the etch tool from Applied or -- I can't remember the other one -- and those

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companies make the recipes, and that is proprietary to the company that makes the machine.

So a company that's writing the patent can't put those numbers in the patent because -- well, you would be violating confidentiality.

Q Are you familiar with the concept of enablement in patent law?

A I am not a lawyer --

MR. DUNTEMAN: Objection. Relevance. This is beyond the scope of the deposition.

BY MR. HSU:

Q But you can answer.

A I am not a lawyer. I am not familiar with it.

Q Is a POSITA reading the '276 Patent able to make and use its invention without undue experimentation?

MR. DUNTEMAN: Same objection. This is beyond the scope of the deposition.

A A POSITA would know that Lam Research or Applied Materials have machines

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that will do the etch processes that are described in '276, period.

Q Would that answer be the same with regard to Kim?

MR. DUNTEMAN: Same objection.

A Yes. However, Kim calls out four different barrier layers, and so you would have to make sure they have recipes for all four of those, or you just select one, I guess, and go with it.

Q What do you mean by Kim calls out four different barrier layers?

A Etch-stop layers, sorry. Kim said for the etch-stop layers silicon carbide, silicon nitride, silicon oxycarbide, and silicon oxynitride.

Q But a POSITA would know that Lam Research or Applied Materials had machines that will do the etch process that are described in Kim, correct?

A They would contact those companies and say I'm interested in these materials as my barrier layers -- as my etch-stop layers, sorry -- and ask do you have, for these materials do you have

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recipes, and then you would go into a discussion with them with the aspects of the parameters of the etch set that you're going to need. And then they'll let you know if they do.

Q The same thing that it would do to implement the invention of the '276 Patent, correct?

A Yes, yes.

Q Is your answer --

A Go ahead.

Q Please finish.

A The etch process -- sorry, let's say this differently.

The process for fabricating the devices in '276 is a roadmap for how you do the steps to get from A to B, what layers you're going to put down, where they are, when they're done and other parameters.

But as to the specific etch, it is not stated and it never is stated.

Q And that is the same with respect to all of the references that are used in the grounds of the petition, correct?

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MR. DUNTEMAN: Objection. Compound.

A To the best of my knowledge, that answer is true.

Q Now, we were talking about etch. Hydrogen bromide is denoted by the symbol HBr, correct?

A That's correct.

Q And argon is denoted by the symbol Ar?

A That's correct.

Q And etch can be done using a hydrogen bromide and argon plasma, correct?

A It can, yes.

Q And are you familiar with the expression HBr plus Ar?

A Yes.

Q Is that a hydrogen bromide and argon mixture?

A Yes.

Q Is it fair to say that the etch-stop layer provides its protective function relative to the etching of the layer that's immediately above it?

A Can you say that again?

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Q Is it fair to say that the etch-stop layer provides its protective function relative to the etching of the layer that's immediately above it?

A Yes.

Q In other words, the layer that is in direct contact with the etch-stop layer that is being etched, right?

A Yes.

Q And when a layer is covered and isn't exposed to the plasma, it doesn't serve as an etch-stop function, right?

A When it's covered? Do you mean it's masked in some way?

Q When a layer is not exposed to the surface and therefore isn't exposed to the plasma, it doesn't -- that layer doesn't serve an etch-stop function, correct?

A Yes.

Q So do you agree that the layer or the layers above, the immediately above layer does not affect the etch-stop characteristic?

A Again, you're going to have to

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say that -- it was rather garbled.

Q Sure.

That's -- that's -- think about this hypothetical where you have, let's say, five layers, starting from the bottom, one, two, three, four, five -- okay? With me so far?

A Yes.

Q Let's say my layer number two, the second from the bottom, is my etch-stop layer. With me so far?

A Yes.

Q So I think you agree that that layer serves as an etch-stop when layer number three that's immediately above layer number two is etched, correct?

A Yes.

Q But layer number two does not serve as an etch-stop during the etch of layers four or five, correct?

A Presumably those layers are gone. I might be getting this the opposite way.

Q Actually, let me just clarify your answer.

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I understood your answer to be that when layer two serves its etch-stop function, during the etching of layer number three, layers number four and five above layer number three would have already been penetrated. Is that fair?

A Yes. Number three has to be exposed if you're going to etch it.

Q And, therefore, is it fair to say that layer number four and layer number five does not affect the characteristic of etch-stop layer number two?

A Four and five are the top ones?

Q Correct.

A Yes. I don't see how they could impact the etch-stop layer on two.

Q Now, we were talking about plasma. Using a plasma etch involves volatilizing the material that is etched, right?

A That is correct.

Q Does silicon oxide volatilize in a fluorine plasma?

A Normally, yes.

Q And that means the fluorine

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plasma can be used to etch silicon oxide, correct?

A Again, yes. It depends on the power of the plasma. It depends on the pressure. But yes, in general, fluorine can attack SiO2.

Q Does silicon nitride volatilize in a fluorine plasma?

A Yes, it can.

Q And that means a fluorine plasma can be used to etch silicon nitride, correct?

A Yes, a fluorine-containing plasma can etch nitride.

Q Does a high-k dielectric volatilize in a fluorine plasma?

A Generally speaking, no, not in fluorine.

Q And that means a fluorine plasma cannot be used to etch a high-k dielectric, correct?

A Cannot is a strong word. There is some etching, but not very much.

Q That's fair.

A POSITA would not intentionally

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use a fluorine plasma to etch a high-k dielectric, correct?

A Yes.

Q Whereas a POSITA might use a fluorine plasma to etch silicon oxide or silicon nitride, correct?

A If we're talking about action silicon nitride, Si3N4, yes.

Q Do you agree that the etch-stop layer cannot protect the underlying structure during the formation of the plurality of openings if it has already been penetrated?

MR. DUNTEMAN: Objection.

Vague.

A Let me ask you to repeat it again.

Q Sure.

Do you agree that the etch-stop layer cannot protect the underlying structure during the forming of the plurality of the vertical openings if it has already been penetrated?

A Yes.

Q In other words, an etch-stop

layer no longer functions as an etch-stop once it has been penetrated, correct?

A Again, it comes back to in reality it isn't completely uniform, the etch. And so yes, it will start attacking what is underneath. And as the etch-stop completely erodes, the attack rate won't increase. So it isn't a zero to one. It just starts eroding.

Q Right.

And a POSITA would understand and appreciate what you have just explained and design an etch-stop layer with etch selectivity and thickness to minimize the possibility of it being penetrated before all of the vertical openings are formed, correct?

A Yes, that's correct.

Q You mentioned the term punch-through in your declaration.

Can you describe the term punch-through?

A Punch-through just means that you have eroded at least some of -- well, you have completely eroded the etch-stop

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layer at least in some area.

Q That you have completely eroded an etch-stop layer, at least in some area, before all of the contact holes are formed and therefore the etch continues below the etch-stop layer before it is intended to happen. Is that fair?

MR. DUNTEMAN: Objection.

Vague.

A Yes. Yes, I think that's a fair assessment.

Q And punch-through would represent a failure of the etch-stop layer, correct?

A I don't know that that's 100% certain. If, for example, what's under the etch-stop layer is a buffer, we're not going to keep that buffer anyway.

And so if it were to etch slightly into the buffer, people might say that it did its job, because it didn't get to the gate. The gate is the part of the device that has to be retained to make a good contact.

Q So let me make sure we are on

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the same page with respect to the term punch-through.

I think I understand you to be saying punch-through refers to penetrating the etch-stop layer before the penetration is intended to occur as opposed to punch-through referring to etching through the gate conductors and causing problems from that over-etch. Is that fair?

A No. Perhaps what I said was somewhat garbled.

Ultimately what you're concerned about is damage to the gate layer, and punch-through is when we start to etch into the gate layer.

Q And causing damages to the gate layer, is that fair?

A Yes.

Q So then punch-through would represent a failure of the etch-stop layer. Is that fair?

A Yes, if the damage to the gate layer is sufficient such that you can't make a contact to it, that's ultimately the failure.

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If it only etches a very small amount at the surface, I don't think you necessarily would call it punch-through because it's still functional.

Q Right.

But if -- if during the etch of the upper insulating layer the shallowest hole already reaches the gate conductor, that penetration will deepen when the layers between the upper insulating layer and the gate conductors are etched in subsequent etch steps, correct?

A Yes, of course.

What I'm saying is if -- if any of the contacts, the gate contacts are open, open circuit, there's a failure. That punch-through has happened. And, of course, it's going to be most likely at the shallowest contact.

But if all of them are -- all of the contacts are continuous and the gates are contacted, I would say we haven't had a punch-through on it.

Q A POSITA would understand that after etching through the upper insulating

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layer, additional etch-stop -- sorry, additional etch step needs to occur to extend the contact holes to the gate conductor layer, correct?

A Yes.

Q And those intermediate layers are relatively uniform from the perspective of contact hole etching, is that right?

A Relatively uniform in the lateral direction, vertical direction?

Q In the vertical direction of contact hole etching.

A Yes, they're relatively uniform.

Q And so it would be desirable to etch through these intermediate layers, meaning starting from the etch-stop layer to whatever is immediately above the gate conductor to etch through these layers approximately in lockstep, in a uniform manner.

Would you agree?

A Yes.

Q Now, I think you also testified that these intermedial layers are relatively thin, correct?

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A Yes, that's true.

Q So would it be desirable to slow down the etch through these intermedial layers as the etch approaches the gate conductors?

A It all depends on the chemistry that you use. If you're using a fluorinated chemistry, fluorine attacks tungsten very effectively, then you would want to be very careful that you don't volatilize much of the tungsten gate.

If you're coming in with something else that doesn't volatilize tungsten, you have less of a concern there.

Q But would it be fair to say that a POSITA would not find it desirable to actually etch faster through these -- through these thin layers, thin intermediate layers?

A The most important thing is that it is controlled. If you have multiple layers, the ideal situation is to etch each one with -- design the layers with a degree of selectivity so that you etch the etch-stop and stop, and then etch the

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barrier and then stop, and then etch the high-k and then stop. Because you want to -- there are variations in thicknesses, there are variations in the etch, and what you want to do is not let those variations accumulate.

Q The ideal situation you described to etch through the etch-stop layer and stop, and then etch through the barrier layer and then stop, and then etch through the high-k layer and then stop, is it fair to say that through these three steps, each time the immediately underneath layer is serving as an etch-stop when the immediate layer above is being etched?

A Yeah, it's not a very good etch-stop because you don't have the thickness difference that you have in what we call a normal etch-stop, right.

The upper insulating layer, I think we called it, is many times larger, thicker than the etch-stop layer, whereas here the thicknesses are not dramatically different. So selectivities of two to one would be just fine.

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So you can call them an etch-stop, but it's not a great etch-stop.

Q Etch selectivity is not dramatic, but it does have the etch-stop function of slowing down the etch, correct?

A Yes, that's correct.

Q Is it fair to say that in this ideal situation you've described, all of the contact holes extend their depth through the etch-stop layer and the intermedial layers and ultimately reaching the gate conductor in roughly a uniform manner?

A Yes.

MR. HSU: This is a good time to pause. We are roughly at a one hour, Mark. So let's take our next 10-minute break.

(Recess taken 12:58 p.m.)

(Resumed 1:11 p.m.)

BY MR. HSU:

Q Dr. Campbell, recall earlier we were talking about this five-layer structure with layer one on the bottom, layer five on top?

A Yes, I recall it.

Q Okay. So I'd like to go back to that structure.

Let's say I want to etch through layers from the top five, four, three, two, to reach layer number one.

With me so far?

A Yes.

Q I think from your earlier testimony, you will agree that when layer number five at the top is being etched, only layer number four serves as an etch-style function and layers two and three are not etch-stops, correct?

A No, I don't agree with that.

An etch-stop layer has the trait that it has a lower etch rate than the material above it.

So if you're etching the top-most layer and you're not penetrating through that layer, the next down layer isn't an etch-stop, it hasn't been -- the etch hasn't reached it yet.

So I can't say it's not an etch-stop or it is an etch-stop. It's

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irrelevant at the moment.

Q Let me make sure I understand your testimony.

During the etching of layer five, the top most layer, layer number three isn't an etch-stop because etch hasn't reached it yet, and so it's -- layer number three is irrelevant at the moment.

Did I understand that correctly?

A Let me try to rephrase it.

When you say layer three is an etch-stop, or not an etch-stop, you have to say to what. It could be an etch-stop to layer four. I don't see any way it could be an etch-stop to layer five because they're not in contact with each other.

I guess if layer four were extremely thin, although I've never thought of things this way, normally etch-stops are directly in contact with the material that you're etching.

Q So if I have designed layer four to function as an etch-stop to layer five, at the time that layer five is etched, layer three is irrelevant because the etch

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hasn't reached it correctly, is that correct?

A Layer three may be an etch-stop, layer two, layer four. I don't know that.

The etch-stop layer has -- in my understanding, the etch-stop layer has to be in contact with the layer that it is being related to.

When you say an etch-stop, it has an etch difference of some ratio. And so you have to have two materials and those two materials have to be in contact.

Q In other words, where an etch-stop functionality is desired for layer -- for the etching of layer five, one would intentionally design layer four to be an etch-stop because layers four and five are in direct contact. Fair?

A Yes, but if you just need an etch-stop for layer five and you don't care about layer four, you can blow through four and still stop the etching.

Normally, etch-stops refer to two layers in contact.

Q Okay. When you say if you don't

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care about layer four you can blow through layer four and stop the etching --

A Right, and then layer three is an etch-stop to layer four.

Q Layer three is an etch-stop to layer four during the etching of layer four?

A Yes.

Q Is that right?

A Yes, that's correct.

Q But layer three is not an etch-stop during the etching of layer five, is that right?

A It's not acting as an etch-stop, but it still is an etch-stop layer to layer four. They're in direct contact and presumably they have a different etch rate.

Q Do you agree that the Kim reference discloses an etch-stop layer over a 3D memory staircase structure?

A Perhaps you can make sure we get this right, and let me know either Kim -- where Kim is or where the declaration is.

Q Sure.

Kim, I think it was previously

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dropped in through chat, Exhibit 1005. We can look at Figure 22A.

A 1005?

Q Yes. Figure 22A, that would be page 39 of the PDF, I think.

A Okay. Yes, I remember it now.

Q So let me reask the question.

Do you agree that Kim discloses an etch-stop layer over a 3D memory staircase structure?

A My recollection of this is that 125A and 125B are -- well, 125B is an etch-stop -- yeah, 125B is an etch-top layer, and I believe it is still a --

Q And --

(Simultaneous crosstalk.)

A Although as I mentioned before, Kim did have four different possibilities for that layer.

Q And 125B is relabeled as 126B after the very top surface has been removed, correct?

A Yes, I believe that's right.

Q Okay. Now, I just dropped in Exhibit 1006, that's the Fang reference.

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A Fang.
Q Okay. So let's go to Figures 5 and 6. That's page 4 of the PDF.
A Yes.
Q Do you agree that Fang discloses an etch-stop layer over a 3D memory staircase structure?
A Yes, layer one three is an etch-stop layer.
Q That's layer 130?
A According to paragraph 20, an etch-stop material -- oh, I'm sorry, 130. My apologies.
Q Now, turning to the Chen reference, which is Exhibit 1008 --
A Yes.
Q -- that was also dropped in earlier and we can to Figures 7A and 7B on page 7 of the PDF.
A Yes.
Q Do you agree that Chen discloses an etch-stop layer over a 3D memory staircase structure?
A Yes, I believe it's silicon nitride over silicon dioxide.

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Q Going back to the Kim reference --

A Yes.

Q -- Exhibit 105. Do you agree that Kim's Figures 5A through 14B together illustrate one embodiment?

A Give me the numbers again?

Q 5A through 14B. And I'll also point you to paragraph 57, if that helps.

A Yes, okay.

Q And do you agree that Kim's Figures 17A through 22B together illustrate one embodiment? And I might point you to paragraph 183.

A The paragraph again?

Q 183.

A Thank you. Yes.

Q Now turning to paragraph 35 of your declaration.

A All right.

Q You said that Dr. Banerjee argues that other embodiments from Kim support inverting the layers of the -- strike that.

You said that Dr. Banerjee

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argues that embodiments from Kim supports inverting the order of these layers, is that correct?

MR. DUNTEMAN: Objection. Mischaracterizes the declaration.

A Repeat the question again, please?

Q Sure.

In paragraph 35, you said that Dr. Banerjee argues that other embodiments from Kim support inverting the order of these layers, meaning the sacrificial and the dielectric layers, correct?

MR. DUNTEMAN: Same objection.

A So 22A is a heavily modified diagram that Dr. Banerjee set up.

I believe that Dr. Banerjee believes that is the embodiments supporting the inverting layers, but I certainly don't see them.

Q Well, I understand that you disagree with Dr. Banerjee's layer inversion. But you don't dispute that other embodiments from Kim discloses inverting the order of these layers,

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correct?

A I would have to go back to Kim and look at those figures one more time. Kim is 1005?

Q Kim is 1005.

Actually, I'll refer you to your declaration, paragraphs 40 and 41.

A Okay.

Q Where you cite Kim, paragraph 90 and 91. So why don't you go ahead and review those two paragraphs first.

A So I do agree with what we've written here in 40, that Dr. Banerjee argues this means the sacrificial/gate stack layer is disposed on top of the dielectric layer in this embodiment.

THE COURT REPORTER: I'm sorry, could you repeat that answer again?

THE WITNESS: Sure.

A I just briefly summarized the end of paragraph 40. Dr. Banerjee argues this means the sacrificial/gate stack layer is disposed on top of the dielectric layer in this embodiment.

Dr. Banerjee then concludes that

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because this language is absent from the description of the embodiment in Figure 17A and 22B, it must still apply and was simply omitted as an overlapping description.

I don't see it that way. I think this patent is well-written. And as we said before, as in 41, it doesn't follow the requirements. It doesn't follow -- it says the 125 layers are not properly aligned.

MR. HSU: Can we go on a slight break? Off the record.

(Recess taken 1:34 p.m.)

(Resumed 1:35 p.m.)

A So summarizing paragraph 40 and briefly 41, Dr. Banerjee argues this sacrificial/gate stack layer is exposed on top of the dielectric layer in the embodiment.

Dr. Banerjee then concludes that because this language is absent from the description of the embodiment, it must still apply and was simply omitted.

As it says there, I disagree. I think this was -- he wrote a relatively

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well-written patent and what he wants to be there was not there.

And then in 41, I'll just say briefly again, the barrier layers are not where they're supposed to be in the construction that Dr. Banerjee set up. Specifically, the 125A is not in the right area.

Q I understand that you dispute Dr. Banerjee's layer inversion with respect to the Figures 17A through 22B embodiment.

The question is: You don't dispute that Kim discloses this layer inversion respecting the Figures AA, AB embodiment, correct?

A Kim does have those figures. So to the extent that they are there, yes, they are there.

Q In paragraph 41, and I'm near the top of page 28, the second line from the top, you said: Covers only end portions or side walls of the sacrificial layers SC1 to SC8.

Do you see that?

A Yes, I do.

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Q Did you mean to say that the end portions and side walls mean the same thing?
A It was my interpretation, yes.
Q Okay. Let's turn to the Chen reference.
A The number?
Q Exhibit 1008.
A Okay.
Q Okay. Let's turn to Figure 8C and 8D, page 9 of the PDF.
A Yes.
Q What do you understand these figures to depict?
A This is a band diagram showing the energy levels for the conduction and bands for the addition of a high-k material along the side walls of the steps.
Q Did you say a band diagram or a Venn diagram?
A B-A-N-D, band, an energy band diagram.
Q And I'll refer you to paragraph 50. Figure AC shows a two-layer etch-stop configuration, correct?

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A Yes, I see that.
Q Okay. And in the Figure AC configuration, silicon oxide is the first stop layer to 10 and silicon nitride is the second stop layer to 20, correct?
A Yes.
Q And Figure AC shows a tunneling length of L3, correct?
A Yes.
Q I'll refer you to figure -- sorry, paragraph 52.
In the Figure 8 -- sorry, in the Figure 8D configuration, silicon oxide is the first stop layer 210 and aluminum oxide is the second stop layer 220, correct?
A I'm just catching up to you. I'm sorry, 52?
Q 52, right.
A Yes.
Q So the silicon nitride stop layer Figure 220 of Figure AC is substituted with a high-k dielectric in Figure AD, correct?
A That's correct.
Q And Figure AD configuration has

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a tunneling length of L4, correct?

A Yes, that's correct.

Q And L4 is larger than L3, correct?

A Yes, that's correct.

Q You can set aside Chen for now.

Now let's go back to your declaration.

A All right.

Q Paragraph 42.

Now, paragraph 42 starts with: "The elements missing from Kim's Figures 4A through 14B embodiment that are disclosed only in Figures 17A through 22B."

Correct?

A You're asking me if these figures are accurate?

Q No. So let me rephrase my question.

In paragraph 42, you start out by identifying elements in the Figure 17A through 22B embodiment that are missing from the Figure 4A through 14B embodiment, correct?

A Yes.

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Q And you identify an etch-stop layer and a barrier layer, correct?
A Those are two examples, yes.
Q Are there additional missing elements that you have not identified here?
A I would have to study it. But as it is written currently, it is "such as," which means that there could be others. I don't recall off the top of my head if there are.
Q (Inaudible) -- for the missing elements that you consider to be relevant to your consideration in forming your opinion?
A I'd just say that at the moment these are the two that are present.
Q Now, this paragraph 42, in the middle of the paragraph is a sentence that begins with: "Attempting such a combination."
Do you see that?
A Yes, I do.
Q What combination were you referring to there?
A I'm sorry, I can't remember at

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the moment. I apologize, but it's going to take a while to think about it.

So this is Kim, in the knowledge of a POSITA, and particularly referring to etch-stops -- the paragraph again is? Could you tell me the paragraph again in the declaration?

Q 42.

A 42. Thank you very much.

Well, what I remember about this, sitting here, is that Kim -- yeah, so Kim, although he did mention an etch-stop, most of Kim was about the CMB planarization. And I recall that there was an attempt to map the planarization process onto the etch-stop layers and to substitute one for the other.

Q So earlier you testified that you agree Kim discloses an etch-stop layer over the 3D memory staircase structure.

Do you remember that?

A As I said, he had four potential etch-stop layers.

Q And Kim's etch-stop layer functions as an etch-stop during the

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etching of the contact holes, correct?

A I can't argue one way or the other. I don't know whether it was an effective etch-stop or not.

Let's see...

All right. So I think this was discussed in 58. "A POSITA would not have understood Kim as disclosing the etch selectivity between the interlayer dielectric 130 and the etch-stop layer 125 for planarization discloses a process for forming contact holes where the etch-stop layer is exposed, but not penetrated through."

A POSITA would not have understood Kim's planarization process to be used for forming contact holes.

Kim's planarization process discussed using chemical mechanical polishing to create a flat surface, not contact holes.

I believe this is related to what we were just discussing.

Q Okay. Let's look at Kim's Figure 22A, Exhibit 1005.

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A All right.

Q Actually, let's start from Figure 19A, PDF page 33.

A All right.

Q There you see the etch-stop layer 105A and 105B covering the entire staircase including the top surface of the staircase, correct?

A You mean 125A and 125B?

Q Correct.

A Yes.

Q And then the CMP planarization process you are referring to can be seen in Figure 20A where now the top surface is planar after the CMP process and with it the top surface layer of the etch-stop 125A and 125B is removed, correct?

A Yes, looks like it's 126 in this figure, but yes.

Q Right. Thank you for that clarification.

We discussed earlier that Kim changes the numbering from 125 to 126 to reflect this removal of the very top surface of the layer 125.

Do you agree?

A Yes.

Q Okay. So then this -- what's left of layer 126A and 126B covers the entire staircase except the top surface where what used to be present in 125A and B has been removed. Correct?

A Yes.

Q Now, what function does this remaining portion that's represented by 126A and 126B perform?

A 126A --

MR. DUNTEMAN: Objection.

Vague.

A From the figure you were showing me, 28, I would expect 126A to be a buffer layer, possibly silicon dioxide, and 126B to be an etch-stop layer.

Q An etch-stop layer that works as an etch-stop during the etching of the upper insulating layer 134, correct?

A Presumably, yes. But don't know if it functions or not.

Q Well, if you look through -- all the way -- let's see, we were on Figure

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20A. If you look through Figures 20A, 21A, 22B -- 22A, excuse me, the upper insulating layer is etched to form contact holes to the gate conductor, correct?

A Correct.

Q And so the etch-stop layer 126B will serve as an etch-stop during the etching of those contact holes, correct?

A That's what its function should be, yes.

Q Let's turn back to your declaration.

A All right.

Q Let's go to paragraph 44, and this is on page 29 or 32 of the PDF.

A All right. What would you like to discuss?

Q In the middle paragraph -- I was trying to find it.

In the middle of the paragraph, probably the easiest way to find it is the line after "my 40 years of experience."

A Okay.

Q So in that line, in the next line it says: "Minor alterations in one

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process step usually changes the outcome of other process steps."

Did I read that correctly?

A Yes, you did.

Q And then you refer to the reversal of the gate stack as one such minor alteration. So that would be costly in money and time, correct?

A I don't think I refer to it as a minor alteration. But yes, reversal on each stack would likely cause problems, would very likely cause problems.

Q Okay. But is it fair to say that the reversal of the gate stack suggested by Dr. Banerjee would change the outcome of other process steps?

A Almost certainly.

Q Now, let's turn back to the Chen reference, Figures 11A and 11B on page 12 of the PDF.

A Yes.

Q You agree that the Figure 11A shows a gate-stack-on-the-bottom configuration and 11B shows a gate-stack-on-top configuration, right?

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A Yes.

Q Would going from Figure 11A to Figure 11B as shown here in Chen change the outcome of other process steps, too?

A Yes.

Q Let's turn back to your declaration, paragraph 45.

Here you discuss the -- Dr. Banerjee's modified figures of the gate-stack-on-top configuration having some steps with two gate conductive layers, correct?

A Yes.

Q And then you show the example in a large figure on page 32 at the end of paragraph 45, right?

A Yes.

Q And you understand that what Dr. Banerjee proposed as swapping -- describing that.

And you understand that what Dr. Banerjee proposed as in place of where Kim shows a dielectric layer, Dr. Banerjee shows a gate stack and vice versa, correct?

A Yeah. Okay, let's say that

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that's the case. But clearly this is not that. We didn't have two gates overlapping -- aligned with each other prior to trying to do this transformation.

So you're asking me do I know what he was trying to do. It doesn't look like -- it doesn't look like he's doing what he thought he said he was doing.

Q Well, I was -- I didn't ask for that, but that's fine.

I was hoping to get to, do you agree that this -- these gate layers shown in the modified figures, the modified gate-stack-on-top figures correspond to what -- correspond to dielectric layers in Kim's original figures?

A We're talking about layers 126A and 126B?

Q No. We're talking about, for example, layers 161, 162 and so forth, the gate stack layers.

A Okay. So the question is, in the attempt to switch 162, 163, 164 with 112, 113, 114, is that what you're asking?

Q So let me rephrase my question.

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Do you agree that what is shown in the modified figures, the locations of gate stack 161 through 166 correspond to the locations of the dielectric layers 111 through 116 in the unmodified figures?

A Yes, that's my understanding.

Q Now, if all of the dielectric layers, for example 116 through -- 111 through 116 have the same thickness in Kim, then there wouldn't be this issue of a gate stack having two layers as you show here on page 32, correct?

A You're asking me to define why this figure came out to be the way that it is. I don't know why it wound up this way, but that's what we get.

Q Okay. Let's go to Kim. Let's look at Figure 12B, page 21 of the PDF.

A I'm on 12B.

Q Here it shows dielectric layers 111 through -- just keeping with our previous discussion -- 116.

Do you agree?

A Yes.

Q And you see that layers 112 and

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116 are thicker than other dielectric layers, right?

A Yes.

Q Do you know if Kim requires some dielectric layers to be thicker than others?

A I do not know.

Q But here you agree that Figure 12B shows some dielectric layers to be thicker than others, right?

A Yes, I do.

Q Now let's go back to your declaration, paragraph 46.

I'm going to start reading from the very bottom, very end of page 32 where you said: "To accommodate the shortening of the contact plugs, it would require alteration of the etch steps and processes used to etch the openings for the word-line contacts."

Did I read that correctly?

A Yes.

Q What etch steps were you referring to?

A This is the etch down to the

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contacts for the gate contact. The distances are going to be different and may very well require changes in the etch process.

Q And can you give me some examples of changes in the etch process?

A It is, again, going back to what we discussed earlier today. The etch process is extremely complex. It is not given to us, so I don't know what the chemistry is, what the power is.

But I know that if you are moving the positions out of the context that you are trying to etch, it is not unusual. You have to tune the etch process to get results that are effective.

Q So you were referring to our earlier discussion about, for example, chamber pressure?

A Yes.

Q Temperature, et cetera, that a POSITA would go to Lam Research or Applied Materials to get the recipes for, correct?

A Yes. The way that it works is that the companies provide a recipe as a

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starting point. Principally, it will do a decent job, but usually it's tweaked by the local POSITA and engineer.

And so I'm not saying that they would have to go back to Applied Materials and get new recipes, but it's very likely that they'll have to tune the recipe because of a change in the position of the contacts.

Q But these are recipes for parameters that none of the patents, including the '276, discloses, correct?

A That's correct.

MR. HSU: Okay. We are at just past the one-hour mark. So I think this will be a good time for a break.

MR. DUNTEMAN: Sounds good.

(Recess taken 2:12 p.m.)

(Resumed 2:24 p.m.)

BY MR. HSU:

Q All right. Let's look at paragraph --

A Before we continue, could I make a correction? I realized something I said was not correct and I'd like to straighten

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it out.

MR. DUNTEMAN: Go ahead, Dr. Campbell.

THE WITNESS: Very good.

A So we were discussing the etch-stop layers and buffer layers on Kim and particularly what the issues were with that. And I thought it was because they weren't there. And, indeed, it was demonstrated to me that the etch-stop layer and buffer layer were there.

The problem is not that they are there, but just covering paragraph 56 and 57 of the declaration, Dr. Banerjee cites paragraph 173 of Kim, but that paragraph does not mention two steps with permission of contact holes. And this is obviously very important.

But rather, it just discloses forming contact holes, not stopping on the etch-stop, but just going straight through down to the gate layer.

As a result of this information, the holes penetrate rather than merely expose the etch-stop layer, and so the

word-line contact plugs can be connected to the gate electrodes which expose the etch-stop layer.

Dr. Banerjee assumes -- asserts that the POSITA would have recognized the need for an extra step in the contact hole and that the etch-stop layer "may be formed of a material having an etch selectivity with respect to the interlayer dielectric."

But I have to disagree. A POSITA would have understood this passage from Kim explicitly discloses when a two-step etching process is intended, specifically etch activity, and the passage relates to the two-step planarization in the cell area region, not formation of contact holes.

This was why I brought up the planarization part of the process. But it was not because the etch-stop layer was there. It was not there. Rather, it was the hole going through the etch-stop layer, the buffer, down to the gate that caused the issue.

So my apologies for getting that

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confused.

Q Okay. I think you read from paragraph 56 and 57 of your declaration, but you cover basically two separate issues. So let's break it down one at a time.

A Very well.

Q First is that you -- in your opinion, a POSITA looking at Kim would not have understood that the etch would stop at the etch-stop layer 126B because -- because Kim's figures do not show such a phase in the etch process, is that correct?

A Well, the figure shown in that and the lack of text describing the second etch process is the reason that we think that a POSITA would be misled.

Q What do you mean by that answer, "the lack of text describing the second etch process is the reason why we think a POSITA would be misled"?

A Kim does not explicitly say that when asked to etch down to the etch-stop layer and then have a second etch process that will etch down to the gate electrode,

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it shows a diagram only of it going all the way down to the gate, and it doesn't say etch down to an etch-stop and then change chemistry and etch down to the gate.

So one would assume then you just go straight down to the gate.

Q And your opinion is based on Kim's disclosure as illustrated in Figures 21A and 22A, correct?

A The Figures 21A and 22A provide a visual demonstration of what I think is incorrect, and the lack of text in Kim calling for the second etch process reinforces that problem.

Q So in your opinion, Kim's process of etching through the upper insulating layer would blow right through the etch-stop layer 126B and other intermedial layers below and go right to the gate conductor.

Did I understand that correctly?

A Yes.

Q So your testimony is that what Kim calls a step-wise etch-stop pattern 126 doesn't function as etch-stop, correct?

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A It's not a perfect etch-stop, no.
Q But there isn't ever a perfect etch-stop, is there?
A No, there isn't. Silicon nitride is not a particular great one.
Q There isn't a perfect etch-stop in Kim, correct?
A There isn't a perfect etch-stop in anyone.
Q Okay. And the second part of your quotation from paragraphs 56 and 57 has to do with planarization.
Actually, before we go there, would you agree that a POSITA does not have to deposit an etch-stop layer uniformly across the entire staircase?
And by uniformly, I mean a single layer all the way through or two layers all the way through, et cetera.
A Are you asking can we have different thicknesses at different steps?
Q Or can we have, for example, one etch-stop layer over certain steps of the staircase, but two layers over only certain

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steps of the staircase?

A As with most processes, anything is possible. But it requires additional masking and overlay. So it would not be desirable, but it could be done.

Q And is it your testimony that Kim's step-wise etch-stop pattern 126 is essentially useless as an etch-stop for the formation of contact holes?

A No, I would not say it's useless.

Q So the step-wise etch-stop pattern 126 of Kim performs an etch-stop function during the etching of the contact holes, correct?

A It will slow the etching process prior to getting to the gate. Really all one needs is an etch process that is highly selective to the gate material.

Q And which etch process were you referring to there? What specifically is being etched?

MR. DUNTEMAN: Objection. Form.

A What you previously called the upper insulator, I believe.

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Q So I think I'm not sure the parts of your answer would -- strike that.

I'm trying to reconcile the two parts of your answer.

You testified that the etch-stop layer of Kim will slow down the etch process of the upper insulating layer during the etching of the contact hole, correct?

MR. DUNTEMAN: Objection. Mischaracterizes testimony.

A Would you repeat it, please?

Q Sure.

You testified that the etch-stop layer of Kim will slow down the etching process through the upper insulating layer during the etching of the contact holes, correct?

A Yes, that's correct.

Q So the etch-stop layer of Kim functions as an etch-stop, correct?

MR. DUNTEMAN: Objection. Form.

A As we have discussed earlier today, when etch-stop is in contact with two materials and has a lower etch rate,

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the answer is yes. It is still an etch-stop.

Q In other words, it will have some effect of slowing down the etching of the contact holes such that the etching or the etch would not blow right through it, correct?

MR. DUNTEMAN: Objection. Form.

A Yes, it will slow down the etch.

Q And that's the etch-stop function that it serves, correct?

A Yes.

Q Now let's turn to paragraph 46 of your declaration.

Here I would just like a clarification.

Starting from the fourth line on page 33, starting -- the sentence starting with "the switching may also."

Do you see that?

A Yes.

Q Okay. And then in the middle of that sentence, you refer to the insulating layer above the sacrificial layers.

Which is the insulating layer

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above that you're referring to there?

A Okay. So we're talking about the insulating layers above the sacrificial layers, which I would take to mean the insulating layer that is on top of what we have been calling the upper insulating layer.

So if we look at the figure on 33, what we've been calling the upper insulating layer in left, in the original is in blue, and the layer above that is the layer that is being described.

Q Okay. So that insulating layer above the sacrificial layer refers to what we have been calling the upper insulating layer, or more specifically as to Kim, Kim calls it the interlayer insulating pattern 134, is that correct?

A Yes, I believe that's the correct one.

Q Okay. Then can you explain this sentence, the same sentence in paragraph 46: "The switching may also change the etch selectivity between the" -- now we clarify -- "the upper insulating layer and

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the sacrificial layers themselves."

Why does that matter?

MR. DUNTEMAN: Objection. Compound.

A So the upper insulating layer, as we're describing it, has to be planarized with the CMP process. The change may alter that process.

I'll leave it at that.

Q So let me make sure I understand.

You're saying the change to the order of the alternating layers in the staircase may alter the CMP process, is that correct?

MR. DUNTEMAN: Objection. Asked and answered.

A I'm sorry, I can't give you a good answer. I don't recall this exact paragraph, so I'm unable to reconstruct it.

Q Okay. Setting that paragraph aside, let's go back to Kim, Figure 19A, page 33 of the PDF.

A Page 33?

Q Yeah, Figure 19A.

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A All right.
Q You see here, this is before the top surface of the staircase is planarized, correct?
A Yes, that's correct.
Q And then in Figure 20A, we see a planarized surface, top surface, correct?
A That's right.
Q And that planarization is performed using CMP, correct?
A Yes, that's correct.
Q So CMP is applied to the surface as it exists in Figure 19A and eventually after the CMP process is done we end up with the top surface of Figure 20A, correct?
A Yes.
Q Now, the alternating layers in the staircase do not appear on the top surface of the staircase, correct?
A Say that again?
Q The alternating sacrificial and dielectric layers of the staircase do not appear on the top surface of the staircase as CMP is applied as shown in Figure 19A,

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correct?

A Yes, that's correct.

Q And CMP has no impact on materials underneath the top surface, is that correct?

A CMP affects a relatively thin layer. So I will say yes, it's close enough to nothing.

Q Let's go to Chen again. That is Exhibit 1008, Figures 7A and 7B, page 7 of the PDF.

A All right.

Q We discussed earlier that 7A is a gate stack-on-bottom configuration and 7B is a gate-stack-on-top configuration.

Do you recall that?

A Yes.

Q Would you agree that implementing the Figure 7A configuration involves a tremendous amount of work?

A Yes.

Q And going from the Figure 7A embodiment to Figure 7B embodiment is not as intensive in terms of the amount of work, correct?

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MR. DUNTEMAN: Objection.
Vague.
A There is not as much work as starting ab initio. Are you saying if you've done 7A first, 7B would not be as hard as 7A?
Q Is that fair?
A Yes, that would be fair.
Q And that tremendous amount of work that we referenced involves, for example, optimizing the etch process, right?
A Yes, one of the things, yes.
Q And that involves the parameters that we discussed earlier, for example, plasma power, bias voltage, chamber pressure, et cetera, right?
A Those are the things that are included, yes. That's just the etch processes. There are lots of processes that are going on, but yes, that's one.
Q And are these parameters interrelated?
A Absolutely.
Q And so adjusting one parameter

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may require adjusting other parameters?

A Usually it does, yes.

Q So in order to make that implementation -- make an implementation such as shown here in Chen's Figure 7A or 7B, a POSITA would have to eventually know all of the parameter, right, because they are interrelated?

A Yes.

Q And it wouldn't be useful to know just one parameter without knowing others, is that correct?

MR. DUNTEMAN: Objection.

Vague.

A Yes, that's correct.

Q But these are parameters that you testified earlier that none of the patents at issue here including the '276 itself disclose --

MR. DUNTEMAN: Objection.

BY MR. HSU:

Q -- in the specification, correct?

MR. DUNTEMAN: Objection.

Vague.

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A Yes. I said that none of the patents involved in this have detailed recipes for their etch processes.

Q And was CMP similar in that regard, namely, that CMP also involves a lot of interrelated parameters?

MR. DUNTEMAN: Objection. Vague.

A The answer to that is a qualified yes, CMP does have multiple parameters that one has to optimize, but it is much less complicated than high aspect ratio etching.

Q As of the date of the patent, was CMP widely used in the industry?

A CMP was widely used in the industry by the time period the patent was -- whatever the word is -- was -- I'm sorry.

Q Effective, the date of the patent?

A Thank you very much.

Q Okay. And was contact hole etching also widely practiced in the semiconductor industry by the priority date

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of the patent?

MR. DUNTEMAN: Objection.

Vague.

A Are we talking about the contact holes to the gate?

Q Yes.

A Or just the contact holes in general?

Q Contact hole to the gates.

A Contact hole to the gate...

Let's say it was pushing the envelope of what was common in the semiconductor industry and it was a -- and has been -- a limitation to how high the stack could be in the 3D.

Q So, for example, the contact hole etching in the Chen reference was pushing the envelope of what was common in the semiconductor industry, is that fair?

MR. DUNTEMAN: Objection.

Vague.

A So it is somewhat difficult to answer that question because Chen doesn't say what the size of the contacts are, exactly how many layers there are in the

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stack. So I can't say that definitely it's pushing the art toward -- well, it's not given, the information is not given.

Q Would you agree that this pushing of the envelope to a large extent depends on what can be provided by the equipment manufacturers, we mentioned Lam Research and Applied Materials, for example?

MR. DUNTEMAN: Objection. Form.

A So say that again?

Q Let me withdraw that question. I'll ask a different one.

Can you explain what you meant by pushing the envelope of what was common in the semiconductor industry?

A Yes. If we step away from 3D and look at those 2D structures, whether they're NAND memory devices or they're logical circuits, the standard parameters -- the standard geometry, sorry, let's say in the early teens when 3D was first starting out, feature sizes were 20 nanometers, let's say -- well, 22 nanometers was the node, so we'll call it

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22 -- and the depth that you would go through half a micron. So we're talking about something that's much shallower than the stack that's used in the 3D.

And the very early days in the 3D, the stacks were not as high as they are now because the etching process has improved.

Q And by the early day of in the 3D, you're referring to the early 2010s, is that fair?

A 2013 is often cited as when it first came out.

Q And do you agree that by 2018, the deposition process for laying down a 48-layer alternating stack was mature?

MR. DUNTEMAN: Objection.

Vague.

A It was common by that time, yes. I mean the leading companies were capable of doing that.

Q And do you agree that by 2018, the general fab techniques for 3D NAND were known?

MR. DUNTEMAN: Objection.

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Vague.

A I will have to agree with my lawyer here. The process technology continues to improve. To suggest that it's stagnant at some point is not the case.

Q I didn't suggest that it was stagnant at some point. So let me maybe try to just repeat the question.

Do you agree -- and with the understanding that I don't mean to suggest it was stagnant -- do you agree that by 2018, the general fab techniques for 3D NAND were known?

MR. DUNTEMAN: Same objection.

A Again, I can't answer that because the new material and new processes are continually coming into use.

The materials that we use for etch-stop, materials held, materials that we used for the gate, it used to be poly and now it's tungsten.

Are you saying that there's no radical difference, it's just a constant improvement? I haven't seen a radical difference. I've seen constant

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improvement, but it is constantly changing.

Q But the change in material that you discuss for the gate, for example from poly to tungsten, that occurred years before 2018, correct?

A Yes, absolutely.

Q Roughly, what year did that occur?

A That was quite early. Certainly before 2017. I don't know, '15, '16. I wasn't really involved in it that early.

Q All right. I'm going to drop in one other reference. Exhibit 1007, the Han reference.

A Sorry, this is Han?

Q Correct.

A All right.

Q All right. Let's turn to paragraph 156 of Han.

A All right. I'm at paragraph 156.

Q This paragraph 156 starts out with "at least one patterning process may be performed on the upper filling insulation layer 200."

Correct?

A Yes.

Q What does that patterning process refer to?

A So when they're talking about lower contact holes and upper contact holes, that refers to what we discussed earlier today of grouping the contacts into etching in the upper contacts and the lower contacts.

Q So each -- when it says at least one patterning process, it implies a potential of using multiple patterning processes, correct?

A Correct.

Q And that's multiple processing -- strike that -- multiple patterning processes to etch the contact holes in multiple groups, correct?

A That's my understanding of it, yes.

Q And each patterning process would involve its own mask, correct?

A Yes.

Q Now, going back to our earlier

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discussion about what was going on in the 2018 timeframe, do you agree that by that time, 2018, 32, 48 and 64-layer 3D NAND layer devices used conventional tools for the high aspect ratio channel hole, contact holes that we've been discussing?

MR. DUNTEMAN: Objection. Vague and compound.

A Can you explain what you mean by conventional etching as opposed to whatever?

Q I'm using conventional etching tools to refer to whatever a POSITA would have understood to be conventional at that point.

MR. DUNTEMAN: Same objection.

A Again, that isn't very helpful.

So again, if we're talking about the 2017-2018 time period, you're looking at about a 5-micron thick stack and the aspect ratio will be higher than what would be used in conventional CMOS, for example.

It could be that someone was able to make that work, but I -- I don't know that it was possible.

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Certainly with the stacks in these days, the technologies used for CMOS for etching are not acceptable.

So what I'm saying is, I'm not sure. I probably -- people were trying to make the existing hardware work because I don't know that the companies that are making this equipment had a large enough user base to invest the money to create such a machine and to develop the technology, the recipes. So you're kind of on the cusp at 2017.

Q Two layers of the same material have the same etch properties, right?

A Two etch materials have the same properties?

Q Let me reask that.

Two layers made from the same material have the same etch properties, correct?

A To say that it's the same material is not sufficient. Does it have the same structure, the same grain size, same dopants -- are you saying in all aspects the two layers are identical?

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Q Right, that's -- keep all else constant, just considering the material, then two layers made from the same material would have the same etch properties, correct?

A Generally speaking, the answer would be right, if the top one is exposed to air and there's some oxidation, there could be a slight difference. But that's -- assuming that there's no air or it's not -- the material doesn't oxidize, then the answer would be yes.

Q Right.

If the material oxidized, it's no longer the same material, right?

A Yeah.

Q And now is the --

(Simultaneous crosstalk.)

A Maybe you put it in there when it was the same material, but it oxidized in the etch chamber. It's not uncommon.

Q Is the converse also true, specifically two layers made from different materials generally have different etch properties?

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A Generally, yeah.
Q Now let's turn back to Chen, Exhibit 1008, and paragraph 41 of Chen.
A One second. Okay, paragraph?
Q 41.
A 41, thank you. Go ahead.
Q Now, Chen discloses six different materials or combinations thereof for the second stop layer, correct?
A Yes.
Q Does Chen restrict the second stop layer to a subset of these six different materials?
A It would appear that there are a few of the materials for the first stop layer are not acceptable for the second stop layer.
Q Can you explain why it would not be acceptable?
A Oh, perhaps I read this wrong. Let me look at this one more time.
All right. So it looks like there are a few materials that are acceptable for the first stop layer, but not for the second stop layer.

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Q Can you explain what is not acceptable for the second stop layer?

A Well, it doesn't allow silicon oxide. It does allow silicon nitride, which does not appear. I guess the difference is just the silicon nitride or the silicon oxide.

Q So let me clarify my question.

We talked about earlier that Chen discloses six different materials for the second stop layer or combinations thereof, correct?

A Yes.

Q Does Chen further restrict the second stop layer to a subset of the six materials or combination thereof?

A There are five for the second stop layer and there are five for the first stop layer. Again, the first stop layer has silicon oxide and the second stop layer has silicon nitride.

Q I stand corrected. Chen discloses five different materials or combinations thereof for the second stop layer.

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A Yes.

Q Does Chen further restrict the second stop layer to a subset of these five different materials or combinations thereof other than the fact that the second and the first ought to be different?

A Are you asking something for beyond the silicon oxide and the silicon nitride?

Q Let me try to be clear. Paragraph 41 of Chen says: "A material of the second stop layer 220 may include silicon nitride, aluminum oxide, magnesium oxide, silicon zirconium oxide, silicon hafnium oxide, or combinations thereof."

Correct?

A Yes.

Q And then it further says: "The first stop layer is different from the second stop layer."

Correct?

A Yes.

Q And that last sentence that the two layers be different, is that because -- is that for the first layer to serve as an

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etch-stop during the etching of the second stop layer 220 so that there can be etch selectivity?

MR. DUNTEMAN: Objection. Calls for speculation.

A I have to agree with my counsel, I would only be speculating on why they are choosing this.

It could be that they want to have different etch rates for the different layers. But again, it's just speculation. I have no definitive data that I can call upon.

MR. HSU: So let me pause for a second. I understand we are up at the one-hour mark.

I am also done. So if you bear me with just a couple of more minutes and then we can take a break, I'll take a quick look through. I'm pretty sure I'm done. Is that okay?

THE WITNESS: It's okay with me.

MR. DUNTEMAN: I'm okay with that if Dr. Campbell is.

MR. HSU: Okay.

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MR. DUNTEMAN: I'm sorry, to be clear, Johannes, you were just saying a couple of minutes, right? It looks --

MR. HSU: Yeah. Yeah.

MR. DUNTEMAN: Yeah, yeah, okay.

BY MR. HSU:

Q So can you think of other reasons why Chen would specify that the two stop layers have different materials?

A I don't have any guesses that I feel certainly strongly about.

Q So etch was one that you --

A Yes.

Q -- thought of.

(Simultaneous crosstalk.)

Q But you can't think of others sitting here, correct?

A None that I feel are likely enough to offer.

Q Okay. So going back to my previous question, which perhaps because the lack of clarity on my part I don't think I've gotten an answer for, Chen specifies five different materials or

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combinations thereof for the second stop layer, correct?

A Yes.

Q But does Chen further restrict the material for the second stop layer to a subset of these five or combinations thereof?

A Well, they do specify that the second layer can't be the same as the first layer.

Q Right, and -- right.

And other than that restriction, there is not a further reducing to a subset of the five or combinations thereof, correct?

A Correct.

MR. HSU: All right. That was my few minutes. So thank you for bearing with me.

Off the record.

(Recess taken 3:29 p.m.)

(Resumed 3:39 p.m.)

MR. HSU: Dr. Campbell, welcome back. I have no further questions on cross.

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MR. DUNTEMAN: Okay. Let's take another break then, if that's all right, and go off the record.

(Recess taken 3:39 p.m.)

(Resumed 4:09 p.m.)

EXAMINATION BY

MR. DUNTEMAN:

Q Dr. Campbell, do you recall counsel asking you about paragraph 46 of your declaration and the switching that Dr. Banerjee did in Figure 22A of Kim?

A Yes.

Q Okay. I want to refer you to Exhibit 1005 of Kim, Figure 22A, in particular.

A I need to pull up Kim?

Q Yeah, Exhibit 1005, please.

A Okay. One second.

Okay. Which figure are you?

Q 22A.

A 22A, okay.

Q In 22A, what is labeled as 111, 112 and 113?

A 111, 112 and 113 are the clear areas and those would apparently be the

dielectric layer.

Q And what function does the dielectric layer perform in this?

A The electrical isolation between gate stacks.

Q Can we go to paragraph 186 of Kim now?

A All right.

Q What does Kim refer to the layer 111 as?

A So I'll just read the relevant sentence. "For instance, the etch-stop layer 125 may be formed of a material having an etch selectivity with respect to the sacrificial layers SC1 to SC8 and the insulating layers 111 to 118 of the stack structure ST. In some embodiments, the etch-stop layer 125 may include at least one of silicon carbide, silicon nitride, silicon oxynitride and/or silicon carbide."

Q Okay. So do you have your declaration in front of you, too?

A I do.

Q Can you go to paragraph -- sorry, not 146 -- 46, please.

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A Paragraph 46. Oh, sorry, everyone.
Q This is Exhibit 2019, to be clear.
A All right. Paragraph 46?
Q Yes.
A "Second, Dr. Banerjee's modified Figure 22A not only swaps the layer, but shortens the contact plugs to terminate within the gate electrode layers, as shown below. This is no trivial change to Kim's processes and devices. To accommodate the shortening of the contact plugs, it would require alteration of the etch steps and processes used to etch the openings for the word-line contacts.

As I discuss below, these etch processes are very complex and are sensitive to even small adjustments. The switching may also change the selectivity between the insulating layer and the sacrificial layers SC1 to 8 and sacrificial layers themselves such that the first stop layer 126A or the second stop layer 126B is not needed, just like in the alternate

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Figures 4 to 15D embodiment.

A POSITA would not use the stop pattern 126 if its function is not needed because a POSITA would not want to add the time or material to include a non-functional component."

MR. HSU: Objection. There was no question pending and Dr. Campbell didn't need to read the entire paragraph 46.

BY MR. DUNTEMAN:

Q Focusing on --

MR. HSU: Move to strike.

BY MR. DUNTEMAN:

Q Focusing on the sentence on page 33 in paragraph 46 that starts "the switching may also change the selectivity" that you just read -- do you see that?

A Yes, I do.

Q Okay. Looking below that, the original and manipulated figures you have in your declaration, what is switched there?

A Well, what is switched is the position of the gates relative to the

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insulating layers, gate on bottom or gate on top.

Q And that's insulating layer for example 111 that we just discussed in Figure 22A?

A That's correct.

Q Are you referring to those insulating layers in that sentence starting the switching may also change the selectivity that we just discussed?

A Yes.

Q Why would switching that change the etch selectivity from the original to the manipulated?

A Why would it change the etch selectivity?

Q Yeah, between the insulating layer above the sacrificial layers and the sacrificial layers themselves?

A In the manipulated one, the electrode comes down -- the tungsten comes down to the gate directly aside from the etch-stop layers, whereas in the original the gate contact comes through a layer in addition to the etch-stop layers. It comes

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down through the insulating layer and the high-k -- and the high-k apparently.

Q So the additional layer you're referring to is the insulating layer?

A Yes.

MR. DUNTEMAN: No further questions.

EXAMINATION (CONTINUED)

BY MR. HSU:

Q Dr. Campbell, quickly.

Counsel asked you about paragraph 46 and in particular the sentence referring to the insulating layer above the sacrificial layers, correct?

A Yes.

Q And in your answer to counsel, you refer to these -- you're saying these insulating areas in that sentence refers to, for example, layers 111 through 116 of the alternating layers, correct?

A Yes.

Q Do you recall earlier you testified that that very same term you testified to referred to the upper insulating layer 134?

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A Yes. So in looking at the structure again, looking at the figure, the primary problem is not going to be the 134, but rather the distance that you have to make the contacts.

MR. HSU: No further questions.

THE WITNESS: Are we done?

MR. DUNTEMAN: One moment, please. Just let me look at this.

(Pause)

EXAMINATION (CONTINUED)

BY MR. DUNTEMAN:

Q Just one final question, Dr. Campbell.

Counsel just pointed out that you had referred to the upper insulating layer 134 in your prior discussion when discussing the insulating layer that you refer to in 46.

Were you confused or why did you -- strike that.

Why did --

MR. DUNTEMAN: Never mind. I withdraw the question. I'm done.

THE WITNESS: Okay.

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THE COURT REPORTER: Just a quick question. Does Latham need a copy of the rough draft?

MR. DUNTEMAN: That would be great.

THE COURT REPORTER: Okay. Thank you, all. Have a great weekend.

(Time noted 5:22 p.m.)

* * *

_____

STEPHEN CAMPBELL

Subscribed and sworn to
before me this day
of , 20__

_____

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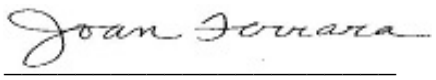
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I, JOAN FERRARA, do hereby certify:

That said deposition was taken at the time and place herein named; and that the transcript is a true record of the testimony as reported by me, a disinterested person, and was thereafter transcribed.

I further certify that I am not interested in the outcome of the said action, nor connected with, nor related to any of the parties in said action, nor to their respective counsel.

IN WITNESS WHEREOF, I have hereunto set my hand this 16th day of January, 2026.



JOAN FERRARA, RMR, CFRR

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I declare under penalty of perjury that I have read the entire transcript of my deposition taken in the captioned matter or the same has been read to me, and the same is true and accurate, save and except for changes and/or corrections, if any, as indicated by me on the DEPOSITION ERRATA SHEET hereof, with the understanding that I offer these changes as if still under oath.

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