UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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MICRON TECHNOLOGY, INC.,
Petitioner,

vs.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

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Case No. IPR2025-00117
U.S. Patent No. 10,672,711

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REMOTE DEPOSITION OF STEPHEN CAMPBELL

Friday, November 7, 2025

8:59 a.m. (CST)

Reported by:

Jaclyn Urzia, RPR, CRR

Job No. 2025-1002161



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IPR2025-00228

November 7, 2025

8:59 a.m. (CST)

Deposition of STEPHEN CAMPBELL, held remotely via Zoom, before Jaclyn Urzia, a Registered Professional Reporter, Certified Stenographic Realtime Reporter and Notary Public.

1 REMOTE APPEARANCES:
2
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8
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14 BY: BEN SMITH, ESQ.
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1 STEPHEN CAMPBELL,
2 called as a witness, having been
3 duly sworn by a Notary Public, was
4 examined and testified as follows:
5 EXAMINATION BY
6 MR. HSU:
7 Q Good morning, Dr. Campbell.
8 A Good morning.
9 Q My name is Johannes Hsu. I
10 represent Micron in this IPR proceeding.
11 Just to sync up, this is the
12 proceeding IPR -- hang on a second --
13 2025-00117 for U.S. Patent 10,672,711.
14 Does that match your
15 expectation?
16 A Yes.
17 Q And if I refer to that patent by
18 the "'711 Patent," you'll understand what
19 I'm referring to?
20 A Yes.
21 Q Great.
22 So thank you for your time
23 today.
24 Actually, if you don't mind,
25 state your name and spell it for the

1 record, please.
2 A My name is Stephen,
3 S-T-E-P-H-E-N, Alan, A-L-A-N, Campbell,
4 C-A-M-P-B-E-L-L.
5 Q Now, you have been deposed
6 before, right?
7 A Yes.
8 Q Roughly how many times?
9 A I believe three.
10 Q Three times.
11 Were they all in connection with
12 an inter partes review proceeding?
13 A No, I don't think they were. I
14 think they were -- not the IPR, it was
15 court.
16 Q So you've been deposed before,
17 so you are probably familiar with what's to
18 come, but just to get us on the same page,
19 let me say a few things just to kind of
20 settle the expectation.
21 So I'm going to give you
22 questions, and you'll give me answers.
23 Okay?
24 And if you don't understand --
25 if anything I say is confusing or you don't

1 understand, please go ahead and ask for
2 clarification.
3 And if you don't, is it fair
4 that we will assume that you understood --
5 you understand my question?
6 A Yes.
7 Q Okay. And, obviously, we -- or
8 for the court reporter and for the
9 transcript, your answer will be verbal and
10 not, you know, nodding your head or shaking
11 your head or something like that, right?
12 A Yes.
13 Q Okay. And I'll do my best not
14 to talk over you and, hopefully, that will
15 work out, and appreciate you doing
16 likewise.
17 Now, from time to time, you may
18 hear your attorney raising an objection.
19 Do you understand that unless
20 your attorney instructs you not to answer,
21 you are to answer the question in spite of
22 objections?
23 A Yes.
24 Q And then roughly, we'll plan on
25 taking a break every hour or so. And if I

1 happen to really get into the deposition
2 and allow time to escape my mind, please
3 remind me when you need a break.
4 Is that all right?
5 A I will do that, yes.
6 Q The only thing is that when
7 there's a question pending, we ask that you
8 answer the question first before we go on a
9 break.
10 A Yes, I understand.
11 Q Is there any reason why you are
12 not able to competently answer questions
13 today, such as any medical conditions or
14 anything of the sort?
15 A No.
16 Q Any other reason why you cannot
17 give complete and accurate testimony today?
18 A No.
19 Q Okay. And just a few other
20 questions since we're on a Zoom call.
21 Now, do you have any papers in
22 front of you?
23 A Yes.
24 Q And what kind of paper are
25 those?

A A clean copy of the '711 Patent, and on my right side -- I apologize for this. My mouse pad stopped working last night, and Amazon couldn't get it here this morning. I have two clean sheets of paper that seem --

(Reporter seeks clarification.)

I have two clean sheets of paper, which seems to work just fine, with no markings on them.

Q And it looks like you are in your home today, correct?

A Yes, my home office.

Q Your home office.

Is there anyone else in the home office with you today?

A No.

Q So let me make sure I understood you correctly.

You said that you have a clean copy of the '711 Patent and then you have those two sheets of clean paper that you showed me but nothing else.

Did I understand that correctly?

A Yes, that's correct.



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1 Q Okay.
2 All right. So that means we
3 will have to make sure that the exhibits,
4 to the extent we use them, will get to you.
5 Oh, so, obviously, you're
6 sitting in front of the computer.
7 Do you have any applications
8 other than Zoom open on the computer?
9 A I have a clean declaration of
10 '711 in PDF format open.
11 Q And when you talk about the
12 declaration, are you referring to
13 Exhibit 2009, your second declaration in
14 this proceeding?
15 (Exhibit 2009, Declaration of
16 Stephen Campbell in Support of Patent
17 Owner's Response, was remotely introduced
18 and provided electronically to the
19 reporter, as of this date.)
20 A Yes, that's correct. It's the
21 same thing that I have printed out. It's
22 the second declaration.
23 Q Oh, okay. So I missed the fact
24 that you had printed that out. I thought
25 you had printed out Exhibit 101, the '711

1 Patent itself.
2 A No. I'm sorry if I gave you the
3 impression. This is the declaration.
4 Q Understood.
5 Okay. Any other files open on
6 your computer besides a clean copy of --
7 A No --
8 Q Okay.
9 A -- nothing else is on my
10 computer.
11 Q Got it.
12 And no other application is
13 running.
14 A No other applications are
15 running.
16 Q Okay. Thank you.
17 Now, what did you do to prepare
18 for the deposition today?
19 A Reviewed the declaration several
20 times, reviewed Kim and Park and Fang. I
21 reviewed the comments by Dr. Banerjee. And
22 then I discussed the declaration with Ben
23 Smith and Adam, another attorney from
24 Latham & Watkins.
25 Q And who was that other attorney?

1 A Adam -- again, you would have to
2 tell me the last name. I don't recall.
3 I only saw him this one time.
4 Q Did you review anything that is
5 not of record in this IPR proceeding to
6 prepare for this deposition?
7 A I probably can't think of
8 anything that I did to prepare for it.
9 MR. SMITH: Can you explain --
10 can you explain just what that means,
11 anything of record, for the witness?
12 THE WITNESS: I appreciate that.
13 Yes, please.
14 MR. HSU: Appreciating the fact
15 anything that I say that's not clear,
16 that the request for clarification
17 comes from Dr. Campbell himself.
18 BY MR. HSU:
19 Q But what I referred to was
20 simply that exhibits and papers that the
21 two parties have submitted to the Patent
22 Office in connection or as part of this IPR
23 proceeding.
24 A Then no, I didn't refer to
25 anything else other than those documents.

1 Q Okay. And how long did you meet
2 with Mr. Smith and Adam to prepare for this
3 deposition?
4 A It was about seven hours.
5 Q And was that -- did that take
6 place yesterday?
7 A Yes.
8 Q Did you speak to anyone else to
9 prepare for this deposition?
10 A So I have to ask exactly what
11 you mean by to prepare for this
12 declaration, because I've been working with
13 several attorneys at Latham & Watkins to
14 create the declaration. They did not
15 participate in the -- getting ready for the
16 deposition.
17 So are you asking about the
18 declaration or the deposition?
19 Q I was asking about the
20 deposition, but apologies if I misspoke.
21 A Then the answer is no, there was
22 no other ones that I worked with on that.
23 Q Now, you mentioned that you work
24 with several Latham & Watkins attorneys to
25 prepare your declaration.

1 Can you describe that process a
2 little bit? For example, did you come up
3 with a first draft of your declaration?
4 MR. SMITH: Objection.
5 Privilege.
6 A My understanding is that if we
7 have a privilege objection, that I'm not
8 required to respond.
9 Q Now, do you recall when you were
10 first contacted about this particular
11 matter?
12 A Yes. It was very early in the
13 year 2025. I can't give you the exact
14 date, but it would be January/February time
15 frame.
16 Q Do you recall when you started
17 working on your -- strike that.
18 You submitted two declarations
19 in this proceeding, correct?
20 A Yes, that's correct.
21 Q Do you recall when you started
22 working on the first declaration?
23 A Relatively early. It was one of
24 the first things -- one of the early things
25 that we did.

1 So March, something like that,
2 maybe even February.
3 Q And do you recall when that
4 first declaration was submitted by any
5 chance, roughly?
6 A No, I'm sorry, I couldn't say.
7 Q Okay. Do you recall when you
8 started working on this second declaration
9 that -- Exhibit 2009 that we had mentioned
10 earlier?
11 A I believe that was in the summer
12 because I believe we submitted it several
13 months ago.
14 So it must have been late to
15 mid, early summer or midsummer.
16 Q Do you recall roughly how much
17 time you spent on -- working on this
18 declaration, Exhibit 2009?
19 A I would guess about 20 to
20 30 hours.
21 As I think more about it, it was
22 closer to 20.
23 Q So let's turn to your
24 declaration, Exhibit 2009, which you have a
25 copy of in front of you --

1 MR. HSU: Actually, if we may go
2 off the record just real quick? I
3 need to -- for some reason, realtime
4 is not working for me.
5 (Whereupon, a brief recess was
6 taken from 9:16 a.m. to 9:17 a.m.)
7 BY MR. HSU:
8 Q Thank you for your patience,
9 Dr. Campbell.
10 Okay. So you have a copy of
11 Exhibit 2009 in front of you.
12 A I do.
13 Q Great.
14 And the first section,
15 "Introduction and Qualification."
16 You have been a professor -- or,
17 actually, you had been a professor at the
18 University of Minnesota since 1986,
19 correct?
20 A That's correct.
21 Q And you haven't engaged in,
22 generally speaking, CMOS fabrication
23 technology.
24 Is that a correct
25 characterization of your work?

A That's a characterization of part of my work, yes.

Q Okay. How would you characterize your work yourself?

A My work, if you want a general version, I work -- I have worked on the fabrication of semiconductor devices and semiconductor materials.

Q And what sort of devices have you worked on?

A The largest section would be CMOS, but in addition, I worked on BioMEMS solar cells, and that is to say, portable devices.

Yeah, those would be the three most prominent.

(Discussion held off the record.)

BY MR. HSU:

Q So, Dr. Campbell, if you don't mind, just repeat for us what sort of CMOS -- or, excuse me, what sort of semiconductor devices have you worked on personally?

A I worked on process technologies

1 and devices for CMOS, for the MEMS in
2 general, but particularly BioMEMS and other
3 devices.
4 Q And by "MEMS," are you referring
5 to micro-electromechanical systems?
6 A That's correct.
7 Q Have you personally worked on
8 solid-state memory devices?
9 A I have worked on solid-state
10 memory devices as a consultant for a
11 company, not as part of my academic work.
12 Q And in what role were you
13 involved in that consulting work?
14 A The company had some problems
15 with the yield and other concerns of the
16 devices. They were trying to bring up a
17 new technology, and they wanted me to
18 provide advice as to what might be the
19 problem.
20 Q And what sort of new technology
21 was that?
22 MR. SMITH: I'd like to caution
23 the witness just not to reveal any
24 confidential -- third-party
25 confidential information.

1 A That's exactly what I was going
2 to say. I signed an NDA for this. I can't
3 tell you -- the company. I can't tell you
4 the name of the device. I can only say a
5 general, that it is a memory device, but I
6 can't tell you any more than that.
7 Q In what year were you engaged in
8 this consulting work?
9 A Late 2023 -- no, early 2023
10 going into -- it was about a year. So
11 let's say all of '23.
12 Q If you can comment on whether
13 the device was a 3D NAND memory device, I'd
14 appreciate that.
15 A Again, I can't say --
16 Q Okay.
17 A -- on account of my NDA.
18 Q Understood.
19 Now, in paragraph 8 of your
20 second declaration -- and unless -- I'll
21 simply refer to that as your declaration,
22 unless I'm explicitly referring to your
23 first declaration. Okay?
24 A That's fine.
25 Q All right. So in paragraph 8 of

1 your declaration, you mention that you were
2 instructed to assume a priority date for
3 the '711 Patent as August 31, 2017,
4 correct?
5 A Yes, I believe that's right.
6 Let me just take a look at it.
7 Again, paragraph number 8?
8 Q Correct.
9 A Yes, August 31, 2017.
10 Q Okay. And let's also use that
11 as the applicable date for questions in
12 this deposition as it relates to the state
13 of the art and your experience, unless I
14 say otherwise.
15 Is that okay?
16 A Yes, I accept that.
17 Q So would it be fair to say that
18 you don't have personal experience working
19 with etch-stop layers in a 3D NAND memory
20 as of the priority date?
21 A As of the priority date, I can
22 safely say that that's true.
23 Q So what makes a layer an
24 etch-stop layer?
25 A An etch-stop layer is a layer of

1 material underneath a film that you are
2 trying to etch, and the etch rate of that
3 etch-stop material is much slower as the
4 etch rate is much lower than the chemistry
5 that's being used to etch the upper film.
6 Q What is the function of that
7 etch-stop layer?
8 A The etch-stop layer is used to
9 protect materials underneath the etch-stop
10 layer.
11 Q Would it be fair to say that in
12 particular -- strike that.
13 And is it fair to say to
14 typically there may be multiple layers of
15 materials underneath the etch-stop layer?
16 MR. SMITH: Objection. Form.
17 A You're saying that it would --
18 I'm sorry, would you say it again?
19 Q Let me re-ask the question.
20 Now, there may be one or
21 multiple layers of material underneath the
22 etch-stop layer.
23 Are you with me so far?
24 A Yes, I agree with that
25 statement.

1 Q Okay. And is the function -- is
2 the primary function of that etch-stop
3 layer to protect the layer that is
4 immediately beneath it?
5 A It's kind of a hazy question.
6 I guess the primary goal is to
7 protect the first layer underneath the
8 etch-stop layer, but if it fails, it's
9 going to attack not just the first layer
10 but any subsequent layers may be attacked
11 as well.
12 So I can make the case that it's
13 to protect all the layers underneath.
14 Yeah.
15 Q How does a POSITA -- strike
16 that.
17 You mentioned that the etch-stop
18 layer may fail, correct?
19 A If it doesn't have a good
20 etch-stop layer, yes, it could happen.
21 We try to prevent that. We try
22 to avoid that.
23 Q And what makes one a good
24 etch-stop layer as opposed to a bad
25 etch-stop layer?

A Going back to my previous response on this, an etch-stop layer should have a very low etch rate when exposed to the etching conditions that are used in the -- in removing material above the etch-stop layer.

Q Is it always -- strike that.

Is the concern always with respect to etching the layer that's above the etch-stop layer?

MR. SMITH: Objection. Form.

A It's hard for me to imagine some other condition. It's an etch-stop.

So the etch must be stopped, which means that there must be something above the etch-stop layer to have it active as a stop.

Q And is it fair to say that the etch-stop layer is protecting the material underneath from the etching of the layer that's immediately above the etch-stop layer?

A Say that again. I'm sorry. It was a little bit convoluted.

Q Sure. Let me try again.

1 There may be one or more layers
2 above the etch-stop layer, correct?
3 A There can be, yes.
4 Q Is it fair to say that the
5 etch-stop layer provides its protective
6 function relative to the etching of the
7 layer that's immediately above it?
8 A Yes.
9 Q In other words, the layer that
10 is in direct contact with the etch-stop
11 layer that is being etched?
12 A Yes. And when we talk about the
13 etch-stop layer having to have a much lower
14 etch rate and the conditions for etching
15 the layer directly on top of the etch-stop
16 layer, layers above that are not of concern
17 from the etch-stop layer.
18 Q How does one select -- strike
19 that.
20 How does one configure the
21 etch-stop layer such as its etch rate is
22 much slower than the layer that's above it?
23 A So etching is a complex process,
24 and you have a lot of variables to use to
25 try to achieve this difference in the etch

1 rate.
2 One of the most common ones that
3 we use is the chemistry. At its heart,
4 what you are trying to do in an etch
5 process is to turn a material which is
6 solid into material which is gas at the
7 temperature of the process, which is
8 typically reasonably close to room
9 temperature.
10 So what you want to have is, in
11 the etch-stop layer, a material that does
12 not become volatile, that is to say
13 gaseous, when it's exposed to the plasma
14 process and used in the layer just above
15 it.
16 That's the ideal situation.
17 Don't always have that, and sometimes it's
18 just slower, but that's the best.
19 Q You mentioned "plasma."
20 And how does the plasma come in?
21 A Plasma has several impacts.
22 One is inside the plasma, we
23 break up the gases that we feed into the
24 etcher, and that creates broken bonds in
25 these molecules, and those conditions, we

1 refer to them as radicals in chemistry, as
2 we call them. It was because they are --
3 they tend to want to form bonds to other
4 materials. So that's one aspect of the
5 plasma.
6 The other aspect of the plasma
7 is that you can develop a DC voltage drop
8 across the plasma, and the plasma can run
9 into numerous issues with noble gases, like
10 helium or argon or xenon, and once the ions
11 in these gases can respond to the electric
12 field and be accelerated down towards the
13 substrate where we can physically remove
14 material by sputtering.
15 Q And is the process that you
16 described involving plasma, is that a type
17 of dry-etch process?
18 A Yes, that's a dry-etch process.
19 Q Are there other types of
20 dry-etch process -- processes?
21 A Yes. And there -- so the one
22 that comes to mind is ion mill, which
23 strictly speaking doesn't have a plasma in
24 the chamber -- the wafer of the substrate
25 doesn't see plasma anywhere. It's just ion

1 bombardment, for example, ion mill.
2 But the plasma that you
3 describe, there are many flavors of them,
4 depending on what you're trying to
5 accomplish.
6 Q You mentioned ion bombardment in
7 the -- in this last process you mentioned,
8 ion mill, I think it was.
9 Now, does the plasma method also
10 involve ion bombardment?
11 A Yes.
12 So let me rephrase that just a
13 bit.
14 We often have ion bombardment in
15 a plasma etch. However, if the pressure on
16 the plasma is high enough, the ions scatter
17 off of the other atoms in the plasma. And
18 so they don't hit the surface with very
19 much energy. So there isn't a lot of
20 sputtering of the surface.
21 If you want ion bombardment, and
22 this is often used to get vertical etching,
23 you need to operate the plasma at a low
24 pressure so you don't have those
25 collisions.

1 Q So you mentioned vertical
2 etching.
3 And would you agree that is the
4 type of etching -- particularly etching of
5 the conductive structures that's at -- that
6 the '711 Patent is directed to?
7 A No. Generally, the vertical
8 etching is done in insulating materials,
9 not in conducting materials. The
10 conducting materials are added after the
11 etching.
12 Q Let me clarify.
13 The '711 Patent discloses
14 etching vertical vias that are later filled
15 with a conducting material, correct?
16 A Yes. That's what I said.
17 Q Okay. And is the vertical
18 etching that you referred to a couple of
19 answers ago the type of etching that would
20 be applicable to the etching of the vias in
21 the '711 Patent?
22 A So the etching process for the
23 vias is one of the most difficult processes
24 and steps for this kind of technology.
25 And yes, you have to have ion

1 bombardment in order to achieve -- the
2 etching engineers refer to it as an aspect
3 ratio. So the ratio has a depth of the
4 hole divided by the width of the hole.
5 You're seeing these days in 3-D
6 flash 100 to 1 aspect ratios, which was
7 unheard of a while ago. So part of that is
8 using ion bombardment. Part of that
9 involves depositing unreactive materials on
10 the sidewalls to prevent the lateral
11 etching.
12 But, yes, ion bombardment is
13 certainly an important part of that
14 process.
15 Q Now, you mentioned an aspect
16 ratio of 100 to 1.
17 What is a typical parameter --
18 strike that.
19 What is a typical diameter of
20 these vertical vias as of the priority date
21 of the '711 Patent?
22 A Well, of course there's
23 variation when you have multiple
24 generations being processed in 2017.
25 But I would expect the hole size

to be somewhere between 50 and let's say 200 nanometers.

Q So an aspect ratio of 100 would put the height in the range of 5,000 nanometers to 20,000 nanometers, or 5 to 20 microns, is that correct?

A Yes. If they had 100 to 1 aspect ratio process in production at that time. That's not true for 2017.

2017, you were probably getting 30 to 1, 40 to 1, something like that. It's only in very recent times you're getting 100 to 1.

Q And is it correct to understand that 30 to 1 or 40 to 1 ratio to be sort of the maximum depth that was achievable around that time?

A If you wanted to have a deeper method to layer stack, you'd have to go to a larger opening because you are limited by the aspect ratio.

Q Right. So a deeper layer stack, that would translate to basically more layers in a memory stream, right, or more memory cells per string, is that correct?

1 A Yes, that's correct.
2 Q So let's just take a ratio of 40
3 to 1. You mentioned the hole size is
4 somewhere between 50 to 200 nanometers. A
5 ratio of 40 to 1 would put it at roughly
6 2,000 to 8,000 nanometers, correct?
7 A I'm sorry, this is what aspect
8 ratio?
9 Q 40 to 1.
10 A 40 to 1.
11 And, I'm sorry, I meant to say
12 what hole size, 200 nanometers?
13 Q You mentioned 50 to 200.
14 A But you only gave me one number,
15 so I'm asking is it the 50 or --
16 Q Oh, so 50 would translate --
17 strike that.
18 A hole size of 50 nanometers at
19 an aspect ratio of 40 to 1 would translate
20 to a depth of 2,000 nanometers, correct?
21 A Yes, 2 microns.
22 Q And the hole size of
23 200 nanometers, again, at a ratio of 40 to
24 1 -- aspect ratio of 40 to 1, which
25 translates to 8,000 nanometers or

8 microns, correct?

A Yes.

So let's -- before we take that too far, let's play out, once they achieve the level of the etch, that's doesn't mean you have to have an 8 micron high stack. It just says that it's capable of forming or etching through that particular stack.

Generally, the companies don't run at the raggedy edge of the capabilities of the technology because you wind up losing yield, and that's not good.

So yeah, no reason to say incorrect, but that's the extreme capability of the etch technology, not the norm.

Q So what would have been -- strike that.

What would have been the typical range of the -- I guess the height of the staircase around the time of the patent, 2017?

A Generally speaking, they're about a micron, maybe a little more. But, yeah, that's what I would expect.

Q And how tall or how -- I guess "tall" is the right word -- is each of the steps involving both the gate layer and the dielectric layer?

MR. SMITH: Objection to form.

A This gets into the design of the device rather than what process capability is.

My expertise is not in design. It is in processing. I can tell you what the processing can do, and you're asking me, well, what is the design, and I don't know.

Q So let me make sure I understand.

Sitting here today, you do not know the typical height or the typical range of heights of a step in a staircase structure as of 2017, is that correct?

A I could make an estimate of it because we know roughly how many transistors are in the string.

But I'm being deposed as an expert in this area, and I'm not an expert in the design of the device.

1 So it would be not unusual to
2 see 32 transistors in a string and then if
3 you take the thickness, you can find out
4 the area of the thickness of each layer.
5 Again, you're asking me
6 design -- not only design now, but design
7 of 2017. That was before I really got into
8 these kinds of memories.
9 Q Okay. So just let me make sure
10 I understand.
11 So you mention in 2017, the
12 typical height of a staircase was roughly a
13 little more than 1 micron, correct?
14 A That's my impression, yes.
15 Q And your impression was also
16 that it was common to have, for example, 32
17 transistors in a memory string, correct?
18 MR. SMITH: Objection. Form.
19 A Again, yes, that was -- that
20 would be my guess. If it turned out to be
21 16, I wouldn't be particularly amazed.
22 Again, I'm not a designer.
23 Q But given the same process, a
24 string of 16 transistors would be expected
25 to have roughly half the height for the

1 staircase than a string of 32 transistors,
2 correct?
3 A If the total stack thickness is
4 the same, then yes.
5 Q By "total stack thickness," are
6 you referring to the thickness of each
7 step, meaning one gate conductor and one
8 dielectric?
9 A No. I'm saying if the height of
10 the total stack remained fixed, then your
11 analysis is correct.
12 Q My apologies. I need to -- I
13 don't quite get it.
14 So my question was, given the
15 same process, a string -- a memory string
16 of 16 transistors would roughly have half
17 the height for the staircase than a string
18 of 32 transistors?
19 A Right. If we want to put it
20 that way, if the thickness of each layer is
21 fixed between these two examples, then yes,
22 the thickness would be approximately half.
23 Q Would that be the more typical
24 way to design a device rather than keeping
25 the height of the total stack fixed

1 regardless of the number of transistors in
2 each string?
3 A Processing is difficult and is
4 strewn with limitations.
5 You want to get more
6 transistors, you have a more capable
7 device, but the etch process at 2017 would
8 not allow things that are really thick.
9 You could make the layers
10 thinner, but then you might have very high
11 resistance in the gate because the metal is
12 very thin on that.
13 So it is a -- it is a highly
14 limited process. What can I really achieve
15 and yield it in a timely manner? It's --
16 yeah. Maybe. But it's very difficult,
17 very complex.
18 Let me provide a small bit of
19 background.
20 We mentioned this company that I
21 was consulting with on a memory device.
22 They hoarded all this technology from
23 another source, and they couldn't get it to
24 yield. Sometimes it would yield, sometimes
25 it won't, but when it yielded, maybe it was

1 10 percent. This is not a -- this is not
2 good.
3 So we found out what was wrong,
4 and I can't tell you what it is, but it was
5 an extremely minor thing that caused a
6 cascade of problems. And it took 18 months
7 for the company to solve that problem.
8 And during that time, they had
9 an etch engineer, a photo engineer, a
10 deposition engineer, a device engineer, a
11 device modeling person, a reliability
12 person, all of them working on this
13 problem, along with dozens of technicians
14 running processes -- running lots through
15 the line sucking up capability that would
16 be used for something else.
17 It is a delicate operation to
18 get something working and have it meet the
19 criteria that you can yield it, and it's
20 very easy to step off that ledge and lose
21 it.
22 Q So you were referring to your
23 consulting work in the 2023 time frame,
24 correct?
25 A Yes, 2023.

1 But I was -- worked in the
2 industry prior to going to university doing
3 obviously larger geometry, but CMOS, same
4 thing. You are always on the edge trying
5 to keep this thing running at a high yield.
6 Very difficult. Very difficult.
7 This is a complex and -- it is
8 up with -- the state of the art CMOS and 3D
9 flash, it's very challenging.
10 Q Now, I think you mentioned sort
11 of a cascading effect in resolving that
12 issue.
13 Is it fair to say that these are
14 adjusting a number of interacting
15 parameters that have certain tradeoffs to
16 together -- strike that.
17 So you mentioned a cascading
18 effect, and I think you agreed, right?
19 A Yes.
20 Q Is it fair to say that this
21 cascading effect is related to or caused by
22 a number of parameters -- a number of
23 interacting parameters that together must
24 form a valid process to fabricate that
25 device?

1 MR. SMITH: Objection. Form.
2 A So yes, but the parameters
3 release the outcomes of the various
4 processes. They have a variation. Even if
5 you think you are doing exactly the same
6 thing, you will get something within a
7 range.
8 And sometimes variations of one
9 process step impacts variation of another
10 one, and the two combining, and you wind up
11 with out-of-spec results, but as a result,
12 the circuit doesn't work.
13 I mention this because, again,
14 if we go back to the etching thing, you
15 don't want to process on the edge of the
16 capability of the etch tool. You want to
17 be very comfortable in the range where
18 you're not going to see a lot of variation
19 from lot to lot.
20 Q Right.
21 And the variation you're
22 referring to is an example of manufacturing
23 tolerance, right?
24 For example, the law of large
25 numbers has sigma distribution, you know,

1 in manufacturing devices of millions of
2 transistors or billions of transistors,
3 correct?
4 A That is correct. All of them
5 have to work.
6 Q And that variation exists even
7 when you're going way back, you know, the
8 first diode, when they mass manufacture the
9 first diode, the same issue existed,
10 manufacturing the variation, correct?
11 A Yes. It isn't accumulating yet
12 because it is the first process step, but
13 every step is essential. Every step has to
14 be -- they work very hard on reducing the
15 variation in their process, every single
16 step.
17 MR. HSU: Now, we've been going
18 for about an hour. Would you like to
19 take a break right now?
20 THE WITNESS: Sure.
21 MR. HSU: Okay. Off the record.
22 (Whereupon, a brief recess was
23 taken from 10:01 a.m. to 10:11 a.m.)
24 BY MR. HSU:
25 Q Dr. Campbell, just before the

1 break, we were talking about manufacturing
2 variability.
3 Do you recall that?
4 A Yes, I recall that.
5 Q Is it fair to say that it has
6 been always a concern in semiconductor
7 manufacturing, for example, from Nvidia's
8 very first GPU until it -- until, you
9 know -- until today as the most advanced AI
10 chip?
11 MR. SMITH: Objection to form.
12 A Are you asking me if process
13 variation has been a concern over that
14 period of time?
15 Q Or longer than that period of
16 time.
17 A I've been working on fabs for
18 40 years, and it's been a problem all that
19 time.
20 Q Something that people always had
21 to be mindful of and address, correct?
22 A Yes, absolutely.
23 Q Five years ago, I would use an
24 Intel CPU as an example, but times have
25 changed.

A Yes, they have.
Q Now, you mentioned that the etch-stop layer needs to have a slower etch rate than the layer immediately above that's being etched, correct?
A That's correct.
Q And you mentioned that etch chemistry is one primary method for achieving that relative etch selectivity, correct?
A That's correct.
Q And that etch chemistry is dependent on the materials that are used for these two adjacent layers, correct?
A I would say it a little bit differently.
You would see the chemistry of the etch that is selected to etch the material on top.
Q And not to etch or to etch very slowly the etch-stop layer, correct?
A Correct, yes.
Q And what is this concept of reverse etch selectivity?
A I haven't heard that term

1 before. Perhaps you could elaborate.
2 Q How about the term "reverse
3 selective etching"?
4 A Again, I haven't heard it.
5 Q Okay. Let's bring up
6 Exhibit 1001.
7 Let me drop it in the chat
8 perhaps. Let me see how this works. Let
9 me see if I can drag it.
10 Okay. That seems to work.
11 (Exhibit 1001, U.S. Patent No.
12 10,672,711 B2, was remotely introduced
13 and provided electronically to the
14 reporter, as of this date.)
15 BY MR. HSU:
16 Q Let me know when you get it.
17 A It says that you have shared a
18 file.
19 Q Do you have the '711 Patent?
20 A '711 Patent, yes.
21 Q Okay.
22 Let's go to column 1, roughly
23 line 64.
24 A One second.
25 Are you going to display it from

your screen or do you want me to pull up my own version?

Q Oh, whichever you prefer.

A Why don't you just project it so I see what you see.

Q Okay. So hang on a second.

All right. Can you see the '711 Patent that I'm sharing on the screen?

A Yes, I can read it now.

Q Okay. So...

Okay. This is column 1. Let me zoom in a little more.

Column 1, line 64, do you see the phrase "reverse selective etching"?

A I see that.

Q Does that refresh your memory as to this term?

A Oh, okay, yes.

All they're saying is that you're using the chemistry that actually is a etch-stop layer, not the layer above it. It's -- yeah, that's fine. Okay. There's nothing magical about it.

Q Let me make sure I understand what you said.

1 You're saying you're using the
2 chemistry that etches the etch-stop layer,
3 not the layer above it?
4 A Correct.
5 Ultimately, you have to make a
6 contact at the bottom of that via. And so
7 when the etching of the upper layer is
8 done, we have the actual hole through the
9 etch-stop layer, so you need an etch
10 chemistry that will attack the etch-stop
11 layer so that you can make a hole in it.
12 Q Now, the '711 Patent discloses a
13 barrier layer, correct.
14 A Yes.
15 Q And that barrier layer is
16 underneath -- or directly underneath the
17 etch-stop layer, correct?
18 A Yes, that's correct.
19 Q And would you agree that the
20 barrier layer also has an etch-stop
21 property with respect to the etch-stop
22 layer?
23 A Yes, that's exactly what it
24 does.
25 Q What is the purpose of having

that additional etch-stop layer, if you would, since it also serves an etch-stop function?

MR. SMITH: Objection. Form.

A There's two potential applications in -- and it depends on the chemistries of the etch and the materials that you're using.

But, generally, you want to ensure that when you remove the layer closest to the gate material, it will have a very high selectivity to compare to removing the gate.

So this is called punch through. If you remove the first number, you have to have a chemistry that doesn't detect tungsten.

Tungsten is the most common gate material that's used in these devices. And so often that's it, it's just the chemistry that we will need to use to etch the etch-stop layer might be -- might attack the tungsten.

And it's not really a punch through in the sense that a punch through

is usually thought of as occurring when you're etching these little long vias and you don't have an etch-stop layer or insufficient etch-stop layer.

But, again, you have to make a hole in the etch-stop and you have to protect the tungsten gate during the etch of the etch-stop layer.

So the buffer layer, the medium layer, provides a -- you can choose the material that you can etch in the chemistry that does not attack tungsten.

Q But can't you do the same with just a single etch-stop layer?

A Again, it comes down to your chemistry and your materials and the thicknesses and process.

You have more leeway by having an extra layer underneath than without it. In general, the etch-stop layers are not easily etched, and so you might have to, for example, have a lot of ion bombardment in order to volatilize that material.

Very common if it's a high-K material. It's very hard to volatilize.

1 And so you don't want those ions slamming
2 into the tungsten, and so you put the
3 second layer in.
4 It is all these pluses and
5 minuses. You get, yes, I have to put an
6 extra layer in, but no, I can do that
7 chemistry. You can -- it's always a
8 compromise.
9 Q So the additional barrier layer
10 makes achieving that compromise -- strike
11 that.
12 So the additional barrier layer
13 provides flexibility in terms of processing
14 parameters in achieving that compromise, is
15 that fair?
16 A I think that's a fair statement,
17 yes. It comes at the price of having extra
18 processing.
19 Q And that's the common tradeoff
20 in engineering, correct?
21 A Yes, absolutely.
22 Q Now, the -- as you recall, the
23 '711 Patent discloses a design in which
24 there is a high-K layer surrounding the
25 gate conductor, correct?

A I'm going to have to see the design, but yes, that's my memory.
Q Okay. And do you also recall that the high-K layer is basically right --
A Yes.
Q -- at the barrier layer?
A Yes, that is correct.
Q And does the -- strike that.
Here I'm showing you on the screen -- bear with me as I rotate this page -- Figure 9B.
Can you see that?
A Yes, I see it.
Q And so this layer that's -- that has -- that's associated with numeral 208, that's a barrier layer, correct?
A We have two layers, the etch-stop and then the lower -- I forget what -- I can never recall it, but that's the bottom of the two.
Q The bottom of the two etch-stop layers is the layer 208, correct?
A Yes.
Q And as you see here in Figure 9B, portions of the barrier layer

208 is in direct contact with the high-K dielectric surrounding the gate conductor, correct?

A That's correct.

Q And can these two layers be etched together during the etching of the via?

MR. SMITH: Objection. Form.

A Refresh my memory. What is the material 208?

Q The material 208...

Okay. So here in column 7, do you see, starting from line 50 -- let me make that a little larger -- "In some embodiments, the second insulating layer 208 can be made of similar material as the first insulating layer 104."

A And 104, you said, was a high-K, is that correct?

Q No, I did not say that.

104 -- actually, it might work better if you download the copy of Exhibit 1001 that I posted to the chat, then you can run your own searches.

But 104 -- let me rotate this

again...

104 is -- 104 is the dielectric in the stack.

A Got it. Okay.

All right. So the question is -- can we -- now that I understand it, could you repeat the question one more time?

Q Sure.

Can the layer -- barrier layer 208 and the high-K dielectric layer that surrounds the gate dielectric 525H in Figure 9B be etched together in one step?

A So I believe, based on the material selection I was just presented with, the answer would be yes because high-K materials typically have metal oxide, which is the most common one, are etched in the chlorine chemistry, whereas tungsten does not etch in chlorine. It etches in fluorine.

So you would be able to have a high etch-stop once it hit the tungsten key.

Q If I understand your answer

1 correctly then, the high-K dielectric that
2 surrounds the gate conductive layer does
3 not serve an etch-stop function in the
4 etching of the via, is that right?
5 MR. SMITH: Objection to form.
6 A No, I didn't say that at all.
7 If you are etching down in the
8 fluorine, that layer would certainly be an
9 etch-stop barrier, an etch-stop.
10 But you asked me, if you are no
11 longer doing the via etch, now we're down
12 to removing the etch-stop layers. If those
13 are high-K, then the high-K liner would be
14 etched as well. And those are done in
15 chlorine chemistry, whereas SiO2 and
16 tungsten are done in fluorine chemistry
17 instead of chlorine.
18 Q But tungsten etches in fluorine,
19 correct?
20 A In fluorine. So we don't use
21 fluorine to etch high-K. It doesn't
22 volatilize.
23 Q Correct.
24 So when fluorine is not used to
25 etch the via, the high-K dielectric doesn't

1 serve an etch-stop function, but instead is
2 etched together with the barrier layer,
3 correct?
4 A So let's review this again.
5 The etching of the via, which is
6 mostly etching on the silicon dioxide, is
7 done in a fluorine plasma.
8 You etch all of the etch-stop
9 layers. If those are high-K, you have to
10 switch to a chlorine plasma. And that will
11 go through right down to the tungsten and
12 stop because the tungsten doesn't etch.
13 So the liner of 525H effectively
14 increases the barrier with etch-stop
15 with -- because it's -- when I say, high-K
16 doesn't etch in fluorine, that's true as
17 far as it goes, but as we discussed before,
18 there's ion bombardment in the plasma, and
19 ion bombardment is not selective, or very
20 little selective.
21 So you are going to get some
22 erosion of the etch-stop layers,
23 particularly for those vias near the top of
24 the stack because they're exposed to the
25 plasma for a long time.

It's never a zero etch rate, it's just lower.

Q Now, let me break down your answer into chunks that I can digest.

So you mentioned etching silicon dioxide in the process of etching the vias, correct?

A Correct.

Q And that silicon dioxide refers to the thick -- what is typically thick layer -- here we show layer 420 in Figure 9A, correct?

A That's correct.

Q And then you mentioned that would be done using a fluorine, typically, I suppose, using a fluorine plasma, correct?

A Correct.

Q And then once that layer is etched and now we're etching through the etch-stop layer, then one might use a chlorine plasma, correct?

A With one small caveat, and that is, once the SiO2 is etched, it's going to continue to eat into the etch-stop layer,

1 but at a slower rate. So some of the
2 etch-stop will be gone by the time you
3 switch from fluorine to chlorine.
4 Q Understood.
5 And then earlier we talked about
6 reverse selective etching, correct?
7 A Right.
8 Q And that's when the etching
9 intentionally targets the removal of the
10 etch-stop layer --
11 A Right.
12 Q -- and then the barrier layer
13 is -- in this reverse selective etching,
14 the barrier layer serves an etch-stop
15 function to protect the layer underneath,
16 correct?
17 A Yes, I believe that's correct.
18 Q And so there's that additional
19 step of etching through -- intentionally
20 etching through the etch-stop layer,
21 correct?
22 A Yes. You have to do that, yes.
23 Q And then there needs to be a
24 further step. Since the barrier layer was
25 protecting the layer underneath during the

1 intentional etching of the etch-stop layer,
2 there needs to be an additional step to
3 etch the barrier layer, correct?
4 A Yes, but if that barrier layer
5 is not high-K, then you have to switch to a
6 chemistry that will etch that barrier
7 layer.
8 Q And in that step, the barrier
9 layer and the high-K dielectric can be
10 etched together using a chlorine plasma,
11 correct?
12 A Again, what this comes down to
13 is that upper layer a high-K material. If
14 it's a high-K material, then we can
15 actually remove that and the liner for the
16 gate for the sacrificial region, then you
17 can go right through both of them with
18 chlorine.
19 But if the buffer layer is let's
20 say SiO2, then you have to switch back to
21 fluorine, then switch back to chlorine.
22 It all depends on what the
23 barrier material is. You can do it either
24 way. There isn't, you know, one way to do
25 it, but you just have to use the right

1 plasma for the right material.
2 Q In cases where you would switch
3 to yet another chemistry between the
4 etching of the barrier layer and the
5 etching of the high-K layer that surrounds
6 the gate conductor, the high-K layer would
7 serve as a etch-stop during the etching of
8 the barrier layer, correct?
9 A Yes, that's correct.
10 Q But it doesn't serve that
11 function doing the etch of the etch-stop
12 layer, correct?
13 A That's correct, yes. It's
14 covered. It isn't exposed to the plasma.
15 Q How does one determine when to
16 end an etching process -- a particular
17 etching step?
18 A Well, the simplest scenario of
19 sequences of this, the simple one is just
20 to know your etch rate and time it, know
21 the thickness.
22 But that's not adequate for
23 manufacturing. Typically, we use sensors
24 to determine when the etching is done.
25 Very commonly, we will use a light source

1 or they'll look at the glow of the plasma
2 directly and you can tell what species,
3 what chemistries are in the plasma.
4 So, for example, if you're
5 etching through SiO2, there will be some
6 oxygen in the plasma because you're etching
7 SiO2. And when the SiO2 is fully etched,
8 the oxygen goes away.
9 And so you interlock the two,
10 the sensor is fed into the computer end of
11 the machine and recognize the switch.
12 Q And is that monitoring technique
13 available for all of the practical type of
14 etch chemistry?
15 A Yes, as far as I know. I mean,
16 there might be some weird chemistry out
17 there that I'm not familiar with, but the
18 standard is yes, absolutely. They've been
19 around for 20 years, 30 years.
20 Q And is that technique known as
21 end pointing or some --
22 A That's certainly one of the most
23 common, yes. There are other techniques as
24 well, but that's one of the most common,
25 end point.

1 Q What are some of the other
2 techniques?
3 A I haven't thought about this for
4 a while.
5 So I'm sorry to say, I can't
6 come up with it right now.
7 This is the one that kind of
8 went out and people typically use it.
9 Q Well, I did kind of put you on
10 the spot because this certainly -- well,
11 let me frame it this way: The '711 Patent
12 doesn't talk about this monitoring
13 technique, correct?
14 A No, no. This is something
15 that -- I mean, you're talking about
16 etching at a very high level. You're not
17 getting into the gritty details of how you
18 etch.
19 Q When you say -- strike that.
20 In your previous answer, when
21 you said you're talking about etching at a
22 very high level, were you referring to the
23 '711 Patent?
24 A Yes. It doesn't provide details
25 in exactly how the etch is going to be

1 done. It doesn't tell you what the
2 chemistry is or the bio plasma or exactly
3 what kind of a machine you're using. Is it
4 inductively coupled plasma, is it a
5 microwave plasma...
6 They're not saying any of these.
7 These are to be developed by the process
8 engineers of the companies. They're
9 providing here is the narrow path to get to
10 this particular device, you figure out how
11 to do the etching.
12 Q You're familiar with the term
13 "chemical mechanical polishing," correct?
14 A Yes.
15 Q How -- and that's known as
16 "CMP"?
17 A That's correct.
18 Q How does CMP work?
19 A CMP was developed to planarize
20 the surface, another word for direct
21 processing.
22 This is very important because
23 as we make smaller features, the window
24 where the image is focused becomes very
25 narrow.

1 So if you have topography on the
2 wafer, you can't pattern -- some of the
3 things will be fuzzy and you won't be able
4 to control the dimensions.
5 So CMP was made to flatten the
6 surface.
7 So how does it work?
8 You put the wafer on the chuck
9 and till down and you apply the solution.
10 If we're going to polish SiO2, for example,
11 you would apply a base solution, potassium
12 hydroxide or something like that, a
13 dilutant like water, and some particles,
14 and the way that it works -- also, then you
15 have a pad that comes down on top of the
16 surface of the wafer.
17 So what happens is, for oxides
18 like this, the KOH would hydrolyze the
19 surface and form OH bonds on the surface,
20 and that gives you kind of a gelatin -- not
21 quite that, but a very soft surface, and
22 the particles, as the pad turns, it pushes
23 down on the wafer, those little particles
24 will scrape off the hydrolyzed surface.
25 And that's only going to happen,

1 of course, on the high spots. And the low
2 spots, you're not pressing down on the
3 wafer. It's only the high spots you're
4 pressing down.
5 So you remove the high spots and
6 then they come down and they -- until
7 eventually it's all one plane.
8 Then they clean it off, you have
9 to get all the particles out and so forth,
10 make sure there's no scratches. Sometimes
11 it will do -- the large particles, at high
12 pressure might etch faster, and then clear
13 all that stuff off, wash it off, and then
14 do a finishing polish with some small
15 particles, a very slow, just to get rid of
16 any scratches on the surface.
17 Q So CMP produces a flat or
18 planarized surface on the top, correct?
19 A Ideally, no.
20 And, as with all processes,
21 there are limitations, but that's sort of
22 the order, description, yes.
23 Q And CMP has no direct impact on
24 materials underneath the top surface, is
25 that fair?

1 A Yes. I am not aware of any case
2 where damage was done to sub-lying layers.
3 Q Now, turning back to your
4 declaration, you mention that you wrote a
5 textbook that is -- that is the -- and I'm
6 quoting now -- the dominant text on the
7 topic, the topic I suppose referring to the
8 title "Fabricating Engineering at the Micro
9 and Nano Scale."
10 Correct?
11 A That's correct. There are
12 currently four editions in English.
13 Q And there have been four
14 editions of this textbook, correct?
15 A Yes, that's correct.
16 Q The editions being published or
17 copyrighted, as the case may be, in 1996,
18 2000, 2008 and 2013, correct?
19 A That's correct.
20 Q I imagine you have taught
21 classes using this textbook yourself?
22 A Yes, I have.
23 Q Roughly how many times have you
24 taught using your own textbook?
25 A 25 times -- let's see...

1 Q So roughly once a year since the
2 first edition almost until your retirement,
3 roughly?
4 A Yes, roughly.
5 Q What level of class was this?
6 A This is a class that is taken by
7 seniors in electrical engineering or
8 technical engineering or mechanical
9 engineering or physics or chemistry and
10 first-year graduate students in those
11 departments.
12 Q Now, we talked about -- going
13 back to the '711 Patent, Exhibit 1001, we
14 talked about the fact that it's directed
15 to -- actually, why don't you tell me what
16 you understand the '711 Patent -- what
17 problem the '711 Patent to be addressing.
18 MR. SMITH: Objection to form.
19 A The '711 Patent describes the
20 underlayer memory device in which we have a
21 gate on the top orientation with two
22 barrier layers and etch polishing -- sorry,
23 not etch polishing -- CMP polishing for
24 planarization.
25 And the other things that go

1 with this, the contacts through the array
2 contact, the active channels, the isolation
3 structures, there are a lot of events, but
4 basically, trying to make this device.
5 MR. SMITH: Counsel, we've been
6 going for about another hour, coming
7 up on the second hour, if there's a
8 good time to break?
9 MR. HSU: Sure. We can break
10 now, if that suits you.
11 MR. SMITH: That's fine.
12 MR. HSU: Okay. Let's take a
13 break.
14 Another ten minutes?
15 MR. SMITH: Sure.
16 (Whereupon, a brief recess was
17 taken from 10:56 a.m. to 11:08 a.m.)
18 THE WITNESS: In your previous
19 question, you asked me what was
20 included in the '711 Patent or what
21 were you trying to path.
22 And I've been consulting with
23 Latham & Watkins on several patents,
24 and including a couple of things that
25 were not part of the '711.

1 '711 is the gate-down top
2 staircase structure, the barrier
3 layers -- the etched-up barrier layers
4 and, oh, the etching on the vias down
5 to the steps.
6 Some of the other things that I
7 brought up were part of other patents,
8 not '711.
9 BY MR. HSU:
10 Q And, Dr. Campbell, can you
11 confirm that you did not discuss the
12 substance of your deposition testimony
13 during either of the prior break that we've
14 had so far?
15 A Yeah, absolutely.
16 Now, your question caught me off
17 guard, and I wasn't expecting that. And as
18 I was sitting here, I was like, oh, that's
19 not '711, that's the other one.
20 So no, I didn't even consult
21 with anybody about this.
22 Q And just for clarity, I thought
23 of that question after the previous break,
24 but this seemed like a perfect time, not
25 that I, you know, suspected anything, but

it just was a good opportunity to do so, let me get that question out of the way. That's all.

A No problem.

Q And, actually, I'd like to go back -- before we proceed further down the '711, I'd like to go back to just a general fabrication topic.

You are familiar with atomic deposition --

A Atomic layer deposition.

Q Atomic layer deposition, correct?

A Yes.

Q It's known by its acronym, ALD?

A Yes.

Q Why is it called atomic layer deposition?

A Because you're depositing a film basically one atom at a time. So you have extraordinary control over the thickness, and you're able to deposit into areas that are very difficult to get uniform films otherwise.

Q And do I understand that there

are, say, a couple of steps that alternate doing the ALD, is that correct?

A So the basic ALD process is to put in reactive gas and let it coat the surface and then pump that out and put in an inert gas, like argon, just to flush out any remaining stuff, and then put in reactive gas immediately after with the stuff on the surface to form the material that you want. And then you pump it out and put it again in an insert gas to flush out any remaining.

So you don't have any reactions in the gas phase, it's only on the surface.

Q And you mentioned previously that at the end of these phases -- I guess I'll call it a step -- you form a layer of -- a uniform film layer, is that correct?

MR. SMITH: Objection to form.

A Yes.

THE WITNESS: Sorry.

A Yes. Ideally, it's atomically smooth. It isn't exactly atomically smooth, but it's very close.

Q Now -- okay. So let's go back to the '711 Patent.

I can share my screen again, or if you'd like to be able to scroll, you can also open up the copy that I posted locally, if you like. Whichever you prefer.

A I have it open now.

Q Okay. You have it open now. Okay.

So then let's look at -- maybe we'll start with the figures.

Do you understand Figures 1 through 9B to illustrate the sequence of steps to form this 3D staircase memory structure?

A I'm scanning through them.

Yes, that's my sense of this sequence of the figures.

Q And then Figure 10 is a flowchart that describes this sequence, but, you know, in verbal form, is that fair?

A Yes, that's fair.

Q And in fact, in the description

of Figure 10, the patent specification frequently refers back to components or -- it mentioned in the first nine -- you know, Figures 1 through 9B or the figures themselves.

Do you recall that?

A Yes.

Q Okay. So going back then to Figure 1, what do you understand that to be illustrating?

MR. SMITH: Objection to form.

A I would say that this is a depiction of the staircase structure after the trim etching has been accomplished.

Q And thereby forming the staircase structure that is shown in Figure 1, is that correct?

A Yes, that's correct.

Q What do you understand Figure 2 to be?

A Figure 2?

Q Figure 2, correct.

A So this shows the deposition of 102, both on the tops of the pads and sides of the pads.

1 Q The deposition of 102, did you
2 say?
3 A Yes, layer 102.
4 Q And what is that there -- layer?
5 A That is the -- I'm not sure if
6 that is the buffer layer or the barrier
7 layer. I can look it up very quickly.
8 There is a staircase layer 102.
9 So it is the first insulating
10 layer in the sacrificial layer. So it's
11 two of them, 104 and 106.
12 Q Now, 104 and 106 existed in
13 Figure 1, correct?
14 A Yes, that's what the text says.
15 Sorry, back up. 104 is the
16 sacrificial layer, and 106 is the -- no,
17 sorry, 106 is the sacrificial layer. 104
18 is the dielectric.
19 So 208 is -- oh, I'm sorry,
20 that's right. I was looking at the wrong
21 part of the figure.
22 208 is the first barrier layer.
23 106 is the sacrificial layer. 104 is the
24 insulating layer.
25 Q So let me just re-ask that

1 question.
2 What do you understand Figure 2
3 to illustrate?
4 A It illustrates the deposition of
5 layer 208.
6 Q Okay. How about Figure 3, what
7 do you understand Figure 3 to illustrate?
8 A Figure 3 is the deposition of
9 the second barrier layer 310.
10 This is our etch-stop layer.
11 Q And would you agree that the
12 thickness of both barrier layer 208 and
13 etch-stop layer 310 appear relatively
14 uniform?
15 A Yes.
16 Q And that's a result of the
17 deposition technique that's used to deposit
18 these layers, correct?
19 A Yes.
20 Q For example, ALD, that we just
21 talked about, can be used to form these
22 layers?
23 A Yes.
24 Q Okay. What do you understand
25 Figure 4 to be illustrating?

A Figure 4 is deposition and planarization of what we would call the third insulating layer 420 in that -- yeah. The deposition and subsequent planarization.

Q And what do you understand Figure 5A to illustrate?

A 5A already shows the active channel along with the deposition of layer 530, which is an insulating layer.

Q And that's where the memory channel is formed or will be formed, correct?

A Yes. They're going to put the semiconductor there -- silicon, and that's where the channel will form.

Q What do you understand Figure 5B to illustrate?

A Figure 5 shows a little over one sequence of sacrificial layer and insulator. Let's see...

Okay. The sacrificial layer is gone. Now we have a 525M, which is usually the tungsten.

So they've done ALD to fill this

1 cavity after they've done the sacrificial
2 layer and conduct --
3 Q And how is that -- strike that.
4 Is it fair to say that the gate
5 layer -- the gate conductive layer,
6 including 525M and 525H, is not in direct
7 contact with the etch-stop layer 310?
8 A There is an intervening layer at
9 208, which is referred to as the second
10 insulating layer.
11 Q So the answer to my question
12 that the gate conductive layer is not in
13 direct contact with the etch-stop layer 310
14 is yes, is that correct?
15 I mean, it's not in direct
16 contact.
17 A It is not in direct contact,
18 that's correct.
19 Q And layer 208, which you called
20 the second insulating layer, is also called
21 the barrier layer, correct?
22 A It is referred to that in some
23 cases, yes.
24 Q And the '711 Patent has a
25 configuration where the barrier layer 208

is not present in the device, correct?
A I would have to look at that to see whether that is in fact true.
Q Okay. Let me just direct your attention then to claim 13, in particular in comparison with claim 1.
A Okay. Will you hang on just a moment?
Q I beg your pardon?
A I said, I'm reading it. Give me a few seconds.
Q Sure.
A So as I read it, it says an etch-stop layer is deposed on a portion of the stack of its step, and an insulating layer is deposed on the etch-stop layer.
So it would seem that this claim would change the sequence of the two layers.
Q And what do you mean by changing the sequence of the two layers?
A The diagram that we just looked at had an insulating layer. It was referred to as the second insulating layer with the etch-stop layer on top of that.

In this one, the etch-stop layer is disposed on a portion of the gate stack of each stop. So it was directly in contact with the high-K, which encapsulates the tungsten, and the insulating layer is disposed on top of that.

Q And is that insulating layer disposed on top of the etch-stop layer?

A That's what it says.

Q The second insulating layer, otherwise known as the barrier layer?

A An insulating layer disposed on the etch-stop layer. So it is on top of the etch-stop layer.

It doesn't use the words that you just gave me, it just says an insulating layer.

Q And what is your understanding of what that refers to?

A That it's an insulating layer.

Q Does it refer to the layer -- insulating layer 208?

A It doesn't say that.

So I'm -- it would be speculation on my part. You're asking for

1 things I know. I don't know. It doesn't
2 say that.
3 Q So going back to my earlier
4 question, you said that claim 13 would
5 change the sequence of the two layers.
6 What did you mean by that?
7 A In the figure that we have been
8 previously looking at, there was an
9 insulating layer between the high-K, which
10 encapsulates the tungsten, and the barrier
11 layer.
12 In this process, the barrier
13 layer is indirectly -- directly in
14 contact -- sorry, erase that.
15 The etch-stop layer is directly
16 in contact with the high-K material, which
17 surrounds the tungsten. And there is an
18 insulating layer on top of the etch-stop
19 layer instead of under the etch-stop layer.
20 Both of them are insulating
21 layers. You're just asking me for what the
22 names are for them, and claim 13 doesn't
23 give it a name other than insulating layer.
24 Q Okay. Now, let's move back to
25 Figure 6.

A Okay.
Q What do you understand Figure 6 to illustrate?
A Okay. So Figure 6, we have put in the semiconducting material 643, and we have etched down the vias by 2 and into the etch-stop layer.
And is there anything else?
Nope. I don't see anything else.
Q And these 640Us and 640Ls are the vias and that will later become conductive structures, correct?
A That's correct.
Q And this is what you discussed earlier as to the aspect ratio because these have to have a relatively deep depth, I guess, for lack of better word, vertically, correct?
A Correct.
Q And so in Figure 6, as you put it, the etch has gone through layer 420 and is partially through the etch-stop layer 310, correct?
A Yes.

Q And so the vias, or these openings, are exposing portions of the etch-stop layer, correct?
A Yes, that's correct.
Q And then let's turn to Figure 7.
What do you understand Figure 7 to illustrate?
A In this process, they have etched all the way through the etch-stop barrier and slightly into the insulating layer that's directly under the etch-stop layer.
Q And so as illustrated in Figure 7, the openings, or the vias, now leaves the barrier layer 208 exposed, is that correct?
A It leaves 208 exposed, that's correct.
Q And the exposing of the etch-stop layer and the exposing -- in Figure 6, and exposing the barrier layer in Figure 7, is it fair to say that they're just the natural consequence of etching vertically through from top to bottom through these layers?

A I don't really understand what the question is.

Q Sure. Let me try to rephrase.

So we're etching these holes from top to bottom through layers 420, 310 and 208, correct?

A Yes.

Q Is it natural in that etching process to be exposing, at some point, the layer -- the etch-stop layer 310?

A By "exposing," you mean opening up a surface area of the barrier to the air?

I'm just not sure exactly what you're asking.

I'm not trying to be trite, I'm just not sure.

Q Totally fine.

By "exposing," I was simply referring back to our earlier discussion. I think you had agreed that in Figure 6, the etch-stop layer 310 is exposed through the openings, correct?

A Again, by "exposed," do you mean that the hole can be accessed -- let's put

1 it that way -- as an interface with air.
2 If that's what we mean by
3 "exposing," then yes for that one and yes
4 for this one.
5 Q And that one and this one refers
6 to Figure 6 and 7 --
7 A Exactly.
8 Q -- in which -- okay -- in which
9 the etch-stop layer and barrier layer are
10 successively exposed, correct?
11 A Yes, correct.
12 Q Let's move to Figure 8A.
13 What do you understand Figure 8A
14 to illustrate?
15 A 8A shows that the etch has
16 proceeded through the insulating layer
17 right down to the gate region.
18 It is not clear, that I can see,
19 whether or not it has gone through the
20 high-K layer in the tungsten gate area.
21 It's either on the high-K or it's on the
22 tungsten, but I can't tell from the
23 diagram.
24 Q Fair enough.
25 I think Figure 8B makes that

clear.

A Okay.

Q If you would describe what your understanding of Figure 8B to illustrate.

A Okay. So they have gone through the lower insulator and through -- the via has gone through the insulator or -- second insulator and gone through the high-K. Yeah, the high-K. And the exposed now is the tungsten.

Q And what do you understand Figure 9A to illustrate?

A So 9A, they have added the 945. That would be what goes down to make the contact. Again, commonly tungsten.

Q And what do you understand Figure 9B to illustrate?

A So 9B now shows the layer 945 making contact with the gate.

Q So then to summarize, the etch -- strike that.

To summarize, the via, or opening, etch process is illustrated between Figure 6 through Figure 8B inclusive, correct?

A Yes. 9, you would start adding layers. So yes.

Q And the successive figures illustrate the etching of successive layers and exposing the layer underneath the layer that has been etched away, correct?

A Yes.

Q And so if I may turn your attention to column 7, line 64 through 66.

Let me know when you get there.

A I'm sorry, can you give me the numbers again?

Q Column 7 starting from line 64.

A Sorry. My Siri came to life.

So column 7, I just need to know which lines.

Q Starting from 64.

A Okay. Thank you.

Q So let me know when you get there.

A Yeah. So far, it just says that there are different etch-stop materials that you can use. It is actually different from the second insulating layer.

Q And would you agree that's

1 because the second insulating layer 208, or
2 barrier layer 208, serves an etch-stop
3 function doing the etching at the etch-stop
4 layer 310?
5 A Certainly that can be one reason
6 for having that layer there. I'm not sure
7 that it's the only reason, but it is a
8 valid reason.
9 Q So I probably wasn't clear.
10 I didn't mean to ask about the
11 reason for having that second insulating
12 layer 208. Rather, I was asking for the
13 reason that the two layers, 310 and 208,
14 are made from different materials.
15 That's to enable the reverse
16 selective etching that we discussed
17 earlier, correct?
18 A A little bit different.
19 When you say, "reverse," it
20 means you're going to etch the barrier
21 layer faster than you would etch the oxide
22 that was on the top that it went down
23 through.
24 It doesn't have to do with the
25 next layer or the next layer. That would

1 just be, again, an etch-stop area with an
2 etch differential.
3 But getting to your question, is
4 it -- I come back to you're asking me the
5 reason why it has to be a different
6 material, and when I say that could be a
7 reason, I can't define what their rationale
8 is besides, yes, that could be a reason.
9 There may be other reasons, I
10 don't know.
11 Q So first, I think I need to
12 clarify your understanding of the two terms
13 "selective etching" and "reverse selective
14 etching" --
15 A Yes.
16 Q -- to make sure we're on the
17 same page.
18 A So "selective etching" means
19 that the material that you are attempting
20 to etch the upper layer, that is to say,
21 etches at a much faster rate under some
22 etch conditions than the layer beneath it.
23 That's a selective etch.
24 A reverse selective etch is the
25 layer that's now exposed at the bottom

1 etches at a higher rate than the oxide that
2 was on top because, again, it can etch
3 laterally through that SiO2, and you don't
4 want it to widen the opening.
5 Q Understood.
6 So back to column 7, line 64,
7 the fact that the etch-stop layer 310 is
8 made of a suitable insulating material
9 different from the barrier layer 208 allows
10 that selective etching to occur through the
11 etch-stop layer 310, correct?
12 A Yes, I agree with that.
13 Q Now, figures -- the figures that
14 we saw shows roughly -- oh, maybe a dozen
15 or so steps?
16 A Yes.
17 Q But you don't understand this to
18 be limiting, right?
19 In 2017, like we discussed
20 earlier, you could have 32 layers, for
21 example, 32 steps in the staircase for
22 example?
23 A Yes. In reading the patent, I
24 assume that the number of steps being shown
25 were not limiting.

1 Q Right. But does the '711 Patent
2 disclose how high the staircase may be?
3 A I didn't see anything in '711
4 that limited it.
5 Q And the etch-stop layer is to
6 protect the underneath layer because
7 etching a hole to a step on the top
8 requires much less time than etching a hole
9 to the bottommost step, for example,
10 correct?
11 A More to the point, you don't
12 have drastically different exposure times,
13 like you do with the initial etch.
14 Yes, there -- that just means
15 the etch is going to be shorter, but the
16 important thing is that the amount of
17 etch-stop that has to be etched doesn't
18 vary nearly as much as the amount of the
19 top insulator how much it has to be etched.
20 Q I probably wasn't clear. So let
21 me rephrase my question.
22 For example, looking at
23 Figure 6, this step involves etching the
24 vertical openings to --
25 A Yes.

1 Q -- on top of each step, correct?
2 A Correct.
3 Q And the height of the
4 openings -- the vertical openings on the
5 left where it's going towards -- going to
6 the -- a step on the bottom is considerably
7 longer or larger than a vertical opening on
8 the right of the figure where it's going to
9 a step near or at the top, correct?
10 A The amount that's etched near
11 the top is much thinner than the amount
12 that's etched further down.
13 Q Which is why this idea of using
14 an etch-stop layer comes in, so that the
15 etching of a vertical hole to a top step
16 would be slowed down significantly by the
17 etch-stop layer while the etching of a
18 deeper hole continues, correct?
19 A That's correct.
20 Q So is it fair to say that the
21 height difference between a topmost step
22 and a bottommost step is an important
23 consideration as to how resistant the
24 etch-stop layer needs to be?
25 A Yes, certainly.

Q And the etch resistance of the etch-stop layer includes factors like its material and the etching -- or the etch chemistry, correct?

A Certainly those are two of the important parameters.

Q And the etch resistance of the etch-stop layer includes a factor like its thickness, correct?

A Yes.

Q In other words, factors such as etch-stop material, etch chemistry, etch-stop thickness are important factors relative to the height difference between a short vertical opening and a long vertical opening, correct?

A Yes.

Q Now, let's turn to -- turn back to your declaration.

A Okay.

Q So you recall that in the Kim and Park reference, their figures illustrate a gate stack on the bottom configuration, correct?

A I'm sorry, Kim and Park?

Q Correct.
A Can you tell me where this is in the declaration?
Q Oh, sure. Certainly.
Kim, roughly around paragraph 35.
Why don't we start there.
A Okay. I'm with you.
Q Okay. And you recall that Figure 22A here, for example, shows a gate stack on the bottom -- as the bottom layer of each step, correct, underneath a dielectric layer?
A Yes. This was the manipulated figures, as I recall.
Yes.
Q Actually, this isn't -- I mean, I'll just point out that --
A Oh, I'm sorry, you're right. This is directly from Kim.
Q Okay. Yeah.
A Yes.
Q And similarly, Park -- and here we can go to paragraph 68, and it's page 45 of the PDF...

A Yes.
Q Similarly shows a gate stack on the bottom of each step, correct?
A So if I look at Figure -- let me put on my glasses -- Figure 6, it shows a gate on the bottom with an insulator on top.
Q Actually, it's Figure 9I.
A Figure 9?
Q Figure 9I, in paragraph -- let's see, which paragraph did I tell you?
A Oh, I'm sorry --
Q Paragraph 68. Paragraph 68.
A Okay. Whatever.
So this is 9I, yes. I see a gate on the bottom, right.
It does not have the etch-stop layers covering the first level on the side, but yes.
Q Okay. And you recall that Dr. Banerjee opined based on a modified version of these figures where the gate stack is on the top layer of each step, correct?
A Yes, I saw that.

Q Now, if I may direct your attention to paragraph -- oh, this is a long paragraph -- 41.

So bottom of PDF page 26 -- sorry, 27 and printed page 26, and top of printed page 27.

Let me know when you get there.

A I'm at 26.

Where do you want me to start?

Q Okay. So on the very last line of page 26, it says, "For example, Dr. Banerjee's modified Figure 22A not only swaps the layers, but also shortens the contact plugs to terminate within gate electrode layers."

Did I read that correctly?

A Yes, you did.

Q Okay. So what do you mean by swaps the layers?

A The insulating layer goes down second -- sorry, the insulating layer is on the one where the gate layer is on top.

Q So is that swap -- layer swapping a reference to the modification of the figures?

A Yes. As I recall, Dr. Banerjee used Kim's diagram and constructed one that would move the gate layer up on top of the oxide.

Q Now, is it fair that this layer swapping describes the modification to the figures, but when a -- when fabricating a device that has a gate stack on top, do you understand Dr. Banerjee to not propose the layer swapping as the word "swapping" may suggest, meaning you start out with a gate layer on the bottom and somehow you -- in the physical device, you physically manipulate it to invert it, the order, is that fair?

A I would say that when you're doing the deposition process, you start with the insulator rather than the sacrificial layer.

Q Okay. And then proceed from there through the steps?

A Yes.

Q Because you now start with the insulating layer at the very bottom and then the sacrificial layer on top of it as

the second layer, when all is said and done, you end up with the gate stack on the top of each step as shown in Dr. Banerjee's modified figures, correct?

A Yes.

Q And is that also true for the Park reference?

A Park has the same sequence as Kim. And so, yes, you would have to swap them to get the same sequence that '711 has.

Q So, again, when you say, "swap," you're talking about when you initially form the staircase structure, you would start with an insulating layer at the bottom instead of the sacrificial layer at the bottom, correct?

A Correct.

Q Okay. Now, I'm going to put another exhibit in the chat.

(Exhibit 1008, U.S. Patent No. 2017/0294384 A1, was remotely introduced and provided electronically to the reporter, as of this date.)

Q Let me know when you get it.

A I have it.
Q Do you recognize this as Exhibit 1008, the Chen reference?
A Yes.
Q Okay. Let's turn to Figure 7A and 7B. It's -- I think it's PDF page 7.
A Yes.
Q What do you understand Figure 7A to illustrate?
A 7A is gate on the bottom, and 7B is gate on the top. However, let's see...
Yes. This one, the 120s are the gate layers and then hashed are the insulators.
Q Okay. So Figure 7A is gate layer on the bottom, and 7B is gate layer on the top of each step, is that correct?
A Yes. That is correct.
Q And the conductive structure -- the vertical conductive structure 300 terminates at the top of the respective conductive gate layer, correct?
A Yes.
Q So the length or height, whichever you prefer, of each vertical

conductive structure is different from its counterpart in these two figures, correct?

A Yes, that's correct.

Q Now, do you see that Figures 7A and 7B illustrate two etch-stop layers, 210 and 220?

A Yes, that appears to be the case.

Whether they are called etch-stop layers or not, I'm not sure, but you're at two layers there. And 220 is most certainly an etch-stop layer.

Q And the terminology that you used before in your description about swapping the layers, meaning with respect to 71A, you would begin constructing the staircase structure by laying down a sacrificial layer first followed by a dielectric layer, whereas you would go the reverse order to construct the device at Figure 7B.

Does that description apply here to the Chen devices?

A Give me a minute.

Yes.

Q Now, I'm going to drop in another reference to the chat.

(Exhibit 1005, U.S. Patent No. US 9,728,547 B1, was remotely introduced and provided electronically to the reporter, as of this date.)

BY MR. HSU:

Q Let me know when you get it.

A All right.

Q Okay. I believe you have Exhibit 1005, the Kim reference, correct?

A Yes.

Q And this is the primary reference Dr. Banerjee relied on for grounds 1 and 2, correct?

A Yes. However, I notice it's afternoon.

THE WITNESS: Would this -- before we get into Kim, would this be a good time to break for lunch?

MR. HSU: Certainly.

(Whereupon, a brief recess was taken from 12:08 p.m. to 12:40 p.m.)

BY MR. HSU:

Q Dr. Campbell, welcome back.

A Thank you.
Q Before we turn to exhibit -- do you recall earlier we had the discussion about selective etching and reverse selective etching, and you described selective etching as etching the layer, which is a top layer that is intended to be etched through at a faster etch rate than the layer immediately underneath, correct?
A Correct.
Q Now, is it -- is that the basic process by which etching is performed, this idea of etching the material that is intended to be etched through at an etch rate faster than the layer underneath?
A I'm trying to envision the negative. I don't come up with any examples.
So yes, almost all the time that's what we're doing.
Q And would you also say it's common where you want additional margin to also etch the layer that is intended to be etched through at a rate faster than, say, for example, not the immediate next layer

1 but the following layer underneath?
2 A This is much less common. The
3 etch-stop is very common.
4 I would like to have you say it
5 again because I'm not sure I really
6 understand what you're asking.
7 Q Sure. Let me rephrase it.
8 Just now, we discussed the
9 idea -- the basic idea of etching, it being
10 selective etching where you're etching
11 through the layer that you intend to etch
12 through at a rate faster than the etch rate
13 of the layer underneath.
14 A Yes.
15 Q And you agree with that?
16 A Yes.
17 Q Okay. Let's say you want to
18 protect also not only the immediately
19 underneath layer but also the layer below
20 that.
21 A So you want to etch the second
22 layer and not disturb the third layer, is
23 that what you mean?
24 Q Well, sorry, then let me set up
25 the scenario a little better.

1 So you have -- let's go from the
2 bottom to the top. You add a first layer,
3 a second layer and a third layer.
4 A Yeah.
5 Q Are you with me so far?
6 A Yes.
7 Q Okay. So we want to etch
8 through the third layer.
9 A Yes.
10 Q And we want to pay particular
11 attention to protecting the first layer.
12 A All right.
13 Q Is it also a good engineering
14 practice to have the etch rates between the
15 first and the third layer be selective,
16 meaning etching have a higher etch rate for
17 the first layer -- for the third layer than
18 the first layer?
19 MR. SMITH: Objection. Form.
20 A I'm trying to envision in what
21 way that would be helpful.
22 The only way that you -- that I
23 can conceive of is if layer two is
24 extremely thin so that ions penetrate not
25 just etch but go all the way through layer

1 two to layer three.
2 Now, that's very, very unusual.
3 You know, common practice would be you just
4 need a selection -- the etch -- can be two
5 over three.
6 You're not going to damage the
7 underlying layer from the first etch. It
8 just doesn't happen.
9 Q Would you characterize -- you
10 mentioned if the second layer is extremely
11 thin, the scenario described as good
12 engineering practice would be, I guess, a
13 good practice.
14 Do you agree so far?
15 A Yeah. I'm talking like a mono
16 layer of atoms or something that's
17 ridiculously thin.
18 It's not clear what role that
19 layer would serve. It's unrealistically
20 thin.
21 Q So would you put the high-K
22 layer around the gate layer within that
23 extremely thin layer or outside that scope?
24 A Those layers are certainly not
25 layers. They are an additional, maybe 2 to

1 10 nanometers. Even 2 is kind of small.
2 Let's say 5 to 10, maybe 15 nanometers.
3 Purpose -- well, so those layers
4 have two reasons for existing. One is that
5 when you do the ALD of the tungsten, you
6 create -- I'm sorry, hydrogen chloride,
7 HL -- HL and silicon dioxide.
8 So the high-K has to be in there
9 before you do the ALD of tungsten,
10 otherwise your insulators will get etched
11 very badly.
12 And the second is the one that
13 we talked about more today, that the high-K
14 in -- that covers the tungsten also helps
15 as an etch barrier, and at, you know, 5 to
16 10 nanometers, it has some effect because
17 it's very hard to etch the hafnium oxide.
18 Q So do I understand you correctly
19 to say -- strike that.
20 Okay. Let's turn to the '711
21 Patent, Exhibit 1001.
22 A One second.
23 Q Sure.
24 A So we're back to 711?
25 Q Yes.

A Okay.
And where?
Q Let's go to column 6, starting from line 27.
A All right.
Q Starting from line 27 through the end of that paragraph, the '711 Patent discloses roughly maybe 10 different types of materials as suitable materials for the sacrificial layer, correct?
A Yes.
Q Okay. Let's go to column 8, starting with line 10.
From line 10 through line 14, the '711 Patent discloses roughly half a dozen or so materials that's suitable for the etch-stop layer, correct?
A Yes.
Q Okay. So if you just take the raw number, roughly 10 different suitable materials for sacrificial layer and 6 for etch-stop layer, we're talking about a combination -- 60 combinations?
A Yes.
Q Okay. Does the '711 Patent

1 disclose the etch-stop layer thickness with
2 respect to any specific combination of
3 materials of the sacrificial layer and the
4 etch-stop layer?
5 A It does state that the -- at
6 least in some of the items, the thickness
7 of the etch-stop layer on the side -- can
8 be the same as many of the tungstens, but
9 they do give a range of thickness for the
10 insulating layer and the etch-stop also
11 they give a range for the thickness.
12 This is column 7, line 57 to 58,
13 I guess.
14 Q So you mentioned a few things in
15 your reply. Let me make sure that I am in
16 sync with what you just explained.
17 You mentioned that the '711
18 Patent discloses the range of thickness for
19 the etch-stop layer, and that is in
20 column 7 starting roughly from line 57 is
21 what you said, correct?
22 A Yes. I think it's actually 58,
23 but yes.
24 Q Okay. And then you mentioned
25 the thickness of the etch-stop layer on the

1 side.
2 What does that refer to --
3 A -- on the side of the step.
4 Q But where do you get that
5 disclosure? Can you point me to --
6 A Oh, I'm sorry. Yes, certainly.
7 One second.
8 I'll have to pick that one up
9 again, but there's also an embodiment on 6,
10 line 38, identifying the range for the
11 thickness of the sacrificial layer in the
12 first insulating layer.
13 Q Okay. And in your previous
14 answer before I started asking follow-up
15 questions, you also referred to a range of
16 thickness for the insulating layer.
17 Is the disclosure in column 6 at
18 line 38 through 40 what you had in mind?
19 A Yes, that is one.
20 Q Are there others?
21 A Number -- in column 8, line --
22 well, the first ten lines or so, just
23 before you get to the labeling of all the
24 various materials that could be used.
25 Q I see. Where it talks about the

1 thickness on the side can be the same as on
2 the top.
3 A Exactly. And, you know, the
4 other one was -- in case I didn't answer
5 that right -- column 7, line 57, the range
6 of the thicknesses.
7 Q And that's the range of
8 thickness for the etch-stop layer 310?
9 A Yes.
10 Q Okay. But none of these
11 thicknesses or thickness ranges are
12 specific to a combination of materials for
13 the sacrificial layer and the etch-stop
14 layer, correct?
15 A They're not narrowed, so I don't
16 know how else to say it. But the materials
17 that are listed would be -- would fall
18 within those ranges.
19 And so when you're on the higher
20 end of the range, and some would be on the
21 lower end of the range, but those materials
22 would fit within that range.
23 Q And a POSITA reading the '711
24 Patent, supposed the POSITA picks out a
25 particular combination of materials for the

1 sacrificial layer and the etch-stop layer,
2 the POSITA would know what's the
3 appropriate thickness or thickness range
4 for that particular combination of
5 materials, is that correct?
6 A No, not completely, no.
7 The range that's given there is
8 a place to start doing experiments to
9 determine the actual thickness that you
10 would need.
11 Oxide, to give an example, in
12 machine number 1 may etch slightly
13 different than machine number 2, and the
14 same thing for the etch tools. And so you
15 have to measure on your etch systems with
16 your etch recipe and your film deposited in
17 order to actually get an exact value.
18 And no, they didn't go through
19 the -- it was 60 various permutations
20 because even if you did go through 60
21 permutations, you would have to verify them
22 on your machines.
23 Q So given the disclosure of the
24 '711 Patent, a POSITA can be instructed to
25 use a particular combination of materials,

1 but then the POSITA would still have to
2 experiment to make that combination work.
3 Is that a fair characterization?
4 A Not only is it a fair
5 characterization, a POSITA would certainly
6 know that's what you have to do.
7 This is not unique to this
8 process. It's every time you do any
9 deposition and etching, you have to do
10 this.
11 Q Now, let's go back to the Chen
12 reference. It was Exhibit 1008.
13 A All right.
14 Q Do you recall we had discussed
15 Figures 7A and 7B?
16 A I remember.
17 Q And you recall that 7A is
18 dielectric on top and 7B is gate conductor
19 on top, right?
20 A Yes.
21 Q And then both of these
22 embodiments have two etch-stop layers,
23 right?
24 A Yes, that appears to be the
25 case. Certainly, one etch-stop layer and a

1 layer under it. I don't know what that
2 layer is.
3 Q Well, that's -- let's take a
4 quick look.
5 So Chen calls -- and this is in
6 paragraph 45, for example. 210 is the
7 first stop layer and 220 is the second stop
8 layer.
9 Let me see if you agree with
10 that, paragraph 48 --
11 A Just getting there.
12 Q -- and 40 -- sorry,
13 paragraphs 45, 46, a description of
14 Figure 7A and 7B.
15 A Okay.
16 Well, it's listed as a stop
17 layer, not an etch-stop layer. And it is a
18 dielectric.
19 That doesn't really help a lot.
20 Q Well, I can direct your
21 attention to paragraph 37.
22 A All right. In 37, they take the
23 two layers together and jointly call them
24 an etch-stop layer and consist of those two
25 stop layers.

1 Q So would it be fair to say 210
2 and 220 are two etch-stop layers?
3 A The two together form an
4 etch-stop layer, and they are both stop
5 layers. That's what it says.
6 Q Okay. And so back to the figure
7 illustration, the two etch-stop layer
8 configuration is compatible with a gate
9 stack or a gate layer -- strike that.
10 Back to Figure 7A, the two
11 etch-stop layer configuration is compatible
12 with dielectric on top configuration,
13 correct?
14 A 7A suggests that it is.
15 Q And whereas 7B would suggest
16 that the two etch-stop layer configuration
17 is compatible with a gate layer on top
18 embodiment, correct?
19 A Well, this comes back to what we
20 talked about earlier this morning, that
21 somehow you can change some diagrams on a
22 PowerPoint and it's going to work in the
23 actual fab.
24 This is a very difficult
25 process, this via etching. And the idea

that you can just swap them and it's going to work, my experience is that good luck with that. It may be made to work eventually, but I will guarantee that there will be a lot of heartache and it's a difficult process development to make that change from 7A to 7B.

Q And does Chen provide additional details in helping a POSITA to implement these two embodiments?

A Generally speaking, yes, but generally speaking is a long way from reality.

Q And when you say, "generally speaking," what are you referring to?

Can you point me to specific disclosures in Chen that assist a POSITA in implementing these two different embodiments as depicted in Figure 7A and 7B?

A In the text that you had recently directed me toward, it identified some of the materials that might be used for these layers. So that's a guiding line. Yes.

1 Q But you would say, even with
2 such guidance, a POSITA still has to do a
3 lot of experiments to make a working
4 device, is that fair?
5 A It's certainly fair.
6 If you are starting from ground
7 zero and you're making 7A, it's a
8 tremendous amount of work, just insane
9 amount of work, and a great deal of money.
10 To get from 7A to 7B is not as
11 intensive as that, but it's still a lot of
12 work to get from A to B.
13 I don't want to leave you with
14 the impression that it's just a matter of
15 changing the sequence and all will be well.
16 That's never going to happen.
17 Q Okay. Now, let's turn to Kim,
18 which we brought up right before lunchtime,
19 and that's Exhibit 1005.
20 A Go ahead.
21 Q Okay. Let's take a look at
22 Figure 22A.
23 Let me know when you get there.
24 A I am there.
25 Q Okay. Right above the substrate

is a lower gate insulating layer 11 in the CAR and WCTR regions, correct?

A Again, could you give me that one more time?

Q Sure.

In the CAR and WCTR regions, right above the substrate, there is a lower gate insulating layer 11, correct?

A Yes, there's a thin insulating layer there, yes.

Q Is that layer a necessary layer or an optional layer?

A Well, the gate has to be isolated electrically from the substrate.

Now, we do have the hafnium oxide liner, and that could serve as the isolation between the gate and the substrate.

Now, it kind of depends -- the answer depends on how thick that high-K is. I have an idea of what it would probably be like, but I don't have an exact number.

So my answer is that I don't know if that hafnium oxide is -- and another oxide, 11, has to be there. And if

1 the -- and if the oxide is thicker, then
2 you might be able to live without it.
3 Q So I want to make sure I'm in
4 sync with you.
5 By having hafnium oxide layer,
6 you're referring to the high-K layer that
7 surrounds the gate conductor layer,
8 correct?
9 A Correct.
10 Q And so do I understand you
11 correctly to say, depending on the
12 thickness of the high-K layer, lower gate
13 insulating layer 11 may or may not be
14 necessary?
15 A Correct.
16 Q Okay. I am going to -- let's
17 see here...
18 I am going to introduce -- or
19 not introduce, but put into chat another
20 reference or exhibit.
21 A Before we leave 22A, can we --
22 can I point something out on it?
23 Am I allowed?
24 Q Well, are you correcting your
25 previous answer or something to that

1 effect?
2 A Good question.
3 No, it's a new topic.
4 Q Okay. Well, I prefer that we
5 stick with the questions I'm asking.
6 A Okay.
7 Q Okay. So I've put into the chat
8 Exhibit 1006. That's the Park reference.
9 (Exhibit 1006, Published Patent
10 No. 10-2015-0051841, was remotely
11 introduced and provided electronically
12 to the reporter, as of this date.)
13 BY MR. HSU:
14 Q Let me know when you have it
15 open.
16 A Yes, I have it open.
17 Q Okay. So do you recall that
18 Dr. Banerjee relied on the Figure 5 and 9
19 embodiments -- embodiment, singular, and he
20 also modify the Figure 9 diagrams to show a
21 gate stack on top configuration, correct?
22 A Figure 9G, 9H...
23 So I am seeing a gate on the
24 bottom of the stack.
25 Q Right. And that's shown in --

1 sorry, go ahead.
2 A No, go ahead.
3 Q Right, as shown in Park.
4 A In Park, yes. Yes.
5 Q Okay. Now, let's look at
6 Figure 9I. This is on top of page 30,
7 printed page number.
8 A Yes.
9 Q Okay. The sacrificial layer is
10 gone by this point, correct?
11 A Sacrificial layer is gone...
12 Let me look for a moment.
13 You have 110B and 110A, and
14 those are the areas that you're going to
15 remove to put the stop in.
16 I have to take a quick look.
17 Hold on a second.
18 Q And let me clarify. I wasn't
19 precise enough.
20 A All right.
21 Q By "sacrificial layer," I was
22 referring to the sacrificial layer in the
23 staircase.
24 A In the staircase, what do you
25 mean by "in the staircase"?

Q The staircase is constructed in the beginning by forming alternative -- alternating layers of dielectric and sacrificial layers, correct?

A Okay. Yes.

Q And that's what I was referring to by "sacrificial layer."

A But Park is different. Park has sacrificial layers in either side of the dielectric AD2, and those things have to be removed and then filled later, in my reading of Park.

Q Okay. Now, if we go back to starting from Figure 9, that's a -- let's start with 9B.

A 9B.

Q On top of page --

A Yes.

Q -- 27. Unfortunately, the caption and the figure got separated on two separate pages.

A Yes.

Q Okay. Would you agree that the layer AD is formed by some sort of deposition technique?

A Yes.
Q And then moving on to Figure 9C, the layers 115A, AD2, and 115B are also formed successively using some deposition technique as well.
A Yes, that's true. And it doesn't cover the side of 171. But yes, so far so good.
Q Okay. And can -- and what sort of deposition techniques are appropriate to form these layers that we were just going over between AD, 115A, AD2, and 115B?
A Generally, it's chemical deposition, sputtering or atomic layer deposition.
Q And so, for example, at least using ALD, as we previously discussed, these layers can have -- can be conformal layers, uniform thickness, correct?
A Yes, as long as there's an ALD chemistry. Not every material is suitable for ALD.
Q Understood.
Now, turning to paragraph 49 in Park.

A Okay.
Q Let me know when you get there.
A I'm there.
Q Would you say this paragraph 49 describes the differences between the Figure 4 embodiment and Figure 5 embodiment?
A All right. So it would appear -- go ahead.
Q I'm sorry.
A It would appear the major difference between that I -- it's obvious to me is the etch-stop structure.
Q And specific --
A Yeah --
Q And specifically, Figure 5 shows two etch-stop layers while Figure 4 only show one etch-stop layer, correct?
A To be more exact, it shows two etch-stop layers and a dielectric, whereas the other one shows just a single etch-stop layer -- in the core.
Q And by "dielectric," you're referring to AD2 --
A Correct.

Q -- in between -- okay.
And those layers are formed on top of the staircase, correct?
A Yes. On the top and on the side, except for 171 -- or, I'm sorry, the GST.
Q Okay. Now, going back to Figure 9I.
As we discussed earlier, the staircase structure starts with two alternating sacrificial layers and dielectric layers, correct?
A Yes.
Q And, for example, in Figure 9A, the numeral 140 denotes the sacrificial layers, correct?
And this is in paragraph --
A Figure 9A?
Q Yeah, Figure 9A.
A I'm sorry, my Figure 9A just shows the stack of the sacrificial layers and the insulators.
Q That's right.
And the sacrificial layers are designated by the numeral 140 --

A Yes.
Q -- including the layers 141 through 146, correct?
A Correct.
Q Okay. And would you agree that by step 9I, the sacrificial layers 140 have been replaced and is no longer present in the structure?
A From the figures and sequence of 9 -- Figures 9A through G, or whatever it goes to, I can't tell.
There is no -- if it had gone through a tungsten gate, you would see the high-K gate. I don't see that.
So I can't tell from just the figures.
Q Okay. Let's then go to paragraph 104.
A All right.
Q And paragraph 104 discusses Figure 9E, correct?
A Yes.
Q And part of the description is that the plurality of sacrificial layers 140 can be removed to provide side openings

as shown in Figure 9F, correct?
A Yes.
Q Okay. And then in the next paragraph, 105, it describes replacing or filling what's now cavities left by -- after removing a sacrificial layer 140 with additional layers, and eventually forming a conductive gate stack, correct?
A That's what it says. I'm surprised that it did not put the high-K in prior to putting in the tungsten, but that's what it says.
Q And so would you agree now, by the time the process reaches what's illustrated in Figure 9I, the sacrificial layer 140 is no longer present in the device?
A Yes.
Q Okay. Let's turn back to your declaration.
A All right.
Q So let's go to paragraph 44 on page 29, and it's PDF page 30.
A All right.
Q Here, you opine regarding

1 claims 14 and 15, correct?
2 A Yes.
3 Q And that runs from paragraph 44
4 through 47, right?
5 A Yes.
6 Q And is it correct to understand
7 your opinion to be based on interpretation
8 that on the surface of something means
9 directly on that surface?
10 A Interpretation is that on can be
11 above the surface in another layer, but on
12 the surface or on the side means that it's
13 directly in contact with the top or the
14 side of that layer.
15 Q Do you mean on the side surface
16 or just simply on the side?
17 A Certainly on the side surface
18 would be direct contact, and I think we
19 would use on the side as well as direct
20 contact.
21 I could be wrong, but I think
22 that's what it is.
23 Q And this interpretation is based
24 on embodiments of the '711 Patent, correct?
25 A Yes.

1 Q Did you rely on anything other
2 than the embodiments of the '711 Patent to
3 arrive at this opinion?
4 A It came directly from the '711.
5 Q Okay. And is that also true of
6 your opinion with regard to claims 14 and
7 15 with respect to Park?
8 And here, let's turn to
9 paragraph 66 through 70 on page -- starting
10 on page 43.
11 A I am at 66, and can you repeat
12 the question, please?
13 Q Is -- so -- strike that.
14 Here, it is also your opinion
15 that Park does not render obvious claims 14
16 or 15 because Park does not disclose the
17 etch-stop layer is formed on a side surface
18 and a top surface of each step, correct?
19 A That's what it says, yes.
20 Q And that opinion -- is that
21 opinion, again, based on the interpretation
22 "on a top surface" or "on a side surface"
23 means that the etch-stop layer must be in
24 direct contact with one of those surfaces?
25 A I would say not one of the

1 surfaces, both of them.
2 Q Fair. I was thinking that as
3 well. I wasn't precise enough.
4 So just let me re-ask it. All
5 right.
6 Your opinion that Park doesn't
7 render obvious claims 14 or 15 is based on
8 interpretation that the etch-stop layer is
9 formed on a side surface and a top surface
10 of each step requires that the etch-stop
11 surface be in direct contact with the side
12 surface and the top surface of each step,
13 is that correct?
14 A Correct.
15 Q Okay. And, again, is it correct
16 that that interpretation is based on the
17 embodiments of the '711 Patent?
18 A That's correct.
19 Q And nothing else?
20 A I take it from the '711. I'm
21 not sure if there are other sources for
22 that, but it was on the '711, so I've taken
23 it there.
24 MR. HSU: Let's take a
25 five-minute break. I think I'm

1 basically done, but I just want to
2 make sure that I didn't miss anything,
3 but --
4 THE WITNESS: Okay.
5 MR. HSU: -- so a five-minute
6 break, if that works for you.
7 THE WITNESS: Sure.
8 MR. HSU: All right. Off the
9 record.
10 (Whereupon, a brief recess was
11 taken from 1:35 p.m. to 1:50 p.m.)
12 BY MR. HSU:
13 Q Okay, Dr. Campbell, I just have
14 a couple more questions, I think.
15 So recall we looked at
16 paragraph 49 of Park, and you described the
17 difference between the Figure 4 and
18 Figure 5 embodiment as Figure 5 has
19 additional etch-stop layer and with it, the
20 AD2 layer that's in between the two
21 etch-stop layer, correct?
22 A Correct.
23 Q What do you understand
24 Dr. Banerjee to be combining from the
25 Figure 4 embodiments with the Figure 5

1 embodiment?
2 A I'm not sure I can answer that
3 question without looking back at Banerjee's
4 declaration.
5 Q Okay. Or do you want to look at
6 your own declaration, or would you like me
7 to put his declaration into the chat?
8 I would be happy to go either
9 way.
10 A Well, I'll look at our
11 declaration.
12 Q Okay.
13 A If you want to just hang on a
14 second.
15 Q And like I said, I'd be happy to
16 put Dr. Banerjee's declaration into the
17 chat, if you'd like. So just let me know.
18 A All right. So in the
19 declaration, we describe that -- you know,
20 given that that's described as our view
21 with the requirement to have the structures
22 on the top of the device. And so the CMP
23 process is done for that.
24 And the concern that was raised
25 in the declaration is that the etch-stop

1 layers could not be completed because the
2 polishing would remove the top layer.
3 Looking at Figure 9F on page 54,
4 the CMP would be damaging the upper
5 layer -- the upper T2 layer prior to the
6 high-K being filled -- sorry, the etch-stop
7 being filled.
8 Q So thank you for that, but I'm
9 not sure that was the question -- that was
10 the answer to the question I asked. So let
11 me try again.
12 A Apology.
13 Q No worries.
14 So the question was, what do you
15 understand Dr. Banerjee to combine from the
16 Figure 4 embodiment into the Figure 5
17 embodiment?
18 A Well, I'm assuming it is this
19 etch-stop structure that has the multiple
20 etch-stop layers. That was really the only
21 significant difference between the two.
22 Q But that exists already in the
23 Figure 5 embodiment, correct?
24 A Right. Okay.
25 So let me go back.

I'm sorry, I can't answer it off the top of my head. My apologies.

Q Okay. Now, recall earlier, we walked through the figures of the '711 Patent, correct?

A Yes.

Q And there was that barrier layer 208 underneath the etch-stop layer 310, correct?

A Yes.

Q And also recall that we had discussed that barrier layer 208 is optional within the disclosure of the '711 Patent, correct?

A Yes.

Q Now, the '711 Patent doesn't disclose a different processing flow for the embodiment where the barrier layer is not included in the structure, correct?

A Yes.

Q Meaning, is it your understanding that the POSITA reading the '711 disclosure would understand to omit the barrier layer, one would still follow the same processing flow but simply omit

1 the step to deposit the barrier layer and
2 then, obviously, when you etch, there's no
3 longer a barrier layer in the etching
4 process, is that fair?
5 A Yes, I believe that's true.
6 MR. HSU: I have no further
7 questions on cross.
8 MR. SMITH: I'll have a few
9 questions.
10 EXAMINATION BY
11 MR. SMITH:
12 Q Dr. Campbell, do you remember
13 being asked previously some questions about
14 your area of expertise and experience?
15 A Yes, certainly.
16 Q Do you recall testifying that
17 you're an expert in fabrication of
18 semiconductor devices and semiconductor
19 materials?
20 A Yes.
21 Q Is etching processes a part of
22 semiconductor fabrication?
23 A Yes.
24 Q Do you recall you were also
25 asked several very specific questions about

1 semiconductor processing and semiconductor
2 design?
3 A Are we talking about today or --
4 Q Yes.
5 A Yes, I was asked about both.
6 Q How are things like the number
7 of layers in a structure or the height of a
8 structure or aspect ratio related to
9 semiconductor fabrication?
10 A So this is a negotiation between
11 designers who want more capability and the
12 processing people who know what can be
13 done, or hopefully know what can be done.
14 So it's a negotiation.
15 Q Does the design of a
16 semiconductor device impact the fabrication
17 of that device?
18 A Immensely.
19 Q As an expert in semiconductor
20 design fabrication, do you have to have an
21 understanding of how the design of the
22 device impacts the fabrication of a device?
23 A Yes. As I understand, the
24 fabricators have to learn to speak each
25 other's language at least.

1 So yes, you have to learn.
2 You're not an expert in it, but you have to
3 understand what they're asking for.
4 Q Could you turn to paragraph 41
5 of your declaration?
6 A Sure.
7 Q And would you mind just taking a
8 moment and reviewing paragraph 41?
9 And you can let me know when
10 you're finished.
11 A All right.
12 Q I'd like to direct you to, on
13 page 26, and about five lines down to the
14 top, it begins, "For example, etch
15 processes." Do you see that?
16 A This is in paragraph 40?
17 Q 41.
18 A 41.
19 Okay.
20 Q Could you review paragraph 41 --
21 or 40, just to be clear?
22 A I'm in the process of reading
23 41.
24 Q Okay. Go ahead and review 41,
25 please.

1 A All right.
2 All right. I'm done.
3 Q All right. Now, on page 26,
4 about five lines down, it starts, "For
5 example."
6 Can you read that sentence?
7 A "For example, etch processes
8 depend on multiple parameters that are
9 optimized to achieve desired etch
10 characteristics for a specific design."
11 Q And then could you read the next
12 sentence as well?
13 A "When the design changes, these
14 parameters must be reoptimized."
15 Q And then jumping down another
16 five lines or so, it starts, "Changes in
17 design."
18 Can you read that sentence and
19 the one after it?
20 Or I can read it if that's
21 easier, too, if you're following along.
22 A I'm trying to find "Changes in
23 design."
24 Okay.
25 Q Did you find it?

It's on that same page.
A All right. Is it down lower?
Q It's about five lines below.
On the right side of the page.
A Why don't you go ahead and read it. I'm not -- oh, "Changes in design"?
Q Yes. Do you see that?
A Yes. "Changes in design" --
Q Go ahead.
A -- "can also affect the number and sequence of steps in the etching process. Further, etch processes are highly dependent on the material used, the depth and aspect ratio of the desired etch, the material to be deposited on the sidewalls, the material on which the etch is stopped, the material used as the mask which can be simply photoresist or a hard mask using other materials such as carbon, and the order of the layers."
Q And how do these excerpts we read relate to your area of expertise?
A These align very well with the areas that I am an expert in.
Q All right. And does the design

1 of the semiconductor device, as you've
2 mentioned here, impact the manufacturing
3 and processing of the device?
4 A Absolutely.
5 Q Does the design of the device
6 affect the etch processes used for the
7 device?
8 A Again, absolutely.
9 Q Okay. Do you consider yourself
10 qualified to offer an opinion on the
11 semiconductor design aspects that you've
12 discussed in your declaration?
13 A The design aspects, no.
14 As I said before, I talked to
15 designers, but I'm not a designer. I'm a
16 processing person.
17 Q As you've discussed design
18 aspects in your declaration that impact
19 etch processes, like the ones we've just
20 read, do you consider yourself qualified to
21 offer an opinion on those types of design
22 aspects that relate to etch processes?
23 A Absolutely. I mean, that's the
24 point to the process people seen -- telling
25 the designers you can't do this -- we can't

1 do this.
2 And yes, I am expert enough to
3 do that.
4 Q Okay. Thank you. Okay.
5 All right. Let's turn to
6 paragraph 35 of your declaration.
7 A All right.
8 I've read it.
9 Q Okay. One moment, please.
10 A Oh, sorry.
11 Q Can I ask you one more question
12 just in the line that we were just
13 discussing?
14 A Of course.
15 You want me to go back to that?
16 Q No, actually, we'll carry on.
17 A Okay.
18 Q So paragraph 35 in your
19 declaration.
20 A Yes.
21 Q Do you recall being asked
22 questions about paragraph 35 here and
23 Figure 22A?
24 You can review those, if you'd
25 like.

A Yes.
Q Do you want to take just a moment to read paragraph 35 briefly?
A I've read it. It isn't very long.
Q How would you describe the ordering in this Figure 22A -- sorry, strike that.
In Figure 22A here, how would you describe the order of the dielectric and gate stack layers of the step?
A This is a gate-on-the-bottom device.
Q And this Figure 22A comes from --
A I'm sorry, I can't look at this figure in that sequence, so...
Q Can you -- strike that.
Where does this Figure 22A come from?
A Kim.
Q Okay. Is this Figure 22A the basis for your opinion that Kim discloses a gate-stack-on-bottom device?
A Yes. This whole sequence from

1 17A to 22A, clearly it's a gate on the
2 bottom.
3 Q Could you please open the Kim
4 reference, Exhibit 1005?
5 And I'd like to direct you to
6 paragraph 185.
7 A Okay. I'm there.
8 Q And can you please review -- or
9 actually, I will -- can you look towards
10 the bottom of paragraph 185. It says --
11 where it says, "The etch-stop layer 125 may
12 cover"?
13 A Yes, "The etch-stop layer 125
14 may cover top surfaces of the contact pads
15 123 in the cell array region CAR and end
16 portions of the sacrificial layers SC1 to
17 SC8 in the word line contact region WCTR."
18 Q And then if we could jump down
19 to 187. It's at the top of the next page.
20 A Yes.
21 Q And partway down, it says, "In
22 some embodiments, the first stop layer."
23 Do you see that?
24 A Yes.
25 Q Can you go ahead and read that?

A Sure.

"In some embodiments, the first stop layer 125a may be formed of silicon" --

Q Sorry.

A Further down?

Q I think it's the one above that, the sentence above that, where it says, "In some embodiments, the first stop layer 125a may cover sidewalls."

A Yes.

Q Can you go ahead and read that sentence?

A "In some embodiments, the first stop layer 125a may cover sidewalls of the sacrificial layers SC1 to SC8 in the contact region WCTR, and the second stop layer 125b may be conformally formed on the first stop layer 125a."

Q Okay. Thank you.

How do these portions we've just read relate to your opinion about Figure 22 being a gate-stack-on-bottom structure?

A Figure 22 does not confirm to these. The sacrificial -- sorry, the

1 etch-stop layers are not conformally over
2 the surface of the stack. There's stuff
3 between the two.
4 The stop has the top and 185 has
5 the side, and it's supposed to be in
6 contact.
7 Q All right. Could you please
8 look at Figure 22A again?
9 A All right.
10 Q And --
11 A Yes.
12 Q Do you mind if I share my screen
13 to indicate -- or to show the portion of
14 your declaration I'm looking at?
15 A Yes, certainly.
16 Q Okay. And this is just your --
17 a marked copy of your declaration,
18 Exhibit 2009.
19 All right. Can you see this
20 imagine here?
21 A Yes.
22 Q Okay. And I will...
23 All right. Looking back at Kim,
24 can you see the Kim reference on your
25 screen?

A I can.
Q And we just read -- let's go down here to 187.
A Yes.
Q And I'd like to direct your attention first off to paragraph 183, where it says, "Figures 17A through 22A and Figures 17 through 22B are section views illustrating methods of fabricating a three-dimensional semiconductor memory device according to other example embodiments of the inventive concepts."
Do you see that?
A Yes.
Q And then do you see at the top of paragraph 185, it says, "According to other example embodiments, as shown in Figures 17A and 17B," and then it continues on to describe the paragraphs we just read?
A Yes.
Q Having reviewed paragraph 183 and 185, is there anything you'd like to clarify about your opinion that these paragraphs do not apply to Figure 17 through 22A?

1 A I'm sorry, I'm having trouble
2 answering. I mean, this is clearly
3 Figures 17A through 22A can be -- it said
4 it right there, 183.
5 Q Okay. So it is your opinion
6 that paragraphs 185 and 187 that we
7 discussed apply to Figures 17A through 22B?
8 A Absolutely.
9 MR. HSU: Objection.
10 Mischaracterizes prior testimony.
11 BY MR. SMITH:
12 Q Can you please restate your
13 opinion, Dr. Campbell, as to whether
14 paragraphs 185 and 187 apply to Figure 17A
15 through 22B?
16 MR. HSU: And objection.
17 Leading.
18 A I'm sorry, paragraph 185
19 explicitly says, examples such as shown in
20 Figures 17A and B, and 17A and 17B are the
21 beginnings of the sequence of figures
22 ending in 22A and 22B.
23 Obviously, this is part of that
24 sequence.
25 Q Okay. Thank you.

And so directing your attention back to the portions that we read previously in 185 where it says, "The etch-stop layer 125 may cover top surfaces of the contact pads."

Do you see that portion again?

A Yes, yes.

Q "The etch-stop layer 125 may cover top surfaces of the contact pads 123 in the cell array region, and end portions of the sacrificial layers SC1 to SC8 in the word line contact region WCTR."

A Yes.

Q And jumping down again to 187, where we read here, you read, "In some embodiments, the first stop layer 125a may cover sidewalls of the sacrificial layers SC1 to SC8 in the contact region WCTR, and the second stop layer 125b may be conformally formed on the first stop layer 125a."

Do you see that?

A Yes.

Q And I'm going to pull up Figure 17A that these are referring to.

1 Do you see SC1 through SC8 on
2 the left being indicated?
3 A Yes, I do.
4 Q Where would the sidewalls
5 discussed in paragraph 187 be found in --
6 the sidewalls of the sacrificial layers be
7 found in this figure?
8 A Sacrificial layers are the
9 dotted rectangles and the side would be
10 where it terminates horizontally.
11 So it's at the end of each step.
12 Q Okay. So as we read in
13 paragraph 187, the etch-stop layer 125a
14 covers the sidewalls of the sacrificial
15 layers.
16 Is that what you were describing
17 just now?
18 A Yes, yes.
19 Q Okay. And then I'd just like to
20 ask a question that I asked previously.
21 How do paragraphs 185 and 187
22 that we've discussed relate to your opinion
23 about whether Kim discloses a
24 gate-stack-on-bottom structure?
25 MR. HSU: Objection. Asked and

1 answered.
2 A I'm sorry, could you repeat that
3 again?
4 If you could enlarge the figure
5 a bit. It's very difficult to read.
6 Q Yes, sorry.
7 A Much better. Thank you.
8 Q Yes.
9 In fact, let me go back to
10 Figure 17A that we were looking at.
11 And one moment, please.
12 My question was, how do
13 paragraphs 185 and 187 -- or strike that.
14 How do the portions we just read
15 of paragraphs 185 and 187 relate to your
16 testimony that Kim discloses a
17 gate-stack-on-bottom structure?
18 MR. HSU: Objection. Asked and
19 answered.
20 A What we read was that the
21 etch-stop barrier should be in contact with
22 the sacrificial layer on the top and on the
23 sides, and clearly, it's not in contact
24 with the sacrificial layers on top.
25 So it does not -- this figure --

1 this device does not conform to what it
2 says in the text.
3 Q Okay.
4 All right. We discussed -- I
5 guess I can stop sharing my screen now.
6 Do you recall being asked
7 questions about the Chen reference,
8 Exhibit 1008?
9 A Yes.
10 Q And specifically you were asked
11 questions about Figure 7A and 7B of the
12 Chen reference?
13 A Yes.
14 Q I'm going to put your
15 declaration up again.
16 Can you see your declaration
17 again?
18 A Yes, I can.
19 Q Do you see where it says,
20 "Ground I"?
21 A Yes.
22 Q Which references are at issue in
23 Ground I?
24 A Well, it's mainly Kim.
25 Q Do you see Ground II --

A Yes.
Q -- below?
A Yes.
Q Which references are at issue in Ground II?
A Kim and Fang.
Q Do you see Ground III?
A Yes.
Q Which references are at issue in Ground III?
A Park.
Q And do you see Ground IV?
A Yes.
Q Which references are issue in Ground IV?
A Park and Fang.
Q Do you see Chen listed as a reference in any of these grounds?
A No.
Q You were also asked some questions about your interpretation of the phrase "on the surface" in the '711 Patent.
Do you remember that?
A Yes.
Q How would an expert in

1 semiconductor fabrication understand the
2 term "on the surface"?
3 A It means there has to be contact
4 between one layer and the other. Not to
5 say they're completely connected, but
6 nothing in between.
7 Q Does your experience as an
8 expert in semiconductor fabrication inform
9 how that term is understood?
10 A Yes.
11 Q One moment, please.
12 Okay. Just a few more
13 questions.
14 I'd like to share my screen
15 again, and I'll put up the Kim reference.
16 And just like to clarify, I just
17 want to make sure I understand your opinion
18 that we discussed previously.
19 I'd like to direct your
20 attention to paragraph 185. And it begins,
21 "According to other example embodiments, as
22 shown in Figures 17A and 17B," and then it
23 goes on to make descriptions.
24 Do you see that?
25 A Yes.

1 Q And we read some of those
2 descriptions?
3 A Yes.
4 Q Is it your opinion that
5 paragraph 185 and 187 is describing
6 Figure 17A and 17B of Kim?
7 A Yes.
8 MR. HSU: Counsel, I'm going to
9 object to this line of questions on --
10 regarding paragraphs 185, 187. I
11 never asked about those paragraphs.
12 It's the whole line of
13 questioning.
14 MR. SMITH: Okay. I'm just
15 trying to understand his basis of the
16 opinion.
17 And I don't have any other
18 questions.
19 MR. HSU: Dr. Campbell, just a
20 few questions to follow up.
21 EXAMINATION (CONTINUED)
22 BY MR. HSU:
23 Q Now, you consider yourself an
24 expert in the area of semiconductor
25 fabrication, correct?

A Yes.
Q But not an expert in the area of semiconductor design, correct?
A Correct.
Q Would you consider yourself a POSITA in the area of semiconductor design?
A Well, I have the education roles and I have two to three years experience in design. Maybe. After 40 years, I might, but it would be a bit of a stretch.
Q Is it your opinion that a POSITA in the area of semiconductor designs can practice what is taught by the '711 Patent?
A Can do what? I'm sorry.
Q Can make a device based on the teaching of the '711 Patent.
A The --
Q So let me -- let me -- strike that. Let me make a clean question.
Is it your opinion that a POSITA in the area of semiconductor design can practice what is taught by the '711 Patent?
A By "practice," you mean to actually build devices?
Q Correct.

1 A As I mentioned before, this is a
2 very, very intensive operation. There's no
3 one single person that could possibly do
4 it.
5 Is that your question, that
6 there's one person that could do it?
7 Q Fair enough.
8 I mean, of course we understand
9 modern technology almost always involve a
10 team of engineers, right?
11 I'm not --
12 A A team --
13 Q That's not where I'm focusing
14 on, but let me put it this way: Is it your
15 opinion that a POSITA in the area of
16 semiconductor designs can build a device
17 using the disclosure of the '711 Patent
18 assuming there's no limit on time and
19 resources?
20 A The '711 Patent is primarily a
21 process in -- a process description.
22 The design, if you will, where
23 the transistors go and so forth is really
24 modest by comparison. I don't know if the
25 processing people are saying which layers

1 go where and how thick they are and how
2 you're going to etch things. Those are all
3 process parameters.
4 So a POSITA in design, probably
5 not because he's not in the right area.
6 MR. HSU: I have no further
7 questions.
8 MR. SMITH: Okay. I just have
9 two brief follow-up questions,
10 Dr. Campbell.
11 THE WITNESS: Sure.
12 EXAMINATION (CONTINUED)
13 BY MR. SMITH:
14 Q And I'm going to put up your
15 declaration.
16 Can you see your declaration
17 here?
18 A Not yet.
19 Q I'm sorry --
20 A Not yet.
21 Q Can --
22 A No.
23 Q Oh, sorry. Can you see it on
24 the screen?
25 A It's coming up now.

Q Okay. Thank you.
A There it is.
Q Could you review paragraphs 21 and 22, and then let me know when you've read those?
A Yes.
Q Is there anything you'd like to clarify about your qualifications as it relates to this definition of a POSITA?
A The issue that I see here is that they're lumping -- no, strike that.
Q I can rephrase the question, if you'd like.
A Please do.
Q Let me direct you to paragraph 22 and the second line down.
Can you read this --
A Yes.
Q -- portion?
A Certainly.
"In view of my educational background and work experience, I surpass Dr. Banerjee's definition of a POSITA, and did so before August 31, 2017."
Q Is there any doubt in your mind

1 that you satisfy this definition of a
2 POSITA as described here?
3 A Yes, obviously. Yeah.
4 Q Is it -- is this -- is this
5 statement accurate that you've described
6 here? Is this still your testimony?
7 A Absolutely.
8 Q The portion we just read here,
9 the highlighted portion?
10 A Yes. In view of my educational
11 background and work experience, I surpass
12 Dr. Banerjee's definition of a POSITA, and
13 did so between August -- or before
14 August 31, 2017.
15 Q Okay. So that statement is
16 correct.
17 A It is correct.
18 MR. SMITH: Okay. Thank you.
19 No further questions.
20 MR. HSU: No further questions.
21 THE COURT REPORTER: Would the
22 witness like to read and sign?
23 MR. SMITH: Yeah, we'd like to
24 review that for errata.
25 THE COURT REPORTER: Okay. I am

1 preparing the final transcript for
2 Friday. Would you also like it on
3 Friday, Ben?
4 MR. SMITH: Yes.
5 (Continued on next page to
6 include signature and jurat.)
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THE COURT REPORTER: And would you also like the rough that's going out today?

MR. SMITH: Yeah. That'd be great.

(Time Noted: 2:38 p.m.)

* * *

_____

STEPHEN CAMPBELL

Subscribed and sworn to
before me this day
of , 20__

_____
NOTARY PUBLIC

---------- I N D E X ----------


| WITNESS | EXAMINATION BY | PAGE |
|---|---|---|
| STEPHEN CAMPBELL | | |
| | MR. HSU | 4, 148 |
| | MR. SMITH | 129, 151 |


------ EXHIBITS FOR IDENTIFICATION ------


| | | |
|---|---|---|
| EXHIBIT 2009 | Declaration of Stephen Campbell in Support of Patent Owner's Response | 9 |
| EXHIBIT 1001 | U.S. Patent No. 10,672,711 B2 | 42 |
| EXHIBIT 1008 | U.S. Patent No. 2017 / 0294384 A1 | 93 |
| EXHIBIT 1005 | U.S. Patent No. US 9,728,547 B1 | 96 |
| EXHIBIT 1006 | Published Patent No. 10-2015-0051841 | 114 |




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REPORTER CERTIFICATE

I, JACLYN URZIA, do hereby certify:

That said deposition was taken at the time and place herein named; and that the transcript is a true record of the testimony as reported by me, a disinterested person, and was thereafter transcribed.

I further certify that I am not interested in the outcome of the said action, nor connected with, nor related to any of the parties in said action, nor to their respective counsel.

IN WITNESS WHEREOF, I have hereunto set my hand this 11th day of November, 2025.

JACLYN URZIA, RPR, CRR



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IPR2025-00228

DEPOSITION ERRATA SHEET

Case Caption:

MICRON TECHNOLOGY, INC.
vs.
YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.

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I declare under penalty of perjury that I have read the entire transcript of my deposition taken in the captioned matter or the same has been read to me, and the same is true and accurate, save and except for changes and/or corrections, if any, as indicated by me on the DEPOSITION ERRATA SHEET hereof, with the understanding that I offer these changes as if still under oath.

SIGNATURE_____DATE:_____
STEPHEN CAMPBELL

Subscribed and sworn to on the ____ day of _____, 20__ before me,
_____
Notary Public,
in and for the State of _____



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Micron v. YMTC
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