

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2025-00228
Patent 11,101,276

PATENT OWNER'S SUR-REPLY

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Exhibit List

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2001	Defendants' Preliminary Invalidity Contentions and Document Production Accompanying Invalidity Contentions re YMTC II Asserted Patents (Patent Local Rules 3-3 and 3-4), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Nov. 25, 2024) (excerpts)
2002	Civil Minutes, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Sept. 18, 2024), ECF No. 141
2003	Order Granting Stipulation to Extend Certain Deadlines Pursuant to Patent L.R. 4-2 and the Scheduling Order (ECF No. 141) Pursuant to Civil Local Rule 6-1(b), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Jan. 8, 2025), ECF No. 194
2004	Order Granting Motion to Stay Case Pending <i>Inter Partes</i> Review, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Mar. 14, 2025), ECF No. 243
2005	Plaintiff/Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.'s and Counterclaim Defendant Yangtze Memory Technologies, Inc.'s Opposition to Micron's Motion to Stay Case Pending <i>Inter Partes</i> Review and Post-Grant Proceedings, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Feb. 3, 2025), ECF No. 221
2006	Declaration of Stephen Campbell in Support of Patent Owner's Preliminary Response ("Campbell")
2007	<i>Curriculum Vitae</i> of Stephen Campbell
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2018	Order Granting Motion to Consolidate, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Aug. 21, 2024), ECF No. 106
2019	Declaration of Steve Campbell in Support of Patent Owner's Response ("Campbell2")
2020	Transcript of the Deposition of Sanjay Banerjee, Ph.D., taken October 2, 2025, <i>Micron Tech., Inc. v. Yangtze Memory Techs. Co.</i> , IPR2025-00228 (Patent No. 11,101,276)
2021	Transcript of the Deposition of Sanjay Banerjee, Ph.D., taken August 13, 2025, <i>Micron Tech., Inc. v. Yangtze Memory Techs. Co.</i> , IPR2025-00117 (Patent No. 10,672,711)
2022	<i>3D Flash Memories</i> (Rino Micheloni ed., 2016)
2023	Harmeet Singh, <i>Overcoming Challenges in 3D NAND Volume Manufacturing</i> , 60 Solid State Tech. 18 (July 2017) (excerpt)
2024	Thermo Fisher Scientific, <i>White Paper: The Challenge of Measuring Buried Critical Dimensions in High-Aspect-Ratio Structures: How Busy Fab Process Owners Can Reduce Time-to-Data in 3D NAND Metrology</i> , https://assets.thermofisher.com/TFS-Assets/MSD/Reference-Materials/helios-5-pxl-3d-nand-whitepaper-wp0025.pdf (last visited Aug. 5, 2025)
2025	Mark Lapedus, <i>What's Next for NAND?: Vendors Pin Hopes on 3D Memory, Raising Specter of 2D NAND Shortages; Other Memory Types Add to Uncertainty</i> , Semiconductor Eng'g (May 19, 2016), https://web.archive.org/web/20161127122539/https://semiengineering.com/whats-next-for-nand/ (last visited Aug. 15, 2025)
2026	Mark Shirey & Janay Camp, <i>Digging Deep Into High Aspect Ratio Process Control for Memory Technology</i> , Semiconductor Eng'g (Oct. 18, 2018), https://web.archive.org/web/20250621011306/https://semiengineering.com/digging-deep-into-high-aspect-ratio-process-control-formemory-technology/ (last visited Aug. 15, 2025)

Ex.	Description
2027	Mark Lapedus, <i>3D NAND Flash Wars Begin: Market Overcrowding, More Efficient Manufacturing, and Growing List of Scaling Issues Create a Challenging Competitive Landscape</i> , Semiconductor Eng'g (Aug. 20, 2018), https://web.archive.org/web/20180822030129/https://semiengineering.com/3d-nand-flash-wars-begin/ (last visited Aug. 15, 2025)
2028	Mark Lapedus, <i>3D NAND Metrology Challenges Growing: Rising Costs and Gaps in Equipment Emerge as Technology Scales; New Tools Under Development</i> , Semiconductor Eng'g (Apr. 9, 2019), https://semiengineering.com/3d-nand-metrology-challenges-growing/ (last visited Aug. 15, 2025)
2029	Mark Lapedus, <i>3D NAND's Vertical Scaling Race: More Competition, Business Uncertainty, and Much More Difficult Manufacturing Processes</i> , Semiconductor Eng'g (Dec. 17, 2020), https://semiengineering.com/3d-nands-vertical-scaling-race/ (last visited Aug. 15, 2025)
2030	Stephen A. Campbell, <i>Fabrication Engineering at the Micro- and Nanoscale</i> 297 (Adel S. Sedra ed., 4th ed. 2013) (excerpt)
2031	Declaration of Benjamin Smith In Response To Petitioner's Objections to Evidence [<i>served only</i>]
2032	Declaration of Robert B. Dunteman In Support of Patent Owner's Unopposed Motion for <i>Pro Hac Vice</i> Admission Under 37 C.F.R. § 42.10(c)
2033	Declaration of Benjamin Smith In Response To Petitioner's Objections to Evidence, with Appendices A-N [<i>served only</i>]

I. Introduction

The patentability of the challenged claims should be confirmed.

Petitioner's hindsight-biased arguments for claim 1's gate-stack-on-top design lacks motivation to combine. Petitioner identifies no problem to be solved or benefit motivating its changes. Petitioner's reliance on "general knowledge" is legally insufficient and ignores the complexity of 3D NAND technology.

Petitioner does not dispute that claim 1 requires exposing the etch-stop layer before etching the exposed portions, nor that Kim fails to teach how it forms contact openings. Petitioner does not show Kim satisfies claim 1's etch process, sequence, or selectivity requirements.

Petitioner disregards differences between the prior art, background references, and embodiments that would have counseled against its modifications, including the impact of additional layers on over-etching and tunneling, materials used, etch chemistry, and structure.

II. Claim Construction

Petitioner does not dispute Patent Owner's proposed construction. Reply 1-2. The Board should interpret the claims to require that "the exposure step does not penetrate through the etch-stop layer prior to forming the plurality of openings." POR 13. Regardless, Petitioner's Grounds fail under any reasonable construction.

III. Ground I: Kim in View of a POSITA's Knowledge

Petitioner fails to show that Kim renders the '276 patent obvious. Petitioner's expert modifies Kim without providing *any* reason a POSITA would have done so because (Pet.33), according to Petitioner, a "well-known" alternative needs no motivation. Reply 4. Not so. *Virtek Vision Int'l ULC v. Assembly Guidance Sys., Inc.*, 97 F.4th 882, 887-88 (Fed. Cir. 2024).

A. Claim 1 would not have been obvious

1. Kim does not render gate-stack-on-top obvious

Petitioner combines Kim's Figures 17A-22B embodiment with Kim's separate Figures 5A-14B embodiment to allegedly render obvious the gate-stack-on-top configuration. Pet.29-34; Reply 4-6. But Petitioner provides no motivation to combine these embodiments, which is necessary even within a single reference. *In re Stepan Co.*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017); *Micron Tech., Inc. v. Netlist, Inc.*, 2026 WL 480156, *5-6 (Fed. Cir. Feb. 20, 2026) (non-precedential).

Petitioner argues there is motivation because the "inverted order is a suitable alternative." Reply 2-5. But the Petition identified no problem solved by modifying the semiconductor structure to include an opposite gate-stack order and other resulting changes, much less that Kim's alternative embodiment solves the *same problem* as the Figures 17A-22B embodiment. Thus, *Intel Corp. v. PACT XPP Schweiz AG* is distinguishable. *See id.* 2-3 (quoting 61 F.4th 1373, 1380 (Fed. Cir. 2023)); POR 16-19.

Petitioner belatedly argues that inverting the gate-stack order is a suitable alternative because either order “meet[s] the demand for higher-density memories.” Reply 3. This over-generalized argument (applicable to *all* memory device improvements), is absent from the Petition and unsupported by evidence. *Icon Health & Fitness, Inc. v. Strava, Inc.*, 849 F.3d 1034, 1043 (Fed. Cir. 2017) (“Attorney argument is not evidence.”¹). It is not that Kim’s various embodiments are not “suitable alternatives” to high-density memory generally, but that features within one embodiment (e.g., gate-stack-on-stop), are not suitable alternatives in the overall structure of another embodiment. Like the petitioner in *CommScope, Inc. v. TQ Delta, LLC*, Petitioner presented no evidence that “identify[s] a need or problem known in the field of endeavor at the time of invention or explained how” the gate-stack-on-top configuration “helped address that problem.” IPR2022-01012, 2023 WL 7491179, *11 (Nov. 13, 2023) (rejecting *Intel*-based argument). This deficiency is fatal and demonstrates Petitioner’s hindsight bias.

Unlike in *Intel*, the stack order here is not a discrete device to be “swapped out,” even assuming both layer orders solve the same problem. 61 F.4th at 1376-79 (replacing “secondary cache” with “segmented global [secondary cache]”).

¹ All emphases added and citations omitted unless indicated otherwise.

Petitioner's "suitable alternative" argument ignores these and other necessary, resulting changes to the device. *Supra* §III.A; POR 18-19.

Petitioner next relies on *Boston Scientific Scimed, Inc. v. Cordis Corp.*, to argue that combining embodiments from a single reference does not require the reference to recognize the resulting benefits. Reply 3-4 (citing 554 F.3d 982, 990-92 (Fed. Cir. 2009)). Petitioner's reliance is misplaced. First, *Boston Scientific* involved a purely additive change (adding optional coating from one stent to another), whereas Petitioner proposes a ***structural rearrangement*** requiring cascading manufacturing changes. POR 18-23, 29-30. Second, even when "combining multiple embodiments from a single reference, ... there must be a motivation to" combine. *Stepan*, 868 F.3d at 1346 n.1. The *Boston Scientific* court found a specific motivation because the missing element would have provided the same "benefits" in both closely related embodiments. 554 F.3d at 992; *Intel Corp. v. Tela Innovations, Inc.*, IPR2019-01521, 2021 WL 912764, *9-10 (Mar. 9, 2021). Here, however, Petitioner identifies no benefit a POSITA would have recognized in reversing the gate-stack orders. Finally, "[c]entral to the motivation-to-combine inquiry is consideration of fundamental differences between the references," which Petitioner failed to do here. *Micron*, 2026 WL 480156, *5; Campbell2 (Ex.2019) ¶¶39-61.

Petitioner points to other Kim embodiments and other references not included in its proposed combination to argue that gate-stack-on-top was known. Reply 4. But

“[t]he mere fact that these possible arrangements existed in the prior art ***does not provide a reason*** that a skilled artisan would have substituted” one reference for another. *Virtek*, 97 F.4th at 887-88. In *Virtek*, the Federal Circuit reversed the Board’s motivation-to-combine finding because the petition failed to “articulate[] any reason to substitute one [system disclosing a missing limitation] for another or any advantages that would flow from doing so,” and the petitioner’s expert did not “articulate any reason why a skilled artisan would combine these references,” other than “both such measurement systems were known.” *Id.*; see *ActiveVideo Networks, Inc. v. Verizon Commc’ns, Inc.*, 694 F.3d 1312, 1327 (Fed. Cir. 2012).

As in *Stepan*, Petitioner provides no evidence supporting a motivation and merely asserts that because (1) Kim’s other embodiments disclose the opposite order, and (2) other references show the claimed order, switching the gate-stack order in Kim was “suitable.” Pet.31-35. In other words, a POSITA could have switched, but had no reason to. Patent Owner’s evidence, in comparison, demonstrates *why* a POSITA would *not* have been motivated to modify Kim. Switching the gate-stack order is not routine and would require other structural changes, and a POSITA would not have reasonably expected success because of changes to etching processes and structure in Kim’s Figures 17A-22B embodiment. POR 16-24; Campbell2 ¶¶34-52; Kim (Ex.1005) [0185], [0187] (disclosing gate-stack-on-bottom in Figures 17-22 embodiment).

2. A POSITA would not have reasonably expected to succeed with Petitioner's modifications

A POSITA would not have reasonably expected success modifying Kim. POR 20-24.

Petitioner fails to adequately address technical problems Dr. Campbell identified with Petitioner's layer inversion. Reply 5-6. Petitioner acknowledges a POSITA would have to omit certain "step-shaped insulating layers" or "adjust layer thicknesses" to avoid these problems (*id.*), but does not show how or why a POSITA would have accomplished either. Petitioner relies on Figures 31-34 embodiments to argue the "step-shaped insulating layers" can be omitted, but provides no motivation to combine these embodiments with Figure 22A. Kim [0227], [0232]. Petitioner's assertion that "a POSITA would have known to adjust layer thicknesses," even though Dr. Banerjee failed to do so in his modified versions of Kim, is the kind of prohibited post-hoc rationalization. *ActiveVideo Networks*, 694 F.3d at 1327. Finally, Petitioner's "bodily incorporat[ion]" argument is irrelevant because Patent Owner did not make that argument. Reply 6. Patent Owner showed Petitioner's layer-reversing modification creates multiple technical issues undermining any reasonable expectation of success. POR 20-24.

Petitioner dismisses the complexities of other cascading modifications as "routine." Reply 6. Dr. Campbell testified, for example, that shortening contact plugs requires altering etching steps and processes that are complex and sensitive to even

minor adjustments. Campbell² ¶46; POR 27-30. Petitioner does not explain why a POSITA would nonetheless have reasonably expected success.

Petitioner argues that “Kim’s etch-stop layer undisputedly facilitates preventing punch-through” and “is thus desirable” regardless of layer order. Reply 7. But undermining that position, Kim itself includes embodiments with no etch-stop layer, including Figures 4-15D, on which Petitioner relies for layer switching. POR 22; *see also* Kim Figs.30-33.²

Petitioner’s argument that “Kim has no missing limitations” is wrong, as evidenced by its reliance on general knowledge. Petitioner does not identify a single embodiment in Kim or any other reference that teaches every claim limitation. Thus, to rely on general knowledge Petitioner must (but cannot) demonstrate that the limitation is “unusually simple” and 3D NAND technology is “particularly straightforward.”³ *See DSS Tech. Mgmt., Inc. v. Apple Inc.*, 885 F.3d 1367, 1374 (Fed. Cir. 2018). Petitioner argues it can rely on general knowledge because the

² *In re Passal* is inapposite. 426 F.2d 409, 412 (C.C.P.A. 1970). In this fifty-year-old case, the “contrary result” was not found in any reference, unlike here.

³ Dr. Campbell’s testimony is not contradictory; Petitioner takes it out of context. Reply 9-10 (citing Ex.1091, 37:20-38:12, 40:12-22). The testimony Petitioner cited discusses manufacturing challenges generally, not layer-order inversion specifically.

missing limitations were allegedly known in the art. Reply 9-10. That certain techniques were known does not make the combination obvious. *Virtek*, 97 F.4th at 887-88; *ActiveVideo*, 694 F.3d at 1327. Nor does the fact that “general fab techniques are known” mean the technology is straightforward. Reply 10. Dr. Campbell and the literature confirm the complexities involved when modifying structure, manufacturing, and etch-processes in a device. Campbell2 ¶¶48-53. Even small changes in the fabrication process can have significant effects, and “details matter.” *Id.*; Ex.2021, 45:9-46:6, 57:2-13. Even if the gate-stack-on-top is a “peripheral limitation,”⁴ and it is not, reliance on common sense “must still be supported by evidence and a reasoned explanation,” which Petitioner fails to provide.⁵ *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1363 (Fed. Cir. 2016). General knowledge “cannot be used as a wholesale substitute for reasoned analysis and evidentiary support.” *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337-38 (Fed. Cir. 2020). Thus, Petitioner fails to meet its burden. *Dynamic*

⁴ This argument is forfeited as it is not in the Petition.

⁵ *Lockwood v. American Airlines, Inc.* (Reply 10), is irrelevant. 107 F.3d 1565, 1570 (Fed. Cir. 1997). *Lockwood* was a public-use case holding that public use of a device was enough to put the claimed features in the public's possession even if unclaimed features were not publicly available.

Drinkware, LLC v. Nat'l Graphics, Inc., 800 F.3d 1375, 1378-79 (Fed. Cir. 2015) (“Failure to prove the matter as required by the applicable standard means that the party with the burden of persuasion,” here Petitioner, “loses.”).

Finally, Petitioner assumes, incorrectly, that the absence of details about changing the gate-stack order in Chen “demonstrates” a POSITA would have reasonably expected success modifying Kim’s Figure 22A to gate-stack-on-top. Reply 5. Petitioner ignores Chen’s teachings. Chen is focused on reducing tunneling effects between gate stack and word lines, which is unaffected by gate-stack ordering, and obviates the need to provide details about layer ordering. *See* Chen (Ex.1008) [0004]-[0007], [0020], [0047]-[0054].

3. Kim does not disclose “forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer”

Petitioner does not dispute that Kim’s Figure 22A omits teaching “how the contact openings are formed” or that claim 1 requires “a process where [the] contact holes are formed by first forming a plurality of openings exposing the etch-stop layer, prior to etching the ‘exposed portions’ of the plurality of openings exposing the conductive layer (i.e., not penetrating through the etch-stop layer).” POR 32; Reply 11-12. Petitioner argues only that the “essence of an etch-stop layer dictates that contact-hole etching stops or slows down upon contact, *i.e.*, exposing without penetrating it,” based on etch-selectivity. Reply 11.

But Petitioner cannot show that Kim teaches forming a “plurality” of openings before etching the exposed portions of the etch-stop without etching through the etch-stop layer. POR 34. Petitioner shows only that when forming a particular opening, Kim’s etch-stop layer performs an etch-stop function *in that* opening, not the plurality of openings. But claim 1 requires that the etch-stop layer remain whole (unetched), until *all* the *plurality* of openings are formed. *Id.* 8-13, 32.

Petitioner provides no evidence that Kim teaches forming all openings before etching the etch-stop layer to expose the conductive layer. *Id.* 32; Reply 1, 11. Instead, Petitioner misdirects by citing Dr. Campbell’s testimony discussing the function of etch-stop layers generally, *not* how Kim’s contact holes are formed and etch-stop layer penetrated in the plurality of contact holes. Reply 11 (citing Ex.1086); Ex.1086, 71:6-13 (questions in “general terms”). Dr. Campbell discussed how contact holes can be formed not simultaneously, which would not meet the requirements of claim 1. Ex.1086, 63:10-20 (“The only caveat is in some technologies they will etch in groups *and not all at once.*”). The ’276 patent overcomes the prior art’s deficiencies, among other things, by forming openings “simultaneously” as opposed to “separate etching processes.” ’276 patent 5:55-6:7.

Petitioner also argues that “Kim’s etch-stop layer prevents punch-through” in response to Patent Owner’s argument that Kim’s etch-selectivity disclosure concerns planarization, not contact-hole formation. Reply 11. This fails for two reasons.

Whether Kim's etch-stop layer prevents punch-through *when forming a particular opening* does not mean Kim's etch-selectivity disclosures relate to CMP planarization—neither Petitioner nor its expert presents contrary evidence. *Id.* 11-12; POR 34 (quoting Dr. Banerjee admitting etch selectivities between CMP and forming contact holes was “comparing apples to oranges”). Indeed, the Petition states that “[e]tch selectivity **depends on the** etchant.” Pet.21. As stated above, the etch-stop function of Kim's etch-stop layer does *not* disclose how openings are formed and the conductive layers subsequently exposed, as claimed. Petitioner does not rebut that “[r]egardless of whether Kim's disclosure regarding planarization applies to forming holes for the WPLGs, Kim does not teach that such a process forms a plurality of openings exposing the etch-stop layer without etching through the etch-stop layer.” POR 34. Thus, Petitioner's position (i.e., that all of Kim's contact holes *must inherently* be formed at once because Kim has an etch-stop layer), contradicts the record and demonstrates Kim does not render obvious claim 1. *Id.*; Reply 11.

Petitioner's shift in Reply to an inherency argument fails as a matter of law because, as shown above, forming the plurality of contact holes *before* etching the etch-stop layer to expose the conductive layer is not inherently disclosed because it is not “necessarily ... present[] or the natural result” of Kim Figure 22A. *PAR Pharm., Inc. v. TWI Pharms., Inc.*, 773 F.3d 1186, 1195-96 (Fed. Cir. 2014).

B. Claims 4 and 5 would not have been obvious

Petitioner does not dispute its reliance on a POSITA's knowledge to supply the missing limitations in claims 4 and 5 and instead argues Patent Owner failed to "address[] why" the limitations are unusually simple. Reply 12. But Petitioner has the burden to prove obviousness and is the one relying on general knowledge. POR 26 & n.5, 35-36. Regardless, Patent Owner demonstrated that 3D NAND is not straightforward (*id.* 27-28) and that etching contact holes through the etch-stop layer is not unusually simple (*id.* 28); *see* Ex.2021, 40:20-22, 41:5-8, 45:12, 46:18, 57:2-3, 61:18-19 (Dr. Banerjee confirming "specifics matter" and "details matter"). Even "*small changes* ... can have significant effects." Campbell2 ¶¶62-63.

Petitioner's Reply does not remedy these deficiencies. Petitioner argues that claim 4's relative-etching-rate limitation represents one of three relationships, and "common knowledge demonstrates that only the claimed relationship is realistic." But that does not mean it is unusually simple or the combination was obvious. Reply 12-13. Petitioner's argument for claim 11 fails for the same reason. POR 38-39. Moreover, Dr. Campbell's statement that punch-through represents "a failure of the etch-stop layer" (Ex.1086, 92:12-25), does not establish a particular etch-rate relationship relative to the conductive layer. Punch-through is merely a defect to avoid. POR 37-39; Campbell2 ¶¶62-68.

For claim 5, Petitioner argues that because “punch-through of gate-electrode layers must be prevented,” a POSITA would have wanted to “further protect the gate electrode” by using the first high-k dielectric layer as an etch-stop.⁶ Pet.52; POR 37-38. But Kim’s multiple etch-stop layers already do. POR 37; Campbell2 ¶¶65-68. Petitioner’s expert responds only that it is “irrelevant.” Banerjee2 (Ex.1085) ¶49; POR 38. But the high-k layer’s protection of the oxide layer during formation of the conductive layer demonstrates it has a purpose separate from being an etch-stop; thus it is not obvious it would have a lower etch rate than the etch-stop layer. Further, making the etch-stop and first high-k dielectric form the same material would increase etch-stop thickness and serve both purposes. POR 38; Campbell2 ¶67.

Petitioner provides no reason why a POSITA would consider further etch-stop protection necessary or “advantageous,” especially where doing so would require an

⁶ Petitioner argues Patent Owner waived argument that the Petition fails to establish a reasonable likelihood of success. Reply 13 n.5. Not so. Reasonable-expectation-of-success and motivation-to-combine arguments can be “intertwined.” *Elekta Ltd. v. ZAP Surgical Sys., Inc.*, 81 F.4th 1368, 1376 (Fed. Cir. 2023). Patent Owner’s arguments that the disadvantages and tradeoffs of further, unnecessary etch-protection would not motivate a POSITA to make such a modification also show the POSITA would not have reasonably expected success. *See id.*; POR 37-38.

additional etch process and etch chemistry during manufacturing. POR 37; Campbell2 ¶67. Instead, Petitioner insufficiently argues a hypothetical etchant not disclosed in Kim would etch silicon nitride (Kim's etch-stop layer) and silicon oxide (Kim's barrier layer), but not aluminum oxide. Pet.52-53; Reply 13 (citing Banerjee2 ¶¶46-48).

IV. Ground II: Kim in View of Fang

Ground II fails for the reasons discussed regarding Ground 1 and additional reasons. POR 39-55.

A. Fang and Kim address different problems

Kim prevents damage during CMP planarization on top of the device, while Fang prevents damage from over-etching contact vias on the staircase steps. POR 41; Campbell2 ¶¶73-75. Petitioner does not dispute the former. Reply 14-15. Petitioner argues instead that Kim *also* is concerned with punch-through because it has an etch-stop layer. *Id.* 14. But a generalized punch-through concern would not have motivated a POSITA to adopt Fang's etch-stop layer and contact-hole etching characteristics for Kim when Kim *already* provided adequate protection against punch-through. For example, Kim includes two etch-stop layers and a high-k dielectric surrounding the gate stack; there would have been no reason to adopt materials or characteristics from Fang to prevent punch-through, especially given the complexity of modifying materials and etch process in its design. POR 47-48;

Campbell2 ¶¶44-53, 71-90; *see South-Tek Sys., LLC v. Engineered Corrosion Sols., LLC*, 748 F. App'x 1003, 1007 (Fed. Cir. 2018) (affirming Board's finding a POSITA would not be motivated to combine a reference that provided "redundant function[]").

B. Fang's use of CDSN would have dissuaded a POSITA from combining it with Kim

Petitioner argues the prior art and Dr. Campbell's testimony contradict Patent Owner's arguments. Reply 15. Not so. Dr. Campbell did not "equate[] silicon nitride and carbon-doped silicon nitride," as Petitioner suggests. *Id.* He discussed them in the context of Chen's *tunneling* length disclosure in Ground 4, *not* etch-stop properties in substituting silicon nitride for CDSN. Campbell2 ¶107 (citing Chen [0053]).

Petitioner argues Fang's disclosures apply broadly to "any suitable etch-stop material." Reply 15. But Kim's silicon nitride is *not* suitable according to Fang. POR 44-47. A POSITA would not have combined Fang's CDSN, or high-k etch-stop, with Kim. *Id.* Kim does not use CDSN, and Fang's etch-stop thickness does not apply to Kim's undoped silicon nitride. *Id.* Petitioner's argument that CDSN is merely "exemplary" ignores that CDSN is central to all aspects of Fang's disclosures, and every claim of Fang requires CDSN. Campbell2 ¶¶76-80.

Petitioner argues that even if Fang's disclosures are specific to CDSN, this is irrelevant because Kim uses a dry etch and, according to Petitioner, "carbon-doping has no impact on the dry-etch rate." Reply 15-16. These arguments fail.

Petitioner's "dry-etch rate" argument, being new and depending on new evidence, is improper. *Wasica Fin. GmbH v. Cont'l Auto. Sys., Inc.*, 853 F.3d 1272, 1286 (Fed. Cir. 2017). The term "dry-etch rate" is not in the Petition; the Board should not credit Ex.1089 because it could have been provided in the Petition and Patent Owner had no opportunity for its expert to challenge it in Sur-Reply. *Pioneer Pet Prods., LLC v. Oil-Dri Corp. of Am.*, IPR2022-00691, 2023 WL 5955777, *12 (Sept. 12, 2023) (acknowledging "the prejudice to Patent Owner [if] we consider the new arguments and evidence in Petitioner's Reply").

Petitioner's reliance on Ex.1089 is also wrong technically. Petitioner incorrectly assumes that because etch-rates for varying levels of carbon-doping in silicon nitride appear constant for the etchant used in Ex.1089, they are constant for *any* etchant or for doped versus undoped silicon nitride. See Campbell² ¶¶50, 63, 76-80. Etch characteristics vary by chemistry and material. *Id.*

Dr. Banerjee relies on additional new evidence (Ex.1090), purporting to demonstrate a constant etch-rate for varying levels of carbon-doping in CDSN. But nowhere does Ex.1090 state it is addressing CDSN or use the term "doped" or

“doping,” as opposed to silicon carbon nitride, which Fang excludes.⁷ Fang (Ex.1006) [0017], [0022]. This untimely evidence should receive no weight. *Pioneer*, 2023 WL 5955777, *12.

C. Petitioner ignores the impact of material differences between Kim and Fang

Petitioner attempts unsuccessfully to mitigate structural differences between Kim and Fang.

1. Underlying structural differences counsel against motivation

First, Petitioner argues that “structural differences below the etch-stop layer are irrelevant to etching the overlying insulating layer” and “to the etch-stop characteristics when the etch-stop layer works as intended.” Reply 17. This argument, that whatever is under the etch-stop layer is irrelevant to the etch-stop layer, contradicts the record and the fundamentals of 3D NAND structures. Petitioner does not dispute that different materials have different etch chemistries or that how layers interact depends on materials used. POR 44. Indeed, Petitioner’s own expert stated that “[d]ifferent materials react to an etchant differently” and

⁷ Petitioner attempts to cure this deficiency with unsupported testimony about “doping.” Banerjee² ¶61 n.15. The Board should disregard Dr. Banerjee’s belated, conclusory opinion.

“etching rate is used to characterize how fast or slow an etchant etches through a particular material.” *Id.* 44-45 (citing Ex.1003 ¶52). Yet Petitioner now contends that underlying layers serving as back-up etch stops “is a made-up issue.” Reply 17-18. Petitioner’s expert testified otherwise. Ex.2021, 44:21-45:5 (two etch-stop layers function as “safety margins” and provide “additional flexibility in preventing over etching”), 45:9-46:6 (underlying high-k dielectric gives “additional margins of safety”), 48:2-49:8 (“the more different materials [that] the etch has to go through, in general, that provides additional safety margins”). That Kim already has adequate “safety margins,” disclosing two etch-stops and a high-k dielectric layer, further demonstrates why a POSTIA would have no motivation to adapt Fang’s etch-stop layer characteristics to Kim when “the etch-stop layer works as intended.” *See* POR 47-48; Reply 17.

2. Fang’s alternative etch-stop material does not support a motivation

Petitioner does not adequately respond to Patent Owner’s arguments. Specifically, Petitioner’s arguments that a POSITA would combine Fang’s alternative high-k material to Kim’s etch-stop to reduce tunneling fail to respond to Patent Owner’s argument that Kim *already includes* a high-k dielectric surrounding its gate stack. POR 52-53. Notably, Chen does not include a high-k dielectric layer. *Id.* Thus, Petitioner cannot derive a motivation to combine based on Chen’s tunneling problems where Chen fails to account for a high-k dielectric surrounding

the gate stack and its effect on tunneling. *Id.* Petitioner's arguments about Kim's two-etch-stop configuration fail for the same reason, as Petitioner fails to show there would be any marginal benefit to using Fang's alternative material in Kim's design that includes two etch-stop layers *and* a high-k dielectric around the gate-stack to further protect against tunneling. Reply 19-20.

Petitioner is also wrong that Fang discloses high-k dielectrics "equally" as an alternative etch-stop material, where "in all other respects Fang is directed exclusively towards CDSN." POR 44, 51 n.10. Nor has Petitioner adequately demonstrated that carbon-doped silicon nitride at varying levels universally has the same dry etch-rate as undoped silicon nitride and for any etchant. Campbell2 ¶¶41, 49-50.

Petitioner argues that Patent Owner's arguments address "only a subset of Petitioner's position" by arguing against the exemplary hafnium oxide as an alternative to CDSN in Fang. But Patent Owner was responding in context of the sole exemplary material Petitioner identified. Pet.65, 67, 72, 80, 93. Patent Owner's arguments regarding hafnium oxide are merely exemplary and apply equally to other alternative materials. POR 51-54.

Petitioner assumes that because Fang does not include guidance on using hafnium oxide, hafnium oxide is so routine a POSITA would have no trouble applying it to Kim. Reply 20; Pet.67, 71. But Petitioner ignores the myriad structural

and design differences between Kim and Fang that would prevent a reasonable expectation of success under Petitioner's theory. POR 40-51, 54.

Finally, Petitioner fails to address Patent Owner's arguments in the context of claim 6 and merely references its earlier arguments. These arguments fail for the reasons described. *Id.* 54-55; Reply 20.

V. Ground III: Han in View of Fang

A. Petitioner fails to show a motivation to combine Han and Fang

Petitioner suggests that because Kim and Park have both an etch-stop layer and an underlying high-k dielectric layer, a POSITA would be motivated to add Fang's etch-stop layer to Han.⁸ Reply 21-22. Petitioner ignores that Kim also discloses embodiments with a single underlying high-k layer and no etch-stop layer. Kim Figs.16, 30. Likewise, Kim discloses embodiments with a single etch-stop layer with no high-k layer, like Fang. *Id.* Fig.34. Kim even discloses embodiments with neither a high-k nor etch-stop layer. *Id.* Fig.33. Petitioner also fails to address the redundancy of the combination. POR 56-60. Han already provides adequate protection against punch-through. *Id.* A POSITA would not be motivated to add a

⁸ Petitioner's Reply relies belatedly for the first time on Park, which is not part of any ground or in the Petition. Reply 6, 21-22, 24; *Pioneer*, 2023 WL 5955777, *12. Petitioner's arguments related to Park are forfeited.

redundant etch-stop to Han only because Kim and Park use an etch-stop with underlying high-k dielectric. *Id.* 56-63. Petitioner also contradicts itself—arguing that having layers underneath an etch-stop serve as back-up etch stops “is a made-up issue,” while simultaneously arguing that added layers “reduc[e] the likelihood of punch through” and would motivate a POSITA to combine Han and Fang. Pet.102 (original alteration); Reply 18, 22-23.

Petitioner fails to adequately address Patent Owner's other arguments. Petitioner argues that it did not rely on Han's multiple high-k layers, but that is irrelevant because they counsel against the combination. Reply 21. Further, Han already addressed the punch-through problem in at least two ways different than Fang. POR 59-60; Reply 22-23. Nor can Petitioner identify anywhere Han expresses the same concerns as Fang for its design, including its choice for using a high-k dielectric layer together with a staged etching process. Petitioner cannot “create a problem with the prior art in hopes of creating a motivation to combine references.” *Arctic Cat Inc. v. Polaris Indus., Inc.*, 795 F. App'x 827, 833 (Fed. Cir. 2019). Further, Fang's etch-stop layer design, including thicknesses, are for a gate-stack-on-bottom model, unlike Han. Reply 23.

B. Petitioner fails to establish that missing limitations of claims 4-5 are unusually simple

Petitioner incorrectly states that Patent Owner *only* argues against combining Han with a POSITA's knowledge to render claim 4 obvious. But Patent Owner

argues that a POSITA would not combine Fang's etch-stop characteristics, including those associated with claim 4, to Han for many reasons. POR 56-60.

Further, Petitioner argues that Patent Owner's arguments were "insufficient to show" that missing limitations of claims 4-5 "are not unusually simple." But that is Petitioner's burden. *Id.* 24-26.

C. Petitioner fails to establish a motivation to combine and reasonable expectation of success to render claim 5 obvious.

Petitioner argues Patent Owner failed to explain why its claim 5 arguments for Kim are applicable to Han, however Patent Owner did just that after referring to the POR, §III.D.2. POR 62. Like Kim, Han already provides adequate protection during contact hole etching, for example, by using multiple protective layers. *Id.* And the claimed etch-rate relationship is not the only sensible relationship. *Id.* Petitioner's arguments also fail for the reasons explained above. *Supra* §§III.B, V.A.

In the Petition, Petitioner argued a POSITA's knowledge based on a background reference's relative etch rates in "argon plasma" renders claim 5 obvious. Pet.92 (citing Ex.1027); POR 63. Petitioner now argues a "hydrogen-bromide-and-argon" *mixture* in the reference produces the etch-rate that renders claim 5 obvious. Reply 24. This argument is forfeited. *Pioneer*, 2023 WL 5955777, *12.

VI. Ground IV: Han in View of Fang and Chen

Petitioner fails to address Patent Owner's arguments that a POSITA would not be motivated to add Chen's barrier layer to Han and Fang. POR 63-68. Petitioner refers only back to its arguments regarding the Han and Fang combination without taking up the further redundant nature of Chen's barrier layer. Reply 25. Both Han alone, and in combination with Fang, adequately address punch-through concerns. There is no motivation to combine them on that basis. *Supra* §V.A; POR 56-66.

Adding Chen's barrier layer would also be redundant for tunneling protection. POR 66. Even where tunneling length is adequate, Petitioner appears to argue that more protection would be even better. Reply 25. But Petitioner has not shown that marginal gains to tunneling length, if any, would have motivated a POSITA to add Chen's barrier layer against the added complexity, expense, and difficulty of the resulting manufacturing and design. POR 66. Han is not concerned with tunneling, and the Han and Fang combination already produces the preferred energy-gap properties listed in Chen. *Id.*

Petitioner minimizes the inherent structural design and processing challenges in adding Chen to Han and Fang and argues the choice between one or two etch stops represents a "common tradeoff in engineering." Reply 26. However, Petitioner's proposed combination deals with tradeoffs between two, three, and four potential etch-stop layers, each requiring new manufacturing and etch processes and adding

complexity. POR 67-68. Petitioner provides no support for its “more is always better” approach to finding a motivation.

Finally, Chen is concerned with etch-stop layers for their effect on tunneling length during device operation, not on their etch-process-control function during fabrication. Chen [0004]-[0007], [0020], [0047]-[0054]; POR 68. Indeed, beyond using the traditional nomenclature of calling the layer an “etch-stop,” Chen describes the layers’ functional benefits exclusively as they relate to electrical isolation properties and not their role in manufacturing etch processes. For example, there is no description of etch selectivity or its ability to protect underlying layers.

VII. Dr. Campbell Is a POSITA

Petitioner challenges Dr. Campbell’s qualifications by selectively quoting its definition and Dr. Campbell’s testimony to omit that a POSITA may be qualified by “knowledge” and “training.” Reply 27; Pet.26. Petitioner fixates on “design[,]” which is merely an example of “experience” under its definition and not necessary to qualify as a POSITA. Reply 27; Pet.26. Regardless, Dr. Campbell meets the qualifications of a POSITA. Ex.1091, 152:21-153:17.

Dr. Campbell testified that, as a fabrication and processing expert, he has adequate knowledge of semiconductor design. He testified that etch processes, the materials selected, the depth and aspect ratio, and the order of layers “align very well with [his] areas” of expertise. *Id.* 133:8-24. Dr. Campbell testified that he has

sufficient experience to opine on design aspects that relate to etch processes. *Id.* 134:17-135:3. Dr. Campbell is uniquely qualified to testify regarding the '276 patent's limitations and its technology based on his fabrication and processing expertise and corresponding understanding of semiconductor design. *Id.* 150:20-151:5.

Moreover, Dr. Campbell testified that the '711 patent, which shares its specification with the '276 patent, is a *processing* patent, and a POSITA in design alone could not practice it. *Id.* 150:13-151:5. Yet, Petitioner challenges Dr. Campbell's testimony about "design" and does so without explaining which aspects of the prior art or the limitations purportedly rely on the "design" of semiconductors as opposed to fabrication. Further, the "design" aspects for which Dr. Campbell said he was not an expert relate specifically to *circuit* design. *Id.* ("The design, if you will, where the transistors go and so forth is really modest by comparison."). If the '276 patent involved aspects of design, Dr. Campbell testified these concepts are sufficiently well-known to a POSITA involved in the fabrication of semiconductor devices. *Id.* 130:19-131:3, 133:8-134:8, 134:17-135:3, 150:20-151:5. Dr. Campbell *is* a processing and fabrication expert regarding "which layers go where and how thick they are and how you're going to etch things." *Id.* 150:13-151:5.

Petitioner's other attacks on Dr. Campbell's testimony also fail. First, Petitioner argues Dr. Campbell's testimony is "virtually unsupported by any

evidence” and “parrots PO’s arguments.” Reply 27. Petitioner argues (without support) for a corroboration requirement to expert testimony, which is plainly wrong: “There is no corroboration requirement for expert testimony asserted to defend *against* an invalidity challenge.” *MEMC Elec. Materials, Inc. v. Mitsubishi Materials Silicon Corp.*, 248 F. App’x 199, 205 (Fed. Cir. 2007) (original emphasis). Dr. Campbell’s testimony *is* evidence. Moreover, Petitioner’s argument is ironic considering Petitioner’s deficient motivation-to-combine arguments rely on nothing but Dr. Banerjee’s conclusory opinion that modifications were well-known, which *is* insufficient. *See, e.g., supra* §III.A; *Virtek*, 97 F.4th at 888. And Dr. Banerjee’s Declaration not only parrots, but is often a carbon copy of Petitioner’s entire arguments. *Compare* Ex.1003 ¶¶88-106, *with* Pet.35-50 (§X.B).

Second, Petitioner argues Dr. Campbell is unfamiliar with his declaration. Reply 27. Petitioner cherry picks a single response to a question Dr. Campbell had already answered. Ex.1086, 133:21-134:9. Petitioner’s attempt to parse words in its definition of a POSITA and assert incorrect legal standards is a red herring.

VIII. Conclusion

For the reasons above, the Board should deny the Petition for Inter Partes Review.

Respectfully submitted,

Dated: March 18, 2026

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CERTIFICATE OF COMPLIANCE WITH 37 C.F.R. § 42.24

I hereby certify that this Patent Owner's Sur-Reply complies with the word count limitation of 37 C.F.R. § 42.24(c)(4) because the Patent Owner's Sur-Reply contains 5,597 words using Microsoft Word's counting feature, excluding the cover page, signature block, and the parts of the Patent Owner's Sur-Reply exempted by 37 C.F.R. § 42.24(c).

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 18th day of March, 2026, a true and correct copy of the foregoing **Patent Owner's Sur-Reply** was served by electronic mail on Petitioner's lead and backup counsel at the following email addresses:

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