

Micron Technology, Inc. (Petitioner)
v.
Yangtze Memory Technologies Company, Ltd. (Patent Owner)

IPR2025-00228 (US Patent 11,101,276)

Patent Owner YMTC's Demonstratives

April 27, 2026



Four Asserted Grounds Fail

Petition

Petitioner challenges the claims on the following grounds:

Ground 1: Claims 1-2, 4-5, 9-18 are obvious over Kim in view of a POSITA's knowledge;

Ground 2: Claims 1-18 are obvious over Kim in view of Fang.

Ground 3: Claims 1-15 are obvious over Han in view of Fang.

Ground 4: Claims 17-18 are obvious over Han in view of Fang and in further view of Chen.

Pet. 12



'276 Patent

Ground 1 (Kim) Fails

Ground 2 (Kim + Fang) Fails

Ground 3 (Han + Fang) Fails

Ground 4 (Han + Fang + Chen) Fails



'276 Patent

Ground 1 (Kim) Fails

Ground 2 (Kim + Fang) Fails

Ground 3 (Han + Fang) Fails

Ground 4 (Han + Fang + Chen) Fails

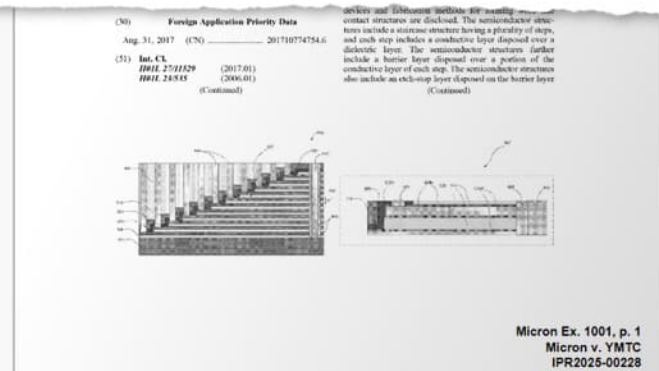


The '276 Patent

WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF



Patent No.: US 11,101,276 B2
Date of Patent: Aug. 24, 2021



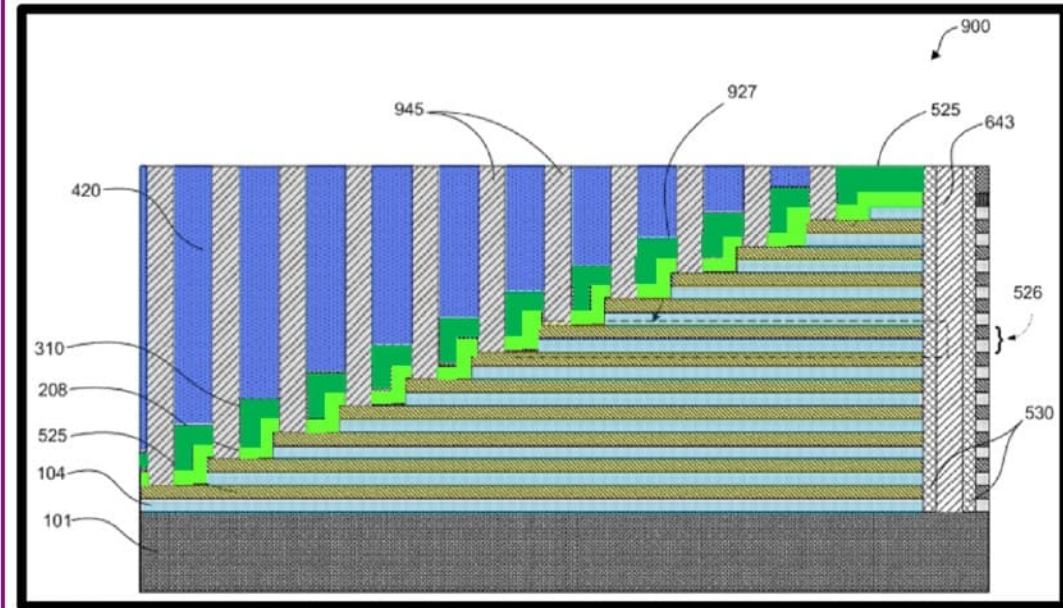
Ex. 1001 ('276 Patent)

'276 Patent - 3D NAND Difficulties

Various embodiments in the present disclosure provide methods and structures for **improving word line contacts for 3D memory devices**. In the present disclosure, a single lithography mask can be used to form contact areas for word lines of 3D memory array. **By adding an etch-stop film over the staircase structure, openings of the vertical interconnect access (VIA) contacts for each level of the staircase structure can be formed simultaneously. The etch-stop film protects underlying layers during etching processes that form contact VIAs. The etch-stop film is exposed on each level of the staircase structure by a selective etching process, and then removed by reverse selective etching.** Accordingly, the disclosed methods and structures can improve fabrication yield and reduce cost. The methods and structures described herein can be used to form semiconductor interconnect structures for inter-connecting components at different layers with an uneven topology.

Ex. 1001 ('276 Patent), 5:61-6:10

'276 Patent, Fig. 9A



No.	Structure
525	Gate Stack
104	First Insulating Layer
208	Second Insulating Layer
310	Etch-Stop Layer
420	Third Insulating Layer
945	Vertical Interconnect Access Conductive Structures

POR 6; Ex. 1001 ('276 Patent), Fig. 9A (annotated)

'276 Patent's Solution

1. A method for forming a semiconductor structure, comprising:

- forming a staircase structure having a plurality of steps, wherein the forming of each step of the plurality of steps comprises disposing a sacrificial layer over a dielectric layer;
- disposing an etch-stop layer on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer;
- disposing an insulating layer on the etch-stop layer;
- replacing the sacrificial layer of each step with a gate stack, the gate stack comprising a conductive layer and a first high-k dielectric layer;
- forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer;
- etching the exposed portions of the etch-stop layer in the plurality of openings and exposing at least a portion of the conductive layer of each step; and
- forming a plurality of conductive structures in each of the plurality of openings.

Ex. 1001 ('276 Patent), Claim 1

'276 Patent, Fig. 6

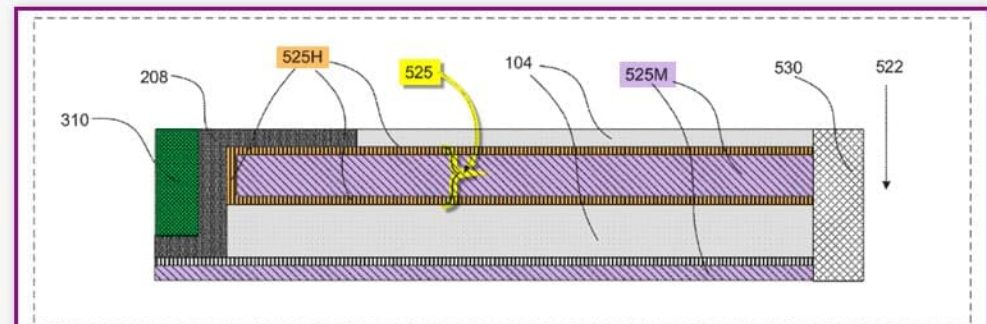
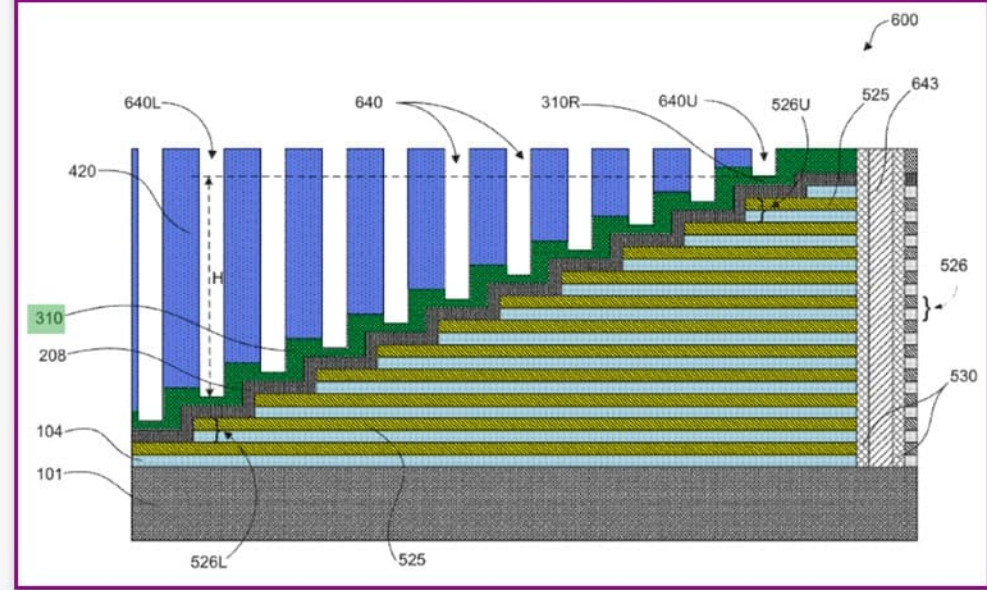
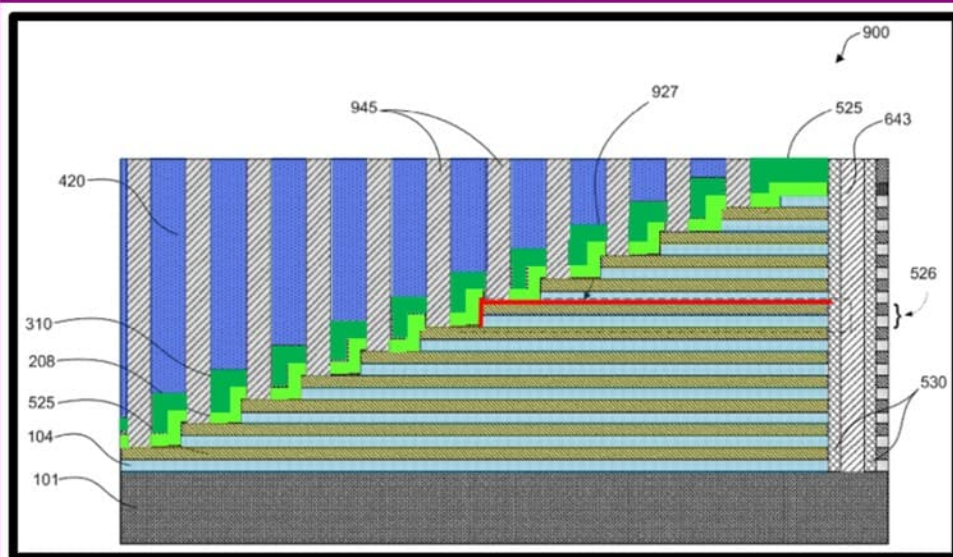


FIG. 5B

POR 11; Ex. 1001 ('276 Patent), Figs. 6, 5B (annotated)

Claim 1: “each step...comprises disposing a sacrificial layer over a dielectric layer; ...replacing the sacrificial layer...with a gate stack”

'276 Patent, Fig. 9A



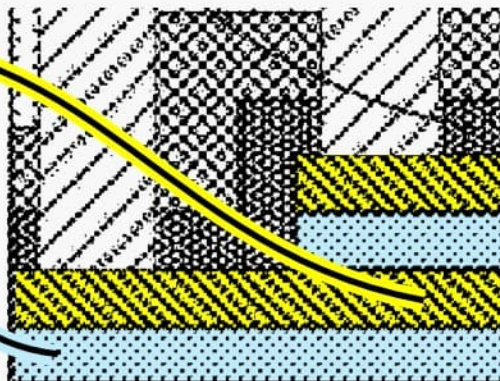
POR 13-14; Ex. 1001 ('276 Patent), Fig. 9A (annotated)

525

gate stack

104

dielectric layer



1. A method for forming a semiconductor structure, comprising:

forming a staircase structure having a plurality of steps, wherein the forming of each step of the plurality of steps comprises disposing a sacrificial layer over a dielectric layer;

disposing an etch-stop layer on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer;

disposing an insulating layer on the etch-stop layer;

replacing the sacrificial layer of each step with a gate stack, the gate stack comprising a conductive layer and a first high-k dielectric layer;

forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer;

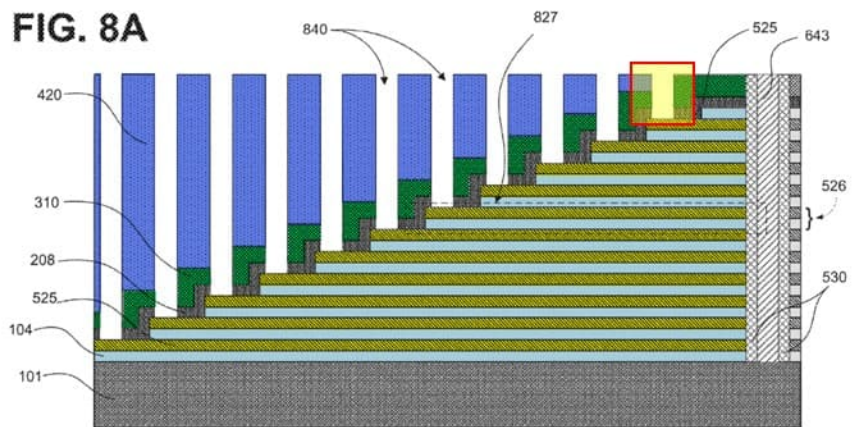
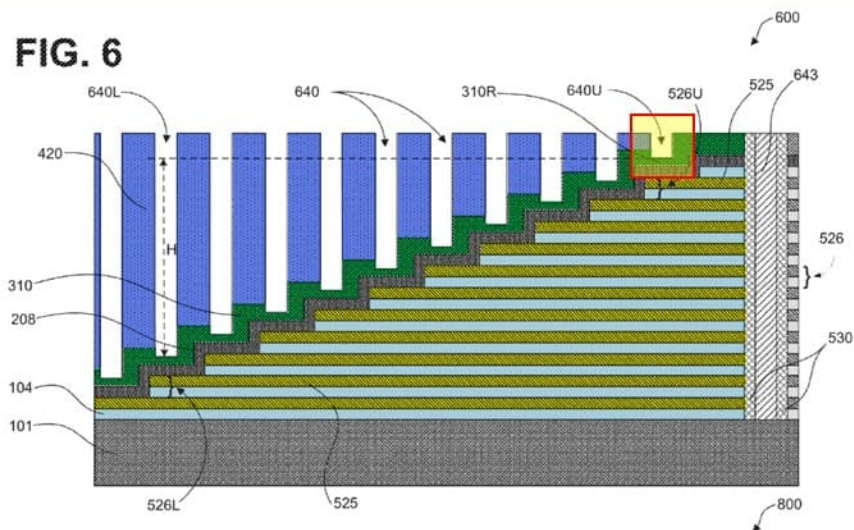
etching the exposed portions of the etch-stop layer in the plurality of openings and exposing at least a portion of the conductive layer of each step; and

forming a plurality of conductive structures in each of the plurality of openings.

Ex. 1001 ('276 Patent), Claim 1

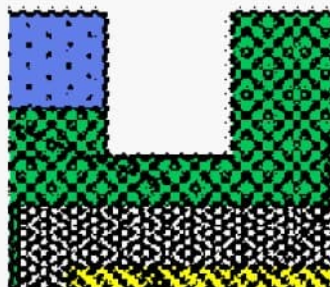
Claim 1: “exposing portions of the etch-stop layer” And “etching the exposed portions”

'276 Patent, Figs. 6, 8A

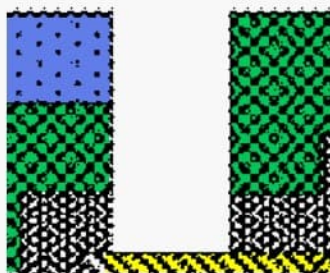


POR 11; Ex. 1001 ('276 Patent), Figs. 6, 8A (annotated)

exposed



etched-through



1. A method for forming a semiconductor structure, comprising:

forming a staircase structure having a plurality of steps, wherein the forming of each step of the plurality of steps comprises disposing a sacrificial layer over a dielectric layer;

disposing an etch-stop layer on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer;

disposing an insulating layer on the etch-stop layer;

replacing the sacrificial layer of each step with a gate stack, the gate stack comprising a conductive layer and a first high-k dielectric layer;

forming a plurality of openings in the insulating layer

exposing portions of the etch-stop layer;

etching the exposed portions of the etch-stop layer in the plurality of openings and exposing at least a portion of the conductive layer of each step; and

forming a plurality of conductive structures in each of the plurality of openings.

Ex. 1001 ('276 Patent), Claim 1



'276 Patent

Ground 1 (Kim) Fails

- I. No Gate-Stack-On-Top (Claims 1-18)
- II. No “exposing” And “etching” Steps (Claims 1-18)
- III. No Showing For Additional Dependent Claims (Claims 4, 5, 11)

Ground 2 (Kim + Fang) Fails

Ground 3 (Han + Fang) Fails

Ground 4 (Han + Fang + Chen) Fails



'276 Patent

Ground 1 (Kim) Fails

I. No Gate-Stack-On-Top (Claims 1-18)

II. No “exposing” And “etching” Steps (Claims 1-18)

III. No Showing For Additional Dependent Claims (Claims 4, 5, 11)

Ground 2 (Kim + Fang) Fails

Ground 3 (Han + Fang) Fails

Ground 4 (Han + Fang + Chen) Fails

Ground 1:

1. A method for forming a semiconductor structure, comprising:

forming a staircase structure having a plurality of steps,
wherein the forming of each step of the plurality of
steps comprises disposing a sacrificial layer over a
dielectric layer;

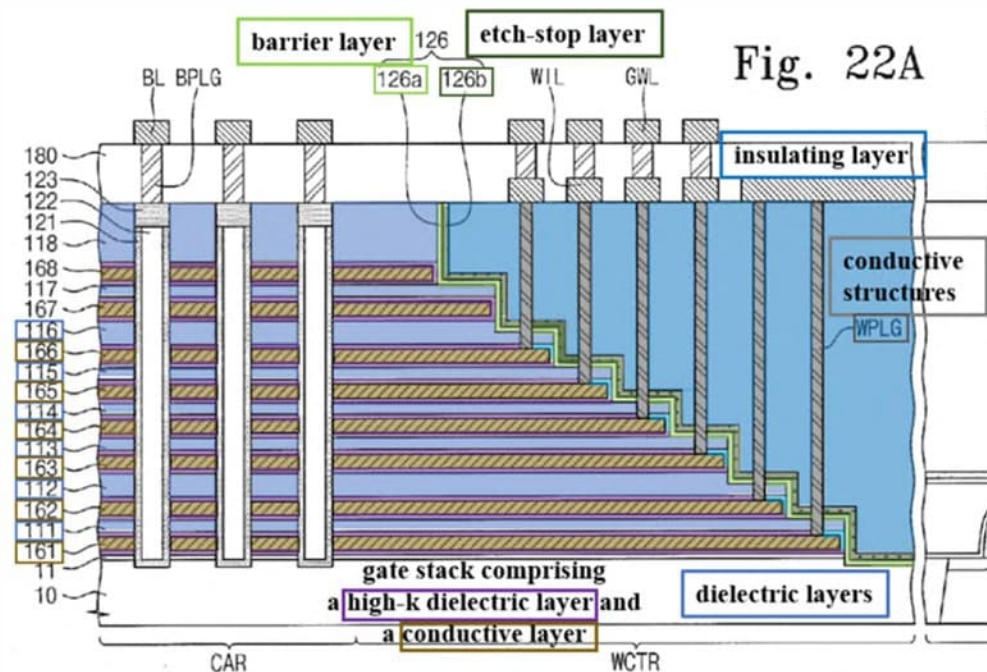
Ex. 1001 ('276 Patent), Claim 1

Petition

Grounds 1 and 2 rely on Kim's Figures 17A-22B embodiment comprising an etch-stop layer and a barrier layer. Kim discloses other embodiments, *e.g.*, Figures 5A-14B.

Pet. 31

Petition



**Pet. 27; Ex. 1005 (Kim), Figs. 17A-22B
(annotated by Petitioner)**

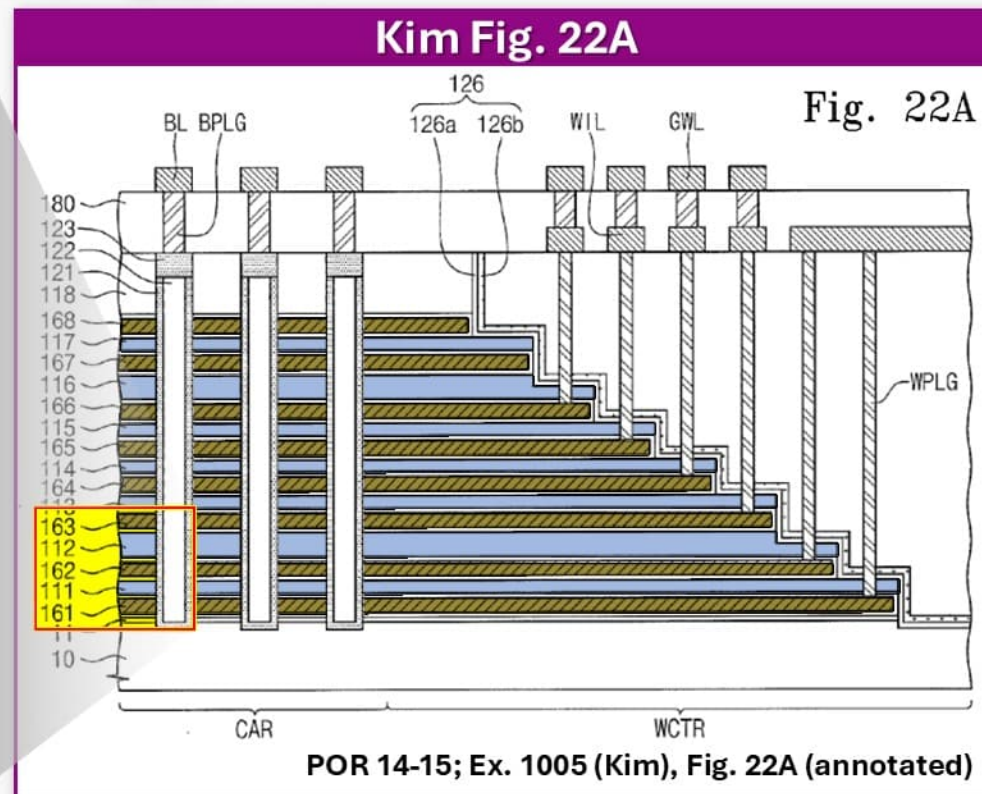
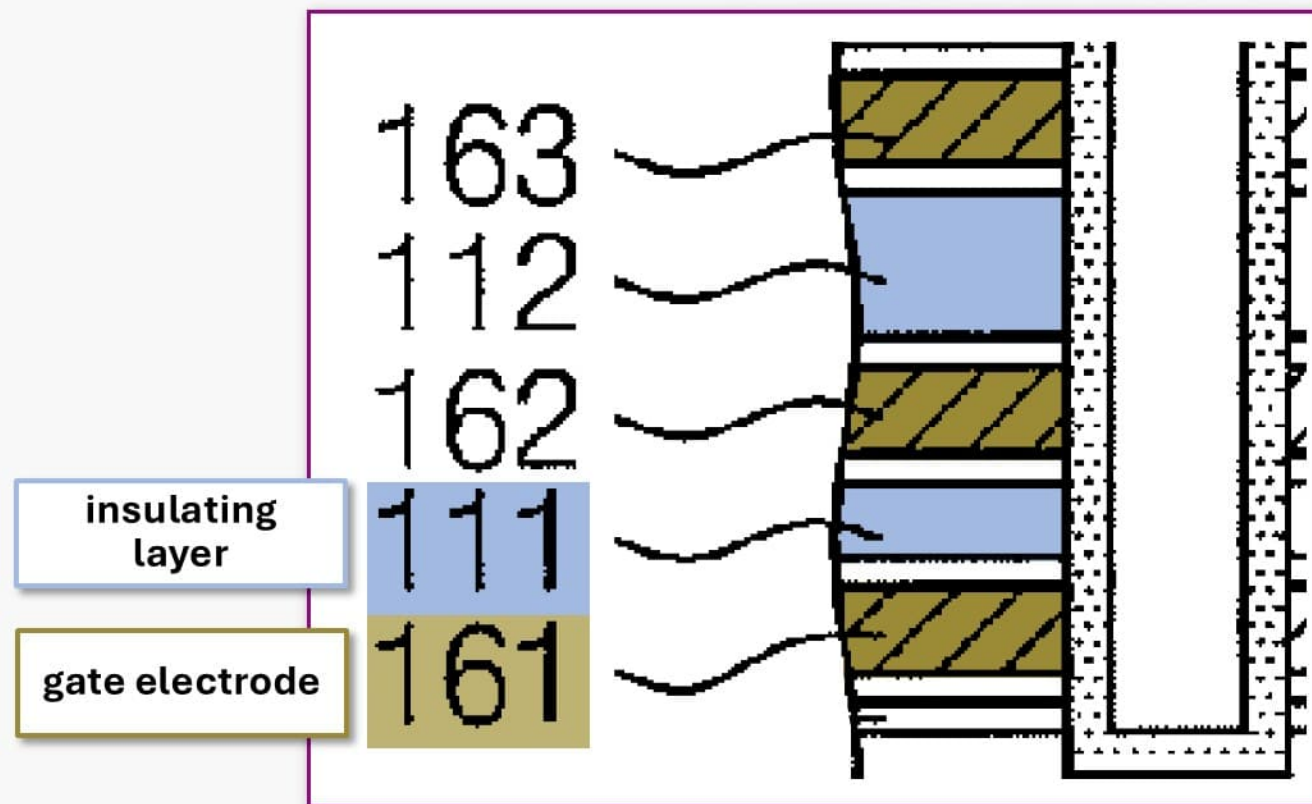


Ground 1: Kim's Figs. 17A-22B Embodiment Is Gate-Stack-On-Bottom

1. A method for forming a semiconductor structure, comprising:

forming a staircase structure having a plurality of steps, wherein the forming of each step of the plurality of steps comprises disposing a sacrificial layer over a dielectric layer;

Ex. 1001 ('276 Patent), Claim 1

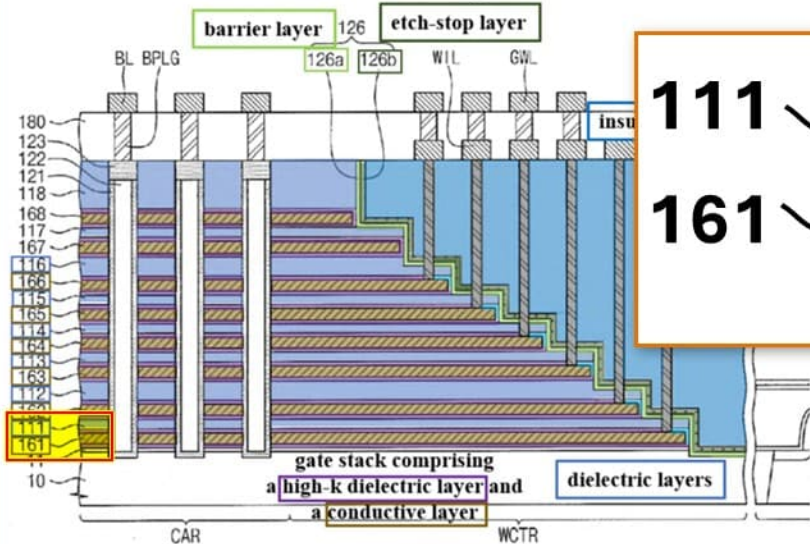




Ground 1: Petitioner's Hindsight Modification Of Kim's Figs. 17A-22B Embodiment

Petition

Fig. 22A



Pet. 27; POR 15-16; Ex. 1005 (Kim), Figs. 22A

111

161

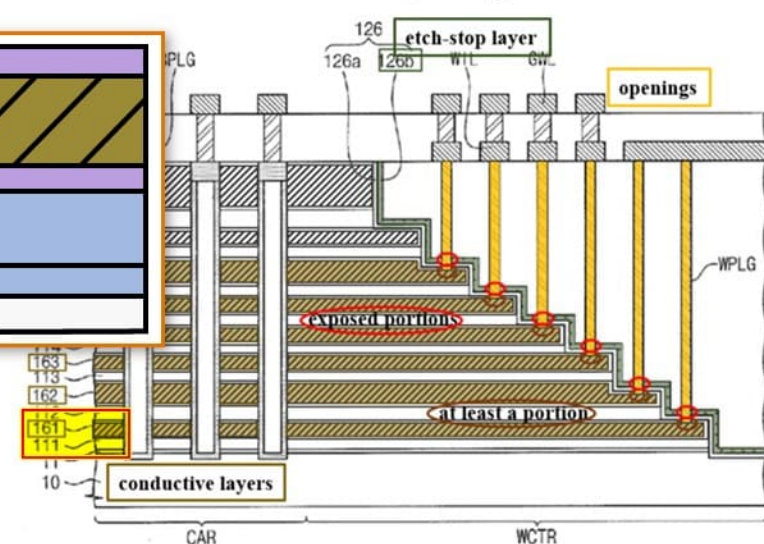
161

111

demonstrative graphics

Petition

Gate-Stack-on-Top Fig. 22A



Pet. 39-49 (modified by Petitioner)

Petition

Kim discloses the sacrificial-layer-on-top/gate-stack-on-top ordering even though its figures show the opposite order. §IX.A. This teaching of the gate-stack-

Pet. 32; Ex. 1003 (Banerjee Pet. Decl.) ¶ 83



A Motivation Is Required To Combine Embodiments From A Single Reference



Micron Technology v. Netlist

“The Board then concluded that Micron failed to address these differences when arguing that a skilled artisan would be motivated to combine these references. There is no legal error here.... Central to the motivation-to-combine inquiry is consideration of fundamental differences between the references. Here, the Board properly considered the differences between Figures 2 and 4 when assessing Micron’s motivation-to-combine argument.”

Micron Tech., Inc. v. Netlist, Inc., 2026 WL 480156, *5 (Fed. Cir. Feb. 20, 2026) (non-precedential) (citations omitted); see also *In re Stepan Co.*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017)

Ground 1: Insufficient Motivation To Modify Kim's Figs. 22A

Petition

Additionally, a POSITA would have known that either order was a common

alternative. For example, Chen discloses both orders side-by-side:

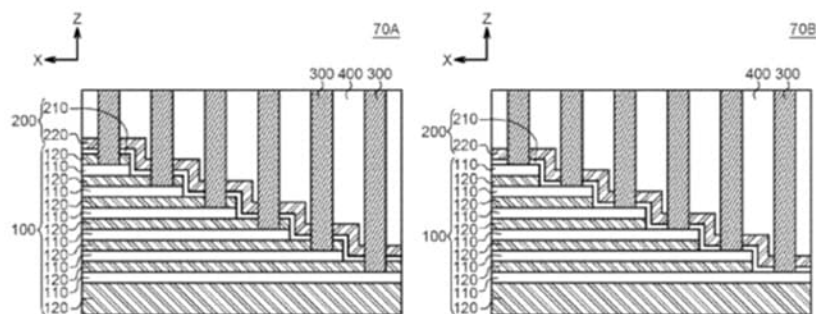


FIG. 7A

FIG. 7B

Chen, Figs. 7A (dielectric on top), 7B (conductor on top), [0044]-[0046]. Yu also

teaches that the layers may be formed in either order. Ex. 1009, [0034]-[0035]. A

POSITA would have known that either order was routine, highly predictable, and

would have had a reasonable expectation of success for implementing a gate-stack-

on-top embodiment.

At a minimum, Kim's teaching on reversing the order represents a "known

technique" that is at least "a *suitable* option" for the Figure 17A-22B embodiment.

Pet. 33



Adidas AG v. Nike

"The obviousness inquiry does not merely ask whether a skilled artisan could combine the reference, but instead asks whether 'they would have been motivated to do so.'"

Adidas AG v. Nike, Inc., 963 F.3d 1355, 1359 (Fed. Cir. 2020) (citation omitted)



Petitioner Identified No Benefit To Reversing Layers

Petitioner's Expert Dr. Banerjee

Q. All right. Now, in your declaration you don't list any benefits to reversing the order of the layers; right?

A. I don't think so. I mean, I cited to other prior arts such as Chen showing that it could go either way it's. A binary choice. Either the gate stack is going to be on top or below and Chen shows two figure side-by-side so it's a matter of simple choice, you can see that.

Q. It's a matter of simple choice, but there's no reason you give to go one way or the other; right?

A. No, I did not.

Ex. 2021 (Banerjee Dep., '711 Pat.), 35:12-36:1



Intel Is Distinguishable

Petitioner



Intel

“That Kabemoto and Bauman address the same problem and that Bauman’s cache was a known way to address that problem is precisely the reason that there’s a motivation to combine under *KSR* and our precedent.”

Intel Corp. v. PACT XPP Schweiz AG, 61 F.4th 1373, 1380 (Fed. Cir. 2023)

Patent Owner



CommScope

“Petitioner *has not* identified a need or problem known in the field of endeavor at the time of invention or explained how Fukushima helped address that problem.”

CommScope, Inc. v. TQ Delta, LLC, IPR2022-01012, 2023 WL 7491179, *11 (P.T.A.B. Nov. 13, 2023) (Paper 31) (original emphasis)



Petitioner's "problem" Is Mere Attorney Argument

Petitioner's Reply

Here, the motivation is stronger than in *Intel*. 3D staircases in either layer
order provide isolated gate stacks, meeting the demand for higher-density memories.

Reply 3 (citing *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1381 (Fed. Cir. 2023))



Kim's Fig. 22A Materially Differs From Other Embodiments

Fig. 22A shows and describes the gate-stack-on-*bottom*

Pet. 32; POR 15-16; Ex. 1005 (Kim), [0185]-[0187]

Fig. 22A has two etch-stop layers.

POR 19

Fig. 22A has high-k dielectric layer surrounding conductive layer of each step.

Pet. 44; POR 21, 37-38, 47-48; POSR 13-14

Distinct materials result in different etch chemistries and safety margins.

POR 29-30, 48

Boston Scientific Is Distinguishable

U.S. Patent No. 5,545,208 From *Boston Scientific*

FIG. 3B

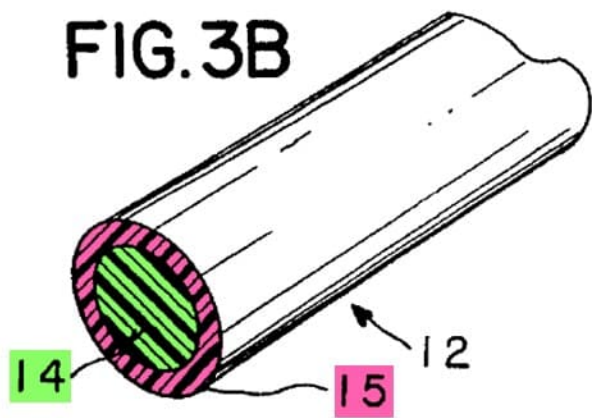
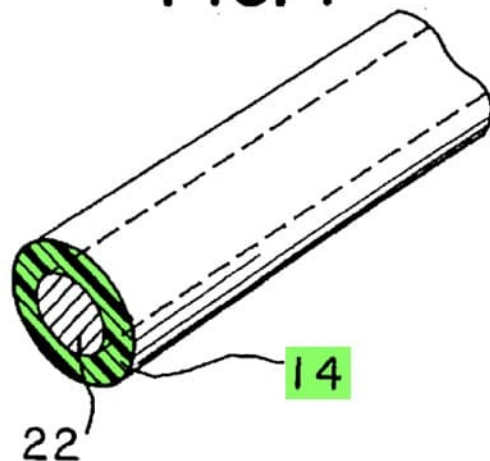


FIG. 4



'208 Patent, Figs. 3B, 4

Boston Scientific

“One of ordinary skill would have been motivated to coat the metal stent of figure 4, including its **layer 14** of drug-containing polymer, with a second layer of polymer, like **layer 15** depicted in figure 3B, that is substantially free of an elutable material.

Just as the stent in figure 3B benefits from the two layers, one containing a drug and the other limiting diffusion of the drug, so would the stent in figure 4 benefit from the same two coating layers.”

Bos. Sci. Scimed, Inc. v. Cordis Corp., 554 F.3d 982, 991 (Fed. Cir. 2009)

Kim Figs. 17A-22B Is Gate-Stack-On-Bottom

Petition

A POSITA would have understood that descriptions of one of Kim's embodiments apply to other embodiments except where the embodiments differ.

Banerjee ¶¶ 80-81. Closely related embodiments with many of the same elements are denoted by the same reference numerals. Kim, [0184]. For example, the embodiments shown in Figures 5A-14B and in Figures 17A-22B are closely related.

Thus, Kim states that overlapping descriptions of the same elements are omitted in the descriptions of Figures 17A-22B. *Id.* Further, the descriptions of Figures 17A-

Pet. 32



No Reasonable Expectation Of Success Because Of Thin Conductive And Insulating Layers In Modified Kim

Thin conductive layers

Increased risk of punch-through

Higher electrical resistance

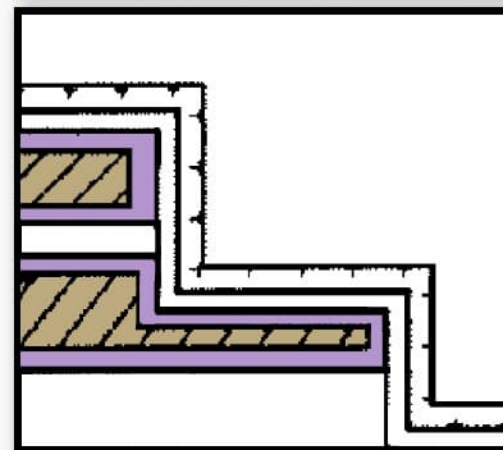
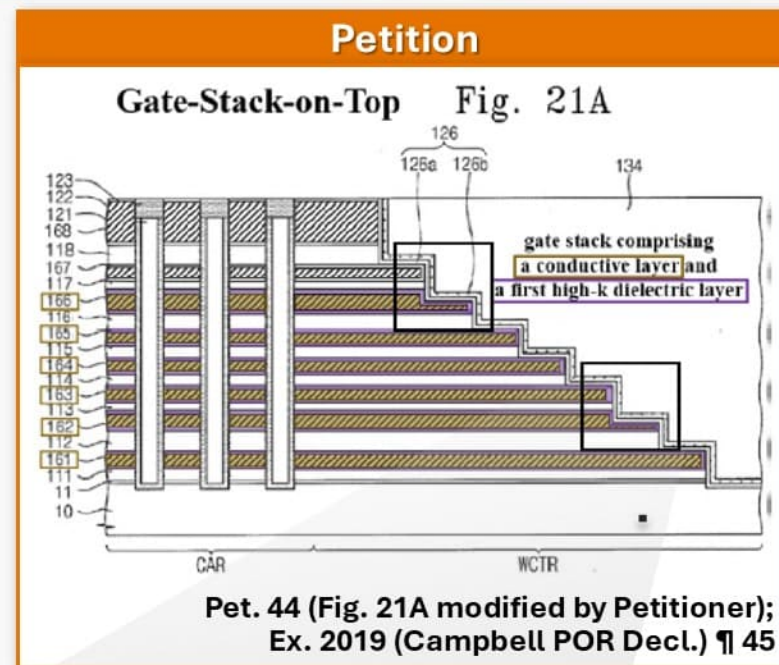
Increased risk of incomplete sacrificial layer replacement

Increased risk of cavity collapse during sacrificial layer replacement

Increased risk of open circuits/holes in conductive material

Thin sandwiched insulating layers

Increased risk of leakage from high voltage



POR 20-21



Additional Reasons A POSITA Would Not Have Had A Reasonable Expectation Of Success

Different etch depths

POR 22-23

Change to etch parameters

POR 29; Ex. 2019 (Campbell POR Decl.) ¶¶ 50-53

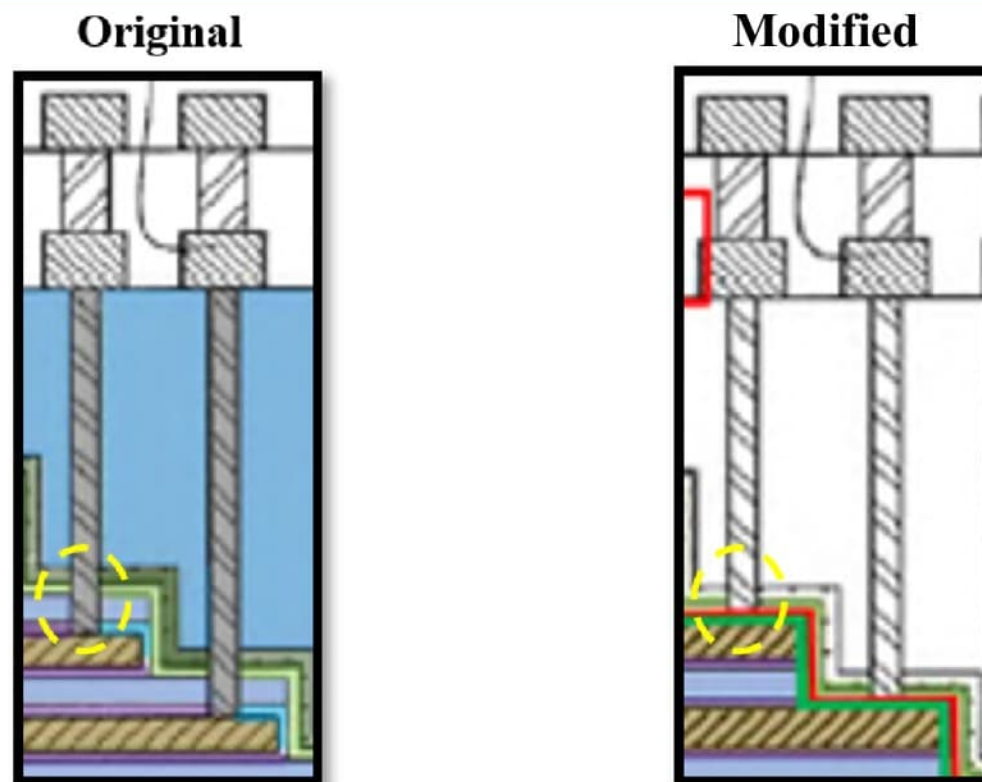
Increased risk of short circuiting

POR 20-24, 29-30

Petitioner's expert said "details matter"

Ex. 2021 (Banerjee Dep., '711 Pat.), 45:9-12

Dr. Campbell POR Declaration



Ex. 2019 (Campbell POR Decl.) ¶ 46



'276 Patent

Ground 1 (Kim) Fails

I. No Gate-Stack-On-Top (Claims 1-18)

II. No “exposing” And “etching” Steps (Claims 1-18)

III. No Showing For Additional Dependent Claims (Claims 4, 5, 11)

Ground 2 (Kim + Fang) Fails

Ground 3 (Han + Fang) Fails

Ground 4 (Han + Fang + Chen) Fails



Construction Of “exposing” And “etching” Steps

Portions of the etch-stop layer are exposed *before* they are etched.

1. A method for forming a semiconductor structure, comprising:

* * *

forming a plurality of openings in the insulating layer
exposing portions of the etch-stop layer;
etching the exposed portions of the etch-stop layer in the
plurality of openings and exposing at least a portion of
the conductive layer of each step; and

Ex. 1001 ('276 Patent), Claim 1

1. Exposing and Etching are separate steps.

POR 8-13

2. Supported by plain language.

POR 8-10

3. Supported by written description.

POR 10-13

4. Combining steps render etch-step superfluous.

POR 9-10

5. Undisputed by Petitioner.

Reply 1-2

forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer;

etching the exposed portions of the etch-stop layer in the plurality of openings and exposing at least a portion of the conductive layer of each step; and

FIG. 6

600

640L

640

310R

640U

526U

525

643

420

H

310

208

104

101

526L

525

526

530

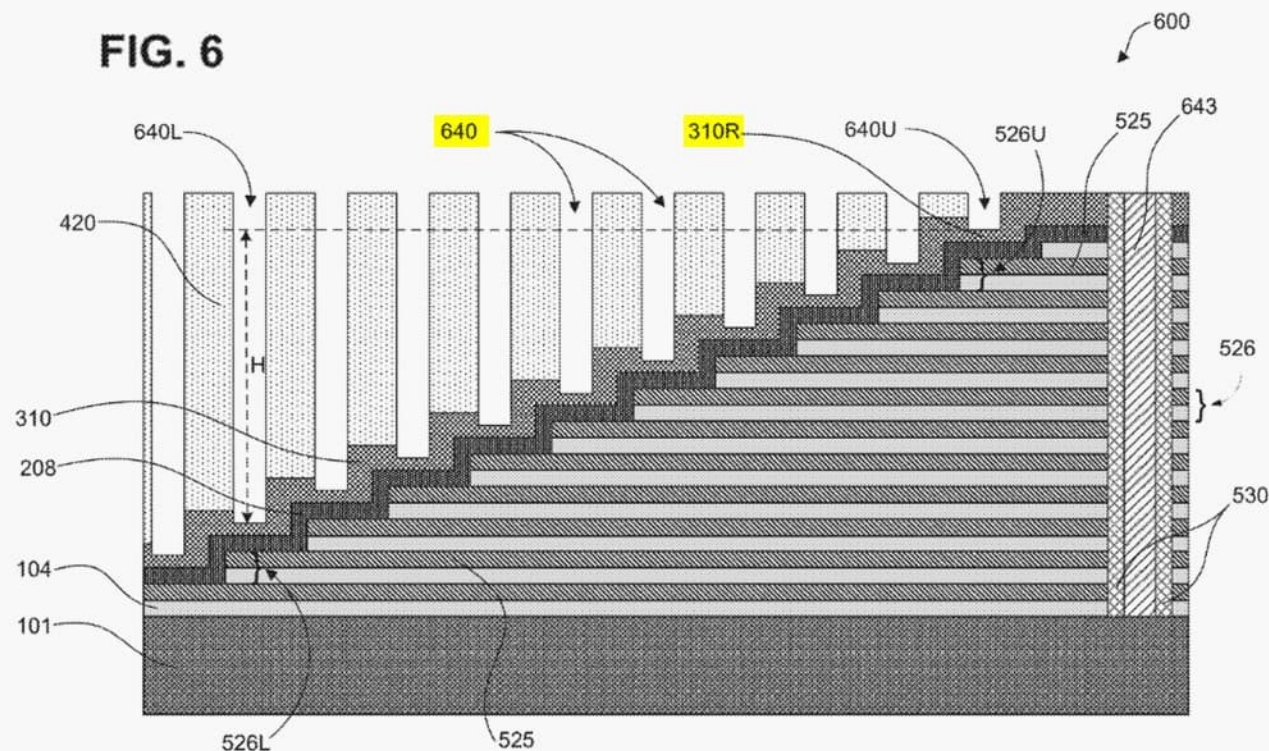
[illegible]

27

Written Description Confirms “exposing” Step Is Distinct From “etching” Step

During the one or more etching processes that form the VIA openings 640, the etch-stop layer 310 protects the underlying structure until all the VIA openings 640 are formed throughout the staircase structure 600. For example, a VIA opening 640L for a lower replacement SC layer 526L requires longer etch time than a VIA opening 640U for an upper replacement SC layer 526U. An additional thickness H of the third insulating layer 420 needs to be removed. The etch-stop layer 310 can protect underlying materials of the replacement SC layers 526 on upper levels, before the VIA openings 640 are formed for the replacement SC layers 526 on lower levels. For example, during the removal process of the extra thickness H of third insulating layer 420, the etch-stop layer 310 on top of the upper replacement SC layer 526U is not etched through, with a remaining etch stop layer 310R. The remaining etch-stop layer 310R provides protection for the replacement SC layers 526U, where the VIA openings 640U are already formed. The staircase structure

Ex. 1001 ('276 Patent), 10:2-19



Ex. 1001 ('276 Patent), Fig. 6



Combining The “exposure” And “etching” Steps Renders The “etching” Step Superfluous



Mformation Technologies v. Research in Motion

“We are persuaded by BlackBerry's argument that the **separate sub-step** for establishing a connection would become ‘superfluous’ if we concluded that a connection did not have to be established (completed) **before transmission**.”

Mformation Techs., Inc. v. Rsch. in Motion Ltd., 764 F.3d 1392, 1399 (Fed. Cir. 2014)



Petitioner Does Not Dispute Distinct “exposing” And “etching” Steps

Petitioner's Reply

II. CLAIM CONSTRUCTION

PO contends that claim 1's limitations “exposing portions of the etch-stop layer” and “etching the exposed portions” are distinct. POR, 8–13. Petitioner never suggested otherwise, but instead explained how Kim discloses these two distinct steps. Pet., 46–49; Banerjee2 ¶¶11–12. Because there is no dispute, no construction is necessary. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019).

Reply 1-2

Kim Does Not Disclose Exposing Portions Of The Etch-Stop Layer Before Etching The Exposed Portions

Kim

[0173] In some embodiments, the formation of word line contact plugs WPLG and peripheral contact plugs PPLG may include forming contact holes to penetrate the interlayer insulating pattern 134 in the word line contact region WCTR and the peripheral circuit region C/P, and filling the contact holes with a conductive material. Since the gate structure GP has a stepwise structure in the word line contact region WCTR, the word line contact plugs WPLG can be connected to the gate electrodes 161 to 168 located at different levels from each other, using the same process. The peripheral contact plugs PPLG may be connected to the peripheral circuits. In some embodiments, the word line contact plugs WPLG and the peripheral contact plugs PPLG may be formed of a metallic material (e.g., tungsten). The formation of the word line contact plugs WPLG and the peripheral contact plugs PPLG may include sequentially forming a barrier metal layer (e.g., a metal nitride layer) and a metal layer (e.g., a tungsten layer).

[0174] In the case that the data storing layer 150 and the gate separation insulating layer 170 are removed on the interlayer insulating pattern 134, the word line contact plugs WPLG and the peripheral contact plugs PPLG may be formed to penetrate the interlayer insulating pattern 134. Otherwise, as shown in FIG. 14A, the word line contact plugs WPLG and the peripheral contact plugs PPLG may be formed to penetrate the gate separation insulating layer 170, the data storing layer 150 and the interlayer insulating pattern 134.

Ex. 1005 (Kim), [0173]-[0174]

Kim

[0213] In other embodiments, the semiconductor patterns 121 and the contact pads 123 on the cell array region CAR may be formed after forming the interlayer insulating pattern 134. In this case, after forming the stacked layer structure ST, the etch stop layer 125 may be formed to conformally cover the stacked layer structure ST. The etch stop layer 125 may be formed of a material having an etch selectivity with respect to the interlayer dielectric 130. Thereafter, the interlayer dielectric 130 may be formed on the etch stop layer 125 and then planarized until a top surface of the etch stop layer 125 is exposed on the cell array region CAR.

Ex. 1005 (Kim), [0213]



'276 Patent

Ground 1 (Kim) Fails

- I. No Gate-Stack-On-Top (Claims 1-18)
- II. No “exposing” And “etching” Steps (Claims 1-18)
- III. No Showing For Additional Dependent Claims (Claims 4, 5, 11)**

Ground 2 (Kim + Fang) Fails

Ground 3 (Han + Fang) Fails

Ground 4 (Han + Fang + Chen) Fails

Petitioner Relies On A POSITA's Knowledge



DSS Technology Management v. Apple

“[T]here are at least three caveats to note in applying ‘common sense’ in an obviousness analysis of [a patent claim]....First, common sense is typically invoked to provide a known *motivation to combine*, not to supply a missing claim limitation....Second, common sense is invoked to fill in a *missing* limitation only when ‘the limitation in question was unusually simple and the technology particularly straightforward.’...Third,...references to ‘common sense’— whether to supply a motivation to combine or a missing limitation—cannot be used as a wholesale substitute for reasoned analysis and evidentiary support....”

DSS Tech. Mgmt., Inc. v. Apple Inc., 885 F.3d 1367, 1374 (Fed. Cir. 2018) (original emphasis)



Virtek Vision International v. Assembly Guidance Systems

“The mere fact that these possible arrangements existed in the prior art does not provide a reason that a skilled artisan would have substituted the one-camera angular direction system in Keitler and Bridges with the two-camera 3D coordinate system disclosed in Briggs.”

Virtek Vision Int’l ULC v. Assembly Guidance Sys., Inc., 97 F.4th 882, 887-88 (Fed. Cir. 2024)



Ground 1: Claim 4 Would Not Have Been Obvious

4. The method of claim 1, wherein etching the exposed portions of the etch-stop layer comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer of each step.

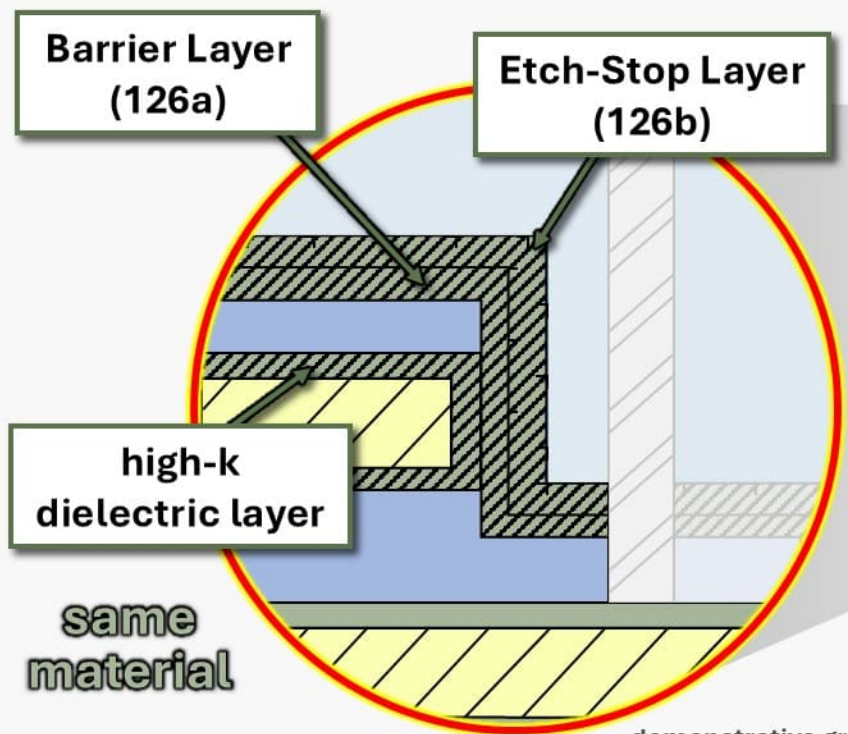
Ex. 1001 ('276 Patent), Claim 4

- **Petitioner cites no disclosure in Kim for rendering the additional requirements of claim 4 obvious**

Ground 1: Claim 5 Would Not Have Been Obvious

5. The method of claim 4, wherein etching the exposed portions of the etch-stop layer further comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the first high-k dielectric layer.

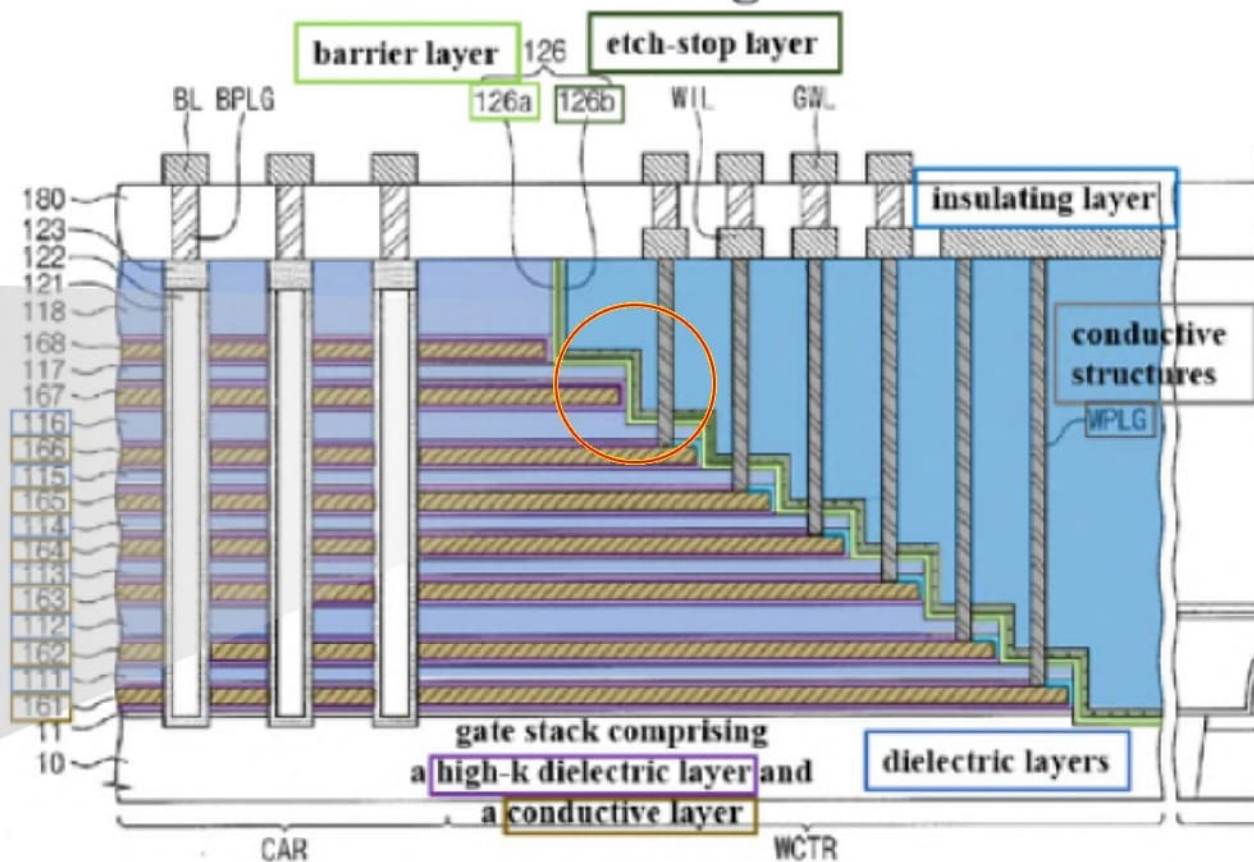
Ex. 1001 ('276 Patent), Claim 5



demonstrative graphic

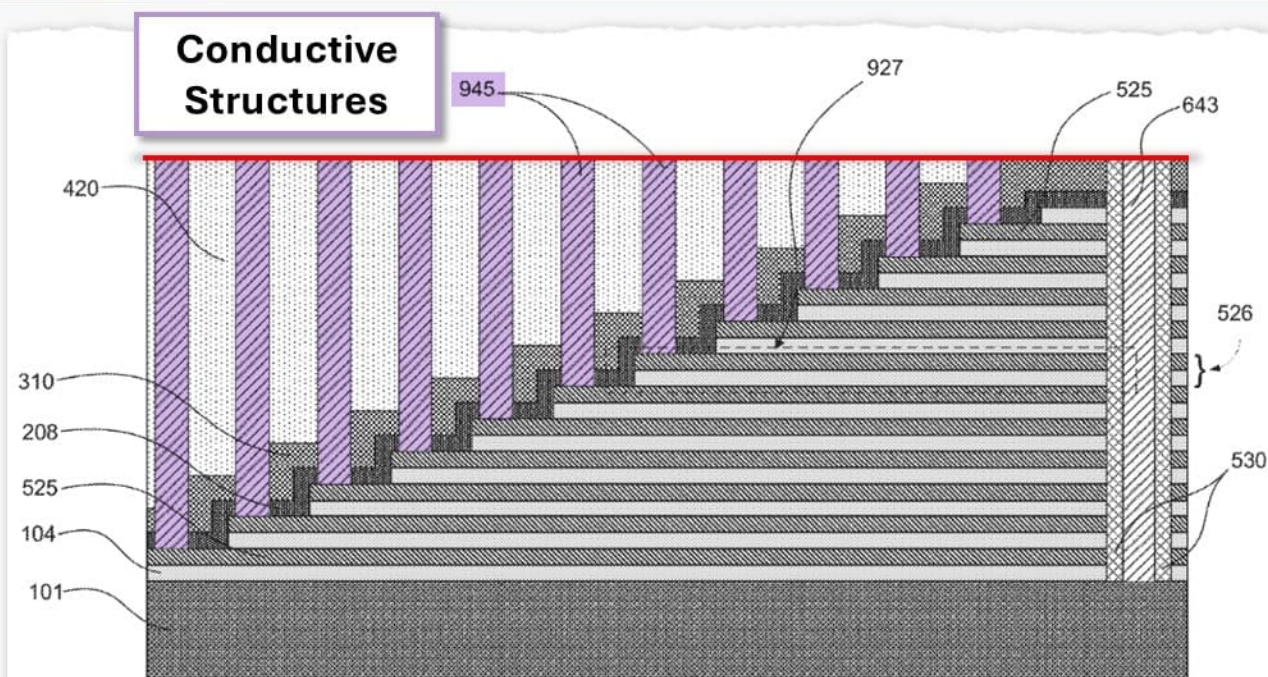
Patent Owner's Response

Fig. 22A



POR 29; Ex. 1005 (Kim), Fig. 22A

Ground 1: Kim Does Not Disclose Claim 11's Limitation



Ex. 1001 ('276 Patent), Fig. 9A (annotated)

Filling and polishing a conductive material in the VIA openings and forming connection to each corresponding conductive layer of the gate stack on the staircase structure

1090

Ex. 1001 ('276 Patent), Fig. 10 (excerpted)

11. The method of claim 1, wherein forming the plurality of conductive structures further comprises planarizing the conductive materials and the insulating layer.

Ex. 1001 ('276 Patent), Claim 11

At process step 1090, VIA conductive structures are formed by disposing and filling a third conductive material in all the VIA openings in the structure. The VIA conductive structure can be the VIA conductive structures 945 in FIGS. 9A and 9B. The third conductive material can be planarized subsequently to form a coplanar surface with the top surface of the third insulating layer. The planarization process includes chemical mechanical polishing (CMP). Residual conductive materials outside the VIA openings can be removed by touch-up dry etching or wet etching. As a result, the conductive material in the VIA openings is connected with the conductive material of the gate stack for each level of the staircase structure. Therefore, the embedded gates of the vertically stacked 3D memory cells can be electrically connected from a planar surface on the top of the structure in the subsequent back-of-line processes, enabling various configurations of word lines for the 3D memory array.

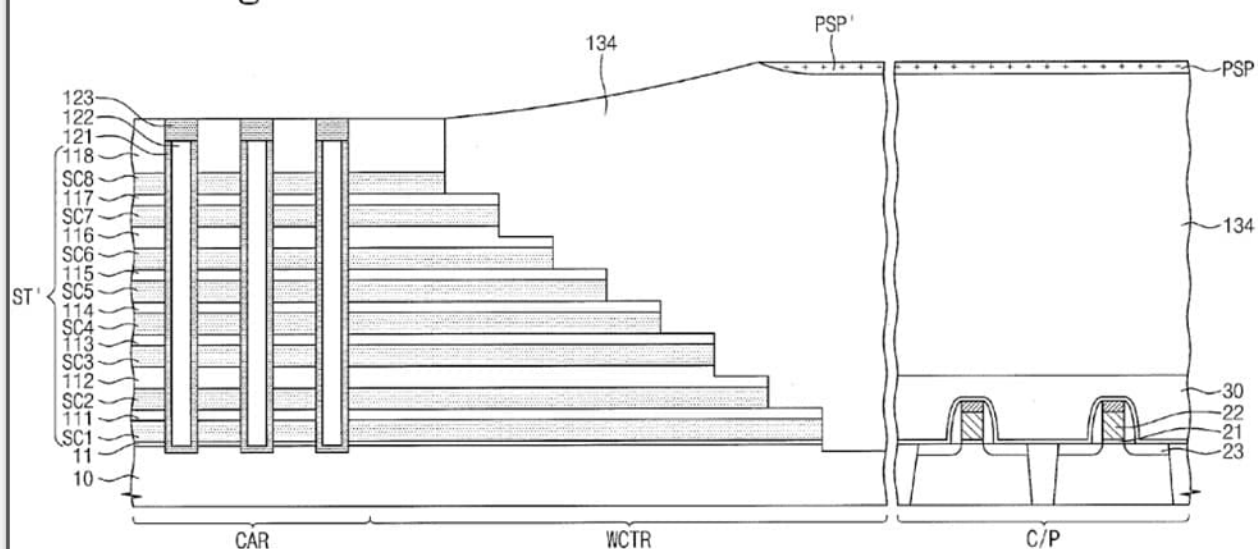
Ex. 1001 ('276 Patent), 13:17-33

Ground 1: Kim Does Not Disclose Claim 11's Limitation

Paragraph [0119] of Kim does not disclose “planarizing the conductive materials” of the conductive structures.

Kim, Fig. 11A

Fig. 11A



Pet. 56-57; Ex. 1005 (Kim), Fig. 11A

Kim [0019]

[0119] In some embodiments, the interlayer insulating pattern 134 may be formed to expose the stacked layer structure ST' and the top surfaces of the contact pads 123 on the cell array region CAR. The polishing stop layer PSL may prevent the interlayer dielectric 130 on the peripheral circuit region C/P and the word line contact region WCTR from being excessively polished during the polishing of the interlayer dielectric 130. In other embodiments, the contact pads 123 of the cell array region CAR may be formed after the formation of the interlayer insulating pattern 134. In this case, the polishing process of the interlayer dielectric 130 may be performed to expose the top surface of the semiconductor pattern 121 on the cell array region CAR.

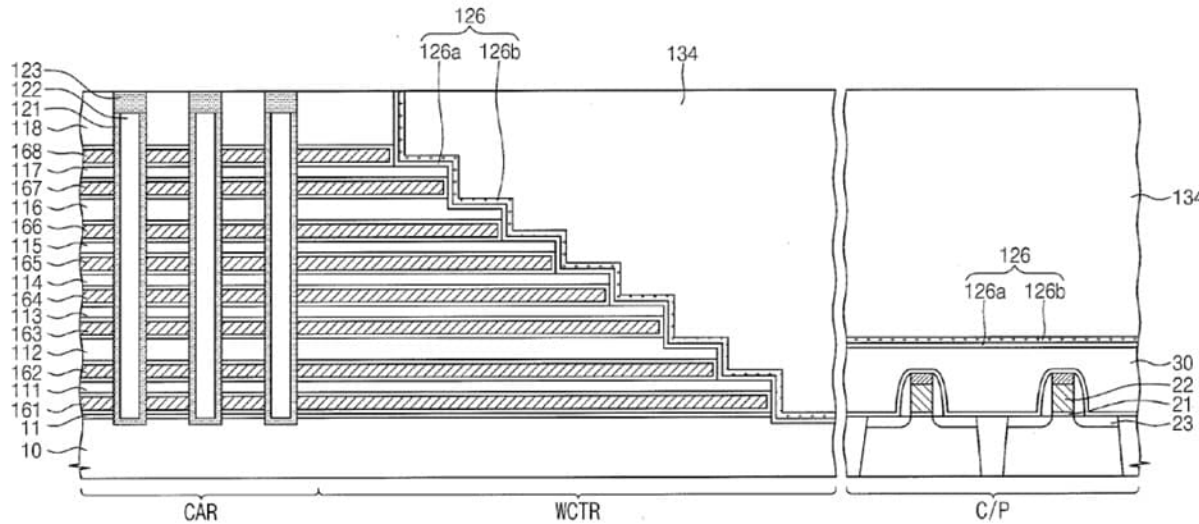
Pet. 56-57; Ex. 1005 (Kim), [0119]

Ground 1: Kim Does Not Disclose Claim 11's Limitation

Paragraphs [0206] and [0209] of Kim do not disclose “planarizing the conductive materials” of the conductive structures.

Kim, Fig. 11A

Fig. 21A



Pet. 56-57; Ex. 1005 (Kim), Fig. 21A

Kim [0206], [0209]

[0206] For instance, the formation of the trench spacer **154** may include forming an insulating layer to conformally cover an inner wall of the trench **140** and anisotropically etching the insulating layer to expose a top surface of the doped region **15**. The data storing layer on the doped region **15** may be removed during trench the formation of the trench spacer **154**.

The formation of the vertical conductive pattern **156** may include forming a metal layer in the trench **140** provided with the trench spacer **154** and etching the metal layer using a planarization method. The etching of the metal layer may be performed to remove the data storing layer **150** and the etch stop layer **125** and to expose top surfaces of the contact pads **123**.

* * *

[0209] Referring to FIGS. **22A** and **22B**, an interconnection structure including contact plugs WPLG, PPLG and BPLG and interconnection lines WIL, GWL and BL may be formed.

Pet. 56-57; Ex. 1005 (Kim), [0206], [0209]



'276 Patent

Ground 1 (Kim) Fails

Ground 2 (Kim + Fang) Fails

Ground 3 (Han + Fang) Fails

Ground 4 (Han + Fang + Chen) Fails



Ground 2: A POSITA Would Not Have Been Motivated To Combine Fang's Etch-stop Characteristics Or Contract-hole Etching To Kim

1. A method for forming a semiconductor structure, comprising:

* * *

disposing an etch-stop layer on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer;

* * *

3. The method of claim 2, wherein the etching process comprises anisotropic dry etching.

Ex. 1001 ('276 Patent), Claims 1, 3

6. The method of claim 1, wherein disposing the etch-stop layer comprises disposing hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, and/or any combination thereof.

7. The method of claim 1, wherein disposing the etch-stop layer comprises disposing the etch-stop layer with a thickness in a range between 10 nm to 100 nm.

8. The method of claim 1, wherein disposing the etch-stop layer comprises performing chemical vapor deposition (CVD), physical vapor deposition (PVD), sputtering, atomic layer deposition (ALD), spin-coating, or any combination thereof.

Ex. 1001 ('276 Patent), Claims 6-8

Petitioner Relied On Fang's CDSN Etch Stop, Which Is Not In Kim

Petition

If more is required (it is not), Kim in view of Fang renders claim 7 obvious. Fang discloses an analogous semiconductor structure with an etch-stop layer. Fang, Fig. 6, [0020]. To start, Kim's and Fang's etch-stop layers are similar. For example, both of their etch-stop layers may comprise silicon nitride. Kim, [0187]; Fang, [0022]. And Fang's alternative (a high-k dielectric) is applicable to Kim. §XI.C.1. Pet. 68; Ex. 1003 (Banerjee Pet. Decl.) ¶¶ 140-141

Kim

125a. In some embodiments, the first stop layer **125a** may be formed of silicon oxide and the second stop layer **125b** may be formed of silicon nitride. In other embodiments, the etch stop layer **125** may be a single layer, which is formed of a material having an etch selectivity with respect to the sacrificial layers SC1 to SC8 and the insulating layers 111 to 118.

Ex. 1005 (Kim), [0187]

Fang

[0022] The etch stop material **130** may be a carbon-doped silicon nitride including from about 1 wt % of carbon to about 30 wt % of carbon, such as from about 1 wt % of

Ex. 1006 (Fang), [0022]

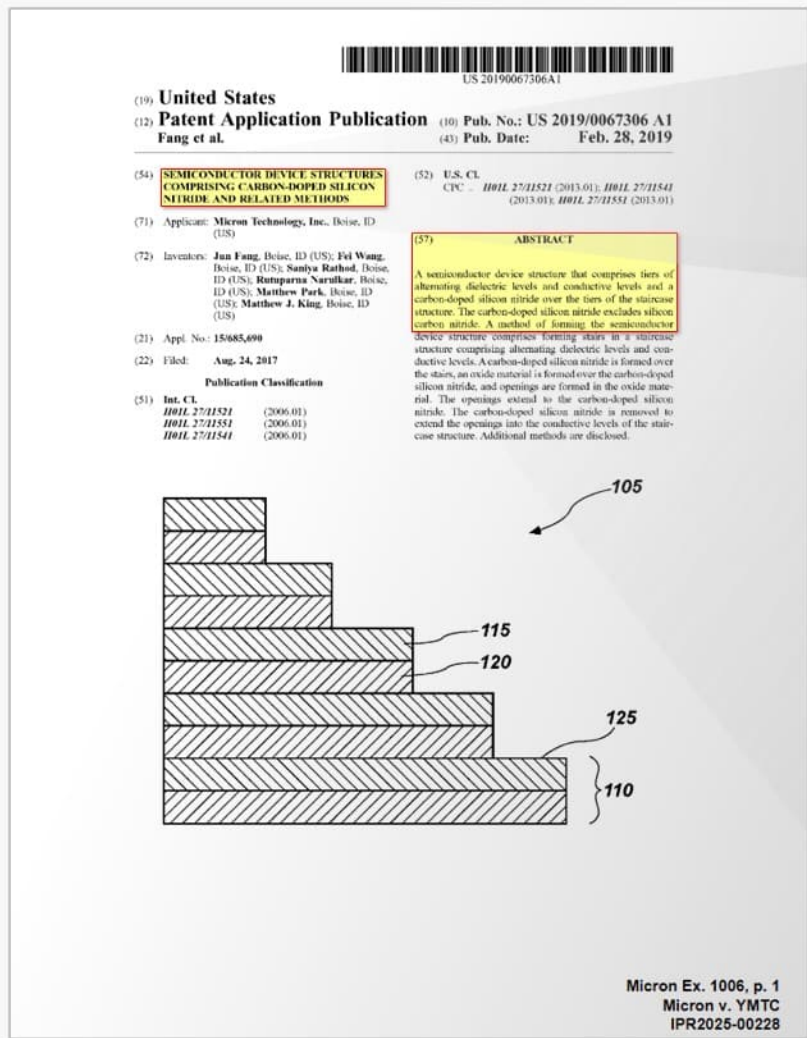
Fang Discloses CDSN Etch-Layer

SEMICONDUCTOR DEVICE STRUCTURES COMPRISING CARBON-DOPED SILICON NITRIDE AND RELATED METHODS

(57)

ABSTRACT

A semiconductor device structure that comprises tiers of alternating dielectric levels and conductive levels and a carbon-doped silicon nitride over the tiers of the staircase structure. The carbon-doped silicon nitride excludes silicon carbon nitride. A method of forming the semiconductor



Ex. 1006 (Fang)



Undisputed That Etch Rate Depends On Materials Composition

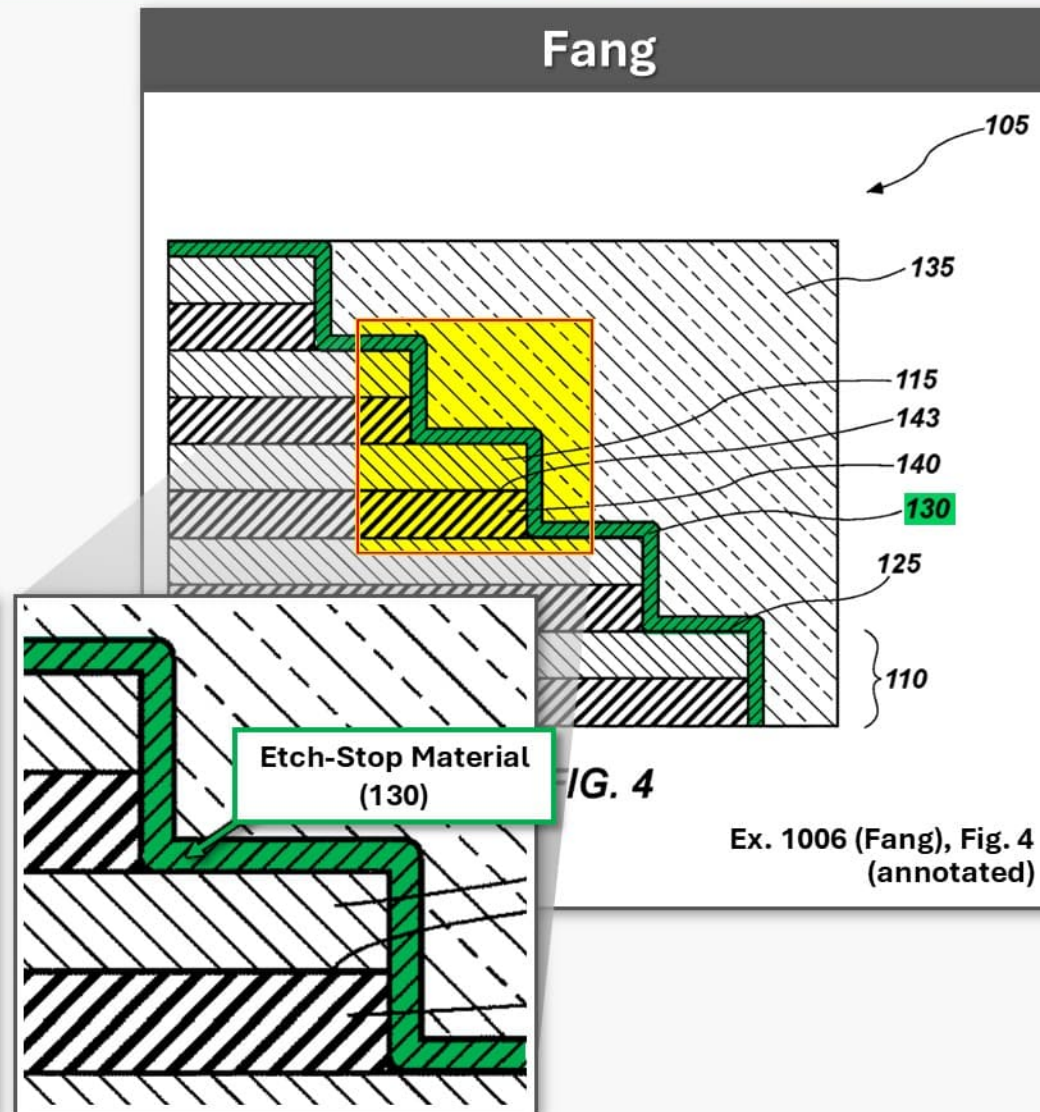
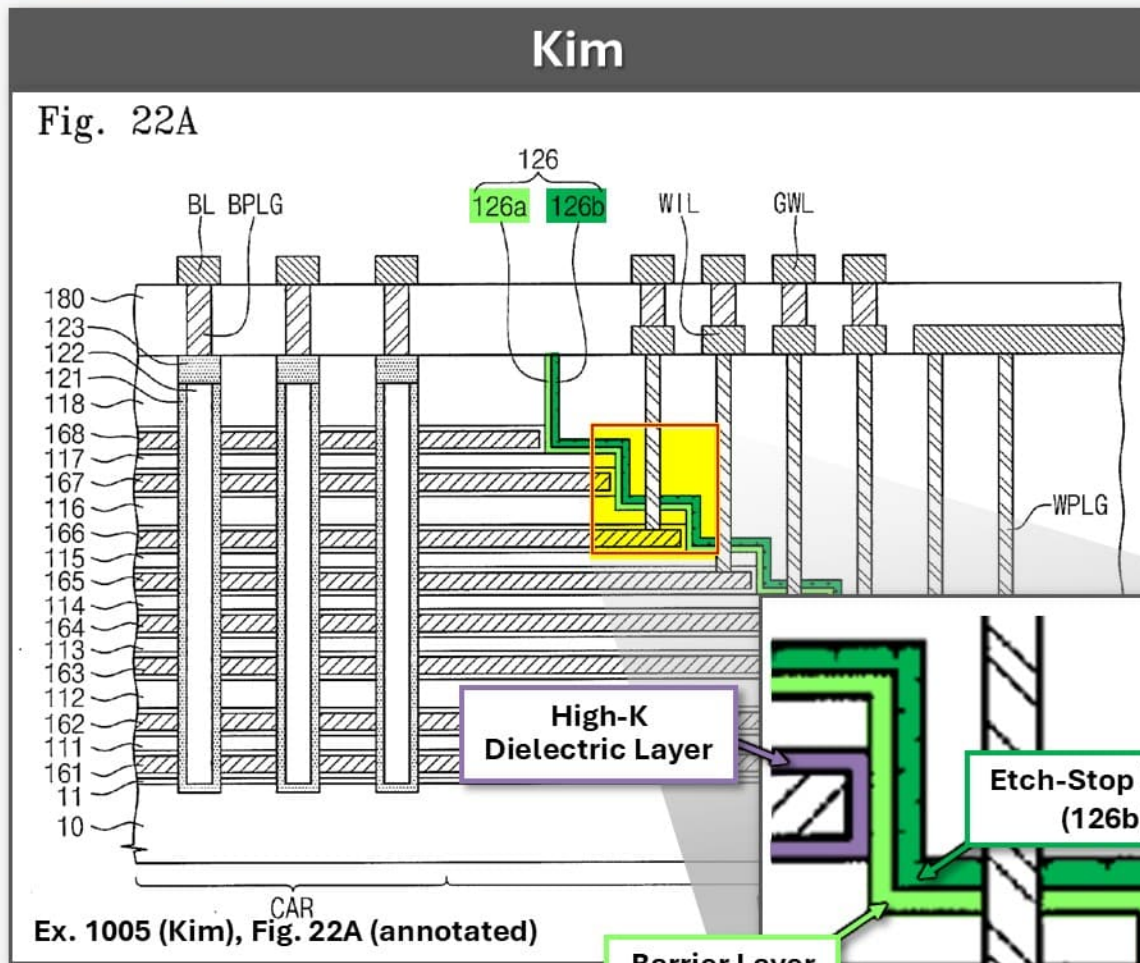
Petitioner's Expert

Q. Is it fair to say that the carbon doping has an impact on the etch rate of the silicon nitride?

A. It could. If you left everything else the same in the etch process, changing the composition in general will change the etch rate.

Ex. 2021 (Banerjee Dep., '711 Pat.), 55:4-9

Material Differences In Kim And Fang's Layer Structures





Petitioner Also Relied On Fang's "alternative" Material, Which Is Not In Kim

Petition

Kim in view of Fang renders obvious claim 6. Specifically, Fang discloses that *the etch-stop layer* may comprise silicon nitride or, "[a]lternatively, ... a high-k dielectric material, such as *hafnium oxide*." Fang, [0022]. Both alternatives would material when removing the sacrificial layers. *Id.*, [0025]. Kim also discloses silicon nitride as a material for the etch-stop layer. Kim, [0186]. Thus, applying Fang's "alternative[]" to silicon nitride (Fang, [0022]) represents nothing more than applying the same alternative toward Kim's "similar device[]" in the same way."

Intel, 61 F.4th at 1380; Banerjee ¶ 139.

Pet. 67-68

Kim

[0186]

* * *

In some embodiments, the etch stop layer 125 may include at least one of silicon carbide (SiC), silicon nitride (SiN), silicon oxynitride (SiON) and/or silicon oxycarbide (SiOC).

Ex. 1005 (Kim), [0186]

Fang

[0022]

* * *

includes a stoichiometric amount of carbon. Alternatively, the etch stop material 130 may be a high-k dielectric material, such as hafnium oxide.

Ex. 1006 (Fang), [0022]



Kim Does Not Disclose Tunneling Problems And Its Structure Protects Against It

No tunneling problems identified in Kim

High-k dielectric surrounding conductive layer protects against tunneling

Two-etch-stop-layer design protects against tunneling

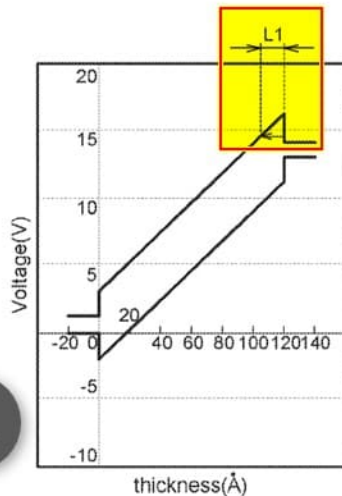


Kim Employs Chen's Disclosed Protections Against Tunneling

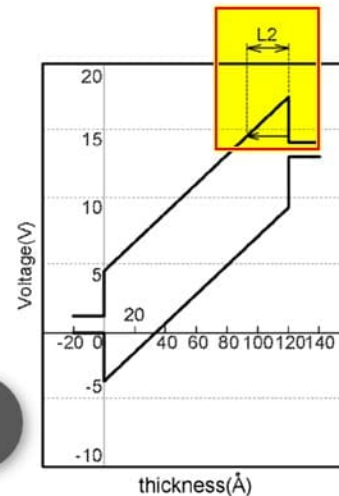
Chen shows that multiple layers where at least one is high-k dielectric reduces tunneling the most

Chen

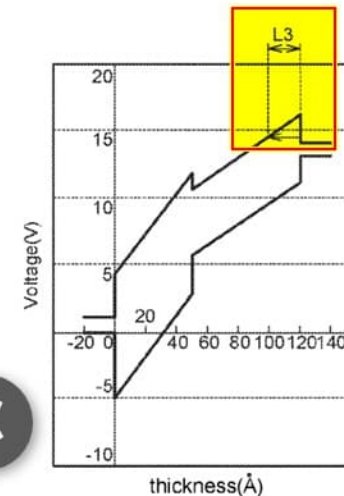
Single-layer:
silicon nitride



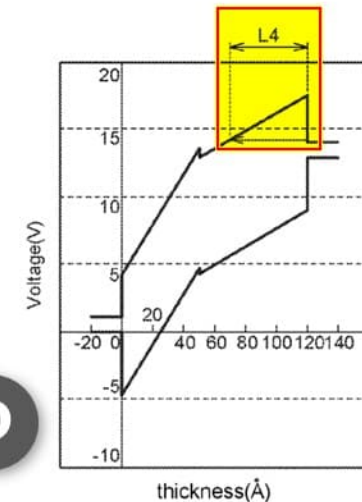
Single-layer:
aluminum oxide
(high-k dielectric)



Double-layer:
silicon oxide + silicon nitride



Double-layer:
silicon oxide + aluminum oxide
(high-k dielectric)



Ex. 1008 (Chen), [0047]-[0053], Figs. 8A-D



'276 Patent

Ground 1 (Kim) Fails

Ground 2 (Kim + Fang) Fails

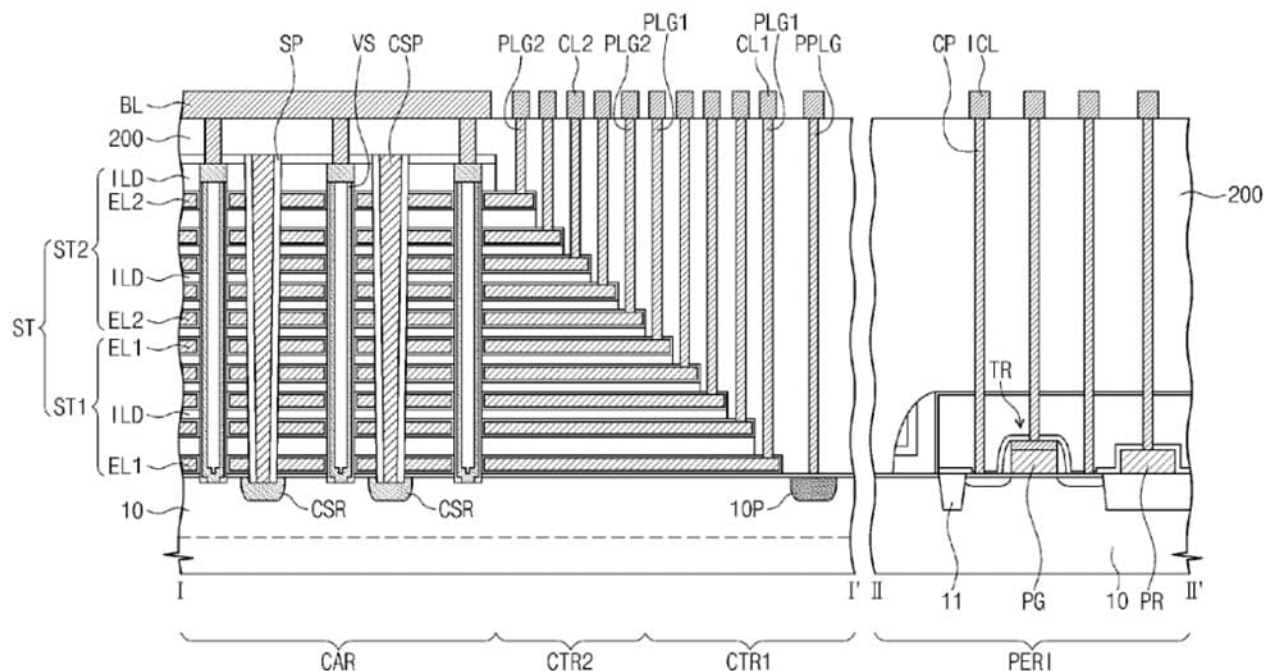
Ground 3 (Han + Fang) Fails

Ground 4 (Han + Fang + Chen) Fails

Ground 3: Petitioner Relies On Han And Fang

Han, Fig. 29

FIG. 29



Ex. 1007 (Han), Fig. 29

disposing an **etch-stop layer** on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer;
disposing an **insulating layer on the etch-stop layer**;

* * *

forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer;
etching the exposed portions of the etch-stop layer in the plurality of openings and exposing at least a portion of the conductive layer of each step; and

Ex. 1001 ('276 Patent), Claim 1

"etch-stop layer"

MISSING

"insulating layer on the etch-stop layer"

MISSING

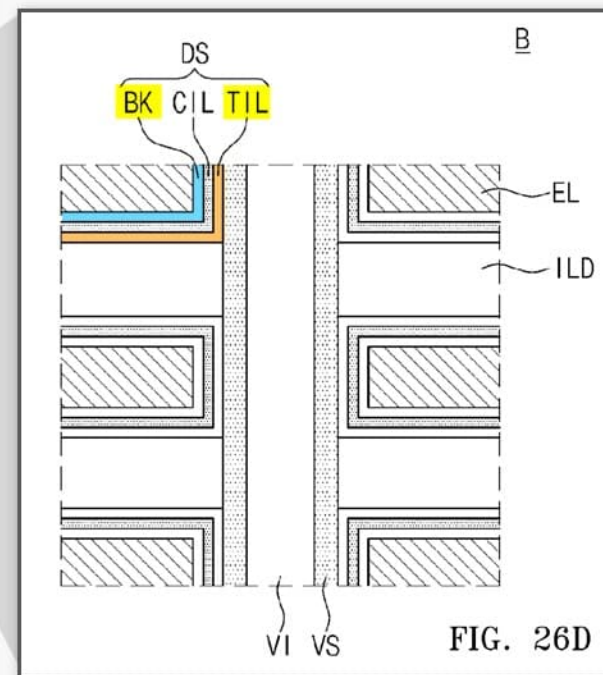
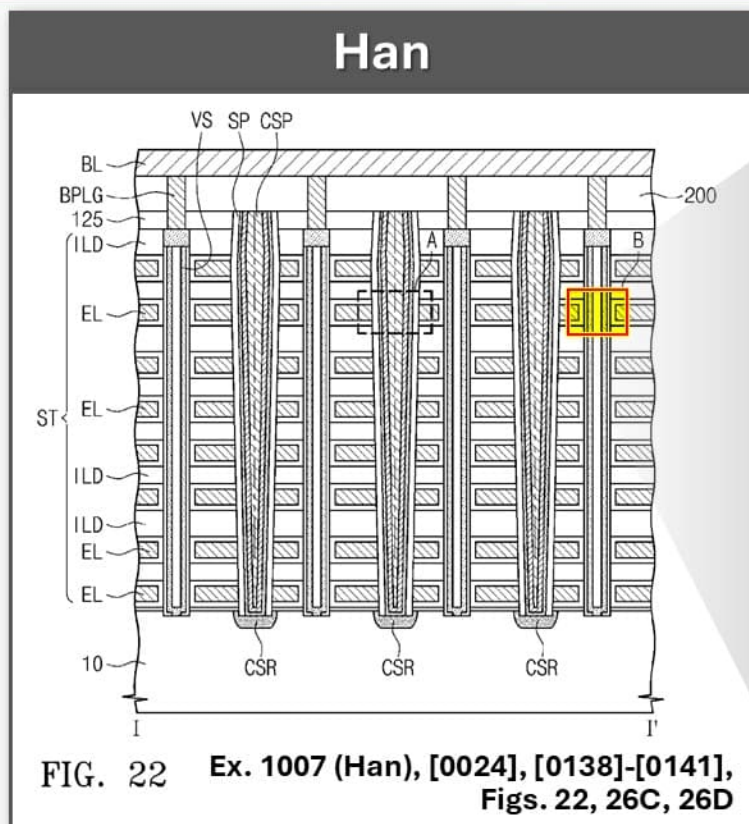
"forming plurality of openings exposing portions of the etch-stop layer"

MISSING

"etching the exposed portions of the etch-stop layer"

MISSING

Han Already Protects Against Punch-through: Multiple High-K Dielectric Layers



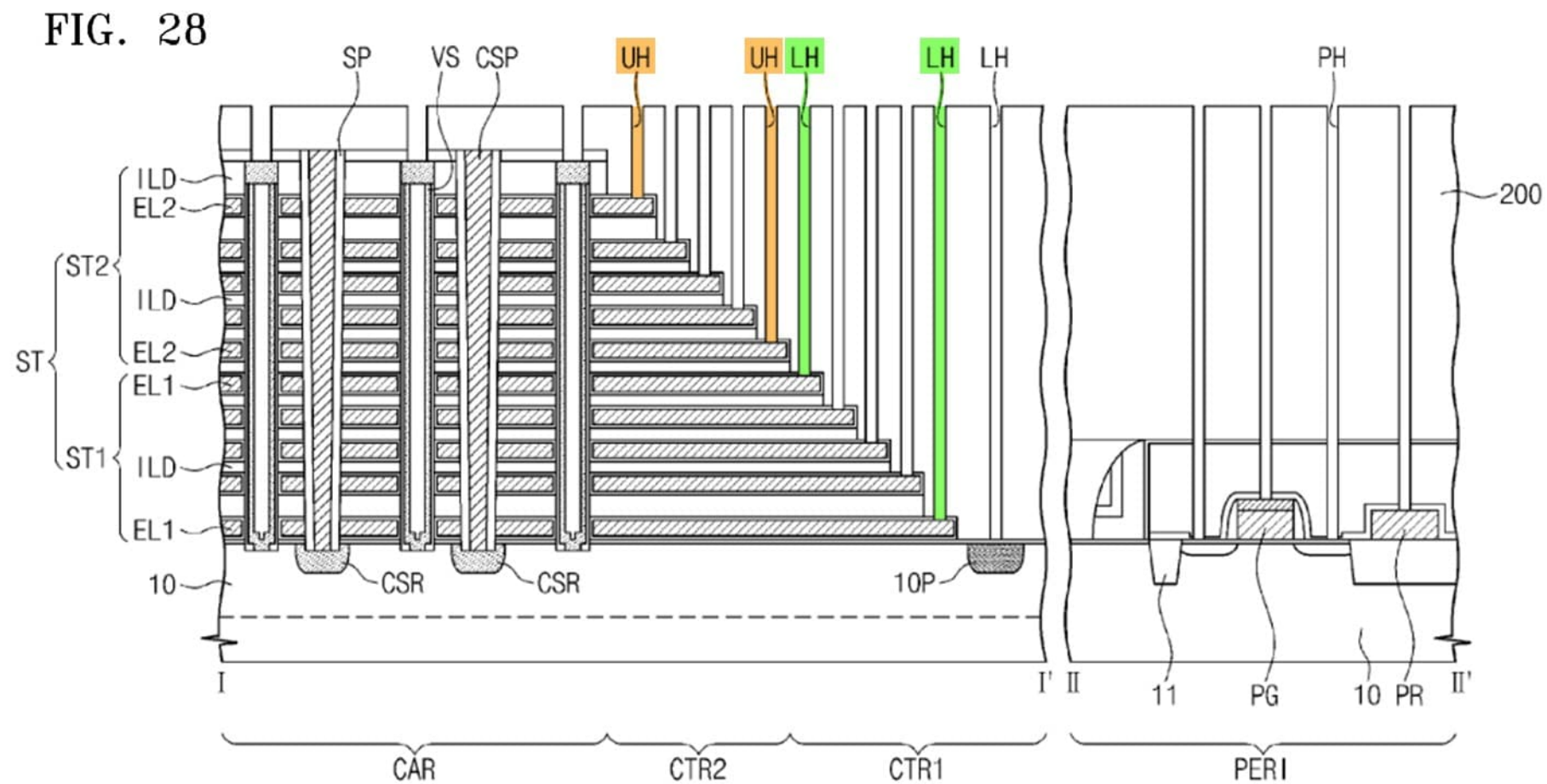
Petitioner's Expert

against such deviations. Accordingly, the first high-k dielectric layer may be advantageously used as an etch stop to protect the conductive layer below. That

Ex. 1003 (Banerjee Pet. Decl.) ¶ 110

Han Already Protects Against Punch-through: Staged Etching

Han, Fig. 28



Ex. 1007 (Han), Fig. 28

Fang's Etch-Stop Layer Is Redundant



South-Tek Systems v. Engineered Corrosion Solutions

“South-Tek only argued that a person of ordinary skill would have been motivated to use Wood’s drain to allow water to drain from Viking’s system. Viking’s system already includes a drum drip drain that serves this purpose. Given the redundant functions of Viking’s drum drip and Wood’s condensate drain, the Board found a person of ordinary skill would not have been motivated to add a condensate drain to Viking in addition to the system’s drum drip drain.”

South-Tek Sys., LLC v. Engineered Corrosion Sols., LLC, 748 F. App’x 1003, 1007 (Fed. Cir. 2018)



Ground 3: As With Ground 1, Claim 4 Would Not Have Been Obvious

4. The method of claim 1, wherein etching the exposed portions of the etch-stop layer comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer of each step.

Ex. 1001 ('276 Patent), Claim 4



DSS Tech. Mgmt. v. Apple

“[T]here are at least three caveats to note in applying ‘common sense’ in an obviousness analysis of [a patent claim]....First, common sense is typically invoked to provide a known *motivation to combine*, not to supply a missing claim limitation....Second, common sense is invoked to fill in a *missing* limitation only when ‘the limitation in question was unusually simple and the technology particularly straightforward.’...Third,...references to ‘common sense’— whether to supply a motivation to combine or a missing limitation—cannot be used as a wholesale substitute for reasoned analysis and evidentiary support....”

DSS Tech. Mgmt., Inc. v. Apple Inc., 885 F.3d 1367, 1374 (Fed. Cir. 2018) (original emphasis)



Virtek Vision International v. Assembly Guidance Systems

“The mere fact that these possible arrangements existed in the prior art does not provide a reason that a skilled artisan would have substituted the one-camera angular direction system in Keitler and Bridges with the two-camera 3D coordinate system disclosed in Briggs.”

Virtek Vision Int’l ULC v. Assembly Guidance Sys., Inc., 97 F.4th 882, 887-88 (Fed. Cir. 2024)



Ground 3: As With Ground 1, Claim 5 Would Not Have Been Obvious

5. The method of claim 4, wherein etching the exposed portions of the etch-stop layer further comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the first high-k dielectric layer.

Ex. 1001 ('276 Patent), Claim 5



DSS Tech. Mgmt. v. Apple

“[T]here are at least three caveats to note in applying ‘common sense’ in an obviousness analysis of [a patent claim]....First, common sense is typically invoked to provide a known *motivation to combine*, not to supply a missing claim limitation....Second, common sense is invoked to fill in a *missing* limitation only when ‘the limitation in question was unusually simple and the technology particularly straightforward.’...Third,...references to ‘common sense’— whether to supply a motivation to combine or a missing limitation—cannot be used as a wholesale substitute for reasoned analysis and evidentiary support....”

DSS Tech. Mgmt., Inc. v. Apple Inc., 885 F.3d 1367, 1374 (Fed. Cir. 2018) (original emphasis)



Virtek Vision International v. Assembly Guidance Systems

“The mere fact that these possible arrangements existed in the prior art does not provide a reason that a skilled artisan would have substituted the one-camera angular direction system in Keitler and Bridges with the two-camera 3D coordinate system disclosed in Briggs.”

Virtek Vision Int’l ULC v. Assembly Guidance Sys., Inc., 97 F.4th 882, 887-88 (Fed. Cir. 2024)



'276 Patent

Ground 1 (Kim) Fails

Ground 2 (Kim + Fang) Fails

Ground 3 (Han + Fang) Fails

Ground 4 (Han + Fang + Chen) Fails

Ground 4: Petitioner Relies On Han, Fang, And Chen

17. The method of claim 1, further comprising: prior to disposing the etch-stop layer, disposing a **barrier layer** on each step of the plurality of steps, wherein the **barrier layer** protects underlying structures during the etching of the exposed portions of the etch-stop layer.

18. The method of claim 17, wherein disposing the **barrier layer** comprises disposing one or more of silicon oxide, silicon oxynitride, silicon nitride, TEOS, aluminum oxide, and silicon oxide incorporated with F, C, N, or H.

Ex. 1001 ('276 Patent), Claims 17, 18

Petition

A POSITA would have been motivated to add Chen's barrier layer to Han's staircase structure with Fang's etch-stop layer.

Pet. 105

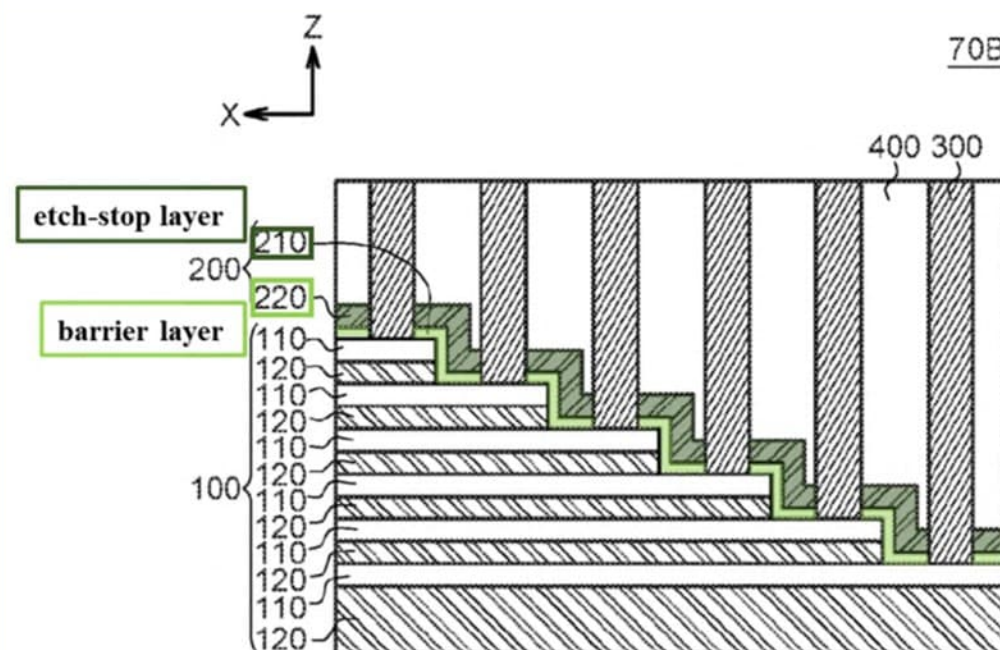


FIG. 7B

Pet. 103-04 (annotating Chen Fig. 7B)



Chen's "stop layer" Exacerbates The Etch-Protection Redundancy In The Han + Fang Combination

1

Multiple high-k dielectric layers surrounding the gate stack.

POR 58

2

Staged Etching process

POR 58

3

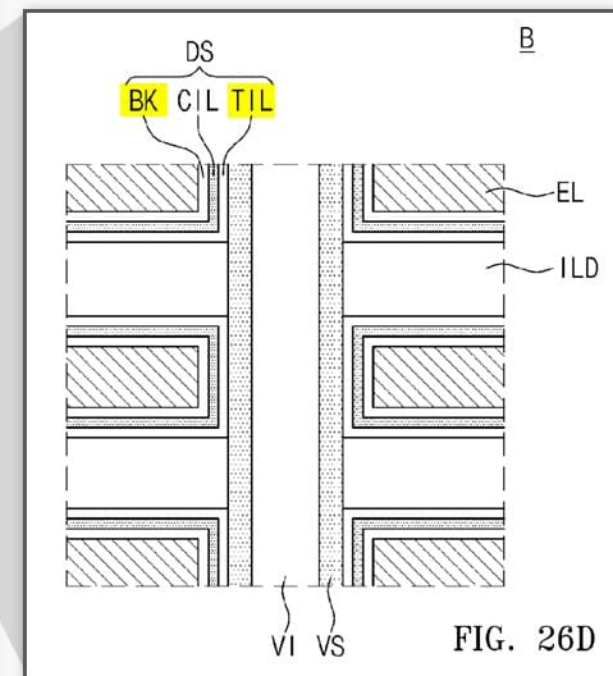
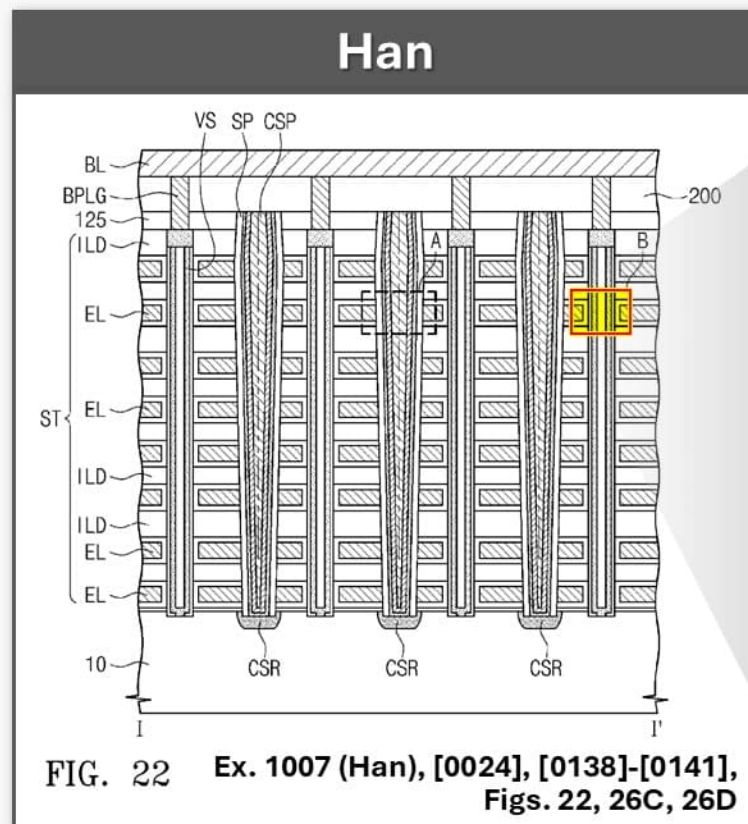
REDUNDANT

Adding Fang's Etch-stop layer

4

REDUNDANT

Adding Chen's "first stop layer"



Chen Discloses Number & Material Of Stop Layers Effect Tunneling For A Constant Thickness

Chen

[0047] FIGS. 8A-8D show curves of applied voltages vs. thicknesses of various etching stop layers according to some embodiments of the present disclosure. In the embodiments

* * *

as shown in FIGS. 8A-8D, the applied voltage is 13V, and the total thickness of the etching stop layer is 120 Å. The elements in the present embodiment sharing similar or the same labels with those in the previous embodiment are similar or the same elements, and the description of which is omitted.

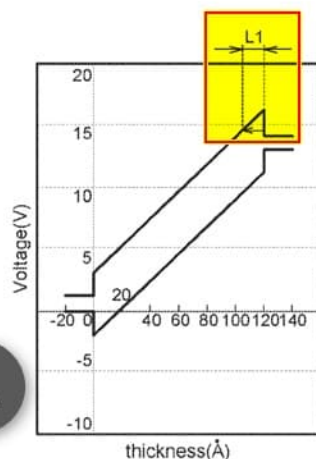
Ex. 1008 (Chen), [0047]

Chen

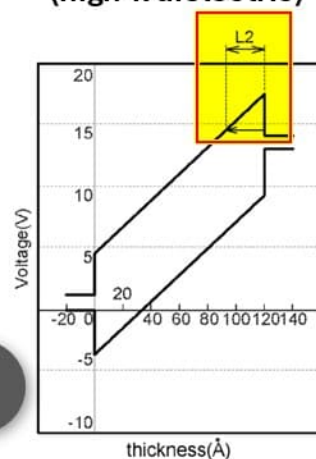
[0052] FIG. 8D shows a curve of applied voltages vs. the thickness of an etching stop layer 200 applying silicon oxide as the first stop layer 210 and aluminum oxide as the second stop layer 220, wherein the composite layer of silicon oxide-aluminum oxide has a tunneling length L4. It is apparent that the tunneling length L4 is larger than the tunneling length L1 as shown in FIG. 8A.

Ex. 1008 (Chen), [0052]

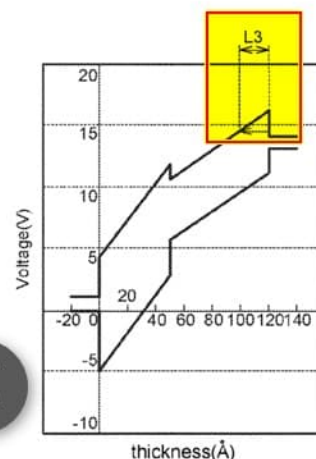
Single-layer:
silicon nitride



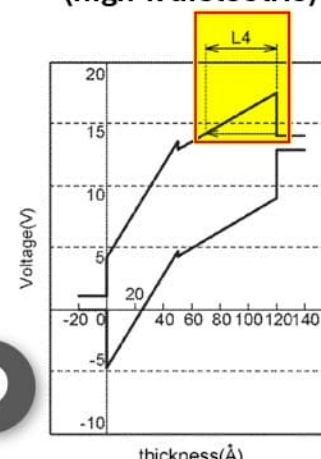
Single-layer:
aluminum oxide
(high-k dielectric)



Double-layer:
silicon oxide + silicon nitride



Double-layer:
silicon oxide + aluminum oxide
(high-k dielectric)



Ex. 1008 (Chen), [0047]-[0053], Figs. 8A-D

Han Already Protects Against Tunneling, Making Chen's "stop layer" Redundant

Han

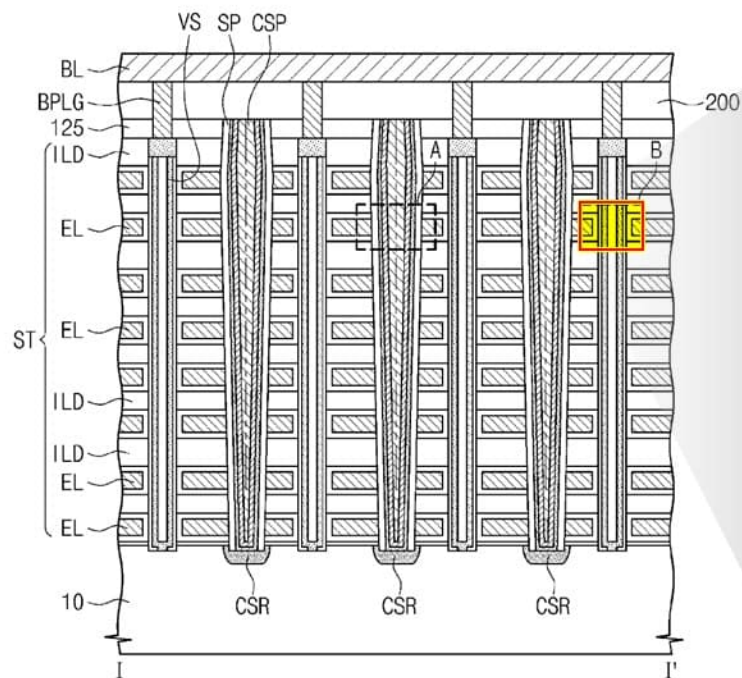


FIG. 22

Ex. 1007 (Han), [0024], [0138]-[0141],
Figs. 22, 26C, 26D

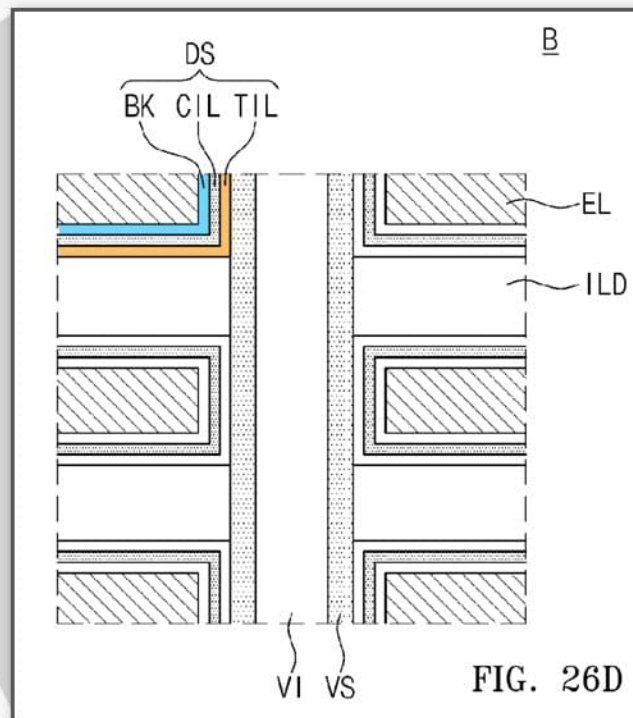


FIG. 26D

Han

[0138] According to the exemplary implementation illustrated in FIG. 26D, the tunnel insulating layer TIL, the charge storage layer CIL, and the blocking insulating layer BK may extend from between the electrode EL and the vertical structure VS onto the top and bottom surfaces of the electrode EL.

[0140] The tunnel insulating layer TIL may include at least one of materials having energy band gaps greater than that of the charge storage layer CIL and may be formed by a CVD technique or an ALD technique. For example, the tunnel insulating layer TIL may include a silicon oxide layer formed using the CVD technique or the ALD technique. Alternatively, the tunnel insulating layer TIL may include at least one of the high-k dielectric layers such as an aluminum oxide layer and hafnium oxide layer.

[0141] The blocking insulating layer BK may include first and second blocking insulating layers that are formed of different materials from each other. One of the first and

* * *

blocking insulating layer. In some exemplary implementations, the second blocking insulating layer may include at least one of the high-k dielectric layers, and the first blocking insulating layer may include a material of which a dielectric constant is lower than that of the second blocking insulating layer.

Ex. 1007 (Han), [0024], [0138]-[0141]



A POSITA Would Not Add Cost And Complexity For Redundant Functions

1

Han already provides adequate punch-through protection

2

Han already provides adequate tunneling protection



South-Tek Systems v. Engineered Corrosion Solutions

“Given the redundant functions...the Board found a [POSITA] would not have been motivated to add a condensate drain to Viking in addition to the system’s drum drip drain.”

South-Tek Sys., LLC v. Engineered Corrosion Sols., LLC, 748 F. App’x 1003, 1007 (Fed. Cir. 2018) (affirming Board’s findings)



Dr. Campbell Is A POSITA

Petition

VIII. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA in the field of the '276 patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (*e.g.*, researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience). This POSITA would have been aware of and generally knowledgeable about 3D NAND's structure, how it is manufactured, and its component parts. Banerjee ¶ 42.

Pet. 26



Dr. Campbell Is A POSITA

Patent Owner's Expert, Dr. Campbell's CV

Curriculum Vitae Stephen A. Campbell

Educational History

PhD	Physics	Northwestern University	1981
MS	Physics	Northwestern University	1978
BA	Physics	College of St. Thomas	1975

* * *

Professor Campbell is the author of *Fabrication Engineering at the Micro and Nanoscale*, one of the most widely used textbook on microfabrication. This text has been used in more than 60 US schools as well as many schools in Europe and Asia.

* * *

Professor Campbell's teaching experience includes Microfabrication, Semiconductor Devices, Electromagnetic Fields, Analog Electronics, Linear Circuits, Circuits Lab, Senior Design, and Materials and Devices. In research, Professor Campbell is most well-known for pioneering efforts in high permittivity (aka high-k) materials for the gate insulator in deeply scaled MOSFETs. This revolution in transistor design has now been adopted by most of the leading-edge integrated circuit manufacturers. His other current interests include ultra-high-speed MEMS and efficient thin film

Ex. 2007 (Campbell CV), 1



Dr. Campbell's Knowledge Shows He Is A POSITA

Etch Material

Patent Owner's Expert, Dr. Campbell

A. ...Further, etch processes are highly dependent on the material used, the depth and aspect ratio of the desired etch, the material to be deposited on the sidewalls, the material on which the etch is stopped...

Q. And how do these excerpts we read relate to your area of expertise?

A. These align very well with the areas that I am an expert in.

Ex. 1091 (Campbell Dep., '711 Pat.), 133:8-24

Etch Process Design Aspects

Patent Owner's Expert, Dr. Campbell

Q. ...[D]o you consider yourself qualified to offer an opinion on those types of design aspects that relate to etch processes?

A. Absolutely...that's the point to the process people...telling the designers you can't do this....

Ex. 1091 (Campbell Dep., '711 Pat.), 134:17-135:3



Petitioner's "design" Attack Is A Strawman

Patent Owner's Expert, Dr. Campbell

- Q. Is it your opinion that a POSITA in the area of semiconductor designs can build a device using the disclosure of the '711 Patent assuming there's no limit on time and resources?
- A. **The '711 Patent is primarily a process in -- a process description. The design, if you will, where the transistors go and so forth is really modest by comparison. I don't know if the processing people are saying which layers go where and how thick they are and how you're going to etch things. Those are all process parameters. So a POSITA in design, probably not because he's not in the right area.**

Ex. 1091 (Campbell Dep., '711 Pat.), 150:14-151:5