

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2025-00228
Patent 11,101,276 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

CYGAN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. *Background and Summary*

Micron Technology, Inc. (“Petitioner”) filed a Petition requesting an *inter partes* review of claims 1–18 of U.S. Patent No. 11,101,276 B2 (Ex. 1001, “the ’276 patent”). Paper 1 (“Pet.”). The Petition is supported by a Declaration from Dr. Sanjay Banerjee. Ex. 1003 (“Banerjee Declaration”). Yangtze Memory Technologies Company, Ltd. (“Patent Owner”) filed a Preliminary Response to the Petition, supported by a Declaration from Dr. Stephen Campbell. Paper 12 (“Prelim. Resp.”); Ex. 2006 (“Campbell Dec.”). On July 25, 2025, we granted institution on all asserted claims and grounds. Paper 22 (Inst. Dec.).

Patent Owner filed a Response, accompanied by a second Declaration of Dr. Campbell. Paper 31 (“PO Resp.”); Ex. 2019 (“2nd Campbell Dec.”) and transcripts of depositions of Dr. Banerjee concerning the instant patent (Ex. 2020) and concerning U.S. Patent 10,672,711 (Ex. 2021). Petitioner filed a Reply Brief, accompanied by a second declaration of Dr. Banerjee and a transcript of a deposition of Dr. Campbell. Paper 49 (“Pet. Reply”); Ex. 1085 (“2nd Banerjee Dec.”); Ex. 1086 (“Campbell Dep.”). Patent Owner filed a Sur-reply. Paper 54 (“PO Sur-reply”). We held oral arguments on April 27, 2026, and a transcript has been entered into the record. Paper 58 (“Tr.”).

B. *Real Parties-in-Interest*

Petitioner identifies itself and its subsidiaries, including Micron Consumer Products Group LLC, as real parties-in-interest. Pet. 7. Patent Owner identifies itself as the real party-in-interest. Paper 5, 1.

C. Related Matters

The parties represent that the '276 patent is involved in *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023). Paper 5, 1; Pet. 7–8. Petitioner also filed IPRs challenging other patents asserted in the district court case. Pet. 8–9.

D. The '276 Patent

The '276 patent is titled “Word Line Contact Structure for Three-Dimensional Memory Devices and Fabrication Methods Thereof.” Ex. 1001, code (54). The '276 patent issued on August 24, 2021, from Application 16/865,056, as a division of Application No. 16/126,947, filed on September 10, 2018, now U.S. Patent No. 10,672,711, which is a continuation of PCT/CN/2018/101308, filed on August 20, 2018. *Id.* at codes (21), (22), (45). The '276 patent relates to a word line contact structure including a staircase structure having a conductor layer disposed over a dielectric layer, with a barrier layer disposed over a portion of the conductive layer on each step of the staircase, and an etch-stop layer disposed on the barrier layer. *Id.* at code (57).

E. Illustrative Claim

Claim 1 is illustrative, and recites as follows:¹

[1.PRE] A method for forming a semiconductor structure, comprising:

[1.A] forming a staircase structure comprising a plurality of steps, wherein the forming of each step of the plurality of steps comprises disposing a sacrificial layer over a dielectric layer;

¹ Bracketed organization added as per the Petition.

[1.B] disposing an etch-stop layer on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer;

[1.C] disposing an insulating layer on the etch-stop layer;

[1.D] replacing the sacrificial layer of each step with a gate stack, the gate stack comprising a conductive layer and a first high-k dielectric layer;

[1.E] forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer;

[1.F] etching the exposed portions of the etch -stop layer in the plurality of openings and exposing at least a portion of the conductive layer of each step, and

[1.G] forming a plurality of conductive structures in each of the plurality of openings.

Ex. 1001, 15:3–23.

F. Evidence

Petitioner relies on the following evidence:

Name	Document	Exhibit
Kim et al. “Kim” ²	US 2012/0070944 A1	1005
Fang et al. “Fang” ³	US 2019/0067306 A1	1006
Han et al. “Han” ⁴	US 2017/0062470 A1	1007
Chen ⁵	US 2017/0294384 A1	1008

² Petitioner asserts that Kim is prior art under 35 U.S.C. §§ 102(a)(1)-(a)(2) based on its March 22, 2012 publication date and the August 31, 2017 priority date of the '276 patent. Pet. 11.

³ Petitioner asserts that Fang is prior art under 35 U.S.C. § 102(a)(2) based on its publication date of February 28, 2019. Pet. 12.

⁴ Petitioner asserts that Han is prior art under 35 U.S.C. §§ 102(a)(1)-(a)(2) based on its filing date of August 26, 2016 and its priority date of August 28, 2015. Pet. 12.

⁵ Petitioner asserts that Chen is prior art under 35 U.S.C. § 102(a)(2) based on its filing date of April 12, 2016 and its publication date of October 12, 2017. Pet. 12.

G. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–19 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2, 4, 5, 9–18	103 ⁶	Kim ⁷
1–18	103	Kim, Fang
1–15	103	Han, Fang
17, 18	103	Han, Fang, Chen

II. ANALYSIS

A. Legal Standards

A claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, “would have been obvious at the time the invention was made to a person having ordinary skill in the art [to which said subject matter pertains].” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual

⁶ We apply AIA 35 U.S.C. § 103 to the ’276 patent because it was filed after, and never claimed the benefit of an effective filing date before, March 16, 2013. Ex. 1001, codes (22), (63); Pet. 11.

⁷ Petitioner styles this ground and the Park ground as also being based on “a POSITA’s [Person of Ordinary Skill In The Art] knowledge.” Pet. 12. However, an *inter partes* review may be requested “only on the basis of prior art consisting of patents or printed publications,” although it may “rely on evidence beyond prior art documents.” 35 U.S.C. § 311(b); *Qualcomm Inc. v. Apple, Inc.*, 24 F.4th 1367, 1374–75 (Fed. Cir. 2022). Patent Owner does not raise a §311(b) challenge. This Petition is not subject to the Memorandum titled, “Enforcement and Non-Waiver of 37 C.F.R. § 42.104(B)(4) and Permissible Uses of General Knowledge in Inter Partes Reviews,” available at https://www.uspto.gov/sites/default/files/documents/aapa_memo_final_signed.pdf, because it was filed on November 29, 2024, prior to the September 1, 2025 applicability date of the Enforcement Memorandum.

determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of non-obviousness.⁸

See Graham v. John Deere Co., 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art (“POSITA”) at the critical time “would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (*e.g.*, researching, designing, or teaching) monolithic 3D structures and NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience).” Pet. 26 (citing Ex. 1003 ¶42). Petitioner further asserts that a POSITA “would have been aware of and generally knowledgeable about 3D NAND’s structure, how it is manufactured, and its component parts.” *Id.* Patent Owner does not dispute this assessment. PO Resp. 7–8. For purposes of this Decision, we adopt Petitioner’s proposed level of ordinary skill, as it appears to be consistent with the specification of the ’276 patent and the prior art of record.

Petitioner argues that Patent Owner’s declarant, Dr. Campbell, is not a person having ordinary skill in the art because he is not a semiconductor designer and has no experience in 3D memories, and that his testimony is mostly unsupported by evidence, and therefore, not entitled to any weight. Pet. Reply 27–28. Patent Owner disagrees, pointing to Dr. Campbell’s testimony that he is a fabrication and processing expert with an adequate

⁸ Neither party presents evidence or arguments regarding objective evidence of non-obviousness. Pet. 107–108; PO Resp.

knowledge of semiconductor design. PO Sur-reply 24 (citing Ex. 1091, 133:8–24).

Dr. Campbell has a Ph.D. in physics, supplying the advanced degree that Petitioner’s definition of a person having ordinary skill in the art accepts as a replacement for some experience. Ex. 2006 ¶ 2. Dr. Campbell has significant experience in semiconductor technology, including in process technologies for submicron CMOS, years of research in semiconductor processing, materials, and device structures, and authored “[t]he leading textbook on semiconductor technology.” *Id.* ¶¶ 2–4. Dr. Campbell qualifies as a person of ordinary skill in the art under the parties’ agreed definition.

C. Claim Construction

In an *inter partes* review, we construe a patent claim “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b).” 37 C.F.R. § 42.100(b). Under this standard, the words of a claim generally are given their “ordinary and customary meaning,” which is the meaning the term would have to a person of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc).

The Petition did not propose any express claim construction. Pet. 25. Patent Owner proposed that the terms “exposing portions” and “etching the exposed portions” require two different steps performed in that order. PO Resp. 7–10. Petitioner does not contest this characterization. Pet. Reply 1–2. Patent Owner also proposes that this requires the exposure step not to perform any etching of the newly exposed layer. PO Resp. 10–12 (citing Ex. 1001, 10:2–5, 10:15–17 (stating that the etch-stop layer “protects the underlying structure until all the VIA openings 640 are formed” and that it

“is not etched through”) (emphasis omitted)). Petitioner agrees, stating, “[t]he essence of an etch-stop layer dictates that contact-hole etching stops or slows down upon contact, i.e., exposing without penetrating it.” Pet. Reply 11. Based on the record before us, we determine that no claim term requires express construction for purposes of this Decision.

D. Obviousness over Kim

Petitioner asserts that claims 1, 2, 4, 5, and 9–18 are unpatentable under 35 U.S.C. § 103 as obvious over Kim in view of the knowledge of a person of ordinary skill in the art. Pet. 31–64. Patent Owner argues against this assertion. PO Resp. 13–39.

Upon consideration of Petitioner’s explanations and the totality of evidence in the complete trial record, we are persuaded that Petitioner has shown, by a preponderance of the evidence, that claims 1, 2, 4, 5, and 9–18 are unpatentable as being obvious over Kim.

1. Kim

Kim is titled “Methods of Manufacturing Three Dimensional Semiconductor Devices.” Ex. 1005, code (54). Kim relates to providing a semiconductor substrate including a peripheral region and a cell array region, with a peripheral structure on the peripheral region and a cell structure in the cell array region that is thicker than the peripheral structure. *Id.* at code (57). Both structures are covered by an interlayer dielectric, on which is formed a polishing stop layer. *Id.* The interlayer dielectric is planarized using the polishing stop layer as a planarization stop. *Id.*

2. Analysis of Claim 1

We begin our analysis of Petitioner’s obviousness contentions with Petitioner’s assertions as to claim 1.

[1.PRE] A method for forming a semiconductor structure, comprising: [1.A] forming a staircase structure comprising a plurality of steps, wherein the forming of each step of the plurality of steps comprises disposing a sacrificial layer over a dielectric layer;

Patent Owner contests Petitioner's assertion that Kim in view of the knowledge of the prior art teaches "disposing a sacrificial layer over a dielectric layer," as set forth in limitation [1.A]. PO Resp. § III.A.

To the extent the preamble [1.PRE] is limiting, Petitioner asserts that it is taught by Kim's description of a 3D semiconductor device at successive stages of manufacturing. Pet. 35 (citing Ex. 1005, code (57), ¶ 183, Figs. 17A–22A). With respect to limitation [1.A], Petitioner asserts that Kim's "stepwise stacked layer structure ST" teaches a staircase structure comprising a plurality of steps. *Id.* at 36–37 (citing Ex. 1005, Fig. 17A (bottom six steps), ¶¶ 7–8, 64; Ex. 1003 ¶¶ 89–91).

Petitioner further asserts that each of Kim's steps comprises a sacrificial layer SC1–SC6 over an insulating dielectric layer 111–116. *Id.* at 35–36 (citing Ex. 1005 ¶¶ 64, 86; Ex. 1003 ¶¶ 89–90). Petitioner points to Kim's description of two embodiments, one in which the sacrificial layer is the top surface and one in which the dielectric layer is the top surface. *Id.* at 27 (citing Ex. 1005 ¶¶ 90, 91, 240). Petitioner asserts that although Kim's Figures show the lower steps having the insulating layer (e.g., 111) atop the sacrificial layer (e.g., SC1), the order would be reversed in the other embodiment to result in the claimed arrangement at each step. *Id.* at 36–37 (citing Ex. 1005, Fig. 17A; Ex. 1003 ¶¶ 89–90). Petitioner asserts that applying the gate stack-on-top order would have been obvious because a person having ordinary skill in the art would understand Kim to teach that this order applies to the Figure 17A–22B embodiment. *Id.* at 32–33.

Patent Owner argues that Petitioner does not show sufficient motivation to combine these embodiments with a reasonable expectation of success. PO Resp. § III.A.1 (citing *In re Stepan Co.*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017) (“[C]ombining multiple embodiments from a single reference” requires “a motivation to make the combination.”). Patent Owner acknowledges that Kim states, “overlapping descriptions of elements previously described with reference to [Figures 5A–14B] may be omitted.” *Id.* at 17 (citing Kim ¶ 184). However, whereas Petitioner interprets Kim’s statement to mean that described elements carry through to later-described embodiments, Patent Owner argues that it merely means that the same numbers are used for the same elements across embodiments. *Id.* (citing Pet. 32).

We determine that Patent Owner interprets Kim’s statement too narrowly. Kim partitions its disclosure into two main sections pertinent to this issue. First, Kim describes its “methods of fabricating,” including numerous embodiments, with reference to Figures 4 through 15. Ex. 1005 ¶¶ 13–14, 56–57. Kim’s statement that the top surfaces of the steps may be either the gate stack (e.g., the replaced sacrificial layers) or the insulating layer are part of this first section. *Id.* ¶¶ 90, 140. Patent Owner does not dispute that Kim teaches that the order of layers may be reversed so as to form the gate stack on top in that first section. Tr. 29:2–3 (“Kim . . . says that either order is acceptable for the first embodiment”). Second, Kim describes “other example embodiments” with reference to Figures 17 through 22. Ex. 1005 ¶¶ 179–184. Kim’s description of its etch-stop and barrier layer structure are part of this second section. *Id.* ¶ 187.

We agree with Petitioner that Kim’s first and second sections are described as compatible, not mutually exclusive, embodiments. Kim’s

second section builds further layers upon the structure of its first section, and states:

In these embodiments, the same elements as in the embodiments previously described with reference to FIGS. 5A through 14A and FIGS. 5B through 14B will be denoted by the same reference numbers therein, and *for concise description, overlapping description of elements* previously described with reference to FIGS. 5A through 14A and FIGS. 5B through 14B *may be omitted*.

Ex. 1005 ¶ 184 (emphasis added). Patent Owner argues that only the embodiments in Figures 17A–22B describe an etch-stop layer and a barrier layer (as claimed), and that the language cited for a gate-stack-on-top configuration (e.g., Ex. 1005 ¶¶ 90, 91, and 240) is “conspicuously absent from the description of Figures 17A–22B.” PO Resp. 19–20 (citing Ex. 2009 ¶ 36).

A requirement that each embodiment explicitly refer back to elements described in earlier embodiments would not be consistent with Kim’s statement that previously described elements are “omitted” in the Figures 17A to 22B section “for concise description.” As admitted by Patent Owner, it would be a “reasonable inference” that materials described in a first embodiment for a particular hypothetical layer L would also be used for that layer L in later embodiments absent an express statement to the contrary “because you have just omitted that sort of duplicative description.” Tr. 37:9–38:12. Kim’s Figures 17A–22B do not further address the underlying staircase structure that was detailed in the descriptions of the Figures 4–15 embodiments. Thus, it would similarly be a “reasonable inference” that aspects of the stack structure would be understood to apply to the same stack in the embodiments of Figures 17A–22B, which rely upon, in unaltered form, the earlier-described elements of the stack.

Patent Owner argues that because Figures 17A–22B show the gate-stack on bottom, they “replace” and “exclude” any prior description of a gate-stack-on-top. PO Resp. 18–19 (citing Ex. 2019 ¶¶ 40–41; Ex. 1005 ¶¶ 185–187 (describing the etch-stop layer as covering the sacrificial layers only at their end portions)). However, as admitted by Patent Owner, all of Kim’s Figures show only a gate-stack-on-bottom structure. Tr. 41:6–7 (“For the first embodiment, it is true that figures show the gate stack on bottom.”). The fact that Kim’s Figures 17A–22B, which add etch-stop and barrier layers to the gate stack, are shown only as gate stack on bottom is merely consistent with the uniform use of gate-stack-on-bottom in Kim’s Figures, which show the layer-by-layer construction of its device. Like Figures 4–15, Figures 17A–22B exemplify rather than limit the description of the previously described memory stack, and do not exclude the gate-stack-on-bottom description of the memory stack. Kim can be used for all it realistically teaches, including descriptions in its disclosure that are not represented by specific Figures. *See In re Chapman*, 357 F.2d 418, 424 (C.C.P.A. 1966) (stating that a reference “is not limited to the disclosures in its specific illustrative examples.”). Accordingly, the record supports Petitioner’s assertion that Kim’s teaching of a gate-stack-on-top alternative for the memory stack would be understood by a POSITA as a memory stack option applicable to its other embodiments having that same memory stack.

With respect to the reason to apply the gate-stack-on-top alternative of Kim’s memory stack to its later-described embodiments of Figures 17A–22B, Patent Owner argues that Petitioner does not identify any benefit to doing so, any problem that would be solved by doing so, or any other reason save hindsight reconstruction of the ’276 patent claims. PO Resp. 16–17. Patent Owner argues that even if Kim teaches that the gate-stack-on-top

alternative could be used with Kim's etch-stop and barrier layers, Petitioner does not explain why a person having ordinary skill would have been motivated to do so. *Id.* at 17–18 (citing *InTouch Techs., inc. v. VGO Commc'ns, Inc.*, 751 F.3d 1327, 1351–52).

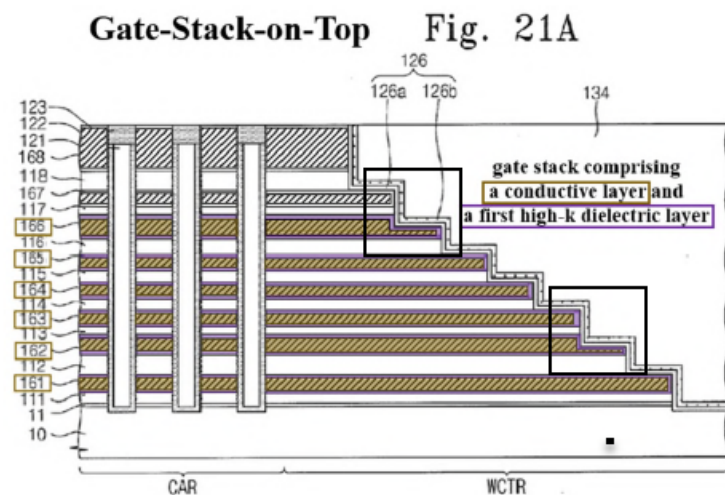
As discussed *supra*, Kim's teaching that its described memory stack may have either ordering provides sufficient reason why a person having ordinary skill would consider it obvious to use either ordering for its memory stack that is covered with etch-stop and barrier layers.

To the extent that Kim's alternate ordering would instead be considered to be limited only to its Figures 4–15 description, Petitioner has provided evidence that a person having ordinary skill in the art would have recognized that the gate-stack-on-top and the gate-stack-on-bottom are generally recognized as being suitable alternatives for each other. Pet. 33. Petitioner points to two references showing both alternatives, one displaying “both orders side-by-side” and the other teaching “that the layers may be formed in either order.” *Id.* (citing Ex. 1008 (“Chen”), Figs. 7A–7B, ¶¶ 44–46; Ex. 1009 ¶¶ 34–35). Petitioner argues that this evidence shows that a person having ordinary skill in the art would have recognized either alternative to be a common alternative. *Id.*; Pet. Reply 2. Patent Owner does not dispute that these were known alternatives. PO Resp; PO Sur-reply. Dr. Campbell agrees that Chen teaches two configurations, a gate-stack-on-top and a gate-stack-on-bottom. Ex. 1086, 118:22–119:1, 136:9–17. Dr. Banerjee attests that both configurations in Chen are “a suitable substitute for each other, and do not make a difference for purposes of constructing a 3D memory staircase.” Ex. 1085 ¶ 15.

Thus, it is uncontested, and supported by sufficient evidence, that the gate-stack-on-top and gate-stack-on-bottom are two predictable, suitable

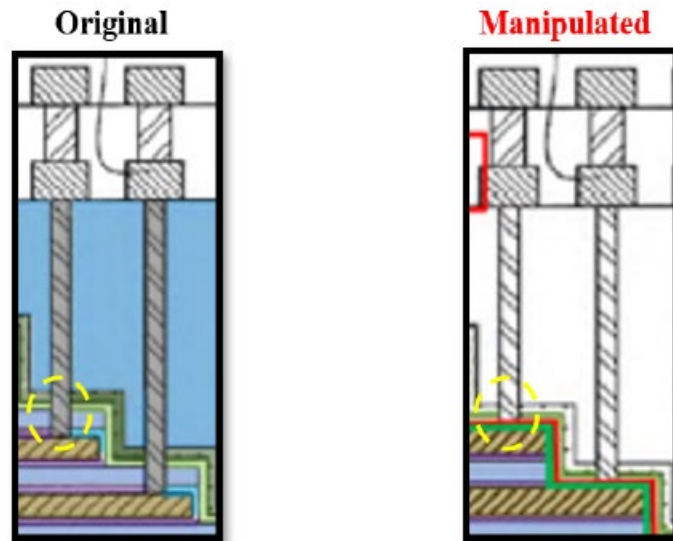
options for a 3D NAND memory staircase. The selection of either of two predictable choices for the same purpose is obvious because a person having ordinary skill in the art “has good reasons to pursue the known options within his or her technical grasp.” *Uber Techs., Inc. v. XOne, Inc.*, 957 F.3d 1334, 1340 (Fed. Cir. 2020) (quoting *KSR*, 550 U.S. at 421); *Intel Corp. v. PACTXPP Schweiz AG*, 61 F.4th 1373, 1381 (Fed. Cir. 2023) (“Intel never had to show that replacing Kabemoto's secondary cache with Bauman’s secondary cache was an “improvement” in a categorical sense [but] just had to show that Bauman’s secondary cache was a “suitable option” to replace Kabemoto’s secondary cache.”). Consequently, we determine that a person having ordinary skill in the art would have found it obvious to use either configuration for the memory stack in Kim’s Figure 17–22A description.

With respect to the reasonable expectation of success, Patent Owner argues that there are technical issues that prevent a reasonable expectation of success in modifying Kim’s etch-stop embodiment of Figures 17A–22B to have the gate stack on the top. PO Resp. 20. Patent Owner points to narrowed sections of conductive gate layers 162 and 166 in Petitioner’s proposed modification:



PO Resp. 21. Modified Figure 21A shows gate stack conductive layers 161–166 and dielectric layers 111–116, with etch-stop and barrier layers 126 disposed thereon. Pet. 44. Patent Owner argues that these thin areas, shown in the added boxes, could lead to a defective device susceptible to punch-through during etching, higher electrical resistance, incomplete etching, replacement, or collapse during gate replacement, and damage of the intervening insulating layers. PO Resp. 20–21 (citing Ex. 2020, 30:18–31:2; 24:25–25:20, 26:23–27:1, 28:4–9, 28:19–29:2; Ex. 2019 ¶ 45). Patent Owner further argues that Petitioner’s modified figures⁹ shorten the contact plugs, requiring non-trivial alteration of the processes used to create the insulating and sacrificial layer stack. *Id.* at 22 (citing Ex. 2019 ¶ 46). Patent Owner provides an illustration of the differences being discussed:

⁹ To the extent that Patent Owner takes issue with Petitioner’s illustrative modified Figures representing Kim’s alternate ordering, rather than Kim’s alternate ordering itself, Dr. Banerjee does not indicate that his modifications are drawn to any scale, but states that they are for the purpose of “to show this . . . ordering.” Ex. 1003 ¶ 86; *see* Pet. Reply 6. We note that Chen, relied upon to evidence the obviousness of the gate-stack-on-top arrangement, does not have such a narrowed area, providing evidence that a person of ordinary skill in the art would not be confined to the exact dimensions of Petitioner’s exemplary modified Figures. Ex. 1008, Figs. 7A–7B.



PO Resp. 23 (left image showing the insulator on top, right image showing the gate on top, with a dashed circle highlighting the contact plugs through intervening layers to reach the gate layer).

The reasonable expectation of success test is applied to a combination of teachings of references or embodiments, not the properties of a single prior art embodiment. *See Guardant Health, Inc. v. Univ. of Washington*, 2026 WL 184334, at *6 (Fed. Cir. Jan. 23, 2026) (stating that “when . . . elements are disclosed in a single embodiment of a single prior art reference,” *In re Stepan* “is inapposite . . . because it addresses combinations”); *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367 (Fed. Cir. 2016) (stating, “[t]he reasonable expectation of success requirement refers to the likelihood of success in combining references to meet the limitations of the claimed invention.”)).

We do not find Patent Owner’s evidence compelling because it is directed solely to the disclosed gate stack in Kim’s gate-stack-on-top embodiment of Figures 4–15, not to drawbacks of combining two embodiments; i.e., of combining Kim’s inverted gate stack configuration with further etch-stop and barrier layers. Patent Owner agrees that Kim

teaches an embodiment in which the gate stack layers are inverted. PO Resp. 18 (stating, “Kim discloses that in some embodiments ‘each of the top surfaces of the sacrificial layers SC1 to SC8, not the top surfaces of the insulating layers 111 to 118, may be partially exposed in the word line contact region WCTR.’”).¹⁰ Patent Owner further agrees that Figure 14A, which is the unmodified left image reproduced above, is part of the same description that may be in either a gate-stack-on-bottom (as shown in Figure 14A) or a gate-stack-on-top (as described at ¶ 90) configuration. *See* PO Sur-reply 2 (“Kim’s separate Figures 5A–14B embodiment”). Because Kim teaches an operative gate-stack-on-top embodiment of the gate stack with contact plugs, we discount Patent Owner’s evidence of potential drawbacks with that configuration. Patent Owner’s argument is that evidence shows a person skilled in the art would not consider using a gate-stack-on-top configuration because it would be more prone to error, yet Kim shows just such a configuration to be known in the art. We determine that Petitioner has sufficiently shown that its combination would have had a reasonable expectation of success.

Consequently, we agree that Petitioner has sufficiently shown Kim to teach or suggest limitations [1.PRE]¹¹ and [1.A].¹²

[1.B] disposing an etch-stop layer on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer; [1.C] disposing an insulating layer on the etch-stop layer; [1.D] replacing the sacrificial layer of each step with a gate

¹⁰ Patent Owner does not contest that the gate-stack-on-top configuration embodiment of Kim’s paragraph 90 is an operable embodiment.

¹¹ We do not express an opinion on whether the preamble is limiting.

¹² Because each element of limitation [1.A] is taught by Kim, we need not assess Patent Owner’s further arguments as to whether the knowledge in the prior art supplies a limitation missing from Kim. PO Resp. 24–30.

stack, the gate stack comprising a conductive layer and a first high-k dielectric layer;

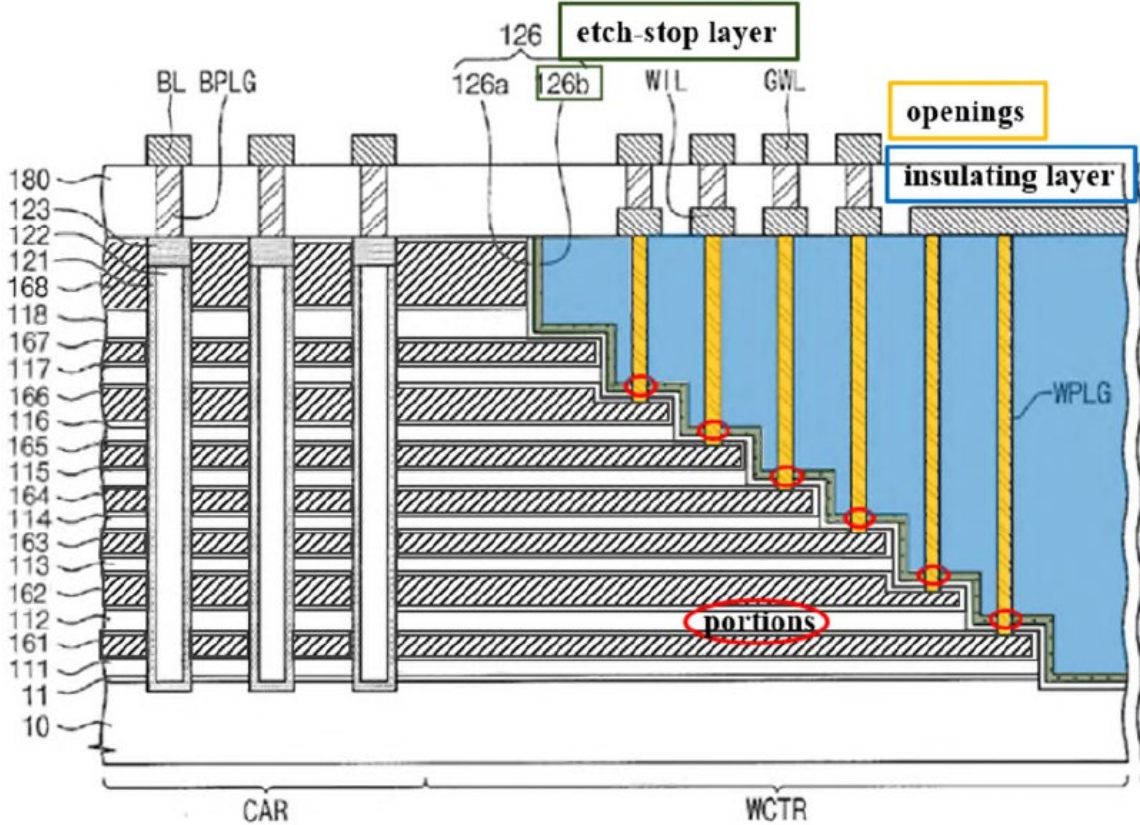
We determine that Petitioner has sufficiently shown Kim to teach uncontested limitations [1.B]–[1.D]. Petitioner has shown that Kim teaches first etch-stop layer 125a, second stop layer 125b (etch stop layer) comprised of high-k dielectric silicon nitride disposed on each step, and interlayer dielectric 130 (insulating layer) disposed on the etch stop layer. Pet. 39–42 (citing Ex. 1005, Figs. 17A, 18A, ¶¶ 94, 185–188, 213; Ex. 1003 ¶¶ 93–96). Petitioner has also shown that Kim teaches replacing the sacrificial layer (e.g., one of SC 1–6) with a gate stack comprising a conductive layer (e.g., one of corresponding gate electrodes 161–166) and a first high-k dielectric layer (data storing layer 150 including a “blocking insulating layer” made of aluminum oxide). *Id.* at 43–44 (citing Ex. 1005 ¶¶ 198–202, Figs. 20A, 21A, Ex. 1003 ¶¶ 97–99).

[1.E] forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer; [1.F] etching the exposed portions of the etch-stop layer in the plurality of openings and exposing at least a portion of the conductive layer of each step; [1.G] forming a plurality of conductive structures in each of the plurality of openings.

Patent Owner argues that Kim does not teach “forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer” as recited in limitation [1.E]. PO Resp. 31.

Petitioner asserts that Kim etches openings through insulating layer 130 to expose portions of the etch-stop layer 126b (which Petitioner asserts to be analogous to etch-stop layer 125b). Pet. 45–46 (citing Ex. 1005 ¶ 173; Ex. 1003 ¶ 102). Petitioner provides an annotated Figure 22A of Kim:

Gate-Stack-on-Top Fig. 22A



Id. at 45–46. Annotated Figure 22A of Kim shows openings (yellow) through insulating layer 130 (blue) extending through etch-stop layer 126b to gate electrodes 161–166. Ex. 1005, Fig. 22A, ¶¶ 185–86; Pet. 45–46. Petitioner asserts that Kim’s openings are “extended to the gate electrodes” and subsequently filled with conductive structures (word line contact plugs (“WPLGs”). Pet. 46–49 (citing Ex. 1005 ¶ 173; Ex. 1003 ¶ 102). Petitioner further asserts that the etch-stop layer has an etch selectivity that stops etching, i.e., by allowing the interlayer dielectric 130 to be etched away without penetrating the etch-stop layer. *Id.* at 47 (citing Ex. 1005 ¶ 213). After the dielectric is etched to reveal the etch-stop layer, Petitioner asserts that Kim’s etch-stop layer is removed per step [1.F] so that the conductive structures may reach the underlying conductive layers, by “one or more

etching steps involving different relative etch selectivities after step [1.E].” *Id.* at 48 (citing Ex. 1005 ¶ 211; Ex. 1003 ¶ 104).

Patent Owner argues that Kim teaches completely penetrating through the etch-stop layer, such that the etch-stop layer is removed entirely, not exposed.” PO Resp. 31 (citing Ex. 1005 ¶ 173; Ex. 2021 ¶ 55). Patent Owner argues that “Petitioner provides no evidence that Kim teaches forming all openings before etching the etch-stop layer to expose the conductive layer.” PO Sur-reply 10. Patent Owner also argues that Kim does not disclose how contact openings are formed for the word line contact plugs WPLGs, and that Kim only shows the contact hole penetrating through etch-stop layer. PO Resp. 32 (citing Kim Fig. 22A).

Patent Owner’s argument is unavailing. Claim 1 does not require that no etching of any portion of the etch-stop layer begin until removal of the insulating layer is complete, but instead reflects that the insulating layer covers the etch-stop layer such that the insulating layer must be removed before the etch-stop layer is exposed. Nor does claim 1 require different processes to expose and penetrate the etch-stop layer. Rather, the claim encompasses a single process of etching that first exposes and then, through continued etching, penetrates the etch-stop layer. Because Petitioner has shown etching to the surface of the etch-stop layer and further etching to penetrate the etch-stop layer to the conductive layer of each step, Petitioner has sufficiently shown Kim to teach limitations [1.E] and [1.F].

Moreover, Petitioner provides a persuasive explanation of how Kim teaches that its dielectric etching stops at the etch-stop layer. Petitioner asserts that Kim teaches this through

Kim’s disclosure that “[t]he etch stop layer 125[126] may be formed of a material having an etch selectivity with respect to

the interlayer dielectric 130.” [Ex. 1005 ¶ 213]. The relative etch selectivity allows the interlayer dielectric to be etched away without penetrating the etch-stop layer.

Pet. 46–47.

With respect to this selective etching, Patent Owner argues that Kim describes the etch selectivity of its etch stop layer with respect to planarization of the dielectric, not for hole formation. PO Resp. 33 (citing Ex. 2006 ¶ 38). Patent Owner argues that the planarization process differs from the hole formation process. *Id.* (citing Ex. 2019 ¶¶ 57–60). However, Dr. Campbell conceded that Kim’s etch-stop layer acts to slow down the etch. Ex. 1086, 117:6–10, 131:14–132:12. Kim further describes its etch stop layer 125b as being formed of silicon nitride, the same material that Kim describes as “exhibiting a slower removal rate than the interlayer dielectric 130” during planarization. Ex. 1005 ¶¶ 187, 190. Dr. Campbell also testifies that a person having ordinary skill in the art would have designed an etch stop layer to minimize the possibility of it being penetrated before all of the vertical openings are formed. Ex. 1086, 90:11–18.

Based on the complete trial record, we determine that Petitioner has shown, by a preponderance of the evidence, that claim 1 would have been obvious over Kim.

3. *Claims 2, 9, 10, and 12–18*

Patent Owner does not separately contest the further limitations of challenged dependent claims 2, 9, 10, and 12–18. PO Resp. We have reviewed Petitioner’s assertions for these claims and determine that they are supported by the record and persuasive to show a teaching of each limitation. Pet. 50–64. Consequently, we determine that Petitioner has

shown by a preponderance of the evidence that claims 2, 9, 10, and 12–18 would have been obvious over Kim.

4. *Claim 4*

Claim 4 depends from claim 1, and further recites,

wherein etching the exposed portions of the etch-stop layer comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the conductive layer of each step.

Ex. 1001, 15:31–34.

Petitioner asserts that claim 4 would have been obvious over Kim because it was known that (1) the differing etch-stop and conductive layer materials inherently result in different etch rates and (2) the conductive layer should be preserved to prevent punch-through of gate electrodes. Pet. 50–51 (citing Ex. 1003 ¶¶ 108–09; Ex 1006 ¶ 28; Ex. 1023).

Petitioner’s assertion is persuasive on the evidence in the full trial record. Dr. Banerjee states that the SiN etch stop layer has a higher etching rate than metal conductive layers. Ex. 1003 ¶ 108 (citing Ex. 1023). Dr. Campbell testifies that an etch stop layer may permit punch-through if the lower level is unnecessary, but that the “gate is the part of the device that has to be retained.” Ex. 1086, 91:19–24; PO Resp. 47 (“A POSITA would understand that the purpose of the etch-stop layer is to protect underlying structures during the etching process”) (citing Ex. 1006 ¶ 26). Given an etch stop layer over a conductive layer as in claim 1, Dr. Campbell’s testimony and Fang (Ex. 1006) support Petitioner’s assertion that the etch-stop layer would have been known to have been preferentially (more rapidly) etched over the conductive layer. This supports Petitioner’s contentions, especially when viewed in the context of Kim, which generically and broadly describes

its etching and describes that the insulating layers may be reversed without providing details on the etching in the reversed-layer form.

Patent Owner argues that the Petition improperly relies on a POSITA's knowledge because etching rates are not unusually simple. PO Resp. 35. Dr. Campbell attests that small changes can have significant effects. PO Sur-reply 12; Ex. 2019 ¶¶ 62–63. However, the cited background art supports that various etch chemistries and processes would be known to remove an etch-stop layer above a conductive material. *See* Ex. 1006 ¶ 29.

Testimony from both declarants, corroborated by specific prior art, sufficiently supports Petitioner's assertion that the etching rate limitation would have been obvious. *See Philips N.V. v. Google LLC*, 948 F.3d 1330, 1338 (Fed. Cir. 2020) (determining that general knowledge may be shown by evidence corroborated by specific prior art). Consequently, we determine that Petitioner has shown, by a preponderance of the evidence, that claim 4 would have been obvious over Kim.

Patent Owner further argues that the USPTO disfavors the use of general knowledge in a ground to supply missing limitations. PO Resp. 24–25 n.4 (citing USPTO Memorandum, Enforcement and Non-Waiver of 37 C.F.R. §42.104(b)(4) and Permissible Uses of General Knowledge in Inter Partes Reviews at 1 (July 31, 2025) (“General Knowledge Memorandum,” https://www.uspto.gov/sites/default/files/documents/aapa_memo_final_signed.pdf)). Patent Owner argues that although this memo does not apply to the instant petition, it is evidence as to the USPTO's desired interpretation of 37 C.F.R. § 42.104(b)(4). PO Resp. 25 n.4.

The General Knowledge Memorandum “imposes on petitioners a procedural requirement to identify in the petition where each claim element

is found in the prior art patents or printed publications relied upon.” General Knowledge Memorandum, 3. The Memorandum states that “as applied in some cases, [37 C.F.R. § 42.104(b)(4)] may be narrower than 35 U.S.C. §311(b).” *Id.* However, we determine that by setting an applicability date of “any petition for IPR filed on or after September 1, 2025” for the General Knowledge Memorandum, the Office did not intend to change the “waiv[er of] enforcement of Rule 104(b)(4)” set by prior USPTO Memoranda for petitions filed prior to September 1, 2025. *Id.* at 1 n.1, 3. We are bound by this intent and the prior USPTO Memoranda. Consequently, we decline to abbreviate the waiver of 37 C.F.R. § 42.104(b)(4) recognized by the General Knowledge Memorandum, and do not rely on its provisions in this decision.

5. *Claim 5*

Claim 5 depends from claim 4 and further recites,

wherein etching the exposed portions of the etch-stop layer further comprises etching the exposed portions of the etch-stop layer at a higher etching rate than an etching rate of the first high-k dielectric layer.

Ex. 1001, 15:35–38.

Petitioner asserts that the high-k dielectric layer (disposed over the conductive layer and under the etch stop layer in claim 1 and altered Kim Fig. 22) would have been obvious to have been etched at a lower rate than the etch stop layer to further protect the conductive gate layer underneath. Pet. 52. Dr. Banerjee (citing Ex. 1024) states that selective etching of SiN (Kim’s etch stop layer) to AlO (Kim’s high-k dielectric layer) was known. Pet. 44, 52; Ex. 1003 ¶¶ 98–99, 110 (citing Ex. 1024).

Patent Owner argues that Petitioner improperly relies upon the prior art to teach missing claim limitations, citing to its arguments relating to claim 1. PO Resp. 36. We determine that this argument is unavailing for

the same reasons detailed above with respect to claims 1 and 4; i.e., that Petitioner has explained why Kim would have been understood by a person having ordinary skill in the art to encompass etching in the claimed manner, and that such explanation was supported by expert testimony corroborated by specific prior art representing the knowledge in the art.

Patent Owner argues that Petitioner does not explain why such further protection is desirable. PO Resp. 37.

We determine Petitioner provides a reasonable explanation for further protection of the underlying gate layer, namely that it would be desirable to prevent punch-through in addition to relying on the layers' low etching rate. Pet. 52. Petitioner relies on Kim's teaching of different materials for etch stop (silicon nitride) and high-k dielectric layer (aluminum oxide). Pet. 40 (citing Ex. 1005 ¶¶ 64, 186), 44 (citing Ex. 1003 ¶¶ 148, 151). Dr. Banerjee's testimony of the relative etch rates of those materials was not traversed. Consequently, Petitioner has sufficiently shown the obviousness of claim 5.

It may be that a person having ordinary skill in the art would also consider the alternative suggested by Patent Owner in which a single material is used for both the etch-stop and high-k dielectric materials, which would have the same etch rate. PO Resp. 37. However, Petitioner need only show that its proposed combination would have been obvious, not that its proposed combination is the only possible combination and that other combinations would not have been desirable. Petitioner's combination maintains the materials of Kim and re-orders the layers as Kim teaches. For the reasons expressed, Petitioner has shown, by a preponderance of the evidence, that claim 5 would have been obvious over Kim.

6. *Claim 11*

Claim 11 depends from claim 1 and further recites, “wherein forming the plurality of conductive structures further comprises planarizing the conductive materials and the insulating layer.” Ex. 1001, 16:13–15.

Petitioner asserts that a person having ordinary skill in the art viewing Kim, which planarizes top surfaces of other components, would have understood that a planar top surface is advantageous and required for forming the word line connecting lines. Pet. 56–57 (citing Ex. 1005 ¶¶ 209, 119, 206, altered Fig. 22A; Ex. 1003 ¶¶ 115–116 (citing Ex. 1021, 14)). Specifically, Petitioner points to Kim’s planarizing the top surfaces of other components. *Id.* (citing Ex. 1005 ¶¶ 119, 206). Dr. Banerjee attests that the top surface above the stack must be planar because the upper-level metal layers need to be planar for proper patterning. Ex. 1003 ¶ 116. Dr. Banerjee points to prior art showing that “filling insulators are understood to surround the stack structures to create a planar surface for the upper-level metal layer.” *Id.* (citing Ex. 1021, 14, 113).

Patent Owner argues, relying on its arguments for claim 1, that Petitioner errs in relying on knowledge that is neither unusually simple nor concerns a particularly straightforward technology. PO Resp. 38–39. We determine that this argument is unavailing for the same reasons detailed above with respect to claims 1 and 4; i.e., that Petitioner has explained why Kim would have been understood by a person having ordinary skill in the art to encompass planarizing in the claimed manner, and that such explanation is supported by expert testimony corroborated by specific prior art cited by Petitioner representing the knowledge in the art.

For the reasons expressed, Petitioner has shown, by a preponderance of the evidence, that claim 11 would have been obvious over Kim.

E. Obviousness over Kim and Fang

Petitioner asserts that claims 1–18 would have been obvious over on the combined teachings of Kim and Fang. Pet. 64–74. Petitioner relies on Fang to teach the additional limitations of claims 3, 6–8, and 12. *Id.* at 64. Petitioner also relies on Fang for an alternate teaching for limitation [1.B]; i.e., that Fang’s etch-stop layer “may be a high-k dielectric material, such as hafnium oxide.” Pet. 65 (citing Ex. 1006 ¶ 22). Petitioner asserts that a person having ordinary skill in the art would have been motivated to use Fang’s “[a]lternative[.]” material, i.e., a high-k dielectric material such as hafnium oxide, for the etch-stop layer. *Id.* at 72 (citing Ex. 1006 ¶ 22). Petitioner asserts that using a high-k dielectric material increases the tunneling length of the etch-stop layer to reduce tunneling current, thereby “more effectively electrically isolat[ing] [the conductive layers] from one another.” *Id.* (quoting Ex. 1006 ¶ 4). Petitioner asserts that “a high-k-dielectric etch-stop layer has a greater tunneling length (L2 in Figure 8B) compared to that of a silicon-nitride etch-stop layer, which improves stability.” *Id.* at 72–73 (citing Ex. 1006 Figs. 8A-8B, ¶¶ 47–48).

With respect to claims 1, 2, 4, 5, and 9–18, Petitioner has shown, by a preponderance of the evidence, that Kim teaches these limitations such that a person having ordinary skill in the art would have found those claims obvious. *Supra* § II.D. Thus, Petitioner’s obviousness assertions for these claims in this ground turn on its reliance on Fang’s high-k dielectric material such as hafnium oxide.

With respect to claim 1, Patent Owner argues that Petitioner fails to establish a motivation to combine Kim in view of Fang or a reasonable expectation of success in doing so. PO Resp. 40. Patent Owner first argues that Kim and Fang address different problems; i.e., that Kim prevents

damage during CMP planarization, and that Fang prevents damage from over-etching contact vias. *Id.* at 40–43 (citing Ex. 2019 ¶¶ 73–75).

However, obviousness does not require both references to address the same problem. *KSR*, 550 U.S. at 420 (“The second error of the Court of Appeals lay in its assumption that a person of ordinary skill attempting to solve a problem will be led only to those elements of prior art designed to solve the same problem.”). To the contrary, Patent Owner argues that each reference focuses on a different portion of a 3D memory device, and *KSR* states that “a person of ordinary skill will often be able to fit the teachings of multiple patents together like pieces of a puzzle,” for instance, beneficial teachings for different portions of a device. *Id.* at 402; PO Resp. 43.

Patent Owner next argues that a person having ordinary skill in the art would not be motivated to use Fang’s carbon-doped silicon nitride in place of Kim’s undoped silicon nitride as an etch-stop layer, because they have different etching properties that would require different etch chemistries and/or different layer thicknesses. PO Resp. 44–47. PO further argues that Fang discredits usage of undoped silicon nitride because Fang requires its etch-stop material to be a material that is not substantially removed during removal of the nitride materials 120 of the staircase structure, where the nitride material is silicon nitride. *Id.* at 45–46 (citing Ex. 1006 ¶¶ 19–20; Ex. 2021, 55:4–9; Ex. 2019 ¶¶ 76, 79).

However, Patent Owner’s arguments are based on Fang’s carbon-doped silicon nitride material only, and do not address Petitioner’s assertions that are based on Fang’s hafnium oxide material or general teaching of a high-k dielectric material. Pet. 65, 72; Pet. Reply 18. Fang is not limited to carbon-doped silicon nitride material. Ex. 1006 ¶¶ 8 (“In some embodiments, the etch stop material is a silicon nitride material, such as a

carbon-doped silicon nitride material.”), 23 (“the etch stop material 130 may be a high-k dielectric material, such as hafnium oxide.”). Further, Fang teaches that various etch chemistries and processes would be known to remove an etch-stop layer. *See* Ex. 1006 ¶ 29.

Patent Owner also argues that Fang’s etch-stop layer is designed for a device that does not use a further dielectric layer underneath to protect the gate stack, whereas Kim’s device does have a dielectric layer beneath in its two-etch-stop layer configuration. PO Resp. 48.

However, Patent Owner admits that the purpose of an etch stop layer is to protect the underlying components. PO Resp. 47 (“A POSITA would understand that the purpose of the etch-stop layer is to protect underlying structures during the etching process”). Patent Owner also cites to evidence that additional different materials provide additional safety margins during etching. *Id.* at 48 (citing Ex. 2021, 49:5–8). This corroborates Petitioner’s reasoning, supported by Dr. Campbell’s deposition testimony, that the presence of an additional underlying protective layer is either desirable as providing extra protection, or irrelevant because the etch-stop is purposed to prevent exposure of the layers below. Pet. Reply 17–18 (citing Ex. 1086, 98:19–99:1, 99:11–16).

Patent Owner further argues that Fang’s single-layer design requires more control of etching time and layer thickness, such that it wouldn’t be used in a multilayer design like Kim. PO Resp. 49. Patent Owner also argues that Kim doesn’t identify any tunneling problem that would motivate using a greater tunneling length material. *Id.* at 50–51. However, these arguments do not address the asserted combination. Petitioner only applies Fang’s teaching of the composition of the etch-stop layer, and does not

displace Kim’s multilayer teachings. Pet. 65, 70–74.¹³ Even if additional control were required for Fang’s layer, the above-discussed evidence emphasizes the importance of protecting the layers beneath the etch-stop layer. Further, Dr. Banerjee attests that “Fang simply applies techniques that Kim already uses” such that a person having ordinary skill in the art “would have found adopting Fang’s techniques to be cost effective because it merely expands the use of Kim’s existing techniques to another layer. Ex. 1003 ¶¶146–47; Pet. 70–71. The evidence supports a determination that it would have been obvious to a person having ordinary skill in the art to use a high-k layer in Kim.

Patent Owner also argues that Fang teaches hafnium oxide as an etch stop material but not specifically as an alternative to SiN, countering Petitioner’s assertion that HfO would be a suitable alternative to SiN having a greater tunneling length. PO Resp. 51–52; Pet. 67–68, 72–73 (HfO used to meet the “second high-k” material of claim 1). However, Fang lists different carbon doping percentages of SiN, noting that the doping amount cannot be so high as to include “stoichiometric” SiCN ($\text{Si}_1\text{C}_1\text{N}_1$), and “[a]lternatively” presents hafnium oxide as an alternative etch stop material. Fang ¶ 22; Pet. Reply 18.

Patent Owner further argues that a person having ordinary skill in the art would not have had a reasonable expectation of success in adapting Fang’s hafnium oxide etch-stop material to Kim’s silicon nitride etch-stop

¹³ We do not consider Petitioner to present an argument that Kim’s single layer embodiment should be combined with Kim’s two-layer embodiment, because Petitioner references Kim’s single layer embodiment only in asserting that “the presence or absence of a barrier layer does not impact either the motivation to combine or the expectation of success.” Pet. 73–74.

“because the prior art provides no guidance or disclosure.” PO Resp. 53 (citing Ex. 2019 ¶¶ 78, 85–87). Patent Owner also cites to its discussion of reasons to combine Fang and Kim in arguing that a person having ordinary skill in the art would not consider Fang a similar device to Kim. *Id.* (citing PO Resp. § IV.B.1).

Regarding the similarity of devices, we do not determine that the devices of Fang and Kim are different with respect to etch-stop layers such that adoption of Fang’s hafnium oxide or generic high-k material layer would present significant difficulties to one having ordinary skill in the art. Dr. Campbell testifies that a person having ordinary skill in the art would expect some experimentation for any deposition and etching. Ex. 1091, 106:23–107:10. As pointed out by Petitioner, Fang discusses hafnium oxide, as well other high-k materials, without discussion of needed adaptations for each individual film, indicating that Fang considered such alternative materials to be within the skill of one having ordinary skill in the art. Pet. Reply 20 (citing Ex. 1006); Ex. 1006 ¶ 22. Considering the record as a whole, including that discussed in our analysis of Petitioner’s rationale to combine, we determine that Petitioner has shown a reasonable expectation of success in the combination.

Consequently, we determine that Petitioner has shown, by a preponderance of the evidence, that the combined teachings of Kim and Fang would have rendered obvious claim 1. Patent Owner does not contest Petitioner’s assertions against any dependent claim except claim 6. PO Resp. 54–55. We further determine that Petitioner has shown the obviousness of claims 2, 4, 5, and 9–18, having further limitations for which Petitioner relies upon Kim, in the same manner as for its assertions based upon Kim alone. Pet. 64–69. We also agree that Petitioner has shown, by a

preponderance of the evidence, that Fang teaches anisotropic and chemical vapor deposition processes recited in claims 3 and 8, and we adopt Petitioner’s reasoning. *Id.* (citing Ex. 1006 ¶¶ 28, 8, 20). We further agree that Petitioner has shown, by a preponderance of the evidence, that the thickness range of claim 7 would have been obvious over the teachings of Kim and Fang, and adopt Petitioner’s reasoning. Pet. 68–69 (highlighting the similarity of their etch-stop layers and the lack of criticality as evidenced by the breadth of the cited range).

Claim 6 depends from claim 1 and limits “disposing the etch-stop layer” to “disposing hafnium oxide” or other listed materials. Petitioner relies on Fang’s teaching that an etch-stop layer may comprise a high-k dielectric material such as hafnium oxide. Pet. 67. Patent Owner refers to its arguments against claim 1, which we have addressed above and found unavailing. PO Resp. 54–55. We determine that Petitioner has shown, by a preponderance of the evidence, that claim 6 would have been obvious over the teachings of Kim and Fang.

F. Obviousness over Han and Fang

Petitioner asserts that claims 1–15 are unpatentable under 35 U.S.C. § 103 as obvious over Han in view of Fang. Pet. 74–103. Patent Owner argues against this assertion. PO Resp. 56–68.

Upon consideration of Petitioner’s explanations and the totality of evidence in the complete trial record, we are persuaded that Petitioner has shown, by a preponderance of the evidence, that claims 1–15 are unpatentable as being obvious over Han in view of Fang.

1. *Han*

Han is titled “Semiconductor Device and Method For Fabricating Same.” Ex. 1007, code (54). Han relates to providing a semiconductor substrate having an upper and lower structure with the upper structure having an opening exposing the lower conductor on the lower structure and a connection structure filling the opening and connected to the lower conductor. *Id.* at code (57).

2. *Analysis of Claim 1*

We begin our analysis of Petitioner’s obviousness contentions with Petitioner’s assertions as to claim 1.

[1.PRE] A method for forming a semiconductor structure, comprising: [1.A] forming a staircase structure comprising a plurality of steps, wherein the forming of each step of the plurality of steps comprises disposing a sacrificial layer over a dielectric layer;

Petitioner asserts that Han discloses a method of forming a semiconductor structure. Pet. 74 (citing Ex. 1007, code (54)). Petitioner asserts that Han also describes forming a staircase structure ST by disposing a sacrificial layer SL over an insulating (dielectric) layer ILD. *Id.* at 76–78 (citing Ex. 1007, Figs. 15–26). Patent Owner does not specifically contest these assertions. Based on the record, we agree that Petitioner has sufficiently shown Kim to teach or suggest limitations [1.PRE]¹⁴ and [1.A].

[1.B] disposing an etch-stop layer on each step of the plurality of steps, wherein the etch-stop layer comprises a second high-k dielectric layer

Petitioner asserts that Fang describes disposing etch stop material 130 in a layer on each step 110 of its staircase. Pet. 79 (citing Ex. 1007, Fig. 2,

¹⁴ We do not express an opinion on whether the preamble is limiting.

¶ 20). Petitioner points to Fang’s description that its etch stop material layer may comprise a high-k dielectric layer such as hafnium oxide. *Id.* at 79–80 (citing Ex. 1007 ¶ 22).

Patent Owner argues that Han’s features, such as a horizontal insulating layer surrounding the conductive layer of each step, remove the need for an etch stop layer and implicates different process considerations than in Fang, such that a person having ordinary skill in the art would not have made the proposed combination. PO Resp. 56–60. Patent Owner argues that Fang does not have a gate-stack-on-top configuration, and thus require an etch-stop layer to protect against punch-through whereas Han does not. *Id.* at 57. Patent Owner argues that adding an etch-stop layer to Han would require changes to etch parameters, additional etch steps, and different etch chemistries, resulting in additional cost, time, and complexity. *Id.* (citing Ex. 2019 ¶¶ 92–96).

Despite such concerns, the record shows that forming an etch-stop layer over staircases comprising high-k dielectric gate stack layers was known in the art. Petitioner points out that both Kim (Ex. 1003) and Park (Ex. 1004) apply etch-stop layers in that manner. Pet. Reply 21 (citing Ex. 1003, Fig. 22A, Ex. 1004, Fig. 9j).¹⁵ Petitioner also asserts that added layers reduce the likelihood of punch-through. Pet. 102. Dr. Banerjee persuasively attests that high-k dielectric layers “tend to be very thin” and “do not provide much additional safety margin.” Ex. 1085 ¶ 76. Dr. Campbell’s testimony supports this, stating that the high-k liner was “very thin . . . a few nanometers.” Ex. 1086, 75:10–25. Dr. Banerjee also

¹⁵ Patent Owner points to other embodiments of Kim, but the presence of other embodiments does not undermine the relevance of the embodiment relied upon by Petitioner. PO Sur-reply 20.

points to Han's staged etching process as indicating that its high-k dielectric layers "are not adequate as an etch-stop." Moreover, even to the extent that high-k dielectric layers may act as an etch stop, both declarants indicate that a thicker etch-stop layer is desirable, despite changes to the layer forming process. Ex. 2019 ¶ 92 ("a POSITA may also adjust the thickness of the protective high-k dielectric layers as needed to provide additional protection to the conductive layer during etching"); Ex. 2020, 17:6–8 ("[A] thicker etch-stop layer will provide more of an insurance policy, if you will."). With respect to considerations in changing etch conditions, Dr. Campbell has previously testified that a person having ordinary skill in the art would expect some experimentation for any deposition and etching. Ex. 1091, 106:23–107:10. Patent Owner also describes the relevant technology as typically requiring additional complexity for improvements. PO Resp. 27–28 (Fabrication of 3D NAND is as complex as the devices themselves and "involves a number of new and *complex process steps*."). Thus, the evidence of record indicates that a person having ordinary skill in the art would have known of the use and desirability of etch-stop layers atop high-k dielectric layers.

Petitioner further points to Dr. Campbell's testimony that Han's staged-etching process involves multiple masks. Pet. Reply 22 (citing Ex. 1086, 144:18–145:24). Petitioner asserts that this provides another reason to apply Fang's teachings of an etch stop to Han, because Fang teaches that using multiple masks incurs "additional processing acts, complexity, and costs." *Id.* (citing Pet. 102 (citing Ex. 1006 ¶ 4)). Petitioner cites to Fang's description that an etch-stop layer resolves this problem "to reduc[e] the likelihood of punch through." Pet. 102 (citing Ex. 1006 ¶¶ 26, 28). Petitioner also argues that Dr. Campbell states that Han's step-by-step,

multiple mask process may mitigate punch-through whereas the etch stop layer would “undisputedly solve[]” it. Pet. Reply 22; Ex. 2019 ¶ 93. Thus, the evidence of record indicates an advantage to be gained by replacing Han’s staged etching with an etch-stop layer as taught by Fang.

Patent Owner also points to the differences between Han’s gate-stack-on-top model and Fang’s different structure. PO Resp. 58 (citing its arguments at § III.A.2. against reordering the layers in Petitioner’s Kim-based assertions). However, Patent Owner’s cited arguments with respect to Petitioner’s reordering of Kim’s layers address issues with reordering of the layers. *Supra* at 16–17. Here, it is uncontested that Han teaches the claimed layer ordering. *Supra* at 31–32. Patent Owner’s arguments at § III.A.2 of the Patent Owner Response address reordering the sacrificial and insulating layers in the context of limitation [1.A] but do not address issues related to adding an etch-stop layer in the context of limitation [1.B].

Based on the foregoing, we determine that the evidence of record supports Petitioner’s assertion that a person having ordinary skill in the art would have combined the teachings of Han and Fang to teach limitation [1.B].

[1.C] disposing an insulating layer on the etch-stop layer; [1.D] replacing the sacrificial layer of each step with a gate stack, the gate stack comprising a conductive layer and a first high-k dielectric layer; [1.E] forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer; [1.F] etching the exposed portions of the etch-stop layer in the plurality of openings and exposing at least a portion of the conductive layer of each step; [1.G] forming a plurality of conductive structures in each of the plurality of openings.

Patent Owner does not contest Petitioner’s assertions for limitations [1.C]–[1.G]. PO Resp. Petitioner asserts that these limitations are taught by Fang’s insulating layer 135 atop its etch-stop layer 130, Han’s insulating

layer 200, Han's replacement of its sacrificial layers SL with a conductive layer of electrodes EL and a high-k dielectric layer of horizontal insulating material that may comprise high-k dielectric layers TIL or BK, Fang's forming a plurality of openings 145 to expose portions of etch-stop material 130 and etching the exposed portions 130 to expose portions of conductive materials 140 of each step, and Han's teachings of forming a plurality of conductive structures PLG1 and PLG2 in each of a plurality of openings LH and UH in the etch-stop layer reaching the conductive layer of each step. Pet. 80–90. We have reviewed these assertions and found them to be sufficiently supported by the record.

For the above-described reasons, we determine that Petitioner has shown, by a preponderance of the evidence, that claim 1 would have been obvious over the combination of Han and Fang.

3. *Claims 2–15*

Patent Owner does not contest Petitioner's assertions for dependent claims 2, 3, and 6–15. PO Resp. We have reviewed these assertions and found them to be sufficiently supported by the record. Pet. 90–101. We adopt Petitioner's reasoning, and determine that Petitioner has shown, by a preponderance of the evidence, that claims 2, 3, and 5–15 would have been obvious over the combination of Han and Fang.

Patent Owner does contest Petitioner's assertions for dependent claims 4 and 5; in particular, Petitioner's reliance on the knowledge of the prior art to meet those limitations. PO Resp. 60–62. We have addressed and found unavailing Patent Owner's arguments based upon a recent USPTO memorandum that, by its provisions, does not apply to this proceeding. *Supra* § II.D.4.

Patent Owner further disputes Petitioner's reliance on general knowledge to supply the limitations of claims 4 and 5. PO Resp. 25–28, 60–62. As discussed, although our case law rejects obviousness determinations based on conclusory and unsupported expert testimony, it permits the general knowledge in the art, where sufficiently established, to be considered. *See Philips*, 948 F.3d at 1338 (determining that general knowledge may be shown by evidence corroborated by specific prior art).

Here, the Petition provides evidence to support its assertions that the background knowledge in the art would have made obvious the additional limitations of claims 4 and 5. Pet. 91–92 (citing Exs. 1025–1027), 50–52 (citing Ex. 1003 ¶¶ 108–09; Ex 1006 ¶ 28; Exs. 1023, 1024). We have determined that such evidence is sufficient to show the obviousness of these limitations. *Supra* § II.D.4–5.

For claim 4, Petitioner specifically relies upon the teachings of Fang in view the teachings of the prior art. Pet. 92 (citing Ex. 1006 ¶¶ 8, 29). Specifically, that Fang teaches its etch-stop layer is selectively etchable relative to other materials and that it is removed to expose the underlying layer. *Id.* Dr. Campbell's testimony that the "gate is the part of the device that has to be retained" further supports that the gate be less amenable to etching than the etch-stop layer. Ex. 1086, 91–92. Combined with the evidence of the prior art that etch-stop materials may be etchable at a higher rate than conductive materials, we determine that Petitioner has shown, by a preponderance of the evidence, that claim 4 would have been obvious over the combined teachings of Han and Fang.

For claim 5, Petitioner relies upon its reasoning and evidence presented in its Kim-based assertions. Pet. 92 (citing Pet. § X.E.1). Petitioner further proffers an example of a high-k Al₂O₃ etch-stop layer has a

higher etching rate than high-k HfO₂ dielectric layers relative to argon plasma. *Id.* (citing Exs. 1003, 1027).

Patent Owner argues that a person having ordinary skill in the art “would not have a reasonable expectation of success achieving the claimed arrangement combining Han in view of Fang where neither device itself is designed to include both an etch-stop layer and a first high-k dielectric layer.” PO Resp. 62 (citing Ex. 2019 ¶¶ 100–103). Patent Owner also repeats its arguments against Petitioner’s Kim-based assertions for claim 5. *Id.* Patent Owner also addresses Petitioner’s argon etching example; while agreeing that the example represents the claimed higher etching rate of an etch stop layer than a high-k layer, Patent Owner argues that the materials differ from those in Han and Fang, and that the argon etchant would not be used in the complex silicon technology at issue. *Id.* at 63. Ex. 2019 ¶ 102.

As noted by Dr. Campbell, Dr. Banerjee relies on prior art to support his statements that the relative etching rates have a sensible relationship, in which the etching rate of the etch-stop layer is greater than the etching rate of the high-k layer. Ex. 2019 ¶¶ 65, 103 (citing Ex. 1003 ¶ 110). As discussed in relation to Petitioner’s Kim-only and Kim and Fang grounds, and with respect to limitation [1.B] of Petitioner’s Han and Fang ground, we have found these arguments unavailing. *Supra* §§ II.D.5, II.D.E, II.F.2. Dr. Banerjee’s “sensible relationship” statement is clearly supported by Kim, which does have both an etch stop layer and a high-k layer, and by Williams (Exhibit 1024), which states that under dry etching, the etching of a silicon nitride etch-stop layer occurs at a significantly greater rate than an aluminum oxide layer (which is Kim’s high-k dielectric material). *Supra* § II.D.5; Ex. 1003 ¶¶ 99, 103 (citing Ex. 1005 ¶¶ 151, 187; Ex. 1024 ¶¶ 17, 29).

Although Patent Owner and Dr. Campbell take issue with Dr. Banerjee's specific example using an argon etchant, neither contests Dr. Banerjee's underlying attestation that different materials have different etching rates. Ex. 1003 ¶110, Pet. 52; PO Resp. 63; PO Sur-reply 22. Instead, Dr. Campbell's testimony appears to confirm Dr. Banerjee's. Ex. 2019 ¶ 100 ("the claimed etch relationships are highly dependent upon the specific materials used."). Dr. Campbell's testimony that the "gate is the part of the device that has to be retained" further supports that the layer closest to the gate (the high-k layer) be less amenable to etching than the layer above it (the etch-stop layer). Ex. 1086, 91:22–24. Taken as a whole, the evidence in the prior art supports Dr. Banerjee's opinion that for an etch-stop layer over a different high-k dielectric layer, it would have been understood in the prior art that having the etch rate of the etch-stop layer be greater than the etch rate of the high-k layer was a known, sensible option.

Based on the entirety of the record, we determine that Petitioner has shown, by a preponderance of the evidence, that claim 5 would have been obvious over the combined teachings of Han and Fang.

G. Obviousness of Han, Fang, and Chen

Petitioner asserts that claims 17 and 18 would have been obvious over the combined teachings of Han and Fang as applied to claims 1–15, and further in view of Chen. Pet. 103–107. Patent Owner contests the motivation to combine Chen with Han and Fang. PO Resp. 63–68.

Claim 17 recites, "The method of claim 1, further comprising: prior to disposing the etch-stop layer, disposing a barrier layer on each step of the plurality of steps, wherein the barrier layer protects underlying structures during the etching of the exposed portions of the etch-stop layer."

Claim 18 recites, “The method of claim 17, wherein disposing the barrier layer comprises disposing one or more of silicon oxide, silicon oxynitride, silicon nitride, TEOS, aluminum oxide: and silicon oxide incorporated with F, C, N, or H.”

Petitioner asserts that motivation to combine Chen’s barrier layer with Han’s staircase structure and Fang’s etch-stop layer is provided by Chen’s solution to “a short-circuit phenomenon through electron tunneling between conductive layers of a word-line staircase.” Pet. 105 (citing Ex. 1008 ¶ 49). Petitioner asserts that Chen’s solution was to increase the tunneling length of the etch-stop layer(s) to reduce tunneling current, thereby “more effectively electrically isolat[ing] [the conductive layers] from one another.” *Id.* (citing Chen ¶ 4). Petitioner points to Chen’s Figures 8B and 8D as illustrating that adding a barrier layer increases the total tunneling length. Pet. 106 (citing Ex. 1008 ¶¶ 48, 52, Figs. 8B, 8D). Petitioner asserts that “by adding a barrier layer to a high-k dielectric etch-stop layer, ‘the overall etching stop layer 200 [including the barrier layer] can further provide a relatively large tunneling length,’ reducing the ‘occurrence of short circuit between different conductive layers’ and increasing ‘the stability of the semiconductor device.’” *Id.* (quoting Ex. 1008 ¶ 53).

Patent Owner argues that just as Fang’s added etch-stop layer provides no benefit to Han’s punch-through-protected method, adding further protective layers from Chen would also provide no benefit. PO Resp. 65–66 (citing Ex. 2019 ¶¶ 105–106). We have found this argument unavailing for Petitioner’s Han and Fang assertions, and for the same reasons, we find this argument unavailing to show that a person having ordinary skill would not have recognized improved protection from adding Chen’s protective layers. *Supra* § II.F.2.

Patent Owner further argues that because Han already has two high-k dielectric layers, and Fang adds a third, Chen's fourth layer would be redundant and increase process complexity, cost, and time. PO Resp. 66 (citing Ex. 2019 ¶ 107). Patent Owner argues that a person having ordinary skill would not be motivated to add such layers where they can be avoided. *Id.*

We determine that the record supports Petitioner's assertions. Petitioner points to Dr. Campbell's deposition testimony in another proceeding agreeing that a "barrier layer provides flexibility in terms of processing parameters," and the choice between one or two etch stops represents a "common tradeoff in engineering." Pet. Reply 26 (citing Ex. 1091, 46:13–47:21.) Thus, adding a barrier layer represents a balance between some increase to complexity, cost, and time of processing, and reducing the occurrence of short circuits to increase device stability. "[A] given course of action often has simultaneous advantages and disadvantages, and this does not necessarily obviate motivation to combine." *Allied Erecting & Dismantling Co. v. Genesis Attachments, LLC*, 825 F.3d 1373, 1381 (Fed. Cir. 2016). Patent Owner describes complexity, cost, and time as being features of 3D NAND processing technology. PO Resp. 27–28 (citing Ex. 2022, 293; Ex. 1023, 3–4). Advances in this technology are expected to add complexity. Ex. 2024, 5 ("With each generation, the fabrication of 3D NAND becomes more complex") (quoted at PO Resp. 28). Thus, some increase in complexity, cost, and time are expected in advances in the technology at issue. As a whole, the record indicates that the process parameter flexibility and reduced risk of short circuit provided by Chen's barrier layer would have outweighed such concerns. Therefore, we

determine that Petitioner has shown by a preponderance of the evidence that claims 17 and 18 would have been obvious over Han, Fang, and Chen.

III. CONCLUSION¹⁶

After reviewing the record and weighing the evidence offered by both parties, we determine that Petitioner shows by a preponderance of the evidence that claims 1–18 are unpatentable.

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1, 2, 4, 5, 9–18	103	Kim	1, 2, 4, 5, 9– 18	
1–18	103	Kim, Fang	1–18	
1–15	103	Han, Fang	1–15	
17, 18	103	Han, Fang, Chen	16, 17	
Overall Outcome			1–18	

¹⁶ Should Patent Owner wish to pursue amendment of the challenged claim in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

I. ORDER

For the foregoing reasons, it is:

ORDERED that Petitioner has established by a preponderance of the evidence that claims 1–18 are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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