(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
07 March 2019 (07.03.2019)

WIPO | PCT

(10) International Publication Number
WO 2019/042091 A1

(51) International Patent Classification:
H01L 27/11551 (2017.01) *H01L 27/11578* (2017.01)

(21) International Application Number:
PCT/CN2018/098962

(22) International Filing Date:
06 August 2018 (06.08.2018)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
201710750398.4 28 August 2017 (28.08.2017) CN

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(54) Title: STAIRCASE STRUCTURE FOR MEMORY DEVICE

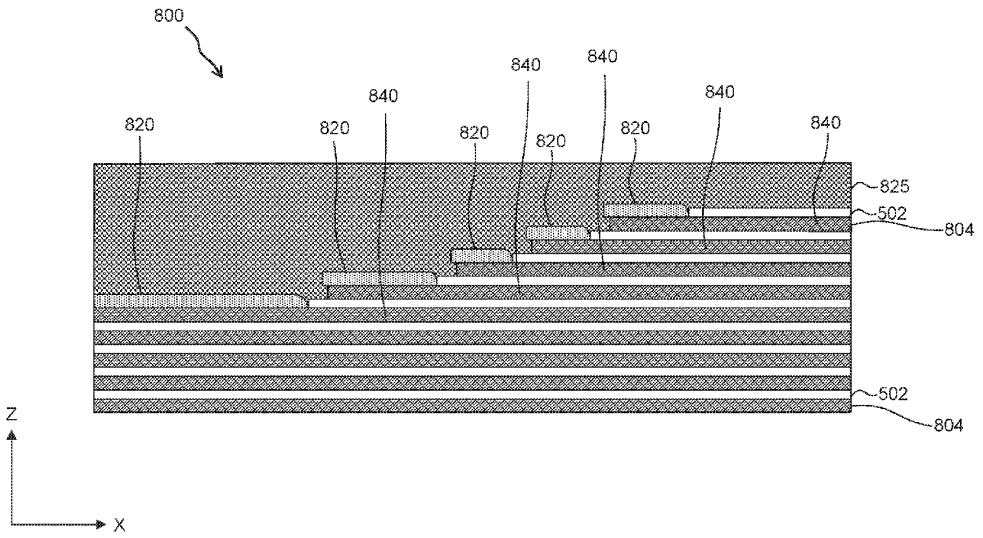

FIG. 8

(57) Abstract: A semiconductor structure is disclosed. The semiconductor structure includes a staircase structure (800) disposed over a substrate (101). The staircase structure (800) includes a plurality of layer stacks, where each layer stack is made of a first material layer (502) over a portion of a second material layer (840). The staircase structure (800) further includes a plurality of landing pads (820), where each landing pad (820) is disposed over another portion of the second material layer (840) of a respective layer stack.

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(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

STAIRCASE STRUCTURE FOR MEMORY DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority of Chinese Patent Application No. 201710750398.4 filed on August 28, 2017, the entire content of which is incorporated herein by reference.

BACKGROUND

[0002] Planar memory cells are scaled to smaller sizes by improving process technology, circuit design, programming algorithm, and fabrication process. However, as feature sizes of the memory cells approach a lower limit, planar process and fabrication techniques become challenging and costly. As a result, memory density for planar memory cells approaches an upper limit.

[0003] A three-dimensional (3D) memory architecture can address the density limitation in planar memory cells. The 3D memory architecture includes a memory array and peripheral devices for controlling signals to and from the memory array. The 3D memory architecture also includes a stack of word lines horizontally arranged over a substrate, with vertical semiconductor channels that intersect the word lines. The intersection of a word line and a vertical semiconductor channel forms a memory cell.

BRIEF SUMMARY

[0004] Embodiments of the present disclosure are directed to a staircase structure for a memory device (e.g., 3D memory device). The disclosed embodiments provide numerous benefits including, but not limiting to, yield and manufacturing cost improvements.

[0005] In some embodiments, a semiconductor structure includes a staircase structure disposed over a substrate. The staircase structure includes a plurality of layer stacks,

where each layer stack includes a first material layer disposed over a first portion of a second material layer. The staircase structure further includes a plurality of landing pads respectively disposed on the plurality of layer stacks, where each landing pad is disposed over a second portion of the second material layer of a respective layer stack. Each of the landing pads is adjacent to a respective side of the first material layer and extends over a respective top surface of the second material layer. The first material layer is made of an insulating material, including silicon oxide, aluminum oxide or a combination thereof. The second material layer is made of a first conductive material. The plurality of landing pads are made of a second conductive material. The first conductive material can be the same or different from the second material. Each of the first and the second conductive materials includes tungsten, silicide, nickel, titanium, platinum, aluminum, titanium nitride, tantalum nitride, tungsten nitride, or a combination thereof. The second material layer of each layer stack is disposed over a portion of the first material layer of an adjacent layer stack. One of the plurality of landing pads is thicker than the first material layer of a corresponding layer stack and is insulated from another landing pad disposed on an adjacent layer stack.

[0006] In some embodiments, a method for forming a semiconductor structure includes forming a plurality of layer stacks over a substrate, where each layer stack includes a first material layer over a portion of a second material layer. The method further includes forming a hard mask layer over the plurality of layer stacks, forming a staircase structure on the plurality of layer stacks to expose a portion of the first material layer of each layer stack, forming a landing pad over a portion of the second material layer of the each layer stack, and removing the portion of the hard mask layer. The method further includes removing the landing pad and the second material layer of the each layer stack to form a recess in each layer stack, disposing a conductive material in the recess of each layer stack, and forming a dielectric layer over the staircase structure. The formation of the landing pad includes removing a portion of the second material layer from a side of each layer stack to form a recess, disposing a material layer over the staircase structure to fill the recess in each layer stack and removing a portion of the material layer to form a spacer at the side of each layer stack and a side of the portion of the hard mask layer. The formation of the landing pad further includes removing a portion of the first material layer of each layer stack using the spacer and the portion of the hard mask layer as a mask, disposing a dielectric layer over the staircase structure and removing the spacer and a

portion of the dielectric layer. The disposing of the dielectric layer over the staircase structure includes disposing the dielectric layer over a portion of the second material layer, a portion of a side of the first material layer and a portion of a side of the spacer. The removing of the portion of the hard mask and the portion of the top layer stack in the plurality of layer stacks includes using dry etching, wet etching or a combination thereof. The trimming the mask stack include etching the mask stack incrementally and inwardly from a boundary of the mask stack. The removing of the portion of the hard mask includes using a wet etch process with tetramethylammonium hydroxide (TMAH), potassium hydroxide (KOH), a base, or a combination thereof. The formation of each layer stack and the hard mask layer includes deposition techniques using chemical vapor deposition (CVD), physical vapor deposition (PVD), plasma-enhanced CVD (PECVD), low pressure CVD (LPCVD), sputtering, metal-organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), or a combination thereof.

[0007] In some embodiments, a memory device includes a memory string disposed over the substrate and a staircase structure disposed adjacent to the memory string. The staircase structure includes a plurality of layer stacks, where each layer stack of the plurality of layer stacks includes an insulating layer disposed over a first portion of the a conductive layer, where a second portion of the conductive layer is in contact with a side surface of the insulating layer. The conductive layer of the each layer stack is disposed over a portion of the insulating layer of an adjacent layer stack. The second portion of the conductive layer is thicker than the first portion of the conductive material layer.

[0008] Other aspects of the present disclosure can be understood by those skilled in the art in light of the description, the claims, and the drawings of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate embodiments of the present disclosure and, together with the description, further serve to explain the principles of the present disclosure and to enable a person skilled in the art to make and use the present disclosure.

[0010] FIG. 1 illustrates a cross-sectional view of a hard mask layer and a plurality of dielectric layer pairs over a substrate, according to some embodiments.

[0011] FIG. 2A illustrates a cross-sectional view of a staircase structure, according to some embodiments.

[0012] FIG. 2B illustrates a cross-sectional view of a staircase structure, according to some embodiments.

[0013] FIG. 3 illustrates a cross-sectional view of a staircase structure with a material layer disposed therein, according to some embodiments.

[0014] FIG. 4 illustrates a cross-sectional view of a staircase structure with spacers, according to some embodiments.

[0015] FIG. 5 illustrates a cross-sectional view of a staircase structure after removal of an insulating layer, according to some embodiments.

[0016] FIG. 6 illustrates a cross-sectional view of a staircase structure with a dielectric layer disposed thereon, according to some embodiments.

[0017] FIG. 7 illustrates a cross-sectional view of a staircase structure with landing pads, according to some embodiments.

[0018] FIG. 8 illustrates a cross-sectional view of a staircase structure with a dielectric layer disposed thereon, according to some embodiments.

[0019] FIG. 9 is a flowchart of a method for forming a memory device, according to some embodiments.

DETAILED DESCRIPTION

[0020] Although specific configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the art will recognize that other configurations and arrangements can be used without departing from the spirit and scope of the present disclosure. It will be apparent to a person skilled in the art that the present disclosure can also be employed in a variety of other applications.

[0021] It is noted that references in the specification to "one embodiment," "an embodiment," "an example embodiment," "some embodiments," etc., indicate that the embodiment described can include a particular feature, structure, or characteristic, but every embodiment can not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in connection with an embodiment, it would be within the knowledge of a person skilled in the art to

affect such feature, structure or characteristic in connection with other embodiments whether or not explicitly described.

[0022] In general, terminology can be understood at least in part from usage in context. For example, the term "one or more" as used herein, depending at least in part upon context, can be used to describe any feature, structure, or characteristic in a singular sense or can be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as "a," "an," or "the," again, can be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context. In addition, the term "based on" can be understood as not necessarily intended to convey an exclusive set of factors and may, instead, allow for existence of additional factors not necessarily expressly described, again, depending at least in part on context.

[0023] The meaning of "on," "above," and "over" in the present disclosure should be interpreted in the broadest manner such that "on" not only means "directly on" something, but also includes the meaning of "on" something with an intermediate feature or a layer therebetween. Moreover, "above" or "over" not only means "above" or "over" something, but can also include the meaning it is "above" or "over" something with no intermediate feature or layer therebetween (i.e., directly on something).

[0024] Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper," and the like, can be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus can be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein can likewise be interpreted accordingly.

[0025] As used herein, the term "substrate" refers to a material onto which subsequent material layers are added. The substrate includes a top surface and a bottom surface. The top surface of the substrate is where a semiconductor device is formed, and therefore the semiconductor device is formed at a top side of the substrate. The bottom surface is opposite to the top surface and therefore a bottom side of the substrate is opposite to the top side of the substrate. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium

arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.

[0026] As used herein, the term "layer" refers to a material portion including a region with a thickness. A layer has a top side and a bottom side where the bottom side of the layer is relatively close to the substrate and the top side is relatively away from the substrate. A layer can extend over the entirety of an underlying or overlying structure, or can have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any set of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend horizontally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow. A layer can include multiple layers. For example, an interconnect layer can include one or more conductor and contact layers (in which contacts, interconnect lines, and/or vias are formed) and one or more dielectric layers.

[0027] As used herein, the term "nominal/nominally" refers to a desired, or target, value of a characteristic or parameter for a component or a process operation, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term "about" indicates the value of a given quantity that can vary based on a particular technology node associated with the subject semiconductor device. Based on the particular technology node, the term "about" can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., ±10%, ±20%, or ±30% of the value).

[0028] In the present disclosure, the term "horizontal/horizontally/lateral/laterally" means nominally parallel to a lateral surface of a substrate.

[0029] As used herein, the term "3D memory device" refers to a semiconductor device with vertically oriented strings of memory cell transistors (referred to herein as "memory strings," such as NAND strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate. As used herein, the term "vertical/vertically" means nominally perpendicular to the lateral surface of a substrate.

[0030] In some embodiments, a NAND string or a 3D memory device includes a semiconductor channel (e.g., a silicon channel) that extends vertically through a plurality conductor/dielectric layer pairs, where the semiconductor channel is surrounded by a dielectric stack. The plurality of conductor/dielectric layer pairs are also referred to herein as an "alternating conductor/dielectric stack." The conductor layer of the alternating conductor/dielectric stack can be used as a word line (e.g., to electrically connect one or more control gates). An intersection of a word line and the semiconductor channel forms a memory cell. Vertically-oriented memory strings require an electrical connection between a word line and an access line (e.g., back end of line (BEOL) interconnection) to select a memory cell along the memory string for read and write functions, where the electrical connection is provided by forming a staircase structure at the plurality of conductor/dielectric pairs.

[0031] The 3D memory device can include a plurality of staircase structures disposed adjacent to a plurality of memory strings for word line fan-out, according to some embodiments. As the demand for higher storage capacity continues to increase, the number of vertical levels of the staircase structures also increases. As a result, when applying a BEOL process to form interconnects on the staircase structures, an upper portion of the staircase structures is exposed to the BEOL process for a longer period of time than a lower portion of the staircase structures. This differential in BEOL exposure time increases the process variation of the final 3D memory device, thus introducing challenges in balancing manufacturing yield and process complexity/cost.

[0032] In the present disclosure, a staircase structure refers to a set of surfaces that include at least two horizontal surfaces (e.g., along an x-y plane) and at least two vertical surfaces (e.g., along a z-axis). Each horizontal surface is adjoined to a first vertical surface that extends upward from a first edge of the horizontal surface, and is also adjoined to a second vertical surface that extends downward from a second edge of the horizontal surface. Each of the horizontal surfaces is referred as a "step" or "stair" of the staircase structure. A horizontal direction can refer to a direction (e.g., the x-axis or the y-axis) parallel with a top surface of the substrate (e.g., the substrate that provides the fabrication platform for formation of structures over it). A vertical direction can refer to a direction (e.g., the z-axis) perpendicular to the top surface of the structure.

[0033] The staircase structure can be formed from a plurality of layer stacks by repetitively etching and trimming the each layer stack using a mask layer, where each

layer stack is also referred to as a "staircase layer" (or "SC layer") of the staircase structure in the present disclosure. A step of the staircase structure exposes a portion of a top surface of a layer stack (e.g. a SC layer) of the plurality of layer stacks. In some embodiments, the staircase structure includes a plurality of layer stacks.

[0034] FIG. 1 illustrates a structure 100 with an alternating layer stack formed over a substrate 101 and a hard mask layer 106 formed over the alternating layer stack. A layer stack within the alternating layer stack can include a dielectric layer pair with an insulating layer 102 over a sacrificial layer 104. In some embodiments, sacrificial layer 104 can be disposed over insulating layer 102. Insulating layer 102 can include silicon oxide. Sacrificial layer 104 can include silicon nitride. In some embodiments, a thickness of insulating layer 102 or sacrificial layer 104 is between 10 nm and 200 nm. In some embodiments, a thickness of hard mask layer 106 is between 10 nm and 200 nm. In some embodiments, the layers in the alternating layer stack can be different thicknesses.

[0035] In some embodiments, substrate 101 includes any suitable material for supporting a memory structure (e.g., 3D memory structure). For example, substrate 101 can include silicon, silicon germanium, silicon carbide, silicon on insulator (SOI), germanium on insulator (GOI), glass, gallium nitride, gallium arsenide, any suitable III-V compounds, any other suitable material, or combinations thereof.

[0036] In some embodiments, sacrificial layer 104 can include any suitable material different from insulating layer 102. For example, sacrificial layer 104 can include poly-crystalline silicon, silicon nitride, poly-crystalline germanium, poly-crystalline germanium-silicon, any other suitable materials, or combinations thereof. In some embodiments, sacrificial layer 104 can include silicon nitride.

[0037] Insulating layer 102 can include any suitable insulating materials, such as silicon oxide or aluminum oxide.

[0038] In some embodiments, sacrificial layer 104 can be a conductive material layer. The conductive material layer can include any suitable conductive material. In some embodiments, the conductive material layer can include poly-crystalline silicon, tungsten, silicide, nickel, titanium, platinum, aluminum, titanium nitride, tantalum nitride, tungsten nitride, any other suitable material, or combinations thereof.

[0039] In some embodiments, hard mask layer 106 can be a poly-crystalline semiconductor layer including poly-crystalline silicon, poly-crystalline germanium, poly-crystalline germanium-silicon, any other suitable material, or combinations thereof. In

some embodiments, hard mask layer 106 can be a metal layer, including cobalt, nickel, tungsten, copper, or silver. In some embodiments, hard mask layer 106 can be a metal silicide layer, including $CoSi_x$, $NiSi_x$, or WSi_x. In some embodiments, hard mask layer 106 can be an organic material layer formed by spin-coating or self-assembling of organic molecules.

[0040] The formation of insulating layer 102, sacrificial layer 104, and hard mask layer 106 can include any suitable deposition methods such as, for example, chemical vapor deposition (CVD), physical vapor deposition (PVD), plasma-enhanced CVD (PECVD), low pressure chemical vapor deposition (LPCVD), sputtering, metal-organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), sputtering, thermal evaporation, e-beam evaporation, molecular beam-epitaxy (MBE), any other suitable deposition method, or combinations thereof. In some embodiments, insulating layer 102, sacrificial layer 104, the conductive material layer, and hard mask layer 106 are each formed by CVD. In some embodiments, the formation of hard mask layer 106 further includes applying a thermal anneal process to form a silicide layer.

[0041] FIGs. 2A-2B illustrate a cross-sectional view of staircase structures 200A and 200B, according to some embodiments. Staircase structure 200A includes a hard mask 206 and a plurality of layer stacks 202/204. Each layer stack 202/204 is also referred to herein as an "SC layer." The steps in staircase structure 200A is formed by repeating an etch-trim process on structure 100 using a mask stack (not shown). After the formation of the steps, the mask stack is removed. In some embodiments, a step exposes a portion of a top surface of an SC layer. In some embodiments, a step exposes a side of a SC layer. In some embodiments, after repeating the etch-trim process, a portion of a top-most SC layer of staircase structure 200A is exposed and another portion of the top-most SC layer is covered by hard mask layer 206. An etch process is also applied to laterally etch a portion of sacrificial layer 204 of each SC layer. As a result, each step of staircase structure 200B has a recess (e.g. recess 220, 222, 224…, etc.). In some embodiments, a lateral dimension of each recess is between 10 nm and 300 nm. In some embodiments, a lateral dimension "a" of each step is between 100 nm and 1500 nm.

[0042] In some embodiments, the mask stack (not shown in FIG. 2A) can include a photoresist or carbon-based polymer material. In some embodiments, the mask stack is removed after forming staircase structure 200A. The etch-trim process includes an etch process and a trim process. In some embodiments, the etch process includes using any

suitable etchants (e.g., wet etch and/or dry etch) to sequentially remove a portion of hard mask layer 106 and a portion of the layer stack, including a portion of insulating layer 102 and a portion of sacrificial layer 104. For example, as shown in FIG.2A, hard mask layer 206, insulating layer 202, and sacrificial layer 204 are formed after removing a portion of hard mask layer 106, a portion of insulating layer 102, and a portion of sacrificial layer 104.

[0043] In the etch process, an etchant for insulating layer 102 has a higher etching selectivity over sacrificial layer 104, and/or vice versa. In some embodiments, the etchant for hard mask layer 106 has a higher etching selectivity over insulating layer 102 and sacrificial layer 104, and/or vice versa. Accordingly, an underlying layer stack can function as an etch-stop layer so that a single layer stack is patterned/etched, according to some embodiments. In some embodiments, insulating layer 102 and sacrificial layer 104 are etched using an anisotropic etch process, such as reactive ion etch (RIE) or other dry etch process. In some embodiments, the etchant includes carbon-fluorine (CF_4) based gases or hexafluoroethane (C_2F_6) based gases. In some embodiments, an etchant includes phosphoric acid and can be used to remove both insulating layer 102 and sacrificial layer 104. The methods and etchants to remove the layer stack described herein are exemplary. Other methods and etchants are within the spirit and scope of the present disclosure.

[0044] The trim process includes applying a suitable etch process (e.g., an isotropic dry etch or a wet etch) on the mask stack at directions parallel to a surface of the substrate. The mask stack is etched incrementally and inwardly from a boundary of the mask stack. The amount of trimmed mask stack can be related to the lateral dimension "a" of each steps of staircase structure 200A.

[0045] The process for forming the recess structure (e.g. recess 220, 222, 224…, etc.) uses an etch process similar to the etching techniques for removing sacrificial layer 104 as described above. In some embodiments, the process etches sacrificial layer 204 at a higher etching rate than that of insulating layer 202 or hard mask layer 206.

[0046] FIG. 3 illustrates a cross-sectional view of a staircase structure 300 with a material layer 310 disposed thereon, according to some embodiments. Material layer 310 is conformally disposed on staircase structure 200B, including on a top surface of hard mask layer 206, a side of hard mask layer 206, a top surface of each SC layer (e.g. each step) of staircase structure 200B, and a recess of the each SC layer. In some embodiments, material layer 310 fills each recesses of staircase structure 200B. Material layer 310 can

be made of similar material as hard mask layer 106, where the formation of material layer 310 can be similar to that of hard mask layer 106. In some embodiments, a thickness of material layer 310 is thicker than that of sacrificial layer 204. In some embodiments, a thickness of material layer 310 is thinner than that of the SC layer.

[0047] FIG. 4 illustrates a cross-sectional view of a staircase structure 400 with spacers 410, according to some embodiments. Each of spacers 410 is formed at a side of each SC layer of staircase structure 300. In some embodiments, spacer 410 is formed at a side of hard mask layer 206. Spacer 410 is formed by removing a portion of material layer 310 from staircase structure 300 using similar techniques as removing hard mask layer 106. In some embodiments, material layer 310 is removed from a top surface of staircase structure 300 and a top surface of hard mask layer 206. In some embodiments, spacer 410 fills a recess (e.g. recess 220, 222, or 224) of each SC layer of staircase structure 300. In some embodiments, spacer 410 covers a side of sacrificial layer 204 of each SC layer of staircase structure 300. In some embodiments, spacer 410 covers a portion of a side of insulating layer 202 of each SC layer of staircase structure 300. In some embodiments, spacer 410 and hard mask layer 106 are made of the same material.

[0048] FIG. 5 illustrates a cross-sectional view of a staircase structure 500 after removal of a portion of insulating layer 202, according to some embodiments. In FIG. 5, the portion of insulating layer 202 of each SC layer of staircase structure 400 is removed using spacers 410 and hard mask layer 206 as masks. Insulating layer 502 is formed after removing the portion of insulating layer 202 using similar techniques as removing insulating layer 102. As illustrated in FIG. 5, each SC layer of staircase structure 500 exposes a portion of a top surface of sacrificial layer 204 and spacer 410 of each SC layer. In some embodiments, a side of insulating layer 502 of each SC layer of staircase structure 500 is exposed.

[0049] FIG. 6 illustrates a cross-sectional view of a staircase structure 600 with a dielectric layer 620 disposed thereon, according to some embodiments. Dielectric layer 620 covers a top surface of staircase structure 500 and a portion of a side of staircase structure 500. In some embodiments, dielectric layer 620 covers a portion of each spacer 410 of staircase structure 500. In some embodiments, dielectric layer 620 covers a top surface of hard mask layer 206, a portion of a top surface of sacrificial layer 204, and a portion of a side of insulating layers 502 of each SC layer of staircase structure 500. In some embodiments, dielectric layer 620 has poor step-coverage on staircase structure 500.

For example, the poor step-coverage includes a thickness of dielectric layer 620 that is substantially thinner at a side of staircase structure 600 than that at a top surface of staircase structure 600. In some embodiments, dielectric layer 620 is discontinuous between each SC layer of staircase structure 600. In some embodiments, a portion of spacer 410 or a portion of a side of insulating layer 502 of each SC layer of staircase structure 600 is exposed.

[0050] In some embodiments, dielectric layer 620 can be a nitride layer, including silicon nitride, silicon oxynitride, any suitable materials, or combinations thereof. In some embodiments, dielectric layer 620 and each sacrificial layer 204 of staircase structure 600 are made of the same material. In some embodiments, a thickness of dielectric layer 620 at a top surface of staircase structure 600 is thinner than that of insulating layer 502 of each SC layer of staircase structure 600. Dielectric layer 620 can be formed using deposition techniques including, but not limiting to plasma-enhanced CVD (PECVD), low pressure CVD (LPCVD), physical vapor deposition (PVD), high density plasma (HDP), atomic layer deposition (ALD), any suitable deposition techniques, or combinations thereof.

[0051] FIG. 7 illustrates a cross-sectional view of a staircase structure700 with landing pads 720, according to some embodiments. In FIG. 7, spacers 410 and a portion of dielectric layer 620 are removed from staircase structure 600. After removing spacers 410 and the portion of dielectric layer 620, a landing pad 720 is formed over each SC layer of staircase structure 700. As shown in FIG. 7, landing pad 720 is in contact with sacrificial layer 204 of each SC layer of staircase structure 700. Both landing pad 720 and sacrificial layer 204 of the SC layer are disposed over a portion of insulating layer 502 of another vertically adjacent SC layer. In some embodiments, landing pad 720 is formed over hard mask layer 206. In some embodiments, landing pad 720 of a SC layer is thicker than insulating layer 502 of the SC layer. Landing pad 720 can also be discontinuous from another landing pad 720 disposed on another vertically adjacent SC layer. In some embodiments, landing pad 720, dielectric layer 620 and sacrificial layer 204 are made of the same material.

[0052] Removal of spacers 410 and the portion of dielectric layer 620 can use an etch process similar to that which removes hard mask layer 106 and sacrificial layer 104, where the etch process has high etching selectivity to insulating layers 502 as described above. In some embodiments, more than two etch processes are applied to etch dielectric

layer 620 and spacers 410, in which the etch processes have high etching selectivity to insulating layers.

[0053] FIG. 8 illustrates a cross-sectional view of a staircase structure 800 with a dielectric layer 825 disposed thereon, according to some embodiments. Staircase structure 800 is formed by removing hard mask layer 206 from staircase structure 700. Further, a wordline layer 804 for each SC layer of staircase structure 800 is formed by replacing landing pad 720 and sacrificial layer 204 of each step of staircase structure 700 with one or more conducting material layers, including poly-crystalline silicon, tungsten, silicide, nickel, tungsten, titanium, platinum, aluminum, titanium nitride, tantalum nitride, tungsten nitride, any other suitable material, or combinations thereof. As shown in FIG. 8, wordline layer 804 includes landing pad 820 and conductive layer 840. Wordline layer 804 of an SC layer is disposed over a portion of insulating layer 502 of another vertically adjacent SC layer. In some embodiments, a length of wordline layer 804 is shorter in a horizontal direction (e.g., x-direction) than that of insulating layer 502 of another vertically adjacent SC layer. In some embodiments, landing pad 820 is thicker than insulating layer 502 and is insulated from another landing pad 820 disposed on another vertically adjacent SC layer. A dielectric layer 825 is disposed on staircase structure 700. Each wordline layer 804, including landing pad 820 and a conductive layer 840, of staircase structure 800 can control a portion of a memory string in the stacked storage region of a memory device (e.g., 3D memory device). In some embodiments, each wordline layer 804 of staircase structure 800 is a wordline of the memory device, where conductive layer 840 contacts a portion of a memory string of a memory device, and landing pad 820 contacts a portion of a side of insulating layer 502. In some embodiments, a thickness of landing pad structure 820 of word line 804 is thicker than that of conductive layer 840 of wordline layer 804. In some embodiments, an edge of wordline layer 804 of each step of staircase structure 800 has landing pad structure 820, where landing pad 820 is made of the same or different conductive material as conductive layer 840.

[0054] In some embodiments, hard mask layer 206 of staircase structure 700 is removed using a wet etch process. In some embodiments, an etchant used in the wet etch process includes tetramethylammonium hydroxide (TMAH). In some embodiments, a landing pad 720 over hard mask layer 206 is lifted-off after the wet etch process. In some

embodiments, hard mask layer 206 is removed using similar techniques as removing hard mask layer 106.

[0055] In some embodiments, replacement of landing pad 720 and sacrificial layer 204 of each SC layer with the conductive material includes formation of one or more recesses in each SC layer by removing landing pad 720 and sacrificial layer 204 from each SC layer, followed by filling the one or more conductive material layers in the one or more recesses. The removal of landing pad 720 or sacrificial layer 204 can be similar to the techniques of removing sacrificial layer 104. In some embodiments, the removal of landing pad 720 uses different techniques from the removal of sacrificial layer 204. The filling of the conductive material can be similar to the techniques of depositing metallic hard mask layer 106. In some embodiments, the filling of a recess formed by the removal of landing pad 720 uses different techniques and/or conductive material from the filling of another recess formed by the removal of sacrificial layer 204.

[0056] In some embodiments, the formation of dielectric layer 825 uses similar techniques as forming insulating layer 102 or sacrificial layer 104. In some embodiments, the formation of dielectric layer 825 uses a spin-coating process. In some embodiments, dielectric layer 825 includes any suitable dielectric materials, such as silicon oxide or a spin-on-dielectric material. In some embodiments, the formation of dielectric layer 825 further includes a planarization process, such as chemical-mechanical planarization (CMP). In some embodiments, dielectric layer 825 is made of the same material as insulating layer 102 or sacrificial layer 104. In some embodiments, dielectric layer 825 is disposed on each step of staircase structure 800.

[0057] FIG. 9 is a flowchart of a method 900 for forming a memory device (e.g., 3D memory device), according to some embodiments. The operations of method 900 can be used to form memory device structures illustrated in FIGs. 1-8. The operations shown in method 900 are not exhaustive and that other operations can be performed as well before, after, or between any of the illustrated operations. In some embodiments, some operations of exemplary method 900 can be omitted or include other operations that are not described here for simplicity. In some embodiments, operations of method 900 can be performed in a different order and/or vary.

[0058] In operation 910, an alternating stack and a hard-mask layer are formed over a substrate. The substrate can include any suitable material for forming a memory structure—e.g., a 3D memory device. For example, the substrate can include silicon,

silicon germanium, silicon carbide, SOI, GOI, glass, gallium nitride, gallium arsenide, plastic sheet, and/or other suitable III-V compound.

[0059] In operation 910, a layer stack in the alternating layer stack can include a dielectric layer pair with a first material layer and a second material layer. In some embodiments, the first material layer can be an insulating layer. The second material layer can be an sacrificial layer or a conductive material layer. The sacrificial layer can include materials such as silicon nitride, poly-crystalline silicon, poly-crystalline germanium, poly-crystalline germanium-silicon, any other suitable material, or combinations thereof. The insulating layer can include silicon oxide, aluminum oxide, or other suitable materials. The conductive material layer can include tungsten, titanium nitride, tantalum nitride, tungsten nitride, any other suitable material, or combinations thereof. Each of the insulating, sacrificial, and conductive material layers can include materials formed by one or more thin film deposition processes including, but not limiting to, CVD, PVD, ALD, or any combinations thereof.

[0060] The hard mask layer can be a poly-crystalline semiconductor layer, including poly-crystalline silicon. In some embodiments, the hard mask layer can be a metal layer, such as cobalt, nickel, tungsten, copper, or silver. In some embodiments, the hard mask layer can be a silicide layer, including $CoSi_x$, $NiSi_x$, or WSi_x . In some embodiments, the hard mask layer can be an organic material layer. The hard mask layer can be formed using similar techniques as forming the alternating layer stack. In some embodiments, the formation of the hard mask layer includes a thermal anneal process.

[0061] In operation 920, a staircase structure is formed, where a layer of each layer stack in the staircase structure is recessed. Each step of the staircase structure can be formed by repeating an etch-trim process using a mask stack. In some embodiments, the mask stack can include a photoresist or carbon-based polymer material. The etch-trim process includes an etch process and a trim process. In some embodiments, the etch process etches a portion of the hard mask layer and a portion of the layer stack. In some embodiments, the etch process etches a portion of the hard mask layer and a portion of a plurality of layer stacks. In some embodiments, one or more etchants are used in the etch process, and each of the etchants etches the first material layer at a higher etch rate than the second material layer or the hard mask layer. In some embodiments, the one or more etchants etches one of the first material layer, the second material layer and the hard mask layer at a higher etch rate than the other two of the first material layer, the second material

layer and the hard mask layer. In some embodiments, the etch process can control the formation of steps of the staircase structure because high etching selectivity between the first and the second material layer allows the etch process to stop on a surface of a layer stack of the alternating layer stack.

[0062] The trim process includes a suitable etch (e.g., an isotropic dry etch or a wet etch) of the mask stack and is performed at a direction parallel to a surface of the substrate. The amount of trimmed mask stack can be related to the lateral dimensions of the staircase structure. After the repetitive etch-trim process, the resulting staircase structure includes a plurality of layer stacks (or plurality of SC layers). In some embodiments, the staircase structure includes a plurality of steps, where each of the steps exposes a side and a portion of a top surface of each SC layer. In some embodiments, the height of each of the steps is one level, which is equal to the thickness of a SC layer.

[0063] Further, in operation 920, a layer of each SC layer is recessed. The recess process uses similar techniques as etching the alternating layer stack. In some embodiments, a sacrificial layer of each SC layer is recessed using the recess process. In some embodiments, the recess process etches a sacrificial layer of each SC layer and has higher etching selectivity to an insulating layer of each SC layer and the hard mask layer. As a result, the staircase structure includes a plurality of steps, where a SC layer exposed by a step has a lateral recess structure. The formation of the staircase structure is described above with respect to FIGs. 2A-2B.

[0064] In operation 930, a spacer is formed at a side of each step of the staircase structure. A material layer is disposed on the staircase structure. In some embodiments, the material layer fills a recess in each of the SC layers. In some embodiments, the material layer is conformally disposed on the staircase structure. In some embodiments, the material layer is made of a similar material as the hard mask layer. In some embodiments, formation of the material layer uses similar techniques as forming the hard mask layer.

[0065] Further, in operation 930, a portion of the material layer is removed to form a spacer at a side of each of the SC layers. The removal of the material layer uses similar techniques as removing the hard mask layer. In some embodiments, the material layer is completely removed from a top of each of the SC layers. In some embodiments, the material layer is completely removed from a top of the hard mask layer. In some embodiments, the spacer fills in the recess of each of the SC layers. The spacer and the

hard mask layer can be made of the same material. The formation of the spacers is described above with respect to FIGs. 3-4.

[0066] In operation 940, a portion of a layer of each of the SC layers is removed using the spacers and hard mask layer as a mask. In some embodiments, a portion of an insulating layer of each of the SC layers is removed. The removal of the portion of the layer of each of the SC layers uses similar techniques as removing the alternating layer stack. An example of operation 940 is described above with respect to FIG. 5.

[0067] In operation 950, a landing pad is formed at each layer stack of the staircase structure. A dielectric layer is disposed to cover a top surface and a portion of a side of the staircase structure, including a portion of a side of each spacer and a side of an insulating layer of each of the SC layers. The dielectric layer is substantially thinner at a side of the staircase structure than at a top surface of the staircase structure. In some embodiments, the dielectric layer is discontinuous between steps of the staircase structure. The dielectric layer can be a nitride layer. In some embodiments, the dielectric layer and the sacrificial layer are made of the same material, where forming the dielectric layer uses similar techniques as forming the sacrificial layer.

[0068] Operation 950 further includes removing a portion of the dielectric layer and the spacer to form a landing pad on each of the SC layers. The removal of the spacer and the dielectric layer uses an etch process similar to that for forming the staircase structure from the alternating layer stack and the hard mask layer. In some embodiments, the dielectric layer is completely removed from a side of each of the SC layers. In some embodiments, after removing the spacer and the portion of the dielectric layer, the dielectric layer remaining on each of the SC layer forms the landing pad. The landing pad and the sacrificial layer can be made of the same material. The formation of landing pads is described above with respect to FIGs 6-7.

[0069] In operation 960, a wordline layer at each layer of the staircase structure is formed. For example, the hard mask layer on a top surface of the staircase structure can be removed using an etch process. The etch process can include a wet etch process using tetramethylammonium hydroxide (TMAH). In some embodiments, the etch process lifts-off a landing pad at a top of the hard mask layer. Operation 960 further includes forming word lines of the memory device (e.g., 3D memory device) by replacing each of the landing pads and the insulating layers of each of the SC layers with one or more conductive material. This replacement starts from forming a recess at each SC layer of the

staircase by removing the landing pad and the insulating layer of each SC layer. The one or more conductive material is disposed in the recess of each SC layer to form a word line in the staircase structure. After forming the word lines, a dielectric layer is disposed over the staircase structure for the BEOL interconnect process.

[0070] The foregoing description of the specific embodiments will so fully reveal the general nature of the present disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt for various applications such specific embodiments, without undue experimentation, without departing from the general concept of the present disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the disclosure and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the disclosure and guidance.

[0071] Embodiments of the present disclosure have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

[0072] The Summary and Abstract sections can set forth one or more but not all exemplary embodiments of the present disclosure and thus are not intended to limit the present disclosure and the appended claims.

[0073] The breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

CLAIMS

1. A semiconductor structure, comprising:

a substrate; and

a staircase structure disposed over the substrate, wherein the staircase structure comprises:

a plurality of layer stacks, each layer stack comprising a first material layer disposed over a first portion of a second material layer; and

a plurality of landing pads respectively disposed on the plurality of layer stacks, each landing pad disposed over a second portion of the second material layer of a respective layer stack.

2. The semiconductor structure of claim 1, wherein each of the plurality of landing pads is adjacent to a respective side of the first material layer.

3. The semiconductor structure of claim 1, wherein each of the plurality of landing pads extends over a respective top surface of the second material layer.

4. The semiconductor structure of claim 1, wherein the first material layer comprises an insulating material, the second material layer comprises a first conductive material, and each of the plurality of landing pads comprises a second conductive material.

5. The semiconductor structure of claim 4, wherein the first conductive material is the same as or different from the second conductive material.

6. The semiconductor structure of claim 4, wherein:

the insulating material layer comprises silicon oxide, aluminum oxide, or a combination thereof; and

each of the first and the second conductive material layers comprises tungsten, silicide, nickel, titanium, platinum, aluminum, titanium nitride, tantalum nitride, tungsten nitride, or a combination thereof.

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7. The semiconductor structure of claim 1, wherein the second material layer of each layer stack is disposed over a portion of the first material layer of an adjacent layer stack.

8. The semiconductor structure of claim 7, wherein one of the plurality of landing pads is thicker than the first material layer of a corresponding layer stack and is insulated from another landing pad disposed on an adjacent layer stack.

9. A method for forming a semiconductor structure, comprising:

forming a plurality of layer stacks over a substrate, wherein each layer stack comprises a first material layer disposed over a second material layer ;

forming a hard mask layer over the plurality of layer stacks;

forming a staircase structure on the plurality of layer stacks to expose a portion of the first material layer of each layer stack;

forming a landing pad over a portion of the second material layer of the each layer stack; and

removing the portion of the hard mask layer.

10. The method of claim 9, further comprising:

removing the landing pad and the second material layer of the each layer stack to form a recess in each layer stack;

disposing a conductive material in the recess of each layer stack; and

forming a dielectric layer over the staircase structure.

11. The method of claim 9, wherein forming the landing pad comprises:

removing a portion of the second material layer from a side of each layer stack to form a recess;

disposing a material layer over the staircase structure to fill the recess in each layer stack; and

removing a portion of the material layer to form a spacer at the side of each layer stack and a side of the portion of the hard mask layer.

12. The method of claim 11, wherein forming the landing pad further comprises:

removing a portion of the first material layer of each layer stack using the spacer and the portion of the hard mask layer as a mask;

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disposing a dielectric layer over the staircase structure; and

removing the spacer and a portion of the dielectric layer.

13. The method of claim 12, wherein disposing the dielectric layer over the staircase structure comprises disposing the dielectric layer over a portion of the second material layer, a portion of a side of the first material layer, and a portion of a side of the spacer.

14. The method of claim 9, wherein removing the portion of the hard mask layer and the portion of the top layer stack in the plurality of layer stacks comprise removing the portion of the hard mask layer and the portion of the top layer stack by dry etching, wet etching, or a combination thereof.

15. The method of claim 9, wherein trimming the mask stack comprises etching the mask stack incrementally and inwardly from a boundary of the mask stack.

16. The method of claim 9, wherein removing the portion of the hard mask layer comprises removing the portion of the hard mask layer by a wet etch process using tetramethylammonium hydroxide (TMAH), potassium hydroxide (KOH), a base, or a combination thereof.

17. The method of claim 9, wherein forming of each layer stack and the forming of the hard mask layer comprises deposition techniques using chemical vapor deposition (CVD), physical vapor deposition (PVD), plasma-enhanced CVD (PECVD), low pressure CVD (LPCVD), sputtering, metal-organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), or a combination thereof.

18. A memory device, comprising:

a substrate;

a memory string disposed over the substrate; and

a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises:

a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer, wherein a second portion of the conductive layer is in contact with a side surface of the insulating layer.

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19. The memory device of claim 18, wherein the conductive layer of each layer stack is disposed over a portion of the insulating layer of an adjacent layer stack.

20. The memory device of claim 18, wherein the second portion of the conductive layer is thicker than the first portion of the conductive material layer.

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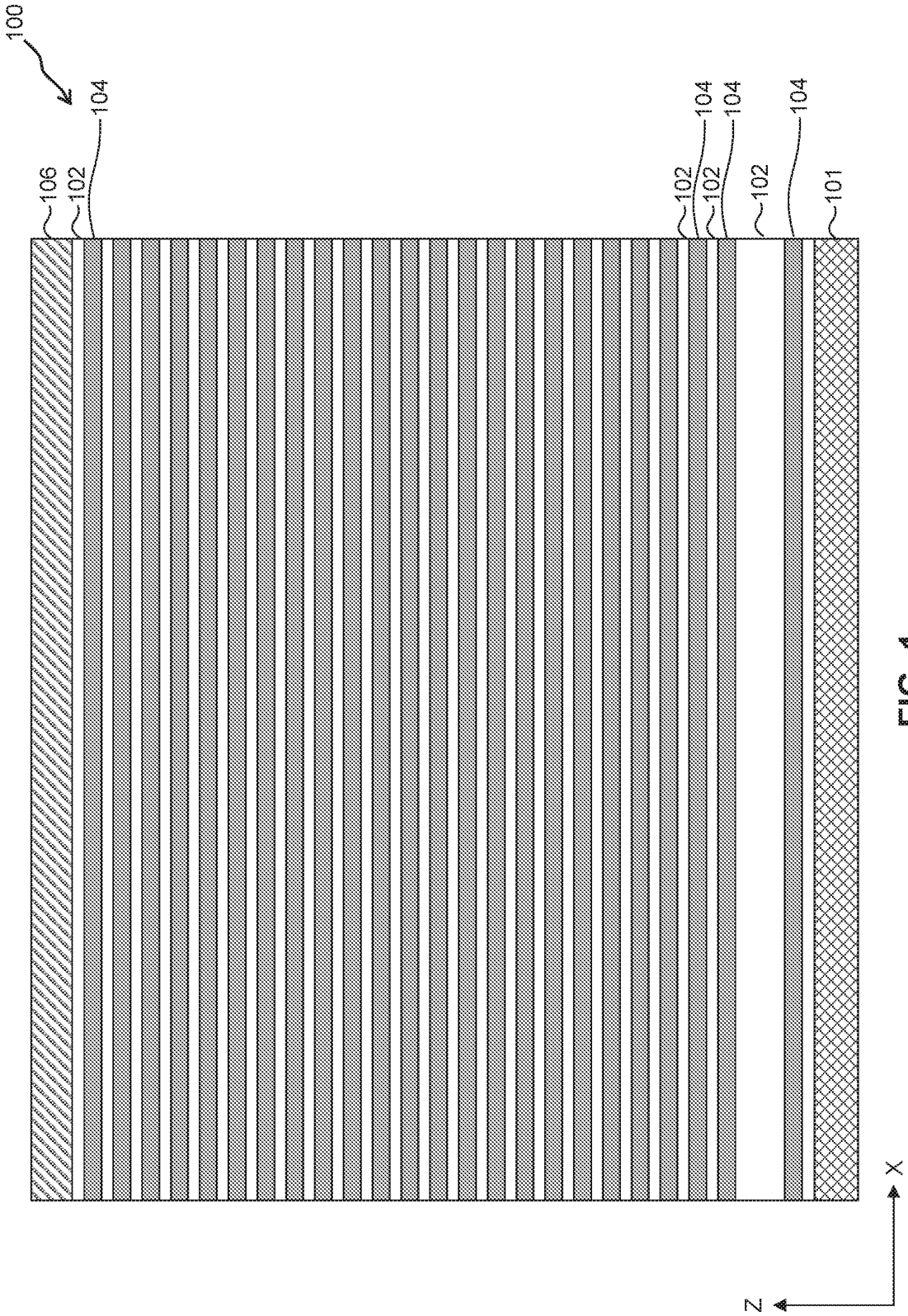

FIG. 1

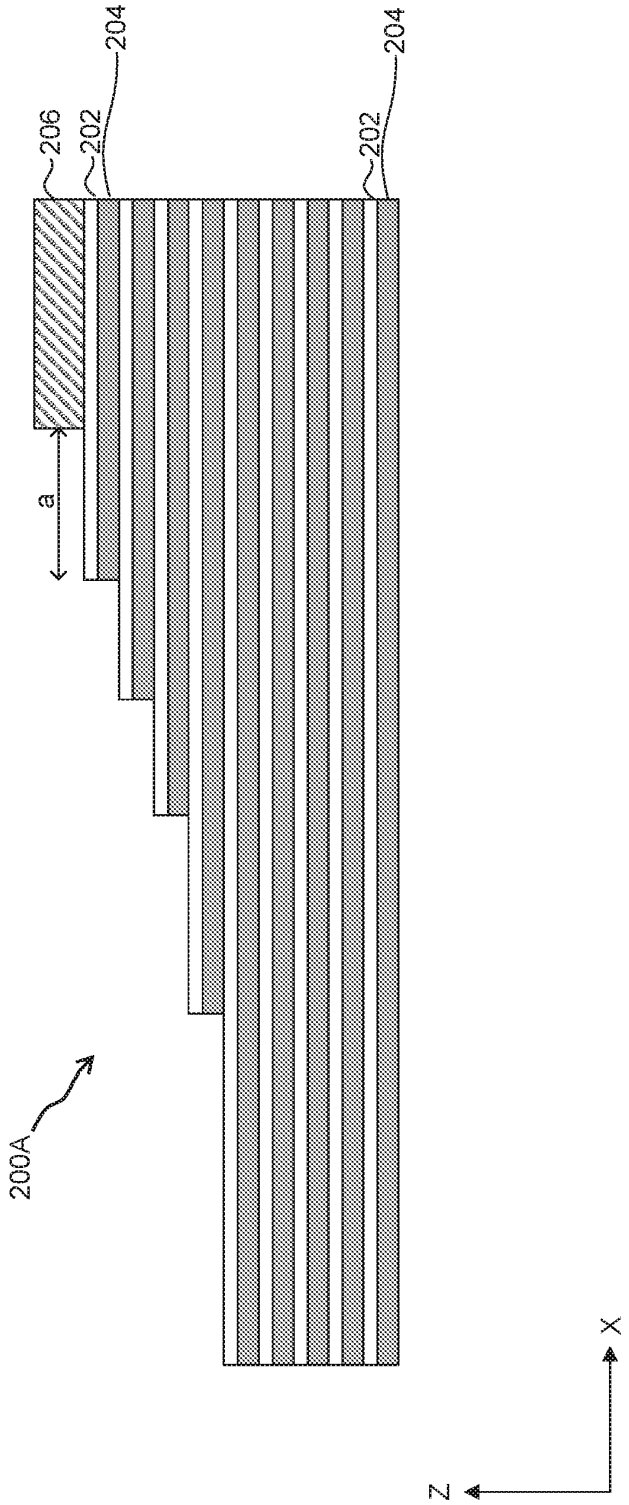

FIG. 2A

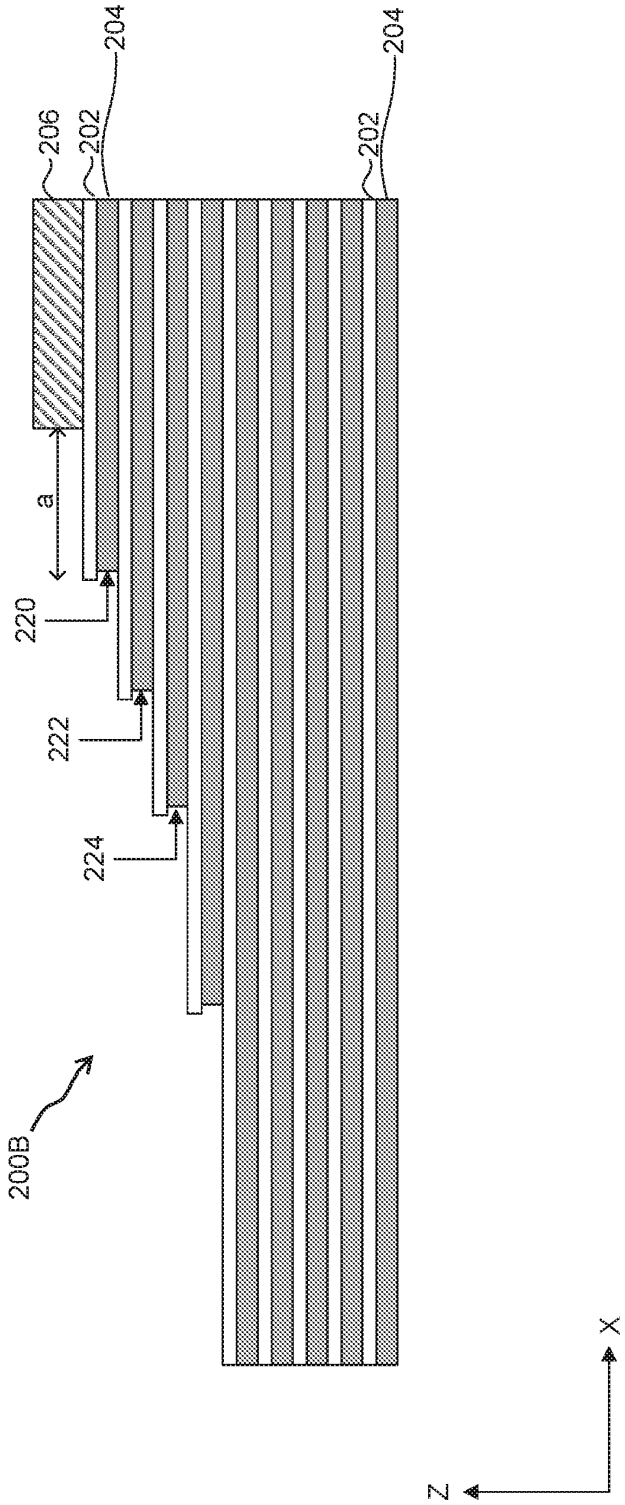

FIG. 2B

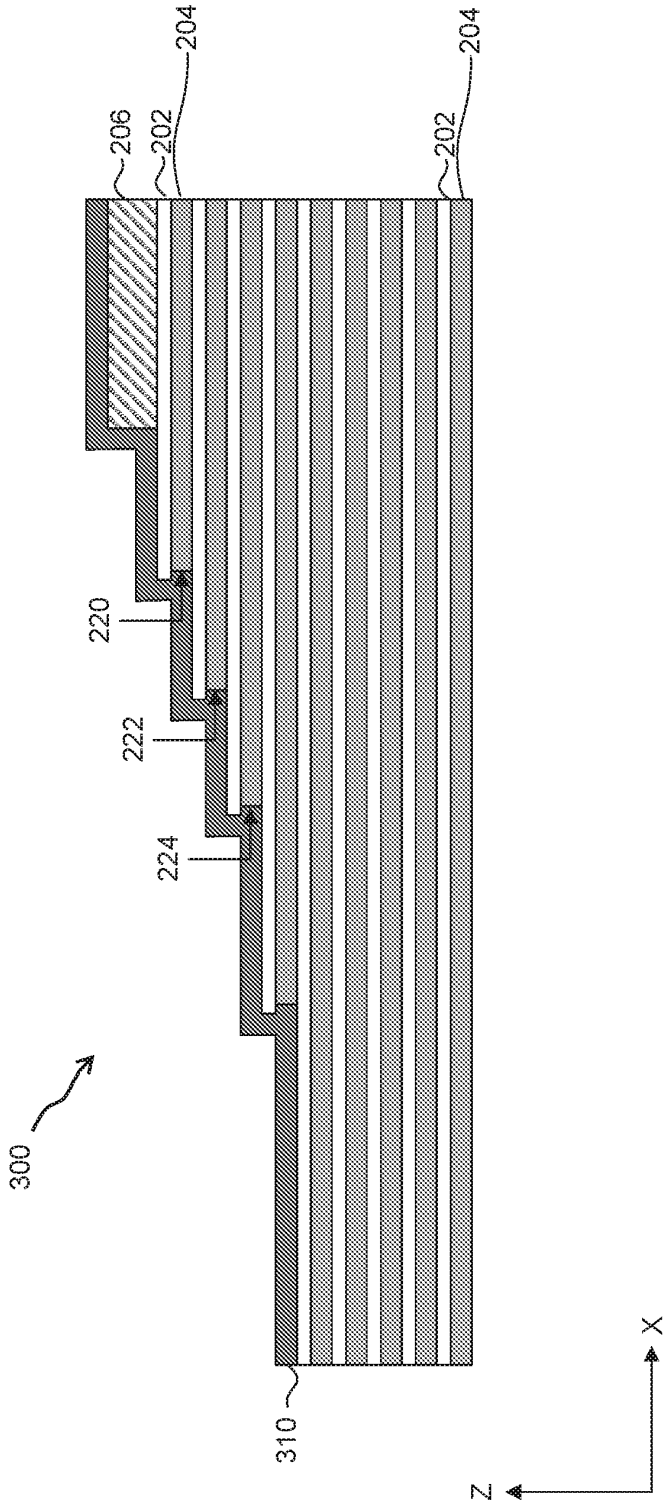

FIG. 3

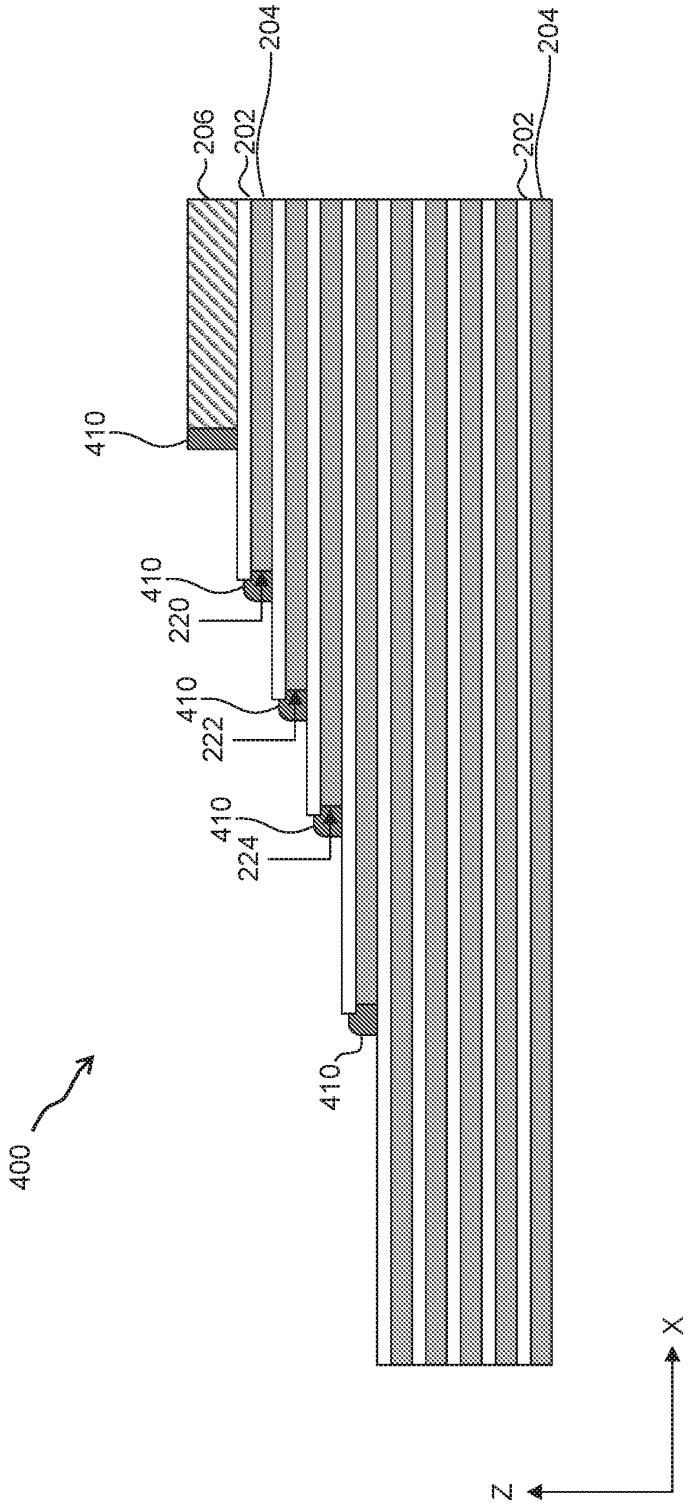

FIG. 4

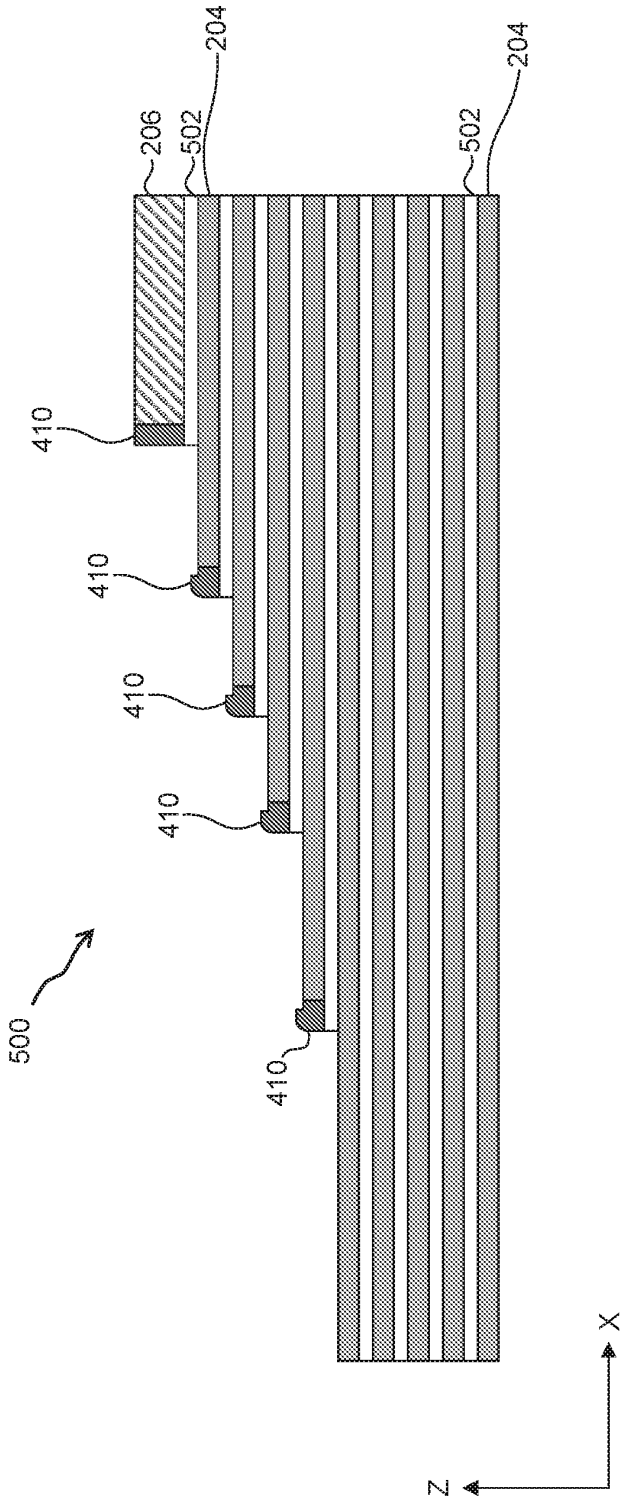

FIG. 5

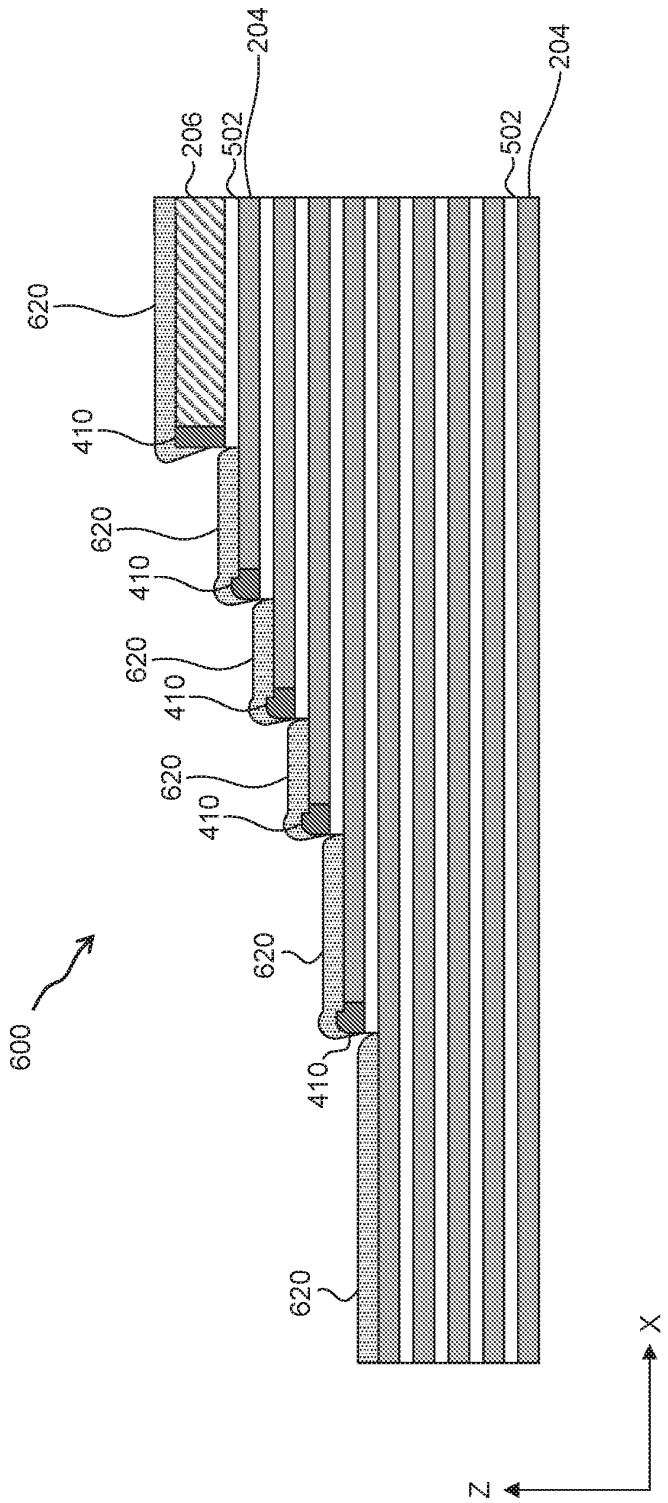

FIG. 6

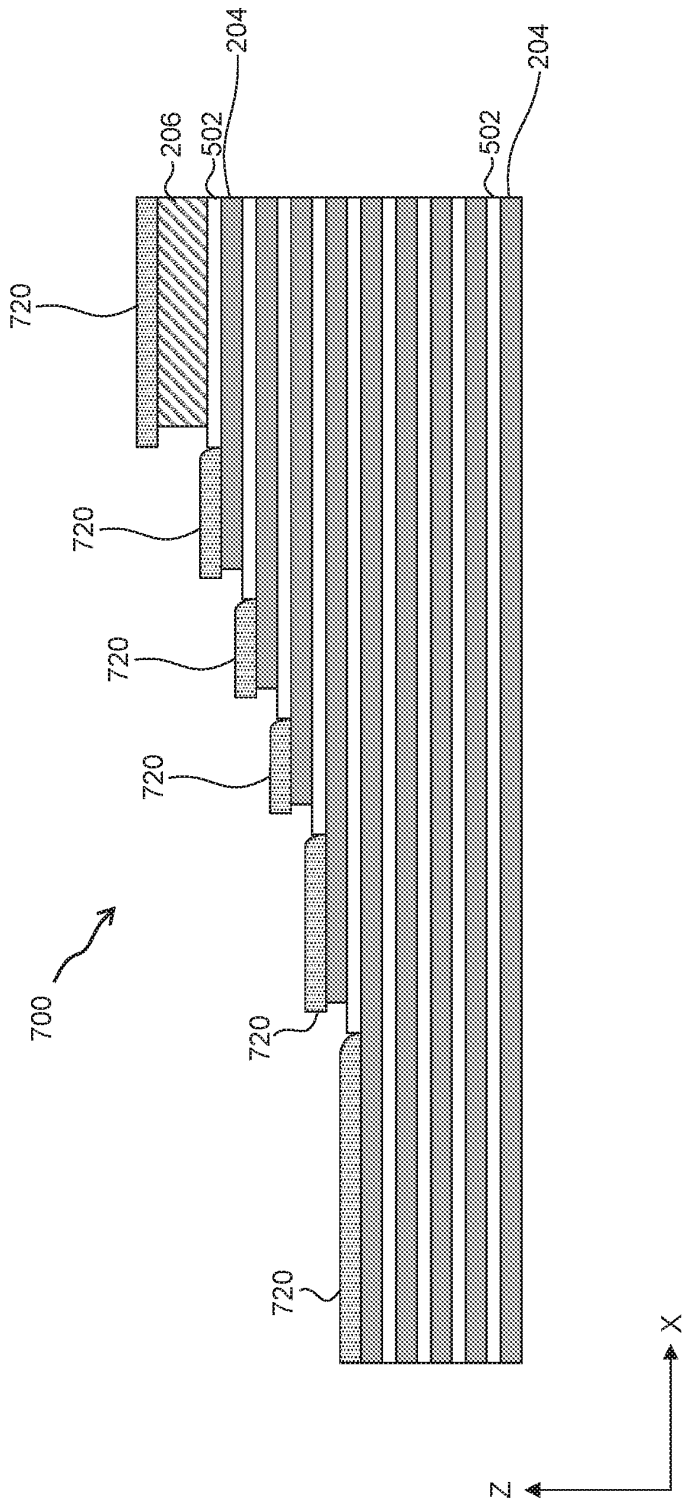

FIG. 7

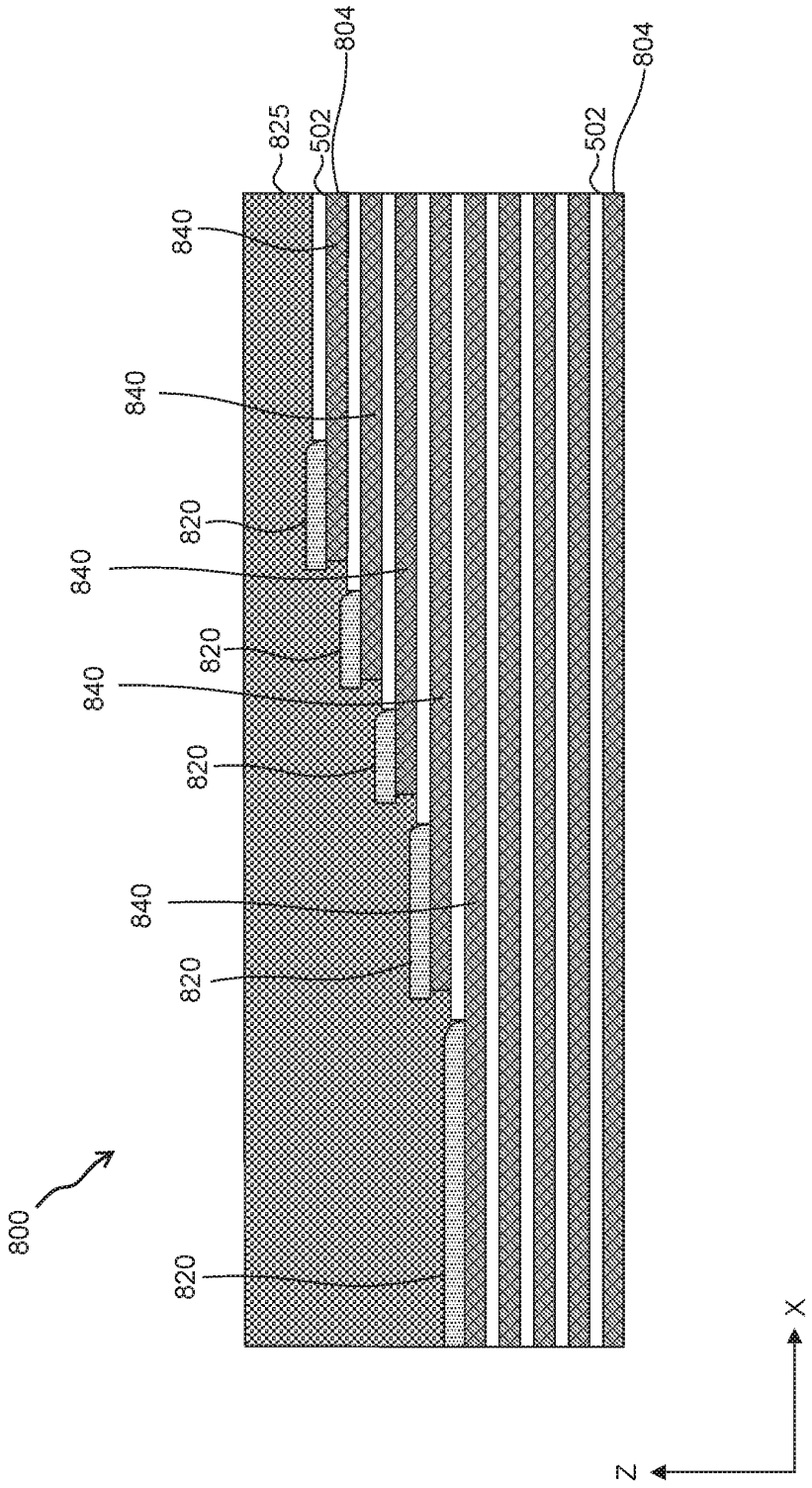
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FIG. 8

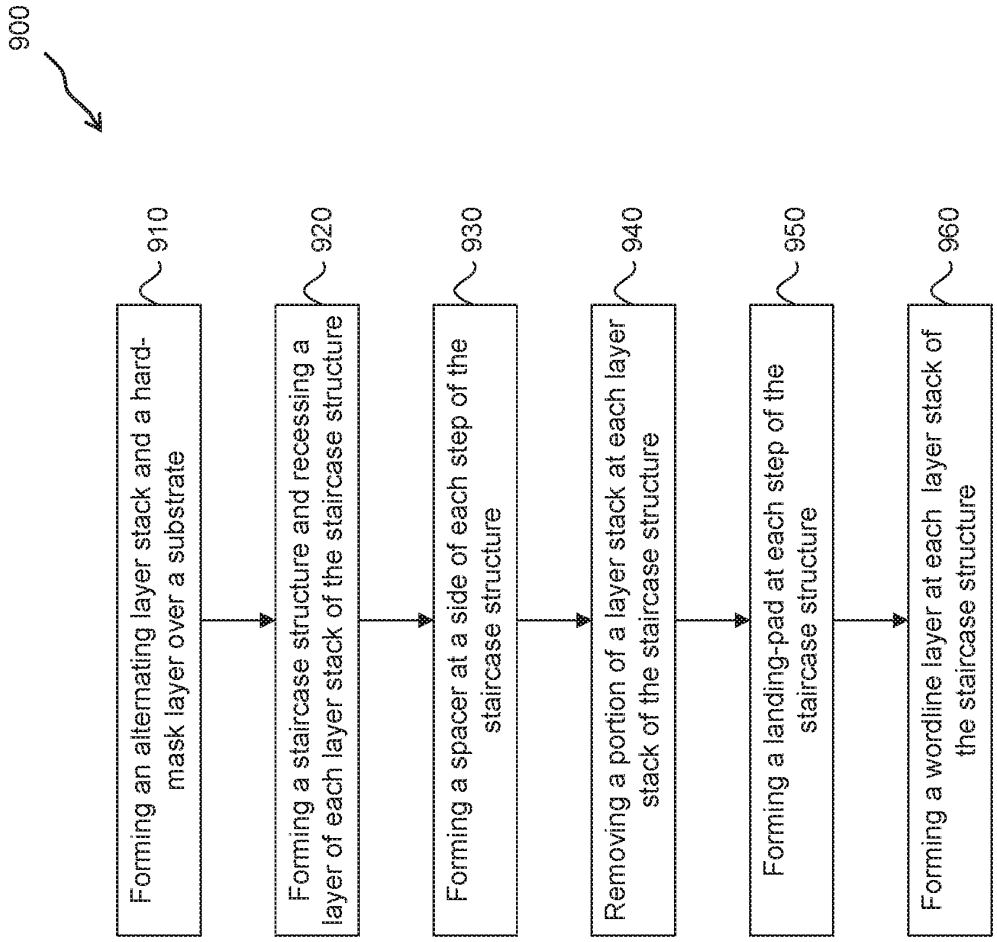
900
910
Forming an alternating layer stack and a hard-mask layer over a substrate
920
Forming a staircase structure and recessing a layer of each layer stack of the staircase structure
930
Forming a spacer at a side of each step of the staircase structure
940
Removing a portion of a layer stack at each layer stack of the staircase structure
950
Forming a landing-pad at each step of the staircase structure
960
Forming a wordline layer at each layer stack of the staircase structure

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2018/098962

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/11551(2017.01)i; H01L 27/11578(2017.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT,WPI,EPODOC,CNKI,IEEE:memory,storage,3D,vertical,stack,step,stair,staircase,stagger,pad,recess

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015255385 A1 (SK HYNIX INC.) 10 September 2015 (2015-09-10) description, paragraphs [0022]-[0115], figures 1A-9	1-10,14-20
X	KR 20110015338 A (HYNIX SEMICONDUCTOR INC.) 15 February 2011 (2011-02-15) description, paragraphs [0025]-[0055], figures 2a-2e	1-9,14-20
PX	CN 107644876 A (YANGTZE MEMORY TECHNOLOGIES CO., LTD.) 30 January 2018 (2018-01-30) description, paragraphs [0037]-[0068], figures 1-10	1-20
A	CN 106601746 A (SAMSUNG ELECTRONICS CO., LTD.) 26 April 2017 (2017-04-26) the whole document	1-20

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 October 2018	**07 November 2018**

Name and mailing address of the ISA/CN	Authorized officer
STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088** **China**	**HUANG,Lina**
Facsimile No. **(86-10)62019451**	Telephone No. **86-(10)-53961458**

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2018/098962

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
US	2015255385	A1	10 September 2015	US	9356038	B2	31 May 2016
				KR	20150104817	A	16 September 2015
KR	20110015338	A	15 February 2011		None		
CN	107644876	A	30 January 2018		None		
CN	106601746	A	26 April 2017	US	9419013	B1	16 August 2016
				KR	20170042449	A	19 April 2017

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PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference **P2018TC556**	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. **PCT/CN2018/098962**	International filing date *(day/month/year)* **06 August 2018**	(Earliest) Priority Date *(day/month/year)* **28 August 2017**
Applicant **Yangtze Memory Technologies Co., Ltd.**		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of **4** sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of:
      ☑ the international application in the language in which it was filed.
      ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,
   ☑ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,
   ☐ the text is approved as submitted by the applicant.
   ☑ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,
   a. the figure of the **drawings** to be published with the abstract is Figure No. **8**
      ☑ as suggested by the applicant.
      ☐ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figures is to be published with the abstract.

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Box No. IV Text of the abstract (Continuation of item 5 of the first sheet)

A semiconductor structure is disclosed. The semiconductor structure includes a staircase structure (800) disposed over a substrate (101). The staircase structure (800) includes a plurality of layer stacks, where each layer stack is made of a first material layer (502) over a portion of a second material layer (840). The staircase structure (800) further includes a plurality of landing pads (820), where each landing pad (820) is disposed over another portion of the second material layer (840) of a respective layer stack.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2018/098962

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/11551(2017.01)i; H01L 27/11578(2017.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT,WPI,EPODOC,CNKI,IEEE:memory,storage,3D,vertical,stack,step,stair,staircase,stagger,pad,recess

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015255385 A1 (SK HYNIX INC.) 10 September 2015 (2015-09-10) description, paragraphs [0022]-[0115], figures 1A-9	1-10,14-20
X	KR 20110015338 A (HYNIX SEMICONDUCTOR INC.) 15 February 2011 (2011-02-15) description, paragraphs [0025]-[0055], figures 2a-2e	1-9,14-20
PX	CN 107644876 A (YANGTZE MEMORY TECHNOLOGIES CO., LTD.) 30 January 2018 (2018-01-30) description, paragraphs [0037]-[0068], figures 1-10	1-20
A	CN 106601746 A (SAMSUNG ELECTRONICS CO., LTD.) 26 April 2017 (2017-04-26) the whole document	1-20

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 October 2018	**07 November 2018**

Name and mailing address of the ISA/CN	Authorized officer
STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088** **China**	**HUANG,Lina**
Facsimile No. **(86-10)62019451**	Telephone No. **86-(10)-53961458**

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2018/098962

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
US	2015255385	A1	10 September 2015	US	9356038	B2	31 May 2016
				KR	20150104817	A	16 September 2015
KR	20110015338	A	15 February 2011	None			
CN	107644876	A	30 January 2018	None			
CN	106601746	A	26 April 2017	US	9419013	B1	16 August 2016
				KR	20170042449	A	19 April 2017

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PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY
(Chapter I of the Patent Cooperation Treaty)

(PCT Rule 44*bis*)

Applicant's or agent's file reference P2018TC556	**FOR FURTHER ACTION**	See item 4 below
International application No. PCT/CN2018/098962	International filing date *(day/month/year)* 06 August 2018 (06.08.2018)	Priority date *(day/month/year)* 28 August 2017 (28.08.2017)
International Patent Classification (8th edition unless older edition indicated) See relevant information in Form PCT/ISA/237		
Applicant YANGTZE MEMORY TECHNOLOGIES CO., LTD.		

1. This international preliminary report on patentability (Chapter I) is issued by the International Bureau on behalf of the International Searching Authority under Rule 44 *bis*.1(a).

2. This REPORT consists of a total of 5 sheets, including this cover sheet.

   In the attached sheets, any reference to the written opinion of the International Searching Authority should be read as a reference to the international preliminary report on patentability (Chapter I) instead.

3. This report contains indications relating to the following items:

☒	Box No. I	Basis of the report
☒	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☐	Box No. VIII	Certain observations on the international application

4. The International Bureau will communicate this report to designated Offices in accordance with Rules 44*bis*.3(c) and 93*bis*.1 but not, except where the applicant makes an express request under Article 23(2), before the expiration of 30 months from the priority date (Rule 44*bis* .2).

	Date of issuance of this report 03 March 2020 (03.03.2020)
The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No. +41 22 338 82 70	Authorized officer Xin Wang e-mail: pct.team2@wipo.int

Form PCT/IB/373 (January 2004)

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:
100013
China 10th Floor, Tower C, Beijing Global Trade Center, 36 North Third Ring Road East, Dongcheng District, Beijing

NTD UNIVATION INTELLECTUAL PROPERTY AGENCY LTD.

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	**07 November 2018**
Applicant's or agent's file reference **P2018TC556**	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/CN2018/098962	**06 August 2018**	**28 August 2017**

International Patent Classification (IPC) or both national classification and IPC
H01L 27/11551(2017.01)i; H01L 27/11578(2017.01)i

Applicant
Yangtze Memory Technologies Co., Ltd.

1. This opinion contains indications relating to the following items:

- [x] Box No. I Basis of the opinion
- [x] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [x] Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/	Date of completion of this opinion	Authorized officer
STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA **China 6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088**	**01 November 2018**	**HUANG,Lina**
Facsimile No. **(86—10) 62019451**		Telephone No. **86-(10)-53961458**

Form PCT/ISA/237 (Cover sheet) (January 2015)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/CN2018/098962

Box No. I **Basis of the opinion**

1. With regard to the **language**, this opinion has been established on the basis of:
   - [✓] the international application in the language in which it was filed.
   - [ ] a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. [ ] This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a)).

3. [ ] With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing:
   - a. [ ] forming part of the international application as filed:
     - [ ] in the form of an Annex C/ST.25 text file.
     - [ ] on paper or in the form of an image file.
   - b. [ ] furnished together with the international application under PCT Rule 13*ter*.1(a) for the purposes of international search only in the form of an Annex C/ST.25 text file.
   - c. [ ] furnished subsequent to the international filing date for the purposes of international search only:
     - [ ] in the form of an Annex C/ST.25 text file (Rule 13*ter*.1(a)).
     - [ ] on paper or in the form of an image file (Rule 13*ter*.1(b) and Administrative Instructions, Section 713).

4. [ ] In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that forming part of the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

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Micron v. YMTC
IPR2025-00229

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/CN2018/098962

Box No. II Priority

1. ☐ The validity of the priority claim has not been considered because the International Searching Authority does not have in its possession a copy of the earlier application whose priority has been claimed or, where required, a translation of that earlier application. This opinion has nevertheless been established on the assumption that the relevant date (Rules 43*bis*.1 and 64.1) is the claimed priority date.

2. ☐ This opinion has been established as if no priority had been claimed due to the fact that the priority claim has been found invalid (Rules 43*bis*.1 and 64.1). Thus for the purposes of this opinion, the international filing date indicated above is considered to be the relevant date.

3. Additional observations, if necessary:

[1] The priority of the application is valid after verified.

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IPR2025-00229

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/CN2018/098962

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	1-20	YES
	Claims	None	NO
Inventive step (IS)	Claims	11-13	YES
	Claims	1-10, 14-20	NO
Industrial applicability (IA)	Claims	1-20	YES
	Claims	None	NO

2. Citations and explanations :

[1] Cited document

[2] D1: US2015255385A1, 10 Sep. 2015

[3] I. Novelty and Inventive step

[4] D1 discloses a memory device, a semiconductor structure and a method for forming the semiconductor structure(see description, paragraphs [0022]-[0115], figures 1A-9): the semiconductor structure comprises a staircase structure, wherein the staircase structure comprises: a plurality of layer stacks ST, each layer stack comprising a first material layer 12 disposed over a first portion 11A of a second material layer 11; and a plurality of landing pads A respectively disposed on the plurality of layer stacks ST, each landing pad A disposed over a second portion 11B of the second material layer 11 of a respective layer stack; the memory device comprises a memory string and a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises: a plurality of layer stacks ST, each layer stack comprising an insulating layer 12 disposed over a first portion 11A of a conductive layer 11, wherein a second portion 11B of the conductive layer 11 is in contact with a side surface of the insulating layer 12; the method comprises: forming a plurality of layer stacks ST, wherein each layer stack comprises a first material layer 22 disposed over a second material layer 21; forming a staircase structure on the plurality of layer stacks ST to expose a portion of the first material layer 22 of each layer stack; forming a landing pad over a portion of the second material layer 21 of the each layer stack.

[5] The difference between claim 1 and D1 is that: the staircase structure is disposed over a substrate.

[6] The differences between claim 9 and D1 are that: forming the layer stacks over a substrate; forming a hard mask layer over the plurality of layer stacks and finally removing the portion of the hard mask layer.

[7] The difference between claim 18 and D1 is that: the memory string is disposed over a substrate.

[8] Therefore, claims 1,9,18 are new in the sense of PCT Article 33(2). Claims 2-8,10-17,19-20 are respectively dependent on claims 1,9,18 directly or indirectly and as such also meet the requirement of PCT Article 33(2).

[9] However, the above differences come within the scope of the customary practice followed by a person skilled in the art. Therefore, claims 1,9,18 do not involve an inventive step in the sense of PCT Article 33(3).

[10] As for claims 2-8,10-17,19-20, the additional features of claims 2-5,7-8,10,19-20 are disclosed by D1(see description, paragraphs [0022]-[0115], figures 1A-9), the additional features of claims 6,14-17 are not disclosed by D1 but come within the scope of the customary practice followed by a person skilled in the art, the additional features of claims 11-13 are not disclosed by D1 and are neither indicated nor obviously rendered from the available prior art. Hence, claims 2-8,10,14-17,19-20 do not involve an inventive step in the sense of PCT Article 33(3), and claims 11-13 involve an inventive step in the sense of PCT Article 33(3).

[11] II. Industrial applicability

[12] The technical solutions of claims 1-20 are industrially applicable in the technical field of memory technology, and thus said claims meet the criteria set out in PCT Article 33(4).

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PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:
100013
China 10th Floor, Tower C, Beijing Global Trade Center, 36 North Third Ring Road East, Dongcheng District, Beijing

NTD UNIVATION INTELLECTUAL PROPERTY AGENCY LTD.

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	**07 November 2018**
Applicant's or agent's file reference **P2018TC556**	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/CN2018/098962	**06 August 2018**	**28 August 2017**

International Patent Classification (IPC) or both national classification and IPC
H01L 27/11551(2017.01)i; H01L 27/11578(2017.01)i

Applicant
Yangtze Memory Technologies Co., Ltd.

1. This opinion contains indications relating to the following items:

- [x] Box No. I Basis of the opinion
- [x] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [x] Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/	Date of completion of this opinion	Authorized officer
STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA **China 6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088**	**01 November 2018**	**HUANG,Lina**
Facsimile No. **(86—10) 62019451**		Telephone No. **86-(10)-53961458**

Form PCT/ISA/237 (Cover sheet) (January 2015)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/CN2018/098962

Box No. I **Basis of the opinion**

1. With regard to the **language**, this opinion has been established on the basis of:
   - [✓] the international application in the language in which it was filed.
   - [ ] a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. [ ] This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a)).

3. [ ] With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing:
   - a. [ ] forming part of the international application as filed:
     - [ ] in the form of an Annex C/ST.25 text file.
     - [ ] on paper or in the form of an image file.
   - b. [ ] furnished together with the international application under PCT Rule 13*ter*.1(a) for the purposes of international search only in the form of an Annex C/ST.25 text file.
   - c. [ ] furnished subsequent to the international filing date for the purposes of international search only:
     - [ ] in the form of an Annex C/ST.25 text file (Rule 13*ter*.1(a)).
     - [ ] on paper or in the form of an image file (Rule 13*ter*.1(b) and Administrative Instructions, Section 713).

4. [ ] In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that forming part of the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

Micron Ex. 1018, p. 47
Micron v. YMTC
IPR2025-00229

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/CN2018/098962

Box No. II Priority

1. ☐ The validity of the priority claim has not been considered because the International Searching Authority does not have in its possession a copy of the earlier application whose priority has been claimed or, where required, a translation of that earlier application. This opinion has nevertheless been established on the assumption that the relevant date (Rules 43*bis*.1 and 64.1) is the claimed priority date.

2. ☐ This opinion has been established as if no priority had been claimed due to the fact that the priority claim has been found invalid (Rules 43*bis*.1 and 64.1). Thus for the purposes of this opinion, the international filing date indicated above is considered to be the relevant date.

3. Additional observations, if necessary:

[1] The priority of the application is valid after verified.

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IPR2025-00229

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/CN2018/098962

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	1-20	YES
	Claims	None	NO
Inventive step (IS)	Claims	11-13	YES
	Claims	1-10, 14-20	NO
Industrial applicability (IA)	Claims	1-20	YES
	Claims	None	NO

2. Citations and explanations :

[1] Cited document

[2] D1: US2015255385A1, 10 Sep. 2015

[3] I. Novelty and Inventive step

[4] D1 discloses a memory device, a semiconductor structure and a method for forming the semiconductor structure(see description, paragraphs [0022]-[0115], figures 1A-9): the semiconductor structure comprises a staircase structure, wherein the staircase structure comprises: a plurality of layer stacks ST, each layer stack comprising a first material layer 12 disposed over a first portion 11A of a second material layer 11; and a plurality of landing pads A respectively disposed on the plurality of layer stacks ST, each landing pad A disposed over a second portion 11B of the second material layer 11 of a respective layer stack; the memory device comprises a memory string and a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises: a plurality of layer stacks ST, each layer stack comprising an insulating layer 12 disposed over a first portion 11A of a conductive layer 11, wherein a second portion 11B of the conductive layer 11 is in contact with a side surface of the insulating layer 12; the method comprises: forming a plurality of layer stacks ST, wherein each layer stack comprises a first material layer 22 disposed over a second material layer 21; forming a staircase structure on the plurality of layer stacks ST to expose a portion of the first material layer 22 of each layer stack; forming a landing pad over a portion of the second material layer 21 of the each layer stack.

[5] The difference between claim 1 and D1 is that: the staircase structure is disposed over a substrate.

[6] The differences between claim 9 and D1 are that: forming the layer stacks over a substrate; forming a hard mask layer over the plurality of layer stacks and finally removing the portion of the hard mask layer.

[7] The difference between claim 18 and D1 is that: the memory string is disposed over a substrate.

[8] Therefore, claims 1,9,18 are new in the sense of PCT Article 33(2). Claims 2-8,10-17,19-20 are respectively dependent on claims 1,9,18 directly or indirectly and as such also meet the requirement of PCT Article 33(2).

[9] However, the above differences come within the scope of the customary practice followed by a person skilled in the art. Therefore, claims 1,9,18 do not involve an inventive step in the sense of PCT Article 33(3).

[10] As for claims 2-8,10-17,19-20, the additional features of claims 2-5,7-8,10,19-20 are disclosed by D1(see description, paragraphs [0022]-[0115], figures 1A-9), the additional features of claims 6,14-17 are not disclosed by D1 but come within the scope of the customary practice followed by a person skilled in the art, the additional features of claims 11-13 are not disclosed by D1 and are neither indicated nor obviously rendered from the available prior art. Hence, claims 2-8,10,14-17,19-20 do not involve an inventive step in the sense of PCT Article 33(3), and claims 11-13 involve an inventive step in the sense of PCT Article 33(3).

[11] II. Industrial applicability

[12] The technical solutions of claims 1-20 are industrially applicable in the technical field of memory technology, and thus said claims meet the criteria set out in PCT Article 33(4).

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Micron v. YMTC
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