Exhibit D-8
Galaxy S applied to U.S. Patent No. 8,604,471 ("471 patent")

As demonstrated in the chart below, claims 1 and 17 of the 471 patent are anticipated by Galaxy S, and/or rendered obvious by Galaxy S (in combination with itself, the secondary references identified below, and/or the knowledge of a person of ordinary skill in the art). On information and belief, the Galaxy S was on sale or offered for sale prior to August 12, 2010, and therefore qualifies as prior art at least under pre-AIA 35 U.S.C. § 102 (a), (b).

Secondary References:

- US 5838399 to Someya ("Someya") was published on November 17, 1998 and qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- Solid State Electronic Devices 4th Edition by Ben Streetman ("Streetman") was published in 1995 and qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- Handbook of Optics 2nd Edition Volume II by Michael Bass et al. ("HandbookII") was published in 1995 and qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- US 2008/0158108 to Hwang et al. ("Hwang") was published on July 3, 2008 and qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- U.S. 2010/0148175 ("Godo") published on June 17, 2010, filed on Dec. 8, 2009 and qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(a), (b) and (e).
- U.S. 2009/0184898 ("Yamashita") published on July 23, 2009 and qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- KR100659756 published on December 19, 2006 and qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- KR100853543 published on August 14, 2008 and qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- Introduction to VLSI Systems by Carver Mead and Lynn Conway ("Mead") was published in 1980 and qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- Schaum's Outline of Theory and Problems of Basic Circuit Analysis 2nd Edition by John O'Malley ("Schaum") was published in 1992 and qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- US 6278504 to Sung ("Sung") was published on August 21, 2001 and qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- US 20070296333 to Kim ("Kim") was published on December 27, 2007 and qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).

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- US 20070290227 to Liang ("Liang") was published on December 20, 2007 and qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- JP H09-90425A to Masumitsu ("Masumitsu") was published on April 4, 1997 and therefore qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- KR20060001753 to Lee ("Lee") was published on December 19, 2006 and therefore qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- U.S. Patent Publication No. 2008/0122373 to Cho ("Cho") was published on May 29, 2008 and therefore qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- U.S. Patent Publication No. 2010/0038643 ("Park") was published on Feb. 18, 2010, and therefore qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).
- WO 2010002029 to Tateishi ("Tateishi") was published on January 7, 2010 and therefore qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).

Claim Language	Exemplary Citations in Galaxy S
[1pre] A semiconductor structure, disposed on a substrate, and comprising:	To the extent the preamble is limiting, Galaxy S discloses a semiconductor structure, disposed on a substrate.

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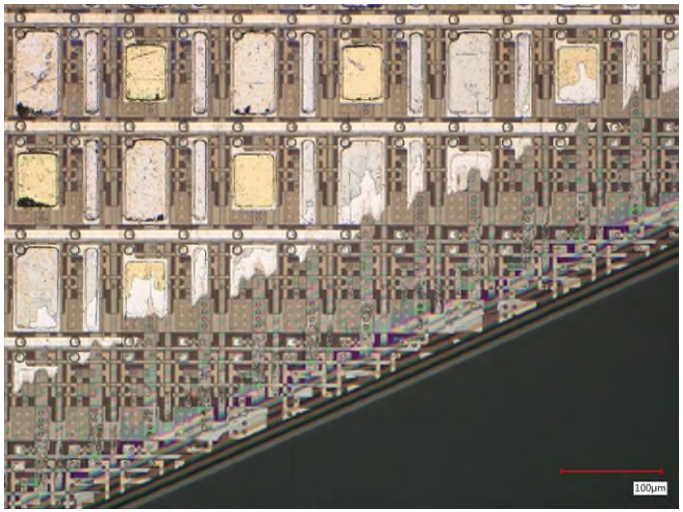
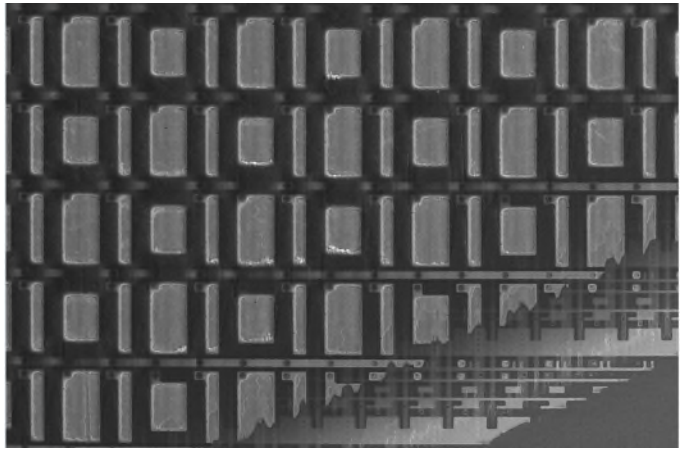
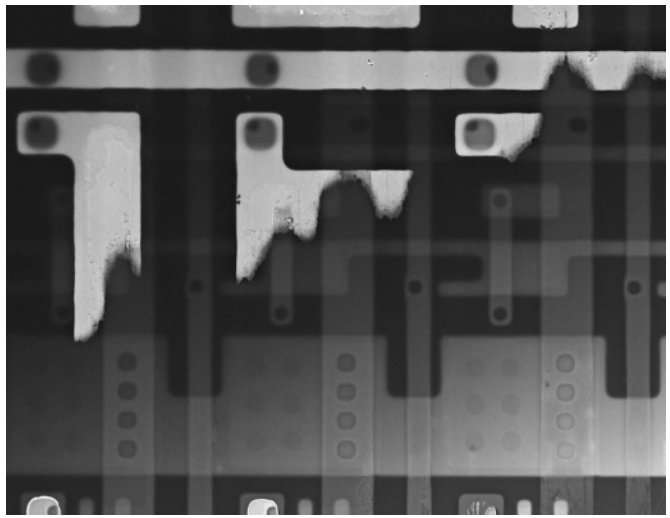
Claim Language	Exemplary Citations in Galaxy S
	 Optical microscope image of Galaxy S panel with some layers removed at a sloped angle (bevel cut) to review underlying structures. 

Claim Language	Exemplary Citations in Galaxy S
	TEM image of Galaxy S panel (with bevel cut).  Magnified TEM image of Galaxy S panel (with bevel cut).

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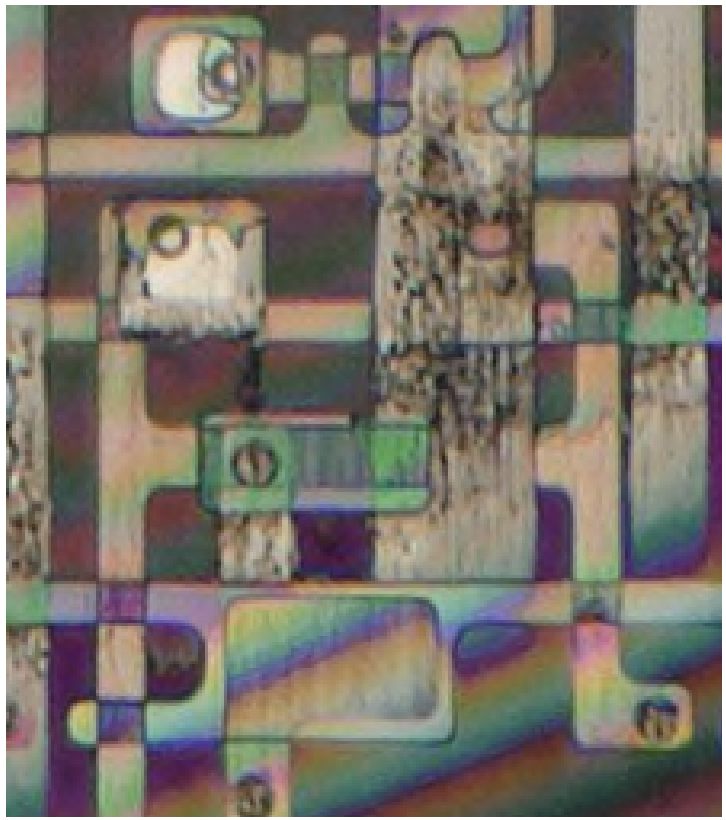
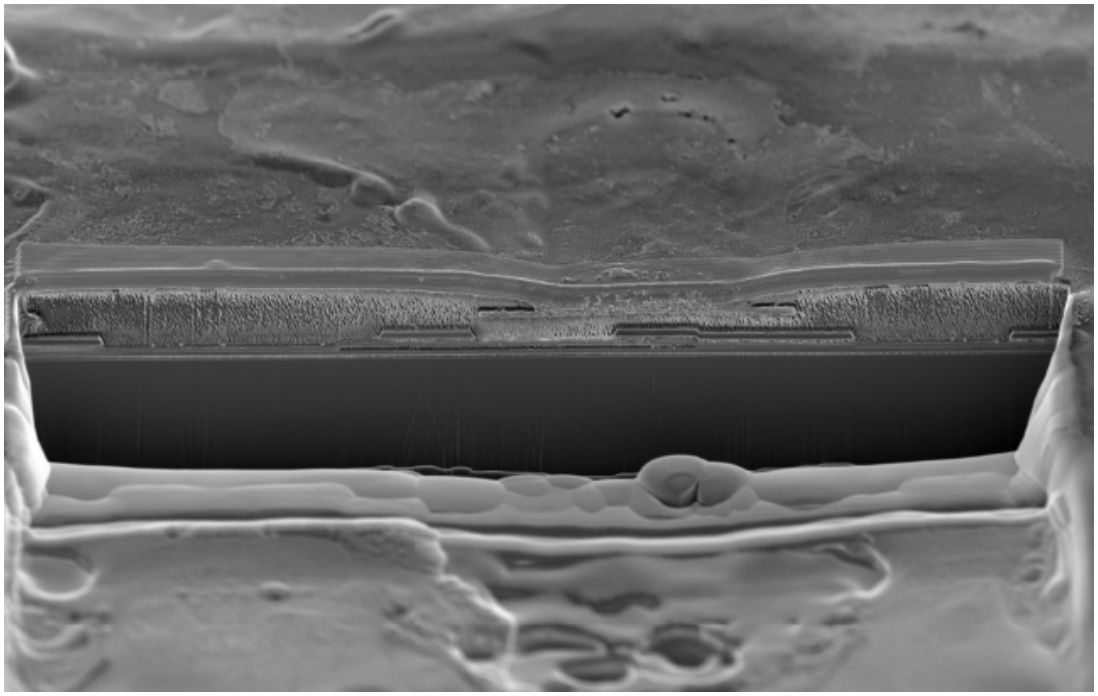
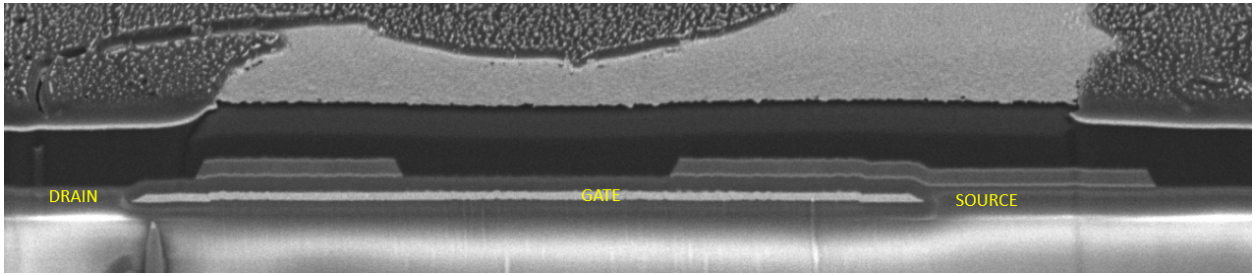
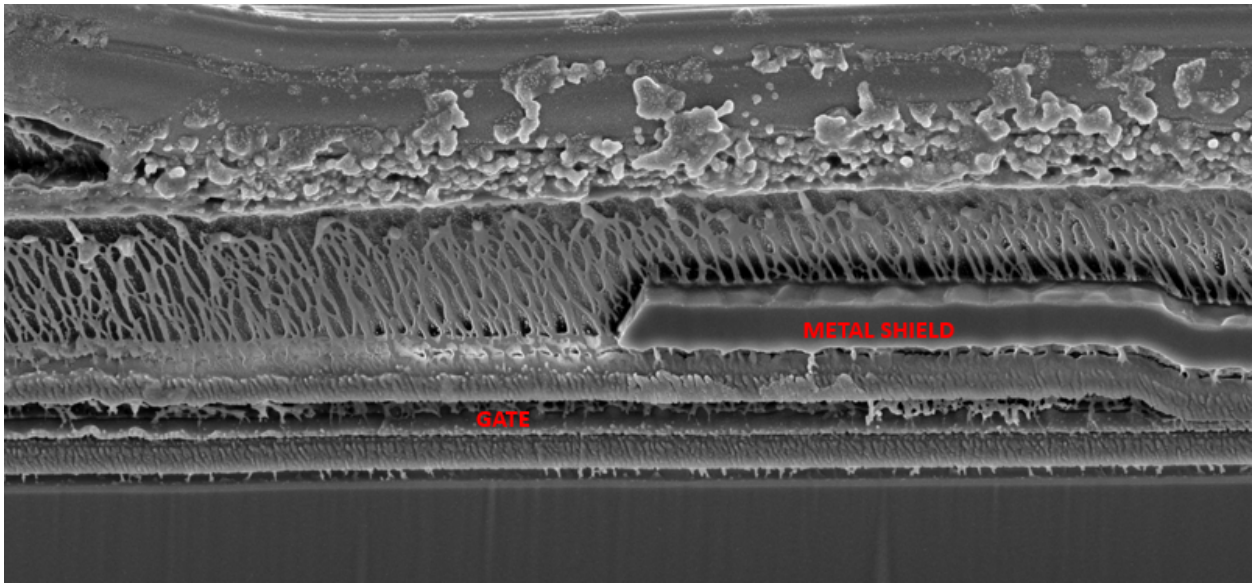
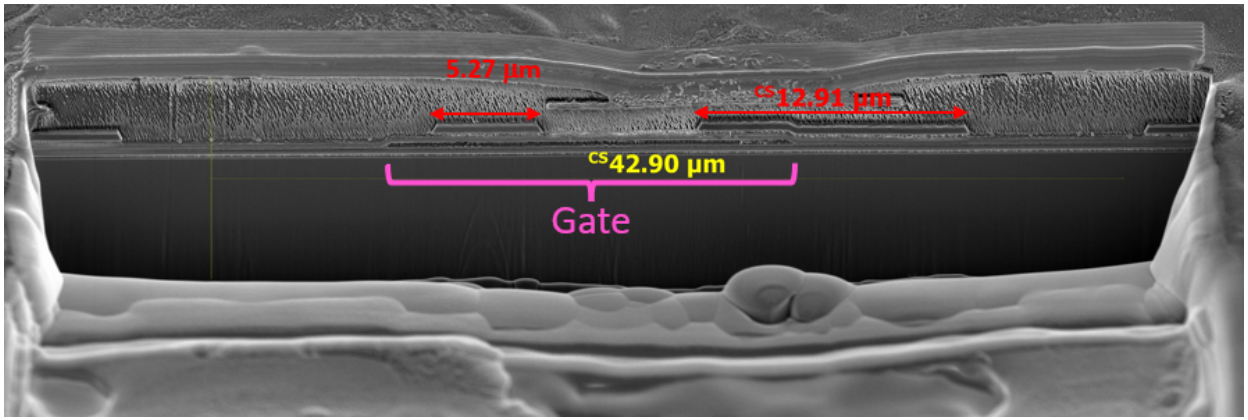
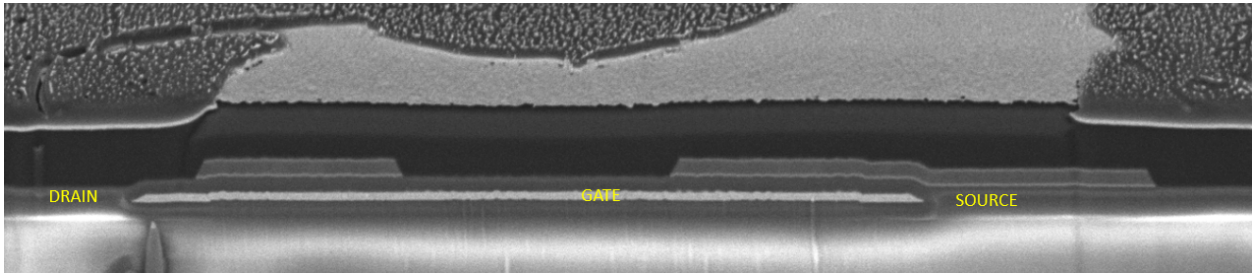
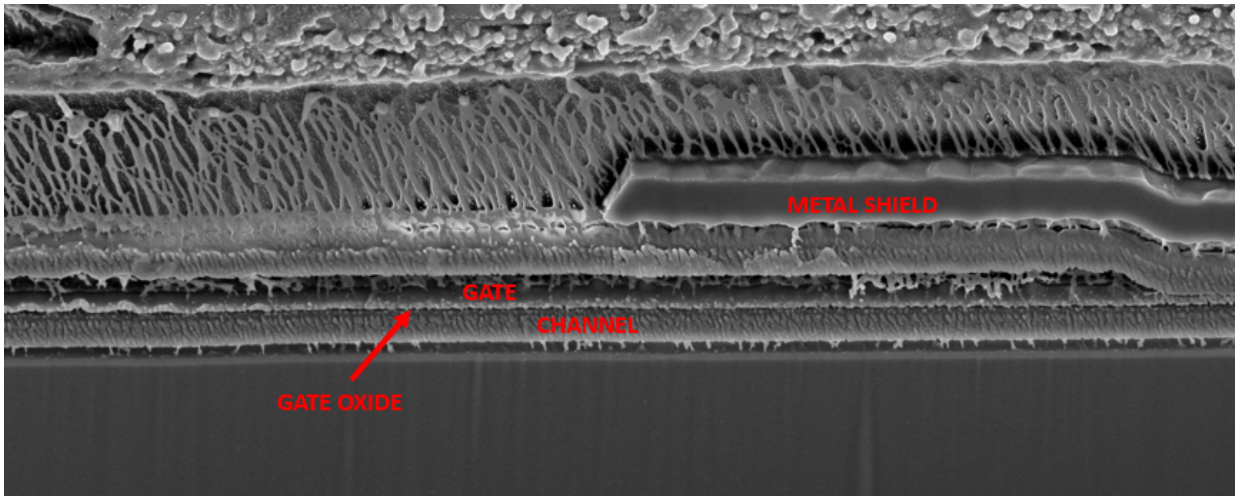
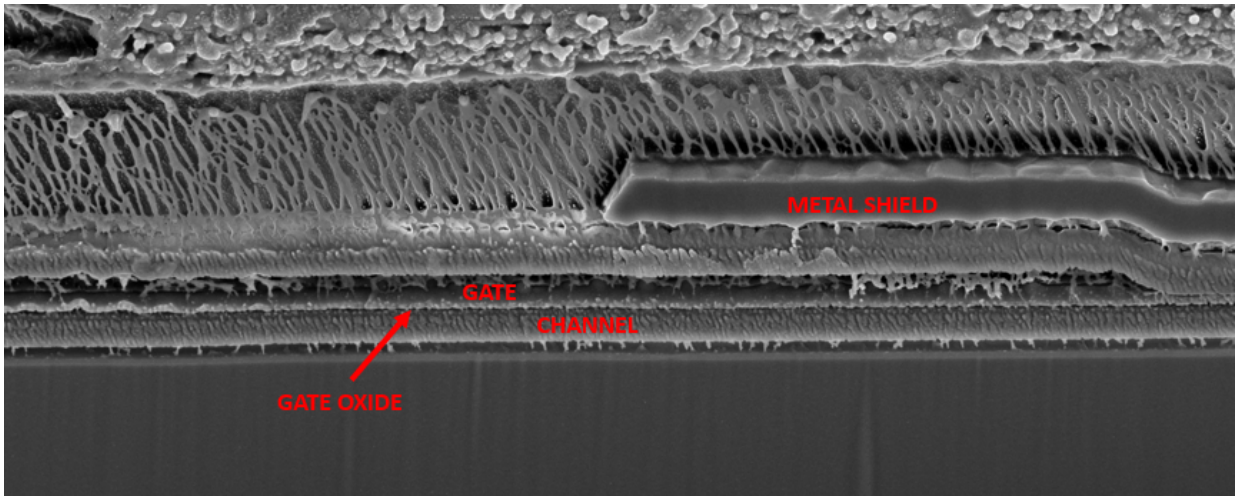
Claim Language	Exemplary Citations in Galaxy S
	 Magnified optical image of a portion of a pixel circuit in Galaxy S.

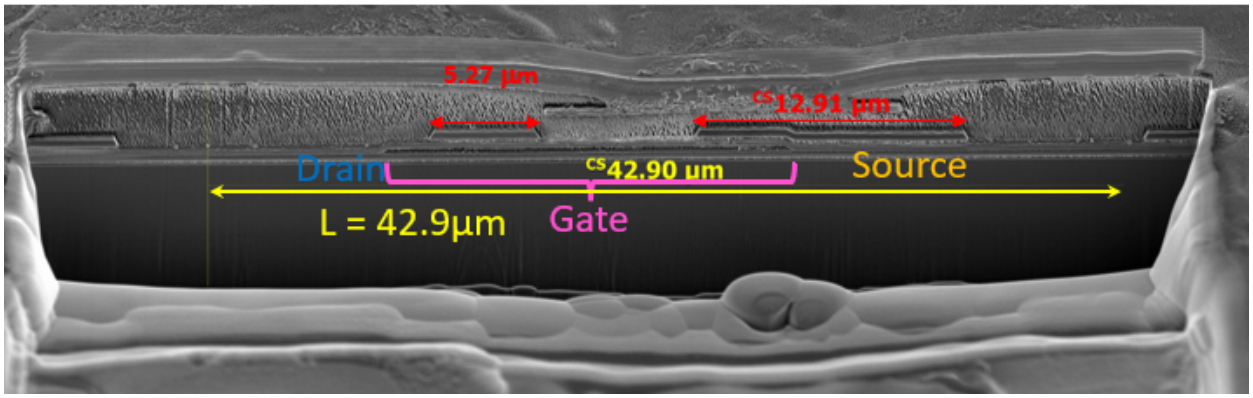
Claim Language	Exemplary Citations in Galaxy S
	 TEM image showing cross-section of a semiconductor structure in Galaxy S.
[1a] a gate electrode, disposed on the substrate;	Galaxy S discloses or renders obvious a gate electrode, disposed on the substrate.

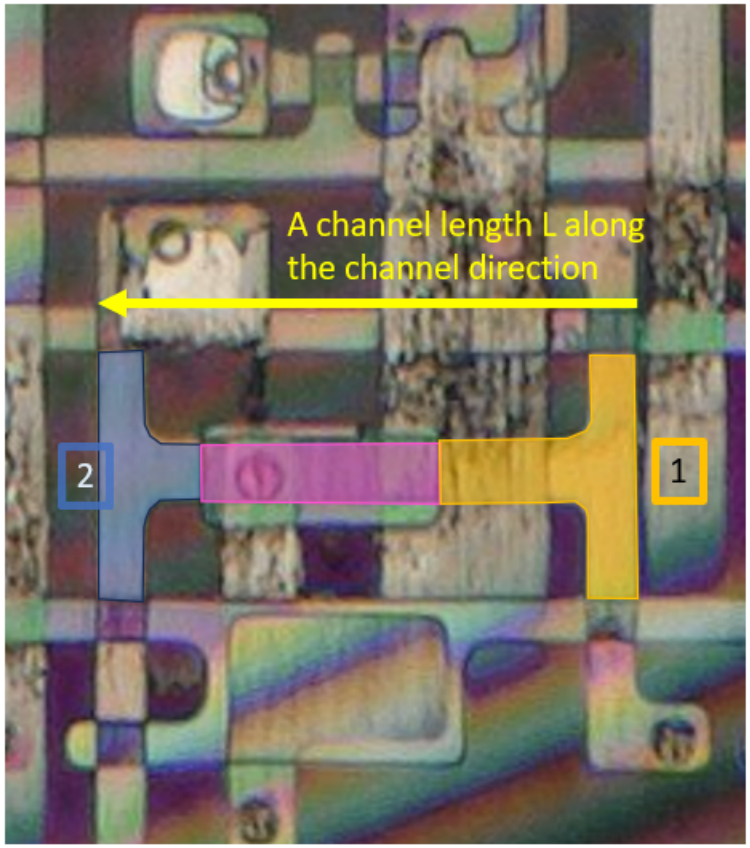
Claim Language	Exemplary Citations in Galaxy S
	 Magnified TEM image (annotations added) showing cross-section of a semiconductor structure in Galaxy S.  Magnified TEM image (annotations added) showing cross-section of a semiconductor structure in Galaxy S.

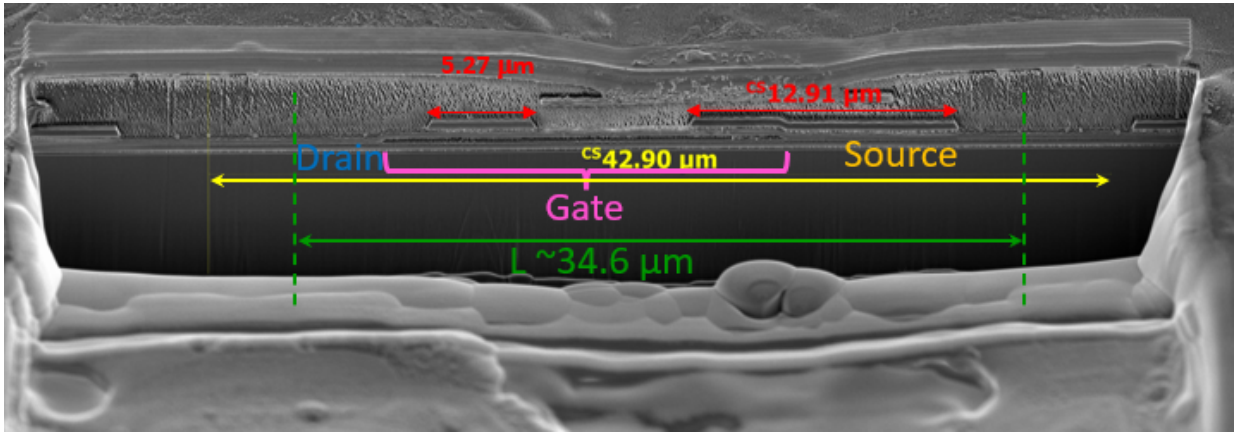
Claim Language	Exemplary Citations in Galaxy S
	 Lower magnification TEM image (annotations added) To the extent this limitation is not expressly or inherently disclosed, this limitation is well-known and common place in the art. It would have been a simple matter of design choice to modify the transistor design in the Galaxy S to the alternative well-known design, as demonstrated by the citations to this limitation in Ex. D2 (Hwang), D3 (Masumitsu), D4 (Lee), D5 (Cho), D6 (Park) and D7 (Tateishi).
[1b] a gate insulating layer, disposed on the substrate, and covering the gate electrode;	Galaxy S discloses or renders obvious a gate insulating layer, disposed on the substrate, and covering the gate electrode.

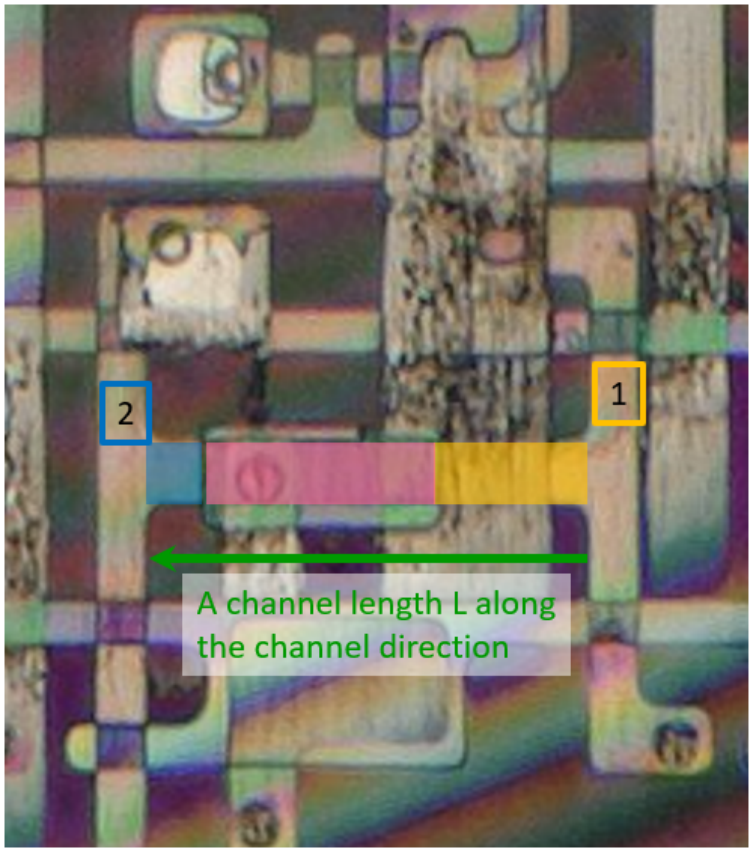
Claim Language	Exemplary Citations in Galaxy S
	 Magnified TEM image (annotations added) showing cross-section of semiconductor structure in Galaxy S.  Magnified TEM image (annotations added) showing cross-section of semiconductor structure in Galaxy S.

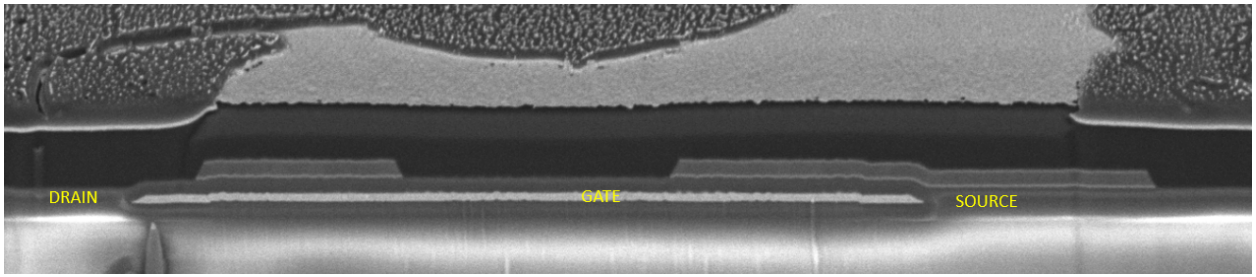
Claim Language	Exemplary Citations in Galaxy S
	To the extent this limitation is not expressly or inherently disclosed, this limitation is well-known and common place in the art. It would have been a simple matter of design choice to modify the transistor design in the Galaxy S to the alternative well-known design, as demonstrated by the citations to this limitation in Ex. D2 (Hwang), D3 (Masumitsu), D4 (Lee), D5 (Cho), D6 (Park) and D7 (Tateishi).
[1c] a channel layer, disposed on the gate insulating layer and located above the gate electrode, wherein the channel layer has a channel length L along a channel direction and has a first side and a second side opposite to the first side;	Galaxy S discloses or renders obvious a channel layer, disposed on the gate insulating layer and located above the gate electrode, wherein the channel layer has a channel length L along a channel direction and has a first side and a second side opposite to the first side.  Magnified TEM image (annotations added) showing cross-section of semiconductor structure in Galaxy S.

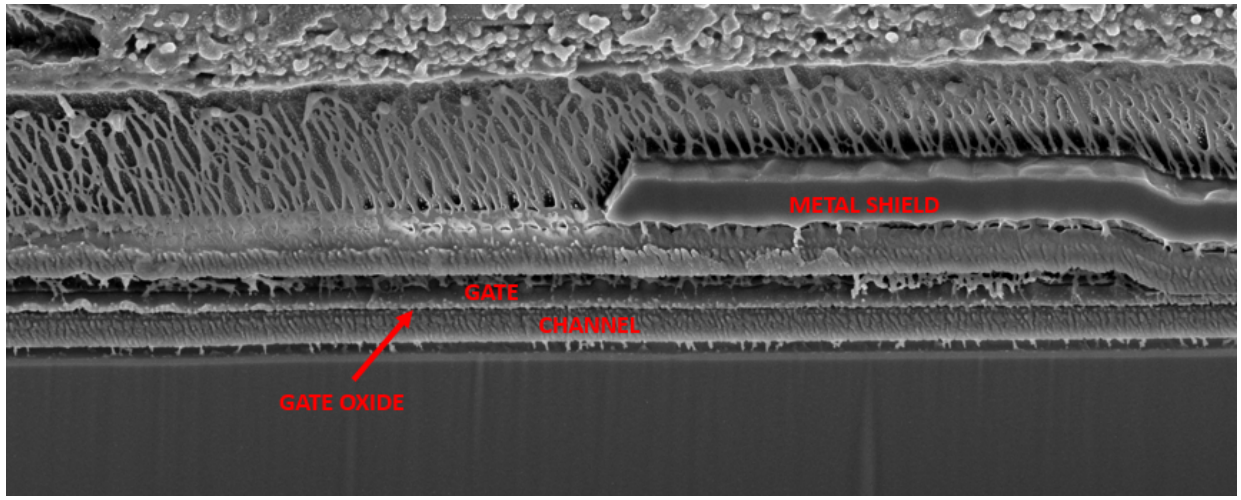
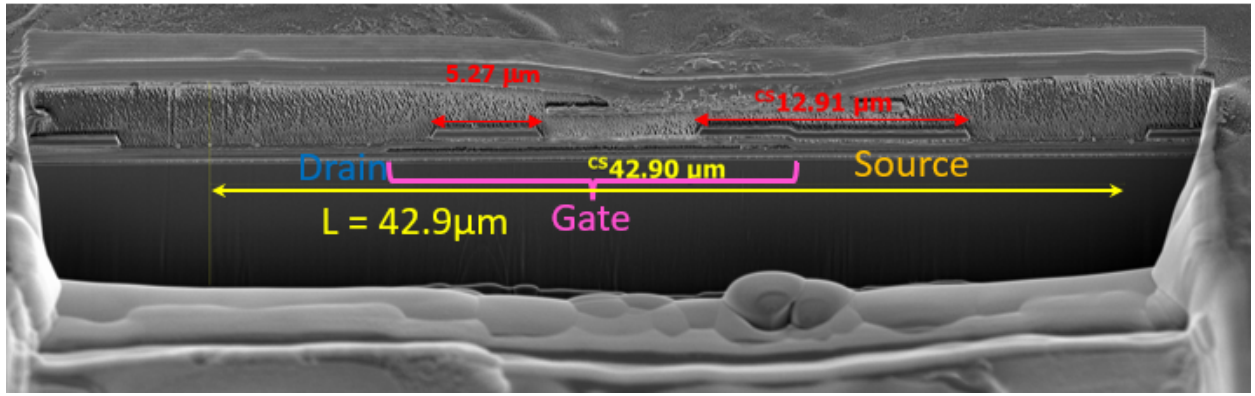
Claim Language	Exemplary Citations in Galaxy S
	 Lower magnification TEM image (annotations added) showing one possible identification of the claimed channel layer, with channel layer length (L).

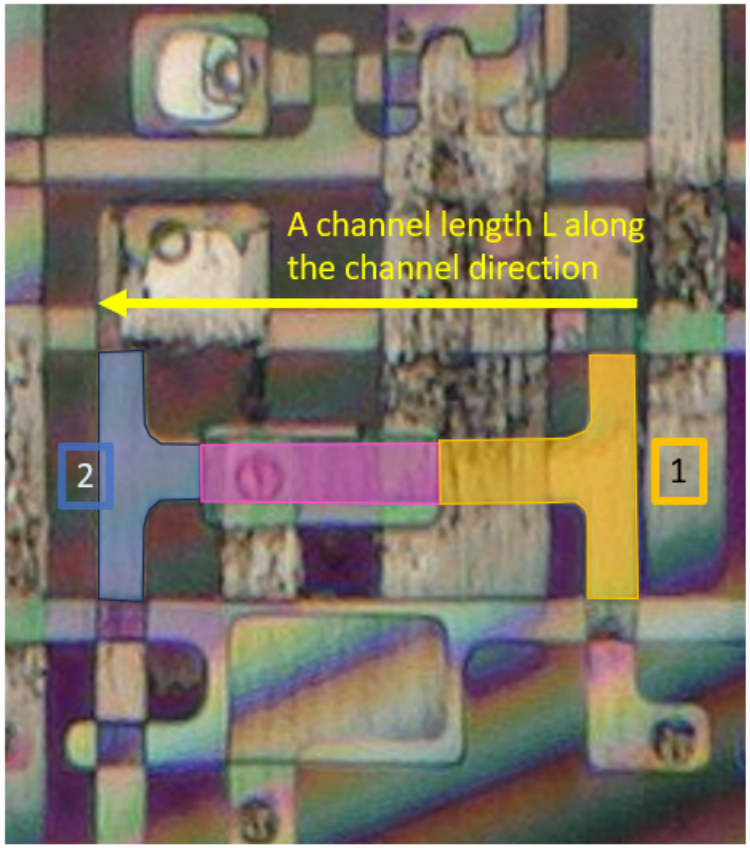
Claim Language	Exemplary Citations in Galaxy S
	 Optical image (annotations added) of a portion of a pixel circuit in Galaxy S. Alternatively, Galaxy S discloses an alternative identification of the claimed channel layer, as shown below.

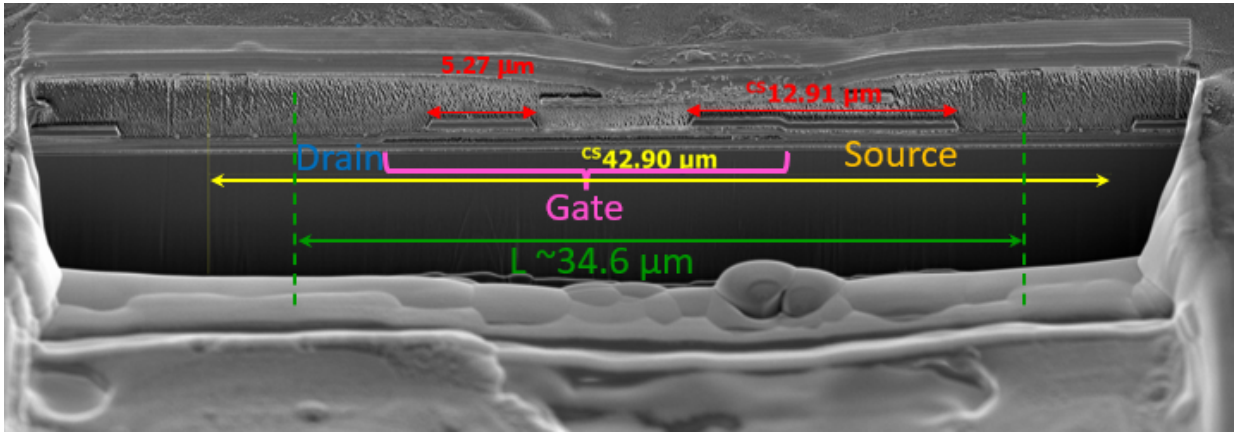
Claim Language	Exemplary Citations in Galaxy S
	 Lower magnification TEM image (annotations added) showing one possible identification of the claimed channel layer, with channel layer length (L).

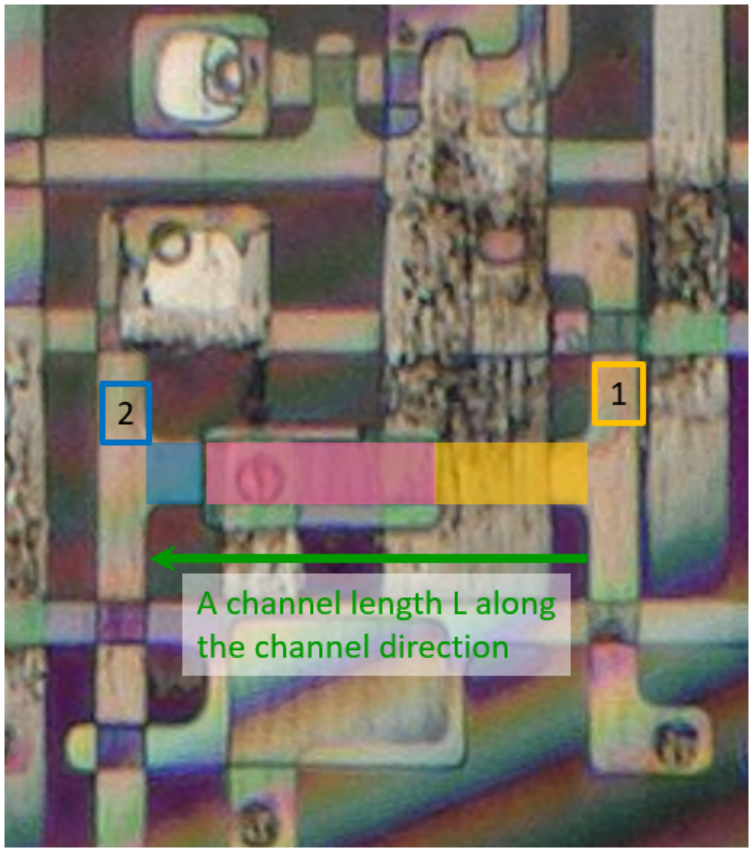
Claim Language	Exemplary Citations in Galaxy S
	 Optical image (annotations added) of a portion of a pixel circuit in Galaxy S.

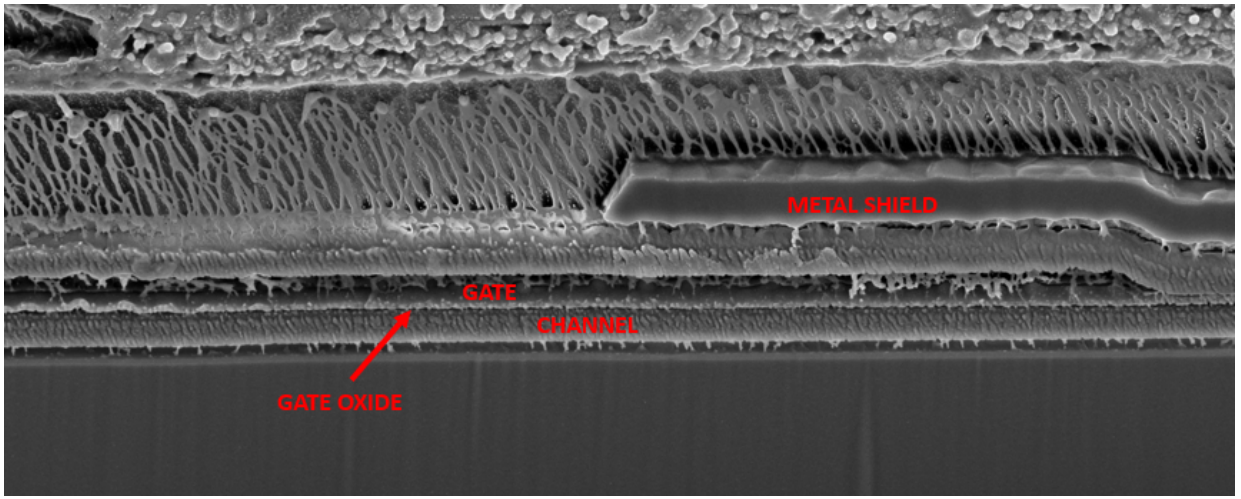
Claim Language	Exemplary Citations in Galaxy S
	To the extent this limitation is not expressly or inherently disclosed, this limitation is well-known and common place in the art. It would have been a simple matter of design choice to modify the transistor design in the Galaxy S to the alternative well-known design, as demonstrated by the citations to this limitation in Ex. D2 (Hwang), D3 (Masumitsu), D4 (Lee), D5 (Cho), D6 (Park) and D7 (Tateishi).
[1d] a source electrode and a drain electrode, located at the two opposite sides of the channel layer, and electrically connected to the first side and the second side of the channel layer, respectively;	Galaxy S discloses or renders obvious a source electrode and a drain electrode, located at the two opposite sides of the channel layer, and electrically connected to the first side and the second side of the channel layer, respectively.  Magnified TEM image (annotations added) showing cross-section of a semiconductor structure in Galaxy S.

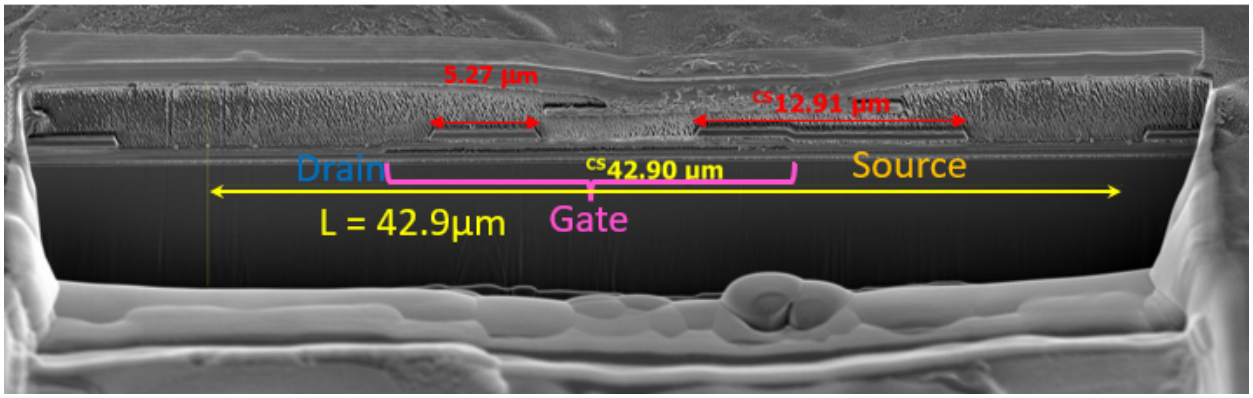
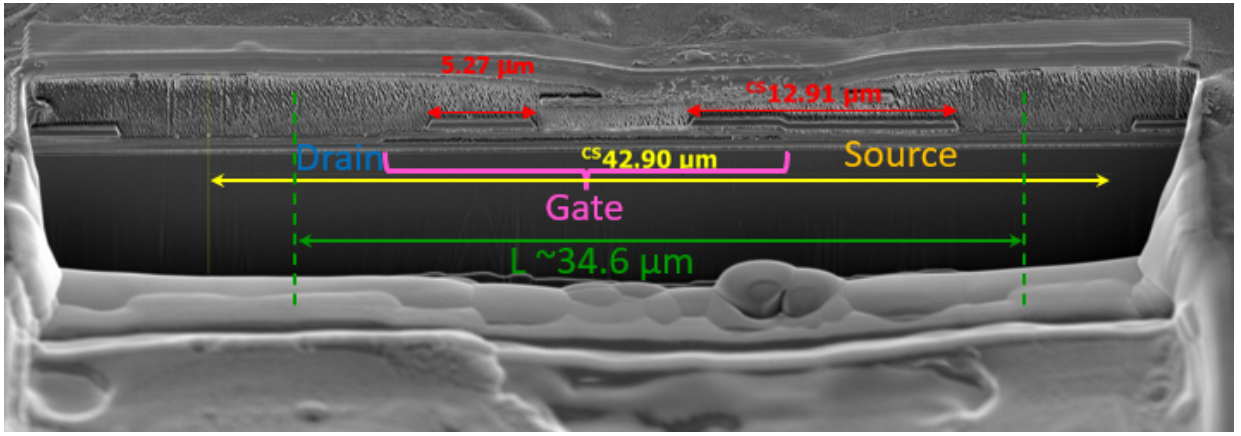
Claim Language	Exemplary Citations in Galaxy S
	 Magnified TEM image (annotations added) showing cross-section of a semiconductor structure in Galaxy S.  Lower magnification TEM image (annotations added)

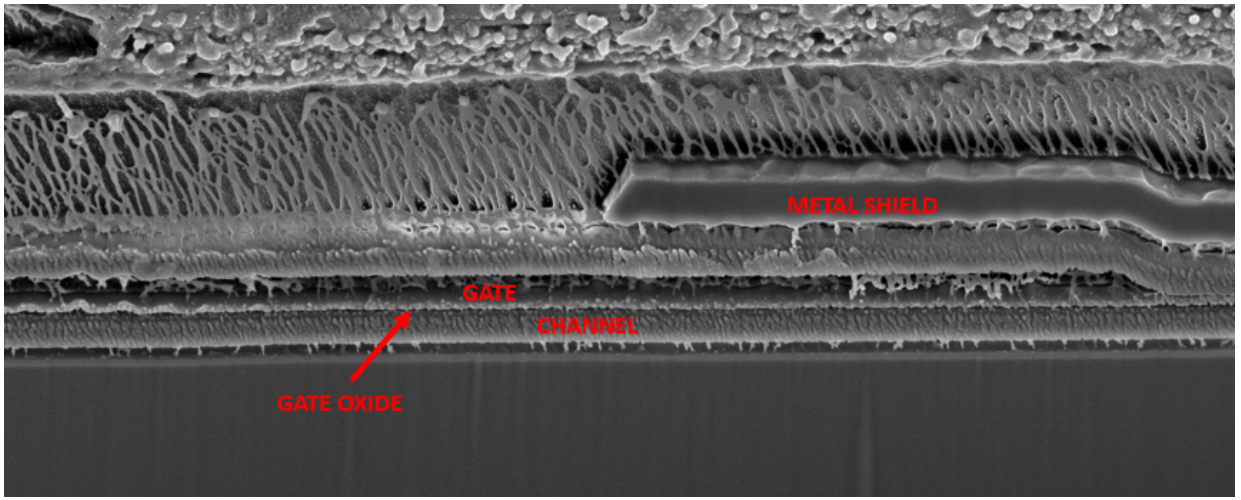
Claim Language	Exemplary Citations in Galaxy S
	 Optical image (annotations added) of a portion of a pixel circuit in Galaxy S.

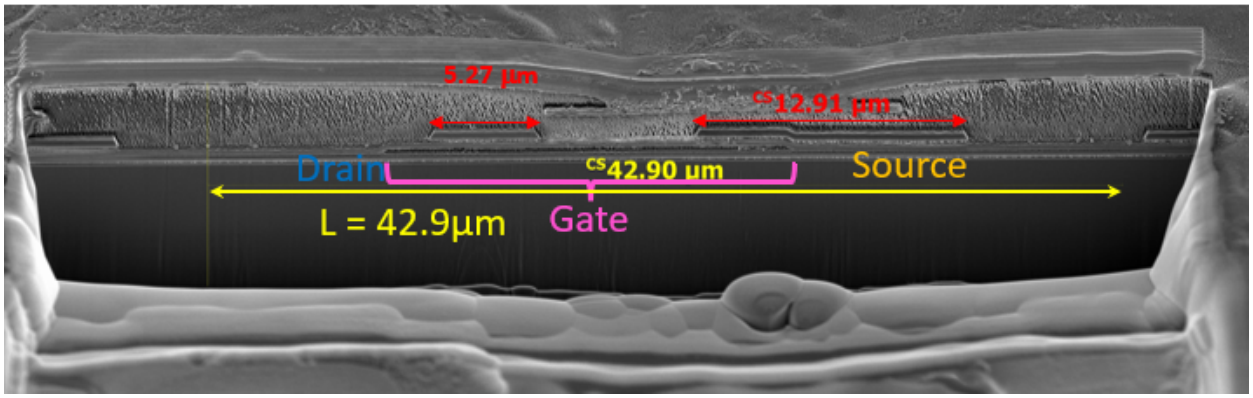
Claim Language	Exemplary Citations in Galaxy S
	 Lower magnification TEM image (annotations added)

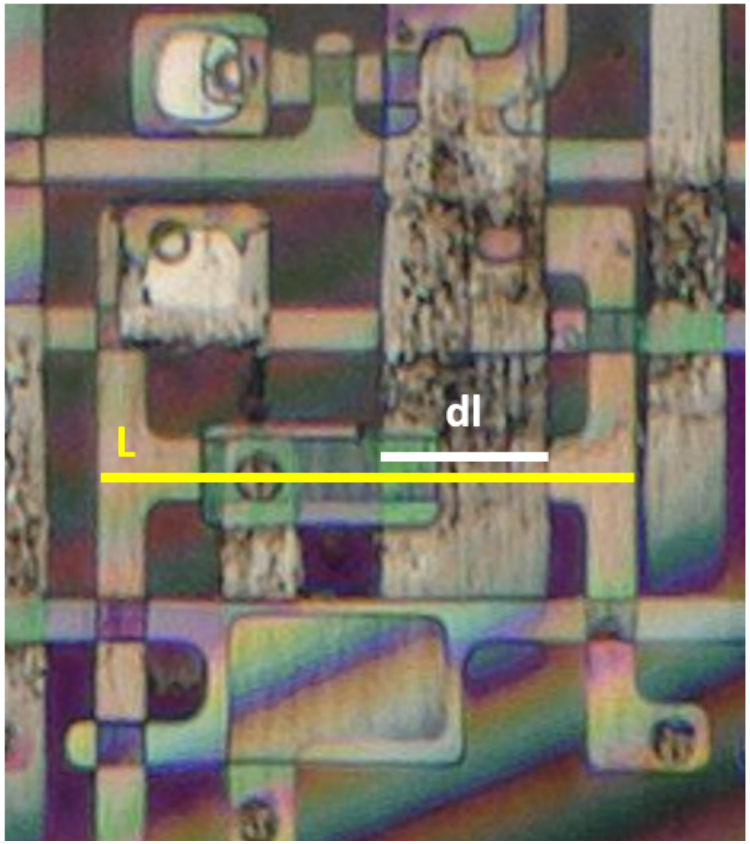
Claim Language	Exemplary Citations in Galaxy S
	 Optical image (annotations added) of a portion of a pixel circuit in Galaxy S. To the extent this limitation is not expressly or inherently disclosed, this limitation is well-known and common place in the art. It would have been a simple matter of design choice to modify the transistor design in the Galaxy S to the alternative well-known design, as demonstrated by the citations to this limitation in Ex. D2 (Hwang), D3 (Masumitsu), D4 (Lee), D5 (Cho), D6 (Park) and D7 (Tateishi).

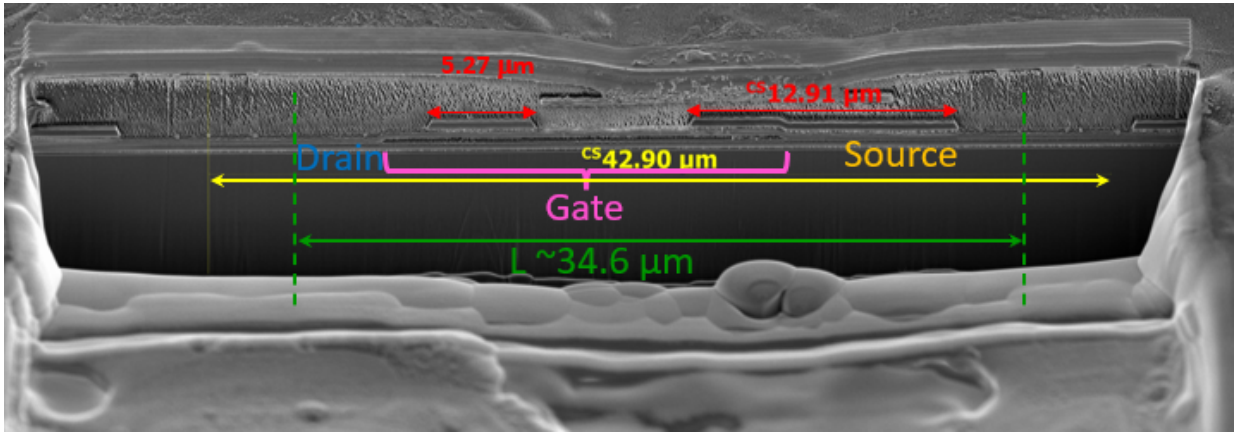
Claim Language	Exemplary Citations in Galaxy S
[1e] a dielectric layer, covering the source electrode, the drain electrode and the channel layer; and	Galaxy S discloses or renders obvious a dielectric layer, covering the source electrode, the drain electrode and the channel layer.  Magnified TEM image (annotations added) showing cross-section of a semiconductor structure in Galaxy S.

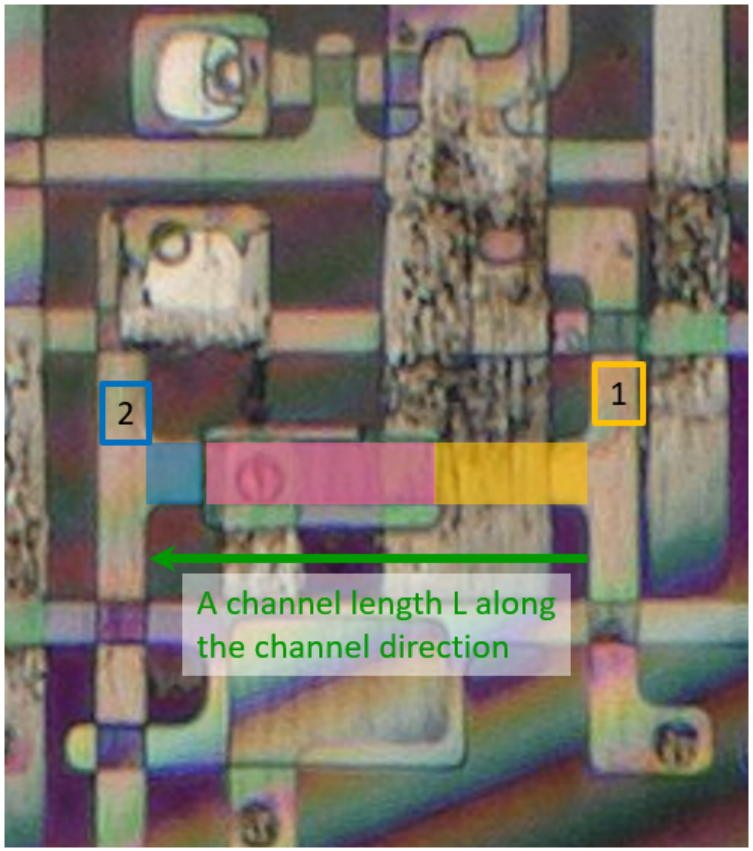
Claim Language	Exemplary Citations in Galaxy S
	 Lower magnification TEM image (annotations added)  Lower magnification TEM image (annotations added) To the extent this limitation is not expressly or inherently disclosed, this limitation is well-known and common place in the art. It would have been a simple matter of design choice to modify the

Claim Language	Exemplary Citations in Galaxy S
	transistor design in the Galaxy S to the alternative well-known design, as demonstrated by the citations to this limitation in Ex. D2 (Hwang), D3 (Masumitsu), D4 (Lee), D5 (Cho), D6 (Park) and D7 (Tateishi).
[1f] a conductive light-shielding pattern layer, disposed on the dielectric layer, and overlapped to a portion of the source electrode and a portion of the channel layer in a vertical projection, wherein the conductive light-shielding pattern layer does not overlap to the drain in the vertical projection, and the conductive light-shielding pattern layer and the channel layer have an overlapping length d1, and 0.3≦d1/L≦0.85.	Galaxy S discloses or renders obvious "a conductive light-shielding pattern layer, disposed on the dielectric layer, and overlapped to a portion of the source electrode and a portion of the channel layer in a vertical projection, wherein the conductive light-shielding pattern layer does not overlap to the drain in the vertical projection, and the conductive light-shielding pattern layer and the channel layer have an overlapping length d1, and 0.3≦d1/L≦0.85.  Magnified TEM image (annotations added) showing cross-section of a semiconductor structure in Galaxy S.

Claim Language	Exemplary Citations in Galaxy S
	 Lower magnification TEM image (annotations added) showing dimensions of one identification of the claimed channel layer and the conductive light shielding layer in the channel direction for a semiconductor structure in Galaxy S.

Claim Language	Exemplary Citations in Galaxy S
	 Optical image (annotations added) of a portion of a pixel circuit in Galaxy S.

Claim Language	Exemplary Citations in Galaxy S
	 Lower magnification TEM image (annotations added) showing dimensions of one identification of the claimed channel layer and the conductive light shielding layer in the channel direction for a semiconductor structure in Galaxy S.

Claim Language	Exemplary Citations in Galaxy S
	 Optical image (annotations added) of a portion of a pixel circuit in Galaxy S. As demonstrated, under any of the identifications of the claimed channel layer and conductive light shielding layer, the d1/L ratio in a semiconductor structure in Galaxy S is greater than 30% and less than 85%.

Claim Language	Exemplary Citations in Galaxy S
	To the extent Galaxy S does not expressly or inherently disclose this limitation, it is rendered obvious alone or in combination with one or more of the references identified below. As demonstrated by the references cited herein, this limitation is disclosed in at least each of Sung, Kim, Liang, Hwang, Masumitsu, Yamashita or Godo, and it would have been obvious to combine Galaxy S with the knowledge of POSITA as well as any one or more of Sung, Kim, Liang, Hwang, Masumitsu, Yamashita or Godo as set forth below. Sung at 2:39-59; 6:55-67; Figs. 1-4 Kim at [0051]-[0057]; Figs. 4-5. See also Liang at Abstract; [0029]-[0031], [0050]-[0058]; Figs. 2-3, 6-7; See also citations to this limitation in Ex. D2 (Hwang), Ex. D3 (Masumitsu). It would have been obvious to include a conductive light shielding pattern layer to overlap with a portion of the channel layer for light shielding. The problems associated with light entering a channel region of a transistor and the adverse impacts on transistor performance are well-known to POSITA and extensively documented in the prior art. Some exemplary references are summarized herein. Light can create electron-hole pairs ("EHPs") in semiconductors and thus alter the density of charge carriers in the material. Streetman at 96-97, 103; *see generally* Chapter 4. These EHPs alter the electrical properties of the semiconductor (and thus the device), including *e.g.*, the threshold voltages in transistors and/or increase leakage current. These problems are especially acute for optoelectronic devices due to the presence of light generating elements integrated with, and in close proximity to, such transistors. For example, this problem is discussed in Yamashita. Yamashita relates to organic electroluminescent devices that incorporates transistor circuitry. Yamashita at [0009]-[0010]. Yamashita addresses the known problem in the art when light enters the channel region of a transistor and causes a shift in the threshold voltage of the transistor. Yamashita at [0036]-[0038]. Yamashita discloses that in such devices, light can enter a channel region of a transistor (even

Claim Language	Exemplary Citations in Galaxy S
	one located in an adjacent pixel) due to internal scattered light from repeated reflections. Yamashita at [0035]-[0037], Fig. 7. Such shifts in the threshold voltage are undesirable in drive transistors for organic light emitting diodes ("OLEDs") as they lead to unintended fluctuations in the drive current, and therefore fluctuations in the brightness of the OLED element. Yamashita at [0013]-[0015], [0038]-[0042], Figs. 8-9. Yamashita discloses a solution to this problem is to form a conductive light-shielding layer that is arranged above the channel region of the TFT in order to shield it from light. Yamashita at [0045]-[0048], [0052], [0095]-[0099] (disclosing "the light shield pattern 67 should preferably be so arranged as to cover the sampling transistor T1 as well as the entire channel layer of the driving transistor T2"), Fig. 13. Yamashita discloses that while any material that reduces the amount of scattered light entering the thin-film transistor would help address the problem, metal materials are superior. Yamashita at [0048]-[0049], [0136]-[0137]. Yamashita further teaches that the metal light-shielding layer should be electrically connected to a constant potential line. Yamashita at [0047], [0101]-[0103]. Similarly, Godo discloses that it is well-known in the art that when semiconductor material (in a transistor of a display device) is irradiated with light, light leakage current will be generated due to the photovoltaic effect and deteriorates the display quality. Godo at [0004]. Godo discloses that mitigation techniques such as shielding the semiconductor layer from light were known. *Id.*, [0004]-[0006]. Reducing the leakage current can be accomplished by shielding the semiconductor layer with a conductive electrode made with various metals and their alloys. *Id.*, [0012]; [0015]-[0016]; [0045]. KR100853543 likewise discloses the use of a light-blocking film in an OLED display to stop light (external or from an adjacent pixel) from entering the semiconductor layer of a TFT to ensure stable driving properties for the transistor. KR100853543 at Abstract, <9>, <16>, <38>, <39>. KR100853543 explains that this light can generate a photocurrent in the semiconductor layer and adversely impact the driving properties of the TFT. KR100853543 at <15>. KR100659756 is yet another reference that discloses the problem with light entering the semiconductor layer of a TFT, particularly those with a bottom-gate structure. KR100659756 at 5. KR100659756 discloses to use one or more metals (including aluminum and molybdenum that

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Claim Language	Exemplary Citations in Galaxy S
	are good light reflectors and good electrical conductors) as suitable materials for forming a conductive light-blocking film to prevent both external light as well as internally generated light (*e.g.* from the OLED) from causing a negative effect on the TFT. KR100659756 at 7. This well-known problem would have provided a POSITA with the motivation to incorporate a conductive light shielding layer. The '471 patent discloses "metal" as the broad class of materials suitable for the conductive light-shielding pattern layer. '471 patent at 3:58-61, 4:40-5:9. A POSITA would have readily recognized that the exemplary metals and metal alloys cited herein have high electrical conductivity because they are well-known metal materials used for interconnects in semiconductor devices. Further, a POSITA would have understood that a layer formed using any one of these exemplary metals would have light-shielding properties for multiple reasons. First, a POSITA would have recognized that metals are good reflectors of light. Therefore, most of the light incident on metal materials are reflected rather than transmitted through the material. Light incident on these exemplary metallic surfaces would instead be reflected back, as is well known to those of skill in the art. Second, with respect to any light that is not reflected back (which will be a small fraction of the incident light), most of it will be absorbed by these metal materials well before it can travel through the thickness of the material. HandbookII at 35.6. A POSITA would have recognized that the absorption rate of light (*i.e.*, an electromagnetic field) as it propagates within a metal material is characterized by its "skin depth," a parameter indicating the distance where the light intensity has attenuated by about 86.5% due to absorption in the material. HandbookII at 35.3-35.7. In other words, after accounting for incident light being reflected at the surface, less than 14% of the light intensity will penetrate past the skin depth, with the light intensity continuing to decrease the further the distance it propagates into the material.

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Claim Language	Exemplary Citations in Galaxy S
	The skin depth parameter δ is given by the formula $\delta = \sqrt{\frac{2}{\omega\mu\sigma}}$, where ω is the frequency of the electromagnetic wave, μ is the magnetic susceptibility of the material, and σ is the electrical conductivity. HandbookII at 35.6 (equation 11). This equation shows that the skin depth (or the penetration depth) of an electric field through a material depends inversely on its frequency and on the conductivity of the material, meaning the skin depth will decrease as frequency increases or as conductivity increases. As is well known, metals are highly conductive, and light oscillates at very high frequencies (light in the visible spectrum is in the Terahertz range, where 1 Terahertz (THz) is 10^{12} oscillations per second). Therefore, both factors contribute to a very small penetration depth for light incident on a metal (due to its high conductivity), thus motivating the use of a conductive light shielding layer. Indeed, at optical frequencies, the skin depth of most metals is only approximately 50 nanometers (where one nanometer is one billionth of a meter). HandbookII at 35.6. Third, it is expressly known in the art that metals such as aluminum, aluminum alloy, tungsten, copper, molybdenum and titanium are conductive materials with light-shielding (or light blocking) properties suitable for shielding a semiconductor from light. Godo at [0006] and [0012] (explaining the use of a gate electrode to shield a semiconductor layer in a TFT from light), [0045] (disclosing the use of metal materials including aluminum, tungsten, copper, molybdenum, titanium and their alloys for the gate electrode); Yamashita at [0046] (use of metal wiring layer to shield a TFT from light), [0096] (disclosing the use of aluminum and molybdenum for the light-shielding pattern); KR100659756 at 7 (disclosing the use of aluminum and molybdenum for the light-shielding pattern); Someya at 12:35-44 (disclosing that an aluminum film has high light shielding properties). Thus, to the extent actually performing the light-shielding function is not inherently or expressly disclosed, or otherwise rendered obvious, this would have been obvious because it was well known and documented in the art that light can interact with semiconductors and adversely impact electrical performance of TFTs. The problem is exacerbated for transistors in devices like

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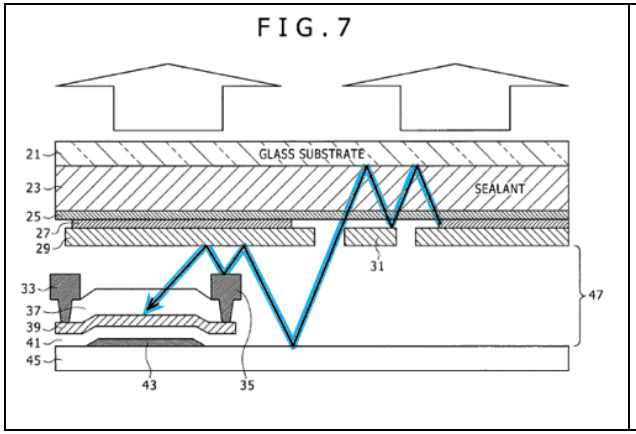
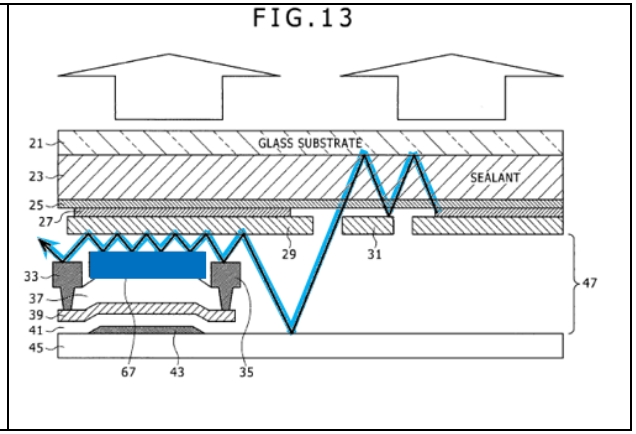
	Hwang due to the proximity of integrated light emitting elements (either within the same pixel or in adjacent pixels). A POSITA would have had a reasonable expectation of success in making the proposed combination. Such a combination would have merely required express recognition that the conductive layer in Galaxy S is not merely capable of, but actually is intended to perform a light-shielding function, as the material has light-shielding properties (as discussed above). Moreover, Yamashita discloses that during operation, light generated by the LED's in adjacent pixels can be scattered internally enter channel region of TFTs integrated into the same chip and adversely impact device performance. Yamashita at [0037]. Figure 7 of Yamashita is an exemplary illustration[1] showing a "light ray" whereby light can be scattered into the channel region of a TFT. Yamashita at Fig. 7, [0035]-[0037]. Yamashita teaches using a patterned metal layer (67) to shield the transistor from the scattered light. Yamashita at [0095]-[0099]; compare Figs. 7 and 13 (annotations added to show scattered light with and without the light shield layer 67).

[1] A POSITA would have recognized that the illustrated light path is merely exemplary, and additional pathways exist for light to scatter into the channel region of the TFT. Further, while different devices may have arrangements of the reflective layers, the different arrangements of the reflective layers would merely lead to different pathways whereby light can reach the TFT channel regions. Thus, Fig. 7 of Yamashita illustrates the more general teachings that motivate the need for shielding the transistor from scattered light.

Claim Language	Exemplary Citations in Galaxy S
	  *See also* KR100853543 at Abstract, <9>, <16>, <38>, <39> disclosing the problem of light generated from an adjacent pixel adversely impacting a drive TFT. Thus, based on the teachings in Yamashita, a POSITA would have recognized that light generated within the device in Galaxy S can be internally scattered and enter the channel region of the transistor, in the absence of the metal layer overlying the transistor (as disclosed in Yamashita). This would motivate a POSITA to modify the design to include a conductive light-shielding pattern layer overlying the channel layer. As discussed for [1c] *supra*, Galaxy S discloses a channel layer with length L in the channel direction[2]. A POSITA would review the disclosure in Galaxy S and at once envisage a commonly-used TFT configuration in which (a) the source and drain regions are equal in length, and (b) where the length of the channel region is no greater than that of the source (or drain) region. At a minimum, the disclosure in Galaxy S would have rendered obvious such a TFT configuration. A POSITA would have recognized this as a common TFT configuration for OLED

[2] Unless other specified, the term "length" with respect to the source, channel and drain regions as used herein refers to the length in the channel direction.

Claim Language	Exemplary Citations in Galaxy S
	drive transistors because a shorter channel region length typically allows higher current and faster switching speeds, whereas lithography limits and the necessity for forming highly conductive source/drain contacts typically result in source/drain regions that are similarly sized but larger than the channel region (*i.e.*, condition (b)). Once the source/drain regions are large enough to accommodate electrical connection to highly conductive contacts, TFT drive transistor designs would not further increase those dimensions unnecessarily. This is because a general design goal would be to increase pixel density in an OLED display panel (thus leaving the source and drain regions equally sized, *i.e.*, condition (a)). Thus, a POSITA would have recognized the figures in Galaxy S to at least render obvious (if not outright depict) a well-known and common TFT drive transistor configuration having relative proportional dimensions as set forth above. See also Sung at 6:55-67; Figs. 1-4. Based on these two conditions for this common (or at least obvious) TFT configuration, a POSITA can ascertain the range for the length of the drain region as a fraction of the total length L. For fixed L, the drain region length reaches a value of approximately 0.33L where the source, channel and drain regions are of equal lengths. A POSITA would have recognized that transistor performance generally improves (*e.g.*, higher speed and greater power efficiency) when the length of the channel region is reduced. Mead at 33-37. This performance improvement is the basis for the drive towards miniaturization of semiconductor devices, manifesting itself as the well-known Moore's Law. Accordingly, a POSITA would have recognized that common transistor designs may have a channel region length that is less than the length of the source/drain regions due to the advantages of a decreased channel region length. Mead at 33-37. Since the drain region length is equal to 0.33L (when the source, drain and channel regions are equal lengths), decreasing the length of the channel region relative to the source/drain region would lead to a corresponding increase in the source/drain region length such that it is greater than 0.33L. Therefore, a POSITA would have recognized that for many common transistor configurations, 0.33L would be a typical lower bound for the drain channel length. Of course, a POSITA would also have recognized that the channel region length cannot be reduced too much because of fabrication tolerances and also because of the well-known short channel effect. Streetman at 298-299, 325-327. However, even if we consider an extreme hypothetical design where the channel region length is negligibly small relative to the equally-sized source and drain

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	regions (such that each of these regions make up 50% of the semiconductor layer 158), the drain region length would still reach a maximum value of no greater than 0.5L. Thus, the relative size of the drain region is bounded between 0.33L and 0.5L. Since the source region is the same size as the drain region, its length is likewise bounded between 0.33L and 0.5L. The length of the channel region would make up the difference (*i.e.*, L - length of source - length of drain), thus ranging between approximately 0L (in the extreme hypothetical case) to 0.33L. Hwang discloses the conductive light-shielding pattern layer that overlies the channel layer that overlaps both the source and channel regions, but there are potential disadvantages if it overlaps the drain region. See, e.g., Hwang at [0048], [0050], [0083]-[0087]; Fig. 6d. See also discussion and citations in claim 17, incorporated herein by reference. Therefore, a POSITA would have been motivated to utilize a conductive light-shielding pattern that overlaps with the source and channel regions, but not the drain region. Based on the relative dimensions for the common TFT configuration as discussed above, the overlapping length d1 is (L – length of drain) which is between 0.5L and 0.67L. Accordingly, a POSITA would have recognized that any TFT drive transistor Td so configured would result in a d1/L ratio to fall between 0.5 to 0.67, the entirety of which falls within the claimed range of 0.3 to 0.85. See also, Kim at [0051]-[0057]; Figs. 4-5. In the alternative, to the extent the claimed relative dimensions of the source, channel and drain regions of a TFT are not taught or rendered obvious to a POSITA by Galaxy S such that the resulting device would meet the claimed d1/L ratio (as set forth above), those dimensions would have been rendered obvious in view of Godo. As discussed below, Godo discloses specific dimensions for bottom gate TFTs. Godo at [0199], [0201], Figs. 1A, 1B, 2A, 2B, 4A, 4B, 20A and 20B. Galaxy S broadly discloses an arrangement of semiconductor materials to form a TFT, and metallic materials for shielding the channel region in the transistor in an organic luminescent device. The combination of Galaxy S with Godo modifies these general teachings for a broad genus of TFTs with Godo's disclosure of more particular species of TFTs (with specific dimensions for the source, channel and drain regions for the transistor) according to known methods to yield predictable results. As discussed above, suitable dimensions for such transistors

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Claim Language	Exemplary Citations in Galaxy S
	would have been well known in the art, and a POSITA would have immediately recognized a broad class of TFTs with at least known ranges of relative proportions for the dimensions of the source, channel and drain regions of the transistor. Nevertheless, to the extent a POSITA remained unaware of suitable dimensions for the drive transistor, the POSITA would have been motivated to investigate known suitable dimensions in the art for transistors suitable for driving an LED device and been led to Godo's disclosures of appropriate dimensions. Godo at [0150], [0161], [0163] (disclosing TFT 420 is a drive transistor), [0165] (disclosing TFT 420 drives LED element 430), [0199], [0201]; Figs. 1A-2B, 4A, 4B, 18A, 18B, 20A (with one set of dimensions) and 20B (another set of dimensions). As will be demonstrated below, regardless of which set of TFT dimensions a POSITA uses from Godo to modify Galaxy S, limitation [1f] is still rendered obvious. A POSITA would have had a reasonable expectation of success in making the proposed combination because techniques such as photolithography for defining patterns for forming transistor elements with the disclosed dimensions were well known in the art. Patterning feature sizes that are in the micron (μm) resolution were well within the ordinary state of the art. Further, the relevant transistors disclosed in both Galaxy S and Godo are both bottom gate TFTs. See e.g. Godo at Figs. 1A-2B, 4A-B. Thus, the only "modification" of Galaxy S is to incorporate the specific geometric dimensions taught in Godo to form the lithography masks, then perform the same standard and routine TFT fabrication steps to thereby form a transistor with the dimensions as disclosed in Godo. The proposed combination would not have required undue experimentation and would have yielded the predictable result, namely, a drive transistor with the dimensions as disclosed in Godo. Godo discloses the dimensions for the source, channel, and drain regions for TFTs suitable for driving an LED device. Godo at Figs. 20A, 20B; *see also id.*, [0150], [0161], [0199], [0201] (explaining the dimensions shown for Figs, 20A and 20B apply to the transistors of Figs. 1A-2B, 4A and 4B); Figs. 1A-2B, 4A, 4B, 18A, 18B. To the extent a POSITA, having reviewed Galaxy S, required additional express guidance on suitable TFT dimensions, the POSITA would have been motivated to seek out those teachings in the art and it would have been obvious to use the TFT dimensions disclosed in Godo as explained above. As will be shown below, forming a

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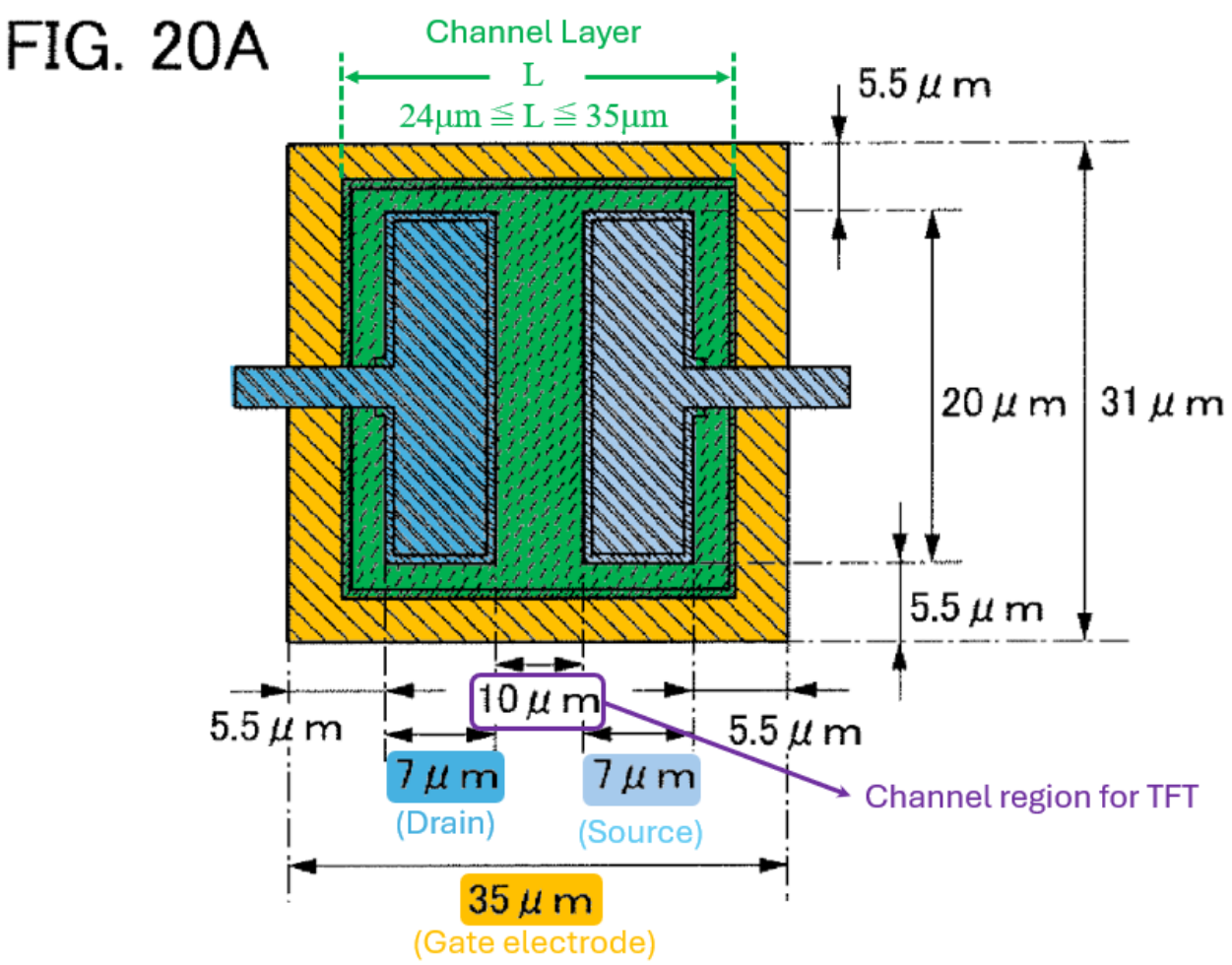
	transistor (using either Godo's Fig. 20A or Fig. 20B dimensions), and thereafter forming a conductive light shielding layer that overlaps the source and channel regions but not the drain region of the transistor would result in $0.3 \leqq d1/L \leqq 0.85$ as required by this limitation. The TFT shown in Godo's Fig. 20A has a channel direction that runs left/right, and the length of source and drain regions along the channel direction are 7μm. The length of the channel region is 10μm.

Claim Language	Exemplary Citations in Galaxy S
	 Godo at Fig. 20A (annotations added). The length of the channel layer ("L" as claimed in [1c]) is not expressly disclosed, but a POSITA would have understood that the disclosed dimensions

<table>
<tr><th>Claim Language</th><th>Exemplary Citations in Galaxy S</th></tr>
<tr><td></td><td>necessarily bound the range of L. In particular, L must be less than 35μm (the length of the gate electrode), but also greater than the sum of the source[3], channel and drain regions (7μm + 10μm + 7μm = 24μm), i.e., 24μm ≦L≦35μm.

As for the d1 dimension, as discussed above, it would be obvious to have an overlap length d1 that shields the source and channel regions but not the drain region. Applying Godo's dimensions, the minimum value for d1 is 17μm (the sum of source region and channel region lengths), and the maximum value for d1 would be the entire channel layer except for the drain, i.e., d1 ≦ L - 7μm.

<table>
<tr><td></td><td>d1 (μm)</td><td>L (μm)</td></tr>
<tr><td>Minimum</td><td>17</td><td>24</td></tr>
<tr><td>Maximum</td><td>L-7</td><td>35</td></tr>
</table>

Based on these allowable ranges for d1 and L, the allowable range of d1/L can be determined. The minimum value for the fraction d1/L is achieved when the numerator d1 is minimized and the denominator L is maximized, i.e., $d1_{min}/L_{max}$ is 17μm/35μm = 0.48. To maximize d1/L, the maximum value for d1 is L-7μm as shown above. Substituting, the ratio $d1_{max}/L$ = (L-7μm)/L = 1-7/L. Thus, d1/L is maximized when 7/L is minimized, i.e., when L is maximized where L = 35μm. Thus, the maximum d1/L ratio is 1-7/35 = 1-0.2 = 0.8. Accordingly, using Godo's dimensions as disclosed in Fig. 20A, the resulting d1/L must be between 0.48≦d1/L≦0.8, wholly within the range as claimed in [1f]. Stated differently, any transistor that is sized consistent with</td></tr>
</table>

[3] This calculation includes only the lengths for the source region, channel region and drain region as disclosed in Godo because it seeks the lower bound for L. In other words, for a transistor to be consistent with the Godo disclosure, the length L must be large enough to accommodate the three expressly disclosed lengths, which is 24μm.

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Claim Language	Exemplary Citations in Galaxy S
	the express dimensions disclosed in Godo's Fig. 20A will necessarily result in d1/L between $0.48 \leqq d1/L \leqq 0.8$ where the channel and source regions are shielded but not the drain region. An illustrative example of a TFT layout consistent with the dimensions of Godo's Fig. 20A is provided below, where the exemplary layout has mirror symmetry about the center of the channel region, and where L is 30μm (which is near the middle of the allowed range).

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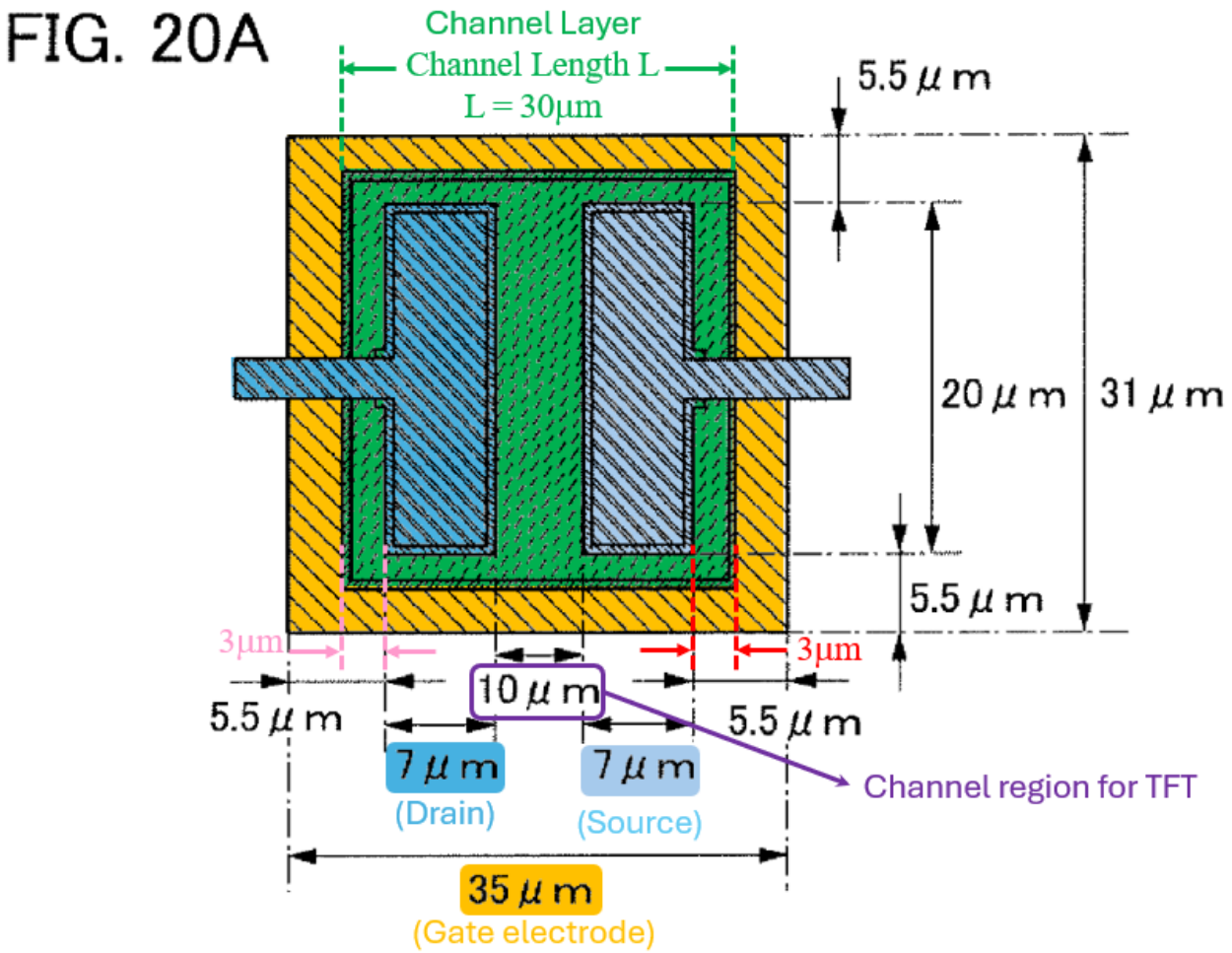
Claim Language	Exemplary Citations in Galaxy S
	 Godo at Fig. 20A (annotations added). Mirror symmetry means the length between the right-edge of the source region to the right-edge of the (green) channel layer is 3μm (*i.e.*, the length between the two dotted red lines), which is also the length between the left-edge of the drain region to the

Claim Language	Exemplary Citations in Galaxy S
	left-edge of the channel layer (*i.e.*, the length between the two dotted pink lines). This means d1 = 3μm+7μm+10μm = 20μm, while L = 30 μm. This leads to an illustrative value of d1/L of 0.67, which falls within the claimed range. Of course, this is but one illustrative example, whereas the more general analysis shows that any TFT with dimensions consistent with Godo's Fig 20A necessarily result in a d1/L within the claimed range where d1 spans the source and channel regions. The TFT shown in Godo's Fig. 20B has a channel direction that runs left-right, and the length of the channel layer is 17μm.

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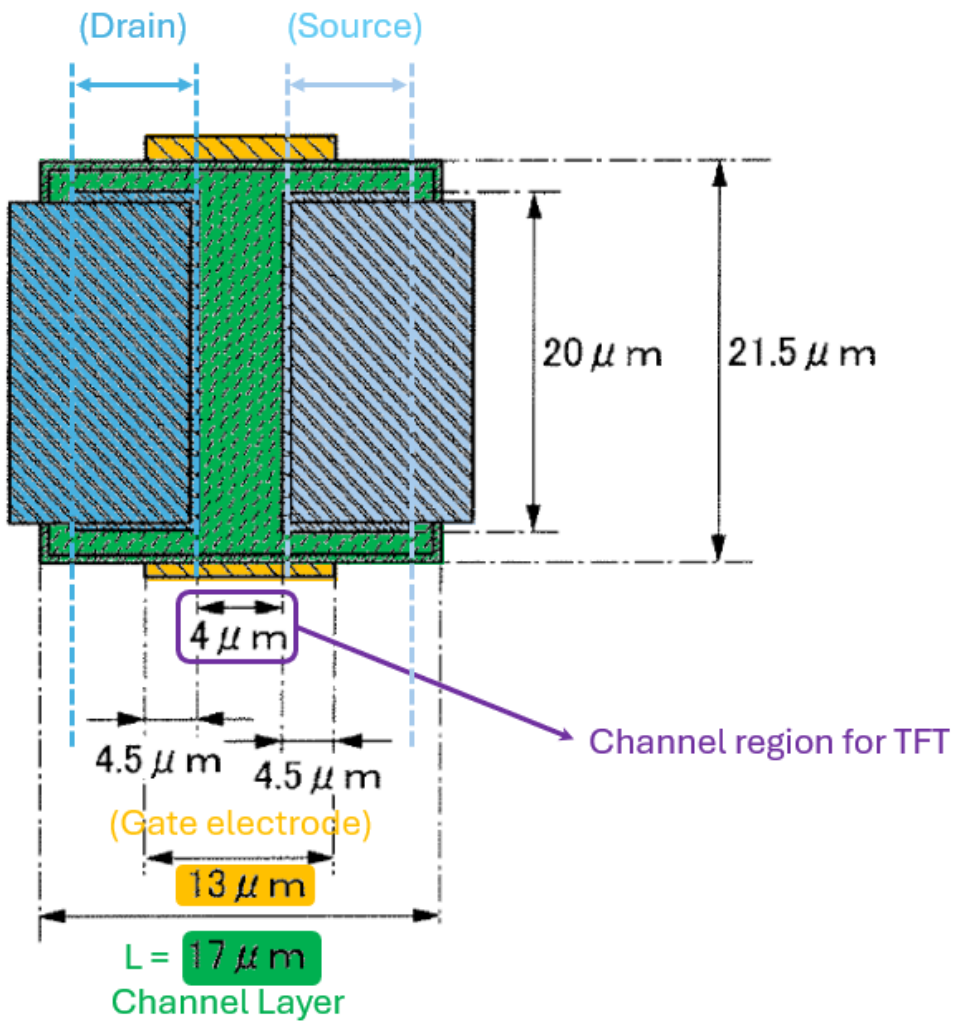
Claim Language	Exemplary Citations in Galaxy S
	FIG. 20B 

<table>
<tr><th>Claim Language</th><th>Exemplary Citations in Galaxy S</th></tr>
<tr><td></td><td>
Godo at Fig. 20B (annotations added). The channel region has length 4μm, but the exact lengths of the source/drain regions are not expressly disclosed, only that they are at least 4.5μm. The maximum source/drain length can be determined because the sum of the lengths of the source, channel and drain regions cannot exceed the channel layer length of 17μm. Thus, the maximum length for the source region is 8.5μm (taking the length of drain at the minimum 4.5μm), and the maximum length for the drain is 8.5μm (minimizing the source).

As for the d1 dimension, as discussed above, it would have been obvious for overlap length d1 to shield at least the source and channel regions, but not the drain region. Thus, applying Godo's Fig. 20B dimensions, the minimum value for d1 is 8.5μm (the sum of channel region length and the minimum source region length), and the maximum value for d1 would be the entire channel layer except for the drain length (which should be minimized), i.e., d1 ≦ 17 – 4.5μm.
<table>
<tr><td></td><td>d1 (μm)</td><td>L (μm)</td></tr>
<tr><td>Minimum</td><td>8.5</td><td>17</td></tr>
<tr><td>Maximum</td><td>12.5</td><td>17</td></tr>
</table>
Based on these allowable d1 values and the disclosed L dimension, the ratio d1/L must be between 8.5/17 and 12.5/17, or 0.5≦d1/L≦0.735, wholly within the range as claimed in [1f]. Stated differently, any transistor that is sized consistent with the express dimensions disclosed in Godo's Fig. 20A will necessarily result in d1/L between 0.5≦d1/L≦0.735 where the channel and source regions are shielded but not the drain region.

An illustrative example of a TFT layout consistent with the dimensions of Godo's Fig. 20B is provided below, where the exemplary layout has mirror symmetry about the center of the channel region.
</td></tr>
</table>

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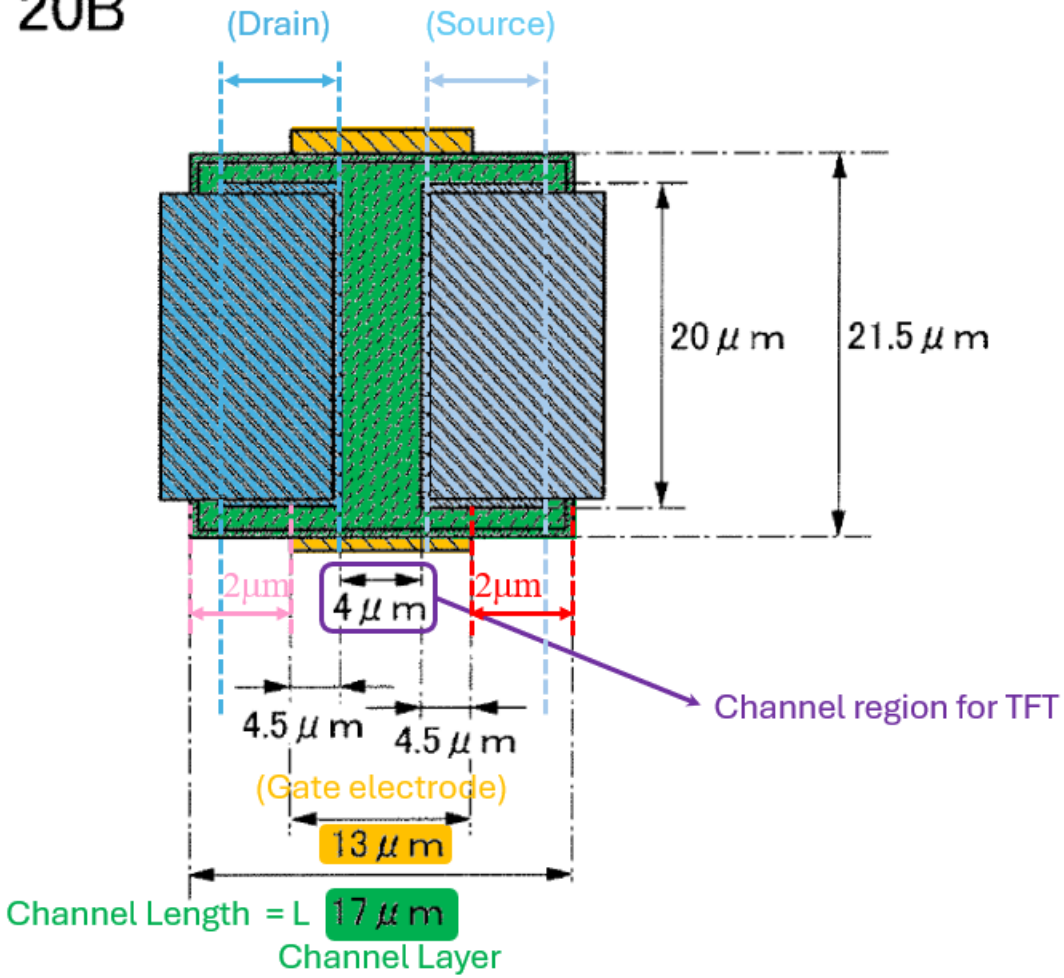
Claim Language	Exemplary Citations in Galaxy S
	FIG. 20B  Godo at Fig. 20A (annotations added). Mirror symmetry means the length between the right-edge of the gate electrode to the right-edge of the (green) channel layer is 2μm (*i.e.*, the length

Claim Language	Exemplary Citations in Galaxy S
	between the two dotted red lines), which is also the length between the left-edge of the gate electrode to the left-edge of the channel layer (*i.e.*, the length between the two dotted pink lines). This means d1 = 2μm+4.5μm+4μm = 10.5μm, while L = 17μm. This leads to an illustrative value of d1/L of 0.62, which falls within the claimed range. Of course, this is but one illustrative example, whereas the more general analysis shows that any TFT with dimensions consistent with Godo's Fig 20B necessarily result in a d1/L within the claimed range where d1 spans the source and channel regions. The analysis also applies for the transistor dimensions as disclosed in Sung (cited above) and results in a d1/L ratio within the claimed range where d1 spans the source and channel regions.
[17] The semiconductor structure as claimed in claim 1, wherein the conductive light-shielding pattern layer and the drain electrode are spaced by a distance along the channel direction in the vertical projection.	Galaxy S discloses or renders obvious the semiconductor structure as claimed in claim 1, wherein the conductive light-shielding pattern layer and the drain electrode are spaced by a distance along the channel direction in the vertical projection. See citations in claim 1. See citations in limitation [1f].

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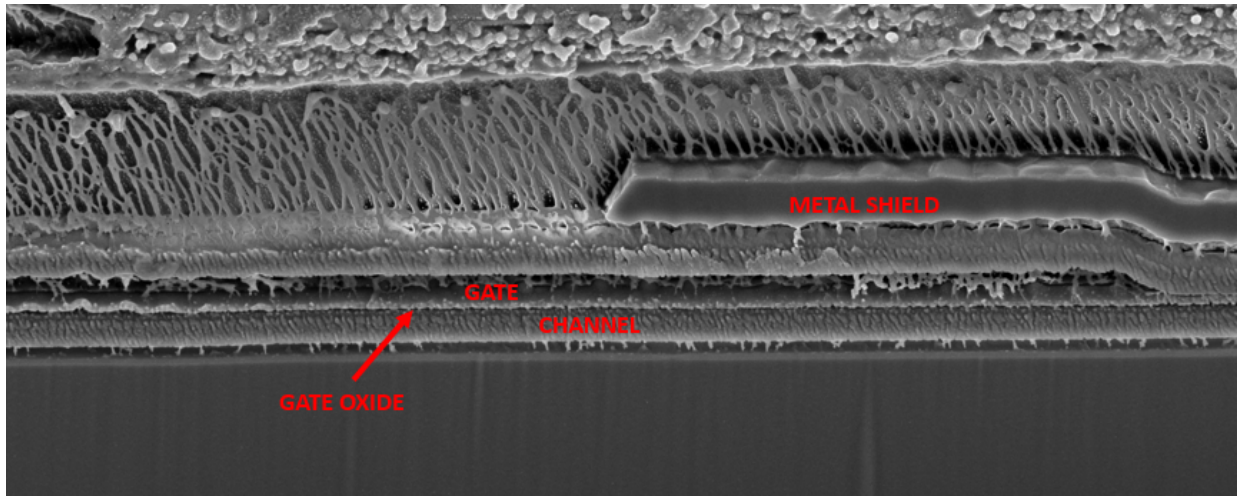
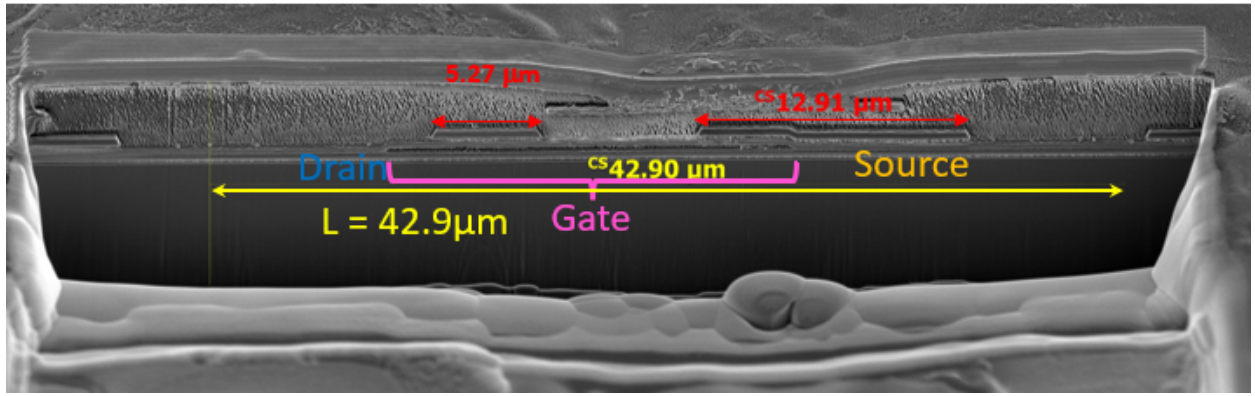
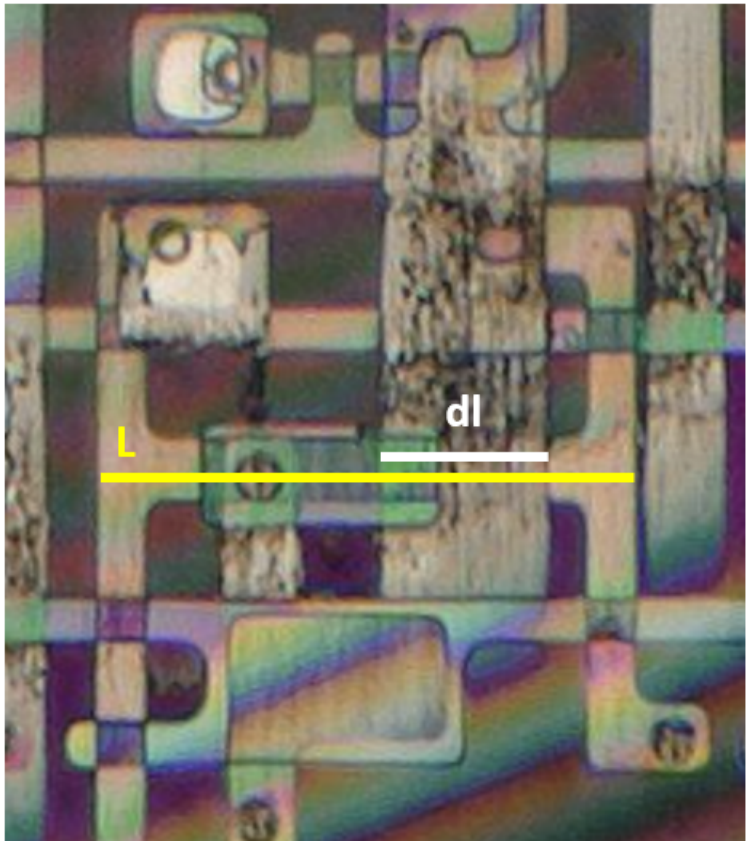
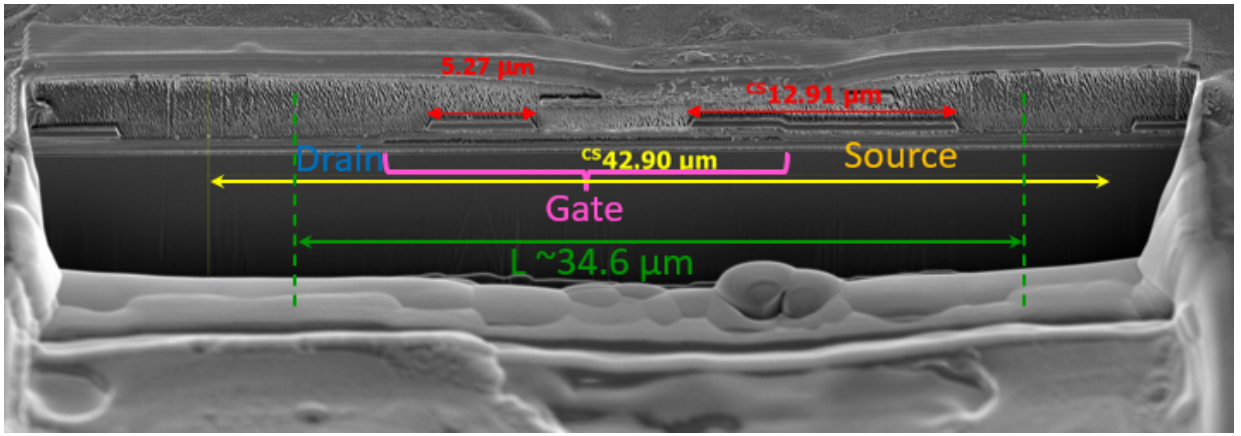
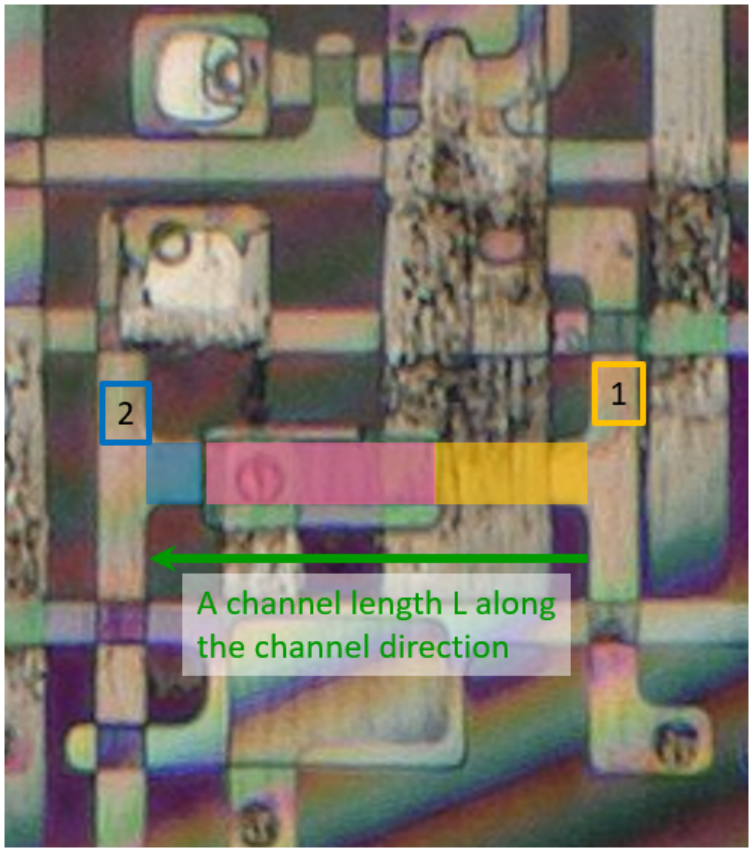
Claim Language	Exemplary Citations in Galaxy S
	 Magnified TEM image (annotations added) showing cross-section of a semiconductor structure in Galaxy S. 

Claim Language	Exemplary Citations in Galaxy S
	Lower magnification TEM image (annotations added) showing the conductive light shielding layer is spaced from the drain by a distance along the channel direction for a semiconductor structure in Galaxy S. 

Claim Language	Exemplary Citations in Galaxy S
	Optical image (annotations added) of a portion of a pixel circuit showing the conductive light shielding layer is spaced from the drain by a distance along the channel direction for a semiconductor structure in Galaxy S.  Lower magnification TEM image (annotations added) showing the conductive light shielding layer is spaced from the drain by a distance along the channel direction for a semiconductor structure in Galaxy S.

Claim Language	Exemplary Citations in Galaxy S
	 Optical image (annotations added) of a portion of a pixel circuit showing the conductive light shielding layer is spaced from the drain by a distance along the channel direction for a semiconductor structure in Galaxy S. To the extent Galaxy S does not expressly or inherently disclose this limitation, it is rendered obvious alone or in combination with one or more of the references identified below. As demonstrated by the references cited herein, this limitation is disclosed in at least each of Hwang,

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	Masumitsu, Sung, Kim, Liang, and/or Godo, and it would have been obvious to combine Galaxy S with the knowledge of POSITA and any one or more of Hwang, Sung, Kim, Liang, and/or Godo as set forth below. See citations to this limitation in Ex. D2 (Hwang). See citations to this limitation in Ex. D3 (Masumitsu). Hwang teaches layer 162/162a should cover the channel region and not overlap the drain electrode 154. Hwang at [0048]. As illustrated in Figure 6d, Hwang teaches that in the vertical projection, there may be very little space between the end of the drain electrode 154 and electrode 162a. Hwang at Fig. 6d. To the extent Figure 6d does not expressly disclose electrode 162a and drain electrode 154 are "spaced by a distance in the vertical projection," Hwang also teaches that, while electrode 162a covers the channel region to block the influence of electrode 170, it could be shortened, depending on need. Hwang at [0050] ("auxiliary electrode 162a. . . does not overlap the second drain electrode 154. The auxiliary electrode 162a may be … shorter… upon need."). One exemplary need disclosed by Hwang is to prevent short circuit between the auxiliary electrode 162a and the drain electrode 154. Hwang at [0050]. Thus, Hwang teaches that electrode 162a (which still should cover the channel region to block the influence of electrode 170) can be shortened (*i.e.*, spaced apart in the vertical projection) by a small amount to account for fabrication variances in order to mitigate a potential short circuit to the drain electrode. Because this claim does not require a particular minimum amount of distance for the "spaced apart" limitation, Hwang's wholistic teaching that electrode 162a covers the channel, does not overlap the second drain electrode and can, in fact, be even shorter expressly discloses this claim to a POSITA. Additionally or alternatively, claim 17 is obvious in view of Hwang. A POSITA would have understood that Hwang's teaching in paragraph [0050] related to shortening electrode 162a would not expose the entire channel region entirely, but only to shorten electrode 162a to the extent needed. This is because the disclosed function of the auxiliary electrode 162a is to shield the channel region from the electric potential at the cathode 170. Indeed, this shielding of the

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	channel region from the cathode voltage specifically solves the problem that Hwang's invention sought to overcome. Hwang at [0016]. Specifically, shielding the channel region overcomes the problems of brightness deterioration and non-uniformity. Hwang at [0072]; *see also id.*, [0069]-[0074] and Fig. 5. Therefore, a POSITA would have understood that shielding the channel region remains important, even though there may be other design tradeoffs that need to be considered. An exemplary tradeoff as expressly disclosed in Hwang that motivates increasing the spacing is to help prevent an unintentional short circuit between auxiliary electrode 162a (which is electrically connected to and thus on the same node as the source electrode) and the drain electrode 154. Hwang at [0050], [0066]. See also, Kim at [0051]-[0057]; Figs. 4-5. See also Liang at Abstract; [0026]-[0029], [0050]-[0058]; Figs. 2-3, 6-7; Further, as discussed in claim 1, the light-shielding pattern layer overlaps with at least the source region and the channel region of the transistor. A POSITA would have recognized that unintended parasitic capacitance between the source and drain has an adverse impact on the transistor performance. Streetman at 323. Thus, a POSITA would have been motivated to mitigate unintended capacitive coupling to the drain electrode by increasing the spacing (in the vertical projection) between the light-shielding layer and drain electrode 154 to increase the distance therebetween, thereby reducing the resulting capacitance. Schaum at 153-154. Therefore, the extent of the overlap of the light-shielding layer with the channel region requires a tradeoff between mitigating unintentional short circuits and/or the capacitive coupling to the drain and the benefits of shielding the channel region. Any decrease in the overlap length would necessarily cause the light shielding pattern layer and the drain electrode to be spaced by a distance along the channel direction in the vertical projection. As for quantifying the spaced apart distance, a POSITA would have recognized that the primary emphasis remains to provide as much shielding to the channel region as possible in order to reap the known benefits of light shielding, as discussed in claim 1. Therefore, this would have suggested to a POSITA that at least half of the channel region should remain shielded (if not more) in balancing these other considerations (such as capacitive coupling to the drain) while still preserving the main benefits for improving performance by shielding the channel region. This

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<table>
<tr><th>Claim Language</th><th>Exemplary Citations in Galaxy S</th></tr>
<tr><td></td><td>results in a minimum d1/L ratio of 0.5 with no change to the maximum d1/L ratio (0.67), which remains within the range claimed in [1f].

Alternatively, claim 17 is rendered obvious in view of Godo. The antecedent basis for the conductive light-shielding pattern layer recited therein comes from limitation [1f]. Therefore, the limitations recited in this claim is met for at least the same reasons set forth above for [1f]. Further, regarding the “spaced by a distance…” limitation, shortening the light-shielding layer (e.g., to mitigate capacitive coupling to the drain region) would decrease the d1 parameter and thereby reduce the d1/L ratio. Therefore, the upper bound for d1/L will still remain within the claimed range for [1f]. To investigate the impact of the modification on the lower bound of d1/L, the relative proportions of the transistor dimensions as disclosed in Godo’s Fig. 20A can be used, and then auxiliary electrode 162a shortened as set forth above (i.e., shielding half of the channel region). Thus, the minimum overlap length d1 is equal to the sum of the length of the source region (7μm) and half the length of the channel region (5μm), or 12μm. The allowable range for length L is unchanged (with a range between 24μm and 35μm), leading to 0.34≦d1/L≦0.5, which remains within the claimed range of [1f].

Using the relative proportions of the transistor dimensions as disclosed in Godo’s Fig. 20B and shortening the light-shielding layer as set forth above, the overlap length d1 is decreased by half of the length of the channel region, i.e., 2μm.

<table>
<tr><td></td><td>Revised d1 (μm)</td><td>L (μm)</td></tr>
<tr><td>Minimum</td><td>8.5 – 2 = 6.5</td><td>17</td></tr>
<tr><td>Maximum</td><td>12.5 – 2 = 10.5</td><td>17</td></tr>
</table>
</td></tr>
</table>

Claim Language	Exemplary Citations in Galaxy S
	This leads to a ratio of d1/L such that 0.38≦d1/L≦0.62, which remains within the claimed range of [1f]. Therefore, by configuring the conductive light-shielding pattern layer and the drain electrode such that they are spaced apart by a distance along the channel direction in a vertical projection, the d1/L ratio will decrease (compared to if the entire channel region is shielded), but the resulting d1/L ratio still lies within the range as recited in claim 1 from which claim 17 depends. The analysis also applies for the transistor dimensions as disclosed in Sung (cited for [1f] above).