

53.5: High-Speed AMOLED Pixel Circuit and Driving Scheme

**Dong-Wook Park, Chul-Kyu Kang, Yongsung Park, Boyong Chung,
Kyung-Hoon Chung, Byung-Hee Kim, and Sang Soo Kim**

**OLED R&D Center, Samsung Mobile Display Co., Ltd.,
Giheung-Gu, Yongin-City, Gyeonggi-Do, Korea**

Abstract

An active matrix organic light emitting diode pixel circuit and its driving scheme for high frame frequency are proposed for implementation of a 3D display. The proposed pixel circuit can compensate the threshold voltage distribution of low temperature poly silicon-thin film transistors at high-speed operation of 240Hz or more. According to the simulation, current deviation of 1.73% and 3.94% are obtained at frame rates of 240Hz and 480Hz when V_{th} distribution is ± 0.5 V.

1. Introduction

Remarkable technology advances in active matrix organic light emitting diode (AMOLED) displays have been achieved over the past few years. Samsung Mobile Display has achieved successful mass production of various AMOLED panels ranging in size from 2 inches to 7 inches. Recently, companies have been focusing on development of large-size AMOLED panels [1] and three-dimensional (3D) displays [2]. In general, 3D displays are classified into two types: stereoscopic 3D displays with special glasses and autostereoscopic 3D displays without glasses. The stereoscopic 3D displays using glasses have some advantages, which result in no degradation of resolution and 3D viewing at any angle. To implement 3D images with glasses, left and right images must be showed alternately at a certain time. In this manner, frame rates of 120 Hz or more are required. However, as the frame rate increases, scan time per pixel line decreases, which can create serious problems for proper operation of AMOLED pixel circuits. In particular, compensation for variation of threshold voltage (V_{th}) of low temperature poly silicon thin film transistors (LTPS TFTs) will not work if time is too short. The problem gets worse in large-sized AMOLED panels as a result of increased rising and falling times due to a large resistive capacitive (RC) load. Although there are some approaches to implement 3D display schemes without increasing frame rates, basically, development of a high-speed pixel circuit is necessary for best quality. Therefore, research and development activities have been investigating operation of panels at high frame rates such as 240Hz. In this paper, we propose a method to implement a 3D AMOLED display using high-speed driving with a practical pixel circuit. The proposed pixel circuit consists of 5 transistors and 2 capacitors. Its input signals are scan (SCAN), emission (EM), and emission bar (EMB). The effect of V_{th} compensation of the pixel circuit is confirmed in simulation results.

2. 3D Display Driving Scheme

Figure 1 shows a comparison of 2D and 3D display driving schemes. Figure 1(a) illustrates a conventional 60Hz 2D display driving scheme. The x-axis indicates time and the y-axis indicates scan lines. At a frame rate of 60Hz, the time for 1 scan line is 16.67 ms. During this time, the AMOLED pixel circuit carries out initialization, V_{th} compensation, data writing, and emission [3-6].

Figure 1(b) shows a 240Hz 3D display driving scheme using shutter glasses. One scan line time for 240 Hz is around 4.17 ms, which is 1/4 of the time compared to that of the 60Hz case. To implement the 3D display, left and black data are written during the first 2 frames, and right and black data are written for the following 2 frames. As described in the figure, the left shutter glass is opened (on) when the left image is emitted and the right shutter glass is on when the right image is emitted. However, it can be difficult to switch the liquid crystal (LC)-based shutter glasses on and off in such a short time because their response time is several milliseconds. This may cause a crosstalk problem which is undesirable in 3D displays. The problem can be solved by reducing the emission duty ratio to meet response time of the shutter glasses. However, reducing the emission time causes a loss of luminance, so that more current must be driven into the OLED to achieve a given luminance. Higher drive levels are not good for AMOLED displays in terms of life and image sticking. In order to avoid this problem, frame rates of faster than 240 Hz can be used. As an example of faster operation, a 480Hz 3D driving scheme is

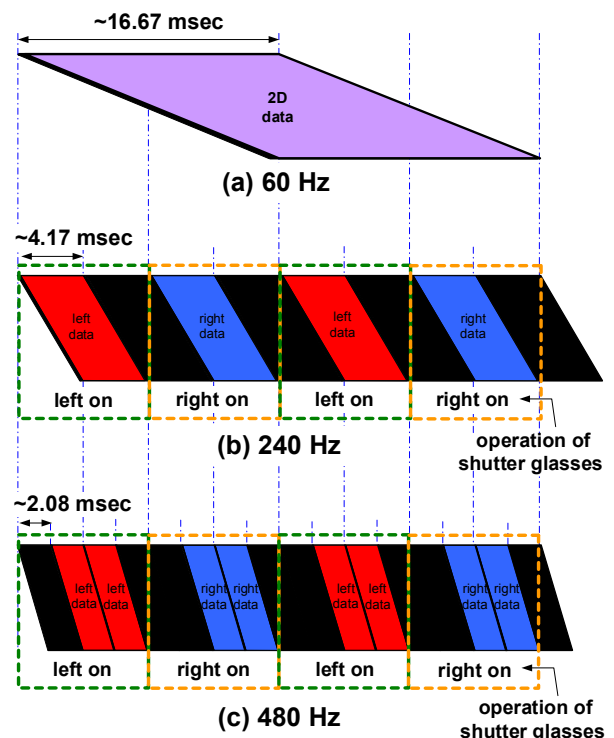


Figure 1. 2D and 3D display driving schemes
(a) Conventional 60Hz 2D driving (b) 240Hz 3D driving
(c) 480Hz 3D driving

described in figure 1(c). In this case, the black emission period has been increased to around 2.08 ms. This means that more on/off timing margin is provided for the shutter glasses in consideration of their response time. Accordingly, crosstalk can be reduced using this scheme.

3. High-Speed Pixel Circuit

3.1. Phenomena at high-speed operation

In order to implement the 240Hz 3D and the 480Hz 3D driving schemes, it is necessary to design a high-speed pixel circuit which is capable of completing V_{th} compensation and data writing in a short time. Usually, V_{th} compensation is accomplished by using a diode connection method. In this method, V_{th} of the driving transistor has to be charged to the transistor's gate node before emission. However, most prior pixel circuits have been designed to have one horizontal line time (1H) for V_{th} charging. Therefore, as frame rates increase, less time is allocated to V_{th} compensation.

Figure 2 shows the pictures of a 14-inch qFHD AMOLED panel at different 1H times. The pixel circuit consists of 6 transistors



(a) 1H = 9.7 μ s



(b) 1H = 0.91 μ s

Figure 2. 14-inch qFHD AMOLED panel driven at different speeds (a) horizontal line time (1H) = 9.7 μ s
(b) horizontal line time (1H) of 0.91 μ s

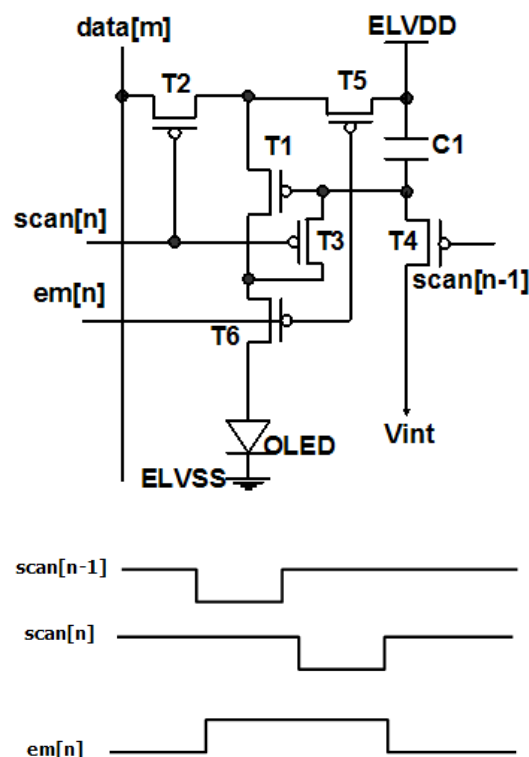


Figure 3. Schematic and timing diagram of 6T-1C AMOLED pixel circuit

and one capacitor as shown in figure 3. When 1H is 9.7 μ s, the image is uniform as shown in fig. 2(a). However, when 1H is 0.91 μ s, image uniformity is lost as shown in fig. 2(b). Specifically, the left and right sides of the image are relatively uniform, but the center of the image shows luminance variation which is known as random mura. The non-uniform image is attributed to the different RC load. Since the scan and emission drivers are integrated into the left and right sides of the panel, the rising and falling times are longer in the central part of the display. As a result, the V_{th} compensation function does not work properly with the shorter V_{th} charging time. The same phenomenon is expected in the conventional 5T-2C pixel circuit [3, 4]. As V_{th} charging time is allocated according to the scan time, image quality will depend on operating speed. In addition, the effect will be more severe for high resolution panels because the 1H time will be shorter.

3.2. Operation of proposed pixel circuit

Figure 4 illustrates the proposed 5-transistor 2-capacitor (5T-2C) pixel circuit and its input signals. The critical point in this circuit design is the input signals. Unlike conventional 5T-2C pixel circuits [3, 4], we use the EMB[n-1] signal to extend the time for V_{th} compensation. Figure 5 shows a timing diagram for the input signals. The operation period is divided into 4 steps: initializing, V_{th} charging, data writing, and emission. A detailed description of the working mechanism is given next.

The first step in the new scheme is initialization, which occurs by turning on the driving transistor (T1). When both of the EM[n]

and EMB[n-1] signals are low, the switching transistors T2 and T5 turn on. Consequently, the T1 transistor turns on regardless of previous data because the gate voltage of T1 is changed to a value less than ELVDD- V_{th} .

The next operation is V_{th} charging, which is a key step for compensation of V_{th} distribution. In this step, only the EMB[n-1] signal is low such that T2 and T4 are turned on while other transistors are turned off. Through T1 and T2, the gate node of T1 is charged to ELVDD- V_{th} as a result of the diode connection of T1. Here, the stored V_{th} voltage level is highly dependent on the timing for charging. For full high definition (FHD) resolution, 1 horizontal line time (1H) for 240 Hz and 480 Hz is around 3.7 μ s and 1.85 μ s, respectively. Because of this short time for V_{th} charging, use of a conventional scheme makes it difficult to save the full level of V_{th} . However, in the proposed driving scheme, it is possible to secure complete V_{th} charging thanks to the controllable length of the EMB signal. In other words, by separating the V_{th} charging period from scan timing, V_{th} compensation can be achieved regardless of frame rates.

The third step is data writing. In this step, the switching transistor T3 turns on so that the data voltage is stored to the gate node of T1 by boosting operation through C_{vth} . The speed of data writing is relatively faster than V_{th} charging due to the nature of boosting. Finally, the OLED emits when EM[n] signal is low. The emission

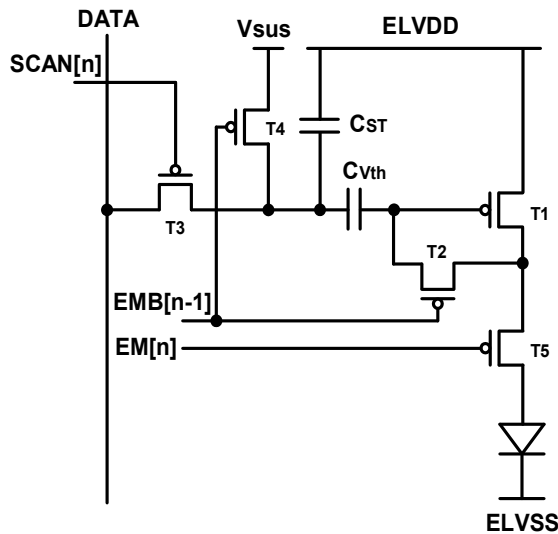


Figure 4. Schematic of 5T-2C AMOLED pixel circuit for high-speed operation

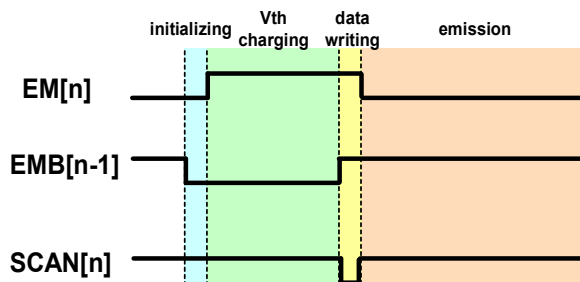


Figure 5. Timing diagram of input signals

current is determined by the equation that follows:

$$\begin{aligned} I_d &= \frac{1}{2} \mu \cdot C_{ox} \frac{W}{L} (V_{sg} - |V_{th}|)^2 \\ &= \frac{1}{2} \mu \cdot C_{ox} \frac{W}{L} (ELVDD - (ELVDD - |V_{th}| + Vdata - Vsus) - |V_{th}|)^2 \\ &= \frac{1}{2} \mu \cdot C_{ox} \frac{W}{L} (Vsus - Vdata)^2 \end{aligned}$$

As a result of complete V_{th} charging and data writing, the V_{th} term in the equation is eliminated so that the final current is proportional to square of (Vsus-Vdata).

3.3. Simulation results

Figure 6 illustrates the simulation result of the proposed driving scheme when frame rates are 480 Hz. The data shows gate voltage of the driving transistor for each operating step. In this simulation, it is assumed that the transistor has V_{th} distribution of ± 0.25 V and ± 0.5 V. The result shows proper circuit operation at each step. Notably, the stored V_{th} distribution of ± 0.49 V results in appropriate V_{th} compensation due to the fact that there is adequate time for V_{th} charging.

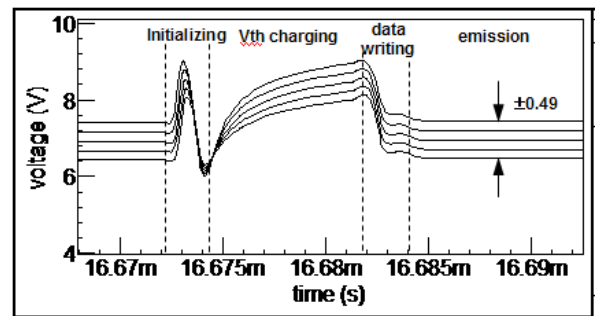


Figure 6. Gate voltage of driving transistor for proposed 480 Hz driving

Table 1 shows a comparison of current deviation between a conventional driving scheme and the proposed driving scheme for frame rates of 240 Hz and 480 Hz. The same RC load is applied for both driving schemes. To compare the effect of V_{th} charging time, it is assumed that both schemes have no problem with initialization. Using the proposed approach, current deviation of 1.73% and 3.94% are obtained for 240 Hz and 480 Hz. On the other hand, current deviation of 8.18% and 16.47% were obtained using the conventional scheme. According to these results, it is clear that the proposed method is better able to compensate for V_{th} variation.

Table 1. Comparison of current deviation between conventional scheme and proposed scheme

	240 Hz	480 Hz
conventional scheme	8.18 %	16.47 %
proposed scheme	1.73 %	3.94 %

In summary, the proposed scheme makes it possible to operate the pixel circuit at high frame rates because the time provided for V_{th} charging is independent of scan time. In addition this high-speed operation is beneficial for 2D image characteristics. When the frame rates are increased, liquid crystal displays show better MPRT, or moving picture response time. Similarly, when driven at higher frame rates, AMOLEDs will achieve better moving picture perceptual resolution (MPPR), where MPPR is a new measurement method for moving image quality [7].

4. Conclusions

An AMOLED pixel circuit and driving scheme are proposed for operation at high frame rates. The proposed driving scheme ensures sufficient time for V_{th} compensation using controllable input signals. A 3D AMOLED display can be achieved using this driving scheme because it is possible to operate the pixel circuit at frame rates of 240Hz or higher. In the 480Hz system, crosstalk between left and right images can be reduced. In addition, high-speed circuit operation results in improved MPPR.

5. References

- [1] M.H. Lee, S.M. Seop, J.S. Kim, J.H. Hwang, H.J. Shin, S.K. Cho, K.W. Min, W.G. Kwak, S.I. Jung, C.S. Kim, W. S. Choi, S. C. Kim, E. J. Yoo, SID Symposium Digest **40**, p. 802 (2009).
- [2] B.-W. Lee, I.-H. Ji, S.-D. Sung, S. Han, K.-S. Shin, B. H Kim, and S. S. Kim, Novel Simultaneous Emission Driving Scheme for Crosstalk-free 3-D AMOLED TV, SID Symposium Digest **41** (these proceedings) (2010).
- [3] R. Dawson, Z. Shen, D.A. Furst, S. Connor, J. Hsu, M.G. Kane, R.G. Stewart, A. Ipri, C.N. King, P.J. Green, R.T. Flegal, S. Pearson, W.A. Barrow, E. Dickey, K. Ping, S. Robinson, C.W. Tang, S. Vanslyke, F. Chen, J. Shi, J.C. Sturm and M.H. Lu, IEDM Tech. Digest **1008**, pp.875-878 (1998).
- [4] N. Komiya, C. Y. Oh, K. M. Eom, J. T. Jeong, H. K. Chung, S. M. Choi, and O. K. Kwon, IDW '03 Tech. Dig., (2003).
- [5] S. M. Choi, O. K. Kwon and H. K. Chung, SID Symposium Digest **35**, pp. 260-263 (2004).
- [6] S.M. Choi, O.K. Kwon, N. Komiya and H.K. Chung, IDW '03 Digest, pp. 535-538 (2003).
- [7] J. Chong, S. Kim, D. Choi, H. Park, S. Lee, J. Bae, H. Lee, S. Kim, Method to Measure Perceptual Resolution of Moving Picture Display, SID Symposium Digest **41** (these proceedings) (2010).