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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	D0480-P13288US01
	Application Number	
Title of Invention	DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Avinash	N.	Ananthakrishnan	

Residence Information (Select One) ● US Residency ○ Non US Residency ○ Active US Military Service

City	Hillsboro	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	2900 NW Adagio Way
Address 2	

City	Hillsboro	State/Province	OR
Postal Code	97124	Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Efraim		Rotem	

Residence Information (Select One) ○ US Residency ● Non US Residency ○ Active US Military Service

City	Haifa	Country of Residence	IL

Mailing Address of Inventor:

Address 1	3 Vizo Street
Address 2	

City	Haifa	State/Province	
Postal Code	34400	Country	IL

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Doron		Rajwan	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	D0480-P13288US01
	Application Number	
Title of Invention	DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR	

Residence Information (Select One) ○ US Residency ◉ Non US Residency Active US Military Service

City	Rishon Le-Zion	Country of Residence [i]	IL

Mailing Address of Inventor:

Address 1	13 Odem Street		
Address 2			
City	Rishon Le-Zion	State/Province	
Postal Code	00000	Country [i]	IL

Inventor 4 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Eliezer		Weissmann	

Residence Information (Select One) ○ US Residency ◉ Non US Residency Active US Military Service

City	Haifa	Country of Residence [i]	IL

Mailing Address of Inventor:

Address 1	Albert Switcher 10		
Address 2			
City	Haifa	State/Province	IL
Postal Code	34995	Country [i]	

Inventor 5 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Nadav		Shulman	

Residence Information (Select One) ○ US Residency ◉ Non US Residency Active US Military Service

City	Tel Mond	Country of Residence [i]	IL

Mailing Address of Inventor:

Address 1	Hasayfan, 19 Street, POB 447		
Address 2			
City	Tel Mond	State/Province	
Postal Code	40600	Country [i]	IL

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	D0480-P13288US01
	Application Number	
Title of Invention	DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR	

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	164		
Email Address	usPatDocket@kinney.com	Add Email	Remove Email

Application Information:

Title of the Invention	DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR		
Attorney Docket Number	D0480-P13288US01	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	8	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	D0480-P13288US01
	Application Number	
Title of Invention	DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR	

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	164		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status: Patented — Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13225677	Continuation of	14143939	2013-12-30	9081557	2015-07-14

Prior Application Status: Patented — Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13225677	Continuation of	13780066	2013-02-28	8775833	2014-07-08

Prior Application Status: Expired — Remove

Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
13225677	Continuation of	PCT/US12/53726	2012-09-05

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. — Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. — Add

PTO/AIA/14 (01-22)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	D0480-P13288US01
	Application Number	
Title of Invention	DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR	

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	D0480-P13288US01
	Application Number	
Title of Invention	DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	D0480-P13288US01
	Application Number	
Title of Invention	DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 — Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Daedalus Prime LLC		
Mailing Address Information For Applicant:			
Address 1	75 South Riverside Avenue		
Address 2			
City	Unit B	**State/Province**	NY
Country	US	Postal Code	10520
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (01-22)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	D0480-P13288US01
	Application Number	
Title of Invention	DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Remove

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Ian D. MacKinnon/			Date (YYYY-MM-DD)	2023-11-06
First Name	Ian D.	Last Name	MacKinnon	Registration Number	34,660

Additional Signature may be generated within this form by selecting the Add button. Add

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Approved for use through 05/31/2024. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	D0480-P13288US01
	Application Number	
Title of Invention	DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	48802269
Application Number:	13225677
International Application Number:	
Confirmation Number:	2063
Title of Invention:	DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Customer Number:	164
Filer:	Ian David MacKinnon
Filer Authorized By:	
Attorney Docket Number:	D0480-P13288US01
Receipt Date:	06-NOV-2023
Filing Date:	06-SEP-2011
Time Stamp:	17:49:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	2023-11-06_SADS_D0480-P13288US01.pdf	2226712 49169654ba48c0ebfe90e4f13f19de2a4fd2ce4a	no	10

Warnings:

Information:	
Total Files Size (in bytes):	2226712

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/225,677	09/06/2011	Avinash N. Ananthakrishnan	D0480-P13288US01

CONFIRMATION NO. 2063

164
KINNEY & LANGE, P.A.
333 S. 7TH ST., SUITE 2700
MINNEAPOLIS, MN 55402-2438

POA ACCEPTANCE LETTER

OC000000063308359

Date Mailed: 10/17/2023

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/03/2023.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/byemane/

MediaTek Exhibit 1002, Page 13 of 398

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/225,677	09/06/2011	Avinash N. Ananthakrishnan	ITL.2495US (P38410)

CONFIRMATION NO. 2063

47795
TROP, PRUNER & HU, P.C.
PO Box 41790
HOUSTON, TX 77241

POWER OF ATTORNEY NOTICE

OC000000063308326

Date Mailed: 10/17/2023

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/03/2023.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/byemane/

MediaTek Exhibit 1002, Page 14 of 398

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	13/225,677
Filing Date	September 6, 2011
First Named Inventor	Avinash N. Ananthakrishnan
Title	DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR
Art Unit	2116
Examiner Name	Stefan Stoynov
Attorney Docket Number	D0480-P13288US01

SIGNATURE of Applicant or Patent Practitioner

Signature	/Ian D. MacKinnon/	Date (Optional)	October 3, 2023
Name	Ian D. MacKinnon	Registration Number	34,660
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 164

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Daedalus Prime LLC

☐ Inventor or Joint Inventor (title not required below)
☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)
☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)
☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	Ed Gomez	Date (Optional)	
Name	Ed Gomez		
Title	Managing Principal		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Daedalus Prime LLC

Application No./Patent No.: 8769316 Filed/Issue Date: July 1, 2014

Titled: DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR

Daedalus Prime LLC, a Limited liability company

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: AVINASH N. ANANTHAKRISHNAN, et al. To: INTEL CORPORATION

   The document was recorded in the United States Patent and Trademark Office at

   Reel 026863, Frame 0663, or for which a copy thereof is attached.

2. From: INTEL CORPORATION To: DAEDALUS PRIME LLC

   The document was recorded in the United States Patent and Trademark Office at

   Reel 060392, Frame 0594, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Ian D. MacKinnon/	October 3, 2023
Signature	Date
Ian D. MacKinnon	34,660
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	48671988
Application Number:	13225677
International Application Number:	
Confirmation Number:	2063
Title of Invention:	DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Customer Number:	47795
Filer:	Ian David MacKinnon
Filer Authorized By:	
Attorney Docket Number:	ITL.2495US (P38410)
Receipt Date:	03-OCT-2023
Filing Date:	06-SEP-2011
Time Stamp:	13:47:12
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	2023-10-03_POA_D0480-P13288US01.pdf	322177 6f26a426548630acc7c10955a1b885844b05b8e8	no	2
Warnings:					

Information:					
2	Assignee showing of ownership per 37 CFR 3.73	2023-10-03_3-73_D0480-P13288US01.pdf	120211 3aeaa4e0bc4e53dd85ca3a5f0890bde5a3c55833	no	3
Warnings:					
Information:					
			Total Files Size (in bytes):	442388	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/225,677	07/01/2014	8769316	ITL.2495US (P38410)	2063

47795 7590 06/11/2014

TROP, PRUNER & HU, P.C.
1616 S. VOSS RD., SUITE 750
HOUSTON, TX 77057-2631

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 297 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Avinash N. Ananthakrishnan, Hillsboro, OR;
Efraim Rotem, Haifa, ISRAEL;
Doron Rajwan, Rishon Le-Zion, ISRAEL;
Eliezer Weissmann, Haifa, ISRAEL;
Nadav Shulman, Tel Mond, ISRAEL;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99) Change(s) applied to document, /R.T.H./ 3/25/2014	Application Number	13225677
	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

	3	20070234083		2007-10-04	Lee	
	4	20110022865		2011-01-27	Gunther, et al.	
	5	20080005603		2008-01-03	~~Deep, et al.~~ Buch et al.	
	6	20090070605		2009-03-12	Nijhawan, et al.	
	7	20110072429		2011-03-24	Celeskey, et al.	
	8	20050046400		2005-03-03	Rotem	
	9	20090271646		2009-10-29	Talwar, et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	~~1~~	~~KR 10-2006-012846~~	~~KR~~		~~2006-12-14~~	~~LG Electronics Inc.~~		☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

EFS Web 2.1.17 ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.S./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13225677
	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

	9	5931950		1999-08-03	Hsu	
	10	7454632		2008-11-18	Kardach, et al.	
	11	5522087		1996-05-28	Hsiang	
	12	7272730		2007-09-18	Acquaviva, et al.	
	13	7529956		2009-05-05	Stufflebeam	
	14	7730340		2010-06-01	Hu, et al.	
	15	7539885		2009-05-26	Ma	
	16	6748546		2004-06-08	Mirov, et al.	
	17	6829713		2004-12-07	Cooper, et al.	
Change(s) applied to document, /R.T.H./ 3/25/2014	18	7,111,179 ~~71111179~~		2006-09-19	Girson, et al.	
	19	6823516		2004-11-23	Cooper	

EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.S./

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/225,677	09/06/2011	Avinash N. Ananthakrishnan	ITL.2495US (P38410)	2063

7590 05/20/2014

TROP, PRUNER & HU, P.C.
1616 S. VOSS RD., SUITE 750
HOUSTON, TX 77057-2631

EXAMINER	
STOYNOV, STEFAN	

ART UNIT	PAPER NUMBER
2116	

MAIL DATE	DELIVERY MODE
05/20/2014	PAPER

NOTICE OF NON-COMPLIANT INFORMATION DISCLOSURE STATEMENT

An Information Disclosure Statement (IDS) filed 4/29/14 in the above-identified application fails to meet the requirements of 37 CFR 1.97(d) for the reason(s) specified below. Accordingly, the IDS will be placed in the file, but the information referred to therein has not been considered.

The IDS is not compliant with 37 CFR 1.97(d) because:

☑ The IDS lacks a statement as specified in 37 CFR 1.97(e).

☐ The IDS lacks the fee set forth in 37 CFR 1.17(p).

☐ The IDS was filed after the issue fee was paid. Applicant may wish to consider filing a petition to withdraw the application from issue under 37 CFR 1.313(c) to have the IDS considered. See MPEP 1308.

For 571-272-4200 or 1-888-786-0101
Application Assistance Unit
Office of Data Management

FORM PTOM327-B (Rev. 02/08)

MediaTek Exhibit 1002, Page 25 of 398

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

47795 7590 02/20/2014
TROP, PRUNER & HU, P.C.
1616 S. VOSS RD., SUITE 750
HOUSTON, TX 77057-2631

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/225,677	09/06/2011	Avinash N. Ananthakrishnan	ITL.2495US (P38410)	2063

TITLE OF INVENTION: DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	05/20/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
STOYNOV, STEFAN	2116	713-300000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☒ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Trop, Pruner & Hu, P.C.
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Intel Corporation

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Santa Clara, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☒ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 20-1504 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ Applicant certifying micro entity status. See 37 CFR 1.29
NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
☐ Applicant asserting small entity status. See 37 CFR 1.27
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
☐ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date 5/16/14

Typed or printed name Mark J. Rozman Registration No. 42,117

PTOL-85 Part B (10-13) Approved for use through 10/31/2013 OMB 0651-0033 U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

MediaTek Exhibit 1002, Page 26 of 398

PTO/SB/47 (03-09)
Approved for use through 05/31/2015. OMB 0651-0016
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

- OR -

Fax to:
571-273-6500

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below**: If you have a Customer Number to represent the fee address. **When to check the second box below**: If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:

☑ Customer Number: 00197

OR

☐ The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
	13/225,677

Completed by (check one):

☐ Applicant/Inventor

/Mark J. Rozman/
Signature

☑ Attorney or Agent of record 42,117 (Reg. No.)

Mark J. Rozman
Typed or printed name

☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

512-418-9944
Requester's telephone number

☐ Assignee recorded at Reel _____ Frame_____

May 16, 2014
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more that one signature is required, see below*.

☑ * Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1. 11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313- 1450. DO NOT SEND COMPLETED FORMS TO THIS ADDRESS.
SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974** (**P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal	
Application Number:	13225677
Filing Date:	06-Sep-2011
Title of Invention:	DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Filer:	Mark J. Rozman/Stephanie Petreas
Attorney Docket Number:	ITL.2495US (P38410)
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
		Total in USD ($)		**960**

Electronic Acknowledgement Receipt	
EFS ID:	19052214
Application Number:	13225677
International Application Number:	
Confirmation Number:	2063
Title of Invention:	DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Customer Number:	47795
Filer:	Mark J. Rozman/Stephanie Petreas
Filer Authorized By:	Mark J. Rozman
Attorney Docket Number:	ITL.2495US (P38410)
Receipt Date:	16-MAY-2014
Filing Date:	06-SEP-2011
Time Stamp:	14:48:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$960
RAM confirmation Number	1103
Deposit Account	201504
Authorized User	ROZMAN, MARK J.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees) Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	ITL2495USIssueFeeTrans.pdf	183401 520db0641bac67ff525063ce936f67b7f955ac1a	no	1
Warnings:					
Information:					
2	Miscellaneous Incoming Letter	ITL2495USFeeAddress.pdf	204633 82a0cb49c764eab66ee5df4b8235e36614a0ed59	no	2
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30897 7c692f0f9f805e4c0b9aa1b971c8af45c1ac02a5	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	418931		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13225667
	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan
	Art Unit	2116
	Examiner Name	Stefan Stoynov
	Attorney Docket Number	ITL.2495US (P38410)

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐
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NON-PATENT LITERATURE DOCUMENTS			Remove
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13225667
	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan
	Art Unit	2116
	Examiner Name	Stefan Stoynov
	Attorney Docket Number	ITL.2495US (P38410)

	1	U.S. Patent Application Serial No. 14/143,939, filed December 30, 2013, entitled, "Dynamically Allocating A Power Budget Over Multiple Domains Of A Processor," by Avinash N. Ananthakrishnan.	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13225667
	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan
	Art Unit	2116
	Examiner Name	Stefan Stoynov
	Attorney Docket Number	ITL.2495US (P38410)

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Mark J. Rozman/	Date (YYYY-MM-DD)	2014-04-29
Name/Print	Mark J. Rozman	Registration Number	42,117

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal	
Application Number:	13225677
Filing Date:	06-Sep-2011
Title of Invention:	DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Filer:	Mark J. Rozman/Stephanie Petreas
Attorney Docket Number:	ITL.2495US (P38410)
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt	
EFS ID:	18891850
Application Number:	13225677
International Application Number:	
Confirmation Number:	2063
Title of Invention:	DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Customer Number:	47795
Filer:	Mark J. Rozman/Stephanie Petreas
Filer Authorized By:	Mark J. Rozman
Attorney Docket Number:	ITL.2495US (P38410)
Receipt Date:	29-APR-2014
Filing Date:	06-SEP-2011
Time Stamp:	15:30:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$180
RAM confirmation Number	2174
Deposit Account	201504
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees) Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	ITL2495USIDS.pdf	612150 455f947a79bab436596d51a620a34bff40b93f2e	no	4
Warnings:					
Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
2	Non Patent Literature	NPLDOcITL2495C2App.pdf	112934 652699e1cfbbab16fa142515cde92d4fb0f85e7a	no	23
Warnings:					
Information:					
3	Non Patent Literature	NPLDOcITL2495C2Xings.pdf	69100 486ace572cc677ee31fbbc9e2ec88ad635df50ef	no	8
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	31062 8f280c0fec23445e05c6aa9fa15e6cb007f8a81f	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	825246		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

47795 7590 02/20/2014

TROP, PRUNER & HU, P.C.
1616 S. VOSS RD., SUITE 750
HOUSTON, TX 77057-2631

EXAMINER	
STOYNOV, STEFAN	
ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 02/20/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/225,677	09/06/2011	Avinash N. Ananthakrishnan	ITL.2495US (P38410)	2063

TITLE OF INVENTION: DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	05/20/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

MediaTek Exhibit 1002, Page 41 of 398

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

47795 7590 02/20/2014
TROP, PRUNER & HU, P.C.
1616 S. VOSS RD., SUITE 750
HOUSTON, TX 77057-2631

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/225,677	09/06/2011	Avinash N. Ananthakrishnan	ITL.2495US (P38410)	2063

TITLE OF INVENTION: DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	05/20/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
STOYNOV, STEFAN	2116	713-300000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

MediaTek Exhibit 1002, Page 42 of 398

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/225,677	09/06/2011	Avinash N. Ananthakrishnan	ITL.2495US (P38410)	2063

47795 7590 02/20/2014

TROP, PRUNER & HU, P.C.
1616 S. VOSS RD., SUITE 750
HOUSTON, TX 77057-2631

EXAMINER	
STOYNOV, STEFAN	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 02/20/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 361 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 361 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/225,677	Applicant(s) ANANTHAKRISHNAN ET AL.	
	Examiner STEFAN STOYNOV	Art Unit 2116	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *communication filed on 02/07/2014*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-7, 9-12, 14, 15, and 17-20 (renumbered as claims 1-17)*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has **THREE MONTHS FROM THE "MAILING DATE"** of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date See Continuation Sheet
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☒ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/STEFAN STOYNOV/
Primary Examiner, Art Unit 2116

Continuation of Attachment(s) 2. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date: 11/20/13, 11/22/13, 2/7/14, and 2/18/14.

MediaTek Exhibit 1002, Page 46 of 398

The present application is being examined under the pre-AIA first to invent provisions.

EXAMINER'S COMMENT

Terminal Disclaimer

The terminal disclaimer filed on 02/07/2014 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of any patent granted on Application Number 13/780,066 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Accordingly, the nonstatutory, obviousness-type double patenting rejection for claims 1-20 against Application Number 13/780,066 has been withdrawn.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEFAN STOYNOV whose telephone number is (571)272-4236. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/STEFAN STOYNOV/
Primary Examiner, Art Unit 2116

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13225677
	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2116
	Examiner Name	Stefan Stoynov
	Attorney Docket Number	ITL.2495US (P38410)

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7603577		2009-10-13	Yamaji, et al.	
If you wish to add additional U.S. Patent citation information please click the Add button.						

U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20120096288		2012-04-19	Bates, et al.	
If you wish to add additional U.S. Published Application citation information please click the Add button.						

FOREIGN PATENT DOCUMENTS								
Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐
If you wish to add additional Foreign Patent Document citation information please click the Add button								

NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.S./

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	Art Unit	2116
	Examiner Name	Stefan Stoynov
	Attorney Docket Number	ITL.2495US (P38410)

	1		☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature	/Stefan Stoynov/ (02/19/2014)	Date Considered	02/19/2014

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.S./

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

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	Examiner Name	Stefan Stoynov
	Attorney Docket Number	ITL.2495US (P38410)

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐
If you wish to add additional Foreign Patent Document citation information please click the Add button								Add

NON-PATENT LITERATURE DOCUMENTS			Remove
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.S./

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	Art Unit	2116
	Examiner Name	Stefan Stoynov
	Attorney Docket Number	ITL.2495US (P38410)

	1	INTEL DEVELOPER FORUM, IDF2010, Opher Kahn, et al., "Intel Next Generation Microarchitecture Codename Sandy Bridge: New Processor Innovations," September 13, 2010, 58 pages.	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/Stefan Stoynov/ (02/19/2014)	Date Considered	02/19/2014

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.S./

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5287292		1994-02-15	Kenny, et al.	
If you wish to add additional U.S. Patent citation information please click the Add button.						
U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20050288886		2005-12-29	Therien, et al.	
	2	20070106428		2007-05-10	Omizo, et al.	
	3	20080077282		2008-03-27	Hartman, et al.	
	4	20040030940		2004-02-12	Espinoza-Ibarra, et al.	
	5	20120114010		2012-05-10	Branch	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.S./

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	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

	6	20070260895		2007-11-08	Aguilar, et al.	
	7	20060041766		2006-02-23	Adachi	

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		☐

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EXAMINER SIGNATURE

Examiner Signature	/Stefan Stoynov/ (02/19/2014)	Date Considered	02/19/2014

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.S./

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3577	((plural$3 or multi$3 or several or (more adj2 one) or different or separate or individual or first or second) adj domain$1) same (processor or microprocessor or cpu or core)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 17:07
L2	1971	((plural$3 or multi$3 or several or (more adj2 one) or different or separate or individual or first or second) adj domain$1) with (processor or microprocessor or cpu or core)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 17:08
L3	7	1 same ((allocat$4 or reallocat$4 or (re adj allocat$4) or assign$5 or reassign$5 or (re adj assign$5) or distribut$4 or redistribut$4 or (re adj distribut$4)) same ((power or energy) near2 (budget or consumption)) same (dynamic$4 or adaptive$2 or runtime or (run adj time)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 17:14
L4	3	2 with ((allocat$4 or reallocat$4 or (re adj allocat$4) or assign$5 or reassign$5 or (re adj assign$5) or distribut$4 or redistribut$4 or (re adj distribut$4)) with ((power or energy) near2 (budget or consumption)) with (dynamic$4 or adaptive$2 or runtime or (run adj time)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 17:14
L5	2	3 same (workload or (work adj load))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 17:16
L6	1	4 with (workload or (work adj load))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 17:16
L7	71	((power or energy) adj (control$4 or manag$5)) same ((plural$3 or multi$3 or several or (more adj2 one) or different or separate or individual or first or second) adj domain$1) same (processor or microprocessor or cpu or core)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 17:19
L8	18	((power or energy) adj (control$4 or manag$5)) with ((plural$3 or multi$3 or several or (more adj2 one) or different or separate or individual or first or second) adj domain$1) with (processor or microprocessor or cpu or core)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 17:20
L9	3	7 same ((allocat$4 or reallocat$4 or (re adj allocat$4) or assign$5 or reassign$5 or (re adj assign$5) or distribut$4 or redistribut$4 or (re adj distribut$4)) same	US-PGPUB; USPAT; EPO; JPO; DERWENT;	OR	OFF	2014/02/18 17:20

		((power or energy) near2 (budget or consumption)))	IBM_TDB			
L10	1	8 with ((allocat$4 or reallocat$4 or (re adj allocat$4) or assign$5 or reassign$5 or (re adj assign$5) or distribut$4 or redistribut$4 or (re adj distribut$4)) with ((power or energy) near2 (budget or consumption)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 17:20
L11	0	9 same (shar$3 near2 polic$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 17:23
L12	2	9 and (shar$3 near2 polic$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 17:23
L13	0	10 and (shar$3 near2 polic$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 17:23
L14	3	7 same ((allocat$4 or reallocat$4 or (re adj allocat$4) or assign$5 or reassign$5 or (re adj assign$5) or distribut$4 or redistribut$4 or (re adj distribut$4)) same ((power or energy) near2 (budget or consumption)) same (minim$2 or least or smallest))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 17:25
L15	1	8 with ((allocat$4 or reallocat$4 or (re adj allocat$4) or assign$5 or reassign$5 or (re adj assign$5) or distribut$4 or redistribut$4 or (re adj distribut$4)) with ((power or energy) near2 (budget or consumption)) with (minim$2 or least or smallest))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 17:25
L16	2	14 same (reservation near2 value$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 17:27
L17	0	15 with (reservation near2 value$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 17:27
L18	53	((plural$3 or multi$3 or several or (more adj2 one) or different or separate or individual or first or second) adj core$1) same (processor or microprocessor) same ((plural$3 or multi$3 or several or (more adj2 one) or different or separate or individual or first or second) adj domain$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 17:29
L19	17	((plural$3 or multi$3 or several or (more adj2 one) or different or separate or individual or first or second) adj core$1) with (processor or microprocessor) with ((plural$3 or multi$3 or several or (more	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 17:29

		adj2 one) or different or separate or individual or first or second) adj domain$1)				
L20	2	18 same ((power or energy) near2 shar$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 17:30
L21	1	19 with ((power or energy) near2 shar$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 17:30
L22	1	20 same ((allocat$4 or reallocat$4 or (re adj allocat$4) or assign$5 or reassign$5 or (re adj assign$5) or distribut$4 or redistribut$4 or (re adj distribut$4)) same ((power or energy) near2 (budget or consumption) near2 (variable or changeable or adjustable or adaptable or alterable)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 17:34
L23	1	21 with ((allocat$4 or reallocat$4 or (re adj allocat$4) or assign$5 or reassign$5 or (re adj assign$5) or distribut$4 or redistribut$4 or (re adj distribut$4)) same ((power or energy) near2 (budget or consumption) near2 (variable or changeable or adjustable or adaptable or alterable)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 17:34
L27	13	("20120096288" | "7603577").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 18:12
L28	17	("20040030940" | "20050288886" | "20060041766" | "20070106428" | "20070230895" | "20080077282" | "20120114010" | "5287292").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 18:12
L29	28	("20050046400" | "20050223258" | "20080028778" | "20080077813" | "20090235108" | "20090271141" | "20110283124" | "20120053897" | "20120066535" | "20120110352" | "20120173907" | "20130179704" | "20130246825" | "7146514").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 18:13
L30	2	(27 or 28 or 29) and 3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 18:13
L31	2	(27 or 28 or 29) and 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 18:13
L32	1	(27 or 28 or 29) and 7	US-PGPUB; USPAT; EPO; JPO; DERWENT;	OR	OFF	2014/02/18 18:14

			IBM_TDB			
L33	1	(27 or 28 or 29) and 8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 18:14
L34	1	(27 or 28 or 29) and 18	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 18:14
L35	1	(27 or 28 or 29) and 19	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/02/18 18:14

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L24	2	(((plural$3 or multi$3) adj domain$1 adj (processor or microprocessor or cpu or core)) and ((plural$3 or multi$3 or several or (more adj2 one) or different or separate or individual or first or second) adj domain$1) and (allocat$4 or reallocat$4 or (re adj allocat$4) or assign$5 or reassign$5 or (re adj assign$5) or distribut$4 or redistribut$4 or (re adj distribut$4)) and ((power or energy) adj (budget or consumption)) and (dynamic$4 or adaptive$2 or runtime or (run adj time)) and ((first or second or plural$3 or multi$3 or different or (more adj2 one)) adj (workload$1 or (work adj load$1)))).clm.	US-PGPUB; USPAT; UPAD	OR	OFF	2014/02/18 17:41
L25	2	(((plural$3 or multi$3) adj domain$1 adj (processor or microprocessor or cpu or core)) and ((plural$3 or multi$3 or several or (more adj2 one) or different or separate or individual or first or second) adj domain$1) and (allocat$4 or reallocat$4 or (re adj allocat$4) or assign$5 or reassign$5 or (re adj assign$5) or distribut$4 or redistribut$4 or (re adj distribut$4)) and ((power or energy) adj (budget or consumption)) and (shar$3 adj polic$3) and ((minim$2 or least or smallest) adj reservation adj value$1) and ((control$4 or manag$5 or adjust$5 or regulat$4 or correct$4 or modif$8 or chang$3 or alter$3 or vary$3) near2 (clock$1 or frequenc$3))).clm.	US-PGPUB; USPAT; UPAD	OR	OFF	2014/02/18 17:45
L26	2	(((((plural$3 or multi$3 or several or (more adj2 one) or different or separate or individual or first or second) adj core$1) or multicore) adj (processor or microprocessor or cpu)) and ((plural$3 or multi$3 or several or (more adj2 one) or different or separate or individual or first or second) adj domain$1) and ((fixed or set or permanent or preset) adj (power or energy) adj (budget or consumption)) and (allocat$4 or reallocat$4 or (re adj allocat$4) or assign$5 or reassign$5 or (re adj assign$5) or distribut$4 or redistribut$4 or (re adj	US-PGPUB; USPAT; UPAD	OR	OFF	2014/02/18 17:57

		distribut$4)) and ((variable or changeable or adjustable or adaptable or alterable) adj (power or energy) adj (budget or consumption)) and (dynamic$4 or adaptive$2 or runtime or (run adj time)) and (current adj (time or period or interval or duration)) and ((power or energy) adj sharing adj value$1) and ((dynamic adj random adj access adj memory) or DRAM)).clm.				

2/ 18/ 2014 6:15:20 PM
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PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13225677
	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7146514		2006-12-05	Kaushik, et al.	
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20110283124		2011-11-07	Branover, et al.	
	2	20120173907		2012-07-05	Moses, et al.	
	3	20130246825		2013-09-19	Shannon	
	4	20090271141		2009-10-29	Coskun, et al.	
	5	20080028778		2008-02-07	Millet	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.S./

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	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

	6	20120053897		2012-03-01	Naffziger	
	7	20050223258		2005-10-06	Watts	
	8	20050046400		2005-03-03	Rotem	
	9	20120110352		2012-05-03	Branover, et al.	
	10	20090235108		2009-09-17	Gold, et al.	
	11	20120066535		2012-03-15	Naffziger	
	12	20080077813		2008-03-27	Keller, et al.	
	13	20130179704		2013-07-11	Ananthakrishnan	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

NON-PATENT LITERATURE DOCUMENTS			Remove
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EXAMINER SIGNATURE			
Examiner Signature	/Stefan Stoynov/ (02/19/2014)	Date Considered	02/19/2014

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.S./

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13225677	ANANTHAKRISHNAN ET AL.
	Examiner	Art Unit
	STEFAN STOYNOV	2116

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
713	300	11/7/13	SS
345	501	11/7/13	SS
700	286	11/7/13	SS
712	28	11/7/13	SS

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search for USPAT, US-PGPUB, EPO, JPO, DERWENT, IBM_TDB (see attached file).	11/7/13	SS
713/330, 345/501, 700/286, 712/28 text search only for USPAT, US-PGPUB, EPO, JPO, DERWENT, IBM_TDB (see attached file).	11/7/13	SS
Inventor's search.	11/7/13	SS
Updated search (see attached file).	2/19/14	SS
Updated Inventor's search.	2/19/14	SS

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
713	300	2/19/14	SS
	See attached Inteference Search printout.	2/19/14	SS

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13225677	ANANTHAKRISHNAN ET AL.
	Examiner	**Art Unit**
	STEFAN STOYNOV	2116

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	11/07/2013	02/19/2014							
1	1	✓	=							
2	2	✓	=							
3	3	✓	=							
4	4	✓	=							
5	5	✓	=							
6	6	✓	=							
7	7	✓	=							
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	16	✓	-							
14	17	✓	=							
15	18	✓	=							
16	19	✓	=							
17	20	✓	=							

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13225677	ANANTHAKRISHNAN ET AL.
	Examiner	**Art Unit**
	STEFAN STOYNOV	2116

CPC		
Symbol	**Type**	**Version**
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CPC Combination Sets				
Symbol	**Type**	**Set**	**Ranking**	**Version**
/				
/				

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	17	
/STEFAN STOYNOV/ Primary Examiner.Art Unit 2116	02/19/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13225677	ANANTHAKRISHNAN ET AL.
	Examiner	**Art Unit**
	STEFAN STOYNOV	2116

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION														
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED									
713	300	G	0	6	F	1 / 00 (2006.01.01)										
CROSS REFERENCE(S)		G	0	6	F	15 / 00 (2006.01.01)										
		G	0	5	D	3 / 12 (2006.01.01)										
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)	G	0	6	F	15 / 00 (2006.01.01)										
345	501															
700	286															
712	28															

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	17	
/STEFAN STOYNOV/ Primary Examiner.Art Unit 2116	02/19/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13225677	ANANTHAKRISHNAN ET AL.
	Examiner	**Art Unit**
	STEFAN STOYNOV	2116

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	20												
2	2														
3	3														
4	4														
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9	10														
10	11														
11	12														
12	14														
13	15														
14	17														
15	18														
16	19														

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	17	
/STEFAN STOYNOV/ Primary Examiner.Art Unit 2116	02/19/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6

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BIB DATA SHEET

CONFIRMATION NO. 2063

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/225,677	09/06/2011	713	2116	ITL.2495US (P38410)

APPLICANTS

INVENTORS

Avinash N. Ananthakrishnan, Hillsboro, OR;
Efraim Rotem, Haifa, ISRAEL;
Doron Rajwan, Rishon Le-Zion, ISRAEL;
Eliezer Weissmann, Haifa, ISRAEL;
Nadav Shulman, Tel Mond, ISRAEL;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
09/15/2011

Foreign Priority claimed	☐ Yes ☑ No	☐ Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
35 USC 119(a-d) conditions met	☐ Yes ☑ No					
Verified and Acknowledged	/STEFAN STOYNOV/ Examiner's Signature	/S.S./ Initials	OR	8	~~20~~ 17	3

ADDRESS

TROP, PRUNER & HU, P.C.
1616 S. VOSS RD., SUITE 750
HOUSTON, TX 77057-2631
UNITED STATES

TITLE

Dynamically Allocating A Power Budget Over Multiple Domains Of A Processor

FILING FEE RECEIVED		
1090	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

PTO/SB/08a (01-10)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7146514		2006-12-05	Kaushik, et al.	
If you wish to add additional U.S. Patent citation information please click the Add button.						Add
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20110283124		2011-11-07	Branover, et al.	
	2	20120173907		2012-07-05	Moses, et al.	
	3	20130246825		2013-09-19	Shannon	
	4	20090271141		2009-10-29	Coskun, et al.	
	5	20080028778		2008-02-07	Millet	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13225677
	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

	6	20120053897		2012-03-01	Naffziger	
	7	20050223258		2005-10-06	Watts	
	8	20050046400		2005-03-03	Rotem	
	9	20120110352		2012-05-03	Branover, et al.	
	10	20090235108		2009-09-17	Gold, et al.	
	11	20120066535		2012-03-15	Naffziger	
	12	20080077813		2008-03-27	Keller, et al.	
	13	20130179704		2013-07-11	Ananthakrishnan	

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CERTIFICATION STATEMENT

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☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Mark J. Rozman/	Date (YYYY-MM-DD)	2014-02-18
Name/Print	Mark J. Rozman	Registration Number	42,117

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Electronic Patent Application Fee Transmittal	
Application Number:	13225677
Filing Date:	06-Sep-2011
Title of Invention:	Dynamically Allocating A Power Budget Over Multiple Domains Of A Processor
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Filer:	Mark J. Rozman/Stephanie Petreas
Attorney Docket Number:	ITL.2495US (P38410)
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt	
EFS ID:	18226097
Application Number:	13225677
International Application Number:	
Confirmation Number:	2063
Title of Invention:	Dynamically Allocating A Power Budget Over Multiple Domains Of A Processor
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Customer Number:	47795
Filer:	Mark J. Rozman/Stephanie Petreas
Filer Authorized By:	Mark J. Rozman
Attorney Docket Number:	ITL.2495US (P38410)
Receipt Date:	18-FEB-2014
Filing Date:	06-SEP-2011
Time Stamp:	14:18:10
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$180
RAM confirmation Number	476
Deposit Account	201504
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees) Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	ITL2495USIDS.pdf	612620 aeeda565882f3462e1b9218544198202074d80df	no	5
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30737 46362b659e8652d1329703c233722953315d5e24	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	643357		

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Ananthakrishnan, et al.	§	Group Art Unit:	2116
		§		
Serial No.:	13/225,677	§	Conf. No.:	2063
		§		
		§	Examiner:	Stoynov, Stefan
Filed:	September 6, 2011	§		
		§	Atty. Dkt. No.:	ITL.2495US (P38410)
		§		
For:	DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR	§		

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY TO OFFICE ACTION MAILED NOVEMBER 13, 2013

Sir:

In response to the Office Action mailed November 13, 2013, please amend the above-referenced patent application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims begin on page 3 of this paper.

Remarks/Arguments begin on page 7 of this paper.

Amendments to the Specification:

Please remove the title from the abstract page as amended below:

~~DYNAMICALLY ALLOCATING A POWER BUDGET~~

~~OVER MULTIPLE DOMAINS OF A PROCESSOR~~

Abstract of the Disclosure

In one embodiment, the present invention includes a method for determining a power budget for a multi-domain processor for a current time interval, determining a portion of the power budget to be allocated to first and second domains of the processor, and controlling a frequency of the domains based on the allocated portions. Such determinations and allocations can be dynamically performed during runtime of the processor. Other embodiments are described and claimed.

MediaTek Exhibit 1002, Page 79 of 398

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An apparatus comprising:

a multi-domain processor including a first domain and a second domain, each of the first and second domains to operate at an independent voltage and frequency, the multi-domain processor further including first logic to dynamically allocate a power budget for the multi-domain processor between the first and second domains at run time, wherein the first logic is to dynamically allocate substantially all of the power budget to the first domain for a first workload, and to dynamically allocate substantially all of the power budget to the second domain for a second workload executed after the first workload.

2. (Original) The apparatus of claim 1, wherein the first logic is to dynamically allocate the power budget according to a first sharing policy value for the first domain and a second sharing policy value for the second domain, the first and second sharing policy values controllable by user-level software.

3. (Original) The apparatus of claim 2, wherein the first logic is to determine a portion of the power budget to allocate to the first domain based on the first sharing policy value.

4. (Original) The apparatus of claim 2, wherein the first logic is to dynamically allocate the power budget further according to a first minimum reservation value for the first domain and a second minimum reservation value for the second domain, the first and second minimum reservation values controllable by the user-level software.

5. (Original) The apparatus of claim 4, wherein the first logic is to provide at least a first portion of the power budget to the first domain, the first portion corresponding to the first minimum reservation value.

6. (Original) The apparatus of claim 1, wherein the first logic is to determine the

MediaTek Exhibit 1002, Page 80 of 398

power budget for a current time interval based at least in part on a power budget carried forward from a previous time interval, a power consumed in the previous time interval, and a power budget decay value.

7. (Original) The apparatus of claim 6, wherein the first logic is to determine the power budget according to $E_n = E_{n-1} * alpha + (1-alpha)*(Power\_Limit*deltaT - Energy)$, where:

E_n is the power budget for the current time interval;

E_{n-1} is the power budget carried forward from the previous time interval;

Power_limit is a threshold power level;

deltaT is a length of the time interval;

Energy is the power consumed during the previous time interval; and

alpha is the power budget decay value.

8. (Canceled)

9. (Currently Amended) A method comprising:

determining, in a power controller of a multi-domain processor, a power budget for the multi-domain processor for a current time interval, the multi-domain processor including at least a first domain and a second domain;

determining, in the power controller, a portion of the power budget to be allocated to the first and second domains, including allocating a minimum reservation value to the first domain and a minimum reservation value to the second domain, and sharing a remaining portion of the power budget according to a first sharing policy value for the first domain and a second sharing policy value for the second domain; and

controlling a frequency of the first domain and a frequency of the second domain based on the allocated portions.

10. (Currently Amended) The method of claim 9, wherein determining the portion of the power budget to be allocated to the first and second domains includes allocating the power budget to the second domain and not to the first domain if the power budget is less than [[a]] the minimum reservation value for the second domain.

MediaTek Exhibit 1002, Page 81 of 398

11. (Original) The method of claim 10, further comprising obtaining the minimum reservation value for the second domain from a configuration register written by user-level software.

12. (Currently Amended) The method of claim 10, further comprising allocating the minimum reservation value for the second domain to the second domain, and allocating a remaining portion of the power budget to the first domain when the power budget is greater than the minimum reservation value for the second domain but less than a sum of the minimum reservation value for the second domain and [[a]] the minimum reservation value for the first domain.

13. (Canceled)

14. (Currently Amended) The method claim [[13]] 9, wherein ~~the first sharing policy value is controllable by software executing on the first domain,~~ the first sharing policy value is to be incremented when a request for a higher frequency for the first domain is not granted, and the ~~second sharing policy value is controllable by software executing on the second domain, the~~ second sharing policy value is to be incremented when a request for a higher frequency for the second domain is not granted.

15. (Currently Amended) A system comprising:

a multicore processor having a first domain including a plurality of cores, a second domain including a graphics engine, and a third domain including system agent circuitry, the third domain to operate at a fixed power budget and to dynamically allocate a variable power budget between the first and second domains, wherein the system agent circuitry includes a power sharing logic to determine the variable power budget for a current time interval and to allocate a first portion of the variable power budget to the first domain according to a first power sharing value for the first domain, and to allocate a second portion of the variable power budget to the second domain according to a second power sharing value for the second domain; and

a dynamic random access memory (DRAM) coupled to the multicore processor.

MediaTek Exhibit 1002, Page 82 of 398

16. (Canceled)

17. (Currently Amended) The system of claim [[16]] 15, wherein the power sharing logic is to dynamically allocate substantially all of the variable power budget to the first domain for a first workload, and to dynamically allocate substantially all of the variable power budget to the second domain for a second workload executed after the first workload.

18. (Currently Amended) The system of claim [[16]] 15, wherein the power sharing logic is to increment the first power sharing value when a request for a higher frequency for the first domain is not granted, and to increment the second power sharing value when a request for a higher frequency for the second domain is not granted.

19. (Currently Amended) The system of claim [[16]] 15, wherein the power sharing logic is to further allocate the first portion of the variable power budget according to a first minimum reservation value for the first domain and allocate the second portion of the variable power budget according to a second minimum reservation value for the second domain.

20. (Currently Amended) The system of claim [[16]] 15, wherein the power sharing logic is to further allocate the variable power budget according to a preference value, the preference value to favor the second domain over the first domain.

REMARKS/ARGUMENTS

Provided herewith is a Terminal Disclaimer and thus it is respectfully submitted that the obviousness-type double patenting rejection is overcome.

Applicants gratefully acknowledge the indication that claims 2-8, 10-14, and 16-20 include allowable subject matter. The subject matter of claims 8, 13, and 16 has been incorporated into respective independent claims 1, 9, and 15, and as such it is respectfully submitted that all pending claims are in condition for allowance.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Respectfully submitted,

Date: February 7, 2014

/Mark J. Rozman/

Mark J. Rozman
Registration No. 42,117
TROP, PRUNER & HU, P.C.
1616 S. Voss Road, Suite 750
Houston, Texas 77057-2631
(512) 418-9944 [Phone]
(713) 468-8883 [Fax]
Customer No.: 47795

PTO/SB/08a (01-10)
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	Art Unit	2116
	Examiner Name	Stefan Stoynov
	Attorney Docket Number	ITL.2495US (P38410)

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	Attorney Docket Number	ITL.2495US (P38410)

	1	INTEL DEVELOPER FORUM, IDF2010, Opher Kahn, et al., "Intel Next Generation Microarchitecture Codename Sandy Bridge: New Processor Innovations," September 13, 2010, 58 pages.	☐

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EXAMINER SIGNATURE

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Signature	/Mark J. Rozman/	Date (YYYY-MM-DD)	2014-02-07
Name/Print	Mark J. Rozman	Registration Number	42,117

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8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal	
Application Number:	13225677
Filing Date:	06-Sep-2011
Title of Invention:	Dynamically Allocating A Power Budget Over Multiple Domains Of A Processor
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Filer:	Mark J. Rozman/Pamela Polnick
Attorney Docket Number:	ITL.2495US (P38410)
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt	
EFS ID:	18150021
Application Number:	13225677
International Application Number:	
Confirmation Number:	2063
Title of Invention:	Dynamically Allocating A Power Budget Over Multiple Domains Of A Processor
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Customer Number:	47795
Filer:	Mark J. Rozman/Pamela Polnick
Filer Authorized By:	Mark J. Rozman
Attorney Docket Number:	ITL.2495US (P38410)
Receipt Date:	07-FEB-2014
Filing Date:	06-SEP-2011
Time Stamp:	16:36:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$180
RAM confirmation Number	3292
Deposit Account	201504
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1		ITL_2495US_ROA_11-13-14.pdf	24295 169a2bc4469cbed357c360876732e2db07819af0	yes	7

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Specification	2	2
	Claims	3	6
	Applicant Arguments/Remarks Made in an Amendment	7	7

Warnings:

Information:

2	Information Disclosure Statement (IDS) Form (SB08)	ITL_2495US_IDS_Refiling_Sandy_Bridge.pdf	612267 c421ccc416edf145481014ff2d7e4664abb1550e	no	4

Warnings:

Information:

A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.

3	Non Patent Literature	NPLSandyBridgePart1.pdf	11121046 e1b640a059e2d50ae56e5832b7b892595fa97b79	no	20

Warnings:

Information:

4	Non Patent Literature	NPLSandyBridgePart2.pdf	12406256 f51761d5c13eff89c805d7c17bada9a63c989983	no	20

Warnings:

Information:

5	Non Patent Literature	NPLSandyBridgePart3.pdf	9193783 27168a01f739c23084aef0de68e18ec80007acdd	no	18

Warnings:

Information:

6	Fee Worksheet (SB06)	fee-info.pdf	30736 a1b3b457ac1a8f6c59f878fbb14c80074541080b	no	2

Warnings:

Information:

Total Files Size (in bytes):	33388383

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: DIST.E.FILE **Document Description: Electronic Terminal Disclaimer - Filed**	PTO/SB/25 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A PROVISIONAL DOUBLE PATENTING REJECTION OVER A PENDING "REFERENCE" APPLICATION**
Application Number	13225677
Filing Date	06-Sep-2011
First Named Inventor	Avinash Ananthakrishnan
Attorney Docket Number	ITL.2495US (P38410)
Title of Invention	Dynamically Allocating A Power Budget Over Multiple Domains Of A Processor

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
Intel Corporation	100%

The owner(s) of percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of any patent granted on pending reference Application Number(s)

13780066 filed on 02/28/2013

as the term of any patent granted on said reference application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending reference application. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and any patent granted on the reference application are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term of any patent granted on said reference application, "as the term of any patent granted on said reference application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending reference application," in the event that any such patent granted on the pending reference application: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.

◉ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

○ I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.	
Applicant claims the following fee status: ○ Small Entity ○ Micro Entity ◉ Regular Undiscounted I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.	
THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES I certify, in accordance with 37 CFR 1.4(d)(4) that I am: ◉ An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application Registration Number 42117 ○ A sole inventor ○ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application ○ A joint inventor; all of whom are signing this request	
Signature	/Mark J. Rozman/
Name	Mark J. Rozman

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal	
Application Number:	13225677
Filing Date:	06-Sep-2011
Title of Invention:	Dynamically Allocating A Power Budget Over Multiple Domains Of A Processor
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Filer:	Mark J. Rozman/Pamela Polnick
Attorney Docket Number:	ITL.2495US (P38410)
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Statutory or Terminal Disclaimer	1814	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
		Total in USD ($)		**160**

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 13225677

Filing Date: 06-Sep-2011

Applicant/Patent under Reexamination: Ananthakrishnan et al.

Electronic Terminal Disclaimer filed on February 7, 2014

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt	
EFS ID:	18144129
Application Number:	13225677
International Application Number:	
Confirmation Number:	2063
Title of Invention:	Dynamically Allocating A Power Budget Over Multiple Domains Of A Processor
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Customer Number:	47795
Filer:	Mark J. Rozman/Pamela Polnick
Filer Authorized By:	Mark J. Rozman
Attorney Docket Number:	ITL.2495US (P38410)
Receipt Date:	07-FEB-2014
Filing Date:	06-SEP-2011
Time Stamp:	16:46:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$160
RAM confirmation Number	3499
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Electronic Terminal Disclaimer-Filed	eTerminal-Disclaimer.pdf	33931 a020ea16bc1261ddda7bfcfbc245de7e939a950f	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30604 a4b58c8a16912781a2514f4029ae381db9364c03	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	64535		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
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National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/225,677	Filing Date 09/06/2011	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 02/07/2014	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 17	Minus	** 20	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SLIE
/KIMBERLY D. WILLIAMS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13225677
	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5287292		1994-02-15	Kenny, et al.	
If you wish to add additional U.S. Patent citation information please click the Add button.						
U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20050288886		2005-12-29	Therien, et al.	
	2	20070106428		2007-05-10	Omizo, et al.	
	3	20080077282		2008-03-27	Hartman, et al.	
	4	20040030940		2004-02-12	Espinoza-Ibarra, et al.	
	5	20120114010		2012-05-10	Branch	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13225677
	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

	6	20070260895		2007-11-08	Aguilar, et al.	
	7	20060041766		2006-02-23	Adachi	

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13225677
	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Mark J. Rozman/	Date (YYYY-MM-DD)	2013-11-22
Name/Print	Mark J. Rozman	Registration Number	42,117

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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Filing Date:	06-Sep-2011
Title of Invention:	Dynamically Allocating A Power Budget Over Multiple Domains Of A Processor
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Filer:	Mark J. Rozman/Stephanie Petreas
Attorney Docket Number:	ITL.2495US (P38410)
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
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Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt	
EFS ID:	17481375
Application Number:	13225677
International Application Number:	
Confirmation Number:	2063
Title of Invention:	Dynamically Allocating A Power Budget Over Multiple Domains Of A Processor
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Customer Number:	47795
Filer:	Mark J. Rozman/Stephanie Petreas
Filer Authorized By:	Mark J. Rozman
Attorney Docket Number:	ITL.2495US (P38410)
Receipt Date:	22-NOV-2013
Filing Date:	06-SEP-2011
Time Stamp:	15:30:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$180
RAM confirmation Number	2350
Deposit Account	201504
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees) Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	ITL2495USIDSToFile.pdf	38171 0acfac42aca4b0b70bffc421f79c092b535805d3	no	4
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
2	Fee Worksheet (SB06)	fee-info.pdf	30737 7d944bdf7ab20a54d04f0ece70d8f566769eb2be	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	68908		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13225677
	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2116
	Examiner Name	Stefan Stoynov
	Attorney Docket Number	ITL.2495US (P38410)

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7603577		2009-10-13	Yamaji, et al.	
If you wish to add additional U.S. Patent citation information please click the Add button.						

U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20120096288		2012-04-19	Bates, et al.	
If you wish to add additional U.S. Published Application citation information please click the Add button.						

FOREIGN PATENT DOCUMENTS								
Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐
If you wish to add additional Foreign Patent Document citation information please click the Add button								

NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13225677
	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2116
	Examiner Name	Stefan Stoynov
	Attorney Docket Number	ITL.2495US (P38410)

	1		☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13225677
	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2116
	Examiner Name	Stefan Stoynov
	Attorney Docket Number	ITL.2495US (P38410)

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Mark J. Rozman/	Date (YYYY-MM-DD)	2013-11-20
Name/Print	Mark J. Rozman	Registration Number	42,117

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal	
Application Number:	13225677
Filing Date:	06-Sep-2011
Title of Invention:	Dynamically Allocating A Power Budget Over Multiple Domains Of A Processor
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Filer:	Mark J. Rozman/Stephanie Petreas
Attorney Docket Number:	ITL.2495US (P38410)
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt	
EFS ID:	17452619
Application Number:	13225677
International Application Number:	
Confirmation Number:	2063
Title of Invention:	Dynamically Allocating A Power Budget Over Multiple Domains Of A Processor
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Customer Number:	47795
Filer:	Mark J. Rozman/Stephanie Petreas
Filer Authorized By:	Mark J. Rozman
Attorney Docket Number:	ITL.2495US (P38410)
Receipt Date:	20-NOV-2013
Filing Date:	06-SEP-2011
Time Stamp:	12:42:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$180
RAM confirmation Number	10804
Deposit Account	201504
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	ITL2495USIDSToFile.pdf	36878 e7e85466f3575cc575355430ebe6f07384a30f65	no	4
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
2	Fee Worksheet (SB06)	fee-info.pdf	30737 ff699bde59db0dc3637ddb4d2a7bc7c09a419479	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	67615		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/225,677	09/06/2011	Avinash N. Ananthakrishnan	ITL.2495US (P38410)	2063

47795 7590 11/13/2013

TROP, PRUNER & HU, P.C.
1616 S. VOSS RD., SUITE 750
HOUSTON, TX 77057-2631

EXAMINER	
STOYNOV, STEFAN	
ART UNIT	PAPER NUMBER
2116	
MAIL DATE	DELIVERY MODE
11/13/2013	PAPERPAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 13/225,677	Applicant(s) ANANTHAKRISHNAN ET AL.	
	Examiner STEFAN STOYNOV	Art Unit 2116	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09/06/2011*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-20* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☒ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *06/06/2011* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some * c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/3/12 and two filed on 5/22/13*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

Information Disclosure Statement

The information disclosure statement (IDS) filed 10/03/2012 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed (no copy was provided for Citation No. 19 under NON-PATENT LITERATURE DOCUMENTS). In addition, the IDS filed 10/03/2012 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language (Citation No. 4 under FOREIGN PATENT DOCUMENTS). It has been placed in the application file, but the information referred to therein has not been considered.

Further, the IDS filed 05/22/2013 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language (Citation No. 1 under FOREIGN PATENT DOCUMENTS). It has been placed in the application file, but the information referred to therein has not been considered.

Specification

The abstract of the disclosure is objected to because the title of the invention appears on the same sheet as the abstract. Correction is required. See MPEP § 608.01(b).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the claims at issue are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the reference application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO internet Web site contains terminal disclaimer forms which may be used. Please visit http://www.uspto.gov/forms/. The filing date of the application will determine what form should be used. A web-based eTerminal Disclaimer may be filled out completely online

using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 1-20 are provisionally rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of copending Application No. 13/780,066. Although the claims at issue are not identical, they are not patentably distinct from each other because all claim limitations of claims 1-20 in the current Application are disclosed in claims 1-20 of copending Application No. 13/780,066.

"Generally, an obviousness-type double patenting analysis entails two steps. First, as a matter of law, a court construes the claim in the earlier patent and the claim in the later patent and determines the differences. Georgia-Pacific Corp. v. United States Gypsum Co., 195 F.3d 1322, 1326, 52, USPQ2d 1590, 1593 (Fed. Cir. 1999). Second, the court determines whether the differences in the subject matter between the two claims render the claims patentably distinct. Id. at 1327, 52 USPQ2d at 1595. A later claim that is not patentably distinct from an earlier claim in a commonly owned patent is invalid for obvious-type double patenting. In re Berg, 140 F.3d 1428, 1431,46 USPQ2d 1226, 1229 (Fed. Cir. 1998). A later patent claim is not patentably distinct from an earlier parent claim if the later claim is obvious over, **or anticipated by**, the patent claim. In re Longi, 759 F.2d at 896, 255 USPQ at 651 (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus)." Eli Lilly and Company v Barr Laboratories, Inc., United States Court of Appeals for the Federal Circuit, On petition for Rehearing en banc (decided: May 30, 2001).

This is a provisional nonstatutory double patenting rejection because the patentably indistinct claims have not in fact been patented.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 9, and 15 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Gunther et al., US Patent Appl. Pub. No. 2008/0136397.

Regarding claim 1, Gunther discloses an apparatus (FIG(s) 1-5) comprising:

a multi-domain processor including a first domain and a second domain (FIG(s) 1, 2, 4, and 5, paragraphs 0009 and 0013), each of the first and second domains to operate at an independent voltage and frequency (paragraph 0008, lines 1-8, paragraph 0010, lines 10-18, paragraph 0014, lines 1-18), the multi-domain processor further including first logic (power management logic 105, power management unit 204) to dynamically allocate a power budget (desired power consumption target, provided by the single power supply 110 – paragraph 0008, lines 8-11, paragraph 0012, lines 1-6) for the multi-domain processor between the first and the second domains at run time (paragraphs 0010-0016).

Regarding claim 9, Gunther discloses a method (FIG(s) 1-5) comprising:

determining, in a power controller (power management logic 105, power management unit 204) of a multi-domain processor (paragraphs 0012, 0017, and 0023), a power budget for

the multi-domain processor for a current time interval (desired power consumption target, provided by the single power supply 110 – paragraph 0008, lines 8-11, paragraph 0012, lines 1-6), the multi-domain processor including at least a first domain and a second domain (FIG(s) 1, 2, 4, and 5, paragraphs 0009 and 0013);

determining, in the power controller, a portion of the power budget to be allocated to the first and the second domains (paragraph 0008, lines 1-8, paragraph 0010, lines 10-18, paragraph 0014, lines 1-18); and

controlling a frequency of the first domain and a frequency of the second domain based on the allocated portions (paragraphs 0010-0016).

Regarding claim 15, Gunther discloses a system (FIG(s) 1-5) comprising:

a multicore processor (paragraph 0012) having a first domain including a plurality of cores (FIG(s) 1 and 2, paragraphs 0009, 0012, and 0013), a second domain including a graphics engine (paragraphs 0009, 0012, and 0013), and a third domain (formed on IC DIE 200 after excluding Domain 1-M) including system agent circuitry (power management unit 204), the third domain to operate at a fixed power budget (inherently disclosed – power management unit receives constant amount of power fed by the single power supply 110, paragraph 0008, lines 8-11, FIG. 2) and to dynamically allocate a variable power budget between the first and the second domains (paragraphs 0010-0016); and

a dynamic random access memory (DRAM) coupled to the multicore processor (paragraphs 0012 and 0018).

Allowable Subject Matter

Claims 2-8, 10-14, and 16-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and the nonstatutory obviousness-type double patenting rejection, set forth in this Office action is overcome.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Axford et al., US Patent No. 7,624,215, Tokue, US Patent No. 7,752,467, Dahan et al., US Patent Appl. Pub. No. 2008/0307240, and Arndt et al., US Patent Appl. Pub. No. 2012/0116599 show similar inventions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEFAN STOYNOV whose telephone number is (571)272-4236. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stefan Stoynov/
Primary Examiner, Art Unit 2116

Notice of References Cited	Application/Control No. 13/225,677	Applicant(s)/Patent Under Reexamination ANANTHAKRISHNAN ET AL.	
	Examiner STEFAN STOYNOV	Art Unit 2116	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2008/0136397	06-2008	Gunther et al.	323/299
*	B	US-7,624,215	11-2009	Axford et al.	710/260
*	C	US-7,752,467	07-2010	Tokue, Tatsuya	713/300
*	D	US-2008/0307240	12-2008	Dahan et al.	713/320
*	E	US-2012/0116599	05-2012	Arndt et al.	700/291
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	297	(plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or third or individual or independent or other or another) adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1))) same (((graphic$2 or video or image or media or multimedia or (multi adj media)) adj (processor$1 or microprocessor$1 or cpu$1 or core$1)) or (graphic$2 adj ((processing adj unit$1) or engine$1 or chip or controller)) or GPU$1) same ((system adj (agent or chip or controller)) or ((power or energy) adj (control$4 or manag$5 or logic)) or PCU or PMU or ((display or monitor or graphic$2 or video) adj (controller or adapter or card)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 16:34
L2	84	(plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or third or individual or independent or other or another) adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1))) with (((graphic$2 or video or image or media or multimedia or (multi adj media)) adj (processor$1 or microprocessor$1 or cpu$1 or core$1)) or (graphic$2 adj ((processing adj unit$1) or engine$1 or chip or controller)) or GPU$1) with ((system adj (agent or chip or controller)) or ((power or energy) adj (control$4 or manag$5 or logic)) or PCU or PMU or ((display or monitor or graphic$2 or video) adj (controller or adapter or card)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 16:36
L3	2	1 same ((fixed or preset or (pre adj set) or constant$2 or permanent$2 or continuous$2 or always) near3 (power$2 or voltage$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 16:41
L4	2	2 with ((fixed or preset or (pre adj set) or constant$2 or permanent$2 or continuous$2 or always) near3 (power$2	US-PGPUB; USPAT; EPO; JPO;	OR	OFF	2013/11/09 16:41

		or voltage$1))	DERWENT; IBM_TDB			
L5	11	1 and ((fixed or preset or (pre adj set) or constant$2 or permanent$2 or continuous$2 or always) near3 (power$2 or voltage$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 16:42
L6	4	2 and ((fixed or preset or (pre adj set) or constant$2 or permanent$2 or continuous$2 or always) near3 (power$2 or voltage$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 16:42
L7	18573	(((power or energy) adj (control$4 or manag$5 or logic)) or PCU or PMU) same ((fixed or preset or (pre adj set) or constant$2 or permanent$2 or continuous$2 or always) near3 (power$2 or voltage$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 16:50
L8	11707	(((power or energy) adj (control$4 or manag$5 or logic)) or PCU or PMU) with ((fixed or preset or (pre adj set) or constant$2 or permanent$2 or continuous$2 or always) near3 (power$2 or voltage$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 16:51
L9	82	7 same (plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or third or individual or independent or other or another) adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 16:51
L10	19	8 with (plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or third or individual or independent or other or another) adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 16:52
L11	2682	(((power or energy) adj (control$4 or manag$5 or logic)) or PCU or PMU) same ((fixed or preset or (pre adj set) or constant$2 or permanent$2 or continuous$2 or always) near3 (power$2 or voltage$1) near3 (supplied or provid$3 or feed$3 or fed or coupl$3 or connect$3 or receiv$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 17:14
L12	1587	(((power or energy) adj (control$4 or manag$5 or logic)) or PCU or PMU) with ((fixed or preset or (pre adj set) or constant$2 or permanent$2 or continuous$2 or always) near3 (power$2 or voltage$1) near3 (supplied or provid$3 or feed$3 or fed or coupl$3 or connect$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 17:14

		or receiv$3))				
L13	315	11.clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 17:14
L14	251	12.clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 17:14
L15	25	13 and (plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or third or individual or independent or other or another) adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 17:15
L16	21	14 and (plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or third or individual or independent or other or another) adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 17:15
L17	2	11/242045	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 17:17
L18	196	11 and 713/3$2.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 17:19
L19	118	12 and 713/3$2.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 17:19
L20	21	18 and (plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or third or individual or independent or other or another) adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 17:19
L21	7	19 and (plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate	US-PGPUB; USPAT;	OR	OFF	2013/11/09 17:20

		or different or first or second or third or individual or independent or other or another) adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1)))	EPO; JPO; DERWENT; IBM_TDB			
L22	1	1 same ((power or energy) near2 shar$3 near2 (value$1 or limit$1 or threshold$1 or setting$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 17:34
L23	1	2 with ((power or energy) near2 shar$3 near2 (value$1 or limit$1 or threshold$1 or setting$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 17:34
L24	2	1 and ((power or energy) near2 shar$3 near2 (value$1 or limit$1 or threshold$1 or setting$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 17:35
L25	2	2 and ((power or energy) near2 shar$3 near2 (value$1 or limit$1 or threshold$1 or setting$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 17:35
L26	2	1 same (shar$3 near3 (power or energy))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 17:35
L27	1	2 with (shar$3 near3 (power or energy))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 17:35
L28	63	1 and (shar$3 near3 (power or energy))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 17:35
L29	2	2 and (shar$3 near3 (power or energy))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 17:35
L38	174	(US-20120079290-$ or US-20110154090-$ or US-20110072429-$ or US-20110022865-$ or US-20100332927-$ or US-20100191997-$ or US-20100146513-$ or US-20100115309-$ or US-20090313489-$ or US-20090271646-$ or US-20090235105-$ or US-20090172428-$ or US-20090172375-$ or US-20090158067-$ or US-20090158061-$ or US-20090150696-$ or US-20090150695-$ or US-20090132844-$ or US-20090070605-$ or US-20090006871-$ or	US-PGPUB; USPAT; DERWENT	OR	OFF	2013/11/09 17:39

		US-20080250260-$ or US-20080028240-$ or US-20080005603-$ or US-20070245163-$ or US-20070239398-$ or US-20070234083-$).did. or (US-20070214342-$ or US-20070156992-$ or US-20070106827-$ or US-20070079294-$ or US-20070033425-$ or US-20070016817-$ or US-20070005995-$ or US-20060184287-$ or US-20060149975-$ or US-20060117202-$ or US-20060069936-$ or US-20060059286-$ or US-20060053326-$ or US-20060050670-$ or US-20050132238-$ or US-20050046400-$ or US-20050033881-$ or US-20050022038-$ or US-20040268166-$ or US-20040139356-$ or US-20040098560-$ or US-20040064752-$ or US-20030061383-$ or US-20020194509-$ or US-20010044909-$).did. or (US-8015427-$ or US-7966511-$ or US-7797512-$ or US-7730340-$ or US-7650518-$ or US-7539885-$ or US-7529956-$ or US-7502948-$ or US-7454632-$ or US-7437270-$ or US-7434073-$ or US-7412615-$ or US-7272730-$ or US-7249268-$ or US-7194643-$ or US-7146514-$ or US-7111179-$ or US-7093147-$ or US-7043649-$ or US-7010708-$ or US-6996728-$ or US-6908227-$ or US-6829713-$ or US-6823516-$ or US-6792392-$ or US-6748546-$).did. or (US-5931950-$ or US-5621250-$ or US-5590341-$ or US-5522087-$ or US-5163153-$).did. or (WO-9016029-$ or WO-2012040052-$ or WO-2008117133-$ or WO-2007038800-$ or WO-2006029152-$ or WO-2004070594-$ or WO-2004066092-$ or WO-0227451-$ or US-7797512-$ or US-7272730-$ or US-7111179-$ or US-6823516-$ or US-6792392-$ or US-5621250-$ or US-5590341-$ or US-5522087-$ or US-4019973-$ or US-20110154090-$ or US-20110072429-$ or US-20110022865-$ or US-20100332927-$ or US-20100191997-$ or US-20100146513-$ or US-20090313489-$ or US-20090271646-$ or US-20090235105-$).did. or (US-20090172428-$ or US-20090172375-$ or US-20090158067-$ or US-20090158061-$ or US-20090150696-$ or US-20090150695-$ or US-20090132844-$ or US-20090070605-$ or US-20090006871-$ or US-20080263384-$ or US-20080250260-$ or US-20080201591-$ or US-20080028240-$ or US-20080016380-$ or US-20080005603-$ or US-20080005592-$ or US-20070245163-$ or US-20070239398-$ or US-20070234083-$ or US-20070214342-$ or US-20070156992-$ or US-20070106827-$ or US-20070033425-$ or US-20070005995-$ or US-20060288240-$ or US-						

		20060184287-$ or US-20060149975-$).did. or (US-20060117202-$ or US-20060069936-$ or US-20060053326-$ or US-20060050670-$ or US-20060026447-$ or US-20050289365-$ or US-20050216719-$ or US-20050132238-$ or US-20050071694-$ or US-20050046400-$ or US-20050033881-$ or US-20050022038-$ or US-20040268166-$ or US-20040215987-$ or US-20040139356-$ or US-20040098631-$ or US-20040098560-$ or US-20040064752-$ or US-20040037346-$ or US-20030204759-$ or US-20030061383-$ or US-20020194509-$ or US-20020087901-$ or US-20010044909-$ or SE-7412615-$ or NL-7412615-$ or JP-2009180784-$).did. or (EP-886427-$ or EP-1363180-$ or DE-2515645-$ or DE-2425579-$ or DE-1813570-$ or CS-7502948-$ or BR-7502948-$ or BE-834006-$ or BE-814753-$ or BE-771069-$).did.				
L39	0	38 and 11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 17:40
S1	21567	(control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or reallocate$3 or (re adj allocate$3) or assign$5 or distrubut$3 or split$3 or divid$3) near5 (((power or energy) adj budget) or ((total or global or full or entire or available) adj (power or energy)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 14:43
S2	4	S1 same (shar$3 near2 (polic$3 or rule$1 or strateg$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 14:43
S3	4	S1 with (shar$3 near2 (polic$3 or rule$1 or strateg$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 14:44
S4	29	S1 and (shar$3 near2 (polic$3 or rule$1 or strateg$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:04
S5	74	((determin$5 or decid$3 or establish$3 or set$4 or estimat$4 or calculat$3 or compute or computes or computing or defin$3 or select$3 or choos$3) same ((power or energy) adj budget)) same (((past or previous$2 or earlier or previous$3) near2 (time$1 or interval$1 or period$1 or duration$1)) or histor$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:06
S6	19	((determin$5 or decid$3 or establish$3 or set$4 or estimat$4 or calculat$3 or compute or computes or computing or	US-PGPUB; USPAT; EPO; JPO;	OR	OFF	2013/11/09 15:06

		defin$3 or select$3 or choos$3) with ((power or energy) adj budget)) with ((((past or previous$2 or earlier or previous$3) near2 (time$1 or interval$1 or period$1 or duration$1)) or histor$4)	DERWENT; IBM_TDB			
S7	2	S5 same ((thermal or temperature or heat or power) near2 (decay$3 or deteriorat$4 or declin$3 or worsen$3 or degrad$6 or degenerat$4) adj (value$1 or rate$1 or degree or amount or level or scale))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:07
S8	2	S6 with ((thermal or temperature or heat or power) near2 (decay$3 or deteriorat$4 or declin$3 or worsen$3 or degrad$6 or degenerat$4) adj (value$1 or rate$1 or degree or amount or level or scale))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:07
S9	2	S5 and ((thermal or temperature or heat or power) near2 (decay$3 or deteriorat$4 or declin$3 or worsen$3 or degrad$6 or degenerat$4) adj (value$1 or rate$1 or degree or amount or level or scale))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:07
S10	2	S6 and ((thermal or temperature or heat or power) near2 (decay$3 or deteriorat$4 or declin$3 or worsen$3 or degrad$6 or degenerat$4) adj (value$1 or rate$1 or degree or amount or level or scale))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:07
S11	1245	S1 same (dynamic$4 or adaptive$2 or runtime or (run adj time))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:10
S12	609	S1 with (dynamic$4 or adaptive$2 or runtime or (run adj time))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:10
S13	14	S11 same (plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent or each or only or all) adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:10
S14	3	S12 with (plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent or each or only or all) adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:11
S15	2	S13 same (workload or (work adj load))	US-PGPUB; USPAT; EPO; JPO; DERWENT;	OR	OFF	2013/11/09 15:13

			IBM_TDB			
S16	2	S14 with (workload or (work adj load))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:13
S17	4	S13 and (workload or (work adj load))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:13
S18	2	S14 and (workload or (work adj load))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:13
S19	199	((preset or predetermined or preestablished or preconfigured or preprogrammed or predefined or prestored or (pre adj (determined or established or configured or programmed or defined or stored)) or minim$2 or set or defined or reserv$5 or registered) near2 (value$1 or limit$1 or threshold$1 or setting$1)) same ((power or energy) adj budget)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:22
S20	101	((preset or predetermined or preestablished or preconfigured or preprogrammed or predefined or prestored or (pre adj (determined or established or configured or programmed or defined or stored)) or minim$2 or set or defined or reserv$5 or registered) near2 (value$1 or limit$1 or threshold$1 or setting$1)) with ((power or energy) adj budget)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:23
S21	2	S19 same (plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent or each or every or all) adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:23
S22	2	S20 with (plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent or each or every or all) adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:24
S23	1137	S1 same ((preset or predetermined or preestablished or preconfigured or preprogrammed or predefined or	US-PGPUB; USPAT; EPO; JPO;	OR	OFF	2013/11/09 15:26

		prestored or (pre adj (determined or established or configured or programmed or defined or stored)) or minim$2 or set or defined or reserv$5 or registered) near2 (value$1 or limit$1 or threshold$1 or setting$1))	DERWENT; IBM_TDB			
S24	526	S1 with ((preset or predetermined or preestablished or preconfigured or preprogrammed or predefined or prestored or (pre adj (determined or established or configured or programmed or defined or stored)) or minim$2 or set or defined or reserv$5 or registered) near2 (value$1 or limit$1 or threshold$1 or setting$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:26
S25	4	S23 same (shar$3 near2 (polic$3 or rule$1 or strateg$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:27
S26	2	S24 with (shar$3 near2 (polic$3 or rule$1 or strateg$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:27
S27	6	S23 same (shar$3 near2 (value$1 or limit$1 or threshold$1 or setting$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:28
S28	2	S24 with (shar$3 near2 (value$1 or limit$1 or threshold$1 or setting$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:28
S29	4	S23 and (shar$3 near2 (polic$3 or rule$1 or strateg$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:28
S30	2	S24 and (shar$3 near2 (polic$3 or rule$1 or strateg$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:28
S31	16	S23 and (shar$3 near2 (value$1 or limit$1 or threshold$1 or setting$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:29
S32	6	S24 and (shar$3 near2 (value$1 or limit$1 or threshold$1 or setting$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:29
S33	201	((power or energy) near2 shar$3) same ((control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or reallocate$3 or (re adj allocate$3) or	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:33

		assign$5 or distrubut$3 or split$3 or divid$3 or var$5) near5 (((power or energy) adj budget) or ((total or global or full or entire or available) adj (power or energy))))				
S34	104	(((power or energy) near2 shar$3) with (((control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or reallocate$3 or (re adj allocate$3) or assign$5 or distrubut$3 or split$3 or divid$3 or var$5) near5 (((power or energy) adj budget) or ((total or global or full or entire or available) adj (power or energy))))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:33
S35	9	S33 same (plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent or each or every or all) adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:34
S36	2	S34 with (plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent or each or every or all) adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:34
S37	2	S35 same (shar$3 near2 (value$1 or limit$1 or threshold$1 or setting$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:35
S38	2	S36 with (shar$3 near2 (value$1 or limit$1 or threshold$1 or setting$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:35
S39	2	S35 and (shar$3 near2 (value$1 or limit$1 or threshold$1 or setting$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:35
S40	2	S36 and (shar$3 near2 (value$1 or limit$1 or threshold$1 or setting$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 15:35

EAST Search History (Interference)

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11/9/2013 5:47:13 PM
C:\Users\sstoynov1\Documents\EAST\Workspaces\13225677_7.wsp

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13225677
	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7966511		2011-06-21	Naveh, et al.	
	~~2~~	~~7434073~~		~~2008-10-07~~	~~Maglins, et al.~~	

Duplicate reference, cited in IDS filed 10/3/12

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

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	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	INTERNATIONAL SEARCHING AUTHORITY, "Notification of Transmittal of the International Search Report and the Written Opinion of the International Searching Authority," mailed March 14, 2013, in International application no. PCT/US2012/053726.	☐

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EXAMINER SIGNATURE

Examiner Signature	/Stefan Stoynov/ (11/07/2013)	Date Considered	11/07/2013

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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PTO/SB/08a (01-10)
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	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6908227		2005-06-21	Fusu, et al.	
	2	7797512		2010-09-14	Cheng, et al.	
	3	7146514		2006-12-05	Kaushik, et al.	
	4	8015427		2011-09-06	Miller, et al.	
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U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20090313489		2009-12-17	Gunther, et al.	
	2	20100332927		2010-12-30	Kurts, et al.	

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	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

	3	20070234083		2007-10-04	Lee	
	4	20110022865		2011-01-27	Gunther, et al.	
	5	20080005603		2008-01-03	Deep, et al.	
	6	20090070605		2009-03-12	Nijhawan, et al.	
	7	20110072429		2011-03-24	Celeskey, et al.	
	8	20050046400		2005-03-03	Rotem	
	9	20090271646		2009-10-29	Talwar, et al.	

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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
~~...~~	~~1~~	~~KR 10-2006-012846~~	~~KR~~		~~2006-12-14~~	~~LG Electronics Inc.~~		☐

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	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	DAVID L. HILL, et al., "The Uncore: A Modular Approach To Feeding The High-Performance Cores," Intel Technology Journal, 2010, Vol 14, Issue 3, pages ~~38-49.~~ 1-23.	☐

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EXAMINER SIGNATURE

Examiner Signature	/Stefan Stoynov/ (11/07/2013)	Date Considered	11/07/2013

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L31	21	(ANANTHAKRISHNAN adj AVINASH).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/07 16:53
L32	97	(ROTEM adj EFRAIM).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/07 16:56
L33	35	(RAJWAN adj DORON).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/07 16:59
L34	65	(WEISSMANN adj ELIEZER).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/07 16:59
L35	28	(SHULMAN adj NADAV).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/07 17:01
L36	2	(31 or 32 or 33 or 34 or 35) and ((multi adj domain adj (processor or microprocessor or cpu or core)) and ((first or second) adj domain$1) and dynamic$4 and logic and (allocat$4 near2 (power or energy)) and ((power or energy) adj (budget$1 or limit$1 or threshold$1)) and (runtime or (run adj time))).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/07 17:10
L37	0	Intel.as. and ((multi adj domain adj (processor or microprocessor or cpu or core)) and ((first or second) adj domain$1) and dynamic$4 and logic and (allocat$4 near2 (power or energy)) and ((power or energy) adj (budget$1 or limit$1 or threshold$1)) and (runtime or (run adj time))).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/07 17:11
L38	2	(31 or 32 or 33 or 34 or 35) and (((power or energy) adj control$4) and (multi adj domain adj (processor or microprocessor or cpu or core)) and ((power or energy) adj (budget$1 or limit$1 or threshold$1)) and allocat$4 and (tim$3 near2 (interval$1 or period$1 or duration$1)) and ((first or second) adj domain$1) and ((control$4 or manag$5 or regulat$4 or correct$4 or	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/07 17:15

		adjust$5 or chang$3 or modif$6 or alter$6 or vary$3) near2 frequenc$3)).clm.				
L39	0	Intel.as. and (((power or energy) adj control$4) and (multi adj domain adj (processor or microprocessor or cpu or core)) and ((power or energy) adj (budget$1 or limit$1 or threshold$1)) and allocat$4 and (tim$3 near2 (interval$1 or period$1 or duration$1)) and ((first or second) adj domain$1) and ((control$4 or manag$5 or regulat$4 or correct$4 or adjust$5 or chang$3 or modif$6 or alter$6 or vary$3) near2 frequenc$3)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/07 17:16
L40	2	(31 or 32 or 33 or 34 or 35) and ((multicore or multiprocessor or ((multi$3 or plural$3 or several or (more adj2 one)) adj (core$1 or processor$1))) and (graphic$2 adj engine) and ((first or second or third) adj domain) and ((power or energy) adj (budget$1 or limit$1 or threshold$1)) and dynamic$4 and (allocat$4 near2 (power or energy)) and ((dynamic adj random adj access adj memory) or DRAM)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/07 17:23
L41	0	Intel.as. and ((multicore or multiprocessor or ((multi$3 or plural$3 or several or (more adj2 one)) adj (core$1 or processor$1))) and (graphic$2 adj engine) and ((first or second or third) adj domain) and ((power or energy) adj (budget$1 or limit$1 or threshold$1)) and dynamic$4 and (allocat$4 near2 (power or energy)) and ((dynamic adj random adj access adj memory) or DRAM)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/07 17:24
L42	1	(multi adj domain adj (processor or microprocessor or cpu or core)) same ((first or second) adj domain$1) same dynamic$4 same logic same (allocat$4 near2 (power or energy)) same ((power or energy) adj (budget$1 or limit$1 or threshold$1)) same (runtime or (run adj time))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/07 17:27
L43	2	((power or energy) adj control$4) same (multi adj domain adj (processor or microprocessor or cpu or core)) same ((power or energy) adj (budget$1 or limit$1 or threshold$1)) same allocat$4 same (tim$3 near2 (interval$1 or period$1 or duration$1)) same ((first or second) adj domain$1) same ((control$4 or manag$5 or regulat$4 or correct$4 or adjust$5 or chang$3 or modif$6 or alter$6 or vary$3) near2 frequenc$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/07 17:28
L44	0	((power or energy) adj control$4) with (multi adj domain adj (processor or microprocessor or cpu or core)) with ((power or energy) adj (budget$1 or limit$1 or threshold$1)) with allocat$4 with (tim$3 near2 (interval$1 or period$1 or duration$1)) with ((first or second) adj domain$1) with ((control$4 or manag$5 or regulat$4 or correct$4 or adjust$5 or chang$3 or modif$6 or alter$6 or vary$3) near2 frequenc$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/07 17:30

L45	2	(multicore or multiprocessor or ((multi$3 or plural$3 or several or (more adj2 one)) adj (core$1 or processor$1))) same (graphic$2 adj engine) same ((first or second or third) adj domain) same ((power or energy) adj (budget$1 or limit$1 or threshold$1)) same dynamic$4 same (allocat$4 near2 (power or energy)) same ((dynamic adj random adj access adj memory) or DRAM)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/07 17:32
L46	0	(multicore or multiprocessor or ((multi$3 or plural$3 or several or (more adj2 one)) adj (core$1 or processor$1))) with (graphic$2 adj engine) with ((first or second or third) adj domain) with ((power or energy) adj (budget$1 or limit$1 or threshold$1)) with dynamic$4 with (allocat$4 near2 (power or energy)) with ((dynamic adj random adj access adj memory) or DRAM)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/07 17:32

EAST Search History (Interference)

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11/7/2013 5:36:41 PM
C:\Users\sstoynov1\Documents\EAST\Workspaces\13225677.wsp

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	989	(plural$3 or multi$3 or (more adj2 one) or two or several or separate or different or first or second) adj power adj domain$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 08:59
L2	38	1 same (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or different or first or second or dual) adj (processor$1 or microprocessor$1 or cpu$1 or core$1)) or multiprocessor or multicpu or multicore or dualcore)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:00
L3	24	1 with (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or different or first or second or dual) adj (processor$1 or microprocessor$1 or cpu$1 or core$1)) or multiprocessor or multicpu or multicore or dualcore)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:00
L4	1	2 same ((power or energy) near3 (allocat$4 or assign$5 or distrubut$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:00
L5	0	3 with ((power or energy) near3 (allocat$4 or assign$5 or distrubut$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:00
L6	0	2 and ((power or energy) near3 (allocat$4 or assign$5 or distrubut$3) near3 (dynamic$4 or adaptive$1 or selective$1 or runtime or (run adj time)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:02
L7	13	2 same (different near2 (power or energy))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:03
L8	6	3 with (different near2 (power or energy))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:03
L9	1049	(plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual) adj power adj domain$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:07
L10	92	9 same (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or different or first or main or master or	US-PGPUB; USPAT; EPO; JPO;	OR	OFF	2013/11/08 09:15

		primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1)) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (digital adj signal adj processor$1))	DERWENT; IBM_TDB			
L11	49	9 with (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1)) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:16
L12	1	10 same ((power or energy) near3 (allocat$4 or assign$5 or distrubut$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:17
L13	0	11 with ((power or energy) near3 (allocat$4 or assign$5 or distrubut$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:17
L14	11	10 and ((power or energy) near3 (allocat$4 or assign$5 or distrubut$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:18
L15	5	11 and ((power or energy) near3 (allocat$4 or assign$5 or distrubut$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:18
L16	2	12/029404	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:29
L17	1424	(plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual) adj power adj (domain$1 or island$1 or partition$1 or section$1 or area$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:30
L18	118	17 same ((power or energy) near3 (allocat$4 or assign$5 or distrubut$3 or	US-PGPUB; USPAT;	OR	OFF	2013/11/08 09:31

		split$3 or divid$3))	EPO; JPO; DERWENT; IBM_TDB			
L19	76	17 with ((power or energy) near3 (allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:31
L21	2	18 same (dynamic$4 or adaptive$2 or runtime or (run adj time))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:33
L22	0	19 with (dynamic$4 or adaptive$2 or runtime or (run adj time))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:33
L23	8	17 and ((power or energy) near3 (allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) near3 (dynamic$4 or adaptive$2 or runtime or (run adj time)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:39
L24	2	18 and ((power or energy) near3 (allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) near3 (dynamic$4 or adaptive$2 or runtime or (run adj time)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:40
L25	1454	(plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual) adj power adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:41
L26	0	25 same ((power or energy) near3 (allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) near3 (dynamic$4 or adaptive$2 or runtime or (run adj time)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:43
L27	8	25 and ((power or energy) near3 (allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) near3 (dynamic$4 or adaptive$2 or runtime or (run adj time)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:43
L28	3	12/662743	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:48
L29	17	11/760263	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:49
L30	122	25 same ((power or energy) near3 (allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:56
L31	80	25 with ((power or energy) near3	US-PGPUB;	OR	OFF	2013/11/08

		(allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3))	USPAT; EPO; JPO; DERWENT; IBM_TDB			09:57
L32	2	30 same (dynamic$4 or adaptive$2 or runtime or (run adj time))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:57
L33	0	31 with (dynamic$4 or adaptive$2 or runtime or (run adj time))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:57
L34	61	30 and (dynamic$4 or adaptive$2 or runtime or (run adj time))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:58
L35	32	31 and (dynamic$4 or adaptive$2 or runtime or (run adj time))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 09:58
L36	22	34 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1)) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:00
L37	13	35 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1)) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:00
L38	22	34 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or audio or media or multimedia or	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:06

		(multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1)) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (digital adj signal adj processor$1))				
L39	13	35 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1)) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:07
L40	22	34 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1)) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:10
L41	13	35 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1)) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:10
L42	1	13/069596	US-PGPUB; USPAT; EPO; JPO;	OR	OFF	2013/11/08 10:11

			DERWENT; IBM_TDB			
L43	1	12/972026	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:14
L44	2	30 same (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1)) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:19
L45	0	31 with (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1)) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:20
L46	39	30 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1)) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:20
L47	30	31 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or	US-PGPUB; USPAT; EPO; JPO; DERWENT;	OR	OFF	2013/11/08 10:21

		supplement$3 or auxiliary or graphic$2 or video or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1)) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	IBM_TDB			
L48	2	30 same (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:23
L49	0	31 with (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:24
L50	2	30 same (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:25

		multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))				
L51	0	31 with (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:25
L52	39	30 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:29
L53	30	31 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:30
L54	39	30 and (((plural$3 or multi$3 or (more	US-PGPUB;	OR	OFF	2013/11/08

		adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	USPAT; EPO; JPO; DERWENT; IBM_TDB			10:34
L55	30	31 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:34
L56	1	13/459812	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:39
L57	1	13/100358	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:40
L58	1	12/765912	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:43
L59	2	12/023916	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:45
L60	1512	(plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent) adj power adj (domain$1 or island$1 or partition$1 or section$1 or	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:51

		area$1 or segment$1 or sector$1)				
L61	15	60 same ((power or energy) near3 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) near3 (dynamic$4 or adaptive$2 or runtime or (run adj time)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:54
L62	10	60 with ((power or energy) near3 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) near3 (dynamic$4 or adaptive$2 or runtime or (run adj time)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:54
L63	15	60 same ((power or energy) near3 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) near3 (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:56
L64	10	60 with ((power or energy) near3 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) near3 (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:56
L65	13	11/041687	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 10:59
L66	52	60 same ((power or energy) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) same (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:02
L67	20	60 with ((power or energy) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) with (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:03
L68	2	66 same (budget$1 or thershold$1 or limit$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:05
L69	2	67 with (budget$1 or thershold$1 or limit$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT;	OR	OFF	2013/11/08 11:05

			IBM_TDB			
L70	9	66 and ((power or energy) adj (budget$1 or thershold$1 or limit$1 or value$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:05
L71	3	67 and ((power or energy) adj (budget$1 or thershold$1 or limit$1 or value$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:06
L72	2	11/532000	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:07
L73	1	12/751670	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:10
L74	4	12/907213	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:13
L75	53	60 same (((power or energy) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) same (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back))) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:19
L76	22	60 with (((power or energy) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) with (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back))) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:20
L77	2	75 same ((power or energy) adj (budget$1 or thershold$1 or limit$1 or value$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:20
L78	2	76 with ((power or energy) adj (budget$1 or thershold$1 or limit$1 or value$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:20
L79	9	75 and ((power or energy) adj (budget$1 or thershold$1 or limit$1 or value$1))	US-PGPUB; USPAT;	OR	OFF	2013/11/08 11:21

			EPO; JPO; DERWENT; IBM_TDB			
L80	3	76 and ((power or energy) adj (budget$1 or thershold$1 or limit$1 or value$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:21
L81	1512	(plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent) adj power adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or subdomain$1 or subsection$1 or subarea$1 or (sub adj (domain$1 or section$1 or area$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:27
L82	53	81 same (((power or energy) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) same (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back))) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:28
L83	22	81 with (((power or energy) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) with (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back))) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:29
L84	2	82 same ((power or energy) adj (budget$1 or thershold$1 or limit$1 or value$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:30
L85	2	83 with ((power or energy) adj (budget$1 or thershold$1 or limit$1 or value$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:30
L86	9	82 and ((power or energy) adj (budget$1 or thershold$1 or limit$1 or value$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:30
L87	3	83 and ((power or energy) adj (budget$1 or thershold$1 or limit$1 or value$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:30
L88	2	82 same (budget$1 or thershold$1 or limit$1)	US-PGPUB; USPAT;	OR	OFF	2013/11/08 11:31

			EPO; JPO; DERWENT; IBM_TDB			
L89	2	83 with (budget$1 or thershold$1 or limit$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:32
L90	25	81 same (((power or energy) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3)) same (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:33
L91	9	81 with (((power or energy) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3)) with (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:34
L92	1676	(plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent) adj power adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:37
L93	67	92 same (((power or energy) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) same (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back))) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:39
L94	24	92 with (((power or energy) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) with (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back))) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:39
L95	2	93 same ((power or energy) adj (budget$1 or thershold$1 or limit$1 or value$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:39
L96	2	94 with ((power or energy) adj (budget$1 or thershold$1 or limit$1 or value$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT;	OR	OFF	2013/11/08 11:40

			IBM_TDB			
L97	9	93 and ((power or energy) adj (budget$1 or thershold$1 or limit$1 or value$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:40
L98	3	94 and ((power or energy) adj (budget$1 or thershold$1 or limit$1 or value$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:40
L99	11	92 same ((power or energy) adj (budget$1 or thershold$1 or limit$1 or value$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:40
L100	6	92 with ((power or energy) adj (budget$1 or thershold$1 or limit$1 or value$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:40
L101	26	92 same (((power or energy) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3)) same (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:43
L102	9	92 with (((power or energy) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3)) with (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:43
L111	174	(US-20120079290-$ or US-20110154090-$ or US-20110072429-$ or US-20110022865-$ or US-20100332927-$ or US-20100191997-$ or US-20100146513-$ or US-20100115309-$ or US-20090313489-$ or US-20090271646-$ or US-20090235105-$ or US-20090172428-$ or US-20090172375-$ or US-20090158067-$ or US-20090158061-$ or US-20090150696-$ or US-20090150695-$ or US-20090132844-$ or US-20090070605-$ or US-20090006871-$ or US-20080250260-$ or US-20080028240-$ or US-20080005603-$ or US-20070245163-$ or US-20070239398-$ or US-20070234083-$).did. or (US-20070214342-$ or US-20070156992-$ or US-20070106827-$ or US-20070079294-$ or US-20070033425-$ or US-20070016817-$ or US-20070005995-$ or US-20060184287-$ or US-20060149975-$ or US-20060117202-$ or US-20060069936-$ or US-20060059286-$ or US-20060053326-$ or US-20060050670-$ or US-20050132238-$ or US-20050046400-$ or US-20050033881-$ or US-20050022038-$ or US-20040268166-$ or US-20040139356-$ or US-20040098560-$ or US-20040064752-$ or	US-PGPUB; USPAT; DERWENT	OR	OFF	2013/11/08 11:56

		US-20030061383-$ or US-20020194509-$ or US-20010044909-$).did. or (US-8015427-$ or US-7966511-$ or US-7797512-$ or US-7730340-$ or US-7650518-$ or US-7539885-$ or US-7529956-$ or US-7502948-$ or US-7454632-$ or US-7437270-$ or US-7434073-$ or US-7412615-$ or US-7272730-$ or US-7249268-$ or US-7194643-$ or US-7146514-$ or US-7111179-$ or US-7093147-$ or US-7043649-$ or US-7010708-$ or US-6996728-$ or US-6908227-$ or US-6829713-$ or US-6823516-$ or US-6792392-$ or US-6748546-$).did. or (US-5931950-$ or US-5621250-$ or US-5590341-$ or US-5522087-$ or US-5163153-$).did. or (WO-9016029-$ or WO-2012040052-$ or WO-2008117133-$ or WO-2007038800-$ or WO-2006029152-$ or WO-2004070594-$ or WO-2004066092-$ or WO-0227451-$ or US-7797512-$ or US-7272730-$ or US-7111179-$ or US-6823516-$ or US-6792392-$ or US-5621250-$ or US-5590341-$ or US-5522087-$ or US-4019973-$ or US-20110154090-$ or US-20110072429-$ or US-20110022865-$ or US-20100332927-$ or US-20100191997-$ or US-20100146513-$ or US-20090313489-$ or US-20090271646-$ or US-20090235105-$).did. or (US-20090172428-$ or US-20090172375-$ or US-20090158067-$ or US-20090158061-$ or US-20090150696-$ or US-20090150695-$ or US-20090132844-$ or US-20090070605-$ or US-20090006871-$ or US-20080263384-$ or US-20080250260-$ or US-20080201591-$ or US-20080028240-$ or US-20080016380-$ or US-20080005603-$ or US-20080005592-$ or US-20070245163-$ or US-20070239398-$ or US-20070234083-$ or US-20070214342-$ or US-20070156992-$ or US-20070106827-$ or US-20070033425-$ or US-20070005995-$ or US-20060288240-$ or US-20060184287-$ or US-20060149975-$).did. or (US-20060117202-$ or US-20060069936-$ or US-20060053326-$ or US-20060050670-$ or US-20060026447-$ or US-20050289365-$ or US-20050216719-$ or US-20050132238-$ or US-20050071694-$ or US-20050046400-$ or US-20050033881-$ or US-20050022038-$ or US-20040268166-$ or US-20040215987-$ or US-20040139356-$ or US-20040098631-$ or US-20040098560-$ or US-20040064752-$ or US-20040037346-$ or US-20030204759-$ or US-20030061383-$ or US-20020194509-$ or US-20020087901-$ or US-20010044909-$ or SE-7412615-$ or NL-7412615-$ or JP-2009180784-$).did.				

		or (EP-886427-$ or EP-1363180-$ or DE-2515645-$ or DE-2425579-$ or DE-1813570-$ or CS-7502948-$ or BR-7502948-$ or BE-834006-$ or BE-814753-$ or BE-771069-$).did.				
L112	2	111 and 92	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:57
L113	2	112 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 11:58
L114	1	12/263411	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 12:02
L115	2	11/707500	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 12:02
L116	0	112 and ((power or energy) adj (budget$1 or thershold$1 or limit$1 or value$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 12:06
L117	1	112 and (((power or energy) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) same (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back))) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 12:07
L118	41	111 and (((power or energy) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) same (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 12:08

		back))) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)				
L119	30	111 and (((power or energy) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) with (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back))) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 12:13
L120	7	118 and ((power or energy) adj (budget$1 or thershold$1 or limit$1 or value$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 12:13
L121	5	119 and ((power or energy) adj (budget$1 or thershold$1 or limit$1 or value$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 12:13
L122	6	120 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 12:14
L123	5	121 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 12:14

		(digital adj signal adj processor$1))				
L124	2	11/195305	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 12:21
L125	30	118 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 12:26
L126	20	119 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 12:26
L127	2	12/889121	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 12:28
L128	8	10/999786	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 12:33
L129	2	128 and 111	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 12:34
L130	8	12/198974	US-PGPUB; USPAT; EPO; JPO;	OR	OFF	2013/11/08 12:40

			DERWENT; IBM_TDB			
L131	1	130 and 111	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 12:41

EAST Search History (Interference)

<This search history is empty>

11/8/2013 12:44:11 PM
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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13225677	ANANTHAKRISHNAN ET AL.
	Examiner	**Art Unit**
	STEFAN STOYNOV	2116

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	11/07/2013								
	1	✓								
	2	✓								
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	18	✓								
	19	✓								
	20	✓								

PTO/SB/08a (01-10)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13225677
	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7434073		2008-10-07	Magklis	
	2	6792392		2004-09-14	Knight	
	3	7194643		2007-03-20	Gonzalez, et al.	
	4	7010708		2006-03-07	Ma	
	5	5621250		1997-04-15	Kim	
	6	7412615		2008-08-12	Yokota, et al.	
	7	5163153		1992-11-10	Cole, et al.	
	8	5590341		1996-12-31	Matter	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.S./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13225677
	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

	9	5931950		1999-08-03	Hsu	
	10	7454632		2008-11-18	Kardach, et al.	
	11	5522087		1996-05-28	Hsiang	
	12	7272730		2007-09-18	Acquaviva, et al.	
	13	7529956		2009-05-05	Stufflebeam	
	14	7730340		2010-06-01	Hu, et al.	
	15	7539885		2009-05-26	Ma	
	16	6748546		2004-06-08	Mirov, et al.	
	17	6829713		2004-12-07	Cooper, et al.	
	18	71111179		2006-09-19	Girson, et al.	
	19	6823516		2004-11-23	Cooper	

EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.S./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

	20	7437270		2008-10-14	Song, et al.	
	21	7093147		2006-08-15	Farkas, et al.	
	22	7043649		2006-05-09	Terrell	
	23	6996728		2006-02-07	Singh	
	24	7249268		2007-07-24	Bhandarkar	
	25	7502948		2009-03-10	Rotem, et al.	
	26	7650518		2010-01-19	Allarey, et al.	

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20090150695		2009-06-11	Song, et al.	
	2	20090150696		2009-06-11	Song, et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.S./

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	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

	3	20110154090		2011-06-23	Dixon, et al.	
	4	20070214342		2007-09-13	Newburn	
	5	20070079294		2007-04-05	Knight	
	6	20060117202		2006-06-11	Magklis, et al.	
	7	20070016817		2007-01-18	Albonesi, et al.	
	8	20060053326		2006-03-09	Naveh	
	9	20070005995		2007-01-04	Kardach, et al.	
	10	20040098560		2004-05-02	Storvik, et al.	
	11	20060050670		2006-03-09	Hillyard, et al.	
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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.S./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13225677
	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

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	15	20080028240		2008-01-31	Arai, et al.	
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	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

	25	20020194509		2002-12-19	Plante, et al.	
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	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

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	Filing Date	2011-09-06
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	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	EP 1 282 030	EP	A1	2003-02-05 ~~2003-05-02~~	Mitsubishi Kenki Kabushiki Kaisha		☐
	2	2001-202155	JP		2001-07-27	Hitachi LTD		☒
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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	U.S. Patent Application Serial No. 13/282,896, filed October 27, 2011, entitled "ENABLING A NON-CORE DOMAIN TO CONTROL MEMORY BANDWIDTH," by AVINASH N. ANANTHAKRISHNAN, et al. (2492)	☐
	2	SPEC-Power and Performance, Design Overview V1.10, Standard Performance Information Corp., October 21, 2008, 6 pages.	☐
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
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	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

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	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

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	21	U.S. Patent Application Serial No. 13/285,414, filed October 31, 2011, entitled "CONTROLLING A TURBO MODE FREQUENCY OF A PROCESSOR," by AVINASH N. ANANTHAKRISHNAN, et al. (2494)	☐
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Examiner Signature	/Stefan Stoynov/ (11/07/2013)	Date Considered	11/07/2013

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	13/282896	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 17:17
S2	1	13/070700	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 17:17
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		or independent) adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1)) adj (processor or microprocessor or cpu)).clm.	IBM_TDB			
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S39	3	S36 and S12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 17:52
S40	49288	(plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent) adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1))) same (processor or microprocessor or cpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 18:18
S41	24099	(plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent) adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1))) with (processor or microprocessor or cpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 18:19
S42	119	S40 same (((power or energy) adj budget) or ((total or global or available or allow$4 or permi$6) near2 (power or energy)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 18:21
S43	27	S41 with (((power or energy) adj budget) or ((total or global or available or allow$4 or permi$6) near2 (power or energy)))	US-PGPUB; USPAT; EPO; JPO;	OR	OFF	2013/11/08 18:21

			DERWENT; IBM_TDB			
S44	80	S42 same (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or reallocate$3 or (re adj allocate$3) or assign$5 or distrubut$3 or split$3 or divid$3 or shift$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 18:22
S45	7	S43 with (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or reallocate$3 or (re adj allocate$3) or assign$5 or distrubut$3 or split$3 or divid$3 or shift$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 18:22
S46	2	12/940273	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 18:23
S47	174	(US-20120079290-$ or US-20110154090-$ or US-20110072429-$ or US-20110022865-$ or US-20100332927-$ or US-20100191997-$ or US-20100146513-$ or US-20100115309-$ or US-20090313489-$ or US-20090271646-$ or US-20090235105-$ or US-20090172428-$ or US-20090172375-$ or US-20090158067-$ or US-20090158061-$ or US-20090150696-$ or US-20090150695-$ or US-20090132844-$ or US-20090070605-$ or US-20090006871-$ or US-20080250260-$ or US-20080028240-$ or US-20080005603-$ or US-20070245163-$ or US-20070239398-$ or US-20070234083-$).did. or (US-20070214342-$ or US-20070156992-$ or US-20070106827-$ or US-20070079294-$ or US-20070033425-$ or US-20070016817-$ or US-20070005995-$ or US-20060184287-$ or US-20060149975-$ or US-20060117202-$ or US-20060069936-$ or US-20060059286-$ or US-20060053326-$ or US-20060050670-$ or US-20050132238-$ or US-20050046400-$ or US-20050033881-$ or US-20050022038-$ or US-20040268166-$ or US-20040139356-$ or US-20040098560-$ or US-20040064752-$ or US-20030061383-$ or US-20020194509-$ or US-20010044909-$).did. or (US-8015427-$ or US-7966511-$ or US-7797512-$ or US-7730340-$ or US-7650518-$ or US-7539885-$ or US-7529956-$ or US-7502948-$ or US-7454632-$ or US-7437270-$ or US-7434073-$ or US-7412615-$ or US-7272730-$ or US-7249268-$ or US-7194643-$ or US-7146514-$ or US-7111179-$ or US-7093147-$ or US-7043649-$ or US-7010708-$ or US-6996728-$ or US-6908227-$ or US-6829713-$ or US-6823516-$ or US-6792392-$ or US-6748546-$).did. or (US-	US-PGPUB; USPAT; DERWENT	OR	OFF	2013/11/08 18:29

		5931950-$ or US-5621250-$ or US-5590341-$ or US-5522087-$ or US-5163153-$).did. or (WO-9016029-$ or WO-2012040052-$ or WO-2008117133-$ or WO-2007038800-$ or WO-2006029152-$ or WO-2004070594-$ or WO-2004066092-$ or WO-0227451-$ or US-7797512-$ or US-7272730-$ or US-7111179-$ or US-6823516-$ or US-6792392-$ or US-5621250-$ or US-5590341-$ or US-5522087-$ or US-4019973-$ or US-20110154090-$ or US-20110072429-$ or US-20110022865-$ or US-20100332927-$ or US-20100191997-$ or US-20100146513-$ or US-20090313489-$ or US-20090271646-$ or US-20090235105-$).did. or (US-20090172428-$ or US-20090172375-$ or US-20090158067-$ or US-20090158061-$ or US-20090150696-$ or US-20090150695-$ or US-20090132844-$ or US-20090070605-$ or US-20090006871-$ or US-20080263384-$ or US-20080250260-$ or US-20080201591-$ or US-20080028240-$ or US-20080016380-$ or US-20080005603-$ or US-20080005592-$ or US-20070245163-$ or US-20070239398-$ or US-20070234083-$ or US-20070214342-$ or US-20070156992-$ or US-20070106827-$ or US-20070033425-$ or US-20070005995-$ or US-20060288240-$ or US-20060184287-$ or US-20060149975-$).did. or (US-20060117202-$ or US-20060069936-$ or US-20060053326-$ or US-20060050670-$ or US-20060026447-$ or US-20050289365-$ or US-20050216719-$ or US-20050132238-$ or US-20050071694-$ or US-20050046400-$ or US-20050033881-$ or US-20050022038-$ or US-20040268166-$ or US-20040215987-$ or US-20040139356-$ or US-20040098631-$ or US-20040098560-$ or US-20040064752-$ or US-20040037346-$ or US-20030204759-$ or US-20030061383-$ or US-20020194509-$ or US-20020087901-$ or US-20010044909-$ or SE-7412615-$ or NL-7412615-$ or JP-2009180784-$).did. or (EP-886427-$ or EP-1363180-$ or DE-2515645-$ or DE-2425579-$ or DE-1813570-$ or CS-7502948-$ or BR-7502948-$ or BE-834006-$ or BE-814753-$ or BE-771069-$).did.				
S48	0	S47 and S42	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 18:30
S49	4	S47 and S40	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 18:30

S50	3	S47 and S41	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 18:30
S51	174	(US-20120079290-$ or US-20110154090-$ or US-20110072429-$ or US-20110022865-$ or US-20100332927-$ or US-20100191997-$ or US-20100146513-$ or US-20100115309-$ or US-20090313489-$ or US-20090271646-$ or US-20090235105-$ or US-20090172428-$ or US-20090172375-$ or US-20090158067-$ or US-20090158061-$ or US-20090150696-$ or US-20090150695-$ or US-20090132844-$ or US-20090070605-$ or US-20090006871-$ or US-20080250260-$ or US-20080028240-$ or US-20080005603-$ or US-20070245163-$ or US-20070239398-$ or US-20070234083-$).did. or (US-20070214342-$ or US-20070156992-$ or US-20070106827-$ or US-20070079294-$ or US-20070033425-$ or US-20070016817-$ or US-20070005995-$ or US-20060184287-$ or US-20060149975-$ or US-20060117202-$ or US-20060069936-$ or US-20060059286-$ or US-20060053326-$ or US-20060050670-$ or US-20050132238-$ or US-20050046400-$ or US-20050033881-$ or US-20050022038-$ or US-20040268166-$ or US-20040139356-$ or US-20040098560-$ or US-20040064752-$ or US-20030061383-$ or US-20020194509-$ or US-20010044909-$).did. or (US-8015427-$ or US-7966511-$ or US-7797512-$ or US-7730340-$ or US-7650518-$ or US-7539885-$ or US-7529956-$ or US-7502948-$ or US-7454632-$ or US-7437270-$ or US-7434073-$ or US-7412615-$ or US-7272730-$ or US-7249268-$ or US-7194643-$ or US-7146514-$ or US-7111179-$ or US-7093147-$ or US-7043649-$ or US-7010708-$ or US-6996728-$ or US-6908227-$ or US-6829713-$ or US-6823516-$ or US-6792392-$ or US-6748546-$).did. or (US-5931950-$ or US-5621250-$ or US-5590341-$ or US-5522087-$ or US-5163153-$).did. or (WO-9016029-$ or WO-2012040052-$ or WO-2008117133-$ or WO-2007038800-$ or WO-2006029152-$ or WO-2004070594-$ or WO-2004066092-$ or WO-0227451-$ or US-7797512-$ or US-7272730-$ or US-7111179-$ or US-6823516-$ or US-6792392-$ or US-5621250-$ or US-5590341-$ or US-5522087-$ or US-4019973-$ or US-20110154090-$ or US-20110072429-$ or US-20110022865-$ or US-20100332927-$ or US-20100191997-$ or US-20100146513-$ or US-	US-PGPUB; USPAT; DERWENT	OR	OFF	2013/11/09 13:29

		20090313489-$ or US-20090271646-$ or US-20090235105-$).did. or (US-20090172428-$ or US-20090172375-$ or US-20090158067-$ or US-20090158061-$ or US-20090150696-$ or US-20090150695-$ or US-20090132844-$ or US-20090070605-$ or US-20090006871-$ or US-20080263384-$ or US-20080250260-$ or US-20080201591-$ or US-20080028240-$ or US-20080016380-$ or US-20080005603-$ or US-20080005592-$ or US-20070245163-$ or US-20070239398-$ or US-20070234083-$ or US-20070214342-$ or US-20070156992-$ or US-20070106827-$ or US-20070033425-$ or US-20070005995-$ or US-20060288240-$ or US-20060184287-$ or US-20060149975-$).did. or (US-20060117202-$ or US-20060069936-$ or US-20060053326-$ or US-20060050670-$ or US-20060026447-$ or US-20050289365-$ or US-20050216719-$ or US-20050132238-$ or US-20050071694-$ or US-20050046400-$ or US-20050033881-$ or US-20050022038-$ or US-20040268166-$ or US-20040215987-$ or US-20040139356-$ or US-20040098631-$ or US-20040098560-$ or US-20040064752-$ or US-20040037346-$ or US-20030204759-$ or US-20030061383-$ or US-20020194509-$ or US-20020087901-$ or US-20010044909-$ or SE-7412615-$ or NL-7412615-$ or JP-2009180784-$).did. or (EP-886427-$ or EP-1363180-$ or DE-2515645-$ or DE-2425579-$ or DE-1813570-$ or CS-7502948-$ or BR-7502948-$ or BE-834006-$ or BE-814753-$ or BE-771069-$).did.				
S52	2	S51 and (shar$3 near3 (polic$3 or rule$1 or strateg$3 or procedure$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 13:34
S53	0	S51 and ((thermal or temperature or heat or power) near2 (conduct$4 or dissipat$4 or releas$3) near2 (decay$3 or deteriorat$4 or declin$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 13:44
S54	3	S51 and ((histor$4 or past or previous$2 or earlier) near3 (power or energy) near3 consum$5)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 13:46
S55	29	S51 and (workload or (work adj load))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 13:48
S56	7	S55 and (((power or energy) adj budget) or ((all or entire or total or global or available) adj (power or energy)))	US-PGPUB; USPAT; EPO; JPO;	OR	OFF	2013/11/09 13:49

			DERWENT; IBM_TDB			
S57	2	11/195305	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 13:52
S58	21	(US-20120284549-$ or US-20120116599-$ or US-20120054479-$ or US-20110271126-$ or US-20110264933-$ or US-20110161690-$ or US-20100318816-$ or US-20090201082-$ or US-20080307240-$ or US-20080186321-$ or US-20080067995-$ or US-20060156045-$ or US-20050184758-$).did. or (US-8452997-$ or US-8199157-$ or US-7812582-$ or US-7551985-$ or US-7509511-$ or US-7490254-$ or US-7257723-$ or US-7227383-$).did.	US-PGPUB; USPAT	OR	OFF	2013/11/09 14:04
S59	0	S58 and (shar$3 near3 (polic$3 or rule$1 or strateg$3 or procedure$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 14:05
S60	0	S58 and ((thermal or temperature or heat or power) near2 (conduct$4 or dissipat$4 or releas$3) near2 (decay$3 or deteriorat$4 or declin$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 14:05
S61	5	S58 and (workload or (work adj load))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 14:05
S62	3	S61 and (((power or energy) adj budget) or ((all or entire or total or global or available) adj (power or energy)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 14:05
S63	25	(US-20120284549-$ or US-20120054479-$ or US-20110276812-$ or US-20110271126-$ or US-20110264933-$ or US-20110173472-$ or US-20110161690-$ or US-20100318816-$ or US-20090256607-$ or US-20090201082-$ or US-20080307240-$ or US-20080186321-$ or US-20080067995-$ or US-20060156045-$ or US-20050184758-$).did. or (US-8452997-$ or US-8255730-$ or US-8199157-$ or US-7812582-$ or US-7551985-$ or US-7509511-$ or US-7490254-$ or US-7257723-$ or US-7227383-$ or US-7051306-$).did.	US-PGPUB; USPAT	OR	OFF	2013/11/09 14:18
S64	0	S63 and (shar$3 near3 (polic$3 or rule$1 or strateg$3 or procedure$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 14:18
S65	0	S63 and ((thermal or temperature or heat or power) near2 (conduct$4 or dissipat$4 or releas$3) near2 (decay$3 or	US-PGPUB; USPAT; EPO; JPO;	OR	OFF	2013/11/09 14:18

		deteriorat$4 or declin$3))	DERWENT; IBM_TDB			
S66	4	S63 and (workload or (work adj load))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 14:18
S67	2	S66 and (((power or energy) adj budget) or ((all or entire or total or global or available) adj (power or energy)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 14:19
S68	10	(US-20090271646-$ or US-20090204834-$ or US-20110264933-$ or US-20090201082-$ or US-20100042858-$ or US-20080136397-$).did. or (US-7659746-$ or US-8064967-$ or US-8327173-$ or US-8020017-$).did.	US-PGPUB; USPAT	OR	OFF	2013/11/09 14:19
S69	0	S68 and (shar$3 near3 (polic$3 or rule$1 or strateg$3 or procedure$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 14:19
S70	0	S68 and ((thermal or temperature or heat or power) near2 (conduct$4 or dissipat$4 or releas$3) near2 (decay$3 or deteriorat$4 or declin$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 14:19
S71	0	S68 and (workload or (work adj load))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 14:19
S72	7	(US-20110264933-$ or US-20110161690-$ or US-20030204760-$ or US-20080186321-$).did. or (US-7509511-$ or US-6920574-$ or US-8199157-$).did.	US-PGPUB; USPAT	OR	OFF	2013/11/09 14:20
S73	0	S72 and (shar$3 near3 (polic$3 or rule$1 or strateg$3 or procedure$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 14:20
S74	0	S72 and ((thermal or temperature or heat or power) near2 (conduct$4 or dissipat$4 or releas$3) near2 (decay$3 or deteriorat$4 or declin$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 14:20
S75	0	S72 and (workload or (work adj load))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/09 14:20

EAST Search History (Interference)

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	910	((power or energy) adj budget) or ((total or global or available or allow$4 or permi$6) adj (power or energy))) same ((plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent) adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:53
L2	277	((power or energy) adj budget) or ((total or global or available or allow$4 or permi$6) adj (power or energy))) with ((plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent) adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:54
L3	4	1 same (((plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent) adj core$1) or multicore or dualcore)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:55
L4	2	2 with (((plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent) adj core$1) or multicore or dualcore)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:56
L5	33	1 and (((plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent) adj core$1) or multicore or dualcore)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:56
L6	7	2 and (((plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent) adj core$1) or multicore or dualcore)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:56
L7	2	11/636425	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:59
L16	174	(US-20120079290-$ or US-20110154090-$	US-PGPUB;	OR	OFF	2013/11/08

		or US-20110072429-$ or US-20110022865-$ or US-20100332927-$ or US-20100191997-$ or US-20100146513-$ or US-20100115309-$ or US-20090313489-$ or US-20090271646-$ or US-20090235105-$ or US-20090172428-$ or US-20090172375-$ or US-20090158067-$ or US-20090158061-$ or US-20090150696-$ or US-20090150695-$ or US-20090132844-$ or US-20090070605-$ or US-20090006871-$ or US-20080250260-$ or US-20080028240-$ or US-20080005603-$ or US-20070245163-$ or US-20070239398-$ or US-20070234083-$).did. or (US-20070214342-$ or US-20070156992-$ or US-20070106827-$ or US-20070079294-$ or US-20070033425-$ or US-20070016817-$ or US-20070005995-$ or US-20060184287-$ or US-20060149975-$ or US-20060117202-$ or US-20060069936-$ or US-20060059286-$ or US-20060053326-$ or US-20060050670-$ or US-20050132238-$ or US-20050046400-$ or US-20050033881-$ or US-20050022038-$ or US-20040268166-$ or US-20040139356-$ or US-20040098560-$ or US-20040064752-$ or US-20030061383-$ or US-20020194509-$ or US-20010044909-$).did. or (US-8015427-$ or US-7966511-$ or US-7797512-$ or US-7730340-$ or US-7650518-$ or US-7539885-$ or US-7529956-$ or US-7502948-$ or US-7454632-$ or US-7437270-$ or US-7434073-$ or US-7412615-$ or US-7272730-$ or US-7249268-$ or US-7194643-$ or US-7146514-$ or US-7111179-$ or US-7093147-$ or US-7043649-$ or US-7010708-$ or US-6996728-$ or US-6908227-$ or US-6829713-$ or US-6823516-$ or US-6792392-$ or US-6748546-$).did. or (US-5931950-$ or US-5621250-$ or US-5590341-$ or US-5522087-$ or US-5163153-$).did. or (WO-9016029-$ or WO-2012040052-$ or WO-2008117133-$ or WO-2007038800-$ or WO-2006029152-$ or WO-2004070594-$ or WO-2004066092-$ or WO-0227451-$ or US-7797512-$ or US-7272730-$ or US-7111179-$ or US-6823516-$ or US-6792392-$ or US-5621250-$ or US-5590341-$ or US-5522087-$ or US-4019973-$ or US-20110154090-$ or US-20110072429-$ or US-20110022865-$ or US-20100332927-$ or US-20100191997-$ or US-20100146513-$ or US-20090313489-$ or US-20090271646-$ or US-20090235105-$).did. or (US-20090172428-$ or US-20090172375-$ or US-20090158067-$ or US-20090158061-$ or US-20090150696-$ or US-20090150695-$ or US-20090132844-$ or US-20090070605-$ or US-20090006871-$ or US-20080263384-$ or US-20080250260-$ or US-20080201591-$	USPAT; DERWENT			17:02		

		or US-20080028240-$ or US-20080016380-$ or US-20080005603-$ or US-20080005592-$ or US-20070245163-$ or US-20070239398-$ or US-20070234083-$ or US-20070214342-$ or US-20070156992-$ or US-20070106827-$ or US-20070033425-$ or US-20070005995-$ or US-20060288240-$ or US-20060184287-$ or US-20060149975-$).did. or (US-20060117202-$ or US-20060069936-$ or US-20060053326-$ or US-20060050670-$ or US-20060026447-$ or US-20050289365-$ or US-20050216719-$ or US-20050132238-$ or US-20050071694-$ or US-20050046400-$ or US-20050033881-$ or US-20050022038-$ or US-20040268166-$ or US-20040215987-$ or US-20040139356-$ or US-20040098631-$ or US-20040098560-$ or US-20040064752-$ or US-20040037346-$ or US-20030204759-$ or US-20030061383-$ or US-20020194509-$ or US-20020087901-$ or US-20010044909-$ or SE-7412615-$ or NL-7412615-$ or JP-2009180784-$).did. or (EP-886427-$ or EP-1363180-$ or DE-2515645-$ or DE-2425579-$ or DE-1813570-$ or CS-7502948-$ or BR-7502948-$ or BE-834006-$ or BE-814753-$ or BE-771069-$).did.				
L17	0	16 and 1	US-PGPUB; USPAT; DERWENT	OR	OFF	2013/11/08 17:02
S1	74	(((plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent) adj core$1) or multicore or dualcore) same (power adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1))))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:57
S2	43	(((plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent) adj core$1) or multicore or dualcore) with (power adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1))))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:58
S3	31	S1 same (((power or energy or voltage$1 or frequenc$3 or clock$1) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or reallocate$3 or (re adj allocate$3) or assign$5 or distrubut$3 or split$3 or divid$3) same (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back) or	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:59

		independent$2)) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)				
S4	4	S2 with (((power or energy or voltage$1 or frequenc$3 or clock$1) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or reallocate$3 or (re adj allocate$3) or assign$5 or distrubut$3 or split$3 or divid$3) with (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back) or independent$2)) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:59
S5	1	13/916039	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:01
S6	3	"2012086040"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:05
S7	1	12/263411	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:07
S8	1	12/029346	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:08
S9	2	S1 same (((total or global or available or allow$4 or permi$6) adj (power or energy)) or ((power or energy) adj budget))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:11
S10	2	S2 with (((total or global or available or allow$4 or permi$6) adj (power or energy)) or ((power or energy) adj budget))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:11
S11	44	S1 and (((power or energy or voltage$1 or frequenc$3 or clock$1) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or reallocate$3 or (re adj allocate$3) or assign$5 or distrubut$3 or split$3 or divid$3) with (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back) or independent$2)) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:11
S12	21	S2 and (((power or energy or voltage$1 or	US-PGPUB;	OR	OFF	2013/11/08

		frequenc$3 or clock$1) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or reallocate$3 or (re adj allocate$3) or assign$5 or distrubut$3 or split$3 or divid$3) with (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back) or independent$2)) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	USPAT; EPO; JPO; DERWENT; IBM_TDB			16:11
S13	17	S11 and (((total or global or available or allow$4 or permi$6) adj (power or energy)) or ((power or energy) adj budget))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:12
S14	4	S12 and (((total or global or available or allow$4 or permi$6) adj (power or energy)) or ((power or energy) adj budget))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:12
S15	21	S1 and (((total or global or available or allow$4 or permi$6) adj (power or energy)) or ((power or energy) adj budget))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:15
S16	8	S2 and (((total or global or available or allow$4 or permi$6) adj (power or energy)) or ((power or energy) adj budget))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:15
S17	48	((power or energy) adj budget) or ((total or global or available or allow$4 or permi$6) adj (power or energy))) same ((plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent) adj power adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:20
S18	25	((power or energy) adj budget) or ((total or global or available or allow$4 or permi$6) adj (power or energy))) with ((plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent) adj power adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:21
S19	3	S17 same (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:22

		multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))				
S20	3	S18 with (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:23
S21	20	S17 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:23
S22	10	S18 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:23

		or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))				
S23	2	12/029442	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:27
S24	2	12/029404	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:29
S25	2	12/192683	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:32
S26	174	(US-20120079290-$ or US-20110154090-$ or US-20110072429-$ or US-20110022865-$ or US-20100332927-$ or US-20100191997-$ or US-20100146513-$ or US-20100115309-$ or US-20090313489-$ or US-20090271646-$ or US-20090235105-$ or US-20090172428-$ or US-20090172375-$ or US-20090158067-$ or US-20090158061-$ or US-20090150696-$ or US-20090150695-$ or US-20090132844-$ or US-20090070605-$ or US-20090006871-$ or US-20080250260-$ or US-20080028240-$ or US-20080005603-$ or US-20070245163-$ or US-20070239398-$ or US-20070234083-$).did. or (US-20070214342-$ or US-20070156992-$ or US-20070106827-$ or US-20070079294-$ or US-20070033425-$ or US-20070016817-$ or US-20070005995-$ or US-20060184287-$ or US-20060149975-$ or US-20060117202-$ or US-20060069936-$ or US-20060059286-$ or US-20060053326-$ or US-20060050670-$ or US-20050132238-$ or US-20050046400-$ or US-20050033881-$ or US-20050022038-$ or US-20040268166-$ or US-20040139356-$ or US-20040098560-$ or US-20040064752-$ or US-20030061383-$ or US-20020194509-$ or US-20010044909-$).did. or (US-8015427-$ or US-7966511-$ or US-7797512-$ or US-7730340-$ or US-7650518-$ or US-7539885-$ or US-7529956-$ or US-7502948-$ or US-7454632-$ or US-7437270-$ or US-7434073-$ or US-7412615-$ or US-7272730-$ or US-7249268-$ or US-7194643-$ or US-7146514-$ or US-7111179-$ or US-7093147-$ or US-7043649-$ or US-7010708-$ or US-6996728-$ or US-6908227-$ or US-6829713-$ or US-6823516-$ or US-	US-PGPUB; USPAT; DERWENT	OR	OFF	2013/11/08 16:36

		6792392-$ or US-6748546-$).did. or (US-5931950-$ or US-5621250-$ or US-5590341-$ or US-5522087-$ or US-5163153-$).did. or (WO-9016029-$ or WO-2012040052-$ or WO-2008117133-$ or WO-2007038800-$ or WO-2006029152-$ or WO-2004070594-$ or WO-2004066092-$ or WO-0227451-$ or US-7797512-$ or US-7272730-$ or US-7111179-$ or US-6823516-$ or US-6792392-$ or US-5621250-$ or US-5590341-$ or US-5522087-$ or US-4019973-$ or US-20110154090-$ or US-20110072429-$ or US-20110022865-$ or US-20100332927-$ or US-20100191997-$ or US-20100146513-$ or US-20090313489-$ or US-20090271646-$ or US-20090235105-$).did. or (US-20090172428-$ or US-20090172375-$ or US-20090158067-$ or US-20090158061-$ or US-20090150696-$ or US-20090150695-$ or US-20090132844-$ or US-20090070605-$ or US-20090006871-$ or US-20080263384-$ or US-20080250260-$ or US-20080201591-$ or US-20080028240-$ or US-20080016380-$ or US-20080005603-$ or US-20080005592-$ or US-20070245163-$ or US-20070239398-$ or US-20070234083-$ or US-20070214342-$ or US-20070156992-$ or US-20070106827-$ or US-20070033425-$ or US-20070005995-$ or US-20060288240-$ or US-20060184287-$ or US-20060149975-$).did. or (US-20060117202-$ or US-20060069936-$ or US-20060053326-$ or US-20060050670-$ or US-20060026447-$ or US-20050289365-$ or US-20050216719-$ or US-20050132238-$ or US-20050071694-$ or US-20050046400-$ or US-20050033881-$ or US-20050022038-$ or US-20040268166-$ or US-20040215987-$ or US-20040139356-$ or US-20040098631-$ or US-20040098560-$ or US-20040064752-$ or US-20040037346-$ or US-20030204759-$ or US-20030061383-$ or US-20020194509-$ or US-20020087901-$ or US-20010044909-$ or SE-7412615-$ or NL-7412615-$ or JP-2009180784-$).did. or (EP-886427-$ or EP-1363180-$ or DE-2515645-$ or DE-2425579-$ or DE-1813570-$ or CS-7502948-$ or BR-7502948-$ or BE-834006-$ or BE-814753-$ or BE-771069-$).did.				
S27	1	S26 and S1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:37
S28	0	S26 and S2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:37

S29	1	S26 and S17	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:38
S30	0	S26 and S18	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 16:38

EAST Search History (Interference)

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11/8/2013 5:03:15 PM
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13225677	ANANTHAKRISHNAN ET AL.
	Examiner	Art Unit
	STEFAN STOYNOV	2116

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
713	300	11/7/13	SS
345	501	11/7/13	SS
700	286	11/7/13	SS
712	28	11/7/13	SS

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search for USPAT, US-PGPUB, EPO, JPO, DERWENT, IBM_TDB (see attached file).	11/7/13	SS
713/330, 345/501, 700/286, 712/28 text search only for USPAT, US-PGPUB, EPO, JPO, DERWENT, IBM_TDB (see attached file).	11/7/13	SS
Inventor's search.	11/7/13	SS

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1676	(plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent) adj power adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 13:39
L2	146	1 same (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 13:41
L3	75	1 with (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or ((graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 13:42
L4	73	2 same ((power or energy) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or	US-PGPUB; USPAT; EPO; JPO; DERWENT;	OR	OFF	2013/11/08 13:42

		distrubut$3 or split$3 or divid$3))	IBM_TDB			
L5	26	3 with ((power or energy) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 13:43
L6	17	4 same (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 13:44
L7	2	5 with (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 13:44
L8	2	4 same (budget$1 or thershold$1 or limit$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 13:47
L9	2	5 with (budget$1 or thershold$1 or limit$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 13:47
L10	8	4 and ((power or energy) adj (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 13:48
L11	2	5 and ((power or energy) adj (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 13:48
L12	1	13/103535	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 13:54
L13	1	12/874593	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 13:56
L14	26	2.clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 13:58
L15	24	3.clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 13:58
L16	10	14 and (((power or energy or voltage$1 or clock$1 or frequenc$3) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or	US-PGPUB; USPAT; EPO; JPO; DERWENT;	OR	OFF	2013/11/08 13:59

		allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) same (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back))) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	IBM_TDB			
L17	10	15 and (((power or energy or voltage$1 or clock$1 or frequenc$3) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) same (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back))) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 13:59
L18	5	14 and (((power or energy or voltage$1 or clock$1 or frequenc$3) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) with (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back))) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 13:59
L19	5	15 and (((power or energy or voltage$1 or clock$1 or frequenc$3) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) with (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back))) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 13:59
L20	0	18 and ((power or energy) adj (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:00
L21	51	2 and 713/3$2.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:01
L22	29	3 and 713/3$2.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:02
L23	34	21 and (((power or energy or voltage$1 or clock$1 or frequenc$3) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) same (dynamic$4 or adaptive$2 or runtime or (run adj time) or	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:02

		feedback or (feed adj back))) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)				
L24	15	22 and (((power or energy or voltage$1 or clock$1 or frequenc$3) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) same (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back))) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:02
L25	24	21 and (((power or energy or voltage$1 or clock$1 or frequenc$3) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) with (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back))) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:02
L26	5	22 and (((power or energy or voltage$1 or clock$1 or frequenc$3) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) with (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back))) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:03
L27	2	26 and ((power or energy) adj (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:03
L28	6	25 and ((power or energy) adj (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:03
L29	5	24 and ((power or energy) adj (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:04
L30	9	23 and ((power or energy) adj (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:04
L31	4	2 and "345".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT;	OR	OFF	2013/11/08 14:07

			IBM_TDB			
L32	0	3 and "345".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:07
L33	2	2 and "700".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:09
L34	1	3 and "700".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:09
L35	2	2 and "712".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:10
L36	2	3 and "712".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:10
L37	65	2 and (((power or energy or voltage$1 or clock$1 or frequenc$3) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) same (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back))) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:10
L38	26	3 and (((power or energy or voltage$1 or clock$1 or frequenc$3) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) same (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back))) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:11
L39	9	37 and ((power or energy) adj (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:11
L40	5	38 and ((power or energy) adj (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:11
L41	44	2 and (((power or energy or voltage$1 or clock$1 or frequenc$3) near5 (control$4 or	US-PGPUB; USPAT;	OR	OFF	2013/11/08 14:11

		manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) with (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back))) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	EPO; JPO; DERWENT; IBM_TDB			
L42	14	3 and (((power or energy or voltage$1 or clock$1 or frequenc$3) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) with (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back))) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:12
L43	34	2 same (((power or energy or voltage$1 or clock$1 or frequenc$3) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) same (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back) or independent$2)) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:17
L44	3	3 with (((power or energy or voltage$1 or clock$1 or frequenc$3) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or assign$5 or distrubut$3 or split$3 or divid$3) with (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back) or independent$2)) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:18
L45	218	1 same (((power or energy or voltage$1 or clock$1 or frequenc$3) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or reallocat$3 or (re adj allocat$3) or assign$5 or distrubut$3 or split$3 or divid$3) same (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back) or independent$2)) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:21
L46	109	1 with (((power or energy or voltage$1 or clock$1 or frequenc$3) near5 (control$4 or manag$5 or adjust$5 or regulat$4 or chang$3 or modif$8 or alter$3 or vary$3 or allocat$4 or reallocat$3 or (re adj	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:22

		allocat$3) or assign$5 or distrubut$3 or split$3 or divid$3) with (dynamic$4 or adaptive$2 or runtime or (run adj time) or feedback or (feed adj back) or independent$2)) or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)				
L47	5	45 same (budget$1 or thershold$1 or limit$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:23
L48	2	46 with (budget$1 or thershold$1 or limit$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:23
L49	45	45.clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:24
L50	30	46.clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:24
L51	24	49 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:24
L52	15	50 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:25

		multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))				
L53	1	51 and ((power or energy) adj (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:25
L54	0	52 and ((power or energy) adj (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:25
L55	33	10/840893	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:27
L56	3	12/662743	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:29
L57	1	49 and ((power or energy) adj (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:31
L58	0	50 and ((power or energy) adj (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:31
L59	73	45 and 713/3$2.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:31
L60	38	46 and 713/3$2.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:31
L61	53	59 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:31

		(graphic$2 adj engine$1) or (digital adj signal adj processor$1))				
L62	27	60 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:32
L63	7	61 and ((power or energy) adj (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:32
L64	6	62 and ((power or energy) adj (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:32
L65	7	59 and ((power or energy) adj (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:35
L66	6	60 and ((power or energy) adj (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:35
L67	1	45 and "345".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:36
L68	0	46 and "345".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:36
L69	6	45 and "700".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:36
L70	5	46 and "700".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:36

L71	4	69 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:36
L72	4	70 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:37
L73	0	71 and ((power or energy) adj (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:37
L74	1	69 and ((power or energy) adj (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:37
L75	1	70 and ((power or energy) adj (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:38
L76	6	45 and "712".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:38
L77	6	46 and "712".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT;	OR	OFF	2013/11/08 14:38

			IBM_TDB			
L78	6	76 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:38
L79	6	77 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:38
L80	0	78 and ((power or energy) adj (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:39
L81	0	76 and ((power or energy) adj (budget$1 or thershold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:39
L82	34	45 same (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:42

		system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))				
L83	3	46 with (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:42
L84	6	82 and ((total or global or allow$4 or permi$6) adj (power or energy))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:45
L85	2	83 and ((total or global or allow$4 or permi$6) adj (power or energy))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:45
L86	9	45 same ((total or global or allow$4 or permi$6) adj (power or energy))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:47
L87	1	46 with ((total or global or allow$4 or permi$6) adj (power or energy))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:47
L88	2	12/101028	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 14:50

EAST Search History (Interference)

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11/8/2013 2:55:06 PM
C:\Users\sstoynov1\Documents\EAST\Workspaces\13225677_3.wsp

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	14596	(allocat$4 or reallocate$3 or (re adj allocate$3) or assign$5 or distrubut$3 or split$3 or divid$3) same (((total or global or available or allow$4 or permi$6) adj (power or energy)) or ((power or energy) adj budget))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:03
L2	7359	(allocat$4 or reallocate$3 or (re adj allocate$3) or assign$5 or distrubut$3 or split$3 or divid$3) with (((total or global or available or allow$4 or permi$6) adj (power or energy)) or ((power or energy) adj budget))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:04
L3	14	1 same (plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent or each) adj power adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:05
L4	9	2 with (plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent or each) adj power adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:06
L5	1	12/765912	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:08
L6	236	(allocat$4 or reallocate$3 or (re adj allocate$3) or assign$5 or distrubut$3 or split$3 or divid$3) same (power or energy) same (plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent or each) adj power adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:11

L7	145	(allocat$4 or reallocate$3 or (re adj allocate$3) or assign$5 or distrubut$3 or split$3 or divid$3) with (power or energy) with (plural$3 or multi$3 or (more adj2 one) or two or dual or several or separate or different or first or second or individual or independent or each) adj power adj (domain$1 or island$1 or partition$1 or section$1 or area$1 or segment$1 or sector$1 or block$1 or subdomain$1 or subsection$1 or subarea$1 or subblock$1 or (sub adj (domain$1 or section$1 or area$1 or block$1)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:12
L8	51	6 same (dynamic$4 or adaptive$2 or runtime or (run adj time) or independent$2 or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:15
L9	26	7 with (dynamic$4 or adaptive$2 or runtime or (run adj time) or independent$2 or (dynamic adj voltage adj frequency adj scaling) or (dynamic adj frequency adj voltage adj scaling) or DVFS or DFVS)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:15
L10	21	8 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:15
L11	6	9 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:16

L12	16	8 same (processor$1 or microprocessor$1 or cpu$1 or core$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:19
L13	4	9 with (processor$1 or microprocessor$1 or cpu$1 or core$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:19
L14	12	6 same (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:23
L15	2	7 with (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:23
L16	65	6 same (processor$1 or microprocessor$1 or cpu$1 or core$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:24
L17	14	7 with (processor$1 or microprocessor$1 or cpu$1 or core$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:24
L18	1	12/972026	US-PGPUB; USPAT; EPO; JPO; DERWENT;	OR	OFF	2013/11/08 15:25

			IBM_TDB			
L19	11	10/135116	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:27
L20	31	6.clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:32
L21	22	7.clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:32
L22	10	20 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:32
L23	8	21 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:33
L24	48	6 and 713/3$2.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:34
L25	22	7 and 713/3$2.ccls.	US-PGPUB; USPAT; EPO; JPO;	OR	OFF	2013/11/08 15:34

			DERWENT; IBM_TDB			
L26	21	24 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:34
L27	18	25 and (((plural$3 or multi$3 or (more adj2 one) or two or several or separate or individual or different or first or main or master or primary or second$3 or slave or supplement$3 or auxiliary or graphic$2 or video or image or audio or media or multimedia or (multi adj media) or dual or ((high or increased or low or decreased) adj (power or energy or speed or consumption or processing or execution or performance)) or fast or slow$2) adj (processor$1 or microprocessor$1 or cpu$1 or core$1 or subsystem$1 or (sub adj system$1) or ((functional or execut$3) adj unit$1))) or multiprocessor or multicpu or multicore or dualcore or GPU$1 or DSP$1 or (graphic$2 adj processing adj unit$1) or (graphic$2 adj engine$1) or (digital adj signal adj processor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:34
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L29	2	7 and "345".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:36
L30	7	6 and "700".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:37
L31	2	7 and "700".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:37
L32	2	6 and "712".clas.	US-PGPUB; USPAT;	OR	OFF	2013/11/08 15:37

			EPO; JPO; DERWENT; IBM_TDB			
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		20110072429-$ or US-20110022865-$ or US-20100332927-$ or US-20100191997-$ or US-20100146513-$ or US-20090313489-$ or US-20090271646-$ or US-20090235105-$).did. or (US-20090172428-$ or US-20090172375-$ or US-20090158067-$ or US-20090158061-$ or US-20090150696-$ or US-20090150695-$ or US-20090132844-$ or US-20090070605-$ or US-20090006871-$ or US-20080263384-$ or US-20080250260-$ or US-20080201591-$ or US-20080028240-$ or US-20080016380-$ or US-20080005603-$ or US-20080005592-$ or US-20070245163-$ or US-20070239398-$ or US-20070234083-$ or US-20070214342-$ or US-20070156992-$ or US-20070106827-$ or US-20070033425-$ or US-20070005995-$ or US-20060288240-$ or US-20060184287-$ or US-20060149975-$).did. or (US-20060117202-$ or US-20060069936-$ or US-20060053326-$ or US-20060050670-$ or US-20060026447-$ or US-20050289365-$ or US-20050216719-$ or US-20050132238-$ or US-20050071694-$ or US-20050046400-$ or US-20050033881-$ or US-20050022038-$ or US-20040268166-$ or US-20040215987-$ or US-20040139356-$ or US-20040098631-$ or US-20040098560-$ or US-20040064752-$ or US-20040037346-$ or US-20030204759-$ or US-20030061383-$ or US-20020194509-$ or US-20020087901-$ or US-20010044909-$ or SE-7412615-$ or NL-7412615-$ or JP-2009180784-$).did. or (EP-886427-$ or EP-1363180-$ or DE-2515645-$ or DE-2425579-$ or DE-1813570-$ or CS-7502948-$ or BR-7502948-$ or BE-834006-$ or BE-814753-$ or BE-771069-$).did.				
L43	0	42 and 6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:39
L44	4	42 and 1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:39
L45	3	42 and 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/08 15:39

EAST Search History (Interference)

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11/8/2013 3:43:02 PM

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PTO/SB/08a (01-10)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13225677
	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7966511		2011-06-21	Naveh, et al.	
	2	7434073		2008-10-07	Magklis, et al.	
If you wish to add additional U.S. Patent citation information please click the Add button.						

U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					
If you wish to add additional U.S. Published Application citation information please click the Add button.						

FOREIGN PATENT DOCUMENTS								
Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐
If you wish to add additional Foreign Patent Document citation information please click the Add button								

NON-PATENT LITERATURE DOCUMENTS

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)		
	Application Number	13225677
	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	INTERNATIONAL SEARCHING AUTHORITY, "Notification of Transmittal of the International Search Report and the Written Opinion of the International Searching Authority," mailed March 14, 2013, in International application no. PCT/US2012/053726.	☐

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Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)		
	Application Number	13225677
	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Mark J. Rozman/	Date (YYYY-MM-DD)	2013-05-22
Name/Print	Mark J. Rozman	Registration Number	42,117

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:

ROZMAN MARK J.

TROP, PRUNER & HU, P.C. 1616 S. VOSS RD. STE. 750
HOUSTON TX 77057-2631 USA

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Applicant's or agent's file reference P38410PCT IR. 249500	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. **PCT/US2012/053726**	International filing date *(day/month/year)* **05 SEPTEMBER 2012 (05.09.2012)**
Applicant **INTEL CORPORATION et al**	

Date of mailing *(day/month/year)* 14 MARCH 2013 (14.03.2013)

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

Filing of amendments and statement under Article 19:

The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70

For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 . 9.011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. Following the expiration of 30 months from the priority date, these comments will also be made available to the public.

Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90bis.1 and 90bis.3).

Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19months.

For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the PCT Applicant's Guide, National Chapters.

Name and mailing address of the ISA/KR Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Authorized officer COMMISSIONER Telephone No. 82-42-481-8753

Form PCT/ISA/220 (July 2010)

* Attention

Copies of the documents cited in the international search report can be searched in the following Korean Intellectual Property Office English website for three months from the date of mailing of the international search report.

http://www.kipo.go.kr/en/ => PCT Services => PCT Services

ID : PCT international application number
PW : **G4NKSXSX**

Inquiries related to PCT International Search Report or Written Opinion prepared by KIPO as an International Searching Authority can be answered not only by KIPO but also through IPKC (Intellectual Property Korea Center), located in Vienna, VA, which functions as a PCT Help Desk for PCT applicants.

Homepage: http://www.ipkcenter.com
Email: ipkc@ipkcenter.com
Phone: +1 703 388 1066
Fax: +1 703 388 1084

Notes to Form PCT/ISA/220 (July 2010)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
P38410PCT		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US2012/053726	**05 SEPTEMBER 2012 (05.09.2012)**	06 SEPTEMBER 2011 (06.09.2011)

Applicant

INTEL CORPORATION et al

This International search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

☒ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of:
      ☒ the international application in the language in which it was filed
      ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.
2. ☐ **Certain claims were found unsearchable** (See Box No. II)
3. ☐ **Unity of invention is lacking** (See Box No. III)
4. With regard to the **title**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:
5. With regard to the **abstract**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.
6. With regard to the drawings,
   a. the figure of the **drawings** to be published with the abstract is Figure No. 6
      ☐ as suggested by the applicant.
      ☒ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figure is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/053726

A. CLASSIFICATION OF SUBJECT MATTER

G06F 1/00(2006.01)i, G06F 1/26(2006.01)i, G06F 13/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 1/26; G06F 1/00; G06F 9/00; G06F 1/26; G01R 31/3177; G06F 11/25

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: multiple domain system, core area and uncore area, power control unit, multiple cores, dynamic allocation power budget and similar terms.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US20090313489 A1 (GUNTHER STEPHEN H. et al.) 17 December 2009 See paragraphs [0016]-[0020], [0022]-[0031], [0033]-[0034];	1,9,15
A	claim 1 and figures 1-6.	2-8,10-14,16-20
A	US7966511 B2 (NAVEH ALON et al.) 21 June 2011 See column 2, line 33-45; column 4, line 27 - column 5, line 10; column 6, line 25-50; claims 1-2 and figure 1.	1-20
A	US7434073 B2 (MAGKLIS GRIGORIOS et al.) 07 October 2008 See column 1, line 42-62; column 2, line 19 - column 3, line 21; column 4, line 8-58; claim 1 and figures 1-3.	1-20
A	US20100332927 A1 (KURTS TSVIKA et al.) 30 December 2010 See paragraphs [0014]-[0016], [0022], [0037]-[0039]; claim 1 and figure 4	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 MARCH 2013 (13.03.2013)	**14 MARCH 2013 (14.03.2013)**
Name and mailing address of the ISA/KR Facsimile No. 82-42-472-7140	Authorized officer AHN, Jeong Hwan Telephone No. 82-42-481-5741

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2012/053726

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US20090313489 A1	17.12.2009	CN 101403944 A	08.04.2009
		DE 102007051841 A1	21.05.2008
		GB 0721314 D0	12.12.2007
		GB 2444597 A	11.06.2008
		JP 2008-117397 A	22.05.2008
		KR 10-0988396 B1	18.10.2010
		KR 10-2010-0075806 A	05.07.2010
		US 2008-0104425 A1	01.05.2008
		US 2011-0022865 A1	27.01.2011
		US 2011-191607 A1	04.08.2011
		US 7949887 B2	24.05.2011
		US 8069358 B2	29.11.2011
US7966511 B2	21.06.2011	CN 1993669 A	04.07.2007
		DE 112005001779 T5	24.05.2007
		JP 2008-507766 A	13.03.2008
		JP 2012-069115 A	05.04.2012
		US 2006-0026447 A1	02.02.2006
		US 2011-252267 A1	13.10.2011
		WO 2006-019973 A1	23.02.2006
US7434073 B2	07.10.2008	CN 100593155 C	03.03.2010
		DE 112005002416 B4	30.04.2009
		GB 0705111 D0	25.04.2007
		GB 0705676 D0	02.05.2007
		GB 2432939 A	06.06.2007
		JP 04-860624 B2	11.11.2011
		JP 2008-515065 A	08.05.2008
		JP 2008-515065 T	08.05.2008
		JP 2012-009061 A	12.01.2012
		JP 4860624 B2	25.01.2012
		US 2006-0117202 A1	01.06.2006
		US 2008-0263376 A1	23.10.2008
		WO 2006-057865 A3	01.06.2006
US20100332927 A1	30.12.2010	US 8074131 B2	06.12.2011

MediaTek Exhibit 1002, Page 227 of 398

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
ROZMAN MARK J.

TROP, PRUNER & HU, P.C. 1616 S. VOSS RD. STE. 750
HOUSTON TX 77057-2631 USA

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing *(day/month/year)*	**14 MARCH 2013 (14.03.2013)**
Applicant's or agent's file reference P38410PCT	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2012/053726	**05 SEPTEMBER 2012 (05.09.2012)**	06 SEPTEMBER 2011 (06.09.2011)

International Patent Classification (IPC) or both national classification and IPC

G06F 1/00(2006.01)i, G06F 1/26(2006.01)i, G06F 13/00(2006.01)i

Applicant

INTEL CORPORATION et al

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.
For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR	Date of completion of this opinion	Authorized officer
Facsimile No. 82-42-472-7140	13 MARCH 2013 (13.03.2013)	AHN, Jeong Hwan Telephone No.82-42-481-5741

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2012/053726

Box No. 1 Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of :

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into _____ , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

   a. a sequence listing filed or furnished
      ☐ on paper
      ☐ in electronic form

   b. time of filing or furnishing
      ☐ contained in the international application as filed.
      ☐ filed together with the international application in electronic form.
      ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additioanl copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2012/053726

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	2-8, 10-14, 16-20	YES
	Claims	1, 9, 15	NO
Inventive step (IS)	Claims	2-8, 10-14, 16-20	YES
	Claims	1, 9, 15	NO
Industrial applicability (IA)	Claims	1-20	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: US 2009-0313489 A1 (STEPHEN H. GUNTHER et al.) 17 December 2009

D2: US 7966511 B2 (ALON NAVEH et al.) 21 June 2011

D3: US 7434073 B2 (GRIGORIOS MAGKLIS et al.) 7 October 2008

D4: US 2010-0332927 A1 (TSVIKA KURTS et al.) 30 December 2010

1. Novelty and Inventive Step

1.1 Independent Claims

1.1.1 Independent Claim 1

The document D1, which is considered to represent the most relevant state of the art, discloses (the references in parentheses applying to this document): an apparatus comprising;

- a multi-domain processor including a first domain and a second domain, each of the first and second domains to operate at an independent voltage and frequency, the multi-domain processor further including a first logic to dynamically allocate a power budget for the multi-domain processor between the first and second domains at run time; (a power control logic or some other detection logic detecting other condition or some combination of conditions in order to indicate a control logic whether to place the corresponding core or un-core logic into a different power state. See paragraph [0026]).

(Continued on the supplemental Box)

MediaTek Exhibit 1002, Page 230 of 398

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of:

Box V.

As all of the features of claim 1 are disclosed in D1, this claim 1 is anticipated by D1. Therefore, claim 1 lacks novelty under PCT Article 33(2).

1.1.2 Independent Claim 9
The document D1, which is considered to represent the most relevant state of the art, discloses (the references in parentheses applying to this document): a method comprising;

- determining, in a power controller of a multi-domain processor, a power budget for the multi-domain processor for a current time interval, the multi-domain processor including at least a first domain and a second domain; (adjusting a clock frequency of one or both of the first and second processor cores based on a workload of at least one of the first and second processing cores. See paragraphs [0016]-[0020], [0022]-[0031], [0033]-[0034], claim 1, and figures 1-6 in D1.)
- determining, in the power controller, a portion of the power budget to be allocated to the first and second domains; (placing, at a power control logic, a different power state into core or un-core. See paragraphs [0016]-[0020], [0022]-[0031], [0033]-[0034], claim 1, and figures 1-6 in D1.)
- and controlling a frequency of the first domain and a frequency of the second domain based on the allocated portions (controlling one or more power circuits to reduce or increase the operating voltage of one or more portions of the core. See paragraphs [0016]-[0020], [0022]-[0031], [0033]-[0034], claim 1, and figures 1-6.)

As all of the features of claim 9 are disclosed in D1, this claim 9 is anticipated by D1. Therefore, claim 9 lacks novelty under PCT Article 33(2).

(Continued on the Next Page)

MediaTek Exhibit 1002, Page 231 of 398

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of:

Previous Page

1.1.3 Independent Claim 15

The document D1, which is considered to represent the most relevant state of the art, discloses (the references in parentheses applying to this document): a system comprising;

- a multi-core processor having a first domain including a plurality of cores; (processing cores within the same die. See paragraph [0020], and figure 1 in D1.)
- a second domain including a graphics engine; (an un-core logic including circuits to perform other functions besides those performed by the core, such as memory interface functions, digital signal processing functions and graphics functions. See paragraph [0025] in D1.)
- a third domain including system agent circuitry, the third domain to operate at a fixed power budget and to dynamically allocate a variable power budget between the first and second domains; (a power control logic placing a core or un-core logic, and corresponding outputs, into one of the power states illustrated in Table 1. See paragraph [0026].)
- and a dynamic random access memory (DRAM) coupled to the multi-core processor (a main memory implemented in various memory sources, such as dynamic random-access memory (DRAM). See paragraph [0031].)

As all of the features of claim 15 are disclosed in D1, this claim 15 is anticipated by D1. Therefore, claim 15 lacks novelty under PCT Article 33(2).

(Continued on the Next Page)

MediaTek Exhibit 1002, Page 232 of 398

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of:

Previous Page

1.2 Dependent Claims

1.2.1 Dependent Claims 2-8

The additional features of claims 2-8 depending on claim 1 are not disclosed in any of the prior art documents, nor are they obvious to a person skilled by the documents, taken alone or in combination. Accordingly, claims 2-8 are novel and involve an inventive step under PCT Article 33(2) and (3).

1.2.2 Dependent Claims 10-14

The additional features of claims 10-14 depending on claim 9 are not disclosed in any of the prior art documents, nor are they obvious to a person skilled by the documents, taken alone or in combination. Accordingly, claims 10-14 are novel and involve an inventive step under PCT Article 33(2) and (3).

1.2.3 Dependent Claims 16-20

The additional features of claims 16-20 depending on claim 15 are not disclosed in any of the prior art documents, nor are they obvious to a person skilled by the documents, taken alone or in combination. Accordingly, claims 16-20 are novel and involve an inventive step under PCT Article 33(2) and (3).

2. Industrial Applicability

Claims 1-20 have industrial applicability and meet the requirement of PCT Article 33(4).

MediaTek Exhibit 1002, Page 233 of 398

(19) 대한민국특허청(KR)
(12) 공개특허공보(A)

(51) Int. Cl.
G06F 1/28

(11) 공개번호 10-2006-0128469
(43) 공개일자 2006년12월14일

(21) 출원번호	10-2005-0049957
(22) 출원일자	2005년06월10일
(71) 출원인	엘지전자 주식회사 서울특별시 영등포구 여의도동 20번지
(72) 발명자	오장근 경기도 수원시 권선구 권선동 신우아파트 708-1105
(74) 대리인	특허법인우린

심사청구 : 없음

(54) 멀티-코어 프로세서의 전원 제어 장치 및 방법

요약

본 발명은 멀티-코어 프로세서의 전원 제어 장치 및 방법에 관한 것으로, 본 발명은 두 개 이상의 코어를 구비하는 프로세서 및 상기 프로세서 내의 각각의 코어에 연결되어, 각 코어의 사용량에 따라 각 코어에 대한 공급전압을 독립적으로 조절하는 복수의 전원변환부를 포함하는 것을 특징으로 하는 멀티-코어 프로세서의 전원 제어 장치 및 방법에 관계한다. 본 발명의 멀티-코어 프로세서의 전원 제어 장치 및 방법은 누설 전류에 의한 불필요한 전력 낭비를 최소화하고 프로세서의 성능을 최적의 상태로 제어할 수 있는 효과를 제공한다.

대표도

도2

색인어

멀티-코어 프로세서, CPU, 사용량, 전압 ID(VID), 전원변환부, PLL, PMU

명세서

도면의 간단한 설명

도 1은 종래 기술에 의한 멀티-코어 프로세서의 전원 제어장치의 기능블록도,

도 2는 본 발명의 일실시예에 의한 멀티-코어 프로세서의 전원제어장치의 기능블록도,

도 3은 본 발명에 의한 멀티-코어 프로세서의 전원 제어 방법을 나타낸 흐름도,

도 4는 본 발명의 일실시예에 의한 멀티-코어 프로세서의 전원 제어 방법의 상세 흐름도이다.

도면의 주요 부분에 대한 부호의 설명

101 : DC/DC 컨트롤러	102, 102' : DC/DC 컨버터
103 : 제 1 코어	103' : 제 2 코어
105 : 프로세서	
303 : 운영체제 (OS)	350 : 프로세서
300 : 제 1 전원변환부	301 : 제 2 전원변환부

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310 : 제 1 코어 320 : 제 2 코어

313, 323 : PLL 340 : 클락발생기

330 : PMU (Power Management Unit)

발명의 상세한 설명

발명의 목적

발명이 속하는 기술분야 및 그 분야의 종래기술

본 발명은 멀티-코어 프로세서의 전원 제어 장치 및 방법에 관한 것으로, 더욱 상세하게는 복수의 코어를 구비하는 프로세서에서 각 코어의 사용량에 따라 각 코어에 대한 공급전압을 독립적으로 조절할 수 있는 멀티-코어 프로세서의 전원 제어 장치 및 방법에 관계한다.

오늘날 고속 프로세서에 대한 요구가 증가하고 있기 때문에 프로세서는 싱글 코어 프로세서에서 멀티-코어 프로세서(multi-core processor)로 진화하고 있다. 멀티-코어 프로세서는 하나의 프로세서 내에 복수의 코어를 구비하는 것으로, 작업을 복수의 코어들이 분담하여 처리하므로 처리 성능을 향상시킬 수 있다. 또한 여러 개의 프로세서들을 부가하여 사용하는 것에 비해 코어 이외의 부분을 공용할 수 있기 때문에 제조 비용이 저렴하고 크기를 소형화할 수 있는 이점을 가진다.

이러한 멀티-코어 프로세서는 복수의 코어들이 동작되므로 싱글-코어 프로세서에 비해 전력 소모가 증가될 것으로 예상된다. 전력 소모의 증가는 휴대용 컴퓨터의 경우 배터리의 연속 동작 시간을 단축시키고, 고정형 시스템에서도 발열로 인해 프로세서의 수명을 단축시키고 기능을 열화시킬 수 있다. 따라서 멀티-코어 프로세서의 전력 소모를 줄이기 위한 기술의 개발이 요구되고 있다.

종래 기술에 의한 멀티-코어 프로세서의 일례를 도 1에 도시하였다. 도 1에 도시된 바와 같이, 기존의 프로세서(105)는 제 1 코어(103) 및 제 2 코어(103'), 배터리 등으로부터 입력 받은 전원을 코어가 사용하는 전압에 맞게 변환하는 복수의 DC/DC 컨버터(102, 102') 및 DC/DC 컨버터를 제어하여 각각의 코어에 대한 전압 인가를 제어하는 DC/DC 컨트롤러(101)를 포함하여 구성된다.

이러한 기존의 멀티-코어 프로세서에서는 DC/DC 컨버터의 갯수에 관계 없이 모든 DC/DC 컨버터의 출력이 하나로 프로세서에 입력되어 각 코어에 대한 전압 인가를 개별적으로 제어할 수 없다. 예를 들어 제 2 코어(103')가 사용되지 않는 경우에도 제 1 코어(103)가 고속으로 동작하고 있다면 제 1 코어(103)와 동일한 전압이 제 2 코어(103')에 인가되므로, 불필요한 누설 전류가 발생되어 제한된 용량의 배터리 전원이 비효율적으로 낭비되는 문제점이 발생할 수 있다.

한편, 프로세서의 저전력 프로세서 관련 기술로서 사용자가 자기의 환경에 맞게 선택할 수 있는 여러 가지 CPU 전원 관리 모드를 지원하고, 각 모드에 따라 프로세서의 공급전압과 코어 주파수를 동적으로 조절함으로써 전원 소비를 줄이는 기술이 제안되었다.

이러한 기술에서 각 코어는 고주파 모드 (High Frequency Mode)와 저주파 모드 (Low Frequency Mode) 사이의 여러 단계의 동작 속도 모드를 가진다. 이 때 각 코어의 공급 전압은 모드에 따라 달라지는데, 고주파 모드에서는 높은 전압을 저주파 모드에서는 낮은 전압을 인가한다.

그러나 이러한 기술을 멀티-코어 프로세서에 적용하는 경우에도 하나의 VID만을 사용한다. 제 1 코어가 고주파 모드(High Frequency Mode)로 동작하다가 저주파 모드(Low Frequency Mode)로 진입했음에도 불구하고, 제 2 코어가 업무를 수행하고 있다면, 제 1 코어는 여전히 고주파 모드의 전압을 인가 받게 되므로 제 1 코어에서 많은 누설 전력이 발생한다. 이러한 종래 기술에서도 각 코어에 대해서 독립적으로 공급전압을 제어하는 것이 불가능하므로, 불필요한 누설 전력의 낭비가 발생하는 문제점이 발생한다.

발명이 이루고자 하는 기술적 과제

본 발명은 상술한 종래 기술의 문제점을 극복하기 위해 안출된 것으로, 본 발명의 하나의 목적은 불필요한 누설 전류에 의한 전력 낭비를 방지할 수 있고, 프로세서의 성능을 최적의 상태로 관리할 수 있는 멀티-코어 프로세서의 전원 제어 장치 및 방법을 제공하는 것이다.

본 발명의 다른 목적은 두 개 이상의 코어를 포함하는 프로세서에서 각 코어의 사용량에 따라 지능적으로 전력을 분배함으로써, 각 코어에 발생하는 전력 소모를 최소화할 수 있는 전원 제어 장치 및 방법을 제공하는 것이다.

본 발명의 또 다른 목적은 멀티-코어 프로세서 내의 각 코어에 대한 공급전압을 소프트웨어적으로 제어할 수 있는 멀티-코어 프로세서의 전원 제어 장치 및 방법을 제공하는 것이다.

발명의 구성 및 작용

상술한 목적을 달성하기 위한 본 발명의 하나의 양상은

두 개 이상의 코어를 구비하는 프로세서; 및

상기 프로세서 내의 각각의 코어에 연결되어, 각 코어의 사용량에 따라 각 코어에 대한 공급전압을 독립적으로 조절하는 복수의 전원변환부를 포함하는 것을 특징으로 하는 멀티-코어 프로세서의 전원 제어 장치를

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특징으로 한다.

상기 전원변환부는 각 코어로부터 서로 상이한 전압 ID(Voltage Identification Signal; 이하에서 "VID"라 한다)를 수신하고, 각각의 VID에 따라 각 코어에 맞는 공급전압을 독립적으로 인가한다. 본 발명에서 각 코어의 사용량은 각 코어의 점유율 또는 스레드니스 (threadness)에 의해 판단될 수 있다.

상술한 목적을 달성하기 위한 본 발명의 다른 양상에 의한 멀티-코어 프로세서의 전원 제어 장치는

두 개 이상의 코어를 구비하는 프로세서; 및

상기 프로세서 내의 각각의 코어에 연결되어 각 코어에 대한 공급전압을 독립적으로 조절하는 복수의 전원변환부를 포함하고,

상기 프로세서는 동작 속도가 상이한 여러 가지 모드로 동작하고, 각각의 동작 모드에 맞는 VID를 생성하여 전원변환부로 전송하고,

상기 전원변환부는 상기 프로세서내의 각각의 코어로부터 독립적으로 VID를 수신하여, 수신한 VID에 따라 각 코어에 대한 공급전압을 독립적으로 조절하는 것을 특징으로 한다.

상술한 목적을 달성하기 위한 본 발명의 또 다른 양상에 의한 멀티-코어 프로세서의 전원 제어 방법은

각 코어의 사용량에 대한 정보를 수득하는 단계 ; 및

각 코어의 사용량에 기초하여 공급전압 조정의 필요성이 있는지 판단하는 단계; 및

공급전압 조정이 필요한 하나 이상의 코어의 공급전압을 해당 코어의 사용량에 따라 독립적으로 조절하는 단계를 포함하는 것을 특징으로 한다.

상기 코어의 사용량 판단 단계에서는 코어의 사용량을 코어의 점유율 또는 스레드니스에 의해 평가한다. 상기 전압 조절 단계는 각 코어로부터 서로 상이한VID를 수신하고, 각각의 VID에 따라 상이한 전압을 각 코어에 공급한다.

본 발명의 방법에서는 각 코어의 사용량에 따라 각 코어에 대한 공급전압과 함께 각 코어의 주파수도 함께 조정하는 것이 바람직하다.

이하에서 첨부 도면을 참고하여 본 발명에 관하여 더욱 상세하게 설명한다.

본 발명에서 "멀티-코어 프로세서"란 하나의 칩에 두 개 이상의 복수의 프로세싱 코어가 포함되어 있는 데이터 처리 능력이 있는 시스템이나 장치를 의미한다. 이러한 멀티-코어 프로세서는 전형적으로는 컴퓨터의 중앙처리장치를 의미하나, 보조처리기, 입출력처리기 등과 같은 프로세서도 모두 포함할 수 있다.

본 발명의 멀티-코어 프로세서의 전원 제어 장치는 각 코어의 사용량을 평가하여 각각의 코어에 대해서 독립적으로 공급전압을 제어하는 복수의 전원변환부를 포함하는 것을 특징으로 한다. 구체적으로, 본 발명의 전원변환부는 각 코어로부터 서로 상이한 VID(Voltage Identification Signal)를 입력 받아, 이에 따라 각 코어에 서로 상이한 공급전압을 제공한다.

프로세서의 각 코어는 자신의 사용량에 따라 서로 다른 VID를 생성하고, 이와 같은 상이한 VID는 전원을 인가하는 각 코어에 연결된 각각의 전원변환부에 인가된다. 각 코어는 서로 상이한 공급 전원을 인가 받고 개별적으로 동작하게 되므로 불필요한 누설 전력 낭비를 감소시켜 효율적으로 전력 소모를 줄일 수 있다.

종래 기술에서와 같이 하나의 VID로 관리하면, 제 1 코어는 저주파 모드로 동작하고 제 2 코어는 고주파 모드로 동작하는 경우에, 제 1 코어도 고주파 모드의 전압을 인가 받게 되므로 제 1 코어에서 많은 누설 전력이 발생한다. 그러나 본 발명에 의하면 각 코어로부터의 개별적인 VID에 따라서 각 코어에 대한 공급전압이 독립적으로 조정되므로, 제 1 코어는 저주파 모드에 맞는 낮은 공급전압을 인가 받게 되어 제 1 코어에서의 누설 전력을 상당히 줄일 수 있다.

도 2는 본 발명의 일실시예에 의한 멀티-코어 프로세서의 전원제어장치의 기능블록도이다. 도 2를 참조하면, 본 발명의 멀티-코어 프로세서의 전원 제어 장치는 제 1 코어 (310) 및 제 2 코어 (320)를 구비하는 프로세서(350)와 상기 프로세서(350) 내의 제 1 코어 (310) 및 제 2 코어(320)에 연결되어, 각각의 코어의 사용량에 따라 각 코어에 상이한 공급전압을 공급하는 제 1 전원변환부(300) 및 제 2 전원변환부(301)를 포함한다.

상기 제 1 및 제 2 전원변환부(300, 301)는 임의의 하나의 코어의 동작 속도를 높여야 하는 경우에는, 해당 코어로부터 VID를 수신하여 그에 따라 해당 코어의 공급전압을 상향 조정한다. 한편, 임의의 하나의 코어의 동작 속도를 낮추어야 하는 경우에는, 해당 코어로부터 VID를 수신하여 그에 따라 해당 코어의 공급전압을 하향 조정한다.

프로세서(350)의 제 1 코어(310) 및 제 2 코어(320)는 동작 속도(코어의 클락 주파수)에 따라 여러 가지 모드로 동작할 수 있다. 일례로 코어의 동작 주파수는 0.8 GHz, 1 GHz, 1.2 GHz, 1.4 GHz, 1.6 GHz의 다섯 단계로 나누어 조절될 수 있다. 각각의 코어는 각각의 동작 주파수에 따라서 서로 상이한 공급전압을 갖게 되는데, 각 주파수로 변화할 때 전압이 따라서 변경된다. 예를 들어, 0.8 GHz (1.0V), 1 GHz (1.05V), 1.2 GHz (1.1V), 1.4 GHz (1.15V), 1.6 GHz (1.2V)와 같이 변경할 수 있다. VID (Voltage Identification Signal)는 이와 같이 다양한 모드로 동작하는 코어에서 각각의 모드의 공급 전압을 구분하는 신호이다.

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배터리 또는 AC 전원과 같은 전원(power supply)으로부터 전력이 공급되면 제 1 전원변환부(300) 및 제 2 전원변환부(301)는 적당한 공급 전압(operating voltage)을 제 1 코어(310) 및 제 2 코어(320)에 독립적으로 공급한다.

멀티-코어 프로세서를 포함하는 시스템의 운영체제(303)가 제 1 코어(310) 및 제 2 코어(320)의 각각의 사용량을 체크한 후에, 그 결과를 PMU (Power Management Unit: 330)에 전달한다. PMU(330)는 프로세서 내의 각각의 코어를 제어하는데, 일반적으로 컴퓨터 시스템의 사우스 브릿지 또는 노스 브릿지에 내장될 수 있다.

제 1 코어(310) 및 제 2 코어(320)는 PMU의 제어를 받아 각각 해당되는 전압을 생성하도록 하는 VID1 및 VID2를 생성한 후에, 이들을 각각 제 1 전원변환부(300) 및 제 2 전원변환부(301)에 개별적으로 제공하여 각 코어에 어느 정도의 공급전압이 필요한지 알린다. 이렇게 되면 제 1 전원변환부(300) 및 제 2 전원변환부(301)는 각 코어의 VID에 따라서 각 코어에 대한 공급전압을 개별적으로 조정할 수 있다.

본 발명에서 각 코어의 사용량은 각 코어의 점유율 또는 스레드니스(threadness)에 의해 판단될 수 있으나, 이를 이외의 다른 방법에 의해서도 평가될 수 있다. 상기 코어의 사용량은 국내 특허출원 제 출원 번호 2000-0050037호와과 같은 CPU 사용량 체크 방법과 유사한 방법을 사용하여 측정할 수 있다. 또한 마이크로소프트사의 Microsoft 사의 윈도우 테 (Windows XP)에서 사용되는 CPU 사용량을 체크하는 방법을 이용하여 상기 코어들의 개별적인 사용량을 쉽게 얻을 수 있다.

제 1 전원변환부(300) 및 제 2 전원변환부(301)는 DC/DC 컨버터를 포함하거나 전원관리부(Power Regulator)의 형태로 구현될 수 있다. DC/DC 컨버터는 각 코어에 직류 성분의 공급전원을 인가한다.

제 1 코어(310)는 제 1 전원변환부(300)로부터 공급 전압(V_{core1})을 인가 받고, 제 2 코어(320)는 제 2 전원변환부(301)로부터 공급 전압(V_{core2})을 인가 받는다.

제 1 코어(310) 및 제 2 코어(320)의 내에는 각각 PLL1 (313) 및 PLL2 (323)가 내장되는데, 이들은 외부 클락 (예컨대, 100 MHz 또는 133 MHz)을 인가 받아서 각 코어의 사용량에 따라 높은 주파수, 중간 주파수, 낮은 주파수 등으로 주파수를 자체적으로 조정하여 코어 내부의 로직에 해당 주파수를 공급해 준다. 클락발생기(340)는 제 1 코어(310) PLL1 (313) 및 제 2 코어(320)의 PLL2 (323)에 클락 신호(clock signal)를 공급한다.

본 발명의 전원 제어 장치에서 상기 제 1 전원변환부(300) 및 제 2 전원변환부(301)는 하드웨어 블록, 소프트웨어 블록 또는 하드웨어 블록과 소프트웨어 블록의 중간 형태로 구현될 수 있다. 상기 제 1 전원변환부(300) 및 제 2 전원변환부(301)의 다른 실시 예로써, 인텔사의 Intel 사의 IMVP(Intel Mobile Voltage Positioning) 기술을 따르는 전압 조절 제어기(Voltage Regulator Controller)와 같은 것을 포함 할 수도 있다.

이하에서 상술한 구성을 갖는 본 발명의 멀티-코어 프로세서의 전원 제어 동작에 대해서 상세하게 설명한다.

PMU (Ppower Mmanagement Uunit)는 운영체제(303)로부터 제 1 코어(310) 및 제 2 코어(320)의 사용량에 관한 정보를 수신하여 제 1 코어(310) 및 제 2 코어(320)를 제어한다. 제 1 코어(310)는 PMU의 제어 하에 제 1 코어의 사용량에 따른 VID (VID1)를 생성해서 제 1 전원변환부(300)로 전송하고, 제 2 코어(320)는 PMU의 제어 하에 제 2 코어의 사용량에 따른 VID (VID2)를 생성해서 제 2 전원변환부(301)로 전송한다.

여기서 상기 PMU(power management unit)는 MicroSoft 사의 Windows XP 같은 OS(operating system)내에 포함되어 구현될 수도 있다.

제 1 전원변환부(300)는 전원(power source)으로부터 입력 받은 전원을 제 1 코어(310)가 사용하는 전압에 맞게 변환하는데, 구체적으로 제 1 코어(310)로부터 수신한 VID1에 따라 제 1 코어에 적합한 공급전압을 생성하여 공급한다. 한편, 제 2 전원변환부(301)는 제 2 코어(320)로부터 수신한 VID2에 따라 제 2 코어에 적합한 공급전압을 생성하여 공급한다. 하나의 실시예로 상기 제 1 코어(310)의 사용량이 95% 이상이면, 그 코어는 최대 동작 속도 모드로 동작한다. 즉, 일례로 코어의 동작 주파수는 0.8 GHz (1.0V), 1 GHz (1.05V), 1.2 GHz (1.1V), 1.4 GHz (1.15V), 1.6 GHz (1.2V)의 다섯 단계로 나누어 조절될 수 있고, 각각의 코어는 각각의 동작 주파수에 따라서 서로 상이한 공급전압을 갖게 된다고 가정하여 설명한다. 상기 최대 동작 속도 모드에서는 1.6 GHz (1.2V)로 동작되도록 해당 VID 생성과 해당 주파수(1.6Ghz)로 변환되는 동작을 수행한다. 그리고, 만약 그 제 1 코어(310)의 사용량이 75%이하이면, 다음 단계인 1.4 GHz (1.15V)로 천이되어 동작되게 할 수 있다. 또는 즉시 최소 속도 동작 모드인 0.8 GHz (1.0V)로 천이될 수도 있다. 상기 제 1 코어(310) 및 제 2 코어(320)의 사용량에 따른 각각의 코어들의 전압 및 동작 주파수는 위의 일 실시예 이외에도 다른 방법으로 변형하여 사용될 수 있다.

예를 들어, 제 1 코어(310)가 저주파 모드(Low Frequency Mode)로 동작해야 한다면, 제 1 코어에 대한 공급전압은 가능한 낮게 조정되어야 하고 아울러 제 1 코어의 클락 주파수도 낮게 조정되어야 한다. 제 1 코어(310)는 이러한 저주파 모드에 매칭되는 VID를 생성해서 제 1 전원변환부(300)로 전송한다. 제 1 전원변환부(300)는 제 1 코어에 대한 공급전압을 현재의 코어의 공급전압 보다 한 단계 낮은 공급전압을 생성하여 제 1 코어(310)에 공급한다.

한편, 제 1 코어(310)의 사용량으로 보아 고주파 모드(High Frequency Mode)로 동작해야 한다면, 제 1 코어에 대한 공급전압은 가능한 높게 유지되어야 하고, 그에 따라 클락 주파수도 높게 유지되어야 한다. 제 1 코어(310)는 고주파 모드에 매칭되는 VID를 생성해서 제 1 전원변환부(300)로 전송한다. 제 1 전원변환부(300)는 현재의 제 1 코어의 공급전압 보다 한 단계 높은 공급전압을 생성하여 제 1 코어(310)에 공급한다.

공급전압 조정이 완료된 후, 제 1 코어에 대한 공급전압이 목표로 하는 수준까지 조정되었는지 판단하고,

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만약 목표 수준까지 조정되지 않은 경우에는 적정수준에 도달할 때까지 공급전압을 단계적으로 조정할 수 있다.

본 발명의 다른 실시예에 의한 멀티-코어 프로세서의 전압 제어 장치는 두 개 이상의 코어를 구비하는 프로세서와 상기 프로세서 내의 각각의 코어에 연결되어 각 코어에 대한 공급전압을 조절하는 복수의 전원변환부를 포함하고, 상기 프로세서내의 각각의 코어는 동작 속도가 상이한 여러 가지 모드로 동작하고, 각 코어의 사용량을 측정하여 각 코어의 사용량에 맞는 VID를 생성하여 복수의 전원변환부로 독립적으로 전송하며, 상기 전원변환부는 상기 프로세서내의 각각의 코어로부터 독립적으로 VID를 수신하여, 수신한 VID에 따라 각 코어에 대한 공급전압을 독립적으로 조절하는 것을 특징으로 한다.

이러한 실시예의 멀티-코어 프레세서의 전원 제어 장치에서는 임의의 하나의 코어가 현재 보다 빠른 동작 속도로 동작되어야 한다면, 그에 해당하는 VID가 해당 코어에 연결된 전원변환부로 전송된다. 전원변환부는 이러한 VID에 따라 그러한 코어의 동작 주파수를 현 단계 보다 한 단계 높이기 위해 해당 코어의 공급전압을 조정한다. 공급전압의 조정이 완료되면, 코어에 대한 공급전압이 목표로 하는 수준까지 조정되었는지 판단하고, 만약 목표 수준까지 조정되지 않은 경우에는 목표에 도달할 때까지 공급전압을 한 단계씩 단계적으로 높일 수 있다.

이상과 같이 본원 발명의 멀티-코어 프로세서의 전원 제어 장치에서는 복수의 코어에 대해 하나의 VID가 생성되는 것이 아니고, 각 코어에 대해 개별적으로 VID가 생성되기 때문에 불필요한 전력 낭비를 최소화할 수 있다.

상기 장치는 각 코어의 사용량에 따라 각 코어의 주파수를 독립적으로 조절하는 복수의 주파수 제어수단을 더 포함할 수 있다. 따라서 각 코어의 사용량에 따라 각 코어의 주파수와 공급전압이 연계되어 조정될 수 있다.

본 발명의 또 다른 실시예는 멀티-코어 프로세서의 전원 제어 방법에 관계한다. 본 발명에 의한 멀티-코어 프로세서의 전원 제어 방법에 관해서 설명하면 다음과 같다.

도 3은 본 발명에 의한 멀티-코어 프로세서의 전원 제어 방법을 나타낸 흐름도이고, 도 4는 본 발명의 일 실시예에 의한 멀티-코어 프로세서의 전원 제어 방법의 상세 흐름도이다.

도 3을 참고하면, 본 발명의 방법에 의해 멀티-코어 프로세서의 전원을 제어하는 경우에는 먼저 각 코어의 사용량에 대한 정보를 수득하고나서(S401, S402), 각 코어의 사용량에 기초하여 공급전압 조정의 필요성이 있는지 판단한다(S403, S404). 그 다음으로는 공급전압 조정이 필요한 하나 이상의 코어의 공급전압을 해당 코어의 사용량에 따라 독립적으로 조절한다(S405, S406). 본 발명에서는 각 코어에 대한 공급전압을 조정함과 동시에, 각 코어의 사용량에 따라 각 코어의 동작 주파수도 함께 제어할 수 있다.

이하에서 본 발명에 의한 멀티-코어 프로세서의 전압제어방법을 두 개의 코어를 포함하는 듀얼-코어 프로세서를 예로 들어 더욱 상세하게 설명한다. 본 발명의 방법에서는 제 1 코어 및 제 2 코어의 공급전압은 개별적으로 제어되고, 아울러 각 코어의 주파수도 각 코어의 사용량에 따라 개별적으로 제어된다. 즉, 본 발명의 하나의 실시예에서는 VID와 코어의 동작 주파수가 동시에 변경될 수 있다.

먼저 제 1 코어에서의 공급전압 조정 과정을 살펴 보면, 제 1 코어의 사용량에 대한 정보는 운영체제로부터 수득한다(S501). 여기서 각 코어의 사용량은 각 코어의 점유율 또는 스레드니스로 판단할 수 있다.

제 1 코어의 사용량에 대한 정보를 수득한 후에는 제 1 코어에 대한 공급전압의 조정이 필요한지 판단한다(S502). 이 단계에서는 현재 상태에서 제 1 코어에 공급되는 전압과 제 1 코어의 사용량을 고려하여, 제 1 코어에 대한 공급전압의 조정이 필요한지 판단한다.

만약 제 1 코어의 사용량이 많아서 제 1 코어의 동작 주파수를 현 단계 보다 상향 조정해야 된다고 판단되면, 제 1 코어로부터 새로운 VID (VID#1)를 수신한다(S503). 이와 같이 코어의 주파수를 상향 조정하는 경우에는, 공급전압을 우선 변경하고 주파수를 변경한다. 즉, 수신한 VID#1에 따라 제 1 코어에 대한 공급전압을 조정하고(S504), 이어서 제 1 코어에 대한 동작 주파수를 조정한다(S505).

한편, 제 1 코어의 사용량이 적어서 제 1 코어의 동작 주파수를 현 단계 보다 하향 조정해야 된다고 판단되는 경우에는, 주파수를 조정한 후에 공급전압을 조정한다. 구체적으로, 제 1 코어의 동작 주파수를 조정하고(S506), 제 1 코어로부터 새로운 VID (VID#1')를 수신한다(S507). 수신한 VID#1'에 따라 제 1 코어에 대한 공급전압을 조정한다(S508).

제 2 코어에 대한 공급전압의 조정은 제 1 코어에 대한 공급전압의 조정 과정에 대해 독립적으로 진행된다. 제 2 코어의 사용량에 대한 정보를 수득한 후(S510)에는 제 2 코어에 대한 공급전압의 조정이 필요한지, 즉 제 2 코어의 주파수를 상향 조정해야 되는지 판단한다(S512).

만약 제 2 코어의 사용량이 많아서 제 2 코어의 동작 주파수를 현 단계 보다 상향 조정해야 된다고 판단되면, 제 2 코어로부터 VID (VID#2)를 수신한다(S513). 수신한 VID#2에 따라 제 2 코어에 대한 공급전압을 조정하고(S514), 이어서 제 2 코어에 대한 동작 주파수를 조정한다(S515).

한편, 제 2 코어의 사용량이 적어서 제 2 코어의 동작 주파수를 현 단계 보다 하향 조정해야 된다고 판단되는 경우에는, 주파수를 조정한 후에 공급전압을 조정한다. 구체적으로, 제 2 코어의 동작 주파수를 조정하고(S516), 제 2 코어로부터 새로운 VID (VID#2')를 수신한다(S517). 수신한 VID#2'에 따라 제 2 코어에 대한 공급전압을 조정한다(S518).

본 발명에 의한 멀티-코어 프로세서의 전원 제어 방법은 컴퓨터로 읽을 수 있는 기록매체에 컴퓨터가 읽을

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수 있는 코드로서 구현하는 것이 가능하다. 컴퓨터가 읽을 수 있는 기록매체는 컴퓨터 시스템에 의하여 읽혀질 수 있는 데이터가 저장되는 모든 종류의 기록장치를 포함한다. 컴퓨터가 읽을 수 있는 기록매체의 예로는 ROM, EEPROM, 플래시 EEPROM, 플로피 디스크, CD-ROM, 광데이터 저장장치 등이 있다.

본 발명에 의한 컴퓨터가 읽을 수 있는 기록매체는 제 1 코어의 사용량에 대한 정보를 수득하는 단계, 제 1 코어로부터 제 1 코어의 사용량에 따른 VID를 수신하는 단계, 제 1 코어에서 수신한 VID에 따라서 제 1 코어에 대한 공급전압을 조정하는 단계, 제 2 코어의 사용량에 대한 정보를 수득하는 단계, 제 2 코어로부터 제 2 코어의 사용량에 따른 VID를 수신하는 단계, 제 2 코어에서 수신한 VID에 따라서 제 2 코어에 대한 공급전압을 조정하는 단계를 포함하는 멀티-코어 프로세서의 전원 제어 방법을 수행하기 위한 컴퓨터에 의해 실행가능한 프로그램 코드를 포함한다.

본 발명의 방법을 구현하기 위한 프로그램이 컴퓨터 시스템 내의 메모리에 저장되는 경우에는 반도체 제조 공정 중에 기록될 수 있다. 상기 프로그램이 별도의 저장 매체에 저장되어 있거나 네트워크 등을 통해서 다운받게 되는 경우에는, 기존의 프로그램을 삭제하고 새로 설치되거나 업데이트 되는 방식으로 컴퓨터에 설치될 수 있다.

이상에서 본 발명의 구체적인 실시예를 예로 들어 설명하였으나, 이들은 단지 설명의 목적을 위한 것으로 본 발명의 보호 범위를 제한하고자 하는 것은 아니다. 본 발명의 기술적 사상을 벗어나지 않는 범위 내에서 다양한 치환, 변형 및 변경이 가능하다는 것은 본 발명이 속하는 기술 분야의 통상의 지식을 가진 자에게 자명할 것이다.

예를 들어, 본 발명의 멀티-코어 프로세서의 전압 제어 장치 및 방법은 데스크탑 컴퓨터 또는 서버 이외에 노트북 컴퓨터, 스마트폰, 핸드폰, PDA 등과 같은 각종 모바일 기기에도 적용될 수 있다.

또한 설명의 편의를 위해 두 개의 코어를 구비하는 듀얼-코어 프로세서를 중심으로 설명하였으나, 본 발명은 반드시 이들로 국한되는 것이 아니고 더 많은 수의 코어를 포함하는 프로세서에도 그대로 적용될 수 있음은 물론이다.

발명의 효과

본 발명의 멀티-코어 프로세서의 전원 제어 장치 및 방법은 두 개 이상의 코어를 포함하는 프로세서에서 각 코어의 사용량에 따라 지능적으로 전력을 분배함으로써, 각 코어에 발생하는 부하를 효율적으로 관리하고 전력 소모를 최소화하는 이점을 가진다.

또한 본 발명의 장치 및 방법에 의하면 불필요한 누설 전류에 의한 배터리 전력 낭비를 방지할 수 있고, 프로세서의 성능을 최적의 상태로 관리할 수 있게 된다.

더욱이 프로세서의 소모 전력은 배터리의 구동시간과 직결되므로, 본 발명의 전원 제어 장치를 포함하는 프로세서는 배터리의 공간을 줄이고 발열 문제도 해결하여 휴대용 컴퓨터의 소형박형화를 가능하게 한다.

본 발명에서는 멀티-코어 프로세서에서 각 코어에 공급되는 전압을 순수하게 소프트웨어적으로 제어함으로써 비용을 절감할 수 있다.

청구의 범위

청구항 1

두 개 이상의 코어를 구비하는 프로세서; 및

상기 프로세서 내의 각각의 코어에 연결되어, 각 코어의 사용량에 따라 각 코어에 대한 공급전압을 독립적으로 조절하는 복수의 전원변환부를 포함하는 것을 특징으로 하는 멀티-코어 프로세서의 전원 제어 장치.

청구항 2

제 1항에 있어서, 상기 전원변환부가 각 코어로부터 서로 상이한 전압 ID(Voltage Identification: VID)를 수신하고, 각각의 VID에 따라 상이한 전압을 각 코어에 인가하도록 되어 있는 것을 특징으로 하는 멀티-코어 프로세서의 전원 제어 장치.

청구항 3

제 1항에 있어서, 상기 전원변환부가 상기 프로세서 내의 각각의 코어에 연결되어, 각 코어에 직류 성분의 공급 전원을 인가하는 복수의 DC/DC 컨버터를 포함하는 것을 특징으로 하는 멀티-코어 프로세서의 전원 제어 장치.

청구항 4

제 1항에 있어서, 상기 장치가 코어의 점유율 또는 스레드니스(threadness)에 의해 코어의 사용량을 판단하도록 되어 있는 것을 특징으로 하는 멀티-코어 프로세서의 전원 제어 장치.

청구항 5

제 1항에 있어서, 상기 전원변환부는 임의의 하나의 코어의 동작 속도를 높여야 하는 경우에는, 해당 코어로부터 VID를 수신하여 그에 따라 해당 코어의 공급전압을 상향 조정하도록 되어 있는 것을 특징으로 하는 멀티-코어 프로세서의 전원 제어 장치.

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청구항 6

제 1항에 있어서, 상기 전원변환부는 임의의 하나의 코어의 동작 속도를 낮추어야 하는 경우에는, 해당 코어로부터 VID를 수신하여 그에 따라 해당 코어의 공급전압을 하향 조정하도록 되어 있는 것을 특징으로 하는 멀티-코어 프로세서의 전원 제어 장치.

청구항 7

제 1항에 있어서, 상기 장치가 각 코어의 사용량에 따라 각 코어의 주파수를 독립적으로 조절하는 복수의 주파수 제어수단을 더 포함하는 것을 특징으로 하는 멀티-코어 프로세서의 전원 제어 장치.

청구항 8

복수의 코어를 구비하는 멀티-코어 프로세서에서 전원을 제어함에 있어서,

각 코어의 사용량에 대한 정보를 수득하는 단계 ; 및

각 코어의 사용량에 기초하여 공급전압 조정 필요성이 있는지 판단하는 단계; 및

공급전압 조정이 필요한 하나 이상의 코어의 공급전압을 해당 코어의 사용량에 따라 독립적으로 조절하는 단계를 포함하는 것을 특징으로 멀티-코어 프로세서의 전원 제어 방법.

청구항 9

제 8항에 있어서, 상기 코어의 사용량 정보 수득 단계가 운영체제로부터 각 코어의 점유율 또는 스레드니스에 관한 정보를 수득하는 단계임을 특징으로 하는 멀티-코어 프로세서의 전원 제어 방법.

청구항 10

제 8항에 있어서, 상기 공급전압 조정 필요성 판단 단계가

각각의 코어의 사용량에 비추어 공급전압의 조정이 필요한 경우에 각 코어로부터 서로 상이한 VID (Voltage Identification)를 입력 받는 단계를 포함하는 것을 특징으로 하는 멀티-코어 프로세서의 전압 제어 방법.

청구항 11

제 10항에 있어서, 상기 방법이 상기 VID에 따라 서로 상이한 공급전압을 각 코어에 인가하는 단계를 포함하는 것을 특징으로 하는 멀티-코어 프로세서의 전원 제어 방법.

청구항 12

제 10항에 있어서, 상기 방법이 각 코어의 사용량에 따라 각 코어의 동작 주파수를 변경하는 단계를 더 포함하는 것을 특징으로 하는 멀티-코어 프로세서의 전원 제어 방법.

청구항 13

제 8항에 있어서, 상기 방법이 임의의 하나의 코어의 동작 속도를 높여야 하는 것으로 판단되는 경우에는, 해당 코어로부터 VID를 수신하여 그에 따라 해당 코어의 공급전압을 상향 조정하는 단계를 포함하는 것을 특징으로 하는 멀티-코어 프로세서의 전원 제어 방법.

청구항 14

제 8항에 있어서, 상기 방법이 임의의 하나의 코어의 동작 속도를 낮추어야 하는 것으로 판단되는 경우에는, 해당 코어로부터 VID를 수신하여 그에 따라 해당 코어의 공급전압을 하향 조정하는 단계를 포함하는 것을 특징으로 하는 멀티-코어 프로세서의 전원 제어 방법.

청구항 15

두 개 이상의 코어를 구비하는 프로세서; 및

상기 프로세서 내의 각각의 코어에 연결되어 각 코어에 대한 공급전압을 조절하는 복수의 전원변환부를 포함하고,

상기 프로세서는 동작 속도가 상이한 여러 가지 모드로 동작하고, 각각의 코어는 각각의 동작 모드에 맞는 VID를 생성하여 전원변환부로 전송하고,

상기 전원변환부들은 상기 프로세서내의 각각의 코어로부터 독립적으로 VID를 수신하여, 수신한 VID에 따라 각 코어에 대한 공급전압을 독립적으로 조절하는 것을 특징으로 하는 멀티-코어 프로세서의 전원 제어 장치.

청구항 16

제 15항에 있어서, 상기 전원변환부가 직류 성분의 공급 전원을 인가하는 복수의 DC/DC 컨버터를 포함하는 것을 특징으로 하는 멀티-코어 프로세서의 전원 제어 장치.

청구항 17

제 15항에 있어서, 상기 장치가 코어의 점유율 또는 스레드니스 (threadness)에 의해 코어의 사용량을 판단하도록 되어 있는 것을 특징으로 하는 멀티-코어 프로세서의 전원 제어 장치.

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청구항 18

제 1 코어의 사용량에 대한 정보를 수득하는 단계;

제 1 코어로부터 제 1 코어의 사용량에 따른 VID를 수신하는 단계;

제 1 코어에서 수신한 VID에 따라서 제 1 코어에 대한 공급전압을 조정하는 단계;

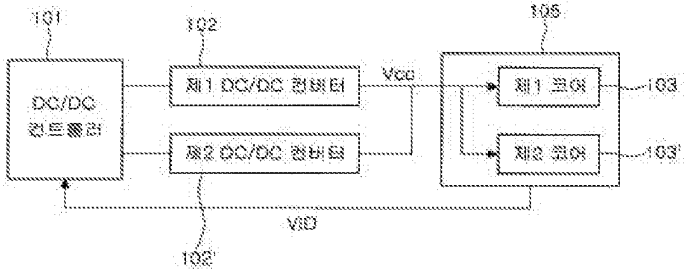
제 2 코어의 사용량에 대한 정보를 수득하는 단계;

제 2 코어로부터 제 2 코어의 사용량에 따른 VID를 수신하는 단계; 및

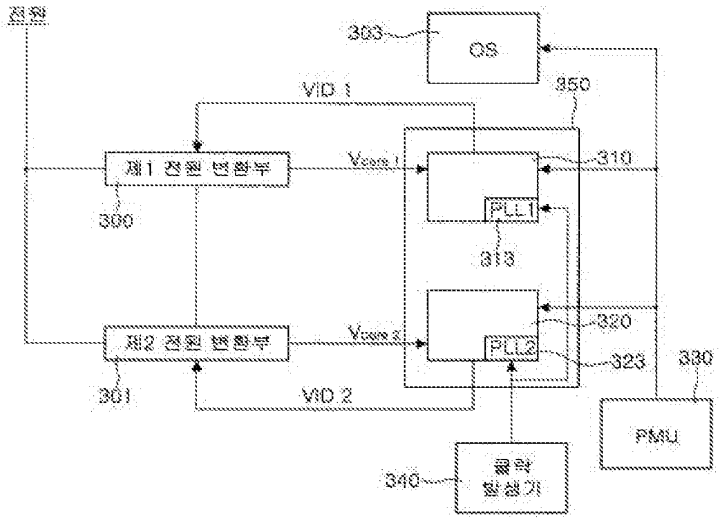
제 2 코어에서 수신한 VID에 따라서 제 2 코어에 대한 공급전압을 조정하는 단계를 포함하는 멀티-코어 프로세서의 전원 제어 방법을 수행하기 위한 컴퓨터에 의해 실행가능한 프로그램 코드를 저장하고 있는 컴퓨터가 읽을 수 있는 기록매체.

도면

도면1

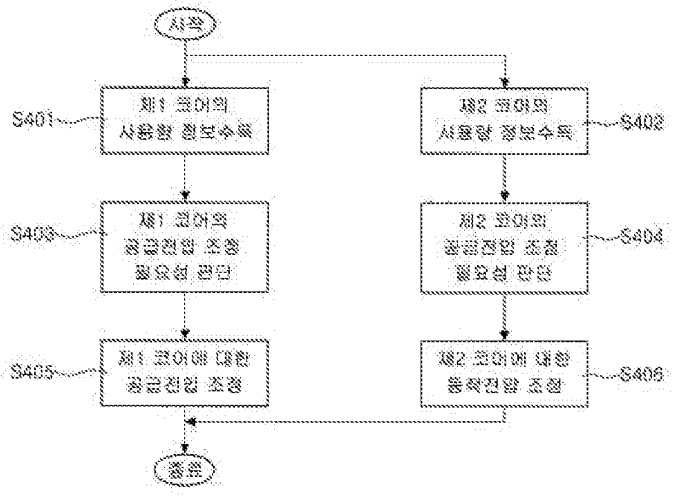


도면2



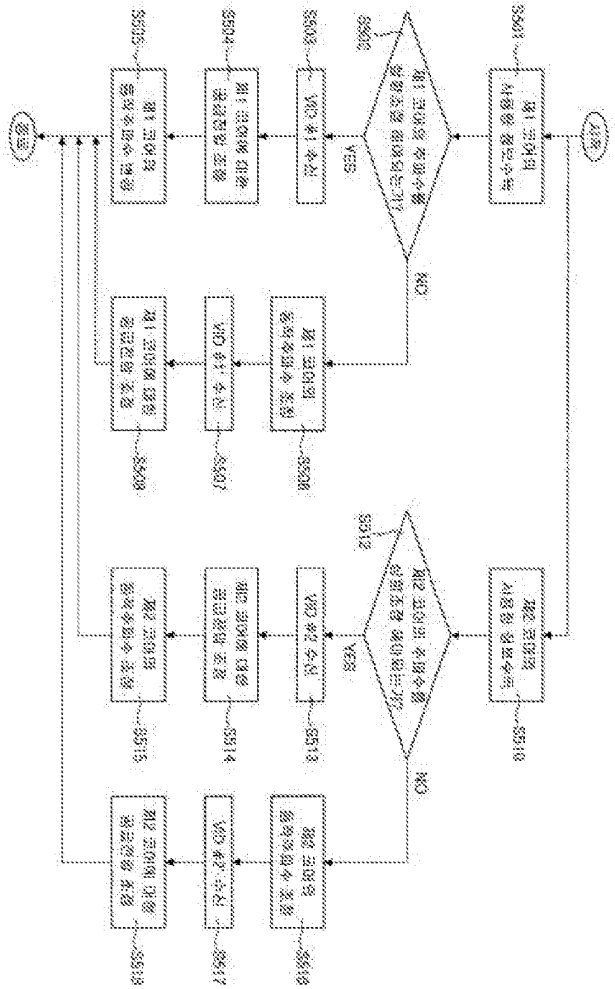
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도면3



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도면4



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Electronic Acknowledgement Receipt

EFS ID:	15840294
Application Number:	13225677
International Application Number:	
Confirmation Number:	2063
Title of Invention:	Dynamically Allocating A Power Budget Over Multiple Domains Of A Processor
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Customer Number:	47795
Filer:	Mark J. Rozman/Stephanie Petreas
Filer Authorized By:	Mark J. Rozman
Attorney Docket Number:	ITL.2495US (P38410)
Receipt Date:	22-MAY-2013
Filing Date:	06-SEP-2011
Time Stamp:	11:54:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	ITL2495USIDSToFile.pdf	71311 300ec9e67aa95741ede36a07cbc57c8a1ae14a89	no	5

Warnings:	
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2	Information Disclosure Statement (IDS) Form (SB08)	ITL2495USIDSwithSRToFile.pdf	67637 e896f8f424602405ab87961314d18311b2bbec2c	no	4
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Non Patent Literature	NPLDoc2495SearchRrt.pdf	2568112 f63d7c9faec95c3b6b145e950e9ed0a7389a9e76	no	11
Warnings:					
Information:					
4	Foreign Reference	ForDocKR1020060128469AToFile.pdf	1184706 a37b57481322a0a4d53749a8bc11b38f0db03602	no	10
Warnings:					
Information:					
5	Non Patent Literature	NPLDocUncoreArticleToFile.pdf	543582 6a077974e82b9996b0cf3f373ffcac26bf4c8628	no	23
Warnings:					
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		Total Files Size (in bytes):	4435348		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13225677
	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6908227		2005-06-21	Fusu, et al.	
	2	7797512		2010-09-14	Cheng, et al.	
	3	7146514		2006-12-05	Kaushik, et al.	
	4	8015427		2011-09-06	Miller, et al.	
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20090313489		2009-12-17	Gunther, et al.	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13225677
	Filing Date	2011-09-06
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2495US (P38410)

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	KR 10-2006-012846	KR		2006-12-14	LG Electronics Inc.		☐

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NON-PATENT LITERATURE DOCUMENTS

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	1	DAVID L. HILL, et al., "The Uncore: A Modular Approach To Feeding The High-Performance Cores," Intel Technology Journal, 2010, Vol 14, Issue 3, pages 30-49.	☐

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/225,677	09/06/2011	Avinash N. Ananthakrishnan	ITL.2495US (P38410)

CONFIRMATION NO. 2063

47795
TROP, PRUNER & HU, P.C.
1616 S. VOSS RD., SUITE 750
HOUSTON, TX 77057-2631

PUBLICATION NOTICE

OC000000059718144

Title: Dynamically Allocating A Power Budget Over Multiple Domains Of A Processor

Publication No.US-2013-0061064-A1
Publication Date:03/07/2013

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	1	7434073		2008-10-07	Magklis	
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	1	EP 1 282 030	EP	A1	2003-05-02	Mitsubishi Kenki Kabushiki Kaisha		☐
	2	2001-202155	JP		2001-07-27	Hitachi LTD		☒
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NON-PATENT LITERATURE DOCUMENTS

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	1	U.S. Patent Application Serial No. 13/282,896, filed October 27, 2011, entitled "ENABLING A NON-CORE DOMAIN TO CONTROL MEMORY BANDWIDTH," by AVINASH N. ANANTHAKRISHNAN, et al. (2492)	☐
	2	SPEC-Power and Performance, Design Overview V1.10, Standard Performance Information Corp., October 21, 2008, 6 pages.	☐
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	21	U.S. Patent Application Serial No. 13/285,414, filed October 31, 2011, entitled "CONTROLLING A TURBO MODE FREQUENCY OF A PROCESSOR," by AVINASH N. ANANTHAKRISHNAN, et al. (2494)	☐
	22	U.S. Patent Application Serial No. 13/247,580, filed September 28, 2011, entitled "CONTROLLING TEMPERATURE OF MULTIPLE DOMAINS OF A MULTI-DOMAIN PROCESSOR," by AVINASH N. ANANTHAKRISHNAN, et al. (2496)	☐
	23	U.S. Patent Application Serial No. 13/285,465, filed October 31, 2011, entitled "DYNAMICALLY CONTROLLING CACHE SIZE TO MAXIMIZE ENERGY EFFICIENCY," by AVINASH N. ANANTHAKRISHNAN, et al. (2497)	☐

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☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Mark J. Rozman/	Date (YYYY-MM-DD)	2012-10-03
Name/Print	Mark J. Rozman	Registration Number	42117

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PATENT ABSTRACTS OF JAPAN

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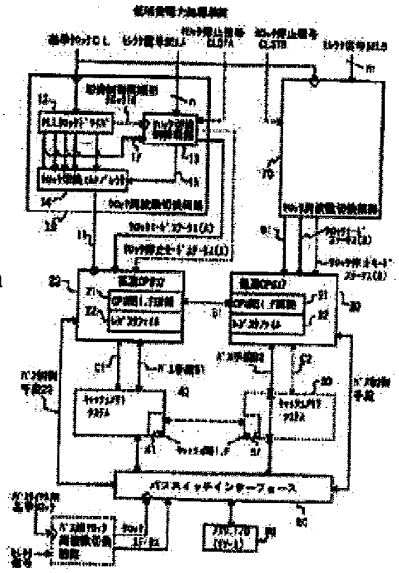
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(71)Applicant : HITACHI LTD
(72)Inventor : KAMETANI MASATSUGU
UMEKITA KAZUHIRO
YAMAMOTO KENJIRO
KOYAMA MASAHIRO
MOMOI YASUYUKI
FUNATSU TERUNOBU
IKE KATSUHISA

(54) LOW POWER CONSUMPTION PROCESSOR

(57)Abstract:
PROBLEM TO BE SOLVED: To finely control power consumption of a processor by enabling high speed, smooth and dynamic switching of multiple clocks and further enabling high speed and dynamic switching of multiple CPUs.
SOLUTION: High speed and smooth switching of clocks is realized by generating a switching signal 15 the clock levels of which before and after switching are the same and which is synchronized with a standard clock CL by a clock switching control circuit 13, taking out a clock from a PLL clock driver 12 by selecting it by a multiplexer 14 by the switching signal 15. The switching is dynamically executed by outputting select signals SELA, SELB by execution of an instruction of the CPU. In the switching between CPUs 20, 30, when the CPU under operation executes a switching instruction of the CPUs, supply of clocks to other CPUs is started, the present CPU enters a stopped state and the CPUs to which the clocks are supplied stop the clocks of other CPUs and starts operation of the present CPU.



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CLAIMS

[Claim(s)]
[Claim 1]A PLL clock driver which generates two or more clocks with frequency which synchronizes with a given reference clock and is mutually different, A clock change multiplexer which is chosen according to a switching signal into which one of clocks generated by this PLL clock driver was inputted, and is outputted as an after-change clock, A signal according to a selector signal for a clock change given to timing which a clock before a change with this clock change multiplexer selected before a change and a clock after said change are in the same signal level, and synchronized with said reference clock is generated, A low-power-consumption processing unit provided with a clock means for switching which outputs this signal as said switching signal to said clock change multiplexer, and CPU which answers an output clock outputted from said clock change multiplexer, and operates.
[Claim 2]In the low-power-consumption processing unit according to claim 1, said clock means for switching, A flip-flop for a synchronization which synchronizes said selector signal with a clock in sync with a reference clock, A selector signal synchronized by this flip-flop is active, and that state is set to timing from which a clock before said change and an after-change clock changed to the same level, and said selector signal is inactive.
And a low-power-consumption processing unit having a flip-flop for selection with which that state is reset to timing from which a clock before said change and an after-change clock changed to the level, and sending out an output of this flip-flop for selection as said switching signal.

[Claim 3]While having a low-power-consumption processing unit of Claim 1 as the 1st processing unit, The 2nd processing unit that contains CPU of low power consumption rather than CPU contained in said 1st processing unit, A CPU-to-CPU interface means for keeping the same information between register files of each CPU in the 1st processing unit and the 2nd processing unit, The 1st cache memory system linked to CPU of the 1st processing unit, The 1st cache memory control means which controls this 1st cache memory system, CPU of the 1st processing unit, and the 1st bus means including a bus control means outputted and inputted via the 1st cache memory system, Answer said bus control means from the 1st processing unit and the 2nd processing unit, and the 2nd bus means including a bus control means from CPU of the 2nd processing unit, and the 1st bus means and the 2nd bus means are switched, A bus switch interface means which outputs and inputs an external bus and an external control signal to timing which suited an external resource, A low-power-consumption processing unit possessing a mode means for switching which chooses operation of the 1st processing unit, and either of the 2nd processing unit, operates them, and is made to stop CPU in a processing unit which was not chosen, or is maintained at an idle state.
[Claim 4]In the low-power-consumption processing unit according to claim 3, said mode means for switching, When it is included in said 1st and 2nd processing units, and while is working as for the 1st or 2nd processing unit and operation is shifted to a processing unit of another side from a processing unit, It controls so that a mode means for switching of a working processing unit cancels a stop of a processing unit of another side, or an idle state and the processing unit

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concerned shifts to an idle state, A mode means for switching of a processing unit of said another side started by this so that clock supply to a working processing unit may be suspended till then. A low-power-consumption processing unit controlling and controlling a processing unit of the another side concerned to succeed a state of a working processing unit and to operate till then.

[Claim 5]When a working processing unit rewrites an own register file in the low-power-consumption processing unit according to claim 3, A low-power-consumption processing unit which carries out the feature of having also rewritten a register file of a processing unit under stop via said CPU-to-CPU interface so that it might be in agreement with the rewriting result.

[Claim 6]A low-power-consumption processing unit, wherein said CPU possesses a clock change command which publishes said selector signal for a clock change, and switches a clock frequency dynamically in the low-power-consumption processing unit according to claim 1 or 2.

[Claim 7]A low-power-consumption processing unit of one description in Claims 3-5 characterized by comprising the following.

A clock change command which CPU of said 1st and 2nd processing units publishes said selector signal for a clock change, and switches a clock frequency dynamically.

a CPU change command which switches a processing unit dynamically by said mode means for switching -- at least -- on the other hand.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to a processing unit with a built-in CPU which aims at power-saving.
[0002]
[Description of the Prior Art]With the function and performance of a computer system centering on personal computer systems, such as a microcomputer/personal computer, and a laptop computer, improving in recent years, the electric power which these processing units consume is increasing quickly, and is posing a problem in respect of being various. Computer processing facilities and control processors, such as general industrial use and object for OA, an object for scientific and engineering calculations, and an object for nests, can also be expected that the demand to power saving will increase from now on from problems, such as a problem to the adverse effect which it has to natural environment, electric power cost, **********, an electric power supply situation. Power-saving which an electric power supply is a cell on an operating environment in many cases, and links especially handheld computer (carrying is possible) processing units, such as a laptop computer, with available time directly is indispensable.
[0003]Conventionally, in the personal computer (PC) which aims at power-saving, the two following methods have been proposed as technique most effective in power-saving. One of them prepares a low speed clock and a high-speed clock as indicated by JP,H8-241145,A, In an idle state (state where processing with effective PC is not performed), or back cloud processing (low-priority processing), operating power is reduced by switching so that a low speed clock may be supplied to CPU.
Other one prepares a low-speed CPU chip (generally there is little power consumption) and a fast chip (generally power consumption is large) as indicated by JP,H11-7344,A, The bus from two CPUs is connected in common, and when performing processing whose problem low-speed processing does not have, either, operating power is reduced by switching to the low-speed CPU-chip side.
The technology which enabled it to perform a smooth clock change by the method of switching a clock rate is indicated by JP,H10-91272,A etc.
[0004]
[Problem to be solved by the invention]In conventional technology, there is a problem in respect of the following and the solution has been SUBJECT.
(a) Parenchyma is impossible for interior-action frequency becoming very high (300-600 MHz), and CPU in recent years switching a clock smoothly in the exterior (substrate superiors) of CPU. About this point, conventional technology is indicating no solution.
(b) Although the low power consumption by fine power controls is called for, the overhead of conventional technology of a clock change or a CPU change is large, and it cannot meet the demand.
(c) In the conventional technology which switches CPU, it is the requisite to use a common CPU chip and change treating operation with it is difficult. [a large overhead of identification

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processing of the inside information of CPU-to-CPU and] [fine]
(d) Although high speed technology, such as cache memory and a high-speed bus system, is used for high-speed CPU, it faces building low-power-consumption CPU, and no conventional technologies are indicated about treatment and the architecture which is newly needed of the high speed technology.
[0005]The purpose of this invention is to provide the processing unit which made large reduce power consumption possible as could perform the clock and the CPU change finely by few smooth overheads and could also perform cache memory and a bus change in a short time.
[0006]
[Means for solving problem]The PLL clock driver which generates two or more clocks with frequency which this invention synchronizes with the given reference clock, and is mutually different, The clock change multiplexer which is chosen according to the switching signal into which one of the clocks generated by this PLL clock driver was inputted, and is outputted as an after-change clock, The signal according to the selector signal for a clock change given to the timing which the clock before a change with this clock change multiplexer selected before the change and the clock after said change are in the same signal level, and synchronized with said reference clock is generated, A low-power-consumption processing unit provided with the clock means for switching which outputs this signal as said switching signal to said clock change multiplexer, and CPU which answers the output clock outputted from said clock change multiplexer, and operates is indicated.
[0007]In the above-mentioned low-power-consumption processing unit, this invention said clock means for switching, The flip-flop for a synchronization which synchronizes said selector signal with the clock in sync with a reference clock, The selector signal synchronized by this flip-flop is active, and that state is set to the timing from which the clock before said change and the after-change clock changed to the same level, Said selector signal is inactive and it has a flip-flop for selection with which the state is reset to the timing from which the clock before said change and the after-change clock changed to the level, The low-power-consumption processing unit sending out the output of this flip-flop for selection as said switching signal is indicated.
[0008]While this invention is provided with a low-power-consumption processing unit as the 1st processing unit, The 2nd processing unit that contains CPU of low power consumption rather than CPU contained in said 1st processing unit, The CPU-to-CPU interface means for keeping the same the information between the register files of each CPU in the 1st processing unit and the 2nd processing unit, The 1st cache memory system linked to CPU of the 1st processing unit, The 1st cache memory control means which controls this 1st cache memory system, CPU of the 1st processing unit, and the 1st bus means including the bus control means outputted and inputted via the 1st cache memory system, Answer said bus control means from the 1st processing unit and the 2nd processing unit, and the 2nd bus means including the bus control means from CPU of the 2nd processing unit, and the 1st bus means and the 2nd bus means are switched, The bus switch interface means which outputs and inputs an external bus and an external control signal to the timing which suited the external resource, Operation of the 1st processing unit and either of the 2nd processing unit are chosen, and are operated, and the low-power-consumption processing unit possessing the mode means for switching which is made to stop CPU in the processing unit which was not chosen, or is maintained at an idle state is indicated.
[0009]In the above-mentioned low-power-consumption processing unit, this invention said mode means for switching, When it is included in said 1st and 2nd processing units, and while is working as for the 1st or 2nd processing unit and operation is shifted to the processing unit of another side from a processing unit, It controls so that the mode means for switching of a working processing unit cancels a stop of the processing unit of another side, or an idle state and the processing unit concerned shifts to an idle state, The mode means for switching of the processing unit of said another side started by this so that the clock supply to the working processing unit may be suspended till then. The low-power-consumption processing unit controlling and controlling the processing unit of the another side concerned to succeed the state of the working processing unit and to operate till then is indicated.

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[0010]When, as for this invention, a working processing unit rewrites an own register file in the above-mentioned low-power-consumption processing unit, The low-power-consumption processing unit which carries out the feature of having also rewritten the register file of the processing unit under stop via said CPU-to-CPU interface so that it might be in agreement with the rewriting result is indicated.
[0011]In the above-mentioned low-power-consumption processing unit, this invention said CPU, The low-power-consumption processing unit possessing at least one side of the clock change command which publishes said selector signal for a clock change, and switches a clock frequency dynamically, and the CPU change command which switches a processing unit dynamically by said mode means for switching is indicated.
[0012]
[Mode for carrying out the invention]Hereafter, an embodiment of the invention is described in detail. First, if the power consumption of a computer is considered, power consumption is mainly proportional to the throughput of CPU. That is, it is thought that the power consumption of CPU of a computer system is going up from the following situations, and it continues to go up.
[0013](1) The throughput which executes without stress large-scale functional programs, such as OS which is becoming large every year, is demanded of CPU, The quantity of the hardwares (a pipeline, cache memory, those control hardwares, etc.) for raising directly functional hardware for that and a CPU process speed is becoming large in connection with it. It means that the amount of switching of the transistor per unit time increases this, and since power consumption is proportional to the amount of switching of a transistor, especially CPU of a CMOS process subject's recent years has caused increase of power consumption.
[0014](2) As prime technology for accelerating CPU, the miniaturization (a 0.1-0.2-micrometer process is used in recent years) of the CMOS process is carried out, Improvement in switching speed of high integration and a transistor is realized, and it waits for the technique of raising the frequency of the clock supplied to CPU (or core based CPU) using the improved efficiency of the process. It is not new that 500-MHz class of a clock is used inside a CPU chip in recent years, either. The high integration characteristic of a process will be used for parallelization of hardware, etc., and will contribute to a pipeline's etc. latency shortening, i.e., the improvement in a clock frequency, according to a synergistic effect with the improvement in switching speed. However, the amount of switching of the transistor described by (1) will increase to the part multiplication target, and has led to the steep power consumption rise.
[0015](3) Possession of the low-power-consumption mode which controls electric power by clock stop when the CPU does not need to operate etc. as the technique of the low power consumption at the time of designing CPU, and low-voltage-operation-ization (3.3V, 2.2V grade) are ********** for the actual condition. However, since low power consumption of the former is not usually carried out at the time of operation, it is not power-saving to effective processing time. Although the latter is the technique of having contributed to low power consumption greatly in recent years, If voltage is dropped too much not much greatly, the switching speed or the driving ability itself of a transistor will be reduced, performances, such as speed of CPU of operation, may be worsened, and it will be thought that it is not desirable in respect of the noise margin of a signal.
[0016]The above (1) If the low voltage operation of CPU of (3) is removed from the consideration about the low power consumption on the CPU design of - (3), and power-saving, While performing processing with effective CPU, it turns out that it becomes a point of the low power consumption of CMOS process highly efficient CPU how the number of effective switching gates in CPU within unit time (or transistor count) can be reduced. The thing which combine well the technique of decreasing the effective operation transistor count itself by the miniaturization of a circuit-logic scale and the technique to which a clock frequency is reduced and which is not spread is also clearer to this than (1) and (2). However, as (1) and (2) described, these techniques, In order to go back thoroughly with highly efficient-ization of CPU and to avoid the inconsistency, It is necessary to provide effectively the architecture of CPU and the instruction set for power saving which can apply these techniques to the processing as which high speed processing is seldom demanded, and the processing it can be considered that are real

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idle processings. Namely, what kind of task and processing step are also received working always, It can shift to free and various power consumption modes required of a high response, and the fine low-power-consumption control which can perform the power-controls operation by the command in a program and the instructions from the outside needs to provide free and dynamically possible CPU. For example, CPU optimized by improvement in the speed although it was high power consumption, and CPU optimized by low power consumption although it was a low speed are summarized for one chip, The basic clock frequency which is switched free, and is carried out as [make / it / operate], and is given to each CPU also has an instruction set for power controls which makes it possible to switch free, and should just arrange the command for power controls finely according to speed of operation required in a program.

[0017]Drawing 1 is the block diagram which was constituted based on the above-mentioned plan and in which showing the example of composition of the low-power-consumption processing unit of this invention, The high-speed core based CPU 20 which operates at high speed although it is high power consumption, and the clock frequency switch circuits 10 and 70 which supply CPU clocks 11 and 81 of a frequency variable to the low-speed core based CPU 30 and both the cores based CPU of low power consumption, respectively although it is not so high-speed are formed. However, frequency regularity may be sufficient as the clock 81 to a low-speed core based CPU, and its switch circuit 70 of a clock frequency is then unnecessary. Between the cores based CPU 20 and 30, it is connected via the CPU-to-CPU interface circuits 21 and 31 incore [each], and is used for the coherency control (control which keeps the contents the same) between the register files 22 and 32 in two cores based CPU, and the exchange of the status information between cores based CPU. Each core based CPU may be equipped with the cache memory 40 and 50, respectively. In order to raise processing efficiency especially to the high-speed core based CPU 20, the cache memory system 40 in which the rapid access for storing the information on the external resources 90, such as external I/O and a memory system, in the inside of CPU is possible is indispensable in many cases. In order to perform access to the external resources 90 (a memory, I/O, a system bath, etc.), the bus means B1 from each core based CPU and B-2 exist, respectively, but. In order to connect only the more active one to an external resource between two cores based CPU, the bus switch interface 60 is provided. The bus means B1 and B-2 are once connected to the cache memory systems 40 and 50, respectively with the cache memory control signal C1 from a core based CPU, and C2, when the cache memory systems 40 and 50 exist, Only when information does not exist on cache memory, information is outputted and inputted from the external resource 90 via the bus switch interface 60. When both cores based CPU have cache memory, the interfaces 41 and 51 between cash for performing coherency control between cache memory are formed.

[0018]Although the clock frequency switch circuits 10 and 70 are formed to each cores based CPU 20 and 30 with the composition of drawing 1 shown above, These switch the clock frequency to each core based CPU free according to the situations at that time (the contents of processing, environment, etc.), and provide the means for controlling operation of each core based CPU to become the optimal processing speed and power consumption. By controlling the whole processing unit by the change of this, and the high-speed core based CPU 20 and the low-speed core based CPU 30 dynamically to become as a whole more optimal processing speed and power consumption. It can become possible to carry out dynamically control of electric power / working speed management more efficient than before working, and the synthetic power consumption of the whole system can be decreased as a result.

[0019]The PLL (phase locked loop) clock driver 12 which generates two or more clocks which synchronized strictly mutually from basic clock CL from which the clock frequency switch circuit 10 serves as a standard of operation, The clock change multiplexer 14 for choosing one from two or more clocks 17 from there, The clock switching control circuit 13 which generates the switching signal 15 corresponding to selector signal SELA synchronizing with the switching control synchronous clock 16 (one of the clocks 17 may be used) from a PLL clock driver, and is sent out to the multiplexer 14 is comprised. The multiplexer 14 gives the clock 11 selected with the switching signal 15 to the core based CPU 20, and the core based CPU 20 operates based on this clock 11 for operation. Although the clock frequency switch circuit 70 is also the same

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composition, the frequency of the clock 81 to output differs.
[0020]The clock driver 12 which contained PLL is used in composition of the above-mentioned clock frequency switch circuit 10. When a mere dividing term circuit generates two or more clocks like the former, this, a) Although there is a problem of delay of an output clock occurring to c basic clock with low (1, 1/2, 1/4, 1/8 — it becomes twice) flexibility of frequency which is made as for b generation which needs to prepare the high-speed clock for an external input, It is because all these problems are solvable if PLL is used. Namely, even if basic clock CL is a thing of low frequency, it generates a clock of very high frequency by internal VCO, Flexibility of frequency generable with constituting so that to carry out dividing of this, what is necessary may just be made to perform a phase comparison with a basic clock and two or more sorts of clocks may be generated using an internal clock from VCO can also be enlarged. Also being able to have two or more sorts of VCO, flexibility of generable frequency becomes still larger. It becomes easy to remove or adjust delay [as opposed to an unformatted input clock for delay of an output clock made into the purpose] of an output clock by returning a feed back clock which serves as a standard via a delay element equivalent to delaying amounts, such as a multiplexer, at PLL.
[0021]Drawing 2 shows the example of composition of the clock switching control circuit 13, and is a case where the clocks 17 from the PLL clock driver 12 are two clocks (a high-speed clock and a low speed clock) in this circuit. Clock selection signal SCIN in selector signal SELA or the SELB itself of drawing 1, or — it is the signal which answered it and was generated — it — a flip-flop (FF) — it is made the signal which synchronized with the clock 16 for a synchronization in 107 and 106, i.e., two or more clocks 17 from the PLL clock driver 12 and the signal synchronized strictly. This signal is taken out as two outputs which Q output of the flip-flop 106 and QN output reversed mutually, and is inputted into the 3 input NAND gates 102 and 101. In NAND gates 102 and 101, these, a high speed, and NAND logic with a low speed clock are taken, and these NAND gate output is inputted into set-terminals S and reset terminal R of RS flip flop 113 for a latch which comprised the gates 104 and 103, respectively. The output of the gate 104 which is an output of the set side of this RS flip flop 113 is outputted to the clock change multiplexer 14 as the clock switching signal 15.
[0022]Drawing 3 shows a timing chart which shows operation of the clock switching control circuit 13 shown in drawing 2, and a high-speed clock is made one twice the frequency of a low speed clock. Altogether, from the PLL clock driver 12, these high speeds and a low speed clock, and the clock 16 for a synchronization synchronize, and are outputted. After Q output of the flip-flop 106 produced by clock selection signal SCIN's changing high-level (time t0), and synchronizing it with the flip-flops 107 and 106 changes high-level, The clock switching signal 15 switches from a low level high-level using timing (time t1) to which both a high-speed clock and a low speed clock change high-level first, and the output clock 11 is also switched to a low speed clock from a high-speed clock. On the contrary, clock selection signal SCIN changes from high level to a low level (time t2), After QN output of the flip-flop 106 produced by synchronizing it with the flip-flops 107 and 106 changes high-level, The clock switching signal 15 is switched to a low level from high level using timing (time t3) to which both a high-speed clock and a low speed clock change high-level first. According to it, the output clock 11 is also switched to a high-speed clock from a low speed clock. However, since a high speed and a low speed clock are already in a high-level state at the time t3, a change is promptly performed in change timing of the clock switching signal 15. The switching timing t1 and t3 here The clock 16 for a synchronization, and a high speed, It has delay tcsd1 [suitable] which comprises gate pass time etc. between low speed clocks, and tcsd2, and the change point serves as [both] a design which exists when a high speed and a low-speed clock level are stabilized and it is high-level certainly. Generating of a hazard at the time of a change, etc. is prevented by this.
[0023]What delayed the inversion clocks 108 of the clock 16 for a synchronization, or the clock 16 in the delay gate 109 as shown in drawing 2, Or if even timing is filled (if the signal 15 changes to the 14 multiplexerA1 and timing whose state of A2 input is stable), An RS flip flop output for a latch is shifted with the flip-flop 105 using clock 16 for a synchronization itself, and even if it uses what was adjusted so that the above-mentioned timing might be satisfied as the clock

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switching signal 15, a hazard etc. can be prevented similarly.

[0024]Drawing 4 is a modification of a clock switching control circuit shown in drawing 2, it is what takes exclusive OR of a high-speed clock and a low speed clock at the gate (EXOR) 114, and supplied the inverted output in NAND gates 101 and 102 of 2 inputs, and others are the same as drawing 2. According to this composition, even when both a high-speed clock and a low speed clock are low levels, and even when high-level, if there is only even an identical level, a circuit which performs switching operation on the basis of a change point of a clock selection signal can be realized. What is necessary is just to supply an output of the gate 114 in NAND gates 101 and 102 via the flip-flop 115 driven with normal rotation of a clock for a synchronization, reversal, or a clock to which delay of the clock was carried out suitably to remove a hazard from EXOR gate 114. Since the multiplexer 14 is constituted by hazard from EXOR gate 114 using a transfer gate switch even if a hazard rides on the clock switching signal 15, As long as a switching signal changes with the characteristics of a CMOS transfer gate mentioned later to timing whose state of an input (A1, A2) is stable in an identical level (a hazard is also included), it may be thought that a hazard does not occur in an output of the multiplexer 14. Therefore, although it is better for the flip-flop 115 to exist, it is thought that it is not an indispensable element.

[0025]Drawing 5 shows the example of composition of the multiplexer 14 which switches two clocks of the high speed and low speed of drawing 2, and is the transfer gate switch constituted from a CMOS process. The transistors 110P and 111P will be conducted, if it is called P type transistor, negative potential is impressed to the gate (S input. connection its ******) and high potential is impressed to A1 (high-speed clock) input to this, and they tell the potential of A1 input to the buffer 112B. On the other hand, the transistors 110N and 111N are called N type transistor, if potential lower than this is impressed to A2 input when positive potential is impressed to the gate, they will be conducted, and they tell the potential of A2 (low speed clock) input to the buffer 112B. Therefore, since one side of A1 and A2 input can be outputted to the terminal Z via the buffer 112B and the path is constituted from 1-2 steps of transistors by the potential of S input, a high speed switch is possible. And although the output side of each transistor serves as high impedance in the state other than the above-mentioned condition, Since the input impedances of the buffer 112B are also a CMOS circuit, therefore high impedance, an electric charge is accumulated in the terminal area between a transistor output and a buffer input, a state just before being in the state is maintained for a while, and this is reflected in the outgoing end Z. Therefore, even if there is the moment both two transistor gate inputs serve as a low by delay of the inverter 112G, at the time of the change of the clock switching signal 15 (S input), If the potential impressed to A1 input and A2 input is then stable, a hazard will not occur from the buffer 112B and a smooth clock change will be performed.

[0026]Drawing 6 is another example of composition of the multiplexer which switches two clocks, and also has a partial function of a clock switching control circuit. Although the basic switch 600 of this circuit is a transfer gate switch constituted from a CMOS process like drawing 5, the forms of the select signal from CPU and the switching signal 15 of the switch 600 differ. That is, the basic switch 600 outputs A2 input, when switching signal SA1 is "0" and switching signal SA2 is "0" about A1 input. Select signal SelA1 inputted and SelA2 are the signals from CPU for choosing A1 input of a clock, and A2 input, when it is "1", respectively, By EXOR gate 602 and NAND gates 603 and 604, SelA1= "1", It becomes signal SA1= "0" and SA2= "1" at the time of SelA2= "0", and the input A1 is outputted, when it is SelA1= "0" and SelA2= "1", it becomes signal SA1= "1" and SA2= "0", and the input A2 is outputted. Furthermore, it has prevented SelA1 and SelA2 becoming signal SA1=SA2= "1" in "0" at both the times of both of "1", and the basic switch's 600 turning off thoroughly, and outputting A1 and A two-car input by work of these gates.

[0027]Although a selector signal is once latched by latch clock LCL using the register 601 and being sent to the basic switch 600, With latching with synchronizing change timing with a clock, and outputting switching signal SA1 and SA2 simultaneously, this minimizes a timing error of a change and has the function to keep two inputs of the basic switch 600 from short-circuiting. Although it is the former synchronization here, it is necessary to make basic clock CL

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synchronize latch clock LCL strictly for the purpose. It is common to synchronize a changeover command from CPU with basic clock CL, and to output it as this method.

[0028]Drawing 8 is the example of a circuit which carries out multistage combination of the circuit of drawing 6, and switched the 4 input clocks CL1-CL4, Multistage combination of the basic switch 600 of drawing 6 is carried out, and it is made to switch with a switching signal which latched and generated them from the select signals CL1-CL4 by latch clock LCL to the register 804 like drawing 6. A buffer (112B of drawing 6) connected to each basic switch 600 outgoing end Z is unnecessary on each switch, should just form the buffer 803 in an outgoing end of the multistage joint last, and uses it as a clock driver by this.

[0029]Although the clock switching control circuit for switching two clocks of a high speed and a low speed and the example of composition of a multiplexer, and operation were explained using drawing 2 - drawing 6 above, each example of a circuit for switching more clocks is described below. Drawing 7 (a) is an example of the circuit which chooses and takes out one of the four clocks CL1-CL4, and is the clock switching control circuit 13 of drawing 1, and a circuit equivalent to the multiplexer 14. The multiplexers 701-703 are [which was shown in drawing 5] for 2 input change, and the switch part comprises these multistage combination. A switching signal is given with the output of the register 704, and the change timing is given as drawing 6 explained by the same latch clock LCL in sync with a basic clock. Selection signal SelE1 inputted into the register 704 and SelE2 are the signals acquired by encoding the select signals SelCL1-SelCL4 from CPU like drawing 7 (b). Although these selection signal SelE1, SelE2, the register 704, and a latch clock are considered to have realized the function of a clock switching control circuit, the portion which generates a selection signal and a latch clock is omitted by drawing 7. Although the example of four clocks was shown here, many changes can be constituted further similarly.

[0030]Although drawing 7 is the example of composition which carried out multistage combination of the multiplexer of drawing 5, even if it carries out multistage combination of these, many clock changes are performed considering the circuit which combined the clock switching control circuit 13 explained by drawing 2 or drawing 4, and the multiplexer 14 as one unit circuit. In this case, only depending on each clock after switching before switching, smooth switching control is realizable similarly by the method of setting the timing switched when those clocks are in the logic of the level. Namely, what is necessary is to take AND logic, to take input **** or EXOR+ reversal logic (EXNOR) to NAND gates 101 and 102, and just to input into NAND gates 101 and 102, after carrying out the mask of the clocked into which is unrelated in the circuit of the first rank. For example, when AND logic is taken, or even when EXOR+ reversal logic is taken when one clocked into was fixed to "1" (mask), It becomes a mere buffer which passes the clock of another side, and, only in the case of the clock with which the clock should switch to the next, switching operation will be performed by the clock and the synchronized clock selection signal. If both clocks are related, in the circuit, the clock selection signal itself should not change and the output of the multiplexer 14 should also be fixed to "1." The clock path which is eventually valid from these two conditions, i.e., the clock path chosen now, Next, since the multiplexer which has switched the path of the clock which should be chosen, and 1 set of its switching control circuit can consider that it is operating as a 2 input-clock switching control circuit used as the foundations explained so far, the same smooth switching operation becomes possible. The clock path selection which should switch newly specifies the selector signal to each multiplexer which decodes the change command which CPU fetched and corresponds, and should just set them as required logic.

[0031]Drawing 9 shows the example of the clock frequency switch circuit at the time of a multistage input, and the example of use of the PLL clock driver in the inside of it. It is the thing each of the switch circuits 911-917 adds a register to the multiplexer shown, for example in drawing 5 like drawing 7, uses the clock of the frequency f for this register, latches a select signal, and it was made to synchronize, and this is the same as that of the composition of drawing 7. Thus, if it synchronizes with the clock of the maximum frequency from PLL, the synchronization to a strict basic clock will be attained. Or it is good also considering the circuit of drawing 6 as these switch circuits.

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[0032]In drawing 9, set to f the clock frequency which should be fed back, and the basic clock of f/32 of frequency is inputted from the outside on the basis of it, The PLL clock driver which can generate f/2, f/3, f/4, f/6, f/10, f/16, f/22, f/32, and nine sorts of frequency of f was assumed. The clock of the frequency f is the high-speed clock currently used also as a clock for a synchronization. The PLL clock driver 901 receives reference clock CL (f/32) as a reference clock (REFCLK), It carries out as [coincide / the phase of a signal and the phase of a reference clock which increased the feed back clock CLB 1/32 times inside / mostly], and the nine above-mentioned sorts each of clock phases are adjusted. That is, since each clock generated synchronizes with the clock of the high-speed frequency f strictly and is generated, it will be outputted from the PLL clock driver with the phase only with the early part according to the delaying amount of the feed back clock CLB. therefore, the sequence of the switch circuits 911-914 -- said -- 915 or 916 sequences -- and -- said -- inserting in a synchronous clock (f) and the clock for a synchronization to each stage being constituted, as the delay correction circuits 921-923 equivalent to each delaying amount of the sequence of 917 were illustrated, and. If it returns to a PLL clock driver by using delay correction circuit 923 output as the feed back clock CLB, the strict synchronization which coincides mostly with a basic clock phase the phase of output clock CLout of the final stage outputted to CPU as a result will be attained. The phase of the output clock generated from a PLL clock driver can tune a loop filter (resistance and a capacitor amend) finely, if PLL in which external is possible is used.
[0033]It is thought that use of PLL for a clock frequency change becomes indispensable [being built in a CPU chip as CPU will be accelerated from now on]. That is, it is not the frequency which 500-MHzclass of CPU exists with an internal clock of LSI, and can be directly treated by an external system (on an electronic board) also in the actual condition. Therefore, as an external basic clock, it suppresses to about 100 MHz or less, and composition which fast frequency operation is made inside an LSI chip becomes indispensable. It can be said that it means that they stop materializing if CPU systems still like drawing 1 are not packed as 1 chip LSI. Namely, in order to synchronize a clock over 500 MHz strictly and to perform switching control. It is a natural flow to unify at least, and for the necessity of carrying out 1 chip making to produce the clock frequency switch circuits 10 and 70 and the cores based CPU 20 and 30 containing a PLL clock driver, and to accumulate whole system ** of drawing 1 as a 1 chip CPU ideally. The actual condition adds examination to below based on drawing 1 about the constitutional feature, a newly realizable function, an effect, etc. at the time of taking into consideration accumulating it on 1 chip CPU, although low-power-consumption 1 chip LSI of such thought does not exist.
[0034]An advantage and necessity which integrate a clock frequency switch circuit and a core based CPU are as having mentioned above. Therefore, a function and an effect by integrating the two cores based CPU 20 and 30 to 1 chip LSI are examined first. By carrying out 1 chip making of the two cores based CPU to the 1st, shortening of a communication latency by a CPU-to-CPU I.F. circuit and fast improvement in a throughput can be aimed at. For example, coherency control between the register files 22 and 32 is realizable in real time. When working CPU changes an own register file, it becomes possible to send register information for writing, alteration data information, and a write command to a register file in CPU of another side in parallel, and to change a corresponding register content in real time. By this, even if a change of CPU-to-CPU occurs, it is not necessary to copy a context anew, and an effect that processing can be promptly started without an excessive overhead is acquired.
[0035]It comes to be able to carry out the high-speed generation of selector signal SELA, SELB, a switching control signal / information of CPU-to-CPU, etc. which changes from a switching signal to the clock frequency switch circuits 10 and 70, a mask signal of an input clock mentioned above, etc. to the 2nd in a low latency. Although a method of preparing for the exterior of CPU a means to generate these signals, as a status register etc., using an MOV command of CPU, loading/store instruction, etc., and setting and resetting a value had to be taken in the former, When CPU fetches it by arranging appropriately in an embedded program as a command of CPU by carrying out 1 chip making, it can constitute so that it can perform promptly. . [whether within a core based CPU, asynchronous FF 107 and 106 for

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synchronization processing in the clock frequency switch circuit 10 and 70 is removable as a result, and] Or it may be able to do that synchronization is possible only at FF106, and, as for CPU interior-action frequency, for a certain reason, an advantage that it is a high speed far can also shorten a latency concerning a change substantially to the exterior. Although an example of wire connection and its example of a change protocol of a control signal for a change of CPU-to-CPU are mentioned later, such CPU-to-CPU signal transduction can be performed quickly, and an advantage that operation and processing corresponding to it can also be quickly performed by high response is born. Fine power controls can be described in a program as a result, and an effect that further low power consumption can be attained is acquired.
[0036]Next, 1 chip LSI built-in-ization of a cache memory part (cache memory systems 40 and 50) is considered. Since the high-speed interface between cash which synchronized with the machine cycle by 1 chip making can be first constituted [1st] like coherency control of a register file, it becomes possible to keep the contents of cache memory the same in real time. When the cache memory of working CPU wrote and replaces, specifically, processing which stands in a row and rewrites the same address part of the cache memory of CPU of another side is performed. The information sent from the working CPU side is the cache memory address and cache data which are made into the purpose, and a write command signal, It rewrites in real time to cache data aiming at the contents of the address of cache memory which corresponds if a write command becomes active. In the former, since the CPU chip was separate, when CPU resumed operation, the flash plate (it repeals) of the cache information in front of once needed to be carried out, but the overhead about the cache memory at the time of a CPU change can be minimum-ized by this method. When preparing a cache memory system for each of each core based CPU, If the structure of a memory system is divided into a high-speed correspondence type and the type corresponding to low power consumption, a design and the former are assigned to a high-speed core based CPU and the latter is assigned to a low-speed core based CPU, respectively, the synthetically optimal structure in respect of power consumption and working speed can be provided. Although 1 chip making only of the cache memory part is carried out and the CPU section by which 1 chip making was carried out independently, the bus means B1, B-2, the cache memory control signal C1, and the method of combining the signal group of C2 grade externally are also considered, Compared with the case where 1 chip making of all is carried out, clearly, the access latency between CPU and a resource increases and it can be told to the performance of CPU systems that it is minus.
[0037]It is also possible the 2nd and to make 2 sets of cache memory into 1 set by 1 chip making. Two cores based CPU specifically share one cache memory, In order to use cache memory more effectively, by access control of a clock synchronization type, etc., perform rapid access, while the high-speed CPU side operates, and while the low-speed CPU side operates, What is necessary is just to take a system which aimed at low power consumption by static access control (in the case of a CMOS process power consumption is zero mostly except when having accessed by a command) by a lead/write command. According to this, a memory part for which the coherency management / control between cache memory need a lot of [it is unnecessary and / not only becoming but] transistors because 1 grouping is removable. that 1 set of other cache memory capacity can be increased, or size of a chip can be made small **** -- etc. -- the further improvement in the speed or low power consumption can be aimed at. In order to realize coherency control and a common cache memory which were inevitably mentioned above also in this case, A control algorithm of cache memory and structure of a cache memory system are the premises of being common to both CPUs, and a cache access control circuit by the side of CPU must be designed. In this case, the bus switch interface 60, It is not a thing of a system which switches a bus from two CPUs, and when access to a unified cache memory system goes wrong, it may constitute as a bus switch buffer for input and output controlled so that access operation to the exterior occurs promptly.
[0038]The system of the bus switch interface unit 60 which is packed into another LSI and arranged near the resource 90 is also effective. When packing especially a cache memory system into one and ******ing by two CPUs; When the bus means B1 and B-2 are combined by cache memory and access to the cache memory goes wrong from cache memory (when the data

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needed on cache memory does not exist), The bus means which is needed when going to access to an external resource becomes a good thing with one. If this internal bus means is defined as an external access bus of the LSI chip of CPU systems, the bus switch interface unit 60 can also be defined as a BIU used as the interface to a resource, a system bath, etc. If this is accumulated on LSI together with the control signal for access to a resource, a decoder, an input output buffer, etc., one or the method of distributing and arranging [two or more] can be taken near each resource or the local resource block. as compared with the case where wiring is taken about, buffer delay, decoder delay, etc. are removable from the CPU chip concentrated and accumulated -- a part (a BIU can be substituted instead of buffer IC which is needed near a resource, or a decoder) -- improvement in the speed may be able to be attained.

[0039]Next, drawing 10 and drawing 11 explain switching control of CPU-to-CPU. Signal connection for switching control of CPU-to-CPU and clock frequency control is first shown in drawing 10. High-speed CPU20 and low-speed CPU30 have the clock selection control circuits 202 and 203, respectively (it may build in an inside of CPU). If CPU fetches clock frequency setting out / variation order, and a CPU change command and execution is started, it will generate the corresponding clock selection control circuit 202 or control signals (Select, Stop, etc.) which need 203, and will control the clock selection drivers 200 and 201. Here, the clock selection drivers 200 and 201 shown in drawing 10 are equivalent to a function of the clock frequency switch circuits 10 and 70 of drawing 1. Selector signal SELA in drawing 1 including control signals, such as a switching signal, a clocked into mask signal, etc. of a clock change multiplexer which mentioned above the signal Select (A) and (B), It shall be equivalent to a function of SELB and the signal Stop (A) and (B) shall be equivalent to clock stop signal CLSTA of drawing 1, and a function of CLSTB.

[0040]In drawing 10, the Stop signal is connected to crossing so that starting/stop processing of the clock mutually supplied to self by CPU of the other party may be performed supposing the composition by which the clock is supplied only to CPU chosen working. Drawing 11 is illustrating signs that the change to low-speed CPU30 from high-speed CPU20 is carried out, and explains this in detail. If high-speed CPU20 which is working CPU fetches a switch command (switch of CPU30) first, the reboot instructions to CPU30 will be generated and it will shift to an idle state. reboot instructions are accompanied by the clock control instructions 23 to the clock selection control circuit 202 -- the clock reboot to CPU30 -- performing (stop (B) is canceled). It escapes from an idle state promptly after a clock reboot to CPU30 via the CPU-to-CPU communication line 61, and it orders so that it may shift to the following processing step. If a clock is rebooted, via the clock selection control circuit 203 so that CPU30 side may stop the clock by the side of CPU20 first, after activating stop (A), it escapes from an idle state, and it shifts to the following processing step -- in addition, CPU30, In order to perform required processing and to go following on CPU20 using the information on CPU20 copied to the own register, inconsistency is produced by neither procedure nor the contents of processing. The change to CPU20 of an opposite direction from CPU30 is also the same.

[0041]As mentioned above, it can include in the instruction set of CPU by the ability to make the switch command of CPU-to-CPU, and the clock frequency change command to CPU into a real-time power control instruction, and it can constitute so that those commands can be freely used in a program. The directions of a power control instruction real-time [these] are explained below.

[0042]When using a real-time power control instruction for controllers for control, such as a sequencer, as shown in drawing 12, the difference in the sampling time of each task is directly related to the difference in a priority in many cases. namely, -- like a task with a short interval of a sampling time (it directs by the triangle seal in a figure) -- high -- it can be said that it is a task with a high tendency for processing [****] to be required, and a high priority. Therefore, when generated by the task switch (a-g in a figure) among these tasks, a power control instruction is executed in OS which supports the head or task switch of the started task, and suitable CPU and clock frequency are chosen according to the priority as a result. For example, task TA1 with the highest priority chooses the high-speed core based CPU 20, and a clock frequency also chooses the highest thing, The task 3 which is the lowest priority chooses a core

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based CPU and a clock frequency as the selection setting of the clock frequency highest [2 / which is the 2nd priority / task TA] of the low-speed core based CPU 30 according to a processing task like the selection setting of a degree in the middle of [clock frequency] the low-speed core based CPU 30. Thus, it is effective, if it shifts to the selection mode which lessens power consumption as a priority of a task falls. If selection setting of the clock frequency minimum of the low-speed core based CPU 30 is used, useless power consumption can be stopped as much as possible at the time of idle modes, such as a sleep mode which performs no task, or wait mode (suspend mode), and it is still more effective.

[0043]Drawing 13 is an example of tasking of each CPU in multiprocessor operation, and shows signs that take a synchronization between tasks with relation by an interprocessor synchronization mechanism, and scheduled parallel processing is advanced. SYNCm-n shows that CPUm and CPUn synchronize and idle shows the state (play task) where NOP processes no idle time (idle time). Since idle and NOP can be recognized in this figure when they carry out the PURISUKE joule of the task, a power control instruction is arranged there, and if it is set as suitable power saving mode (it is set as the clock frequency minimum of for example, a low-speed core based CPU), power-saving can be attained effectively.

[0044]Next, an example of the power control means in a working processing unit, for example, a notebook computer, and use technology is given using a battery system.

(1) In the battery-operated type processing unit which has a power control means to adjust power consumption dynamically, and a battery monitor means to detect the residue of a battery, When the target movable time which a processor system wants to work with a battery is set up, target movable time is guaranteed by adjusting power consumption dynamically, referring to the residue of a battery.

(2) In above (1), a priority is given according to a processing load to application which a processing unit processes, From lowering and (= processing speed is also lowering) carrying out ****** of the power consumption more as light processing of load, power consumption is adjusted during heavy load application execution, without giving load in an operator.

In (3), (1), or (2), means (an external hard switch or a software switch) by which a user of a processing unit can choose a priority of direct processing as supervisor mode are formed, and are adjusted to power consumption corresponding to a selected priority (power control). This operation may be carried out in real time working. Such (1) A power control means used by directions of - (3) is the most effective if a power control means by a combination of a CPU change (the high speed / low-speed CPU change) and a clock frequency change which were mentioned above is used.

[0045]Next, an example is similarly described using a power control means of this invention about power controls (power save) in a system which performs power consumption setting out finely in a window screen on CRT of processing units (PC etc.).

(1) Provide a control button which performs priority setting out of multitasking application in each window, or display a setting-out window of a priority at the time of each application starting, and set up a priority with a mouse. A power consumption setting-out controller Control of processing frequency of each application, Optimal clock frequency can be determined from a priority state, whole PC power consumption, and a power supply state of all the applications, and performance of PC which a user expects by this can be efficiently assigned to power of CPU, and low power consumption can be attained.

(2) When separating from the terminal of PC, specify the application which needs time to separate in a power consumption setting-out window screen and background high speed operation. A power consumption setting-out controller stops a device without necessities, such as a display, immediately, and the optimal clock frequency is determined from the operation amount and the relation of power consumption and a power supply state which will be performed by the time a user returns. Processing [a user does not access by this] of a between to expect is performed efficiently, and low power consumption can be attained. As a mechanism which senses having separated from the terminal here, methods, such as setting up the shift to direct low-power-consumption mode in the detection by input devices (a keyboard, a mouse, etc.) or a setting-out window screen, are used.

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(3) Specify in a window specification of the device which is not used and make it into hibernation. Thereby according to a user's Assessment on Search Report by Designated Searching Authority, power consumption can be reduced.

[0046]Here, a power consumption setting-out controller is the program module described using the above-mentioned power control instruction set which operates the power control means (combination of a CPU change and a clock frequency change) of this invention too mentioned above. This controller may be firmware-ized when high-speed control is required. When firmware executive systems other than CPU exist, said power control instruction set, It is necessary to perform directions of direct instruction execution from the executive system by a bit line or an information input output means from the outside, etc., to answer it, and to establish the external instruction directing means which performs promptly the corresponding power control instruction in CPU and a system. A firmware executive system performs procedure for required power controls using this external instruction directing means.

[0047]As mentioned above, although use technology has been described, The program which describes these procedure is inserted and generated automatically [on condition of a power control instruction] to the conventional program with a pre-compiler, It can download to a system, or can incorporate as the driver and system call of OS, and can realize, without applying a burden to a user directly because OS prepares the mechanism started if needed.

[0048]Although the processing unit shown in drawing 1 has presented the form which contains two CPUs as a form which is the easiest to realize, it can also constitute the processing unit containing three or more CPUs. The contents of the register which operating effectively before long is only one CPU, and the CPU changed working, It copies to the register of other CPUs which are not chosen in real time like the case where it constitutes from two CPUs, and a CPU-to-CPU interface is constituted and operates so that a coherency can be maintained. CPU which should be change ordering at the time of the change of CPU-to-CPU, and should switch will be specified. Execution of a command will carry out switching operation procedure of two CPU-to-CPU explained in this example between specified CPU and CPU chosen now.

[0049]A processing unit containing such two or more CPUs can also be applied to a fault tolerant system, a high reliability system with vicarious execution processing at the time of abnormalities, etc. That is, when trouble has been perceived to instruction processing under execution (for example, parity error etc.), it switches to other CPUs using a switching means of CPU-to-CPU, a command is reworked, and high reliability-ized operation of avoiding malfunction is attained. It is necessary to have whether a register by command which an error generated in this case is changed, and a means to which a register content of CPU chosen as a state at the time of rerunning by crawling and holding a register content of a processing step of the past of shoes in CPU is returned.

[0050]

[Effect of the Invention]According to this invention, the following effects are acquired.

(1) Electric power can be controlled at high speed dynamically and finely, and the effect of attaining low power consumption of a processing unit by it is acquired.

(2) The technology in which the low price formation of 1 chip CPU is possible is shown, and an effect applicable while securing high cost performance to various applications which need low power consumption is acquired.

[Translation done.]

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02

PATENT ABSTRACTS OF JAPAN

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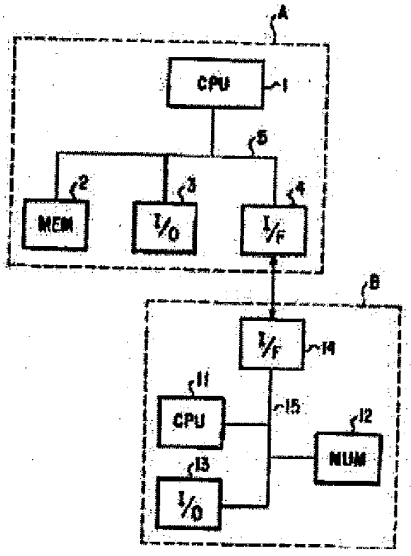
(71)Applicant : **TOSHIBA CORP**
(72)Inventor : **OSUMI ATSUSHI**

(54) OPERATING INFORMATION/FAULT INFORMATION SAMPLING SYSTEM

(57)Abstract:

PROBLEM TO BE SOLVED: To easily sample the operating information and fault information on a computer by outputting an interruption signal to a computer, outputting the operating information and fault information stored in the computer and storing this information in an information sampling device when the information sampling device is connected with the computer.

SOLUTION: When a computer A is connected with an information sampling device B, the information sampling device B outputs an interruption signal to a computer A and requests the release of the main bus 5 of the computer A. When the main bus 5 is released, the computer A notifies the information sampling device B that the main bus 5 is released and notifies an operator of the effect that an information sampling is performed. The information sampling device B samples working information and fault information from the storage device 2 of the computer A and stores this sampled information in the storage device 112 of the information sampling device B. Thus, the operating information and fault information on the computer A can be easily sampled without depending on the operator having techanical knowledge.



* NOTICES *

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damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1]In operation information and a fault information extraction system extracted with information extraction equipment, operation information stored in a memory measure of a computer, and fault information said computer, A main bus release means to release a main bus to which said memory measure is connected based on an interrupt signal, Have a main bus release notice means to report that a main bus was released by said main bus release means, and said information extraction equipment, An interrupt signal output means which outputs an interrupt signal to said computer when connected to said computer, If it is reported that a main bus was released by said main bus release notice means, Operation information and a fault information extraction system provided with an information extraction means to extract static operation information and fault information which are memorized by said memory measure, and an information storage means which memorizes operation information and fault information which were extracted by said information extraction means.
[Claim 2]In operation information and a fault information extraction system extracted with information extraction equipment, operation information stored in a memory measure of a computer, and fault information said computer, A clock means for stopping which suspends a clock supplied to CPU and an input/output device of said computer based on an interrupt signal, Have a clock stop reporting means which reports that a clock supplied to CPU and an input/output device of said computer by said clock means for stopping was suspended, and said information extraction equipment, An interrupt signal output means which outputs an interrupt signal to said computer when connected to said computer, If it is reported that a clock supplied to CPU and an input/output device of said computer by said clock stop reporting means was suspended, Operation information and a fault information extraction system provided with an information extraction means to extract static operation information and fault information which are memorized by said memory measure, and an information storage means which memorizes static operation information and fault information which were extracted by said information extraction means.
[Claim 3]Operation information and the fault information extraction system according to claim 1 or 2 adding an alarming means which reports what operation information and fault information were memorized for by said information storage means to said information extraction equipment.

[Translation done.]

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]This invention relates to the operation information and the fault information extraction system which extracts the operation information and fault information of a computer.
[0002]
[Description of the Prior Art]Conventionally, when extracting the operation information and fault information of a computer, in the state where CPU of a computer is working, the operator operated the computer and was outputting operation information and fault information to operation information and fault information extraction equipment from the computer.
[0003]
[Problem to be solved by the invention]However, when the operation information of a computer and fault information were extracted by operating a computer as mentioned above, the operator which has a know how had to operate the computer.
[0004]In the state where CPU of a computer is working, since the operation information and fault information of the computer were extracted, only dynamic information could be acquired and static information was not able to be acquired.
[0005]Here, "dynamic information" means the information extracted in the state where access is performed to the equipment which is the target of information extraction. Therefore, the information extracted by the timing of information extraction may differ.
[0006]When access is performed to a computer during information extraction operation, the simultaneity of information extracted first and information extracted by the last may not be maintained. On the other hand, "static information" means information extracted where access to a computer which is the target of information extraction is suspended. Therefore, information extracted is not based on timing of extraction, but becomes settled uniquely.
[0007]When extracting fault information, extraction of information on a time of an obstacle occurring is important, and information after a state of a computer changes may become completely meaningless. Therefore, although "static information" extracted where a computer is stopped needed to be acquired to timing which wants to extract information, according to operation information and the fault information extraction system of the conventional computer, only dynamic information was able to be acquired as mentioned above.
[0008]This invention is made in view of the above-mentioned actual condition, and is a thing. The purpose is to provide operation information and a fault information extraction system which can extract operation information and fault information easily.

[0009]
[Means for solving problem]Therefore, invention which relates to Claim 1 to achieve the above objects first, In operation information and a fault information extraction system extracted with information extraction equipment, operation information stored in a memory measure of a computer, and fault information said computer, A main bus release means to release a main bus to which said memory measure is connected based on an interrupt signal, Have a main bus

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release notice means to report that a main bus was released by said main bus release means, and said information extraction equipment, An interrupt signal output means which outputs an interrupt signal to said computer when connected to said computer, If it is reported that a main bus was released by said main bus release notice means, They are operation information and a fault information extraction system provided with an information extraction means to extract operation information and fault information which are memorized by said memory measure, and an information storage means which memorizes operation information and fault information which were extracted by said information extraction means.

[0010]Invention concerning Claim 2 the operation information stored in the memory measure of a computer, and fault information in the operation information and the fault information extraction system extracted with information extraction equipment said computer, The clock means for stopping which suspends the clock supplied to CPU and the input/output device of said computer based on an interrupt signal, Have a clock stop reporting means which reports that the clock supplied to CPU and the input/output device of said computer by said clock means for stopping was suspended, and said information extraction equipment, The interrupt signal output means which outputs an interrupt signal to said computer when connected to said computer, If it is reported that the clock supplied to CPU and the input/output device of said computer by said clock stop reporting means was suspended, They are operation information and a fault information extraction system provided with an information extraction means to extract the static operation information and fault information which are memorized by said memory measure, and the information storage means which memorizes the static operation information and fault information which were extracted by said information extraction means.

[0011]Invention concerning Claim 3 is the operation information and the fault information extraction system which added the alarming means which reports that operation information and fault information were memorized by said information extraction equipment at said information storage means in operation information and the fault information extraction system according to claim 1 or 2.

[0012]

[Function]If information extraction equipment is connected to a computer, as for invention concerning Claim 1, an interrupt signal will be outputted to a computer from information extraction equipment. It reports that the main bus was released by information extraction equipment while releasing the main bus to which the memory measure in which operation information and fault information are stored is connected, if a computer is outputted [an interrupt signal] from information extraction equipment. And since the operation information and fault information which are memorized by the memory measure by the information extraction means of information extraction equipment are extracted and this extracted information is memorized by the information storage means, for information extraction, an operator is not needed but information can be extracted easily.

[0013]If information extraction equipment is connected to a computer, as for invention concerning Claim 2, an interrupt signal will be outputted to a computer from information extraction equipment. It reports that the clock was suspended by information extraction equipment by the clock stop reporting means while suspending the clock supplied to the main bus to which the memory measure is connected, if a computer is outputted [an interrupt signal] from information extraction equipment. And since the operation information and fault information which are memorized by the memory measure by the information extraction means of information extraction equipment are extracted and this extracted information is memorized by the information storage means, static operation information and fault information are easily extractable.

[0014]Since invention concerning Claim 3 reports what operation information and fault information were memorized for by the information storage means by the alarming means in operation information and the fault information extraction system according to claim 1 or 2, It can be made to recognize that extraction of operation information and fault information was completed with information extraction equipment to the operator.

[0015]

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[Working example]Hereafter, the embodiment of this invention is described with reference to Drawings.
<1st embodiment> drawing 1 is a figure showing the composition of the operation information and the fault information extraction system concerning the 1st embodiment of this invention (embodiment corresponding to invention of Claim 1).
[0016]In the figure, A is a computer and B is information extraction equipment. The computer A comprises CPU1, the memory storage 2, the input/output device 3, and Interface Division 4. These CPU1, the memory storage 2, the input/output device 3, and Interface Division 4 each are connected by the main bus 5.
[0017]CPU1 releases the main bus 5 to which the memory storage 2 and the input/output device 3 are connected based on an interrupt signal. CPU1 notifies CPU11 that the main bus 5 was released via Interface Division 4 of the computer A, and Interface Division 14 of the information extraction equipment B.
[0018]CPU1 reports that information extraction is performed to the operator of the computer A via the input/output device 3 of the computer A. The memory storage 2 memorizes the operation information of the computer A, and fault information.
[0019]A display, FDD, HDD, etc. are connected to the input/output device 3. Interface Division 4 is connected with Interface Division 14 of the information extraction equipment B.
[0020]The information extraction equipment B comprises CPU11, the memory storage 12, the input/output device 13, and Interface Division 14. These CPU11, the memory storage 12, the input/output device 13, and Interface Division 14 each are connected by the main bus 15.
[0021]CPU11 outputs an interrupt signal to CPU1 via Interface Division 14 of the information extraction equipment B, and Interface Division 4 of the computer A, when connected to the computer A.
[0022]A notice of that the main bus 5 was released from CPU1 of the computer A will extract the movement information and fault information stored in memory storage, such as FDD connected to the memory storage 2 of the computer A, and the input/output device 3.
[0023]An operator is told about what the extracted operation information and fault information were memorized for by the memory storage connected to the memory storage 12 and the input/output device 13 via the input/output device 13.
[0024]The memory storage 12 memorizes the operation information and fault information of the extracted computer A. A display, FDD, HDD, etc. are connected to the input/output device 13. Interface Division 14 is connected with Interface Division 4 of the computer A.
[0025]Next, operation of the constituted operation information and the fault information extraction system is explained like ****. First, an operator connects the information extraction equipment B to Interface Division 4 of the computer A. Then, CPU11 of the information extraction equipment B outputs an interrupt signal to CPU1 of the computer A, and requires release of the main bus 5 of the computer A.
[0026]If the release request of the main bus 5 is outputted from CPU11 of the information processing equipment B, while the main bus 5 will be released by CPU1 of the computer A, it is reported that the main bus 5 was released by CPU11 of the information extraction equipment B. It is reported that information extraction is performed to the operator of the computer A by CPU1 of the computer A via the input/output device 3.
[0027]From CPU1 of the computer A, if the notice of the purport that the main bus 5 was released is issued, CPU9 of the information extraction equipment B extracts operation information and fault information from the memory storage 2 of the computer A, and the input/output device 3, and it stores in the memory storage 12 of the information extraction equipment B.
[0028]Next, CPU11 of the information extraction equipment B notifies CPU1 of the computer A that release of the main bus 5 is canceled. And CPU11 of the information extraction equipment B tells an operator about an end of information extraction operation via the input/output device 13.
[0029]Therefore, according to operation information and the fault information extraction system of this example, operation information and fault information of a static computer can be

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extracted easily, without being based on an operator which has a know how.
<2nd embodiment> drawing 2 is a figure showing composition of operation information and a fault information extraction system concerning the 2nd embodiment of this invention (embodiment corresponding to invention of Claim 2).
[0030]In the figure, C is a computer and D is information extraction equipment. The computer C comprises CPU21, the memory storage 22, the input/output device 23, Interface Division 24, the clock generator 25, and the clock control systems 26 and 27.
[0031]The above-mentioned memory storage 22, the clock generator 25, and Interface Division 24 each are connected to the main bus 28. The input/output device 23 is connected to the main bus 28 via the clock control system 27 via the clock control system 26 CPU21.
[0032]CPU21 notifies an operator that a clock supplied to CPU21 and the input/output device 23 by the above-mentioned clock control systems 25 and 27 was suspended via the input/output device 23.
[0033]The memory storage 22 memorizes operation information of the computer C, and fault information. A display, FDD, HDD, etc. are connected to the input/output device 23. Interface Division 24 is connected with Interface Division 34 of the information extraction equipment D.
[0034]The clock generator 25 generates a clock supplied to CPU21 and the input/output device 23 via the main bus 28. If an interrupt signal of a purport that Interface Division 34 of the information extraction equipment D was connected to Interface Division 24 of the computer C from CPU31 of the information extraction equipment D is outputted, the clock control system 26, A clock supplied to CPU21 via the main bus 28 from the clock generator 25 is suspended.
[0035]If an interrupt signal of a purport that Interface Division 34 of the information extraction equipment D was connected to Interface Division 24 of the computer C from CPU31 of the information extraction equipment D is outputted, the clock control system 27, A clock supplied to the input/output device 23 via the main bus 28 from the clock generator 25 is suspended.
[0036]The information extraction equipment D comprises CPU31, the input/output device 32, the memory storage 33, and Interface Division 34. These CPU31, the input/output device 32, the memory storage 33, and Interface Division 34 each are connected by the main bus 35.
[0037]CPU31 will output an interrupt signal to the clock control systems 26 and 27 of the computer C, if Interface Division 34 of the information extraction equipment D is connected to Interface Division 24 of the computer C.
[0038]Via the input/output device 32 of the information extraction equipment D, the start of extraction of operation information and fault information is notified to an operator, operation information and fault information are extracted from the memory storage 22 of the computer C, and the input/output device 23, and it stores in the memory storage 33 of the information extraction equipment D.
[0039]After extraction of the operation information and fault information to the memory storage 33 is completed, it reports that clock supply is resumed to the clock control systems 26 and 27 of the computer C, and CPU21 and the clock supply to the input/output device 23 are made to resume.
[0040]It is reported that extraction of fault information and operation information was completed to the operator via the input/output device 32 of the information extraction equipment D. A display, FDD, HDD, etc. are connected to the input/output device 32. Interface Division 34 is connected with Interface Division 24 of the computer C.
[0041]The memory storage 33 memorizes operation information and fault information of the extracted computer C. Next, operation of constituted operation information and a fault information extraction system is explained like ****.
[0042]First, an operator connects the information extraction equipment D to Interface Division 24 of the computer C. Then, CPU31 of the information extraction equipment D outputs an interrupt signal to the clock control systems 26 and 27 of the computer C.
[0043]The clock control systems 26 and 27 suspend a clock supplied to CPU21 of the computer C, and the input/output device 23 based on an interrupt signal, and CPU21 notifies CPU31 of the information extraction equipment D that supply of a clock was suspended.
[0044]Next, by CPU31 of the information extraction equipment D, a start of information

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extraction is notified to an operator via the input/output device 32, operation information and fault information are extracted from the memory storage 22 of the computer C, and the input/output device 23, and this extracted operation information and fault information are stored in the memory storage 33 of the information extraction equipment D.

[0045]After storing of operation information and fault information to the memory storage 33 is completed, it reports that CPU31 resumes supply of a clock to the clock control systems 26 and 27 of the computer C, and CPU21 and clock supply to the input/output device 23 are resumed by the clock control systems 26 and 27.

[0046]An end of storing of operation information and fault information to the memory storage 33 will report that information extraction was completed to an operator via the input/output device 32 by CPU31.

[0047]Therefore, as operation information and a fault information extraction system of this example also described the 1st above-mentioned embodiment, operation information and fault information of a static computer can be extracted easily, without being based on an operator which has a know how.

[0048]

[Effect of the Invention]As a full account was given above, according to the operation information and the fault information extraction system of this invention, the static operation information of a computer and fault information are easily extractable.

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D3

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(71)出願人　503121103
株式会社ルネサステクノロジ
東京都千代田区丸の内二丁目４番１号
(74)代理人　100080001
弁理士　筒井　大和
(72)発明者　三坂　智
東京都国分寺市東恋ヶ窪一丁目２８０番地
株式会社日立製作所中央研究所内
(72)発明者　佐圓　真
東京都国分寺市東恋ヶ窪一丁目２８０番地
株式会社日立製作所中央研究所内
(72)発明者　山田　哲也
東京都国分寺市東恋ヶ窪一丁目２８０番地
株式会社日立製作所中央研究所内

最終頁に続く

(54)【発明の名称】半導体集積回路装置および消費電力管理装置

(57)【要約】
【課題】機能ブロックの総要求電力を供給可能な電力予算値内に管理するように機能ブロックの実行スケジューリングを行うことにより、低消費電力で安定動作を実現する。
【解決手段】全ての機能ブロックに対して機能ブロック識別子を付け、消費電力管理装置が読み書き可能なＲＡＭ領域に、識別子とタスクの優先度と、電力状態を表す電力モード値と、電力状態の持続時間を表す電力モード時間を格納するリストの連結を可能とする。機能ブロック上で動作するタスクのスケジュールを管理する単数ないし複数のリンクリストと、現在高電力モードで実行中の機能ブロックを管理するリンクリストと、現在停止モードで停止中の機能ブロックを管理するリンクリストと、現在低電力モードで実行中の機能ブロックを管理するリンクリストを割り付けて前記消費電力管理装置で電源および動作クロックを制御する。
【選択図】　図1

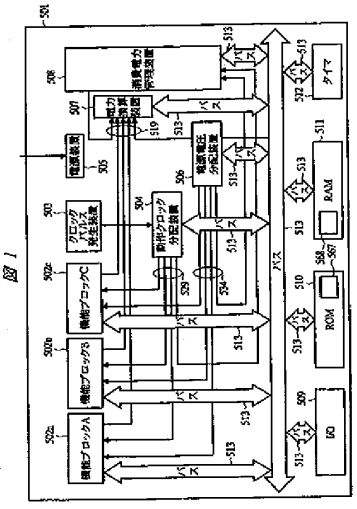


図1

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【特許請求の範囲】
【請求項１】
消費電力構成要素信号を出力するセンサと機能設定可能なレジスタを装備する単数ないし複数の機能ブロックと、不揮発性半導体メモリと、揮発性半導体メモリと、タイマとを有する半導体集積回路装置であって、
全ての前記機能ブロックからアクセスして消費電力の設定が可能なレジスタを装備し、さらに全ての前記機能ブロックに動作クロックを供給する動作クロック分配装置と、
全ての前記機能ブロックからアクセスして消費電力の設定が可能なレジスタを装備し、さらにすべての前記機能ブロックに電源電圧を供給する電源電圧分配装置と、
全ての前記消費電力構成要素信号を集計し加算して総要求電力値に変換し格納して任意の前記機能ブロックからもアクセスして前記総要求電力値を読み込ませることが可能な電力換算装置と、
前記タイマのタイマ割込みを受付且つ前記総要求電力値をロードする消費電力管理装置と、
前記機能ブロックと前記動作クロック分配装置と前記電源電圧分配装置と前記電力換算装置と前記消費電力管理装置と前記不揮発性半導体メモリと前記揮発性半導体メモリと前記タイマとの間を繋いで相互にデータを通信しあうことが可能なバスを装備し、
前記消費電力管理装置は、
予めロード済みで、電源の許容電力から任意のマージンを差し引いた値である電力予算値から、前記総要求電力値を引き算した電力結果値が負の場合は前記総要求電力値が前記電力予算値以下になるように前記動作クロック分配装置に対して前記動作クロックの遮断、または動作周波数の低減、または前記電源電圧分配装置に対して前記電源電圧の遮断を行うことを特徴とする半導体集積回路装置。
【請求項２】
請求項１記載の半導体集積回路装置において、
前記機能ブロックが実行開始直後であることを表す実行開始直後データを前記揮発性半導体メモリの所定共有メモリに書き込んだ後に前記消費電力管理装置に対して実行開始直後通知割込みイベントを発信し、前記消費電力管理装置が前記実行開始直後通知割込みイベントを受け付けて前記所定共有メモリから前記データを読み込み、保持をする、および
前記機能ブロックが実行開始直前であることを表す実行開始直前データを前記揮発性半導体メモリの所定共有メモリに書き込んだ後に前記消費電力管理装置に対して実行開始直前通知割込みイベントを発信し、前記消費電力管理装置が前記実行開始直前通知割込みイベントを受け付けて前記所定共有メモリから前記データを読み込む、保持をする、および
前記機能ブロックが実行終了直後であることを表す実行終了直後データを前記揮発性半導体メモリの所定共有メモリに書き込んだ後に前記消費電力管理装置に対して実行終了直後通知割込みイベントを発信し、前記消費電力管理装置が前記実行終了直後通知割込みイベントを受け付けて前記所定共有メモリから前記データを読み込み、保持をすることを特徴とする半導体集積回路装置。
【請求項３】
請求項２記載の半導体集積回路装置において、
前記機能ブロックが他の単数ないし複数の前記機能ブロックに対して命令を発行する場合、命令を発行する前記機能ブロックが実行開始直後通知割込みイベント、および実行開始直前通知割込みイベント、実行終了直後通知割込みイベントを発信することを特徴とする半導体集積回路装置。
【請求項４】
請求項３記載の半導体集積回路装置において、
前記消費電力管理装置が、前記消費電力管理装置それ自体に対して前記実行開始直後通知割込みイベント、および前記実行開始直前通知割込みイベント、前記実行終了直後通知割込みイベントを発信することを特徴とする半導体集積回路装置。
【請求項５】

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請求項４記載の半導体集積回路装置において、
前記機能ブロックおよび前記消費電力管理装置が前記実行開始直後通知割込みイベント、および前記実行開始直前通知割込みイベントを発信することにより、前記消費電力管理装置が前記電力予算値および前記総要求電力値を取得することを特徴とする半導体集積回路装置。
【請求項６】
請求項５記載の半導体集積回路装置において、
前記消費電力管理装置は、
タスク単位をスレッドおよびプロセスおよび命令が発行される機能ブロック単位とし、
全ての前記機能ブロックに対して機能ブロック識別子を割り振り、
タスクの管理を行う機能ブロック管理用リンクリストを全ての前記機能ブロックに対して装備し、電力モードが高電力モードで動作中の前記機能ブロックを管理する電力管理用リンクリストを装備し、前記電力モードが低電力モードで動作中の前記機能ブロックを管理する低電力管理用リンクリストを装備し、前記電力モードが停止モードの機能ブロックを管理するサスペンド用リンクリストを装備し、
前記機能ブロック管理用リンクリストおよび前記電力管理用リンクリストおよび低電力管理用リンクリストおよびサスペンド用リンクリストに挿入するリストには、前記タスク優先度および前記機能ブロック識別子および前記電力モードおよび前記電力モードの持続時間を設定する電力モード時間を格納し、
前記電力管理用リンクリストは前記リストを前記タスク優先度の低い順に並び替え、前記機能ブロック管理用リンクリスト、前記低電力管理用リンクリスト、および前記サスペンド用リンクリストは前記リストを前記タスク優先度の高い順に並び替えることにより、前記機能ブロックをスケジューリングすることを特徴とする半導体集積回路装置。
【請求項７】
請求項６記載の半導体集積回路装置において、
前記消費電力管理装置は、
前記実行開始直後通知割込みイベント、前記実行開始直前通知割込みイベント、前記実行終了直後通知割込みイベントを契機に、前記機能ブロック管理用リンクリストおよび前記電力管理用リンクリストおよび前記低電力管理用リンクリストおよび前記サスペンド用リンクリストは前記リストに対して前記スケジューリングを施すことを特徴とする半導体集積回路装置。
【請求項８】
請求項７記載の半導体集積回路装置において、
前記消費電力管理装置は、
前記タイマからのタイマイベントを周期イベントおよびアラームイベントに変換する時間管理部を装備し、前記周期イベントおよび前記アラームイベントを契機に、前記機能ブロック管理用リンクリストおよび前記電力管理用リンクリストおよび前記低電力管理用リンクリストおよび前記サスペンド用リンクリストは前記リストに対して前記スケジューリングを施すことを特徴とする半導体集積回路装置。
【請求項９】
請求項８の半導体集積回路装置において、
前記消費電力管理装置は、
前記電力結果値が負の場合、前記電力管理用リンクリストから最もタスク優先度の低い順に前記リストを外し、
外した前記リストに格納の前記電力モード時間をアラーム時間として前記時間管理部に設定し、
同じく格納の前記電力モードが前記低電力モードならば同じく格納の前記機能ブロック識別子に対応する前記機能ブロックを前記低電力モードに設定し、前記低電力管理用リンクリストにタスク優先度が高い順に外した前記リストを挿入し、
反対に同じく格納の前記電力モードが前記停止モードならば同じく格納の前記機能ブロ

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ック識別子に対応する前記機能ブロックを前記停止モードに設定し、前記サスペンド管理用リンクリストにタスク優先度が高い順に外した前記リストを挿入することを特徴とする半導体集積回路装置。

【請求項１０】

請求項９記載の半導体集積回路装置において、

前記消費電力管理装置は、

前記アラーム時間経過後、前記低電力管理用リンクリストないし前記サスペンド管理用リンクリストが空でない場合、最もタスク優先度が高い前記リストを外し、

外した前記リストに格納の前記機能ブロック識別子に対応する前記機能ブロックを前記高電力モードに設定し、

外した前記リストを前記電力管理用リンクリストから最もタスク優先度の低い順に挿入することを特徴とする半導体集積回路装置。

【請求項１１】

請求項１０記載の半導体集積回路装置において、

前記消費電力管理装置は、

前記機能ブロック管理用リンクリストが空になった際に動作クロックないし電源電圧を遮断することを特徴とする半導体集積回路装置。

【請求項１２】

請求項１１記載の半導体集積回路装置において、

前記消費電力管理装置は、

電源スイッチを同じくする前記機能ブロックの集合であって、前記集合の全ての前記機能ブロックに対応する前記機能ブロック管理用リンクリストが空になった際に動作クロックないし電源電圧を遮断することを特徴とする半導体集積回路装置。

【請求項１３】

請求項１２記載の半導体集積回路装置において、

前記消費電力管理装置は、

前記実行開始直後通知割込みイベントを契機に、前記実行開始直後データ内の前記タスク優先度、前記機能ブロック識別子、前記電力モード、前記電力時間を新規に前記リストに格納し、前記機能ブロック識別子に相当する前記機能ブロック管理用リンクリストに前記リストを前記タスク優先度の高い順に挿入後、前記リストを前記電力管理用リンクリストにタスク優先度の低い順に挿入することを特徴とする半導体集積回路装置。

【請求項１４】

請求項１３記載の半導体集積回路装置において、

前記消費電力管理装置は、

前記実行開始直前通知割込みイベントを契機に、前記実行開始直前データ内の前記タスク優先度、前記機能ブロック識別子、前記電力モード、前記電力時間を新規に前記リストに格納し、前記機能ブロック識別子に相当する前記機能ブロック管理用リンクリストに前記リストを前記タスク優先度の高い順に挿入後、前記リストを前記電力管理用リンクリストにタスク優先度の低い順に挿入し、

前記機能ブロック識別子に相当する機能ブロックに割り込みを発生することを特徴とする半導体集積回路装置。

【請求項１５】

請求項１４記載の半導体集積回路装置において、

前記消費電力管理装置は、

前記実行終了直後通知割込みイベントを契機に、前記実行終了直後データ内の前記機能ブロック識別子に相当する前記機能ブロック管理用リンクリストから最もタスク優先度の高い前記リストを外し、外した前記リストに格納の前記機能ブロック識別子に相当する前記リストを前記電力管理用リンクリストから外すことを特徴とする半導体集積回路装置。

【請求項１６】

消費電力構成要素信号を出力するセンサと機能設定可能なレジスタを装備する単数ない

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し複数の機能ブロックと、不揮発性半導体メモリと、揮発性半導体メモリと、タイマを有する半導体集積回路装置の消費電力を制御する消費電力管理装置であって、
前記消費電力管理装置は、
予めロード済みで、電源の許容電力から任意のマージンを差し引いた値である電力予算値から、総要求電力値を引き算した電力結果値が負の場合は前記総要求電力値が前記電力予算値以下になるように動作クロック分配装置に対して前記動作クロックの遮断、または動作周波数を低減することを特徴とする消費電力管理装置。
【請求項１７】
請求項１６記載の消費電力管理装置において、
前記消費電力管理装置は、
前記機能ブロックが実行開始直後であることを表す実行開始直後データを前記揮発性半導体メモリの所定共有メモリに書き込んだ後に発信された実行開始直後通知割込みイベントを受け付けて前記所定共有メモリから前記データを読み込み、保持し、
前記機能ブロックが実行開始直前であることを表す実行開始直前データを前記揮発性半導体メモリの所定共有メモリに書き込んだ後に発信された実行開始直前通知割込みイベントを受け付けて前記所定共有メモリから前記データを読み込み、保持し、
前記機能ブロックが実行終了直後であることを表す実行終了直後データを前記揮発性半導体メモリの所定共有メモリに書き込んだ後に発信する実行終了直後通知割込みイベントを受け付けて前記所定共有メモリから前記データを読み込み、保持をすることを特徴とする消費電力管理装置。
【発明の詳細な説明】
【技術分野】
【０００１】
本発明は、半導体集積回路装置における低消費電力化技術に関し、特に、半導体集積回路装置内の機能ブロックにおける電力消費管理に有効な技術に関する。
【背景技術】
【０００２】
近年、携帯電話、ディジタルカメラ、携帯オーディオプレーヤーなどのバッテリ駆動型や、ディジタルテレビ、ディジタルビデオディスクプレイヤー、ディジタルハードディスクレコーダなどの据え置き型のディジタル家電などは、小型薄型軽量化が進んでおり、ディジタルＬＳＩ（Ｌａｒｇｅ　Ｓｃａｌｅ　Ｉｎｔｅｇｒａｔｉｏｎ）などの半導体集積回路装置が広く用いられている。
【０００３】
ディジタルＬＳＩを生産する半導体の微細化加工技術は年々発展を遂げており、例えばＣＭＯＳ（Ｃｏｍｐｌｅｍｅｎｔａｒｙ　Ｍｅｔａｌ　Ｏｘｉｄｅ　Ｓｅｍｉｃｏｎｄｕｃｔｏｒ）回路のゲート幅や酸化膜厚などを薄くすることにより、ディジタルＬＳＩそれ自体を薄く小さく生産することが可能になった。ディジタルＬＳＩの小型薄型軽量化こそ、半導体の価値とされている。
【０００４】
また前記ゲート幅や前記酸化膜厚を薄くする為、ディジタルＬＳＩに印加する電源電圧も同時に低くする必要がある。その結果、一世代前の微細化加工技術で生産したディジタルＬＳＩと同じ処理性能以上の確保、つまり同じ動作周波数以上の駆動が可能なディジタルＬＳＩを生産するためには、前記酸化膜厚に対する耐圧の関係上、前記電源電圧を低くすることと同時に、前記ディジタルＬＳＩよりもしきい値電圧を低くする必要がある。
【０００５】
しかししきい値電圧を低くしていくと、ディジタルＬＳＩが駆動してもしなくても、つまりＣＭＯＳ回路がスイッチングしてもしなくても、電源電圧が印加されている限り、電流が漏れてエネルギーが勝手に消費されるという特性を持つリーク電流の増加が顕著になる。
【０００６】

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２０００年より以前ではＣＭＯＳ回路が実際に駆動することによりエネルギーを消費するという特性を持つスイッチング電流が全消費電力の大部分を占めていた。しかし２０００年以降は微細化加工技術の発展に伴い、リーク電流によるエネルギー消費の割合が指数的に占めてくると予想されている。

【０００７】

そこで前記ディジタルＬＳＩと同じ処理性能以上のディジタルＬＳＩを、電源電圧を低く、動作周波数を高くして実現するのではなく、電源電圧は可能な限り低く設定せず、つまりしきい値電圧の低下を抑えて、同様な複数の処理機構を並列駆動して実現するという方向に進みつつある。

【０００８】

例えば、一つの高速プロセッサを実現するのではなく、前記動作周波数と同程度である代わりに、並列動作可能な複数のプロセッサおよびＡＳＩＣ（Ａｐｐｌｉｃａｔｉｏｎ Ｓｐｅｃｉｆｉｃ Ｉｎｔｅｇｒａｔｅｄ Ｃｉｒｃｕｉｔ）の混載チップを実現することに相当する。

【０００９】

その方が今後の前記リーク電流の指数的増加の抑制が図れて且つ、微細化加工技術により、半導体の価値とされている、ディジタルＬＳＩの小型薄型軽量化も実現し易くなる。

【００１０】

さらにディジタルＬＳＩの小型薄型軽量化が実現できると、前記ディジタルＬＳＩと同じチップ面積で且つ、更なる処理機能を付加することで製品の差別化を行う為、前記混載チップよりもさらに並列処理が可能な複数個のプロセッサおよびＡＳＩＣを搭載すること、つまり集積化が必然的に行われる。

【００１１】

しかし集積化により、単位チップ面積当たりのＣＭＯＳ回路規模を表すトランジスタ数が増加し、ＬＳＩが大負荷容量化し、スイッチング電流による消費電力が増加する。２０１０年辺りでは１チップ当りプロセッサやＡＳＩＣの搭載数が数十個から百個前後と見込まれており、電源電圧が飽和状態になりながらも低くなっていくのとは反対に、前記スイッチング電流やリーク電流の合計である消費電流は１チップに搭載するプロセッサやＡＳＩＣの搭載数に比例して増加の一途を辿っていくと考えられる。

【００１２】

今後、ディジタルＬＳＩの微細化および集積化に起因した低電圧、大電流時代において解決すべき問題が主に２つ、発生しつつある。一つはディジタルＬＳＩ自体が熱の発生源となって生じる熱設計電力問題、もう一つはディジタルＬＳＩ自体が電磁雑音の発生源となって生じる電磁雑音対策問題である。

【００１３】

熱設計電力問題は、熱計算式を用いてディジタルＬＳＩのパッケージを設計する際に伴う問題である。ディジタルＬＳＩが駆動している、していないに関わらず、電流が消費した分、消費電力は熱に変換し、ディジタルＬＳＩ自身のチップ温度を上昇させる。

【００１４】

チップ温度には動作保証温度の範囲が存在し、前記温度範囲を超えるとディジタルＬＳＩは誤動作し、最悪の場合は、ＣＭＯＳ回路が破損して動作不可能に陥ることがある。パーソナルコンピュータなどではＬＳＩ近傍に冷却ファンを設置することでチップ温度の上昇を抑制している。

【００１５】

しかし前記冷却ファンは騒音となるのでディジタル家電への実装は好まれない。またヒートシンクなど、熱を拡散させる経路をパッケージに設けて、同様にチップ温度の上昇を抑制している例もある。

【００１６】

今後、ディジタルＬＳＩに対して微細化且つ集積化を施していくと消費電流の増加と共に前記チップ温度も上昇し、前記チップ温度が前記動作保証温度の範囲を超す恐れがあり

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、問題となる。

【００１７】

また電磁雑音対策問題は、ディジタルＬＳＩから前記ディジタルＬＳＩを搭載するボードに至るまでの半導体集積回路装置全体のシステム設計に関わる問題である。電磁雑音は、ボードに搭載されるディジタルＬＳＩと電池までも含む、全電源配線回路の抵抗成分で起こる消費電流の直流成分電圧の値と、前記全電源配線回路で形成されるインダクタンス成分で起こる消費電流の交流成分電圧変化の値の合計値である。

【００１８】

前記直流成分電圧の値は前記全電源配線回路の抵抗の値Ｒと消費電流の値Ｉの積ＩＲに相当する。また、前記交流成分電圧変化の値は前記全電源配線回路のインダクタンスの値Ｌと消費電流の単位時間当たりの変化率ｄＩ／ｄｔの積Ｌ（ｄＩ／ｄｔ）に相当する。

【００１９】

電磁雑音には、許容できる動作電圧マージンが存在し、動作電圧マージンは前記電源電圧の約５％に相当する電圧とされている。

【００２０】

しかし微細化に伴い、電源電圧は飽和状態ではあっても低くなっているので動作電圧マージンも小さくなる。一般的に電磁雑音は前記動作電圧マージンの範囲内に収める必要がある。

【００２１】

もし電源雑音が動作電圧マージンの範囲を超すと、本来一定であるべき電源電圧や接地電位が激しく変動するなど、電力品質（Ｐｏｗｅｒ　Ｉｎｔｅｇｒｉｔｙ）が悪化する。

【００２２】

そして同時に各回路間の信号品質（Ｓｉｇｎａｌ　Ｉｎｔｅｇｒｉｔｙ）も悪化し、ＬＳＩが誤動作し、最悪の場合は不要輻射、つまり不要な電磁波の発生により、ＥＭＩ（Ｅｌｅｃｔｒｏｍａｇｎｅｔｉｃ　Ｉｎｔｅｒｆａｃｅ）が許容値を超えてしまって環境問題となる。

【００２３】

今後、ディジタルＬＳＩに対して微細化且つ集積化を施していくと消費電流や消費電流の時間変化率が増加し易くなり、今後小さくなっていく前記動作電圧マージンの範囲を前記電磁雑音が超してしまう恐れがある。

【００２４】

従って、微細化および集積化によって小型薄型軽量化および多機能化を維持しながらディジタルＬＳＩを生産するには、今後増加していく消費電流が主要素と成る前記チップ温度を前記動作保証温度の範囲内に、さらに同じく主要素と成る電源雑音を動作電圧マージンの範囲内に抑制する為、半導体集積回路装置の最大電力以内で電力の供給が可能な電力予算値を予め設定しておき、前記電力予算値の範囲内でアプリケーション仕様を満足することが可能な機構、工夫をディジタルＬＳＩに施す必要がある。

【００２５】

一般的に消費電流を小さくする技術として２つの技術が考えられる。一つは、ディジタルＬＳＩに搭載される複数のプロセッサやＡＳＩＣに対して、電源電圧を断つ電源遮断や動作クロックを断つ動作クロック遮断などを施す電力ゲーティング技術で、もう一つは同じく前記プロセッサやＡＳＩＣに対して、電源電圧ないし動作周波数を制御する電力コントロール技術である。

【特許文献１】特開平８－１５２９４５号公報

【発明の開示】

【発明が解決しようとする課題】

【００２６】

本願発明者などは本願に先立って、前記ディジタル家電を対象に特許文献１の従来技術である消費電力管理装置について検討した。特許文献１は、前記電力コントロール技術を用い、前記電力予算値以内でアプリケーション仕様を満足させることを特徴とした消費電

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力管理装置に関する特許である。また特許文献１では前記電力ゲーティング技術の使用も範疇になっている。課題抽出に先立ち、特許文献１について説明する。

【００２７】

図２１は、特許文献１の図４に記載の消費電力管理装置の構成図であり、図２２は、特許文献１の図２に記載の消費電力管理装置の構成図である。

【００２８】

機能ブロック１１１は、現在の負荷状況から必要な電力を要求する。情報集計装置１０４は、各機能ブロックからの要求電力を加算集計する。供給電力分配決定装置１０２は、加算集計された電力の総和が供給可能な電力値以内の場合は、電力分配装置１０５に指示して各機能ブロックに電力要求を出力し、電力の総和が供給可能な電力値を超えた場合には、予め定められた方法によって電力分配方法を決定し、電力分配装置１０５に指示して各機能ブロックに供給可能な電力を電力分配方法に従って分配し出力する。

【００２９】

このような構成の消費電力管理装置による消費電力管理技術では、以下の課題が残されている。

【００３０】

まず、第一の課題として、例えば機能ブロック１１１が処理内容を柔軟に変えることが可能なプロセッサの場合、電力値の固定化が図れるＡＳＩＣとは異なり、処理内容つまりタスク毎に前記要求電力が異なることで電力分配２０３の組合せが多く複雑になってしまい、電力分配候補表装置２０２の実装が困難になってしまうという問題がある。

【００３１】

また、消費電力管理装置４０１は、所望の複数の機能ブロック１１１が動作しても電力分配候補表装置２０２、選択装置２０４および分配装置２０６を搭載し、適切な電力分配２０３で電力分配装置１０５を設定することにより、前記電力予算値以内に前記電力供給制御を可能としている。

【００３２】

しかし、第二の課題として、例えば処理の過程で電力分配装置１０５が低電源電圧且つ低動作周波数つまり低く電力を供給した前記機能ブロックが所定の処理を満足して終了した場合、前記優先度と前記電力分配方法の内容が不明な為、電力分配装置１０５に高い電力を供給することができずに今後常に高速処理状態に戻せないという恐れが生じる。

【００３３】

また処理の過程で総要求電力が電力予算値を超えた場合、例えばある優先度に従ってある機能ブロック１１１に対して前記電力ゲーティング技術を使って前記総要求電力を低くした場合、前記機能ブロック１１１の処理が前記消費電力管理装置４０１に止められている為、前記消費電力管理装置４０１が前記機能ブロック１１１を放置しておくと後々動作することができず、アプリケーション仕様のデッドラインを満たせないという恐れが生じる。

【００３４】

従って前記優先度に基づいて停止状態にある前記機能ブロック１１１に対して時間を設定して前記停止状態を解除して電力を供給することなどの作業が必要である。

【００３５】

第三の課題は、前記消費電力管理装置４０１の消費電力も総要求電力に加えることである。

【００３６】

前記ディジタルＬＳＩを１つのディジタルＬＳＩで実現する場合、前記消費電力管理装置４０１も含めた総要求電力を電力予算値以内する必要が生じる。

【００３７】

また、第四の課題は、電源ＩＣの許容電力以内に前記ディジタルＬＳＩの最大電力値を制限することである。

【００３８】

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多くの機能ブロックの同時駆動による急激な大総要求電力のサンプリングを前記消費電力管理装置が逃してしまう、つまり電力予算値との比較のタイミングがずれてしまうと、電源ＩＣの許容電力を超してしまい、十分な電力が各機能ブロックに供給できず、処理が破綻し不具合が生じる。

【００３９】

従って精度高く前記許容電力以内に電力のマージンを見積もって前記最大電力を制限することが必要である。

【００４０】

第五の課題は、機能ブロックのある集合がアイドル状態にあるか判別することである。

【００４１】

前記ディジタルＬＳＩを１つの半導体集積回路装置で実現する場合、機能ブロック毎に電源電圧分配装置を設けることが理想であるが、ディジタルＬＳＩのチップ面積の肥大化を抑える為、相関のある機能ブロックの集合に対して電源電圧分配装置を割り当てて実装することが多々ある。

【００４２】

そこで前記集合に属する機能ブロックの全てがアイドル状態になっていることが分れば、前記集合に所属の機能ブロックに対して纏めて電源電圧の遮断を施せ、低消費電力化の実現が可能となる。

【００４３】

第六の課題は、機能ブロック１１１が複数搭載しても前記消費電力管理装置以外の機能ブロックでも電力を設定できるようにすることである。

【００４４】

機能ブロック１１１がプロセッサやコントローラとしてみなした場合、通常、機能ブロックを動かすソフトウェアから電力分配装置１０５の電源電圧の値や動作周波数の設定を換えることができており、例えば機能ブロックが所定の処理を終えてアイドル状態に入る際に前記ソフトウェアの設定により、前記機能ブロック自ら停止状態にすることができ、低消費電力の実現が可能になる。

【００４５】

しかし特許文献１における消費電力管理装置４０１では、該消費電力管理装置でしか電力の設定ができないので、機能ブロックから電力を設定できる仕掛けが必要となってしまうことになる。

【課題を解決するための手段】

【００４６】

本願において開示される主な発明の要点は以下のとおりである。

【００４７】

半導体集積回路装置は、単数ないし複数の機能ブロックと、機能ブロックの総要求電力を管理して各機能ブロックの供給電力を決定する消費電力管理装置と、機能ブロック毎および消費電力管理装置に動作クロックを供給する動作クロック分配装置と、機能ブロック毎および消費電力管理装置に電源電圧を供給する電源電圧分配装置と、機能ブロックおよび消費電力管理装置における消費電力構成要素信号を集計して総要求電力に換算する電力換算装置と、機能ブロックおよび消費電力管理装置が読み書きできるＲＡＭなどの揮発性半導体メモリと、機能ブロックおよび消費電力管理装置が読めるＲＯＭなどの不揮発性半導体メモリと、タイマで構成し、それぞれをバスで繋ぎ、データ送受信を可能にする。

【００４８】

全ての機能ブロックに対して識別子を付け、前記機能ブロックと前記消費電力管理装置が読み書き可能なＲＡＭ領域に相当するローカルメモリ領域上に、前記識別子と前記機能ブロック上で動作するタスクに割り当てたタスクの優先度と、機能ブロックが高電源電圧、高速動作クロックで動作する高電力モードまたは低電源電圧、低速動作クロックで動作する低電力モードまたは停止状態とする停止モードを表す電力モード値と、前記低電力モードまたは前記停止モードの持続時間を表す電力モード時間をパラメータとして格納する

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リストを設け、前記リストと連結可能な、前記タスクのスケジュールを管理する単数ないし複数の機能ブロック対応リンクリスト（機能ブロック管理用リンクリスト）と、現在高電力モードで実行中の機能ブロックを管理する電力管理用リンクリストと、現在停止モードで停止中の機能ブロックを管理するサスペンド用リンクリストと、現在低電力モードで実行中の機能ブロックを管理する低電力管理用リンクリストを用意する。

【００４９】

ある機能ブロックを利用する際には、前記機能ブロックの識別子に対応する機能ブロック対応リンクリストに、前記機能ブロック上で動作するタスクの前記優先度と前記識別子と高電力モードを表す電力モード値と電力モード時間を書き込んだリストを前記優先度の高い順番に挿入して連結し、同時に電力管理用リンクリストに全ての前記機能ブロック対応リンクリストの先頭リストを前記優先度の低い順に連結する。

【００５０】

もし前記総要求電力が電源ＩＣの許容電圧からマージン電圧を引いた値に相当する電力予算値を超えない場合は電力分配装置の設定は不動にする。

【００５１】

反対にもし超えて且つ電力供給を停止してもアプリケーション仕様に悪影響を及ぼさない場合は、タイマを管理する時間管理部に停止モードを表す電力モード値と電力モード時間を設定し、電力管理用リンクリストの先頭リストに前記電力モード値と前記電力モード時間を格納し、電力管理用リンクリストから前記先頭リストを外し、外した前記先頭リストに格納の識別子に対応した機能ブロックに供給している動作クロックや電源電圧を前記電力分配装置で遮断して前記機能ブロックを停止モードにさせ、外した前記先頭リストをサスペンド用リンクリストに前記優先度の高い順に連結する。

【００５２】

同じくもし超えて且つ電力供給を停止してもアプリケーション仕様に悪影響を及ぼす場合は、時間管理部に低電力モードを表す電力モード値と電力モード時間を設定し、電力管理用リンクリストの先頭リストに前記電力モード値と前記電力モード時間を格納し、電力管理用リンクリストから前記先頭リストを外し、外した前記先頭リストに格納の識別子に対応した機能ブロックに供給している動作クロックや電源電圧を前記電力分配装置で下げて前記機能ブロックを低電力モードにさせ、外した前記先頭リストを低電力用リンクリストに前記優先度の高い順に連結する。

【００５３】

またある機能ブロックの利用が終了した際には、サスペンド用リンクリストの先頭リストに格納の識別子に対応した機能ブロックに供給している動作クロックや電源電圧を前記電力分配装置で上げて、前記先頭リストを外して前記電力管理用リンクリストに低い優先度順に再挿入すると同時に、低電力用リンクリストの先頭リストに格納の識別子に対応した機能ブロックに供給している動作クロックや電源電圧を前記電力分配装置で上げ、前記先頭リストを外して前記電力管理用リンクリストに低い優先度順に再挿入した後、終了した前記機能ブロック対応リンクリストの先頭リストを削除する。

【００５４】

前記時間管理部に設定した前記電力モード時間経過後に前記時間管理部から出力される前記電力モード値が停止モードを表していれば、サスペンド用リンクリストの先頭リストに格納の識別子に対応する電力分配装置の動作クロックや電源電圧の遮断を解除し、サスペンド用リンクリストから前記先頭リストを外して電力管理用リンクリストに再挿入する。

【００５５】

同じく前記電力モード値が低電力モードを表していれば、低電力用リンクリストの先頭リストに格納の識別子に対応する電力分配装置を動作クロックや電源電圧を上げて、低電力用リンクリストから前記先頭リストを外して電力管理用リンクリストに再挿入する。

【００５６】

以上、提案する手段のうち、ローカルメモリ上に前記機能ブロック対応リンクリスト、

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前記電力管理用リンクリスト、前記サスペンド用リンクリストおよび前記低電力用リンクリスト等の線形リンクリストを設けることにより、電力分配候補表のような機能ブロックの数および電力分配が固定された表では不可能であったスケーラブルな機能ブロックの追加および削除に対しても、また前記機能ブロックがプロセッサでオペレーティングシステム（以下、ＯＳとする）によってタスクがスケーラブルに追加および削除されても、柔軟に容易に実装および運用を図ることができ、これにより第一の課題を解決することができる。

【００５７】

そして提案する手段のうち、前記識別子と情報処理装置に対して割り当てたタスクの優先度と、機能ブロックが高電源電圧、高速動作クロックで動作する高電力モードまたは低電源電圧、低速動作クロックで動作する低電力モードまたは停止状態とする停止モードを表すモード値と、前記低電力モードまたは前記停止モードの持続時間を表すモード時間をパラメータとして格納するリストを、前記機能ブロック対応リンクリスト、前記電力管理用リンクリスト、前記サスペンド用リンクリストおよび前記低電力用リンクリストで管理することにより、一旦、前記機能ブロックが前記停止状態や前記低電力状態になっても、前記モード時間後に電力分配装置に高い電力を供給することができるので、第二の課題を解決することができる。

【００５８】

さらに同じく提案する手段のうち、半導体集積回路装置を単数ないし複数の前記機能ブロックと、前記消費電力管理装置と、前記動作クロック分配装置と、前記電源電圧分配装置と、前記電力換算装置と、前記揮発性半導体メモリと、前記不揮発性半導体メモリで構成してそれぞれをバスで繋ぎ、データ送受信を可能にすることで、機能ブロックおよび消費電力管理装置から自分自身の電力を設定できる仕組みと、該消費電力管理装置の消費電力も総要求電力に加える仕組みを設けることが可能となり、第三の課題ならびに第六の課題を解決することができる。

【００５９】

またさらに、前記消費電力管理装置は、電源、例えば前記電源ＩＣの許容電力から電力マージン値を引いた値である電力予算値と前記総要求電力との比較により、前記総要求電力を前記許容電力以下になるように管理する。前記電力予算値とすることで、精度よく、前記許容電力以内に前記総要求電力を収めることが可能となり、第四の課題を解決することができる。

【００６０】

最後に相関のある機能ブロックの集合に対して前記電源電圧分配装置を割り当てている場合、前記集合の全ての機能ブロックの識別子に対応する機能ブロック対応リンクリストに前記リストが連結されているかどうかの判別を行うことにより、全ての前記識別子に対応する前記電源電圧分配装置で電源電圧を遮断することが可能となり、第五の課題を解決することができる。

【００６１】

本発明の目的は、単数ないし複数の機能ブロックの総要求電力を供給可能な電力予算値内に管理するように機能ブロックの実行スケジューリングを行うことにより、低消費電力で安定動作を実現することのできる技術を提供することにある。

【００６２】

本発明の前記ならびにそのほかの目的と新規な特徴については、本明細書の記述および添付図面から明らかになるであろう。

【発明の効果】

【００６３】

本願において開示される発明のうち、代表的なものによって得られる効果を簡単に説明すれば以下のとおりである。

【００６４】

半導体集積回路装置に搭載の機能ブロックのスケーラブルな追加および削減に対して柔

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軟に容易に実装および運用することが可能となり、低消費電力効果および安定動作を達成することができる。

【発明を実施するための最良の形態】

【００６５】

以下、本発明の実施の形態を図面に基づいて詳細に説明する。なお、実施の形態を説明するための全図において、同一の部材には原則として同一の符号を付し、その繰り返しの説明は省略する。

【００６６】

図１は、本発明の代表例のハードウェア構成の実施例を説明する図である。

【００６７】

半導体集積回路装置５０１は単数ないし複数の機能ブロック５０２と、クロックパルス発生装置５０３と、動作クロック分配装置５０４と、電源装置５０５、電源電圧分配装置５０６と、電力換算装置５０７と、消費電力管理装置５０８と、Ｉ／Ｏ装置５０９と、ＲＯＭ（不揮発性半導体メモリ）５１０と、ＲＡＭ（揮発性半導体メモリ）５１１、タイマ５１２、およびバス５１３で構成される。

【００６８】

機能ブロック５０２、動作クロック分配装置５０４、電源電圧分配装置５０６、電力換算装置５０７と、消費電力管理装置５０８と、Ｉ／Ｏ装置５０９と、ＲＯＭ５１０、ＲＡＭ５１１、およびタイマ５１２はバス５１３を介して接続されている。

【００６９】

図２は、機能ブロックとバスの関係を説明する図である。

【００７０】

機能ブロック５０２は、ＡＳＩＣ、アクセラレータなどの専用回路や、プロセッサ、ＤＳＰ、ＦＰＵ、およびＦＰＧＡなどのＲＯＭ５１０、ＲＡＭ５１１に格納したソフトウェアに従ってプログラマブルに命令制御、データ処理などを実施する汎用回路に相当する。それぞれの機能ブロックには割込み受付装置５１４を内蔵する。

【００７１】

バス５１３は、機能ブロック５０２で発行する命令を実行する命令制御線５１５および機能ブロック５０２がＲＯＭ５１０、ＲＡＭ５１１で読み書きを実施するデータ転送線５１６で構成するが、本明細書では説明し易くする為、さらに単数ないし複数の割込み受信線５１７、割込み発信線５１８も構成に加える。

【００７２】

また機能ブロック５０２には消費電力構成要素信号５１９を測定する電力センサ５２０を実装する。電力センサ５２０は逐次、電力換算装置５０７に消費電力構成要素信号５１９を転送する。電力センサ５２０は例えばＣＭＯＳ回路のスイッチング回数などを計測するパフォーマンスカウンター、熱量を測る温度センサ、消費電流や電圧を測る電力モニタ、などに相当する。

【００７３】

図３は、電力換算装置を説明する図である。

【００７４】

電力換算装置５０７は、電力変換装置５２１と加算器５２２と総要求電力格納レジスタ５２３で構成する。

【００７５】

電力変換装置５２１は、消費電力構成要素信号５１９を機能要求電力値に変換する。加算器５２２は、全ての機能要求電力値を合計して得られた総要求電力を総要求電力格納レジスタ５２３に逐次、格納する。

【００７６】

図４は、クロックパルス発生器と動作クロック分配装置を説明する図である。

【００７７】

クロックパルス発生装置５０３は例えば水晶子として実装し、パルス５２４を発生する

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【００７８】

動作クロック分配装置５０４は、全ての機能ブロック５０２と消費電力管理装置５０８に対応したＰＬＬ（Ｐｈａｓｅ Ｌｏｃｋｅｄ Ｌｏｏｐ）回路５２５、分周器５２６、動作クロック遮断装置５２７、動作周波数状態制御レジスタ５２８で構成する。

【００７９】

動作クロック分配装置５０４はクロックパルス発生装置５０３で発生したパルス５２４をＰＬＬ５２５で逓倍化し、その結果を分周器５２６で動作クロック５２９に変換して、各機能ブロック５０２に出力する。

【００８０】

動作周波数状態制御レジスタ５２８は設定に従って所定の機能ブロック５０２に対する動作クロック５２９を遮断する。また同じく動作周波数状態制御レジスタ５２８のビットパターンの設定に従ってＰＬＬ５２５および分周器５２６を変更して所望の動作周波数を機能ブロック５０２に供給する。

【００８１】

図５は、電源装置と電源電圧分配装置を説明する図である。

【００８２】

電源装置５０５は例えば電池電圧５３０を電源電圧５３１に変換する電源ＩＣとして実装し、電源電圧５３１を機能ブロック５０２と消費電力管理装置５０８に供給する。また電源回路の系統として、電源装置５０５の他に電源スイッチ５３２を機能ブロック５０２に実装する。

【００８３】

電源電圧分配装置５０６は、電源スイッチ５３２を設定する電源スイッチレジスタ５３３を有し、電源スイッチレジスタ５３３のビットパターンを設定することにより、所定の機能ブロック５０２の電源スイッチ５３２をＯＮまたはＯＦＦにする電源スイッチ制御信号５３４を送り、電源電圧５３１を供給したり遮断したりする。

【００８４】

図６は、本発明の代表的な消費電力管理装置の実施例を説明する図である。

【００８５】

消費電力管理装置５０８は、命令解読装置５３５、割込み受付装置５１４、割込み発生装置５３６、時間管理装置５３７、リスト登録装置５３８、リスト解除装置５３９、電力予算値取得装置５４０、事象処理装置５４１、および電力センサ５２０から構成される。また消費電力管理装置５０８には、バス５１３とタイマ５１２を繋ぐ。

【００８６】

図が複雑になる為、記述はしないが、タイマ５１２は機能ブロック５０２の同種類とする。タイマ５１２は動作クロック分配装置５０４から入力した動作クロック５２９をタイマイベント５４２に変換する。

【００８７】

割込み受付装置５１４はタイマイベント５４２でタイマ割り込みがあったことを時間管理装置５３７に知らせる。

【００８８】

時間管理装置５３７はタイマイベント５４２の入力の度にシステム時刻メモリ５４３に１ずつ加算し、タイマ割込み回数をカウントする。

【００８９】

また時間管理装置５３７は、機能ブロック５０２から所定の周期時間をカウントダウンメモリＡ５４４ａに設定することにより、タイマイベント５４２の度にカウントダウンメモリＡ５４４ａから１ずつ減算していって０になった時に周期イベント５４５ａを発生し、事象処理装置５４１に起動をかけ、自動的にカウントダウンメモリＡ５４４ａに前記周期時間の再設定、周期イベント５４５ａを繰り返す。

【００９０】

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さらに時間管理装置５３７は、機能ブロック５０２から所定のアラーム時間をカウントダウンメモリＢ５４４ｂに設定することにより、タイマイベント５４２の度にカウントダウンメモリＢ５４４ｂから１ずつ減算していって０になった時にアラームイベントを発生し、事象処理装置５４１に起動をかける。

【００９１】

事象処理装置５４１は、総要求電力値取得装置５４５、電力予算値レジスタ５４６、減算器５４７、比較器５４８、電力正常処理部５４９、電力異常処理部５５０、および電力遮断処理部５５１で構成する。

【００９２】

事象処理装置５４１が起動すると、命令解読装置５３５は総要求電力値取得装置５４５に対して、電力換算装置５０７の総要求電力格納レジスタ５２３からバス５１３経由で前記総要求電力を取得し総要求電力値取得装置５４５に格納する。

【００９３】

次に事象処理装置５４１は減算器５４７で電力予算値レジスタ５４６に格納の電力予算値から総要求電力値取得装置５４５に格納の前記総要求電力を引き算した減算結果を比較器５４８に入力する。

【００９４】

比較器５４８は前記減算結果が０以上かどうかを判別する。もし前記減算結果が０以上ならば電力正常処理部５４９に、反対にマイナスならば電力異常処理部５５０に実行を移す。

【００９５】

最後に電力正常処理部５４９および電力異常処理部５５０の実行後、電力遮断処理部５５１に実行を移す。

【００９６】

消費電力管理装置５０８は、機能ブロック５０２からの割込みを割込み受付装置５１４が受け取ると、命令解読装置５３５に実行を移す。

【００９７】

命令解読装置５３５は割込み要因の種類によって、リスト登録装置５３８、リスト解除装置５３９、電力予算値取得装置５４０、時間管理装置５３７の何れかに実行を移す。

【００９８】

リスト登録装置５３８およびリスト解除装置５３９は処理終了直後に、事象処理装置５４１に対して起動イベント５５２をかける。

【００９９】

割込み発生装置５３６は電力正常処理部５４９で用いる。

【０１００】

図７は、機能ブロックと消費電力管理装置を動かすソフトウェアを説明する図である。

【０１０１】

また本明細書では機能ブロック５０２間におけるマスタとスレーブの関係は、マスタ機能ブロックはスレーブ機能ブロックに命令を下し、スレーブ機能ブロックはスレーブ機能ブロックの所定の処理終了後にマスタ機能ブロックに対して割込みを発生し、マスタ機能ブロックは前記割込みを受け付ける、と定義する。

【０１０２】

またタスクの定義を、マスタ機能ブロック上で動作するＯＳが管理するスレッドまたはプロセスと、スレーブ機能ブロックとする。つまりスレッド、プロセスおよびスレーブ機能ブロック単位がタスク単位となる。但し、スレーブ機能ブロック上にＯＳが搭載した場合はスレーブ機能ブロックが単位ではなく、スレーブ機能ブロック上で動作するスレッドまたはプロセスがタスク単位となる。

【０１０３】

従って図７の機能ブロックＡ５０２ａはマスタ、機能ブロックＢ５０２ｂはスレーブ、という関係となる。また機能ブロックＡ５０２ａと消費電力管理装置５０８との関係はお

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互いにマスタ、またはスレーブとなる。

【０１０４】

消費電力管理装置５０８は、前記専用回路、前記汎用回路のどちらで実装しても構わないが、以降では前記汎用回路、つまりプロセッサを用いることを想定して説明を続ける。

【０１０５】

機能ブロックＡ５０２ａ上で動作するソフトウェアは、ＯＳ＿Ａ５５３ａ、機能ブロックＡ用ソフトウェア５５４、機能ブロックＢ制御ソフトウェア５５５、電力設定ソフトウェア５５６、機能ブロック間通信ソフトウェア５５７、およびアプリケーションソフトウェア５５８で構成し、消費電力管理装置５０８上で動作するソフトウェアは、ＯＳ＿Ｘ５５３ｘ、電力設定ソフトウェア５５６、機能ブロック間通信ソフトウェア５５７、および電力管理アプリケーションソフトウェア５５９で構成する。

【０１０６】

アプリケーションソフトウェア５５８は、ＯＳ＿Ａ５５３ａが管理するスレッド５６０で構成し、スレッド５６０からＯＳ＿Ａ５５３ａのシステムコール５６１ａ、機能ブロックＡ用ソフトウェア５５４の機能ブロックＡ用アプリケーションプログラミングインターフェース（以下、ＡＰＩとする）５６２、機能ブロックＢ制御ソフトウェア５５５の機能ブロックＢ制御ＡＰＩ５６３、電力設定ソフトウェア５５６の電力設定ＡＰＩ５６４、および機能ブロック間通信ソフトウェア５５７の機能ブロック間通信ＡＰＩ５６５を呼び出し、アプリケーション仕様を実現する。

【０１０７】

同じく電力管理アプリケーションソフトウェア５５９は、ＯＳ＿Ｘ５５３ｘが管理するスレッド５６０で構成し、その内の電力管理スレッド５６６からＯＳ＿Ｘ５５３ｘのシステムコール５６１ｘ、電力設定ＡＰＩ５６４、および機能ブロック間通信ＡＰＩ５６５を呼び出し、電力管理アプリケーション仕様を実現する。

【０１０８】

スレッド５６０および電力管理スレッド５６６は、ＯＳ＿Ａ５５３ａおよびＯＳ＿Ｘ５５３ｘが提供するシステムコールＡ５６１ａ、システムコールＸ５６１ｘを呼び出すことで、スレッド管理、時間管理、同期非同期通信、などの機能を実現する。

【０１０９】

同じく、機能ブロックＡ用ソフトウェア５５４が提供する機能ブロックＡ用ＡＰＩ５６２を呼び出すことで、機能ブロックＡ５０２ａで所定の処理を実施する。

【０１１０】

同じく、機能ブロックＢ制御ソフトウェア５５５が提供する機能ブロックＢ制御ＡＰＩ５６３を呼び出すことにより、機能ブロックＢ５０２ｂの実行を実施する。

【０１１１】

同じく、電力設定ソフトウェア５５６が提供する電力設定ＡＰＩ５６４を呼び出すことにより、機能ブロック５０２に対する電力の設定、つまり動作クロック、電源電圧の遮断、供給、および動作周波数を設定する。

【０１１２】

同じく、機能ブロック間通信ソフトウェア５５７が提供する機能ブロック間通信ＡＰＩ５６５を呼び出すことにより、機能ブロック５０２の間でデータを互いに転送し合う機能を実現する。

【０１１３】

また電力設定ソフトウェア５５６、機能ブロック間通信ソフトウェア５５７、および電力管理スレッド５６６は、ＲＯＭ５１０の一部である特定プログラムメモリ５６７に格納する。

【０１１４】

さらに電力設定ソフトウェア５５６、機能ブロック間通信ソフトウェア５５７、および電力管理スレッド５６６は、消費電力管理装置５０８で読み書き可能なＲＡＭ５１１の一領域である特定ワーキングメモリ５６８を用いて所定の処理を行う。

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【０１１５】
特定ワーキングメモリ５６８をデータ処理に用いる。その他のソフトウェアは、特定プログラムメモリ５６７以外のＲＯＭ５１０内にマッピングし、データ処理は特定ワーキングメモリ５６８以外のＲＡＭ５１１領域を用いる。
【０１１６】
図８は、特定ワーキングメモリの構成の実施例を説明する図である。
【０１１７】
特定ワーキングメモリ５６８は、機能ブロック間通信用構造体５６９、リストプール５７０、機能ブロック数の単数ないし複数の機能ブロック用番兵５７１、電力管理用番兵５７２、サスペンド用番兵５７３、および低電力用番兵５７４で構成する。
【０１１８】
機能ブロック間通信用構造体５６９は、命令識別子メモリ５７５と単数ないし複数の通信パラメータメモリ５７６を格納するメモリブロックとする。
【０１１９】
リストプール５７０は、リンクリストに対して提供するリスト５７７の集合体である。またリスト５７７は、タスク管理ポインタメモリ５７８、電力管理ポインタメモリ５７９、タスク優先度メモリ５８０、機能ブロック識別子メモリ５８１、電力モード値メモリ５８２および電力モード時間メモリ５８３と言ったパラメータを格納する動的メモリブロックとする。
【０１２０】
機能ブロック用番兵５７１、電力管理用番兵５７２、サスペンド用番兵５７３、および低電力用番兵５７４はリスト５７７と同じメモリフォーマットであるが、リストプール５７０からは提供されない静的なメモリブロックとする。
【０１２１】
また機能ブロック用番兵５７１、電力管理用番兵５７２、サスペンド用番兵５７３、および低電力用番兵５７４はリスト５７７を用いてそれぞれ、機能ブロック用リンクリスト、電力管理用リンクリスト、サスペンド用リンクリスト、および低電力用リンクリストを管理する。
【０１２２】
機能ブロック用リンクリストは機能ブロック５０２のタスク管理を行う。機能ブロック用番兵５７１のタスク管理ポインタメモリ５７８には先頭リストのアドレスを格納すると同時に、機能ブロック用番兵５７１のアドレスは後尾リストのタスク管理ポインタメモリ５７８に格納される。
【０１２３】
先頭リストのタスク優先度が最高優先で、後尾リストのタスク優先度が最低優先となるように、先頭リストと後尾リストの間に高優先度順にリスト５７７をタスク管理ポインタメモリ５７８で繋ぐ。また同じタスク優先度のリスト５７７を連結する場合はＦＩＦＯ（Ｆｉｒｓｔ　Ｉｎ　Ｆｉｒｓｔ　Ｏｕｔ：先入れ先出し）順に繋ぐ。
【０１２４】
電力管理用リンクリストは前記総要求電力の管理を行う。電力管理用番兵５７２の電力管理ポインタメモリ５７９には先頭リストのアドレスを格納すると同時に、電力管理用番兵５７２のアドレスには後尾リストの電力管理ポインタメモリ５７９に格納する。
【０１２５】
先頭リストのタスク優先度が最低優先で、後尾リストのタスク優先度が最高優先となるように、先頭リストと後尾リストの間に電力管理ポインタメモリ５７９を用いて低優先度順にリスト５７７を繋ぐ。また同じタスク優先度のリスト５７７を連結する場合はＦＩＦＯ順に繋ぐ。
【０１２６】
サスペンド用リンクリストは動作クロック分配装置５０４における動作クロックの遮断および供給の管理を行う。サスペンド用番兵５７３の電力管理ポインタメモリ５７９には

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先頭リストのアドレスを格納すると同時に、電力管理用番兵５７２のアドレスは後尾リストの電力管理ポインタメモリ５７９に格納される。

【０１２７】

先頭リストのタスク優先度が最高優先で、後尾リストのタスク優先度が最低優先となるように、先頭リストと後尾リストの間に電力管理ポインタメモリ５７９を用いて高優先度順にリスト５７７を繋ぐ。また同じタスク優先度のリスト５７７を連結する場合はＦＩＦＯ順に繋ぐ。

【０１２８】

低電力処理用リンクリストは動作クロック分配装置５０４における動作周波数の管理を行う。低電力用番兵５７４の電力管理ポインタメモリ５７９には先頭リストのアドレスを格納すると同時に、電力管理用番兵５７２のアドレスは後尾リストの電力管理ポインタメモリ５７９に格納される。

【０１２９】

先頭リストのタスク優先度メモリ５８０が最高優先で、後尾リストのタスク優先度メモリ５８０が最低優先となるように、先頭リストと後尾リストの間に電力管理ポインタメモリ５７９を用いて高優先度順にリスト５７７を繋ぐ。また同じタスク優先度のリスト５７７を連結する場合はＦＩＦＯ順に繋ぐ。

【０１３０】

以下に電力設定ＡＰＩ５６４および機能ブロック間通信ＡＰＩ５６５の詳細について説明する。

【０１３１】

なお、使用プログラミング言語仕様はＡＮＳＩ　Ｃを想定するが、他のプログラミング言語でも構わない。ＡＰＩの形式は関数形式とする。

【０１３２】

説明に先立ち、消費電力管理装置５０８をプロセッサで実現し、電力管理スレッド５６６、ＯＳ＿Ｘ５５３ｘ、電力設定ソフトウェア５５６、および機能ブロック間通信ソフトウェア５５７で構成するものとする。つまり消費電力管理装置５０８の命令解読装置５３５、割込み受付装置５１４および割込み発生装置５３６はプロセッサ、時間管理装置５３７はＯＳ＿Ｘ５５３ｘの時間管理機能を用いる。

【０１３３】

電力設定ＡＰＩ５６４としては、動作クロック分配装置５０４の動作周波数状態制御レジスタ５２８にアクセスして動作周波数の設定を行う電力設定ＡＰＩ１、同じくアクセスして動作クロックの遮断および供給の設定を行う電力設定ＡＰＩ２、電源電圧分配装置５０６の電源スイッチレジスタ５３３にアクセスして電源電圧の遮断および供給の設定を行う電力設定ＡＰＩ３、電力換算装置５０７の総要求電力格納レジスタ５２３にアクセスして前記総要求電力値を消費電力管理装置５０８にロードする電力設定ＡＰＩ４などを設ける。

【０１３４】

また機能ブロック間通信ＡＰＩ５６５としては、スレッド５６０を生成したことを消費電力管理装置５０８に伝える機能ブロック間通信ＡＰＩ１、スレーブ機能ブロックを動作させたことを消費電力管理装置５０８に伝える機能ブロック間通信ＡＰＩ２、スレッド５６０をこれから削除することを消費電力管理装置５０８に伝える機能ブロック間通信ＡＰＩ３、スレーブ機能ブロックの動作が終了したことを消費電力管理装置５０８に伝える機能ブロック間通信ＡＰＩ４、マスタ機能ブロックから前記電力予算値を設定する機能ブロック間通信ＡＰＩ５、マスタ機能ブロックから事象処理装置５４１に対する周期イベントの前記周期時間を設定する機能ブロック間通信ＡＰＩ６、などを設ける。

【０１３５】

図９は、機能ブロック間通信ＡＰＩ１および機能ブロック間通信ＡＰＩ２のフローチャートの図である。

【０１３６】

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機能ブロック間通信ＡＰＩ１は、プログラマーまたはＯＳ＿Ａ５５３ａが設定するスレッド５６０のタスク優先度、機能ブロックA５０２ａの機能ブロック識別子、機能ブロック間の通信が同期か非同期かを設定する通信モード値、機能ブロックを前記高電力モード、前記中電力モード、または前記低電力モードの何れかを設定する電力モード値、および電力モード値の持続時間を表す電力モード時間を引数として設定する。

【０１３７】

第１処理（ステップＳ５８４）は、機能ブロック間通信用構造体５６９の命令識別子メモリ５７５に自分の命令に対応する命令識別子、通信パラメータメモリＡ５７６ａに前記タスク優先度、通信パラメータメモリＢ５７６ｂに機能ブロック識別子、通信パラメータメモリＣ５７６ｃに前記通信モード値、通信パラメータメモリＤ５７６ｄに前記電力モード値、および通信パラメータメモリＥ５７６ｅに前記電力モード時間をそれぞれ格納する。

【０１３８】

第２処理（ステップＳ５８５）は、機能ブロックＡ５０２ａから消費電力管理装置５０８に割込みをかける。

【０１３９】

次に前記通信モードが同期かどうか判別し、同期ならば第３処理（ステップＳ５８６）へ移行する。

【０１４０】

第３処理（ステップＳ５８６）は、電力設定ＡＰＩ２を用いてマスタ機能ブロックである機能ブロックＡ５０２ａの動作を停止させる。

【０１４１】

機能ブロック間通信ＡＰＩ２でも同様にプログラマーが設定するスレッド５６０のタスク優先度、機能ブロックＢ５０２ｂの機能ブロック識別子、機能ブロック間の通信が同期か非同期かを設定する通信モード値、機能ブロックを前記高電力モード、前記中電力モード、または前記低電力モードの何れかを設定する電力モード値、および電力モード値の持続時間を表す電力モード時間を引数として設定し、第１処理（Ｓ５８４）、第２処理（Ｓ５８５）、第３処理（Ｓ５８６）を同様に行う。

【０１４２】

但し第３処理（ステップＳ５８６）で、電力設定ＡＰＩ２を用いて動作を停止させるのはスレーブ機能ブロックである機能ブロックＢである。

【０１４３】

図１０は、機能ブロック間通信ＡＰＩ３および機能ブロック間通信ＡＰＩ４のフローチャートの図である。

【０１４４】

機能ブロック間通信ＡＰＩ３は、機能ブロックA５０２ａの機能ブロック識別子を引数として設定する。

【０１４５】

第４処理（ステップＳ５８７）は、機能ブロック間通信用構造体５６９の命令識別子メモリ５７５に自分の命令に対応する命令識別子、通信パラメータメモリＡ５７６ａに前記機能ブロック識別子をそれぞれ格納し、第２処理（ステップＳ５８５）を実施する。

【０１４６】

同様に機能ブロック間通信ＡＰＩ４でも、機能ブロックＢの機能ブロック識別子を引数として設定し、第４処理（ステップＳ５８７）後、第２処理（ステップＳ５８５）を実施する。

【０１４７】

図１１は、機能ブロック間通信ＡＰＩ５のフローチャートを説明する図である。

【０１４８】

機能ブロック間通信ＡＰＩ５は、前記電力予算値を引数として設定する。

【０１４９】

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第５処理（ステップＳ５８８）は、機能ブロック間通信用構造体５６９の命令識別子メモリ５７５に自分の命令に対応する命令識別子、通信パラメータメモリＡ５７６ａに前記電力予算値をそれぞれ格納し、第２処理（ステップＳ５８５）を実施する。

【０１５０】

図１２は、機能ブロック間通信ＡＰＩ６のフローチャートの図である。

【０１５１】

機能ブロック間通信ＡＰＩ６は、前記周期時間を引数として設定する。

【０１５２】

第６処理（ステップＳ５８９）は、機能ブロック間通信用構造体５６９の命令識別子メモリ５７５に自分の命令に対応する命令識別子、通信パラメータメモリＡ５７６ａに前記電力予算値をそれぞれ格納し、第２処理（ステップＳ５８５）を実施する。

【０１５３】

図１３は、消費電力管理装置上の機能ブロック間通信ソフトウェアのフローチャートを説明する図である。

【０１５４】

消費電力管理装置５０８の割込み受付け装置５１４で割込みを受け付けると、機能ブロック間通信ソフトウェア５５７は第７処理（ステップＳ５９０）として、命令解読装置５３５を介して機能ブロック間通信用構造体５６９にアクセスする。

【０１５５】

次に機能ブロック間通信用構造体５６９の命令識別子メモリ５７５から前記命令識別子を読み込み、所望の機能ブロック間通信ＡＰＩ５６５に対応する処理を第８処理（ステップＳ５９１）から第１３処理（ステップＳ５９６）の中から選択する。

【０１５６】

つまり、もし前記命令識別子が機能ブロック間通信ＡＰＩ１を表していたら第８処理（ステップＳ５９１）、機能ブロック間通信ＡＰＩ２を表していたら第９処理（ステップＳ５９２）、機能ブロック間通信ＡＰＩ３を表していたら第１０処理（ステップＳ５９３）、機能ブロック間通信ＡＰＩ４を表していたら第１１処理（ステップＳ５９４）、機能ブロック間通信ＡＰＩ５を表していたら第１２処理（ステップＳ５９５）、機能ブロック間通信ＡＰＩ６を表していたら第１３処理（ステップＳ５９６）に処理を移す。

【０１５７】

図１４は、リスト登録時の機能ブロック用リンクリストを説明する図である。

【０１５８】

第８処理（ステップＳ５９１）はリスト登録装置５３８に相当する。

【０１５９】

先ずリストプール５７０からリストＡ５７７ａを確保して、機能ブロック間通信用構造体５６９の通信パラメータメモリＡ５７６ａに格納の値をリストＡ５７７ａのタスク優先度メモリ５８０に、通信パラメータメモリＢ５７６ｂに格納の値を同じく機能ブロック識別子メモリ５８１に、通信パラメータメモリＤ５７６ｄに格納の値を同じく電力モード値メモリ５８２に、および通信パラメータメモリＥ５７６ｅに格納の値を同じく電力モード時間メモリ５８３に格納する。

【０１６０】

そして機能ブロック識別子メモリ５８１の値に対応する機能ブロック用番兵Ｂ５７１ｂが管理する機能ブロック用リンクリストに、タスク管理ポインタメモリ５７８を用いてリスト５７７をタスク優先度順およびタスク優先度が同じ場合にはＦＩＦＯ順に挿入する。

【０１６１】

例えば機能ブロック用番兵Ｂ５７１ｂにリストＢ５７７ｂが連結されている場合、リストＡ５７７ａが先頭リストであるリストＢ５７７ｂのタスク優先度よりも高い場合は機能ブロック用番兵Ｂ５７１ｂの次に挿入してリンクし、反対に低い場合および同じタスク優先度の場合は後尾リストとしてリストＢ５７７ｂの後に挿入してリンクする。

【０１６２】

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図１５は、リスト登録時の機能ブロック用リンクリストと電力管理用リンクリストを説明する図である。

【０１６３】

第８処理（ステップＳ５９１）では機能ブロック用リンクリストにリストＡ５７７ａを挿入後、さらにリストＡ５７７ａを電力管理用番兵５７２が管理する電力管理用リンクリストに電力管理ポインタメモリ５７９を用いて、タスク優先度の低い順およびタスク優先度が同じ場合にはＦＩＦＯ順に挿入する。

【０１６４】

リストＡ５７７ａを前記機能ブロック用リンクリストおよび電力管理用リンクリスト挿入後、事象処理装置５４１に起動イベント５５２をかけて第８処理（Ｓ５９１）が完了する。

【０１６５】

また第９処理（ステップＳ５９２）も第８処理（ステップＳ５９１）と同様のリスト登録処理となる。

【０１６６】

図１６は、リスト削除時の機能ブロック用リンクリストと電力管理用リンクリストを説明する図である。

【０１６７】

第１０処理（ステップＳ５９３）はリスト削除装置５３９に相当する。

【０１６８】

先ず機能ブロック間通信用構造体５６９の通信パラメータメモリＡ５７６ａの値である機能ブロック識別子に対応する機能ブロック用番兵Ｃ５７１ｃが管理する機能ブロック用リンクリストの先頭のリストＣ５７７ｃのタスク管理ポインタメモリ５７８を外す。

【０１６９】

次に外したリストＣ５７７ｃの機能ブロック識別子メモリ５８１に格納の値に対応するリストＣ５７７ｃの電力管理ポインタメモリ５７９を前記電力管理用リンクリストから外し、リストＣ５７７ｃをリストプール５７０に戻す。

【０１７０】

図１７は、リスト削除時の電力管理用、サスペンド用、低電力用リンクリストを説明する図である。

【０１７１】

第１０処理（ステップＳ５９３）は次に、サスペンド用番兵５７３が管理するサスペンド用リンクリストおよび低電力用番兵５７４が管理する低電力用リンクリストにもし先頭リストが存在する場合、つまりサスペンド用番兵５７３にリストＤ５７７ｄ、または低電力用番兵５７４にリストＥ５７７ｅがリンクされている場合、前記サスペンド用リンクリストからリストＤ５７７ｄのタスク管理ポインタメモリ５７８を外す。同様に前記低電力用リンクリストからリストＥ５７７ｅのタスク管理ポインタメモリ５７８も外す。

【０１７２】

反対に、もしリンクされているリスト５７７が存在しない場合は何も施さない。

【０１７３】

最後に電力設定ＡＰＩ２、さらに電力設定ＡＰＩ１を呼び出して、外したリストＤ５７７ｄおよびリストＥ５７７ｅの機能ブロック識別子メモリ５８１に対応する機能ブロック５０２を、動作クロック分配装置５０４で前記高電力モードに設定、つまり最高動作周波数に戻す。

【０１７４】

第１１処理（ステップＳ５９４）も第１０処理（ステップＳ５９３）と同様のリスト削除処理となる。

【０１７５】

第１２処理（ステップＳ５９５）は電力予算値取得装置５４０に相当する。

【０１７６】

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機能ブロック間通信用構造体５６９の通信パラメータメモリＡ５７６ａの値である前記電力予算値を電力予算値レジスタ５４６に格納する。

【０１７７】

第１３処理（ステップＳ５９６）は機能ブロック間通信用構造体５６９の通信パラメータメモリＡ５７６ａの値である前記周期時間をＯＳ＿Ｘ５５３ｘの時間管理機能のシステムコールＸ５６１ｘを用いて設定する。

【０１７８】

事象処理（ステップＳ５９７）は電力管理スレッド５６６で実現する。つまり事象処理Ｓ５９７の起動は電力管理スレッド５６６の起動に相当する。

【０１７９】

電力管理スレッド５６９は先ず総要求電力値取得装置５４５に相当する前記電力設定ＡＰＩ４を呼び出して前記総要求電力値をロードする。

【０１８０】

次に電力予算値レジスタ５４６に格納の前記電力予算値から前記総要求電力値を引き、正または０ならば電力正常処理部５４９、負ならば電力異常処理部５５０に実行を移す。

【０１８１】

電力正常処理部５４９は、機能ブロック間通信用構造体５６９の通信パラメータメモリＣ５７６ｃの値である前記通信モード値と通信パラメータメモリＢ５７６ｂの値である機能ブロック識別子をロードする。

【０１８２】

もし前記通信モード値が同期と設定されているならば、前記機能ブロック識別子に対応する機能ブロック５０２に割込み発生装置５３６で割込みをかける。

【０１８３】

図１８は、電力異常処理部を説明する図である。

【０１８４】

電力異常処理部５５０は、先ず前記電力管理用リンクリストの電力管理ポインタメモリ５７９から先頭のリストＦ５７７ｆを外す。

【０１８５】

そしてリストＦ５７７ｆの電力モード時間メモリ５８３の値である電力モード時間をシステムコールX５６１で前記アラーム時間としてＯＳ＿Ｘ５５３ｘのアラーム機能に設定する。

【０１８６】

さらに外したリストＦ５７７ｆの電力モード値メモリ５８２がもし停止モードであったら、前記サスペンド用リンクリストにタスク優先度の高い順に挿入した後、電力設定ＡＰＩ２を呼び出し、挿入したリストＦ５７７ｆの機能ブロック識別子メモリ５８１の値に対応する機能ブロック５０２に対して動作クロック５２９を遮断する。

【０１８７】

同じく電力モード値メモリ５８２がもし低電力モードであったら、前記低電力用リンクリストにタスク優先度の高い順に挿入してリンクした後、電力設定ＡＰＩ１を呼び出し、挿入したリストＦ５７７ｆの機能ブロック識別子メモリ５８１に対応する機能ブロック５０２に対応する動作クロック５２９の動作周波数を低くする。

【０１８８】

また前記アラーム時間経過後、前記アラームイベントにより、サスペンド用番兵５７３および低電力用番兵５７４に直にリンクされている先頭リストを電力管理ポインタメモリ５７９から外す。

【０１８９】

そして電力設定ＡＰＩ２、さらに電力設定ＡＰＩ１を呼び出して、外したリスト５７７の機能ブロック識別子メモリ５８１に対応する機能ブロック５０２を、動作クロック分配装置５０４で前記高電力モードに設定、つまり最高動作周波数に戻す。

【０１９０】

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図１９は、電力遮断処理部を説明する図である。

【０１９１】

機能ブロックＡ５０２ａ、機能ブロックＣ５０２ｃ、および機能ブロックD５０２ｄが同じ電源スイッチ５３２を共有していると想定する。

【０１９２】

先ず機能ブロック用リンクリストＡ、機能ブロック用リンクリストＣ、および機能ブロック用リンクリストDのそれぞれが空であるか、つまり機能ブロック用番兵５７１のタスク管理ポインタメモリ５７８に自分自身の機能ブロック用番兵５７１の先頭アドレスが格納されているかを検出する。

【０１９３】

もし機能ブロック用リンクリストＡ、機能ブロック用リンクリストＣ、機能ブロック用リンクリストＤの全てが空である場合は、低消費電力化を施すように電源電圧分配装置５０６の電源スイッチレジスタ５３３を設定して、電源スイッチ５３２で電源電圧５３１を遮断する。

【０１９４】

反対に一つでも空でならば、何も施さない。

【０１９５】

勿論、任意の前記機能ブロック用リンクリストが空であれば動作クロック分配装置５０４で動作クロック５２９を遮断する。

【０１９６】

図２０は、電力管理スレッドを機能ブロック上で動作させる実施例を説明する図である。

【０１９７】

本発明は、図２０のように機能ブロック上に電力設定ソフトウェア５５６、機能ブロック間通信ソフトウェア５５７および電力管理スレッド５６６を搭載することにより、図７の実施例と同様の情報処理装置５０１の電力管理が可能である。つまり電力管理スレッド５６６を任意の機能ブロック５０２が持つことで消費電力管理装置５０８を兼ねる。

【０１９８】

以上、本発明者によってなされた発明を実施の形態に基づき具体的に説明したが、本発明は前記実施の形態に限定されるものではなく、その要旨を逸脱しない範囲で種々変更可能であることはいうまでもない。

【産業上の利用可能性】

【０１９９】

本発明は、半導体集積回路装置における電力管理を行い、該半導体集積回路装置を安定した動作で低消費電力化することのできる技術に適している。

【図面の簡単な説明】

【０２００】

【図１】本発明の代表例のハードウェア構成の実施例を説明する図である。

【図２】機能ブロックとバスの関係を説明する図である。

【図３】電力換算装置を説明する図である。

【図４】クロックパルス発生器と動作クロック分配装置を説明する図である。

【図５】電源装置と電源電圧分配装置を説明する図である。

【図６】本発明の代表的な消費電力管理装置の実施例を説明する図である。

【図７】機能ブロックと消費電力管理装置を動かすソフトウェアを説明する図である。

【図８】特定ワーキングメモリの構成の実施例を説明する図である。

【図９】機能ブロック間通信ＡＰＩ１および機能ブロック間通信ＡＰＩ２のフローチャートである。

【図１０】機能ブロック間通信ＡＰＩ３および機能ブロック間通信ＡＰＩ４のフローチャートである。

【図１１】機能ブロック間通信ＡＰＩ５のフローチャートである。

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【図１２】機能ブロック間通信ＡＰＩ６のフローチャートである。
【図１３】消費電力管理装置上の機能ブロック間通信ソフトウェアのフローチャートである。
【図１４】リスト登録時の機能ブロック用リンクリストを説明する図である。
【図１５】リスト登録時の機能ブロック用リンクリストと電力管理用リンクリストを説明する図である。
【図１６】リスト削除時の機能ブロック用リンクリストと電力管理用リンクリストを説明する図である。
【図１７】リスト削除時の電力管理用、サスペンド用、低電力用リンクリストを説明する図である。
【図１８】電力異常処理部を説明する図である。
【図１９】電力遮断処理部を説明する図である。
【図２０】電力管理スレッドを機能ブロック上で動作させる実施例を説明する図である。
【図２１】特許文献１の図４に記載の消費電力管理装置の構成図である。
【図２２】特許文献１の図２に記載の消費電力管理装置の構成図である。
【符号の説明】
【０２０１】
５０１　半導体集積回路装置
５０２　機能ブロック
５０３　クロックパルス発生装置
５０４　動作クロック分配装置
５０５　電源装置
５０６　電源電圧分配装置
５０７　電力換算装置
５０８　消費電力管理装置
５０９　Ｉ／Ｏ装置
５１０　ＲＯＭ（不揮発性半導体メモリ）
５１１　ＲＡＭ（揮発性半導体メモリ）
５１２　タイマ
５１３　バス
５１４　割込み受付装置
５１５　命令制御線
５１６　データ転送線
５１７　割込み受信線
５１８　割込み発信線
５１９　消費電力構成要素信号
５２０　電力センサ
５２１　電力変換装置
５２２　加算器
５２３　総要求電力格納レジスタ
５２４　パルス
５２５　ＰＬＬ
５２６　分周器
５２７　動作クロック遮断装置
５２８　動作周波数状態制御レジスタ
５２９　動作クロック
５３０　電池電圧
５３１　電源電圧
５３２　電源スイッチ
５３３　電源スイッチレジスタ

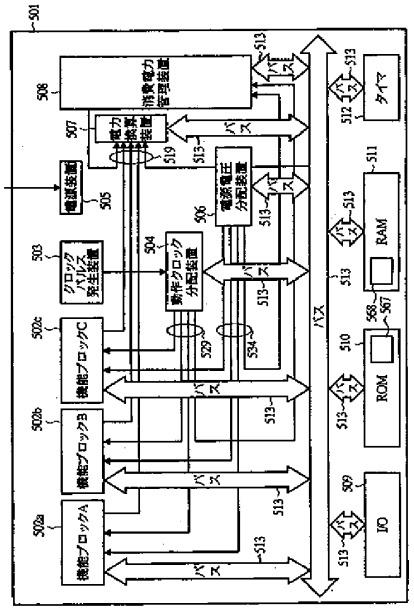
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５３４　電源スイッチ制御信号
５３５　命令解読装置
５３６　割込み発生装置
５３７　時間管理装置
５３８　リスト登録装置
５３９　リスト解除装置
５４０　電力予算値取得装置
５４１　事象処理装置
５４２　タイマイベント
５４３　システム時刻メモリ
５４４　カウントダウンメモリ
５４５　総要求電力値取得装置
５４５ａ　周期イベント
５４６　電力予算値レジスタ
５４７　減算器
５４８　比較器
５４９　電力正常処理部
５５０　電力異常処理部
５５１　電力遮断処理部
５５２　起動イベント
５５３　ＯＳ
５５４　機能ブロックＡ用ソフトウェア
５５５　機能ブロックＢ制御ソフトウェア
５５６　電力設定ソフトウェア
５５７　機能ブロック間通信ソフトウェア
５５８　アプリケーションソフトウェア
５５９　電力管理アプリケーションソフトウェア
５６０　スレッド
５６１　システムコール
５６２　機能ブロックＡ用ＡＰＩ
５６３　機能ブロックＢ制御ＡＰＩ
５６４　電力設定ＡＰＩ
５６５　機能ブロック間通信ＡＰＩ
５６６　電力管理スレッド
５６７　特定プログラムメモリ
５６８　特定ワーキングメモリ
５６９　機能ブロック間通信用構造体
５７０　リストプール
５７１　機能ブロック用番兵
５７２　電力管理用番兵
５７３　サスペンド用番兵
５７４　低電力用番兵
５７５　命令識別子メモリ
５７６　通信パラメータメモリ
５７７　リスト
５７８　タスク管理ポインタメモリ
５７９　電力管理ポインタメモリ
５８０　タスク優先度メモリ
５８１　機能ブロック識別子メモリ
５８２　電力モード値メモリ

５８３　電力モード時間メモリ
５９８　機能ブロックＣ用ソフトウェア
５９９　機能ブロックＣ用ＡＰＩ

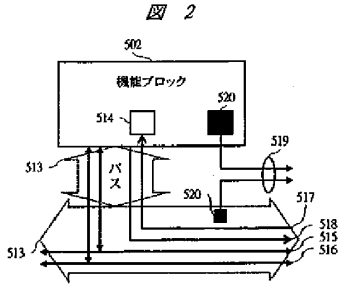
【図１】

図 1



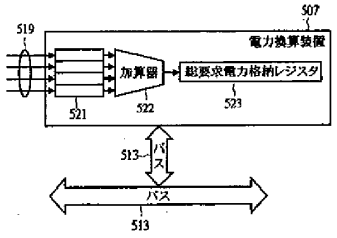
【図２】

図 2



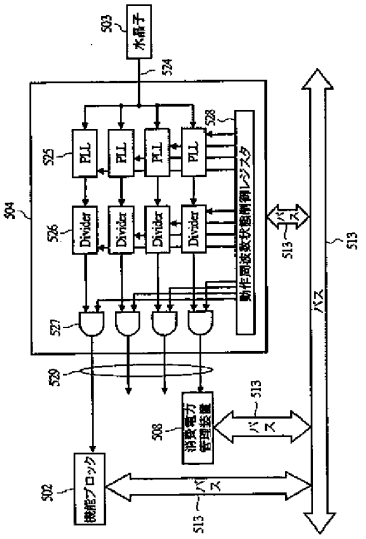
【図３】

図 3



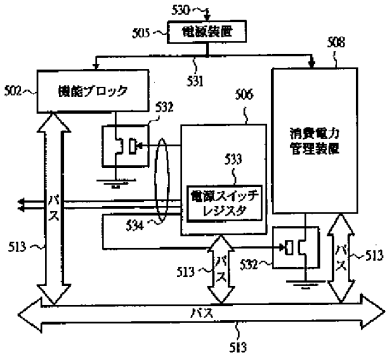
【図４】

図 4



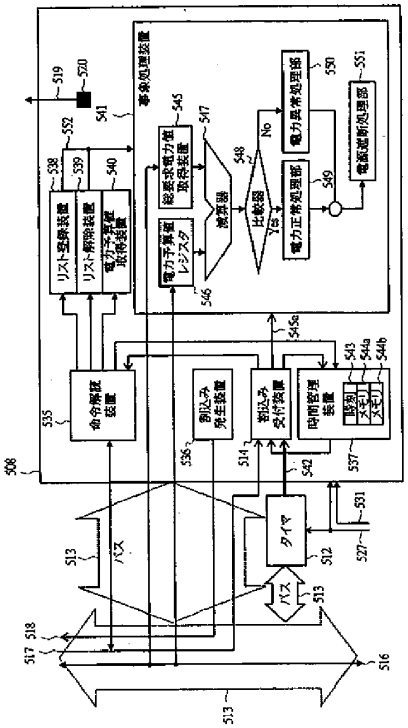
【図５】

図 5



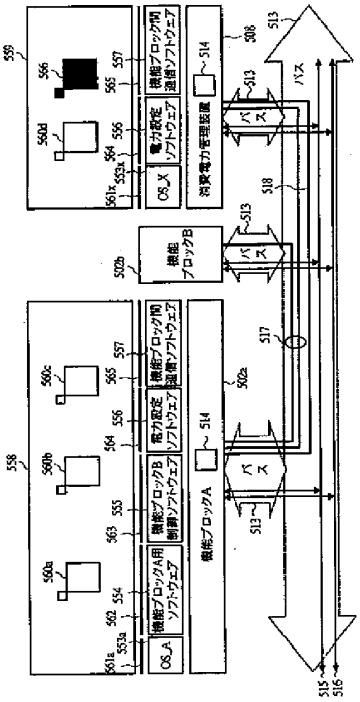
【図６】

図 6



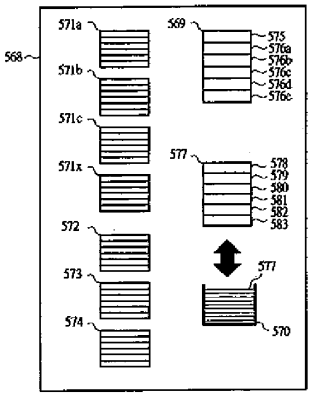
【図７】

図 7



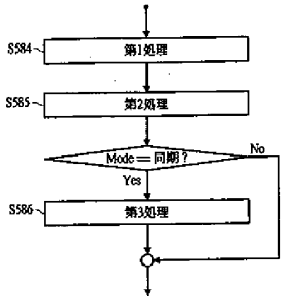
【図８】

図 8



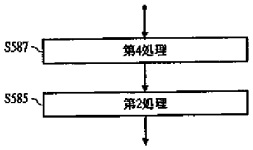
【図９】

図 9



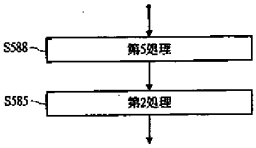
【図１０】

図 10



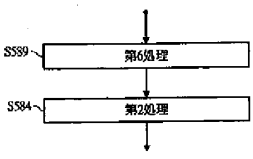
【図１１】

図 11



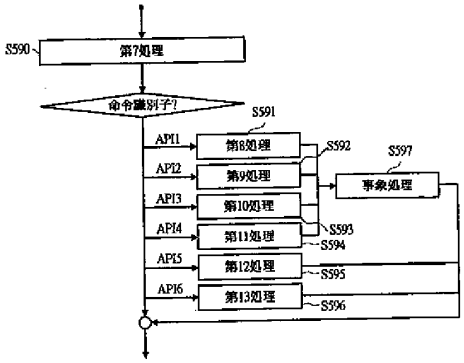
【図１２】

図 12



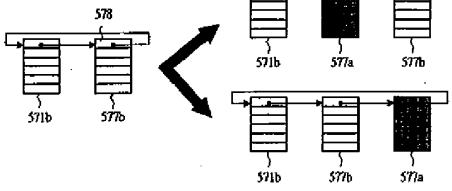
【図１３】

図 13



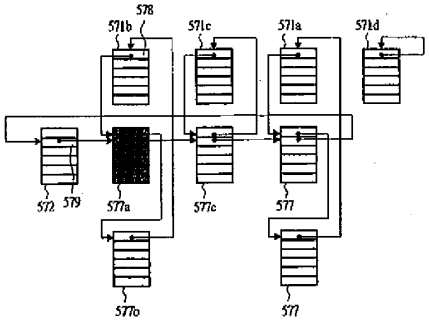
【図１４】

図 14



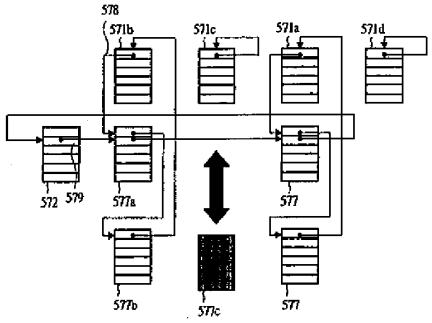
【図１５】

図 15



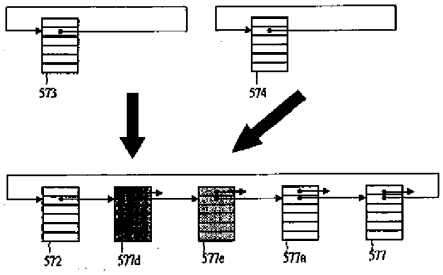
【図１６】

図 16



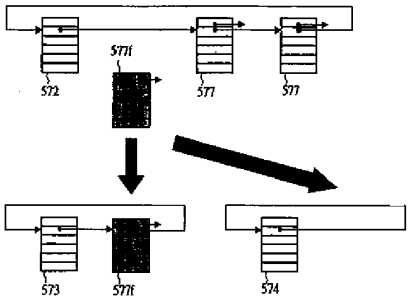
【図１７】

図 17



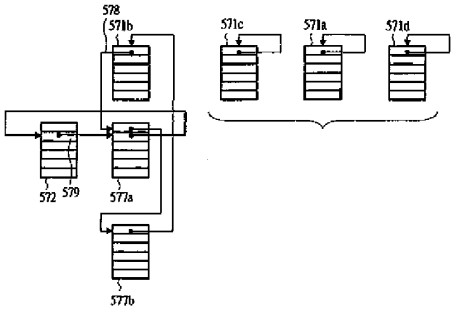
【図１８】

図 18

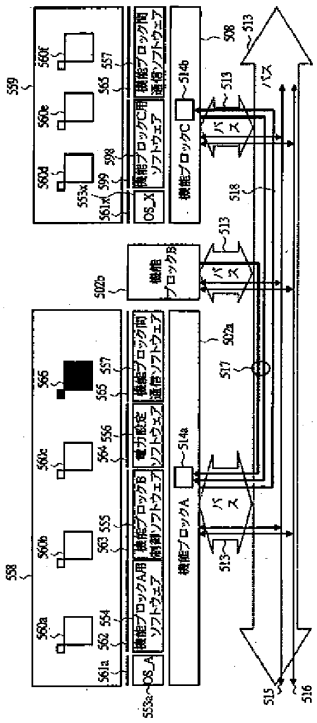


【図１９】

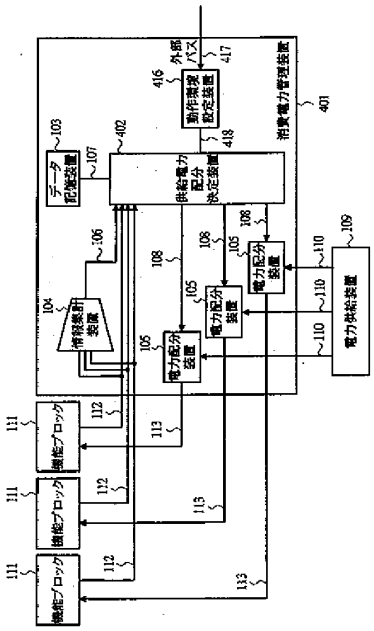
図 19



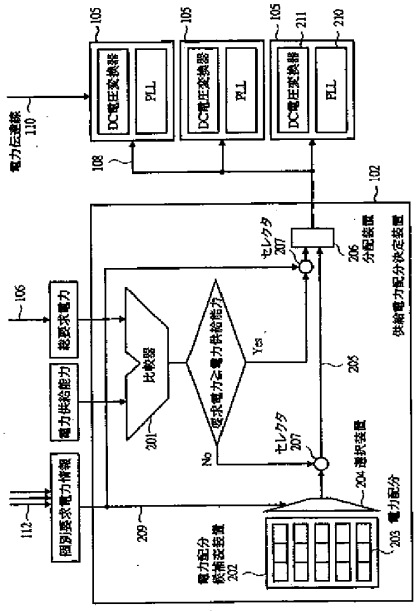
【図２０】



【図２１】



【図２２】



フロントページの続き

(72)発明者 十山 圭介
東京都国分寺市東恋ヶ窪一丁目２８０番地 株式会社日立製作所中央研究所内
(72)発明者 長田 健一
東京都国分寺市東恋ヶ窪一丁目２８０番地 株式会社日立製作所中央研究所内

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(71) Applicant: **MITSUBISHI DENKI KABUSHIKI KAISHA**
Tokyo 100-8310 (JP)

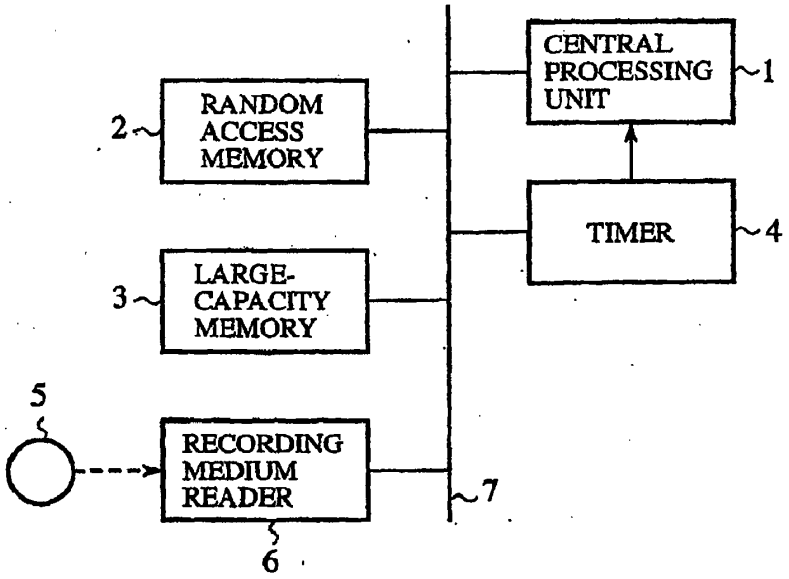
(72) Inventor: **KUROSAWA, Hisayoshi,**
MITSUBISHI DENKI K.K.
Tokyo 100-8310 (JP)

(74) Representative: **Pfenning, Meinig & Partner**
Mozartstrasse 17
80336 München (DE)

(54) **COMPUTER SYSTEM AND COMPUTER-READABLE RECORDING MEDIUM**

(57) A central processing unit is provided with a plurality of power saving modes so that an optimum power saving mode determined by an interval between requested time-out interruptions is selected.

FIG.2



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Description

TECHNICAL FIELD

[0001] The present invention relates to a computer system provided with a central processing unit having, in addition to a normal mode, a plurality of power saving modes characterized by difference levels of power consumption and to a computer readable recording medium readable by such a system. More particularly, the invention relates to a computer system capable of effectively reducing power consumption while an application is being executed, by appropriately switching between the plurality of power saving modes of the central processing unit while appropriately executing jobs based on time-out interruptions.

BACKGROUND ART

[0002] Sophisticated performance of application programs recently used requires that a central processing unit executing the program be provided with a high-level processing performance. As a result, many central processing units are now operated at an increasingly high speed. The resultant increase in power consumed in the central processing unit now presents a serious challenge in building a system using the central processing unit.

[0003] A computer system provided with a function of reducing power consumption of a central processing unit is disclosed, for example, in Japanese Laid-Open Patent Application No. 11-184550. A computer system using a difference timer is also proposed elsewhere.

[0004] Fig. 1 shows a construction of a related-art computer system disclosed in Japanese Laid-Open Patent Application No. 11-184550. Referring to Fig. 1, the system comprises a central processing unit (CPU) 8, a memory 9, a hard disk drive (HDD) 10, a basic input and output system read-only memory (BIOSROM) 11, a system controller 12, a clock oscillation circuit 13, a system bus 14, an operating system program 14, and a monitor system program 16.

[0005] A description will now be given of the operation according to the related art.

[0006] The central processing unit 8 performs predetermined processes in accordance with the operating system program stored in the memory 9. When in an idle state, the central processing unit 8 notifies the system controller 12 of the CPU usage rate. The system controller 12 controls intervals between timer interruptions presented to the central processing unit 8 and an oscillation frequency of the clock oscillation circuit 13. More specifically, as the idle time becomes extended and the usage rate becomes low, the intervals between timer interruptions are extended and the oscillation frequency is lowered, thereby reducing the power consumption by the central processing unit 8.

[0007] The aforementioned system using a difference timer sets, in a timer means, a difference time indicating a period of time that elapses since the immediately preceding time-out interruption. The operation of the central processing unit is switched between a power saving mode and a normal mode, based on a time-out interruption of the timer means.

[0008] In the related-art systems constructed as described above, various measures directed to low power consumption of the central processing unit 8 are employed. However, these measures fail to provide effective and satisfactory solutions.

[0009] For example, in the system disclosed in Laid-Open Application, a minimum interval between interruptions (i.e. interruption interval at an initial state) should be set so that it is smaller than the smallest transition interval between two states occurring in a system in which the technology of the Laid-Open Application is applied, in order to properly differentiate between two states that occur in succession. As a result, even when a situation arises in which a time interval between different states becomes significantly large, unnecessary interruptions occur repeatedly, causing the central processing unit 8 to operate each time and wasting the power accordingly.

[0010] Further, by setting a small time interval, the central processing unit 8 is required to return to its operation at the small interval to perform an interruption process. Thus, it is not expected that the processing speed of the central processing unit 8 drops in any substantial manner. A considerable reduction in power consumption cannot be hoped for by switching to the power saving mode. In the aforementioned system using a difference timer, too, the central processing unit is expected to perform an interruption process by returning to operation at the minimum interval defined by the system. Thus, it is not expected that the processing speed of the central processing unit 8 drops in any substantial manner. An appreciable reduction in power consumption cannot be hoped for by switching to the power saving mode.

[0011] The present invention has been developed in view of the aforementioned problems and has an objective of providing a computer system provided with a central processing unit having, in addition to a normal mode, a plurality of power saving modes with difference power consumption levels, the computer system being suitably adapted for a battery-driven operation by providing the capability of effectively reducing power consumption of the central processing unit while an application is being executed, by switching between the plurality of power saving modes and executing jobs appropriately based on time-out interruptions. Another object is to provide a recording medium readable by such a system.

DISCLOSURE OF THE INVENTION

[0012] The present invention provides a computer system comprising: a central processing unit provided,

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in addition to a normal mode, with a plurality of power saving modes characterized by respective power consumption levels, and sequentially executing a plurality of jobs generating associated time-out interruption requests; storage means storing a return time table mapping the plurality of power saving modes of the central processing unit into respective return time required for the central processing unit to return from the corresponding power saving mode to the normal mode; list updating means updating a time-out list, chronologically listing the time-out interruption requests, based on the time-out interruption requests from the plurality of jobs executed by the central processing unit; timer means outputting time-out interruptions to the central processing unit when the time-out time listed in the time-out list elapses; setting means setting a next time-out time in the timer means whenever a time-out interruption occurs in accordance with the order listed in the time-out list; transition mode selection means referring to the return time table when the central processing unit is put in an idle state, and selecting, as a transition mode, a power saving mode having the longest return time, from a group of one or a plurality of power saving modes having a return time shorter than the time-out time designated for the subsequent time-out interruption; and operation mode control means controlling the central processing unit to operate in the transition mode since the start of the idle state until an input of the subsequent time-out interruption, and returning the central processing unit to the normal mode when the time-out interruption is generated.

[0013] According to this aspect of the invention, the central processing unit is operated in a power-saving mode having the longest return time of a plurality of power-saving modes provided in the central processing unit, the maximum of the return time being defined by the interval between time-out interruptions.

[0014] Moreover, it is possible to suitably employ the power-saving mode having a return time longer than that of the power-saving mode in which the processing unit returns to a normal mode before the shortest interruption interval occurring in the system expires so as to perform an interruption process. Accordingly, power consumption in the corresponding period is reduced. Further, since the time-out time of the jobs is managed based on the time-out list such that the time-out interruption occurs at the designated time, unnecessary interruptions are prevented from occurring in the period in which the processing unit is set to the power-saving mode, providing further reduction in power consumption.

[0015] The power-saving mode is selected such that the central processing unit is returned to a normal mode before the next interruption occurs so that the central processing unit is capable of executing the process for the preceding interruption prior to the occurrence of the next interruption. Thus, two successive time-out interruptions are appropriately processed as separate time-out interruptions.

[0016] The computer system is capable of effectively reducing power consumption while an application is being executed, by appropriately switching between the plurality of power saving modes of the central processing unit while appropriately executing jobs based on time-out interruptions.

[0017] The present invention also provides a computer system comprising: transition mode selection means referring to the return time table when the central processing unit is put in an idle state, and selecting, as a transition mode, a power saving mode having the longest return time from a group of one or a plurality of power saving modes having a return time shorter than a period of time that remains until the subsequent time-out interruption; and remaining time setting means setting a period of time that remains after subtracting the return time of the transition mode from the remaining time.

[0018] With this, it is ensured that the processing unit is returned to a normal mode at the time of time-out interruption requested from the job. Therefore, the central processing unit is capable of executing the job at a desired speed at the requested timing. Extension of time required for completion of the job is prevented. The performance of the central processing unit is prevented from dropping.

[0019] According to the invention, the list updating means may update a time-out list listing, for each job requesting a time-out interruption, a difference time from the immediately preceding time-out interruption and a permitted error time permitted for the occurrence of the time-out interruption from the listed job. When it is determined, in setting a next time-out time subsequent to the time-out interruption, that the difference time is longer than the permitted error time, the setting means may successively examine the listed jobs until an accumulation of the difference time is longer than the permitted error time associated with the job, so as to set an accumulated time immediately preceding the satisfaction of the above-mentioned criterion. The central processing unit may successively execute, at the time-out interruption, time-out interruption processes from jobs including the last examined job.

[0020] With this, the frequency of time-out interruptions is reduced. A plurality of idle periods are combined into a single idle period, thereby enabling selection of a power-saving mode characterized by smaller power consumption than when the idle periods are separate. Thus, power consumption is further reduced.

[0021] The list updating means may update the time-out list when there is a time-out interruption request from a new job such that the new job is added to the time-out list at a proper location determined by a time-out interruption request time, and combining time-out interruptions when an error time permitted for the occurrence of the time-out interruption from the new job is longer than a difference in time between the new job and an immediately preceding time-out interruption or a difference in

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time between the new job and an immediately following time-out interruption, such that the immediately preceding time-out interruption or the immediately following time-out interruption is processed as a time-out interruption from the new job.

[0022] With this, the frequency of time-out interruptions is reduced. A plurality of idle periods are combined into a single idle period, thereby enabling selection of a power-saving mode characterized by smaller power consumption than when the idle periods are separate. Thus, power consumption is further reduced.

[0023] The present invention provides a computer readable recording medium storing a program causing a computer to function as: table storage control means causing storage means to store a return time table mapping each of a plurality of power saving modes of a central processing unit into a respective return time required for the central processing unit to return to a normal mode; list updating means updating a time-out list, chronologically listing the time-out interruption requests, based on the time-out interruption requests from the plurality of jobs executed by the central processing unit; setting means setting a next time-out time in the timer means whenever a time-out interruption occurs in accordance with the order listed in the time-out list; transition mode selection means referring to the return time table when the central processing unit is put in an idle state, and selecting, as a transition mode, a power saving mode having the longest return time, from a group of one or a plurality of power saving modes having return times shorter than the time-out time set designated for the subsequent time-out interruption; and operation mode control means controlling the central processing unit to operate in the transition mode since the start of the idle state until an input of the subsequent time-out interruption, and returning the central processing unit to the normal mode when the time-out interruption is generated.

[0024] With this, it is possible to provide the list updating means, the setting means, the transition mode selection means, the operation mode control means in a computer-readable recording medium together with the table storage control means for causing the return time table to be stored in the storage means.

[0025] The computer readable recording medium may store a program causing the computer to function as transition mode selection means referring to the return time table when the central processing unit is put in an idle state, and selecting, as a transition mode, a power saving mode having the longest return time from a group of one or a plurality of power saving modes having a return time shorter than a period of time that remains until the subsequent time-out interruption; and remaining time setting means setting a period of time that remains after subtracting the return time of the transition mode from the remaining time.

[0026] With this, it is possible to provide the list updating means, the setting means, the transition mode selection means, the operation mode control means in a computer-readable recording medium together with the table storage control means for causing the return time table to be stored in the storage means.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027]

Fig. 1 shows a construction of a system showing a construction of a related-art computer system;

Fig. 2 is a block diagram showing a hardware construction of a computer system according to a first embodiment of the present invention;

Fig. 3 is a return time table stored in a recording medium according to the first embodiment;

Fig. 4 is a main flowchart showing an operation of an operating system stored in the recording medium according to the first embodiment;

Fig. 5 is a flowchart showing a branch process performed when it is determined in step of the first embodiment for creation of a branch that a time-out interruption is input in the form of an event;

Fig. 6 shows an example of time-out list according to the first embodiment;

Fig. 7 is a timing chart showing an example of operation executed according to the first embodiment by a central processing unit in accordance with the time-out list of Fig. 6;

Fig. 8 is a flowchart showing a branch process performed when it is determined in step of the second embodiment for creation of a branch that a time-out interruption is input in the form of an event;

Fig. 9 is a timing chart showing an example of operation executed according to the second embodiment by a central processing unit in accordance with the time-out list of Fig. 6;

Fig. 10 is a flowchart showing a branch process performed when it is determined in step of the third embodiment for creation of a branch that a time-out interruption is input in the form of an event;

Fig. 11 shows an example of time-out list according to the third embodiment;

Fig. 12 is a timing chart showing an example of operation executed according to the third embodiment by a central processing unit in accordance with the time-out list of Fig. 11;

Fig. 13 is a flowchart showing a branch process performed when it is determined in step of the fourth embodiment for creation of a branch that a time-out interruption is input in the form of an event; and

Fig. 14 shows how a list is updated in a time-out list updating step of the fourth embodiment.

BEST MODE OF CARRYING OUT THE INVENTION

[0028] Hereinafter, in order to describe the invention in further detail, the best mode of carrying out the inven-

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tion will be described with reference to the attached drawings.

First embodiment

[0029] Fig. 2 is a block diagram showing a hardware construction of a computer system according to a first embodiment of the present invention. Referring to Fig. 2, the system comprises a central processing unit 1 provided, in addition to a normal mode, with a plurality of power saving modes characterized by respective power consumption levels and sequentially executing a program in units of jobs, a random access memory 2 in which a program execution area is set up for the central processing unit 1, a large-capacity memory 3 (storage means) such as a hard disk drive for storing a program etc., a timer (timer means) 4 outputting a time-out interruption to the central processing unit 1 when a preset period of time elapses, a recording medium 5 storing an operating system (OS) executed by the central processing unit 1, an application program (AP) executed on the OS, and various data. Reference numeral 6 indicates a recording medium reader for reading data from the recording medium and 7 indicates a system bus for input and output of data exchanged between the central processing unit 1, the random access memory 2, the large-capacity memory 3, the timer 4 and the recording medium reader 6.

[0030] Fig. 3 is a return time table stored in a recording medium 5 according to the first embodiment. The left column of the table lists power saving modes provided in the central processing unit 1 and the right column lists return time required for the power saving mode to return to the normal mode. The table of Fig. 3 shows that the central processing unit 1 is provided with three power saving modes a, b, c characterized by reduced power consumption, in addition to the normal mode in which the central processing unit 1 is operated at the full operating power. Units of time "0", "1" and "3" are required for the respective power saving modes to return to the normal mode. The longer the period of time required before a return, the smaller the power consumption in the power saving mode.

[0031] Fig. 4 is a main flowchart showing an operation of an operating system stored in the recording medium according to the first embodiment. Referring to Fig. 4, ST1 is an initial setting step wherein execution areas and the return time table are set up in the random access memory 2 in response to the start of the OS, and various environmental settings are established so that the AP is operated on the OS in response to an input of an event. Step ST2 is an event input determination step wherein a determination is made as to whether there is an input from a key (not shown) or the like. Step ST3 is for creation of a branch wherein a determination is made on the type of event so that a job adapted for the event type is executed.

[0032] Fig. 5 is a flowchart showing a branch process performed when it is determined in step ST3 of the first embodiment that a time-out interruption is input in the form of an event. Referring to Fig. 5, step ST4 is a return process step wherein the central processing unit 1 is returned from the power saving mode to the normal mode (operation mode control means). Step ST5 is a setting process step wherein a point of time at which the next time-out interruption is expected is set in the timer 4 (setting means). Step ST6 is a job execution step wherein a job that requested the time-out interruption is executed. Step ST7 is a time-out interruption request determination step wherein a determination is made as to whether a new time-out interruption request is generated as a result of executing the job in the execution step ST6. Step ST8 is a time-out list updating step wherein a new time-out interruption request is added to the time-out list (list updating means). Step ST9 is a cued job determination step wherein a determination is made as to whether there is a cued job to be executed subsequently. Step ST10 is a transition mode selection step (transition mode selection means) wherein a power saving mode, in which the central processing unit 1 should be operated in a transition time prior to the expected time-out interruption input, is selected. The selected mode is designated as a transition mode. Step ST11 is a transition mode setting step wherein the transition mode is set in the central processing unit 1 (operation mode control means).

[0033] The time-out list updated in step ST8 may be a sequential list of the time-out interruption requests not yet processed, and the associated information specifying the timing of the time-out interruptions. For example, the time-out list may be as shown in Fig. 6 in a computer readable format. Referring to Fig. 6, the left column lists jobs that generated time-out interruption requests in the order of occurrence of the time-out interruption requests. The right column lists differences in time (difference time) between a time-out interruption from a job on a given row and an expected time-out interruption from a job in the next row. By using the table described above and formatted as computer readable data, when a time-out interruption occurs, the job located at the head of the data is executed after an elapse of the designated difference time. The job executed is removed from the list so that the job to be executed (selected) next and the associated difference time is placed at the head of the list.

[0034] In the transition mode selection step ST10 of the first embodiment, the return time table is referred to so as to select, as the transition mode, a power saving mode having the longest return time, from a group of one or a plurality of power saving modes having a return time shorter than the difference time designated for the occurrence of the next time-out interruption (the difference time in the second row).

[0035] A description will now be given of the operation according to the first embodiment.

[0036] When the central processing unit 1 provides an

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instruction for installation while the recording medium 5 is set in the recording medium reader 6, the OS and the like are read via the recording medium reader 6 and stored in the large-capacity memory 3. When the central processing unit 1 starts execution of the OS, the initial setting step ST1 is performed. The execution areas and the return time table are set up in the random access memory 2. In this state, the system waits for an input of an event (step ST2). When an event that demands reading from the return time table is input, the table is read via the recording medium reader 6 and stored in the large-capacity memory 3 (table storage control means).

[0037] Subsequently, when a new event demanding execution of the AP is input, the central processing unit 1 starts the designated AP in response to the input of the event so that the jobs of the AP are sequentially executed. When a time-out interruption request occurs, for example, in an input pending state of a job, that time-out interruption is added to the time-out list. When the jobs, including those generated in response to other event inputs, are removed from the cue, the central processing unit 1 makes a transition to the power saving mode so that the system waits for an input of an event again.

[0038] When the preset difference time elapses, the timer 4 issues a time-out interruption to the central processing unit 1. The central processing unit 1 determines that a time-out interruption event is input and performs the steps of the flowchart of Fig. 5. The central processing unit 1 first performs the return process step ST4 so as to make a transition from the power saving mode to the normal mode. In the setting process step ST5, the difference time listed at the head of the time-out list is set in the timer 4. In the job execution step ST6, the job at the first row is executed. The row containing the executed job is then deleted from the list. A determination is made in the time-out interrupt request determination step ST7 as to whether there is generated a time-out interrupt request. When it is determined that the time-out interruption request is generated, the new time-out interruption request is added to the time-out list in the time-out list updating step ST8. When the time-out list updating step ST8 is completed, a determination is made as to whether there is a cued job to be executed subsequently. When it is determined that there is a job to be executed, steps ST6 through ST8 are repeated until the cued jobs are removed. When it is determined at the completion of the time-out list updating step ST8 that there is no more cued jobs to be executed, the transition mode selecting step ST10 is performed so that the difference time listed in the first line (corresponding to the second line in Fig. 6) of the time-out list and the return time table are referred to so as to select, as the transition mode, a power saving mode (a) having the longest return time, from a group of one or a plurality of power saving modes (a) having a return time shorter than the difference time. In the transition mode setting step ST11, the selected transition mode (a) is set in the central processing unit 1. The central processing unit 1 makes a transition to the selected power saving mode and waits for an input of a new event.

[0039] By repeating the above-described steps, the central processing unit 1 executes a predetermined AP in response to an input of an event.

[0040] Fig. 7 is a timing chart showing an example of operation executed according to the first embodiment by the central processing unit 1 in accordance with the time-out list of Fig. 6. Referring to Fig. 7, (a) indicates a time line extending from a current time at "0"; (b) indicates a chart illustrating operating statuses of the central processing unit 1; and (c) indicates a chart indicating a time-out time set in the timer 4. Boxes in the chart (b) in which capital letters are entered indicate duration in which the jobs A, B, ..., E of Fig. 6 are being executed. Two-way arrows to which lower-case letters are attached indicate that the corresponding one of the power saving modes a, b, c of Fig. 3 is being set. Referring to the chart (c), a time out counting in the timer proceeds based on the numeral entered in the boxes. Upward arrows above the borders between the boxes indicate that a time-out interruption occurs.

[0041] As shown in Fig. 7, the central processing unit 1 of the computer system according to the first embodiment executes jobs in the time-out list in the listed order, in accordance with time-out interruption requests from the timer 4 at intervals defined by the difference times. The central processing unit 1 sets a new time-out time in the timer 4 whenever a time-out interruption is input. When the job is completed and an idle time occurs until the execution of the next job (i.e. until the input of an event such as a next time-out interruption), the power saving mode having the longest return time is selected from a group of power saving modes having a return time shorter than the difference time designated for the next time-out interruption so that the system waits for the next time-out interruption. When the next time-out interruption is input, the central processing unit returns from the power saving mode to the normal mode so as to execute the predetermined job.

[0042] Accordingly, an appropriate one of a plurality of power saving modes a, b, c prepared for the central processing unit 1 is selected such that the selection is not restricted by the shortest interruption interval occurring in the computer system. Thereby, the power consumption in the idle state of the central processing unit 1 is effectively reduced. The difference time designated for a time-out interruption from a job is managed based on a time-out list. It is thus known that time-out interruptions are timed to occur as listed in the time-out list. Undesired interruptions are prevented from occurring during the power saving mode so that the power consumption is reduced more effectively.

[0043] The power saving mode is selected to ensure that the central processing unit 1 returns to the normal mode before the occurrence of the next time-out interruption so as to be capable of starting the process re-

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sponsive to the interruption. Therefore, failure to properly respond to a time-out interruption by returning to the normal mode too late is prevented. Two successive time-out interruptions are properly processed as separate interruptions.

[0044] Accordingly, the system according to the first embodiment is capable of effectively reducing power consumption of the central processing unit 1 while an application is being executed, by appropriately executing jobs based on time-out interruptions. Such a system is suitably used in a battery-driven condition.

Second embodiment

[0045] Fig. 8 is a flowchart showing a branch process performed when it is determined in step ST3 of the second embodiment that a time-out interruption is input in the form of an event. Referring to Fig. 8, step ST12 is a transition mode selection step (transition mode selection means) wherein the return time table and the timer 4 are referred to so as to select, of those power saving modes characterized by a return time shorter than the time that remains until the next time-out interruption, a power saving mode characterized by the longest return time. Step ST13 is a remaining time setting step (remaining time setting means) wherein a period of time determined by subtracting the return time of the transition mode from the remaining time is set in the timer 4. The system construction and steps executed by the OS are the same as those in the first embodiment so that the description thereof is omitted.

[0046] A description will now be given of the operation according to the second embodiment.

[0047] When it is determined subsequent to the time-out list updating step ST8 that there are no cued jobs to be executed, the return time table and the timer 4 are referred to in a transition mode selection step ST12 so as to select, of those power saving modes characterized by a return time shorter than the time that remains until the next time-out interruption, a power saving mode characterized by the longest return time. In the remaining time setting step ST13, a period of time determined by subtracting the return time of the transition mode from the remaining time is set in the timer 4. In the transition mode setting step ST11, the selected transition mode is set in the central processing unit 1 so that the central processing unit 1 is returned to the power saving mode to wait for a new event. The other aspects of the operation according to the second embodiment are the same as the corresponding aspects of the first embodiment so that the description thereof is omitted.

[0048] Fig. 9 is a timing chart showing an example of operation executed according to the second embodiment by the central processing unit 1 in accordance with the time-out list of Fig. 6. The legends entered are the same as those of Fig. 7 so that the description thereof is omitted. As shown in Fig. 7, in the computer system according to the second embodiment, the central processing unit 1, once in an idle state, switches to a power saving mode characterized by a return time shorter than a remaining period of time available at the start of the idle state. The value set in the timer is changed to a value obtained by subtraction of the return time of the power saving mode from the remaining period of time.

[0049] Accordingly, in a similar configuration as the first embodiment, the system according to the second embodiment is capable of effectively reducing power consumption while an application is being executed by appropriately executing jobs based on time-out interruptions. Moreover, since a time-out interruption is timed to occur earlier than scheduled point of time specified in the time-out list by selecting the power saving mode appropriately, the period of time by which the interruption is advanced being equal to the return time of the selected power saving mode. Accordingly, at a scheduled interruption time requested by the job, the central processing unit 1 is already in the normal mode for immediate processing of the job. It is thus ensured that execution of the job is started at the same point of time as when the switching to the power saving mode did not occur. Therefore, the period of time that elapses before the completion of the job is prevented from becoming extended and the processing performance of the central processing unit 1 is prevented from dropping.

Third embodiment

[0050] Fig. 10 is a flowchart showing a branch process performed when it is determined in step ST3 of the third embodiment for creation of a branch that a time-out interruption is input in the form of an event. Referring to Fig. 10, step ST14 is a time-out list updating step (list updating means) wherein a time-out list listing, for each job generating a time-out interruption, a time difference (difference time) from an immediately preceding time-out interruption and a permitted error time defining a margin in which the time-out interruption from that job may occur. Step ST15 is a setting process step (setting means) wherein, if it is determined, when setting the next time-out time subsequent to a current time-out interruption, that the difference time is longer than the permitted error time, listed jobs are successively examined until an accumulation of the difference time is longer than the permitted error time associated with the job. The accumulated time immediately preceding the satisfaction of this criterion is set in the timer 4. Step ST16 is a cued job determination step wherein a determination is made as to whether there are any cued jobs to be executed, including the job last examined in step ST15. The system construction and steps executed by the OS are the same as those in the first embodiment so that the description thereof is omitted.

[0051] Fig. 11 shows an example of time-out list according to the third embodiment. Referring to Fig. 11, the right column lists the permitted error times, which

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are introduced in this embodiment and are not found in Fig. 6. Each row stores an error time permitted for the occurrence of the time-out interruption from the job listed in the next row.

[0052] A description will now be given of the operation according to the third embodiment.

[0053] When a time-out interruption is input from the timer 4 to the central processing unit 1, the central processing unit 1 determines that a time-out interruption is input in the form of an event and executes the steps of the flowchart of Fig. 10. In accordance with the illustrated flow, the central processing unit 1 executes the return process step ST4. Further, in a setting process step ST15, the central processing unit 1 sequentially examines the time-out list, starting at the first row, to compare the accumulated difference time with the permitted error time. Job-by-job search is continued until the accumulated difference time is longer than the permitted error time listed in the row. The accumulated time immediately preceding the satisfaction of this criterion is set in the timer 4.

[0054] In a job determination step ST16, a determination is made as to whether there are any cued jobs to be executed, including the job last examined in step ST15. One or a plurality of jobs including those jobs examined in step ST15 are executed in step ST6.

[0055] Whenever the job is executed, a determination is made in the time-out interruption request determination step ST7 as to whether a time-out interruption request occurs. When it is determined that the request occurs, the new time-out interruption request is added to the time-out list in the time-out list updating step ST14. The job, the difference time and the permitted error time are entered in the time-out list. The other aspects of the third embodiment are the same as the corresponding aspects according to the first embodiment so that the description thereof is omitted.

[0056] Fig. 12 is a timing chart showing an example of operation executed according to the third embodiment by a central processing unit in accordance with the time-out list of Fig. 11. The legends entered are the same as those of Fig. 7 so that the description thereof is omitted. As shown in Fig. 12, in the computer system according to the third embodiment, job c, characterized by a permitted error time shorter than the accumulated difference time, is executed following the job b in connection with the time-out interruption from the job B. 16 (=1+15) is set in the timer 4. Similarly, the job E is executed following the job D in connection with the time-out interruption from the job D. 8(=3+5) is set in the timer 4.

[0057] Accordingly, the frequency of time-out interruptions actually occurring is reduced as compared with the first embodiment. Combining a plurality of idle periods into a single idle period enables selection of a power saving mode characterized by lower power consumption as compared to a case where the plurality of idle periods are separated from each other on a time line. Therefore, the low power consumption performance is improved.

Fourth embodiment

[0058] Fig. 13 is a flowchart showing a branch process performed when it is determined in step ST3 of the fourth embodiment for creation of a branch that a time-out interruption is input in the form of an event. Referring to Fig. 13, step ST17 is a time-out list updating step (list updating means) wherein, when there is a time-out interruption request from a new job, the time-out list is updated such that the new job is placed at a proper location determined by the associated time-out interruption request time. When it is determined that the permitted error time designated for the occurrence of the time-out interruption from the new job is longer than the time difference between the new job and the occurrence of time-out interruption from the immediately preceding job, the time-out interruption from the immediately preceding job is also used to trigger the time-out interruption from the new job. The system construction and steps executed by the OS are the same as those in the first embodiment so that the description thereof is omitted.

[0059] A description will now be given of the operation according to the fourth embodiment.

[0060] Fig. 14 shows how a list is updated in a time-out list updating step ST17 of the fourth embodiment. As shown in (a) of Fig. 14, when there is a time-out interruption request from a new job C, the job C is inserted into a proper location (between B and D) based on the time-out interruption request time, as shown in (b) of Fig. 14 so that the time-out list is updated ((b) of Fig. 14). Subsequently, a comparison is made between the permitted error time "4" designated for the job c and the difference time designated for the job C at execution of the job B ("1" in the second row of the list). In this case, since the permitted error time is longer than the difference time, the time list is updated in the time-out list updating step ST17 such that the jobs B and C are placed in the second row, as shown in (a) of Fig. 14. In transition from the stage indicated by (b) to the stage indicated by (c), the difference time in the combined second row is returned to the value of (c) of Fig. 14. The other aspects of the fourth embodiment are the same as the corresponding aspects of the first embodiment so that the description thereof is omitted. Since the jobs B and C are executed in response to the input of the time-out interruption from the job B, the central processing unit 1 operates in the same manner as illustrated in Fig. 12.

[0061] As described, according to the fourth embodiment, a comparison is made between the permitted error time "4" of the newly added job C and the difference time "1" since the job B. Upon determination that the permitted error time is longer than the difference time, for example, the time-out list is updated such that the new job C is executed in response to the input of time-out interruption from the job B. Accordingly, the same

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advantage available in the third embodiment is provided without storing the permitted error time in that the frequency of time-out interruptions actually occurring is reduced. Moreover, according to the fourth embodiment, there is no need to store the permitted error time in the time-out list.

INDUSTRIAL APPLICABILITY

[0062] As described, the computer system and the computer-readable recording medium according to the invention uses the central processing unit provided, in addition to a normal mode, with a plurality of power saving modes characterized by respective power consumption levels and are capable of effectively reducing power consumption of the central processing unit while an application is being executed, by appropriately switching between the plurality of power saving modes while appropriately execute jobs based on time-out interruptions.

Claims

1. A computer system comprising:

a central processing unit provided, in addition to a normal mode, with a plurality of power saving modes **characterized by** respective power consumption levels, and sequentially executing a plurality of jobs generating associated time-out interruption requests;
storage means storing a return time table mapping the plurality of power saving modes of said central processing unit into respective return time required for said central processing unit to return from the corresponding power saving mode to the normal mode;
list updating means updating a time-out list, chronologically listing the time-out interruption requests, based on the time-out interruption requests from the plurality of jobs executed by said central processing unit;
timer means outputting time-out interruptions to said central processing unit when the time-out time listed in the time-out list elapses;
setting means setting a next time-out time in said timer means whenever a time-out interruption occurs in accordance with the order listed in the time-out list;
transition mode selection means referring to the return time table when said central processing unit is put in an idle state, and selecting, as a transition mode, a power saving mode having the longest return time, from a group of one or a plurality of power saving modes having a return time shorter than the time-out time designated for the subsequent time-out interruption; and
operation mode control means controlling said central processing unit to operate in the transition mode since the start of the idle state until an input of the subsequent time-out interruption, and returning said central processing unit to the normal mode when the time-out interruption is generated.

2. A computer system comprising:

a central processing unit provided, in addition to a normal mode, with a plurality of power saving modes **characterized by** respective power consumption levels, and sequentially executing a plurality of jobs generating associated time-out interruption requests;
storage means storing a return time table mapping the plurality of power saving modes of said central processing unit into respective return time required for said central processing unit to return from the corresponding power saving mode to the normal mode;
list updating means updating a time-out list, chronologically listing the time-out interruption requests, based on the time-out interruption requests from the plurality of jobs executed by said central processing unit;
timer means outputting time-out interruptions to said central processing unit when the time-out time listed in the time-out list elapses;
setting means setting a next time-out time in said timer means whenever a time-out interruption occurs in accordance with the order listed in the time-out list;
transition mode selection means referring to the return time table when said central processing unit is put in an idle state, and selecting, as a transition mode, a power saving mode having the longest return time from a group of one or a plurality of power saving modes having a return time shorter than a period of time that remains until the subsequent time-out interruption,
remaining time setting means setting a period of time that remains after subtracting the return time of the transition mode from the remaining time; and
operation mode control means controlling said central processing unit to operate in the transition mode since the start of the idle state until an input of the subsequent time-out interruption, and returning said central processing unit to the normal mode when the time-out interruption is generated.

3. The computer system according to claim 1, wherein said list updating means updates a time-out list list-

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ing, for each job requesting a time-out interruption, a difference time from the immediately preceding time-out interruption and a permitted error time permitted for the occurrence of the time-out interruption from the listed job,

when it is determined, in setting a next time-out time subsequent to the time-out interruption, that the difference time is longer than the permitted error time, said setting means successively examine the listed jobs until an accumulation of the difference time is longer than the permitted error time associated with the job, so as to set an accumulated time immediately preceding the satisfaction of the above-mentioned criterion, and

said central processing unit successively executes, at the time-out interruption, time-out interruption processes from jobs including the last examined job.

4. The computer system according to claim 2, wherein said list updating means updates a time-out list listing, for each job requesting a time-out interruption, a difference time from the immediately preceding time-out interruption and a permitted error time permitted for the occurrence of the time-out interruption from the listed job,

when it is determined, in setting a next time-out time subsequent to the time-out interruption, that the difference time is longer than the permitted error time, said setting means successively examine the listed jobs until an accumulation of the difference time is longer than the permitted error time associated with the job, so as to set an accumulated time immediately preceding the satisfaction of the above-mentioned criterion, and

said central processing unit successively executes, at the time-out interruption, time-out interruption processes from jobs including the last examined job.

5. The computer system according to claim 1, wherein said list updating means updates the time-out list when there is a time-out interruption request from a new job such that the new job is added to the time-out list at a proper location determined by a time-out interruption request time, and combining time-out interruptions when an error time permitted for the occurrence of the time-out interruption from the new job is longer than a difference in time between the new job and an immediately preceding time-out interruption or a difference in time between the new job and an immediately following time-out interruption, such that the immediately preceding time-out interruption or the immediately following time-out interruption is processed as a time-out interruption from the new job.

6. The computer system according to claim 2, wherein said list updating means updates the time-out list when there is a time-out interruption request from a new job such that the new job is added to the time-out list at a proper location determined by a time-out interruption request time, and combining time-out interruptions when an error time permitted for the occurrence of the time-out interruption from the new job is longer than a difference in time between the new job and an immediately preceding time-out interruption or a difference in time between the new job and an immediately following time-out interruption, such that the immediately preceding time-out interruption or the immediately following time-out interruption is processed as a time-out interruption from the new job.

7. A computer readable recording medium storing a program causing a computer to function as:

table storage control means causing storage means to store a return time table mapping each of a plurality of power saving modes of a central processing unit into a respective return time required for the central processing unit to return to a normal mode;

list updating means updating a time-out list, chronologically listing the time-out interruption requests, based on the time-out interruption requests from the plurality of jobs executed by said central processing unit;

setting means setting a next time-out time in said timer means whenever a time-out interruption occurs in accordance with the order listed in the time-out list;

transition mode selection means referring to the return time table when said central processing unit is put in an idle state, and selecting, as a transition mode, a power saving mode having the longest return time, from a group of one or a plurality of power saving modes having return times shorter than the time-out time set designated for the subsequent time-out interruption; and

operation mode control means controlling said central processing unit to operate in the transition mode since the start of the idle state until an input of the subsequent time-out interruption, and returning said central processing unit to the normal mode when the time-out interruption is generated.

8. A computer readable recording medium storing a program causing a computer to function as:

table storage control means causing storage means to store a return time table mapping each of a plurality of power saving modes of a central processing unit into a respective return

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time required for the central processing unit to return to a normal mode;

list updating means updating a time-out list, chronologically listing the time-out interruption requests, based on the time-out interruption requests from the plurality of jobs executed by said central processing unit;

setting means setting a next time-out time in said timer means whenever a time-out interruption occurs in accordance with the order listed in the time-out list;

transition mode selection means referring to the return time table when said central processing unit is put in an idle state, and selecting, as a transition mode, a power saving mode having the longest return time from a group of one or a plurality of power saving modes having a return time shorter than a period of time that remains until the subsequent time-out interruption,

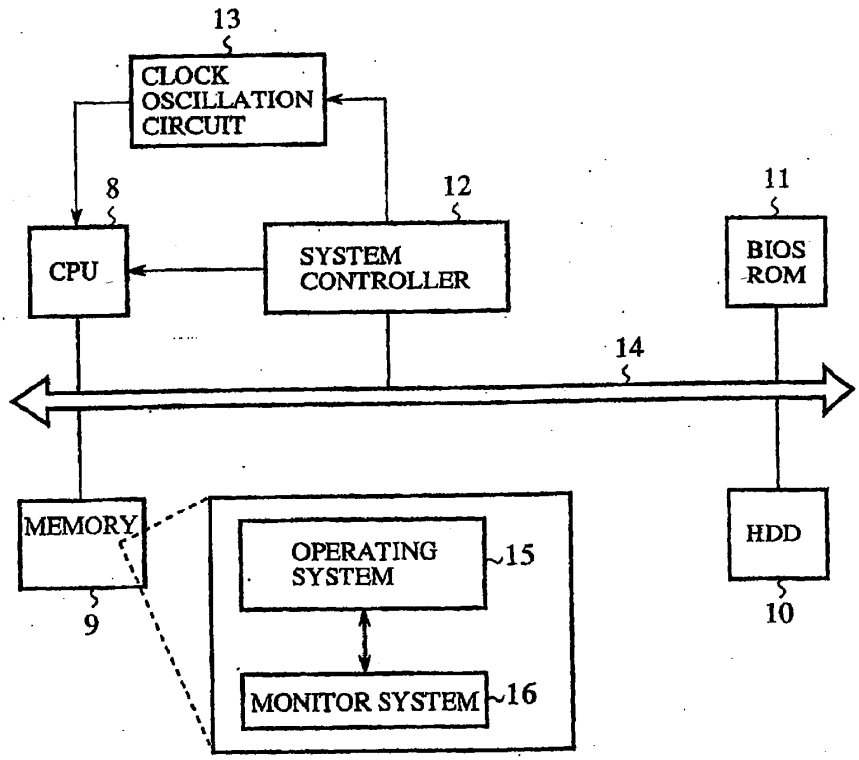
remaining time setting means setting a period of time that remains after subtracting the return time of the transition mode from the remaining time; and

operation mode control means controlling said central processing unit to operate in the transition mode since the start of the idle state until an input of the subsequent time-out interruption, and returning said central processing unit to the normal mode when the time-out interruption is generated.

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FIG.1



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FIG.2

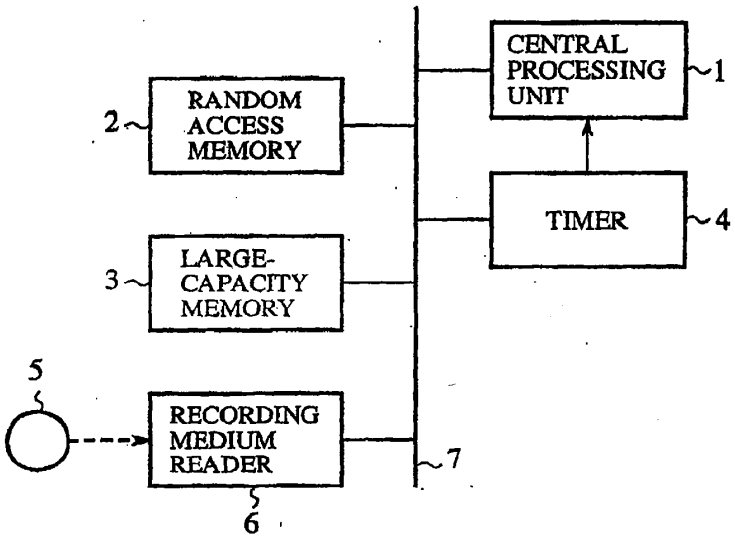


FIG.3

POWER SAVING MODE	RETURN TIME
a	0
b	1
c	3

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FIG.4

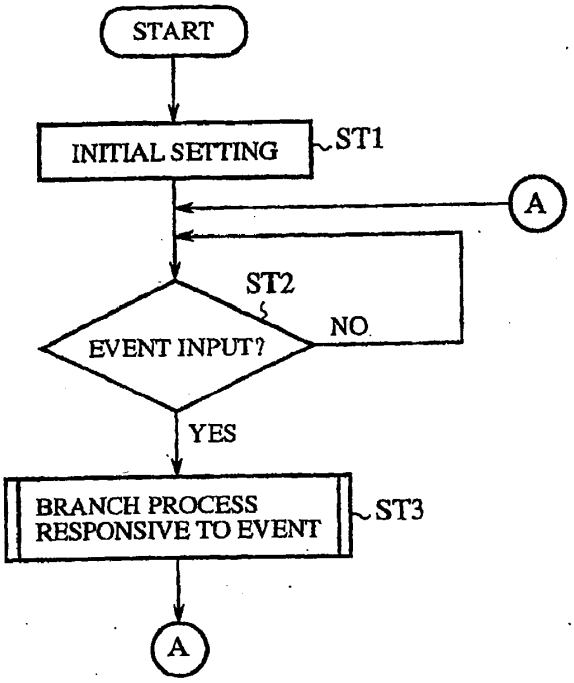


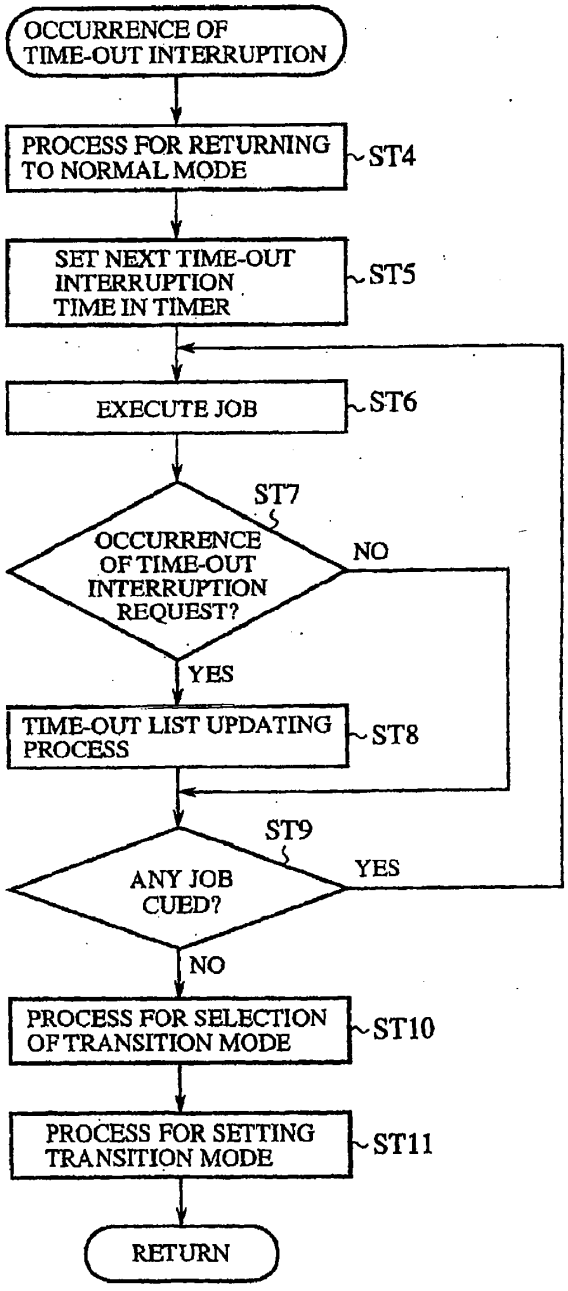
FIG.6

JOB TO BE EXECUTED	DIFFERENCE TIME
A	5
B	1
C	15
D	3
E	5

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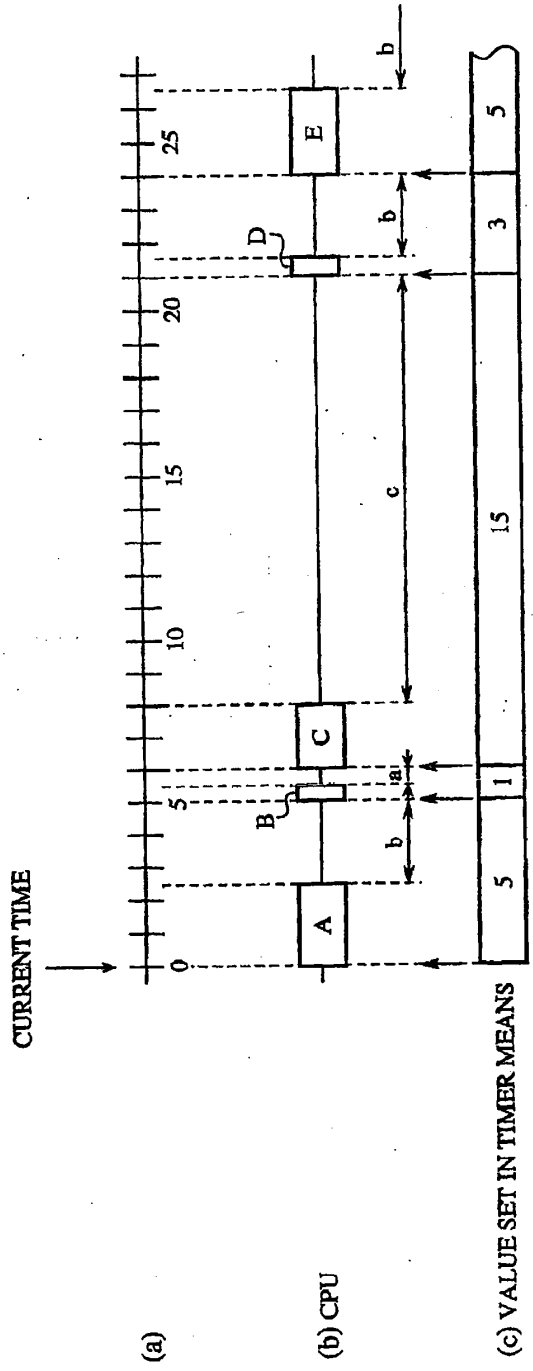
FIG.5



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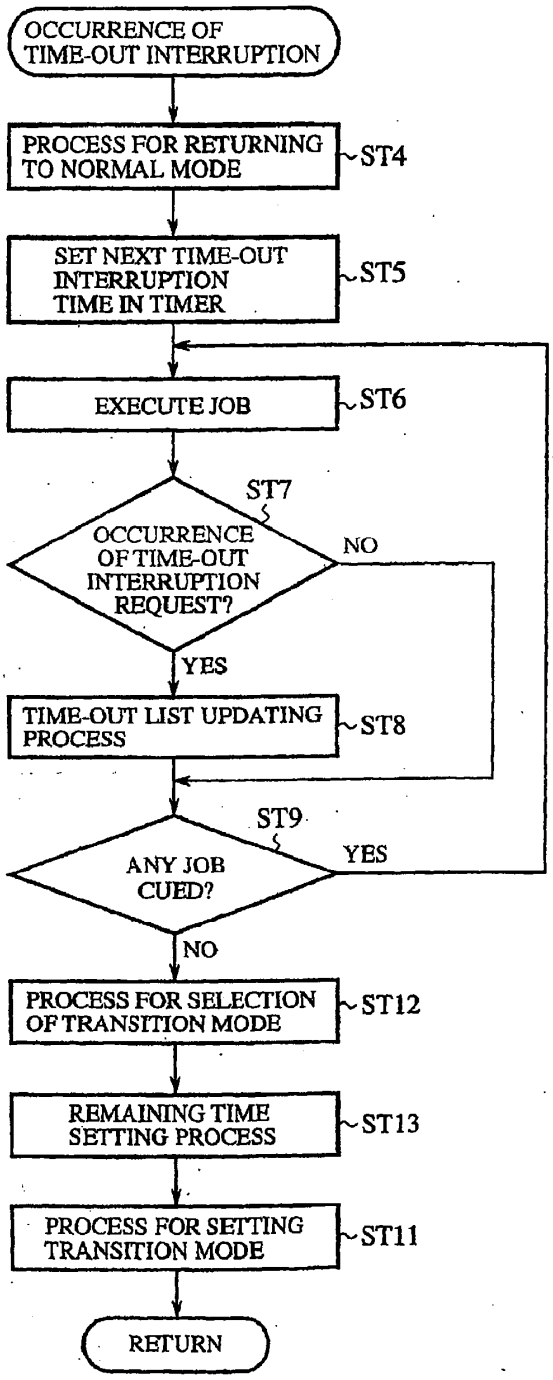
FIG.7



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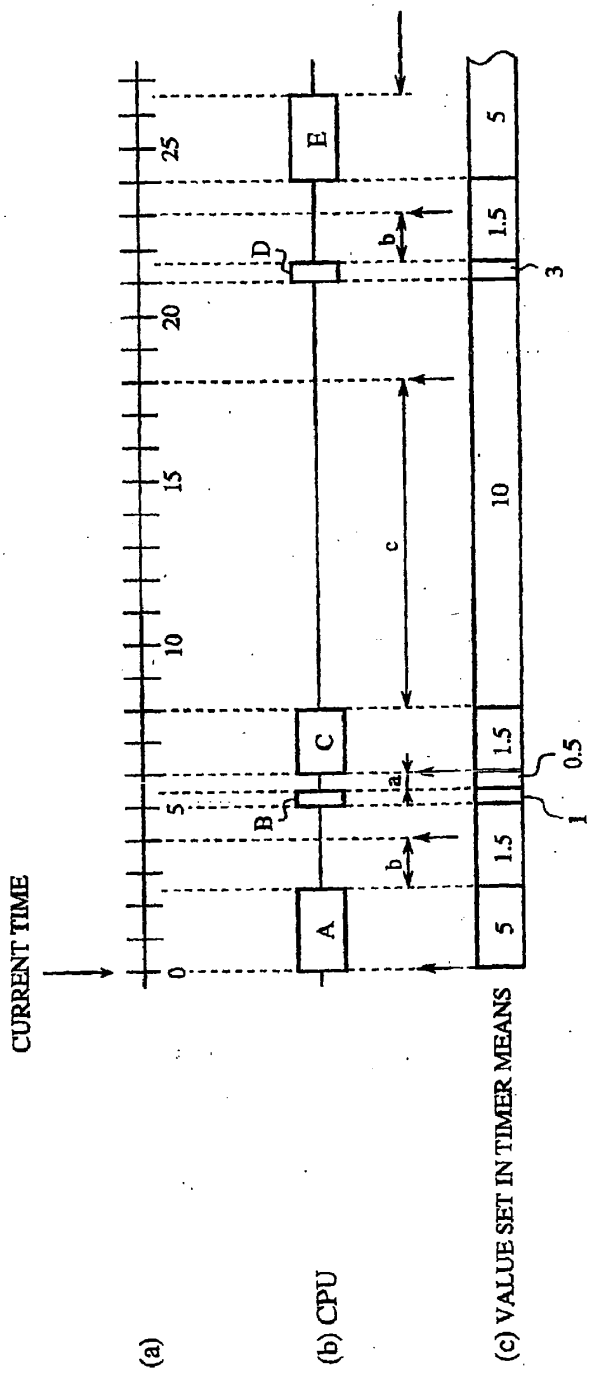
FIG.8



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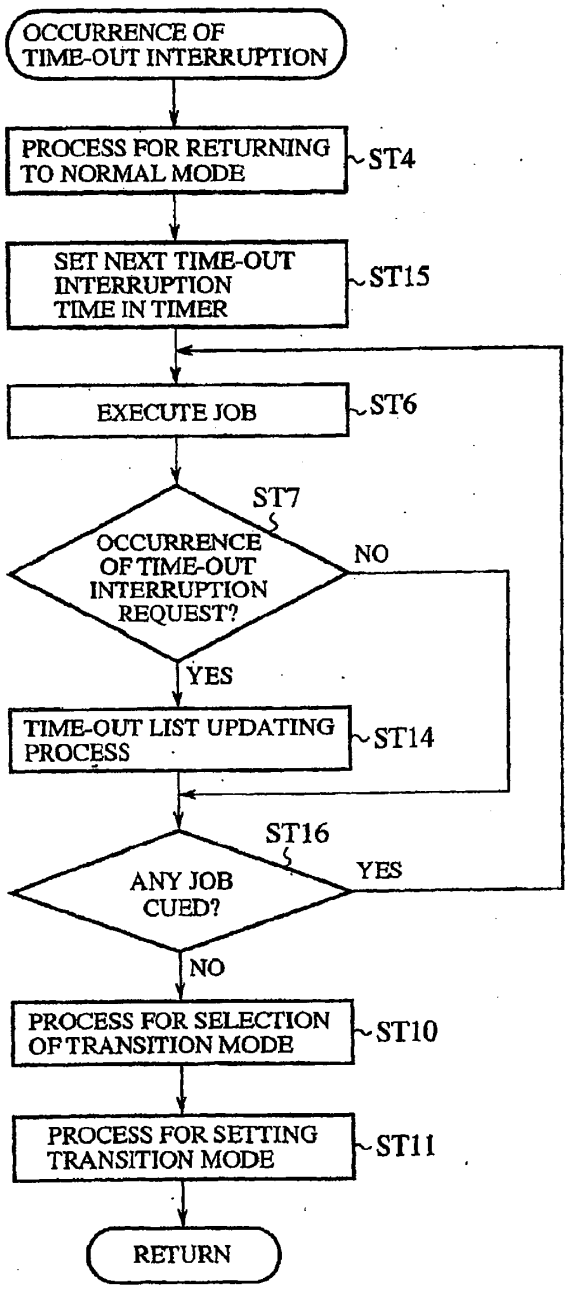
FIG.9



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FIG.10



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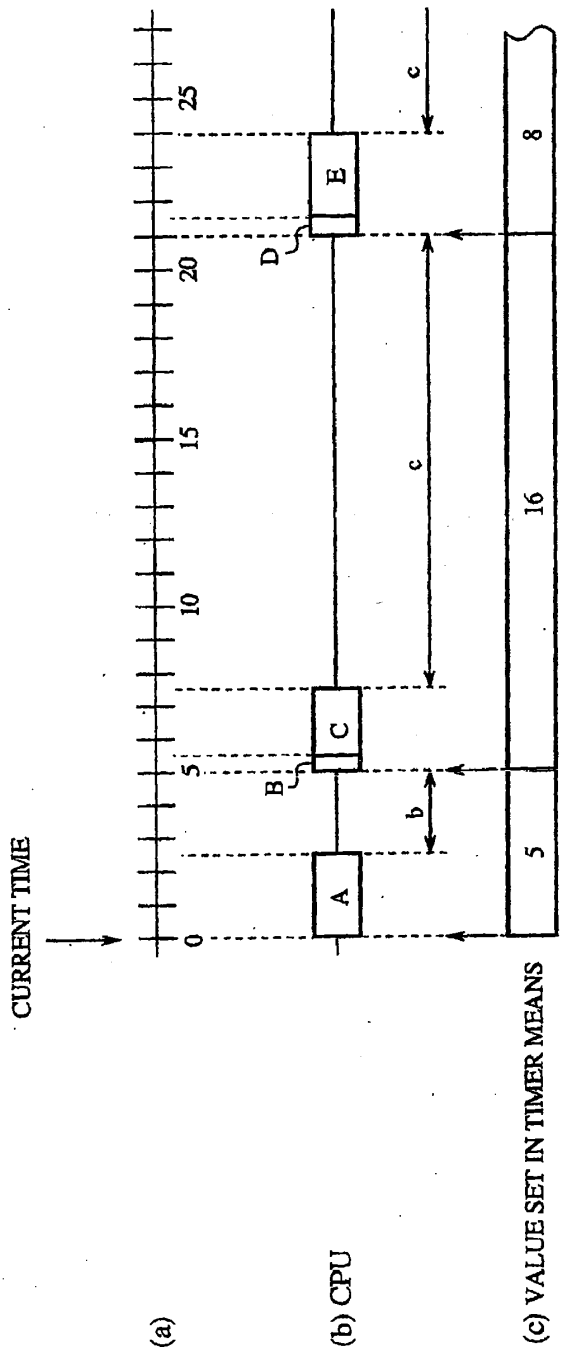
FIG.11

JOB TO BE EXECUTED	DIFFERENCE TIME	PERMITTED ERROR TIME
A	5	2
B	1	4
C	15	0
D	3	4
E	5	4

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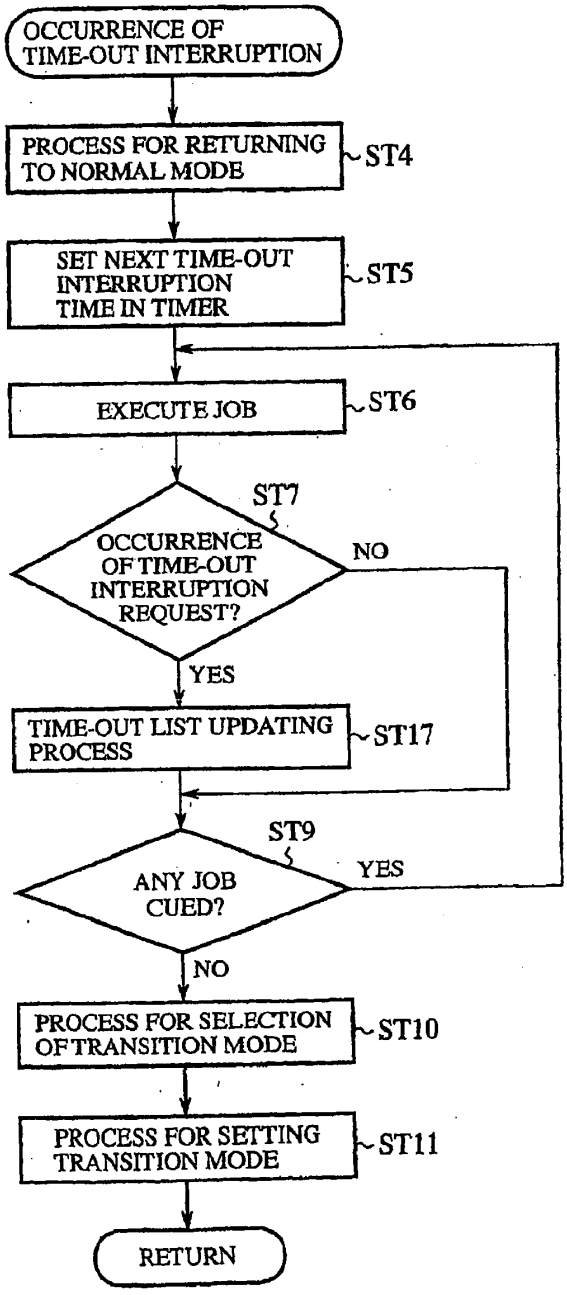
FIG.12



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FIG.13



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FIG.14

(a)

C
6
4

→

POWER SAVING MODE	RETURN TIME
A	5
B	16
D	3
E	5

(b)

POWER SAVING MODE	RETURN TIME	
A	5	
B	1	4
C	15	
D	3	
E	5	

(c)

POWER SAVING MODE	RETURN TIME
A	5
B, C	16
D	3
E	5

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP01/03821

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] G06F1/32

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] G06F1/32

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Toroku Jitsuyo Shinan Koho 1994-2001
Kokai Jitsuyo Shinan Koho 1971-2001 Jitsuyo Shinan Toroku Koho 1996-2001

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP, 6-19592, A (Ricoh Co., Ltd.), 28 January, 1994 (28.01.94), Par. Nos. [0022] to [0026] (Family: none)	1-8
A	JP, 8-234876, A (Fujitsu Ltd.), 13 September, 1996 (13.09.96), Par. Nos. [0021] to [0034] (Family: none)	1-8
A	JP, 7-295694, A (Matsushita Electric Ind. Co., Ltd.), 10 November, 1995 (10.11.95), Par. Nos. [0009] to [0021] (Family: none)	1-8

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 May, 2001 (29.05.01)	12 June, 2001 (12.06.01)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)

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Electronic Acknowledgement Receipt	
EFS ID:	13899755
Application Number:	13225677
International Application Number:	
Confirmation Number:	2063
Title of Invention:	Dynamically Allocating A Power Budget Over Multiple Domains Of A Processor
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Customer Number:	47795
Filer:	Mark J. Rozman/Stephanie Petreas
Filer Authorized By:	Mark J. Rozman
Attorney Docket Number:	ITL.2495US (P38410)
Receipt Date:	03-OCT-2012
Filing Date:	06-SEP-2011
Time Stamp:	12:33:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	ITL2495IDSPwrMgmtToFile.pdf	100006 1d902e5060d47b0b1b4efa3787f2d371496227e6	no	13
Warnings:					
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2	Foreign Reference	ForRefJP1.pdf	2473460 ec845fdda099f8a2bd06f5fc3bad8963e3e54cc8	no	16
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3	Foreign Reference	ForRefJP2.pdf	970344 348a43f5ad665307f230e9ee5b69bcb59028e597	no	8
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Information:					
4	Foreign Reference	ForRefJP3.pdf	3415013 f3be4dc289d035aa76ae22c8b2c2b3d5cb24b234	no	30
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Information:					
5	Foreign Reference	ForDocEP1282030.pdf	3164132 a529a4560038a8519da60a1cc9c74a2528bffc49	no	24
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Information:					
6	Non Patent Literature	ITL2495USIDSNPLDocIDF2010.pdf	676176 d4bb2d32e86df571d90b8f927ce60d52ae8e5154	no	7
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7	Non Patent Literature	ITL2495USNPLDoc2391App.pdf	2784936 be03214bcb7796b02185f6837becaa323db1dda7	no	32
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Information:					
8	Non Patent Literature	NPLDoc2492App13282896.pdf	2031576 b6db5cf79bd4a887ec268881507bd2825aca4a4e	no	24
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Information:					
9	Non Patent Literature	NPLDoc2493App13282947.pdf	2150414 eb7b806ece5265c6903cc45c6ab73a34222f67b0	no	25
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10	Non Patent Literature	NPLDoc2494App13285414.pdf	2591028 fda9be54633173b85952253a401b3ef1ba5c9b6e	no	29

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11	Non Patent Literature	NPLDoc2496App13247580.pdf	1896900 90672de074c3833ae70d28b5c159e71fec63308c	no	22
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Information:					
12	Non Patent Literature	NPLDoc2497App13285465.pdf	1999957 b7ea8a90cb161f2fcc249881d6d62ffe4cc0eb55	no	23
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13	Non Patent Literature	NPLIntelDevForumSandybridgeIDF.pdf	5378 d371740842a1f430b1408bd38ada90d626b0efa7	no	2
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14	Non Patent Literature	NPL2408Spec.pdf	2455146 a0b72b0465e98bb1b79723ffea6da10ad1e2ba0a	no	29
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15	Non Patent Literature	NPLBenini.pdf	1409787 91bc18e367db6c6f27e04587d330187e90754661	no	10
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16	Non Patent Literature	NPLIntelTech.pdf	2536643 61d481fdcacbfb230841be83406bc5f7bed03f52	no	16
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17	Non Patent Literature	NPLIyer.pdf	2075106 8a596da61d74879dc8400adf0e3ea2010a80f60a	no	11
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18	Non Patent Literature	NPLJejurikar.pdf	1107972 409ed57836182898013 59e3b446f927fb6df9615	no	6
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20	Non Patent Literature	NPLKalman.pdf	2776463 cea21f2f1bd2370ca724cd5c74bd8dd8a1526eb9	no	12
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25	Non Patent Literature	NPLSemeraro2.pdf	2366153 0526e267c1c6637d2c3079abade1547ed587ec06	no	12
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26	Non Patent Literature	NPLSemeraro3.pdf	2979756 d803b2367db284a631763f11c05b2db87cce7d1c	no	12
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27	Non Patent Literature	NPLSPEC.pdf	602595 5a6dc7e18fe12e47b5dcebdf8e63a79b13221d14	no	6
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28	Non Patent Literature	NPLTodling.pdf	3122120 5644d1270315238b9239c5b24e6899cf033cac84	no	21

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New International Application Filed with the USPTO as a Receiving Office
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/225,677	09/06/2011	2115	1090	ITL.2495US (P38410)	20	3

CONFIRMATION NO. 2063

47795
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HOUSTON, TX 77057-2631

FILING RECEIPT

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Date Mailed: 09/19/2011

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Applicant(s)

Avinash N. Ananthakrishnan, Hillsboro, OR;
Efraim Rotem, Haifa, ISRAEL;
Doron Rajwan, Rishon Le-Zion, ISRAEL;
Eliezer Weissmann, Haifa, ISRAEL;
Nadav Shulman, Tel Mond, ISRAEL;

Power of Attorney: The patent practitioners associated with Customer Number 47795

Domestic Priority data as claimed by applicant

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If Required, Foreign Filing License Granted: 09/15/2011

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/225,677**

Projected Publication Date: 03/07/2013

Non-Publication Request: No

Early Publication Request: No

MediaTek Exhibit 1002, Page 348 of 398

Title

Dynamically Allocating A Power Budget Over Multiple Domains Of A Processor

Preliminary Class

713

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/225,677

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	330
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	540
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	220
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 52 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 220 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $270 ($135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1090

APPLICATION AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
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The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
ITL.2495US (P38410)
Total Pages in this Submission

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

Dynamically Allocating A Power Budget Over Multiple Domains Of A Processor

and invented by:

Avinash N. Ananthakrishnan; Efraim Rotem; Doron Rajwan; Eliezer Weissmann; Nadav Shulman

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

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Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 25 pages and including the following:
   - a. ☒ Descriptive Title of the Invention
   - b. ☐ Cross References to Related Applications *(if applicable)*
   - c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   - d. ☐ Reference to Sequence Listing, a Table, or a Computer Program Listing Appendix
   - e. ☒ Background of the Invention
   - f. ☐ Brief Summary of the Invention
   - g. ☒ Brief Description of the Drawings *(if filed)*
   - h. ☒ Detailed Description
   - i. ☒ Claim(s) as Classified Below
   - j. ☒ Abstract of the Disclosure

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
ITL.2495US (P38410)
Total Pages in this Submission

Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   a. ☒ Formal Number of Sheets 8
   b. ☐ Informal Number of Sheets
4. ☒ Oath or Declaration
   a. ☒ Newly executed *(original or copy)* ☐ Unexecuted
   b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   c. ☒ With Power of Attorney ☐ Without Power of Attorney
   d. ☐ *DELETION OF INVENTOR(S)*
      Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ CD ROM or CD-R in duplicate, large table or Computer Program (Appendix)
7. ☐ Application Data Sheet (See 37 CFR 1.76)
8. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   a. ☐ Computer Readable Form (CRF)
   b. ☐ Specification Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper
   c. ☐ Statement(s) Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

9. ☐ Assignment Papers *(cover sheet & document(s))*
10. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
11. ☐ English Translation Document *(if applicable)*
12. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations
13. ☐ Preliminary Amendment
14. ☐ Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. ☐ Certificate of Mailing
    ☐ First Class ☐ Express Mail *(Specify Label No.):* **Filed Via EFS**

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UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity) *(Only for new nonprovisional applications under 37 CFR 1.53(b))*	Docket No. ITL.2495US (P38410)
	Total Pages in this Submission

Accompanying Application Parts (Continued)

17. ☐ Additional Enclosures *(please identify below)*:

Request That Application Not Be Published Pursuant To 35 U.S.C. 122(b)(2)

18. ☐ Pursuant to 35 U.S.C. 122(b)(2), Applicant hereby requests that this patent application not be published pursuant to 35 U.S.C. 122(b)(1). Applicant hereby certifies that the invention disclosed in this application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication of applications 18 months after filing of the application.

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19. ☐ Other:

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
ITL.2495US (P38410)
Total Pages in this Submission

Fee Calculation and Transmittal

CLAIMS AS FILED						
For	**#Filed**	**#Allowed**	**#Extra**		**Rate**	**Fee**
Total Claims	20	- 20 =	0	x	$52.00	$0.00
Indep. Claims	3	- 3 =	0	x	$220.00	$0.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
Total # of Pages in Specification	25	**Total # of Drawing Sheets**	8			
Total # of Sheets	33				**Application Size Fee**	$0.00
					Basic Fee	$330.00
					Search Fee	$540.00
					Examination Fee	$220.00
OTHER FEE *(specify purpose)*						$0.00
					TOTAL FILING FEE	$1,090.00

☐ A check in the amount of to cover the filing fee is enclosed.

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Dated: 7/6/11

Signature

Mark J. Rozman, Reg. No. 42,117
TROP, PRUNER & HU, P.C.
1616 S. Voss Road, Suite 750
Houston, TX 77057

Customer Number: **47795**

cc:

ITL.2495US
(P38410)

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: **DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR**

INVENTORS: **AVINASH N. ANANTHAKRISHNAN; EFRAIM ROTEM; DORON RAJWAN; ELIEZER WEISSMANN; NADAV SHULMAN**

Filed Via EFS

Date: September 6, 2011

Prepared by: Trop, Pruner & Hu, P.C., Mark J. Rozman
1616 S. Voss Road, Suite 750, Houston, TX 77057
713/468-8880 [Office], 713/468-8883 [Fax]

DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR

Background

[0001] As technology advances in the semiconductor field, devices such as processors incorporate ever-increasing amounts of circuitry. Over time, processor designs have evolved from a collection of independent integrated circuits (ICs), to a single integrated circuit, to multicore processors that include multiple processor cores within a single IC package. As time goes on, ever greater numbers of cores and related circuitry are being incorporated into processors and other semiconductors.

[0002] Multicore processors are being extended to include additional functionality by incorporation of other functional units within the processor. One issue that arises is that the different circuitry can consume differing amounts of power based on their workloads. However, suitable mechanisms to ensure that these different units have sufficient power do not presently exist.

Brief Description of the Drawings

[0003] FIG. 1 is a flow diagram of a high level method of performing power budget allocations between multiple domains in accordance with an embodiment of the present invention.

[0004] FIG. 2 is a flow diagram of a method describing further details of allocating a package power budget between multiple domains in accordance with an embodiment of the present invention.

[0005] FIG. 3 is a graphical illustration of allocation of a power budget to multiple domains in accordance with one embodiment of the present invention.

[0006] FIG. 4 is a graphical illustration of power consumption for a variety of workloads in accordance with one embodiment of the present invention.

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[0007] FIG. 5 is another graphical illustration of power consumption for a variety of workloads in accordance with an embodiment of the present invention.

[0008] FIG. 6 is a block diagram of a processor in accordance with an embodiment of the present invention.

[0009] FIG. 7 is a block diagram of a multi-domain processor in accordance with another embodiment of the present invention.

[0010] FIG. 8 is a block diagram of a system in accordance with an embodiment of the present invention.

Detailed Description

[0011] In various embodiments, a power budget of a processor including multiple domains can be dynamically apportioned at run time. As used herein the term "domain" is used to mean a collection of hardware and/or logic that operates at the same voltage and frequency point. As an example, a multicore processor can further include other non-core processing engines such as fixed function units, graphics engines, and so forth. Such processor can include at least two independent domains, one associated with the cores (referred to herein as a core domain) and one associated with a graphics engine (referred to herein as a graphics domain). Although many implementations of a multi-domain processor can be formed on a single semiconductor die, other implementations can be realized by a multi-chip package in which different domains can be present on different semiconductor die of a single package.

[0012] In a multi-domain processor, the multiple domains collectively share a single power budget. Accordingly, the higher the frequency at which, e.g., the core domain is operating, the higher the power consumed by the core domain. And in turn, the higher the power consumed by the core domain, there is less power left for the graphics domain to consume and vice versa. On workloads that utilize both one or more cores of a core domain and a graphics engine of a graphics domain, embodiments may at run time dynamically re-partition

how a package power budget is shared between these domains. Thus embodiments provide a power balancing mechanism that can be implemented between the different domains of a multicore processor. For ease of discussion, embodiments described herein are with regard to a multi-domain processor including a core domain and a graphics domain that can share a power budget. However understand the scope of the present invention is not limited in this regard and additional domains can be present. As another example, each core can be allocated to a different domain and each of the domains can be provided with a dynamically re-partitionable amount of a power budget. Furthermore, in addition to core domains and graphics domains, understand that additional domains can be present. For example, another domain can be formed of other processing units such as fixed function units, accelerators or so forth. And a still further domain can be provided for certain management agents of a processor, which can receive a fixed portion of a total power budget.

[0013] In various embodiments a power budget management (PBM) algorithm may be executed by logic such as logic of a power control unit (PCU) of a processor to control the power of an entire processor or an individual domain to a configured power limit. Such algorithm may be based in part on various processor parameters. One such parameter is a guaranteed frequency (P1), which is a frequency that a domain is guaranteed to operate at and not exceed power or thermal specifications of the product. A processor can be tested, e.g., during fabrication to determine this guaranteed frequency, which can be stored in a non-volatile storage or other mechanism of the processor. In various embodiments such guaranteed frequency can be set on a per domain basis. This guaranteed frequency can be fixed upon manufacture and not changed, or in certain embodiments this frequency can be dynamically updated, e.g., as a processor ages due to various degradation mechanisms of the semiconductor product. In various embodiments, all power domains of a processor can be run at their respective guaranteed frequency simultaneously and the processor should not exceed power or thermal specifications.

[0014] Note that this guaranteed frequency can correspond to a performance state of a processor, namely a P1 processor state. According to an operating system (OS)-based mechanism, namely the Advanced Configuration and Platform Interface (ACPI) standard (e.g., Rev. 3.0b, published October 10, 2006), a processor can operate at various performance states or levels, namely from P0 to PN. In general, the P1 performance state may correspond to the highest guaranteed performance state that can be requested by an OS. In addition to this P1 state, the OS can further request a higher performance state, namely a P0 state. This P0 state may thus be an opportunistic state in which, when power and/or thermal budget is available, processor hardware can configure the processor or at least portions thereof to operate at a higher than guaranteed frequency. In many implementations a processor can include multiple so-called bin frequencies above this P1 frequency.

[0015] Another parameter to be used in a PBM algorithm is a maximum turbo frequency (P0), which is a highest frequency at which a domain can operate. This maximum turbo frequency thus is the highest end of multiple bin frequencies greater than the P1 frequency and corresponds to a maximum non-guaranteed highest performance level that can be achieved. Note that at this frequency there are no guarantees on whether the domain exceeds the power or thermal specifications of the processor. In many situations, device characterization during fabrication of a processor can be used to set a maximum turbo frequency, which can be set on a per domain basis. Bin frequencies up to the maximum turbo frequency can be stored in a non-volatile storage or other mechanism of a processor. Note that it is not guaranteed that a processor with more than one domain is able to simultaneously run all domains at their respective maximum turbo frequencies. It is also not guaranteed that a given domain can run at its maximum turbo frequency while other domains are running at their respective guaranteed frequencies.

[0016] Embodiments may dynamically calculate a package power budget which is a metric that measures the power headroom available to the processor for a given time interval.

Depending on this power budget, one or more domains may be controlled to enter into a turbo mode in which a frequency can be raised above the guaranteed frequency.

[0017] In one embodiment, the power budget can be calculated using the following equation:

$E_n = E_{n-1} * alpha + (1-alpha)*(Power\_Limit*deltaT - Energy)$ [1]

where

E_n = energy budget for the current (Nth) evaluation instant (which can be measured in Joules);

E_{n-1} = energy budget carried forward from the previous evaluation instant (which can be measured in Joules);

Power_limit = threshold power level that the processor is configured to maintain, and which may correspond to a thermal design processor (TDP). This thermal design power may thus be a measure of an average power at which the processor can operate. In many implementations, this TDP can be measured in units of power, namely Watts (W). For example, a processor can be rated at a TDP of 40W. This means that on average, the processor can withstand a power consumption level of 40W. But at any instant, its instantaneous power consumption level may be higher or lower than this TDP level.

deltaT = evaluation interval at which a power budget is computed, which in one embodiment may be approximately 1 millisecond (ms);

Energy = energy consumed during the previous evaluation interval, which can be measured in Joules. In one embodiment, energy can be estimated based on counters that trace various micro-architectural activity. For example, an energy value can be associated with each micro-operation retiring, or each cache access. Then based on these events occurring over the time interval, energy consumed can be determined. In another embodiment, energy can be obtained from reading external current and voltage monitoring sensors such as current monitoring circuitry implemented in a voltage regulator; and

alpha = rate of power budget decay, which can be a function of the thermal resistance of a heatsink and cooling solution of the platform. In general, an alpha value can vary inversely with the selected deltaT. Where the deltaT is relatively small, e.g., 1ms, the alpha value may be higher, and vice-versa.

[0018] In various embodiments, a user may be provided with control, e.g., by user-level software to enable the software to determine how package power budget is shared between different domains. In one embodiment, this control can be exposed by way of configuration information that can be set by such software, e.g., as entries in one or more configuration registers. In one particular embodiment of a processor having a first domain and a second domain (also referred to as "planes"), two such configuration registers may be provided as follows in Table 1:

TABLE 1

Primary Plane Turbo Power Policy

[31.5]	[4.0]
Reserved	POLICY_FIRST

Secondary Plane Turbo Power Policy

[31.5]	[4.0]
Reserved	POLICY_SECOND

[0019] These two values, referred to as policy values (and in the example of Table 1 can be 5-bit values), can be used to determine how a package power budget is to be shared between these two domains. For purposes of discussion herein, assume that these two domains are a core domain and a graphics domain. Furthermore, the core domain is referred to also herein as an "IA" domain, referring to processor cores in accordance with an Intel Architecture™ instruction set architecture (ISA) (although embodiments can be used in connection with processors of other manufacturers and ISAs), while the graphics domain can be referred to as a "GT" domain, which refers to an embedded graphics engine that can be implemented on the same die as such IA cores. In one embodiment, the following equations may govern how the package power budget is shared between core and graphics domains:

IA_percentage_of_package_budget = 0.5 + (POLICY_FIRST – POLICY_SECOND)/62 [2]

GT_percentage_of_package_budget = 0.5 + (POLICY_SECOND – POLICY_FIRST)/62 [3]

[0020] More generally, for the case of N domains over which an allocation of a package power budget is based on priority over these N domains, the following equations can be used:

$$BIAS_x = \frac{POLICY_x}{\sum POLICY_i} \qquad [4]$$

$$E_{domain(x)} = E_n * BIAS_x \qquad [5]$$

Here a BIAS can be calculated for each domain x based on the policy value (x) of that domain and the sum of total policy values of all the domains, and again En is the energy budget at time instant n.

[0021] In some embodiments, these configuration registers that store policy values can be controlled generally as incrementing counters. That is, in some embodiments both an OS or other scheduler for the core domain and a graphics driver, which is software and/or firmware that controls various parameters of the graphics engine such as its frequency of operation and so forth, can make requests for a given frequency of operation to the PCU. If the requested frequency is not allowed (e.g., due to a power or thermal limit), the corresponding entity can increment the associated policy value. Thus over time, as a given entity's requests for a higher frequency are not granted, the policy values can be raised. These policy values similarly can be decremented. For example, policy values can be decremented on reset and when a domain gets the frequency it requested, or if a workload profile on the domain changes. For example if the workload utilization on that domain decreases (e.g., C0 residency decreases), the OS or driver software can chose to reduce the policy value for that domain. Then based on these policy values and the above Equations 2 and 3, a percentage of the package budget, e.g., as determined in accordance with Equation 1, can be allocated to each of the domains by controlling their

frequency and/or voltage accordingly. In various embodiments, the above mechanism of splitting budget between the domains is done on a continuous basis every deltaT time interval.

[0022] Referring now to FIG. 1, shown is a flow diagram of a high level method of performing power budget allocations between multiple domains in accordance with an embodiment of the present invention. As shown in FIG. 1, method 100 can be implemented by logic within a processor, such as power sharing logic of a PCU or other power controller. As seen, method 100 may begin by determining a package power budget for a current interval (block 110). In various embodiments, this determination can be made in accordance with Equation 1 above, although other manners of determining a package power budget for a given interval can occur.

[0023] Next, at block 120 a portion of this package power budget to be allocated amongst multiple domains can be determined. For purposes of discussion herein, assume a multi-domain processor including a core domain and a graphics domain. Different manners of allocating or sharing a power budget between these domains can occur in different embodiments. In general however, information regarding the manner in which sharing is to be performed, e.g., as indicated within configuration registers that can be set by system level and/or user-level software in addition to any floors or minimum values to be allocated to the different domains, can be considered in this determination. Accordingly, block 120 determines the allocation of the package power budget to be provided to each domain. Thus control next passes to block 130 where these domains can be controlled in accordance with this allocation. More specifically at block 130 a frequency and/or voltage of these domains can be updated based on the allocated portion of the power budget. In this way, for the given interval each of the domains can execute operations in accordance with this budget. While shown at this high level in the embodiment of FIG. 1, understand the scope of the present invention is not limited in this regard.

[0024] To handle cases where a certain amount of budget may be desired to be reserved for a domain, embodiments may support additional tunable parameters. These parameters, which may also be exposed by way of configuration registers or in another manner, can reserve a predetermined amount of budget for a given domain. In one embodiment, these parameters may be referred to as reservation values and can be used to identify a minimum power budget (e.g., in terms of Watts) to be allocated to a given domain. In the described multi-domain processor, these parameters may be as follows:

Min_reserved_for_IA = amount of budget to be reserved for the core domain; and

Min_reserved_for_GT = amount of budget to be reserved for the graphics domain.

[0025] Referring now to FIG. 2, shown is a flow diagram of a method describing further details of allocating a package power budget between multiple domains in accordance with an embodiment of the present invention. As shown in FIG. 2, method 200 may similarly be performed by power sharing logic of a PCU or other power controller of a processor. Method 200 can begin by obtaining minimum reservation values for the domains (block 210). As in the embodiment of FIG. 1 assume a multi-domain processor including at least a core domain and a graphics domain. These minimum reservation values can be obtained, e.g., from configuration registers set by user-level software to indicate a floor level corresponding to a minimum amount of power budget to be allocated to the given domain. Of course, these values instead can be set by other entities such as an OS and/or graphics driver, respectively for the core and graphics domains.

[0026] At diamond 220 it can be determined whether the package power budget is greater than the minimum reservation value for the second domain. The package power budget can be calculated in different manners, but assume for purposes of discussion that it is calculated in accordance with Equation 1 above. If the budget is not greater than this minimum reservation value, control passes to block 230 where all of the package power budget can be

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allocated to the second domain. Thus the embodiment shown in FIG. 2 favors providing power to the second domain (which may correspond to a graphics domain) over the first domain (which may correspond to a core domain). Although shown with this preference in FIG. 2, understand the scope of the present invention is not limited in this regard, and in other implementations the preference can be in the other direction. And note that this preference can be dynamically changed based on a workload of a processor (e.g., a graphics intensive workload versus a computing intensive workload). As an example, a preference for the graphics domain can be hard mapped to first allocate to the graphics domain and then to the core domain to share the rest between core domain and graphics domain. This decision can be made based on the POLICY_FIRST and POLICY_SECOND values. For example, if POLICY_FIRST is greater than POLICY_SECOND, the preference may be to first allocate to the core domain and then allocate the remaining budget to graphics domain and so on.

[0027] If instead at diamond 220 it is determined that the package power budget is greater than the minimum reservation value for the second domain, control passes to diamond 240, where it can be determined whether the package power budget is greater than this minimum reservation value but less than the sum of the minimum reservation values for the two domains. If this is the case, control passes to block 250 where the minimum reservation value can be allocated to the second domain, and any remaining package power budget can be allocated to the first domain. Note again with regard to this allocation that a preference is made in favor of the second domain over the first domain. But in another implementation (or different workload), the preferences can be in the other direction.

[0028] Finally, if the package power budget is greater than the sum of the minimum reservation values, control passes to block 260 where the minimum reservation values can be allocated to the domains, and then any remaining package power budget can be shared according to sharing policy values. These sharing policy values may also be obtained, e.g., from the configuration registers of Table 1. As one example, these sharing values can be set at

equal values such that the remaining power budget can be allocated equally amongst the two domains. However in other examples, one of the domains may have a higher policy sharing value and thus may obtain more of the available power budget. Although shown with this particular implementation in the embodiment of FIG. 2, understand the scope of the present invention is not limited in this regard. For example, in products having greater than two domains, the analysis may proceed similarly but the available power budget is shared amongst the m>2 variable power domains based on policy values, reservation values, and/or preferences for each of the domains.

[0029] Thus, based on the scenarios in FIG. 2 using the programmable reservation parameters, there can be four potential cases with regard to the packet budget (and assuming that the graphics domain has a higher preference value than the core domain):

1. Package budget < Min_reserved_for_GT. In this case the graphics domain receives the entire package budget, and the core domain receives no part of the package budget.

2. Min_reserved_for_IA + min_reserved_for_GT > Package budget > Min reserved for GT. In this case the graphics domain receives its minimum reservation value and the core domain receives the remaining budget (i.e., Packet budget – Min reserved for GT).

3. Package budget > Min_reserved_for_IA + Min_reserved_for_GT. In this case the graphics domain receives its minimum reservation value and a portion of the budget that exceeds the sum of the minimum reservation values. Identically the core domain receives its minimum reservation value and a portion of the budget that exceeds the sum of the minimum reservation values. The portions allocated to the two domains can be a function of POLICY_FIRST and POLICY_SECOND (of Table 1) as follows:

Pkg_budget_for_IA = Min Guaranteed IA + PKG_BUDGET * IA_percentage_of_package_budget. [6]

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Similarly, Pkg_budget_GT = Min Guaranteed GT +
PKG_BUDGET * GT_percentage_of_package_budget. [7]

4. Package budget > Min reserved for IA + GT but with a non-uniform split. In this case the graphics domain receives its minimum reservation value and a portion of the budget that exceeds the sum of the minimum reservation values. The portion of budget given to the graphics domain is governed by Equation 7 listed above (and that allocated to the core domain in Equation 6). Based on the POLICY_FIRST and POLICY_SECOND values, the excess power budget can by split asymmetrically between the domains. For example if POLICY_FIRST is 0 and POLICY_SECOND is 16, the graphics domain receives 75% of the package budget and the core domain receives the remaining 25%. FIG. 3 is a graphical illustration of the different allocation cores for these four cases, which are listed as cases 1-4 in the illustration.

[0030] To further illustrate how different domains can share a power budget, and furthermore how this power budget can shift between the domains based on a type of workload being executed, reference can be made to FIGS. 4 and 5, which are graphical illustrations of various allocations of a power budget between multiple domains in different workload environments.

[0031] Referring first to FIG. 4, shown is a power consumption diagram in which a graphics domain power consumption is on the X-axis and a core domain power consumption is on the Y-axis. As seen, each domain may have an independent specification power level, which may correspond to a P1 or thermal design power level, which is the maximum guaranteed frequency at which the domain can execute. In addition, the domains can execute at higher power levels in a turbo mode (namely, a higher than guaranteed operating frequency, corresponding to a P0 performance state). As seen, a line 10 joining the axes corresponds to a total package power budget. When a core-intensive workload is executed, the portion of the total power budget allocated to the core domain can be higher, and in turn when a graphics-

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intensive workload is being executed, the portion of the total package power budget being allocated to the graphics domain can be higher.

[0032] As further seen, the sum of the power budgets when both domains are executing at their highest guaranteed frequency corresponds to a sum of the maximum power budgets at a point 20. This sum can exceed the total package power budget and thus, the realistic current maximum power consumption level may fall on a range between points 30 and 40. Operating at points 30 or 40 depends on how the power budget is split between the core and graphics domains. Prioritizing towards the graphics domain will result in operating at point 40 and prioritizing towards the core domain will result in operating at point 30.

[0033] However as seen in FIG. 5, it is possible that both domains can execute at their guaranteed maximum operating frequency and not violate the total package power budget in a turbo mode, as the total package power budget can be set to a higher level 15, when the turbo mode is available. Thus for at least short time periods, a turbo mode may be available in which both domains can at least meet their maximum guaranteed operating frequency.

[0034] Referring now to FIG. 6, shown is a block diagram of a processor in accordance with an embodiment of the present invention. As shown in FIG. 6, processor 300 may be a multicore processor including a plurality of cores $310_a - 310_n$. In one embodiment, each such core may be of an independent power domain and can be configured to operate at an independent voltage and/or frequency, and to enter turbo mode when available headroom exists. The various cores may be coupled via an interconnect 315 to a system agent or uncore 320 that includes various components. As seen, the uncore 320 may include a shared cache 330 which may be a last level cache. In addition, the uncore may include an integrated memory controller 340, various interfaces 350 and a power control unit 355.

[0035] In various embodiments, power control unit 355 may include a power sharing logic 359, which may be a logic to perform dynamic control and re-allocation of an available power budget between multiple independent domains of the processor. In the embodiment of

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FIG. 6, assuming that each core is of an independent power domain, logic 359 can calculate an available power budget for a given time interval and dynamically allocate portions of this available power budget to the different cores. Such allocations can be on equal footing, or preferenced to one or more of the domains. These allocations can thus be based on policy values for the different domains, minimum reservation values for the different domains, and preference values. In one embodiment, these preference values may be of a ranked order in which each domain is ranked according to its preference. For example, in a two domain system the two domains can be ranked as a higher and lower preference such that an algorithm as discussed in FIG. 2 can allocate a minimum reservation value to the higher ranked domain when there is insufficient power budget for both domains' minimum reservation values. And of course such rankings can be extended to additional domains. As further seen in FIG. 6 to provide for storage of various policy values, minimum reservation values and preference values, a power control storage 357 may further be present within PCU 355 to store these various values. Although shown at this location in the embodiment of FIG. 6, understand that the scope of the present invention is not limited in this regard and the storage of this information can be in other locations, such as configuration registers, non-volatile storage or the like.

[0036] With further reference to FIG. 6, processor 300 may communicate with a system memory 360, e.g., via a memory bus. In addition, by interfaces 350, connection can be made to various off-chip components such as peripheral devices, mass storage and so forth. While shown with this particular implementation in the embodiment of FIG. 6, the scope of the present invention is not limited in this regard.

[0037] Referring now to FIG. 7, shown is a block diagram of a multi-domain processor in accordance with another embodiment of the present invention of the present invention. As shown in the embodiment of FIG. 7, processor 400 includes multiple domains. Specifically, a core domain 410 can include a plurality of cores 410a–410n, a graphics domain 420 can include

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one or more graphics engines, and a system agent domain 450 may further be present. In various embodiments, system agent domain 450 may execute at a fixed frequency and may remain powered on at all times to handle power control events and power management such that domains 410 and 420 can be controlled to dynamically enter into and exit low power states. In addition, these domains can dynamically share a package power budget between them in accordance with an embodiment of the present invention. Each of domains 410 and 420 may operate at different voltage and/or power.

[0038] Note that while only shown with three domains, understand the scope of the present invention is not limited in this regard and additional domains can be present in other embodiments. For example, multiple core domains may be present each including at least one core. In this way, finer grained control of the amount of processor cores that can be executing at a given frequency can be realized.

[0039] In general, each core 410 may further include low level caches in addition to various execution units and additional processing elements. In turn, the various cores may be coupled to each other and to a shared cache memory formed of a plurality of units of a last level cache (LLC) $440_0 - 440_n$. In various embodiments, LLC 450 may be shared amongst the cores and the graphics engine, as well as various media processing circuitry. As seen, a ring interconnect 430 thus couples the cores together, and provides interconnection between the cores, graphics domain 420 and system agent circuitry 450.

[0040] In the embodiment of FIG. 7, system agent domain 450 may include display controller 452 which may provide control of and an interface to an associated display. As further seen, system agent domain 450 may include a power control unit 455 which can include a power sharing logic 459 in accordance with an embodiment of the present invention. In various embodiments, this logic may execute algorithms such as shown in FIGS. 1 and 2 to thus dynamically share an available package power budget between the core domain and the graphics domain.

[0041] As further seen in FIG. 7, processor 400 can further include an integrated memory controller (IMC) 470 that can provide for an interface to a system memory, such as a dynamic random access memory (DRAM). Multiple interfaces 480_0 – 480_n may be present to enable interconnection between the processor and other circuitry. For example, in one embodiment at least one direct media interface (DMI) interface may be provided as well as one or more Peripheral Component Interconnect Express (PCI Express™ (PCIe™)) interfaces. Still further, to provide for communications between other agents such as additional processors or other circuitry, one or more interfaces in accordance with a Intel® Quick Path Interconnect (QPI) protocol may also be provided. Although shown at this high level in the embodiment of FIG. 7, understand the scope of the present invention is not limited in this regard.

[0042] Thus in various embodiments, a technique is provided to enable selection of how much of a common power envelope can be allocated to each of multiple independent power domains of a semiconductor device. Note that this power sharing approach is different than conventional power management control of processing engines, which simply acts to select one or more engines to be placed into a low power state, but does not provide for the dynamic power sharing of a power budget between domains as described herein. That is, embodiments provide a mechanism to dynamically share the power budget between different compute components in the same die. As a result, a power budget or power headroom can be reallocated between cores and graphics engine when they are both integrated on the same die. Although embodiments described herein are with regard to a multi-domain processor having at least one core domain and a graphics domain, the scope of the present invention is not so limited, and can be extended to any integrated semiconductor device where common power resources are dynamically allocated between multiple compute entities.

[0043] Embodiments thus may dynamically redistribute power between core domain and graphics domain, enabling flexibility to handle various different workload requirements.

[0044] Embodiments may be implemented in many different system types. Referring now to FIG. 8, shown is a block diagram of a system in accordance with an embodiment of the present invention. As shown in FIG. 8, multiprocessor system 500 is a point-to-point interconnect system, and includes a first processor 570 and a second processor 580 coupled via a point-to-point interconnect 550. As shown in FIG. 8, each of processors 570 and 580 may be multicore processors, including first and second processor cores (i.e., processor cores 574a and 574b and processor cores 584a and 584b), although potentially many more cores may be present in the processors. Each of the processors can include a PCU or other logic to perform dynamic allocation of a package power budget between multiple domains of the processor, as described herein.

[0045] Still referring to FIG. 8, first processor 570 further includes a memory controller hub (MCH) 572 and point-to-point (P-P) interfaces 576 and 578. Similarly, second processor 580 includes a MCH 582 and P-P interfaces 586 and 588. As shown in FIG. 8, MCH's 572 and 582 couple the processors to respective memories, namely a memory 532 and a memory 534, which may be portions of system memory (e.g., DRAM) locally attached to the respective processors. First processor 570 and second processor 580 may be coupled to a chipset 590 via P-P interconnects 552 and 554, respectively. As shown in FIG. 8, chipset 590 includes P-P interfaces 594 and 598.

[0046] Furthermore, chipset 590 includes an interface 592 to couple chipset 590 with a high performance graphics engine 538, by a P-P interconnect 539. In turn, chipset 590 may be coupled to a first bus 516 via an interface 596. As shown in FIG. 8, various input/output (I/O) devices 514 may be coupled to first bus 516, along with a bus bridge 518 which couples first bus 516 to a second bus 520. Various devices may be coupled to second bus 520 including, for example, a keyboard/mouse 522, communication devices 526 and a data storage unit 528 such as a disk drive or other mass storage device which may include code 530, in one embodiment. Further, an audio I/O 524 may be coupled to second bus 520. Embodiments can be

incorporated into other types of systems including mobile devices such as a smart cellular telephone, tablet computer, netbook, or so forth.

[0047] Embodiments may be implemented in code and may be stored on a non-transitory storage medium having stored thereon instructions which can be used to program a system to perform the instructions. The storage medium may include, but is not limited to, any type of disk including floppy disks, optical disks, solid state drives (SSDs), compact disk read-only memories (CD-ROMs), compact disk rewritables (CD-RWs), and magneto-optical disks, semiconductor devices such as read-only memories (ROMs), random access memories (RAMs) such as dynamic random access memories (DRAMs), static random access memories (SRAMs), erasable programmable read-only memories (EPROMs), flash memories, electrically erasable programmable read-only memories (EEPROMs), magnetic or optical cards, or any other type of media suitable for storing electronic instructions.

[0048] While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

1. An apparatus comprising:

a multi-domain processor including a first domain and a second domain, each of the first and second domains to operate at an independent voltage and frequency, the multi-domain processor further including first logic to dynamically allocate a power budget for the multi-domain processor between the first and second domains at run time.

2. The apparatus of claim 1, wherein the first logic is to dynamically allocate the power budget according to a first sharing policy value for the first domain and a second sharing policy value for the second domain, the first and second sharing policy values controllable by user-level software.

3. The apparatus of claim 2, wherein the first logic is to determine a portion of the power budget to allocate to the first domain based on the first sharing policy value.

4. The apparatus of claim 2, wherein the first logic is to dynamically allocate the power budget further according to a first minimum reservation value for the first domain and a second minimum reservation value for the second domain, the first and second minimum reservation values controllable by the user-level software.

5. The apparatus of claim 4, wherein the first logic is to provide at least a first portion of the power budget to the first domain, the first portion corresponding to the first minimum reservation value.

6. The apparatus of claim 1, wherein the first logic is to determine the power budget for a current time interval based at least in part on a power budget carried forward

from a previous time interval, a power consumed in the previous time interval, and a power budget decay value.

7. The apparatus of claim 6, wherein the first logic is to determine the power budget according to $E_n = E_{n-1} * alpha + (1-alpha)*(Power\_Limit*deltaT - Energy)$, where:

E_n is the power budget for the current time interval;

E_{n-1} is the power budget carried forward from the previous time interval;

Power_limit is a threshold power level;

deltaT is a length of the time interval;

Energy is the power consumed during the previous time interval; and

alpha is the power budget decay value.

8. The apparatus of claim 1, wherein the first logic is to dynamically allocate substantially all of the power budget to the first domain for a first workload, and to dynamically allocate substantially all of the power budget to the second domain for a second workload executed after the first workload.

9. A method comprising:

determining, in a power controller of a multi-domain processor, a power budget for the multi-domain processor for a current time interval, the multi-domain processor including at least a first domain and a second domain;

determining, in the power controller, a portion of the power budget to be allocated to the first and second domains; and

controlling a frequency of the first domain and a frequency of the second domain based on the allocated portions.

10. The method of claim 9, wherein determining the portion of the power budget to be allocated to the first and second domains includes allocating the power budget to the second domain and not to the first domain if the power budget is less than a minimum reservation value for the second domain.

11. The method of claim 10, further comprising obtaining the minimum reservation value for the second domain from a configuration register written by user-level software.

12. The method of claim 10, further comprising allocating the minimum reservation value for the second domain to the second domain, and allocating a remaining portion of the power budget to the first domain when the power budget is greater than the minimum reservation value for the second domain but less than a sum of the minimum reservation value for the second domain and a minimum reservation value for the first domain.

13. The method of claim 9, further comprising allocating a minimum reservation value to the first domain and a minimum reservation value to the second domain, and sharing a remaining portion of the power budget according to a first sharing policy value for the first domain and a second sharing policy value for the second domain.

14. The method claim 13, wherein the first sharing policy value is controllable by software executing on the first domain, the first sharing policy value to be incremented when a request for a higher frequency for the first domain is not granted, and the second sharing policy value is controllable by software executing on the second

domain, the second sharing policy value to be incremented when a request for a higher frequency for the second domain is not granted.

15. A system comprising:

a multicore processor having a first domain including a plurality of cores, a second domain including a graphics engine, and a third domain including system agent circuitry, the third domain to operate at a fixed power budget and to dynamically allocate a variable power budget between the first and second domains; and

a dynamic random access memory (DRAM) coupled to the multicore processor.

16. The system of claim 15, wherein the system agent circuitry includes a power sharing logic to determine the variable power budget for a current time interval and to allocate a first portion of the variable power budget to the first domain according to a first power sharing value for the first domain, and to allocate a second portion of the variable power budget to the second domain according to a second power sharing value for the second domain.

17. The system of claim 16, wherein the power sharing logic is to dynamically allocate substantially all of the variable power budget to the first domain for a first workload, and to dynamically allocate substantially all of the variable power budget to the second domain for a second workload executed after the first workload.

18. The system of claim 16, wherein the power sharing logic is to increment the first power sharing value when a request for a higher frequency for the first domain is not granted, and to increment the second power sharing value when a request for a higher frequency for the second domain is not granted.

19. The system of claim 16, wherein the power sharing logic is to further allocate the first portion of the variable power budget according to a first minimum reservation value for the first domain and allocate the second portion of the variable power budget according to a second minimum reservation value for the second domain.

20. The system of claim 16, wherein the power sharing logic is to further allocate the variable power budget according to a preference value, the preference value to favor the second domain over the first domain.

DYNAMICALLY ALLOCATING A POWER BUDGET
OVER MULTIPLE DOMAINS OF A PROCESSOR

Abstract of the Disclosure

In one embodiment, the present invention includes a method for determining a power budget for a multi-domain processor for a current time interval, determining a portion of the power budget to be allocated to first and second domains of the processor, and controlling a frequency of the domains based on the allocated portions. Such determinations and allocations can be dynamically performed during runtime of the processor. Other embodiments are described and claimed.

100

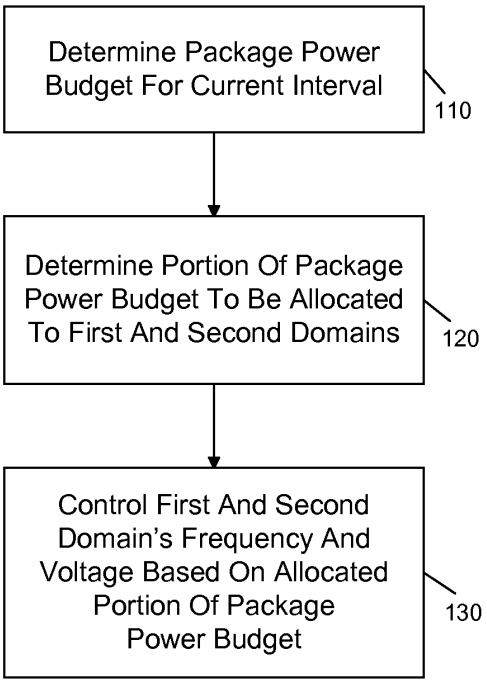

Determine Package Power Budget For Current Interval
110
Determine Portion Of Package Power Budget To Be Allocated To First And Second Domains
120
Control First And Second Domain's Frequency And Voltage Based On Allocated Portion Of Package Power Budget
130

FIG. 1

200

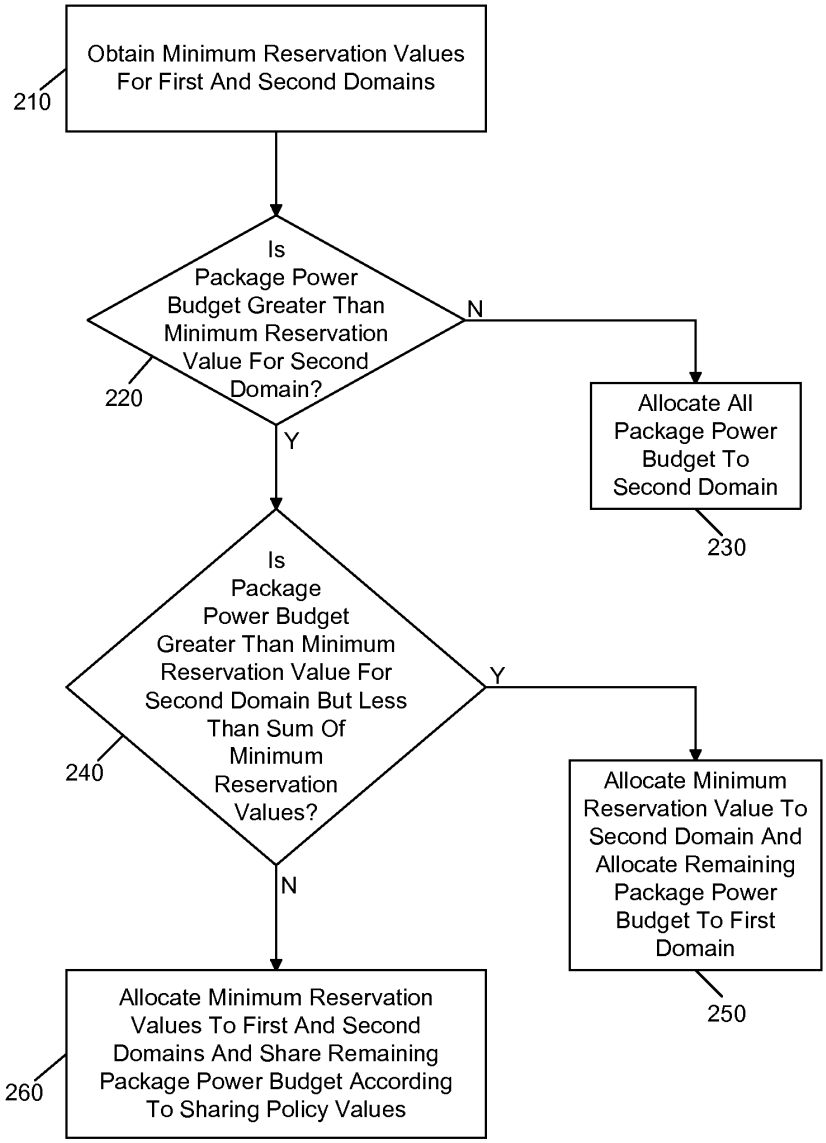

Obtain Minimum Reservation Values For First And Second Domains
210
Is Package Power Budget Greater Than Minimum Reservation Value For Second Domain?
220
N
Y
Allocate All Package Power Budget To Second Domain
230
Is Package Power Budget Greater Than Minimum Reservation Value For Second Domain But Less Than Sum Of Minimum Reservation Values?
240
Y
N
Allocate Minimum Reservation Value To Second Domain And Allocate Remaining Package Power Budget To First Domain
250
Allocate Minimum Reservation Values To First And Second Domains And Share Remaining Package Power Budget According To Sharing Policy Values
260

FIG. 2

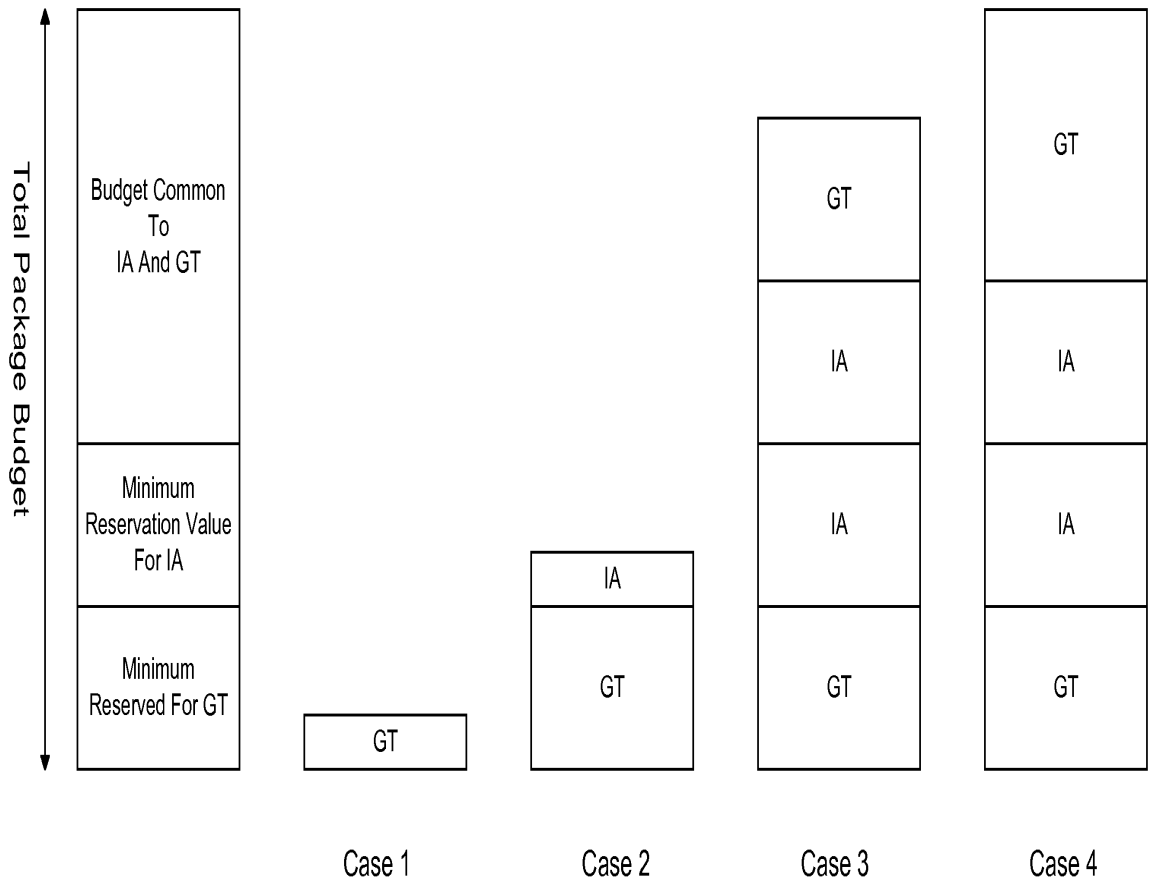

Total Package Budget
Budget Common To IA And GT
Minimum Reservation Value For IA
Minimum Reserved For GT
GT
IA
GT
GT
IA
IA
GT
GT
IA
IA
GT
Case 1
Case 2
Case 3
Case 4

FIG. 3

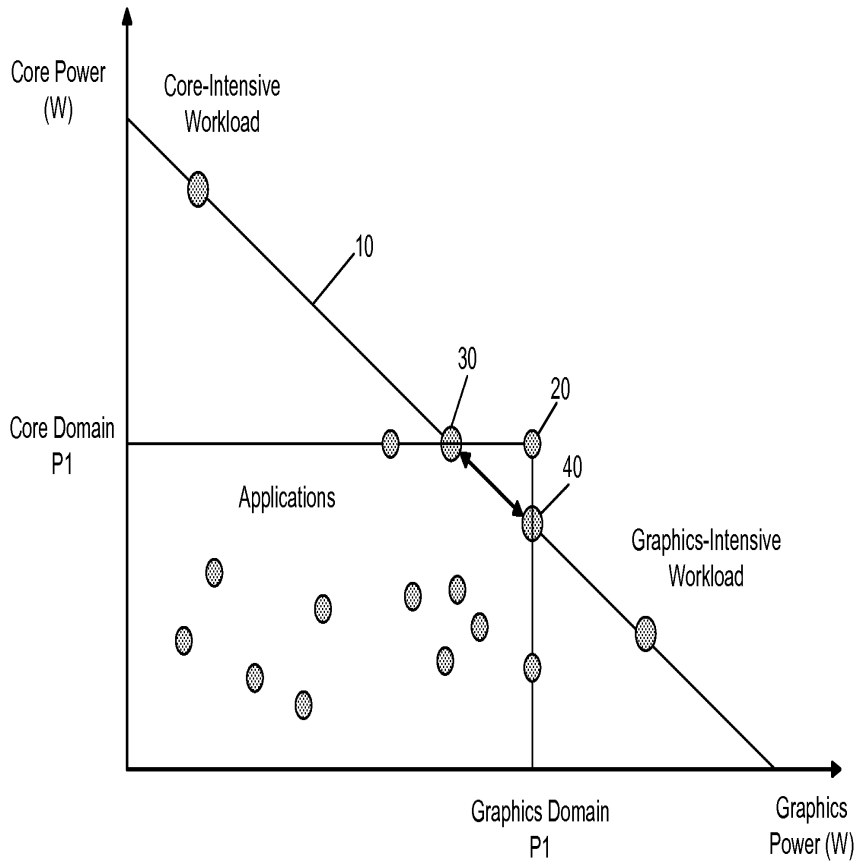

Core Power
(W)
Core-Intensive
Workload
10
30
20
Core Domain
P1
40
Applications
Graphics-Intensive
Workload
Graphics Domain
P1
Graphics
Power (W)

FIG. 4

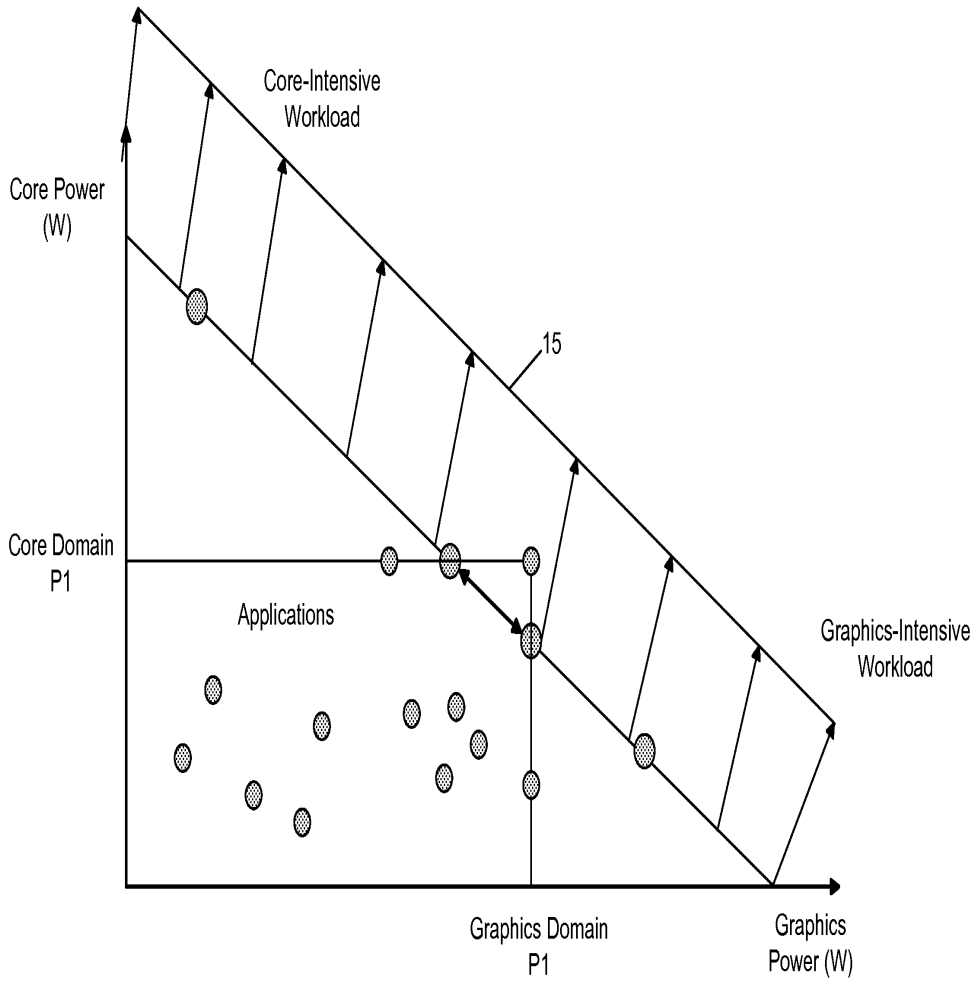

Core-Intensive
Workload
Core Power
(W)
15
Core Domain
P1
Applications
Graphics-Intensive
Workload
Graphics Domain
P1
Graphics
Power (W)

FIG. 5

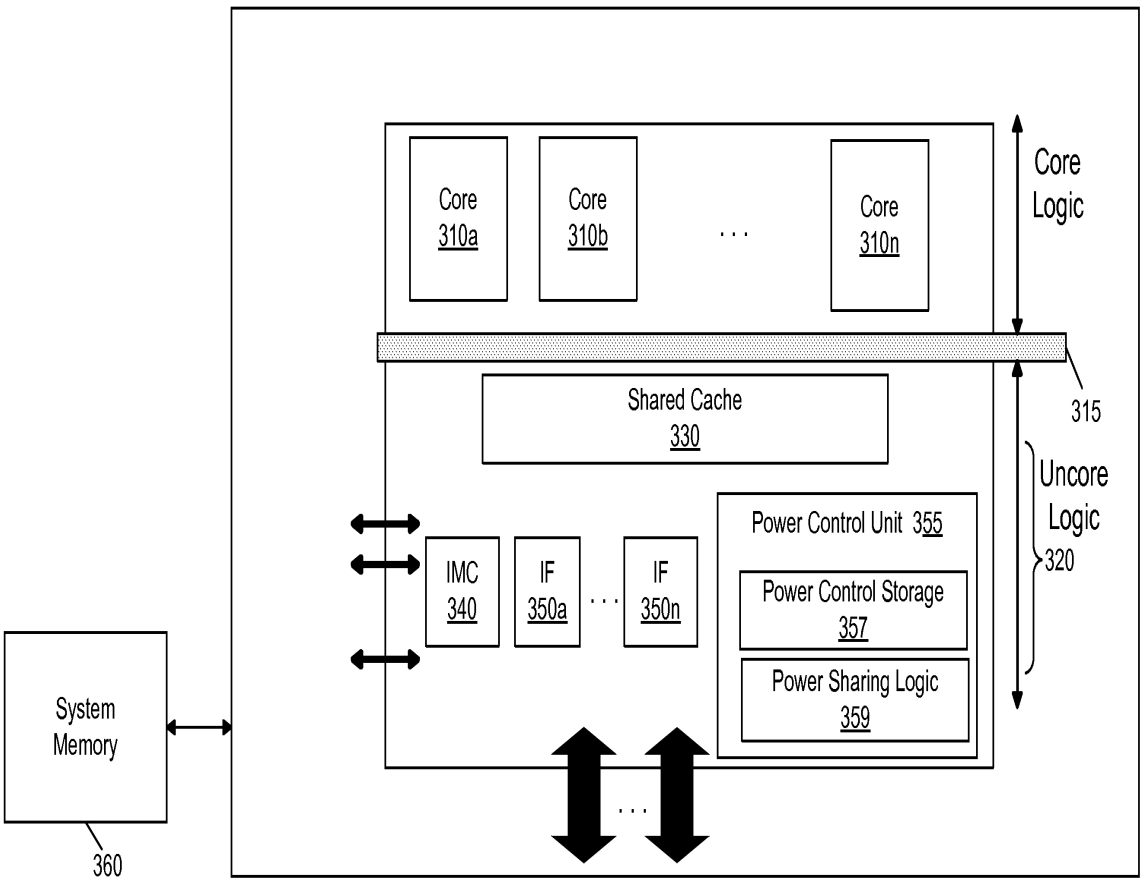

300
Core
310a
Core
310b
Core
310n
Core
Logic
315
Shared Cache
330
Uncore
Logic
320
Power Control Unit 355
Power Control Storage
357
Power Sharing Logic
359
IMC
340
IF
350a
IF
350n
System
Memory
360

FIG. 6

400

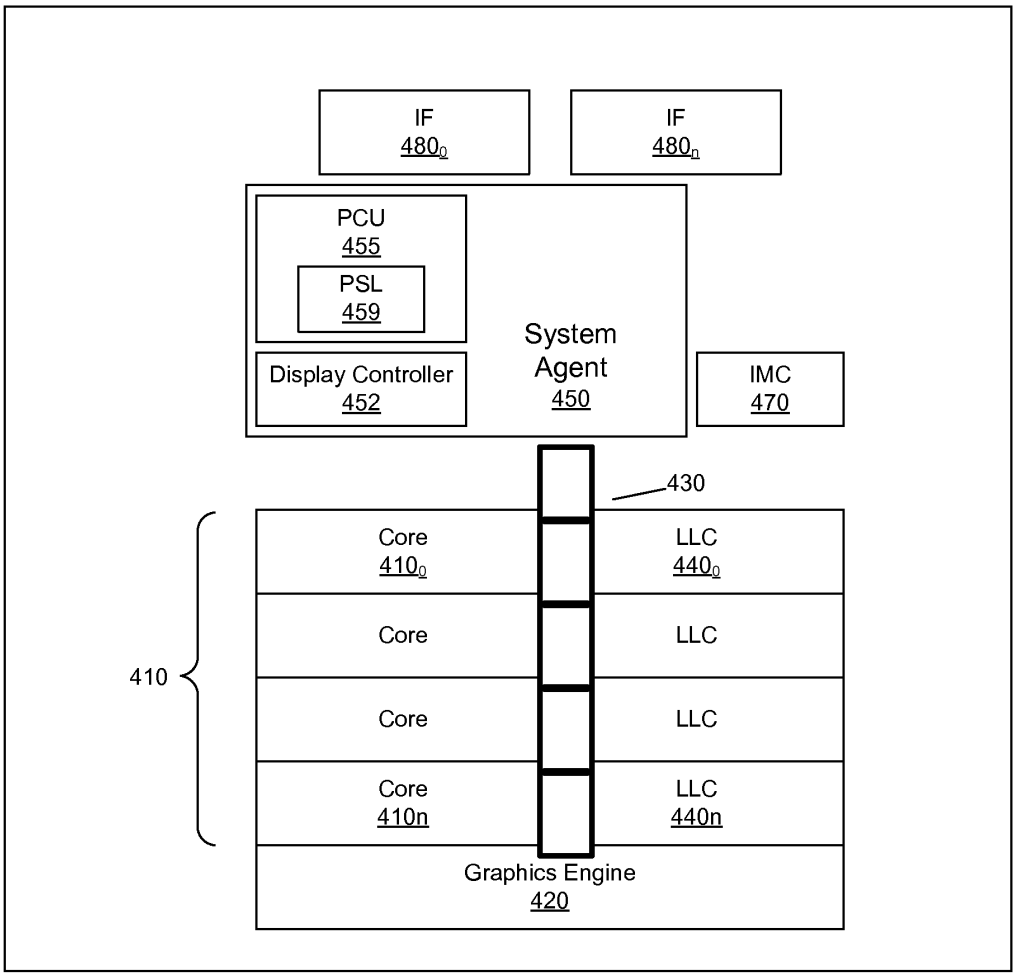

IF
480$_0$
IF
480$_n$
PCU
455
PSL
459
Display Controller
452
System
Agent
450
IMC
470
430
Core
410$_0$
LLC
440$_0$
Core
LLC
Core
LLC
Core
410n
LLC
440n
410
Graphics Engine
420

FIG. 7

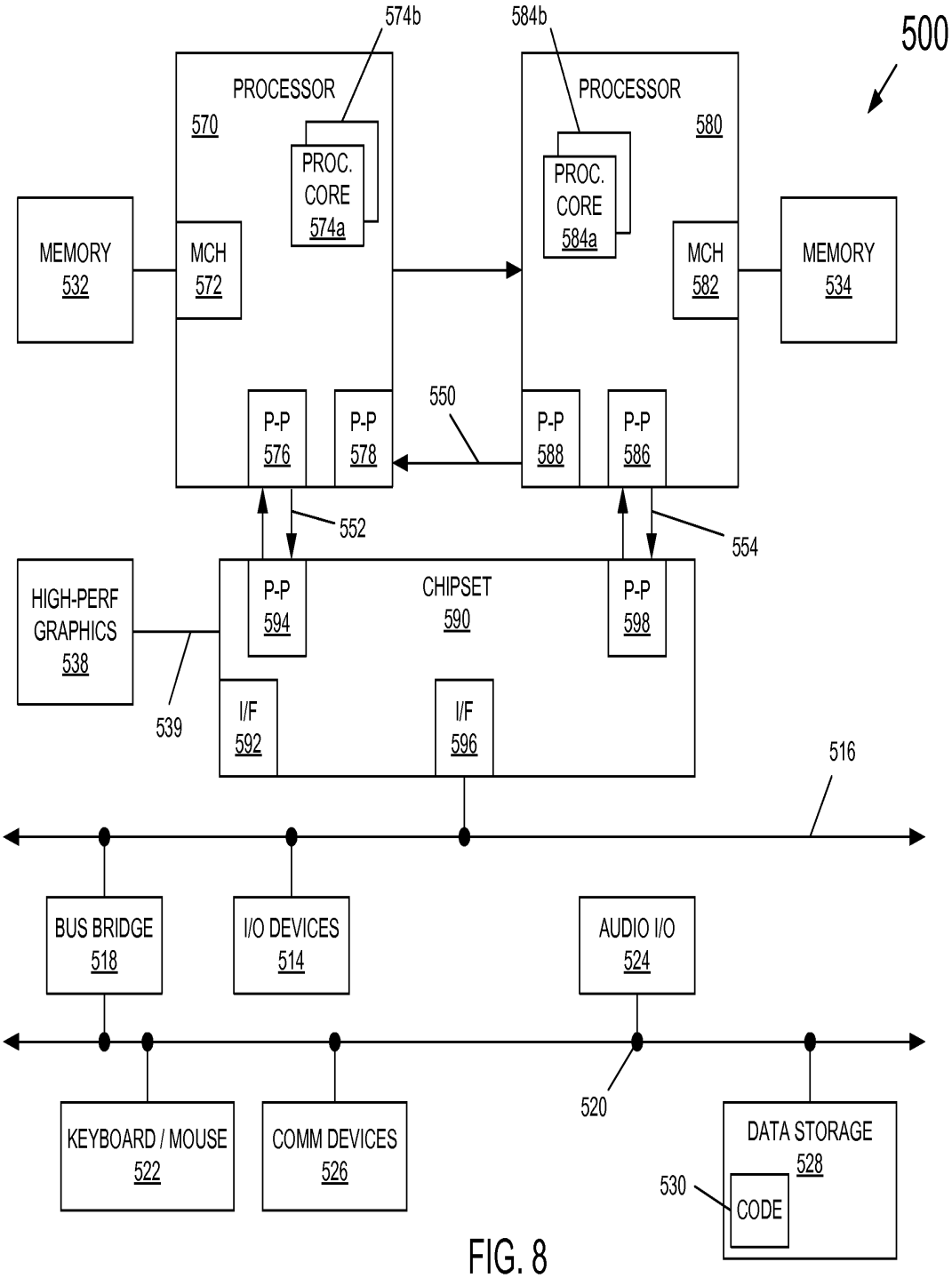

500
574b
584b
PROCESSOR
570
PROC.
CORE
574a
PROCESSOR
580
PROC.
CORE
584a
MEMORY
532
MCH
572
MCH
582
MEMORY
534
550
P-P
576
P-P
578
P-P
588
P-P
586
552
554
HIGH-PERF
GRAPHICS
538
539
P-P
594
CHIPSET
590
P-P
598
I/F
592
I/F
596
516
BUS BRIDGE
518
I/O DEVICES
514
AUDIO I/O
524
520
KEYBOARD / MOUSE
522
COMM DEVICES
526
DATA STORAGE
528
530
CODE

FIG. 8

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, mailing address, and citizenship are as stated below, next to my name.

I believe I am the original and first inventor (if only one name is listed below) or an original and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR

the specification of which (check one):

__X__ is attached hereto.
____ was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____.
(if applicable)

I hereby authorize and request my attorney, associated with Customer Number 47795, to insert on the designated lines above, the filing date, application number, PCT International Application Number and amendment date, as applicable, of the patent application should this Declaration be filed after filing the specification.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed?		Certified Copy Attached?	
(Number)	(Country)	(Foreign Filing Date - MM/DD/YYYY)	Yes	No	Yes	No
(Number)	(Country)	(Foreign Filing Date - MM/DD/YYYY)	Yes	No	Yes	No
(Number)	(Country)	(Foreign Filing Date - MM/DD/YYYY)	Yes	No	Yes	No

I hereby appoint practitioners associated with the Customer Number: **47795**
as my/our attorney(s) or agents(s), with full power of substitution and revocation, to prosecute this application and to

transact all business in the United States Patent and Trademark Office connected therewith.

Please direct all correspondence to the address associated with the Customer Number: 47795

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor AVINASH N. ANANTHAKRISHNAN

Inventor's Signature _____ Date 2-Sep-2011

Residence Hillsboro, OR (City, State) Citizenship INDIA (Country)

Post Office Address 2900 NW Adagio Way, Hillsboro, OR 97124

Full Name of Second Joint Inventor EFRAIM ROTEM

Inventor's Signature _____ Date 2/9/2011

Residence Haifa, HA, IL (City, State) Citizenship ISRAEL (Country)

Post Office Address 8 Vizo Street, Haifa, HA, IL 34400

Full Name of Third Joint Inventor DORON RAJWAN

Inventor's Signature _____ Date 5/9/2011

Residence Rishon Le-Zion, M, IL (City, State) Citizenship ISRAEL (Country)

Post Office Address 13 Odem Street, Rishon Le-Zion, M, IL 00000

Full Name of Fourth Joint Inventor ELIEZER WEISSMANN

Inventor's Signature _____ Date _____

Residence Haifa, HA, IL (City, State) Citizenship ISRAEL (Country)

Post Office Address Albert Switcher 10, Haifa, HA, IL 34995

Docket No. : [illegible] 2005 S P3841.1
PATENT

Transmit all correspondence to the United States Patent and Trademark Office connected therewith.

Please direct all correspondence to the address associated with the Customer Number: **47795**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole or First Joint Inventor: **AVINASH N. ANANTHAKRISHNAN**

Inventor's Signature: [signature] Date: [illegible]

Residence: Hillsboro, OR (City, State) Citizenship: INDIA (Country)

Post Office Address: 2900 NW Adagio Way, Hillsboro, OR 97124

Full Name of Second Joint Inventor: **EFRAIM ROTEM**

Inventor's Signature: [signature] Date: 4/11/2011

Residence: Haifa, HA, IL (City, State) Citizenship ISRAEL (Country)

Post Office Address: 8 Yaziz Street, Haifa, HA, IL 34406

Full Name of Third Joint Inventor: **DORON RAJWAN**

Inventor's Signature: [signature] Date: [illegible]

Residence: Rishon LeZion, MI, IL (City, State) Citizenship ISRAEL (Country)

Post Office Address: 13 Alon Street, Rishon LeZion, MI, IL 75656

Full Name of Fourth Joint Inventor: **ELIEZER WEISSMANN**

Inventor's Signature: [signature] Date: 4/9/2011

Residence: [illegible] (City, State) Citizenship ISRAEL (Country)

Post Office Address: [illegible]

Full Name of Fifth/Joint Inventor NADAV SHULMAN

Inventor's Signature _____ Date: Sep-4-2011

Residence Tel Mond, M, IL (City, State) Citizenship ISRAEL (Country)

Post Office Address Hasayfan 19 Street, POB 447, Tel Mond, M, IL 40600

Electronic Patent Application Fee Transmittal	
Application Number:	
Filing Date:	
Title of Invention:	Dynamically Allocating A Power Budget Over Multiple Domains Of A Processor
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Filer:	Mark J. Rozman/Stephanie Petreas
Attorney Docket Number:	ITL.2495US (P38410)
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1090**

Electronic Acknowledgement Receipt	
EFS ID:	10880170
Application Number:	13225677
International Application Number:	
Confirmation Number:	2063
Title of Invention:	Dynamically Allocating A Power Budget Over Multiple Domains Of A Processor
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Customer Number:	47795
Filer:	Mark J. Rozman/Stephanie Petreas
Filer Authorized By:	Mark J. Rozman
Attorney Docket Number:	ITL.2495US (P38410)
Receipt Date:	06-SEP-2011
Filing Date:	
Time Stamp:	12:16:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1090
RAM confirmation Number	9377
Deposit Account	201504
Authorized User	ROZMAN,MARK J.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	ITL2495USPatentApplicationTrans.pdf	252876 b837f0832f6472ecc8bb65657c7d034291c5ed9b	no	4
Warnings:					
Information:					
2		ITL2495USPatentApplication.pdf	136329 33128906476ebabb468e5d88e70c082f3089af6c	yes	25
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Specification		1	19	
	Claims		20	24	
	Abstract		25	25	
Warnings:					
Information:					
3	Drawings-only black and white line drawings	ITL2495Drawings.pdf	41696 1ec4411c9102795fb2394b64817338103bab13fa	no	8
Warnings:					
Information:					
4	Oath or Declaration filed	ITL2495Declaration.pdf	189544 e7311cd3b0432e4f017a73a98951d4d9ab607dcf	no	4
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	33232 8cb54924dea749722e0d802e911a7bdf24d87b6b	no	2
Warnings:					
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		Total Files Size (in bytes):	653677		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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Application Number: 13225677 Document Date: 9/6/2011

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