

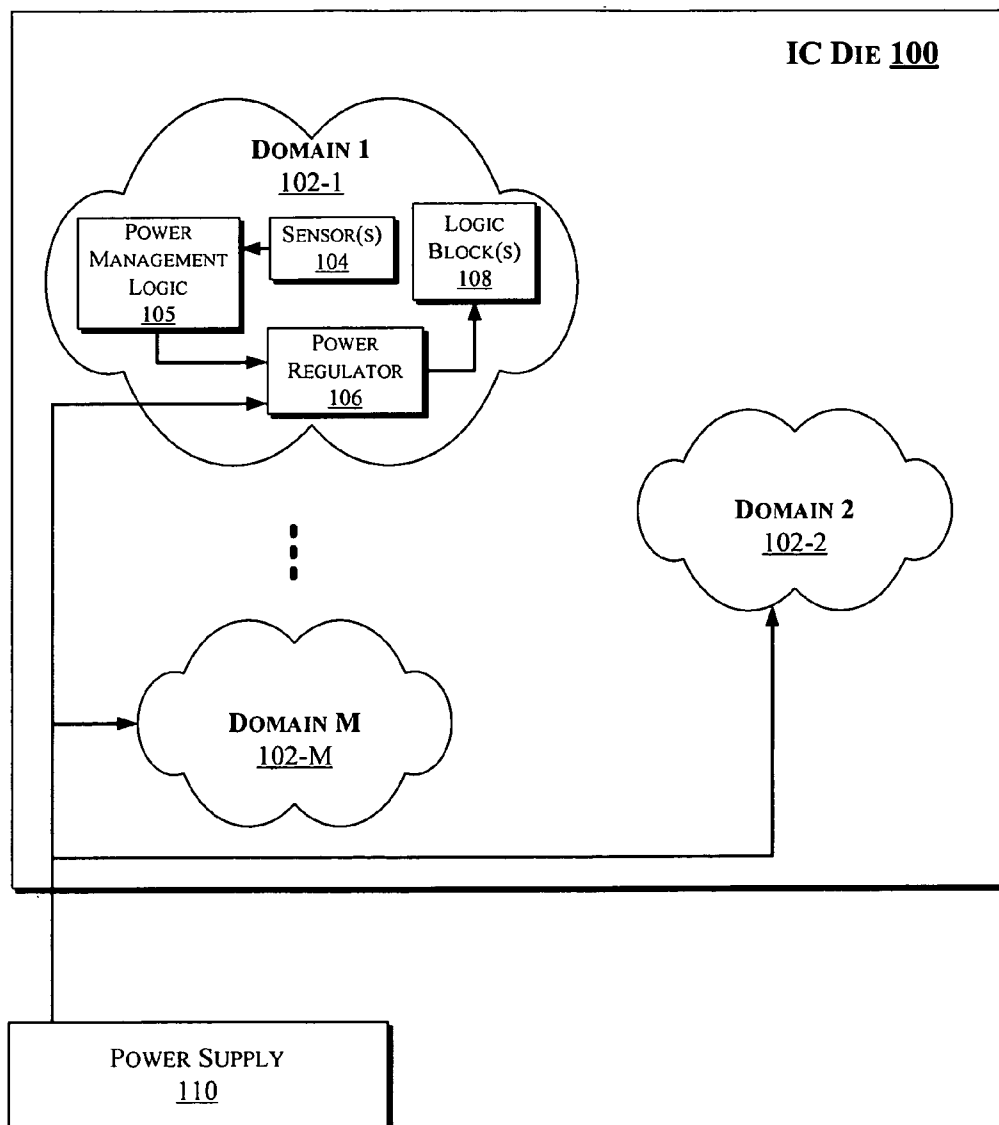


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(19) **United States**(12) **Patent Application Publication**
Gunther et al.(10) **Pub. No.: US 2008/0136397 A1**(43) **Pub. Date: Jun. 12, 2008**(54) **OPERATING INTEGRATED CIRCUIT LOGIC
BLOCKS AT INDEPENDENT VOLTAGES
WITH SINGLE VOLTAGE SUPPLY**(21) Appl. No.: **11/636,425**(22) Filed: **Dec. 8, 2006**(76) Inventors: **Stephen H. Gunther**, Beaverton,
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OR (US)**Publication Classification**(51) **Int. Cl.**
G05F 5/00 (2006.01)(52) **U.S. Cl.** **323/299**(57) **ABSTRACT**

Methods and apparatus to operate various logic blocks of an integrated circuit (IC) at independent voltages are described. In one embodiment, supply of power to one or more domains in an IC is adjusted based on an indication that power consumption by components of the corresponding domain is to be modified. Other embodiments are also described.

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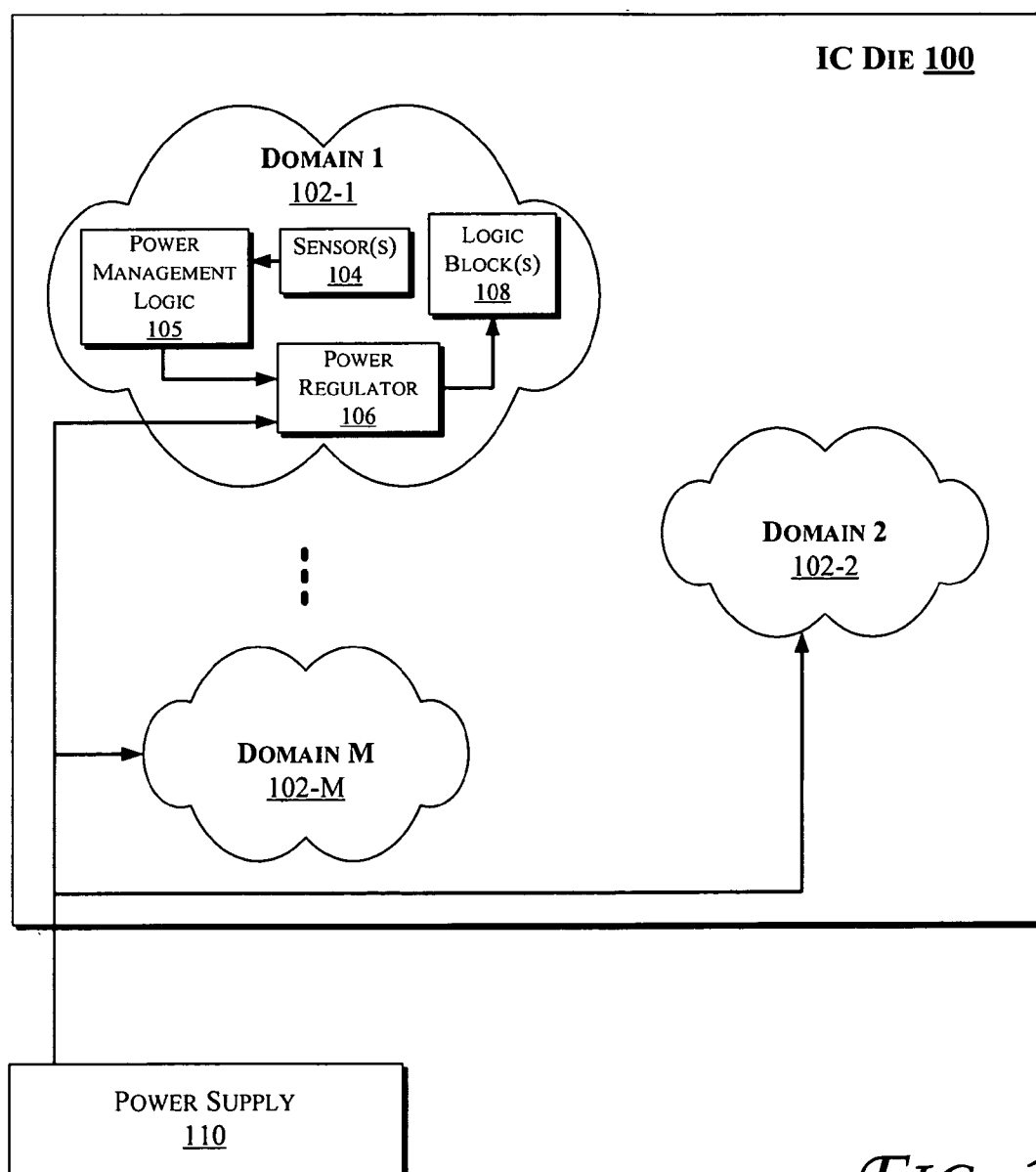
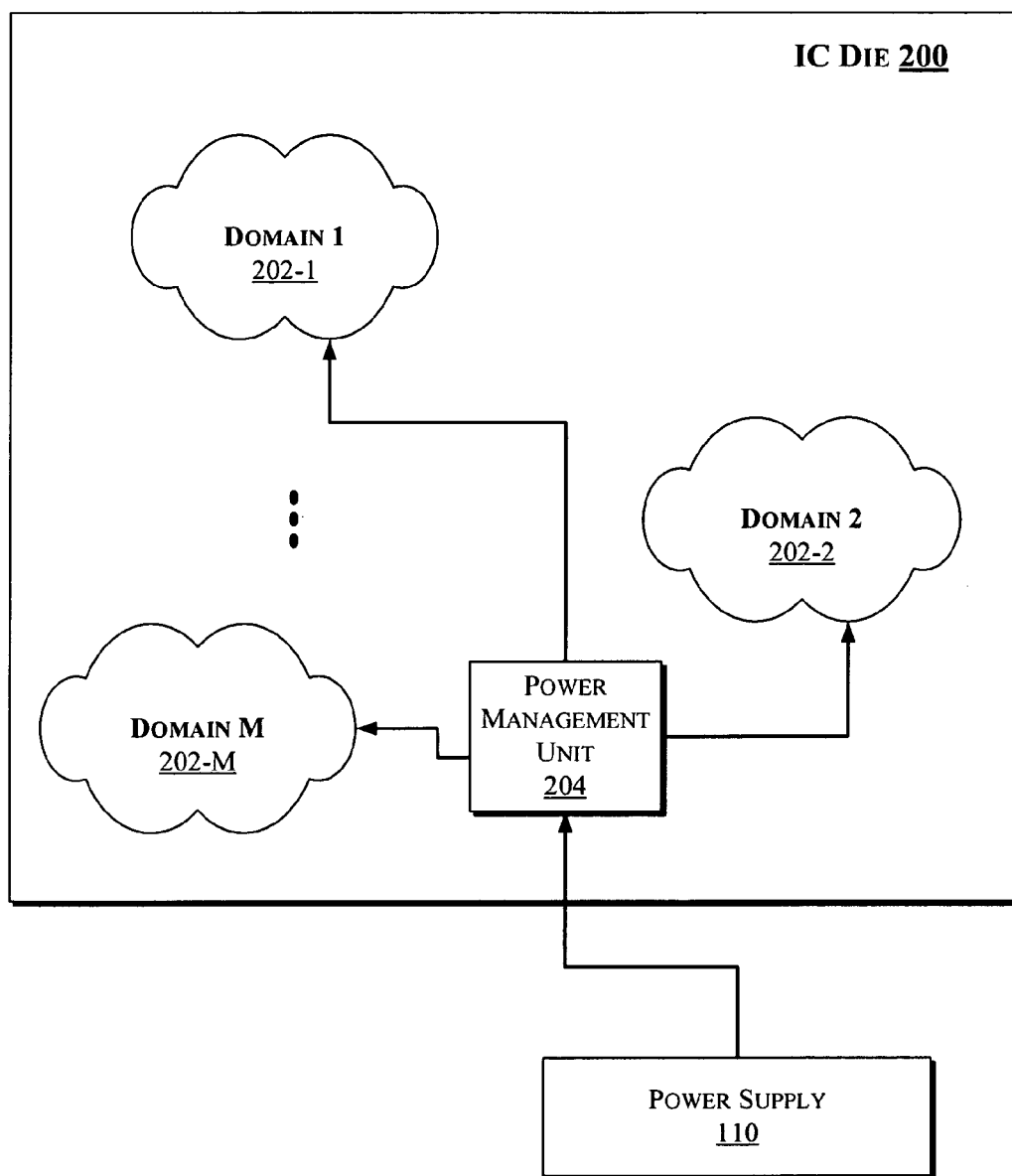
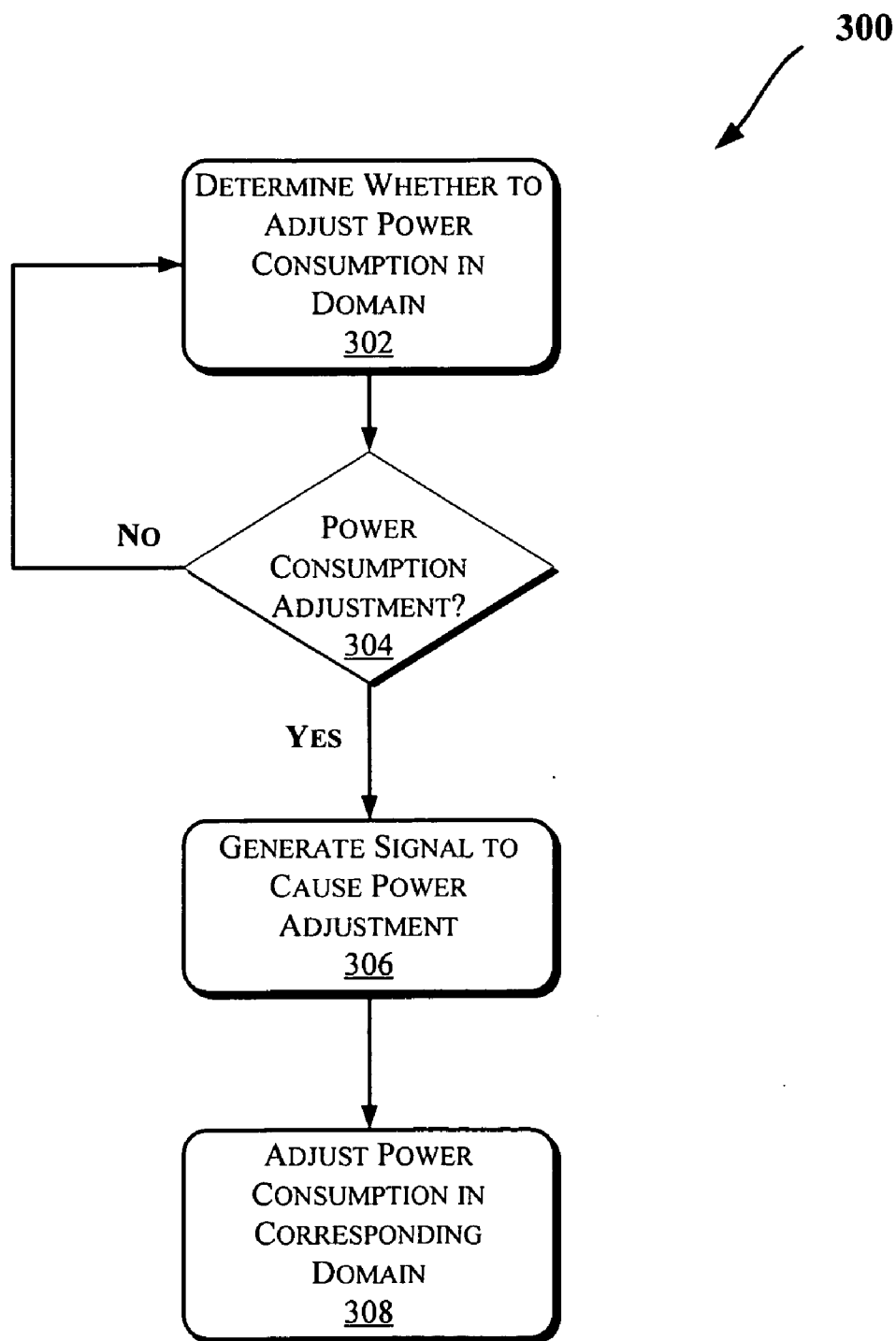
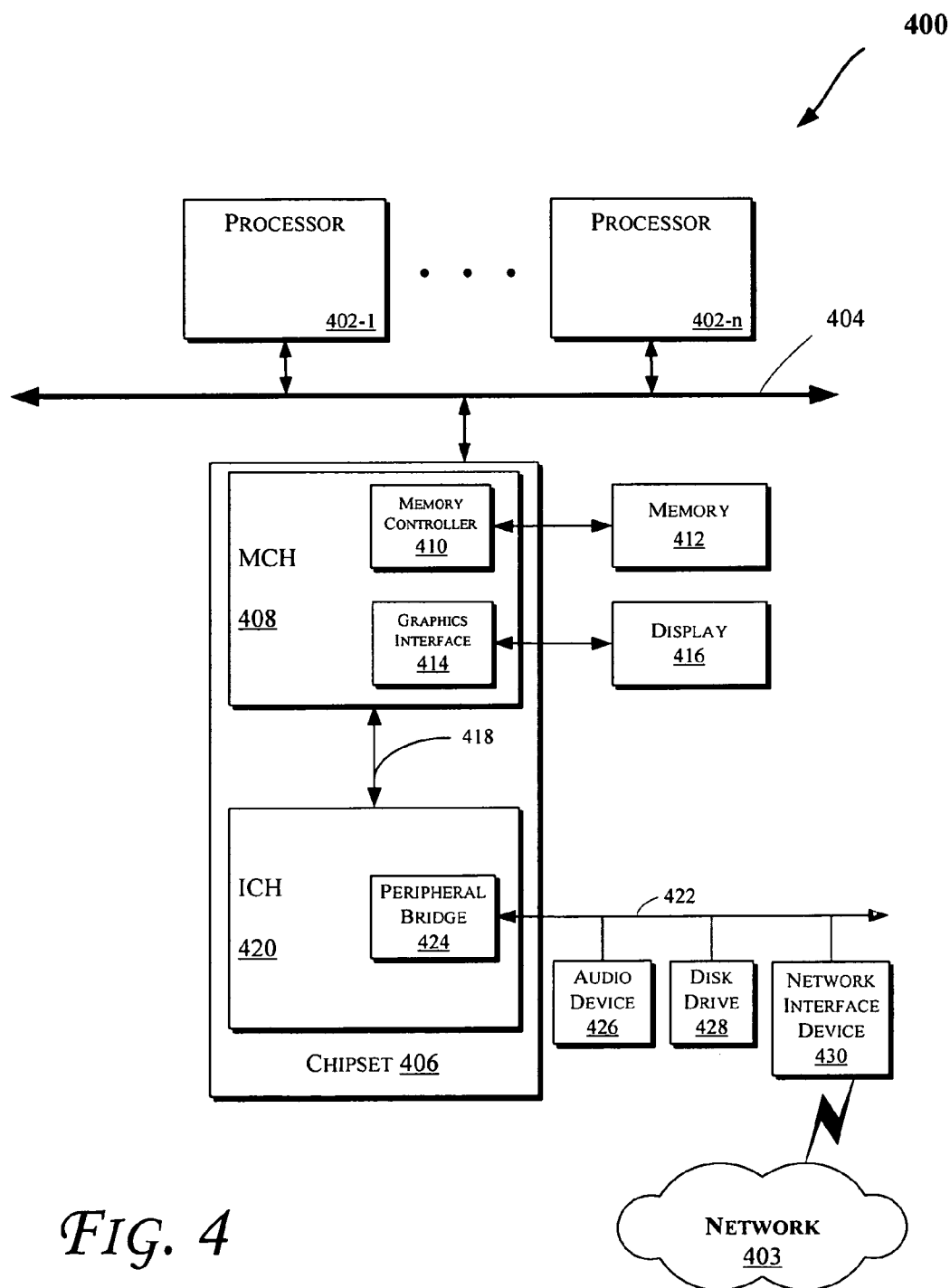


FIG. 1

*FIG. 2*

*FIG. 3*



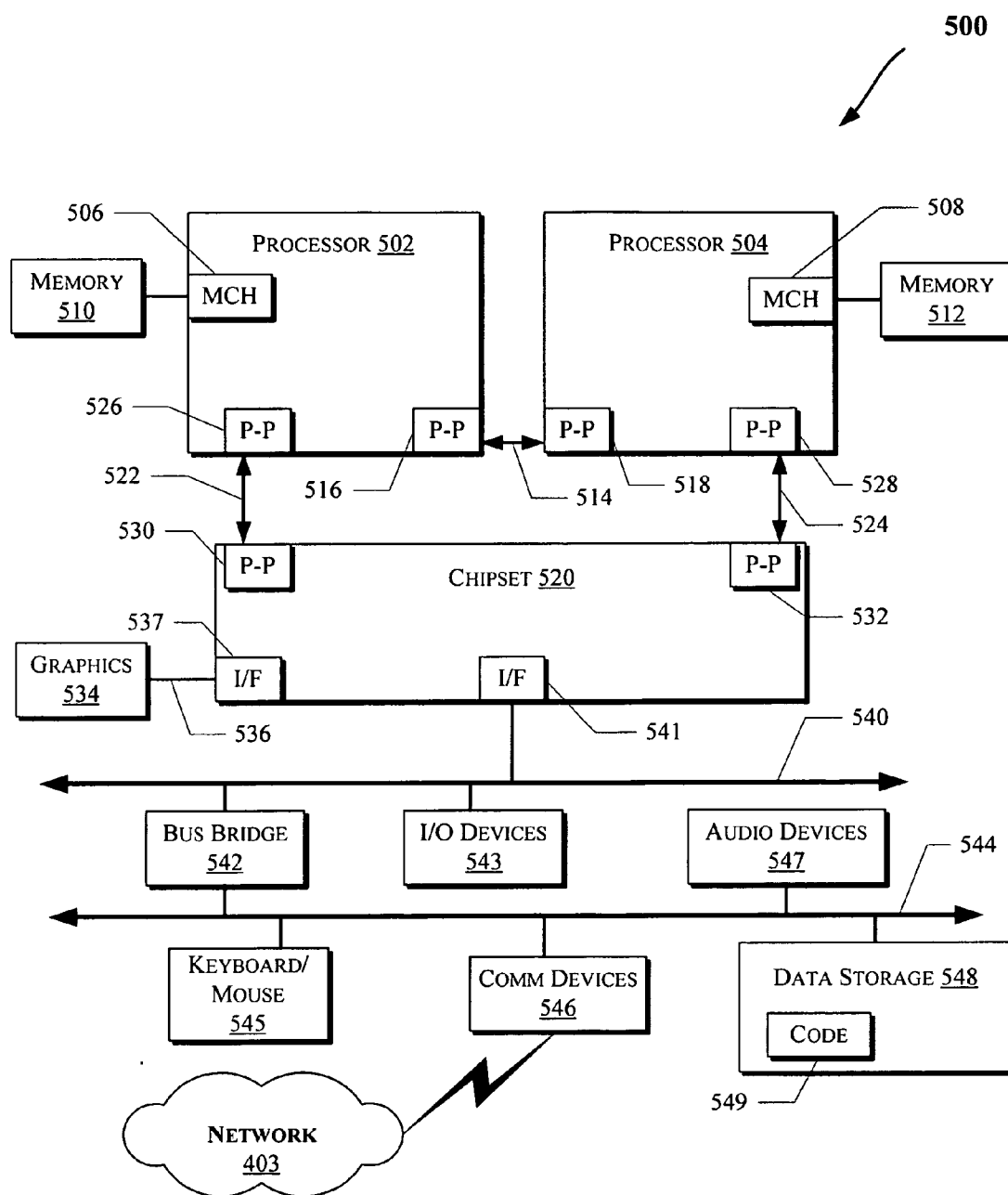


FIG. 5

OPERATING INTEGRATED CIRCUIT LOGIC BLOCKS AT INDEPENDENT VOLTAGES WITH SINGLE VOLTAGE SUPPLY

BACKGROUND

[0001] The present disclosure generally relates to the field of electronics. More particularly, an embodiment of the invention relates to operating integrated circuit (IC) logic blocks at independent voltages with a single source of voltage supply.

[0002] When providing power to IC dies, multiple power rails may be used to supply power to various components present on the die. To do this, some predefined amount of power resources may be allocated to each of the component. For example, some existing processors may operate all logic blocks present on the processor die at the same voltage and frequency. Alternatively, independent voltage supplies may be provided for each independent logic block. However, partitioning the supply of power in advance does not allow for dynamic power allocation. Also, the cost of providing these independent voltage supplies may be often prohibitive.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] The detailed description is provided with reference to the accompanying figures. In the figures, the left-most digit(s) of a reference number identifies the figure in which the reference number first appears. The use of the same reference numbers in different figures indicates similar or identical items.

[0004] FIGS. 1 and 2 illustrate block diagrams of domains and other logic that may be present on IC dies, according to various embodiments.

[0005] FIG. 3 illustrates a flow diagram of a method, according to an embodiment.

[0006] FIGS. 4 and 5 illustrate block diagrams of computing systems in accordance with various embodiments of the invention.

DETAILED DESCRIPTION

[0007] In the following description, numerous specific details are set forth in order to provide a thorough understanding of various embodiments. However, various embodiments of the invention may be practiced without the specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail so as not to obscure the particular embodiments of the invention. Further, various aspects of embodiments of the invention may be performed using various means, such as integrated semiconductor circuits ("hardware"), computer-readable instructions organized into one or more programs ("software"), or some combination of hardware and software. For the purposes of this disclosure reference to "logic" shall mean either hardware, software, or some combination thereof.

[0008] Some of the embodiments discussed herein may provide techniques for adjusting supply of power to one or more domains in an IC based on a determination (or indication) that power consumption by components of the corresponding domain is to be modified. In one embodiment, each IC die may include a plurality of domains. The power consumed by one or more components present in each domain may be individually adjusted. Also, a single power supply

(that may be external to the die) may supply power to power regulators that adjust the power consumption of the components within each domain.

[0009] Additionally, some embodiments may be provided in various environments, such as those discussed with reference to FIGS. 1-5. For example, FIG. 1 illustrates a block diagram of domains and other logic that may be present on an IC die 100, according to an embodiment. The die 100 may include one or more domains 102-1 through 102-M. Each of the domains 102-1 through 102-M may include various components, but for clarity, sample components are only shown with reference to the domain 102-1.

[0010] As illustrated in FIG. 1, each domain may include one or more sensors 104, a power management logic 105, a power regulator 106, and one or more logic blocks 108. The sensors 104 may sense variations (such as magnitude of semiconductor manufacturing process (P), operating voltage (V), temperature (T), and input vectors or values (I) variations (PVTI)) within the corresponding domain. In one embodiment, the sensors 104 may be coupled to one or more components of the corresponding domain (e.g., one or more of the logic blocks 108 within the domain 102-1). The power management logic 105 may be coupled to the sensors 104 and utilize sensed variations to cause adjustment(s) to the target operating frequency of one or more of the logic blocks 108. The power regulator 106 may adjust the supply of power provided by a power supply 110 (which may be external to the IC die 100 in one embodiment) to one or more components of the corresponding domain such as one or more of the logic blocks 108. In an embodiment, the power regulator 106 may include a power gating transistor (such as a power metal-oxide semiconductor field-effect transistor (MOSFET)), which may be utilized as a linear regulator by modulating its gate impedance. The power regulator 106 may also include inductors, capacitors, etc.

[0011] In one embodiment, the power management logic 105 (instead of or in conjunction with the detected values provided by the sensors 104) may determine whether the power consumption by one or more components of each of the plurality of domains 102 is to be modified based on one or more of an efficiency demand and/or a performance demand. Efficiency and/or performance demands may be configured by various techniques, such as predefined threshold values, analysis of input vectors or values, etc.

[0012] In an embodiment, the logic 105 may generate and transmit a signal to the power regulator 106 that corresponds to the target operating frequency of one or more components of the domain 102-1, such as the logic blocks 108. In some embodiments, the signal may be an indication to change the frequency to meet a desired power consumption target. In various embodiments, the transmitted signal may indicate a delta frequency change or it may be an indication to increase or decrease the frequency of the component. In one embodiment, the power regulator 106 may adjust the voltage supplied to the one or more components in response to the transmitted signal. In an embodiment, adjusting the supplied voltage may be made in conjunction with an operating frequency change, for example, where the level of both the supplied voltage and the operating frequency of one or more components are reduced. In some embodiments, the components (such as the logic blocks 108) may include one or more of: a processor core, a memory (such as a private or shared cache or a main or system memory), a digital signal processor engine, a co-processor, a vector processing engine, a floating

point processor, a memory controller, an input/output controller, a graphics controller, a network processor, a router (e.g., which may be used to communicate between various components of the die 100 and/or between components of the die 100 and other dies (not shown)), and/or a graphics processor. Also, the die 100 may be provided in any suitable computing device such as a personal digital assistant (PDA), a mobile phone, a laptop computer, a desktop computer, a server computer (including a server utilizing blade modules, also referred to herein as “blade server”), a workstation, etc. Furthermore, the die 100 may be provided in one or more components of the systems 400 of FIG. 4 and/or 500 of FIG. 5 in various embodiments.

[0013] FIG. 2 illustrates a block diagram of domains present on an IC die 200, according to an embodiment. In an embodiment, domains 202-1 through 202-M (collectively referred to herein as “domains 202”) may be similar to or the same as domains 102-1 through 102-M of FIG. 1. A power management unit 204 may be coupled to domains 202 and may adjust power consumption by components present in the domains 202 (such as the logic blocks 108 discussed with reference to FIG. 1).

[0014] Furthermore, domains 202-1 through 202-M may include more or less components than the domains 102-1 through 102-M of FIG. 1. For example, one or more of the domains 202 may include the sensors 104 and/or logic blocks 108. In an embodiment, the power management unit 204 may include a power regulator (such as the power regulator 106 discussed with reference to FIG. 1) for each of the domains 202. Alternatively, a power regulator (such as the power regulator 106 discussed with reference to FIG. 1) may be included in each of the domains 202. Also, the power supplied by the power supply 110 may be routed directly to the domains 202 (not shown) and the power management unit 204 may generate and transmit a signal to the power regulators within each domain 202 to adjust the power consumption of various components of the domains 202. Hence, in an embodiment, the power management unit 204 may perform the operations discussed herein with reference to the power management logic 105 for all domains of the IC die 200. This embodiment may allow for power management decisions to be made while considering the state and goal for all components of the die 200 rather than individual domains such as the embodiment discussed with reference to FIG. 1. Alternatively, the power management unit 204 may solely consider individual domain state and goals for components within each domain and cause the corresponding power regulator (which may be provided within the unit 204 and/or domains 202) to adjust the power consumption by various components in the domains 202.

[0015] FIG. 3 illustrates a flow diagram of a method 300 to adjust power consumption in a domain, according to an embodiment. In one embodiment, various components discussed with reference to FIGS. 1-2, 4, and 5 may be utilized to perform one or more of the operations discussed with reference to FIG. 3. For example, the method 300 may be used to adjust power consumption of the logic blocks 108 discussed with reference to FIG. 1.

[0016] Referring to FIGS. 1-3, at an operation 302, it is determined whether to adjust the power consumption of one or more components present in a domain of an IC die. For example, the power management logic 105, power regulator 106, and/or the power management unit 204 may be utilized at operation 302 to adjust the power consumption of logic blocks 108 such as discussed with reference to FIGS. 1 and 2.

At an operation 304, if power consumption is not to be adjusted, the method 300 returns to operation 302. Otherwise, if power consumption is to be adjusted, at an operation 306, a signal may be generated to cause the power adjustment. For example, the logic 105 and/or the power management unit 204 may generate a signal to indicate to the power regulator 106 (which may be provided within the unit 204 and/or domains 102 or 202) that power consumption of a corresponding component is to be adjusted. As discussed with reference to FIGS. 1 and 2, the generated signal may correspond to the target operating frequency of the component in one embodiment. At an operation 308, the power consumption may be adjusted in the corresponding domain. For example, the power regulator 106 may adjust the power consumption of the logic blocks 108 in accordance with a signal generated by the logic 105 and/or 204. In one embodiment, the power regulator 106 may adjust the voltage supplied to the component in response to the generated signal.

[0017] FIG. 4 illustrates a block diagram of a computing system 400 in accordance with an embodiment of the invention. The computing system 400 may include one or more central processing unit(s) (CPUs) 402 or processors that communicate via an interconnection network (or bus) 404. The processors 402 may include a general purpose processor, a network processor (that processes data communicated over a computer network 403), or other types of a processor (including a reduced instruction set computer (RISC) processor or a complex instruction set computer (CISC)). Moreover, the processors 402 may have a single or multiple core design. The processors 402 with a multiple core design may integrate different types of processor cores on the same IC die (such as dies 100 and 200 of FIGS. 1 and 2). Also, the processors 402 with a multiple core design may be implemented as symmetrical or asymmetrical multiprocessors. In an embodiment, one or more of the processors 402 may be provided on the dies 100 and/or 200 of FIGS. 1 and 2. Also, the operations discussed with reference to FIGS. 1-3 may be performed by one or more components of the system 400.

[0018] A chipset 406 may also communicate with the interconnection network 404. The chipset 406 may include a memory control hub (MCH) 408. The MCH 408 may include a memory controller 410 that communicates with a memory 412. The memory 412 may store data, including sequences of instructions, that are executed by the CPU 402, or any other device included in the computing system 400. In one embodiment of the invention, the memory 412 may include one or more volatile storage (or memory) devices such as random access memory (RAM), dynamic RAM (DRAM), synchronous DRAM (SDRAM), static RAM (SRAM), or other types of storage devices. Nonvolatile memory may also be utilized such as a hard disk. Additional devices may communicate via the interconnection network 404, such as multiple CPUs and/or multiple system memories.

[0019] The MCH 408 may also include a graphics interface 414 that communicates with a display device 416. In one embodiment of the invention, the graphics interface 414 may communicate with the display device 416 via an accelerated graphics port (AGP). In an embodiment of the invention, the display 416 (such as a flat panel display) may communicate with the graphics interface 414 through, for example, a signal converter that translates a digital representation of an image stored in a storage device such as video memory or system memory into display signals that are interpreted and displayed by the display 416. The display signals produced by

the display device may pass through various control devices before being interpreted by and subsequently displayed on the display 416.

[0020] A hub interface 418 may allow the MCH 408 and an input/output control hub (ICH) 420 to communicate. The ICH 420 may provide an interface to I/O device(s) that communicate with the computing system 400. The ICH 420 may communicate with a bus 422 through a peripheral bridge (or controller) 424, such as a peripheral component interconnect (PCI) bridge, a universal serial bus (USB) controller, or other types of peripheral bridges or controllers. The bridge 424 may provide a data path between the CPU 402 and peripheral devices. Other types of topologies may be utilized. Also, multiple buses may communicate with the ICH 420, e.g., through multiple bridges or controllers. Moreover, other peripherals in communication with the ICH 420 may include, in various embodiments of the invention, integrated drive electronics (IDE) or small computer system interface (SCSI) hard drive(s), USB port(s), a keyboard, a mouse, parallel port(s), serial port(s), floppy disk drive(s), digital output support (e.g., digital video interface (DVI)), or other devices.

[0021] The bus 422 may communicate with an audio device 426, one or more disk drive(s) 428, and a network interface device 430 (which is in communication with the computer network 403). Other devices may communicate via the bus 422. Also, various components (such as the network interface device 430) may communicate with the MCH 408 via a high speed (e.g., general purpose) I/O bus channel in some embodiments of the invention. In addition, the processor 402 and the MCH 408 may be combined to form a single chip. Furthermore, a graphics accelerator may be included within the MCH 408 in other embodiments of the invention.

[0022] Furthermore, the computing system 400 may include volatile and/or nonvolatile memory (or storage). For example, nonvolatile memory may include one or more of the following: read-only memory (ROM), programmable ROM (PROM), erasable PROM (EPROM), electrically EPROM (EEPROM), a disk drive (e.g., 428), a floppy disk, a compact disk ROM (CD-ROM), a digital versatile disk (DVD), flash memory, a magneto-optical disk, or other types of nonvolatile machine-readable media that are capable of storing electronic data (e.g., including instructions).

[0023] FIG. 5 illustrates a computing system 500 that is arranged in a point-to-point (PtP) configuration, according to an embodiment of the invention. In particular, FIG. 5 shows a system where processors, memory, and input/output devices are interconnected by a number of point-to-point interfaces. The operations discussed with reference to FIGS. 1-4 may be performed by one or more components of the system 500.

[0024] As illustrated in FIG. 5, the system 500 may include several processors, of which only two, processors 502 and 504 are shown for clarity. The processors 502 and 504 may each include a local memory controller (MC) 506 and 508 to enable communication with memories 510 and 512. The memories 510 and/or 512 may store various data such as those discussed with reference to the memory 412 of FIG. 4.

[0025] In an embodiment, the processors 502 and 504 may be one of the processors 402 discussed with reference to FIG. 4. The processors 502 and 504 may exchange data via a point-to-point (PtP) interface 514 using PtP interface circuits 516 and 518, respectively. Further, the processors 502 and 504 may include a high speed (e.g., general purpose) I/O bus channel in some embodiments of the invention to facilitate communication with various components (such as I/O device

(s)). Also, the processors 502 and 504 may each exchange data with a chipset 520 via individual PtP interfaces 522 and 524 using point-to-point interface circuits 526, 528, 530, and 532. The chipset 520 may further exchange data with a graphics circuit 534 via a graphics interface 536, e.g., using a PtP interface circuit 537.

[0026] At least one embodiment of the invention may be provided within the processors 502 and 504. For example, one or more of the components discussed with reference to FIGS. 1-2 may be provided on the dies 100 and 200, respectively, in conjunction with the processors 502 and/or 504. Other embodiments of the invention, however, may exist in other circuits, logic units, or devices within the system 500 of FIG. 5. Furthermore, other embodiments of the invention may be distributed throughout several circuits, logic units, or devices illustrated in FIG. 5.

[0027] The chipset 520 may communicate with a bus 540 using a PtP interface circuit 541. The bus 540 may communicate with one or more devices, such as a bus bridge 542 and I/O devices 543. Via a bus 544, the bus bridge 542 may communicate with other devices such as a keyboard/mouse 545, communication devices 546 (such as modems, network interface devices, or other communication devices that may communicate with the computer network 403), audio I/O device 547, and/or a data storage device 548. The data storage device 548 may store code 549 that may be executed by the processors 502 and/or 504.

[0028] In various embodiments of the invention, the operations discussed herein, e.g., with reference to FIGS. 1-5, may be implemented as hardware (e.g., logic circuitry), software, firmware, or combinations thereof, which may be provided as a computer program product, e.g., including a machine-readable or computer-readable medium having stored thereon instructions (or software procedures) used to program a computer to perform a process discussed herein. The machine-readable medium may include a storage device such as those discussed with respect to FIGS. 1-5.

[0029] Additionally, such computer-readable media may be downloaded as a computer program product, wherein the program may be transferred from a remote computer (e.g., a server) to a requesting computer (e.g., a client) by way of data signals embodied in a carrier wave or other propagation medium via a communication link (e.g., a bus, a modem, or a network connection). Accordingly, herein, a carrier wave shall be regarded as comprising a machine-readable medium.

[0030] Reference in the specification to "one embodiment," "an embodiment," or "some embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiment(s) may be included in at least an implementation. The appearances of the phrase "in one embodiment" in various places in the specification may or may not be all referring to the same embodiment.

[0031] Also, in the description and claims, the terms "coupled" and "connected," along with their derivatives, may be used. In some embodiments of the invention, "connected" may be used to indicate that two or more elements are in direct physical or electrical contact with each other. "Coupled" may mean that two or more elements are in direct physical or electrical contact. However, "coupled" may also mean that two or more elements may not be in direct contact with each other, but may still cooperate or interact with each other.

[0032] Thus, although embodiments of the invention have been described in language specific to structural features and/or methodological acts, it is to be understood that claimed

subject matter may not be limited to the specific features or acts described. Rather, the specific features and acts are disclosed as sample forms of implementing the claimed subject matter.

What is claimed is:

1. An integrated circuit die comprising:
a plurality of domains; and
a plurality of power regulators, each of the plurality of power regulators to:
receive a supply of power from a power supply that is external to the integrated circuit die; and
adjust a supply of power to one or more components of a corresponding one of the plurality of domains based on an indication that a power consumption by the one or more components of the corresponding domain is to be modified.
2. The integrated circuit die of claim 1, wherein each of the plurality of domains comprise a first logic to determine whether the power consumption by the one or more components of the corresponding domain is to be modified.
3. The integrated circuit die of claim 2, wherein the first logic is to determine whether the power consumption by the one or more components of the corresponding domain is to be modified in response to detection of one or more variations in the corresponding domain.
4. The integrated circuit die of claim 3, further comprising one or more sensors to detect the one or more variations in the corresponding domain.
5. The integrated circuit die of claim 1, further comprising a first logic to determine whether the power consumption by one or more components of each of the plurality of domains is to be modified.
6. The integrated circuit die of claim 5, wherein the first logic comprises the plurality of power regulators.
7. The integrated circuit die of claim 5, wherein each of the plurality of domains comprises one of the plurality of power regulators and wherein the first logic transmits a signal to at least one of the plurality of power regulators to indicate that the power consumption by the one or more components is to be modified.
8. The integrated circuit die of claim 5, wherein the first logic causes transmission of a signal to at least one of the plurality of power regulators to indicate a change to a target operating frequency of the one or more components to meet a power consumption target.
9. The integrated circuit die of claim 7, wherein the at least one of the plurality of the power regulators adjusts a voltage supplied to the one or more components in response to the transmitted signal.
10. The integrated circuit die of claim 5, further comprising one or more sensors to detect one or more variations in the corresponding domain, wherein the first logic generates a signal to cause at least one of the plurality of power regulators to adjust the supply of power to the one or more components.
11. The integrated circuit die of claim 1, wherein each of the one or more components comprises one or more of: a processor core, a memory, a digital signal processor engine, a co-processor, a vector processing engine, a floating point processor, a memory controller, an input/output controller, a graphics controller, a network processor, or a graphics processor.
12. The integrated circuit die of claim 1, further comprising a first logic to determine whether the power consumption by

one or more components of each of the plurality of domains is to be modified based on one or more of an efficiency demand or a performance demand.

13. A method comprising:
determining whether a power consumption by one or more domains of a plurality of domains on an integrated circuit die is to be modified;
generating one or more signals to indicate that the power consumption of the one or more domains is to be modified; and
adjusting a supply of power from an external power supply to the one or more domains in response to the one or more generated signals.
14. The method of claim 13, wherein the one or more signals correspond to indications to modify target operating frequencies of the one or more domains.
15. The method of claim 13, wherein adjusting the supply of power comprises adjusting a voltage supplied to the one or more domains in response to the one or more signals.
16. The method of claim 13, further comprising detecting one or more variations in the one or more domains.
17. The method of claim 16, wherein generating the one or more signals is performed in response to the detection of the one or more variations.
18. The method of claim 16, wherein detecting the one or more variations comprises sensing a temperature variation.
19. The method of claim 13, wherein determining whether the power consumption by the one or more domains is to be modified is performed based on efficiency or performance demands.
20. A computing system comprising:
a power supply; and
one or more semiconductor dies coupled to the power supply, at least one of the one or more dies to comprise:
a first domain to comprise a first logic to perform one or more computing functions;
a second logic to determine whether a power consumption by the first logic is to be modified; and
a first power regulator to adjust a supply of power to the first logic in accordance with a first signal caused to be generated by the second logic.
21. The system of claim 20, wherein the at least one of the dies comprises a second domain to comprise a third logic and wherein the second logic is to determine whether a power consumption by the third logic is to be modified.
22. The system of claim 21, further comprising a second power regulator to adjust a supply of power to the third logic in accordance with a second signal caused to be generated by the second logic.
23. The system of claim 20, wherein the first logic comprises one or more of: a processor core, a memory, a digital signal processor engine, a co-processor, a vector processing engine, a floating point processor, a memory controller, an input/output controller, a graphics controller, a network processor, or a graphics processor.
24. The system of claim 20, wherein the second logic comprises the first power regulator.
25. The system of claim 20, further comprising one or more sensors to detect one or more variations in the first domain.
26. The system of claim 20, wherein the second logic is to determine whether the power consumption by the first logic is to be modified in response to a detection of one or more variations in the first domain.

27. The system of claim 20, wherein the second logic is to determine whether the power consumption by the first logic is to be modified based on one or more of an efficiency demand or a performance demand.

28. The system of claim 20, wherein the second logic comprises a plurality of power regulators.

29. The system of claim 20, wherein the first signal corresponds to an indication to change a target operating frequency of the first logic.

30. The system of claim 20, further comprising an audio device coupled to the at least one or more dies.

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