PTO/AIA/15 (10-17)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	4123.0110002
First Named Inventor	Zhenyu LU
Title	See 1 in Addendum
Priority Mail Express® Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☐ **Fee Transmittal Form** (PTO/SB/17 or equivalent)
2. ☐ **Applicant asserts small entity status.** See 37 CFR 1.27
3. ☐ **Applicant certifies micro entity status.** See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.
4. ☑ **Specification** [*Total Pages* 68] Both the claims and abstract must start on a new page. *(See MPEP § 608.01(a) for information on the preferred arrangement)*
5. ☑ **Drawing(s)** (35 U.S.C. 113) [*Total Sheets* 120]
6. **Inventor's Oath or Declaration** [*Total Pages* ____] *(including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))*
   a. ☐ Newly executed (original or copy)
   b. ☐ A copy from a prior application (37 CFR 1.63(d))
7. ☑ **Application Data Sheet** ** See note below.* See 37 CFR 1.76 (PTO/AIA/14 or equivalent)
8. **CD-ROM or CD-R** in duplicate, large table, or Computer Program (*Appendix*)
   ☐ Landscape Table on CD
9. **Nucleotide and/or Amino Acid Sequence Submission** (*if applicable, items a. – c. are required*)
   a. ☐ Computer Readable Form (CRF)
   b. ☐ Specification Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper
   c. ☐ Statements verifying identity of above copies

ADDRESS TO:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ACCOMPANYING APPLICATION PAPERS

10. ☐ **Assignment Papers** (cover sheet & document(s))
    Name of Assignee See 2 in Addendum
11. ☐ **37 CFR 3.73(c) Statement** (*when there is an assignee*) ☑ **Power of Attorney**
12. ☐ **English Translation Document** (*if applicable*)
13. ☐ **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    ☐ Copies of citations attached
14. ☐ **Preliminary Amendment**
15. ☐ **Return Receipt Postcard** (*MPEP § 503*) (*Should be specifically itemized*)
16. ☐ **Certified Copy of Priority Document(s)** (*if foreign priority is claimed*)
17. ☐ **Nonpublication Request** Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
18. ☑ **Other:** Authorization to Treat a Reply as Incorporating an Extension of Time

***Note:** (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS

☑ The address associated with Customer Number: 26111 **OR** ☐ Correspondence address below

Name					
Address					
City		State		Zip Code	
Country		Telephone		Email	

Signature	/Donald J. Featherstone/	Date	7/26/18
Name (Print/Type)	Donald J. Featherstone	Registration No. (Attorney/Agent)	33,876

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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9722569

Addendum

1. JOINT OPENNING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME

2. Yangtze Memory Technologies Co., Ltd.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
dionf@sternekessler.com

July 26, 2018

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: U.S. Non-Provisional Utility Patent Application under 37 C.F.R. § 1.53(b)
(Continuation of Appl. No. PCT/CN2018/077785; Filed: March 1, 2018)
Appl. No. *To Be Assigned*; Filed Date: *Herewith*
For: **JOINT OPENNING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME**
Inventors: LU *et al.*
Our Ref: 4123.0110002

Commissioner:

The following documents are transmitted herewith for appropriate action by the U.S. Patent and Trademark Office:

1. Utility Patent Application Transmittal Form (PTO/AIA/15);

2. Authorization to Treat a Reply As Incorporating An Extension of Time Under 37 C.F.R. § 1.136(a)(3);

3. U.S. Utility Patent Application entitled:

JOINT OPENNING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME

and naming as inventors:

Zhenyu LU
Wenguang SHI
Guanping WU
Feng PAN
Xianjin WAN
Baoyou CHEN

Micron Ex. 1002, p. 4
Micron v. YMTC
IPR2025-00244

the application consisting of:

a. An Application Data Sheet (37 C.F.R. § 1.76);

b. A specification containing:

i. 61 pages of description prior to the claims;

ii. 6 pages of claims (20 claims); and

iii. a 1 page abstract; and

c. 120 sheets of drawings (Figures 1-6, 7A, 7B, 8A, 8B, 9A, 9B, 10A, 10B, 11A 11B, 12-20, 21A, 21B, 22A, 22B, 23A, 23B, 24-29, 30A, 30B, 31A, 31B, 32A, 32B, 33A, 33B, 34A, 34B, 35-47, 48A, 48B, 49A, 49B, 50A, 50B, 51-55, 56A, 56B, 57A, 57B, 58A, 58B, 59A, 59B, 60-71, 72A, 72B, 73A-74B, 75-79, 80A, 80B, 81A, 81B, 82A, 82B, 83A, 83B, 84-100, 101A, 101B, 102A, 102B, 103A, and 103B); and

4. An executed Power of Attorney by Applicant (PTO/AIA/82B) and the Transmittal for Power of Attorney form (PTO/AIA/82A).

The above-listed documents are filed electronically through EFS-Web.

Correspondence should be sent to Customer Number 26111.

This patent application is being submitted under 37 C.F.R. § 1.53(b) without Declaration and without the required fees.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/W-S/:mlb
Enclosures

9714868_1.doc

Electronic Acknowledgement Receipt

EFS ID:	33297553
Application Number:	16046847
International Application Number:	
Confirmation Number:	7612
Title of Invention:	JOINT OPENNING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME
First Named Inventor/Applicant Name:	Zhenyu LU
Customer Number:	26111
Filer:	Donald J. Featherstone/Maya Bennett
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0110002
Receipt Date:	26-JUL-2018
Filing Date:	
Time Stamp:	19:22:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		41270110002application.pdf	7735883 ac6a4a0f11cad90ce57a9c938c669fddff8b631e	yes	206

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Power of Attorney	205	206
	Drawings-only black and white line drawings	85	204
	Abstract	84	84
	Claims	78	83
	Specification	17	77
	Application Data Sheet	7	16
	Authorization for Extension of Time all replies	6	6
	Transmittal of New Application	3	5
	Transmittal Letter	1	2
Warnings:			
Information:			
	Total Files Size (in bytes):	7735883	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
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TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	To Be Assigned
Filing Date	Herewith
First Named Inventor	Zhenyu LU
Title	JOINT OPENNING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME
Art Unit	To Be Assigned
Examiner Name	To Be Assigned
Attorney Docket Number	4123.0110002

SIGNATURE of Applicant or Patent Practitioner

Signature	/Donald J. Featherstone/	Date (Optional)	7/26/18
Name	Donald J. Featherstone	Registration Number	33,876
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 (one) forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 26111

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number: 26111

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Yangtze Memory Technologies Co., Ltd.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

✓ 1 **SIGNATURE of Applicant for Patent**

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	
Name	Simon Shi-Ning Yang		
Title	CEO		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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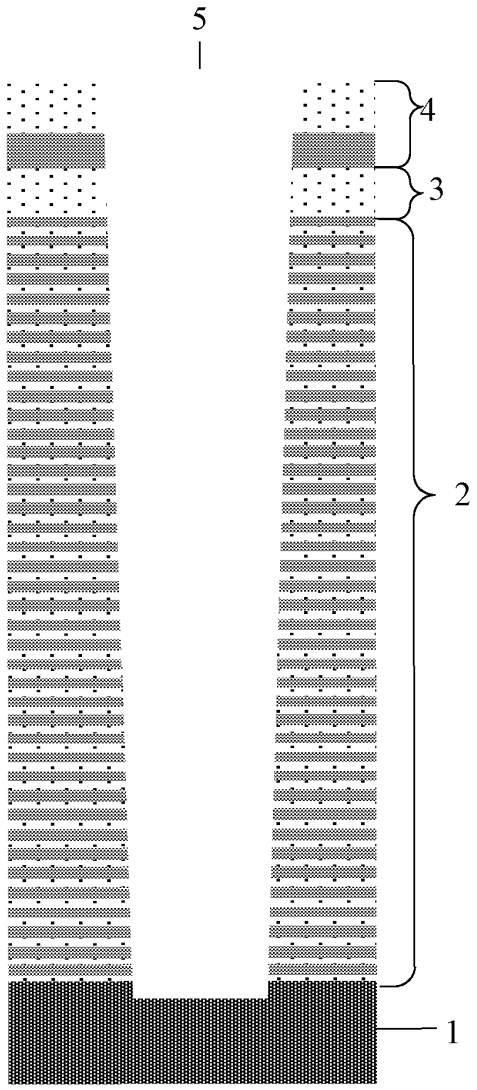


FIG. 1

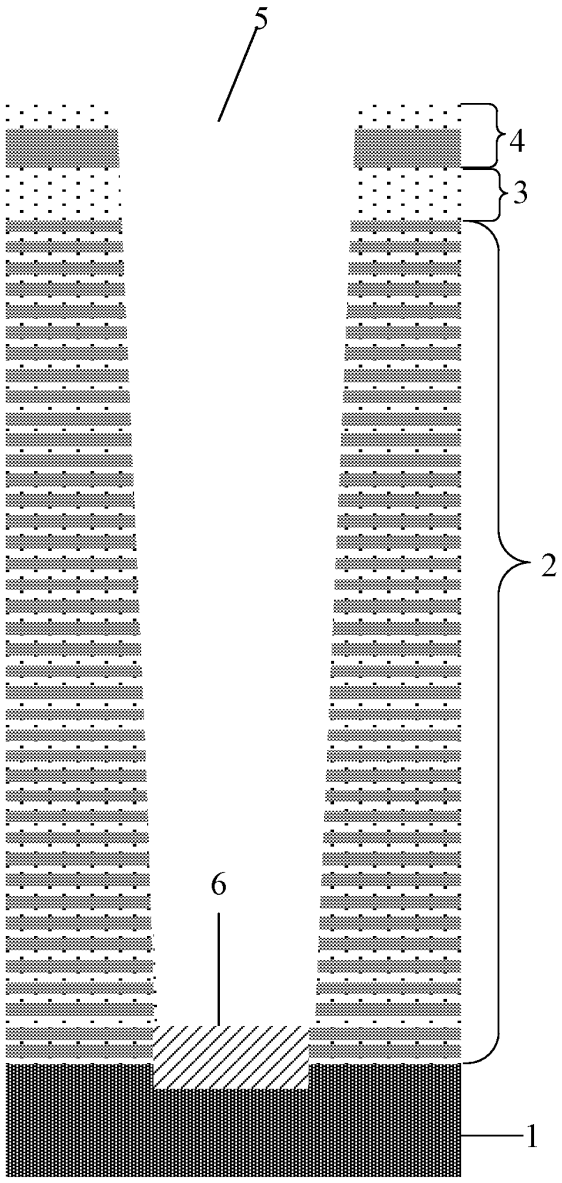


FIG. 2

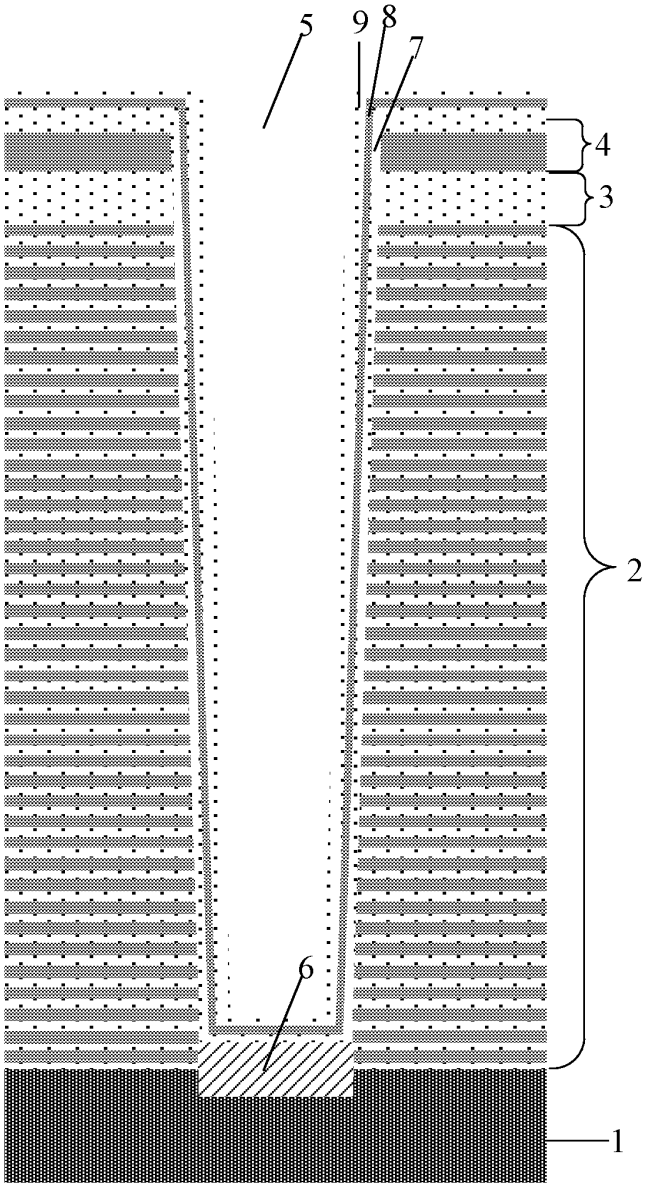


FIG. 3

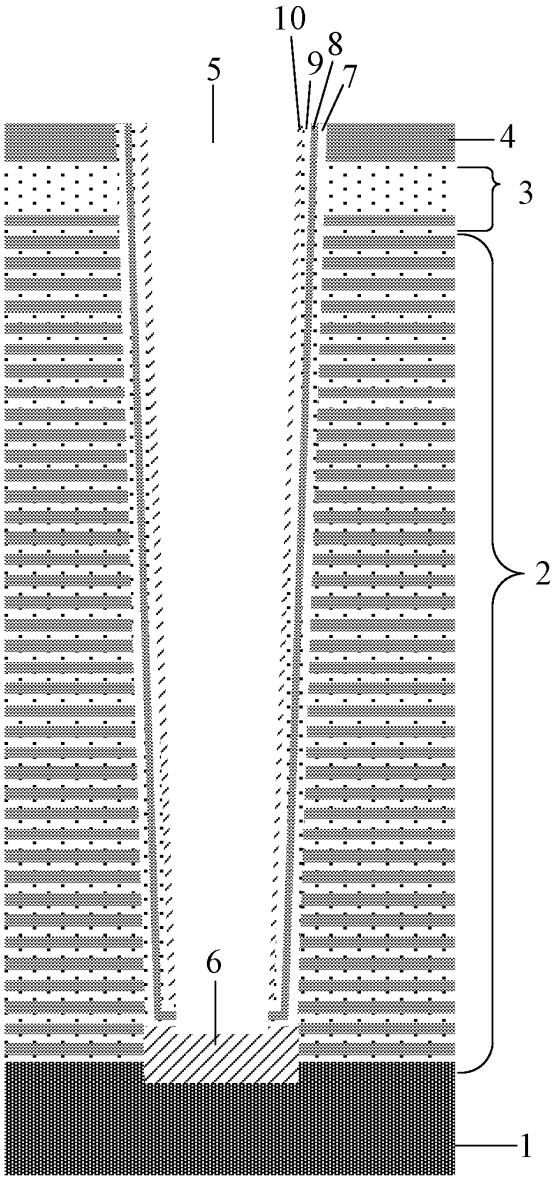


FIG. 4

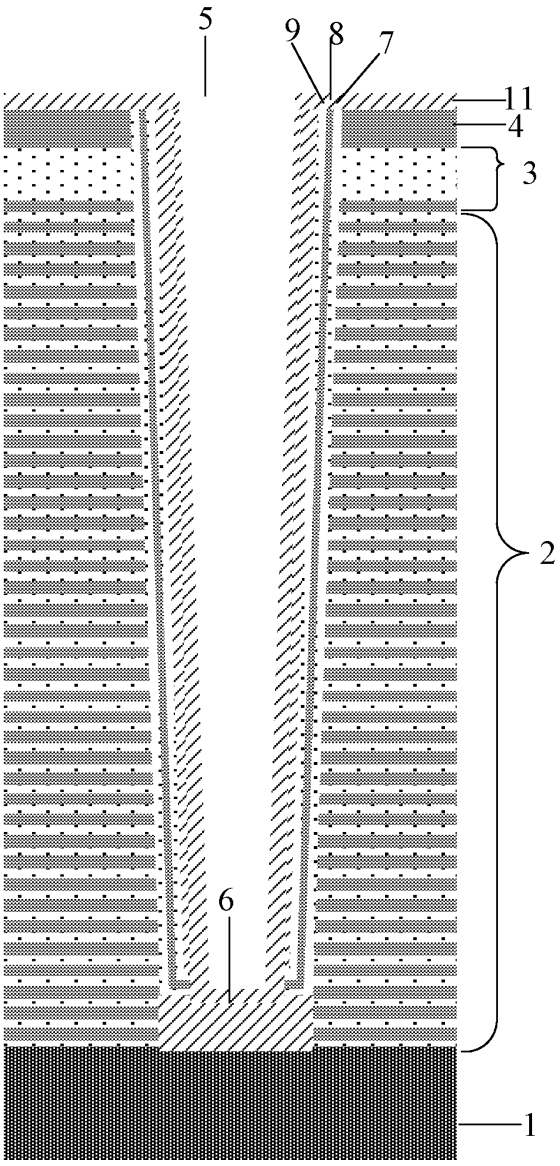


FIG. 5

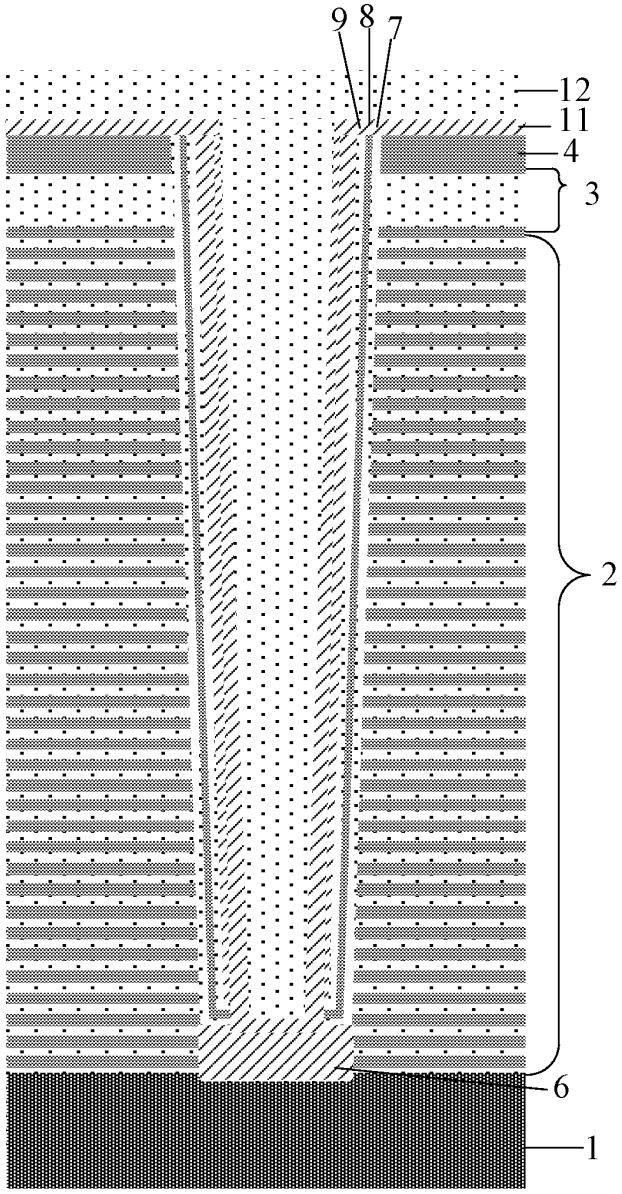


FIG. 6

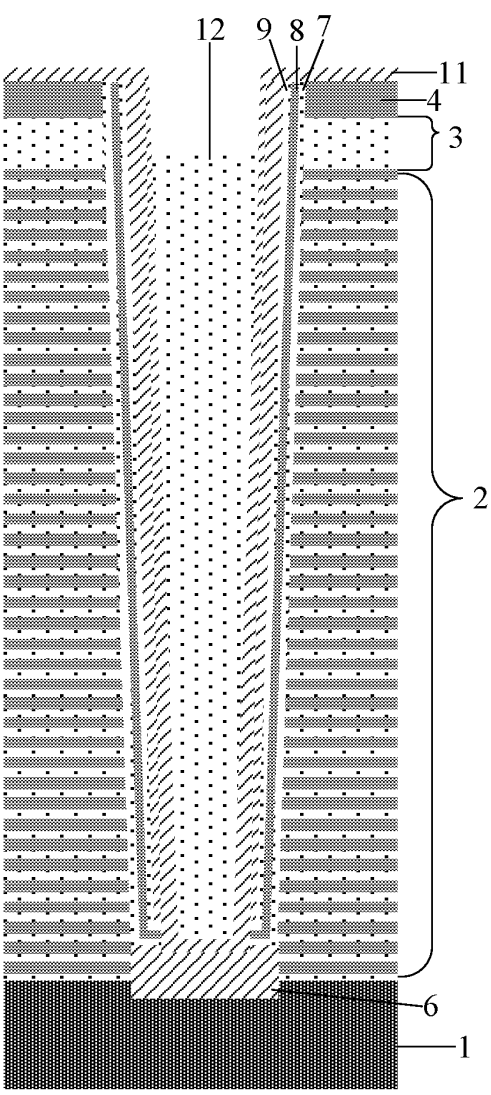


FIG. 7A

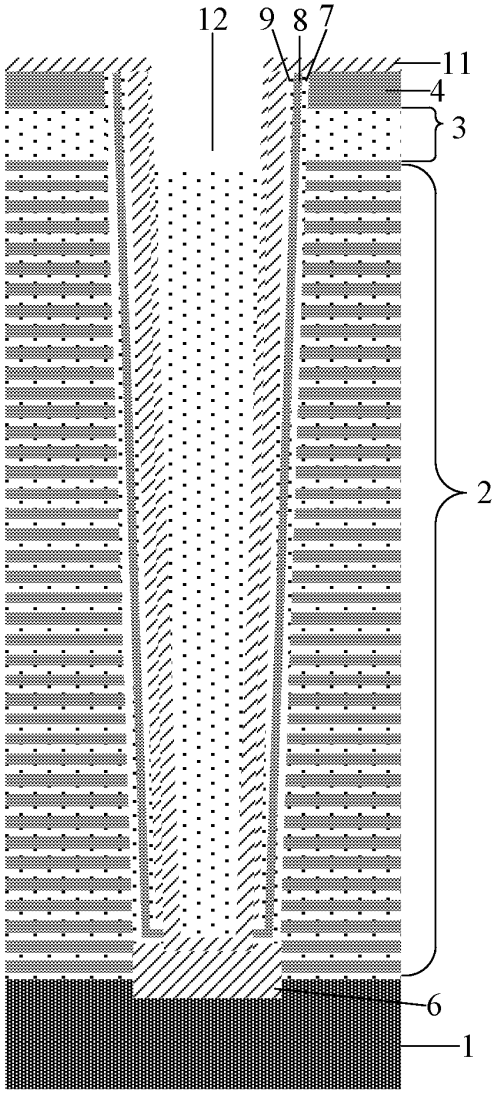


FIG. 7B

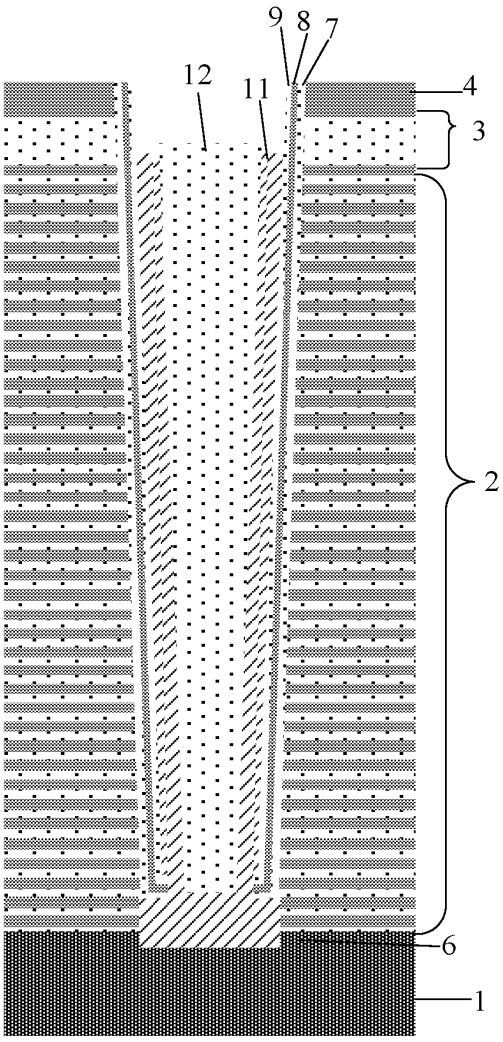


FIG. 8A

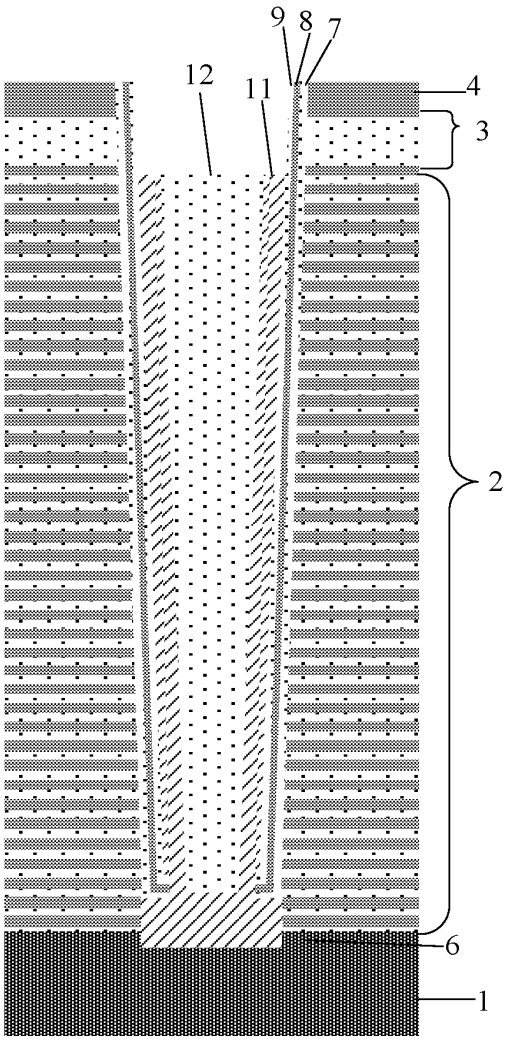


FIG. 8B

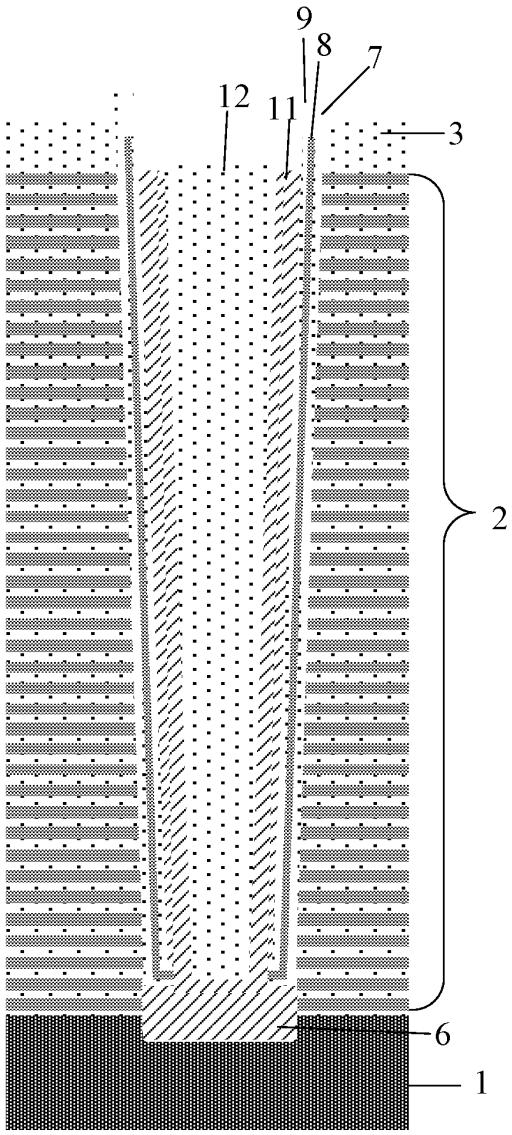


FIG. 9A

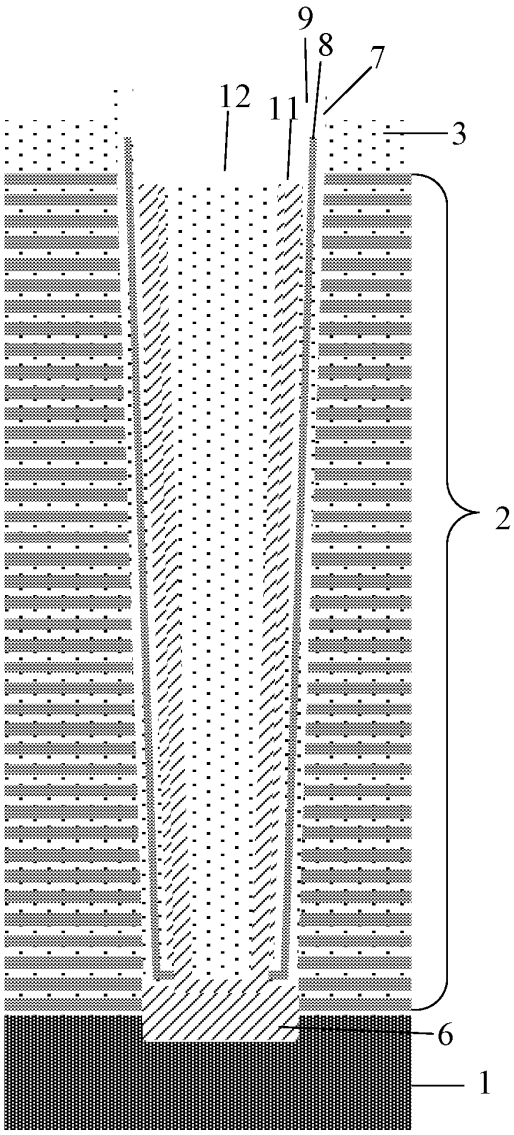


FIG. 9B

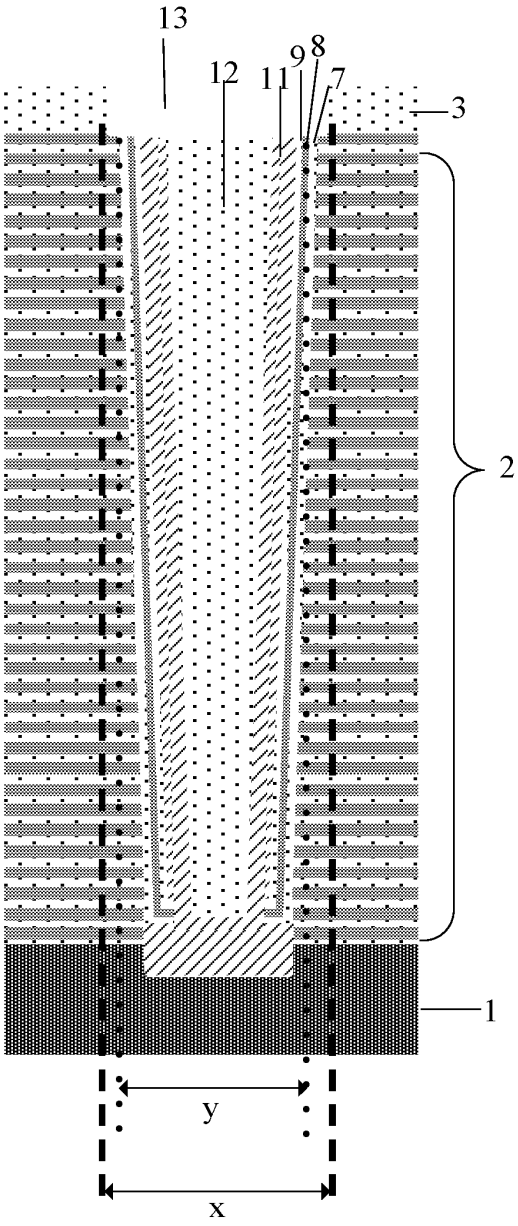


FIG. 10A

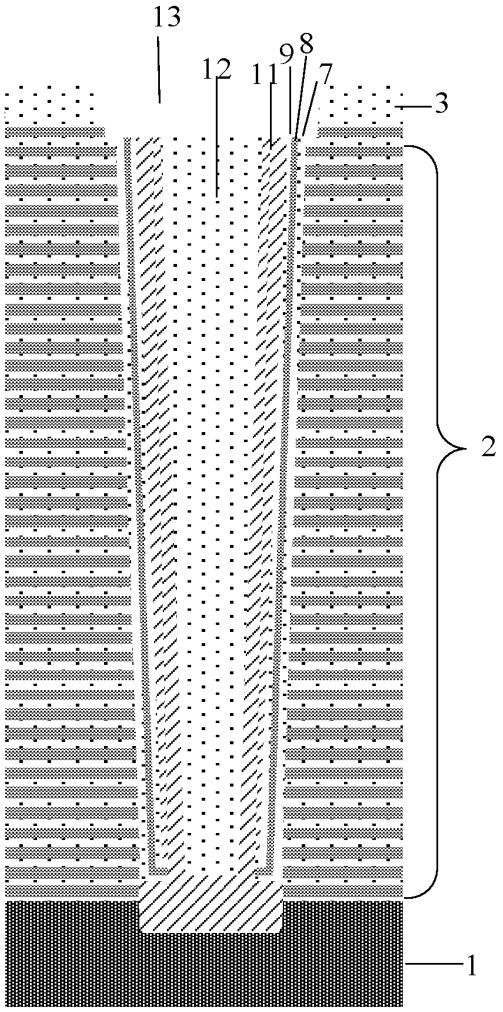


FIG. 10B

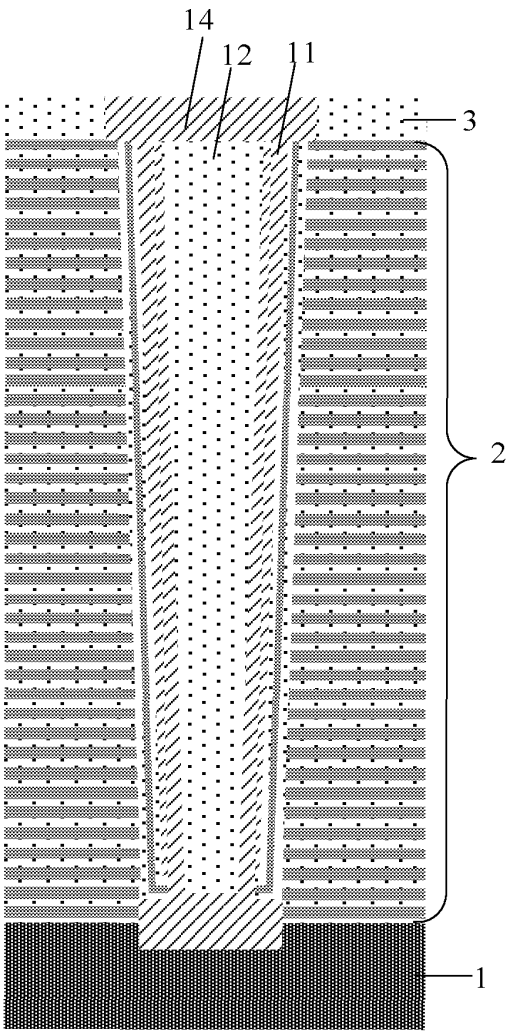


FIG. 11A

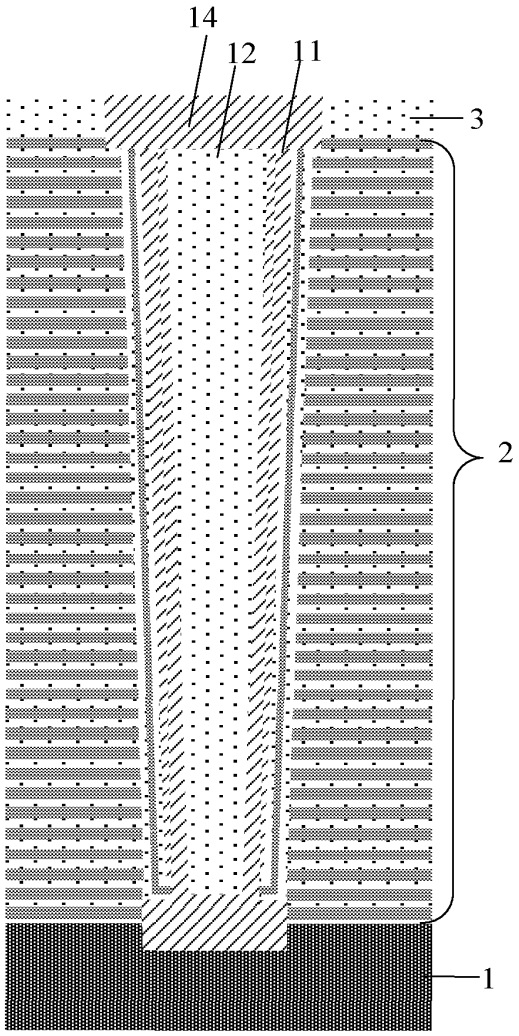


FIG. 11B

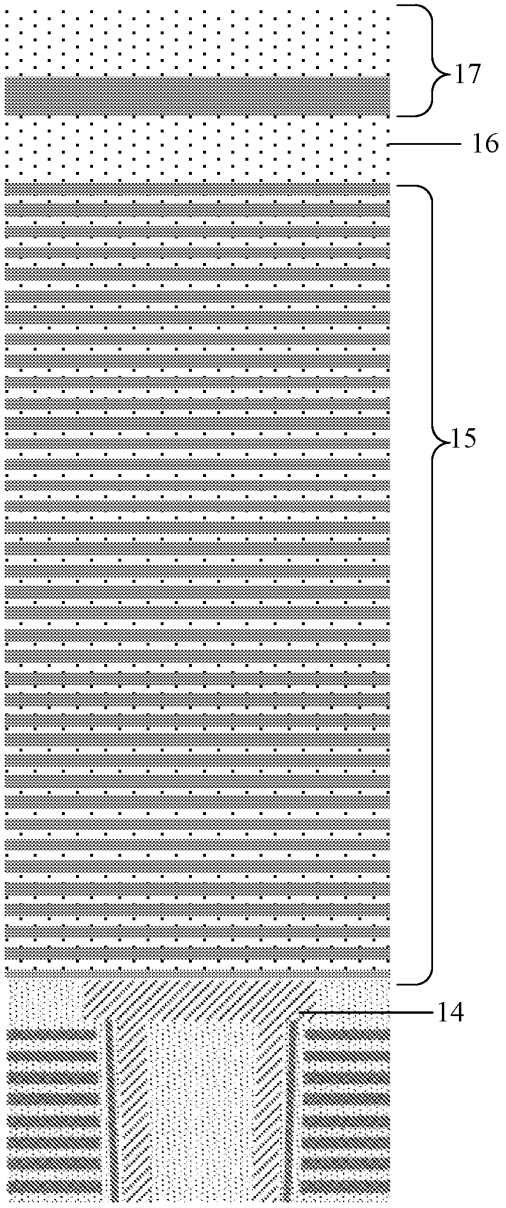


FIG. 12

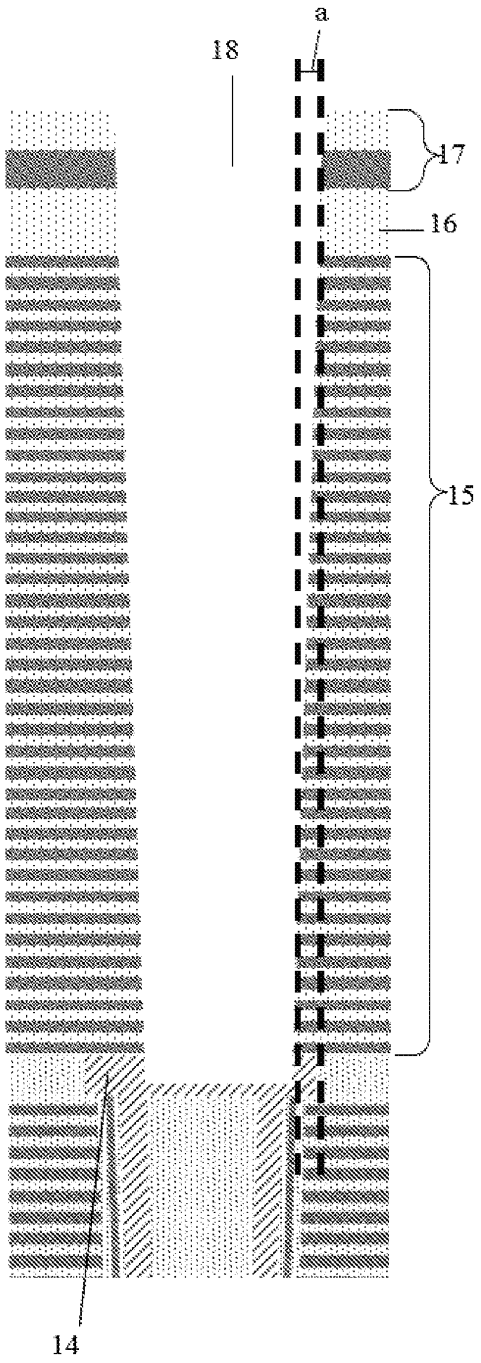


FIG. 13

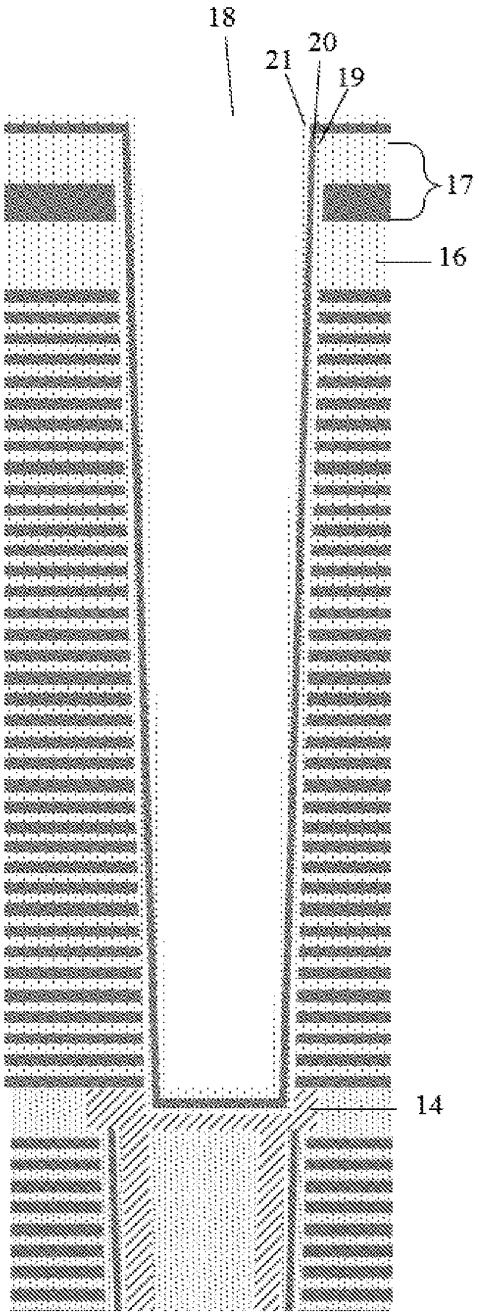


FIG. 14

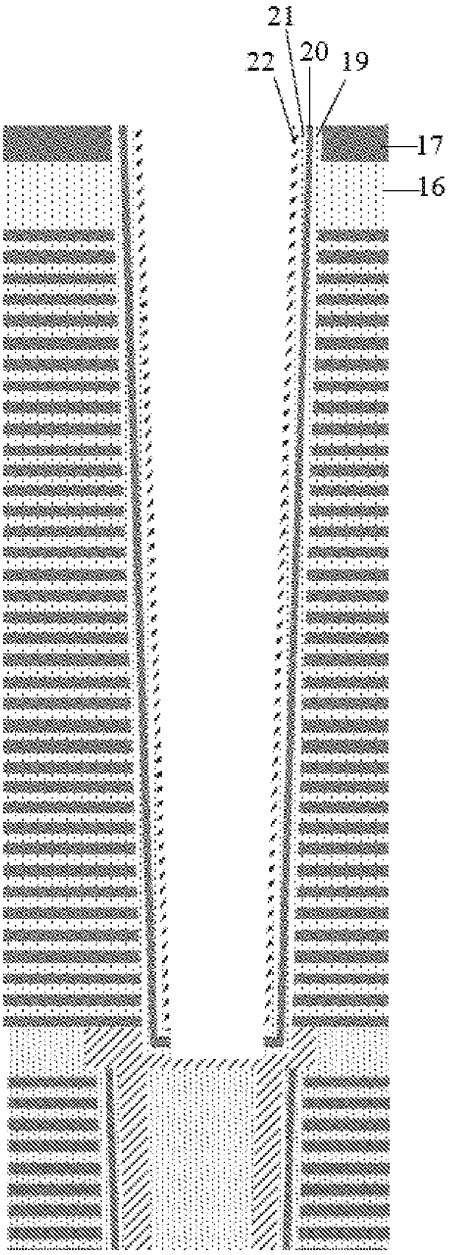


FIG. 15

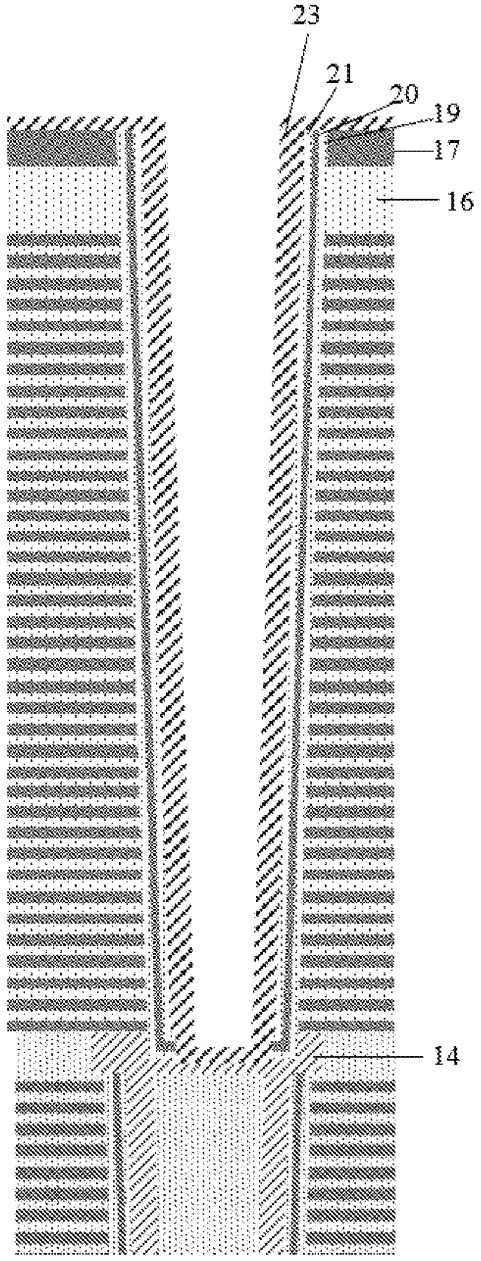


FIG. 16

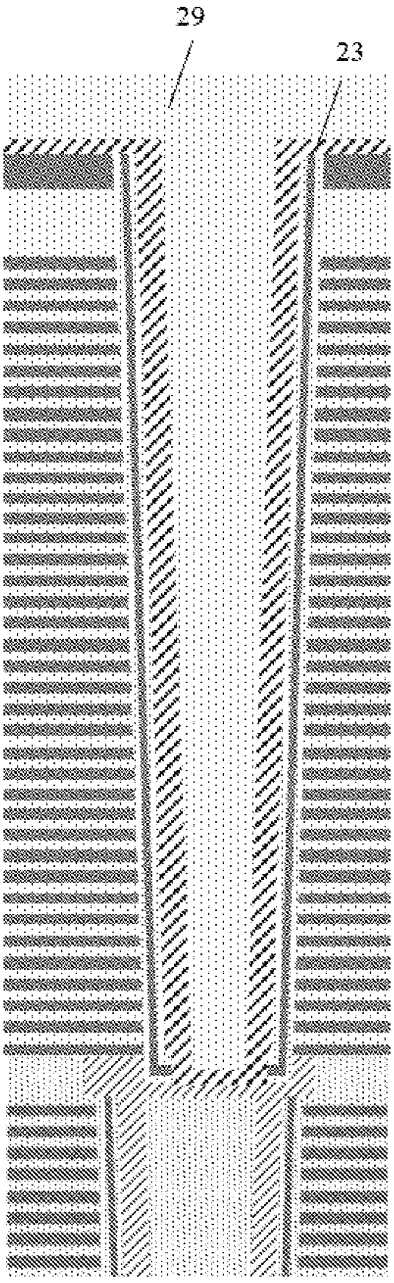


FIG. 17

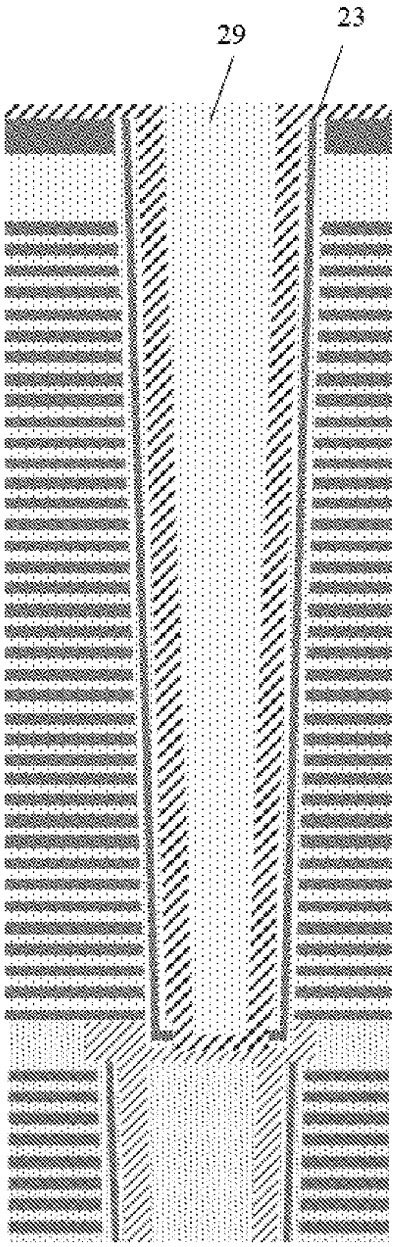


FIG. 18

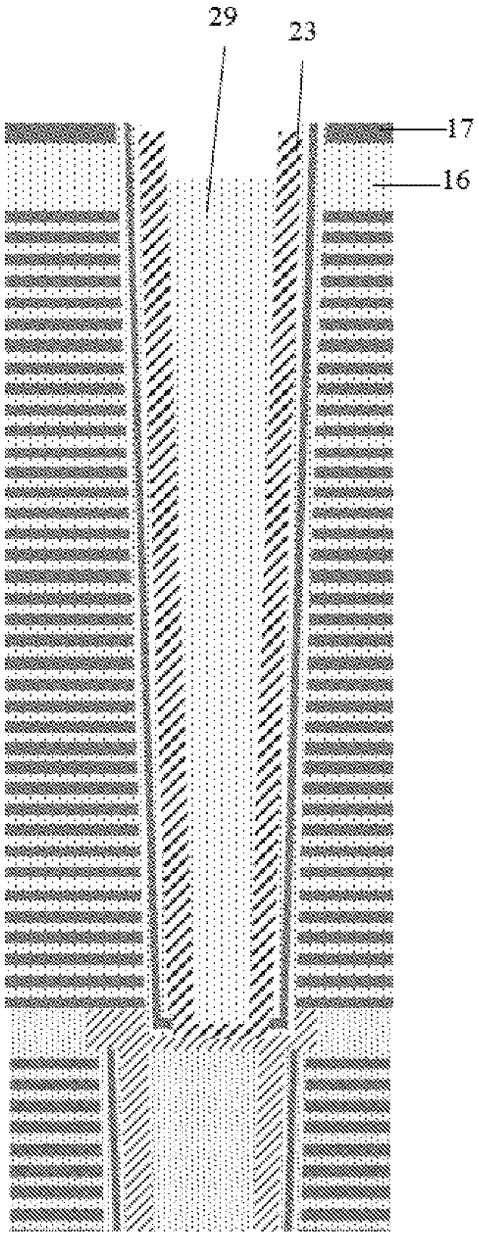


FIG. 19

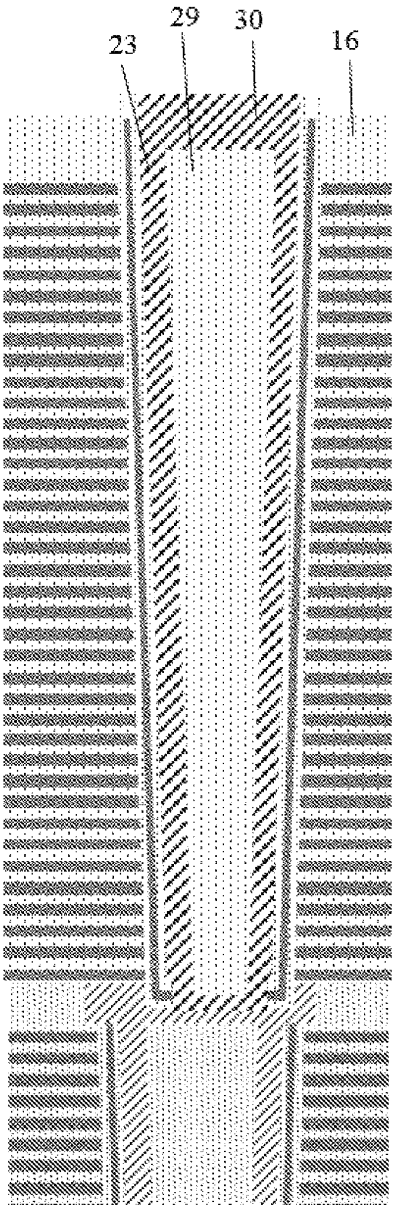


FIG. 20

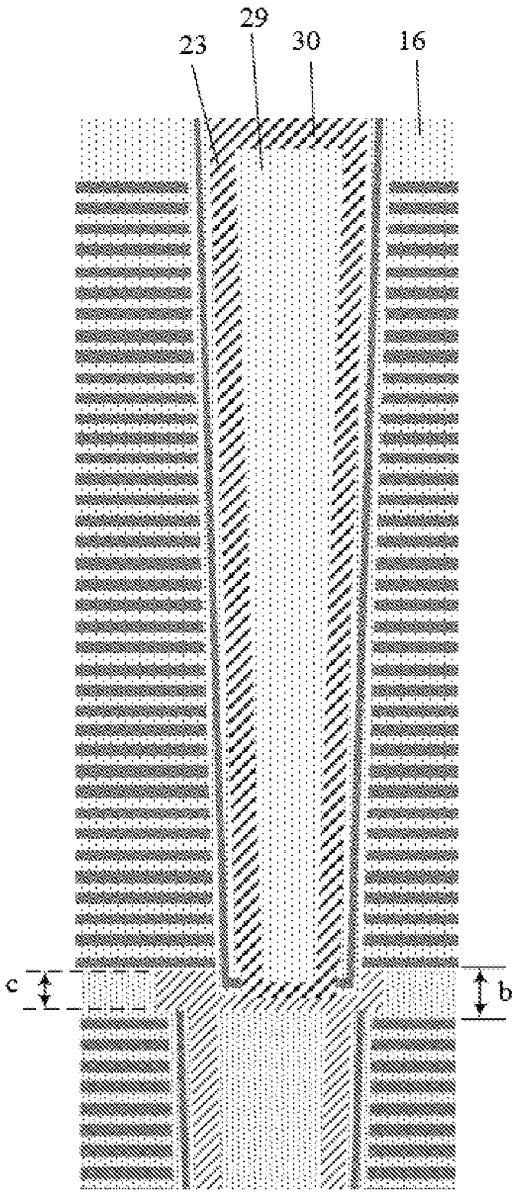


FIG. 21A

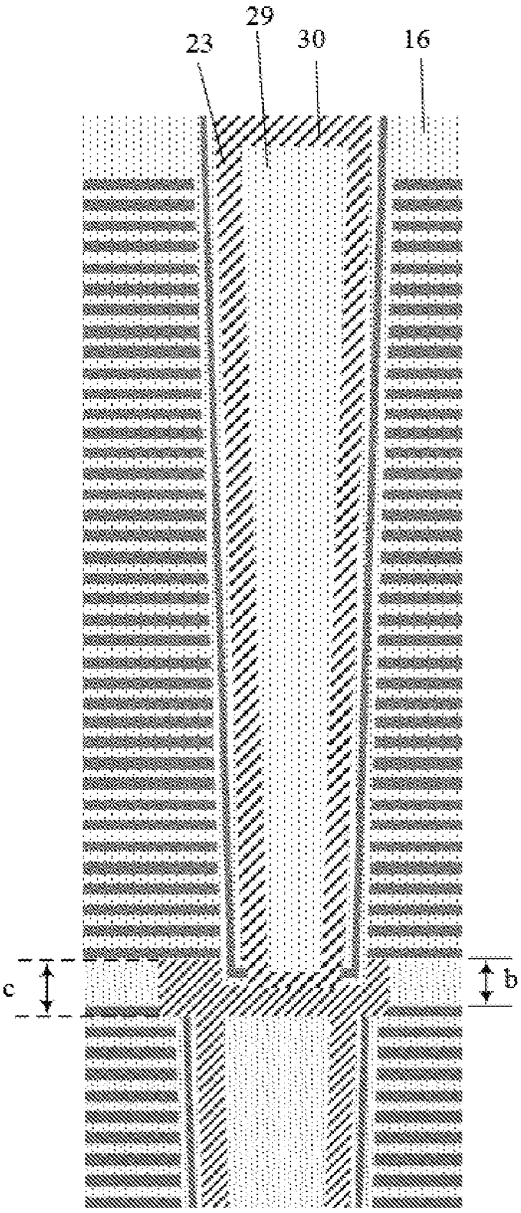


FIG. 21B

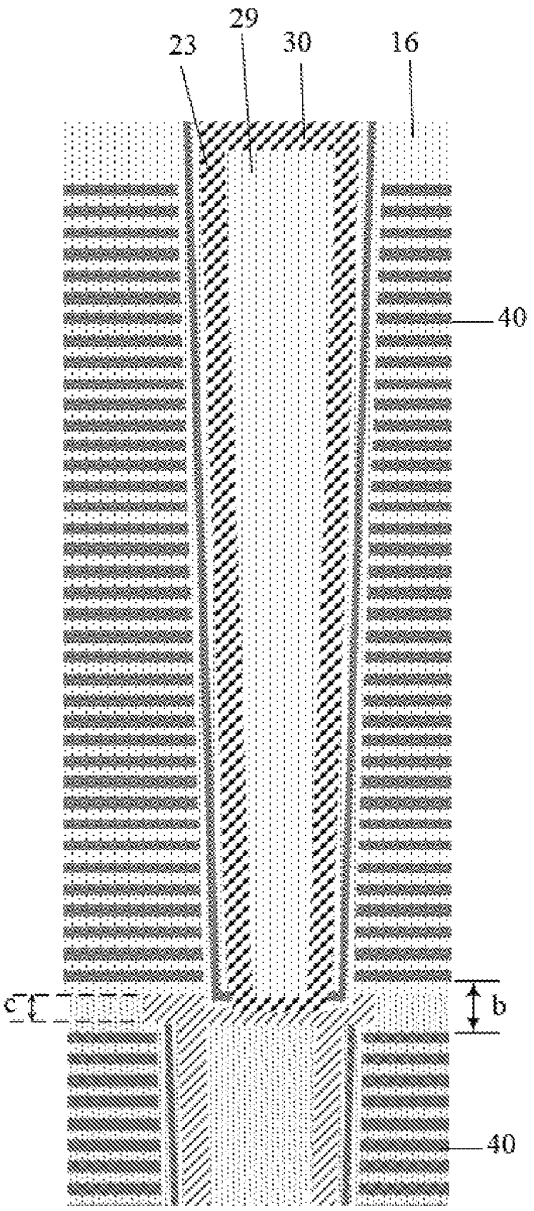


FIG. 22A

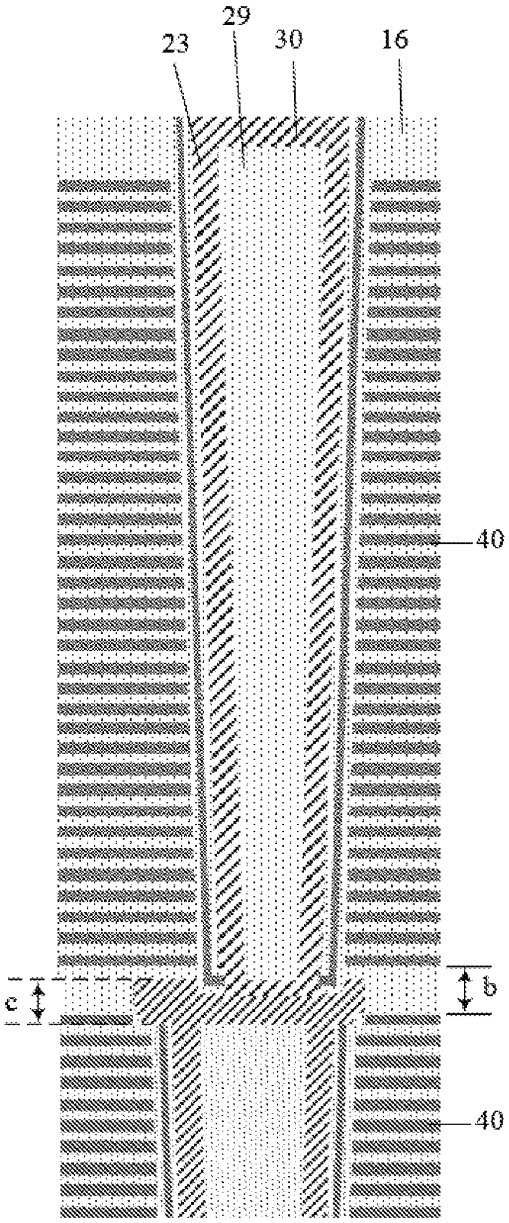


FIG. 22B

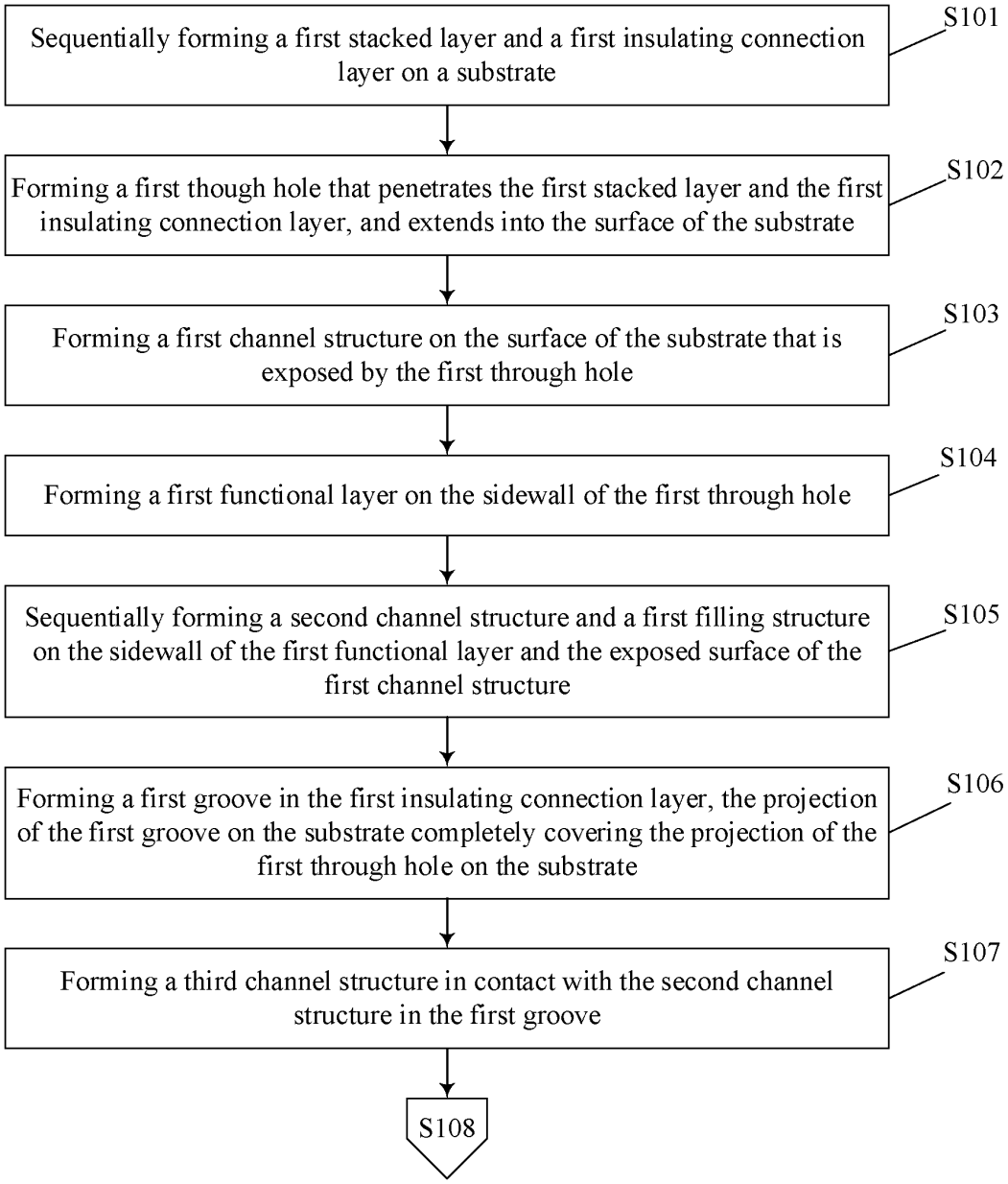

Sequentially forming a first stacked layer and a first insulating connection layer on a substrate
S101
Forming a first though hole that penetrates the first stacked layer and the first insulating connection layer, and extends into the surface of the substrate
S102
Forming a first channel structure on the surface of the substrate that is exposed by the first through hole
S103
Forming a first functional layer on the sidewall of the first through hole
S104
Sequentially forming a second channel structure and a first filling structure on the sidewall of the first functional layer and the exposed surface of the first channel structure
S105
Forming a first groove in the first insulating connection layer, the projection of the first groove on the substrate completely covering the projection of the first through hole on the substrate
S106
Forming a third channel structure in contact with the second channel structure in the first groove
S107
S108

FIG. 23A

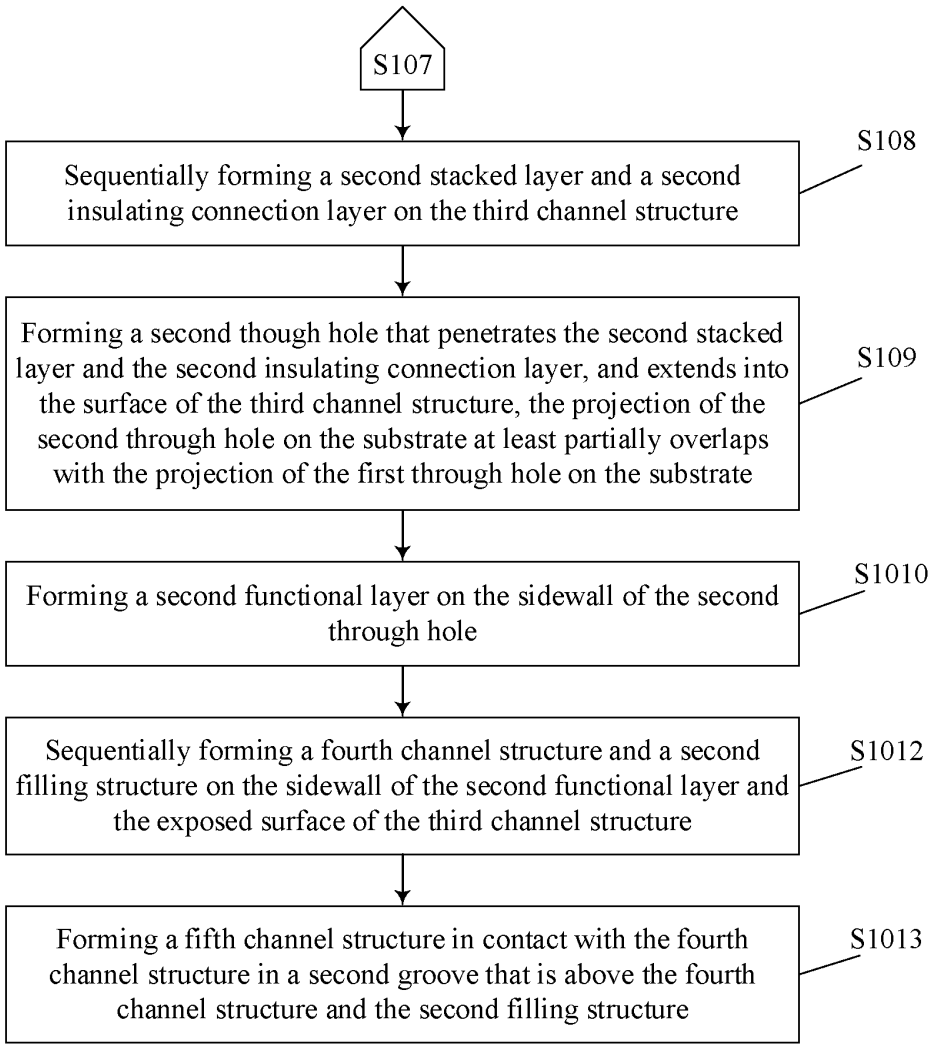

S107
Sequentially forming a second stacked layer and a second insulating connection layer on the third channel structure
S108
Forming a second though hole that penetrates the second stacked layer and the second insulating connection layer, and extends into the surface of the third channel structure, the projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate
S109
Forming a second functional layer on the sidewall of the second through hole
S1010
Sequentially forming a fourth channel structure and a second filling structure on the sidewall of the second functional layer and the exposed surface of the third channel structure
S1012
Forming a fifth channel structure in contact with the fourth channel structure in a second groove that is above the fourth channel structure and the second filling structure
S1013

FIG. 23B

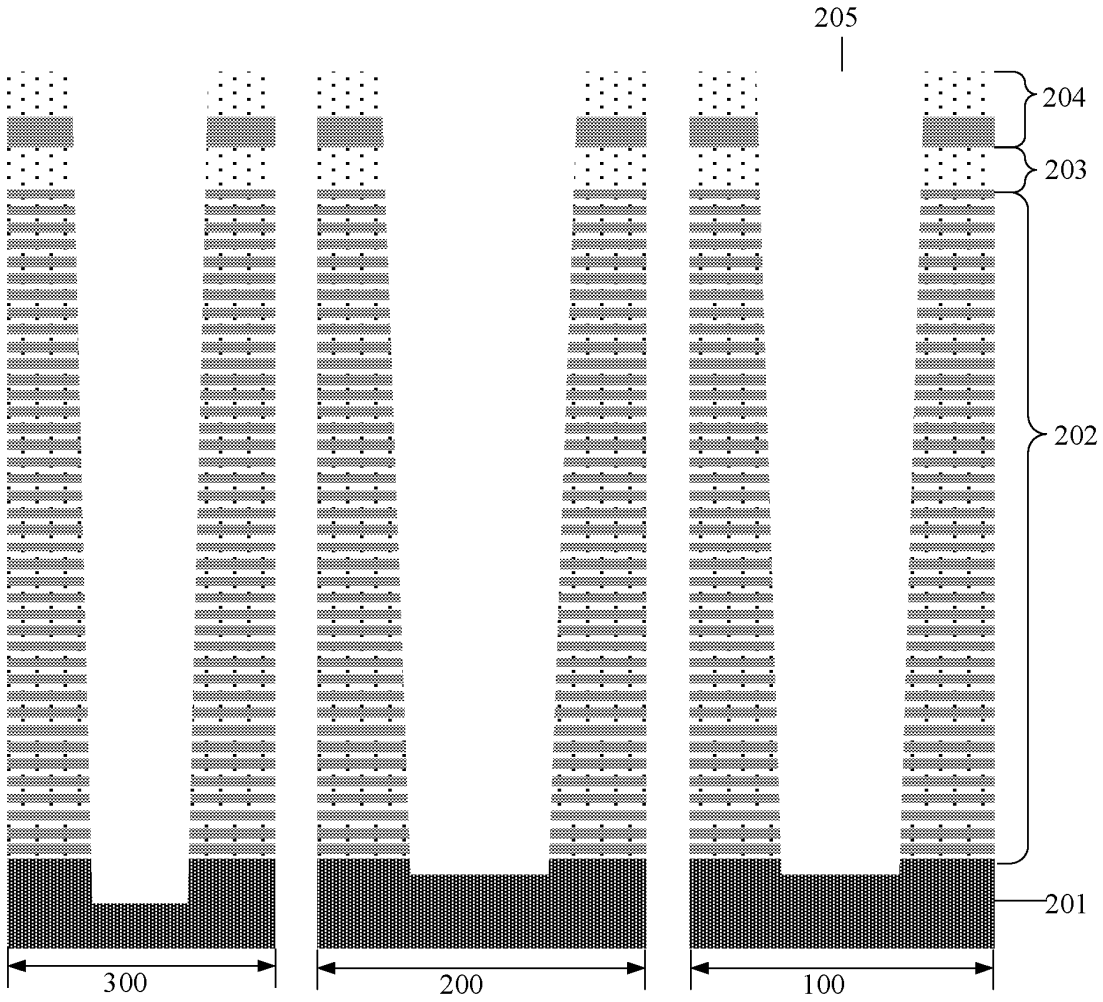


FIG. 24

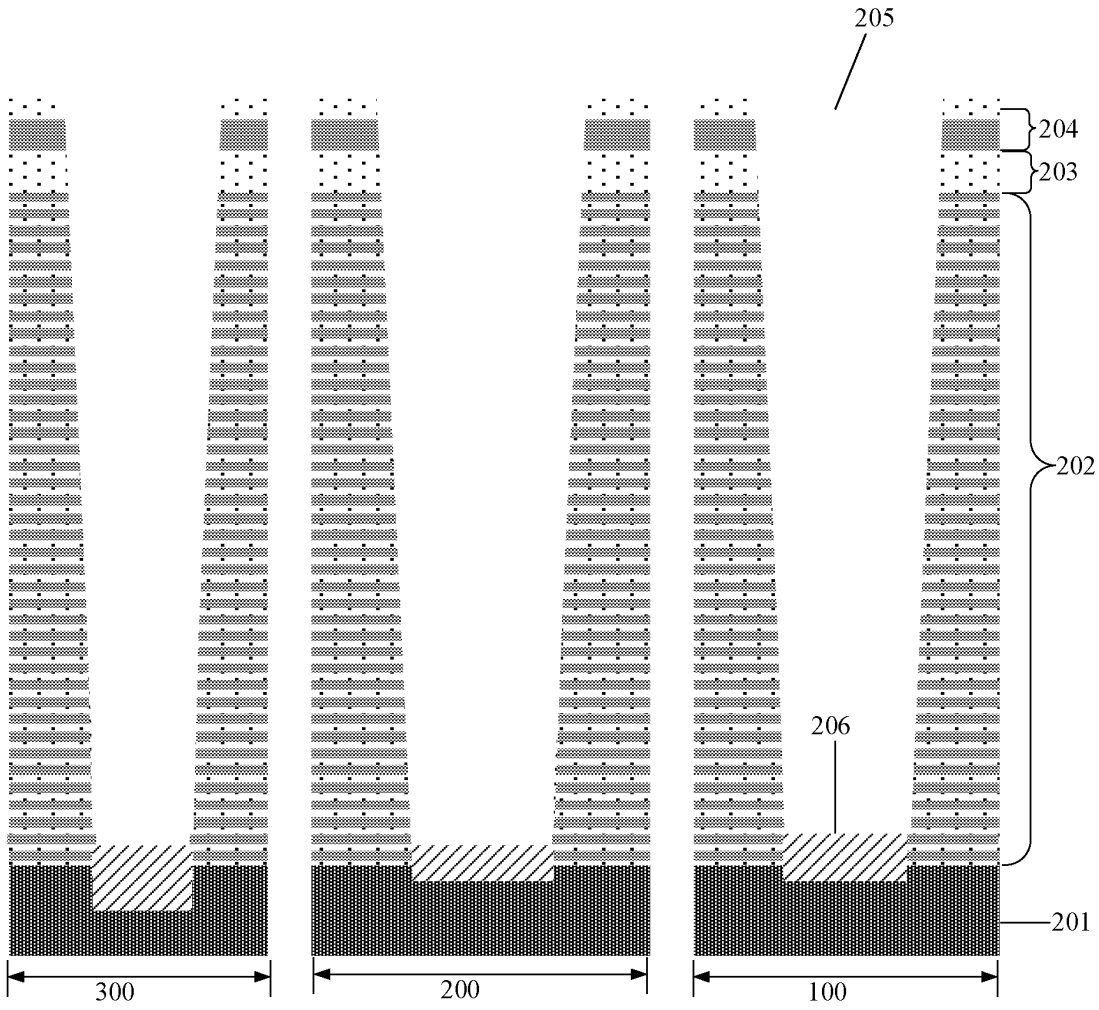


FIG. 25

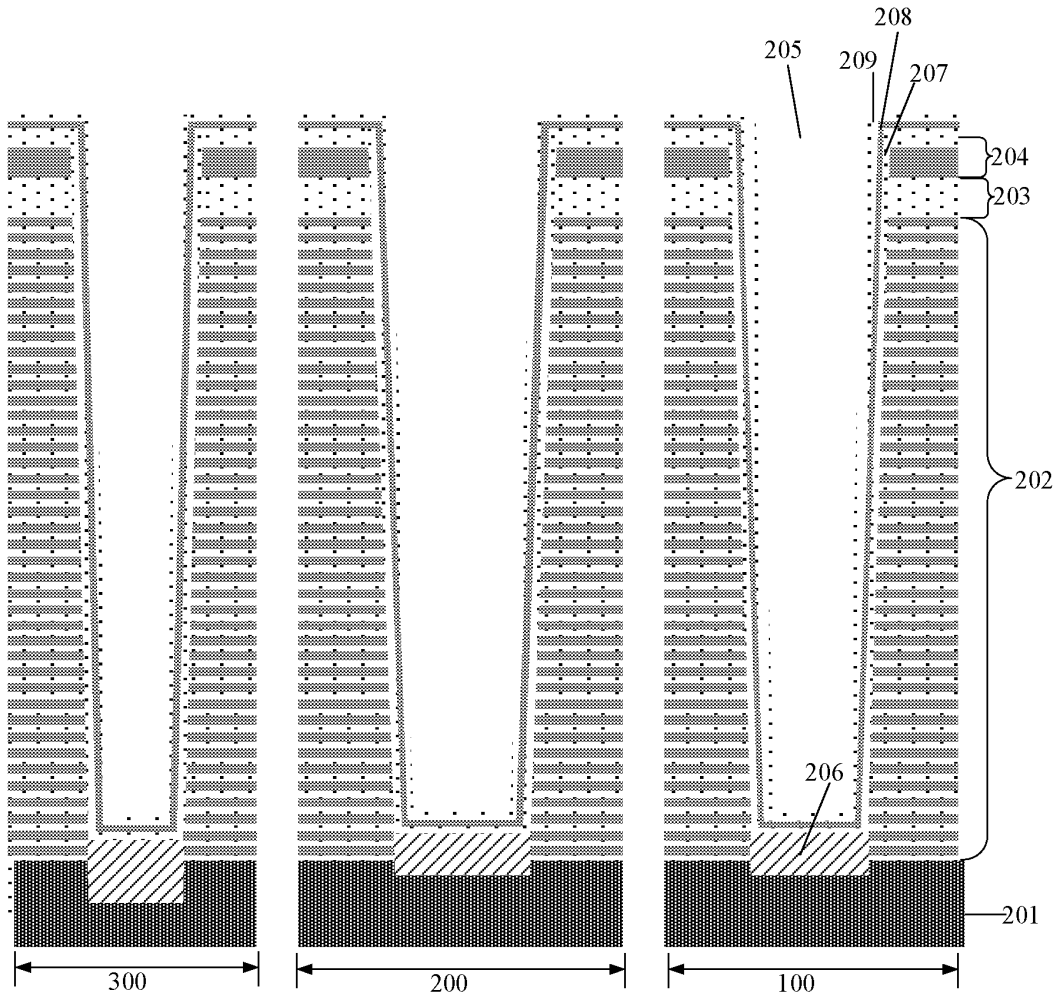


FIG. 26

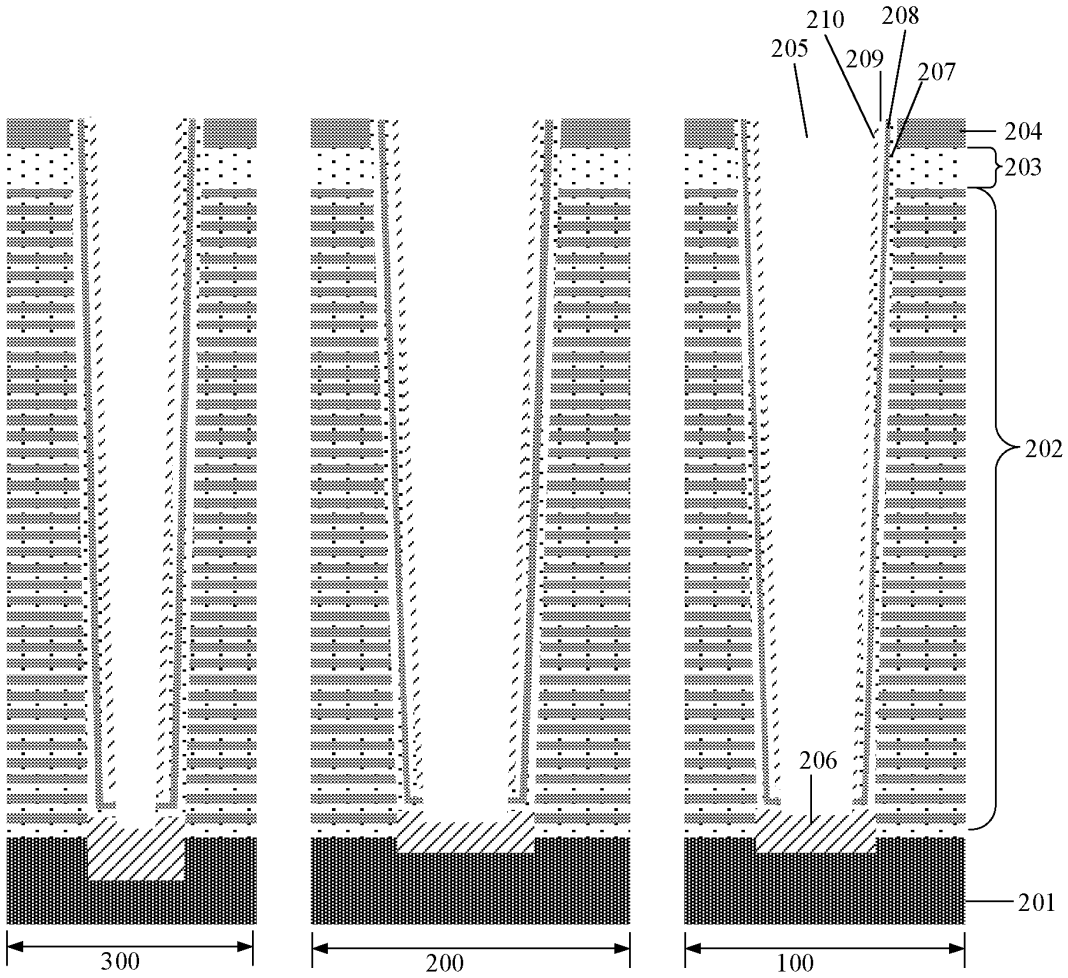


FIG. 27

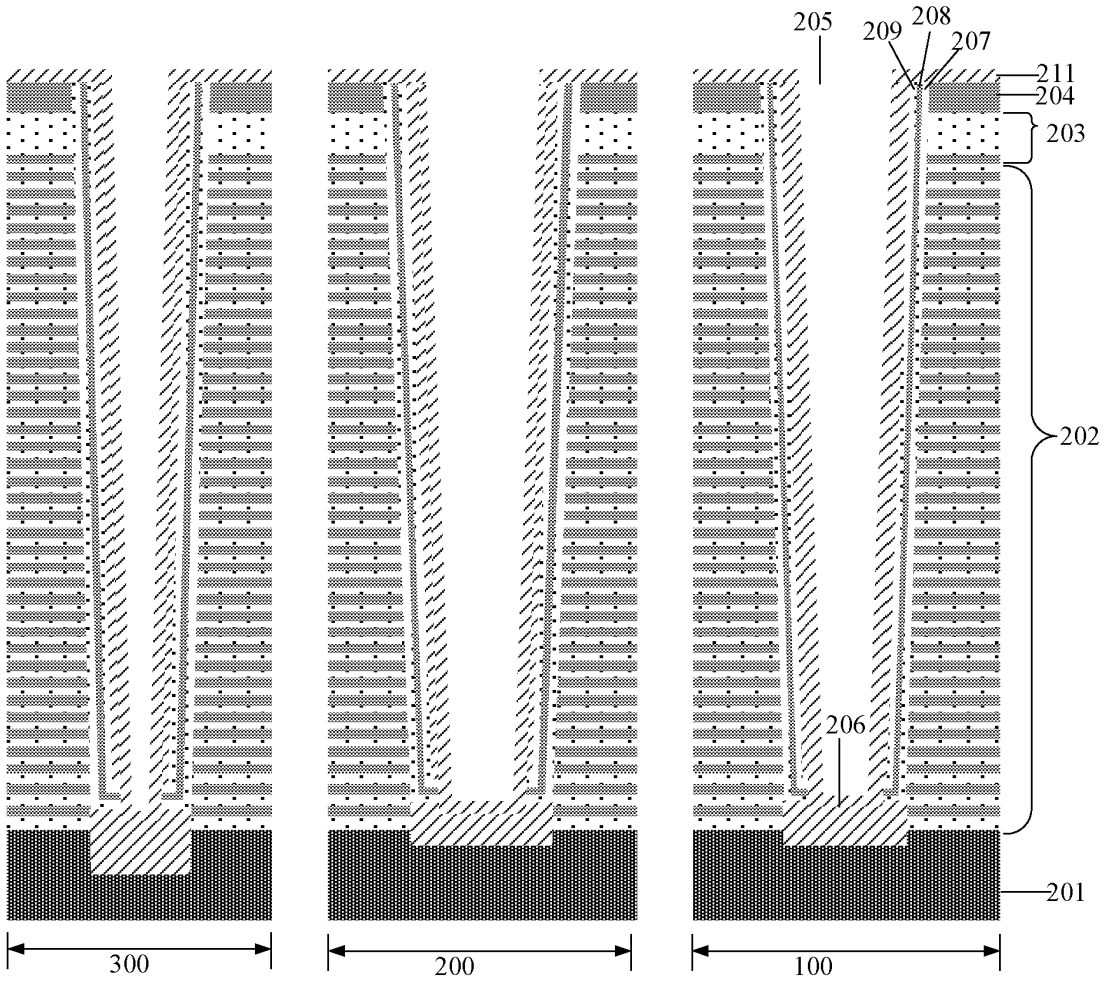


FIG. 28

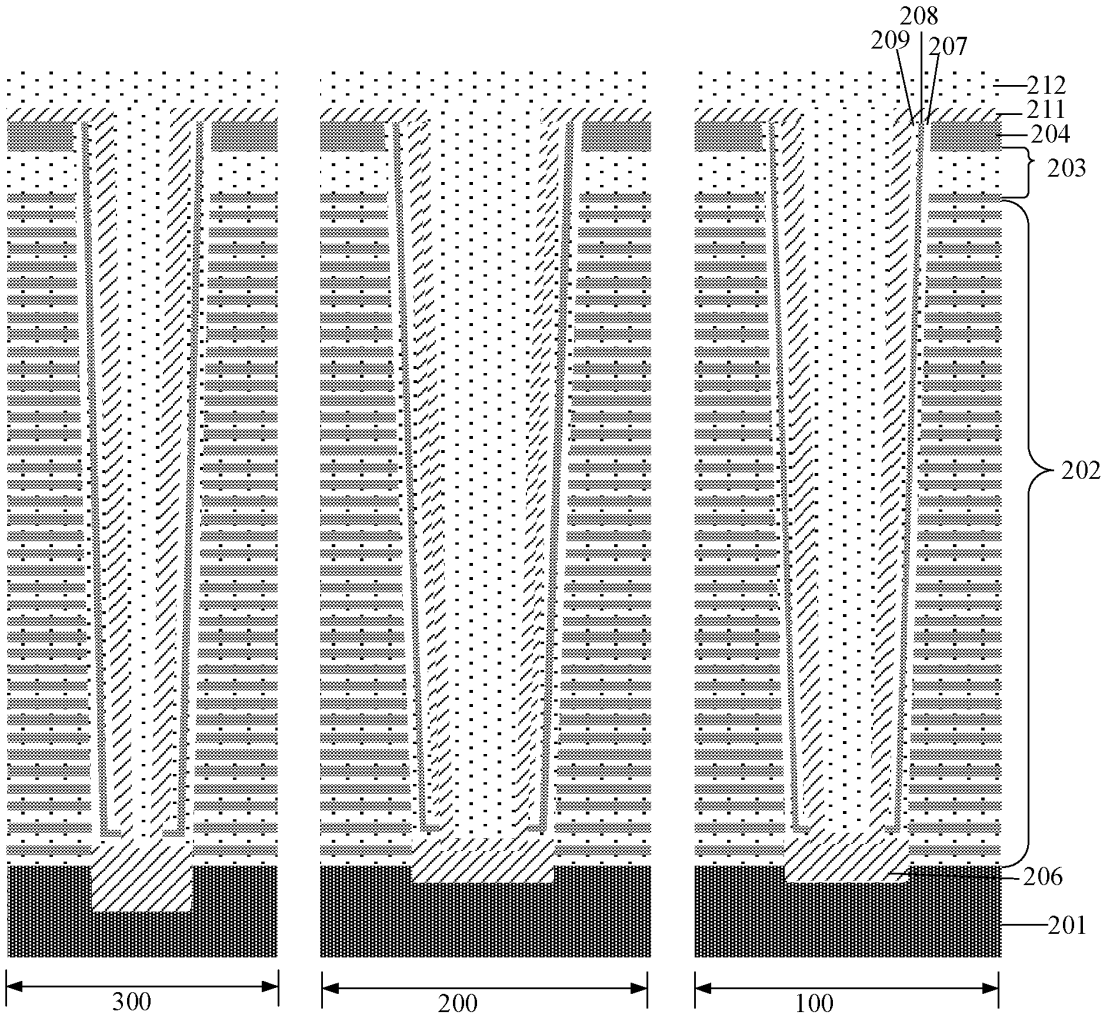


FIG. 29

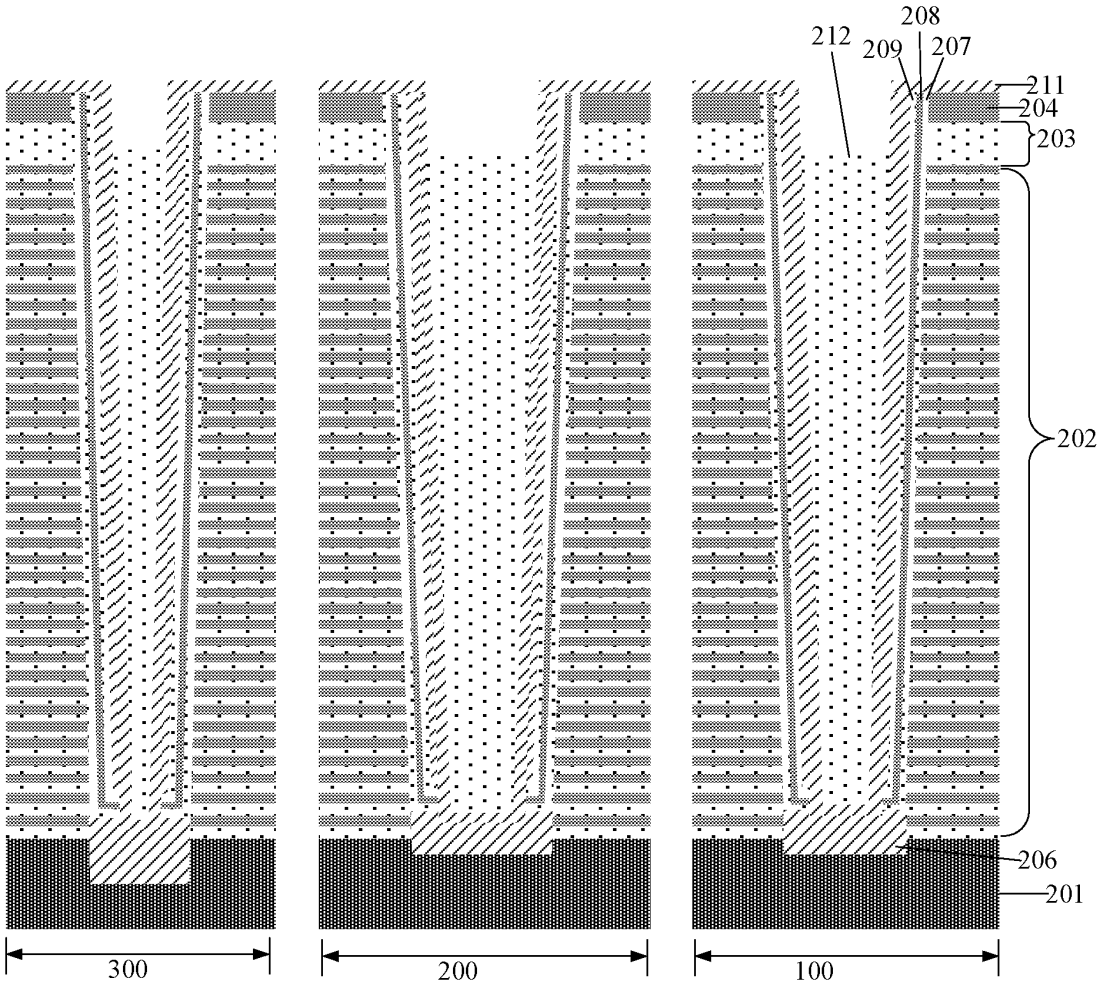


FIG.30A

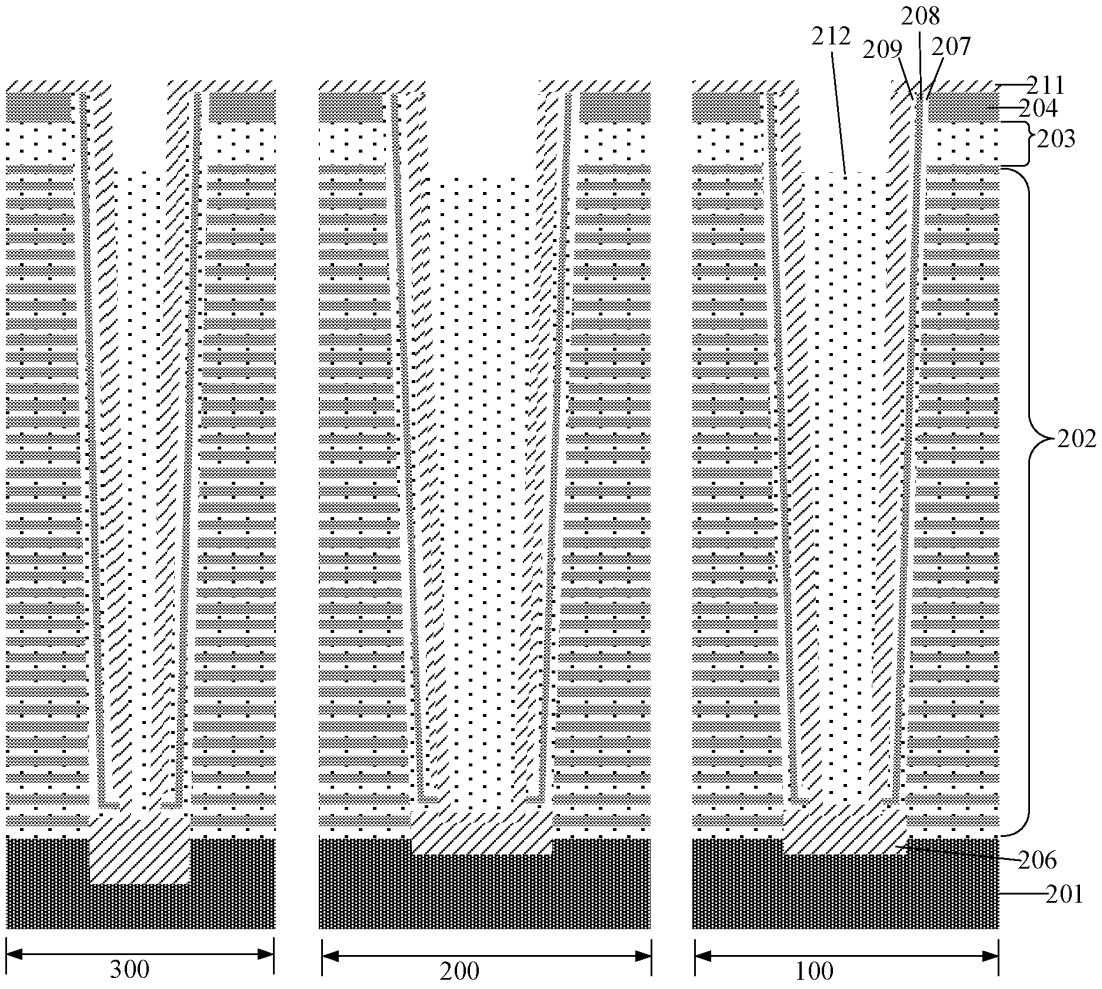


FIG.30B

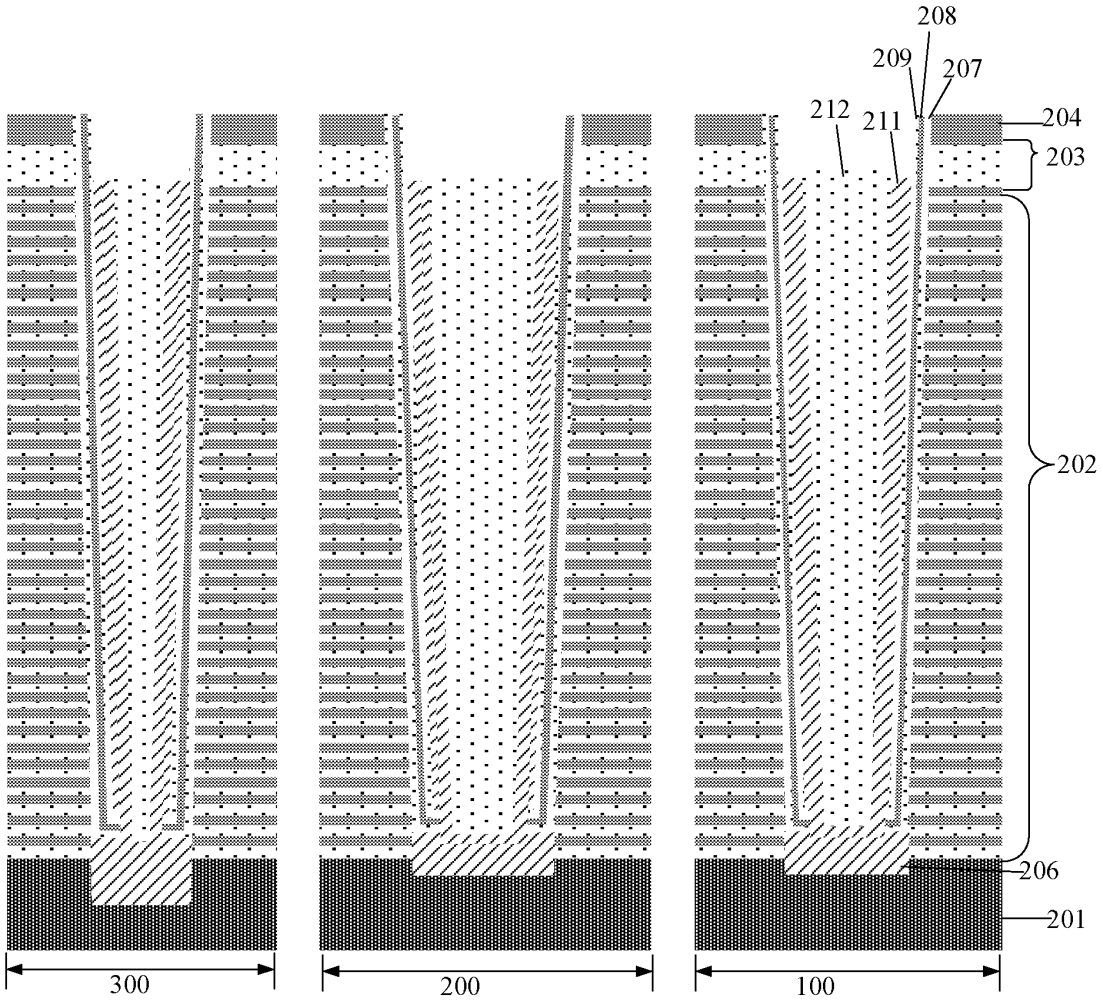


FIG. 31A

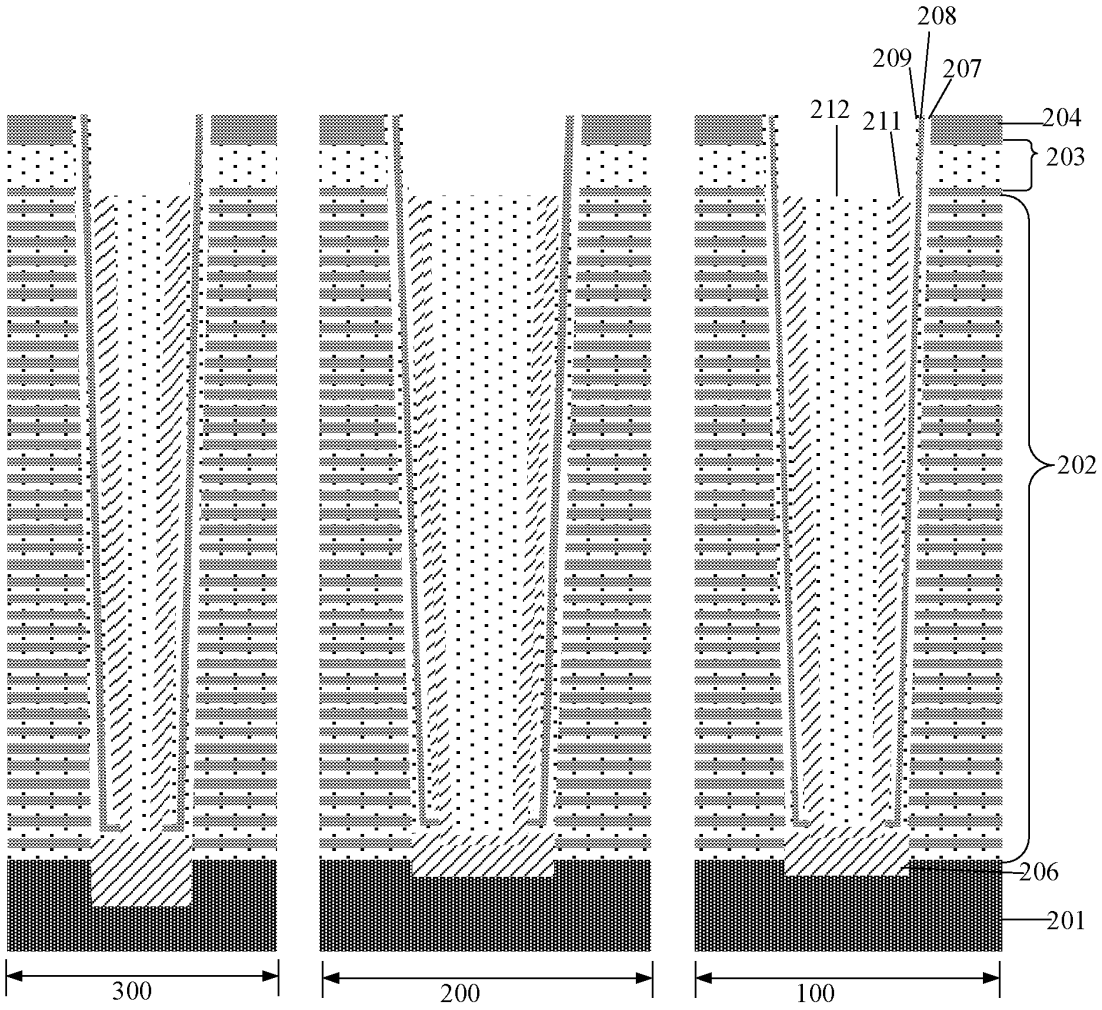


FIG. 31B

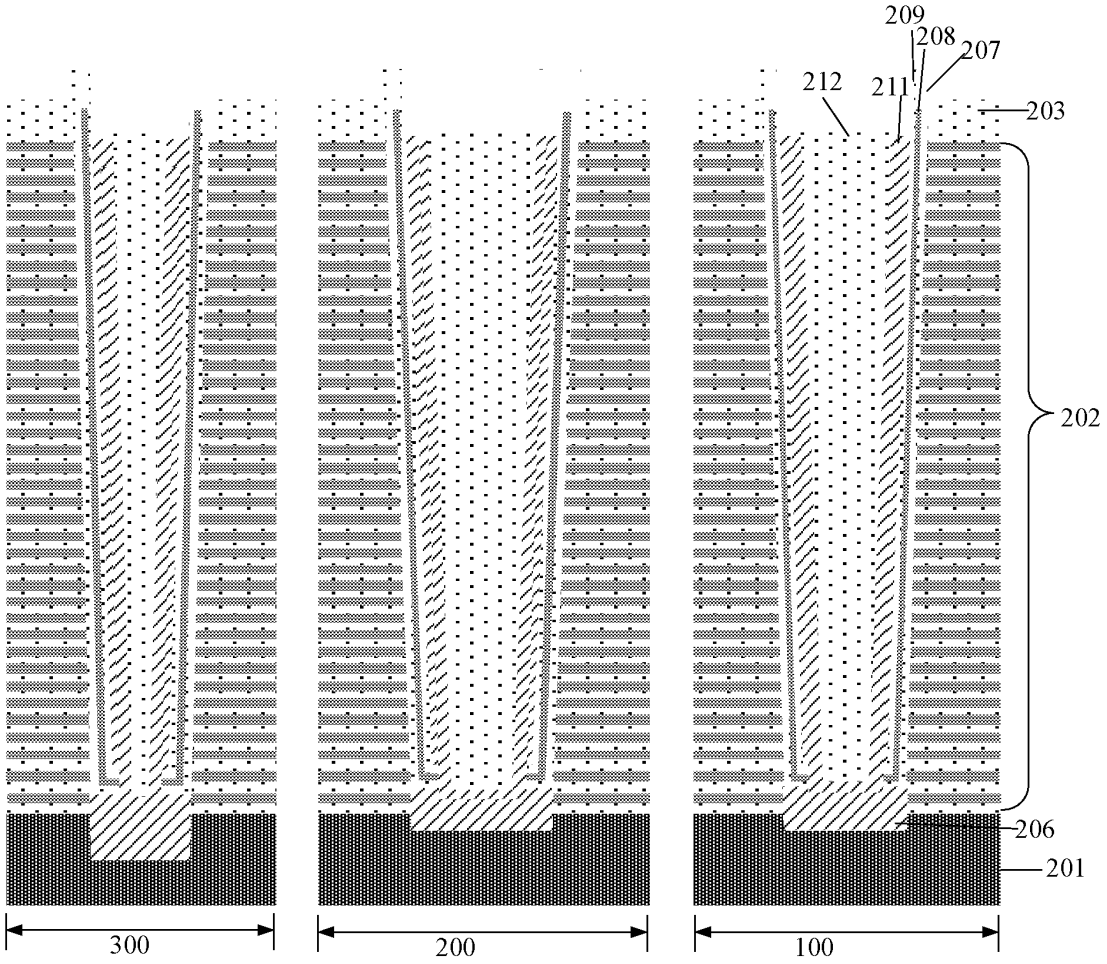


FIG. 32A

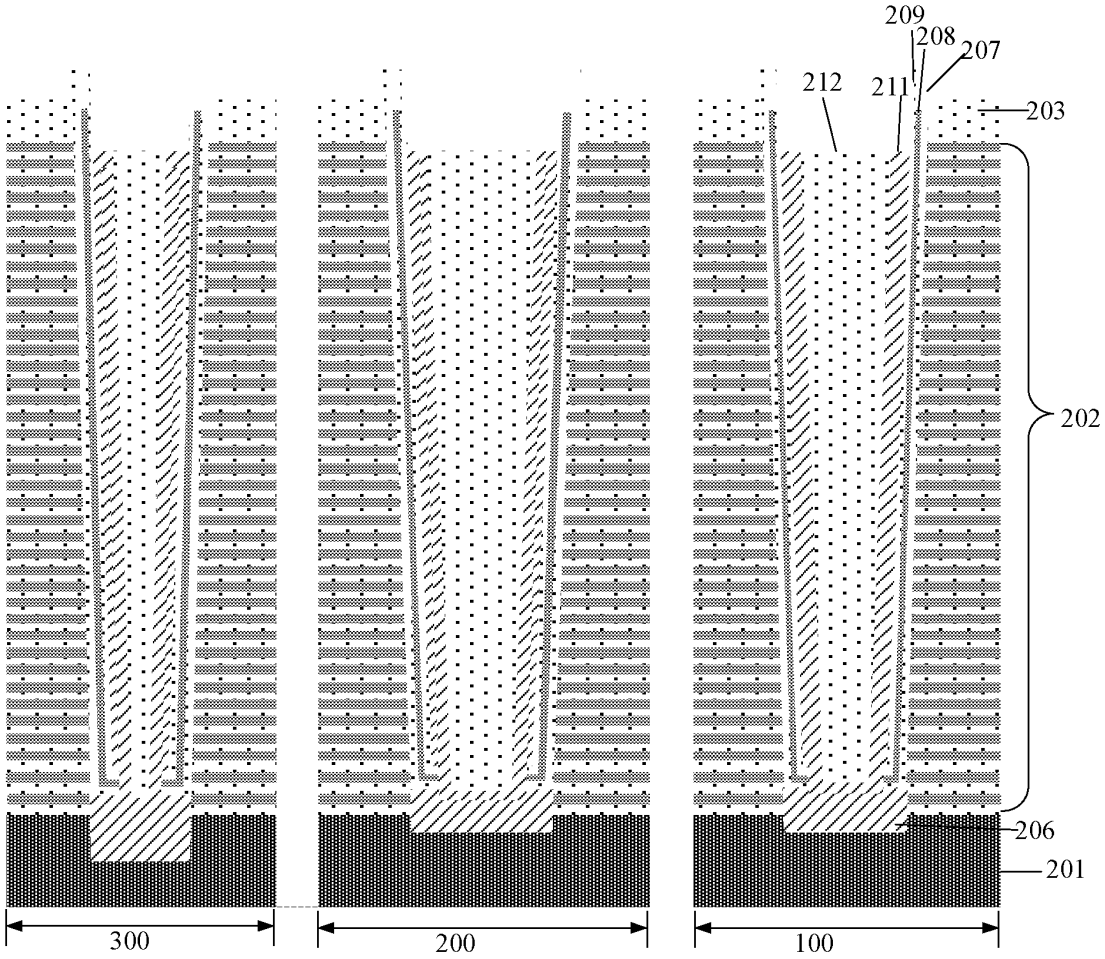


FIG. 32B

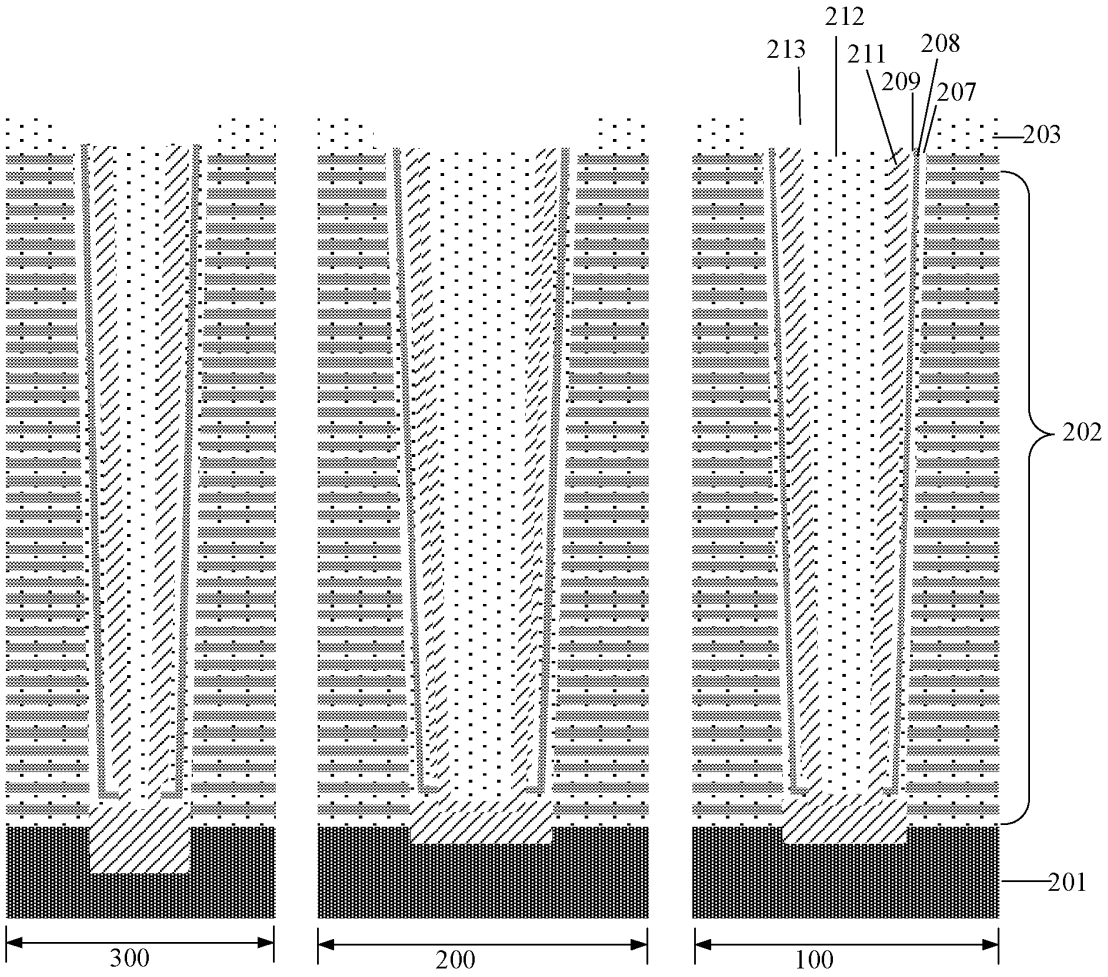


FIG. 33A

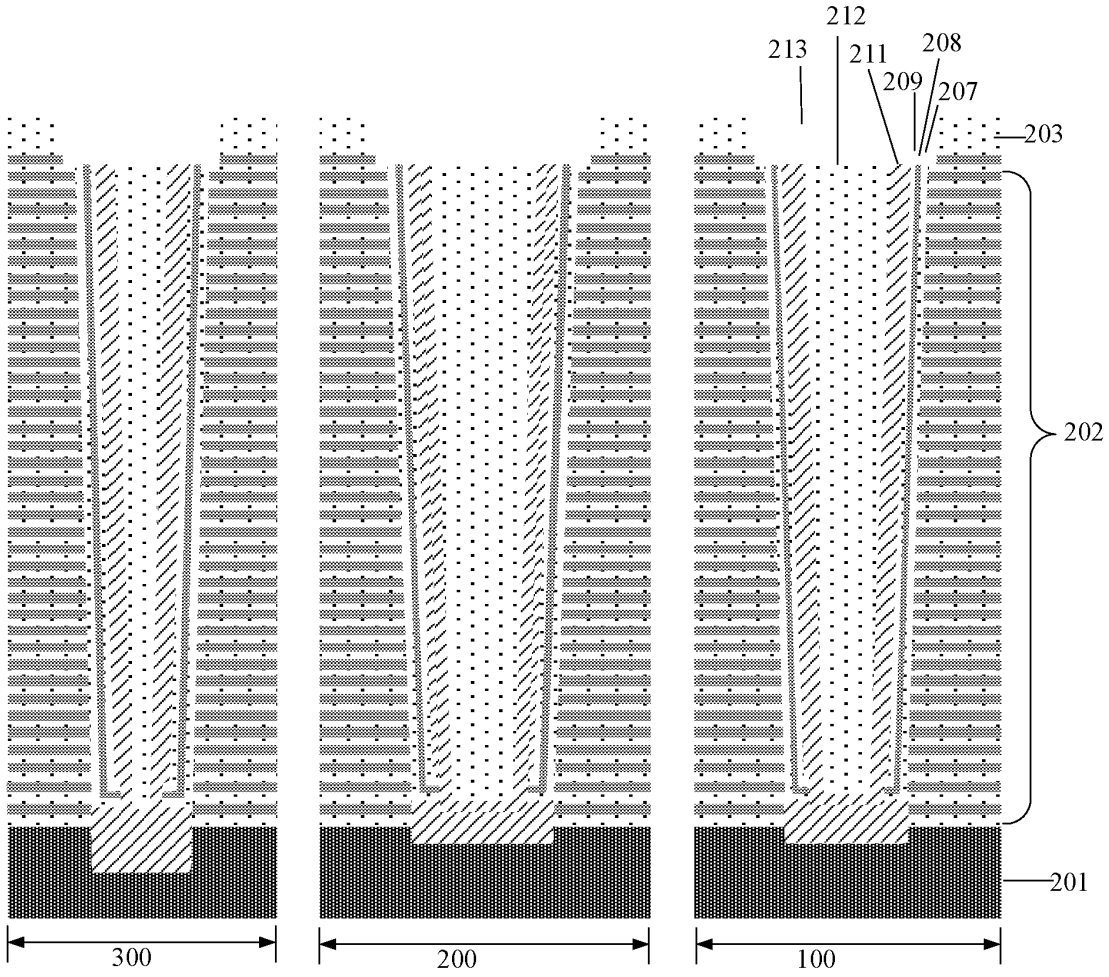


FIG. 33B

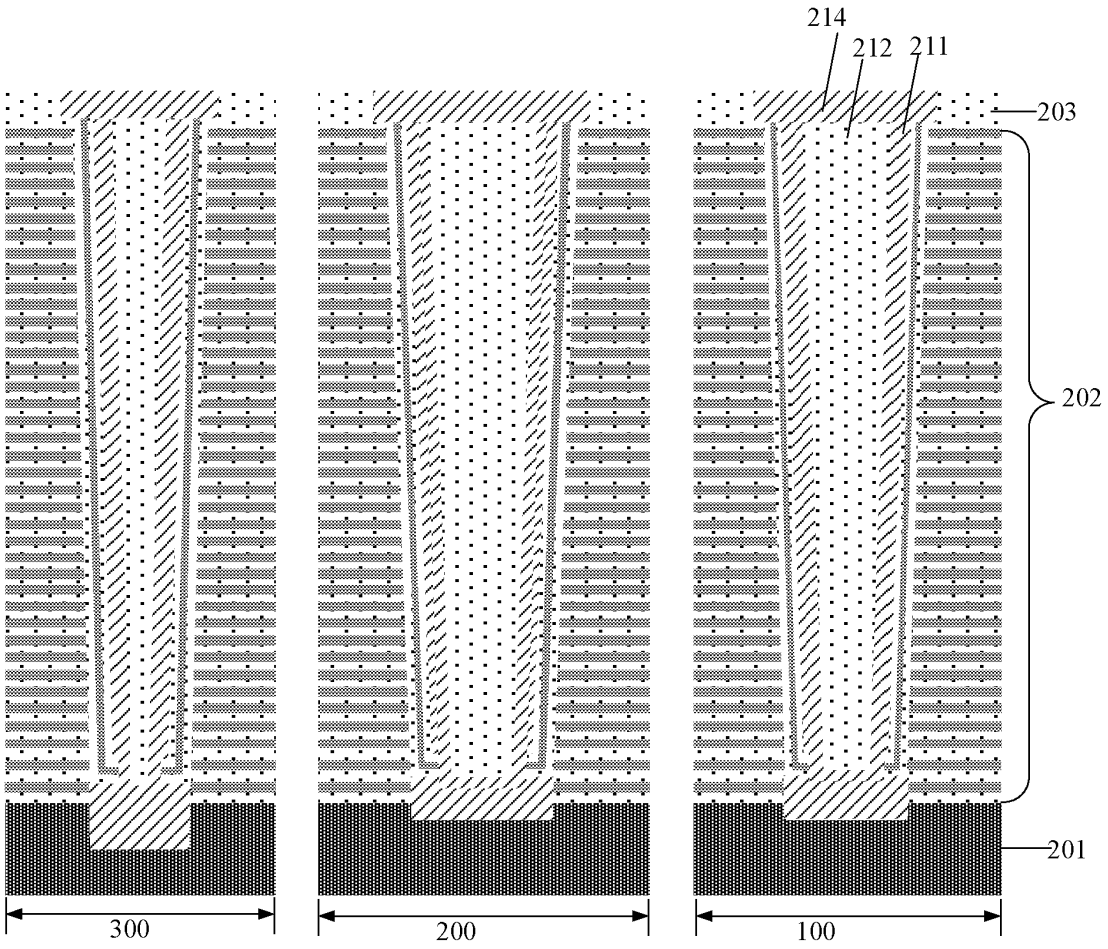


FIG. 34A

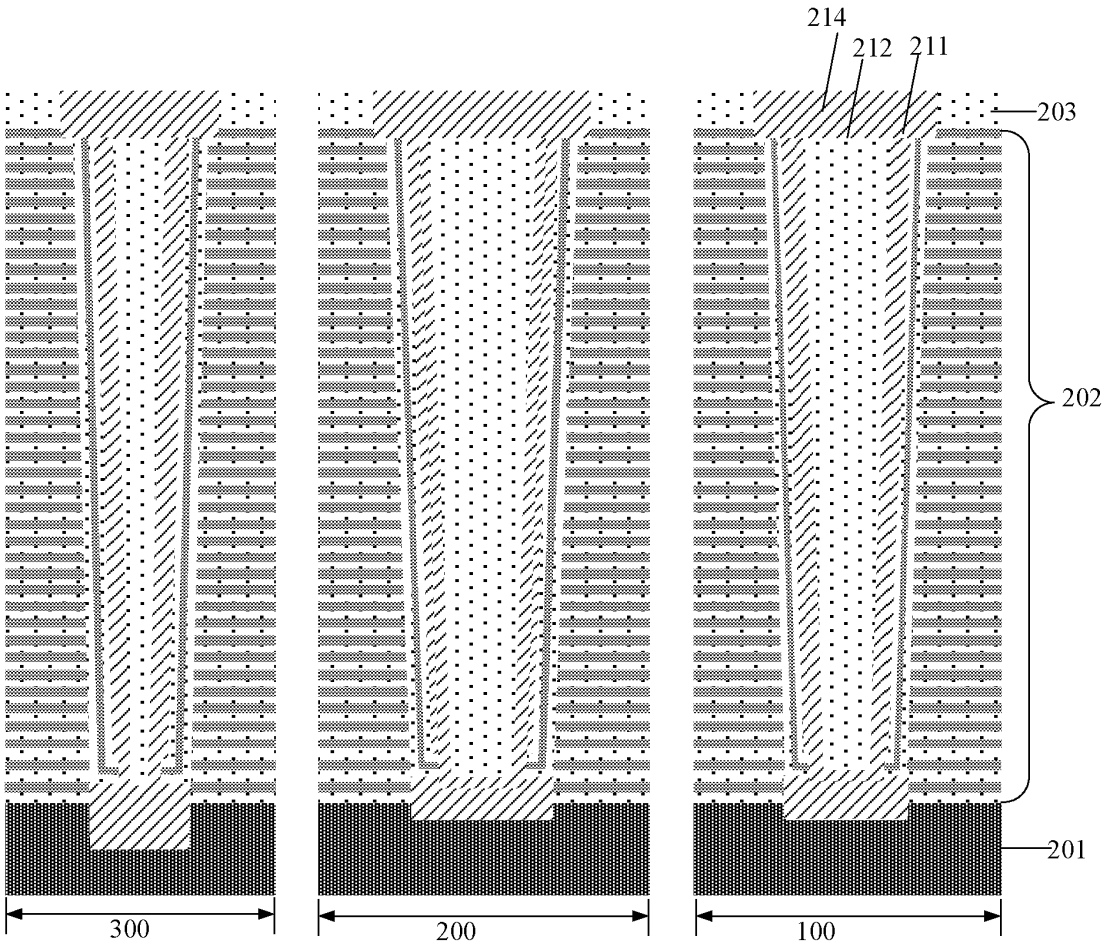


FIG. 34B

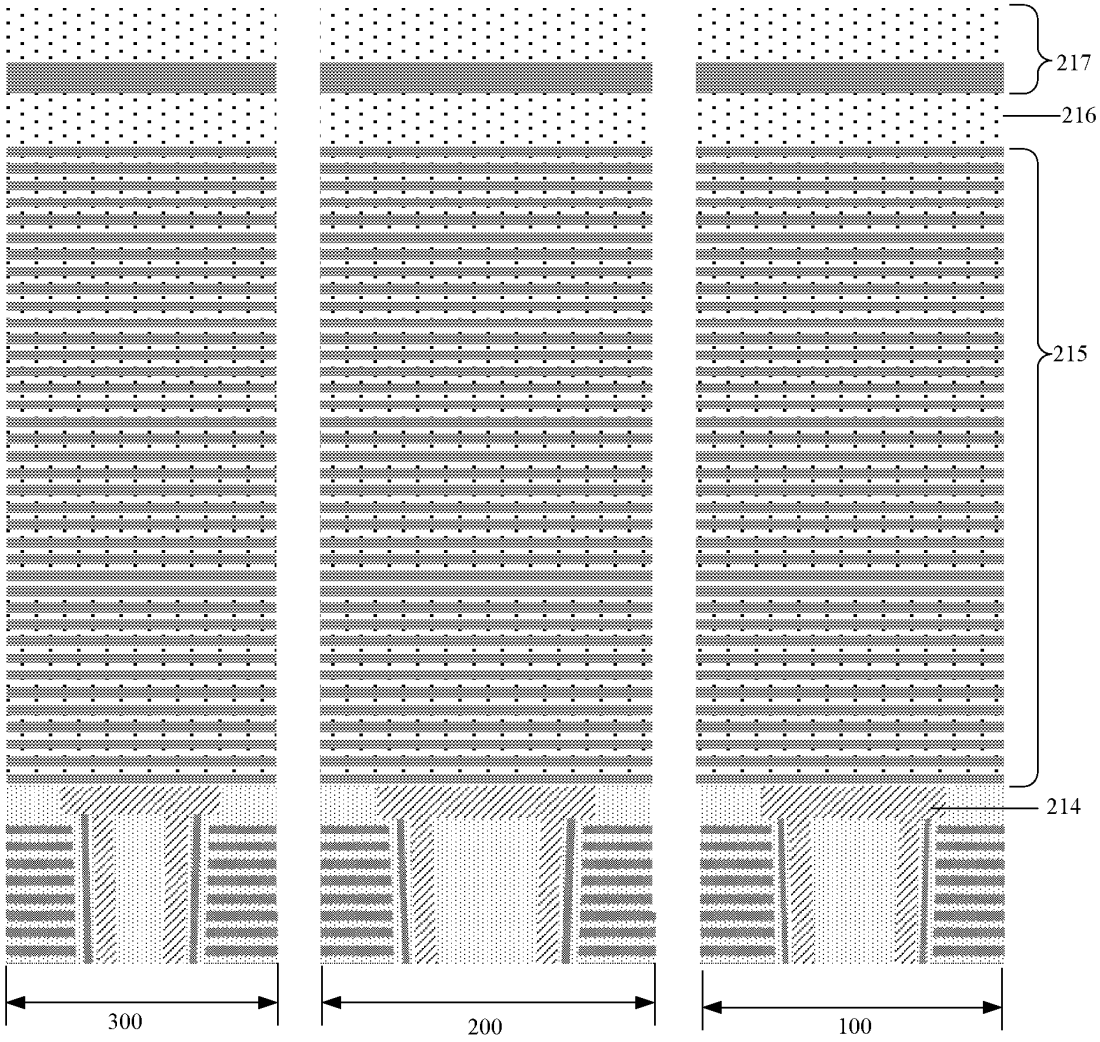


FIG.35

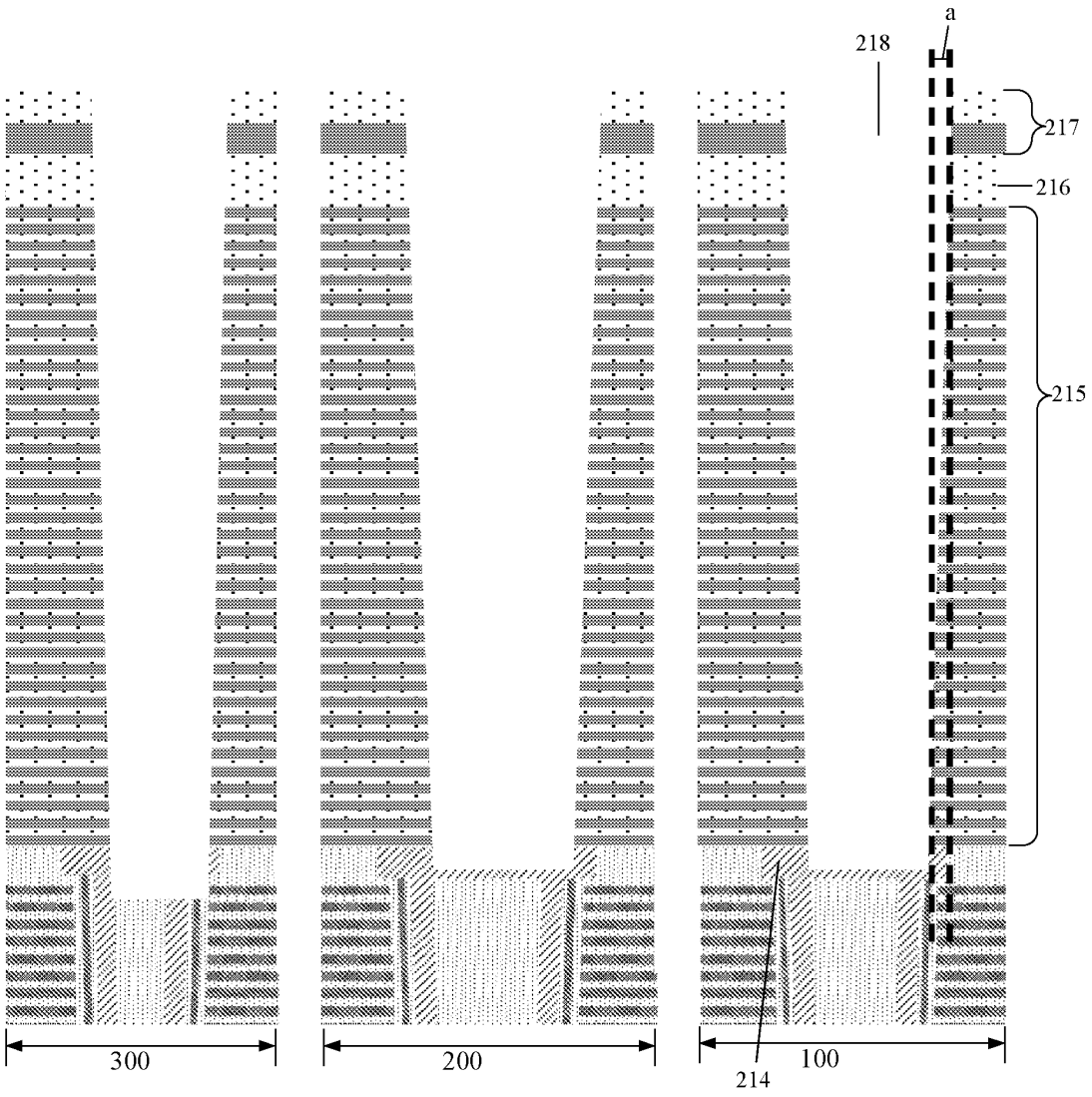


FIG. 36

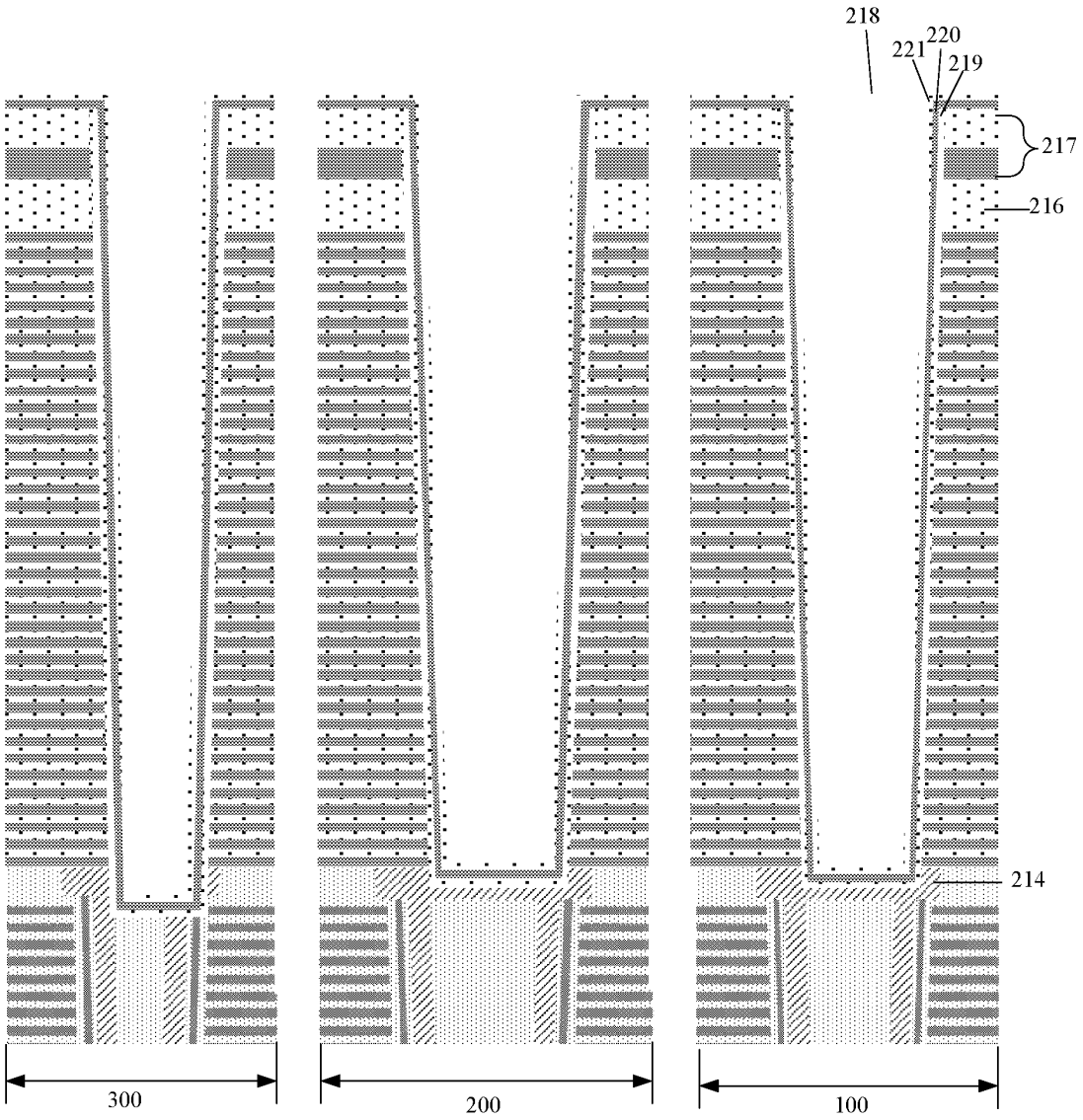


FIG. 37

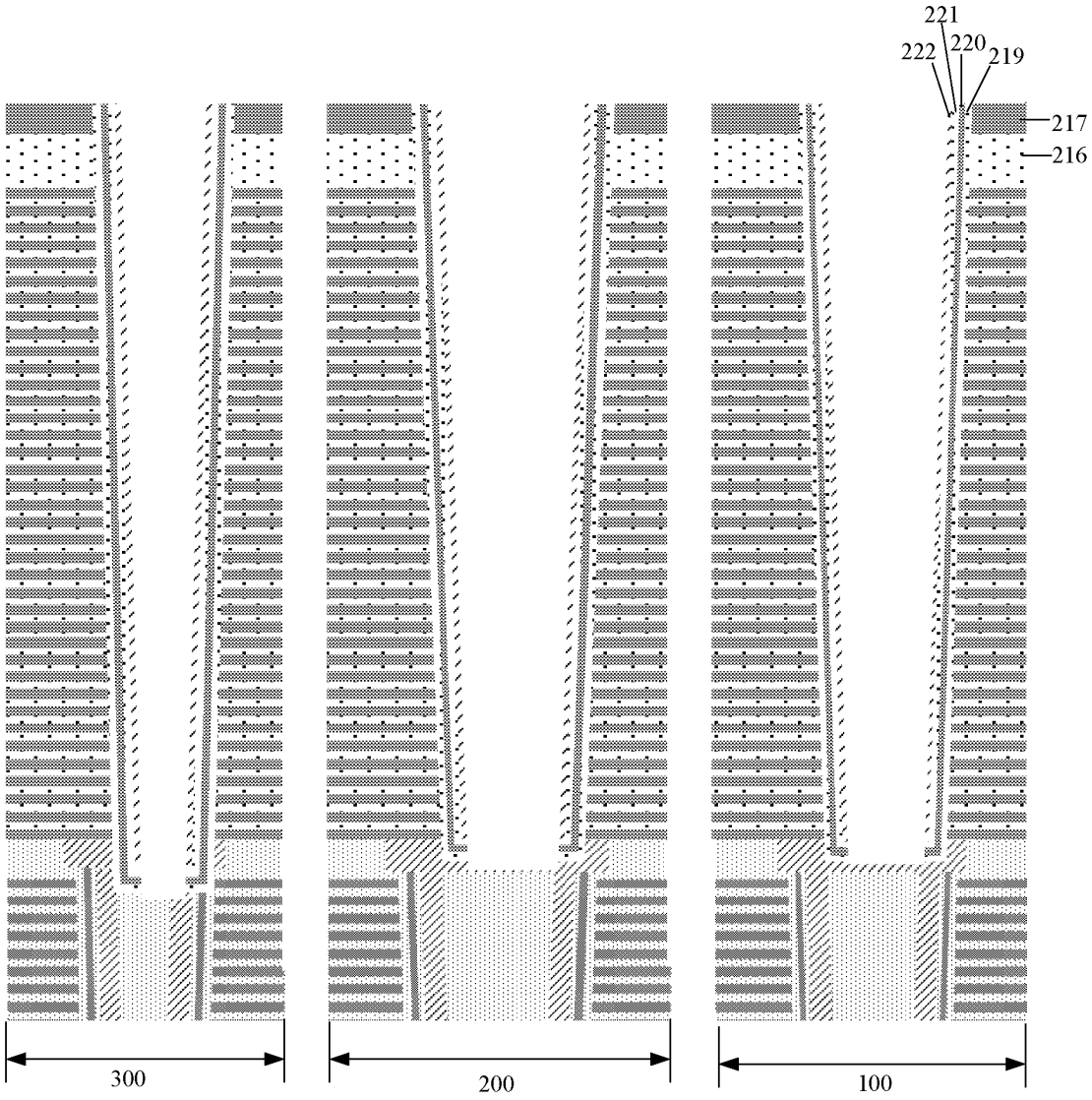


FIG. 38

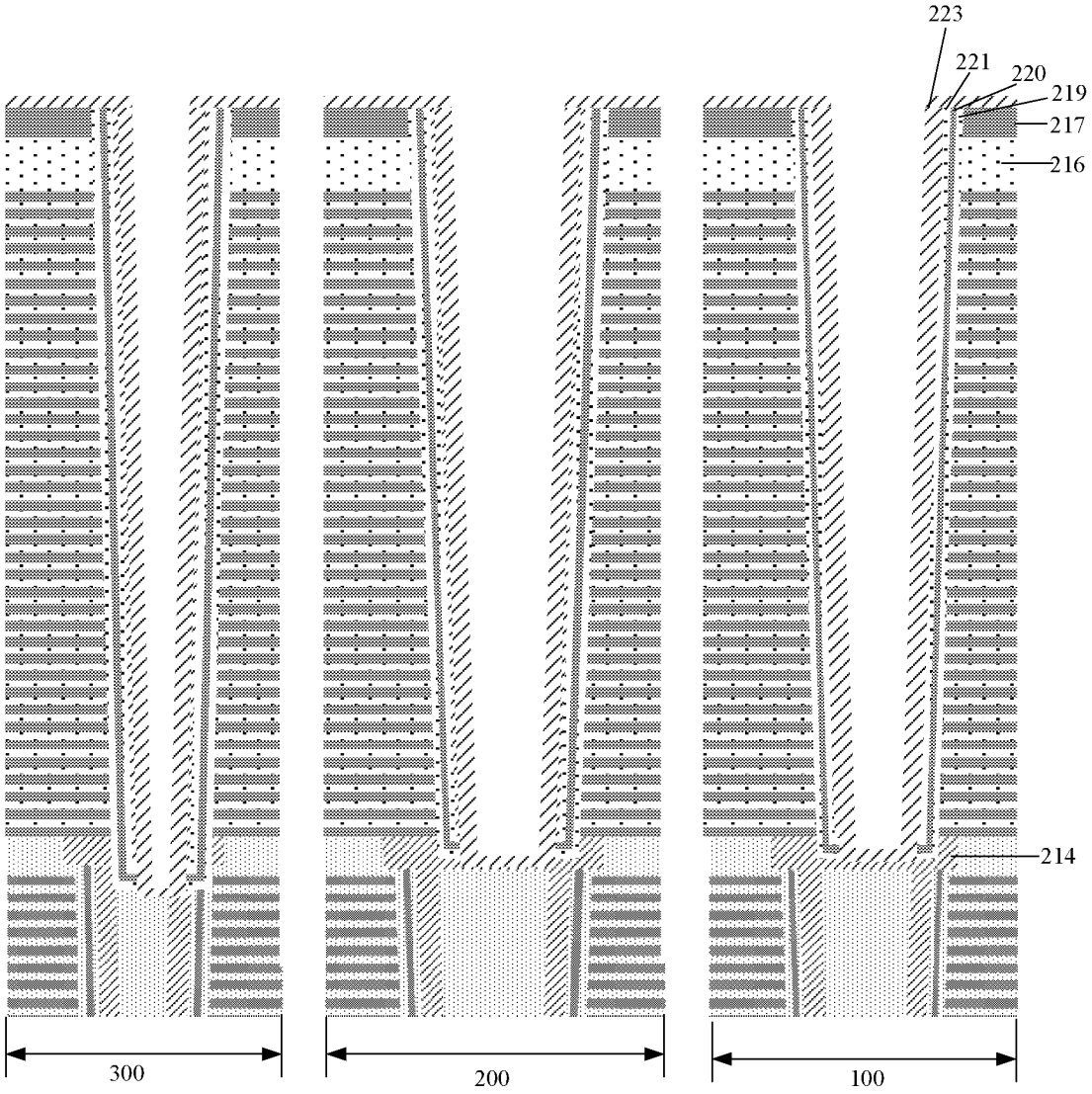


FIG. 39

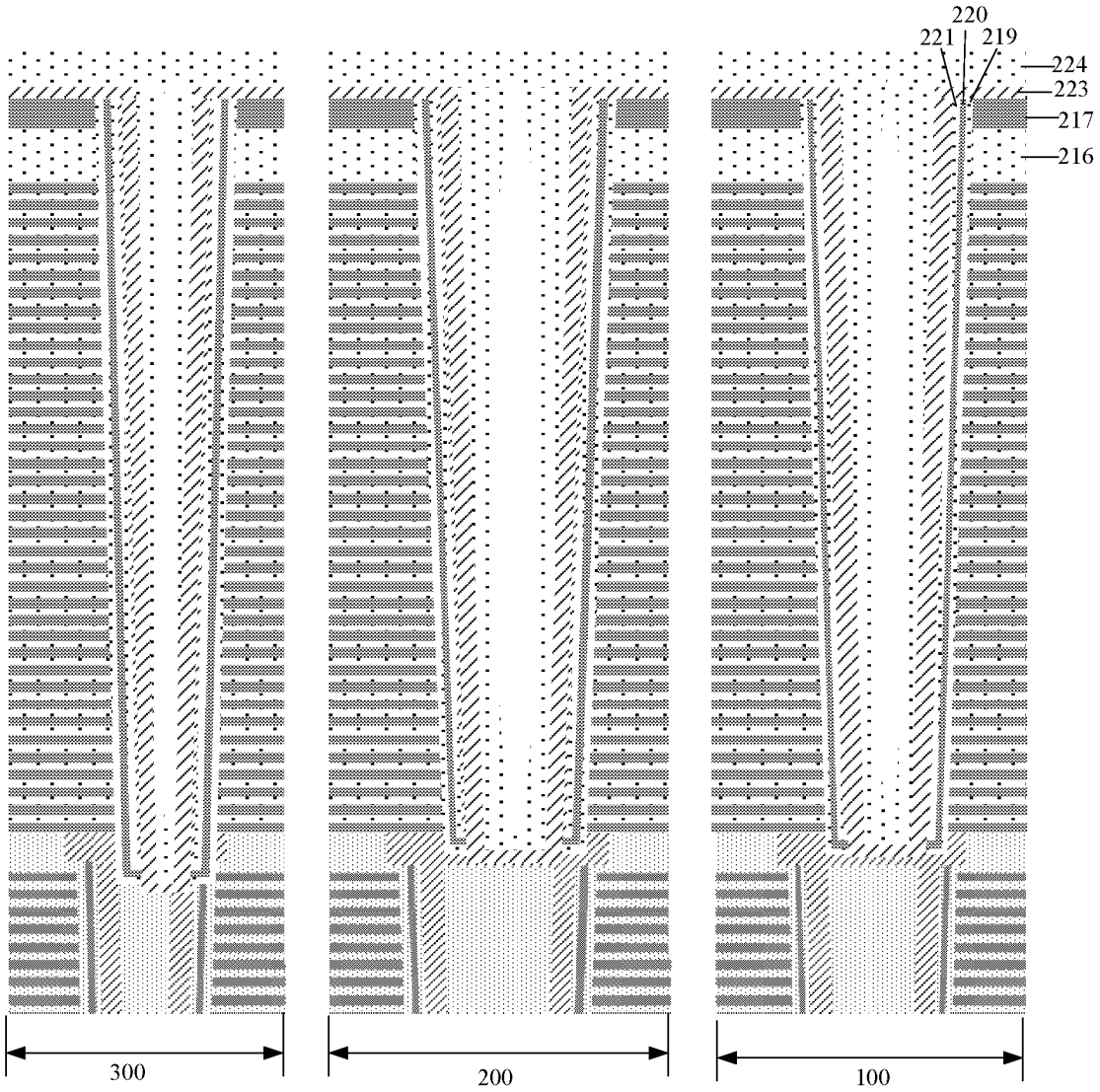


FIG. 40

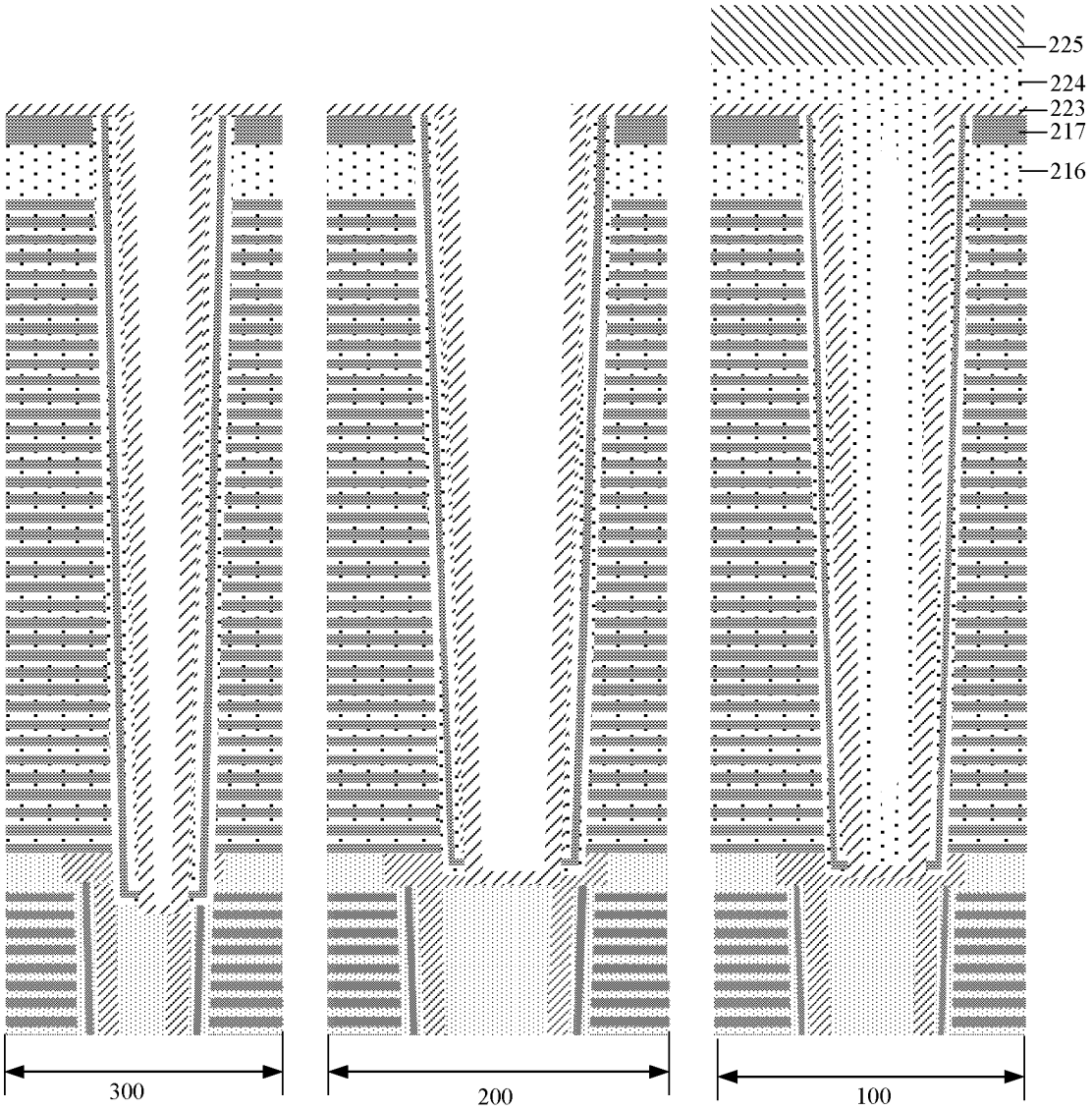


FIG. 41

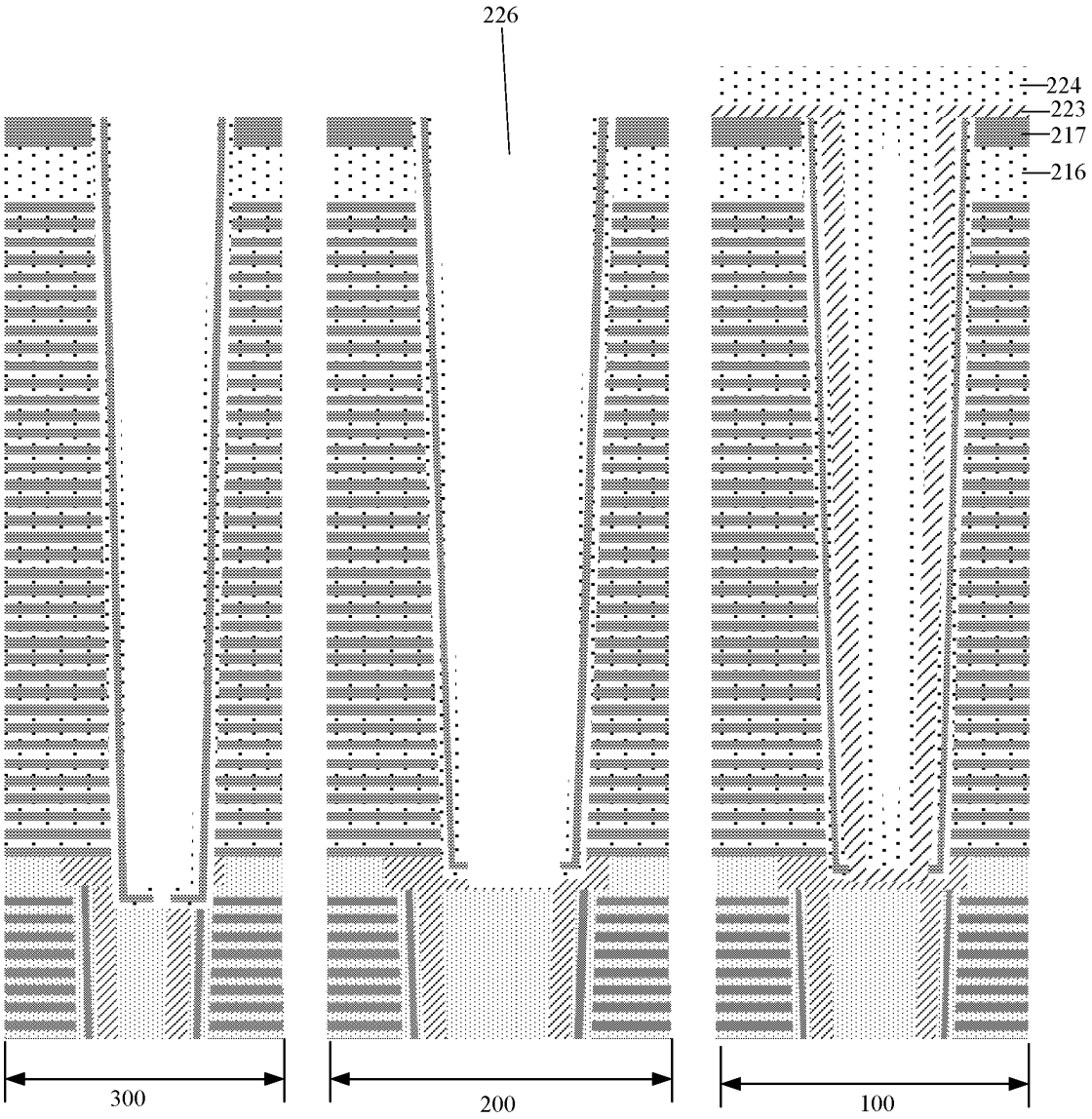


FIG. 42

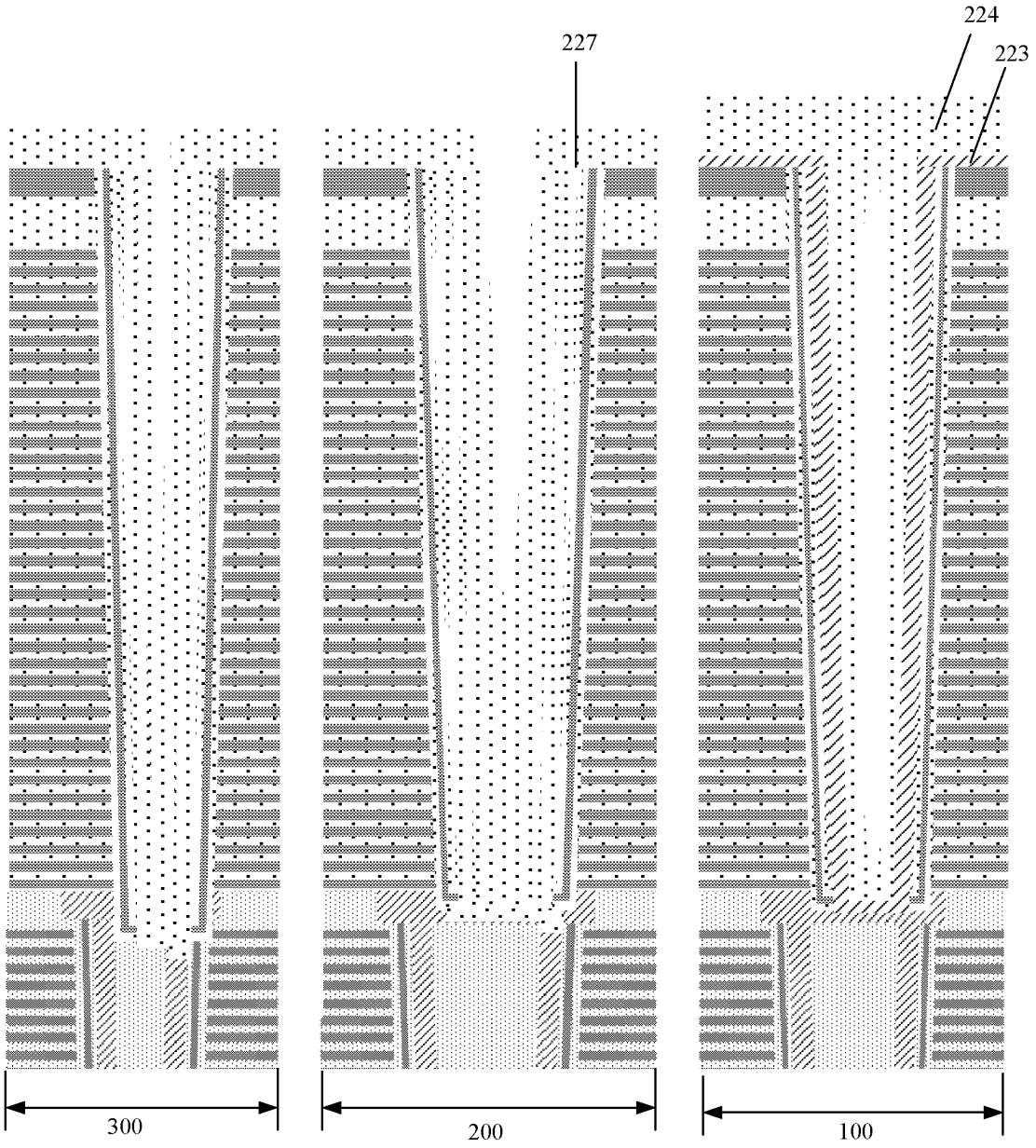


FIG. 43

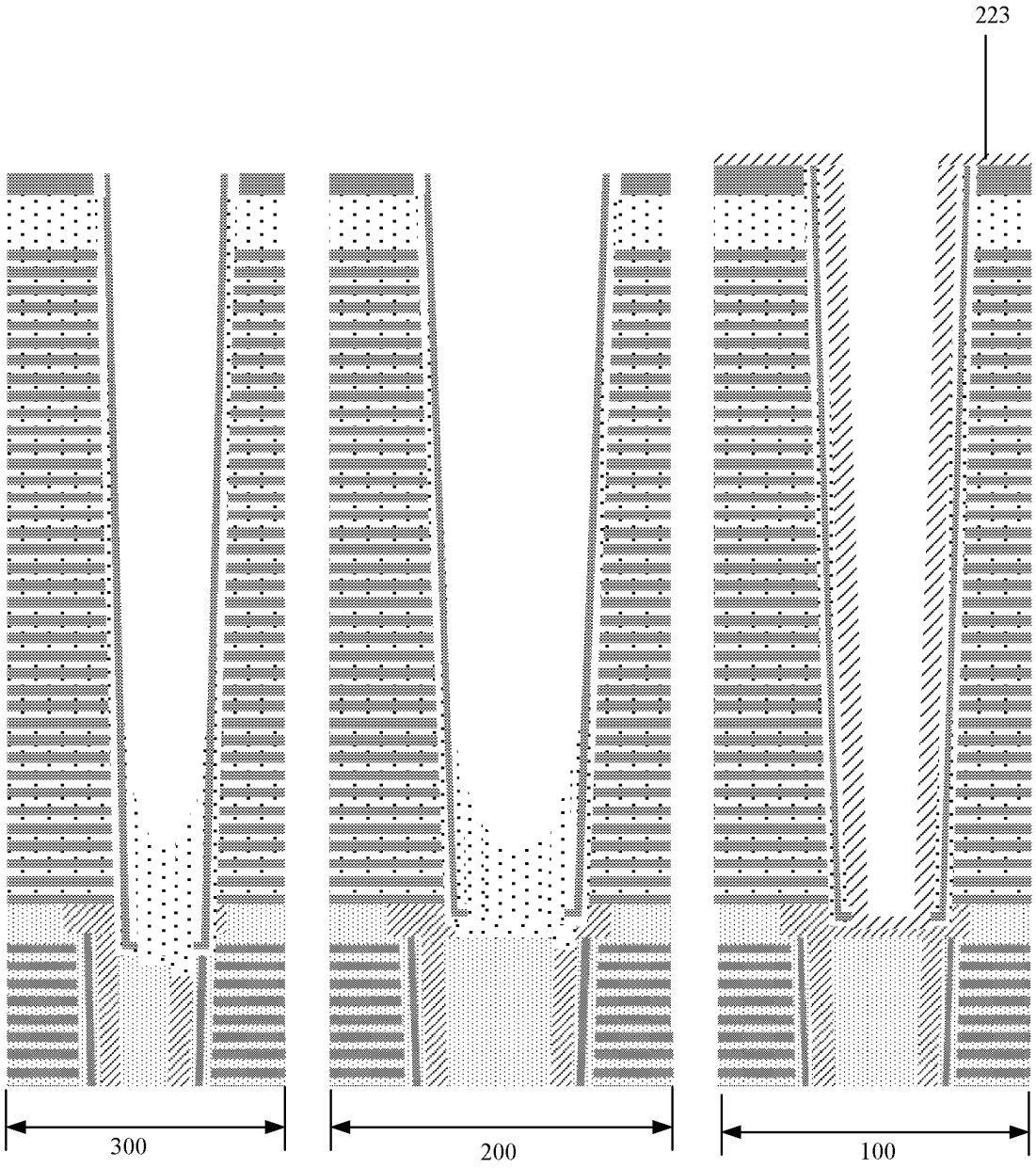


FIG. 44

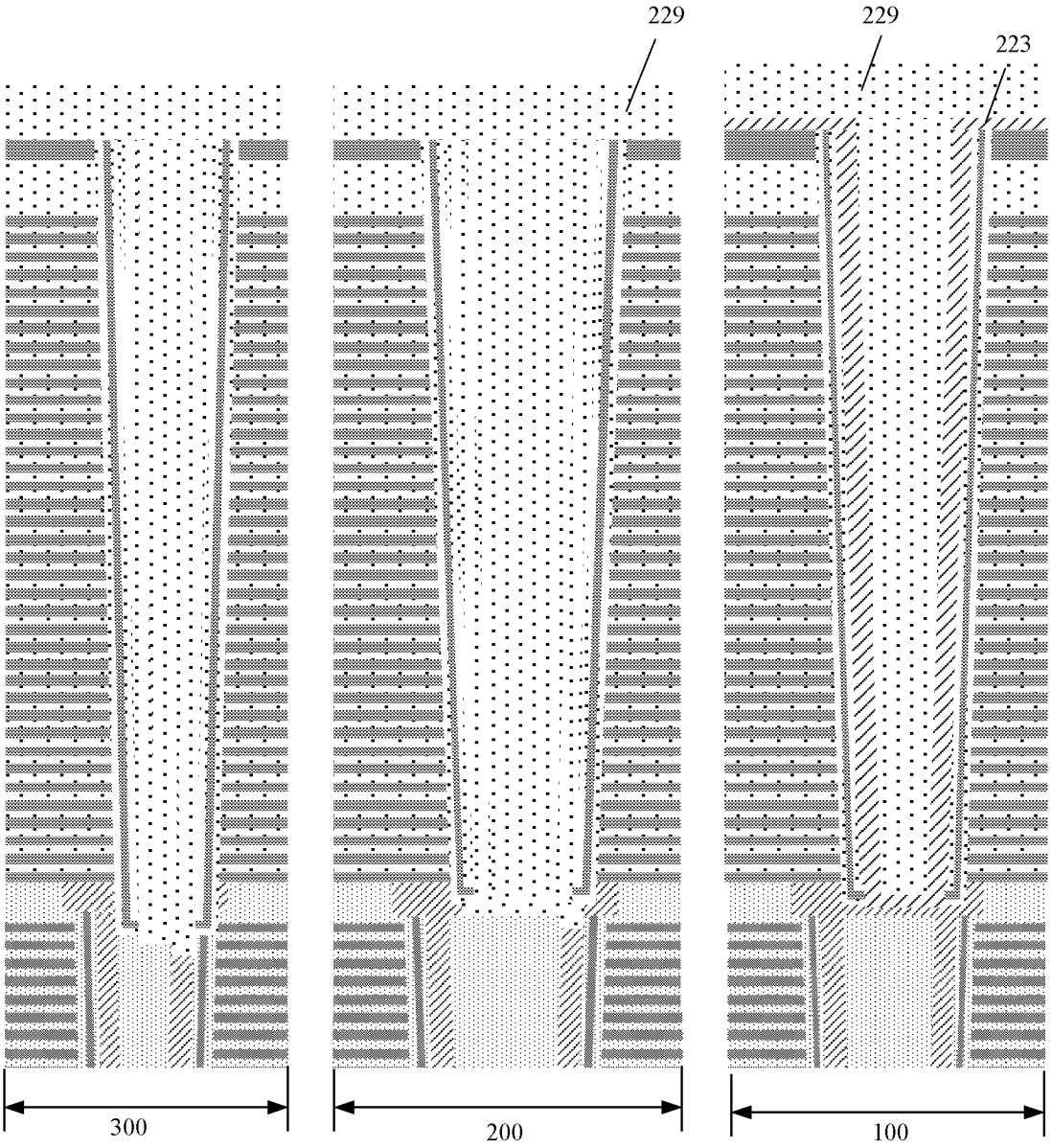


FIG. 45

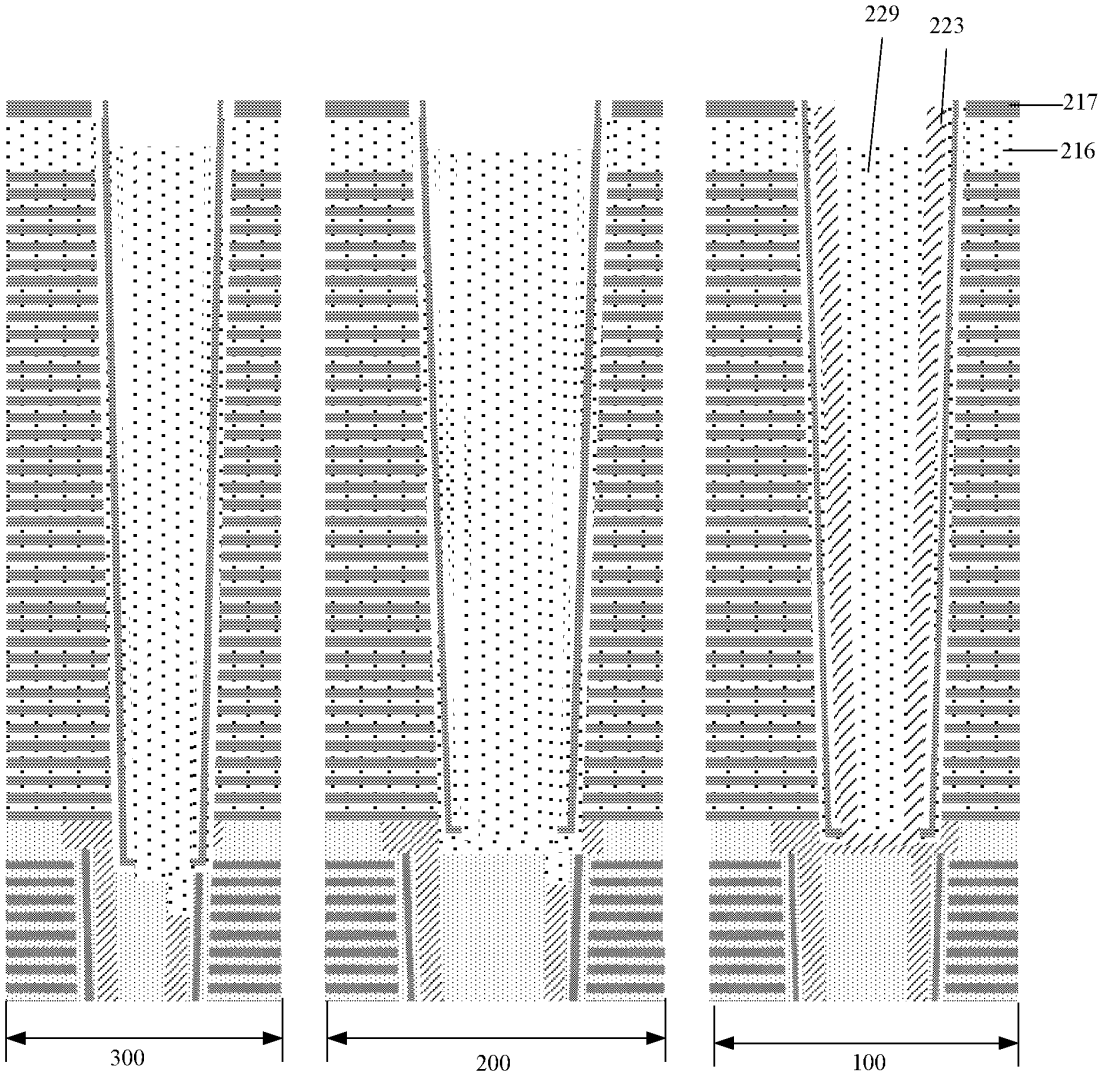


FIG. 46

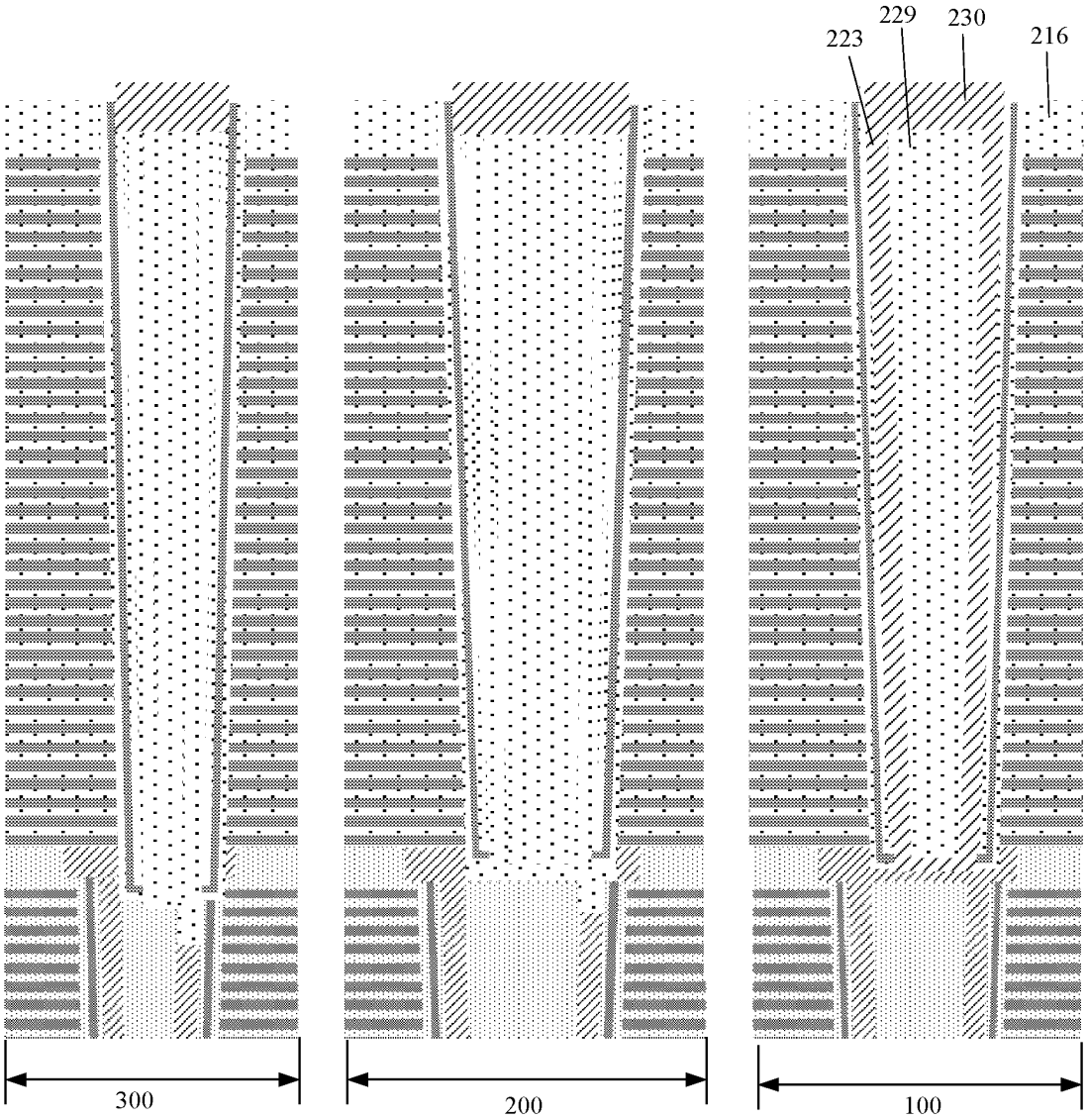


FIG. 47

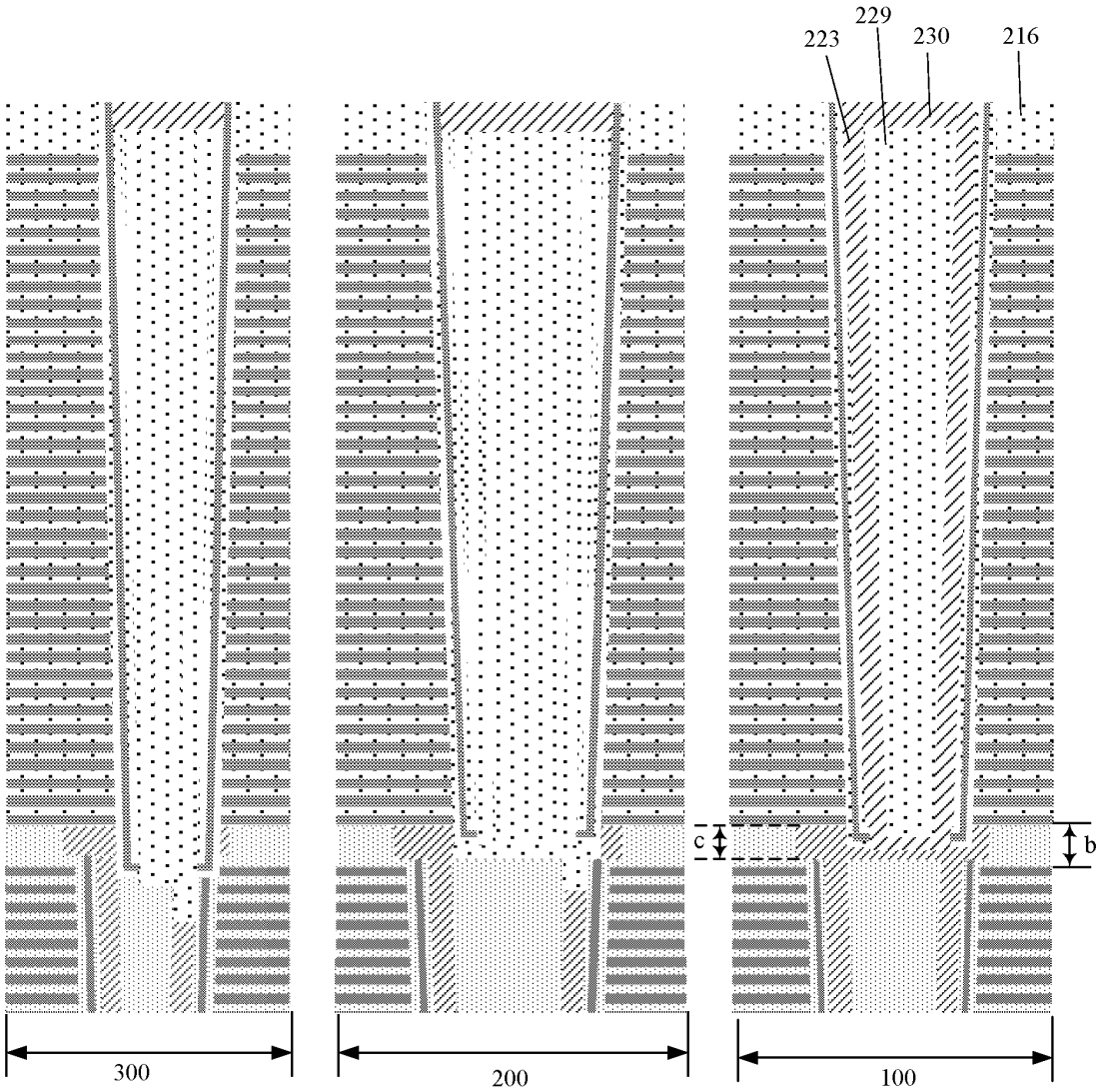


FIG. 48A

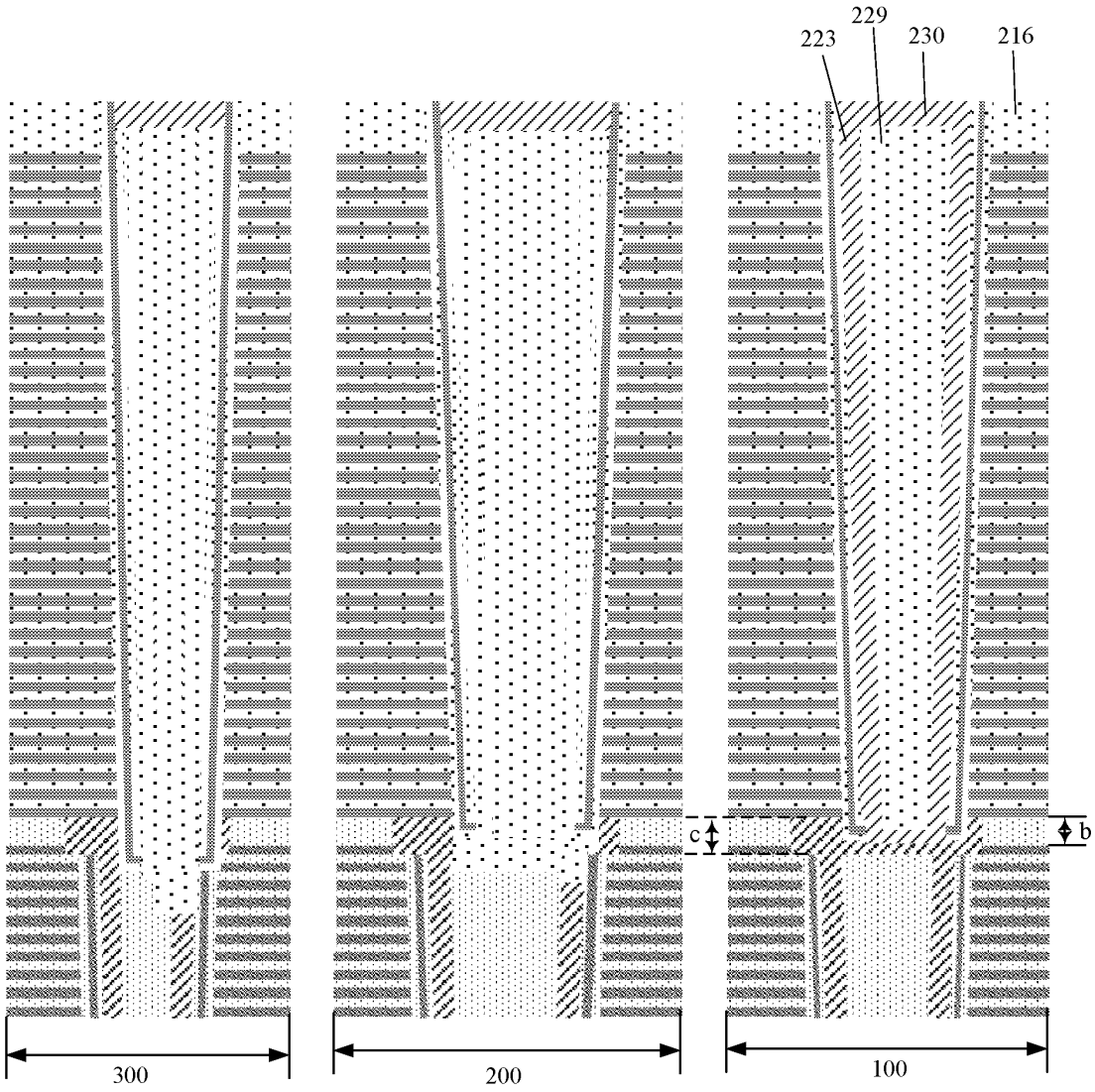


FIG. 48B

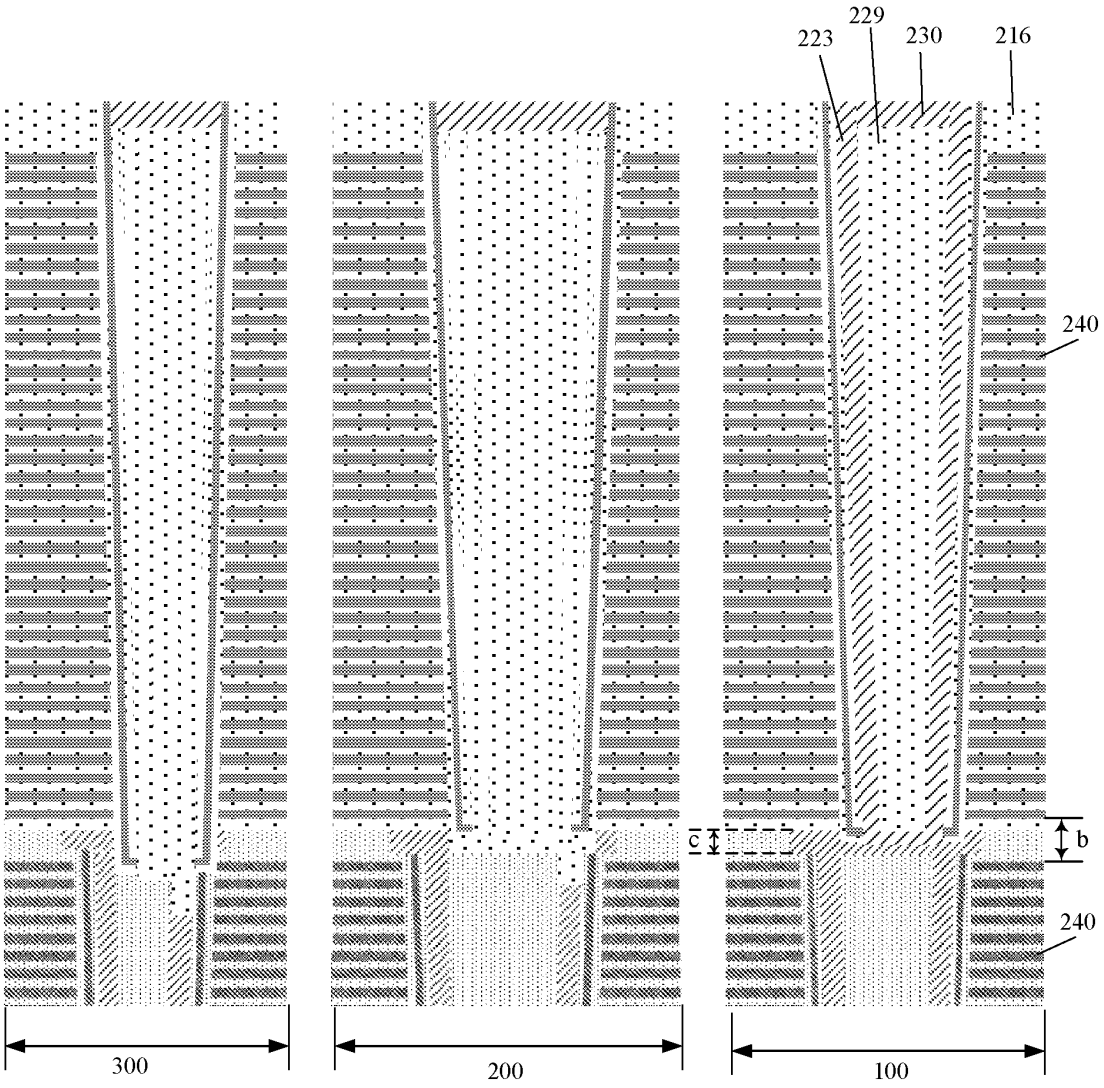


FIG. 49A

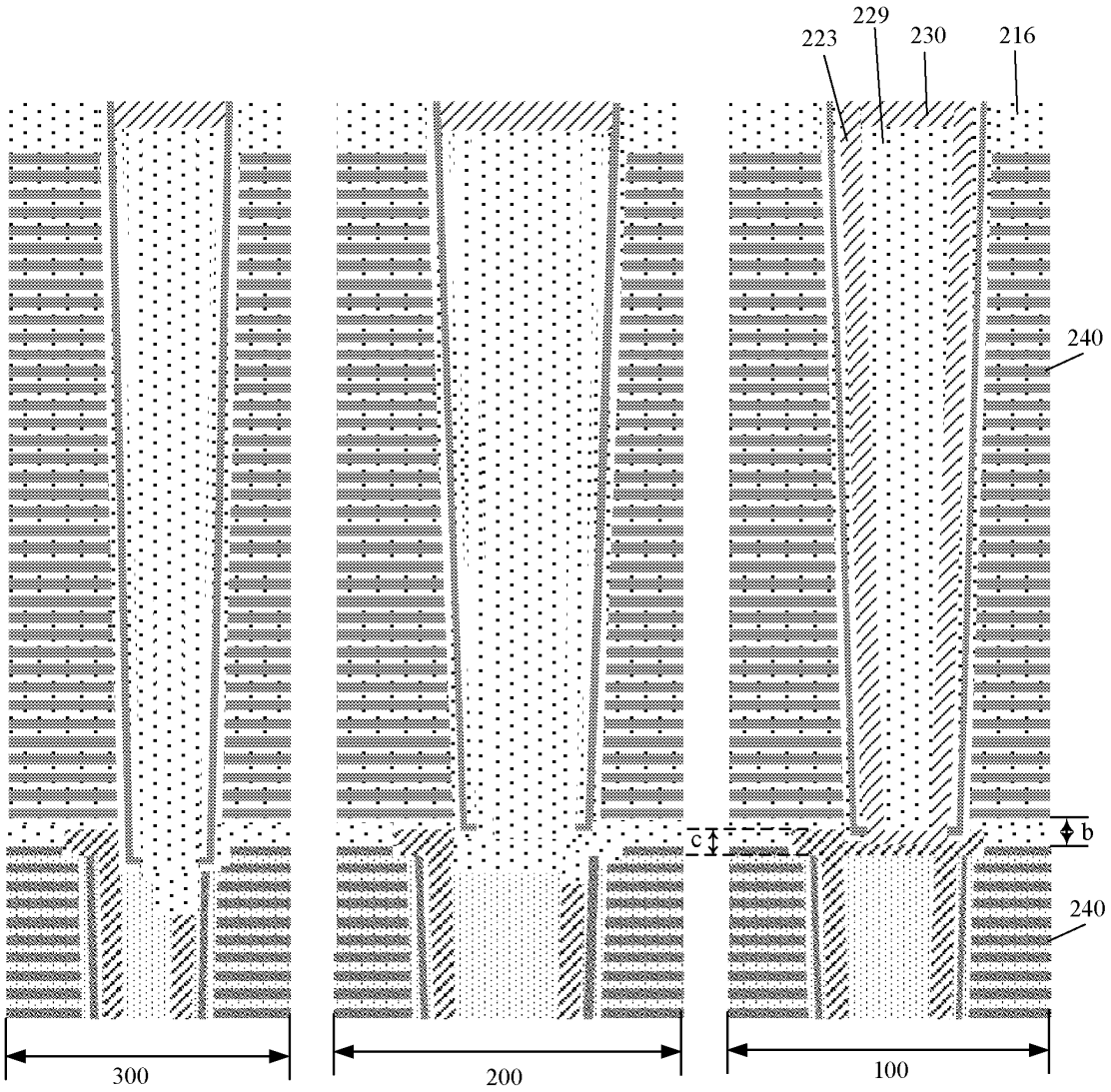


FIG. 49B

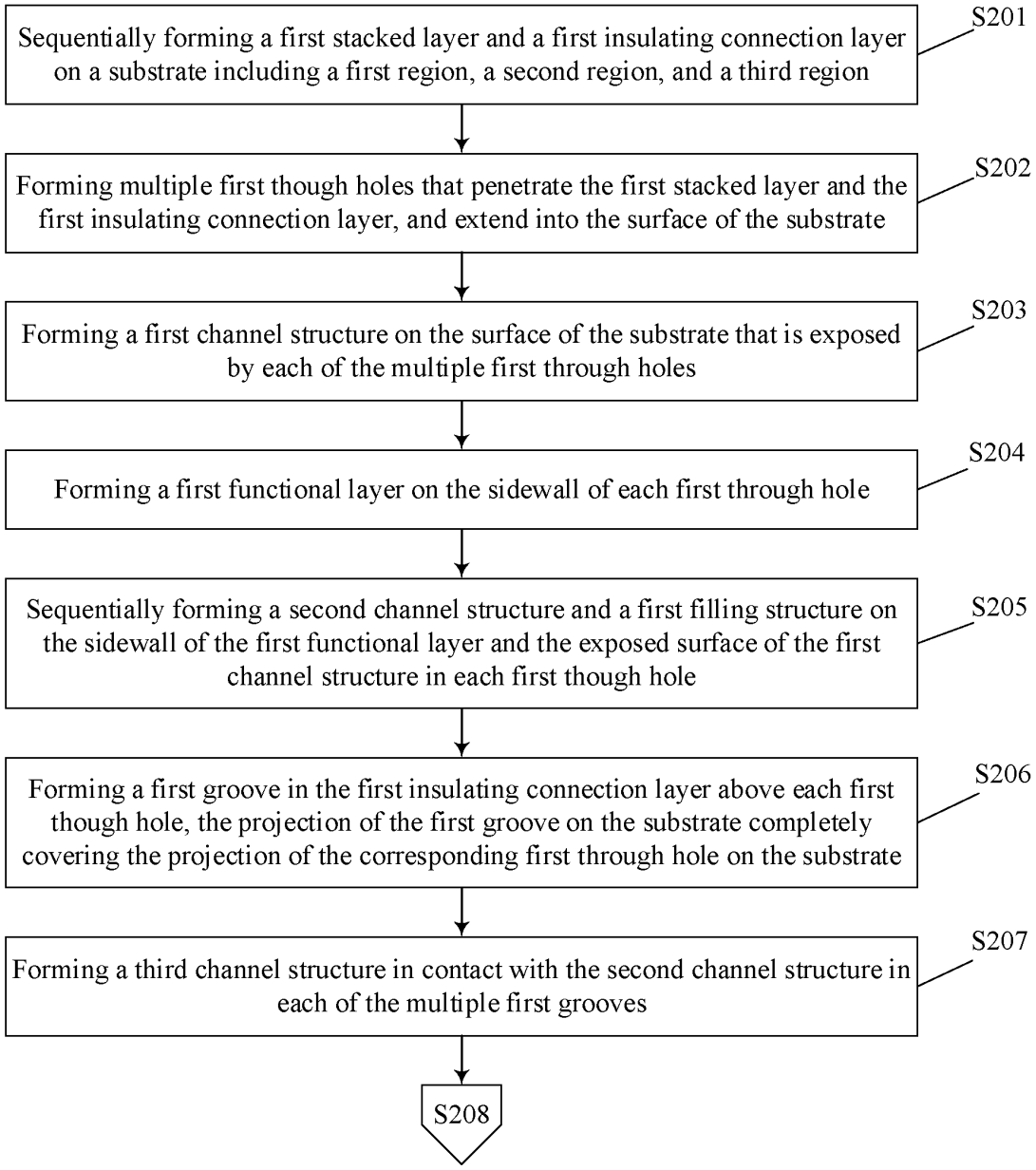

Sequentially forming a first stacked layer and a first insulating connection layer on a substrate including a first region, a second region, and a third region
S201
Forming multiple first though holes that penetrate the first stacked layer and the first insulating connection layer, and extend into the surface of the substrate
S202
Forming a first channel structure on the surface of the substrate that is exposed by each of the multiple first through holes
S203
Forming a first functional layer on the sidewall of each first through hole
S204
Sequentially forming a second channel structure and a first filling structure on the sidewall of the first functional layer and the exposed surface of the first channel structure in each first though hole
S205
Forming a first groove in the first insulating connection layer above each first though hole, the projection of the first groove on the substrate completely covering the projection of the corresponding first through hole on the substrate
S206
Forming a third channel structure in contact with the second channel structure in each of the multiple first grooves
S207
S208

FIG. 50A

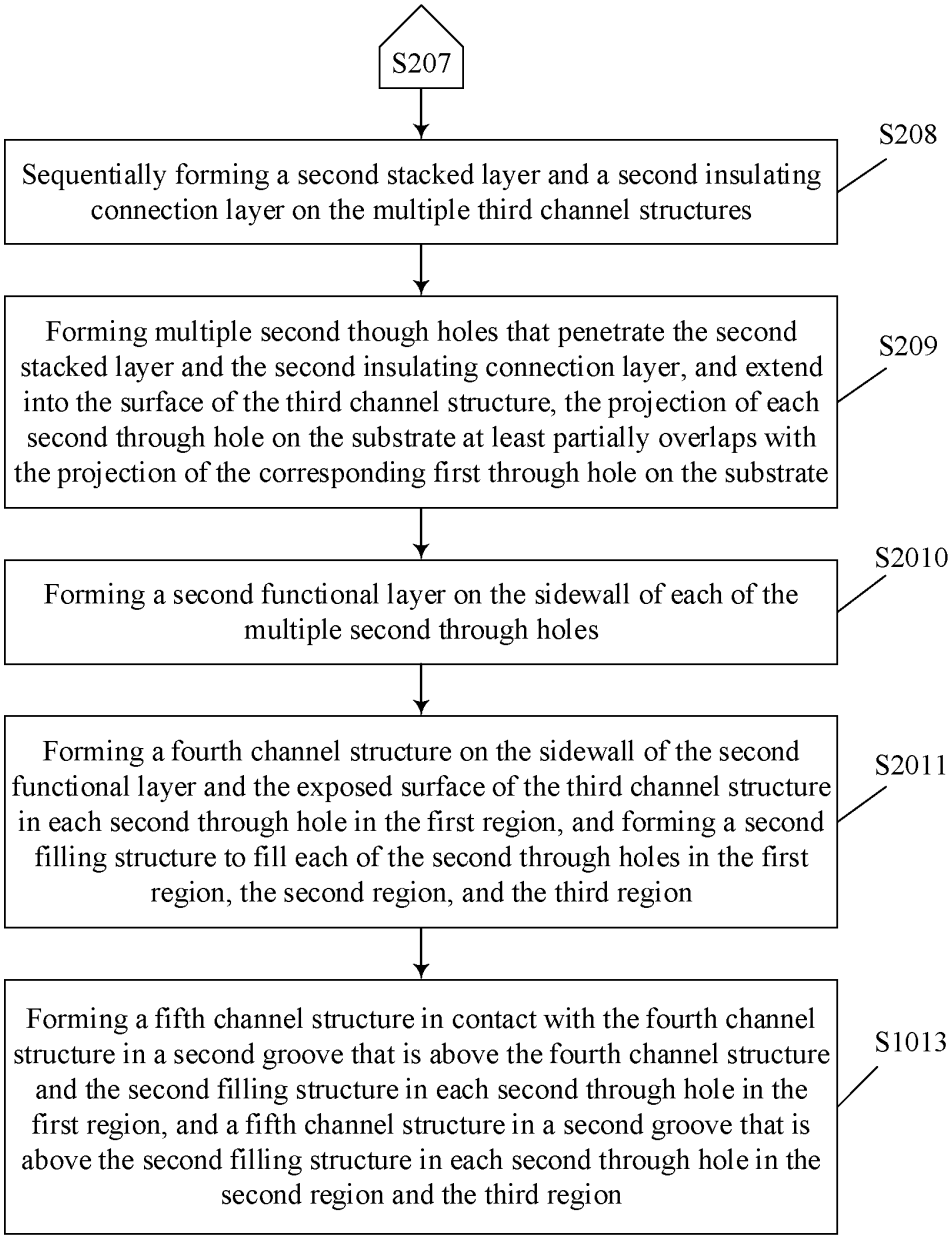

S207
S208
Sequentially forming a second stacked layer and a second insulating connection layer on the multiple third channel structures
S209
Forming multiple second though holes that penetrate the second stacked layer and the second insulating connection layer, and extend into the surface of the third channel structure, the projection of each second through hole on the substrate at least partially overlaps with the projection of the corresponding first through hole on the substrate
S2010
Forming a second functional layer on the sidewall of each of the multiple second through holes
S2011
Forming a fourth channel structure on the sidewall of the second functional layer and the exposed surface of the third channel structure in each second through hole in the first region, and forming a second filling structure to fill each of the second through holes in the first region, the second region, and the third region
S1013
Forming a fifth channel structure in contact with the fourth channel structure in a second groove that is above the fourth channel structure and the second filling structure in each second through hole in the first region, and a fifth channel structure in a second groove that is above the second filling structure in each second through hole in the second region and the third region

FIG. 50B

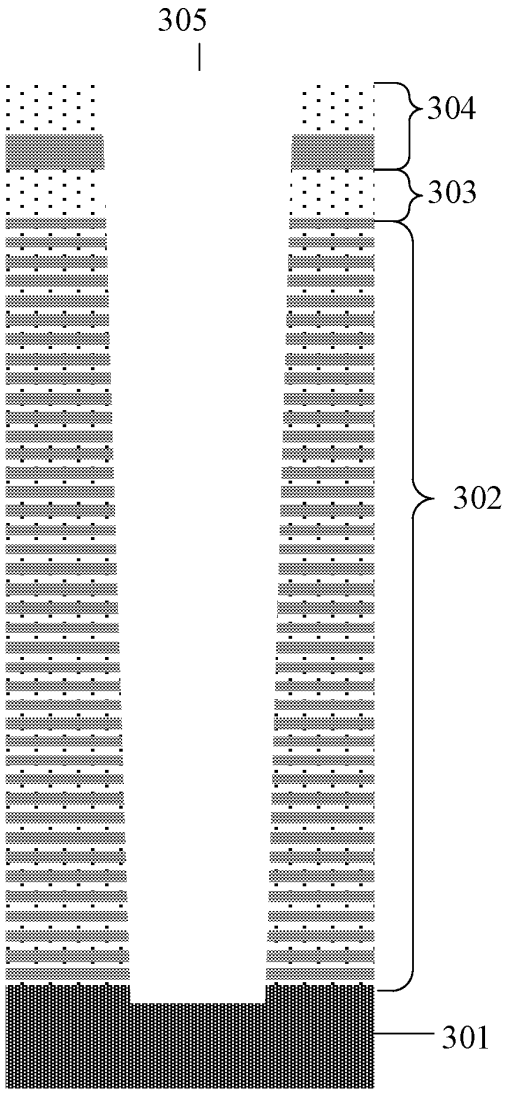


FIG. 51

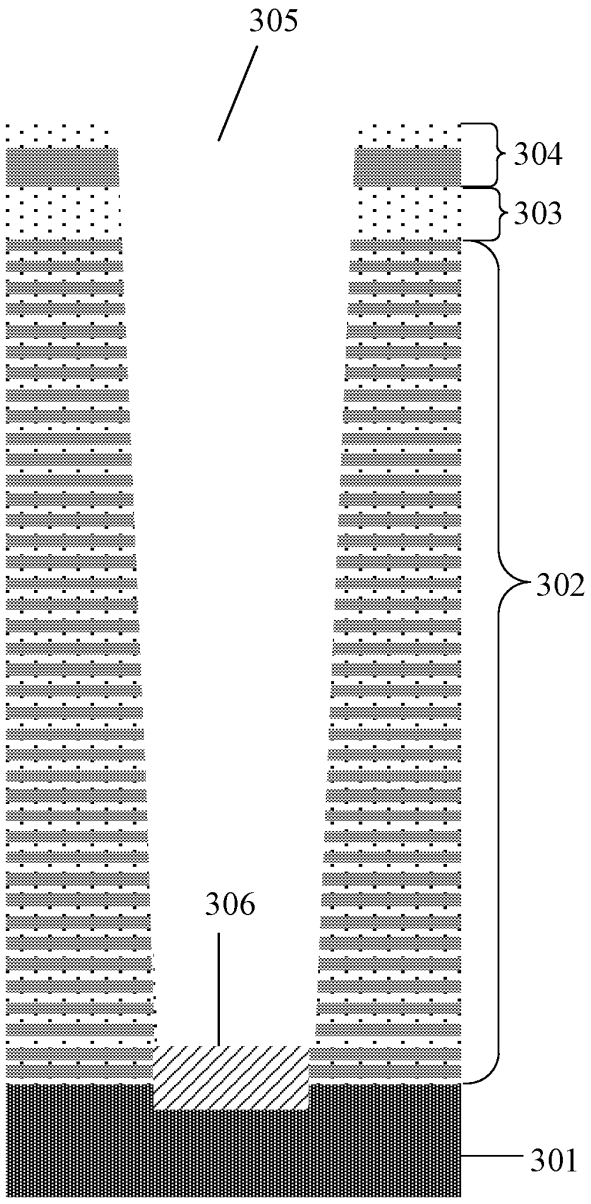


FIG. 52

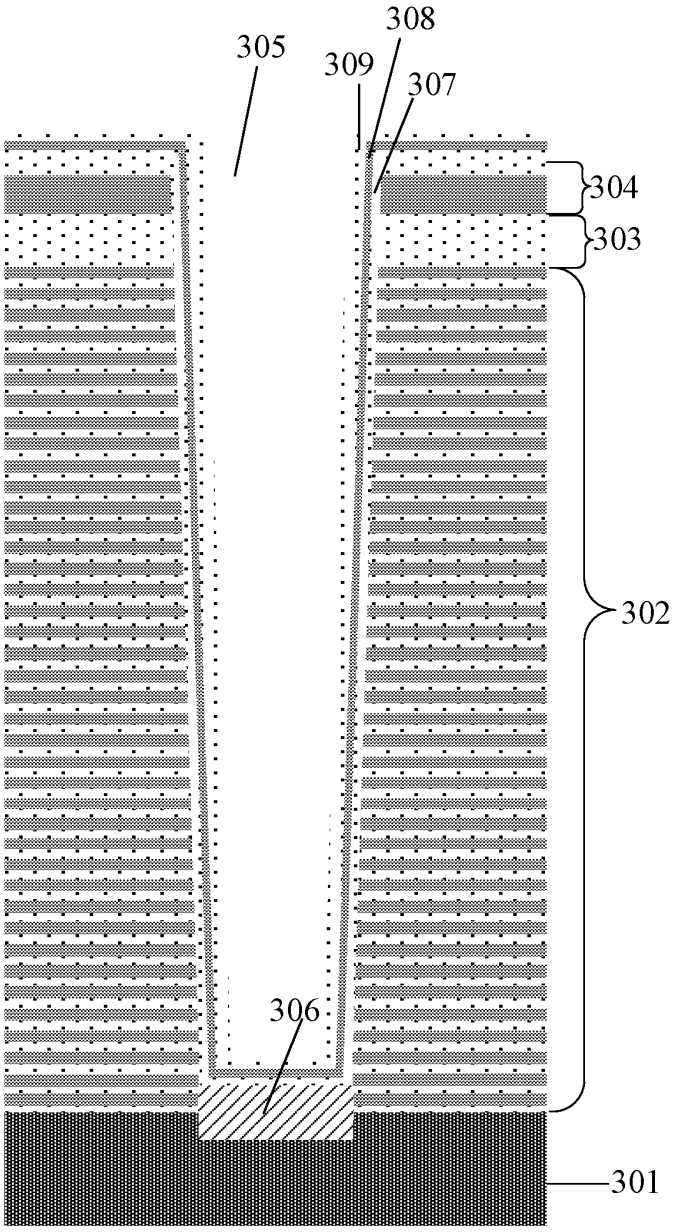


FIG. 53

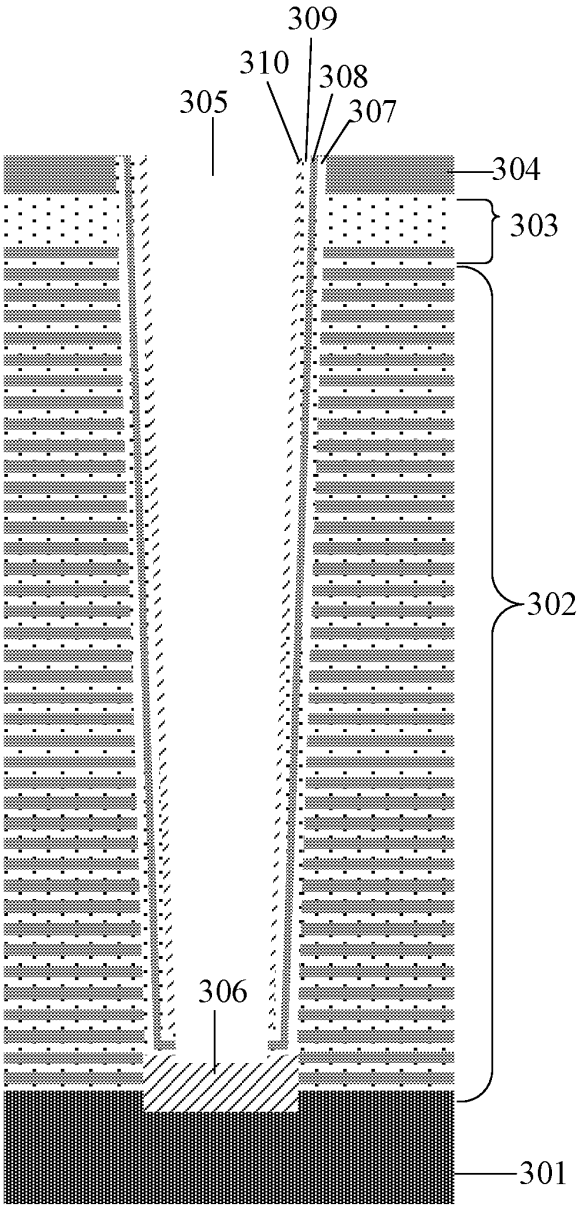


FIG. 54

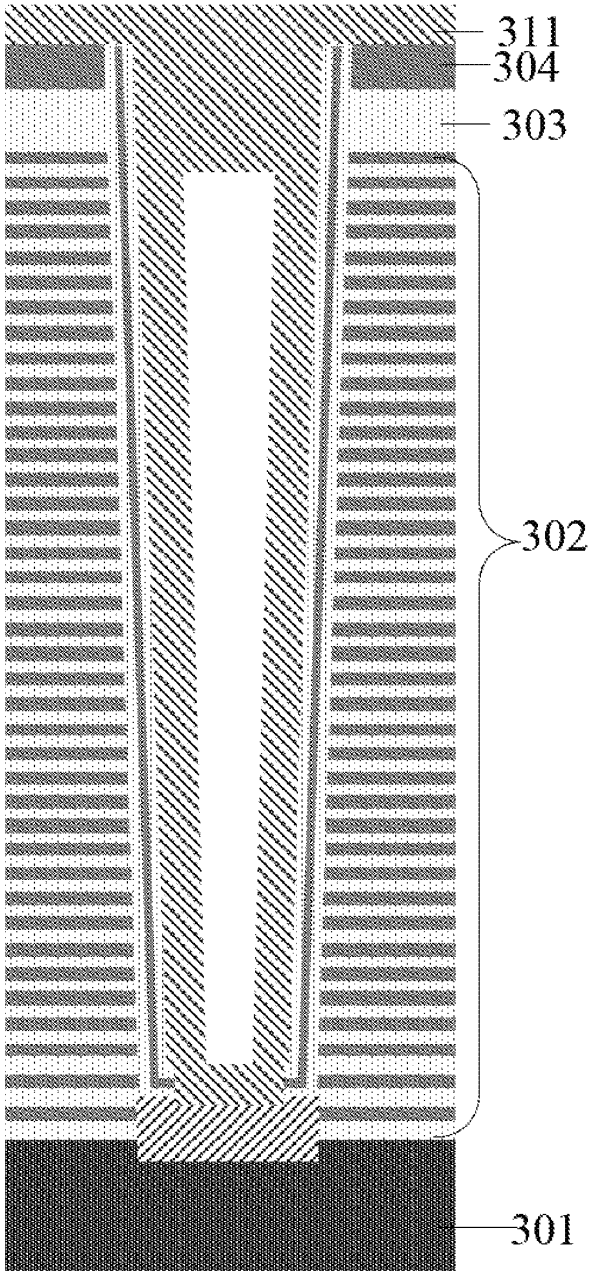


FIG. 55

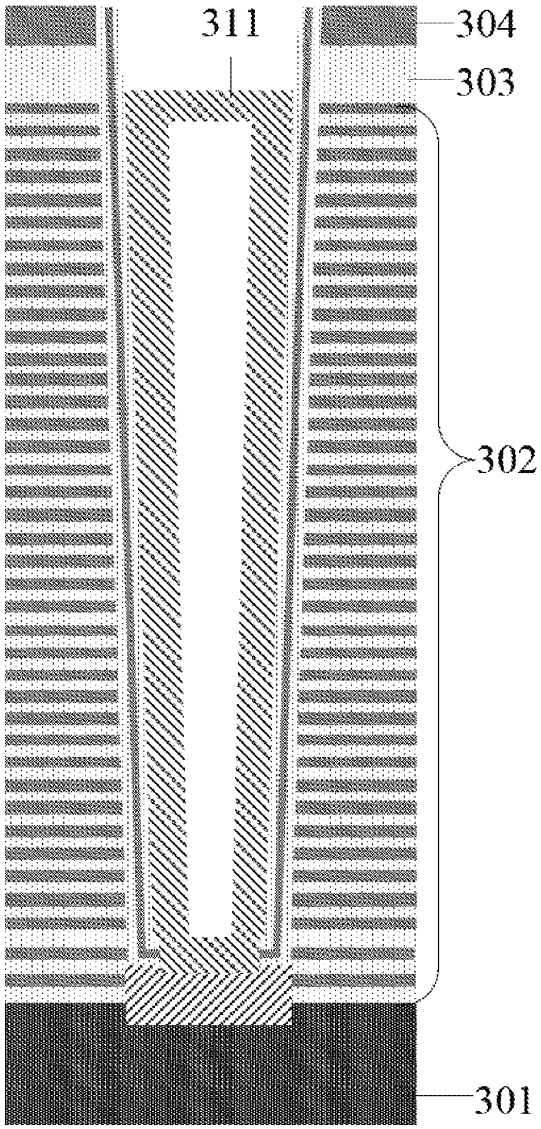


FIG. 56A

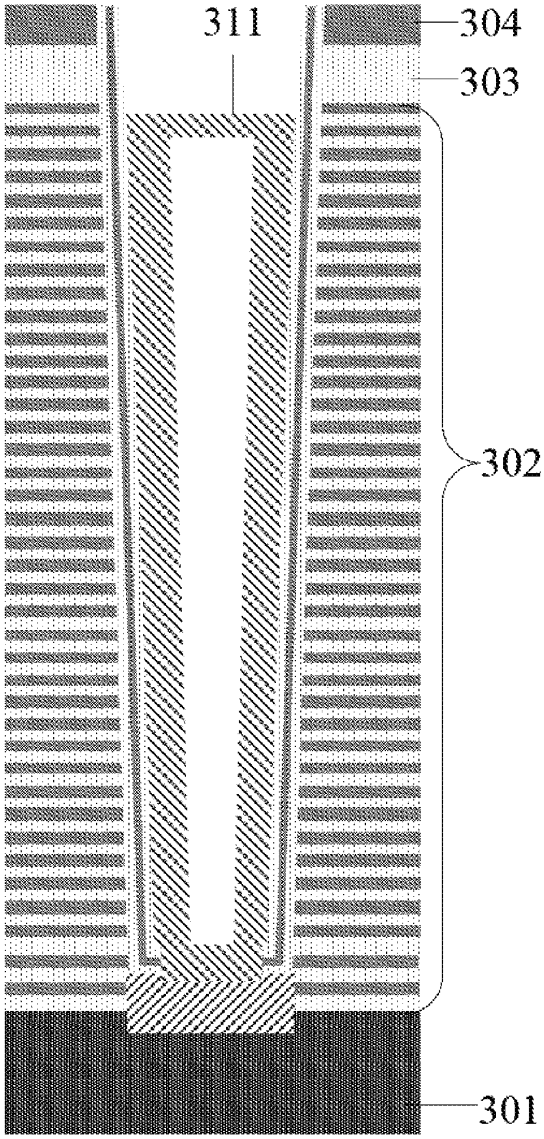


FIG. 56B

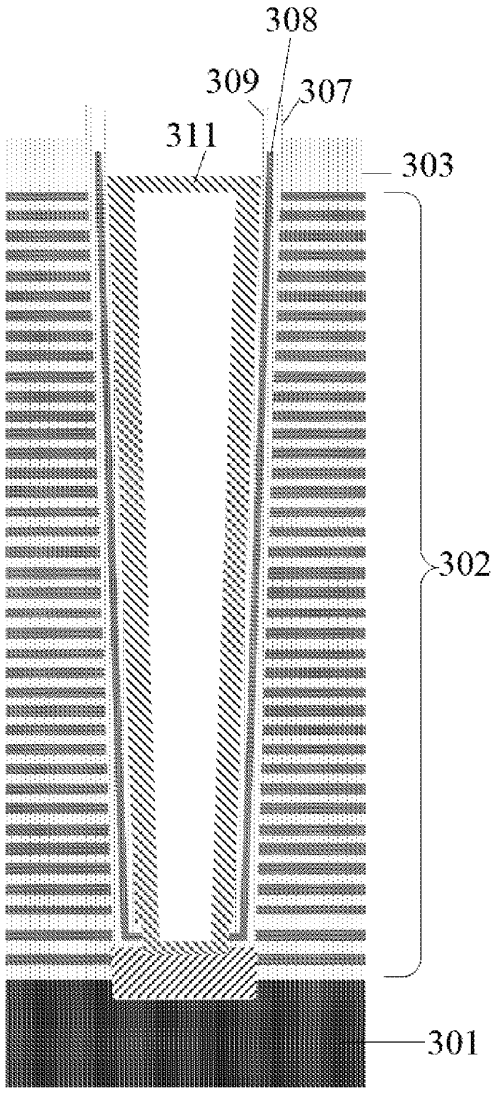


FIG. 57A

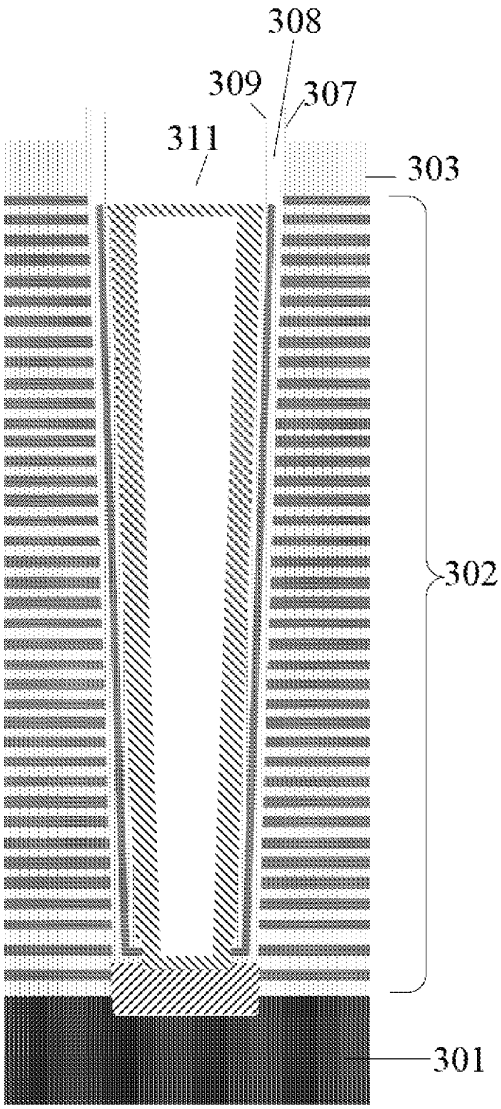


FIG. 57B

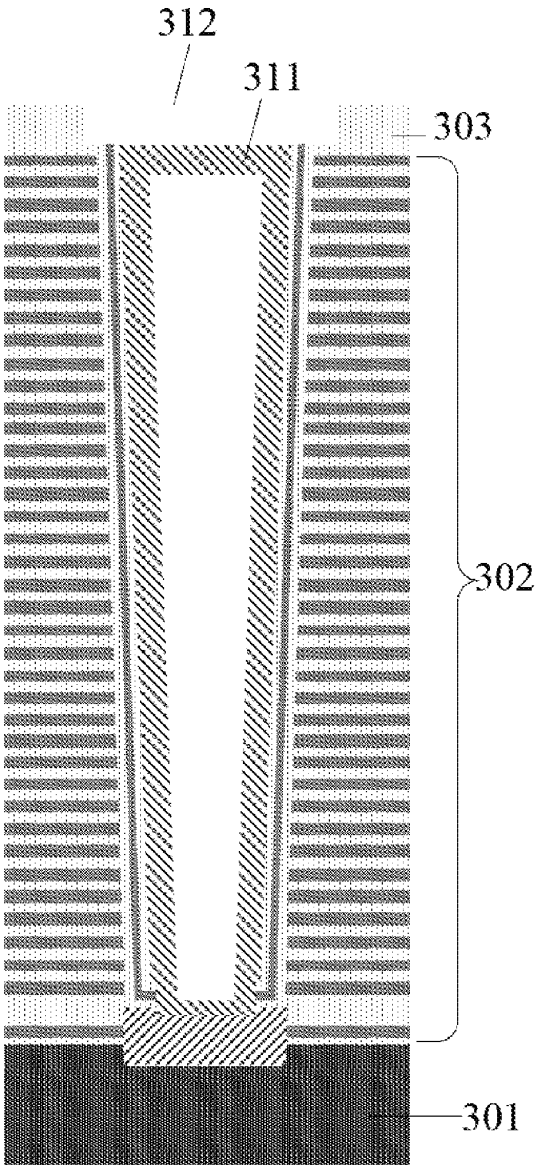


FIG. 58A

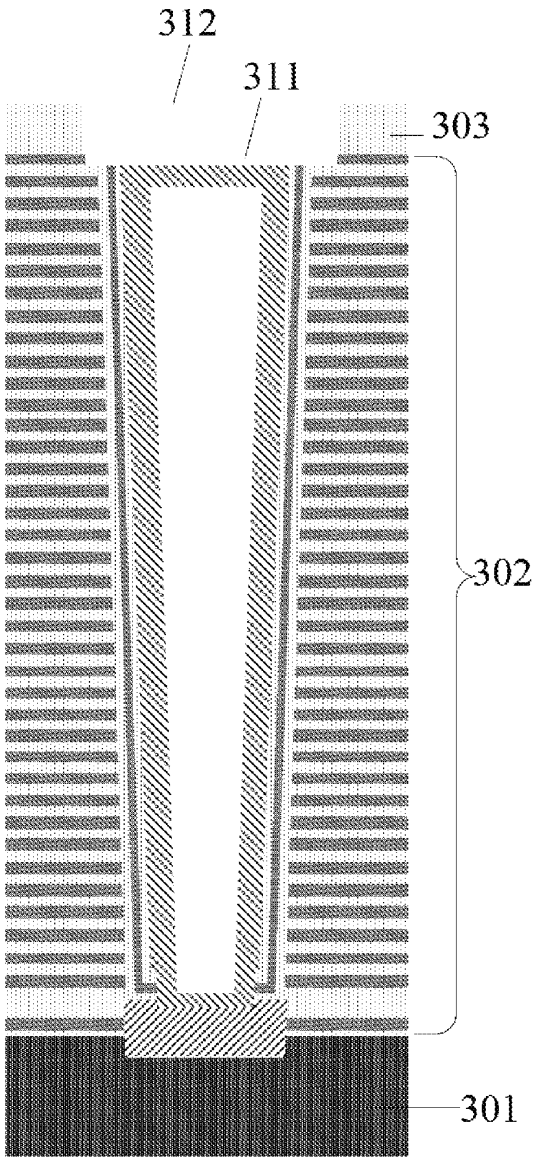


FIG. 58B

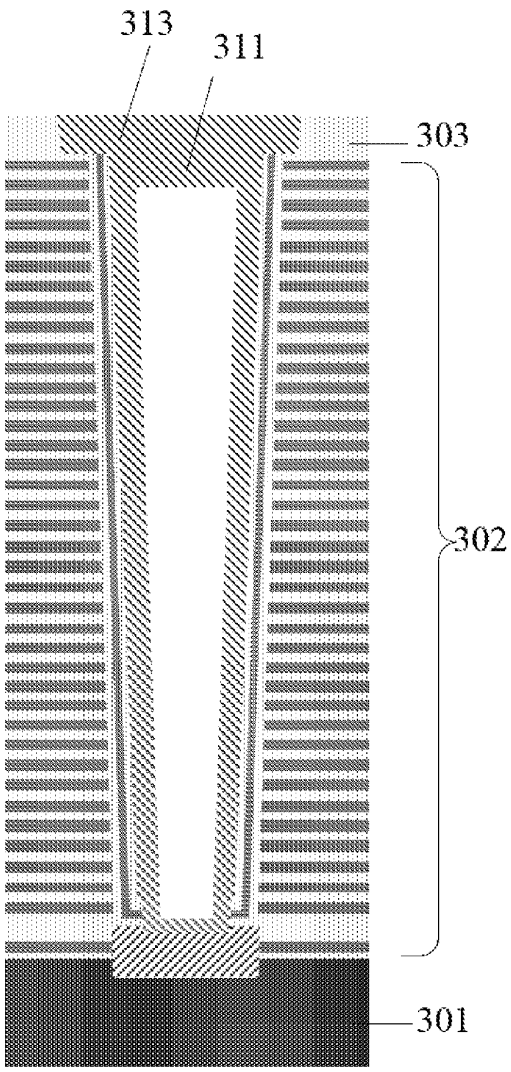


FIG. 59A

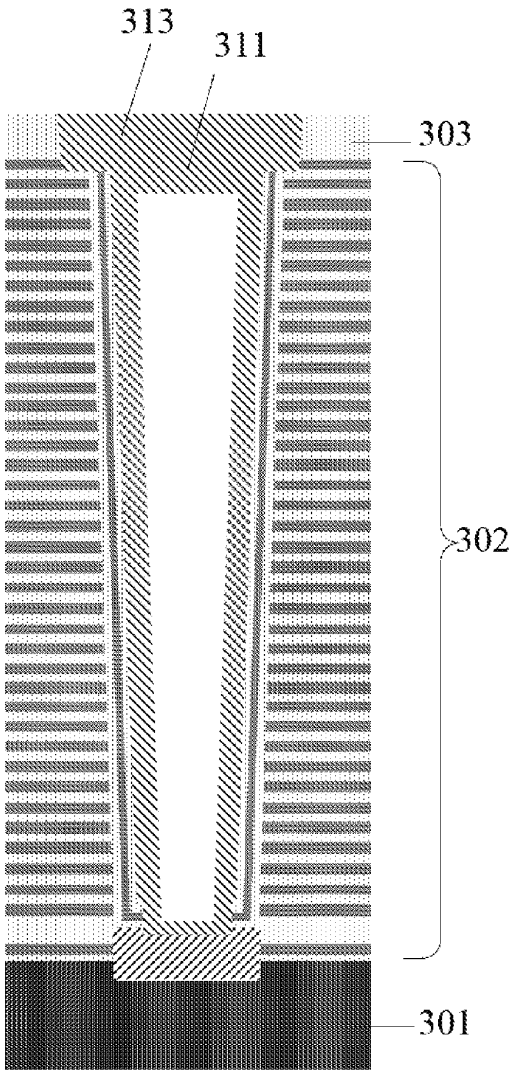


FIG. 59B

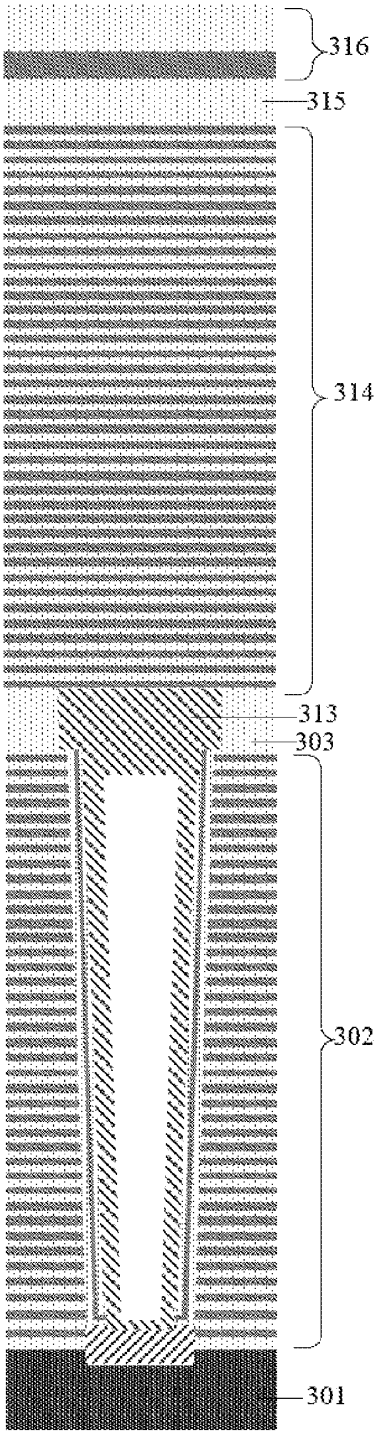


FIG. 60

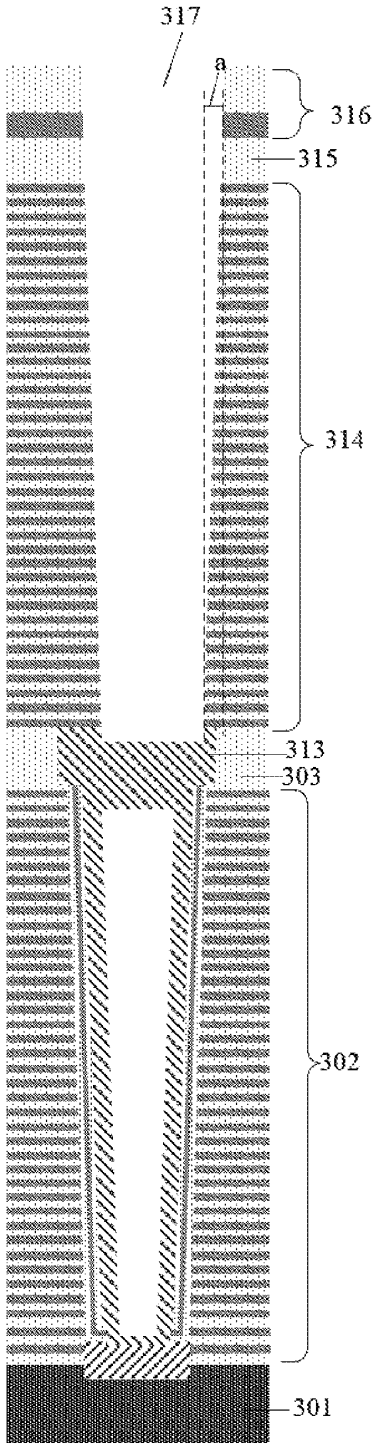


FIG. 61

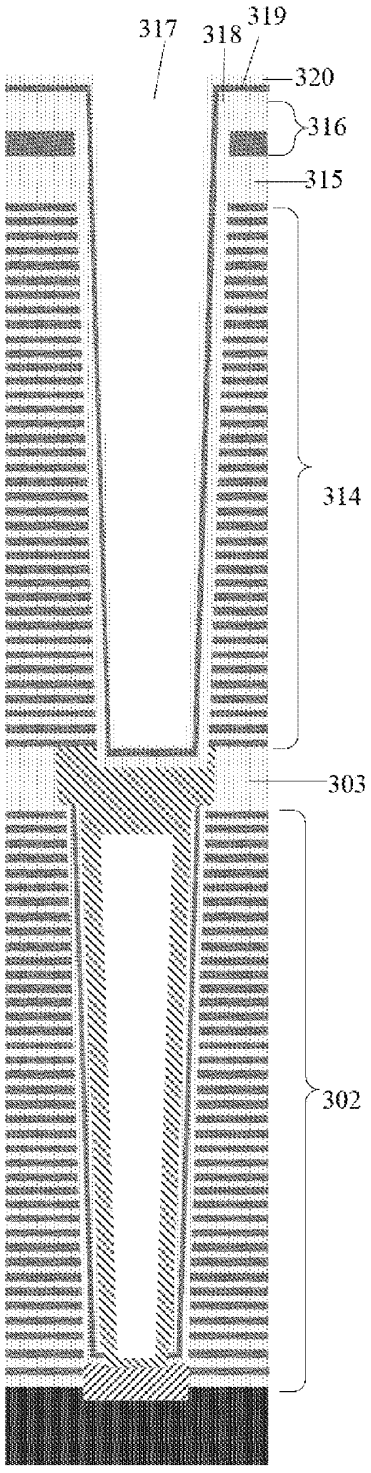


FIG. 62

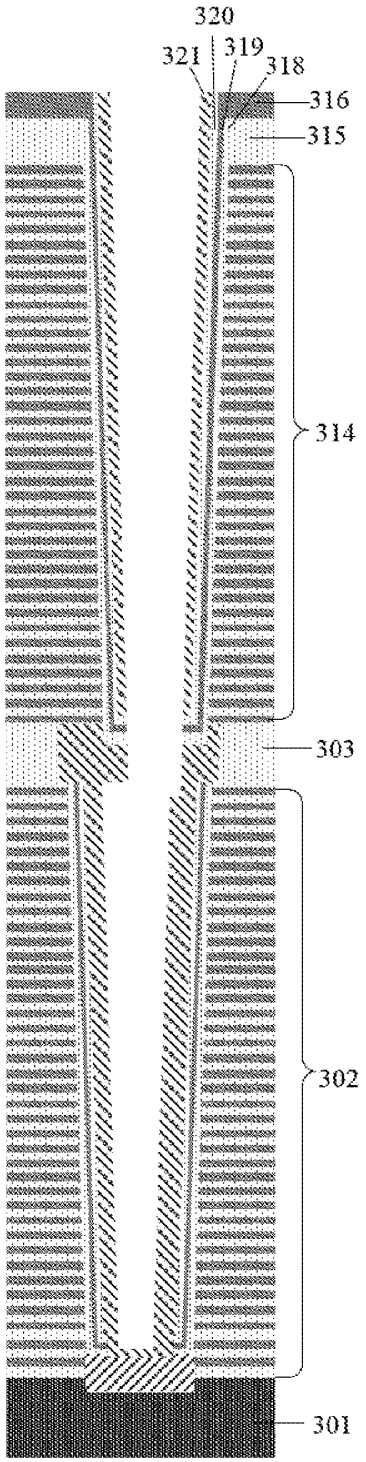


FIG. 63

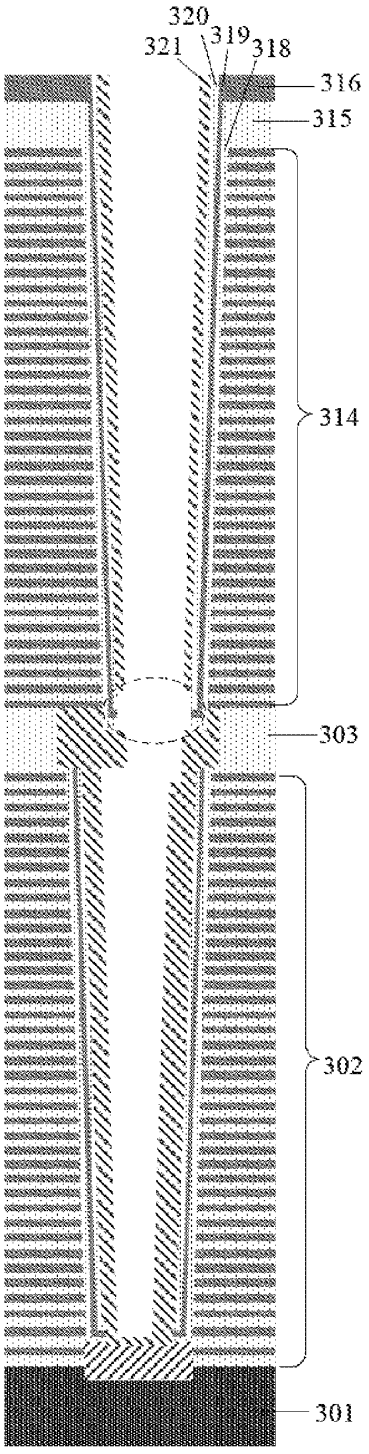


FIG. 64

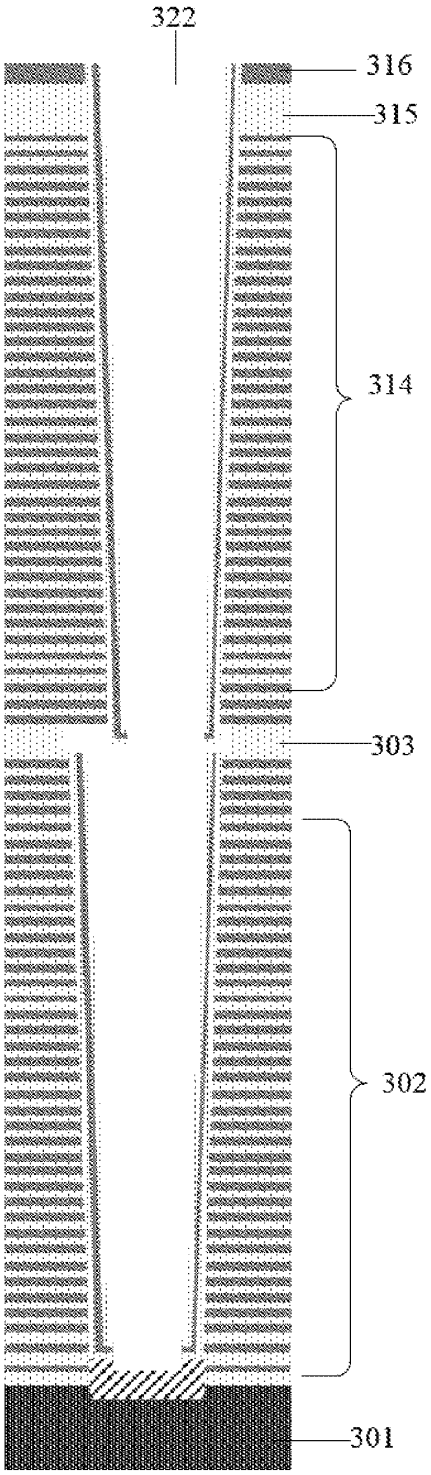


FIG. 65

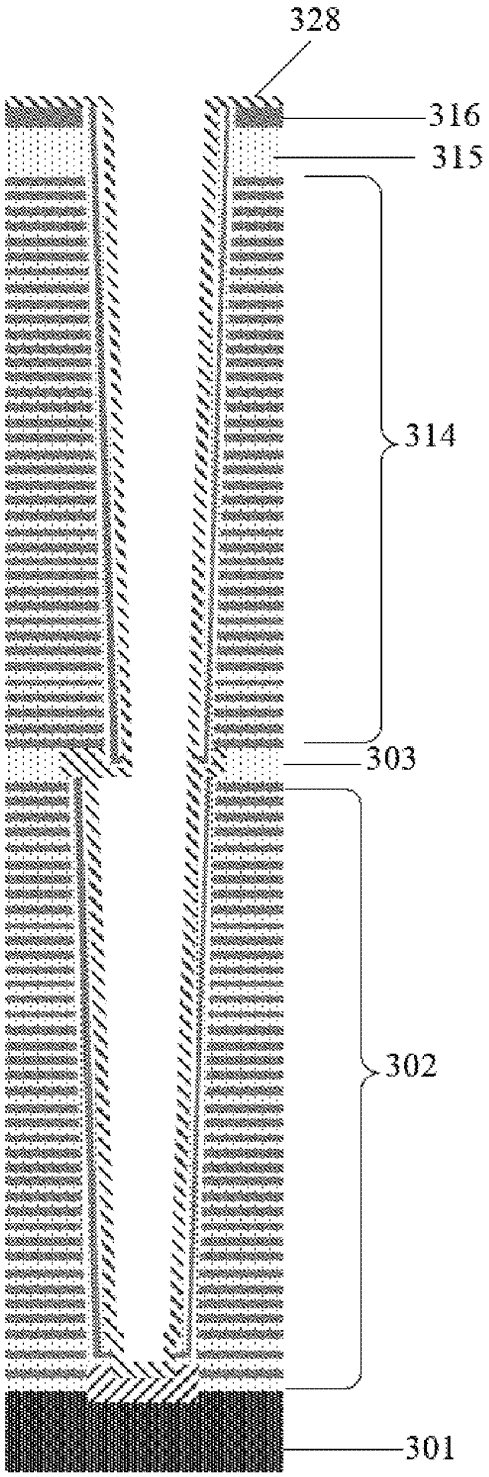


FIG. 66

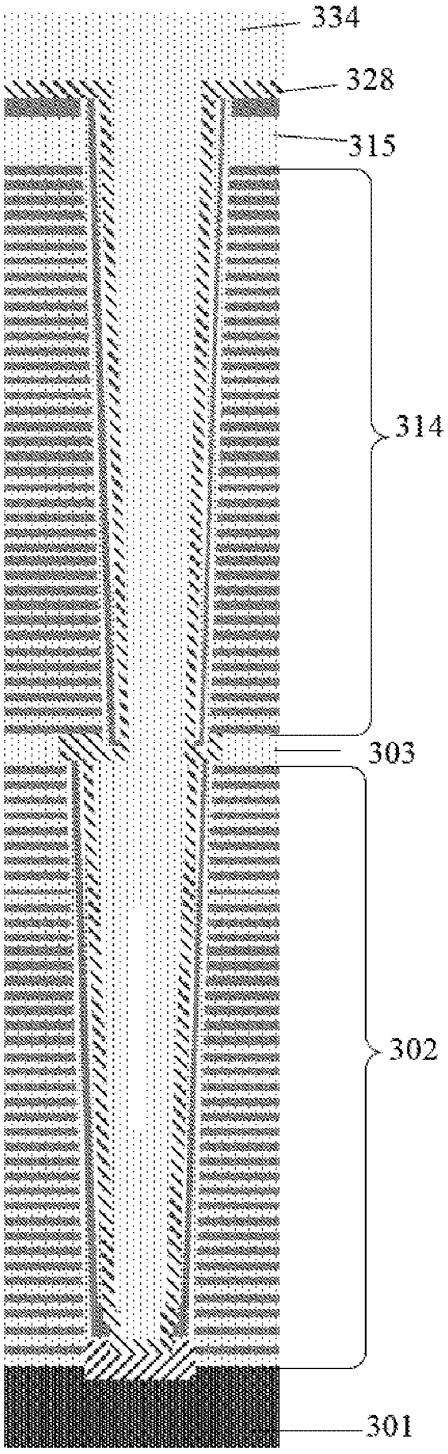


FIG. 67

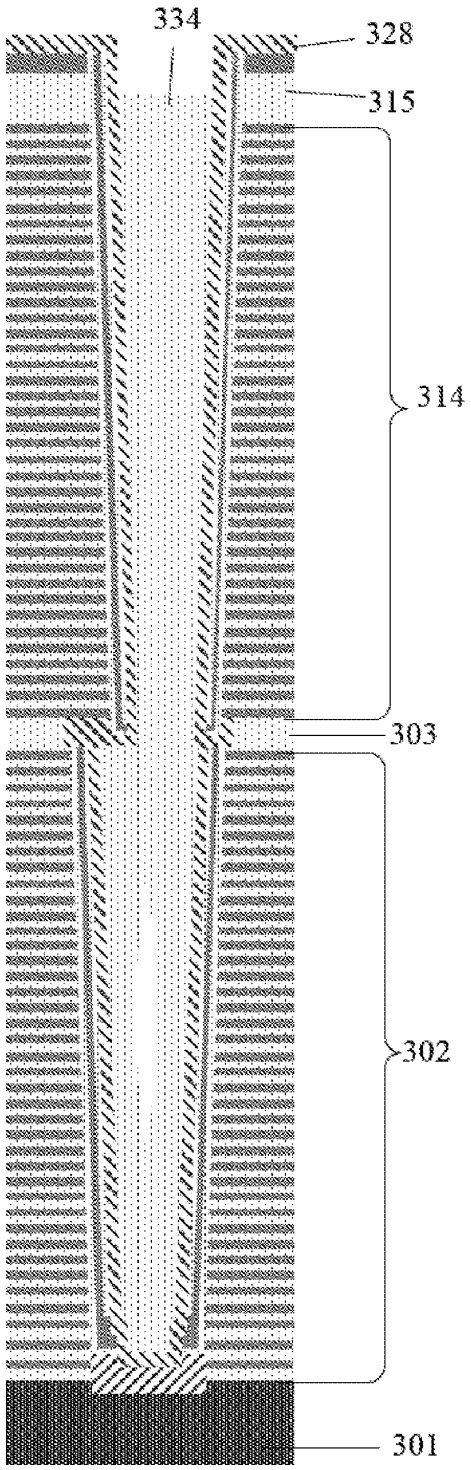


FIG. 68

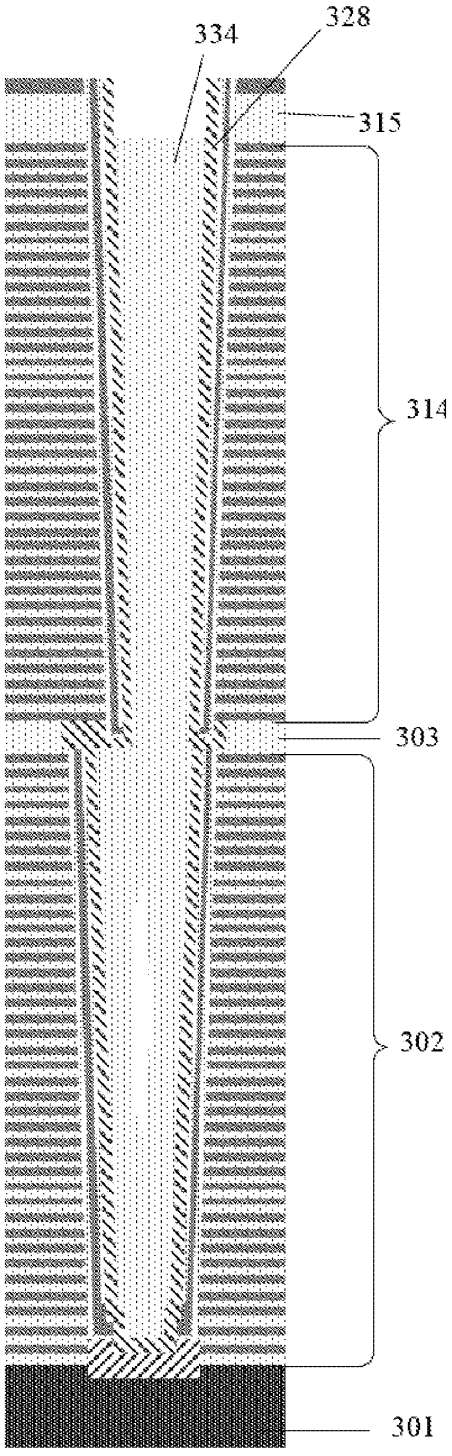


FIG. 69

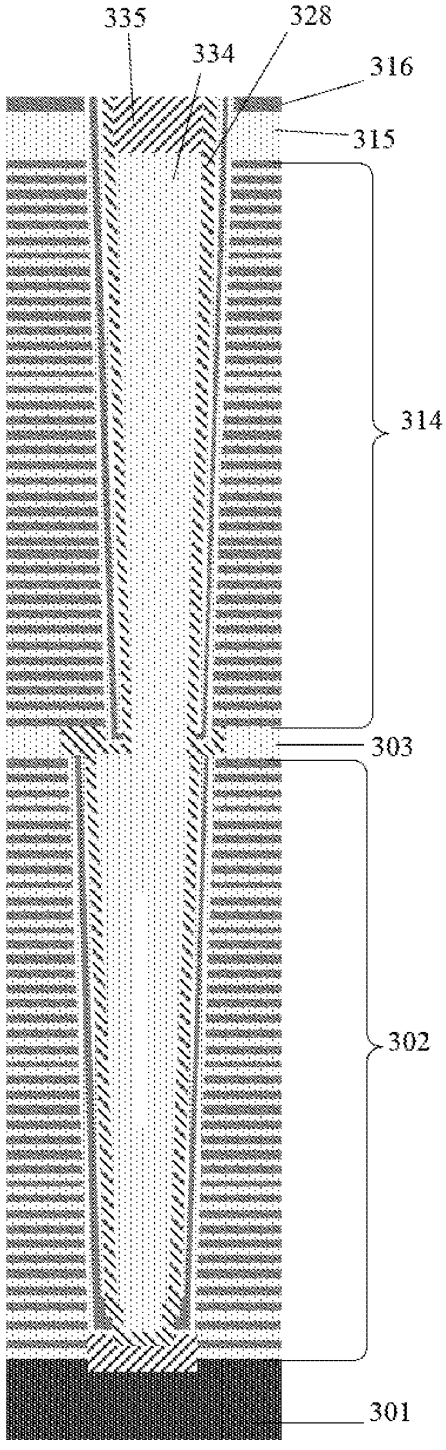


FIG. 70

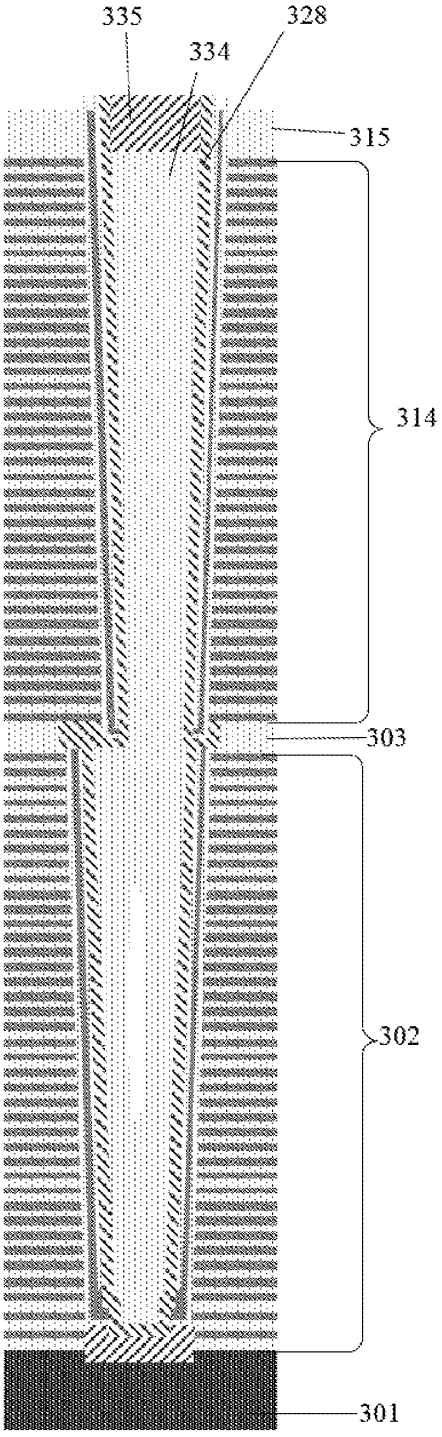


FIG. 71

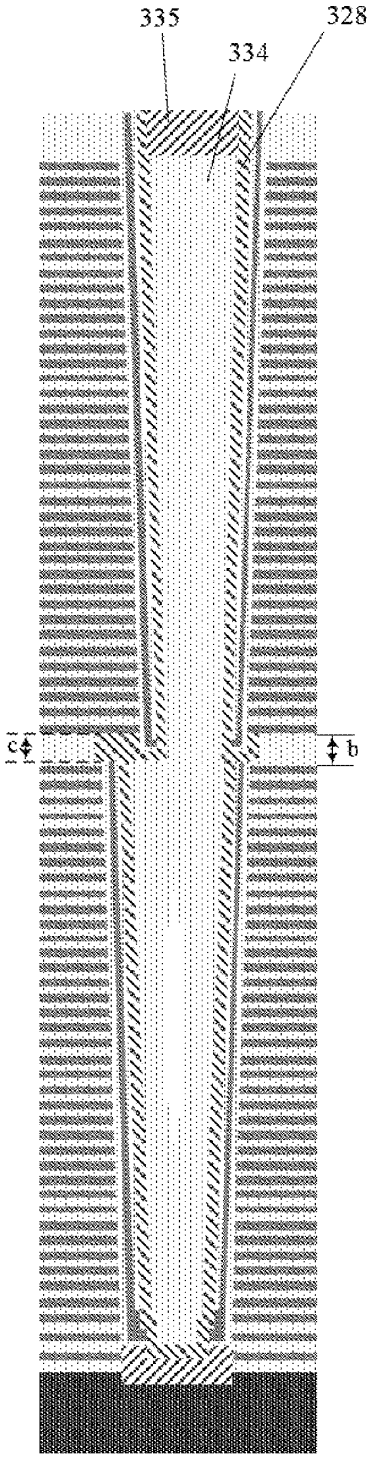


FIG. 72A

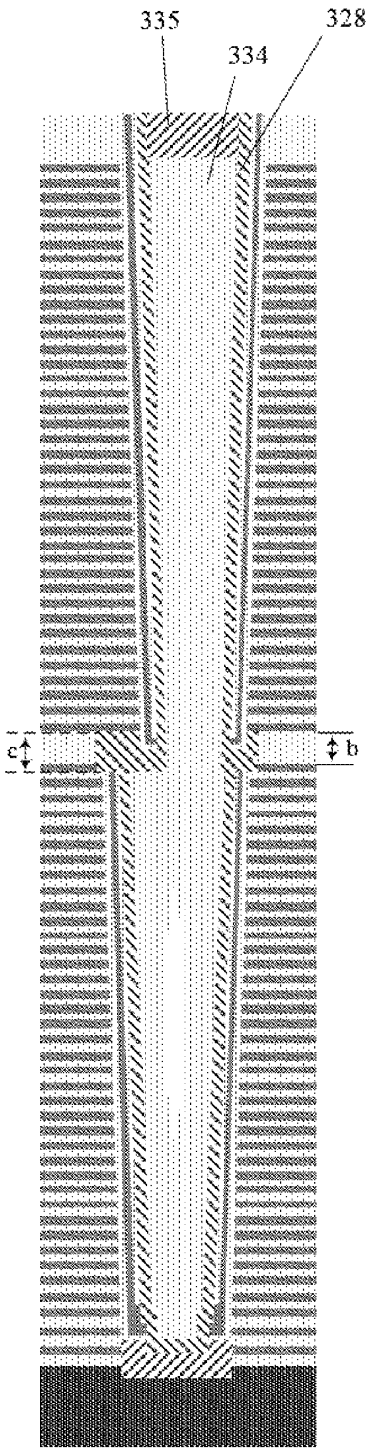


FIG. 72B

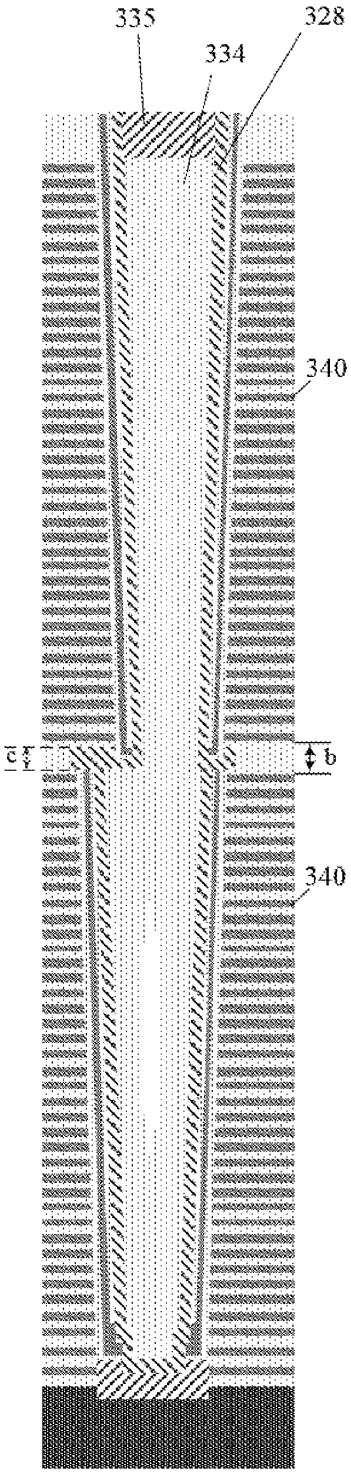


FIG. 73A

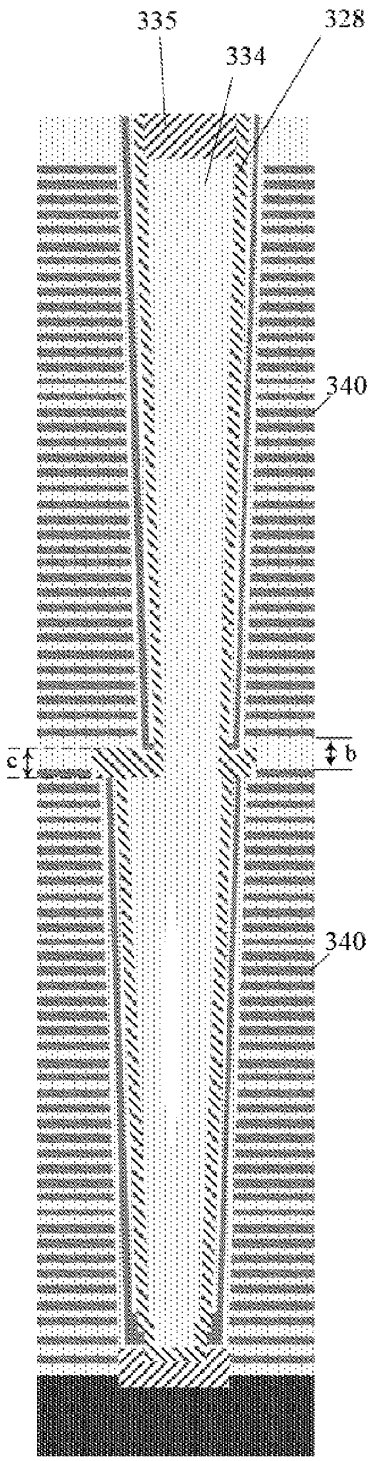


FIG. 73B

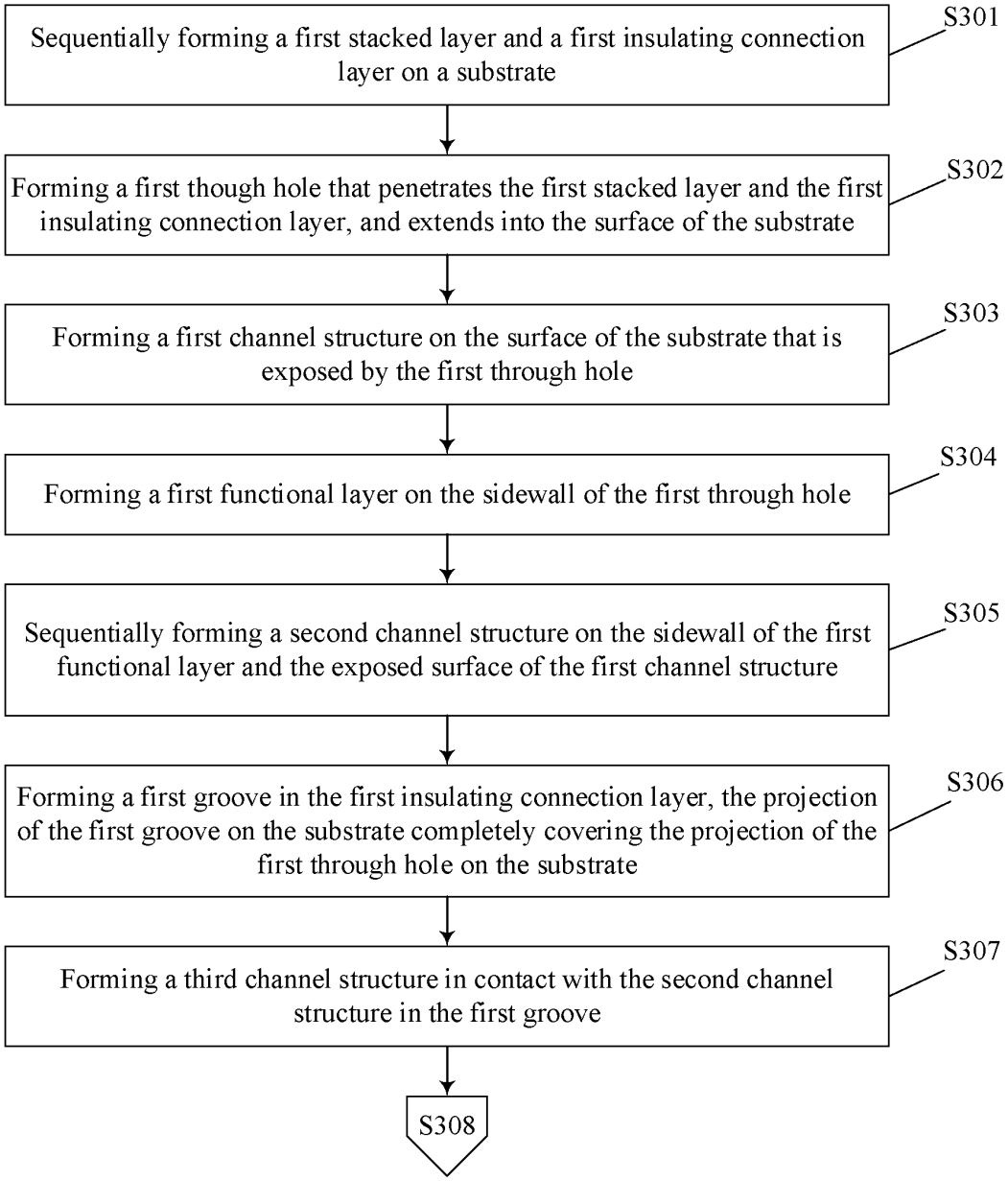

Sequentially forming a first stacked layer and a first insulating connection layer on a substrate
S301
Forming a first though hole that penetrates the first stacked layer and the first insulating connection layer, and extends into the surface of the substrate
S302
Forming a first channel structure on the surface of the substrate that is exposed by the first through hole
S303
Forming a first functional layer on the sidewall of the first through hole
S304
Sequentially forming a second channel structure on the sidewall of the first functional layer and the exposed surface of the first channel structure
S305
Forming a first groove in the first insulating connection layer, the projection of the first groove on the substrate completely covering the projection of the first through hole on the substrate
S306
Forming a third channel structure in contact with the second channel structure in the first groove
S307
S308

FIG. 74A

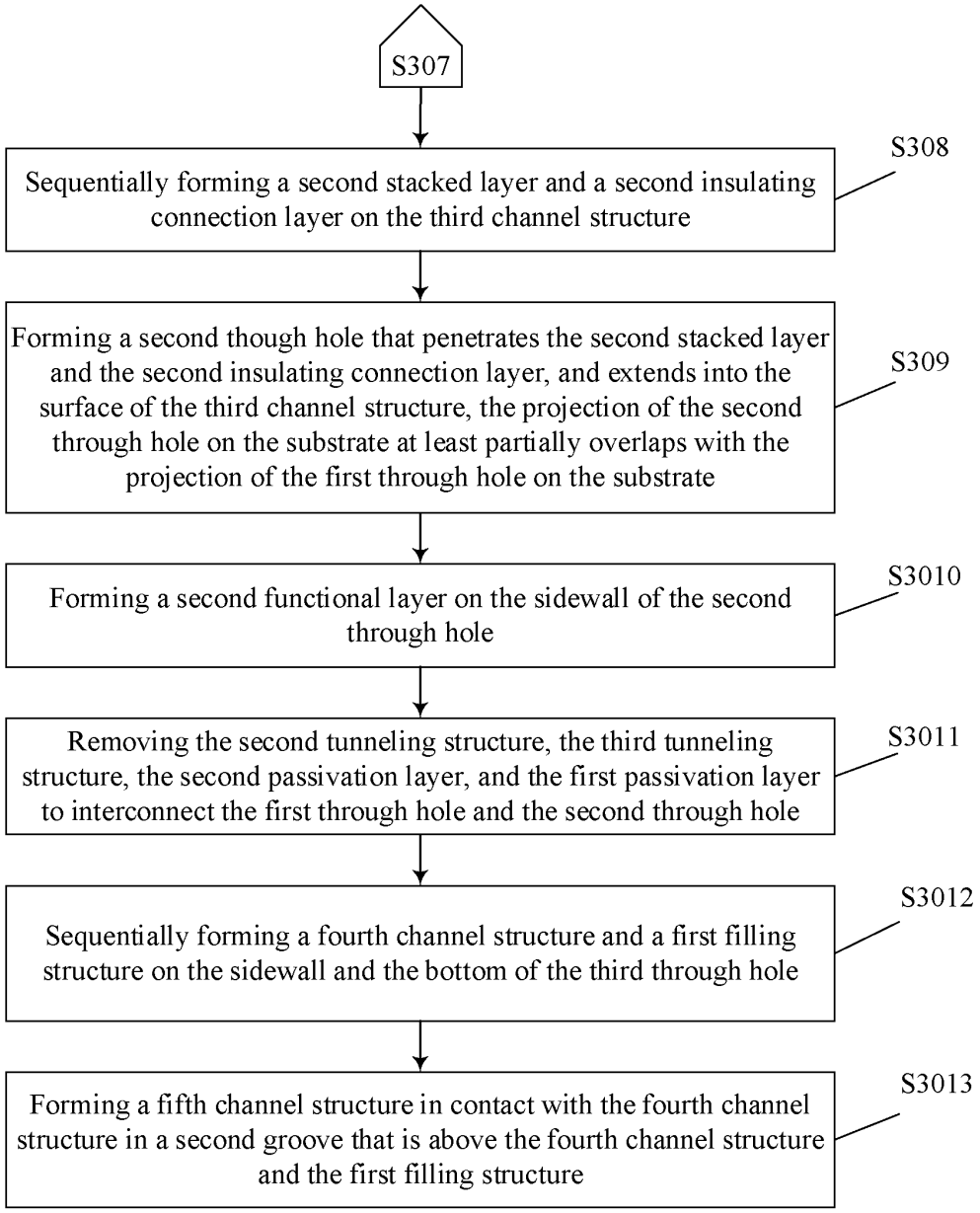

S307
Sequentially forming a second stacked layer and a second insulating connection layer on the third channel structure
S308
Forming a second though hole that penetrates the second stacked layer and the second insulating connection layer, and extends into the surface of the third channel structure, the projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate
S309
Forming a second functional layer on the sidewall of the second through hole
S3010
Removing the second tunneling structure, the third tunneling structure, the second passivation layer, and the first passivation layer to interconnect the first through hole and the second through hole
S3011
Sequentially forming a fourth channel structure and a first filling structure on the sidewall and the bottom of the third through hole
S3012
Forming a fifth channel structure in contact with the fourth channel structure in a second groove that is above the fourth channel structure and the first filling structure
S3013

FIG. 74B

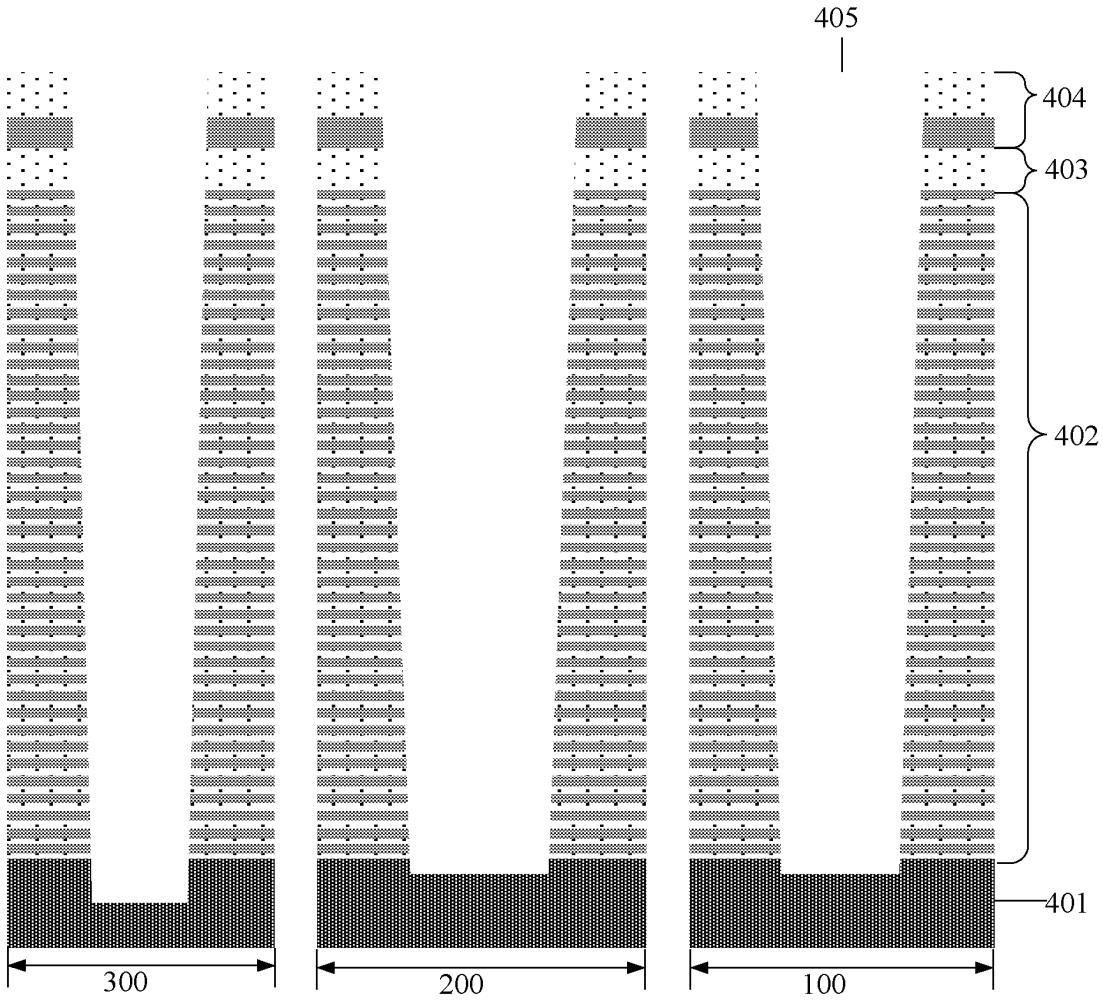


FIG. 75

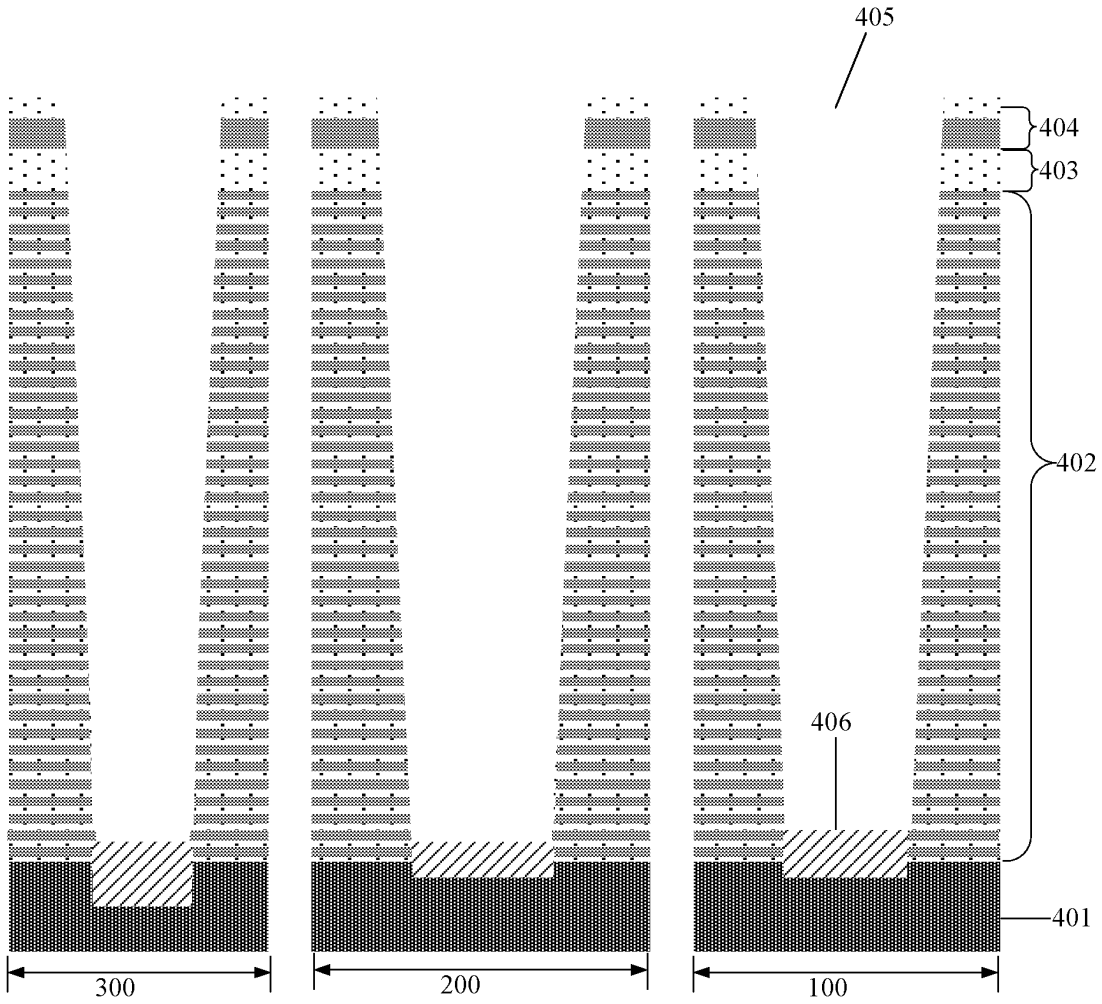


FIG. 76

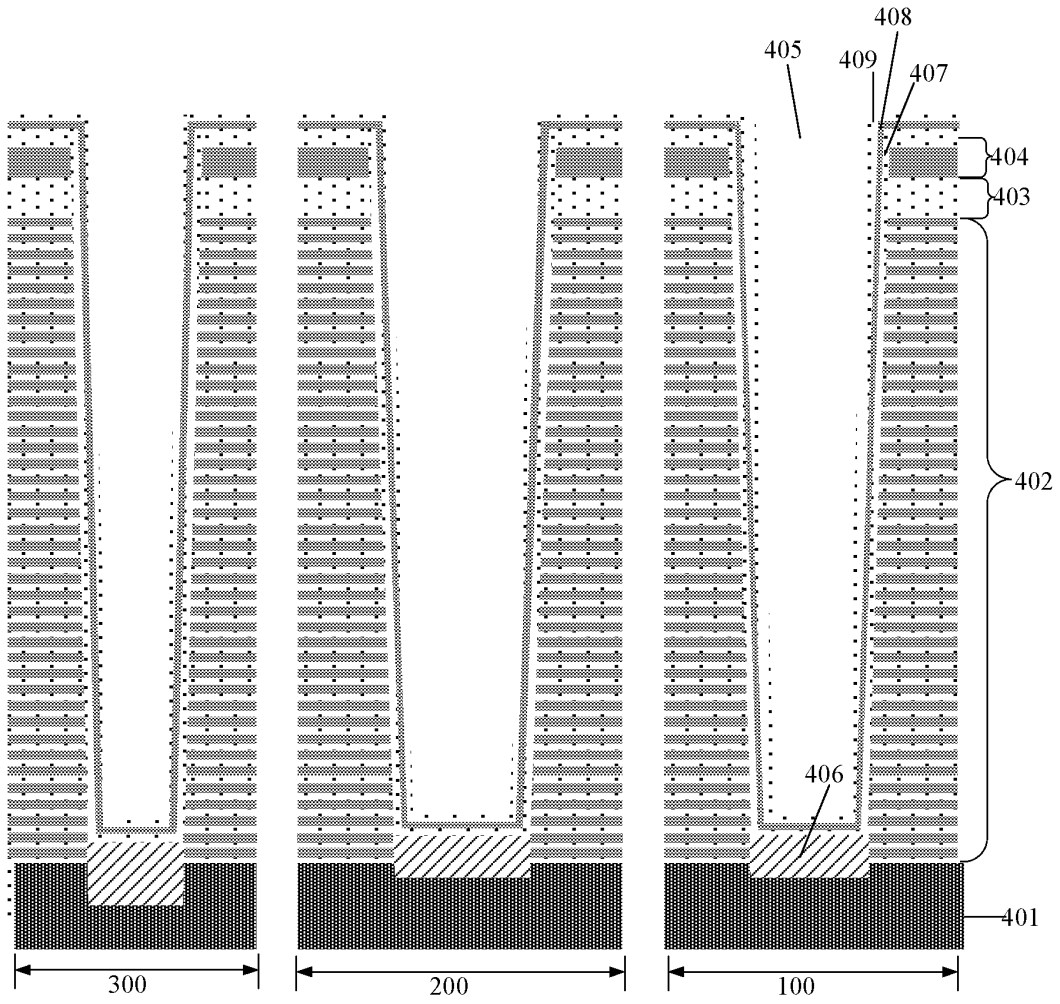


FIG. 77

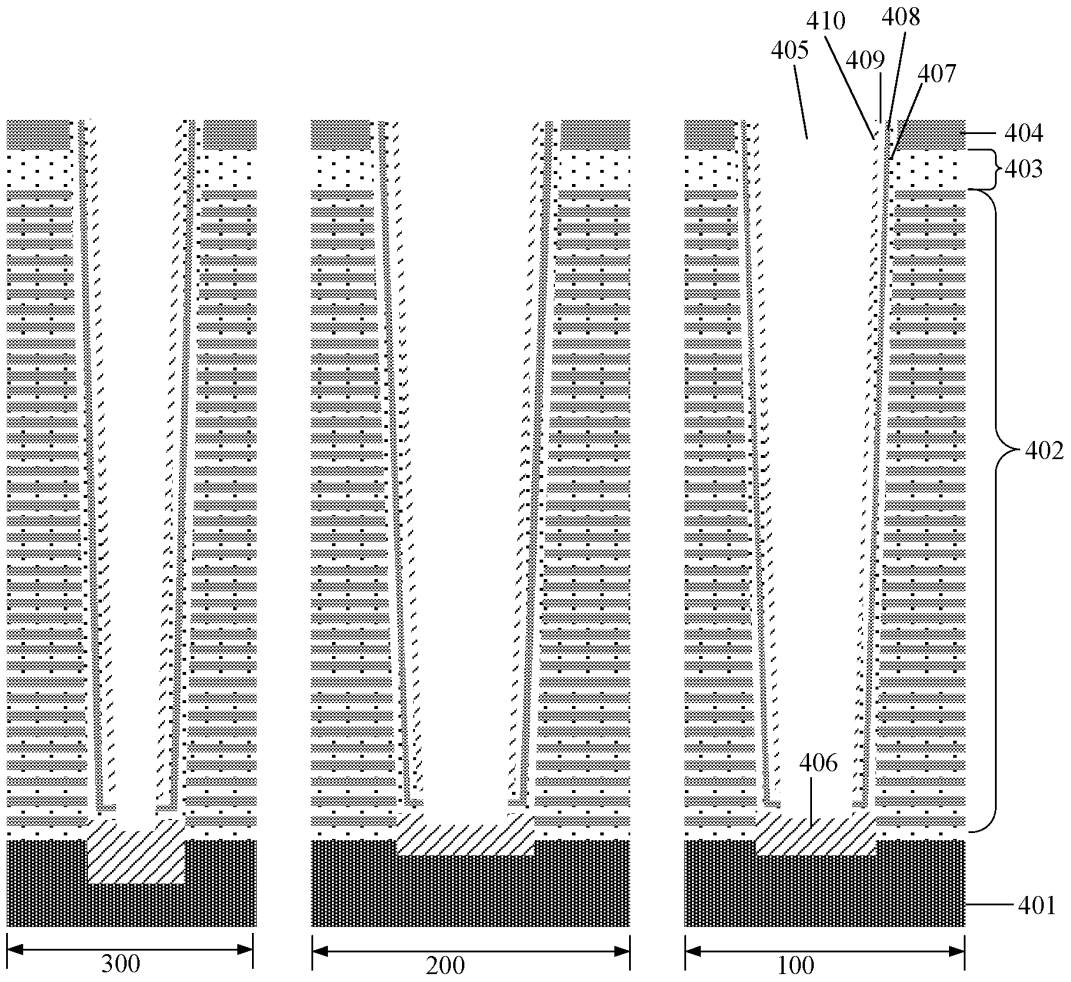


FIG. 78

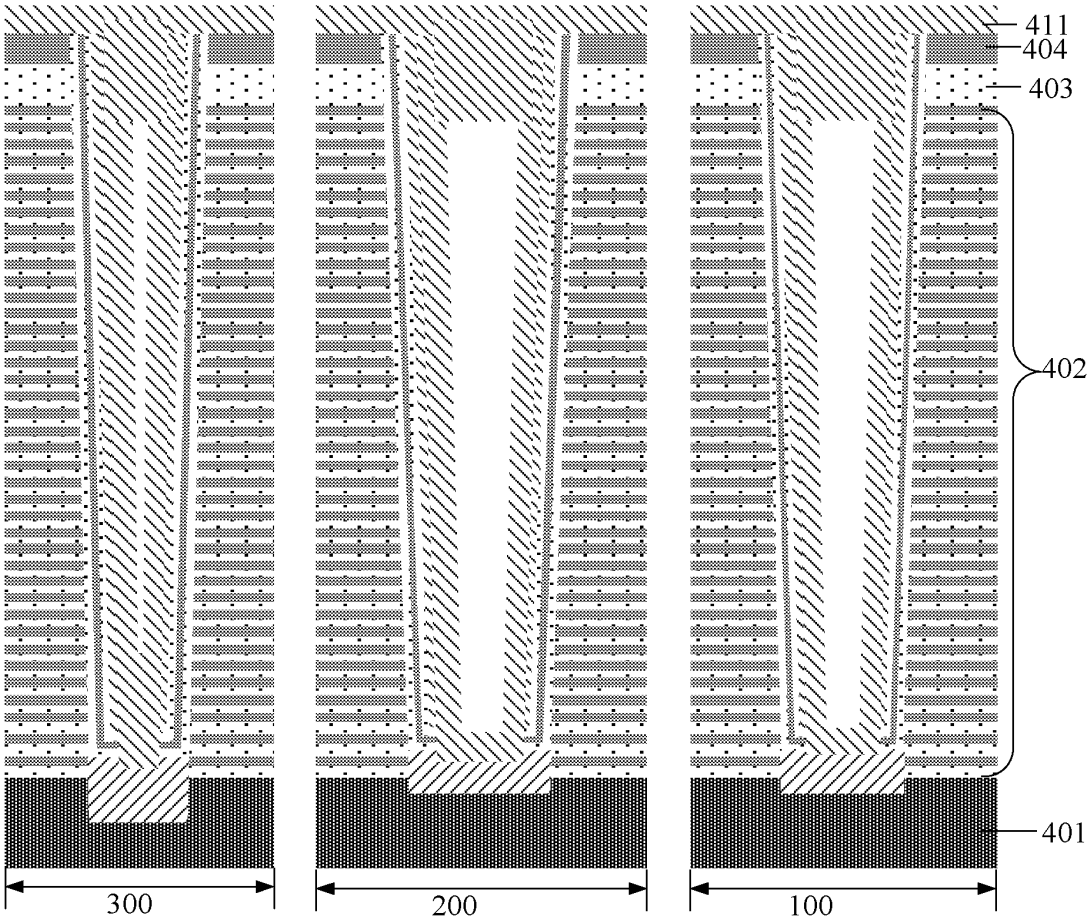


FIG. 79

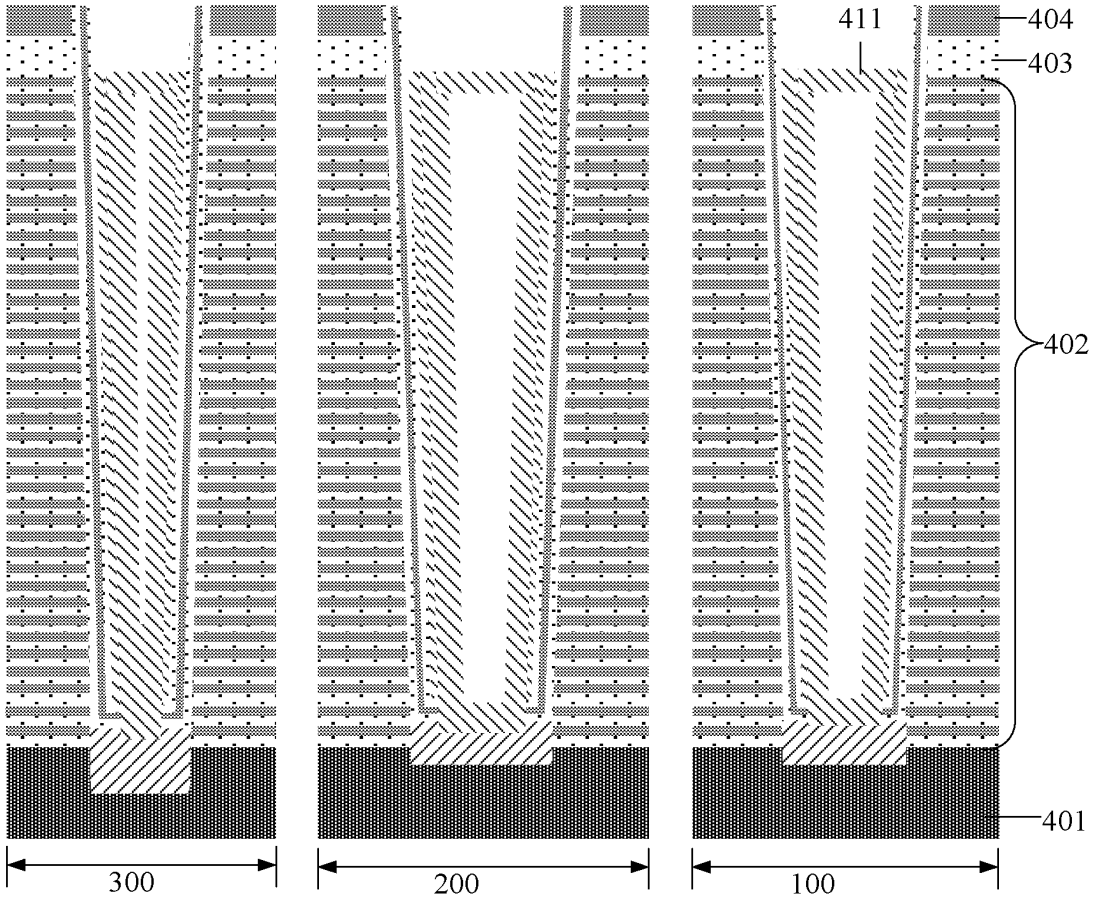


FIG. 80A

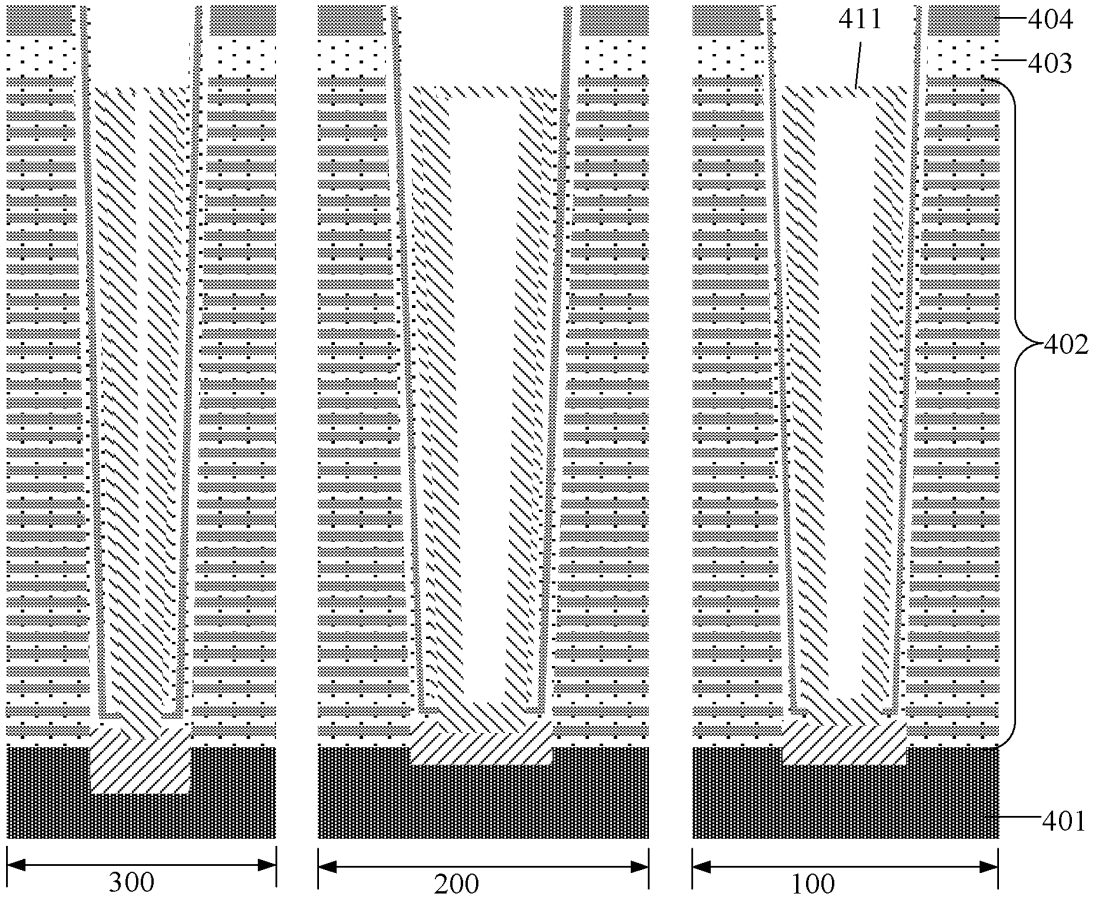


FIG. 80B

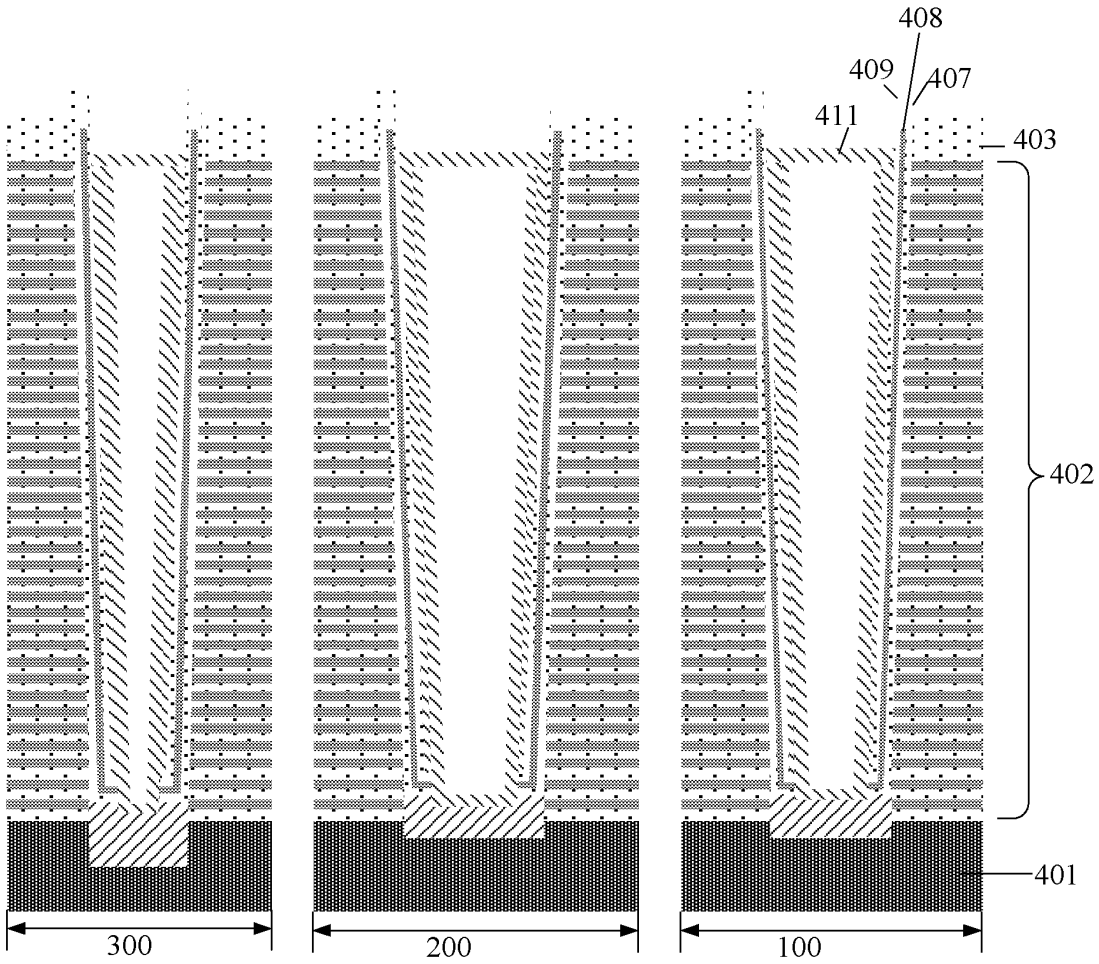


FIG. 81A

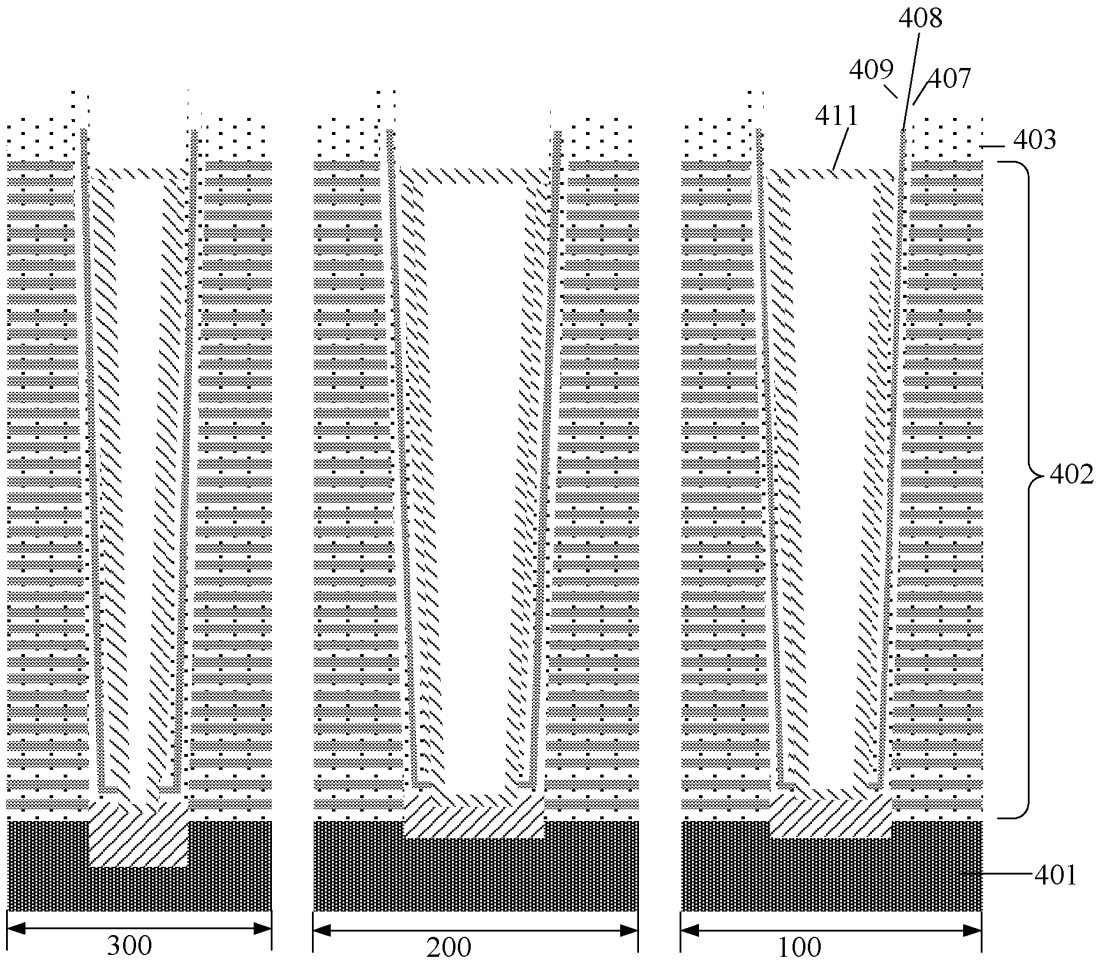


FIG. 81B

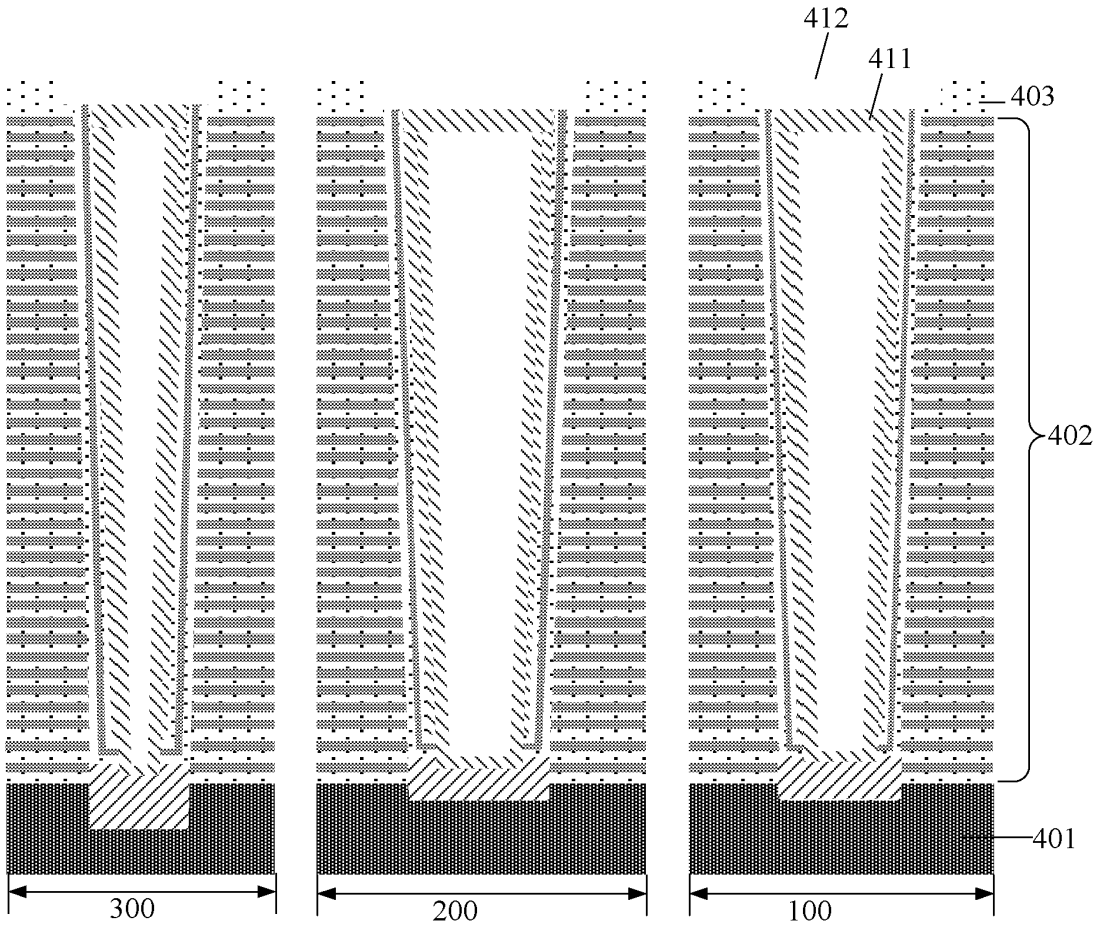


FIG. 82A

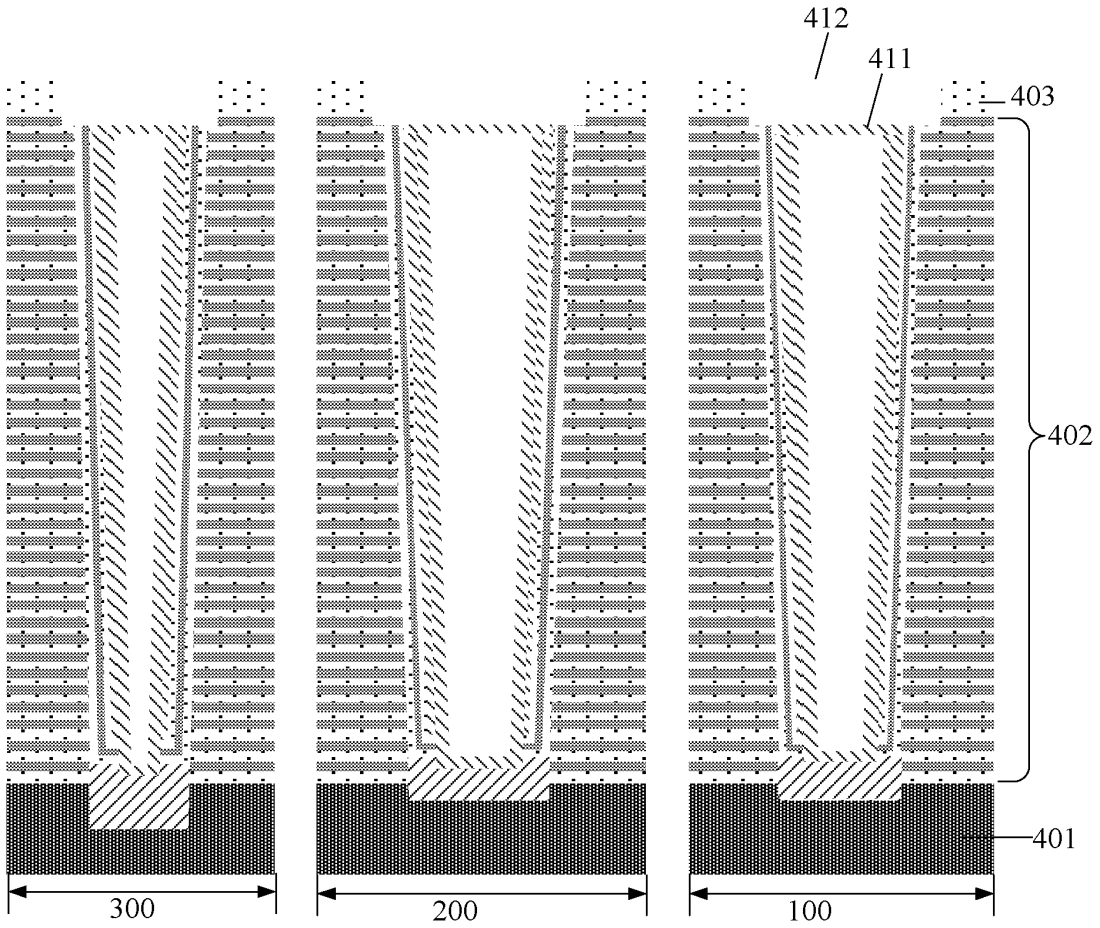


FIG. 82B

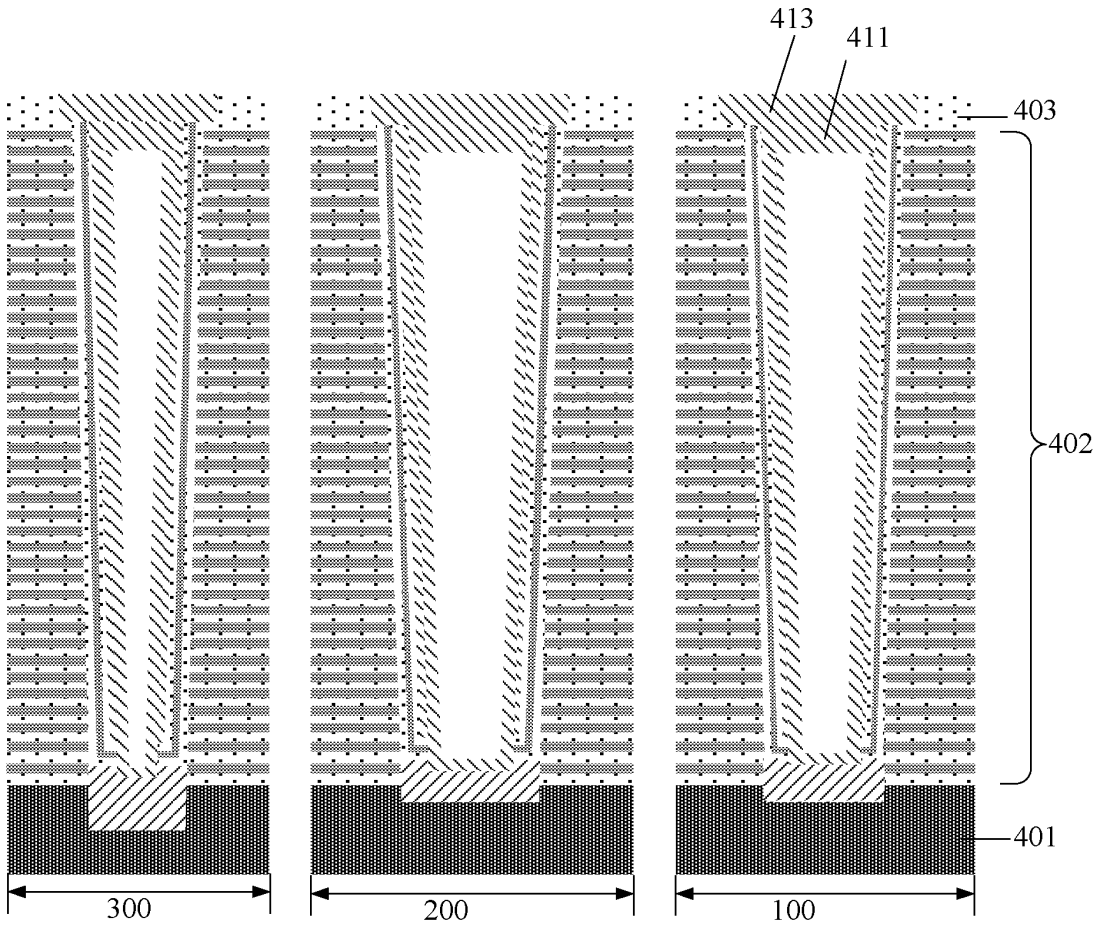


FIG. 83A

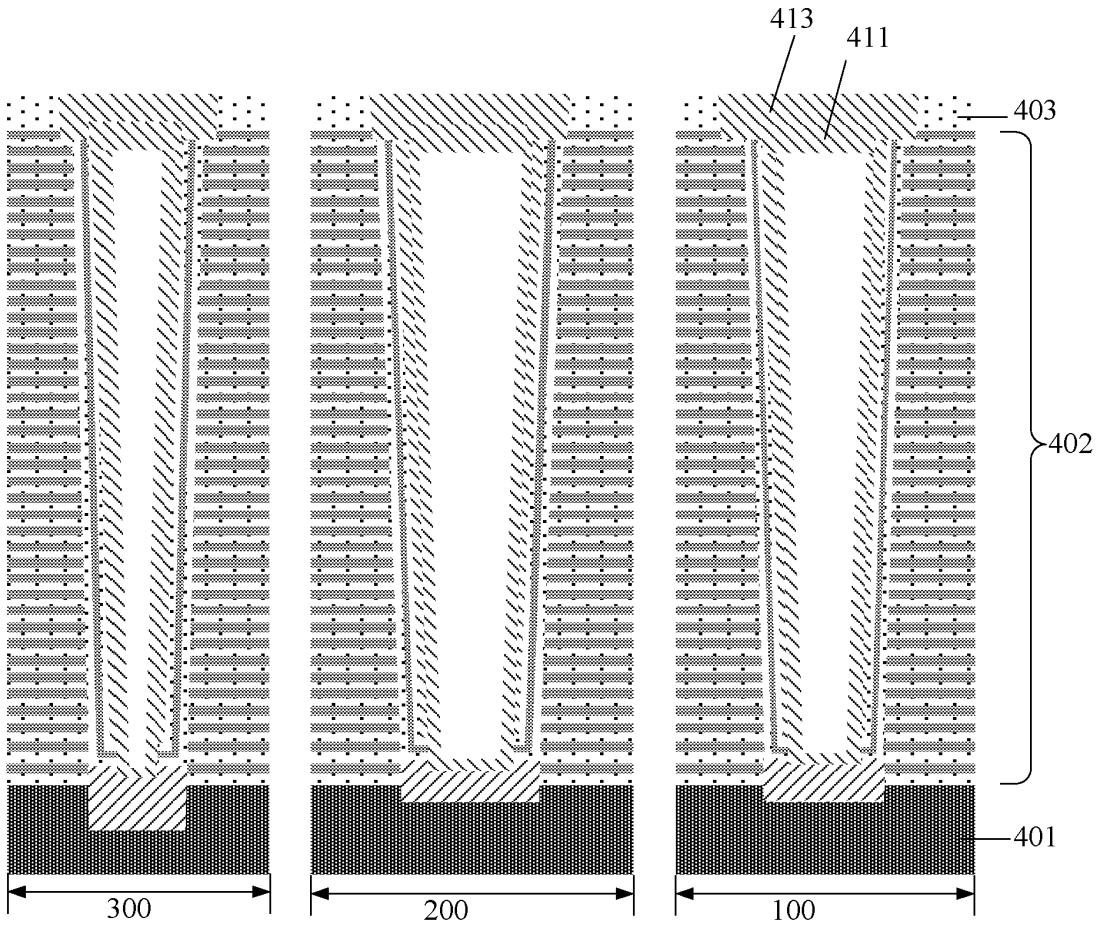


FIG. 83B

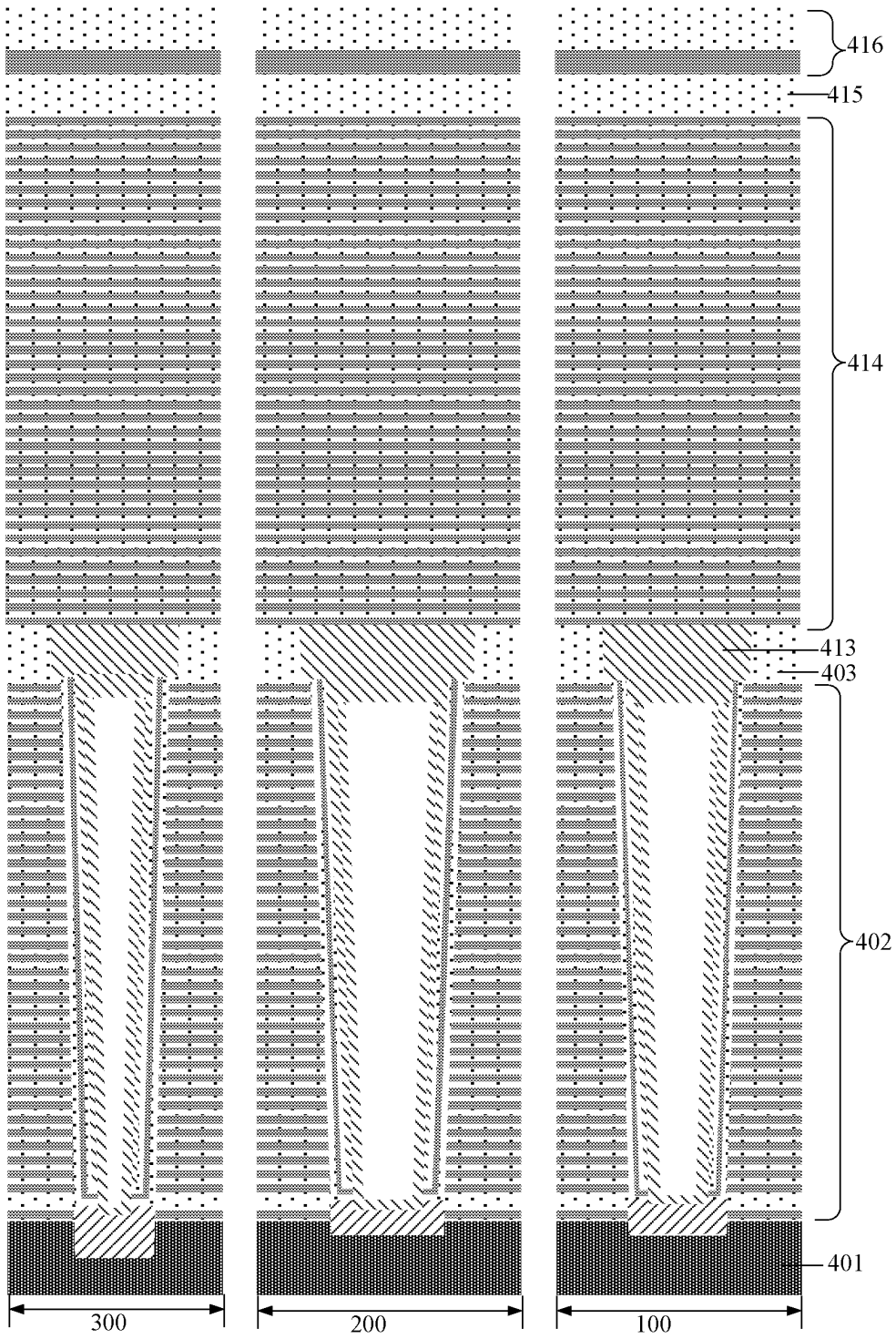


FIG. 84

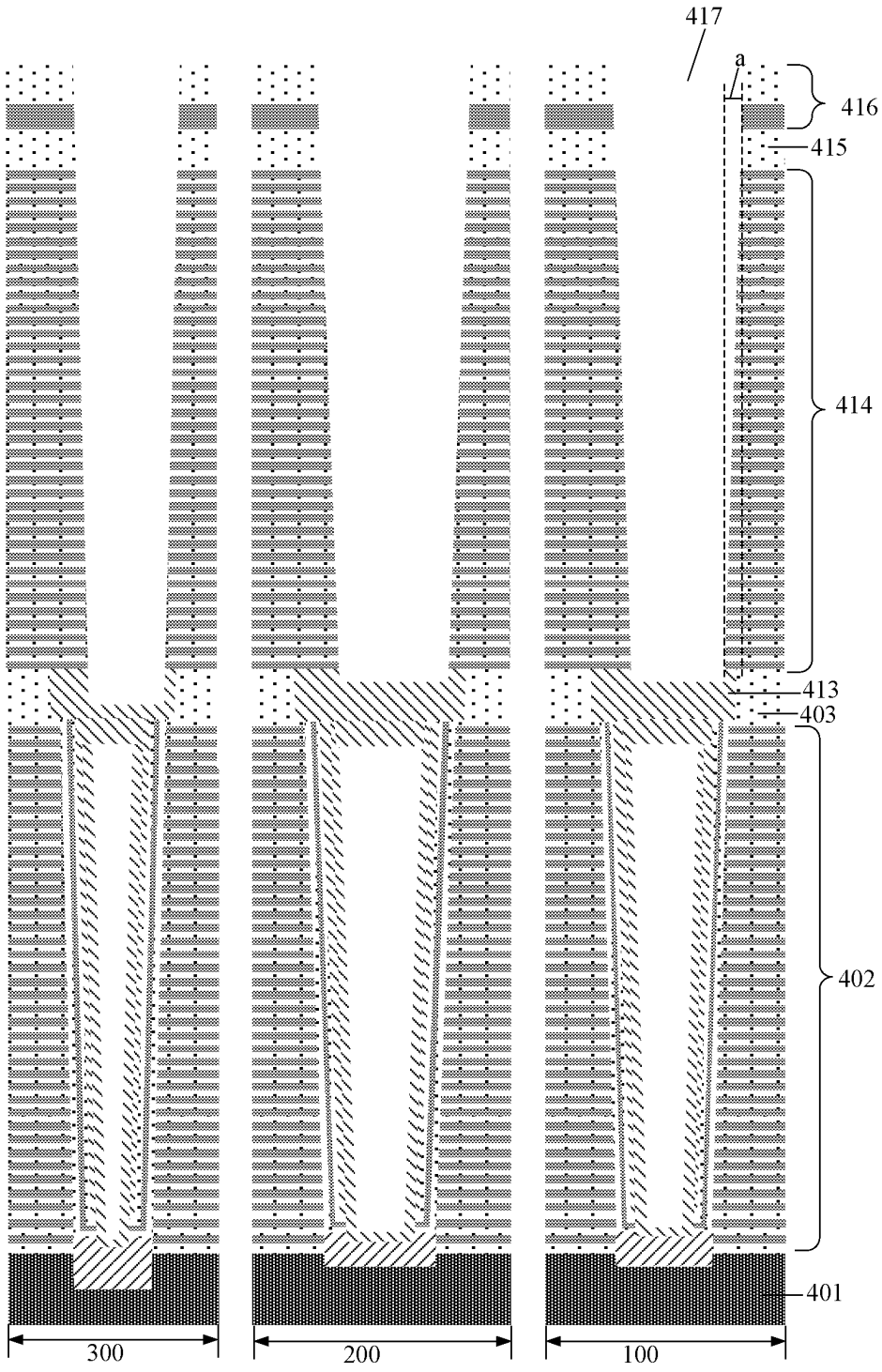


FIG. 85

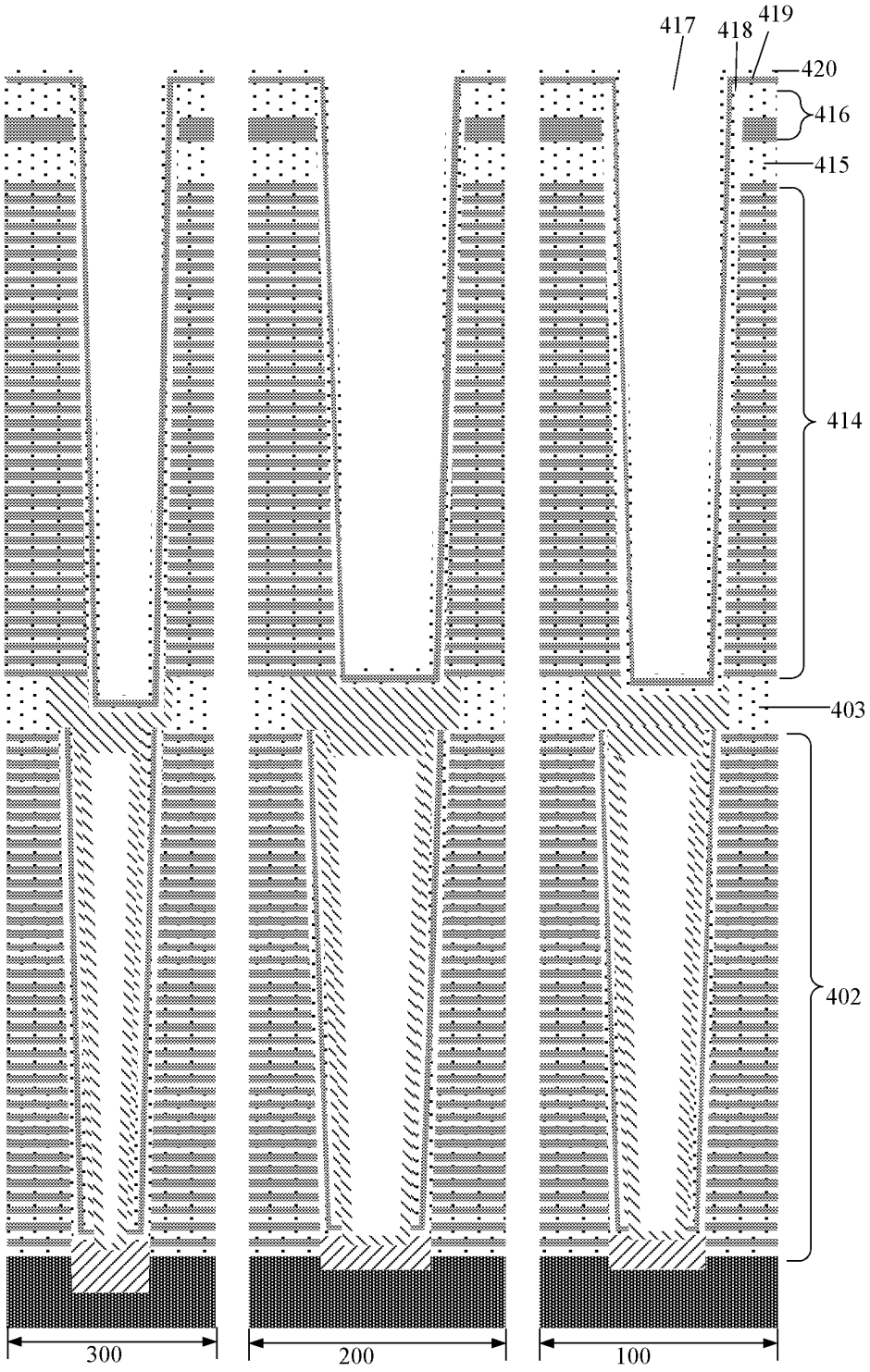


FIG. 86

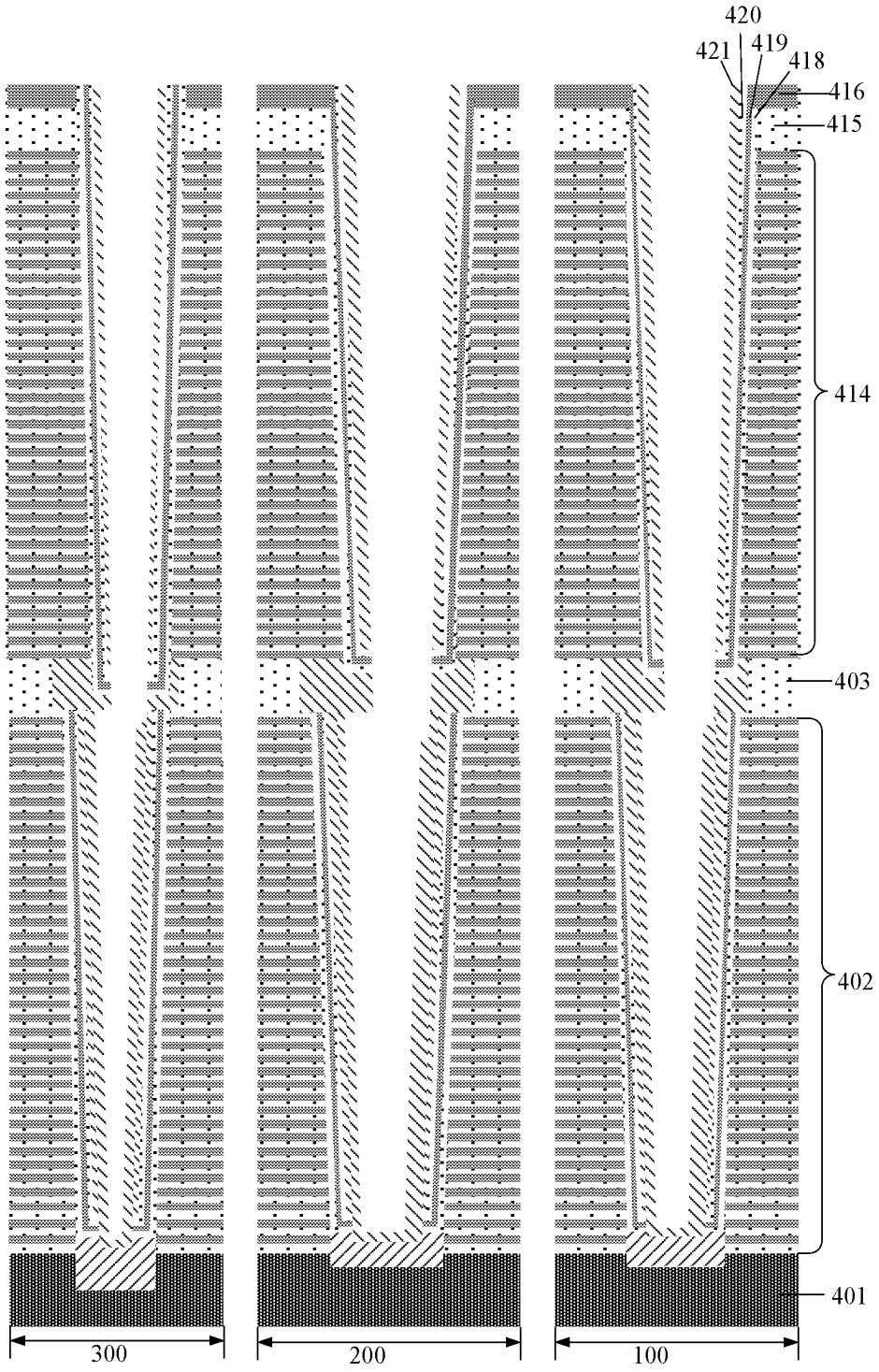


FIG. 87

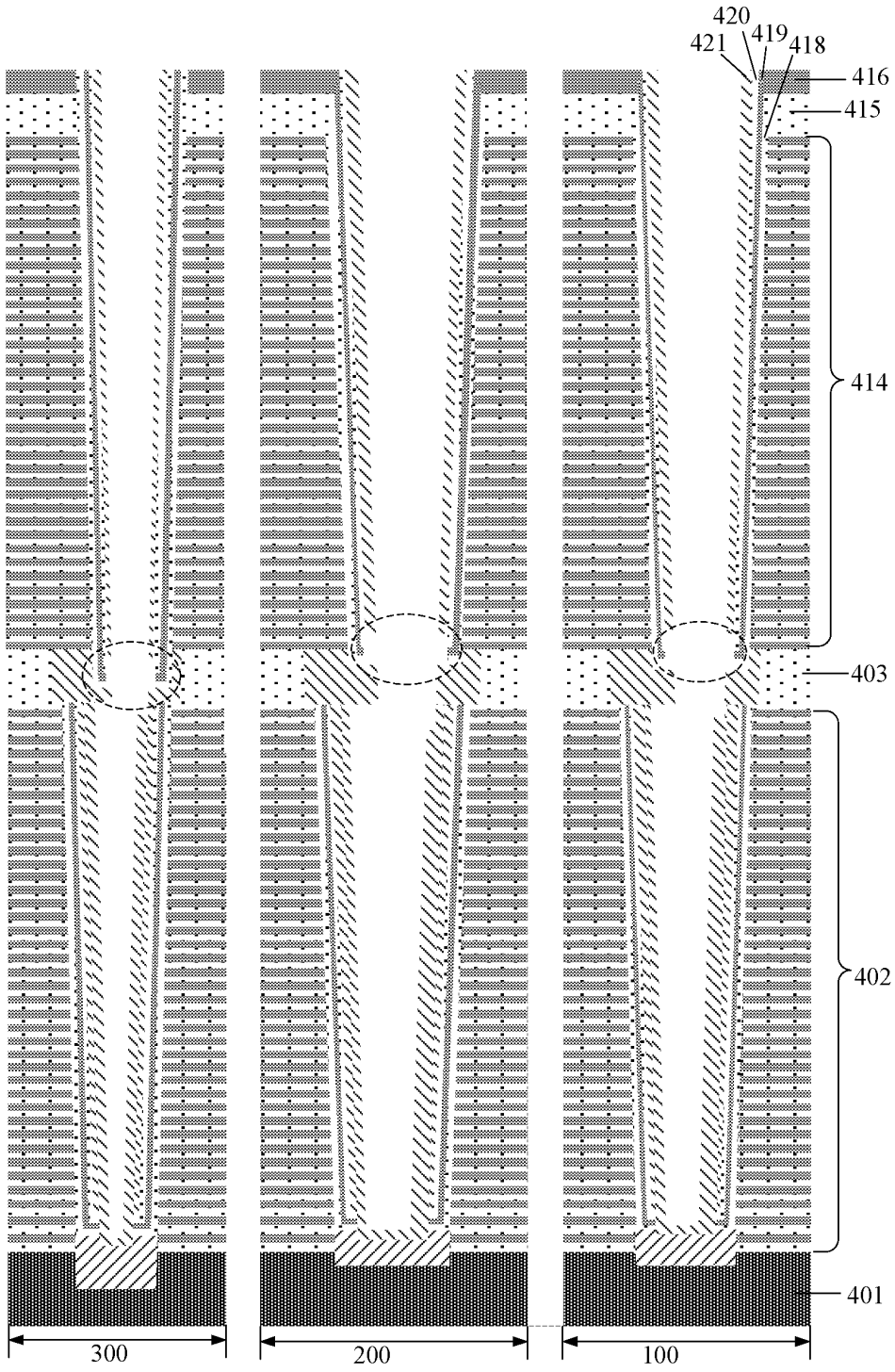


FIG. 88

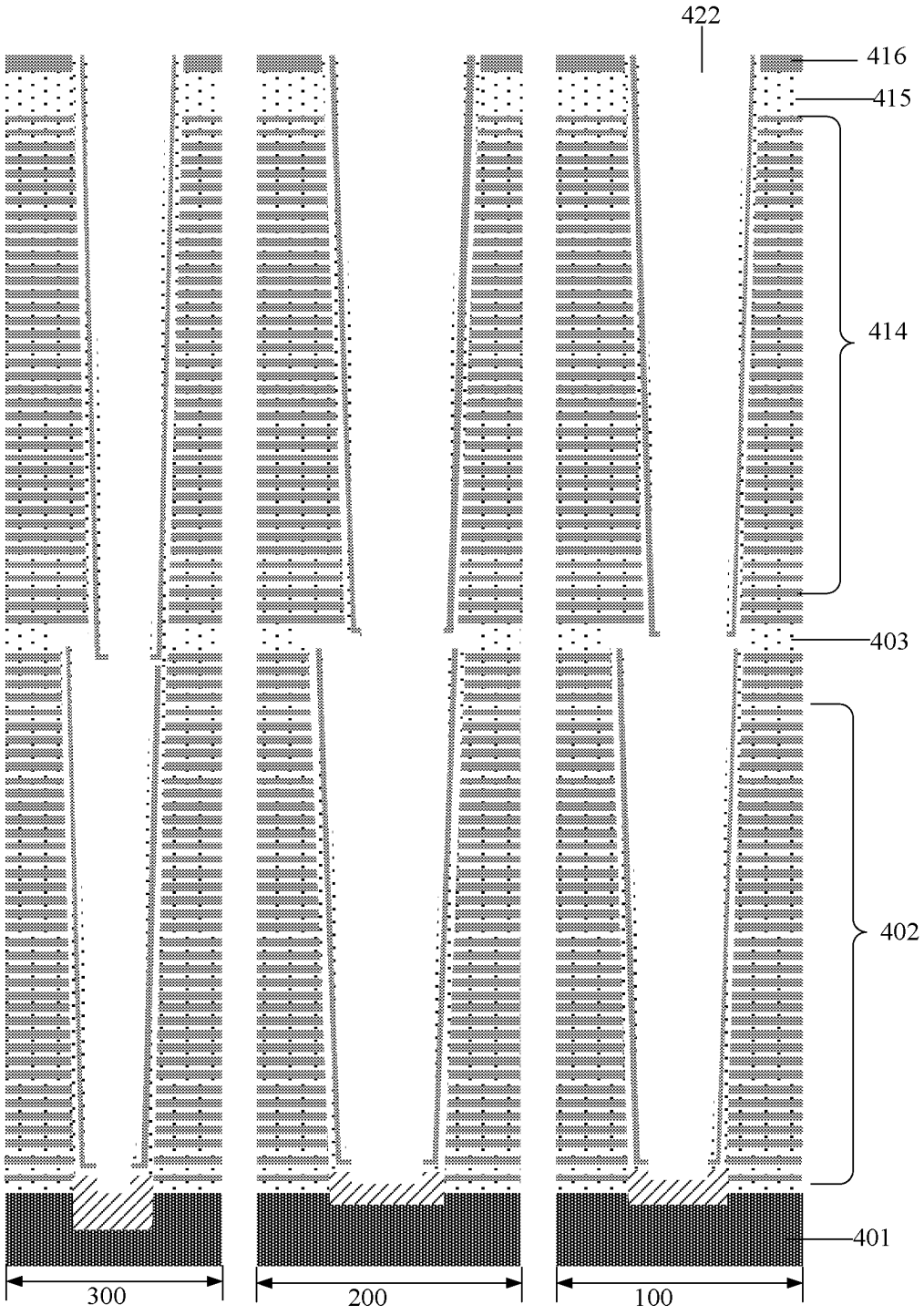


FIG. 89

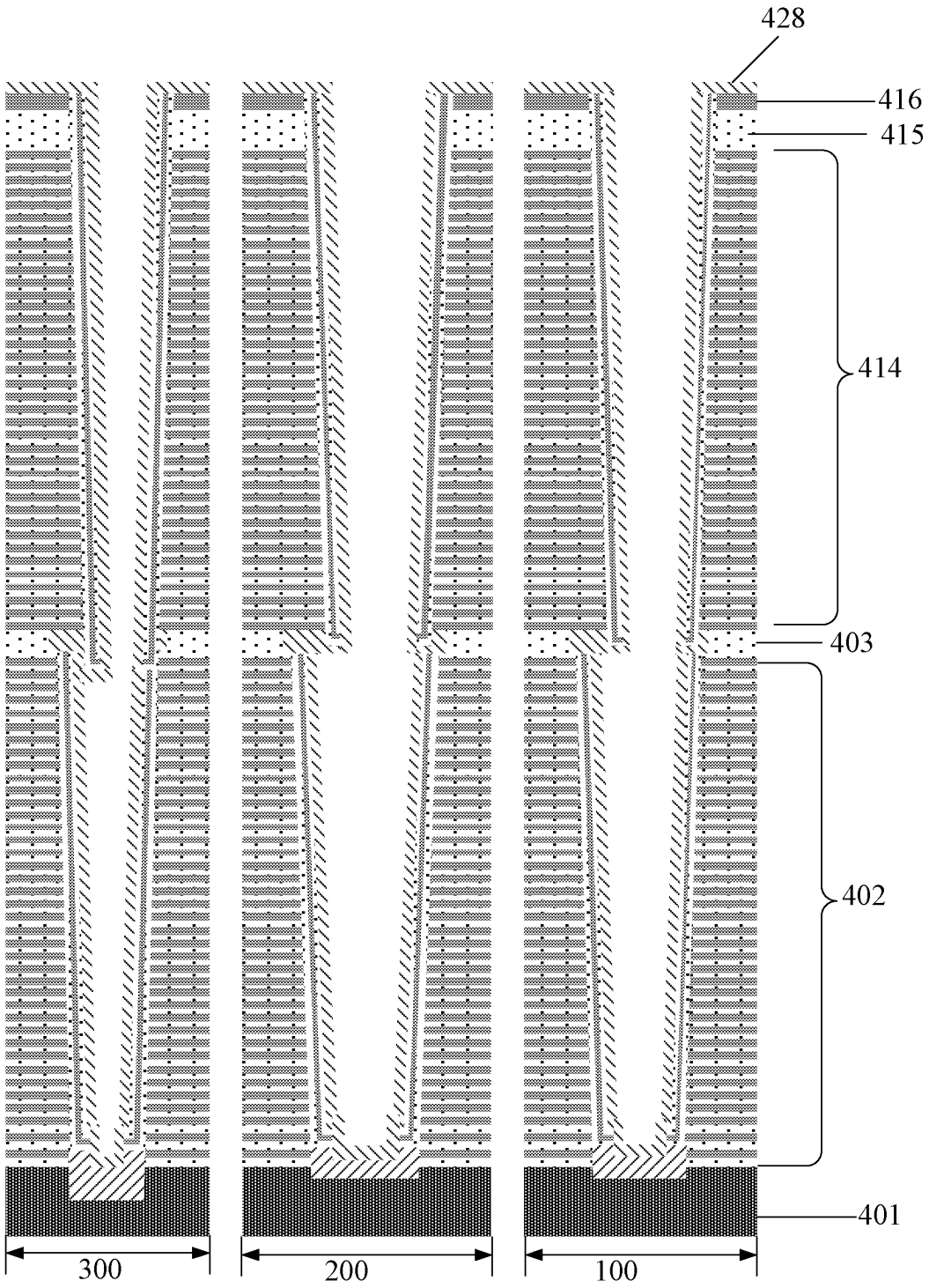


FIG. 90

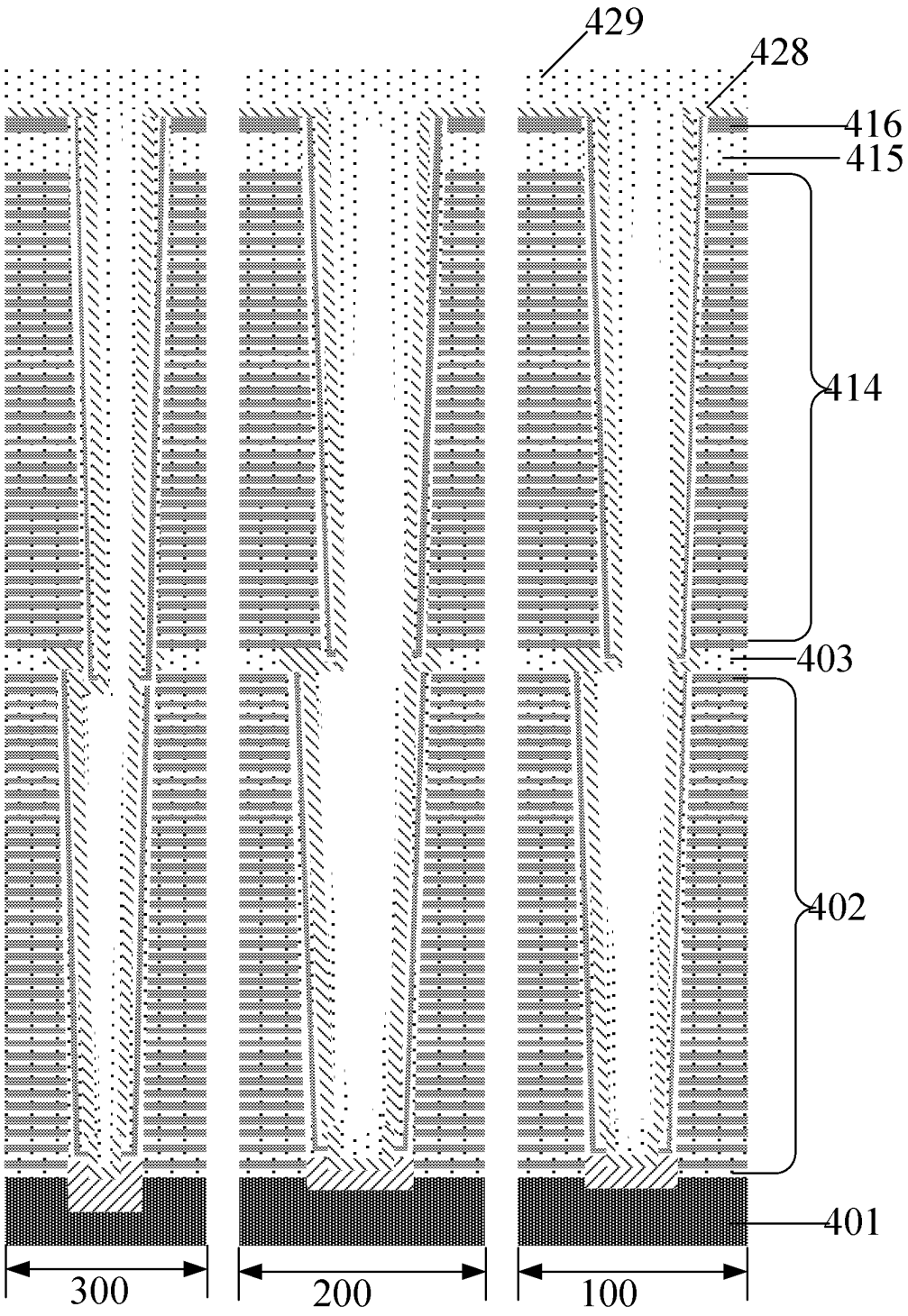


FIG. 91

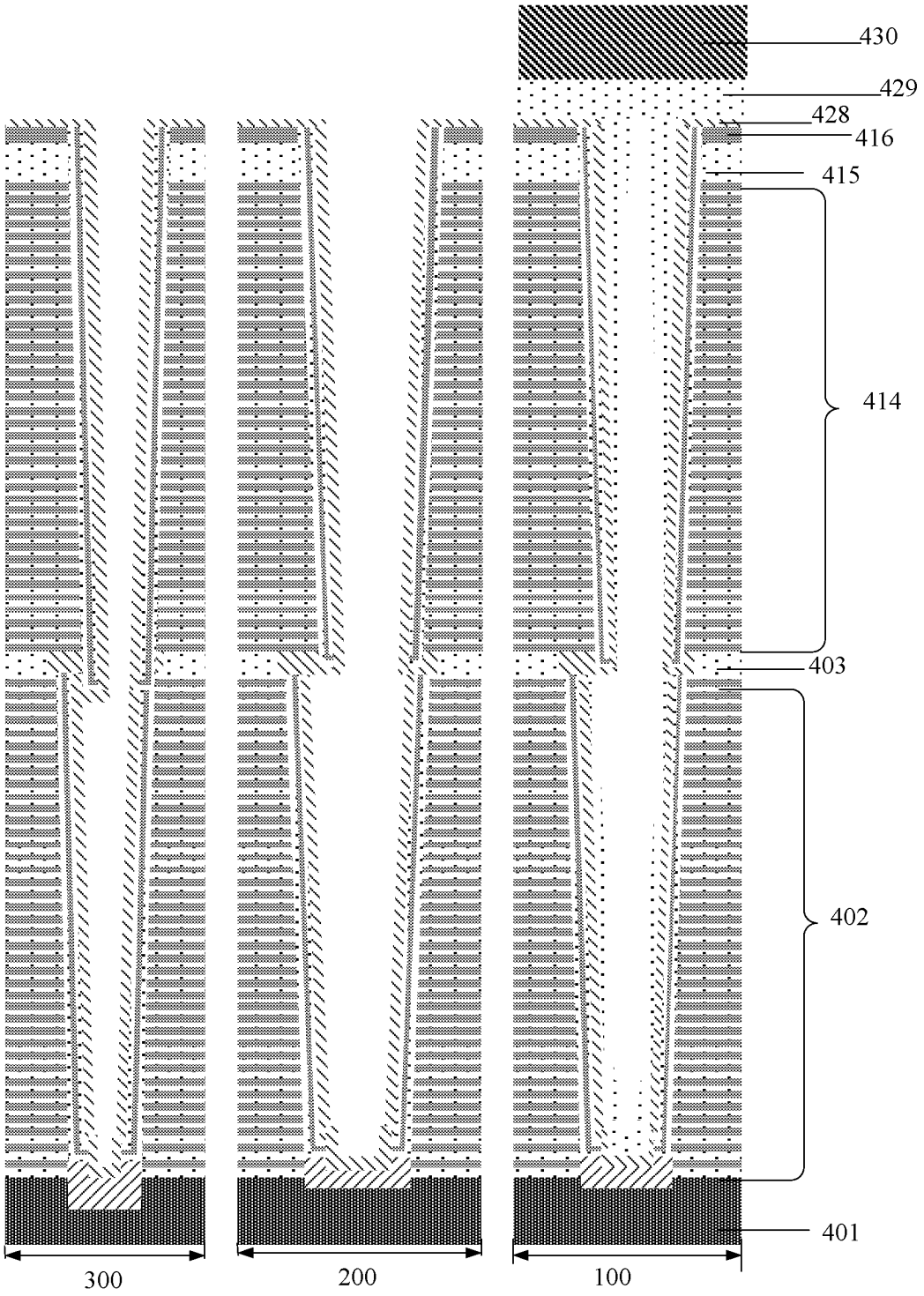


FIG. 92

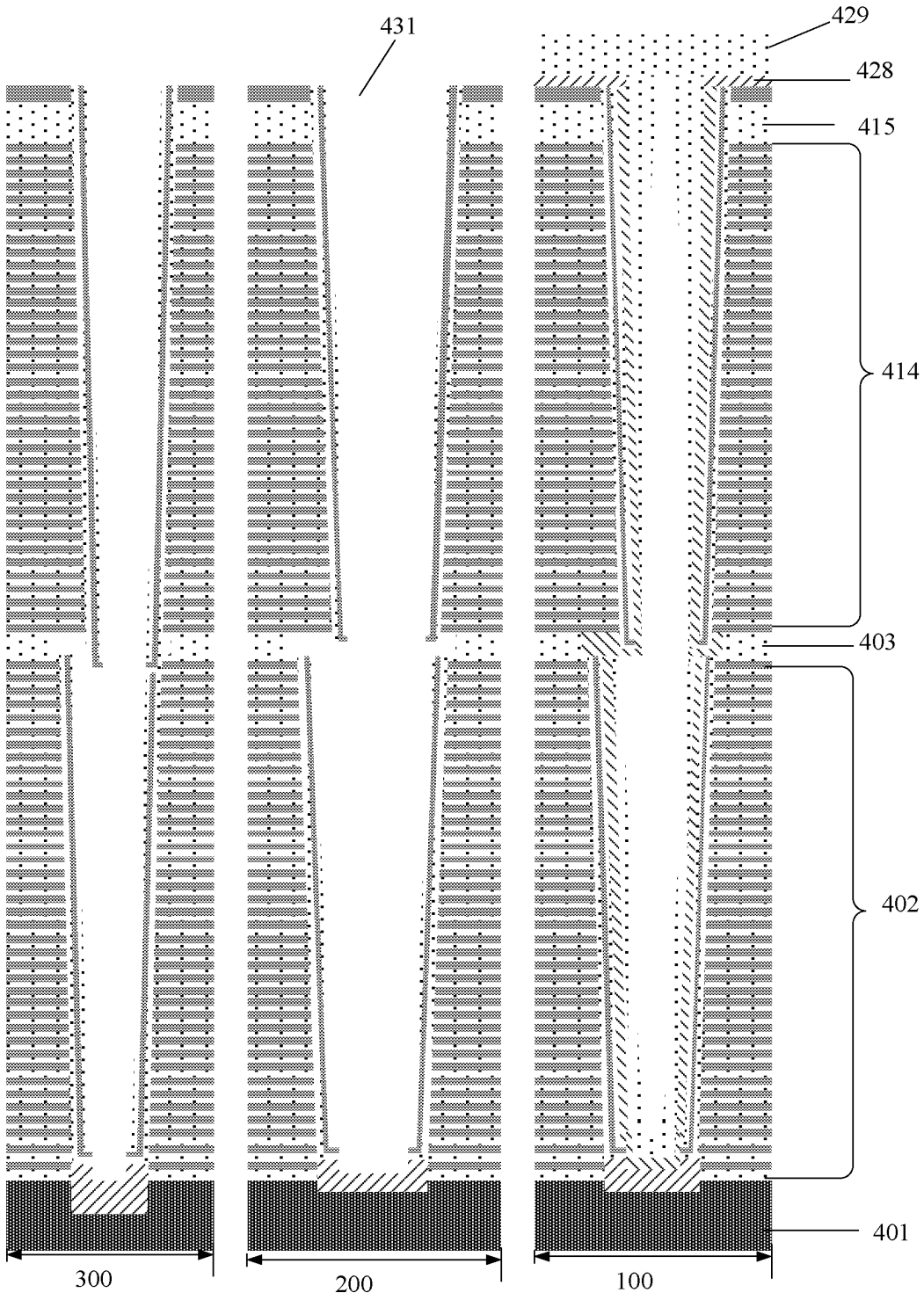


FIG. 93

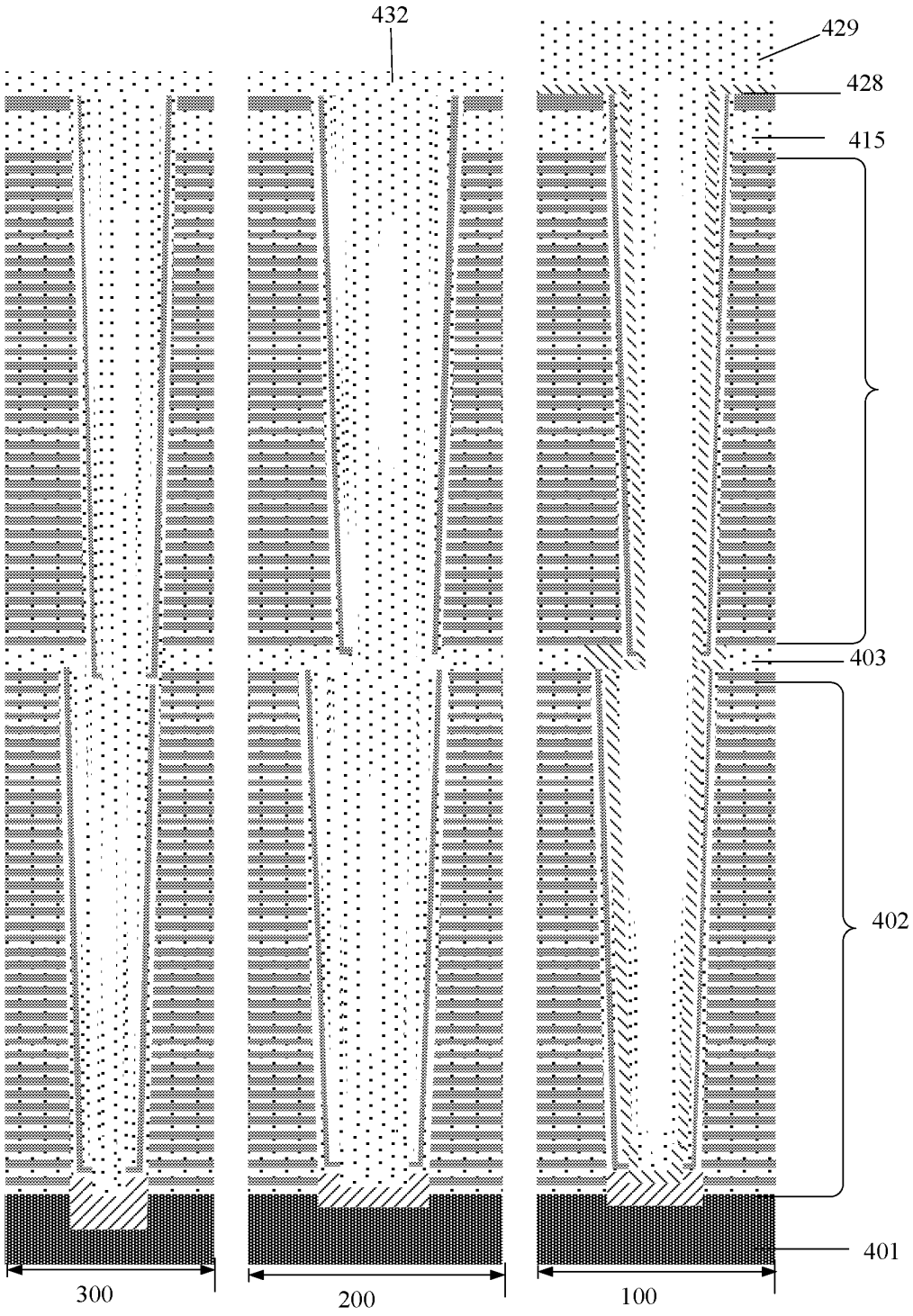


FIG. 94

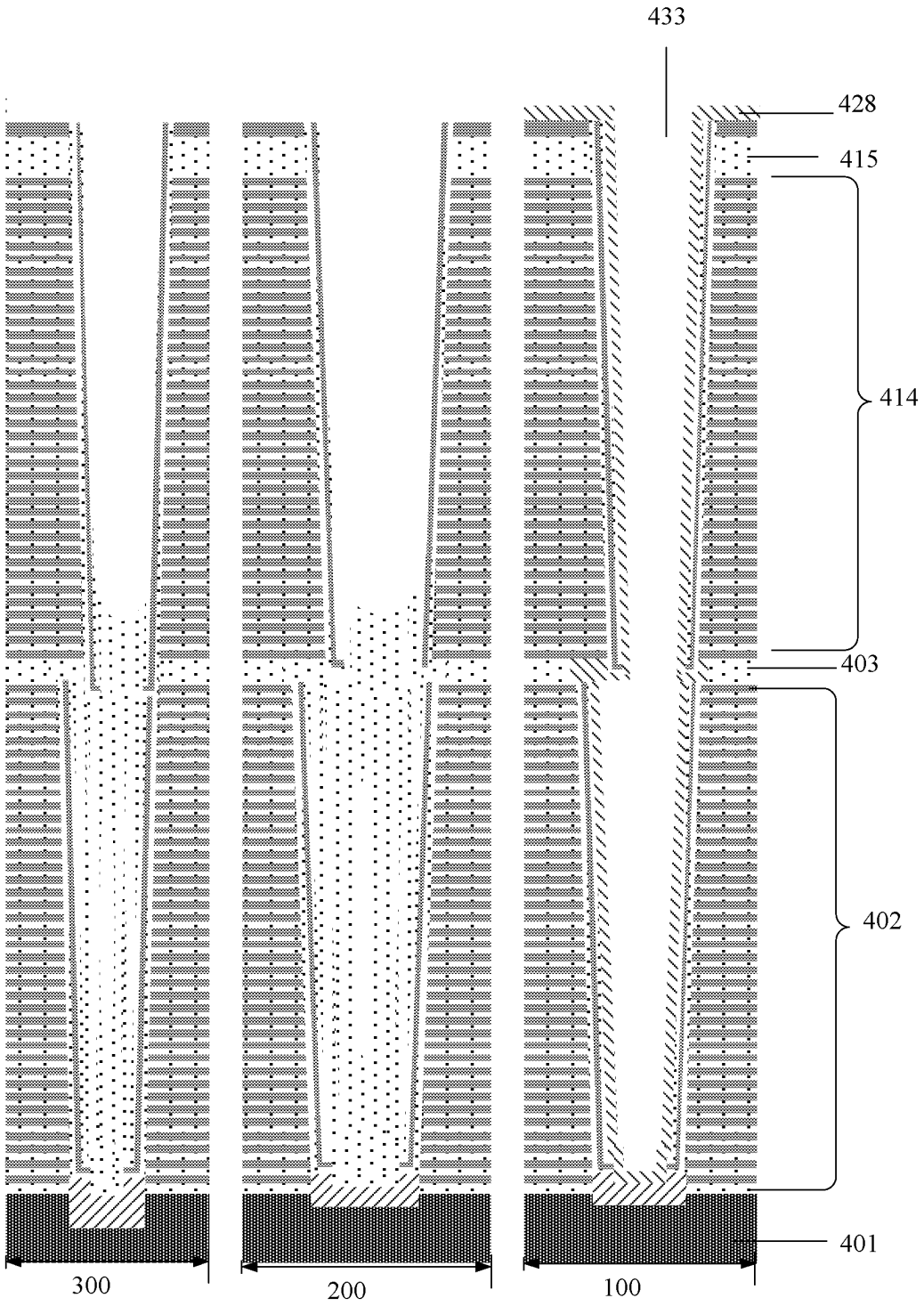


FIG. 95

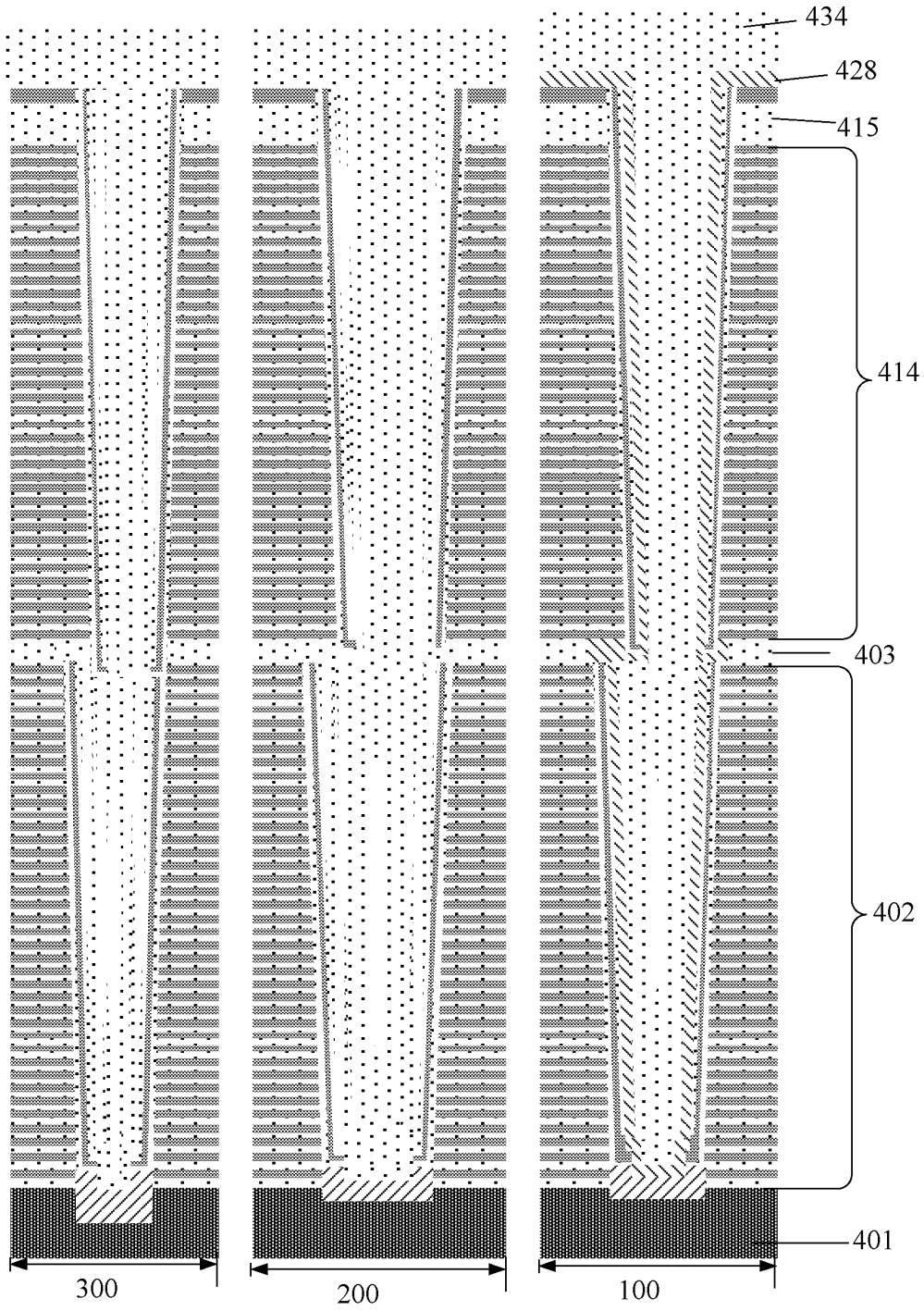


FIG. 96

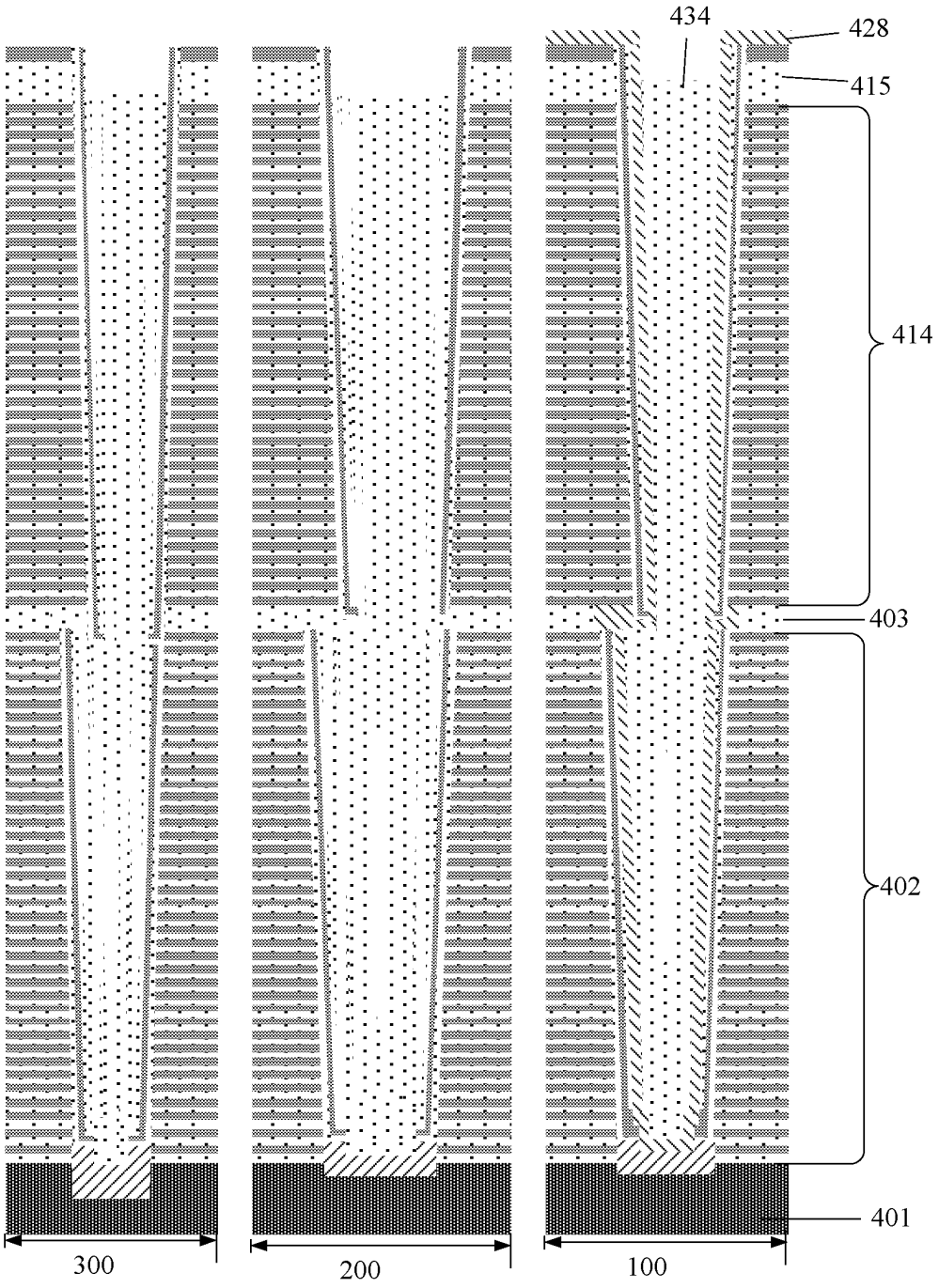


FIG. 97

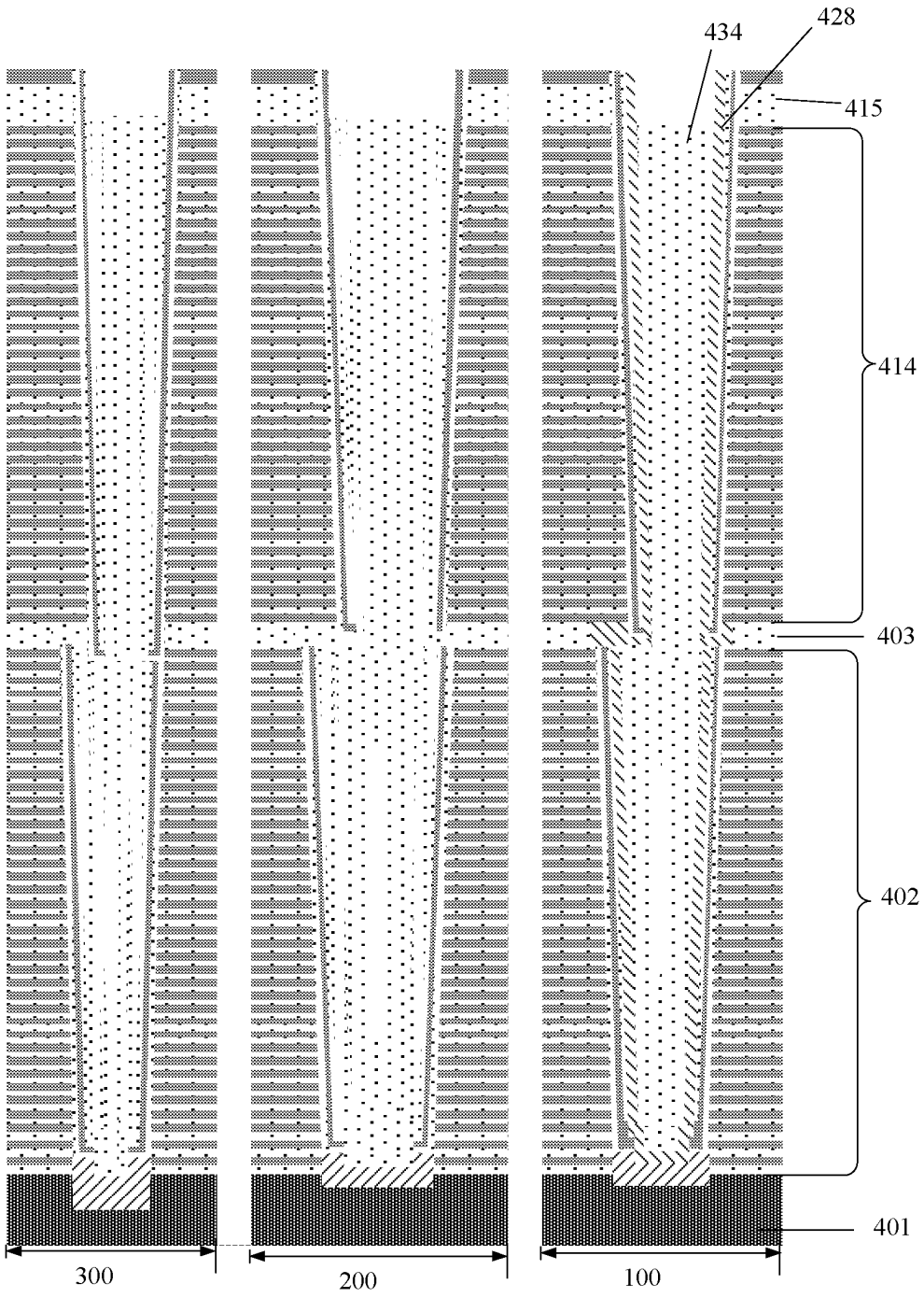


FIG. 98

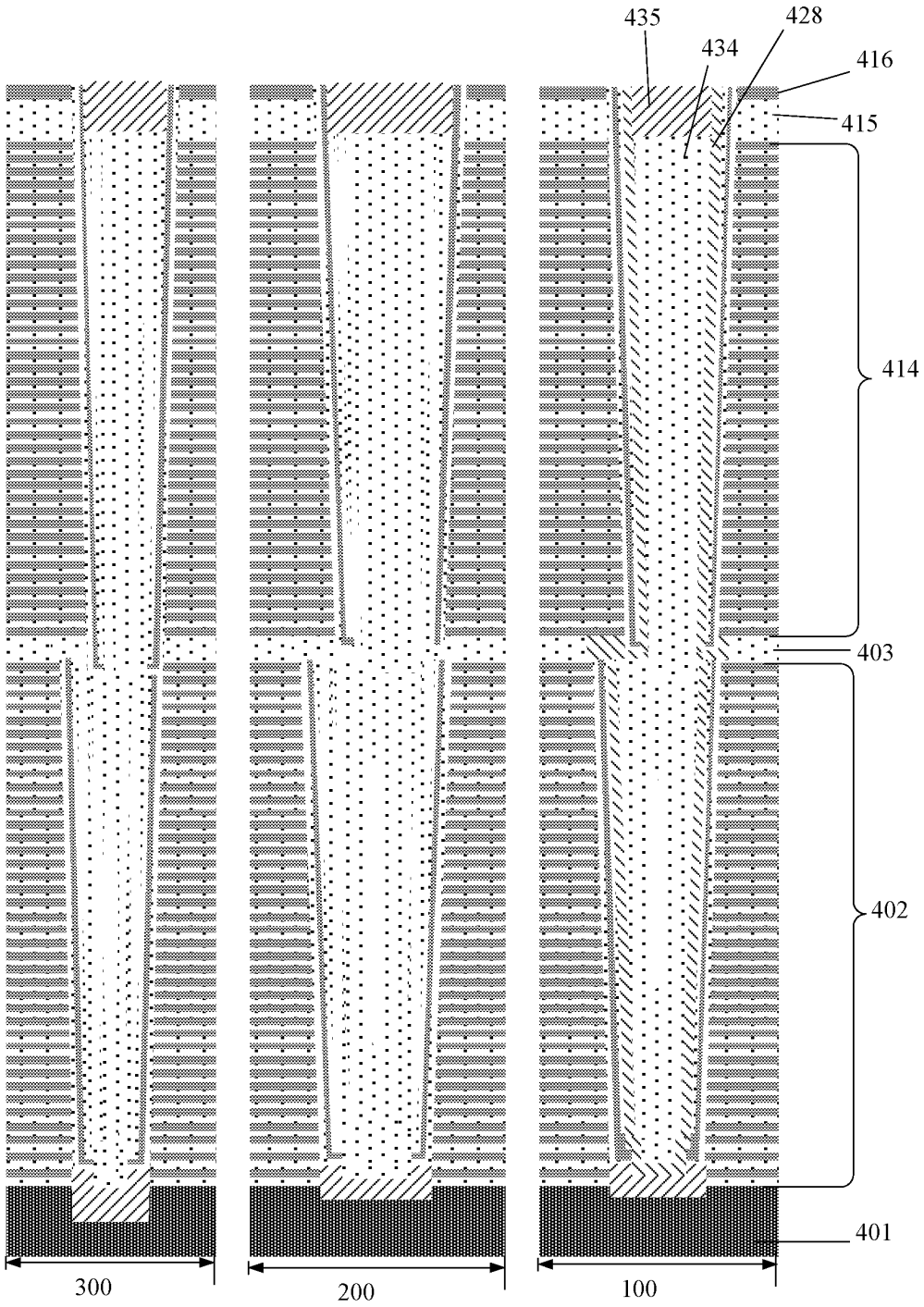


FIG. 99

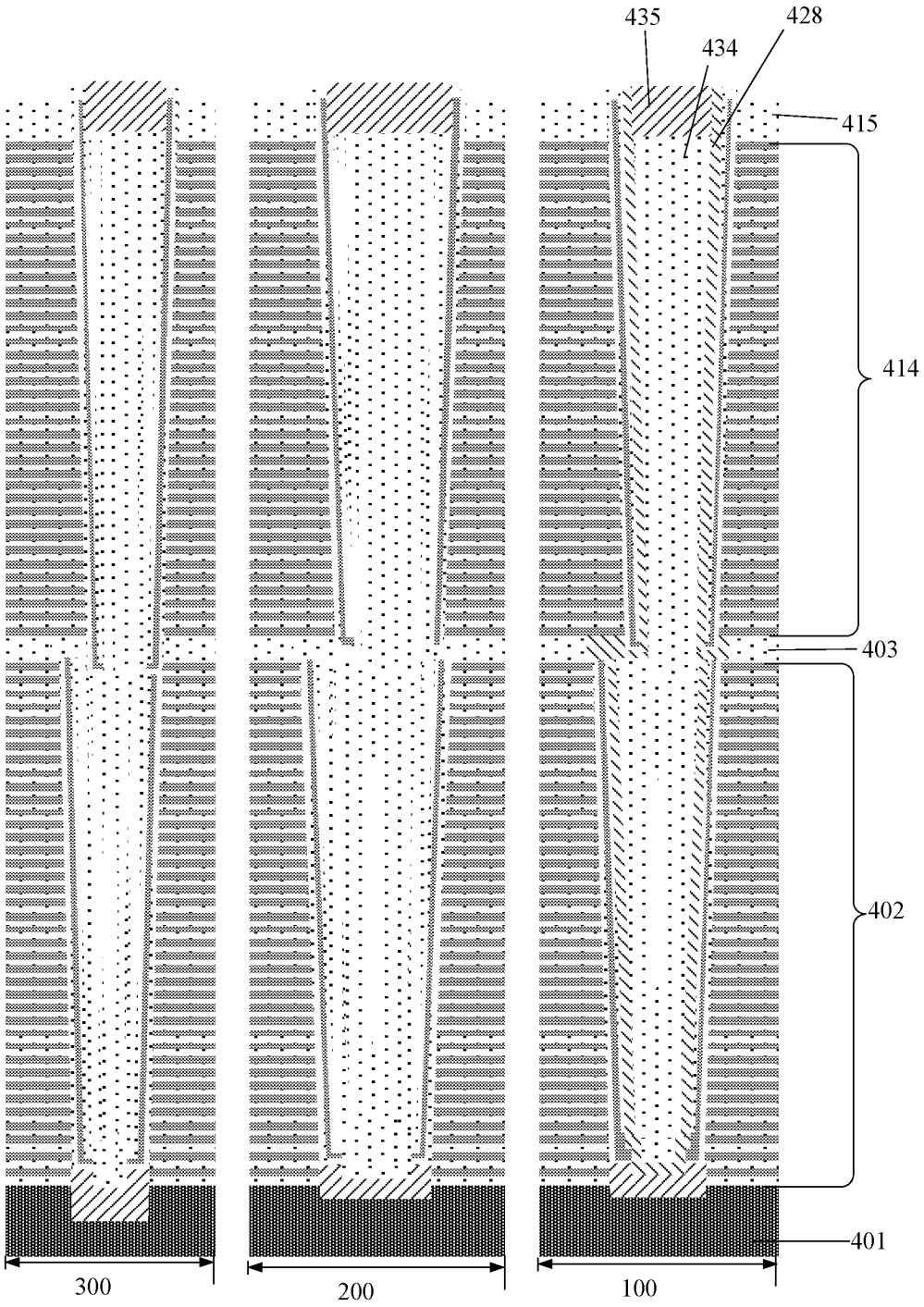


FIG. 100

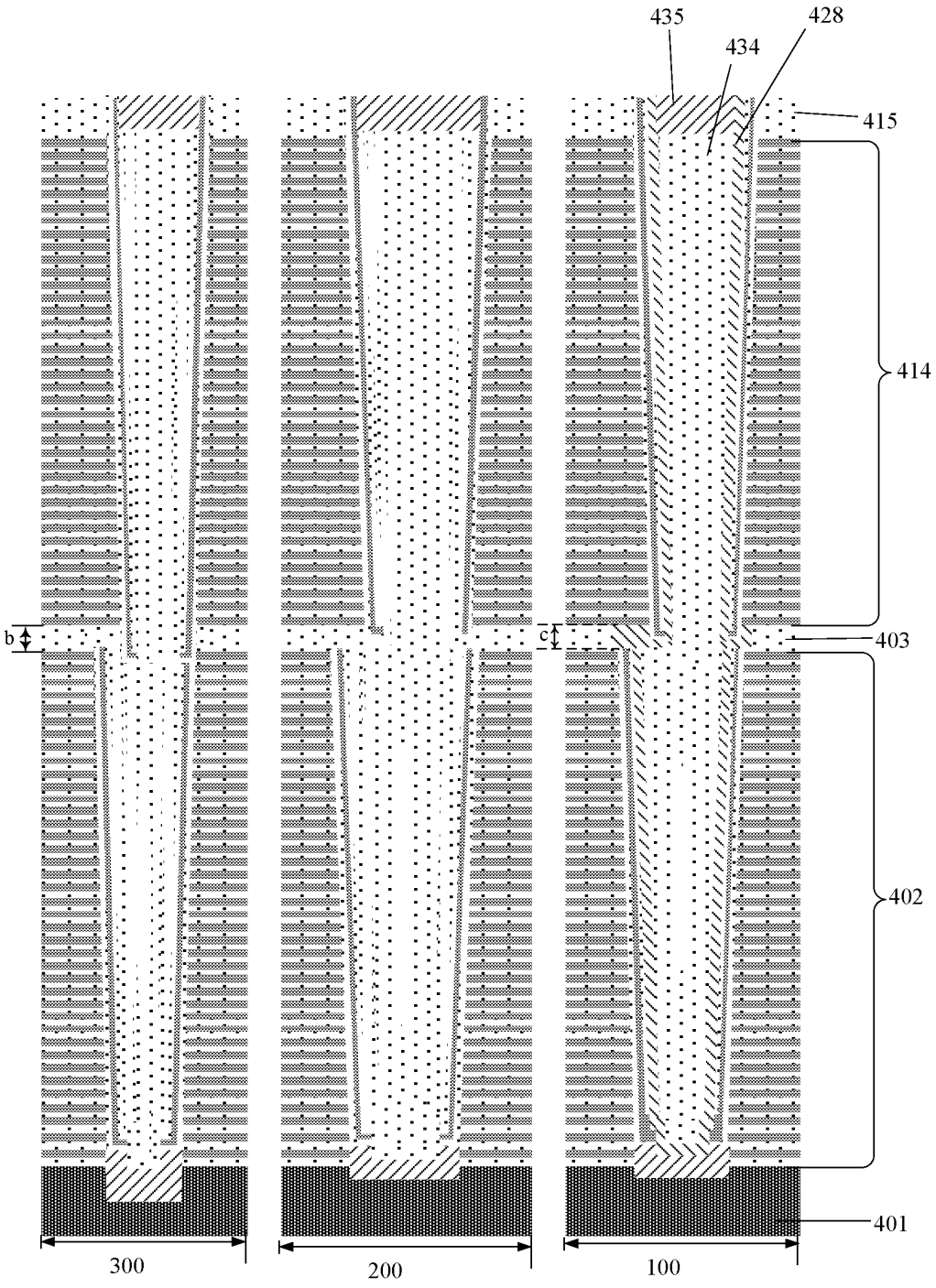


FIG. 101A

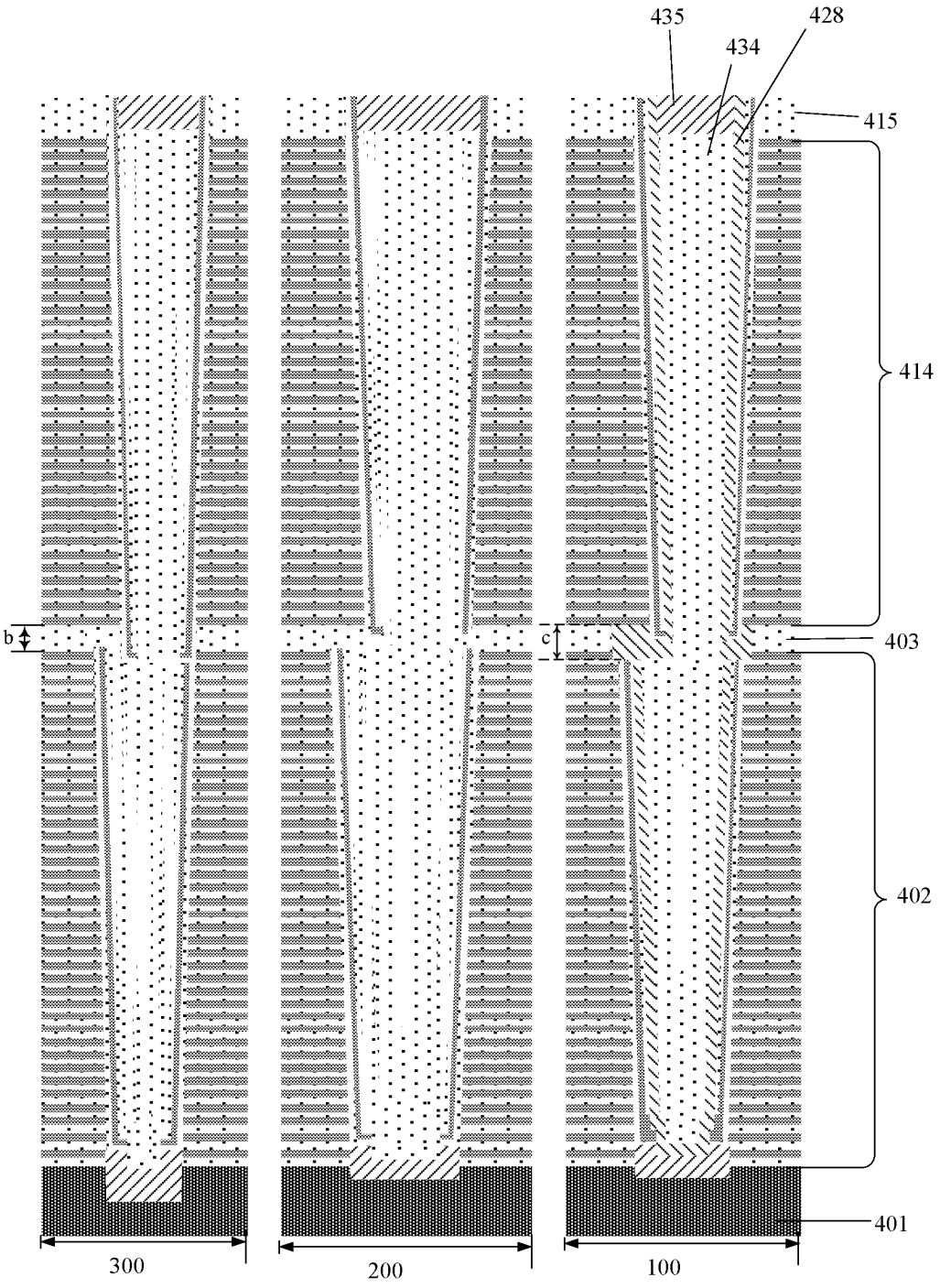


FIG. 101B

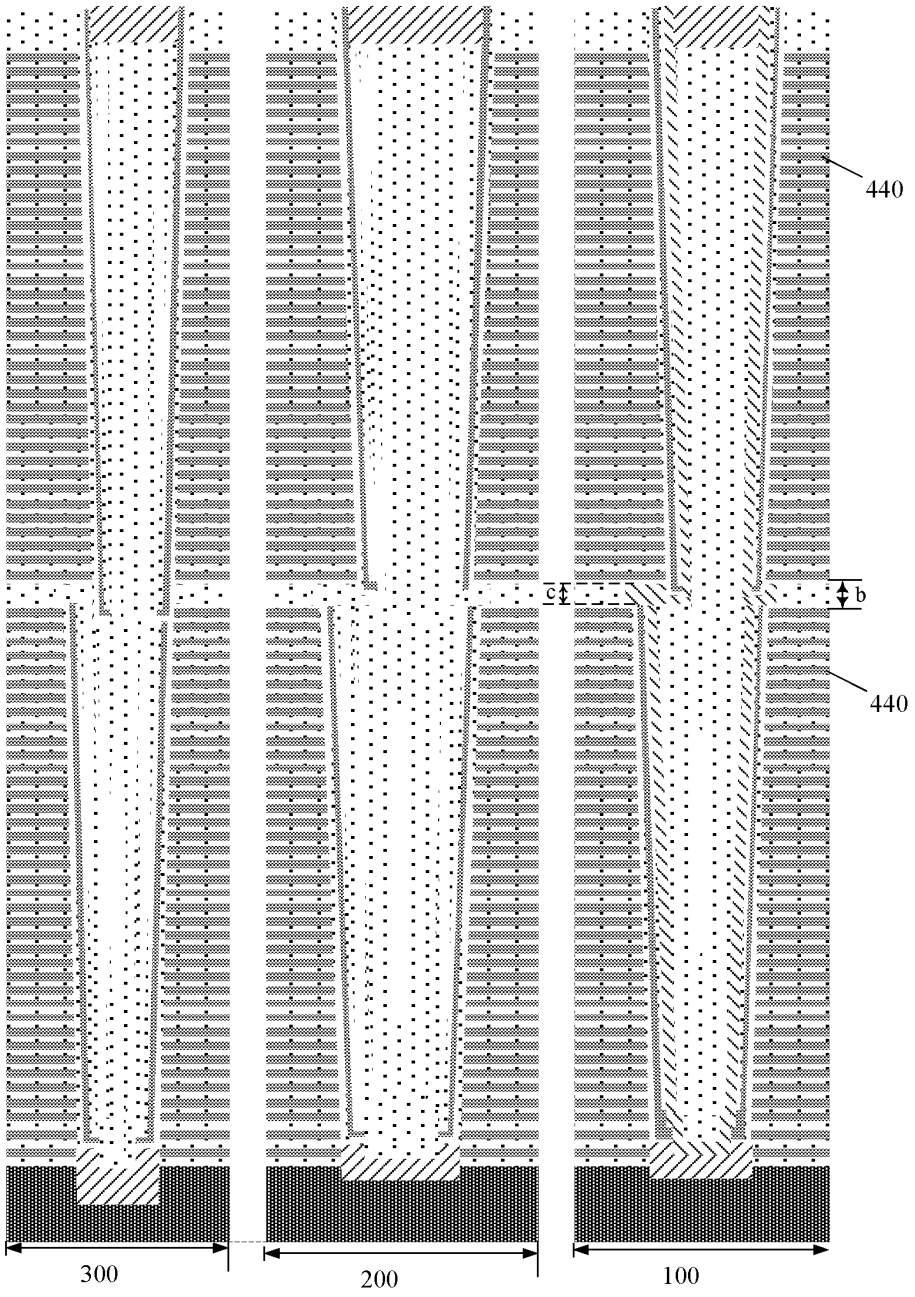


FIG. 102A

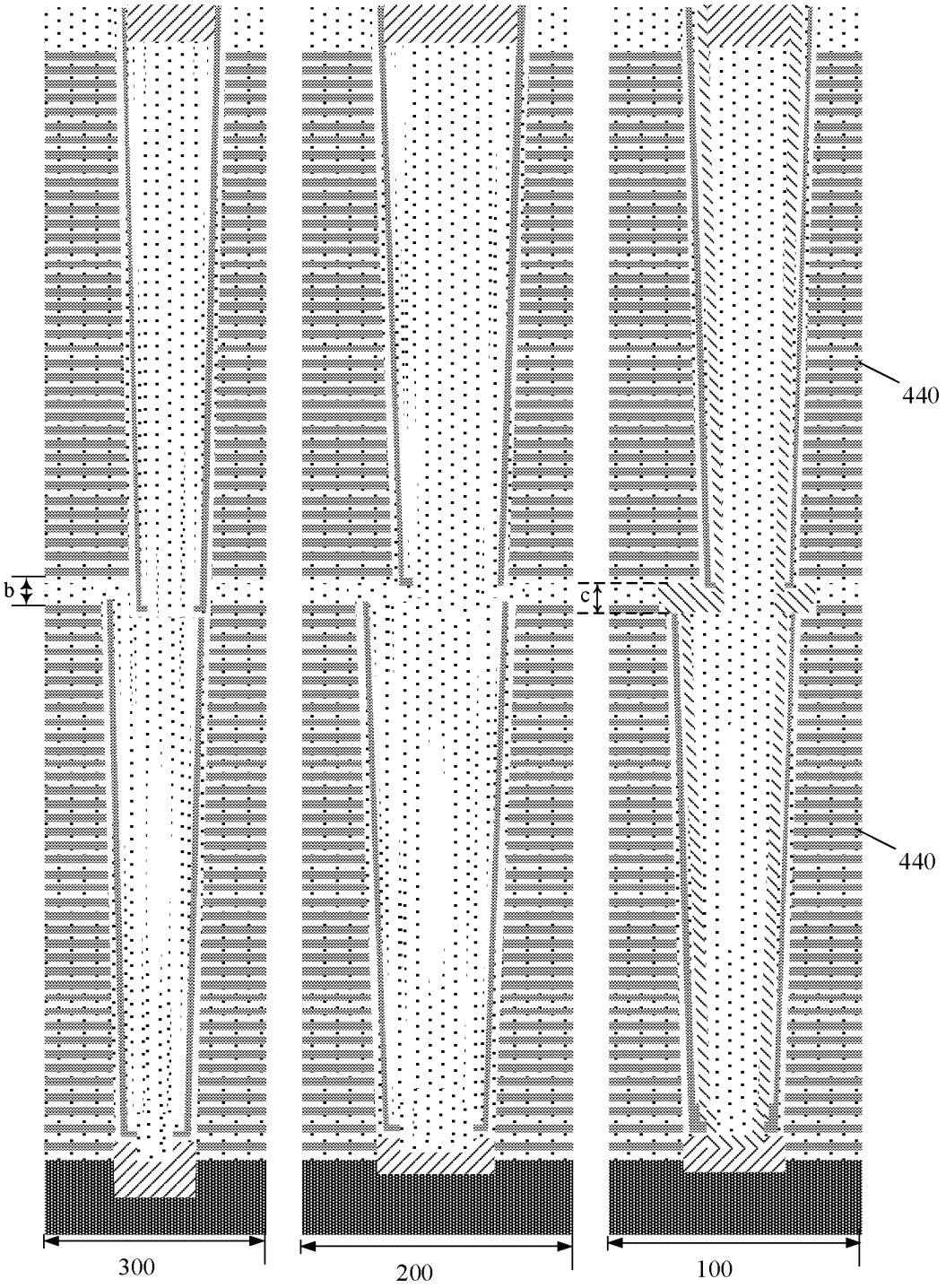


FIG. 102B

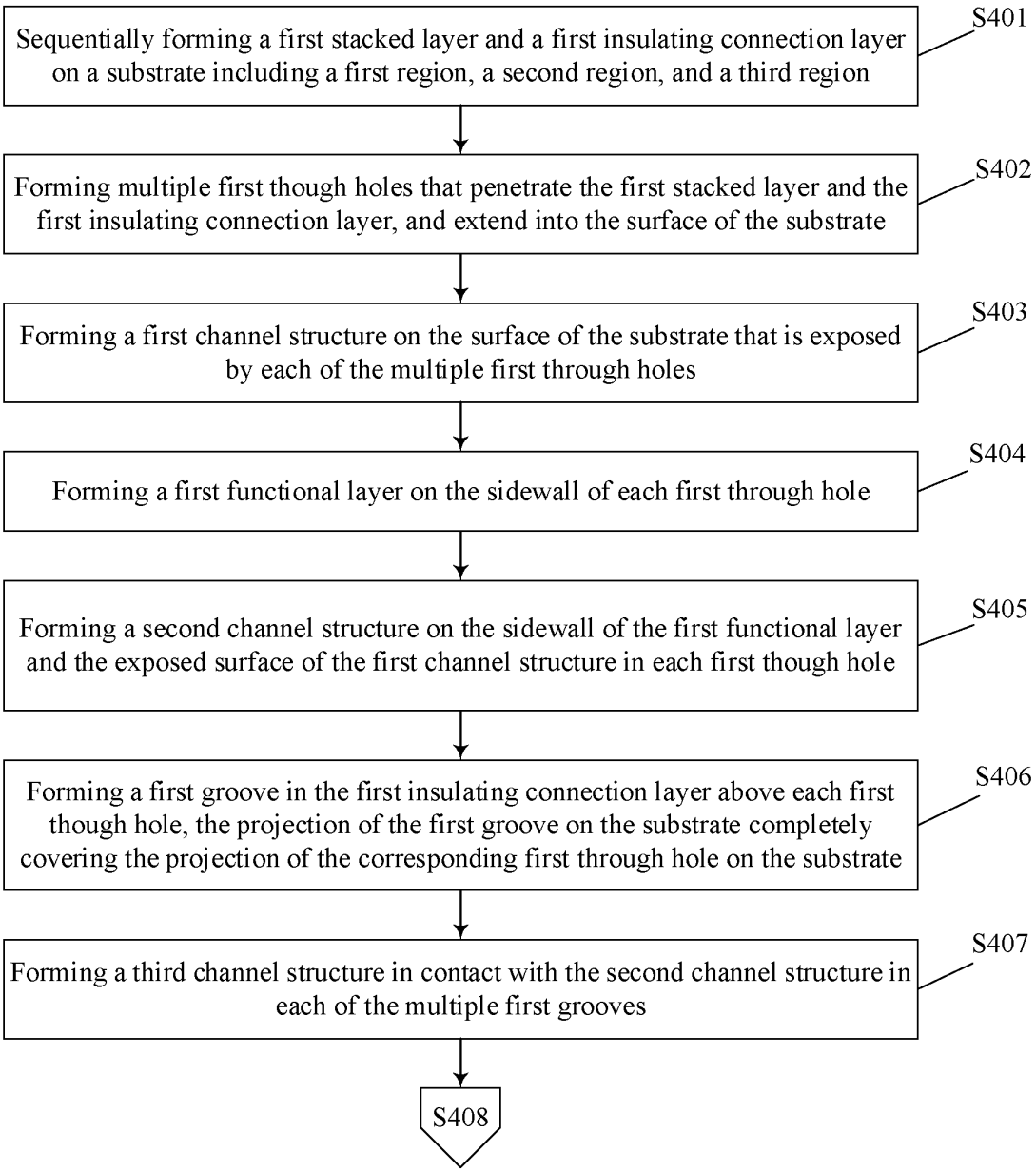

Sequentially forming a first stacked layer and a first insulating connection layer on a substrate including a first region, a second region, and a third region
S401
Forming multiple first though holes that penetrate the first stacked layer and the first insulating connection layer, and extend into the surface of the substrate
S402
Forming a first channel structure on the surface of the substrate that is exposed by each of the multiple first through holes
S403
Forming a first functional layer on the sidewall of each first through hole
S404
Forming a second channel structure on the sidewall of the first functional layer and the exposed surface of the first channel structure in each first though hole
S405
Forming a first groove in the first insulating connection layer above each first though hole, the projection of the first groove on the substrate completely covering the projection of the corresponding first through hole on the substrate
S406
Forming a third channel structure in contact with the second channel structure in each of the multiple first grooves
S407
S408

FIG. 103A

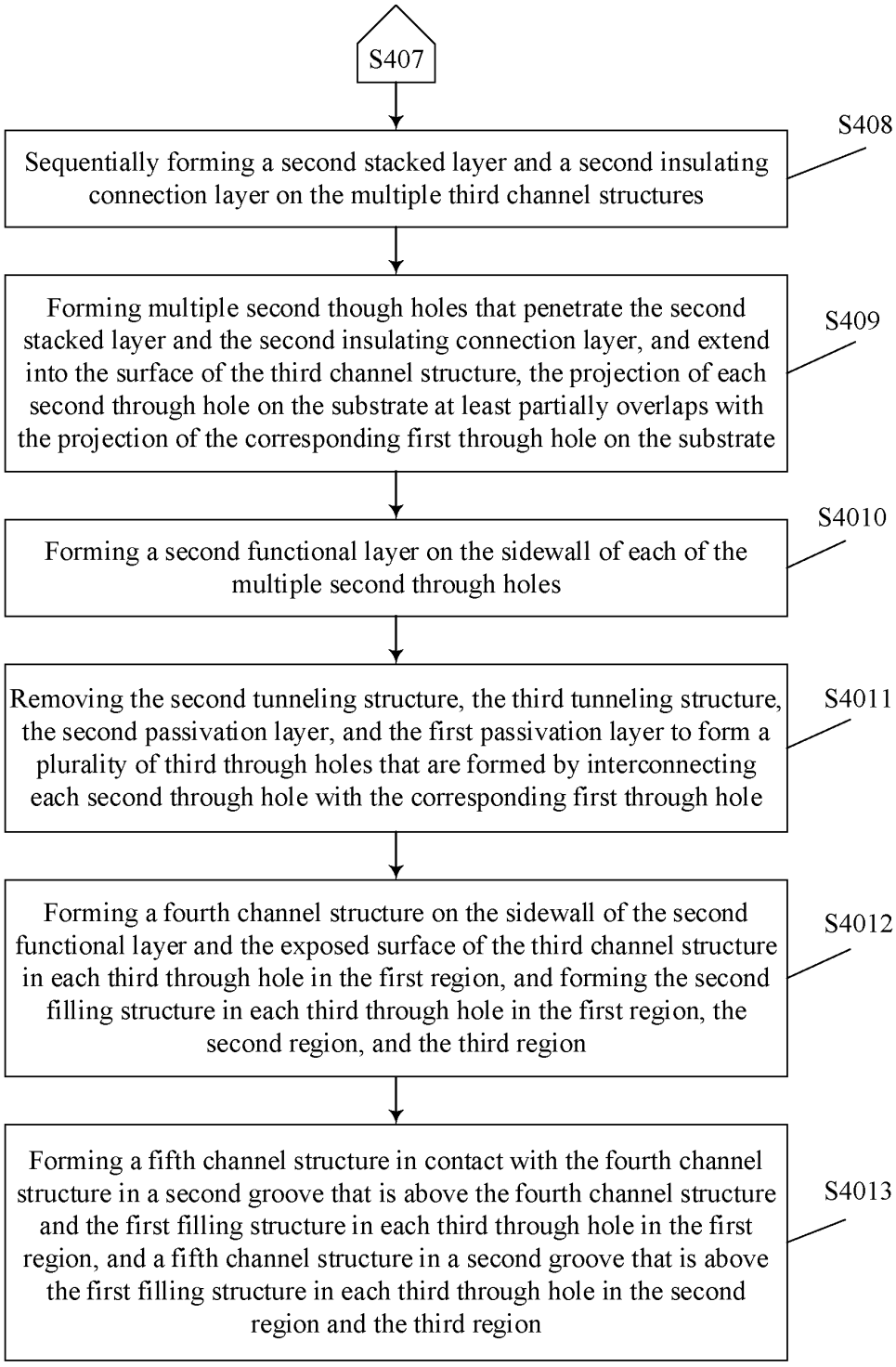

S407
S408
Sequentially forming a second stacked layer and a second insulating connection layer on the multiple third channel structures
S409
Forming multiple second though holes that penetrate the second stacked layer and the second insulating connection layer, and extend into the surface of the third channel structure, the projection of each second through hole on the substrate at least partially overlaps with the projection of the corresponding first through hole on the substrate
S4010
Forming a second functional layer on the sidewall of each of the multiple second through holes
S4011
Removing the second tunneling structure, the third tunneling structure, the second passivation layer, and the first passivation layer to form a plurality of third through holes that are formed by interconnecting each second through hole with the corresponding first through hole
S4012
Forming a fourth channel structure on the sidewall of the second functional layer and the exposed surface of the third channel structure in each third through hole in the first region, and forming the second filling structure in each third through hole in the first region, the second region, and the third region
S4013
Forming a fifth channel structure in contact with the fourth channel structure in a second groove that is above the fourth channel structure and the first filling structure in each third through hole in the first region, and a fifth channel structure in a second groove that is above the first filling structure in each third through hole in the second region and the third region

FIG. 103B

ABSTRACT

Joint opening structures of 3D memory devices and fabricating method are provided. A joint opening structure comprises a first through hole penetrating a first stacked layer and a first insulating connection layer, a first channel structure at the bottom of the first through hole, a first functional layer on the sidewall of the first through hole, a second channel structure on the sidewall of the first functional layer, a third channel structure over the first through hole, a second stacked layer on the third channel structure, a second insulating connection layer on the second stacked layer, a second through hole penetrating the second stacked layer and the second insulating connection layer, a second functional layer disposed on the sidewall of the second through hole, a fourth channel structure on the sidewall of the second functional layer, and a fifth channel structure over the second through hole.

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WHAT IS CLAIMED IS:

1. A method of forming a joint opening structure in a three-dimensional (3D) memory device, comprising:

forming a first stacked layer and forming a first insulating connection layer on the first stacked layer;

forming a first through hole that penetrates the first stacked layer and the first insulating connection layer;

forming a first channel structure overlaying the surface of the substrate that is exposed by the first through hole;

forming a first functional layer on the sidewall of the first through hole;

forming a second channel structure and forming a first filling structure on the sidewall of the first functional layer and the exposed surface of the first channel structure;

forming a third channel structure in contact with the second channel structure above the first through hole, wherein a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate;

forming a second stacked layer and forming a second insulating connection layer on the first insulating connection layer;

forming a second through hole that penetrates the second stacked layer and the second insulating connection layer, wherein a projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate;

forming a second functional layer on the sidewall of the second through hole;

forming a fourth channel structure and forming a second filling structure on the sidewall of the second functional layer and the exposed surface of the third channel structure; and

forming a fifth channel structure in contact with the fourth channel structure above the second through hole.

2. The method of claim 1, wherein:

the first stacked layer includes a first number of oxide/nitride layer pairs; and

the second stacked layer includes a second number of oxide/nitride layer pairs.

3. The method of claim 2, wherein:

the first number and the second number are not less than 32.

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4. The method of claim 1, wherein forming the first functional layer comprises:

forming a first tunneling layer on the sidewall of the first through hole and the exposed surface of the first channel structure, wherein the first tunneling layer is configured, in operation, to generate charges;

forming a first storage layer on the surface of the first tunneling layer to store the charges generated by the first tunneling layer;

forming a first barrier layer on the surface of the first storage layer to block the outflow of charges in the first storage layer;

forming a first passivation layer on the surface of the first barrier layer to protect the first barrier layer from being damaged in a subsequent removal process; and

removing portions of the first passivation layer, the first barrier layer, the first storage layer, and the first tunneling layer on the surface of the first channel structure, wherein remaining portions of the first passivation layer, the first barrier layer, the first storage layer, and the first tunneling layer on the sidewall of the first through hole to form the first functional layer.

5. The method of claim 4, wherein forming the second channel structure and the first filling structure comprises:

forming a second channel layer that covers the sidewall of the first passivation layer and the exposed surface of the first channel layer;

forming the first filling layer that covers the surface of the second channel layer;

removing a portion of the first filling layer to form the first filling structure, wherein the top surface of the first filling structure is lower than the top surface of the first insulating connection layer; and

removing a portion of the second channel layer to form the second channel structure, wherein a top surface of the second channel structure is lower than a top surface of the first insulating connection layer.

6. The method of claim 1, wherein forming the third channel structure comprises:

etching the first insulating connection layer to form a first groove, wherein a projection of the first groove on the substrate covers the projection of the first through hole on the substrate;

forming a third channel layer in the first groove, wherein the third channel layer is in contact with the second channel structure; and

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planarizing the top surfaces of the first insulating connection layer and the third channel layer to form the third channel structure.

7. The method of claim 1, wherein forming the third channel structure comprises:

etching the first insulating connection layer and at least a portion of the top nitride layer of the first stacked layer to form a first groove, wherein a projection of the first groove on the substrate covers the projection of the first through hole on the substrate;

forming the third channel structure in the first groove, wherein the third channel structure is in contact with the second channel structure; and

planarizing the top surfaces of the first insulating connection layer and the third channel structure.

8. The method of claim 1, further comprising:

forming a first mask layer overlaying the first insulating connection layer before forming the first through hole; and

removing the first mask layer after forming the first filling structure;

forming a second mask layer on the second insulating connection layer before forming the second through hole; and

removing the second mask layer after forming the second filling structure.

9. The method of claim 1, wherein forming the fourth channel structure and the second filling structure comprises:

forming a fourth channel layer that covers the sidewall of a second functional layer and the exposed surface of the third channel layer;

forming a second filling layer that covers the surface of the fourth channel layer;

removing a portion of the second filling layer to form the second filling structure, wherein the top surface of the second filling structure is lower than the top surface of the second insulating connection layer; and

removing a portion of the fourth channel layer to form the fourth channel structure, wherein a top surface of the fourth channel structure is lower than a top surface of the second insulating connection layer.

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10. The method of claim 1, wherein forming the fifth channel structure comprises:

etching the second insulating connection layer to form a second groove, wherein a projection of the second groove on the substrate covers the projection of the second through hole on the substrate;

forming a fifth channel layer in the second groove, wherein the fifth channel layer is in contact with the fourth channel structure; and

planarizing the top surfaces of the second insulating connection layer and the fifth channel layer to form the fifth channel structure.

11. A joint opening structure of a three-dimensional (3D) memory device, comprising:

a first stacked layer disposed overlaying a substrate;

a first insulating connection layer disposed on the first stacked layer;

a first through hole penetrating the first stacked layer and the first insulating connection layer;

a first channel structure disposed at the bottom of the first through hole and overlaying the substrate;

a first functional layer disposed on the sidewall of the first through hole;

a second channel structure in contact with the first channel structure disposed on the sidewall of the first functional layer;

a third channel structure in contact with the second channel structure disposed over the first through hole, wherein a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate;

a second stacked layer disposed on the third channel structure;

a second insulating connection layer disposed on the second stacked layer;

a second through hole penetrating the second stacked layer and the second insulating connection layer, wherein a projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate;

a second functional layer disposed on the sidewall of the second through hole;

a fourth channel structure in contact with the third channel structure disposed on the sidewall of the second functional layer; and

a fifth channel structure in contact with the fourth channel structure disposed over the second through hole.

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12. The joint opening structure of claim 11, further comprising:

a first filling structure covering the surface of the second channel structure; and

a second filling structure covering the surface of the fourth channel structure;

wherein the first through hole is non-interconnected with the second through hole.

13. The joint opening structure of claim 11, further comprising:

a first filling structure covering the surfaces of the second channel structure and the fourth channel structure;

wherein the first through hole is interconnected with the second through hole.

14. The joint opening structure of claim 11, wherein:

the first stacked layer includes a first number of conductor/dielectric layer pairs; and

the second stacked layer includes a second number of conductor/dielectric layer pairs.

15. The joint opening structure of claim 14, wherein:

the first number and the second number are not less than 32.

16. The joint opening structure of claim 11, wherein:

the first stacked layer includes a first number of oxide/nitride layer pairs; and

the second stacked layer includes a second number of oxide/nitride layer pairs.

17. The joint opening structure of claim 16, wherein:

the first number and the second number are not less than 32.

18. The joint opening structure of claim 11, wherein:

a thickness of the third channel structure is in a range between 30nm and 70nm.

19. The joint opening structure of claim 11, wherein:

a size difference between a top aperture and a bottom aperture of the first through hole is equal to or less than 30nm; and

a size difference between a top aperture and a bottom aperture of the second through hole is equal to or less than 30nm.

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20. A joint opening structure of a three-dimensional (3D) memory device, comprising:

a first stacked layer disposed overlaying a substrate;

a first insulating connection layer disposed on the first stacked layer;

a second stacked layer disposed on the first insulating connection layer;

a second insulating connection layer disposed on the second stacked layer;

a plurality of channel holes in a first region of the 3D memory device;

a plurality of staircase structure dummy holes in a second region of the 3D memory device; and

a plurality of through array contact barriers in a third region of the 3D memory device;

wherein each of the plurality of channel holes includes:

a first through hole penetrating the first stacked layer and the first insulating connection layer,

a first channel structure disposed at the bottom of the first through hole and overlaying the substrate,

a first functional layer disposed on the sidewall of the first through hole,

a second channel structure in contact with the first channel structure disposed on the sidewall of the first functional layer,

a third channel structure in contact with the second channel structure disposed over the first through hole, wherein a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate,

a second through hole penetrating the second stacked layer and the second insulating connection layer, wherein a projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate,

a second functional layer disposed on the sidewall of the second through hole,

a fourth channel structure in contact with the third channel structure disposed on the sidewall of the second functional layer, and

a fifth channel structure in contact with the fourth channel structure disposed over the second through hole.

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JOINT OPENNING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application claims priority to PCT/CN2018/077785 filed on March 1, 2018, which claims the priorities of Chinese Patent Application No. 201710134782.1, filed on March 8, 2017, and Chinese Patent Application No. 201710134783.6, filed on March 8, 2017, the entire contents of which are incorporated herein by reference.

TECHNICAL FIELD

[0002] The present disclosure generally relates to the field of semiconductor technology, and more particularly, to joint opening structures of three-dimensional (3D) memory devices and method for forming the same.

BACKGROUND

[0003] As semiconductor technology advances, three-dimensional (3D) memory devices, such as 3D NAND memory devices, keep scaling more oxide/nitride (ON) layers. As such, it becomes difficult to use a single etching process to form the channel holes in the 3D memory devices that have a substantial depth. As the channel hole aspect ratio increases, channel hole etching becomes exponentially slower. Further, the process capability control of the formed channel holes, including bow-free, straight profile, critical dimension (CD) uniformity, minimal twisting, etc., tend to be more challenging. Thus, a single etching method may not be efficient in both cost and process capability.

BRIEF SUMMARY

[0004] In accordance with some embodiments of the present disclosure, joint opening structures of three-dimensional (3D) memory devices and method for forming the same are provided.

[0005] One aspect of the present disclosure provides a method of forming a joint opening structure in a three-dimensional (3D) memory device. The method includes forming a

first stacked layer and forming a first insulating connection layer on the first stacked layer, forming a first through hole that penetrates the first stacked layer and the first insulating connection layer, forming a first channel structure overlay the surface of the substrate that is exposed by the first through hole, forming a first functional layer on the sidewall of the first through hole, forming a second channel structure and forming a first filling structure on the sidewall of the first functional layer and the exposed surface of the first channel structure, and forming a third channel structure in contact with the second channel structure above the first through hole. A projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate. The method further includes forming a second stacked layer and forming a second insulating connection layer on the first insulating connection layer, forming a second through hole that penetrates the second stacked layer and the second insulating connection layer. A projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate. The method further includes forming a second functional layer on the sidewall of the second through hole, forming a fourth channel structure and forming a second filling structure on the sidewall of the second functional layer and the exposed surface of the third channel structure, and forming a fifth channel structure in contact with the fourth channel structure above the second through hole.

[0006] In some embodiments, the first stacked layer includes a first number of oxide/nitride layer pairs, and the second stacked layer includes a second number of oxide/nitride layer pairs. The first number and the second number are not less than 32.

[0007] Forming the first functional layer includes forming a first tunneling layer on the sidewall of the first through hole and the exposed surface of the first channel structure. The first tunneling layer is configured, in operation, to generate charges. Forming the first functional further includes forming a first storage layer on the surface of the first tunneling layer to store the charges generated by the first tunneling layer, forming a first barrier layer on the surface of the first storage layer to block the outflow of charges in the first storage layer, forming a first passivation layer on the surface of the first barrier layer to protect the first barrier layer from being damaged in a subsequent removal process, and removing portions of the first passivation layer, the first barrier layer, the first storage layer, and the first tunneling layer on the surface of the first channel structure. The remaining portions of the first passivation layer, the first barrier layer, the first storage

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layer, and the first tunneling layer on the sidewall of the first through hole form the first functional layer.

[0008] Forming the second channel structure and the first filling structure includes forming a second channel layer that covers the sidewall of the first passivation layer and the exposed surface of the first channel layer, forming the first filling layer that covers the surface of the second channel layer, removing a portion of the first filling layer to form the first filling structure, wherein the top surface of the first filling structure is lower than the top surface of the first insulating connection layer, and removing a portion of the second channel layer to form the second channel structure. A top surface of the second channel structure is lower than a top surface of the first insulating connection layer.

[0009] Forming the third channel structure includes etching the first insulating connection layer to form a first groove. In some other embodiments, forming the third channel structure includes etching the first insulating connection layer and at least a portion of the top nitride layer of the first stacked layer to form a first groove. A projection of the first groove on the substrate covers the projection of the first through hole on the substrate. Forming the third channel structure further includes forming a third channel layer in the first groove, wherein the third channel layer is in contact with the second channel structure, and planarizing the top surfaces of the first insulating connection layer and the third channel layer to form the third channel structure.

[0010] In some embodiments, the method further includes forming a first mask layer overlaying the first insulating connection layer before forming the first through hole, and removing the first mask layer after forming the third channel structure, and forming a second mask layer on the second insulating connection layer before forming the second through hole, and removing the first mask layer after forming the fifth channel structure

[0011] Forming the fourth channel structure and the second filling structure includes forming a fourth channel layer that covers the sidewall of the second functional layer and the exposed surface of the third channel layer, forming a second filling layer that covers the surface of the fourth channel layer, removing a portion of the second filling layer to form the second filling structure, and removing a portion of the fourth channel layer to form the fourth channel structure, wherein a top surface of the fourth channel structure is lower than a top surface of the second insulating connection layer. A top surface of the second filling structure is lower than the top surface of the second insulating connection layer.

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[0012] Forming the fifth channel structure includes etching the second insulating connection layer to form a second groove, forming a fifth channel layer in the second groove, wherein the fifth channel layer is in contact with the fourth channel structure, and planarizing the top surfaces of the second insulating connection layer and the fifth channel layer to form the fifth channel structure. A projection of the second groove on the substrate covers the projection of the second through hole on the substrate.

[0013] Another aspect of the present disclosure provides another method of forming a joint opening structure in a three-dimensional (3D) memory device. The method includes forming a first stacked layer and forming a first insulating connection layer on a substrate of the 3D memory device. The 3D memory device includes a first region for forming a plurality of channel holes, a second region for forming a plurality of staircase structure dummy holes, and a third region for forming a plurality of through array contact barriers. The method further includes forming a plurality of first through holes, each penetrating the first stacked layer and the first insulating connection layer in the first region, the second region, and the third region, forming a first channel structure overlaying the surface of the substrate in each first through hole, forming a first functional layer on the sidewall of each first through hole, forming a second channel structure and forming a first filling structure on the sidewall of the first functional layer and the exposed surface of the first channel structure in each first through hole, forming a third channel structure in contact with the second channel structure above each first through hole. A projection of the third channel structure on the substrate covers a projection of the corresponding first through hole on the substrate. The method further includes forming a second stacked layer on the first insulating connection layer, forming a second insulating connection layer on the second stacked layer, forming a plurality of second through holes, each penetrating the second stacked layer and the second insulating connection layer. A projection of each of the plurality of second through holes on the substrate at least partially overlaps with the projection of the corresponding first through hole on the substrate. The method further includes forming a second functional layer on the sidewall of each second through hole, forming a fourth channel structure and forming a second filling structure on the sidewall of the second functional layer and the exposed surface of the third channel structure in each second through hole in the first region, and forming a second filling structure on the sidewall of the second functional layer in each second through hole in the second region and the third region, and forming a fifth channel

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structure above each second through hole in the first region, the second region, and the third region. Each fifth channel structure is in contact with the corresponding fourth channel structure in each second through hole in the first region.

[0014] Forming the fourth channel structure and the second filling structure includes forming a fourth channel layer that covers the sidewall of the first passivation layer and the exposed surface of the third channel layer, forming a third filling layer that covers the surface of the fourth channel layer, forming a third mask layer that covers the third filling layer in the first region, and using the third mask layer as a mask to remove the third filling layer in the second region and the third region, removing the third mask layer;, using the third filling layer in the first region as a mask to remove the fourth channel layer in the second region and the third region, forming a fourth filling layer on the surface of the second functional layer in the second region and the third region, removing the third filling layer in the first region, forming a second filling layer in each second through hole in the first region, the second region, and the third region, removing a portion of the second filling layer to form the second filling structure in each second through hole, and removing a portion of the fourth channel layer to form the fourth channel structure in each second through hole. The top surface of the second filling structure is lower than the top surface of the second insulating connection layer, and the top surface of the fourth channel structure is lower than the top surface of the second insulating connection layer.

[0015] Another aspect of the present disclosure provides annother method of forming a joint opening structure in a three-dimensional (3D) memory device. The method includes forming a first stacked layer and forming a first insulating connection layer on a substrate, forming a first through hole that penetrates the first stacked layer and the first insulating connection layer, forming a first channel structure overlay the surface of the substrate that is exposed by the first through hole, forming a first functional layer on the sidewall of the first through hole, forming a second channel on the sidewall of the first functional layer and the exposed surface of the first channel structure, forming a third channel structure in contact with the second channel structure above the first through hole. A projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate. The method further includes forming a second stacked layer and forming a second insulating connection layer on the third channel structure, forming a second through hole that penetrates the second stacked layer and the second insulating connection layer. A projection of the second through hole on the substrate at least

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partially overlaps with the projection of the first through hole on the substrate. The method further includes forming a second functional layer on the sidewall of the second through hole, removing portions of the second functional layer and the third channel structure at the bottom of the second through hole to interconnect the second through hole and the first through hole to form a joint through hole, removing the remaining portion of the third channel structure and the second channel structure, forming a fourth channel structure in contact with the first channel structure on the sidewall of the joint through hole and the exposed surface of the first insulating connection layer, forming a first filling structure that covers the surface of the fourth channel structure, and forming a fifth channel structure in contact with the fourth channel structure above the joint through hole.

[0016] Another aspect of the present disclosure provides another method of forming a joint opening structure in a three-dimensional (3D) memory device. The method includes forming a first stacked layer and forming a first insulating connection layer on a substrate of the 3D memory device. The 3D memory device includes a first region for forming a plurality of channel holes, a second region for forming a plurality of staircase structure dummy holes, and a third region for forming a plurality of through array contact barriers. The method further includes forming a plurality of first through holes, each penetrating the first stacked layer and the first insulating connection layer in the first region, the second region, and the third region, forming a first channel structure on the surface of the substrate in each first through hole, forming a first functional layer on the sidewall of each first through hole, forming a second channel structure on the sidewall of the first functional layer and the exposed surface of the first channel structure in each first through hole, forming a third channel structure in contact with the second channel structure above each first through hole. A projection of the third channel structure on the substrate covers a projection of the corresponding first through hole on the substrate. The method further includes forming a second stacked layer and forming a second insulating connection layer on the plurality of third channel structures, forming a plurality of second through holes, each penetrating the second stacked layer and the second insulating connection layer. A projection of each of the plurality of second through holes on the substrate at least partially overlaps with the projection of the corresponding first through hole on the substrate. The method further includes forming a second functional layer on the sidewall of each second through hole, removing portions of the second functional layer and the third channel structure at the bottom of each second through hole to interconnect the

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second through hole and the corresponding first through hole to form a plurality of joint through holes, removing the remaining portions of the third channel structure and the second channel structure in each joint through hole, forming a fourth channel structure in contact with the first channel structure on the sidewall of each joint through hole and the exposed surfaces of the first insulating connection layer, forming a first filling structure that covers the surface of the fourth channel structure in each joint through hole, and forming a fifth channel structure above each joint through hole in the first region, the second region, and the third region. Each fifth channel structure is in contact with the corresponding fourth channel structure in each joint through hole in the first region.

[0017] Another aspect of the present disclosure provides a joint opening structure of a three-dimensional (3D) memory device, including a first stacked layer disposed overlaying a substrate, a first insulating connection layer disposed on the first stacked layer, a first through hole penetrating the first stacked layer and the first insulating connection layer, a first channel structure disposed at the bottom of the first through hole and overlaying the surface of the substrate, a first functional layer disposed on the sidewall of the first through hole, a second channel structure in contact with the first channel structure disposed on the sidewall of the first functional layer, a third channel structure in contact with the second channel structure disposed over the first through hole. A projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate. The joint opening structure further includes a second stacked layer disposed on the third channel structure, a second insulating connection layer disposed on the second stacked layer. A second through hole penetrating the second stacked layer and the second insulating connection layer. A projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate. The joint opening structure further includes a second functional layer disposed on the sidewall of the second through hole, a fourth channel structure in contact with the third channel structure disposed on the sidewall of the second functional layer, and a fifth channel structure in contact with the fourth channel structure disposed over the second through hole.

[0018] In some embodiments, a first filling structure covers the surface of the second channel structure, and a second filling structure covers the surface of the fourth channel structure. The first through hole is non-interconnected with the second through hole.

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[0019] In some other embodiments, a first filling structure covers the surfaces of the second channel structure and the fourth channel structure. The first through hole is interconnected with the second through hole.

[0020] In some embodiments, the first stacked layer includes a first number of conductor/dielectric layer pairs, and the second stacked layer includes a second number of conductor/dielectric layer pairs.

[0021] In some other embodiments, the first stacked layer includes a first number of oxide/nitride layer pairs, and the second stacked layer includes a second number of oxide/nitride layer pairs. The first number and the second number are not less than 32.

[0022] A thickness of the third channel structure is in a range between 30nm and 70nm. A size difference between a top aperture and a bottom aperture of the first through hole is equal to or less than 30nm. A size difference between a top aperture and a bottom aperture of the second through hole is equal to or less than 30nm.

[0023] Another aspect of the present disclosure provides a three-dimensional (3D) memory device, including a first stacked layer disposed on a substrate, a first insulating connection layer disposed on the first stacked layer, a second stacked layer disposed on the first insulating connection layer, a second insulating connection layer disposed on the second stacked layer, a plurality of channel holes in a first region of the 3D memory device, a plurality of staircase structure dummy holes in a second region of the 3D memory device, and a plurality of through array contact barriers in a third region of the 3D memory device. Each of the plurality of channel holes includes the disclosed joint opening structure.

[0024] Other aspects of the present disclosure can be understood by those skilled in the art in light of the description, the claims, and the drawings of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] Various objectives, features, and advantages of the present disclosure can be more fully appreciated with reference to the detailed description of the present disclosure when considered in contact with the following drawings, in which like reference numerals identify like elements. It is noted that the following drawings are merely examples for illustrative purposes according to various disclosed embodiments and are not intended to limit the scope of the present disclosure.

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[0026] FIGs. 1-22 illustrate schematic structural cross-sectional diagrams of an exemplary joint opening structure of three-dimensional (3D) memory device at certain stages of a fabricating process in accordance with some embodiments of the present disclosure;

[0027] FIGs. 23A and 23B illustrate schematic flow diagrams of an exemplary fabricating process for forming a joint opening structure of three-dimensional (3D) memory device are illustrated in accordance with some embodiments of the present disclosure;

[0028] FIGs. 24-49 illustrate schematic structural cross-sectional diagrams of another exemplary joint opening structure of three-dimensional (3D) memory device at certain stages of another fabricating process in accordance with some embodiments of the present disclosure;

[0029] FIGs. 50A and 50B illustrate schematic flow diagrams of another exemplary fabricating process for forming a joint opening structure of three-dimensional (3D) memory device are illustrated in accordance with some embodiments of the present disclosure;

[0030] FIGs. 51-73 illustrate schematic structural cross-sectional diagrams of another exemplary joint opening structure of three-dimensional (3D) memory device at certain stages of another fabricating process in accordance with some embodiments of the present disclosure;

[0031] FIGs. 74A and 74B illustrate schematic flow diagrams of another exemplary fabricating process for forming a joint opening structure of three-dimensional (3D) memory device are illustrated in accordance with some embodiments of the present disclosure;

[0032] FIGs. 75-102 illustrate schematic structural cross-sectional diagrams of another exemplary joint opening structure of three-dimensional (3D) memory device at certain stages of another fabricating process in accordance with some embodiments of the present disclosure;

[0033] FIGs. 103A and 103B illustrate schematic flow diagrams of another exemplary fabricating process for forming a joint opening structure of three-dimensional (3D) memory device are illustrated in accordance with some embodiments of the present disclosure.

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[0034] Embodiments of the present disclosure will be described with reference to the accompanying drawings.

DETAILED DESCRIPTION

[0035] Reference now be made in detail to exemplary embodiments of the invention, which are illustrated in the accompanying drawings in order to understand and implement the present disclosure and to realize the technical effect. It can be understood that the following description has been made only by way of example, but not to limit the present disclosure. Various embodiments of the present disclosure and various features in the embodiments that are not conflicted with each other can be combined and rearranged in various ways. Without departing from the spirit and scope of the present disclosure, modifications, equivalents, or improvements to the present disclosure are understandable to those skilled in the art and are intended to be encompassed within the scope of the present disclosure.

[0036] It is noted that references in the specification to "one embodiment," "an embodiment," "an example embodiment," "some embodiments," etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in contact with an embodiment, it would be within the knowledge of a person skilled in the pertinent art to effect such feature, structure or characteristic in contact with other embodiments whether or not explicitly described.

[0037] In general, terminology may be understood at least in part from usage in context. For example, the term "one or more" as used herein, depending at least in part upon context, may be used to describe any feature, structure, or characteristic in a singular sense or may be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as "a," "an," or "the," again, may be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context.

[0038] It should be readily understood that the meaning of "on," "above," and "over" in the present disclosure should be interpreted in the broadest manner such that "on" not

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only means "directly on" something but also includes the meaning of "on" something with an intermediate feature or a layer therebetween, and that "above" or "over" not only means the meaning of "above" or "over" something but can also include the meaning it is "above" or "over" something with no intermediate feature or layer therebetween (i.e., directly on something).

[0039] Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper," and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0040] As used herein, the term "substrate" refers to a material onto which subsequent material layers are added. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.

[0041] As used herein, the term "layer" refers to a material portion including a region with a thickness. A layer can extend over the entirety of an underlying or overlying structure, or may have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend horizontally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow. A layer can include multiple layers. For example, an interconnect layer can include one or more conductor and contact layers (in which contacts, interconnect lines, and/or through holes are formed) and one or more dielectric layers.

[0042] As used herein, the term "nominal/nominally" refers to a desired, or target, value of a characteristic or parameter for a component or a process operation, set during the

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design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term "about" indicates the value of a given quantity that can vary based on a particular technology node associated with the subject semiconductor device. Based on the particular technology node, the term "about" can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., ±10%, ±20%, or ±30% of the value).

[0043] In accordance with some embodiments of the present disclosure, joint opening structures of three-dimensional (3D) memory devices and method for forming the same are provided to reduce the process difficulty and cost of the channel hole structures in 3D memory devices.

[0044] As used herein, the term "3D memory device" refers to a semiconductor device with vertically oriented strings of memory cell transistors (referred to herein as "memory strings," such as NAND strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate. As used herein, the term "vertical/vertically" means nominally perpendicular to the lateral surface of a substrate, while the term "horizontal/horizontally" means nominally parallel to the lateral surface of a substrate.

[0045] Referring to FIGs. 23A and 23B, schematic flow diagrams of an exemplary fabricating process for forming a joint opening structure of three-dimensional (3D) memory device are illustrated in accordance with some embodiments of the present disclosure. And FIGs. 1-22 illustrate schematic structural cross-sectional diagrams of an exemplary joint opening structure of three-dimensional (3D) memory device at certain stages of the fabricating process shown in FIGs. 23A and 23B.

[0046] As shown in FIG. 23A, at S101, a first stacked layer 2 and a first insulating connection layer 3 can be sequentially formed on the surface of a substrate 1.

[0047] As shown in FIG. 1, the first stacked layer 2 can be formed on the substrate 1. The first stacked layer 2 can include a plurality of oxide/nitride layer pairs. The plurality of oxide/nitride layer pairs are also referred to herein as an "alternating oxide/nitride stack." That is, in the first stacked layer 2, multiple oxide layers (shown in the areas with dotes) and multiple nitride layers (shown in the areas with meshes) alternate in a vertical direction. In other words, except a top and a bottom layer of a given stack, each of the

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other oxide layers can be sandwiched by two adjacent nitride layers, and each nitride layer can be sandwiched by two adjacent oxide layers.

[0048] Oxide layers can each have the same thickness or have different thicknesses. For example, a thickness of each oxide layer can be in a range from 90nm to 160nm, preferably about 150nm. Similarly, nitride layers can each have the same thickness or have different thicknesses. For example, a thickness of each nitride layer can be in a range from 80nm to 110nm, preferably about 100nm.

[0049] It is noted that, in the present disclosure, the oxide layers and/or nitride layers can include any suitable oxide materials and/or nitride materials. For example, the element of the oxide materials and/or nitride materials can include, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof. In some embodiments, the oxide layers can be silicon oxide layers, and the nitride layers can be silicon nitride layer.

[0050] The first stacked layer 2 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide layers and the nitride layers in the first stacked layer 2 is equal to or larger than 64. In some embodiments, alternating conductor/dielectric stack includes more oxide layers or more nitride layers with different materials and/or thicknesses than the oxide/nitride layer pair.

[0051] The first insulating connection layer 3 can be formed on the first stacked layer 2. In some embodiments, the first insulating connection layer 3 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is noted that, the material of the first insulating connection layer 3 can be different from the material of the nitride layer in the first stacked layer 2.

[0052] Further, in some embodiments, a first mask layer 4 can be formed on the top surface of the first insulating connection layer 3. The first mask layer 4 can include a nitride layer on the top surface of the first insulating connection layer 3, and an oxide layer on the top surface of such nitride layer.

[0053] In some embodiments, the first stacked layer 2, the first insulating connection layer 3, and/or the first mask layer 4 can be formed by using one or more deposition processes. It is noted that, the term "deposition process" used in the present disclosure can be referred to any suitable deposition process including, but not limited to, a chemical vapor deposition (CVD) process, a physical vapor deposition (PVD) process, an atomic layer deposition (ALD) process, and/or any suitable combination thereof.

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[0054] At S102, a first through hole 5 can be formed. As shown in FIG. 1, the first through hole 5 can completely penetrate the first stacked layer 2 and the first insulating connection layer 3, and can extend into the surface of the substrate 1.

[0055] In some embodiments, the first through hole 5 can be formed by etching the first stacked layer 2 and the first insulating connection layer 3 and a subsequent cleaning process. The etching process to form the first through hole 5 can be a wet etching, a dry etching, or a combination thereof.

[0056] In some embodiments, when the first mask layer 4 is formed on the top surface of the first insulating connection layer 3, the etching process also etch the first mask layer 4 to form the first through holes 5.

[0057] At S103, a first channel structure 6 can be formed on the surface of the substrate 1 that is exposed by the first through hole 5, as shown in FIG. 2. In some embodiments, the first channel structure 6 can be a polycrystalline silicon (polysilicon) layer formed by using a selective epitaxial process.

[0058] In some embodiments, the first channel structure 6 may not directly formed on the surface of the substrate 1. One or more layers can be formed between the first channel structure 6 and the substrate 1. That is, the first channel structure 6 is overlay the substrate 1.

[0059] At S104, a first functional layer can be formed on the sidewall of the first through hole 5. The first functional layer can include a first tunneling layer 7, a first storage layer 8, a first barrier layer 9, and a first passivation layer 10.

[0060] As shown in FIG. 3, the first tunneling layer 7 can be formed on the sidewall of the first through hole 5 and the top surface of the first channel structure 6. The first tunneling layer 7 can be used for generating electronic charges (electrons or holes). In some embodiments, the first tunneling layer 7 can be an oxide layer formed by using a deposition process.

[0061] The first storage layer 8 can be formed on the surface of the first tunneling layer 7. The first storage layer 8 can be used for storing electronic charges. The storage or removal of charge in the first storage layer 7 can impact the on/off state and/or a conductance of the semiconductor channel. The first storage layer 7 can include polycrystalline silicon (polysilicon) or silicon nitride. In some embodiments, the first storage layer 8 can be a nitride layer formed by using a deposition process.

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[0062] The first barrier layer 9 can be formed on the surface of the first storage layer 8. The first barrier layer 9 can be used for blocking the outflow of the electronic charges stored in the first storage layer 8. In some embodiments, the first barrier layer 9 can be a silicon oxide layer or a combination of silicon oxide/silicon nitride/silicon oxide (ONO) layers. In some embodiments, the first barrier layer 9 includes high dielectric constant (high-k) dielectrics (e.g., aluminum oxide). In one example, the first barrier layer 9 is an oxide layer formed by using a deposition process.

[0063] As shown in FIG. 4, a first passivation layer 10 can be formed on the surface of the first barrier layer 9. The first passivation layer 10 can be used for protecting the first barrier layer 9 from being damaged in a subsequent removal process. In some embodiments, the first passivation layer 10 can be an amorphous silicon layer formed by using a deposition process.

[0064] The portions of the first passivation layer 10, the first barrier layer 9, the first storage layer 8 and the first tunneling layer 7 located on the top surface of the first channel structure 6 on the bottom of the first through hole 5 can be removed. In some embodiments, the removal process can include an etching process and a cleaning process. As such, the first functional layer can be formed on the sidewall of the first through hole 5.

[0065] In some embodiment, in the same removal process, the first barrier layer 9, the first storage layer 8, the first tunneling layer 7, and the oxide layer of the first mask layer 4 located on the surface of the nitride layer of first mask layer 4 can also be removed. As such, the nitride layer of first mask layer 4 is remained on the surface of the first insulating connection layer 3.

[0066] At S105, a second channel structure and a first filling structure can be sequentially formed on the sidewall of the first functional layer and the exposed surface of the first channel structure 6. The surfaces of the second channel structure and the first filling structure can be lower than the surface of the first insulating connection layer 3.

[0067] As shown in FIG. 5, a second channel layer 11 can be formed to cover the sidewall of the first passivation layer 10, the bottom surface of the first through hole 5. The second channel layer 11 can also cover the top surface of the first insulating connection layer 3, or cover the top surface of the nitride layer of the first mask layer 4. In some embodiments, the second channel layer 11 can be an amorphous silicon layer formed by using a deposition process.

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[0068] As shown in FIG. 6, a first filling layer 12 can be formed to cover the second channel layer 11 and fill the first through hole 5. In some embodiments, the first filling layer 12 can be an oxide layer formed by using a deposition process. In some embodiments, the first filling layer 12 can include one or more airgaps.

[0069] As shown in FIGs. 7A and 7B, a portion of the first filling layer 12 can be removed, so that the top surface of the first filling layer 12 can be lower than the top surface of the first insulating connection layer 3. As such, the remaining portion of the first filling layer 12 in the first through hole 5 can form the first filling structure. In some embodiments, the portion of the first filling layer 12 can be removed by using an etching process. It is noted that, the term "etching process" used in the present disclosure can be referred to any suitable etching process including, but not limit to, a wet etching, a dry etching, or a combination thereof.

[0070] In some embodiments, as shown in FIG. 7A, the top surface of the first filling layer 12 can be higher than the top surface of the second stacker layer 2. For example, the top surface of the first filling layer 12 can be 20nm to 40nm higher than the top surface of the top nitride layer of the second stacker layer 2. Preferably, the top surface of the first filling layer 12 can be about 30nm higher than the top surface of the top nitride layer of the second stacker layer 2.

[0071] In some alternative embodiments, as shown in FIG. 7B, the top surface of the first filling layer 12 can be lower than the top surface of the second stacker layer 2. For example, the top surface of the first filling layer 12 can be 30nm to 40nm lower than the top surface of the top nitride layer of the second stacker layer 2. Preferably, the top surface of the first filling layer 12 can be about 35nm lower than the top surface of the top nitride layer of the second stacker layer 2.

[0072] As shown in FIGs. 8A and 8B, a portion of the second channel layer 11 can be removed, such that the surface of the second channel layer 11 is lower than the first insulating connection layer 3. The remaining portion of the second channel layer 11 can form the second channel structure that is in contact with the first channel structure 6. In some embodiments, the portion of the second channel layer 11 can be removed by using an etching process.

[0073] It is noted that, in various embodiments, the top surface of the second channel structure can be higher or lower than the top surface of the first stacked layer 2. However, the top surface of the second channel structure is not lower than the top surface

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of the top oxide layer in the first stacked layer 2. In some embodiments, the top surface of the second channel structure can be higher than the top nitride layer in the first stacked layer 2, as shown in FIG. 8A. In some alternative embodiments, the top surface of the second channel structure is in a same plane of the top surface of the top oxide layer in the first stacked layer 2, as shown in FIG. 8B.

[0074] At S106, a first groove can be formed in the first insulating connection layer 3. In some embodiments, the projection of the first groove on the substrate 1 can completely cover the projection of the first through hole 5 on the substrate 1.

[0075] As shown in FIGs. 9A and 9B, the nitride layer of the first mask layer 4 can be removed. In some embodiments, the nitride layer of the first mask layer 4 can be removed by using an etching process.

[0076] As shown in FIGs. 10A and 10 B, the surface of the first insulating connection layer 3 can be planarized by using any suitable techniques, such as backside grinding, and/or chemical mechanical polishing (CMP). A portion of the first insulating connection layer 3 can be removed to form the first groove that penetrates the first insulating connection layer 3. An area of the projection "x" of the first groove on the substrate 1 can be larger than an area of the projection "y" of the first through hole 5 on the substrate 1.

[0077] In some embodiments, a depth of the first groove can be equal to or less than the thickness of the planarized first insulating connection layer 3, as shown in FIG. 10A. For example, the depth of the first groove can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 3 is about 90nm, while the depth of the first groove is about 60nm.

[0078] In some alternative embodiments, the depth of the first groove can be greater than the thickness of the planarized first insulating connection layer 3, as shown in FIG. 10B. That is, a portion of the top nitride layer in the first stacked layer 2 can also be removed to form the first groove. For example, the depth of the first groove can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 3 is about 30nm, while the depth of the first groove is about 60nm.

[0079] At S107, a third channel structure 14 can be formed in the first groove 13. As shown in FIGs. 11A and 11B, the third channel structure 14 can be in contact with the

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second channel structure. In some embodiments, the third channel structure can be a polycrystalline silicon player formed by using a deposition process.

[0080] A thickness of the third channel structure 14 can be equal to the depth of the first groove 13. As described above, in some embodiments, a thickness of the third channel structure 14 can be equal to or less than the thickness of the planarized first insulating connection layer 3, as shown in FIG. 11A. For example, the thickness of the third channel structure 14 can be in a range between 50nm and 70nm, preferably about 60nm. In some alternative embodiments, the thickness of the third channel structure 14 can be greater than the thickness of the planarized first insulating connection layer 3, as shown in FIG. 11B. For example, the thickness of the third channel structure 14 can be in a range between 60nm and 80nm, preferably about 70nm.

[0081] Referring to FIG. 23B, at S108, a second stacked layer 15 and a second insulating connection layer 16 can be sequentially formed on the third channel structure 14. As shown in FIG. 12, the second stacked layer 15 can include a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs. Similar to the first stacked layer 2 as described above, the multiple oxide layers (shown in the areas with dotes) and multiple nitride layers (shown in the areas with meshes) in the second stacked layer 15 alternate in a vertical direction. The second stacked layer 15 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide layers and the nitride layers in the second stacked layer 15 is equal to or larger than 64.

[0082] In some embodiments, the second insulating connection layer 16 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is noted that, the material of the second insulating connection layer 16 can be different from the material of the nitride layer in the second stacked layer 15.

[0083] Further, in some embodiments, a second mask layer 17 can be formed on the surface of the second insulating connection layer 16. The second mask layer 17 can include a nitride layer on the surface of the second insulating connection layer 16, and an oxide layer on the surface of such nitride layer.

[0084] At S109, a second through hole 18 is formed. As shown in FIG. 13, the second through hole 18 can completely penetrate the second stacked layer 15 and the second insulating connection layer 16, and can extend into the surface of the third channel

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structure 14. The projection of the second through hole 18 on the substrate 1 can at least partially overlap with the projection of the first through hole 5 on the substrate 1.

[0085] In some embodiments, the second stacked layer 15, the second insulating connection layer 16, the second mask layer 17, and the third channel structure 14 can be etched to form the second through hole 18. The second stacked layer 15, the second insulating connection layer 16, the second mask layer 17, and/or the third channel structure 14 can be etched by using a dry etching process, a wet etching process, or a combination thereof. A cleaning process can then be performed to clean the second through hole 18.

[0086] It is noted that, the second through hole 18 can extend to the surface of the third channel structure 14, or can extend into the third channel structure 14. As such, a fourth channel structure formed subsequently in the second through hole 18 can directly contact the third channel structure.

[0087] In some embodiments, a maximum difference between the radius of the top aperture of each second through hole 18 and the radius of the bottom aperture of the second through hole 18 can be 15nm. That is, as shown in FIG. 13, a distance "a" between the boundary line of the top surface of each second through hole 18 and the boundary of the bottom surface of the second through hole 18 can be no more than 15 nm.

[0088] At S1010, a second functional layer can be formed on the sidewall of the second through hole 18. In some embodiments, the second functional layer can include a second tunneling layer 19, a second storage layer 20, a second barrier layer 21, and a second passivation layer 22.

[0089] As shown in FIG. 14, the second tunneling layer 19 can be formed on the sidewall of the second through hole 18 and the surface of the second channel structure 14. The second tunneling layer 19 can be used for generating electronic charges. In some embodiments, the second tunneling layer 19 can be an oxide layer formed by using a deposition process.

[0090] The second storage layer 20 can be formed on the surface of the second tunneling layer 19. The second storage layer 20 can be used for storing electronic charges. In some embodiments, the second storage layer 20 can be a nitride layer formed by using a deposition process.

[0091] The second barrier layer 21 can be formed on the surface of the second storage layer 20. The second barrier layer 21 can be used for blocking the outflow of the

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electronic charges in the second storage layer 20. In some embodiments, the second barrier layer 21 can be an oxide layer formed by using a deposition process.

[0092] As shown in FIG. 15, a second passivation layer 22 can be formed on the surface of the second barrier layer 21. The second passivation layer 22 can be used for protecting the second barrier layer 21 from being damaged in a subsequent removal process. In some embodiments, the second passivation layer 22 can be an amorphous silicon layer formed by using a deposition process.

[0093] As shown in FIG. 15, the portions of the second passivation layer 22, the second barrier layer 21, the second storage layer 20 and the second tunneling layer 19 that are located on the surface of the second channel structure 14 can be removed. In some embodiments, the removal process can include an etching process and a cleaning process. In some embodiments, the portions of the second passivation layer 22, the second barrier layer 21, the second storage layer 20, the second tunneling layer 19, the oxide layer of the second mask layer 17 that are located on the nitride layer of the second mask layer 17 can also be removed by using an etching process. As such, the second functional layer can be formed on the sidewall of the second through hole 18.

[0094] At S1012, a fourth channel structure and a second filling structure can be sequentially formed on the sidewall of the second functional layer and the exposed surface of the third channel structure. In some embodiments, the top surface of the fourth channel structure can be higher than the top surface of the second filling structure.

[0095] As shown in FIG. 16, a fourth channel layer 23 can be formed to cover the sidewall of the second passivation layer 22 and the bottom surface of the second through hole 18. In some embodiments, the fourth channel layer 23 can also cover the surface of the second insulating connection layer 16, or the surface of the nitride layer of the second mask layer 17. In some embodiments, the fourth channel layer 23 can be an amorphous silicon layer formed by using a deposition process.

[0096] As shown in FIG. 17, a second filling layer 29 can be formed to cover the fourth channel layer 23 and to fill the second through hole 18. In some embodiments, the second filling layer 29 can be an oxide layer formed by using a deposition process.

[0097] As shown in FIG. 18, a portion of the second filling layer 29 can be removed, such that the surface of the second filling layer 29 is lower than the surface of the second insulating connection layer 16. In some embodiments, the removal process can include

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an etching process. The remaining portion of the second filling layer 29 in the second through hole 18 can form the second filling structure.

[0098] As shown in FIG. 19, the portion of the fourth channel layer 23 located on the surface of the second insulating connection layer 16 or the surface of the second mask layer 17 can be removed. In some embodiments, the removal process can include an etching process. The remaining portion of the fourth channel layer 23 in the second through hole 18 can form the fourth channel structure. The top surface of the fourth channel structure can be higher than the top surface of the second filling structure. As such, a second groove can be formed on the fourth channel structure and the second filling structure, and in the second through hole 18.

[0099] It is noted that, the top surface of the fourth channel structure can be higher than the top surface of the second stacked layer 15, or can be lower than the top surface of the second stacked layer 15. The top surface of the fourth channel structure is not lower than the top surface of the top oxide layer in the second stacked layer 15. In some embodiments, the top surface of the fourth channel structure can be in a same plane of the top surface of the top oxide layer in the second stacked layer 15.

[00100] At S1013, a fifth channel structure can be formed in the second groove. The fifth channel structure can be in contact with the fourth channel structure. As shown in FIG. 20, the fifth channel structure 30 can be formed in the second groove that is on the fourth channel structure and the second filling structure and in the second through hole 18. The nitride layer of the second mask layer 17 can be then removed by an etching process.

[00101] As shown in FIGs. 21A and 21B, the top surface of the second insulating connection layer 16 and the top surface of the fifth channel structure 30 can be planarized by any suitable techniques, such as backside grinding, and/or chemical mechanical polishing (CMP).

[00102] Accordingly, the disclosed method as shown in FIGs. 23A and 23B can form a joint opening structure of a three-dimensional (3D) memory device by combining two through hole formation processes. As such, the formed channel hole having the joint opening structure can have a large aspect ratio and a limited top-bottom aperture error. Further, the disclosed method of forming a joint opening structure in a 3D memory device can result in an efficient process capability control, a simplified process complexity, and a reduced cost.

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[00103] In some embodiments, the present disclosure also provides a three-dimensional memory device formed by using the above disclosed method as shown in FIGs. 23A and 23B. The three-dimensional memory can include the following components described below.

[00104] A first stacked layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer silicon nitride layer pairs, is formed on a substrate. A first insulating connection layer is formed on the first stacked layer. A first through hole penetrates the first stacked layer and the first insulating connection layer, and extends into the surface of the substrate.

[00105] A first channel structure is formed on the surface of the substrate exposed by the first through hole. A first functional layer is formed on the sidewall of the first through hole. A second channel structure is formed on the sidewall of the first functional layer and the surface of the first channel structure. A first filling structure is formed on the sidewall and the surface of the second channel structure to fill the first through hole. In some embodiments, an airgap is enclosed in the first filling structure. The top surfaces of the second channel structure and the first filling structure are lower than the top surfaces of the first insulating connection layer.

[00106] A first groove is formed in the first insulating connection layer, and above the first functional layer, the second channel structure and the first filling structure. A projection of the first groove on the substrate completely covers a projection of the first through hole on the substrate. A third channel structure in contact with the second channel structure is formed in the first groove.

[00107] A second stack layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs, is formed on the top surfaces of the first insulating connection layer and the third channel structure. A second insulating connection layer is formed on the second stack layer. A second through hole penetrates through the second stacked layer and the second insulating connection layer, and extends into a surface of the third channel structure. A projection of the second through hole on the substrate at least partially overlaps the projection of the first through hole on the substrate.

[00108] A second functional layer is formed on the sidewall of the second through hole. A fourth channel structure is formed on the sidewall of the second functional layer and the bottom surface of the second through hole. A second filling structure is formed on the

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sidewall and the surface of the fourth channel structure to fill the second through hole. In some embodiments, an airgap is enclosed in the second filling structure. The top surface of the fourth channel structure is higher than the top surface of the second filling structure. A fifth channel structure in contact with the fourth channel structure is formed in a second groove that is surrounded by the second functional layer, and above the fourth channel structure and the second filling structure.

[00109] In some embodiments, as shown in FIG. 21A, a thickness "b" of the first insulating connection layer, which is the distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 80nm and 100nm, preferably about 90nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00110] In some alternative embodiments, as shown in FIG. 21B, a thickness "b" of the first insulating connection layer, which is the distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 20nm and 40nm, preferably about 30nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00111] Further, the difference between the radiuses of the top aperture and the bottom aperture of the second channel structure, and the difference between the radiuses of the top aperture and the bottom aperture of the fourth channel structure can be within 15nm. Accordingly, the disclosed channel hole having a joint opening structure can have a large aspect ratio and a limited top-bottom aperture error.

[00112] In some embodiments, a replacement process can be performed to replace each of the plurality of nitride layers in the first stacked layer 2 and the second stacked layer 15 with a conductive layer 40, as shown in FIGs. 22A and 22B. The conductive layer can include any suitable material that is electronically conductive, including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof.

[00113] In some embodiments, during the replacement process, a portion of the third channel structure 14 that is adjacent with the bottom nitride layer of the second stacked layer 15, or is adjacent with the top nitride layer of the first stacked layer 2 can be converted to an oxide layer by an oxidation process. For example, an etching process can be performed to remove all nitride layers in the first stacked layer 2 and the second stacked layer 15. Then an oxide process can be formed to oxide the exposed surface of the third channel structure. As a result, a portion of the third channel structure can be

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converter to the oxide layer as shown in FIGs. 22A and 22B. In some embodiments,, a thickness "c" of the third channel structure can be reduced after the replacement process. For example, the thickness "c" of the third channel structure can be reduced to a range between 30nm and 50nm, preferably about 40nm.

[00114] Referring to FIGs. 50A and 50B, schematic flow diagrams of another exemplary fabricating process for forming a joint opening structure of three-dimensional (3D) memory device are illustrated in accordance with some other embodiments of the present disclosure. And FIGs. 24-49 illustrate schematic structural cross-sectional diagrams of an exemplary joint opening structure of three-dimensional (3D) memory device at certain stages of the fabricating process shown in FIGs. 50A and 50B.

[00115] As shown in FIG. 50A, at S201, a first stacked layer 202 and a first insulating connection layer 203 can be sequentially formed on the surface of a substrate 201. In some embodiments, the 3D memory device can include a first region 100, a second region 200, and a third region 300, as shown in FIG. 24. The first region 100 can be used to form one or more channel holes, the second region 200 can be used to form one or more staircase structure (SS) dummy holes, while the third region 300 can be used to form one or more through array contact (TAC) barriers.

[00116] As shown in FIG. 24, the first stacked layer 202 can be formed on the substrate 201. The first stacked layer 202 can include a plurality of oxide/nitride layer pairs. That is, in the first stacked layer 202, multiple oxide layers (shown in the areas with dotes) and multiple nitride layers (shown in the areas with meshes) alternate in a vertical direction. In other words, except a top and a bottom layer of a given stack, each of the other oxide layers can be sandwiched by two adjacent nitride layers, and each nitride layer can be sandwiched by two adjacent oxide layers.

[00117] Oxide layers can each have the same thickness or have different thicknesses. For example, a thickness of each oxide layer can be in a range from 90nm to 160nm, preferably about 150nm. Similarly, nitride layers can each have the same thickness or have different thicknesses. For example, a thickness of each nitride layer can be in a range from 80nm to 110nm, preferably about 100nm. In some embodiments, the oxide layers can be silicon oxide layers, and the nitride layers can be silicon nitride layer.

[00118] The first stacked layer 202 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide layers and the nitride layers in the first stacked layer 202 is equal to or larger than 64. In

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some embodiments, alternating conductor/dielectric stack includes more oxide layers or more nitride layers with different materials and/or thicknesses than the oxide/nitride layer pair.

[00119] The first insulating connection layer 203 can be formed on the first stacked layer 202. In some embodiments, the first insulating connection layer 203 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is noted that, the material of the first insulating connection layer 203 can be different from the material of the nitride layer in the first stacked layer 202.

[00120] Further, in some embodiments, a first mask layer 204 can be formed on the surface of the first insulating connection layer 203. The first mask layer 204 can include a nitride layer on the surface of the first insulating connection layer 203, and an oxide layer on the surface of such nitride layer.

[00121] In some embodiments, the first stacked layer 202, the first insulating connection layer 203, and/or the first mask layer 204 can be formed by using one or more deposition processes, such as one or more chemical vapor deposition (CVD) processes, one or more physical vapor deposition (PVD) processes, one or more atomic layer deposition (ALD) processes, and/or any suitable combinations thereof.

[00122] At S202, one or more first through holes 205 can be formed in each of the first region 100, the second region 200, and the third region 300. As shown in FIG. 24, each of the one or more first through holes 205 can completely penetrate the first stacked layer 202 and the first insulating connection layer 203, and can extend into the surface of the substrate 201. In some embodiments, when the first mask layer 204 is formed on the surface of the first insulating connection layer 203, the etching process also etch the first mask layer 204 to form the first through holes 205.

[00123] In some embodiments, the first through holes 205 can be formed by etching the first stacked layer 202 and the first insulating connection layer 203 and a subsequent cleaning process. The etching process to form the first through holes 205 can be a wet etching, a dry etching, or a combination thereof. It is noted that, in the direction perpendicular to the surface of the substrate 201, the depth of the one or more first through holes 205 in the third region 300 can be larger than the depth of the one or more first through holes 205 in the first region 100.

[00124] At S203, a first channel structure 206 can be formed on the surface of the substrate 201 that is exposed by each of the plurality of first through holes 205, as shown

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in FIG. 25. In some embodiments, the first channel structure 206 can be a polycrystalline silicon (polysilicon) layer formed by using a selective epitaxial process.

[00125] At S204, a first functional layer can be formed on the sidewall of each of the plurality of first through holes 205. The first functional layer can include a first tunneling layer 207, a first storage layer 208, a first barrier layer 209, and a first passivation layer 210.

[00126] As shown in FIG. 26, the first tunneling layer 207 can be formed on the sidewall of the plurality of first through holes 205 and the exposed surfaces of the first channel structures 206. The first tunneling layer 207 can be used for generating electronic charges (electrons or holes). In some embodiments, the first tunneling layer 207 can be an oxide layer formed by using a deposition process.

[00127] The first storage layer 208 can be formed on the surface of the first tunneling layer 207. The first storage layer 208 can be used for storing electronic charges. The storage or removal of charge in the first storage layer 207 can impact the on/off state and/or a conductance of the semiconductor channel. The first storage layer 207 can include polycrystalline silicon (polysilicon) or silicon nitride. In some embodiments, the first storage layer 208 can be a nitride layer formed by using a deposition process.

[00128] The first barrier layer 209 can be formed on the surface of the first storage layer 208. The first barrier layer 209 can be used for blocking the outflow of the electronic charges stored in the first storage layer 208. In some embodiments, the first barrier layer 209 can be a silicon oxide layer or a combination of silicon oxide/silicon nitride/silicon oxide (ONO) layers. In some embodiments, the first barrier layer 209 includes high dielectric constant (high-k) dielectrics (e.g., aluminum oxide). In one example, the first barrier layer 209 is an oxide layer formed by using a deposition process.

[00129] As shown in FIG. 27, a first passivation layer 210 can be formed on the surface of the first barrier layer 209. The first passivation layer 210 can be used for protecting the first barrier layer 209 from being damaged in a subsequent removal process. In some embodiments, the first passivation layer 210 can be an amorphous silicon layer formed by using a deposition process.

[00130] The portions of the first passivation layer 210, the first barrier layer 209, the first storage layer 208 and the first tunneling layer 207 located on the surfaces of the plurality of first channel structures 206 on the bottom of the plurality of first through holes 205 can

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be removed. In some embodiments, the removal process can include an etching process and a cleaning process. As such, the first functional layer can be formed on the sidewalls of the plurality of first through holes 205.

[00131] In some embodiment, in the same removal process, the first barrier layer 209, the first storage layer 208, the first tunneling layer 207, and the oxide layer of the first mask layer 204 located on the surface of the nitride layer of first mask layer 204 can also be removed. As such, the nitride layer of first mask layer 204 is remained on the surface of the first insulating connection layer 203.

[00132] At S205, a second channel structure and a first filling structure can be sequentially formed on the sidewall of the first functional layer and the exposed surface of the first channel structure 206 in each of the plurality of first through holes 205. The surfaces of the second channel structure and the first filling structure can be lower than the surface of the first insulating connection layer 203.

[00133] As shown in FIG. 28, a second channel layer 211 can be formed to cover the sidewalls of the first passivation layer 210 and the bottom of each of the plurality of first through holes 205. The second channel layer 211 can also cover the surface of the first insulating connection layer 203, or cover the surface of the nitride layer of the first mask layer 204. In some embodiments, the second channel layer 211 can be an amorphous silicon layer formed by using a deposition process.

[00134] As shown in FIG. 29, a first filling layer 212 can be formed to cover the second channel layer 211 and fill each of the plurality of first through holes 205. In some embodiments, the first filling layer 212 can be an oxide layer formed by using a deposition process.

[00135] As shown in FIGs. 30A and 30B, a portion of the first filling layer 212 can be removed, such that the top surface of the first filling layer 212 can be lower than the top surface of the first insulating connection layer 203. As such, the remaining portion of the first filling layer 212 in each of the plurality of first through holes 205 can form the first filling structure. In some embodiments, the portion of the first filling layer 212 can be removed by using an etching process, such as a wet etching, a dry etching, or a combination thereof.

[00136] In some embodiments, as shown in FIG. 30A, the top surface of the first filling layer 212 can be higher than the top surface of the second stacker layer 202. For example, the top surface of the first filling layer 212 can be 20nm to 40nm higher

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than the top surface of the top nitride layer of the second stacker layer 202. Preferably, the top surface of the first filling layer 212 can be about 30nm higher than the top surface of the top nitride layer of the second stacker layer 202.

[00137] In some alternative embodiments, as shown in FIG. 30B, the top surface of the first filling layer 212 can be lower than the top surface of the second stacker layer 202. For example, the top surface of the first filling layer 212 can be 30nm to 40nm lower than the top surface of the top nitride layer of the second stacker layer 202. Preferably, the top surface of the first filling layer 212 can be about 35nm lower than the top surface of the top nitride layer of the second stacker layer 202.

[00138] As shown in FIGs. 31A and 31B, a portion of the second channel layer 211 can be removed, such that the surface of the second channel layer 211 is lower than the first insulating connection layer 203. The remaining portion of the second channel layer 211 can form the second channel structure that is in contact with the first channel structure 206. In some embodiments, the portion of the second channel layer 211 can be removed by using an etching process.

[00139] It is noted that, in various embodiments, the top surface of the second channel structure can be higher than the top surface of the first stacked layer 202 or lower than the top surface of the first stacked layer 202. However, the top surface of the second channel structure is not lower than the top surface of the top oxide layer in the first stacked layer 202. In some embodiments, the top surface of the second channel structure can be higher than the top nitride layer in the first stacked layer 202, as shown in FIG. 31A. In some alternative embodiments, the top surface of the second channel structure is in a same plane of the top surface of the top oxide layer in the first stacked layer 202, as shown in FIG. 31B.

[00140] At S206, a first groove can be formed in the first insulating connection layer 203 above each of the plurality of first through holes 205. In some embodiments, the projection of the first groove on the substrate 201 can completely cover the projection of the corresponding first through hole 205 on the substrate 201.

[00141] As shown in FIGs. 32A and 32B, the nitride layer of the first mask layer 204 can be removed. In some embodiments, the nitride layer of the first mask layer 204 can be removed by using an etching process.

[00142] As shown in FIGs. 33A and 33 B, the surface of the first insulating connection layer 203 can be planarized by any suitable techniques, such as backside grinding, and/or

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chemical mechanical polishing (CMP). A portion of the first insulating connection layer 203 can be removed to form a plurality of first grooves that penetrate the first insulating connection layer 203. An area of the projection of each of the plurality of first grooves on the substrate 201 can be larger than an area of the projection of each of the plurality of first through holes 205 on the substrate 201.

[00143] In some embodiments, a depth of the first groove can be equal to or less than the thickness of the planarized first insulating connection layer 203, as shown in FIG. 33A. For example, the depth of the first groove can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 203 is about 90nm, while the depth of the first groove is about 60nm.

[00144] In some alternative embodiments, the depth of the first groove can be greater than the thickness of the planarized first insulating connection layer 203, as shown in FIG. 33B. That is, a portion of the top nitride layer in the first stacked layer 202 can also be removed to form the first groove. For example, the depth of the first groove can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 203 is about 30nm, while the depth of the first groove is about 60nm.

[00145] At S207, a third channel structure 214 can be formed in each of the plurality of first grooves 213. As shown in FIGs. 34A and 34B, the third channel structure 214 can be in contact with the second channel structure in each of the plurality of first through holes 205. In some embodiments, the third channel structure can be a polycrystalline silicon player formed by using a deposition process.

[00146] A thickness of each third channel structure 214 can be equal to the depth of each first groove 213. As described above, in some embodiments, a thickness of each third channel structure 214 can be equal to or less than the thickness of the planarized first insulating connection layer 203, as shown in FIG. 34A. For example, the thickness of each third channel structure 214 can be in a range between 50nm and 70nm, preferably about 60nm. In some alternative embodiments, the thickness of each third channel structure 214 can be greater than the thickness of the planarized first insulating connection layer 203, as shown in FIG. 34B. For example, the thickness of each third channel structure 214 can be in a range between 60nm and 80nm, preferably about 70nm.

[00147] Referring to FIG. 50B, at S208, a second stacked layer 215 and a second insulating connection layer 216 can be sequentially formed on the plurality of third

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channel structures 214. As shown in FIG. 35, the second stacked layer 215 can include a plurality of oxide/nitride layer pairs, such as silicon oxide layers and silicon nitride layers. Similar to the first stacked layer 202 as described above, the multiple oxide layers (shown in the areas with dotes) and multiple nitride layers (shown in the areas with meshes) in the second stacked layer 215 alternate in a vertical direction. The second stacked layer 215 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide layers and the nitride layers in the second stacked layer 215 is equal to or larger than 64.

[00148] In some embodiments, the second insulating connection layer 216 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is noted that, the material of the second insulating connection layer 216 can be different from the material of the nitride layer in the second stacked layer 215.

[00149] Further, in some embodiments, a second mask layer 217 can be formed on the surface of the second insulating connection layer 216. The second mask layer 217 can include a nitride layer on the surface of the second insulating connection layer 216, and an oxide layer on the surface of such nitride layer.

[00150] At S209, one or more second through holes 218 are formed in each of the first region 100, the second region 200, and the third region 300. As shown in FIG. 36, each of the plurality of second through holes 218 can completely penetrate the second stacked layer 215, the second insulating connection layer 216, and the second mask layer 217, and can extend into the surface of the corresponding third channel structure 214. The projection of each second through hole 218 on the substrate 201 can at least partially overlap with the projection of the corresponding first through hole 205 on the substrate 201.

[00151] In some embodiments, the second stacked layer 215, the second insulating connection layer 216, the second mask layer 217, and the third channel structures 214 can be etched to form the plurality of second through holes 218 that penetrate the second stacked layer 215 and the second insulating connection layer 216. The second stacked layer 215, the second insulating connection layer 216, the second mask layer 217, and/or the third channel structure 214 can be etched by using a dry etching process, a wet etching process, or a combination thereof. A cleaning process can then be performed to clean the plurality of second through holes 218.

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[00152] It is noted that, each second through hole 218 can extend to the surface of the corresponding third channel structure 214, or can extend into the corresponding third channel structure 214. As such, a fourth channel structure formed subsequently in each second through hole 218 can directly contact the corresponding third channel structure. It is also noted that, the one or more second through holes 218 in the third region 300 can also completely penetrate the corresponding third channel structures 214, as shown in FIG. 36. However, the one or more third channel structures 214 in the first region 100 are not completely penetrated by the one or more second through holes 218.

[00153] In some embodiments, a maximum difference between the radius of the top aperture of each second through hole 218 and the radius of the bottom aperture of the second through hole 218 can be 15nm. That is, as shown in FIG. 36, a distance "a" between the boundary line of the top surface of each second through hole 218 and the boundary of the bottom surface of the second through hole 218 can be no more than 15 nm.

[00154] At S2010, a second functional layer can be formed on the sidewall of each second through hole 218. In some embodiments, the second functional layer can include a second tunneling layer 219, a second storage layer 220, a second barrier layer 221, and a second passivation layer 222.

[00155] As shown in FIG. 37, the second tunneling layer 219 can be formed on the sidewall of each second through hole 218 and the surface of the corresponding third channel structure 214. The second tunneling layer 219 can be used for generating electronic charges. In some embodiments, the second tunneling layer 219 can be an oxide layer formed by using a deposition process.

[00156] The second storage layer 220 can be formed on the surface of the second tunneling layer 219. The second storage layer 220 can be used for storing electronic charges. In some embodiments, the second storage layer 220 can be a nitride layer formed by using a deposition process.

[00157] The second barrier layer 221 can be formed on the surface of the second storage layer 220. The second barrier layer 221 can be used for blocking the outflow of the electronic charges in the second storage layer 220. In some embodiments, the second barrier layer 221 can be an oxide layer formed by using a deposition process.

[00158] As shown in FIG. 38, a second passivation layer 222 can be formed on the surface of the second barrier layer 221. The second passivation layer 222 can be used for

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protecting the second barrier layer 221 from being damaged in a subsequent removal process. In some embodiments, the second passivation layer 222 can be an amorphous silicon layer formed by using a deposition process.

[00159] As shown in FIG. 38, the portions of the second passivation layer 222, the second barrier layer 221, the second storage layer 220 and the second tunneling layer 219 that are located on the surface of each third channel structure 214 can be removed. In some embodiments, the removal process can include an etching process and a cleaning process. In some embodiments, the portions of the second passivation layer 222, the second barrier layer 221, the second storage layer 220, the second tunneling layer 219, the oxide layer of the second mask layer 217 that are located on the nitride layer of the second mask layer 217 can also be removed by using an etching process. As such, the second functional layer can be formed on the sidewall of each second through hole 218.

[00160] At S2011, a fourth channel structure can be formed on the sidewall of the second functional layer and the exposed surface of the third channel structure in each second through hole 218 in the first region 100. Further, a second filling structure can be formed in each of the plurality of second through holes 218 in the first region 100, the second region 200, and the third region 300. In some embodiments, the top surface of the fourth channel structure can be higher than the top surface of the second filling structure.

[00161] As shown in FIG. 39, a fourth channel layer 223 can be formed to cover the sidewall of the second passivation layer 222 and the bottom surface of each of the plurality of second through holes 218 in the first region 100, the second region 200, and the third region 300. In some embodiments, the fourth channel layer 223 can also cover the top surface of the second insulating connection layer 216, or the top surface of the nitride layer of the second mask layer 217. In some embodiments, the fourth channel layer 223 can be an amorphous silicon layer formed by using a deposition process.

[00162] As shown in FIG. 40, a third filling layer 224 can be formed to cover the fourth channel layer 223. In some embodiments, the third filling layer 224 can include one or more airgaps in each second through hole 218. In some embodiments, the third filling layer 224 can be an oxide layer formed by using a deposition process.

[00163] As shown in FIG. 41, a third mask layer 25 can be formed on the top surface of the third filling layer 224 in the first region 100. Using the third mask layer 225 as a mask, the portions of the third filling layer 224 located in the second region 200 and the third region 300 can be removed by using an etching process.

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[00164] As shown in FIG. 42, the third mask layer 225 can be removed. Using the remaining third filling layer 224 in the first region 100 as a mask, the fourth channel layer 223 located in the second region 200 and the third region 300 can be removed by using an etching process.

[00165] As shown in FIG. 43, a fourth filling layer 227 can be formed on the surface of the second functional layer located in the second region 200 and the third region 300. In some embodiments, the filling performance of the fourth filling layer 227 can be better than the filling performance of the third filling layer 224. That is, in a same removing process, the removal rate of the fourth filling layer 227 can be less than the removal rate of the third filling layer 224.

[00166] As shown in FIG. 44, the third filling layer 224 on the surface of the fourth channel layer 223 in the first region 100 can be removed by using an etching process. It is noted that, a portion of the fourth filling layer 227 can also be removed by the same etching process.

[00167] As shown in FIG. 45, a second filling layer 229 can be formed in each second through hole 218 in the first region 100, the second region 200 and the third region 300. The material of the second filling layer 229 can be the same material of the fourth filling layer 227.

[00168] As shown in FIG. 46, a portion of the second filling layer 29 can be removed by using an etching process, such that the top surface of the second filling layer 229 in each second through hole 218 is lower than the top surface of the second insulating connection layer 216. The remaining portion of the second filling layer 29 in each second through hole 218 can form the second filling structure.

[00169] Further, the portion of the fourth channel layer 223 located on the surface of the second insulating connection layer 216 or the surface of the second mask layer 217 can be removed by using an etching process. The remaining portion of the fourth channel layer 223 in each second through hole 218 can form the fourth channel structure. The top surface of the fourth channel structure can be higher than the top surface of the second filling structure. As such, a second groove can be formed on the fourth channel structure and the second filling structure in each second through hole 218 in the first region 100, and on the second filling structure in each second through hole 218 in the second region 200 and the third region 300.

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[00170] It is noted that, the top surface of the fourth channel structure can be higher than the top surface of the second stacked layer 215, or can be lower than the top surface of the second stacked layer 215. The top surface of the fourth channel structure is not lower than the top surface of the top oxide layer in the second stacked layer 215. In some embodiments, the top surface of the fourth channel structure can be in a same plane of the top surface of the top oxide layer in the second stacked layer 215.

[00171] At S2012, a fifth channel structure can be formed in the second groove of each second through hole 218 in the first region 100. The fifth channel structure can be in contact with the fourth channel structure.

[00172] As shown in FIG. 47, the fifth channel structure 230 can be formed in the second groove that is on the fourth channel structure and the second filling structure in each second through hole 218 in the first region 100. The fifth channel structure 230 can also be formed in the second groove that is on the second filling structure in each second through hole 218 in the second region 200 and the third region 300. The nitride layer of the second mask layer 217 can be then removed by an etching process.

[00173] As shown in FIGs. 48A and 48B, the top surface of the second insulating connection layer 216 and the top surface of the plurality of fifth channel structures 230 can be planarized by any suitable techniques, such as backside grinding, and/or chemical mechanical polishing (CMP).

[00174] Accordingly, the disclosed method as shown in FIGs. 50A and 50B can form another joint opening structure of a three-dimensional (3D) memory device by combining two through hole formation processes. As such, the formed channel holes having the joint opening structure can have a large aspect ratio and a limited top-bottom aperture error. Further, the disclosed method of forming a joint opening structure in a 3D memory device can simultaneously form a plurality of channel holes, staircase dummy holes, and through array contact barriers, resulting in an efficient process capability control, a simplified process complexity, and a reduced cost.

[00175] In some embodiments, the present disclosure also provides another three-dimensional memory device formed by using the above disclosed method as shown in FIGs. 50A and 50B. The three-dimensional memory device can include a first region for forming a plurality of channel holes, a second region for forming a plurality of staircase structure (SS) dummy holes, and a third region for forming a plurality of through array contact (TAC) barriers. Along a direction perpendicular to the surface of the three-

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dimensional memory device, the three-dimensional memory device can include the following components.

[00176] A first stacked layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs, is formed on a substrate. A first insulating connection layer is formed on the first stacked layer. A plurality of first through holes penetrating the first stacked layer and the first insulating connection layer and extending into the surface of the substrate are formed in the first region, the second region, and the third region.

[00177] A first channel structure is formed on the surface of the substrate exposed by each first through hole. A first functional layer is formed on the sidewall of each first through hole. A second channel structure is formed on the sidewall of the first functional layer and the surface of the first channel structure in each first through hole. A first filling structure is formed on the sidewall and the surface of the second channel structure to fill each of the plurality of first through holes. In some embodiments, an airgap can be enclosed in the first filling structure in each first through hole. The top surfaces of the second channel structure and the first filling structure are lower than the top surfaces of the first insulating connection layer.

[00178] A first groove is formed in the first insulating connection layer, and above the first functional layer, the second channel structure and the first filling structure in each first through hole. A projection of each of the plurality of first grooves on the substrate completely covers a projection of the corresponding first through hole on the substrate. A third channel structure in contact with the second channel structure in the corresponding first through hole is formed in each first groove.

[00179] A second stack layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs, is formed on the top surfaces of the first insulating connection layer and the plurality of third channel structures. A second insulating connection layer is formed on the second stack layer. A plurality of second through holes penetrating through the second stacked layer and the second insulating connection layer and extending into a surface of the third channel structure are formed in the first region, the second region, and the third region. A projection of each of the plurality of second through holes on the substrate at least partially overlaps the projection of the corresponding first through hole on the substrate.

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[00180] A second functional layer is formed on the sidewall of each second through hole. A fourth channel structure is formed on the sidewall of the second functional layer and the bottom surface of each second through hole in the first region. A second filling is formed to fill each of the plurality of second through holes in the first region, the second region, and the third region. In some embodiments, an airgap can be enclosed in the second filling structure. The top surface of the fourth channel structure is higher than the top surface of the second filling structure in each second through hole in the first region.

[00181] In the first region, a fifth channel structure in contact with the fourth channel structure is formed in a second groove in each second through hole that is surrounded by the second functional layer, and above the fourth channel structure and the second filling structure. And in the second region and the third region, a fifth channel structure is formed in a second groove in each second through hole that is surrounded by the second functional layer, and above the second filling structure.

[00182] Due to the fourth channel structures being formed in the second through holes in the first region rather than the third region, the fifth channel structure in each second through hole in the first region can be electronically connected with the first channel structure in the corresponding first through hole, while the fifth channel structure in each second through hole in the third region can be electronically insulated with the first channel structure in the corresponding first through hole. Thus, in the three-dimensional memory device, a plurality of channel holes can be formed in the first region, and a plurality of through array contact (TAC) barriers can be formed in the third region. The plurality of staircase structure dummy holes in the second region can have a supporting function of the staircase structure.

[00183] In some embodiments, as shown in FIG. 48A, in each channel hole in the first region, a thickness "b" of the first insulating connection layer, which is the distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 80nm and 100nm, preferably about 90nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00184] In some alternative embodiments, as shown in FIG. 47B, in each channel hole in the first region, a thickness "b" of the first insulating connection layer, which is the distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 20nm and 40nm, preferably

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about 30nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00185] Further, the difference between the radiuses of the top aperture and the bottom aperture of the second channel structure, and the difference between the radiuses of the top aperture and the bottom aperture of the fourth channel structure can be within 15nm. Accordingly, the disclosed channel hole having a joint opening structure can have a large aspect ratio and a limited top-bottom aperture error.

[00186] In some embodiments, a replacement process can be performed to replace each of the plurality of nitride layers in the first stacked layer 202 and the second stacked layer 215 with a conductive layer 240, as shown in FIGs. 49A and 49B. The conductive layer can include any suitable material that is electronically conductive, including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof.

[00187] In some embodiments, the replacement process can be performed in one or more of the first region 100, the second region 200, and the third region 300. In one embodiments, the replacement process is performed in the first region 100 and the second region 200, but not in the third region 300. That is, the first stacked layer and the second stacked layer in the first region and the second region can be alternating conductive/dielectric stack, while the first stacked layer and the second stacked layer in the third region can be alternating oxide/nitride stack.

[00188] In some embodiments, during the replacement process, a portion of the third channel structure 214 that is adjacent with the bottom nitride layer of the second stacked layer 215, or is adjacent with the top nitride layer of the first stacked layer 202 can be converted to an oxide layer by an oxidation process. That is, as shown in FIGs. 49A and 49B, a thickness "c" of the third channel structure can be reduced after the replacement process. For example, the thickness "c" of the third channel structure can be reduced to a range between 30nm and 50nm, preferably about 40nm.

[00189] Referring to FIGs. 74A and 74B, schematic flow diagrams of another exemplary method for forming a joint opening structure of three-dimensional (3D) memory device are illustrated in accordance with some embodiments of the present disclosure. And FIGs. 51-73 illustrate schematic structural cross-sectional diagrams of an exemplary joint opening structure of three-dimensional (3D) memory device at certain stages of the fabricating process shown in FIGs. 74A and 74B.

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[00190] At S301, a substrate 301 can be provided, a first stacked layer 302 and a first insulating connection layer 303 can be formed on the surface of the substrate 301. As shown in FIG. 51, the first stacked layer 302 can include a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs. The multiple oxide layers (shown in the areas with dotes) and multiple nitride layers (shown in the areas with meshes) in the first stacked layer 302 alternate in a vertical direction. The first stacked layer 302 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide layers and the nitride layers in the first stacked layer 302 is equal to or larger than 64.

[00191] In some embodiments, the first insulating connection layer 303 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is noted that, the material of the first insulating connection layer 303 can be different from the material of the nitride layer in the first stacked layer 302.

[00192] Further, in some embodiments, a first mask layer 304 can be formed on the surface of the first insulating connection layer 303. The first mask layer 304 can include a nitride layer on the surface of the first insulating connection layer 303, and an oxide layer on the surface of such nitride layer.

[00193] At S302, a first through hole 305 can be formed. As shown in FIG. 51, the first through hole 305 can completely penetrate the first stacked layer 302 and the first insulating connection layer 303, and can extend into the surface of the substrate 301.

[00194] In some embodiments, the first through hole 305 can be formed by etching the first stacked layer 302 and the first insulating connection layer 303 and a subsequent cleaning process. The etching process to form the first through hole 305 can be a wet etching, a dry etching, or a combination thereof.

[00195] In some embodiments, when the first mask layer 304 is formed on the surface of the first insulating connection layer 303, the etching process also etch the first mask layer 304 to form the first through holes 305.

[00196] At S303, a first channel structure 306 can be formed on the surface of the substrate 301 that is exposed by the first through hole 305, as shown in FIG. 52. In some embodiments, the first channel structure 306 can be a polycrystalline silicon layer formed by using a selective epitaxial process.

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[00197] At S304, a first functional layer can be formed on the sidewall of the first through hole 305. The first functional layer can include a first tunneling layer 307, a first storage layer 308, a first barrier layer 309, and a first passivation layer 310.

[00198] As shown in FIG. 53, the first tunneling layer 307 can be formed on the sidewall of the first through hole 305 and the surface of the first channel structure 306. The first tunneling layer can be used for generating electronic charges. In some embodiments, the first tunneling layer 307 can be an oxide layer formed by using a deposition process.

[00199] The first storage layer 308 can be formed on the surface of the first tunneling layer 307. The first storage layer 308 can be used for storing electronic charges. In some embodiments, the first storage layer 308 can be a nitride layer formed by using a deposition process.

[00200] The first barrier layer 309 can be formed on the surface of the first storage layer 308. The first barrier layer 309 can be used for blocking the outflow of the electronic charges stored in the first storage layer 308. In some embodiments, the first barrier layer 309 can be an oxide layer formed by using a deposition process.

[00201] As shown in FIG. 54, a first passivation layer 310 can be formed on the surface of the first barrier layer 309. The first passivation layer 310 can be used for protecting the first barrier layer 309 from being damaged in a subsequent removal process. In some embodiments, the first passivation layer 310 can be an amorphous silicon layer formed by using a deposition process.

[00202] The portions of the first passivation layer 310, the first barrier layer 309, the first storage layer 308 and the first tunneling layer 307 located on the surface of the first channel structure 306 on the bottom of the first through hole 305 can be removed. In some embodiments, the removal process can include an etching process and a cleaning process. As such, the first functional layer can be formed on the sidewall of the first through hole 305.

[00203] In some embodiment, in the same removal process, the first barrier layer 309, the first storage layer 308, the first tunneling layer 307, and the oxide layer of the first mask layer 304 located on the surface of the nitride layer of first mask layer 304 can also be removed. As such, the nitride layer of first mask layer 304 is remained on the surface of the first insulating connection layer 303.

[00204] At S305, a second channel structure can be formed on the sidewall of the first functional layer sidewall and the surface of the first channel structure 306. The surfaces

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of the second channel structure can be lower than the surface of the first insulating connection layer 303.

[00205] As shown in FIG. 55, a second channel layer 311 can be formed to cover the sidewall of the first passivation layer 310, the bottom of the first through hole 305. The second channel layer 311 can also cover the surface of the first insulating connection layer 303, or cover the surface of the nitride layer of the first mask layer 304. In some embodiments, the second channel layer 311 can be an amorphous silicon layer formed by using a deposition process.

[00206] As shown in FIGs. 56A and 56B, a portion of the second channel layer 311 can be removed, such that the surface of the second channel layer 311 is lower than the first insulating connection layer 303. The remaining portion of the second channel layer 311 can form the second channel structure that is in contact with the first channel structure 306. In some embodiments, an airgap can be enclosed by the second channel structure, as shown in FIGs. 56A and 56B. In some embodiments, the portion of the second channel layer 311 can be removed by using an etching process.

[00207] It is noted that, in various embodiments, the top surface of the second channel structure can be higher than the top surface of the first stacked layer 302 or lower than the top surface of the first stacked layer 302. However, the top surface of the second channel structure is not lower than the top surface of the top oxide layer in the first stacked layer 302. In some embodiments, the top surface of the second channel structure can be higher than the top nitride layer in the first stacked layer 302, as shown in FIG. 56A. In some alternative embodiments, the top surface of the second channel structure is in a same plane of the top surface of the top oxide layer in the first stacked layer 302, as shown in FIG. 56B.

[00208] At S306, a first groove 312 can be formed in the first insulating connection layer 303. In some embodiments, the projection of the first groove 312 on the substrate 301 can completely cover the projection of the first through hole 305 on the substrate 301.

[00209] As shown in FIGs. 57A and 57B, the nitride layer of the first mask layer 304 can be removed by using an etching process. As shown in FIGs. 58A and 58B, the surface of the first insulating connection layer 303 can be planarized. A portion of the first insulating connection layer 303 can be removed to form the first groove 312 that penetrates the first insulating connection layer 303. An area of the projection of the first

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groove 312 on the substrate 301 can be larger than an area of the projection of the first through hole 305 on the substrate 301.

[00210] In some embodiments, a depth of the first groove can be equal to or less than the thickness of the planarized first insulating connection layer 303, as shown in FIG. 58A. For example, the depth of the first groove can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 303 is about 90nm, while the depth of the first groove is about 60nm.

[00211] In some alternative embodiments, the depth of the first groove can be greater than the thickness of the planarized first insulating connection layer 303, as shown in FIG. 58B. That is, a portion of the top nitride layer in the first stacked layer 302 can also be removed to form the first groove. For example, the depth of the first groove can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 303 is about 30nm, while the depth of the first groove is about 60nm.

[00212] At S307, a third channel structure 313 can be formed in the first groove 312. As shown in FIGs. 59A and 59B, the third channel structure 313 can be in contact with the second channel structure. In some embodiments, the third channel structure can be a polycrystalline silicon player formed by using a deposition process.

[00213] A thickness of the third channel structure 313 can be equal to the depth of the first groove 312. As described above, in some embodiments, a thickness of the third channel structure 313 can be equal to or less than the thickness of the planarized first insulating connection layer 303, as shown in FIG. 59A. For example, the thickness of the third channel structure 313 can be in a range between 50nm and 70nm, preferably about 60nm. In some alternative embodiments, the thickness of the third channel structure 313 can be greater than the thickness of the planarized first insulating connection layer 303, as shown in FIG. 59B. For example, the thickness of the third channel structure 313 can be in a range between 60nm and 80nm, preferably about 70nm.

[00214] At S308, a second stacked layer 314 and a second insulating connection layer 315 can be sequentially formed on the third channel structure 313. As shown in FIG. 60, the second stacked layer 315 can include a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs. Similar to the first stacked layer 302 as described above, the multiple oxide layers (shown in the areas with dotes) and multiple nitride layers (shown in the areas with meshes) in the second stacked layer 314 alternate

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in a vertical direction. The second stacked layer 314 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide layers and the nitride layers in the second stacked layer 314 is equal to or larger than 64.

[00215] In some embodiments, the second insulating connection layer 315 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is noted that, the material of the second insulating connection layer 315 can be different from the material of the nitride layer in the second stacked layer 314.

[00216] Further, in some embodiments, a second mask layer 316 can be formed on the surface of the second insulating connection layer 315. The second mask layer 316 can include a nitride layer on the surface of the second insulating connection layer 315, and an oxide layer on the surface of such nitride layer.

[00217] At S309, a second through hole 317 can be formed. As shown in FIG. 61, the second through hole 317 can completely penetrate the second stacked layer 314 and the second insulating connection layer 315, and can extend into the surface of the third channel structure 313. The projection of the second through hole 317 on the substrate 301 can at least partially overlap with the projection of the first through hole 305 on the substrate 301.

[00218] In some embodiments, the second stacked layer 314, the second insulating connection layer 315, the second mask layer 316, and a portion of the third channel structure 314 can be etched to form the second through hole 317. The second stacked layer 314, the second insulating connection layer 315, the second mask layer 316, and/or the third channel structure 314 can be etched by using a dry etching process, a wet etching process, or a combination thereof. A cleaning process can then be performed to clean the second through hole 317.

[00219] In some embodiments, a maximum difference between the radius of the top aperture of each second through hole 317 and the radius of the bottom aperture of the second through hole 317 can be 15nm. That is, as shown in FIG. 61, a distance "a" between the boundary line of the top surface of the second through hole 317 and the boundary of the bottom surface of the second through hole 317 can be no more than 15 nm.

[00220] At S3010, a second functional layer can be formed on the sidewall of the second through hole 317. In some embodiments, the second functional layer can include

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a second tunneling layer 318, a second storage layer 319, a second barrier layer 320, and a second passivation layer 321.

[00221] As shown in FIG. 62, the second tunneling layer 318 can be formed on the sidewall of the second through hole 317 and the surface of the second channel structure 313. The second tunneling layer 318 can be used for generating electronic charges. In some embodiments, the second tunneling layer 318 can be an oxide layer formed by using a deposition process.

[00222] The second storage layer 319 can be formed on the surface of the second tunneling layer 318. The second storage layer 319 can be used for storing electronic charges. In some embodiments, the second storage layer 319 can be a nitride layer formed by using a deposition process.

[00223] The second barrier layer 320 can be formed on the surface of the second storage layer 319. The second barrier layer 320 can be used for blocking the outflow of the electronic charges in the second storage layer 319. In some embodiments, the second barrier layer 320 can be an oxide layer formed by using a deposition process.

[00224] As shown in FIG. 63, a second passivation layer 321 can be formed on the surface of the second barrier layer 320. The second passivation layer 321 can be used for protecting the second barrier layer 320 from being damaged in a subsequent removal process. In some embodiments, the second passivation layer 322 can be an amorphous silicon layer formed by using a deposition process.

[00225] As shown in FIG. 63, the portions of the second passivation layer 321, the second barrier layer 320, the second storage layer 319, the second tunneling layer 318, and the third channel structure 313 that are located at the bottom of the second through hole 317 and the top of the first through hole 305 can be removed. In some embodiments, the removal process can include an etching process and a cleaning process.

[00226] In some embodiments, the portions of the second passivation layer 321, the second barrier layer 320, the second storage layer 319, the second tunneling layer 318, and the oxide layer of the second mask layer 316 that are located on the nitride layer of the second mask layer 316 can also be removed by using an etching process. As such, the second functional layer can be formed on the sidewall of the second through hole 318, and the second through hole 317 and the first through hole 305 can be interconnected with each other, as shown in FIG. 63.

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[00227] In some embodiments, the portions of the second barrier layer 320, the second storage layer 319, and the second tunneling layer 318 that are located under the second passivation layer 321, as shown in the dashed circle in FIG. 64, can also be removed by using an etching process.

[00228] At S3011, the second tunneling structure, the third tunneling structure, the second passivation layer 321, and the first passivation layer 310 can be removed. In some embodiments, the second tunneling structure, the third tunneling structure, the second passivation layer 321, and the first passivation layer 310 can be removed by using one or more etching processes. As such, a third through hole 322 can be formed by interconnecting the first through hole and the second through hole, as shown in FIG. 65.

[00229] At S3012, a fourth channel structure and a first filling structure can be sequentially formed on the sidewall and the bottom of the third through hole 322. In some embodiments, the surface of the fourth channel structure can be higher than the surface of the first filling structure. In some embodiments, the fourth channel structure includes a joint channel structure that is sandwiched between the first stacked layer 302 and the second stacked layer 314, and covers the exposed surface of the first insulating connection layer 303.

[00230] As shown in FIG. 66, a fourth channel layer 328 can be formed to cover the sidewall and bottom of the third through hole 322 and the exposed surface of the third insulating connection layer 303. In some embodiments, the fourth channel layer 323 can also cover the surface of the second insulating connection layer 315, or the surface of the nitride layer of the second mask layer 316. In some embodiments, the fourth channel layer 328 can be an amorphous silicon layer formed by using a deposition process.

[00231] As shown in FIG. 67, a first filling layer 334 can be formed to cover the fourth channel layer 328 and to fill the third through hole 322. In some embodiments, the first filling layer 334 can be an oxide layer formed by using a deposition process.

[00232] As shown in FIG. 68, a portion of the first filling layer 334 can be removed, such that the surface of the first filling layer 334 is lower than the top surface of the second insulating connection layer 315. In some embodiments, the removal process can include an etching process. The remaining portion of the second filling layer 334 in the third through hole 322 can form the second filling structure.

[00233] As shown in FIG. 69, the portion of the fourth channel layer 328 located on the top surface of the second insulating connection layer 315 or the top surface of the second

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mask layer 316 can be removed. In some embodiments, the removal process can include an etching process. The remaining portion of the fourth channel layer 328 in the third through hole 322 can form the fourth channel structure. The top surface of the fourth channel structure can be higher than the top surface of the second filling structure. As such, a second groove can be formed on the fourth channel structure and the second filling structure, and in the third through hole 322.

[00234] It is noted that, the top surface of the fourth channel structure can be higher than the top surface of the second stacked layer 314, or can be lower than the top surface of the second stacked layer 314. The top surface of the fourth channel structure is not lower than the top surface of the top oxide layer in the second stacked layer 314. In some embodiments, the top surface of the fourth channel structure can be in a same plane of the top surface of the top oxide layer in the second stacked layer 314.

[00235] At S3013, a fifth channel structure can be formed in the second groove. The fifth channel structure can be in contact with the fourth channel structure. As shown in FIG. 70, the fifth channel structure 335 can be formed in the second groove that is on the fourth channel structure and the second filling structure and in the third through hole 322.

[00236] As shown in FIG. 71, the nitride layer of the second mask layer 316 can be removed by an etching process. As shown in FIGs. 72A and 72B, the top surface of the second insulating connection layer 315 and the top surface of the fifth channel structure 335 can be planarized.

[00237] Accordingly, the disclosed method as shown in FIGs. 74A and 74B can form a joint opening structure of a three-dimensional (3D) memory device by combining two through hole formation processes. As such, the formed channel hole having the joint opening structure can have a large aspect ratio and a limited top-bottom aperture error. Further, the disclosed method of forming a joint opening structure in a 3D memory device can result in an efficient process capability control, a simplified process complexity, and a reduced cost.

[00238] In some embodiments, the present disclosure also provides a three-dimensional memory device formed by using the above disclosed method as shown in FIGs. 74A and 74B. The three-dimensional memory can include the following components described below.

[00239] A first stacked layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer silicon nitride layer pairs, is formed on a substrate. A first insulating

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connection layer is formed on the first stacked layer. A first through hole penetrates the first stacked layer and the first insulating connection layer, and extends into the surface of the substrate. A first channel structure is formed on the surface of the substrate exposed by the first through hole. A first functional layer is formed on the sidewall of the first through hole.

[00240] A second stack layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs, is formed on the top surfaces of the first insulating connection layer. A second insulating connection layer is formed on the second stack layer. A second through hole penetrates through the second stacked layer and the second insulating connection layer, and is interconnected with the first through hole. A second functional layer is formed on the sidewall of the second through hole.

[00241] The first through hole and the second through hole constitute the third through hole. A fourth channel structure being contact with the first channel structure is formed on the sidewall and the bottom of the third through hole. A first filling structure is formed on the sidewall and the surface of the fourth channel structure to fill the third through hole. In some embodiments, an airgap is enclosed in the first filling structure. The top surface of the fourth channel structure is higher than the top surface of the first filling structure. A fifth channel structure in contact with the fourth channel structure is formed in a second groove that is surrounded by the second functional layer, and above the fourth channel structure and the first filling structure.

[00242] In some embodiments, as shown in FIG. 72A, a thickness "b" of the first insulating connection layer, which is the distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 80nm and 100nm, preferably about 90nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00243] In some alternative embodiments, as shown in FIG. 72B, a thickness "b" of the first insulating connection layer, which is the distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 20nm and 40nm, preferably about 30nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00244] Further, the error the radius of the aperture of different positions of the third through hole can be within 15nm. That is, a difference between a maximum radius of the third through hole and a minimum radius of the third through hole is less than or equal to

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15nm. Accordingly, the disclosed channel hole having a joint opening structure can have a large aspect ratio and a limited top-bottom aperture error.

[00245] In some embodiments, a replacement process can be performed to replace each of the plurality of nitride layers in the first stacked layer 302 and the second stacked layer 314 with a conductive layer 440, as shown in FIGs. 73A and 73B. The conductive layer can include any suitable material that is electronically conductive, including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof.

[00246] In some embodiments, during the replacement process, a portion of the third channel structure 313 that is adjacent with the bottom nitride layer of the second stacked layer 314, or is adjacent with the top nitride layer of the first stacked layer 302 can be converted to an oxide layer by an oxidation process. That is, as shown in FIGs. 73A and 73B, a thickness "c" of the third channel structure can be reduced after the replacement process. For example, the thickness "c" of the third channel structure can be reduced to a range between 30nm and 50nm, preferably about 40nm.

[00247] Referring to FIGs. 103A and 103B, schematic flow diagrams of another exemplary fabricating process for forming a joint opening structure of three-dimensional (3D) memory device are illustrated in accordance with some other embodiments of the present disclosure. And FIGs. 75-102 illustrate schematic structural cross-sectional diagrams of an exemplary joint opening structure of three-dimensional (3D) memory device at certain stages of the fabricating process shown in FIGs. 103A and 103B.

[00248] As shown in FIG. 103A, at S401, a first stacked layer 402 and a first insulating connection layer 403 can be sequentially formed on the surface of a substrate 401. In some embodiments, the 3D memory device can include a first region 100, a second region 200, and a third region 300, as shown in FIG. 75. The first region 100 can be used to form one or more channel holes, the second region 200 can be used to form one or more staircase structure (SS) dummy holes, while the third region 300 can be used to form one or more through array contact (TAC) barriers.

[00249] As shown in FIG. 75, the first stacked layer 402 can be formed on the substrate 401. The first stacked layer 402 can include a plurality of oxide/nitride layer pairs. That is, in the first stacked layer 402, multiple oxide layers (shown in the areas with dotes) and multiple nitride layers (shown in the areas with meshes) alternate in a vertical direction. In other words, except a top and a bottom layer of a given stack, each of the other oxide

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layers can be sandwiched by two adjacent nitride layers, and each nitride layer can be sandwiched by two adjacent oxide layers.

[00250] Oxide layers can each have the same thickness or have different thicknesses. For example, a thickness of each oxide layer can be in a range from 90nm to 160nm, preferably about 150nm. Similarly, nitride layers can each have the same thickness or have different thicknesses. For example, a thickness of each nitride layer can be in a range from 80nm to 110nm, preferably about 100nm. In some embodiments, the oxide layers can be silicon oxide layers, and the nitride layers can be silicon nitride layer.

[00251] The first stacked layer 402 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide layers and the nitride layers in the first stacked layer 402 is equal to or larger than 64. In some embodiments, alternating conductor/dielectric stack includes more oxide layers or more nitride layers with different materials and/or thicknesses than the oxide/nitride layer pair.

[00252] The first insulating connection layer 403 can be formed on the first stacked layer 402. In some embodiments, the first insulating connection layer 403 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is noted that, the material of the first insulating connection layer 403 can be different from the material of the nitride layer in the first stacked layer 402.

[00253] Further, in some embodiments, a first mask layer 404 can be formed on the surface of the first insulating connection layer 403. The first mask layer 404 can include a nitride layer on the surface of the first insulating connection layer 403, and an oxide layer on the surface of such nitride layer.

[00254] In some embodiments, the first stacked layer 402, the first insulating connection layer 403, and/or the first mask layer 404 can be formed by using one or more deposition processes, such as one or more chemical vapor deposition (CVD) processes, one or more physical vapor deposition (PVD) processes, one or more atomic layer deposition (ALD) processes, and/or any suitable combinations thereof.

[00255] At S402, one or more first through holes 405 can be formed in each of the first region 100, the second region 200, and the third region 300. As shown in FIG. 75, each of the one or more first through holes 405 can completely penetrate the first stacked layer 402 and the first insulating connection layer 403, and can extend into the surface of the substrate 401. In some embodiments, when the first mask layer 404 is formed on the

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surface of the first insulating connection layer 403, the etching process also etch the first mask layer 404 to form the first through holes 405.

[00256] In some embodiments, the first through holes 405 can be formed by etching the first stacked layer 402 and the first insulating connection layer 403 and a subsequent cleaning process. The etching process to form the first through holes 405 can be a wet etching, a dry etching, or a combination thereof. It is noted that, in the direction perpendicular to the surface of the substrate 201, the depth of the one or more first through holes 405 in the third region 300 can be larger than the depth of the one or more first through holes 405 in the first region 100.

[00257] At S403, a first channel structure 406 can be formed on the surface of the substrate 401 that is exposed by each of the plurality of first through holes 405, as shown in FIG. 76. In some embodiments, the first channel structure 406 can be a polycrystalline silicon (polysilicon) layer formed by using a selective epitaxial process.

[00258] At S404, a first functional layer can be formed on the sidewall of each of the plurality of first through holes 405. The first functional layer can include a first tunneling layer 407, a first storage layer 408, a first barrier layer 409, and a first passivation layer 410.

[00259] As shown in FIG. 77, the first tunneling layer 407 can be formed on the sidewall of the plurality of first through holes 405 and the exposed surfaces of the first channel structures 406. The first tunneling layer 407 can be used for generating electronic charges (electrons or holes). In some embodiments, the first tunneling layer 407 can be an oxide layer formed by using a deposition process.

[00260] The first storage layer 408 can be formed on the surface of the first tunneling layer 407. The first storage layer 408 can be used for storing electronic charges. The storage or removal of charge in the first storage layer 407 can impact the on/off state and/or a conductance of the semiconductor channel. The first storage layer 407 can include polycrystalline silicon (polysilicon) or silicon nitride. In some embodiments, the first storage layer 408 can be a nitride layer formed by using a deposition process.

[00261] The first barrier layer 409 can be formed on the surface of the first storage layer 408. The first barrier layer 409 can be used for blocking the outflow of the electronic charges stored in the first storage layer 408. In some embodiments, the first barrier layer 409 can be a silicon oxide layer or a combination of silicon oxide/silicon nitride/silicon oxide (ONO) layers. In some embodiments, the first barrier layer 409

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includes high dielectric constant (high-k) dielectrics (e.g., aluminum oxide). In one example, the first barrier layer 409 is an oxide layer formed by using a deposition process.

[00262] As shown in FIG. 78, a first passivation layer 410 can be formed on the surface of the first barrier layer 409. The first passivation layer 410 can be used for protecting the first barrier layer 409 from being damaged in a subsequent removal process. In some embodiments, the first passivation layer 410 can be an amorphous silicon layer formed by using a deposition process.

[00263] The portions of the first passivation layer 410, the first barrier layer 409, the first storage layer 408 and the first tunneling layer 407 located on the surfaces of the plurality of first channel structures 406 on the bottom of the plurality of first through holes 405 can be removed. In some embodiments, the removal process can include an etching process and a cleaning process. As such, the first functional layer can be formed on the sidewalls of the plurality of first through holes 405.

[00264] In some embodiment, in the same removal process, the first barrier layer 409, the first storage layer 408, the first tunneling layer 407, and the oxide layer of the first mask layer 404 located on the surface of the nitride layer of first mask layer 404 can also be removed. As such, the nitride layer of first mask layer 404 is remained on the surface of the first insulating connection layer 403.

[00265] At S405, a second channel structure can be formed on the sidewall of the first functional layer and the exposed surface of the first channel structure 406 in each of the plurality of first through holes 405. The second channel structure can be in contact with the first channel structure 406 in each first through hole 405. The surface of the second channel structure in each first through hole 405 can be lower than the top surface of the first insulating connection layer 403.

[00266] As shown in FIG. 79, a second channel layer 411 can be formed to cover the sidewalls of the first passivation layer 410 and the bottom of each of the plurality of first through holes 405. The second channel layer 411 can also cover the surface of the first insulating connection layer 403, or cover the surface of the nitride layer of the first mask layer 404. In some embodiments, the second channel layer 411 can be an amorphous silicon layer formed by using a deposition process.

[00267] As shown in FIGs. 80A and 80B, a portion of the second channel layer 411 can be removed, such that the top surface of the second channel layer 411 can be lower than the

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top surface of the first insulating connection layer 403. The remaining portion of the second channel layer 411 can form the second channel structure that is in contact with the first channel structure 406. In some embodiments, the portion of the second channel layer 411 can be removed by using an etching process.

[00268] It is noted that, in various embodiments, the top surface of the second channel structure can be higher than the top surface of the first stacked layer 402 or lower than the top surface of the first stacked layer 402. However, the top surface of the second channel structure is not lower than the top surface of the top oxide layer in the first stacked layer 402. In some embodiments, the top surface of the second channel structure can be higher than the top nitride layer in the first stacked layer 402, as shown in FIG. 80A. In some alternative embodiments, the top surface of the second channel structure is in a same plane of the top surface of the top oxide layer in the first stacked layer 402, as shown in FIG. 80B.

[00269] At S406, a first groove can be formed above the first insulating connection layer 403 above each of the plurality of first through holes 405. In some embodiments, the projection of the first groove on the substrate 401 can completely cover the projection of the corresponding first through hole 405 on the substrate 401.

[00270] As shown in FIGs. 81A and 81B, the nitride layer of the first mask layer 404 can be removed. In some embodiments, the nitride layer of the first mask layer 404 can be removed by using an etching process.

[00271] As shown in FIGs. 82A and 82B, the surface of the first insulating connection layer 403 can be planarized by any suitable techniques, such as backside grinding, and/or chemical mechanical polishing (CMP). A portion of the first insulating connection layer 403 can be removed to form a plurality of first grooves that penetrate the first insulating connection layer 403. An area of the projection of each of the plurality of first grooves on the substrate 401 can be larger than an area of the projection of each of the plurality of first through holes 405 on the substrate 401.

[00272] In some embodiments, a depth of the first groove 412 can be equal to or less than the thickness of the planarized first insulating connection layer 403, as shown in FIG. 82A. For example, the depth of the first groove 412 can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 403 is about 90nm, while the depth of the first groove is about 60nm.

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[00273] In some alternative embodiments, the depth of the first groove 412 can be greater than the thickness of the planarized first insulating connection layer 403, as shown in FIG. 82B. That is, a portion of the top nitride layer in the first stacked layer 402 can also be removed to form the first groove. For example, the depth of the first groove 412 can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 403 is about 30nm, while the depth of the first groove is about 60nm.

[00274] At S407, a third channel structure 413 can be formed in each of the plurality of first grooves 412. As shown in FIGs. 83A and 83B, the third channel structure 413 can be in contact with the second channel structure in each of the plurality of first through holes 405. In some embodiments, the third channel structure 413 can be a polycrystalline silicon player formed by using a deposition process.

[00275] A thickness of each third channel structure 413 can be equal to the depth of each first groove 412. As described above, in some embodiments, a thickness of each third channel structure 413 can be equal to or less than the thickness of the planarized first insulating connection layer 403, as shown in FIG. 83A. For example, the thickness of each third channel structure 413 can be in a range between 50nm and 70nm, preferably about 60nm. In some alternative embodiments, the thickness of each third channel structure 413 can be greater than the thickness of the planarized first insulating connection layer 403, as shown in FIG. 83B. For example, the thickness of each third channel structure 413 can be in a range between 60nm and 80nm, preferably about 70nm.

[00276] Referring to FIG. 103B, at S408, a second stacked layer 414 and a second insulating connection layer 415 can be sequentially formed on the plurality of third channel structures 413. As shown in FIG. 84, the second stacked layer 414 can include a plurality of oxide/nitride layer pairs, such as silicon oxide layers and silicon nitride layers. Similar to the first stacked layer 402 as described above, the multiple oxide layers (shown in the areas with dotes) and multiple nitride layers (shown in the areas with meshes) in the second stacked layer 414 alternate in a vertical direction. The second stacked layer 414 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide layers and the nitride layers in the second stacked layer 414 is equal to or larger than 64.

[00277] In some embodiments, the second insulating connection layer 415 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is

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noted that, the material of the second insulating connection layer 415 can be different from the material of the nitride layer in the second stacked layer 414.

[00278] Further, in some embodiments, a second mask layer 416 can be formed on the surface of the second insulating connection layer 415. The second mask layer 416 can include a nitride layer on the surface of the second insulating connection layer 415, and an oxide layer on the surface of such nitride layer.

[00279] At S409, one or more second through holes 417 are formed in each of the first region 100, the second region 200, and the third region 300. As shown in FIG. 85, each of the plurality of second through holes 417 can completely penetrate the second stacked layer 414, the second insulating connection layer 415, and the second mask layer 416, and can extend into the surface of the corresponding third channel structure 413. The projection of each second through hole 417 on the substrate 401 can at least partially overlap with the projection of the corresponding first through hole 405 on the substrate 401.

[00280] In some embodiments, the second stacked layer 414, the second insulating connection layer 415, the second mask layer 416, and the third channel structures 413 can be etched to form the plurality of second through holes 417 that penetrate the second stacked layer 414 and the second insulating connection layer 415. The second stacked layer 414, the second insulating connection layer 415, the second mask layer 416, and/or the third channel structure 413 can be etched by using a dry etching process, a wet etching process, or a combination thereof. A cleaning process can then be performed to clean the plurality of second through holes 417.

[00281] It is noted that, each second through hole 417 can extend to the surface of the corresponding third channel structure 413, or can extend into the corresponding third channel structure 413. As such, a fourth channel structure formed subsequently in each second through hole 417 can directly contact the corresponding third channel structure.

[00282] In some embodiments, a maximum difference between the radius of the top aperture of each second through hole 417 and the radius of the bottom aperture of the second through hole 417 can be 15nm. That is, as shown in FIG. 85, a distance "a" between the boundary line of the top surface of each second through hole 417 and the boundary of the bottom surface of the second through hole 417 can be no more than 15 nm.

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[00283] At S4010, a second functional layer can be formed on the sidewall of each second through hole 417. In some embodiments, the second functional layer can include a second tunneling layer 418, a second storage layer 419, a second barrier layer 420, and a second passivation layer 421.

[00284] As shown in FIG. 86, the second tunneling layer 418 can be formed on the sidewall of each second through hole 417 and the surface of the corresponding third channel structure 413. The second tunneling layer 418 can be used for generating electronic charges. In some embodiments, the second tunneling layer 418 can be an oxide layer formed by using a deposition process.

[00285] The second storage layer 419 can be formed on the surface of the second tunneling layer 418. The second storage layer 419 can be used for storing electronic charges. In some embodiments, the second storage layer 419 can be a nitride layer formed by using a deposition process.

[00286] The second barrier layer 420 can be formed on the surface of the second storage layer 419. The second barrier layer 420 can be used for blocking the outflow of the electronic charges in the second storage layer 419. In some embodiments, the second barrier layer 420 can be an oxide layer formed by using a deposition process.

[00287] As shown in FIG. 87, a second passivation layer 421 can be formed on the surface of the second barrier layer 420. The second passivation layer 421 can be used for protecting the second barrier layer 420 from being damaged in a subsequent removal process. In some embodiments, the second passivation layer 421 can be an amorphous silicon layer formed by using a deposition process.

[00288] As shown in FIG. 87, the portions of the second passivation layer 421, the second barrier layer 420, the second storage layer 419, the second tunneling layer 418, and the third channel structure 413 between each second through hole 417 and the corresponding first through hole 405 can be removed. In some embodiments, the removal process can include an etching process and a cleaning process. In some embodiments, the portions of the second passivation layer 421, the second barrier layer 420, the second storage layer 419, the second tunneling layer 418, the oxide layer of the second mask layer 416 that are located on the nitride layer of the second mask layer 416 can also be removed by the same removal process. As such, the second functional layer can be formed on the sidewall of each second through hole 417, and each second through hole 417 and the corresponding first through hole 405 can be interconnected with each other.

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[00289] In some embodiments, the portions of the second barrier layer 420, the second storage layer 419, and the second tunneling layer 418 that are located under the second passivation layer 421, as shown in the dashed circle in FIG. 88, can also be removed by using an etching process.

[00290] At S4011, the second tunneling structure, the third tunneling structure, the second passivation layer 421, and the first passivation layer 410 can be removed. In some embodiments, the second tunneling structure, the third tunneling structure, the second passivation layer 421, and the first passivation layer 410 can be removed by using one or more etching processes. As such, a plurality of third through holes 422 can be formed in the first region 100, the second region 200, and the third region 300 by interconnecting each first through hole and the corresponding second through hole, as shown in FIG. 89.

[00291] At S4012, a fourth channel structure can be formed on the sidewall of the second functional layer and the exposed surface of the third channel structure in each third through hole 422 in the first region 100. Further, a first filling structure can be formed in each of the plurality of third through holes 422 in the first region 100, the second region 200, and the third region 300. In some embodiments, the top surface of the fourth channel structure can be higher than the top surface of the first filling structure.

[00292] As shown in FIG. 90, a fourth channel layer 428 can be formed to cover the sidewall and the bottom surface of each of the plurality of third through holes 422 in the first region 100, the second region 200, and the third region 300. In some embodiments, the fourth channel layer 428 can also cover the top surface of the nitride layer of the second mask layer 416. In some embodiments, the fourth channel layer 428 can be an amorphous silicon layer formed by using a deposition process. In some embodiments, the fourth channel structure 428 includes a joint channel structure that is sandwiched between the first stacked layer 402 and the second stacked layer 414, and covers the exposed surface of the first insulating connection layer 403.

[00293] As shown in FIG. 91, a second filling layer 429 can be formed to cover the fourth channel layer 428. In some embodiments, the second filling layer 429 can include one or more airgaps in each third through hole 417. In some embodiments, the second filling layer 429 can be an oxide layer formed by using a deposition process.

[00294] As shown in FIG. 92, a third mask layer 430 can be formed on the top surface of the second filling layer 429 in the first region 100. Using the third mask layer 430 as

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a mask, the portions of the second filling layer 429 located in the second region 200 and the third region 300 can be removed by using an etching process.

[00295] As shown in FIG. 93, the third mask layer 430 can be removed. Using the remaining second filling layer 429 in the first region 100 as a mask, the fourth channel layer 428 located in the second region 200 and the third region 300 can be removed by using an etching process. As such, one or more fourth through holes 431 can be formed in the second region 200 and the third region 300.

[00296] As shown in FIG. 94, a third filling layer 432 can be formed to cover the sidewall and the bottom of the one or more fourth through holes 431 in the second region 200 and the third region 300. The third filling layer 432 can also cover the exposed surface of the first insulating connection layer 403 in each fourth through hole 431 in the second region 200 and the third region 300. In some embodiments, the third filling layer 432 can enclose one or more airgap in one or more fourth through holes 431. In some embodiments, the filling performance of the third filling layer 432 can be better than the filling performance of the second filling layer 429. That is, in a same removing process, the removal rate of the third filling layer 432 can be less than the removal rate of the second filling layer 429.

[00297] As shown in FIG. 95, the second filling layer 429 on the surface of the fourth channel layer 428 in the first region 100 can be removed by using an etching process. As such, one or more fifth through holes 433 can be formed in the first region 100. It is noted that, a portion of the third filling layer 432 can also be removed by the same etching process.

[00298] As shown in FIG. 96, a first filling layer 434 can be formed in each fifth through hole 433 in the first region 100, and in each fourth through hole 431 in the second region 200 and the third region 300. The material of the first filling layer 434 can be the same material of the third filling layer 432.

[00299] As shown in FIG. 97, a portion of the first filling layer 434 can be removed by using an etching process, such that the top surface of the first filling layer 434 in each fifth through hole 433 or fourth through hole 431 is lower than the top surface of the second insulating connection layer 415. The remaining portion of the first filling layer 434 in each fourth through hole 431 or fifth through hole 433 can form the first filling structure.

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[00300] Further, the portion of the fourth channel layer 428 located on the surface of the second insulating connection layer 415 or the surface of the second mask layer 416 can be removed by using an etching process. The remaining portion of the fourth channel layer 428 in each fifth through hole 433 can form the fourth channel structure. The top surface of the fourth channel structure can be higher than the top surface of the first filling structure. As such, a second groove can be formed on the fourth channel structure and the first filling structure in each fifth through hole 433 in the first region 100, and on the first filling structure in each fourth through hole 431 in the second region 200 and the third region 300.

[00301] It is noted that, the top surface of the fourth channel structure can be higher than the top surface of the second stacked layer 414, or can be lower than the top surface of the second stacked layer 414. The top surface of the fourth channel structure is not lower than the top surface of the top oxide layer in the second stacked layer 414. In some embodiments, the top surface of the fourth channel structure can be in a same plane of the top surface of the top oxide layer in the second stacked layer 414.

[00302] At S4013, a fifth channel structure can be formed in the second groove of each fifth through hole 433 in the first region 100 and each fourth 431 in the second region 200 and third region 300. The fifth channel structure can be in contact with the fourth channel structure in each fifth through hole 433 in the first region 100.

[00303] As shown in FIG. 99, the fifth channel structure 435 can be formed in the second groove that is on the fourth channel structure and the first filling structure in each fifth through hole 433 in the first region 100. The fifth channel structure 435 can also be formed in the second groove that is on the first filling structure in each fourth through hole 431 in the second region 200 and the third region 300.

[00304] As shown in FIG. 100, the nitride layer of the second mask layer 416 can be then removed by an etching process. As shown in FIGs. 101A and 101B, the top surface of the second insulating connection layer 415 and the top surface of the plurality of fifth channel structures 435 can be planarized by any suitable techniques, such as backside grinding, and/or chemical mechanical polishing (CMP).

[00305] Accordingly, the disclosed method as shown in FIGs. 101A and 101B can form another joint opening structure of a three-dimensional (3D) memory device by combining two through hole formation processes. As such, the formed channel holes having the joint opening structure can have a large aspect ratio and a limited top-bottom aperture

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error. Further, the disclosed method of forming a joint opening structure in a 3D memory device can simultaneously form a plurality of channel holes, staircase dummy holes, and through array contact barriers, resulting in an efficient process capability control, a simplified process complexity, and a reduced cost.

[00306] In some embodiments, the present disclosure also provides another three-dimensional memory device formed by using the above disclosed method as shown in FIGs. 101A and 101B. The three-dimensional memory device can include a first region for forming a plurality of channel holes, a second region for forming a plurality of staircase structure (SS) dummy holes, and a third region for forming a plurality of through array contact (TAC) barriers. Along a direction perpendicular to the surface of the three-dimensional memory device, the three-dimensional memory device can include the following components.

[00307] A first stacked layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs, is formed on a substrate. A first insulating connection layer is formed on the first stacked layer. A plurality of first through holes penetrating the first stacked layer and the first insulating connection layer and extending into the surface of the substrate are formed in the first region, the second region, and the third region.

[00308] A first channel structure is formed on the surface of the substrate exposed by each first through hole. A first functional layer is formed on the sidewall of each first through hole. A second channel structure is formed on the sidewall of the first functional layer and the surface of the first channel structure in each first through hole. A first filling structure is formed on the sidewall and the surface of the second channel structure to fill each of the plurality of first through holes. In some embodiments, an airgap can be enclosed in the first filling structure in each first through hole. The top surfaces of the second channel structure and the first filling structure are lower than the top surfaces of the first insulating connection layer.

[00309] A first groove is formed in the first insulating connection layer, and above the first functional layer, the second channel structure and the first filling structure in each first through hole. A projection of each of the plurality of first grooves on the substrate completely covers a projection of the corresponding first through hole on the substrate. A third channel structure in contact with the second channel structure in the corresponding first through hole is formed in each first groove.

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[00310] A second stack layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs, is formed on the top surfaces of the first insulating connection layer and the plurality of third channel structures. A second insulating connection layer is formed on the second stack layer. A plurality of second through holes penetrating through the second stacked layer and the second insulating connection layer and extending into a surface of the third channel structure are formed in the first region, the second region, and the third region. A projection of each of the plurality of second through holes on the substrate at least partially overlaps the projection of the corresponding first through hole on the substrate.

[00311] A second functional layer is formed on the sidewall of each second through hole. A fourth channel structure is formed on the sidewall of the second functional layer and the bottom surface of each second through hole in the first region. A second filling is formed to fill each of the plurality of second through holes in the first region, the second region, and the third region. In some embodiments, an airgap can be enclosed in the second filling structure. The top surface of the fourth channel structure is higher than the top surface of the second filling structure in each second through hole in the first region.

[00312] In the first region, a fifth channel structure in contact with the fourth channel structure is formed in a second groove in each second through hole that is surrounded by the second functional layer, and above the fourth channel structure and the second filling structure. And in the second region and the third region, a fifth channel structure is formed in a second groove in each second through hole that is surrounded by the second functional layer, and above the second filling structure.

[00313] Due to the fourth channel structures being formed in the second through holes in the first region rather than the third region, the fifth channel structure in each second through hole in the first region can be electronically connected with the first channel structure in the corresponding first through hole, while the fifth channel structure in each second through hole in the third region can be electronically insulated with the first channel structure in the corresponding first through hole. Thus, in the three-dimensional memory device, a plurality of channel holes can be formed in the first region, and a plurality of through array contact (TAC) barriers can be formed in the third region. The plurality of staircase structure dummy holes in the second region can have a supporting function of the staircase structure.

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[00314] In some embodiments, as shown in FIG. 101A, in each channel hole in the first region, a thickness "b" of the first insulating connection layer, which is the distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 80nm and 100nm, preferably about 90nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00315] In some alternative embodiments, as shown in FIG. 101B, in each channel hole in the first region, a thickness "b" of the first insulating connection layer, which is the distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 20nm and 40nm, preferably about 30nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00316] Further, the difference between the radiuses of the top aperture and the bottom aperture of the second channel structure, and the difference between the radiuses of the top aperture and the bottom aperture of the fourth channel structure can be within 15nm. Accordingly, the disclosed channel hole having a joint opening structure can have a large aspect ratio and a limited top-bottom aperture error.

[00317] In some embodiments, a replacement process can be performed to replace each of the plurality of nitride layers in the first stacked layer 402 and the second stacked layer 414 with a conductive layer 440, as shown in FIGs. 102A and 102B. The conductive layer can include any suitable material that is electronically conductive, including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof.

[00318] In some embodiments, the replacement process can be performed in one or more of the first region 100, the second region 200, and the third region 300. In one embodiments, the replacement process is performed in the first region 100 and the second region 200, but not in the third region 300. That is, the first stacked layer and the second stacked layer in the first region and the second region can be alternating conductive/dielectric stack, while the first stacked layer and the second stacked layer in the third region can be alternating oxide/nitride stack.

[00319] In some embodiments, during the replacement process, a portion of the third channel structure 413 that is adjacent with the bottom nitride layer of the second stacked layer 414, or is adjacent with the top nitride layer of the first stacked layer 402 can be

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converted to an oxide layer by an oxidation process. That is, as shown in FIGs. 102A and 102B, a thickness “c” of the third channel structure can be reduced after the replacement process. For example, the thickness “c” of the third channel structure can be reduced to a range between 30nm and 50nm, preferably about 40nm.

[00320] The provision of the examples described herein (as well as clauses phrased as "such as," "e.g.," "including," and the like) should not be interpreted as limiting the claimed subject matter to the specific examples; rather, the examples are intended to illustrate only some of many possible aspects.

[00321] Further, the words "first", "second" and the like used in this disclosure do not denote any order, quantity or importance, but are merely intended to distinguish between different constituents. The words "comprise" or "include" and the like mean that the elements or objects preceding the word can cover the elements or objects listed after the word and their equivalents, without excluding other elements or objects. The words "connect" or "link" and the like are not limited to physical or mechanical connections, but can include electrical connections, either directly or indirectly.

[00322] Although the present disclosure has been described and illustrated in the foregoing illustrative embodiments, it is understood that the present disclosure has been made only by way of example, and that numerous changes in the details of embodiment of the present disclosure can be made without departing from the spirit and scope of the present disclosure, which is only limited by the claims which follow. Features of the disclosed embodiments can be combined and rearranged in various ways. Without departing from the spirit and scope of the present disclosure, modifications, equivalents, or improvements to the present disclosure are understandable to those skilled in the art and are intended to be encompassed within the scope of the present disclosure.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0110002
	Application Number	
Title of Invention	JOINT OPENNING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME	

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Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Zhenyu		LU	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Wuhan, Hubei	Country of Residence [i]	CN

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.		
Address 2	18 Gaoxin 4th Road, East Lake High-Tech Dev. Zone		
City	Wuhan, Hubei	**State/Province**	
Postal Code	430074	**Country** [i]	CN

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Wenguang		SHI	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Wuhan, Hubei	Country of Residence [i]	CN

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.		
Address 2	18 Gaoxin 4th Road, East Lake High-Tech Dev. Zone		
City	Wuhan, Hubei	**State/Province**	
Postal Code	430074	**Country** [i]	CN

Inventor 3 Remove

Legal Name

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0110002
	Application Number	
Title of Invention	JOINT OPENNING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME	

Prefix	Given Name	Middle Name	Family Name	Suffix
	Guanping		WU	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Wuhan, Hubei	Country of Residence [i]	CN

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.		
Address 2	18 Gaoxin 4th Road, East Lake High-Tech Dev. Zone		
City	Wuhan, Hubei	**State/Province**	
Postal Code	430074	**Country** [i]	CN

Inventor 4 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Feng		PAN	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Wuhan, Hubei	Country of Residence [i]	CN

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.		
Address 2	18 Gaoxin 4th Road, East Lake High-Tech Dev. Zone		
City	Wuhan, Hubei	**State/Province**	
Postal Code	430074	**Country** [i]	CN

Inventor 5 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Xianjin		WAN	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Wuhan, Hubei	Country of Residence [i]	CN

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.		
Address 2	18 Gaoxin 4th Road, East Lake High-Tech Dev. Zone		
City	Wuhan, Hubei	**State/Province**	
Postal Code	430074	**Country** [i]	CN

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PTO/AIA/14 (02-18)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0110002
	Application Number	
Title of Invention	JOINT OPENNING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME	

Inventor 6 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Baoyou		CHEN	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Wuhan, Hubei	Country of Residence [i]	CN

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.		
Address 2	18 Gaoxin 4th Road, East Lake High-Tech Dev. Zone		
City	Wuhan, Hubei	**State/Province**	
Postal Code	430074	**Country** [i]	CN

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	26111		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	JOINT OPENNING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME		
Attorney Docket Number	4123.0110002	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	120	**Suggested Figure for Publication (if any)**	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0110002
	Application Number	
Title of Invention	JOINT OPENNING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	26111		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	PCT/CN2018/077785	2018-03-01

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

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PTO/AIA/14 (02-18)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0110002
	Application Number	
Title of Invention	JOINT OPENNING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME	

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove			
Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201710134782.1	CN	2017-03-08	
Remove			
Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201710134783.6	CN	2017-03-08	

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

PTO/AIA/14 (02-18)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0110002
	Application Number	
Title of Invention	JOINT OPENNING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0110002
	Application Number	
Title of Invention	JOINT OPENNING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

○ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
◉ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Yangtze Memory Technologies Co., Ltd.		
Mailing Address Information For Applicant:			
Address 1	18 Gaoxin 4th Road		
Address 2	East Lake High-Tech Development Zone		
City	Wuhan, Hubei	**State/Province**	
Country	CN	Postal Code	430074
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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PTO/AIA/14 (02-18)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0110002
	Application Number	
Title of Invention	JOINT OPENNING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☒

Organization Name	Yangtze Memory Technologies Co., Ltd.

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1	18 Gaoxin 4th Road		
Address 2	East Lake High-Tech Development Zone		
City	Wuhan, Hubei	**State/Province**	
Country i	CN	Postal Code	430074
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Donald J. Featherstone/			Date (YYYY-MM-DD)	2018-07-26
First Name	Donald	Last Name	Featherstone	Registration Number	33,876

Additional Signature may be generated within this form by selecting the Add button.

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Micron v. YMTC
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PTO/AIA/14 (02-18)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0110002
	Application Number	
Title of Invention	JOINT OPENNING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Micron v. YMTC
IPR2025-00244

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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IPR2025-00244

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: LU *et al.*	Confirmation No.: *To Be Assigned*
Applicant: **Yangtze Memory Technologies Co., Ltd.**	Art Unit: *To Be Assigned*
Application No.: *To Be Assigned*	Examiner: *To Be Assigned*
Filing Date: *Herewith*	Atty. Docket: 4123.0110002

Title: **JOINT OPENNING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME**

Authorization to Treat a Reply as Incorporating an Extension of Time Under 37 C.F.R. § 1.136(a)(3)

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

The U.S. Patent and Trademark Office is hereby authorized to treat any concurrent or future reply that requires a petition for an extension of time under this paragraph for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. The U.S. Patent and Trademark Office is hereby authorized to charge all required extension of time fees to our Deposit Account No. 19-0036, if such fees are not otherwise provided for in such reply.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: 7/26/18

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

9722585_1.docx

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 16/046,847

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						400
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	2120

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/046,847	07/26/2018	Zhenyu LU	4123.0110002

CONFIRMATION NO. 7612

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

FORMALITIES LETTER

OC000000101946287

Date Mailed: 08/30/2018

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.

The application is informal since it does not comply with the regulations for the reason(s) indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- A substitute specification in compliance with 37 CFR 1.52, 1.121(b)(3), and 1.125, is required. The substitute specification must be submitted with markings and be accompanied by a clean version (without markings) as set forth in 37 CFR 1.125(c) and a statement that the substitute specification contains no new matter (see 37 CFR 1.125(b)). The specification, claims, and/or abstract page(s) submitted is not acceptable and cannot be scanned or properly stored because:
  - The application contains drawings, but the specification does not contain a brief description of the several views of the drawings as required by 37 CFR 1.74 and 37 CFR 1.77(b)(9).

The following item(s) appear to have been **omitted** from the application:

- Figure(s) **22, 49, 73, 102** described in the specification.

Applicant must reply to this notice within the time period set forth in this notice to avoid abandonment of this application. Applicant must select one of the three following options and the reply must comply with the requirements set forth in the selected option and any other requirements set forth in this notice. The reply should also indicate which option applicant has selected.

I. Petition for date of deposit: Should applicant contend that the above-noted omitted item(s) was in fact deposited in the U.S. Patent and Trademark Office (USPTO) with the nonprovisional application papers, a copy of this Notice and a petition (and the petition fee set forth in 37 CFR 1.17(f) with evidence of such deposit **must** be

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filed within **TWO MONTHS** of the date of this Notice. The petition fee will be refunded if it is determined that the item(s) was received by the USPTO. **THIS TWO MONTH PERIOD IS EXTENDABLE UNDER 37 CFR 1.136(a) or (b).**

Applicant should review their application file and determine whether their file differs from USPTO's records. In some situations there may be a mislabeling of the drawings and/or a failure to describe in the brief description each of the figures as labeled.

The brief description of the drawings in the specification must correspond with the figures and the figures must be labeled in accordance with 37 CFR 1.84(u)(1). For example, if the brief description describes Figure 1 and Figure 2 only, but the drawings show Fig. 1 and Fig. 2A and Fig. 2B, then the specification must be amended to refer to Figure 2A and Figure 2B and delete the reference to Figure 2 and a substitute specification in compliance with 37 CFR 1.52, 1.121(b)(3), and 1.125, is required. As another example, if a drawing is labeled Figure 2, but there are actually multiple figures within the labeled Figure 2 having labels A, B, and C, then the drawings must be relabeled in accordance with 37 CFR 1.84(u)(1) (e.g., Fig. 2A, Fig. 2B, and Fig. 2C). If the specification does not refer to the figures as relabeled, then the specification must be amended to refer to the relabeled figures (e.g., Fig. 2A, Fig. 2B, and Fig. 2C) and a substitute specification in compliance with 37 CFR 1.52, 1.121(b)(3), and 1.125, is required. A petition for date of deposit under option I should **NOT** be filed in either situation or in similar situations where there is simply a mislabeling of the drawings and/or a failure to describe in the brief description each of the figures. Instead, applicant should file a reply under option III.A below (including replacement drawing sheets and/or a substitute specification as required in III.A.2).

II. Petition for later filing date: Should applicant desire to supply the omitted item(s) and accept the date that such omitted item(s) was filed in the USPTO as the filing date of the above-identified application, a copy of this Notice, the omitted item(s), and a petition under 37 CFR 1.182 with the petition fee set forth in 37 CFR 1.17(f) requesting the later filing date **must** be filed within **TWO MONTHS** of the date of this Notice. **THIS TWO MONTH PERIOD IS EXTENDABLE UNDER 37 CFR 1.136(a) or (b).**
Applicant is advised that generally the filing fee required for an application is the filing fee in effect on the filing date accorded the application and that payment of the requisite basic filing fee on a date later than the filing date of the application requires payment of a surcharge (37 CFR 1.16(f)). To avoid processing delays and payment of a surcharge, applicant should submit any balance due for the requisite filing fee based on the later filing date being requested when submitting the omitted item(s) and the petition (and petition fee) requesting the later filing date.

III. Acceptance of application as deposited: Applicant may accept the application as deposited in the USPTO by filing an appropriate amendment as set forth in either (A) or (B) below within **TWO MONTHS** of the date of this Notice. **THIS TWO MONTH PERIOD IS EXTENDABLE UNDER 37 CFR 1.136(a) or (b)** . The application will maintain a filing date as of the date of deposit of the application papers in the USPTO, and original application papers (i.e., the original disclosure of the invention) will include only those application papers present in the USPTO on the date of deposit. A petition is not required for this option.
(A) If applicant wants to accept the application as deposited without adding the subject matter that was in the omitted item (e.g., a missing page or figure), applicant is required to submit one or more of the following items without adding any new matter (see 35 U.S.C. 132(a)):

1. For a missing page of the specification,
   a) a substitute specification including claims that amends the specification to renumber the pages consecutively and cancels any incomplete sentences, and
   b) a statement that the substitute specification includes no new matter, in compliance with 37 CFR 1.121(b)(3) and 1.125;
2. For a missing figure of the drawings (including a mislabeled figure),
   a) replacement drawing sheets in compliance with 37 CFR 1.121(d) to renumber the drawing figures consecutively (if necessary),

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b) a substitute specification excluding claims that amends the specification to cancel any references to any omitted drawing(s) and corrects the references in the specification to the drawing figures to correspond with any relabeled drawing figures, and
c) a statement that the substitute specification includes no new matter, in compliance with 37 CFR 1.121(b)(3) and 1.125;

3. For a missing page of the claim listing only, a replacement claim listing with the claims renumbered consecutively or, if amendment to the claims is also necessary, then a complete claim listing in compliance with 37 CFR 1.121(c);
4. For a missing or unreadable compact disc,
   a) a substitute specification (excluding the claims) deleting the reference to the compact disc and the files contained on the compact disc, and
   b) a statement that the substitute specification includes no new matter, in compliance with 37 CFR 1.121(b)(3) and 1.125; and
5. For a missing or unreadable file submitted on a compact disc,
   a) a substitute specification (excluding the claims) deleting the reference to the missing or unreadable file, and a statement that the substitute specification includes no new matter, in compliance with 37 CFR 1.121(b)(3) and 1.125; and
   b) a replacement transmittal letter listing all of the files except the missing or unreadable file in compliance with 37 CFR 1.52(e)(3)(ii).

(B) Alternatively, if applicant wants to accept the application as deposited but wishes to add the subject matter in the omitted item (e.g., a missing page or figure) by relying on an incorporation by reference under 37 CFR 1.57 or other portions of the original disclosure, applicant is required to submit one or more of the following items without adding any new matter (see 35 U.S.C. 132(a)):

1. To add the subject matter in a missing page of specification,
   a) a substitute specification excluding claims and
   b) a statement that the substitute specification includes no new matter, in compliance with 37 CFR 1.121(b)(3) and 1.125;
2. To add a missing figure of the drawings, new and replacement drawing sheets in compliance with 37 CFR 1.121(d);
3. To add the subject matter in a missing page of the claim listing, a complete claim listing in compliance with 37 CFR 1.121(c) (e.g., a claim in the missing page should be submitted as a new claim);
4. To add the subject matter in a missing or unreadable compact disc,
   a) a replacement compact disc and a duplicate copy of the compact disc, in compliance with 37 CFR 1.52(e); and
   b) a statement that the replacement compact disc contains no new matter in compliance with 37 CFR 1.52(e)(4); and,
5. To add the subject matter in a missing or unreadable file submitted on a compact disc,
   a) a replacement compact disc that contains all of the files listed in the specification including the missing or unreadable file and a duplicate copy of the compact disc, in compliance with 37 CFR 1.52(e); and
   b) a statement that the replacement compact disc contains no new matter in compliance with 37 CFR 1.52(e)(4).

If applicant is relying on an incorporation by reference under 37 CFR 1.57 to add the omitted subject matter, then applicant must also comply with the requirements of 37 CFR 1.57.

Applicant is cautioned that correction of the above items may cause the specification and drawings page count to exceed 100 pages. If the specification and drawings exceed 100 pages, applicant will need to submit the required application size fee.

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- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **300** basic filing fee.
- $ **400** for **42** electronically equivalent pages in excess of **100** application size fee.
- $ **160** surcharge.
- $ **660** search fee.
- $ **760** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **2280** TOTAL FEE BALANCE DUE.

Items Required To Avoid Processing Delays:

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  Zhenyu LU
  Wenguang SHI
  Guanping WU
  Feng PAN
  Xianjin WAN
  Baoyou CHEN

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Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/ygizaw/

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/046,847	07/26/2018	2811	0.00	4123.0110002	20	3

CONFIRMATION NO. 7612

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

FILING RECEIPT

OC000000101946286

Date Mailed: 08/30/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Zhenyu LU, Wuhan, CHINA;
Wenguang SHI, Wuhan, CHINA;
Guanping WU, Wuhan, CHINA;
Feng PAN, Wuhan, CHINA;
Xianjin WAN, Wuhan, CHINA;
Baoyou CHEN, Wuhan, CHINA;

Applicant(s)

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Assignment For Published Patent Application

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Power of Attorney: The patent practitioners associated with Customer Number 26111

Domestic Priority data as claimed by applicant

This application is a CON of PCT/CN2018/077785 03/01/2018

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
CHINA 201710134782.1 03/06/2017
CHINA 201710134783.6 03/08/2017

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

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Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 08/29/2018

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/046,847**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

JOINT OPENNING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign

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patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

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PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT5258007

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
ZHENYU LU	09/12/2018
WENGUANG SHI	10/15/2018
GUANPING WU	09/13/2018
XIANJIN WAN	09/13/2018
BAOYOU CHEN	09/13/2018

RECEIVING PARTY DATA

Name:	YANGTZE MEMORY TECHNOLOGIES CO., LTD.
Street Address:	18 GAOXIN 4TH ROAD
Internal Address:	EAST LAKE HIGH-TECH DEVELOPMENT ZONE
City:	WUHAN, HUBEI
State/Country:	CHINA
Postal Code:	430074

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	16046847

CORRESPONDENCE DATA

Fax Number: (202)371-2540

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 2023712600
Email: wshu@sternekessler.com, deniseb@sternekessler.com
Correspondent Name: STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
Address Line 1: 1100 NEW YORK AVENUE, NW
Address Line 4: WASHINGTON, D.C. 20005

ATTORNEY DOCKET NUMBER:	4123.0110002
NAME OF SUBMITTER:	DONALD J. FEATHERSTONE
SIGNATURE:	/Donald J. Featherstone/
DATE SIGNED:	11/29/2018
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 4
source=41230110002_ASGN#page1.tif
source=41230110002_ASGN#page2.tif
source=41230110002_ASGN#page3.tif
source=41230110002_ASGN#page4.tif

COMBINED DECLARATION AND ASSIGNMENT

DECLARATION

As the below named inventors, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 16/046,847

filed on July 26, 2018

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar ($1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is 18 Gaoxin 4th Road, East Lake High-Tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **JOINT OPENNING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME** for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 26111** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

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IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: **Zhenyu LU** Date: 2018.9.12.

Signature of Inventor: Zhenyu Lu

LEGAL NAME OF INVENTOR

Inventor: **Wenguang SHI** Date: 10/15/2018

Signature of Inventor:

LEGAL NAME OF INVENTOR

Inventor: **Guanping WU** Date: 2018.9.13

Signature of Inventor:

LEGAL NAME OF INVENTOR

Inventor: **Feng PAN** Date:

Signature of Inventor:

LEGAL NAME OF INVENTOR

Inventor: **Xianjin WAN** Date: 2018.9.13

Signature of Inventor: Xianjin Wan

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IPR2025-00244

LEGAL NAME OF INVENTOR

Inventor: Baoyou CHEN Date: 2018.9.13

Signature of Inventor: Baoyou CHEN

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: LU *et al.*	Confirmation No.: 7612
Applicant: Yangtze Memory Technologies Co., Ltd.	Art Unit: 2811
Application No.: 16/046,847	Examiner: To Be Assigned
(*Continuation of Appl. No. PCT/CN2018/077785; Filed: March 1, 2018*)	Atty. Docket: 4123.0110002
Filing Date: July 26, 2018	

Title: **JOINT OPENING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME** (as amended)

Preliminary Amendment Under 37 C.F.R. § 1.115

Mail Stop Missing Parts

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

In response to the Notice to File Missing Parts of Nonprovisional Application dated August 30, 2018, and in advance of prosecution, Applicant submits the following amendments and remarks. Applicant accepts the present application as deposited in the Office. Accordingly, this application shall maintain its filing date of July 26, 2018.

Amendments to the Specification begin on page 2 of this paper.

Remarks and Arguments begin on page 3 of this paper.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments to the Specification

Please enter the Substitute Specification filed herewith. Marked-up and clean versions of the Substitute Specification are provided.

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Remarks

The specification has been amended to correct the spelling of "OPENING" in the title. The "Brief Description of the Drawings" section has been amended at ¶¶ [0026], [0028], [0030], [0032], [0045], [00114], [00189] and [00247] to correctly identify the drawings that coincide with the drawing numbers improperly recited in the original specification. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Conclusion

Prompt and favorable consideration of this Preliminary Amendment is respectfully requested. Applicant believes the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

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1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

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JOINT ~~OPENNING~~ OPENING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application claims priority to PCT/CN2018/077785 filed on March 1, 2018, which claims the priorities of Chinese Patent Application No. 201710134782.1, filed on March 8, 2017, and Chinese Patent Application No. 201710134783.6, filed on March 8, 2017, the entire contents of which are incorporated herein by reference.

TECHNICAL FIELD

[0002] The present disclosure generally relates to the field of semiconductor technology, and more particularly, to joint opening structures of three-dimensional (3D) memory devices and method for forming the same.

BACKGROUND

[0003] As semiconductor technology advances, three-dimensional (3D) memory devices, such as 3D NAND memory devices, keep scaling more oxide/nitride (ON) layers. As such, it becomes difficult to use a single etching process to form the channel holes in the 3D memory devices that have a substantial depth. As the channel hole aspect ratio increases, channel hole etching becomes exponentially slower. Further, the process capability control of the formed channel holes, including bow-free, straight profile, critical dimension (CD) uniformity, minimal twisting, etc., tend to be more challenging. Thus, a single etching method may not be efficient in both cost and process capability.

BRIEF SUMMARY

[0004] In accordance with some embodiments of the present disclosure, joint opening structures of three-dimensional (3D) memory devices and method for forming the same are provided.

[0005] One aspect of the present disclosure provides a method of forming a joint opening structure in a three-dimensional (3D) memory device. The method includes forming a

first stacked layer and forming a first insulating connection layer on the first stacked layer, forming a first through hole that penetrates the first stacked layer and the first insulating connection layer, forming a first channel structure overlay the surface of the substrate that is exposed by the first through hole, forming a first functional layer on the sidewall of the first through hole, forming a second channel structure and forming a first filling structure on the sidewall of the first functional layer and the exposed surface of the first channel structure, and forming a third channel structure in contact with the second channel structure above the first through hole. A projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate. The method further includes forming a second stacked layer and forming a second insulating connection layer on the first insulating connection layer, forming a second through hole that penetrates the second stacked layer and the second insulating connection layer. A projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate. The method further includes forming a second functional layer on the sidewall of the second through hole, forming a fourth channel structure and forming a second filling structure on the sidewall of the second functional layer and the exposed surface of the third channel structure, and forming a fifth channel structure in contact with the fourth channel structure above the second through hole.

[0006] In some embodiments, the first stacked layer includes a first number of oxide/nitride layer pairs, and the second stacked layer includes a second number of oxide/nitride layer pairs. The first number and the second number are not less than 32.

[0007] Forming the first functional layer includes forming a first tunneling layer on the sidewall of the first through hole and the exposed surface of the first channel structure. The first tunneling layer is configured, in operation, to generate charges. Forming the first functional further includes forming a first storage layer on the surface of the first tunneling layer to store the charges generated by the first tunneling layer, forming a first barrier layer on the surface of the first storage layer to block the outflow of charges in the first storage layer, forming a first passivation layer on the surface of the first barrier layer to protect the first barrier layer from being damaged in a subsequent removal process, and removing portions of the first passivation layer, the first barrier layer, the first storage layer, and the first tunneling layer on the surface of the first channel structure. The remaining portions of the first passivation layer, the first barrier layer, the first storage

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layer, and the first tunneling layer on the sidewall of the first through hole form the first functional layer.

[0008] Forming the second channel structure and the first filling structure includes forming a second channel layer that covers the sidewall of the first passivation layer and the exposed surface of the first channel layer, forming the first filling layer that covers the surface of the second channel layer, removing a portion of the first filling layer to form the first filling structure, wherein the top surface of the first filling structure is lower than the top surface of the first insulating connection layer, and removing a portion of the second channel layer to form the second channel structure. A top surface of the second channel structure is lower than a top surface of the first insulating connection layer.

[0009] Forming the third channel structure includes etching the first insulating connection layer to form a first groove. In some other embodiments, forming the third channel structure includes etching the first insulating connection layer and at least a portion of the top nitride layer of the first stacked layer to form a first groove. A projection of the first groove on the substrate covers the projection of the first through hole on the substrate. Forming the third channel structure further includes forming a third channel layer in the first groove, wherein the third channel layer is in contact with the second channel structure, and planarizing the top surfaces of the first insulating connection layer and the third channel layer to form the third channel structure.

[0010] In some embodiments, the method further includes forming a first mask layer overlaying the first insulating connection layer before forming the first through hole, and removing the first mask layer after forming the third channel structure, and forming a second mask layer on the second insulating connection layer before forming the second through hole, and removing the first mask layer after forming the fifth channel structure

[0011] Forming the fourth channel structure and the second filling structure includes forming a fourth channel layer that covers the sidewall of the second functional layer and the exposed surface of the third channel layer, forming a second filling layer that covers the surface of the fourth channel layer, removing a portion of the second filling layer to form the second filling structure, and removing a portion of the fourth channel layer to form the fourth channel structure, wherein a top surface of the fourth channel structure is lower than a top surface of the second insulating connection layer. A top surface of the second filling structure is lower than the top surface of the second insulating connection layer.

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[0012] Forming the fifth channel structure includes etching the second insulating connection layer to form a second groove, forming a fifth channel layer in the second groove, wherein the fifth channel layer is in contact with the fourth channel structure, and planarizing the top surfaces of the second insulating connection layer and the fifth channel layer to form the fifth channel structure. A projection of the second groove on the substrate covers the projection of the second through hole on the substrate.

[0013] Another aspect of the present disclosure provides another method of forming a joint opening structure in a three-dimensional (3D) memory device. The method includes forming a first stacked layer and forming a first insulating connection layer on a substrate of the 3D memory device. The 3D memory device includes a first region for forming a plurality of channel holes, a second region for forming a plurality of staircase structure dummy holes, and a third region for forming a plurality of through array contact barriers. The method further includes forming a plurality of first through holes, each penetrating the first stacked layer and the first insulating connection layer in the first region, the second region, and the third region, forming a first channel structure overlaying the surface of the substrate in each first through hole, forming a first functional layer on the sidewall of each first through hole, forming a second channel structure and forming a first filling structure on the sidewall of the first functional layer and the exposed surface of the first channel structure in each first through hole, forming a third channel structure in contact with the second channel structure above each first through hole. A projection of the third channel structure on the substrate covers a projection of the corresponding first through hole on the substrate. The method further includes forming a second stacked layer on the first insulating connection layer, forming a second insulating connection layer on the second stacked layer, forming a plurality of second through holes, each penetrating the second stacked layer and the second insulating connection layer. A projection of each of the plurality of second through holes on the substrate at least partially overlaps with the projection of the corresponding first through hole on the substrate. The method further includes forming a second functional layer on the sidewall of each second through hole, forming a fourth channel structure and forming a second filling structure on the sidewall of the second functional layer and the exposed surface of the third channel structure in each second through hole in the first region, and forming a second filling structure on the sidewall of the second functional layer in each second through hole in the second region and the third region, and forming a fifth channel

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structure above each second through hole in the first region, the second region, and the third region. Each fifth channel structure is in contact with the corresponding fourth channel structure in each second through hole in the first region.

[0014] Forming the fourth channel structure and the second filling structure includes forming a fourth channel layer that covers the sidewall of the first passivation layer and the exposed surface of the third channel layer, forming a third filling layer that covers the surface of the fourth channel layer, forming a third mask layer that covers the third filling layer in the first region, and using the third mask layer as a mask to remove the third filling layer in the second region and the third region, removing the third mask layer;, using the third filling layer in the first region as a mask to remove the fourth channel layer in the second region and the third region, forming a fourth filling layer on the surface of the second functional layer in the second region and the third region, removing the third filling layer in the first region, forming a second filling layer in each second through hole in the first region, the second region, and the third region, removing a portion of the second filling layer to form the second filling structure in each second through hole, and removing a portion of the fourth channel layer to form the fourth channel structure in each second through hole. The top surface of the second filling structure is lower than the top surface of the second insulating connection layer, and the top surface of the fourth channel structure is lower than the top surface of the second insulating connection layer.

[0015] Another aspect of the present disclosure provides annother method of forming a joint opening structure in a three-dimensional (3D) memory device. The method includes forming a first stacked layer and forming a first insulating connection layer on a substrate, forming a first through hole that penetrates the first stacked layer and the first insulating connection layer, forming a first channel structure overlay the surface of the substrate that is exposed by the first through hole, forming a first functional layer on the sidewall of the first through hole, forming a second channel on the sidewall of the first functional layer and the exposed surface of the first channel structure, forming a third channel structure in contact with the second channel structure above the first through hole. A projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate. The method further includes forming a second stacked layer and forming a second insulating connection layer on the third channel structure, forming a second through hole that penetrates the second stacked layer and the second insulating connection layer. A projection of the second through hole on the substrate at least

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partially overlaps with the projection of the first through hole on the substrate. The method further includes forming a second functional layer on the sidewall of the second through hole, removing portions of the second functional layer and the third channel structure at the bottom of the second through hole to interconnect the second through hole and the first through hole to form a joint through hole, removing the remaining portion of the third channel structure and the second channel structure, forming a fourth channel structure in contact with the first channel structure on the sidewall of the joint through hole and the exposed surface of the first insulating connection layer, forming a first filling structure that covers the surface of the fourth channel structure, and forming a fifth channel structure in contact with the fourth channel structure above the joint through hole.

[0016] Another aspect of the present disclosure provides another method of forming a joint opening structure in a three-dimensional (3D) memory device. The method includes forming a first stacked layer and forming a first insulating connection layer on a substrate of the 3D memory device. The 3D memory device includes a first region for forming a plurality of channel holes, a second region for forming a plurality of staircase structure dummy holes, and a third region for forming a plurality of through array contact barriers. The method further includes forming a plurality of first through holes, each penetrating the first stacked layer and the first insulating connection layer in the first region, the second region, and the third region, forming a first channel structure on the surface of the substrate in each first through hole, forming a first functional layer on the sidewall of each first through hole, forming a second channel structure on the sidewall of the first functional layer and the exposed surface of the first channel structure in each first through hole, forming a third channel structure in contact with the second channel structure above each first through hole. A projection of the third channel structure on the substrate covers a projection of the corresponding first through hole on the substrate. The method further includes forming a second stacked layer and forming a second insulating connection layer on the plurality of third channel structures, forming a plurality of second through holes, each penetrating the second stacked layer and the second insulating connection layer. A projection of each of the plurality of second through holes on the substrate at least partially overlaps with the projection of the corresponding first through hole on the substrate. The method further includes forming a second functional layer on the sidewall of each second through hole, removing portions of the second functional layer and the third channel structure at the bottom of each second through hole to interconnect the

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second through hole and the corresponding first through hole to form a plurality of joint through holes, removing the remaining portions of the third channel structure and the second channel structure in each joint through hole, forming a fourth channel structure in contact with the first channel structure on the sidewall of each joint through hole and the exposed surfaces of the first insulating connection layer, forming a first filling structure that covers the surface of the fourth channel structure in each joint through hole, and forming a fifth channel structure above each joint through hole in the first region, the second region, and the third region. Each fifth channel structure is in contact with the corresponding fourth channel structure in each joint through hole in the first region.

[0017] Another aspect of the present disclosure provides a joint opening structure of a three-dimensional (3D) memory device, including a first stacked layer disposed overlaying a substrate, a first insulating connection layer disposed on the first stacked layer, a first through hole penetrating the first stacked layer and the first insulating connection layer, a first channel structure disposed at the bottom of the first through hole and overlaying the surface of the substrate, a first functional layer disposed on the sidewall of the first through hole, a second channel structure in contact with the first channel structure disposed on the sidewall of the first functional layer, a third channel structure in contact with the second channel structure disposed over the first through hole. A projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate. The joint opening structure further includes a second stacked layer disposed on the third channel structure, a second insulating connection layer disposed on the second stacked layer. A second through hole penetrating the second stacked layer and the second insulating connection layer. A projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate. The joint opening structure further includes a second functional layer disposed on the sidewall of the second through hole, a fourth channel structure in contact with the third channel structure disposed on the sidewall of the second functional layer, and a fifth channel structure in contact with the fourth channel structure disposed over the second through hole.

[0018] In some embodiments, a first filling structure covers the surface of the second channel structure, and a second filling structure covers the surface of the fourth channel structure. The first through hole is non-interconnected with the second through hole.

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[0019] In some other embodiments, a first filling structure covers the surfaces of the second channel structure and the fourth channel structure. The first through hole is interconnected with the second through hole.

[0020] In some embodiments, the first stacked layer includes a first number of conductor/dielectric layer pairs, and the second stacked layer includes a second number of conductor/dielectric layer pairs.

[0021] In some other embodiments, the first stacked layer includes a first number of oxide/nitride layer pairs, and the second stacked layer includes a second number of oxide/nitride layer pairs. The first number and the second number are not less than 32.

[0022] A thickness of the third channel structure is in a range between 30nm and 70nm. A size difference between a top aperture and a bottom aperture of the first through hole is equal to or less than 30nm. A size difference between a top aperture and a bottom aperture of the second through hole is equal to or less than 30nm.

[0023] Another aspect of the present disclosure provides a three-dimensional (3D) memory device, including a first stacked layer disposed on a substrate, a first insulating connection layer disposed on the first stacked layer, a second stacked layer disposed on the first insulating connection layer, a second insulating connection layer disposed on the second stacked layer, a plurality of channel holes in a first region of the 3D memory device, a plurality of staircase structure dummy holes in a second region of the 3D memory device, and a plurality of through array contact barriers in a third region of the 3D memory device. Each of the plurality of channel holes includes the disclosed joint opening structure.

[0024] Other aspects of the present disclosure can be understood by those skilled in the art in light of the description, the claims, and the drawings of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] Various objectives, features, and advantages of the present disclosure can be more fully appreciated with reference to the detailed description of the present disclosure when considered in contact with the following drawings, in which like reference numerals identify like elements. It is noted that the following drawings are merely examples for illustrative purposes according to various disclosed embodiments and are not intended to limit the scope of the present disclosure.

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[0026] FIGs. ~~1-22~~ 1-6, 7A, 7B, 8A, 8B, 9A, 9B, 10A, 10B, 11A, 11B, 12-20, 21A, 21B, 22A and 22B illustrate schematic structural cross-sectional diagrams of an exemplary joint opening structure of three-dimensional (3D) memory device at certain stages of a fabricating process in accordance with some embodiments of the present disclosure;

[0027] FIGs. 23A and 23B illustrate schematic flow diagrams of an exemplary fabricating process for forming a joint opening structure of three-dimensional (3D) memory device are illustrated in accordance with some embodiments of the present disclosure;

[0028] FIGs. ~~24-49~~24-29, 30A, 30B, 31A, 31B, 32A, 32B, 33A, 33B, 34A, 34B, 35-47, 48A, 48B, 49A and 49B illustrate schematic structural cross-sectional diagrams of another exemplary joint opening structure of three-dimensional (3D) memory device at certain stages of another fabricating process in accordance with some embodiments of the present disclosure;

[0029] FIGs. 50A and 50B illustrate schematic flow diagrams of another exemplary fabricating process for forming a joint opening structure of three-dimensional (3D) memory device are illustrated in accordance with some embodiments of the present disclosure;

[0030] FIGs. ~~51-73~~51-55, 56A, 56B, 57A, 57B, 58A, 58B, 59A, 59B, 60-71, 72A, 72B, 73A and 73B illustrate schematic structural cross-sectional diagrams of another exemplary joint opening structure of three-dimensional (3D) memory device at certain stages of another fabricating process in accordance with some embodiments of the present disclosure;

[0031] FIGs. 74A and 74B illustrate schematic flow diagrams of another exemplary fabricating process for forming a joint opening structure of three-dimensional (3D) memory device are illustrated in accordance with some embodiments of the present disclosure;

[0032] FIGs. ~~75-102~~75-79, 80A, 80B, 81A, 81B, 82A, 82B, 83A, 83B, 84-100, 101A, 101B, 102A and 102B illustrate schematic structural cross-sectional diagrams of another exemplary joint opening structure of three-dimensional (3D) memory device at certain stages of another fabricating process in accordance with some embodiments of the present disclosure;

[0033] FIGs. 103A and 103B illustrate schematic flow diagrams of another exemplary fabricating process for forming a joint opening structure of three-dimensional (3D)

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memory device are illustrated in accordance with some embodiments of the present disclosure.

[0034] Embodiments of the present disclosure will be described with reference to the accompanying drawings.

DETAILED DESCRIPTION

[0035] Reference now be made in detail to exemplary embodiments of the invention, which are illustrated in the accompanying drawings in order to understand and implement the present disclosure and to realize the technical effect. It can be understood that the following description has been made only by way of example, but not to limit the present disclosure. Various embodiments of the present disclosure and various features in the embodiments that are not conflicted with each other can be combined and rearranged in various ways. Without departing from the spirit and scope of the present disclosure, modifications, equivalents, or improvements to the present disclosure are understandable to those skilled in the art and are intended to be encompassed within the scope of the present disclosure.

[0036] It is noted that references in the specification to "one embodiment," "an embodiment," "an example embodiment," "some embodiments," etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in contact with an embodiment, it would be within the knowledge of a person skilled in the pertinent art to effect such feature, structure or characteristic in contact with other embodiments whether or not explicitly described.

[0037] In general, terminology may be understood at least in part from usage in context. For example, the term "one or more" as used herein, depending at least in part upon context, may be used to describe any feature, structure, or characteristic in a singular sense or may be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as "a," "an," or "the," again, may be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context.

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[0038] It should be readily understood that the meaning of "on," "above," and "over" in the present disclosure should be interpreted in the broadest manner such that "on" not only means "directly on" something but also includes the meaning of "on" something with an intermediate feature or a layer therebetween, and that "above" or "over" not only means the meaning of "above" or "over" something but can also include the meaning it is "above" or "over" something with no intermediate feature or layer therebetween (i.e., directly on something).

[0039] Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper," and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0040] As used herein, the term "substrate" refers to a material onto which subsequent material layers are added. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.

[0041] As used herein, the term "layer" refers to a material portion including a region with a thickness. A layer can extend over the entirety of an underlying or overlying structure, or may have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend horizontally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow. A layer can include multiple layers. For example, an interconnect layer can include one or more conductor and contact layers (in which contacts, interconnect lines, and/or through holes are formed) and one or more dielectric layers.

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[0042] As used herein, the term "nominal/nominally" refers to a desired, or target, value of a characteristic or parameter for a component or a process operation, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term "about" indicates the value of a given quantity that can vary based on a particular technology node associated with the subject semiconductor device. Based on the particular technology node, the term "about" can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., ±10%, ±20%, or ±30% of the value).

[0043] In accordance with some embodiments of the present disclosure, joint opening structures of three-dimensional (3D) memory devices and method for forming the same are provided to reduce the process difficulty and cost of the channel hole structures in 3D memory devices.

[0044] As used herein, the term "3D memory device" refers to a semiconductor device with vertically oriented strings of memory cell transistors (referred to herein as "memory strings," such as NAND strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate. As used herein, the term "vertical/vertically" means nominally perpendicular to the lateral surface of a substrate, while the term "horizontal/horizontally" means nominally parallel to the lateral surface of a substrate.

[0045] Referring to FIGs. 23A and 23B, schematic flow diagrams of an exemplary fabricating process for forming a joint opening structure of three-dimensional (3D) memory device are illustrated in accordance with some embodiments of the present disclosure. And FIGs. ~~1-22~~ 1-6, 7A, 7B, 8A, 8B, 9A, 9B, 10A, 10B, 11A, 11B, 12-20, 21A, 21B, 22A and 22B illustrate schematic structural cross-sectional diagrams of an exemplary joint opening structure of three-dimensional (3D) memory device at certain stages of the fabricating process shown in FIGs. 23A and 23B.

[0046] As shown in FIG. 23A, at S101, a first stacked layer 2 and a first insulating connection layer 3 can be sequentially formed on the surface of a substrate 1.

[0047] As shown in FIG. 1, the first stacked layer 2 can be formed on the substrate 1. The first stacked layer 2 can include a plurality of oxide/nitride layer pairs. The plurality of oxide/nitride layer pairs are also referred to herein as an "alternating oxide/nitride stack." That is, in the first stacked layer 2, multiple oxide layers (shown in the areas with

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dotes) and multiple nitride layers (shown in the areas with meshes) alternate in a vertical direction. In other words, except a top and a bottom layer of a given stack, each of the other oxide layers can be sandwiched by two adjacent nitride layers, and each nitride layer can be sandwiched by two adjacent oxide layers.

[0048] Oxide layers can each have the same thickness or have different thicknesses. For example, a thickness of each oxide layer can be in a range from 90nm to 160nm, preferably about 150nm. Similarly, nitride layers can each have the same thickness or have different thicknesses. For example, a thickness of each nitride layer can be in a range from 80nm to 110nm, preferably about 100nm.

[0049] It is noted that, in the present disclosure, the oxide layers and/or nitride layers can include any suitable oxide materials and/or nitride materials. For example, the element of the oxide materials and/or nitride materials can include, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof. In some embodiments, the oxide layers can be silicon oxide layers, and the nitride layers can be silicon nitride layer.

[0050] The first stacked layer 2 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide layers and the nitride layers in the first stacked layer 2 is equal to or larger than 64. In some embodiments, alternating conductor/dielectric stack includes more oxide layers or more nitride layers with different materials and/or thicknesses than the oxide/nitride layer pair.

[0051] The first insulating connection layer 3 can be formed on the first stacked layer 2. In some embodiments, the first insulating connection layer 3 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is noted that, the material of the first insulating connection layer 3 can be different from the material of the nitride layer in the first stacked layer 2.

[0052] Further, in some embodiments, a first mask layer 4 can be formed on the top surface of the first insulating connection layer 3. The first mask layer 4 can include a nitride layer on the top surface of the first insulating connection layer 3, and an oxide layer on the top surface of such nitride layer.

[0053] In some embodiments, the first stacked layer 2, the first insulating connection layer 3, and/or the first mask layer 4 can be formed by using one or more deposition processes. It is noted that, the term "deposition process" used in the present disclosure can be referred to any suitable deposition process including, but not limited to, a chemical

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vapor deposition (CVD) process, a physical vapor deposition (PVD) process, an atomic layer deposition (ALD) process, and/or any suitable combination thereof.

[0054] At S102, a first through hole 5 can be formed. As shown in FIG. 1, the first through hole 5 can completely penetrate the first stacked layer 2 and the first insulating connection layer 3, and can extend into the surface of the substrate 1.

[0055] In some embodiments, the first through hole 5 can be formed by etching the first stacked layer 2 and the first insulating connection layer 3 and a subsequent cleaning process. The etching process to form the first through hole 5 can be a wet etching, a dry etching, or a combination thereof.

[0056] In some embodiments, when the first mask layer 4 is formed on the top surface of the first insulating connection layer 3, the etching process also etch the first mask layer 4 to form the first through holes 5.

[0057] At S103, a first channel structure 6 can be formed on the surface of the substrate 1 that is exposed by the first through hole 5, as shown in FIG. 2. In some embodiments, the first channel structure 6 can be a polycrystalline silicon (polysilicon) layer formed by using a selective epitaxial process.

[0058] In some embodiments, the first channel structure 6 may not directly formed on the surface of the substrate 1. One or more layers can be formed between the first channel structure 6 and the substrate 1. That is, the first channel structure 6 is overlay the substrate 1.

[0059] At S104, a first functional layer can be formed on the sidewall of the first through hole 5. The first functional layer can include a first tunneling layer 7, a first storage layer 8, a first barrier layer 9, and a first passivation layer 10.

[0060] As shown in FIG. 3, the first tunneling layer 7 can be formed on the sidewall of the first through hole 5 and the top surface of the first channel structure 6. The first tunneling layer 7 can be used for generating electronic charges (electrons or holes). In some embodiments, the first tunneling layer 7 can be an oxide layer formed by using a deposition process.

[0061] The first storage layer 8 can be formed on the surface of the first tunneling layer 7. The first storage layer 8 can be used for storing electronic charges. The storage or removal of charge in the first storage layer 7 can impact the on/off state and/or a conductance of the semiconductor channel. The first storage layer 7 can include

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polycrystalline silicon (polysilicon) or silicon nitride. In some embodiments, the first storage layer 8 can be a nitride layer formed by using a deposition process.

[0062] The first barrier layer 9 can be formed on the surface of the first storage layer 8. The first barrier layer 9 can be used for blocking the outflow of the electronic charges stored in the first storage layer 8. In some embodiments, the first barrier layer 9 can be a silicon oxide layer or a combination of silicon oxide/silicon nitride/silicon oxide (ONO) layers. In some embodiments, the first barrier layer 9 includes high dielectric constant (high-k) dielectrics (e.g., aluminum oxide). In one example, the first barrier layer 9 is an oxide layer formed by using a deposition process.

[0063] As shown in FIG. 4, a first passivation layer 10 can be formed on the surface of the first barrier layer 9. The first passivation layer 10 can be used for protecting the first barrier layer 9 from being damaged in a subsequent removal process. In some embodiments, the first passivation layer 10 can be an amorphous silicon layer formed by using a deposition process.

[0064] The portions of the first passivation layer 10, the first barrier layer 9, the first storage layer 8 and the first tunneling layer 7 located on the top surface of the first channel structure 6 on the bottom of the first through hole 5 can be removed. In some embodiments, the removal process can include an etching process and a cleaning process. As such, the first functional layer can be formed on the sidewall of the first through hole 5.

[0065] In some embodiment, in the same removal process, the first barrier layer 9, the first storage layer 8, the first tunneling layer 7, and the oxide layer of the first mask layer 4 located on the surface of the nitride layer of first mask layer 4 can also be removed. As such, the nitride layer of first mask layer 4 is remained on the surface of the first insulating connection layer 3.

[0066] At S105, a second channel structure and a first filling structure can be sequentially formed on the sidewall of the first functional layer and the exposed surface of the first channel structure 6. The surfaces of the second channel structure and the first filling structure can be lower than the surface of the first insulating connection layer 3.

[0067] As shown in FIG. 5, a second channel layer 11 can be formed to cover the sidewall of the first passivation layer 10, the bottom surface of the first through hole 5. The second channel layer 11 can also cover the top surface of the first insulating connection layer 3, or cover the top surface of the nitride layer of the first mask layer 4.

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In some embodiments, the second channel layer 11 can be an amorphous silicon layer formed by using a deposition process.

[0068] As shown in FIG. 6, a first filling layer 12 can be formed to cover the second channel layer 11 and fill the first through hole 5. In some embodiments, the first filling layer 12 can be an oxide layer formed by using a deposition process. In some embodiments, the first filling layer 12 can include one or more airgaps.

[0069] As shown in FIGs. 7A and 7B, a portion of the first filling layer 12 can be removed, so that the top surface of the first filling layer 12 can be lower than the top surface of the first insulating connection layer 3. As such, the remaining portion of the first filling layer 12 in the first through hole 5 can form the first filling structure. In some embodiments, the portion of the first filling layer 12 can be removed by using an etching process. It is noted that, the term "etching process" used in the present disclosure can be referred to any suitable etching process including, but not limit to, a wet etching, a dry etching, or a combination thereof.

[0070] In some embodiments, as shown in FIG. 7A, the top surface of the first filling layer 12 can be higher than the top surface of the second stacker layer 2. For example, the top surface of the first filling layer 12 can be 20nm to 40nm higher than the top surface of the top nitride layer of the second stacker layer 2. Preferably, the top surface of the first filling layer 12 can be about 30nm higher than the top surface of the top nitride layer of the second stacker layer 2.

[0071] In some alternative embodiments, as shown in FIG. 7B, the top surface of the first filling layer 12 can be lower than the top surface of the second stacker layer 2. For example, the top surface of the first filling layer 12 can be 30nm to 40nm lower than the top surface of the top nitride layer of the second stacker layer 2. Preferably, the top surface of the first filling layer 12 can be about 35nm lower than the top surface of the top nitride layer of the second stacker layer 2.

[0072] As shown in FIGs. 8A and 8B, a portion of the second channel layer 11 can be removed, such that the surface of the second channel layer 11 is lower than the first insulating connection layer 3. The remaining portion of the second channel layer 11 can form the second channel structure that is in contact with the first channel structure 6. In some embodiments, the portion of the second channel layer 11 can be removed by using an etching process.

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[0073] It is noted that, in various embodiments, the top surface of the second channel structure can be higher or lower than the top surface of the first stacked layer 2. However, the top surface of the second channel structure is not lower than the top surface of the top oxide layer in the first stacked layer 2. In some embodiments, the top surface of the second channel structure can be higher than the top nitride layer in the first stacked layer 2, as shown in FIG. 8A. In some alternative embodiments, the top surface of the second channel structure is in a same plane of the top surface of the top oxide layer in the first stacked layer 2, as shown in FIG. 8B.

[0074] At S106, a first groove can be formed in the first insulating connection layer 3. In some embodiments, the projection of the first groove on the substrate 1 can completely cover the projection of the first through hole 5 on the substrate 1.

[0075] As shown in FIGs. 9A and 9B, the nitride layer of the first mask layer 4 can be removed. In some embodiments, the nitride layer of the first mask layer 4 can be removed by using an etching process.

[0076] As shown in FIGs. 10A and 10 B, the surface of the first insulating connection layer 3 can be planarized by using any suitable techniques, such as backside grinding, and/or chemical mechanical polishing (CMP). A portion of the first insulating connection layer 3 can be removed to form the first groove that penetrates the first insulating connection layer 3. An area of the projection "x" of the first groove on the substrate 1 can be larger than an area of the projection "y" of the first through hole 5 on the substrate 1.

[0077] In some embodiments, a depth of the first groove can be equal to or less than the thickness of the planarized first insulating connection layer 3, as shown in FIG. 10A. For example, the depth of the first groove can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 3 is about 90nm, while the depth of the first groove is about 60nm.

[0078] In some alternative embodiments, the depth of the first groove can be greater than the thickness of the planarized first insulating connection layer 3, as shown in FIG. 10B. That is, a portion of the top nitride layer in the first stacked layer 2 can also be removed to form the first groove. For example, the depth of the first groove can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 3 is about 30nm, while the depth of the first groove is about 60nm.

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[0079] At S107, a third channel structure 14 can be formed in the first groove 13. As shown in FIGs. 11A and 11B, the third channel structure 14 can be in contact with the second channel structure. In some embodiments, the third channel structure can be a polycrystalline silicon player formed by using a deposition process.

[0080] A thickness of the third channel structure 14 can be equal to the depth of the first groove 13. As described above, in some embodiments, a thickness of the third channel structure 14 can be equal to or less than the thickness of the planarized first insulating connection layer 3, as shown in FIG. 11A. For example, the thickness of the third channel structure 14 can be in a range between 50nm and 70nm, preferably about 60nm. In some alternative embodiments, the thickness of the third channel structure 14 can be greater than the thickness of the planarized first insulating connection layer 3, as shown in FIG. 11B. For example, the thickness of the third channel structure 14 can be in a range between 60nm and 80nm, preferably about 70nm.

[0081] Referring to FIG. 23B, at S108, a second stacked layer 15 and a second insulating connection layer 16 can be sequentially formed on the third channel structure 14. As shown in FIG. 12, the second stacked layer 15 can include a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs. Similar to the first stacked layer 2 as described above, the multiple oxide layers (shown in the areas with dotes) and multiple nitride layers (shown in the areas with meshes) in the second stacked layer 15 alternate in a vertical direction. The second stacked layer 15 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide layers and the nitride layers in the second stacked layer 15 is equal to or larger than 64.

[0082] In some embodiments, the second insulating connection layer 16 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is noted that, the material of the second insulating connection layer 16 can be different from the material of the nitride layer in the second stacked layer 15.

[0083] Further, in some embodiments, a second mask layer 17 can be formed on the surface of the second insulating connection layer 16. The second mask layer 17 can include a nitride layer on the surface of the second insulating connection layer 16, and an oxide layer on the surface of such nitride layer.

[0084] At S109, a second through hole 18 is formed. As shown in FIG. 13, the second through hole 18 can completely penetrate the second stacked layer 15 and the second

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insulating connection layer 16, and can extend into the surface of the third channel structure 14. The projection of the second through hole 18 on the substrate 1 can at least partially overlap with the projection of the first through hole 5 on the substrate 1.

[0085] In some embodiments, the second stacked layer 15, the second insulating connection layer 16, the second mask layer 17, and the third channel structure 14 can be etched to form the second through hole 18. The second stacked layer 15, the second insulating connection layer 16, the second mask layer 17, and/or the third channel structure 14 can be etched by using a dry etching process, a wet etching process, or a combination thereof. A cleaning process can then be performed to clean the second through hole 18.

[0086] It is noted that, the second through hole 18 can extend to the surface of the third channel structure 14, or can extend into the third channel structure 14. As such, a fourth channel structure formed subsequently in the second through hole 18 can directly contact the third channel structure.

[0087] In some embodiments, a maximum difference between the radius of the top aperture of each second through hole 18 and the radius of the bottom aperture of the second through hole 18 can be 15nm. That is, as shown in FIG. 13, a distance "a" between the boundary line of the top surface of each second through hole 18 and the boundary of the bottom surface of the second through hole 18 can be no more than 15 nm.

[0088] At S1010, a second functional layer can be formed on the sidewall of the second through hole 18. In some embodiments, the second functional layer can include a second tunneling layer 19, a second storage layer 20, a second barrier layer 21, and a second passivation layer 22.

[0089] As shown in FIG. 14, the second tunneling layer 19 can be formed on the sidewall of the second through hole 18 and the surface of the second channel structure 14. The second tunneling layer 19 can be used for generating electronic charges. In some embodiments, the second tunneling layer 19 can be an oxide layer formed by using a deposition process.

[0090] The second storage layer 20 can be formed on the surface of the second tunneling layer 19. The second storage layer 20 can be used for storing electronic charges. In some embodiments, the second storage layer 20 can be a nitride layer formed by using a deposition process.

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[0091] The second barrier layer 21 can be formed on the surface of the second storage layer 20. The second barrier layer 21 can be used for blocking the outflow of the electronic charges in the second storage layer 20. In some embodiments, the second barrier layer 21 can be an oxide layer formed by using a deposition process.

[0092] As shown in FIG. 15, a second passivation layer 22 can be formed on the surface of the second barrier layer 21. The second passivation layer 22 can be used for protecting the second barrier layer 21 from being damaged in a subsequent removal process. In some embodiments, the second passivation layer 22 can be an amorphous silicon layer formed by using a deposition process.

[0093] As shown in FIG. 15, the portions of the second passivation layer 22, the second barrier layer 21, the second storage layer 20 and the second tunneling layer 19 that are located on the surface of the second channel structure 14 can be removed. In some embodiments, the removal process can include an etching process and a cleaning process. In some embodiments, the portions of the second passivation layer 22, the second barrier layer 21, the second storage layer 20, the second tunneling layer 19, the oxide layer of the second mask layer 17 that are located on the nitride layer of the second mask layer 17 can also be removed by using an etching process. As such, the second functional layer can be formed on the sidewall of the second through hole 18.

[0094] At S1012, a fourth channel structure and a second filling structure can be sequentially formed on the sidewall of the second functional layer and the exposed surface of the third channel structure. In some embodiments, the top surface of the fourth channel structure can be higher than the top surface of the second filling structure.

[0095] As shown in FIG. 16, a fourth channel layer 23 can be formed to cover the sidewall of the second passivation layer 22 and the bottom surface of the second through hole 18. In some embodiments, the fourth channel layer 23 can also cover the surface of the second insulating connection layer 16, or the surface of the nitride layer of the second mask layer 17. In some embodiments, the fourth channel layer 23 can be an amorphous silicon layer formed by using a deposition process.

[0096] As shown in FIG. 17, a second filling layer 29 can be formed to cover the fourth channel layer 23 and to fill the second through hole 18. In some embodiments, the second filling layer 29 can be an oxide layer formed by using a deposition process.

[0097] As shown in FIG. 18, a portion of the second filling layer 29 can be removed, such that the surface of the second filling layer 29 is lower than the surface of the second

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insulating connection layer 16. In some embodiments, the removal process can include an etching process. The remaining portion of the second filling layer 29 in the second through hole 18 can form the second filling structure.

[0098] As shown in FIG. 19, the portion of the fourth channel layer 23 located on the surface of the second insulating connection layer 16 or the surface of the second mask layer 17 can be removed. In some embodiments, the removal process can include an etching process. The remaining portion of the fourth channel layer 23 in the second through hole 18 can form the fourth channel structure. The top surface of the fourth channel structure can be higher than the top surface of the second filling structure. As such, a second groove can be formed on the fourth channel structure and the second filling structure, and in the second through hole 18.

[0099] It is noted that, the top surface of the fourth channel structure can be higher than the top surface of the second stacked layer 15, or can be lower than the top surface of the second stacked layer 15. The top surface of the fourth channel structure is not lower than the top surface of the top oxide layer in the second stacked layer 15. In some embodiments, the top surface of the fourth channel structure can be in a same plane of the top surface of the top oxide layer in the second stacked layer 15.

[00100] At S1013, a fifth channel structure can be formed in the second groove. The fifth channel structure can be in contact with the fourth channel structure. As shown in FIG. 20, the fifth channel structure 30 can be formed in the second groove that is on the fourth channel structure and the second filling structure and in the second through hole 18. The nitride layer of the second mask layer 17 can be then removed by an etching process.

[00101] As shown in FIGs. 21A and 21B, the top surface of the second insulating connection layer 16 and the top surface of the fifth channel structure 30 can be planarized by any suitable techniques, such as backside grinding, and/or chemical mechanical polishing (CMP).

[00102] Accordingly, the disclosed method as shown in FIGs. 23A and 23B can form a joint opening structure of a three-dimensional (3D) memory device by combining two through hole formation processes. As such, the formed channel hole having the joint opening structure can have a large aspect ratio and a limited top-bottom aperture error. Further, the disclosed method of forming a joint opening structure in a 3D memory device can result in an efficient process capability control, a simplified process complexity, and a reduced cost.

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[00103] In some embodiments, the present disclosure also provides a three-dimensional memory device formed by using the above disclosed method as shown in FIGs. 23A and 23B. The three-dimensional memory can include the following components described below.

[00104] A first stacked layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer silicon nitride layer pairs, is formed on a substrate. A first insulating connection layer is formed on the first stacked layer. A first through hole penetrates the first stacked layer and the first insulating connection layer, and extends into the surface of the substrate.

[00105] A first channel structure is formed on the surface of the substrate exposed by the first through hole. A first functional layer is formed on the sidewall of the first through hole. A second channel structure is formed on the sidewall of the first functional layer and the surface of the first channel structure. A first filling structure is formed on the sidewall and the surface of the second channel structure to fill the first through hole. In some embodiments, an airgap is enclosed in the first filling structure. The top surfaces of the second channel structure and the first filling structure are lower than the top surfaces of the first insulating connection layer.

[00106] A first groove is formed in the first insulating connection layer, and above the first functional layer, the second channel structure and the first filling structure. A projection of the first groove on the substrate completely covers a projection of the first through hole on the substrate. A third channel structure in contact with the second channel structure is formed in the first groove.

[00107] A second stack layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs, is formed on the top surfaces of the first insulating connection layer and the third channel structure. A second insulating connection layer is formed on the second stack layer. A second through hole penetrates through the second stacked layer and the second insulating connection layer, and extends into a surface of the third channel structure. A projection of the second through hole on the substrate at least partially overlaps the projection of the first through hole on the substrate.

[00108] A second functional layer is formed on the sidewall of the second through hole. A fourth channel structure is formed on the sidewall of the second functional layer and the bottom surface of the second through hole. A second filling structure is formed on the

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sidewall and the surface of the fourth channel structure to fill the second through hole. In some embodiments, an airgap is enclosed in the second filling structure. The top surface of the fourth channel structure is higher than the top surface of the second filling structure. A fifth channel structure in contact with the fourth channel structure is formed in a second groove that is surrounded by the second functional layer, and above the fourth channel structure and the second filling structure.

[00109] In some embodiments, as shown in FIG. 21A, a thickness "b" of the first insulating connection layer, which is the distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 80nm and 100nm, preferably about 90nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00110] In some alternative embodiments, as shown in FIG. 21B, a thickness "b" of the first insulating connection layer, which is the distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 20nm and 40nm, preferably about 30nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00111] Further, the difference between the radiuses of the top aperture and the bottom aperture of the second channel structure, and the difference between the radiuses of the top aperture and the bottom aperture of the fourth channel structure can be within 15nm. Accordingly, the disclosed channel hole having a joint opening structure can have a large aspect ratio and a limited top-bottom aperture error.

[00112] In some embodiments, a replacement process can be performed to replace each of the plurality of nitride layers in the first stacked layer 2 and the second stacked layer 15 with a conductive layer 40, as shown in FIGs. 22A and 22B. The conductive layer can include any suitable material that is electronically conductive, including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof.

[00113] In some embodiments, during the replacement process, a portion of the third channel structure 14 that is adjacent with the bottom nitride layer of the second stacked layer 15, or is adjacent with the top nitride layer of the first stacked layer 2 can be converted to an oxide layer by an oxidation process. For example, an etching process can be performed to remove all nitride layers in the first stacked layer 2 and the second stacked layer 15. Then an oxide process can be formed to oxide the exposed surface of the third channel structure. As a result, a portion of the third channel structure can be

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converter to the oxide layer as shown in FIGs. 22A and 22B. In some embodiments,, a thickness "c" of the third channel structure can be reduced after the replacement process. For example, the thickness "c" of the third channel structure can be reduced to a range between 30nm and 50nm, preferably about 40nm.

[00114] Referring to FIGs. 50A and 50B, schematic flow diagrams of another exemplary fabricating process for forming a joint opening structure of three-dimensional (3D) memory device are illustrated in accordance with some other embodiments of the present disclosure. And FIGs. 24-29, 30A, 30B, 31A, 31B, 32A, 32B, 33A, 33B, 34A, 34B, 35-47, 48A, 48B, 49A and 49B~~24-49~~ illustrate schematic structural cross-sectional diagrams of an exemplary joint opening structure of three-dimensional (3D) memory device at certain stages of the fabricating process shown in FIGs. 50A and 50B.

[00115] As shown in FIG. 50A, at S201, a first stacked layer 202 and a first insulating connection layer 203 can be sequentially formed on the surface of a substrate 201. In some embodiments, the 3D memory device can include a first region 100, a second region 200, and a third region 300, as shown in FIG. 24. The first region 100 can be used to form one or more channel holes, the second region 200 can be used to form one or more staircase structure (SS) dummy holes, while the third region 300 can be used to form one or more through array contact (TAC) barriers.

[00116] As shown in FIG. 24, the first stacked layer 202 can be formed on the substrate 201. The first stacked layer 202 can include a plurality of oxide/nitride layer pairs. That is, in the first stacked layer 202, multiple oxide layers (shown in the areas with dotes) and multiple nitride layers (shown in the areas with meshes) alternate in a vertical direction. In other words, except a top and a bottom layer of a given stack, each of the other oxide layers can be sandwiched by two adjacent nitride layers, and each nitride layer can be sandwiched by two adjacent oxide layers.

[00117] Oxide layers can each have the same thickness or have different thicknesses. For example, a thickness of each oxide layer can be in a range from 90nm to 160nm, preferably about 150nm. Similarly, nitride layers can each have the same thickness or have different thicknesses. For example, a thickness of each nitride layer can be in a range from 80nm to 110nm, preferably about 100nm. In some embodiments, the oxide layers can be silicon oxide layers, and the nitride layers can be silicon nitride layer.

[00118] The first stacked layer 202 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide

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layers and the nitride layers in the first stacked layer 202 is equal to or larger than 64. In some embodiments, alternating conductor/dielectric stack includes more oxide layers or more nitride layers with different materials and/or thicknesses than the oxide/nitride layer pair.

[00119] The first insulating connection layer 203 can be formed on the first stacked layer 202. In some embodiments, the first insulating connection layer 203 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is noted that, the material of the first insulating connection layer 203 can be different from the material of the nitride layer in the first stacked layer 202.

[00120] Further, in some embodiments, a first mask layer 204 can be formed on the surface of the first insulating connection layer 203. The first mask layer 204 can include a nitride layer on the surface of the first insulating connection layer 203, and an oxide layer on the surface of such nitride layer.

[00121] In some embodiments, the first stacked layer 202, the first insulating connection layer 203, and/or the first mask layer 204 can be formed by using one or more deposition processes, such as one or more chemical vapor deposition (CVD) processes, one or more physical vapor deposition (PVD) processes, one or more atomic layer deposition (ALD) processes, and/or any suitable combinations thereof.

[00122] At S202, one or more first through holes 205 can be formed in each of the first region 100, the second region 200, and the third region 300. As shown in FIG. 24, each of the one or more first through holes 205 can completely penetrate the first stacked layer 202 and the first insulating connection layer 203, and can extend into the surface of the substrate 201. In some embodiments, when the first mask layer 204 is formed on the surface of the first insulating connection layer 203, the etching process also etch the first mask layer 204 to form the first through holes 205.

[00123] In some embodiments, the first through holes 205 can be formed by etching the first stacked layer 202 and the first insulating connection layer 203 and a subsequent cleaning process. The etching process to form the first through holes 205 can be a wet etching, a dry etching, or a combination thereof. It is noted that, in the direction perpendicular to the surface of the substrate 201, the depth of the one or more first through holes 205 in the third region 300 can be larger than the depth of the one or more first through holes 205 in the first region 100.

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[00124] At S203, a first channel structure 206 can be formed on the surface of the substrate 201 that is exposed by each of the plurality of first through holes 205, as shown in FIG. 25. In some embodiments, the first channel structure 206 can be a polycrystalline silicon (polysilicon) layer formed by using a selective epitaxial process.

[00125] At S204, a first functional layer can be formed on the sidewall of each of the plurality of first through holes 205. The first functional layer can include a first tunneling layer 207, a first storage layer 208, a first barrier layer 209, and a first passivation layer 210.

[00126] As shown in FIG. 26, the first tunneling layer 207 can be formed on the sidewall of the plurality of first through holes 205 and the exposed surfaces of the first channel structures 206. The first tunneling layer 207 can be used for generating electronic charges (electrons or holes). In some embodiments, the first tunneling layer 207 can be an oxide layer formed by using a deposition process.

[00127] The first storage layer 208 can be formed on the surface of the first tunneling layer 207. The first storage layer 208 can be used for storing electronic charges. The storage or removal of charge in the first storage layer 207 can impact the on/off state and/or a conductance of the semiconductor channel. The first storage layer 207 can include polycrystalline silicon (polysilicon) or silicon nitride. In some embodiments, the first storage layer 208 can be a nitride layer formed by using a deposition process.

[00128] The first barrier layer 209 can be formed on the surface of the first storage layer 208. The first barrier layer 209 can be used for blocking the outflow of the electronic charges stored in the first storage layer 208. In some embodiments, the first barrier layer 209 can be a silicon oxide layer or a combination of silicon oxide/silicon nitride/silicon oxide (ONO) layers. In some embodiments, the first barrier layer 209 includes high dielectric constant (high-k) dielectrics (e.g., aluminum oxide). In one example, the first barrier layer 209 is an oxide layer formed by using a deposition process.

[00129] As shown in FIG. 27, a first passivation layer 210 can be formed on the surface of the first barrier layer 209. The first passivation layer 210 can be used for protecting the first barrier layer 209 from being damaged in a subsequent removal process. In some embodiments, the first passivation layer 210 can be an amorphous silicon layer formed by using a deposition process.

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[00130] The portions of the first passivation layer 210, the first barrier layer 209, the first storage layer 208 and the first tunneling layer 207 located on the surfaces of the plurality of first channel structures 206 on the bottom of the plurality of first through holes 205 can be removed. In some embodiments, the removal process can include an etching process and a cleaning process. As such, the first functional layer can be formed on the sidewalls of the plurality of first through holes 205.

[00131] In some embodiment, in the same removal process, the first barrier layer 209, the first storage layer 208, the first tunneling layer 207, and the oxide layer of the first mask layer 204 located on the surface of the nitride layer of first mask layer 204 can also be removed. As such, the nitride layer of first mask layer 204 is remained on the surface of the first insulating connection layer 203.

[00132] At S205, a second channel structure and a first filling structure can be sequentially formed on the sidewall of the first functional layer and the exposed surface of the first channel structure 206 in each of the plurality of first through holes 205. The surfaces of the second channel structure and the first filling structure can be lower than the surface of the first insulating connection layer 203.

[00133] As shown in FIG. 28, a second channel layer 211 can be formed to cover the sidewalls of the first passivation layer 210 and the bottom of each of the plurality of first through holes 205. The second channel layer 211 can also cover the surface of the first insulating connection layer 203, or cover the surface of the nitride layer of the first mask layer 204. In some embodiments, the second channel layer 211 can be an amorphous silicon layer formed by using a deposition process.

[00134] As shown in FIG. 29, a first filling layer 212 can be formed to cover the second channel layer 211 and fill each of the plurality of first through holes 205. In some embodiments, the first filling layer 212 can be an oxide layer formed by using a deposition process.

[00135] As shown in FIGs. 30A and 30B, a portion of the first filling layer 212 can be removed, such that the top surface of the first filling layer 212 can be lower than the top surface of the first insulating connection layer 203. As such, the remaining portion of the first filling layer 212 in each of the plurality of first through holes 205 can form the first filling structure. In some embodiments, the portion of the first filling layer 212 can be removed by using an etching process, such as a wet etching, a dry etching, or a combination thereof.

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[00136] In some embodiments, as shown in FIG. 30A, the top surface of the first filling layer 212 can be higher than the top surface of the second stacker layer 202. For example, the top surface of the first filling layer 212 can be 20nm to 40nm higher than the top surface of the top nitride layer of the second stacker layer 202. Preferably, the top surface of the first filling layer 212 can be about 30nm higher than the top surface of the top nitride layer of the second stacker layer 202.

[00137] In some alternative embodiments, as shown in FIG. 30B, the top surface of the first filling layer 212 can be lower than the top surface of the second stacker layer 202. For example, the top surface of the first filling layer 212 can be 30nm to 40nm lower than the top surface of the top nitride layer of the second stacker layer 202. Preferably, the top surface of the first filling layer 212 can be about 35nm lower than the top surface of the top nitride layer of the second stacker layer 202.

[00138] As shown in FIGs. 31A and 31B, a portion of the second channel layer 211 can be removed, such that the surface of the second channel layer 211 is lower than the first insulating connection layer 203. The remaining portion of the second channel layer 211 can form the second channel structure that is in contact with the first channel structure 206. In some embodiments, the portion of the second channel layer 211 can be removed by using an etching process.

[00139] It is noted that, in various embodiments, the top surface of the second channel structure can be higher than the top surface of the first stacked layer 202 or lower than the top surface of the first stacked layer 202. However, the top surface of the second channel structure is not lower than the top surface of the top oxide layer in the first stacked layer 202. In some embodiments, the top surface of the second channel structure can be higher than the top nitride layer in the first stacked layer 202, as shown in FIG. 31A. In some alternative embodiments, the top surface of the second channel structure is in a same plane of the top surface of the top oxide layer in the first stacked layer 202, as shown in FIG. 31B.

[00140] At S206, a first groove can be formed in the first insulating connection layer 203 above each of the plurality of first through holes 205. In some embodiments, the projection of the first groove on the substrate 201 can completely cover the projection of the corresponding first through hole 205 on the substrate 201.

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[00141] As shown in FIGs. 32A and 32B, the nitride layer of the first mask layer 204 can be removed. In some embodiments, the nitride layer of the first mask layer 204 can be removed by using an etching process.

[00142] As shown in FIGs. 33A and 33 B, the surface of the first insulating connection layer 203 can be planarized by any suitable techniques, such as backside grinding, and/or chemical mechanical polishing (CMP). A portion of the first insulating connection layer 203 can be removed to form a plurality of first grooves that penetrate the first insulating connection layer 203. An area of the projection of each of the plurality of first grooves on the substrate 201 can be larger than an area of the projection of each of the plurality of first through holes 205 on the substrate 201.

[00143] In some embodiments, a depth of the first groove can be equal to or less than the thickness of the planarized first insulating connection layer 203, as shown in FIG. 33A. For example, the depth of the first groove can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 203 is about 90nm, while the depth of the first groove is about 60nm.

[00144] In some alternative embodiments, the depth of the first groove can be greater than the thickness of the planarized first insulating connection layer 203, as shown in FIG. 33B. That is, a portion of the top nitride layer in the first stacked layer 202 can also be removed to form the first groove. For example, the depth of the first groove can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 203 is about 30nm, while the depth of the first groove is about 60nm.

[00145] At S207, a third channel structure 214 can be formed in each of the plurality of first grooves 213. As shown in FIGs. 34A and 34B, the third channel structure 214 can be in contact with the second channel structure in each of the plurality of first through holes 205. In some embodiments, the third channel structure can be a polycrystalline silicon player formed by using a deposition process.

[00146] A thickness of each third channel structure 214 can be equal to the depth of each first groove 213. As described above, in some embodiments, a thickness of each third channel structure 214 can be equal to or less than the thickness of the planarized first insulating connection layer 203, as shown in FIG. 34A. For example, the thickness of each third channel structure 214 can be in a range between 50nm and 70nm, preferably about 60nm. In some alternative embodiments, the thickness of each third channel

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structure 214 can be greater than the thickness of the planarized first insulating connection layer 203, as shown in FIG. 34B. For example, the thickness of each third channel structure 214 can be in a range between 60nm and 80nm, preferably about 70nm.

[00147] Referring to FIG. 50B, at S208, a second stacked layer 215 and a second insulating connection layer 216 can be sequentially formed on the plurality of third channel structures 214. As shown in FIG. 35, the second stacked layer 215 can include a plurality of oxide/nitride layer pairs, such as silicon oxide layers and silicon nitride layers. Similar to the first stacked layer 202 as described above, the multiple oxide layers (shown in the areas with dotes) and multiple nitride layers (shown in the areas with meshes) in the second stacked layer 215 alternate in a vertical direction. The second stacked layer 215 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide layers and the nitride layers in the second stacked layer 215 is equal to or larger than 64.

[00148] In some embodiments, the second insulating connection layer 216 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is noted that, the material of the second insulating connection layer 216 can be different from the material of the nitride layer in the second stacked layer 215.

[00149] Further, in some embodiments, a second mask layer 217 can be formed on the surface of the second insulating connection layer 216. The second mask layer 217 can include a nitride layer on the surface of the second insulating connection layer 216, and an oxide layer on the surface of such nitride layer.

[00150] At S209, one or more second through holes 218 are formed in each of the first region 100, the second region 200, and the third region 300. As shown in FIG. 36, each of the plurality of second through holes 218 can completely penetrate the second stacked layer 215, the second insulating connection layer 216, and the second mask layer 217, and can extend into the surface of the corresponding third channel structure 214. The projection of each second through hole 218 on the substrate 201 can at least partially overlap with the projection of the corresponding first through hole 205 on the substrate 201.

[00151] In some embodiments, the second stacked layer 215, the second insulating connection layer 216, the second mask layer 217, and the third channel structures 214 can be etched to form the plurality of second through holes 218 that penetrate the second stacked layer 215 and the second insulating connection layer 216. The second stacked

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layer 215, the second insulating connection layer 216, the second mask layer 217, and/or the third channel structure 214 can be etched by using a dry etching process, a wet etching process, or a combination thereof. A cleaning process can then be performed to clean the plurality of second through holes 218.

[00152] It is noted that, each second through hole 218 can extend to the surface of the corresponding third channel structure 214, or can extend into the corresponding third channel structure 214. As such, a fourth channel structure formed subsequently in each second through hole 218 can directly contact the corresponding third channel structure. It is also noted that, the one or more second through holes 218 in the third region 300 can also completely penetrate the corresponding third channel structures 214, as shown in FIG. 36. However, the one or more third channel structures 214 in the first region 100 are not completely penetrated by the one or more second through holes 218.

[00153] In some embodiments, a maximum difference between the radius of the top aperture of each second through hole 218 and the radius of the bottom aperture of the second through hole 218 can be 15nm. That is, as shown in FIG. 36, a distance "a" between the boundary line of the top surface of each second through hole 218 and the boundary of the bottom surface of the second through hole 218 can be no more than 15 nm.

[00154] At S2010, a second functional layer can be formed on the sidewall of each second through hole 218. In some embodiments, the second functional layer can include a second tunneling layer 219, a second storage layer 220, a second barrier layer 221, and a second passivation layer 222.

[00155] As shown in FIG. 37, the second tunneling layer 219 can be formed on the sidewall of each second through hole 218 and the surface of the corresponding third channel structure 214. The second tunneling layer 219 can be used for generating electronic charges. In some embodiments, the second tunneling layer 219 can be an oxide layer formed by using a deposition process.

[00156] The second storage layer 220 can be formed on the surface of the second tunneling layer 219. The second storage layer 220 can be used for storing electronic charges. In some embodiments, the second storage layer 220 can be a nitride layer formed by using a deposition process.

[00157] The second barrier layer 221 can be formed on the surface of the second storage layer 220. The second barrier layer 221 can be used for blocking the outflow of the

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electronic charges in the second storage layer 220. In some embodiments, the second barrier layer 221 can be an oxide layer formed by using a deposition process.

[00158] As shown in FIG. 38, a second passivation layer 222 can be formed on the surface of the second barrier layer 221. The second passivation layer 222 can be used for protecting the second barrier layer 221 from being damaged in a subsequent removal process. In some embodiments, the second passivation layer 222 can be an amorphous silicon layer formed by using a deposition process.

[00159] As shown in FIG. 38, the portions of the second passivation layer 222, the second barrier layer 221, the second storage layer 220 and the second tunneling layer 219 that are located on the surface of each third channel structure 214 can be removed. In some embodiments, the removal process can include an etching process and a cleaning process. In some embodiments, the portions of the second passivation layer 222, the second barrier layer 221, the second storage layer 220, the second tunneling layer 219, the oxide layer of the second mask layer 217 that are located on the nitride layer of the second mask layer 217 can also be removed by using an etching process. As such, the second functional layer can be formed on the sidewall of each second through hole 218.

[00160] At S2011, a fourth channel structure can be formed on the sidewall of the second functional layer and the exposed surface of the third channel structure in each second through hole 218 in the first region 100. Further, a second filling structure can be formed in each of the plurality of second through holes 218 in the first region 100, the second region 200, and the third region 300. In some embodiments, the top surface of the fourth channel structure can be higher than the top surface of the second filling structure.

[00161] As shown in FIG. 39, a fourth channel layer 223 can be formed to cover the sidewall of the second passivation layer 222 and the bottom surface of each of the plurality of second through holes 218 in the first region 100, the second region 200, and the third region 300. In some embodiments, the fourth channel layer 223 can also cover the top surface of the second insulating connection layer 216, or the top surface of the nitride layer of the second mask layer 217. In some embodiments, the fourth channel layer 223 can be an amorphous silicon layer formed by using a deposition process.

[00162] As shown in FIG. 40, a third filling layer 224 can be formed to cover the fourth channel layer 223. In some embodiments, the third filling layer 224 can include one or more airgaps in each second through hole 218. In some embodiments, the third filling layer 224 can be an oxide layer formed by using a deposition process.

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[00163] As shown in FIG. 41, a third mask layer 25 can be formed on the top surface of the third filling layer 224 in the first region 100. Using the third mask layer 225 as a mask, the portions of the third filling layer 224 located in the second region 200 and the third region 300 can be removed by using an etching process.

[00164] As shown in FIG. 42, the third mask layer 225 can be removed. Using the remaining third filling layer 224 in the first region 100 as a mask, the fourth channel layer 223 located in the second region 200 and the third region 300 can be removed by using an etching process.

[00165] As shown in FIG. 43, a fourth filling layer 227 can be formed on the surface of the second functional layer located in the second region 200 and the third region 300. In some embodiments, the filling performance of the fourth filling layer 227 can be better than the filling performance of the third filling layer 224. That is, in a same removing process, the removal rate of the fourth filling layer 227 can be less than the removal rate of the third filling layer 224.

[00166] As shown in FIG. 44, the third filling layer 224 on the surface of the fourth channel layer 223 in the first region 100 can be removed by using an etching process. It is noted that, a portion of the fourth filling layer 227 can also be removed by the same etching process.

[00167] As shown in FIG. 45, a second filling layer 229 can be formed in each second through hole 218 in the first region 100, the second region 200 and the third region 300. The material of the second filling layer 229 can be the same material of the fourth filling layer 227.

[00168] As shown in FIG. 46, a portion of the second filling layer 29 can be removed by using an etching process, such that the top surface of the second filling layer 229 in each second through hole 218 is lower than the top surface of the second insulating connection layer 216. The remaining portion of the second filling layer 29 in each second through hole 218 can form the second filling structure.

[00169] Further, the portion of the fourth channel layer 223 located on the surface of the second insulating connection layer 216 or the surface of the second mask layer 217 can be removed by using an etching process. The remaining portion of the fourth channel layer 223 in each second through hole 218 can form the fourth channel structure. The top surface of the fourth channel structure can be higher than the top surface of the second filling structure. As such, a second groove can be formed on the fourth channel structure

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and the second filling structure in each second through hole 218 in the first region 100, and on the second filling structure in each second through hole 218 in the second region 200 and the third region 300.

[00170] It is noted that, the top surface of the fourth channel structure can be higher than the top surface of the second stacked layer 215, or can be lower than the top surface of the second stacked layer 215. The top surface of the fourth channel structure is not lower than the top surface of the top oxide layer in the second stacked layer 215. In some embodiments, the top surface of the fourth channel structure can be in a same plane of the top surface of the top oxide layer in the second stacked layer 215.

[00171] At S2012, a fifth channel structure can be formed in the second groove of each second through hole 218 in the first region 100. The fifth channel structure can be in contact with the fourth channel structure.

[00172] As shown in FIG. 47, the fifth channel structure 230 can be formed in the second groove that is on the fourth channel structure and the second filling structure in each second through hole 218 in the first region 100. The fifth channel structure 230 can also be formed in the second groove that is on the second filling structure in each second through hole 218 in the second region 200 and the third region 300. The nitride layer of the second mask layer 217 can be then removed by an etching process.

[00173] As shown in FIGs. 48A and 48B, the top surface of the second insulating connection layer 216 and the top surface of the plurality of fifth channel structures 230 can be planarized by any suitable techniques, such as backside grinding, and/or chemical mechanical polishing (CMP).

[00174] Accordingly, the disclosed method as shown in FIGs. 50A and 50B can form another joint opening structure of a three-dimensional (3D) memory device by combining two through hole formation processes. As such, the formed channel holes having the joint opening structure can have a large aspect ratio and a limited top-bottom aperture error. Further, the disclosed method of forming a joint opening structure in a 3D memory device can simultaneously form a plurality of channel holes, staircase dummy holes, and through array contact barriers, resulting in an efficient process capability control, a simplified process complexity, and a reduced cost.

[00175] In some embodiments, the present disclosure also provides another three-dimensional memory device formed by using the above disclosed method as shown in FIGs. 50A and 50B. The three-dimensional memory device can include a first region for

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forming a plurality of channel holes, a second region for forming a plurality of staircase structure (SS) dummy holes, and a third region for forming a plurality of through array contact (TAC) barriers. Along a direction perpendicular to the surface of the three-dimensional memory device, the three-dimensional memory device can include the following components.

[00176] A first stacked layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs, is formed on a substrate. A first insulating connection layer is formed on the first stacked layer. A plurality of first through holes penetrating the first stacked layer and the first insulating connection layer and extending into the surface of the substrate are formed in the first region, the second region, and the third region.

[00177] A first channel structure is formed on the surface of the substrate exposed by each first through hole. A first functional layer is formed on the sidewall of each first through hole. A second channel structure is formed on the sidewall of the first functional layer and the surface of the first channel structure in each first through hole. A first filling structure is formed on the sidewall and the surface of the second channel structure to fill each of the plurality of first through holes. In some embodiments, an airgap can be enclosed in the first filling structure in each first through hole. The top surfaces of the second channel structure and the first filling structure are lower than the top surfaces of the first insulating connection layer.

[00178] A first groove is formed in the first insulating connection layer, and above the first functional layer, the second channel structure and the first filling structure in each first through hole. A projection of each of the plurality of first grooves on the substrate completely covers a projection of the corresponding first through hole on the substrate. A third channel structure in contact with the second channel structure in the corresponding first through hole is formed in each first groove.

[00179] A second stack layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs, is formed on the top surfaces of the first insulating connection layer and the plurality of third channel structures. A second insulating connection layer is formed on the second stack layer. A plurality of second through holes penetrating through the second stacked layer and the second insulating connection layer and extending into a surface of the third channel structure are formed in the first region, the second region, and the third region. A projection of each of the

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plurality of second through holes on the substrate at least partially overlaps the projection of the corresponding first through hole on the substrate.

[00180] A second functional layer is formed on the sidewall of each second through hole. A fourth channel structure is formed on the sidewall of the second functional layer and the bottom surface of each second through hole in the first region. A second filling is formed to fill each of the plurality of second through holes in the first region, the second region, and the third region. In some embodiments, an airgap can be enclosed in the second filling structure. The top surface of the fourth channel structure is higher than the top surface of the second filling structure in each second through hole in the first region.

[00181] In the first region, a fifth channel structure in contact with the fourth channel structure is formed in a second groove in each second through hole that is surrounded by the second functional layer, and above the fourth channel structure and the second filling structure. And in the second region and the third region, a fifth channel structure is formed in a second groove in each second through hole that is surrounded by the second functional layer, and above the second filling structure.

[00182] Due to the fourth channel structures being formed in the second through holes in the first region rather than the third region, the fifth channel structure in each second through hole in the first region can be electronically connected with the first channel structure in the corresponding first through hole, while the fifth channel structure in each second through hole in the third region can be electronically insulated with the first channel structure in the corresponding first through hole. Thus, in the three-dimensional memory device, a plurality of channel holes can be formed in the first region, and a plurality of through array contact (TAC) barriers can be formed in the third region. The plurality of staircase structure dummy holes in the second region can have a supporting function of the staircase structure.

[00183] In some embodiments, as shown in FIG. 48A, in each channel hole in the first region, a thickness "b" of the first insulating connection layer, which is the distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 80nm and 100nm, preferably about 90nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00184] In some alternative embodiments, as shown in FIG. 47B, in each channel hole in the first region, a thickness "b" of the first insulating connection layer, which is the

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distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 20nm and 40nm, preferably about 30nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00185] Further, the difference between the radiuses of the top aperture and the bottom aperture of the second channel structure, and the difference between the radiuses of the top aperture and the bottom aperture of the fourth channel structure can be within 15nm. Accordingly, the disclosed channel hole having a joint opening structure can have a large aspect ratio and a limited top-bottom aperture error.

[00186] In some embodiments, a replacement process can be performed to replace each of the plurality of nitride layers in the first stacked layer 202 and the second stacked layer 215 with a conductive layer 240, as shown in FIGs. 49A and 49B. The conductive layer can include any suitable material that is electronically conductive, including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof.

[00187] In some embodiments, the replacement process can be performed in one or more of the first region 100, the second region 200, and the third region 300. In one embodiments, the replacement process is performed in the first region 100 and the second region 200, but not in the third region 300. That is, the first stacked layer and the second stacked layer in the first region and the second region can be alternating conductive/dielectric stack, while the first stacked layer and the second stacked layer in the third region can be alternating oxide/nitride stack.

[00188] In some embodiments, during the replacement process, a portion of the third channel structure 214 that is adjacent with the bottom nitride layer of the second stacked layer 215, or is adjacent with the top nitride layer of the first stacked layer 202 can be converted to an oxide layer by an oxidation process. That is, as shown in FIGs. 49A and 49B, a thickness "c" of the third channel structure can be reduced after the replacement process. For example, the thickness "c" of the third channel structure can be reduced to a range between 30nm and 50nm, preferably about 40nm.

[00189] Referring to FIGs. 74A and 74B, schematic flow diagrams of another exemplary method for forming a joint opening structure of three-dimensional (3D) memory device are illustrated in accordance with some embodiments of the present disclosure. And FIGs. 51-55, 56A, 56B, 57A, 57B, 58A, 58B, 59A, 59B, 60-71, 72A, 72B, 73A and 73B~~51-73~~ illustrate schematic structural cross-sectional diagrams of an exemplary joint

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opening structure of three-dimensional (3D) memory device at certain stages of the fabricating process shown in FIGs. 74A and 74B.

[00190] At S301, a substrate 301 can be provided, a first stacked layer 302 and a first insulating connection layer 303 can be formed on the surface of the substrate 301. As shown in FIG. 51, the first stacked layer 302 can include a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs. The multiple oxide layers (shown in the areas with dotes) and multiple nitride layers (shown in the areas with meshes) in the first stacked layer 302 alternate in a vertical direction. The first stacked layer 302 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide layers and the nitride layers in the first stacked layer 302 is equal to or larger than 64.

[00191] In some embodiments, the first insulating connection layer 303 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is noted that, the material of the first insulating connection layer 303 can be different from the material of the nitride layer in the first stacked layer 302.

[00192] Further, in some embodiments, a first mask layer 304 can be formed on the surface of the first insulating connection layer 303. The first mask layer 304 can include a nitride layer on the surface of the first insulating connection layer 303, and an oxide layer on the surface of such nitride layer.

[00193] At S302, a first through hole 305 can be formed. As shown in FIG. 51, the first through hole 305 can completely penetrate the first stacked layer 302 and the first insulating connection layer 303, and can extend into the surface of the substrate 301.

[00194] In some embodiments, the first through hole 305 can be formed by etching the first stacked layer 302 and the first insulating connection layer 303 and a subsequent cleaning process. The etching process to form the first through hole 305 can be a wet etching, a dry etching, or a combination thereof.

[00195] In some embodiments, when the first mask layer 304 is formed on the surface of the first insulating connection layer 303, the etching process also etch the first mask layer 304 to form the first through holes 305.

[00196] At S303, a first channel structure 306 can be formed on the surface of the substrate 301 that is exposed by the first through hole 305, as shown in FIG. 52. In some embodiments, the first channel structure 306 can be a polycrystalline silicon layer formed by using a selective epitaxial process.

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[00197] At S304, a first functional layer can be formed on the sidewall of the first through hole 305. The first functional layer can include a first tunneling layer 307, a first storage layer 308, a first barrier layer 309, and a first passivation layer 310.

[00198] As shown in FIG. 53, the first tunneling layer 307 can be formed on the sidewall of the first through hole 305 and the surface of the first channel structure 306. The first tunneling layer can be used for generating electronic charges. In some embodiments, the first tunneling layer 307 can be an oxide layer formed by using a deposition process.

[00199] The first storage layer 308 can be formed on the surface of the first tunneling layer 307. The first storage layer 308 can be used for storing electronic charges. In some embodiments, the first storage layer 308 can be a nitride layer formed by using a deposition process.

[00200] The first barrier layer 309 can be formed on the surface of the first storage layer 308. The first barrier layer 309 can be used for blocking the outflow of the electronic charges stored in the first storage layer 308. In some embodiments, the first barrier layer 309 can be an oxide layer formed by using a deposition process.

[00201] As shown in FIG. 54, a first passivation layer 310 can be formed on the surface of the first barrier layer 309. The first passivation layer 310 can be used for protecting the first barrier layer 309 from being damaged in a subsequent removal process. In some embodiments, the first passivation layer 310 can be an amorphous silicon layer formed by using a deposition process.

[00202] The portions of the first passivation layer 310, the first barrier layer 309, the first storage layer 308 and the first tunneling layer 307 located on the surface of the first channel structure 306 on the bottom of the first through hole 305 can be removed. In some embodiments, the removal process can include an etching process and a cleaning process. As such, the first functional layer can be formed on the sidewall of the first through hole 305.

[00203] In some embodiment, in the same removal process, the first barrier layer 309, the first storage layer 308, the first tunneling layer 307, and the oxide layer of the first mask layer 304 located on the surface of the nitride layer of first mask layer 304 can also be removed. As such, the nitride layer of first mask layer 304 is remained on the surface of the first insulating connection layer 303.

[00204] At S305, a second channel structure can be formed on the sidewall of the first functional layer sidewall and the surface of the first channel structure 306. The surfaces

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of the second channel structure can be lower than the surface of the first insulating connection layer 303.

[00205] As shown in FIG. 55, a second channel layer 311 can be formed to cover the sidewall of the first passivation layer 310, the bottom of the first through hole 305. The second channel layer 311 can also cover the surface of the first insulating connection layer 303, or cover the surface of the nitride layer of the first mask layer 304. In some embodiments, the second channel layer 311 can be an amorphous silicon layer formed by using a deposition process.

[00206] As shown in FIGs. 56A and 56B, a portion of the second channel layer 311 can be removed, such that the surface of the second channel layer 311 is lower than the first insulating connection layer 303. The remaining portion of the second channel layer 311 can form the second channel structure that is in contact with the first channel structure 306. In some embodiments, an airgap can be enclosed by the second channel structure, as shown in FIGs. 56A and 56B. In some embodiments, the portion of the second channel layer 311 can be removed by using an etching process.

[00207] It is noted that, in various embodiments, the top surface of the second channel structure can be higher than the top surface of the first stacked layer 302 or lower than the top surface of the first stacked layer 302. However, the top surface of the second channel structure is not lower than the top surface of the top oxide layer in the first stacked layer 302. In some embodiments, the top surface of the second channel structure can be higher than the top nitride layer in the first stacked layer 302, as shown in FIG. 56A. In some alternative embodiments, the top surface of the second channel structure is in a same plane of the top surface of the top oxide layer in the first stacked layer 302, as shown in FIG. 56B.

[00208] At S306, a first groove 312 can be formed in the first insulating connection layer 303. In some embodiments, the projection of the first groove 312 on the substrate 301 can completely cover the projection of the first through hole 305 on the substrate 301.

[00209] As shown in FIGs. 57A and 57B, the nitride layer of the first mask layer 304 can be removed by using an etching process. As shown in FIGs. 58A and 58B, the surface of the first insulating connection layer 303 can be planarized. A portion of the first insulating connection layer 303 can be removed to form the first groove 312 that penetrates the first insulating connection layer 303. An area of the projection of the first

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groove 312 on the substrate 301 can be larger than an area of the projection of the first through hole 305 on the substrate 301.

[00210] In some embodiments, a depth of the first groove can be equal to or less than the thickness of the planarized first insulating connection layer 303, as shown in FIG. 58A. For example, the depth of the first groove can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 303 is about 90nm, while the depth of the first groove is about 60nm.

[00211] In some alternative embodiments, the depth of the first groove can be greater than the thickness of the planarized first insulating connection layer 303, as shown in FIG. 58B. That is, a portion of the top nitride layer in the first stacked layer 302 can also be removed to form the first groove. For example, the depth of the first groove can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 303 is about 30nm, while the depth of the first groove is about 60nm.

[00212] At S307, a third channel structure 313 can be formed in the first groove 312. As shown in FIGs. 59A and 59B, the third channel structure 313 can be in contact with the second channel structure. In some embodiments, the third channel structure can be a polycrystalline silicon player formed by using a deposition process.

[00213] A thickness of the third channel structure 313 can be equal to the depth of the first groove 312. As described above, in some embodiments, a thickness of the third channel structure 313 can be equal to or less than the thickness of the planarized first insulating connection layer 303, as shown in FIG. 59A. For example, the thickness of the third channel structure 313 can be in a range between 50nm and 70nm, preferably about 60nm. In some alternative embodiments, the thickness of the third channel structure 313 can be greater than the thickness of the planarized first insulating connection layer 303, as shown in FIG. 59B. For example, the thickness of the third channel structure 313 can be in a range between 60nm and 80nm, preferably about 70nm.

[00214] At S308, a second stacked layer 314 and a second insulating connection layer 315 can be sequentially formed on the third channel structure 313. As shown in FIG. 60, the second stacked layer 315 can include a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs. Similar to the first stacked layer 302 as described above, the multiple oxide layers (shown in the areas with dotes) and multiple nitride layers (shown in the areas with meshes) in the second stacked layer 314 alternate

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in a vertical direction. The second stacked layer 314 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide layers and the nitride layers in the second stacked layer 314 is equal to or larger than 64.

[00215] In some embodiments, the second insulating connection layer 315 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is noted that, the material of the second insulating connection layer 315 can be different from the material of the nitride layer in the second stacked layer 314.

[00216] Further, in some embodiments, a second mask layer 316 can be formed on the surface of the second insulating connection layer 315. The second mask layer 316 can include a nitride layer on the surface of the second insulating connection layer 315, and an oxide layer on the surface of such nitride layer.

[00217] At S309, a second through hole 317 can be formed. As shown in FIG. 61, the second through hole 317 can completely penetrate the second stacked layer 314 and the second insulating connection layer 315, and can extend into the surface of the third channel structure 313. The projection of the second through hole 317 on the substrate 301 can at least partially overlap with the projection of the first through hole 305 on the substrate 301.

[00218] In some embodiments, the second stacked layer 314, the second insulating connection layer 315, the second mask layer 316, and a portion of the third channel structure 314 can be etched to form the second through hole 317. The second stacked layer 314, the second insulating connection layer 315, the second mask layer 316, and/or the third channel structure 314 can be etched by using a dry etching process, a wet etching process, or a combination thereof. A cleaning process can then be performed to clean the second through hole 317.

[00219] In some embodiments, a maximum difference between the radius of the top aperture of each second through hole 317 and the radius of the bottom aperture of the second through hole 317 can be 15nm. That is, as shown in FIG. 61, a distance "a" between the boundary line of the top surface of the second through hole 317 and the boundary of the bottom surface of the second through hole 317 can be no more than 15 nm.

[00220] At S3010, a second functional layer can be formed on the sidewall of the second through hole 317. In some embodiments, the second functional layer can include

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a second tunneling layer 318, a second storage layer 319, a second barrier layer 320, and a second passivation layer 321.

[00221] As shown in FIG. 62, the second tunneling layer 318 can be formed on the sidewall of the second through hole 317 and the surface of the second channel structure 313. The second tunneling layer 318 can be used for generating electronic charges. In some embodiments, the second tunneling layer 318 can be an oxide layer formed by using a deposition process.

[00222] The second storage layer 319 can be formed on the surface of the second tunneling layer 318. The second storage layer 319 can be used for storing electronic charges. In some embodiments, the second storage layer 319 can be a nitride layer formed by using a deposition process.

[00223] The second barrier layer 320 can be formed on the surface of the second storage layer 319. The second barrier layer 320 can be used for blocking the outflow of the electronic charges in the second storage layer 319. In some embodiments, the second barrier layer 320 can be an oxide layer formed by using a deposition process.

[00224] As shown in FIG. 63, a second passivation layer 321 can be formed on the surface of the second barrier layer 320. The second passivation layer 321 can be used for protecting the second barrier layer 320 from being damaged in a subsequent removal process. In some embodiments, the second passivation layer 322 can be an amorphous silicon layer formed by using a deposition process.

[00225] As shown in FIG. 63, the portions of the second passivation layer 321, the second barrier layer 320, the second storage layer 319, the second tunneling layer 318, and the third channel structure 313 that are located at the bottom of the second through hole 317 and the top of the first through hole 305 can be removed. In some embodiments, the removal process can include an etching process and a cleaning process.

[00226] In some embodiments, the portions of the second passivation layer 321, the second barrier layer 320, the second storage layer 319, the second tunneling layer 318, and the oxide layer of the second mask layer 316 that are located on the nitride layer of the second mask layer 316 can also be removed by using an etching process. As such, the second functional layer can be formed on the sidewall of the second through hole 318, and the second through hole 317 and the first through hole 305 can be interconnected with each other, as shown in FIG. 63.

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[00227] In some embodiments, the portions of the second barrier layer 320, the second storage layer 319, and the second tunneling layer 318 that are located under the second passivation layer 321, as shown in the dashed circle in FIG. 64, can also be removed by using an etching process.

[00228] At S3011, the second tunneling structure, the third tunneling structure, the second passivation layer 321, and the first passivation layer 310 can be removed. In some embodiments, the second tunneling structure, the third tunneling structure, the second passivation layer 321, and the first passivation layer 310 can be removed by using one or more etching processes. As such, a third through hole 322 can be formed by interconnecting the first through hole and the second through hole, as shown in FIG. 65.

[00229] At S3012, a fourth channel structure and a first filling structure can be sequentially formed on the sidewall and the bottom of the third through hole 322. In some embodiments, the surface of the fourth channel structure can be higher than the surface of the first filling structure. In some embodiments, the fourth channel structure includes a joint channel structure that is sandwiched between the first stacked layer 302 and the second stacked layer 314, and covers the exposed surface of the first insulating connection layer 303.

[00230] As shown in FIG. 66, a fourth channel layer 328 can be formed to cover the sidewall and bottom of the third through hole 322 and the exposed surface of the third insulating connection layer 303. In some embodiments, the fourth channel layer 323 can also cover the surface of the second insulating connection layer 315, or the surface of the nitride layer of the second mask layer 316. In some embodiments, the fourth channel layer 328 can be an amorphous silicon layer formed by using a deposition process.

[00231] As shown in FIG. 67, a first filling layer 334 can be formed to cover the fourth channel layer 328 and to fill the third through hole 322. In some embodiments, the first filling layer 334 can be an oxide layer formed by using a deposition process.

[00232] As shown in FIG. 68, a portion of the first filling layer 334 can be removed, such that the surface of the first filling layer 334 is lower than the top surface of the second insulating connection layer 315. In some embodiments, the removal process can include an etching process. The remaining portion of the second filling layer 334 in the third through hole 322 can form the second filling structure.

[00233] As shown in FIG. 69, the portion of the fourth channel layer 328 located on the top surface of the second insulating connection layer 315 or the top surface of the second

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mask layer 316 can be removed. In some embodiments, the removal process can include an etching process. The remaining portion of the fourth channel layer 328 in the third through hole 322 can form the fourth channel structure. The top surface of the fourth channel structure can be higher than the top surface of the second filling structure. As such, a second groove can be formed on the fourth channel structure and the second filling structure, and in the third through hole 322.

[00234] It is noted that, the top surface of the fourth channel structure can be higher than the top surface of the second stacked layer 314, or can be lower than the top surface of the second stacked layer 314. The top surface of the fourth channel structure is not lower than the top surface of the top oxide layer in the second stacked layer 314. In some embodiments, the top surface of the fourth channel structure can be in a same plane of the top surface of the top oxide layer in the second stacked layer 314.

[00235] At S3013, a fifth channel structure can be formed in the second groove. The fifth channel structure can be in contact with the fourth channel structure. As shown in FIG. 70, the fifth channel structure 335 can be formed in the second groove that is on the fourth channel structure and the second filling structure and in the third through hole 322.

[00236] As shown in FIG. 71, the nitride layer of the second mask layer 316 can be removed by an etching process. As shown in FIGs. 72A and 72B, the top surface of the second insulating connection layer 315 and the top surface of the fifth channel structure 335 can be planarized.

[00237] Accordingly, the disclosed method as shown in FIGs. 74A and 74B can form a joint opening structure of a three-dimensional (3D) memory device by combining two through hole formation processes. As such, the formed channel hole having the joint opening structure can have a large aspect ratio and a limited top-bottom aperture error. Further, the disclosed method of forming a joint opening structure in a 3D memory device can result in an efficient process capability control, a simplified process complexity, and a reduced cost.

[00238] In some embodiments, the present disclosure also provides a three-dimensional memory device formed by using the above disclosed method as shown in FIGs. 74A and 74B. The three-dimensional memory can include the following components described below.

[00239] A first stacked layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer silicon nitride layer pairs, is formed on a substrate. A first insulating

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connection layer is formed on the first stacked layer. A first through hole penetrates the first stacked layer and the first insulating connection layer, and extends into the surface of the substrate. A first channel structure is formed on the surface of the substrate exposed by the first through hole. A first functional layer is formed on the sidewall of the first through hole.

[00240] A second stack layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs, is formed on the top surfaces of the first insulating connection layer. A second insulating connection layer is formed on the second stack layer. A second through hole penetrates through the second stacked layer and the second insulating connection layer, and is interconnected with the first through hole. A second functional layer is formed on the sidewall of the second through hole.

[00241] The first through hole and the second through hole constitute the third through hole. A fourth channel structure being contact with the first channel structure is formed on the sidewall and the bottom of the third through hole. A first filling structure is formed on the sidewall and the surface of the fourth channel structure to fill the third through hole. In some embodiments, an airgap is enclosed in the first filling structure. The top surface of the fourth channel structure is higher than the top surface of the first filling structure. A fifth channel structure in contact with the fourth channel structure is formed in a second groove that is surrounded by the second functional layer, and above the fourth channel structure and the first filling structure.

[00242] In some embodiments, as shown in FIG. 72A, a thickness "b" of the first insulating connection layer, which is the distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 80nm and 100nm, preferably about 90nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00243] In some alternative embodiments, as shown in FIG. 72B, a thickness "b" of the first insulating connection layer, which is the distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 20nm and 40nm, preferably about 30nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00244] Further, the error the radius of the aperture of different positions of the third through hole can be within 15nm. That is, a difference between a maximum radius of the third through hole and a minimum radius of the third through hole is less than or equal to

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15nm. Accordingly, the disclosed channel hole having a joint opening structure can have a large aspect ratio and a limited top-bottom aperture error.

[00245] In some embodiments, a replacement process can be performed to replace each of the plurality of nitride layers in the first stacked layer 302 and the second stacked layer 314 with a conductive layer 440, as shown in FIGs. 73A and 73B. The conductive layer can include any suitable material that is electronically conductive, including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof.

[00246] In some embodiments, during the replacement process, a portion of the third channel structure 313 that is adjacent with the bottom nitride layer of the second stacked layer 314, or is adjacent with the top nitride layer of the first stacked layer 302 can be converted to an oxide layer by an oxidation process. That is, as shown in FIGs. 73A and 73B, a thickness "c" of the third channel structure can be reduced after the replacement process. For example, the thickness "c" of the third channel structure can be reduced to a range between 30nm and 50nm, preferably about 40nm.

[00247] Referring to FIGs. 103A and 103B, schematic flow diagrams of another exemplary fabricating process for forming a joint opening structure of three-dimensional (3D) memory device are illustrated in accordance with some other embodiments of the present disclosure. And FIGs. 75-79, 80A, 80B, 81A, 81B, 82A, 82B, 83A, 83B, 84-100, 101A, 101B, 102A and 102B~~75-102~~ illustrate schematic structural cross-sectional diagrams of an exemplary joint opening structure of three-dimensional (3D) memory device at certain stages of the fabricating process shown in FIGs. 103A and 103B.

[00248] As shown in FIG. 103A, at S401, a first stacked layer 402 and a first insulating connection layer 403 can be sequentially formed on the surface of a substrate 401. In some embodiments, the 3D memory device can include a first region 100, a second region 200, and a third region 300, as shown in FIG. 75. The first region 100 can be used to form one or more channel holes, the second region 200 can be used to form one or more staircase structure (SS) dummy holes, while the third region 300 can be used to form one or more through array contact (TAC) barriers.

[00249] As shown in FIG. 75, the first stacked layer 402 can be formed on the substrate 401. The first stacked layer 402 can include a plurality of oxide/nitride layer pairs. That is, in the first stacked layer 402, multiple oxide layers (shown in the areas with dotes) and multiple nitride layers (shown in the areas with meshes) alternate in a vertical direction. In other words, except a top and a bottom layer of a given stack, each of the other oxide

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layers can be sandwiched by two adjacent nitride layers, and each nitride layer can be sandwiched by two adjacent oxide layers.

[00250] Oxide layers can each have the same thickness or have different thicknesses. For example, a thickness of each oxide layer can be in a range from 90nm to 160nm, preferably about 150nm. Similarly, nitride layers can each have the same thickness or have different thicknesses. For example, a thickness of each nitride layer can be in a range from 80nm to 110nm, preferably about 100nm. In some embodiments, the oxide layers can be silicon oxide layers, and the nitride layers can be silicon nitride layer.

[00251] The first stacked layer 402 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide layers and the nitride layers in the first stacked layer 402 is equal to or larger than 64. In some embodiments, alternating conductor/dielectric stack includes more oxide layers or more nitride layers with different materials and/or thicknesses than the oxide/nitride layer pair.

[00252] The first insulating connection layer 403 can be formed on the first stacked layer 402. In some embodiments, the first insulating connection layer 403 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is noted that, the material of the first insulating connection layer 403 can be different from the material of the nitride layer in the first stacked layer 402.

[00253] Further, in some embodiments, a first mask layer 404 can be formed on the surface of the first insulating connection layer 403. The first mask layer 404 can include a nitride layer on the surface of the first insulating connection layer 403, and an oxide layer on the surface of such nitride layer.

[00254] In some embodiments, the first stacked layer 402, the first insulating connection layer 403, and/or the first mask layer 404 can be formed by using one or more deposition processes, such as one or more chemical vapor deposition (CVD) processes, one or more physical vapor deposition (PVD) processes, one or more atomic layer deposition (ALD) processes, and/or any suitable combinations thereof.

[00255] At S402, one or more first through holes 405 can be formed in each of the first region 100, the second region 200, and the third region 300. As shown in FIG. 75, each of the one or more first through holes 405 can completely penetrate the first stacked layer 402 and the first insulating connection layer 403, and can extend into the surface of the substrate 401. In some embodiments, when the first mask layer 404 is formed on the

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surface of the first insulating connection layer 403, the etching process also etch the first mask layer 404 to form the first through holes 405.

[00256] In some embodiments, the first through holes 405 can be formed by etching the first stacked layer 402 and the first insulating connection layer 403 and a subsequent cleaning process. The etching process to form the first through holes 405 can be a wet etching, a dry etching, or a combination thereof. It is noted that, in the direction perpendicular to the surface of the substrate 201, the depth of the one or more first through holes 405 in the third region 300 can be larger than the depth of the one or more first through holes 405 in the first region 100.

[00257] At S403, a first channel structure 406 can be formed on the surface of the substrate 401 that is exposed by each of the plurality of first through holes 405, as shown in FIG. 76. In some embodiments, the first channel structure 406 can be a polycrystalline silicon (polysilicon) layer formed by using a selective epitaxial process.

[00258] At S404, a first functional layer can be formed on the sidewall of each of the plurality of first through holes 405. The first functional layer can include a first tunneling layer 407, a first storage layer 408, a first barrier layer 409, and a first passivation layer 410.

[00259] As shown in FIG. 77, the first tunneling layer 407 can be formed on the sidewall of the plurality of first through holes 405 and the exposed surfaces of the first channel structures 406. The first tunneling layer 407 can be used for generating electronic charges (electrons or holes). In some embodiments, the first tunneling layer 407 can be an oxide layer formed by using a deposition process.

[00260] The first storage layer 408 can be formed on the surface of the first tunneling layer 407. The first storage layer 408 can be used for storing electronic charges. The storage or removal of charge in the first storage layer 407 can impact the on/off state and/or a conductance of the semiconductor channel. The first storage layer 407 can include polycrystalline silicon (polysilicon) or silicon nitride. In some embodiments, the first storage layer 408 can be a nitride layer formed by using a deposition process.

[00261] The first barrier layer 409 can be formed on the surface of the first storage layer 408. The first barrier layer 409 can be used for blocking the outflow of the electronic charges stored in the first storage layer 408. In some embodiments, the first barrier layer 409 can be a silicon oxide layer or a combination of silicon oxide/silicon nitride/silicon oxide (ONO) layers. In some embodiments, the first barrier layer 409

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includes high dielectric constant (high-k) dielectrics (e.g., aluminum oxide). In one example, the first barrier layer 409 is an oxide layer formed by using a deposition process.

[00262] As shown in FIG. 78, a first passivation layer 410 can be formed on the surface of the first barrier layer 409. The first passivation layer 410 can be used for protecting the first barrier layer 409 from being damaged in a subsequent removal process. In some embodiments, the first passivation layer 410 can be an amorphous silicon layer formed by using a deposition process.

[00263] The portions of the first passivation layer 410, the first barrier layer 409, the first storage layer 408 and the first tunneling layer 407 located on the surfaces of the plurality of first channel structures 406 on the bottom of the plurality of first through holes 405 can be removed. In some embodiments, the removal process can include an etching process and a cleaning process. As such, the first functional layer can be formed on the sidewalls of the plurality of first through holes 405.

[00264] In some embodiment, in the same removal process, the first barrier layer 409, the first storage layer 408, the first tunneling layer 407, and the oxide layer of the first mask layer 404 located on the surface of the nitride layer of first mask layer 404 can also be removed. As such, the nitride layer of first mask layer 404 is remained on the surface of the first insulating connection layer 403.

[00265] At S405, a second channel structure can be formed on the sidewall of the first functional layer and the exposed surface of the first channel structure 406 in each of the plurality of first through holes 405. The second channel structure can be in contact with the first channel structure 406 in each first through hole 405. The surface of the second channel structure in each first through hole 405 can be lower than the top surface of the first insulating connection layer 403.

[00266] As shown in FIG. 79, a second channel layer 411 can be formed to cover the sidewalls of the first passivation layer 410 and the bottom of each of the plurality of first through holes 405. The second channel layer 411 can also cover the surface of the first insulating connection layer 403, or cover the surface of the nitride layer of the first mask layer 404. In some embodiments, the second channel layer 411 can be an amorphous silicon layer formed by using a deposition process.

[00267] As shown in FIGs. 80A and 80B, a portion of the second channel layer 411 can be removed, such that the top surface of the second channel layer 411 can be lower than the

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top surface of the first insulating connection layer 403. The remaining portion of the second channel layer 411 can form the second channel structure that is in contact with the first channel structure 406. In some embodiments, the portion of the second channel layer 411 can be removed by using an etching process.

[00268] It is noted that, in various embodiments, the top surface of the second channel structure can be higher than the top surface of the first stacked layer 402 or lower than the top surface of the first stacked layer 402. However, the top surface of the second channel structure is not lower than the top surface of the top oxide layer in the first stacked layer 402. In some embodiments, the top surface of the second channel structure can be higher than the top nitride layer in the first stacked layer 402, as shown in FIG. 80A. In some alternative embodiments, the top surface of the second channel structure is in a same plane of the top surface of the top oxide layer in the first stacked layer 402, as shown in FIG. 80B.

[00269] At S406, a first groove can be formed above the first insulating connection layer 403 above each of the plurality of first through holes 405. In some embodiments, the projection of the first groove on the substrate 401 can completely cover the projection of the corresponding first through hole 405 on the substrate 401.

[00270] As shown in FIGs. 81A and 81B, the nitride layer of the first mask layer 404 can be removed. In some embodiments, the nitride layer of the first mask layer 404 can be removed by using an etching process.

[00271] As shown in FIGs. 82A and 82B, the surface of the first insulating connection layer 403 can be planarized by any suitable techniques, such as backside grinding, and/or chemical mechanical polishing (CMP). A portion of the first insulating connection layer 403 can be removed to form a plurality of first grooves that penetrate the first insulating connection layer 403. An area of the projection of each of the plurality of first grooves on the substrate 401 can be larger than an area of the projection of each of the plurality of first through holes 405 on the substrate 401.

[00272] In some embodiments, a depth of the first groove 412 can be equal to or less than the thickness of the planarized first insulating connection layer 403, as shown in FIG. 82A. For example, the depth of the first groove 412 can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 403 is about 90nm, while the depth of the first groove is about 60nm.

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[00273] In some alternative embodiments, the depth of the first groove 412 can be greater than the thickness of the planarized first insulating connection layer 403, as shown in FIG. 82B. That is, a portion of the top nitride layer in the first stacked layer 402 can also be removed to form the first groove. For example, the depth of the first groove 412 can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 403 is about 30nm, while the depth of the first groove is about 60nm.

[00274] At S407, a third channel structure 413 can be formed in each of the plurality of first grooves 412. As shown in FIGs. 83A and 83B, the third channel structure 413 can be in contact with the second channel structure in each of the plurality of first through holes 405. In some embodiments, the third channel structure 413 can be a polycrystalline silicon player formed by using a deposition process.

[00275] A thickness of each third channel structure 413 can be equal to the depth of each first groove 412. As described above, in some embodiments, a thickness of each third channel structure 413 can be equal to or less than the thickness of the planarized first insulating connection layer 403, as shown in FIG. 83A. For example, the thickness of each third channel structure 413 can be in a range between 50nm and 70nm, preferably about 60nm. In some alternative embodiments, the thickness of each third channel structure 413 can be greater than the thickness of the planarized first insulating connection layer 403, as shown in FIG. 83B. For example, the thickness of each third channel structure 413 can be in a range between 60nm and 80nm, preferably about 70nm.

[00276] Referring to FIG. 103B, at S408, a second stacked layer 414 and a second insulating connection layer 415 can be sequentially formed on the plurality of third channel structures 413. As shown in FIG. 84, the second stacked layer 414 can include a plurality of oxide/nitride layer pairs, such as silicon oxide layers and silicon nitride layers. Similar to the first stacked layer 402 as described above, the multiple oxide layers (shown in the areas with dotes) and multiple nitride layers (shown in the areas with meshes) in the second stacked layer 414 alternate in a vertical direction. The second stacked layer 414 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide layers and the nitride layers in the second stacked layer 414 is equal to or larger than 64.

[00277] In some embodiments, the second insulating connection layer 415 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is

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noted that, the material of the second insulating connection layer 415 can be different from the material of the nitride layer in the second stacked layer 414.

[00278] Further, in some embodiments, a second mask layer 416 can be formed on the surface of the second insulating connection layer 415. The second mask layer 416 can include a nitride layer on the surface of the second insulating connection layer 415, and an oxide layer on the surface of such nitride layer.

[00279] At S409, one or more second through holes 417 are formed in each of the first region 100, the second region 200, and the third region 300. As shown in FIG. 85, each of the plurality of second through holes 417 can completely penetrate the second stacked layer 414, the second insulating connection layer 415, and the second mask layer 416, and can extend into the surface of the corresponding third channel structure 413. The projection of each second through hole 417 on the substrate 401 can at least partially overlap with the projection of the corresponding first through hole 405 on the substrate 401.

[00280] In some embodiments, the second stacked layer 414, the second insulating connection layer 415, the second mask layer 416, and the third channel structures 413 can be etched to form the plurality of second through holes 417 that penetrate the second stacked layer 414 and the second insulating connection layer 415. The second stacked layer 414, the second insulating connection layer 415, the second mask layer 416, and/or the third channel structure 413 can be etched by using a dry etching process, a wet etching process, or a combination thereof. A cleaning process can then be performed to clean the plurality of second through holes 417.

[00281] It is noted that, each second through hole 417 can extend to the surface of the corresponding third channel structure 413, or can extend into the corresponding third channel structure 413. As such, a fourth channel structure formed subsequently in each second through hole 417 can directly contact the corresponding third channel structure.

[00282] In some embodiments, a maximum difference between the radius of the top aperture of each second through hole 417 and the radius of the bottom aperture of the second through hole 417 can be 15nm. That is, as shown in FIG. 85, a distance "a" between the boundary line of the top surface of each second through hole 417 and the boundary of the bottom surface of the second through hole 417 can be no more than 15 nm.

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[00283] At S4010, a second functional layer can be formed on the sidewall of each second through hole 417. In some embodiments, the second functional layer can include a second tunneling layer 418, a second storage layer 419, a second barrier layer 420, and a second passivation layer 421.

[00284] As shown in FIG. 86, the second tunneling layer 418 can be formed on the sidewall of each second through hole 417 and the surface of the corresponding third channel structure 413. The second tunneling layer 418 can be used for generating electronic charges. In some embodiments, the second tunneling layer 418 can be an oxide layer formed by using a deposition process.

[00285] The second storage layer 419 can be formed on the surface of the second tunneling layer 418. The second storage layer 419 can be used for storing electronic charges. In some embodiments, the second storage layer 419 can be a nitride layer formed by using a deposition process.

[00286] The second barrier layer 420 can be formed on the surface of the second storage layer 419. The second barrier layer 420 can be used for blocking the outflow of the electronic charges in the second storage layer 419. In some embodiments, the second barrier layer 420 can be an oxide layer formed by using a deposition process.

[00287] As shown in FIG. 87, a second passivation layer 421 can be formed on the surface of the second barrier layer 420. The second passivation layer 421 can be used for protecting the second barrier layer 420 from being damaged in a subsequent removal process. In some embodiments, the second passivation layer 421 can be an amorphous silicon layer formed by using a deposition process.

[00288] As shown in FIG. 87, the portions of the second passivation layer 421, the second barrier layer 420, the second storage layer 419, the second tunneling layer 418, and the third channel structure 413 between each second through hole 417 and the corresponding first through hole 405 can be removed. In some embodiments, the removal process can include an etching process and a cleaning process. In some embodiments, the portions of the second passivation layer 421, the second barrier layer 420, the second storage layer 419, the second tunneling layer 418, the oxide layer of the second mask layer 416 that are located on the nitride layer of the second mask layer 416 can also be removed by the same removal process. As such, the second functional layer can be formed on the sidewall of each second through hole 417, and each second through hole 417 and the corresponding first through hole 405 can be interconnected with each other.

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[00289] In some embodiments, the portions of the second barrier layer 420, the second storage layer 419, and the second tunneling layer 418 that are located under the second passivation layer 421, as shown in the dashed circle in FIG. 88, can also be removed by using an etching process.

[00290] At S4011, the second tunneling structure, the third tunneling structure, the second passivation layer 421, and the first passivation layer 410 can be removed. In some embodiments, the second tunneling structure, the third tunneling structure, the second passivation layer 421, and the first passivation layer 410 can be removed by using one or more etching processes. As such, a plurality of third through holes 422 can be formed in the first region 100, the second region 200, and the third region 300 by interconnecting each first through hole and the corresponding second through hole, as shown in FIG. 89.

[00291] At S4012, a fourth channel structure can be formed on the sidewall of the second functional layer and the exposed surface of the third channel structure in each third through hole 422 in the first region 100. Further, a first filling structure can be formed in each of the plurality of third through holes 422 in the first region 100, the second region 200, and the third region 300. In some embodiments, the top surface of the fourth channel structure can be higher than the top surface of the first filling structure.

[00292] As shown in FIG. 90, a fourth channel layer 428 can be formed to cover the sidewall and the bottom surface of each of the plurality of third through holes 422 in the first region 100, the second region 200, and the third region 300. In some embodiments, the fourth channel layer 428 can also cover the top surface of the nitride layer of the second mask layer 416. In some embodiments, the fourth channel layer 428 can be an amorphous silicon layer formed by using a deposition process. In some embodiments, the fourth channel structure 428 includes a joint channel structure that is sandwiched between the first stacked layer 402 and the second stacked layer 414, and covers the exposed surface of the first insulating connection layer 403.

[00293] As shown in FIG. 91, a second filling layer 429 can be formed to cover the fourth channel layer 428. In some embodiments, the second filling layer 429 can include one or more airgaps in each third through hole 417. In some embodiments, the second filling layer 429 can be an oxide layer formed by using a deposition process.

[00294] As shown in FIG. 92, a third mask layer 430 can be formed on the top surface of the second filling layer 429 in the first region 100. Using the third mask layer 430 as

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a mask, the portions of the second filling layer 429 located in the second region 200 and the third region 300 can be removed by using an etching process.

[00295] As shown in FIG. 93, the third mask layer 430 can be removed. Using the remaining second filling layer 429 in the first region 100 as a mask, the fourth channel layer 428 located in the second region 200 and the third region 300 can be removed by using an etching process. As such, one or more fourth through holes 431 can be formed in the second region 200 and the third region 300.

[00296] As shown in FIG. 94, a third filling layer 432 can be formed to cover the sidewall and the bottom of the one or more fourth through holes 431 in the second region 200 and the third region 300. The third filling layer 432 can also cover the exposed surface of the first insulating connection layer 403 in each fourth through hole 431 in the second region 200 and the third region 300. In some embodiments, the third filling layer 432 can enclose one or more airgap in one or more fourth through holes 431. In some embodiments, the filling performance of the third filling layer 432 can be better than the filling performance of the second filling layer 429. That is, in a same removing process, the removal rate of the third filling layer 432 can be less than the removal rate of the second filling layer 429.

[00297] As shown in FIG. 95, the second filling layer 429 on the surface of the fourth channel layer 428 in the first region 100 can be removed by using an etching process. As such, one or more fifth through holes 433 can be formed in the first region 100. It is noted that, a portion of the third filling layer 432 can also be removed by the same etching process.

[00298] As shown in FIG. 96, a first filling layer 434 can be formed in each fifth through hole 433 in the first region 100, and in each fourth through hole 431 in the second region 200 and the third region 300. The material of the first filling layer 434 can be the same material of the third filling layer 432.

[00299] As shown in FIG. 97, a portion of the first filling layer 434 can be removed by using an etching process, such that the top surface of the first filling layer 434 in each fifth through hole 433 or fourth through hole 431 is lower than the top surface of the second insulating connection layer 415. The remaining portion of the first filling layer 434 in each fourth through hole 431 or fifth through hole 433 can form the first filling structure.

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[00300] Further, the portion of the fourth channel layer 428 located on the surface of the second insulating connection layer 415 or the surface of the second mask layer 416 can be removed by using an etching process. The remaining portion of the fourth channel layer 428 in each fifth through hole 433 can form the fourth channel structure. The top surface of the fourth channel structure can be higher than the top surface of the first filling structure. As such, a second groove can be formed on the fourth channel structure and the first filling structure in each fifth through hole 433 in the first region 100, and on the first filling structure in each fourth through hole 431 in the second region 200 and the third region 300.

[00301] It is noted that, the top surface of the fourth channel structure can be higher than the top surface of the second stacked layer 414, or can be lower than the top surface of the second stacked layer 414. The top surface of the fourth channel structure is not lower than the top surface of the top oxide layer in the second stacked layer 414. In some embodiments, the top surface of the fourth channel structure can be in a same plane of the top surface of the top oxide layer in the second stacked layer 414.

[00302] At S4013, a fifth channel structure can be formed in the second groove of each fifth through hole 433 in the first region 100 and each fourth 431 in the second region 200 and third region 300. The fifth channel structure can be in contact with the fourth channel structure in each fifth through hole 433 in the first region 100.

[00303] As shown in FIG. 99, the fifth channel structure 435 can be formed in the second groove that is on the fourth channel structure and the first filling structure in each fifth through hole 433 in the first region 100. The fifth channel structure 435 can also be formed in the second groove that is on the first filling structure in each fourth through hole 431 in the second region 200 and the third region 300.

[00304] As shown in FIG. 100, the nitride layer of the second mask layer 416 can be then removed by an etching process. As shown in FIGs. 101A and 101B, the top surface of the second insulating connection layer 415 and the top surface of the plurality of fifth channel structures 435 can be planarized by any suitable techniques, such as backside grinding, and/or chemical mechanical polishing (CMP).

[00305] Accordingly, the disclosed method as shown in FIGs. 101A and 101B can form another joint opening structure of a three-dimensional (3D) memory device by combining two through hole formation processes. As such, the formed channel holes having the joint opening structure can have a large aspect ratio and a limited top-bottom aperture

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error. Further, the disclosed method of forming a joint opening structure in a 3D memory device can simultaneously form a plurality of channel holes, staircase dummy holes, and through array contact barriers, resulting in an efficient process capability control, a simplified process complexity, and a reduced cost.

[00306] In some embodiments, the present disclosure also provides another three-dimensional memory device formed by using the above disclosed method as shown in FIGs. 101A and 101B. The three-dimensional memory device can include a first region for forming a plurality of channel holes, a second region for forming a plurality of staircase structure (SS) dummy holes, and a third region for forming a plurality of through array contact (TAC) barriers. Along a direction perpendicular to the surface of the three-dimensional memory device, the three-dimensional memory device can include the following components.

[00307] A first stacked layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs, is formed on a substrate. A first insulating connection layer is formed on the first stacked layer. A plurality of first through holes penetrating the first stacked layer and the first insulating connection layer and extending into the surface of the substrate are formed in the first region, the second region, and the third region.

[00308] A first channel structure is formed on the surface of the substrate exposed by each first through hole. A first functional layer is formed on the sidewall of each first through hole. A second channel structure is formed on the sidewall of the first functional layer and the surface of the first channel structure in each first through hole. A first filling structure is formed on the sidewall and the surface of the second channel structure to fill each of the plurality of first through holes. In some embodiments, an airgap can be enclosed in the first filling structure in each first through hole. The top surfaces of the second channel structure and the first filling structure are lower than the top surfaces of the first insulating connection layer.

[00309] A first groove is formed in the first insulating connection layer, and above the first functional layer, the second channel structure and the first filling structure in each first through hole. A projection of each of the plurality of first grooves on the substrate completely covers a projection of the corresponding first through hole on the substrate. A third channel structure in contact with the second channel structure in the corresponding first through hole is formed in each first groove.

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[00310] A second stack layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs, is formed on the top surfaces of the first insulating connection layer and the plurality of third channel structures. A second insulating connection layer is formed on the second stack layer. A plurality of second through holes penetrating through the second stacked layer and the second insulating connection layer and extending into a surface of the third channel structure are formed in the first region, the second region, and the third region. A projection of each of the plurality of second through holes on the substrate at least partially overlaps the projection of the corresponding first through hole on the substrate.

[00311] A second functional layer is formed on the sidewall of each second through hole. A fourth channel structure is formed on the sidewall of the second functional layer and the bottom surface of each second through hole in the first region. A second filling is formed to fill each of the plurality of second through holes in the first region, the second region, and the third region. In some embodiments, an airgap can be enclosed in the second filling structure. The top surface of the fourth channel structure is higher than the top surface of the second filling structure in each second through hole in the first region.

[00312] In the first region, a fifth channel structure in contact with the fourth channel structure is formed in a second groove in each second through hole that is surrounded by the second functional layer, and above the fourth channel structure and the second filling structure. And in the second region and the third region, a fifth channel structure is formed in a second groove in each second through hole that is surrounded by the second functional layer, and above the second filling structure.

[00313] Due to the fourth channel structures being formed in the second through holes in the first region rather than the third region, the fifth channel structure in each second through hole in the first region can be electronically connected with the first channel structure in the corresponding first through hole, while the fifth channel structure in each second through hole in the third region can be electronically insulated with the first channel structure in the corresponding first through hole. Thus, in the three-dimensional memory device, a plurality of channel holes can be formed in the first region, and a plurality of through array contact (TAC) barriers can be formed in the third region. The plurality of staircase structure dummy holes in the second region can have a supporting function of the staircase structure.

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[00314] In some embodiments, as shown in FIG. 101A, in each channel hole in the first region, a thickness "b" of the first insulating connection layer, which is the distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 80nm and 100nm, preferably about 90nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00315] In some alternative embodiments, as shown in FIG. 101B, in each channel hole in the first region, a thickness "b" of the first insulating connection layer, which is the distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 20nm and 40nm, preferably about 30nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00316] Further, the difference between the radiuses of the top aperture and the bottom aperture of the second channel structure, and the difference between the radiuses of the top aperture and the bottom aperture of the fourth channel structure can be within 15nm. Accordingly, the disclosed channel hole having a joint opening structure can have a large aspect ratio and a limited top-bottom aperture error.

[00317] In some embodiments, a replacement process can be performed to replace each of the plurality of nitride layers in the first stacked layer 402 and the second stacked layer 414 with a conductive layer 440, as shown in FIGs. 102A and 102B. The conductive layer can include any suitable material that is electronically conductive, including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof.

[00318] In some embodiments, the replacement process can be performed in one or more of the first region 100, the second region 200, and the third region 300. In one embodiments, the replacement process is performed in the first region 100 and the second region 200, but not in the third region 300. That is, the first stacked layer and the second stacked layer in the first region and the second region can be alternating conductive/dielectric stack, while the first stacked layer and the second stacked layer in the third region can be alternating oxide/nitride stack.

[00319] In some embodiments, during the replacement process, a portion of the third channel structure 413 that is adjacent with the bottom nitride layer of the second stacked layer 414, or is adjacent with the top nitride layer of the first stacked layer 402 can be

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converted to an oxide layer by an oxidation process. That is, as shown in FIGs. 102A and 102B, a thickness “c” of the third channel structure can be reduced after the replacement process. For example, the thickness “c” of the third channel structure can be reduced to a range between 30nm and 50nm, preferably about 40nm.

[00320] The provision of the examples described herein (as well as clauses phrased as "such as," "e.g.," "including," and the like) should not be interpreted as limiting the claimed subject matter to the specific examples; rather, the examples are intended to illustrate only some of many possible aspects.

[00321] Further, the words "first", "second" and the like used in this disclosure do not denote any order, quantity or importance, but are merely intended to distinguish between different constituents. The words "comprise" or "include" and the like mean that the elements or objects preceding the word can cover the elements or objects listed after the word and their equivalents, without excluding other elements or objects. The words "connect" or "link" and the like are not limited to physical or mechanical connections, but can include electrical connections, either directly or indirectly.

[00322] Although the present disclosure has been described and illustrated in the foregoing illustrative embodiments, it is understood that the present disclosure has been made only by way of example, and that numerous changes in the details of embodiment of the present disclosure can be made without departing from the spirit and scope of the present disclosure, which is only limited by the claims which follow. Features of the disclosed embodiments can be combined and rearranged in various ways. Without departing from the spirit and scope of the present disclosure, modifications, equivalents, or improvements to the present disclosure are understandable to those skilled in the art and are intended to be encompassed within the scope of the present disclosure.

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JOINT OPENING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application claims priority to PCT/CN2018/077785 filed on March 1, 2018, which claims the priorities of Chinese Patent Application No. 201710134782.1, filed on March 8, 2017, and Chinese Patent Application No. 201710134783.6, filed on March 8, 2017, the entire contents of which are incorporated herein by reference.

TECHNICAL FIELD

[0002] The present disclosure generally relates to the field of semiconductor technology, and more particularly, to joint opening structures of three-dimensional (3D) memory devices and method for forming the same.

BACKGROUND

[0003] As semiconductor technology advances, three-dimensional (3D) memory devices, such as 3D NAND memory devices, keep scaling more oxide/nitride (ON) layers. As such, it becomes difficult to use a single etching process to form the channel holes in the 3D memory devices that have a substantial depth. As the channel hole aspect ratio increases, channel hole etching becomes exponentially slower. Further, the process capability control of the formed channel holes, including bow-free, straight profile, critical dimension (CD) uniformity, minimal twisting, etc., tend to be more challenging. Thus, a single etching method may not be efficient in both cost and process capability.

BRIEF SUMMARY

[0004] In accordance with some embodiments of the present disclosure, joint opening structures of three-dimensional (3D) memory devices and method for forming the same are provided.

[0005] One aspect of the present disclosure provides a method of forming a joint opening structure in a three-dimensional (3D) memory device. The method includes forming a

first stacked layer and forming a first insulating connection layer on the first stacked layer, forming a first through hole that penetrates the first stacked layer and the first insulating connection layer, forming a first channel structure overlay the surface of the substrate that is exposed by the first through hole, forming a first functional layer on the sidewall of the first through hole, forming a second channel structure and forming a first filling structure on the sidewall of the first functional layer and the exposed surface of the first channel structure, and forming a third channel structure in contact with the second channel structure above the first through hole. A projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate. The method further includes forming a second stacked layer and forming a second insulating connection layer on the first insulating connection layer, forming a second through hole that penetrates the second stacked layer and the second insulating connection layer. A projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate. The method further includes forming a second functional layer on the sidewall of the second through hole, forming a fourth channel structure and forming a second filling structure on the sidewall of the second functional layer and the exposed surface of the third channel structure, and forming a fifth channel structure in contact with the fourth channel structure above the second through hole.

[0006] In some embodiments, the first stacked layer includes a first number of oxide/nitride layer pairs, and the second stacked layer includes a second number of oxide/nitride layer pairs. The first number and the second number are not less than 32.

[0007] Forming the first functional layer includes forming a first tunneling layer on the sidewall of the first through hole and the exposed surface of the first channel structure. The first tunneling layer is configured, in operation, to generate charges. Forming the first functional further includes forming a first storage layer on the surface of the first tunneling layer to store the charges generated by the first tunneling layer, forming a first barrier layer on the surface of the first storage layer to block the outflow of charges in the first storage layer, forming a first passivation layer on the surface of the first barrier layer to protect the first barrier layer from being damaged in a subsequent removal process, and removing portions of the first passivation layer, the first barrier layer, the first storage layer, and the first tunneling layer on the surface of the first channel structure. The remaining portions of the first passivation layer, the first barrier layer, the first storage

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layer, and the first tunneling layer on the sidewall of the first through hole form the first functional layer.

[0008] Forming the second channel structure and the first filling structure includes forming a second channel layer that covers the sidewall of the first passivation layer and the exposed surface of the first channel layer, forming the first filling layer that covers the surface of the second channel layer, removing a portion of the first filling layer to form the first filling structure, wherein the top surface of the first filling structure is lower than the top surface of the first insulating connection layer, and removing a portion of the second channel layer to form the second channel structure. A top surface of the second channel structure is lower than a top surface of the first insulating connection layer.

[0009] Forming the third channel structure includes etching the first insulating connection layer to form a first groove. In some other embodiments, forming the third channel structure includes etching the first insulating connection layer and at least a portion of the top nitride layer of the first stacked layer to form a first groove. A projection of the first groove on the substrate covers the projection of the first through hole on the substrate. Forming the third channel structure further includes forming a third channel layer in the first groove, wherein the third channel layer is in contact with the second channel structure, and planarizing the top surfaces of the first insulating connection layer and the third channel layer to form the third channel structure.

[0010] In some embodiments, the method further includes forming a first mask layer overlaying the first insulating connection layer before forming the first through hole, and removing the first mask layer after forming the third channel structure, and forming a second mask layer on the second insulating connection layer before forming the second through hole, and removing the first mask layer after forming the fifth channel structure

[0011] Forming the fourth channel structure and the second filling structure includes forming a fourth channel layer that covers the sidewall of the second functional layer and the exposed surface of the third channel layer, forming a second filling layer that covers the surface of the fourth channel layer, removing a portion of the second filling layer to form the second filling structure, and removing a portion of the fourth channel layer to form the fourth channel structure, wherein a top surface of the fourth channel structure is lower than a top surface of the second insulating connection layer. A top surface of the second filling structure is lower than the top surface of the second insulating connection layer.

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[0012] Forming the fifth channel structure includes etching the second insulating connection layer to form a second groove, forming a fifth channel layer in the second groove, wherein the fifth channel layer is in contact with the fourth channel structure, and planarizing the top surfaces of the second insulating connection layer and the fifth channel layer to form the fifth channel structure. A projection of the second groove on the substrate covers the projection of the second through hole on the substrate.

[0013] Another aspect of the present disclosure provides another method of forming a joint opening structure in a three-dimensional (3D) memory device. The method includes forming a first stacked layer and forming a first insulating connection layer on a substrate of the 3D memory device. The 3D memory device includes a first region for forming a plurality of channel holes, a second region for forming a plurality of staircase structure dummy holes, and a third region for forming a plurality of through array contact barriers. The method further includes forming a plurality of first through holes, each penetrating the first stacked layer and the first insulating connection layer in the first region, the second region, and the third region, forming a first channel structure overlaying the surface of the substrate in each first through hole, forming a first functional layer on the sidewall of each first through hole, forming a second channel structure and forming a first filling structure on the sidewall of the first functional layer and the exposed surface of the first channel structure in each first through hole, forming a third channel structure in contact with the second channel structure above each first through hole. A projection of the third channel structure on the substrate covers a projection of the corresponding first through hole on the substrate. The method further includes forming a second stacked layer on the first insulating connection layer, forming a second insulating connection layer on the second stacked layer, forming a plurality of second through holes, each penetrating the second stacked layer and the second insulating connection layer. A projection of each of the plurality of second through holes on the substrate at least partially overlaps with the projection of the corresponding first through hole on the substrate. The method further includes forming a second functional layer on the sidewall of each second through hole, forming a fourth channel structure and forming a second filling structure on the sidewall of the second functional layer and the exposed surface of the third channel structure in each second through hole in the first region, and forming a second filling structure on the sidewall of the second functional layer in each second through hole in the second region and the third region, and forming a fifth channel

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structure above each second through hole in the first region, the second region, and the third region. Each fifth channel structure is in contact with the corresponding fourth channel structure in each second through hole in the first region.

[0014] Forming the fourth channel structure and the second filling structure includes forming a fourth channel layer that covers the sidewall of the first passivation layer and the exposed surface of the third channel layer, forming a third filling layer that covers the surface of the fourth channel layer, forming a third mask layer that covers the third filling layer in the first region, and using the third mask layer as a mask to remove the third filling layer in the second region and the third region, removing the third mask layer;, using the third filling layer in the first region as a mask to remove the fourth channel layer in the second region and the third region, forming a fourth filling layer on the surface of the second functional layer in the second region and the third region, removing the third filling layer in the first region, forming a second filling layer in each second through hole in the first region, the second region, and the third region, removing a portion of the second filling layer to form the second filling structure in each second through hole, and removing a portion of the fourth channel layer to form the fourth channel structure in each second through hole. The top surface of the second filling structure is lower than the top surface of the second insulating connection layer, and the top surface of the fourth channel structure is lower than the top surface of the second insulating connection layer.

[0015] Another aspect of the present disclosure provides annother method of forming a joint opening structure in a three-dimensional (3D) memory device. The method includes forming a first stacked layer and forming a first insulating connection layer on a substrate, forming a first through hole that penetrates the first stacked layer and the first insulating connection layer, forming a first channel structure overlay the surface of the substrate that is exposed by the first through hole, forming a first functional layer on the sidewall of the first through hole, forming a second channel on the sidewall of the first functional layer and the exposed surface of the first channel structure, forming a third channel structure in contact with the second channel structure above the first through hole. A projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate. The method further includes forming a second stacked layer and forming a second insulating connection layer on the third channel structure, forming a second through hole that penetrates the second stacked layer and the second insulating connection layer. A projection of the second through hole on the substrate at least

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partially overlaps with the projection of the first through hole on the substrate. The method further includes forming a second functional layer on the sidewall of the second through hole, removing portions of the second functional layer and the third channel structure at the bottom of the second through hole to interconnect the second through hole and the first through hole to form a joint through hole, removing the remaining portion of the third channel structure and the second channel structure, forming a fourth channel structure in contact with the first channel structure on the sidewall of the joint through hole and the exposed surface of the first insulating connection layer, forming a first filling structure that covers the surface of the fourth channel structure, and forming a fifth channel structure in contact with the fourth channel structure above the joint through hole.

[0016] Another aspect of the present disclosure provides another method of forming a joint opening structure in a three-dimensional (3D) memory device. The method includes forming a first stacked layer and forming a first insulating connection layer on a substrate of the 3D memory device. The 3D memory device includes a first region for forming a plurality of channel holes, a second region for forming a plurality of staircase structure dummy holes, and a third region for forming a plurality of through array contact barriers. The method further includes forming a plurality of first through holes, each penetrating the first stacked layer and the first insulating connection layer in the first region, the second region, and the third region, forming a first channel structure on the surface of the substrate in each first through hole, forming a first functional layer on the sidewall of each first through hole, forming a second channel structure on the sidewall of the first functional layer and the exposed surface of the first channel structure in each first through hole, forming a third channel structure in contact with the second channel structure above each first through hole. A projection of the third channel structure on the substrate covers a projection of the corresponding first through hole on the substrate. The method further includes forming a second stacked layer and forming a second insulating connection layer on the plurality of third channel structures, forming a plurality of second through holes, each penetrating the second stacked layer and the second insulating connection layer. A projection of each of the plurality of second through holes on the substrate at least partially overlaps with the projection of the corresponding first through hole on the substrate. The method further includes forming a second functional layer on the sidewall of each second through hole, removing portions of the second functional layer and the third channel structure at the bottom of each second through hole to interconnect the

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second through hole and the corresponding first through hole to form a plurality of joint through holes, removing the remaining portions of the third channel structure and the second channel structure in each joint through hole, forming a fourth channel structure in contact with the first channel structure on the sidewall of each joint through hole and the exposed surfaces of the first insulating connection layer, forming a first filling structure that covers the surface of the fourth channel structure in each joint through hole, and forming a fifth channel structure above each joint through hole in the first region, the second region, and the third region. Each fifth channel structure is in contact with the corresponding fourth channel structure in each joint through hole in the first region.

[0017] Another aspect of the present disclosure provides a joint opening structure of a three-dimensional (3D) memory device, including a first stacked layer disposed overlaying a substrate, a first insulating connection layer disposed on the first stacked layer, a first through hole penetrating the first stacked layer and the first insulating connection layer, a first channel structure disposed at the bottom of the first through hole and overlaying the surface of the substrate, a first functional layer disposed on the sidewall of the first through hole, a second channel structure in contact with the first channel structure disposed on the sidewall of the first functional layer, a third channel structure in contact with the second channel structure disposed over the first through hole. A projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate. The joint opening structure further includes a second stacked layer disposed on the third channel structure, a second insulating connection layer disposed on the second stacked layer. A second through hole penetrating the second stacked layer and the second insulating connection layer. A projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate. The joint opening structure further includes a second functional layer disposed on the sidewall of the second through hole, a fourth channel structure in contact with the third channel structure disposed on the sidewall of the second functional layer, and a fifth channel structure in contact with the fourth channel structure disposed over the second through hole.

[0018] In some embodiments, a first filling structure covers the surface of the second channel structure, and a second filling structure covers the surface of the fourth channel structure. The first through hole is non-interconnected with the second through hole.

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[0019] In some other embodiments, a first filling structure covers the surfaces of the second channel structure and the fourth channel structure. The first through hole is interconnected with the second through hole.

[0020] In some embodiments, the first stacked layer includes a first number of conductor/dielectric layer pairs, and the second stacked layer includes a second number of conductor/dielectric layer pairs.

[0021] In some other embodiments, the first stacked layer includes a first number of oxide/nitride layer pairs, and the second stacked layer includes a second number of oxide/nitride layer pairs. The first number and the second number are not less than 32.

[0022] A thickness of the third channel structure is in a range between 30nm and 70nm. A size difference between a top aperture and a bottom aperture of the first through hole is equal to or less than 30nm. A size difference between a top aperture and a bottom aperture of the second through hole is equal to or less than 30nm.

[0023] Another aspect of the present disclosure provides a three-dimensional (3D) memory device, including a first stacked layer disposed on a substrate, a first insulating connection layer disposed on the first stacked layer, a second stacked layer disposed on the first insulating connection layer, a second insulating connection layer disposed on the second stacked layer, a plurality of channel holes in a first region of the 3D memory device, a plurality of staircase structure dummy holes in a second region of the 3D memory device, and a plurality of through array contact barriers in a third region of the 3D memory device. Each of the plurality of channel holes includes the disclosed joint opening structure.

[0024] Other aspects of the present disclosure can be understood by those skilled in the art in light of the description, the claims, and the drawings of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] Various objectives, features, and advantages of the present disclosure can be more fully appreciated with reference to the detailed description of the present disclosure when considered in contact with the following drawings, in which like reference numerals identify like elements. It is noted that the following drawings are merely examples for illustrative purposes according to various disclosed embodiments and are not intended to limit the scope of the present disclosure.

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[0026] FIGs. 1-6, 7A, 7B, 8A, 8B, 9A, 9B, 10A, 10B, 11A, 11B, 12-20, 21A, 21B, 22A and 22B illustrate schematic structural cross-sectional diagrams of an exemplary joint opening structure of three-dimensional (3D) memory device at certain stages of a fabricating process in accordance with some embodiments of the present disclosure;

[0027] FIGs. 23A and 23B illustrate schematic flow diagrams of an exemplary fabricating process for forming a joint opening structure of three-dimensional (3D) memory device are illustrated in accordance with some embodiments of the present disclosure;

[0028] FIGs. 24-29, 30A, 30B, 31A, 31B, 32A, 32B, 33A, 33B, 34A, 34B, 35-47, 48A, 48B, 49A and 49B illustrate schematic structural cross-sectional diagrams of another exemplary joint opening structure of three-dimensional (3D) memory device at certain stages of another fabricating process in accordance with some embodiments of the present disclosure;

[0029] FIGs. 50A and 50B illustrate schematic flow diagrams of another exemplary fabricating process for forming a joint opening structure of three-dimensional (3D) memory device are illustrated in accordance with some embodiments of the present disclosure;

[0030] FIGs. 51-55, 56A, 56B, 57A, 57B, 58A, 58B, 59A, 59B, 60-71, 72A, 72B, 73A and 73B illustrate schematic structural cross-sectional diagrams of another exemplary joint opening structure of three-dimensional (3D) memory device at certain stages of another fabricating process in accordance with some embodiments of the present disclosure;

[0031] FIGs. 74A and 74B illustrate schematic flow diagrams of another exemplary fabricating process for forming a joint opening structure of three-dimensional (3D) memory device are illustrated in accordance with some embodiments of the present disclosure;

[0032] FIGs. 75-79, 80A, 80B, 81A, 81B, 82A, 82B, 83A, 83B, 84-100, 101A, 101B, 102A and 102B illustrate schematic structural cross-sectional diagrams of another exemplary joint opening structure of three-dimensional (3D) memory device at certain stages of another fabricating process in accordance with some embodiments of the present disclosure;

[0033] FIGs. 103A and 103B illustrate schematic flow diagrams of another exemplary fabricating process for forming a joint opening structure of three-dimensional (3D)

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memory device are illustrated in accordance with some embodiments of the present disclosure.

[0034] Embodiments of the present disclosure will be described with reference to the accompanying drawings.

DETAILED DESCRIPTION

[0035] Reference now be made in detail to exemplary embodiments of the invention, which are illustrated in the accompanying drawings in order to understand and implement the present disclosure and to realize the technical effect. It can be understood that the following description has been made only by way of example, but not to limit the present disclosure. Various embodiments of the present disclosure and various features in the embodiments that are not conflicted with each other can be combined and rearranged in various ways. Without departing from the spirit and scope of the present disclosure, modifications, equivalents, or improvements to the present disclosure are understandable to those skilled in the art and are intended to be encompassed within the scope of the present disclosure.

[0036] It is noted that references in the specification to "one embodiment," "an embodiment," "an example embodiment," "some embodiments," etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in contact with an embodiment, it would be within the knowledge of a person skilled in the pertinent art to effect such feature, structure or characteristic in contact with other embodiments whether or not explicitly described.

[0037] In general, terminology may be understood at least in part from usage in context. For example, the term "one or more" as used herein, depending at least in part upon context, may be used to describe any feature, structure, or characteristic in a singular sense or may be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as "a," "an," or "the," again, may be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context.

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[0038] It should be readily understood that the meaning of "on," "above," and "over" in the present disclosure should be interpreted in the broadest manner such that "on" not only means "directly on" something but also includes the meaning of "on" something with an intermediate feature or a layer therebetween, and that "above" or "over" not only means the meaning of "above" or "over" something but can also include the meaning it is "above" or "over" something with no intermediate feature or layer therebetween (i.e., directly on something).

[0039] Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper," and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0040] As used herein, the term "substrate" refers to a material onto which subsequent material layers are added. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.

[0041] As used herein, the term "layer" refers to a material portion including a region with a thickness. A layer can extend over the entirety of an underlying or overlying structure, or may have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend horizontally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow. A layer can include multiple layers. For example, an interconnect layer can include one or more conductor and contact layers (in which contacts, interconnect lines, and/or through holes are formed) and one or more dielectric layers.

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[0042] As used herein, the term "nominal/nominally" refers to a desired, or target, value of a characteristic or parameter for a component or a process operation, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term "about" indicates the value of a given quantity that can vary based on a particular technology node associated with the subject semiconductor device. Based on the particular technology node, the term "about" can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., ±10%, ±20%, or ±30% of the value).

[0043] In accordance with some embodiments of the present disclosure, joint opening structures of three-dimensional (3D) memory devices and method for forming the same are provided to reduce the process difficulty and cost of the channel hole structures in 3D memory devices.

[0044] As used herein, the term "3D memory device" refers to a semiconductor device with vertically oriented strings of memory cell transistors (referred to herein as "memory strings," such as NAND strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate. As used herein, the term "vertical/vertically" means nominally perpendicular to the lateral surface of a substrate, while the term "horizontal/horizontally" means nominally parallel to the lateral surface of a substrate.

[0045] Referring to FIGs. 23A and 23B, schematic flow diagrams of an exemplary fabricating process for forming a joint opening structure of three-dimensional (3D) memory device are illustrated in accordance with some embodiments of the present disclosure. And FIGs. 1-6, 7A, 7B, 8A, 8B, 9A, 9B, 10A, 10B, 11A, 11B, 12-20, 21A, 21B, 22A and 22B illustrate schematic structural cross-sectional diagrams of an exemplary joint opening structure of three-dimensional (3D) memory device at certain stages of the fabricating process shown in FIGs. 23A and 23B.

[0046] As shown in FIG. 23A, at S101, a first stacked layer 2 and a first insulating connection layer 3 can be sequentially formed on the surface of a substrate 1.

[0047] As shown in FIG. 1, the first stacked layer 2 can be formed on the substrate 1. The first stacked layer 2 can include a plurality of oxide/nitride layer pairs. The plurality of oxide/nitride layer pairs are also referred to herein as an "alternating oxide/nitride stack." That is, in the first stacked layer 2, multiple oxide layers (shown in the areas with

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dotes) and multiple nitride layers (shown in the areas with meshes) alternate in a vertical direction. In other words, except a top and a bottom layer of a given stack, each of the other oxide layers can be sandwiched by two adjacent nitride layers, and each nitride layer can be sandwiched by two adjacent oxide layers.

[0048] Oxide layers can each have the same thickness or have different thicknesses. For example, a thickness of each oxide layer can be in a range from 90nm to 160nm, preferably about 150nm. Similarly, nitride layers can each have the same thickness or have different thicknesses. For example, a thickness of each nitride layer can be in a range from 80nm to 110nm, preferably about 100nm.

[0049] It is noted that, in the present disclosure, the oxide layers and/or nitride layers can include any suitable oxide materials and/or nitride materials. For example, the element of the oxide materials and/or nitride materials can include, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof. In some embodiments, the oxide layers can be silicon oxide layers, and the nitride layers can be silicon nitride layer.

[0050] The first stacked layer 2 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide layers and the nitride layers in the first stacked layer 2 is equal to or larger than 64. In some embodiments, alternating conductor/dielectric stack includes more oxide layers or more nitride layers with different materials and/or thicknesses than the oxide/nitride layer pair.

[0051] The first insulating connection layer 3 can be formed on the first stacked layer 2. In some embodiments, the first insulating connection layer 3 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is noted that, the material of the first insulating connection layer 3 can be different from the material of the nitride layer in the first stacked layer 2.

[0052] Further, in some embodiments, a first mask layer 4 can be formed on the top surface of the first insulating connection layer 3. The first mask layer 4 can include a nitride layer on the top surface of the first insulating connection layer 3, and an oxide layer on the top surface of such nitride layer.

[0053] In some embodiments, the first stacked layer 2, the first insulating connection layer 3, and/or the first mask layer 4 can be formed by using one or more deposition processes. It is noted that, the term "deposition process" used in the present disclosure can be referred to any suitable deposition process including, but not limited to, a chemical

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vapor deposition (CVD) process, a physical vapor deposition (PVD) process, an atomic layer deposition (ALD) process, and/or any suitable combination thereof.

[0054] At S102, a first through hole 5 can be formed. As shown in FIG. 1, the first through hole 5 can completely penetrate the first stacked layer 2 and the first insulating connection layer 3, and can extend into the surface of the substrate 1.

[0055] In some embodiments, the first through hole 5 can be formed by etching the first stacked layer 2 and the first insulating connection layer 3 and a subsequent cleaning process. The etching process to form the first through hole 5 can be a wet etching, a dry etching, or a combination thereof.

[0056] In some embodiments, when the first mask layer 4 is formed on the top surface of the first insulating connection layer 3, the etching process also etch the first mask layer 4 to form the first through holes 5.

[0057] At S103, a first channel structure 6 can be formed on the surface of the substrate 1 that is exposed by the first through hole 5, as shown in FIG. 2. In some embodiments, the first channel structure 6 can be a polycrystalline silicon (polysilicon) layer formed by using a selective epitaxial process.

[0058] In some embodiments, the first channel structure 6 may not directly formed on the surface of the substrate 1. One or more layers can be formed between the first channel structure 6 and the substrate 1. That is, the first channel structure 6 is overlay the substrate 1.

[0059] At S104, a first functional layer can be formed on the sidewall of the first through hole 5. The first functional layer can include a first tunneling layer 7, a first storage layer 8, a first barrier layer 9, and a first passivation layer 10.

[0060] As shown in FIG. 3, the first tunneling layer 7 can be formed on the sidewall of the first through hole 5 and the top surface of the first channel structure 6. The first tunneling layer 7 can be used for generating electronic charges (electrons or holes). In some embodiments, the first tunneling layer 7 can be an oxide layer formed by using a deposition process.

[0061] The first storage layer 8 can be formed on the surface of the first tunneling layer 7. The first storage layer 8 can be used for storing electronic charges. The storage or removal of charge in the first storage layer 7 can impact the on/off state and/or a conductance of the semiconductor channel. The first storage layer 7 can include

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polycrystalline silicon (polysilicon) or silicon nitride. In some embodiments, the first storage layer 8 can be a nitride layer formed by using a deposition process.

[0062] The first barrier layer 9 can be formed on the surface of the first storage layer 8. The first barrier layer 9 can be used for blocking the outflow of the electronic charges stored in the first storage layer 8. In some embodiments, the first barrier layer 9 can be a silicon oxide layer or a combination of silicon oxide/silicon nitride/silicon oxide (ONO) layers. In some embodiments, the first barrier layer 9 includes high dielectric constant (high-k) dielectrics (e.g., aluminum oxide). In one example, the first barrier layer 9 is an oxide layer formed by using a deposition process.

[0063] As shown in FIG. 4, a first passivation layer 10 can be formed on the surface of the first barrier layer 9. The first passivation layer 10 can be used for protecting the first barrier layer 9 from being damaged in a subsequent removal process. In some embodiments, the first passivation layer 10 can be an amorphous silicon layer formed by using a deposition process.

[0064] The portions of the first passivation layer 10, the first barrier layer 9, the first storage layer 8 and the first tunneling layer 7 located on the top surface of the first channel structure 6 on the bottom of the first through hole 5 can be removed. In some embodiments, the removal process can include an etching process and a cleaning process. As such, the first functional layer can be formed on the sidewall of the first through hole 5.

[0065] In some embodiment, in the same removal process, the first barrier layer 9, the first storage layer 8, the first tunneling layer 7, and the oxide layer of the first mask layer 4 located on the surface of the nitride layer of first mask layer 4 can also be removed. As such, the nitride layer of first mask layer 4 is remained on the surface of the first insulating connection layer 3.

[0066] At S105, a second channel structure and a first filling structure can be sequentially formed on the sidewall of the first functional layer and the exposed surface of the first channel structure 6. The surfaces of the second channel structure and the first filling structure can be lower than the surface of the first insulating connection layer 3.

[0067] As shown in FIG. 5, a second channel layer 11 can be formed to cover the sidewall of the first passivation layer 10, the bottom surface of the first through hole 5. The second channel layer 11 can also cover the top surface of the first insulating connection layer 3, or cover the top surface of the nitride layer of the first mask layer 4.

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In some embodiments, the second channel layer 11 can be an amorphous silicon layer formed by using a deposition process.

[0068] As shown in FIG. 6, a first filling layer 12 can be formed to cover the second channel layer 11 and fill the first through hole 5. In some embodiments, the first filling layer 12 can be an oxide layer formed by using a deposition process. In some embodiments, the first filling layer 12 can include one or more airgaps.

[0069] As shown in FIGs. 7A and 7B, a portion of the first filling layer 12 can be removed, so that the top surface of the first filling layer 12 can be lower than the top surface of the first insulating connection layer 3. As such, the remaining portion of the first filling layer 12 in the first through hole 5 can form the first filling structure. In some embodiments, the portion of the first filling layer 12 can be removed by using an etching process. It is noted that, the term "etching process" used in the present disclosure can be referred to any suitable etching process including, but not limit to, a wet etching, a dry etching, or a combination thereof.

[0070] In some embodiments, as shown in FIG. 7A, the top surface of the first filling layer 12 can be higher than the top surface of the second stacker layer 2. For example, the top surface of the first filling layer 12 can be 20nm to 40nm higher than the top surface of the top nitride layer of the second stacker layer 2. Preferably, the top surface of the first filling layer 12 can be about 30nm higher than the top surface of the top nitride layer of the second stacker layer 2.

[0071] In some alternative embodiments, as shown in FIG. 7B, the top surface of the first filling layer 12 can be lower than the top surface of the second stacker layer 2. For example, the top surface of the first filling layer 12 can be 30nm to 40nm lower than the top surface of the top nitride layer of the second stacker layer 2. Preferably, the top surface of the first filling layer 12 can be about 35nm lower than the top surface of the top nitride layer of the second stacker layer 2.

[0072] As shown in FIGs. 8A and 8B, a portion of the second channel layer 11 can be removed, such that the surface of the second channel layer 11 is lower than the first insulating connection layer 3. The remaining portion of the second channel layer 11 can form the second channel structure that is in contact with the first channel structure 6. In some embodiments, the portion of the second channel layer 11 can be removed by using an etching process.

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[0073] It is noted that, in various embodiments, the top surface of the second channel structure can be higher or lower than the top surface of the first stacked layer 2. However, the top surface of the second channel structure is not lower than the top surface of the top oxide layer in the first stacked layer 2. In some embodiments, the top surface of the second channel structure can be higher than the top nitride layer in the first stacked layer 2, as shown in FIG. 8A. In some alternative embodiments, the top surface of the second channel structure is in a same plane of the top surface of the top oxide layer in the first stacked layer 2, as shown in FIG. 8B.

[0074] At S106, a first groove can be formed in the first insulating connection layer 3. In some embodiments, the projection of the first groove on the substrate 1 can completely cover the projection of the first through hole 5 on the substrate 1.

[0075] As shown in FIGs. 9A and 9B, the nitride layer of the first mask layer 4 can be removed. In some embodiments, the nitride layer of the first mask layer 4 can be removed by using an etching process.

[0076] As shown in FIGs. 10A and 10 B, the surface of the first insulating connection layer 3 can be planarized by using any suitable techniques, such as backside grinding, and/or chemical mechanical polishing (CMP). A portion of the first insulating connection layer 3 can be removed to form the first groove that penetrates the first insulating connection layer 3. An area of the projection "x" of the first groove on the substrate 1 can be larger than an area of the projection "y" of the first through hole 5 on the substrate 1.

[0077] In some embodiments, a depth of the first groove can be equal to or less than the thickness of the planarized first insulating connection layer 3, as shown in FIG. 10A. For example, the depth of the first groove can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 3 is about 90nm, while the depth of the first groove is about 60nm.

[0078] In some alternative embodiments, the depth of the first groove can be greater than the thickness of the planarized first insulating connection layer 3, as shown in FIG. 10B. That is, a portion of the top nitride layer in the first stacked layer 2 can also be removed to form the first groove. For example, the depth of the first groove can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 3 is about 30nm, while the depth of the first groove is about 60nm.

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[0079] At S107, a third channel structure 14 can be formed in the first groove 13. As shown in FIGs. 11A and 11B, the third channel structure 14 can be in contact with the second channel structure. In some embodiments, the third channel structure can be a polycrystalline silicon player formed by using a deposition process.

[0080] A thickness of the third channel structure 14 can be equal to the depth of the first groove 13. As described above, in some embodiments, a thickness of the third channel structure 14 can be equal to or less than the thickness of the planarized first insulating connection layer 3, as shown in FIG. 11A. For example, the thickness of the third channel structure 14 can be in a range between 50nm and 70nm, preferably about 60nm. In some alternative embodiments, the thickness of the third channel structure 14 can be greater than the thickness of the planarized first insulating connection layer 3, as shown in FIG. 11B. For example, the thickness of the third channel structure 14 can be in a range between 60nm and 80nm, preferably about 70nm.

[0081] Referring to FIG. 23B, at S108, a second stacked layer 15 and a second insulating connection layer 16 can be sequentially formed on the third channel structure 14. As shown in FIG. 12, the second stacked layer 15 can include a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs. Similar to the first stacked layer 2 as described above, the multiple oxide layers (shown in the areas with dotes) and multiple nitride layers (shown in the areas with meshes) in the second stacked layer 15 alternate in a vertical direction. The second stacked layer 15 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide layers and the nitride layers in the second stacked layer 15 is equal to or larger than 64.

[0082] In some embodiments, the second insulating connection layer 16 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is noted that, the material of the second insulating connection layer 16 can be different from the material of the nitride layer in the second stacked layer 15.

[0083] Further, in some embodiments, a second mask layer 17 can be formed on the surface of the second insulating connection layer 16. The second mask layer 17 can include a nitride layer on the surface of the second insulating connection layer 16, and an oxide layer on the surface of such nitride layer.

[0084] At S109, a second through hole 18 is formed. As shown in FIG. 13, the second through hole 18 can completely penetrate the second stacked layer 15 and the second

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insulating connection layer 16, and can extend into the surface of the third channel structure 14. The projection of the second through hole 18 on the substrate 1 can at least partially overlap with the projection of the first through hole 5 on the substrate 1.

[0085] In some embodiments, the second stacked layer 15, the second insulating connection layer 16, the second mask layer 17, and the third channel structure 14 can be etched to form the second through hole 18. The second stacked layer 15, the second insulating connection layer 16, the second mask layer 17, and/or the third channel structure 14 can be etched by using a dry etching process, a wet etching process, or a combination thereof. A cleaning process can then be performed to clean the second through hole 18.

[0086] It is noted that, the second through hole 18 can extend to the surface of the third channel structure 14, or can extend into the third channel structure 14. As such, a fourth channel structure formed subsequently in the second through hole 18 can directly contact the third channel structure.

[0087] In some embodiments, a maximum difference between the radius of the top aperture of each second through hole 18 and the radius of the bottom aperture of the second through hole 18 can be 15nm. That is, as shown in FIG. 13, a distance "a" between the boundary line of the top surface of each second through hole 18 and the boundary of the bottom surface of the second through hole 18 can be no more than 15 nm.

[0088] At S1010, a second functional layer can be formed on the sidewall of the second through hole 18. In some embodiments, the second functional layer can include a second tunneling layer 19, a second storage layer 20, a second barrier layer 21, and a second passivation layer 22.

[0089] As shown in FIG. 14, the second tunneling layer 19 can be formed on the sidewall of the second through hole 18 and the surface of the second channel structure 14. The second tunneling layer 19 can be used for generating electronic charges. In some embodiments, the second tunneling layer 19 can be an oxide layer formed by using a deposition process.

[0090] The second storage layer 20 can be formed on the surface of the second tunneling layer 19. The second storage layer 20 can be used for storing electronic charges. In some embodiments, the second storage layer 20 can be a nitride layer formed by using a deposition process.

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[0091] The second barrier layer 21 can be formed on the surface of the second storage layer 20. The second barrier layer 21 can be used for blocking the outflow of the electronic charges in the second storage layer 20. In some embodiments, the second barrier layer 21 can be an oxide layer formed by using a deposition process.

[0092] As shown in FIG. 15, a second passivation layer 22 can be formed on the surface of the second barrier layer 21. The second passivation layer 22 can be used for protecting the second barrier layer 21 from being damaged in a subsequent removal process. In some embodiments, the second passivation layer 22 can be an amorphous silicon layer formed by using a deposition process.

[0093] As shown in FIG. 15, the portions of the second passivation layer 22, the second barrier layer 21, the second storage layer 20 and the second tunneling layer 19 that are located on the surface of the second channel structure 14 can be removed. In some embodiments, the removal process can include an etching process and a cleaning process. In some embodiments, the portions of the second passivation layer 22, the second barrier layer 21, the second storage layer 20, the second tunneling layer 19, the oxide layer of the second mask layer 17 that are located on the nitride layer of the second mask layer 17 can also be removed by using an etching process. As such, the second functional layer can be formed on the sidewall of the second through hole 18.

[0094] At S1012, a fourth channel structure and a second filling structure can be sequentially formed on the sidewall of the second functional layer and the exposed surface of the third channel structure. In some embodiments, the top surface of the fourth channel structure can be higher than the top surface of the second filling structure.

[0095] As shown in FIG. 16, a fourth channel layer 23 can be formed to cover the sidewall of the second passivation layer 22 and the bottom surface of the second through hole 18. In some embodiments, the fourth channel layer 23 can also cover the surface of the second insulating connection layer 16, or the surface of the nitride layer of the second mask layer 17. In some embodiments, the fourth channel layer 23 can be an amorphous silicon layer formed by using a deposition process.

[0096] As shown in FIG. 17, a second filling layer 29 can be formed to cover the fourth channel layer 23 and to fill the second through hole 18. In some embodiments, the second filling layer 29 can be an oxide layer formed by using a deposition process.

[0097] As shown in FIG. 18, a portion of the second filling layer 29 can be removed, such that the surface of the second filling layer 29 is lower than the surface of the second

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insulating connection layer 16. In some embodiments, the removal process can include an etching process. The remaining portion of the second filling layer 29 in the second through hole 18 can form the second filling structure.

[0098] As shown in FIG. 19, the portion of the fourth channel layer 23 located on the surface of the second insulating connection layer 16 or the surface of the second mask layer 17 can be removed. In some embodiments, the removal process can include an etching process. The remaining portion of the fourth channel layer 23 in the second through hole 18 can form the fourth channel structure. The top surface of the fourth channel structure can be higher than the top surface of the second filling structure. As such, a second groove can be formed on the fourth channel structure and the second filling structure, and in the second through hole 18.

[0099] It is noted that, the top surface of the fourth channel structure can be higher than the top surface of the second stacked layer 15, or can be lower than the top surface of the second stacked layer 15. The top surface of the fourth channel structure is not lower than the top surface of the top oxide layer in the second stacked layer 15. In some embodiments, the top surface of the fourth channel structure can be in a same plane of the top surface of the top oxide layer in the second stacked layer 15.

[00100] At S1013, a fifth channel structure can be formed in the second groove. The fifth channel structure can be in contact with the fourth channel structure. As shown in FIG. 20, the fifth channel structure 30 can be formed in the second groove that is on the fourth channel structure and the second filling structure and in the second through hole 18. The nitride layer of the second mask layer 17 can be then removed by an etching process.

[00101] As shown in FIGs. 21A and 21B, the top surface of the second insulating connection layer 16 and the top surface of the fifth channel structure 30 can be planarized by any suitable techniques, such as backside grinding, and/or chemical mechanical polishing (CMP).

[00102] Accordingly, the disclosed method as shown in FIGs. 23A and 23B can form a joint opening structure of a three-dimensional (3D) memory device by combining two through hole formation processes. As such, the formed channel hole having the joint opening structure can have a large aspect ratio and a limited top-bottom aperture error. Further, the disclosed method of forming a joint opening structure in a 3D memory device can result in an efficient process capability control, a simplified process complexity, and a reduced cost.

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[00103] In some embodiments, the present disclosure also provides a three-dimensional memory device formed by using the above disclosed method as shown in FIGs. 23A and 23B. The three-dimensional memory can include the following components described below.

[00104] A first stacked layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer silicon nitride layer pairs, is formed on a substrate. A first insulating connection layer is formed on the first stacked layer. A first through hole penetrates the first stacked layer and the first insulating connection layer, and extends into the surface of the substrate.

[00105] A first channel structure is formed on the surface of the substrate exposed by the first through hole. A first functional layer is formed on the sidewall of the first through hole. A second channel structure is formed on the sidewall of the first functional layer and the surface of the first channel structure. A first filling structure is formed on the sidewall and the surface of the second channel structure to fill the first through hole. In some embodiments, an airgap is enclosed in the first filling structure. The top surfaces of the second channel structure and the first filling structure are lower than the top surfaces of the first insulating connection layer.

[00106] A first groove is formed in the first insulating connection layer, and above the first functional layer, the second channel structure and the first filling structure. A projection of the first groove on the substrate completely covers a projection of the first through hole on the substrate. A third channel structure in contact with the second channel structure is formed in the first groove.

[00107] A second stack layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs, is formed on the top surfaces of the first insulating connection layer and the third channel structure. A second insulating connection layer is formed on the second stack layer. A second through hole penetrates through the second stacked layer and the second insulating connection layer, and extends into a surface of the third channel structure. A projection of the second through hole on the substrate at least partially overlaps the projection of the first through hole on the substrate.

[00108] A second functional layer is formed on the sidewall of the second through hole. A fourth channel structure is formed on the sidewall of the second functional layer and the bottom surface of the second through hole. A second filling structure is formed on the

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sidewall and the surface of the fourth channel structure to fill the second through hole. In some embodiments, an airgap is enclosed in the second filling structure. The top surface of the fourth channel structure is higher than the top surface of the second filling structure. A fifth channel structure in contact with the fourth channel structure is formed in a second groove that is surrounded by the second functional layer, and above the fourth channel structure and the second filling structure.

[00109] In some embodiments, as shown in FIG. 21A, a thickness "b" of the first insulating connection layer, which is the distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 80nm and 100nm, preferably about 90nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00110] In some alternative embodiments, as shown in FIG. 21B, a thickness "b" of the first insulating connection layer, which is the distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 20nm and 40nm, preferably about 30nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00111] Further, the difference between the radiuses of the top aperture and the bottom aperture of the second channel structure, and the difference between the radiuses of the top aperture and the bottom aperture of the fourth channel structure can be within 15nm. Accordingly, the disclosed channel hole having a joint opening structure can have a large aspect ratio and a limited top-bottom aperture error.

[00112] In some embodiments, a replacement process can be performed to replace each of the plurality of nitride layers in the first stacked layer 2 and the second stacked layer 15 with a conductive layer 40, as shown in FIGs. 22A and 22B. The conductive layer can include any suitable material that is electronically conductive, including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof.

[00113] In some embodiments, during the replacement process, a portion of the third channel structure 14 that is adjacent with the bottom nitride layer of the second stacked layer 15, or is adjacent with the top nitride layer of the first stacked layer 2 can be converted to an oxide layer by an oxidation process. For example, an etching process can be performed to remove all nitride layers in the first stacked layer 2 and the second stacked layer 15. Then an oxide process can be formed to oxide the exposed surface of the third channel structure. As a result, a portion of the third channel structure can be

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converter to the oxide layer as shown in FIGs. 22A and 22B. In some embodiments,, a thickness "c" of the third channel structure can be reduced after the replacement process. For example, the thickness "c" of the third channel structure can be reduced to a range between 30nm and 50nm, preferably about 40nm.

[00114] Referring to FIGs. 50A and 50B, schematic flow diagrams of another exemplary fabricating process for forming a joint opening structure of three-dimensional (3D) memory device are illustrated in accordance with some other embodiments of the present disclosure. And FIGs. 24-29, 30A, 30B, 31A, 31B, 32A, 32B, 33A, 33B, 34A, 34B, 35-47, 48A, 48B, 49A and 49B illustrate schematic structural cross-sectional diagrams of an exemplary joint opening structure of three-dimensional (3D) memory device at certain stages of the fabricating process shown in FIGs. 50A and 50B.

[00115] As shown in FIG. 50A, at S201, a first stacked layer 202 and a first insulating connection layer 203 can be sequentially formed on the surface of a substrate 201. In some embodiments, the 3D memory device can include a first region 100, a second region 200, and a third region 300, as shown in FIG. 24. The first region 100 can be used to form one or more channel holes, the second region 200 can be used to form one or more staircase structure (SS) dummy holes, while the third region 300 can be used to form one or more through array contact (TAC) barriers.

[00116] As shown in FIG. 24, the first stacked layer 202 can be formed on the substrate 201. The first stacked layer 202 can include a plurality of oxide/nitride layer pairs. That is, in the first stacked layer 202, multiple oxide layers (shown in the areas with dotes) and multiple nitride layers (shown in the areas with meshes) alternate in a vertical direction. In other words, except a top and a bottom layer of a given stack, each of the other oxide layers can be sandwiched by two adjacent nitride layers, and each nitride layer can be sandwiched by two adjacent oxide layers.

[00117] Oxide layers can each have the same thickness or have different thicknesses. For example, a thickness of each oxide layer can be in a range from 90nm to 160nm, preferably about 150nm. Similarly, nitride layers can each have the same thickness or have different thicknesses. For example, a thickness of each nitride layer can be in a range from 80nm to 110nm, preferably about 100nm. In some embodiments, the oxide layers can be silicon oxide layers, and the nitride layers can be silicon nitride layer.

[00118] The first stacked layer 202 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide

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layers and the nitride layers in the first stacked layer 202 is equal to or larger than 64. In some embodiments, alternating conductor/dielectric stack includes more oxide layers or more nitride layers with different materials and/or thicknesses than the oxide/nitride layer pair.

[00119] The first insulating connection layer 203 can be formed on the first stacked layer 202. In some embodiments, the first insulating connection layer 203 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is noted that, the material of the first insulating connection layer 203 can be different from the material of the nitride layer in the first stacked layer 202.

[00120] Further, in some embodiments, a first mask layer 204 can be formed on the surface of the first insulating connection layer 203. The first mask layer 204 can include a nitride layer on the surface of the first insulating connection layer 203, and an oxide layer on the surface of such nitride layer.

[00121] In some embodiments, the first stacked layer 202, the first insulating connection layer 203, and/or the first mask layer 204 can be formed by using one or more deposition processes, such as one or more chemical vapor deposition (CVD) processes, one or more physical vapor deposition (PVD) processes, one or more atomic layer deposition (ALD) processes, and/or any suitable combinations thereof.

[00122] At S202, one or more first through holes 205 can be formed in each of the first region 100, the second region 200, and the third region 300. As shown in FIG. 24, each of the one or more first through holes 205 can completely penetrate the first stacked layer 202 and the first insulating connection layer 203, and can extend into the surface of the substrate 201. In some embodiments, when the first mask layer 204 is formed on the surface of the first insulating connection layer 203, the etching process also etch the first mask layer 204 to form the first through holes 205.

[00123] In some embodiments, the first through holes 205 can be formed by etching the first stacked layer 202 and the first insulating connection layer 203 and a subsequent cleaning process. The etching process to form the first through holes 205 can be a wet etching, a dry etching, or a combination thereof. It is noted that, in the direction perpendicular to the surface of the substrate 201, the depth of the one or more first through holes 205 in the third region 300 can be larger than the depth of the one or more first through holes 205 in the first region 100.

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[00124] At S203, a first channel structure 206 can be formed on the surface of the substrate 201 that is exposed by each of the plurality of first through holes 205, as shown in FIG. 25. In some embodiments, the first channel structure 206 can be a polycrystalline silicon (polysilicon) layer formed by using a selective epitaxial process.

[00125] At S204, a first functional layer can be formed on the sidewall of each of the plurality of first through holes 205. The first functional layer can include a first tunneling layer 207, a first storage layer 208, a first barrier layer 209, and a first passivation layer 210.

[00126] As shown in FIG. 26, the first tunneling layer 207 can be formed on the sidewall of the plurality of first through holes 205 and the exposed surfaces of the first channel structures 206. The first tunneling layer 207 can be used for generating electronic charges (electrons or holes). In some embodiments, the first tunneling layer 207 can be an oxide layer formed by using a deposition process.

[00127] The first storage layer 208 can be formed on the surface of the first tunneling layer 207. The first storage layer 208 can be used for storing electronic charges. The storage or removal of charge in the first storage layer 207 can impact the on/off state and/or a conductance of the semiconductor channel. The first storage layer 207 can include polycrystalline silicon (polysilicon) or silicon nitride. In some embodiments, the first storage layer 208 can be a nitride layer formed by using a deposition process.

[00128] The first barrier layer 209 can be formed on the surface of the first storage layer 208. The first barrier layer 209 can be used for blocking the outflow of the electronic charges stored in the first storage layer 208. In some embodiments, the first barrier layer 209 can be a silicon oxide layer or a combination of silicon oxide/silicon nitride/silicon oxide (ONO) layers. In some embodiments, the first barrier layer 209 includes high dielectric constant (high-k) dielectrics (e.g., aluminum oxide). In one example, the first barrier layer 209 is an oxide layer formed by using a deposition process.

[00129] As shown in FIG. 27, a first passivation layer 210 can be formed on the surface of the first barrier layer 209. The first passivation layer 210 can be used for protecting the first barrier layer 209 from being damaged in a subsequent removal process. In some embodiments, the first passivation layer 210 can be an amorphous silicon layer formed by using a deposition process.

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[00130] The portions of the first passivation layer 210, the first barrier layer 209, the first storage layer 208 and the first tunneling layer 207 located on the surfaces of the plurality of first channel structures 206 on the bottom of the plurality of first through holes 205 can be removed. In some embodiments, the removal process can include an etching process and a cleaning process. As such, the first functional layer can be formed on the sidewalls of the plurality of first through holes 205.

[00131] In some embodiment, in the same removal process, the first barrier layer 209, the first storage layer 208, the first tunneling layer 207, and the oxide layer of the first mask layer 204 located on the surface of the nitride layer of first mask layer 204 can also be removed. As such, the nitride layer of first mask layer 204 is remained on the surface of the first insulating connection layer 203.

[00132] At S205, a second channel structure and a first filling structure can be sequentially formed on the sidewall of the first functional layer and the exposed surface of the first channel structure 206 in each of the plurality of first through holes 205. The surfaces of the second channel structure and the first filling structure can be lower than the surface of the first insulating connection layer 203.

[00133] As shown in FIG. 28, a second channel layer 211 can be formed to cover the sidewalls of the first passivation layer 210 and the bottom of each of the plurality of first through holes 205. The second channel layer 211 can also cover the surface of the first insulating connection layer 203, or cover the surface of the nitride layer of the first mask layer 204. In some embodiments, the second channel layer 211 can be an amorphous silicon layer formed by using a deposition process.

[00134] As shown in FIG. 29, a first filling layer 212 can be formed to cover the second channel layer 211 and fill each of the plurality of first through holes 205. In some embodiments, the first filling layer 212 can be an oxide layer formed by using a deposition process.

[00135] As shown in FIGs. 30A and 30B, a portion of the first filling layer 212 can be removed, such that the top surface of the first filling layer 212 can be lower than the top surface of the first insulating connection layer 203. As such, the remaining portion of the first filling layer 212 in each of the plurality of first through holes 205 can form the first filling structure. In some embodiments, the portion of the first filling layer 212 can be removed by using an etching process, such as a wet etching, a dry etching, or a combination thereof.

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[00136] In some embodiments, as shown in FIG. 30A, the top surface of the first filling layer 212 can be higher than the top surface of the second stacker layer 202. For example, the top surface of the first filling layer 212 can be 20nm to 40nm higher than the top surface of the top nitride layer of the second stacker layer 202. Preferably, the top surface of the first filling layer 212 can be about 30nm higher than the top surface of the top nitride layer of the second stacker layer 202.

[00137] In some alternative embodiments, as shown in FIG. 30B, the top surface of the first filling layer 212 can be lower than the top surface of the second stacker layer 202. For example, the top surface of the first filling layer 212 can be 30nm to 40nm lower than the top surface of the top nitride layer of the second stacker layer 202. Preferably, the top surface of the first filling layer 212 can be about 35nm lower than the top surface of the top nitride layer of the second stacker layer 202.

[00138] As shown in FIGs. 31A and 31B, a portion of the second channel layer 211 can be removed, such that the surface of the second channel layer 211 is lower than the first insulating connection layer 203. The remaining portion of the second channel layer 211 can form the second channel structure that is in contact with the first channel structure 206. In some embodiments, the portion of the second channel layer 211 can be removed by using an etching process.

[00139] It is noted that, in various embodiments, the top surface of the second channel structure can be higher than the top surface of the first stacked layer 202 or lower than the top surface of the first stacked layer 202. However, the top surface of the second channel structure is not lower than the top surface of the top oxide layer in the first stacked layer 202. In some embodiments, the top surface of the second channel structure can be higher than the top nitride layer in the first stacked layer 202, as shown in FIG. 31A. In some alternative embodiments, the top surface of the second channel structure is in a same plane of the top surface of the top oxide layer in the first stacked layer 202, as shown in FIG. 31B.

[00140] At S206, a first groove can be formed in the first insulating connection layer 203 above each of the plurality of first through holes 205. In some embodiments, the projection of the first groove on the substrate 201 can completely cover the projection of the corresponding first through hole 205 on the substrate 201.

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[00141] As shown in FIGs. 32A and 32B, the nitride layer of the first mask layer 204 can be removed. In some embodiments, the nitride layer of the first mask layer 204 can be removed by using an etching process.

[00142] As shown in FIGs. 33A and 33 B, the surface of the first insulating connection layer 203 can be planarized by any suitable techniques, such as backside grinding, and/or chemical mechanical polishing (CMP). A portion of the first insulating connection layer 203 can be removed to form a plurality of first grooves that penetrate the first insulating connection layer 203. An area of the projection of each of the plurality of first grooves on the substrate 201 can be larger than an area of the projection of each of the plurality of first through holes 205 on the substrate 201.

[00143] In some embodiments, a depth of the first groove can be equal to or less than the thickness of the planarized first insulating connection layer 203, as shown in FIG. 33A. For example, the depth of the first groove can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 203 is about 90nm, while the depth of the first groove is about 60nm.

[00144] In some alternative embodiments, the depth of the first groove can be greater than the thickness of the planarized first insulating connection layer 203, as shown in FIG. 33B. That is, a portion of the top nitride layer in the first stacked layer 202 can also be removed to form the first groove. For example, the depth of the first groove can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 203 is about 30nm, while the depth of the first groove is about 60nm.

[00145] At S207, a third channel structure 214 can be formed in each of the plurality of first grooves 213. As shown in FIGs. 34A and 34B, the third channel structure 214 can be in contact with the second channel structure in each of the plurality of first through holes 205. In some embodiments, the third channel structure can be a polycrystalline silicon player formed by using a deposition process.

[00146] A thickness of each third channel structure 214 can be equal to the depth of each first groove 213. As described above, in some embodiments, a thickness of each third channel structure 214 can be equal to or less than the thickness of the planarized first insulating connection layer 203, as shown in FIG. 34A. For example, the thickness of each third channel structure 214 can be in a range between 50nm and 70nm, preferably about 60nm. In some alternative embodiments, the thickness of each third channel

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structure 214 can be greater than the thickness of the planarized first insulating connection layer 203, as shown in FIG. 34B. For example, the thickness of each third channel structure 214 can be in a range between 60nm and 80nm, preferably about 70nm.

[00147] Referring to FIG. 50B, at S208, a second stacked layer 215 and a second insulating connection layer 216 can be sequentially formed on the plurality of third channel structures 214. As shown in FIG. 35, the second stacked layer 215 can include a plurality of oxide/nitride layer pairs, such as silicon oxide layers and silicon nitride layers. Similar to the first stacked layer 202 as described above, the multiple oxide layers (shown in the areas with dotes) and multiple nitride layers (shown in the areas with meshes) in the second stacked layer 215 alternate in a vertical direction. The second stacked layer 215 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide layers and the nitride layers in the second stacked layer 215 is equal to or larger than 64.

[00148] In some embodiments, the second insulating connection layer 216 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is noted that, the material of the second insulating connection layer 216 can be different from the material of the nitride layer in the second stacked layer 215.

[00149] Further, in some embodiments, a second mask layer 217 can be formed on the surface of the second insulating connection layer 216. The second mask layer 217 can include a nitride layer on the surface of the second insulating connection layer 216, and an oxide layer on the surface of such nitride layer.

[00150] At S209, one or more second through holes 218 are formed in each of the first region 100, the second region 200, and the third region 300. As shown in FIG. 36, each of the plurality of second through holes 218 can completely penetrate the second stacked layer 215, the second insulating connection layer 216, and the second mask layer 217, and can extend into the surface of the corresponding third channel structure 214. The projection of each second through hole 218 on the substrate 201 can at least partially overlap with the projection of the corresponding first through hole 205 on the substrate 201.

[00151] In some embodiments, the second stacked layer 215, the second insulating connection layer 216, the second mask layer 217, and the third channel structures 214 can be etched to form the plurality of second through holes 218 that penetrate the second stacked layer 215 and the second insulating connection layer 216. The second stacked

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layer 215, the second insulating connection layer 216, the second mask layer 217, and/or the third channel structure 214 can be etched by using a dry etching process, a wet etching process, or a combination thereof. A cleaning process can then be performed to clean the plurality of second through holes 218.

[00152] It is noted that, each second through hole 218 can extend to the surface of the corresponding third channel structure 214, or can extend into the corresponding third channel structure 214. As such, a fourth channel structure formed subsequently in each second through hole 218 can directly contact the corresponding third channel structure. It is also noted that, the one or more second through holes 218 in the third region 300 can also completely penetrate the corresponding third channel structures 214, as shown in FIG. 36. However, the one or more third channel structures 214 in the first region 100 are not completely penetrated by the one or more second through holes 218.

[00153] In some embodiments, a maximum difference between the radius of the top aperture of each second through hole 218 and the radius of the bottom aperture of the second through hole 218 can be 15nm. That is, as shown in FIG. 36, a distance "a" between the boundary line of the top surface of each second through hole 218 and the boundary of the bottom surface of the second through hole 218 can be no more than 15 nm.

[00154] At S2010, a second functional layer can be formed on the sidewall of each second through hole 218. In some embodiments, the second functional layer can include a second tunneling layer 219, a second storage layer 220, a second barrier layer 221, and a second passivation layer 222.

[00155] As shown in FIG. 37, the second tunneling layer 219 can be formed on the sidewall of each second through hole 218 and the surface of the corresponding third channel structure 214. The second tunneling layer 219 can be used for generating electronic charges. In some embodiments, the second tunneling layer 219 can be an oxide layer formed by using a deposition process.

[00156] The second storage layer 220 can be formed on the surface of the second tunneling layer 219. The second storage layer 220 can be used for storing electronic charges. In some embodiments, the second storage layer 220 can be a nitride layer formed by using a deposition process.

[00157] The second barrier layer 221 can be formed on the surface of the second storage layer 220. The second barrier layer 221 can be used for blocking the outflow of the

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electronic charges in the second storage layer 220. In some embodiments, the second barrier layer 221 can be an oxide layer formed by using a deposition process.

[00158] As shown in FIG. 38, a second passivation layer 222 can be formed on the surface of the second barrier layer 221. The second passivation layer 222 can be used for protecting the second barrier layer 221 from being damaged in a subsequent removal process. In some embodiments, the second passivation layer 222 can be an amorphous silicon layer formed by using a deposition process.

[00159] As shown in FIG. 38, the portions of the second passivation layer 222, the second barrier layer 221, the second storage layer 220 and the second tunneling layer 219 that are located on the surface of each third channel structure 214 can be removed. In some embodiments, the removal process can include an etching process and a cleaning process. In some embodiments, the portions of the second passivation layer 222, the second barrier layer 221, the second storage layer 220, the second tunneling layer 219, the oxide layer of the second mask layer 217 that are located on the nitride layer of the second mask layer 217 can also be removed by using an etching process. As such, the second functional layer can be formed on the sidewall of each second through hole 218.

[00160] At S2011, a fourth channel structure can be formed on the sidewall of the second functional layer and the exposed surface of the third channel structure in each second through hole 218 in the first region 100. Further, a second filling structure can be formed in each of the plurality of second through holes 218 in the first region 100, the second region 200, and the third region 300. In some embodiments, the top surface of the fourth channel structure can be higher than the top surface of the second filling structure.

[00161] As shown in FIG. 39, a fourth channel layer 223 can be formed to cover the sidewall of the second passivation layer 222 and the bottom surface of each of the plurality of second through holes 218 in the first region 100, the second region 200, and the third region 300. In some embodiments, the fourth channel layer 223 can also cover the top surface of the second insulating connection layer 216, or the top surface of the nitride layer of the second mask layer 217. In some embodiments, the fourth channel layer 223 can be an amorphous silicon layer formed by using a deposition process.

[00162] As shown in FIG. 40, a third filling layer 224 can be formed to cover the fourth channel layer 223. In some embodiments, the third filling layer 224 can include one or more airgaps in each second through hole 218. In some embodiments, the third filling layer 224 can be an oxide layer formed by using a deposition process.

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[00163] As shown in FIG. 41, a third mask layer 25 can be formed on the top surface of the third filling layer 224 in the first region 100. Using the third mask layer 225 as a mask, the portions of the third filling layer 224 located in the second region 200 and the third region 300 can be removed by using an etching process.

[00164] As shown in FIG. 42, the third mask layer 225 can be removed. Using the remaining third filling layer 224 in the first region 100 as a mask, the fourth channel layer 223 located in the second region 200 and the third region 300 can be removed by using an etching process.

[00165] As shown in FIG. 43, a fourth filling layer 227 can be formed on the surface of the second functional layer located in the second region 200 and the third region 300. In some embodiments, the filling performance of the fourth filling layer 227 can be better than the filling performance of the third filling layer 224. That is, in a same removing process, the removal rate of the fourth filling layer 227 can be less than the removal rate of the third filling layer 224.

[00166] As shown in FIG. 44, the third filling layer 224 on the surface of the fourth channel layer 223 in the first region 100 can be removed by using an etching process. It is noted that, a portion of the fourth filling layer 227 can also be removed by the same etching process.

[00167] As shown in FIG. 45, a second filling layer 229 can be formed in each second through hole 218 in the first region 100, the second region 200 and the third region 300. The material of the second filling layer 229 can be the same material of the fourth filling layer 227.

[00168] As shown in FIG. 46, a portion of the second filling layer 29 can be removed by using an etching process, such that the top surface of the second filling layer 229 in each second through hole 218 is lower than the top surface of the second insulating connection layer 216. The remaining portion of the second filling layer 29 in each second through hole 218 can form the second filling structure.

[00169] Further, the portion of the fourth channel layer 223 located on the surface of the second insulating connection layer 216 or the surface of the second mask layer 217 can be removed by using an etching process. The remaining portion of the fourth channel layer 223 in each second through hole 218 can form the fourth channel structure. The top surface of the fourth channel structure can be higher than the top surface of the second filling structure. As such, a second groove can be formed on the fourth channel structure

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and the second filling structure in each second through hole 218 in the first region 100, and on the second filling structure in each second through hole 218 in the second region 200 and the third region 300.

[00170] It is noted that, the top surface of the fourth channel structure can be higher than the top surface of the second stacked layer 215, or can be lower than the top surface of the second stacked layer 215. The top surface of the fourth channel structure is not lower than the top surface of the top oxide layer in the second stacked layer 215. In some embodiments, the top surface of the fourth channel structure can be in a same plane of the top surface of the top oxide layer in the second stacked layer 215.

[00171] At S2012, a fifth channel structure can be formed in the second groove of each second through hole 218 in the first region 100. The fifth channel structure can be in contact with the fourth channel structure.

[00172] As shown in FIG. 47, the fifth channel structure 230 can be formed in the second groove that is on the fourth channel structure and the second filling structure in each second through hole 218 in the first region 100. The fifth channel structure 230 can also be formed in the second groove that is on the second filling structure in each second through hole 218 in the second region 200 and the third region 300. The nitride layer of the second mask layer 217 can be then removed by an etching process.

[00173] As shown in FIGs. 48A and 48B, the top surface of the second insulating connection layer 216 and the top surface of the plurality of fifth channel structures 230 can be planarized by any suitable techniques, such as backside grinding, and/or chemical mechanical polishing (CMP).

[00174] Accordingly, the disclosed method as shown in FIGs. 50A and 50B can form another joint opening structure of a three-dimensional (3D) memory device by combining two through hole formation processes. As such, the formed channel holes having the joint opening structure can have a large aspect ratio and a limited top-bottom aperture error. Further, the disclosed method of forming a joint opening structure in a 3D memory device can simultaneously form a plurality of channel holes, staircase dummy holes, and through array contact barriers, resulting in an efficient process capability control, a simplified process complexity, and a reduced cost.

[00175] In some embodiments, the present disclosure also provides another three-dimensional memory device formed by using the above disclosed method as shown in FIGs. 50A and 50B. The three-dimensional memory device can include a first region for

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forming a plurality of channel holes, a second region for forming a plurality of staircase structure (SS) dummy holes, and a third region for forming a plurality of through array contact (TAC) barriers. Along a direction perpendicular to the surface of the three-dimensional memory device, the three-dimensional memory device can include the following components.

[00176] A first stacked layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs, is formed on a substrate. A first insulating connection layer is formed on the first stacked layer. A plurality of first through holes penetrating the first stacked layer and the first insulating connection layer and extending into the surface of the substrate are formed in the first region, the second region, and the third region.

[00177] A first channel structure is formed on the surface of the substrate exposed by each first through hole. A first functional layer is formed on the sidewall of each first through hole. A second channel structure is formed on the sidewall of the first functional layer and the surface of the first channel structure in each first through hole. A first filling structure is formed on the sidewall and the surface of the second channel structure to fill each of the plurality of first through holes. In some embodiments, an airgap can be enclosed in the first filling structure in each first through hole. The top surfaces of the second channel structure and the first filling structure are lower than the top surfaces of the first insulating connection layer.

[00178] A first groove is formed in the first insulating connection layer, and above the first functional layer, the second channel structure and the first filling structure in each first through hole. A projection of each of the plurality of first grooves on the substrate completely covers a projection of the corresponding first through hole on the substrate. A third channel structure in contact with the second channel structure in the corresponding first through hole is formed in each first groove.

[00179] A second stack layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs, is formed on the top surfaces of the first insulating connection layer and the plurality of third channel structures. A second insulating connection layer is formed on the second stack layer. A plurality of second through holes penetrating through the second stacked layer and the second insulating connection layer and extending into a surface of the third channel structure are formed in the first region, the second region, and the third region. A projection of each of the

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plurality of second through holes on the substrate at least partially overlaps the projection of the corresponding first through hole on the substrate.

[00180] A second functional layer is formed on the sidewall of each second through hole. A fourth channel structure is formed on the sidewall of the second functional layer and the bottom surface of each second through hole in the first region. A second filling is formed to fill each of the plurality of second through holes in the first region, the second region, and the third region. In some embodiments, an airgap can be enclosed in the second filling structure. The top surface of the fourth channel structure is higher than the top surface of the second filling structure in each second through hole in the first region.

[00181] In the first region, a fifth channel structure in contact with the fourth channel structure is formed in a second groove in each second through hole that is surrounded by the second functional layer, and above the fourth channel structure and the second filling structure. And in the second region and the third region, a fifth channel structure is formed in a second groove in each second through hole that is surrounded by the second functional layer, and above the second filling structure.

[00182] Due to the fourth channel structures being formed in the second through holes in the first region rather than the third region, the fifth channel structure in each second through hole in the first region can be electronically connected with the first channel structure in the corresponding first through hole, while the fifth channel structure in each second through hole in the third region can be electronically insulated with the first channel structure in the corresponding first through hole. Thus, in the three-dimensional memory device, a plurality of channel holes can be formed in the first region, and a plurality of through array contact (TAC) barriers can be formed in the third region. The plurality of staircase structure dummy holes in the second region can have a supporting function of the staircase structure.

[00183] In some embodiments, as shown in FIG. 48A, in each channel hole in the first region, a thickness "b" of the first insulating connection layer, which is the distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 80nm and 100nm, preferably about 90nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00184] In some alternative embodiments, as shown in FIG. 47B, in each channel hole in the first region, a thickness "b" of the first insulating connection layer, which is the

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distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 20nm and 40nm, preferably about 30nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00185] Further, the difference between the radiuses of the top aperture and the bottom aperture of the second channel structure, and the difference between the radiuses of the top aperture and the bottom aperture of the fourth channel structure can be within 15nm. Accordingly, the disclosed channel hole having a joint opening structure can have a large aspect ratio and a limited top-bottom aperture error.

[00186] In some embodiments, a replacement process can be performed to replace each of the plurality of nitride layers in the first stacked layer 202 and the second stacked layer 215 with a conductive layer 240, as shown in FIGs. 49A and 49B. The conductive layer can include any suitable material that is electronically conductive, including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof.

[00187] In some embodiments, the replacement process can be performed in one or more of the first region 100, the second region 200, and the third region 300. In one embodiments, the replacement process is performed in the first region 100 and the second region 200, but not in the third region 300. That is, the first stacked layer and the second stacked layer in the first region and the second region can be alternating conductive/dielectric stack, while the first stacked layer and the second stacked layer in the third region can be alternating oxide/nitride stack.

[00188] In some embodiments, during the replacement process, a portion of the third channel structure 214 that is adjacent with the bottom nitride layer of the second stacked layer 215, or is adjacent with the top nitride layer of the first stacked layer 202 can be converted to an oxide layer by an oxidation process. That is, as shown in FIGs. 49A and 49B, a thickness "c" of the third channel structure can be reduced after the replacement process. For example, the thickness "c" of the third channel structure can be reduced to a range between 30nm and 50nm, preferably about 40nm.

[00189] Referring to FIGs. 74A and 74B, schematic flow diagrams of another exemplary method for forming a joint opening structure of three-dimensional (3D) memory device are illustrated in accordance with some embodiments of the present disclosure. And FIGs. 51-55, 56A, 56B, 57A, 57B, 58A, 58B, 59A, 59B, 60-71, 72A, 72B, 73A and 73B illustrate schematic structural cross-sectional diagrams of an exemplary joint opening

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structure of three-dimensional (3D) memory device at certain stages of the fabricating process shown in FIGs. 74A and 74B.

[00190] At S301, a substrate 301 can be provided, a first stacked layer 302 and a first insulating connection layer 303 can be formed on the surface of the substrate 301. As shown in FIG. 51, the first stacked layer 302 can include a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs. The multiple oxide layers (shown in the areas with dotes) and multiple nitride layers (shown in the areas with meshes) in the first stacked layer 302 alternate in a vertical direction. The first stacked layer 302 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide layers and the nitride layers in the first stacked layer 302 is equal to or larger than 64.

[00191] In some embodiments, the first insulating connection layer 303 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is noted that, the material of the first insulating connection layer 303 can be different from the material of the nitride layer in the first stacked layer 302.

[00192] Further, in some embodiments, a first mask layer 304 can be formed on the surface of the first insulating connection layer 303. The first mask layer 304 can include a nitride layer on the surface of the first insulating connection layer 303, and an oxide layer on the surface of such nitride layer.

[00193] At S302, a first through hole 305 can be formed. As shown in FIG. 51, the first through hole 305 can completely penetrate the first stacked layer 302 and the first insulating connection layer 303, and can extend into the surface of the substrate 301.

[00194] In some embodiments, the first through hole 305 can be formed by etching the first stacked layer 302 and the first insulating connection layer 303 and a subsequent cleaning process. The etching process to form the first through hole 305 can be a wet etching, a dry etching, or a combination thereof.

[00195] In some embodiments, when the first mask layer 304 is formed on the surface of the first insulating connection layer 303, the etching process also etch the first mask layer 304 to form the first through holes 305.

[00196] At S303, a first channel structure 306 can be formed on the surface of the substrate 301 that is exposed by the first through hole 305, as shown in FIG. 52. In some embodiments, the first channel structure 306 can be a polycrystalline silicon layer formed by using a selective epitaxial process.

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[00197] At S304, a first functional layer can be formed on the sidewall of the first through hole 305. The first functional layer can include a first tunneling layer 307, a first storage layer 308, a first barrier layer 309, and a first passivation layer 310.

[00198] As shown in FIG. 53, the first tunneling layer 307 can be formed on the sidewall of the first through hole 305 and the surface of the first channel structure 306. The first tunneling layer can be used for generating electronic charges. In some embodiments, the first tunneling layer 307 can be an oxide layer formed by using a deposition process.

[00199] The first storage layer 308 can be formed on the surface of the first tunneling layer 307. The first storage layer 308 can be used for storing electronic charges. In some embodiments, the first storage layer 308 can be a nitride layer formed by using a deposition process.

[00200] The first barrier layer 309 can be formed on the surface of the first storage layer 308. The first barrier layer 309 can be used for blocking the outflow of the electronic charges stored in the first storage layer 308. In some embodiments, the first barrier layer 309 can be an oxide layer formed by using a deposition process.

[00201] As shown in FIG. 54, a first passivation layer 310 can be formed on the surface of the first barrier layer 309. The first passivation layer 310 can be used for protecting the first barrier layer 309 from being damaged in a subsequent removal process. In some embodiments, the first passivation layer 310 can be an amorphous silicon layer formed by using a deposition process.

[00202] The portions of the first passivation layer 310, the first barrier layer 309, the first storage layer 308 and the first tunneling layer 307 located on the surface of the first channel structure 306 on the bottom of the first through hole 305 can be removed. In some embodiments, the removal process can include an etching process and a cleaning process. As such, the first functional layer can be formed on the sidewall of the first through hole 305.

[00203] In some embodiment, in the same removal process, the first barrier layer 309, the first storage layer 308, the first tunneling layer 307, and the oxide layer of the first mask layer 304 located on the surface of the nitride layer of first mask layer 304 can also be removed. As such, the nitride layer of first mask layer 304 is remained on the surface of the first insulating connection layer 303.

[00204] At S305, a second channel structure can be formed on the sidewall of the first functional layer sidewall and the surface of the first channel structure 306. The surfaces

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of the second channel structure can be lower than the surface of the first insulating connection layer 303.

[00205] As shown in FIG. 55, a second channel layer 311 can be formed to cover the sidewall of the first passivation layer 310, the bottom of the first through hole 305. The second channel layer 311 can also cover the surface of the first insulating connection layer 303, or cover the surface of the nitride layer of the first mask layer 304. In some embodiments, the second channel layer 311 can be an amorphous silicon layer formed by using a deposition process.

[00206] As shown in FIGs. 56A and 56B, a portion of the second channel layer 311 can be removed, such that the surface of the second channel layer 311 is lower than the first insulating connection layer 303. The remaining portion of the second channel layer 311 can form the second channel structure that is in contact with the first channel structure 306. In some embodiments, an airgap can be enclosed by the second channel structure, as shown in FIGs. 56A and 56B. In some embodiments, the portion of the second channel layer 311 can be removed by using an etching process.

[00207] It is noted that, in various embodiments, the top surface of the second channel structure can be higher than the top surface of the first stacked layer 302 or lower than the top surface of the first stacked layer 302. However, the top surface of the second channel structure is not lower than the top surface of the top oxide layer in the first stacked layer 302. In some embodiments, the top surface of the second channel structure can be higher than the top nitride layer in the first stacked layer 302, as shown in FIG. 56A. In some alternative embodiments, the top surface of the second channel structure is in a same plane of the top surface of the top oxide layer in the first stacked layer 302, as shown in FIG. 56B.

[00208] At S306, a first groove 312 can be formed in the first insulating connection layer 303. In some embodiments, the projection of the first groove 312 on the substrate 301 can completely cover the projection of the first through hole 305 on the substrate 301.

[00209] As shown in FIGs. 57A and 57B, the nitride layer of the first mask layer 304 can be removed by using an etching process. As shown in FIGs. 58A and 58B, the surface of the first insulating connection layer 303 can be planarized. A portion of the first insulating connection layer 303 can be removed to form the first groove 312 that penetrates the first insulating connection layer 303. An area of the projection of the first

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groove 312 on the substrate 301 can be larger than an area of the projection of the first through hole 305 on the substrate 301.

[00210] In some embodiments, a depth of the first groove can be equal to or less than the thickness of the planarized first insulating connection layer 303, as shown in FIG. 58A. For example, the depth of the first groove can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 303 is about 90nm, while the depth of the first groove is about 60nm.

[00211] In some alternative embodiments, the depth of the first groove can be greater than the thickness of the planarized first insulating connection layer 303, as shown in FIG. 58B. That is, a portion of the top nitride layer in the first stacked layer 302 can also be removed to form the first groove. For example, the depth of the first groove can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 303 is about 30nm, while the depth of the first groove is about 60nm.

[00212] At S307, a third channel structure 313 can be formed in the first groove 312. As shown in FIGs. 59A and 59B, the third channel structure 313 can be in contact with the second channel structure. In some embodiments, the third channel structure can be a polycrystalline silicon player formed by using a deposition process.

[00213] A thickness of the third channel structure 313 can be equal to the depth of the first groove 312. As described above, in some embodiments, a thickness of the third channel structure 313 can be equal to or less than the thickness of the planarized first insulating connection layer 303, as shown in FIG. 59A. For example, the thickness of the third channel structure 313 can be in a range between 50nm and 70nm, preferably about 60nm. In some alternative embodiments, the thickness of the third channel structure 313 can be greater than the thickness of the planarized first insulating connection layer 303, as shown in FIG. 59B. For example, the thickness of the third channel structure 313 can be in a range between 60nm and 80nm, preferably about 70nm.

[00214] At S308, a second stacked layer 314 and a second insulating connection layer 315 can be sequentially formed on the third channel structure 313. As shown in FIG. 60, the second stacked layer 315 can include a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs. Similar to the first stacked layer 302 as described above, the multiple oxide layers (shown in the areas with dotes) and multiple nitride layers (shown in the areas with meshes) in the second stacked layer 314 alternate

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in a vertical direction. The second stacked layer 314 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide layers and the nitride layers in the second stacked layer 314 is equal to or larger than 64.

[00215] In some embodiments, the second insulating connection layer 315 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is noted that, the material of the second insulating connection layer 315 can be different from the material of the nitride layer in the second stacked layer 314.

[00216] Further, in some embodiments, a second mask layer 316 can be formed on the surface of the second insulating connection layer 315. The second mask layer 316 can include a nitride layer on the surface of the second insulating connection layer 315, and an oxide layer on the surface of such nitride layer.

[00217] At S309, a second through hole 317 can be formed. As shown in FIG. 61, the second through hole 317 can completely penetrate the second stacked layer 314 and the second insulating connection layer 315, and can extend into the surface of the third channel structure 313. The projection of the second through hole 317 on the substrate 301 can at least partially overlap with the projection of the first through hole 305 on the substrate 301.

[00218] In some embodiments, the second stacked layer 314, the second insulating connection layer 315, the second mask layer 316, and a portion of the third channel structure 314 can be etched to form the second through hole 317. The second stacked layer 314, the second insulating connection layer 315, the second mask layer 316, and/or the third channel structure 314 can be etched by using a dry etching process, a wet etching process, or a combination thereof. A cleaning process can then be performed to clean the second through hole 317.

[00219] In some embodiments, a maximum difference between the radius of the top aperture of each second through hole 317 and the radius of the bottom aperture of the second through hole 317 can be 15nm. That is, as shown in FIG. 61, a distance "a" between the boundary line of the top surface of the second through hole 317 and the boundary of the bottom surface of the second through hole 317 can be no more than 15 nm.

[00220] At S3010, a second functional layer can be formed on the sidewall of the second through hole 317. In some embodiments, the second functional layer can include

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a second tunneling layer 318, a second storage layer 319, a second barrier layer 320, and a second passivation layer 321.

[00221] As shown in FIG. 62, the second tunneling layer 318 can be formed on the sidewall of the second through hole 317 and the surface of the second channel structure 313. The second tunneling layer 318 can be used for generating electronic charges. In some embodiments, the second tunneling layer 318 can be an oxide layer formed by using a deposition process.

[00222] The second storage layer 319 can be formed on the surface of the second tunneling layer 318. The second storage layer 319 can be used for storing electronic charges. In some embodiments, the second storage layer 319 can be a nitride layer formed by using a deposition process.

[00223] The second barrier layer 320 can be formed on the surface of the second storage layer 319. The second barrier layer 320 can be used for blocking the outflow of the electronic charges in the second storage layer 319. In some embodiments, the second barrier layer 320 can be an oxide layer formed by using a deposition process.

[00224] As shown in FIG. 63, a second passivation layer 321 can be formed on the surface of the second barrier layer 320. The second passivation layer 321 can be used for protecting the second barrier layer 320 from being damaged in a subsequent removal process. In some embodiments, the second passivation layer 322 can be an amorphous silicon layer formed by using a deposition process.

[00225] As shown in FIG. 63, the portions of the second passivation layer 321, the second barrier layer 320, the second storage layer 319, the second tunneling layer 318, and the third channel structure 313 that are located at the bottom of the second through hole 317 and the top of the first through hole 305 can be removed. In some embodiments, the removal process can include an etching process and a cleaning process.

[00226] In some embodiments, the portions of the second passivation layer 321, the second barrier layer 320, the second storage layer 319, the second tunneling layer 318, and the oxide layer of the second mask layer 316 that are located on the nitride layer of the second mask layer 316 can also be removed by using an etching process. As such, the second functional layer can be formed on the sidewall of the second through hole 318, and the second through hole 317 and the first through hole 305 can be interconnected with each other, as shown in FIG. 63.

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[00227] In some embodiments, the portions of the second barrier layer 320, the second storage layer 319, and the second tunneling layer 318 that are located under the second passivation layer 321, as shown in the dashed circle in FIG. 64, can also be removed by using an etching process.

[00228] At S3011, the second tunneling structure, the third tunneling structure, the second passivation layer 321, and the first passivation layer 310 can be removed. In some embodiments, the second tunneling structure, the third tunneling structure, the second passivation layer 321, and the first passivation layer 310 can be removed by using one or more etching processes. As such, a third through hole 322 can be formed by interconnecting the first through hole and the second through hole, as shown in FIG. 65.

[00229] At S3012, a fourth channel structure and a first filling structure can be sequentially formed on the sidewall and the bottom of the third through hole 322. In some embodiments, the surface of the fourth channel structure can be higher than the surface of the first filling structure. In some embodiments, the fourth channel structure includes a joint channel structure that is sandwiched between the first stacked layer 302 and the second stacked layer 314, and covers the exposed surface of the first insulating connection layer 303.

[00230] As shown in FIG. 66, a fourth channel layer 328 can be formed to cover the sidewall and bottom of the third through hole 322 and the exposed surface of the third insulating connection layer 303. In some embodiments, the fourth channel layer 323 can also cover the surface of the second insulating connection layer 315, or the surface of the nitride layer of the second mask layer 316. In some embodiments, the fourth channel layer 328 can be an amorphous silicon layer formed by using a deposition process.

[00231] As shown in FIG. 67, a first filling layer 334 can be formed to cover the fourth channel layer 328 and to fill the third through hole 322. In some embodiments, the first filling layer 334 can be an oxide layer formed by using a deposition process.

[00232] As shown in FIG. 68, a portion of the first filling layer 334 can be removed, such that the surface of the first filling layer 334 is lower than the top surface of the second insulating connection layer 315. In some embodiments, the removal process can include an etching process. The remaining portion of the second filling layer 334 in the third through hole 322 can form the second filling structure.

[00233] As shown in FIG. 69, the portion of the fourth channel layer 328 located on the top surface of the second insulating connection layer 315 or the top surface of the second

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mask layer 316 can be removed. In some embodiments, the removal process can include an etching process. The remaining portion of the fourth channel layer 328 in the third through hole 322 can form the fourth channel structure. The top surface of the fourth channel structure can be higher than the top surface of the second filling structure. As such, a second groove can be formed on the fourth channel structure and the second filling structure, and in the third through hole 322.

[00234] It is noted that, the top surface of the fourth channel structure can be higher than the top surface of the second stacked layer 314, or can be lower than the top surface of the second stacked layer 314. The top surface of the fourth channel structure is not lower than the top surface of the top oxide layer in the second stacked layer 314. In some embodiments, the top surface of the fourth channel structure can be in a same plane of the top surface of the top oxide layer in the second stacked layer 314.

[00235] At S3013, a fifth channel structure can be formed in the second groove. The fifth channel structure can be in contact with the fourth channel structure. As shown in FIG. 70, the fifth channel structure 335 can be formed in the second groove that is on the fourth channel structure and the second filling structure and in the third through hole 322.

[00236] As shown in FIG. 71, the nitride layer of the second mask layer 316 can be removed by an etching process. As shown in FIGs. 72A and 72B, the top surface of the second insulating connection layer 315 and the top surface of the fifth channel structure 335 can be planarized.

[00237] Accordingly, the disclosed method as shown in FIGs. 74A and 74B can form a joint opening structure of a three-dimensional (3D) memory device by combining two through hole formation processes. As such, the formed channel hole having the joint opening structure can have a large aspect ratio and a limited top-bottom aperture error. Further, the disclosed method of forming a joint opening structure in a 3D memory device can result in an efficient process capability control, a simplified process complexity, and a reduced cost.

[00238] In some embodiments, the present disclosure also provides a three-dimensional memory device formed by using the above disclosed method as shown in FIGs. 74A and 74B. The three-dimensional memory can include the following components described below.

[00239] A first stacked layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer silicon nitride layer pairs, is formed on a substrate. A first insulating

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connection layer is formed on the first stacked layer. A first through hole penetrates the first stacked layer and the first insulating connection layer, and extends into the surface of the substrate. A first channel structure is formed on the surface of the substrate exposed by the first through hole. A first functional layer is formed on the sidewall of the first through hole.

[00240] A second stack layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs, is formed on the top surfaces of the first insulating connection layer. A second insulating connection layer is formed on the second stack layer. A second through hole penetrates through the second stacked layer and the second insulating connection layer, and is interconnected with the first through hole. A second functional layer is formed on the sidewall of the second through hole.

[00241] The first through hole and the second through hole constitute the third through hole. A fourth channel structure being contact with the first channel structure is formed on the sidewall and the bottom of the third through hole. A first filling structure is formed on the sidewall and the surface of the fourth channel structure to fill the third through hole. In some embodiments, an airgap is enclosed in the first filling structure. The top surface of the fourth channel structure is higher than the top surface of the first filling structure. A fifth channel structure in contact with the fourth channel structure is formed in a second groove that is surrounded by the second functional layer, and above the fourth channel structure and the first filling structure.

[00242] In some embodiments, as shown in FIG. 72A, a thickness "b" of the first insulating connection layer, which is the distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 80nm and 100nm, preferably about 90nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00243] In some alternative embodiments, as shown in FIG. 72B, a thickness "b" of the first insulating connection layer, which is the distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 20nm and 40nm, preferably about 30nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00244] Further, the error the radius of the aperture of different positions of the third through hole can be within 15nm. That is, a difference between a maximum radius of the third through hole and a minimum radius of the third through hole is less than or equal to

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15nm. Accordingly, the disclosed channel hole having a joint opening structure can have a large aspect ratio and a limited top-bottom aperture error.

[00245] In some embodiments, a replacement process can be performed to replace each of the plurality of nitride layers in the first stacked layer 302 and the second stacked layer 314 with a conductive layer 440, as shown in FIGs. 73A and 73B. The conductive layer can include any suitable material that is electronically conductive, including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof.

[00246] In some embodiments, during the replacement process, a portion of the third channel structure 313 that is adjacent with the bottom nitride layer of the second stacked layer 314, or is adjacent with the top nitride layer of the first stacked layer 302 can be converted to an oxide layer by an oxidation process. That is, as shown in FIGs. 73A and 73B, a thickness "c" of the third channel structure can be reduced after the replacement process. For example, the thickness "c" of the third channel structure can be reduced to a range between 30nm and 50nm, preferably about 40nm.

[00247] Referring to FIGs. 103A and 103B, schematic flow diagrams of another exemplary fabricating process for forming a joint opening structure of three-dimensional (3D) memory device are illustrated in accordance with some other embodiments of the present disclosure. And FIGs. 75-79, 80A, 80B, 81A, 81B, 82A, 82B, 83A, 83B, 84-100, 101A, 101B, 102A and 102B illustrate schematic structural cross-sectional diagrams of an exemplary joint opening structure of three-dimensional (3D) memory device at certain stages of the fabricating process shown in FIGs. 103A and 103B.

[00248] As shown in FIG. 103A, at S401, a first stacked layer 402 and a first insulating connection layer 403 can be sequentially formed on the surface of a substrate 401. In some embodiments, the 3D memory device can include a first region 100, a second region 200, and a third region 300, as shown in FIG. 75. The first region 100 can be used to form one or more channel holes, the second region 200 can be used to form one or more staircase structure (SS) dummy holes, while the third region 300 can be used to form one or more through array contact (TAC) barriers.

[00249] As shown in FIG. 75, the first stacked layer 402 can be formed on the substrate 401. The first stacked layer 402 can include a plurality of oxide/nitride layer pairs. That is, in the first stacked layer 402, multiple oxide layers (shown in the areas with dotes) and multiple nitride layers (shown in the areas with meshes) alternate in a vertical direction. In other words, except a top and a bottom layer of a given stack, each of the other oxide

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layers can be sandwiched by two adjacent nitride layers, and each nitride layer can be sandwiched by two adjacent oxide layers.

[00250] Oxide layers can each have the same thickness or have different thicknesses. For example, a thickness of each oxide layer can be in a range from 90nm to 160nm, preferably about 150nm. Similarly, nitride layers can each have the same thickness or have different thicknesses. For example, a thickness of each nitride layer can be in a range from 80nm to 110nm, preferably about 100nm. In some embodiments, the oxide layers can be silicon oxide layers, and the nitride layers can be silicon nitride layer.

[00251] The first stacked layer 402 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide layers and the nitride layers in the first stacked layer 402 is equal to or larger than 64. In some embodiments, alternating conductor/dielectric stack includes more oxide layers or more nitride layers with different materials and/or thicknesses than the oxide/nitride layer pair.

[00252] The first insulating connection layer 403 can be formed on the first stacked layer 402. In some embodiments, the first insulating connection layer 403 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is noted that, the material of the first insulating connection layer 403 can be different from the material of the nitride layer in the first stacked layer 402.

[00253] Further, in some embodiments, a first mask layer 404 can be formed on the surface of the first insulating connection layer 403. The first mask layer 404 can include a nitride layer on the surface of the first insulating connection layer 403, and an oxide layer on the surface of such nitride layer.

[00254] In some embodiments, the first stacked layer 402, the first insulating connection layer 403, and/or the first mask layer 404 can be formed by using one or more deposition processes, such as one or more chemical vapor deposition (CVD) processes, one or more physical vapor deposition (PVD) processes, one or more atomic layer deposition (ALD) processes, and/or any suitable combinations thereof.

[00255] At S402, one or more first through holes 405 can be formed in each of the first region 100, the second region 200, and the third region 300. As shown in FIG. 75, each of the one or more first through holes 405 can completely penetrate the first stacked layer 402 and the first insulating connection layer 403, and can extend into the surface of the substrate 401. In some embodiments, when the first mask layer 404 is formed on the

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surface of the first insulating connection layer 403, the etching process also etch the first mask layer 404 to form the first through holes 405.

[00256] In some embodiments, the first through holes 405 can be formed by etching the first stacked layer 402 and the first insulating connection layer 403 and a subsequent cleaning process. The etching process to form the first through holes 405 can be a wet etching, a dry etching, or a combination thereof. It is noted that, in the direction perpendicular to the surface of the substrate 201, the depth of the one or more first through holes 405 in the third region 300 can be larger than the depth of the one or more first through holes 405 in the first region 100.

[00257] At S403, a first channel structure 406 can be formed on the surface of the substrate 401 that is exposed by each of the plurality of first through holes 405, as shown in FIG. 76. In some embodiments, the first channel structure 406 can be a polycrystalline silicon (polysilicon) layer formed by using a selective epitaxial process.

[00258] At S404, a first functional layer can be formed on the sidewall of each of the plurality of first through holes 405. The first functional layer can include a first tunneling layer 407, a first storage layer 408, a first barrier layer 409, and a first passivation layer 410.

[00259] As shown in FIG. 77, the first tunneling layer 407 can be formed on the sidewall of the plurality of first through holes 405 and the exposed surfaces of the first channel structures 406. The first tunneling layer 407 can be used for generating electronic charges (electrons or holes). In some embodiments, the first tunneling layer 407 can be an oxide layer formed by using a deposition process.

[00260] The first storage layer 408 can be formed on the surface of the first tunneling layer 407. The first storage layer 408 can be used for storing electronic charges. The storage or removal of charge in the first storage layer 407 can impact the on/off state and/or a conductance of the semiconductor channel. The first storage layer 407 can include polycrystalline silicon (polysilicon) or silicon nitride. In some embodiments, the first storage layer 408 can be a nitride layer formed by using a deposition process.

[00261] The first barrier layer 409 can be formed on the surface of the first storage layer 408. The first barrier layer 409 can be used for blocking the outflow of the electronic charges stored in the first storage layer 408. In some embodiments, the first barrier layer 409 can be a silicon oxide layer or a combination of silicon oxide/silicon nitride/silicon oxide (ONO) layers. In some embodiments, the first barrier layer 409

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includes high dielectric constant (high-k) dielectrics (e.g., aluminum oxide). In one example, the first barrier layer 409 is an oxide layer formed by using a deposition process.

[00262] As shown in FIG. 78, a first passivation layer 410 can be formed on the surface of the first barrier layer 409. The first passivation layer 410 can be used for protecting the first barrier layer 409 from being damaged in a subsequent removal process. In some embodiments, the first passivation layer 410 can be an amorphous silicon layer formed by using a deposition process.

[00263] The portions of the first passivation layer 410, the first barrier layer 409, the first storage layer 408 and the first tunneling layer 407 located on the surfaces of the plurality of first channel structures 406 on the bottom of the plurality of first through holes 405 can be removed. In some embodiments, the removal process can include an etching process and a cleaning process. As such, the first functional layer can be formed on the sidewalls of the plurality of first through holes 405.

[00264] In some embodiment, in the same removal process, the first barrier layer 409, the first storage layer 408, the first tunneling layer 407, and the oxide layer of the first mask layer 404 located on the surface of the nitride layer of first mask layer 404 can also be removed. As such, the nitride layer of first mask layer 404 is remained on the surface of the first insulating connection layer 403.

[00265] At S405, a second channel structure can be formed on the sidewall of the first functional layer and the exposed surface of the first channel structure 406 in each of the plurality of first through holes 405. The second channel structure can be in contact with the first channel structure 406 in each first through hole 405. The surface of the second channel structure in each first through hole 405 can be lower than the top surface of the first insulating connection layer 403.

[00266] As shown in FIG. 79, a second channel layer 411 can be formed to cover the sidewalls of the first passivation layer 410 and the bottom of each of the plurality of first through holes 405. The second channel layer 411 can also cover the surface of the first insulating connection layer 403, or cover the surface of the nitride layer of the first mask layer 404. In some embodiments, the second channel layer 411 can be an amorphous silicon layer formed by using a deposition process.

[00267] As shown in FIGs. 80A and 80B, a portion of the second channel layer 411 can be removed, such that the top surface of the second channel layer 411 can be lower than the

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top surface of the first insulating connection layer 403. The remaining portion of the second channel layer 411 can form the second channel structure that is in contact with the first channel structure 406. In some embodiments, the portion of the second channel layer 411 can be removed by using an etching process.

[00268] It is noted that, in various embodiments, the top surface of the second channel structure can be higher than the top surface of the first stacked layer 402 or lower than the top surface of the first stacked layer 402. However, the top surface of the second channel structure is not lower than the top surface of the top oxide layer in the first stacked layer 402. In some embodiments, the top surface of the second channel structure can be higher than the top nitride layer in the first stacked layer 402, as shown in FIG. 80A. In some alternative embodiments, the top surface of the second channel structure is in a same plane of the top surface of the top oxide layer in the first stacked layer 402, as shown in FIG. 80B.

[00269] At S406, a first groove can be formed above the first insulating connection layer 403 above each of the plurality of first through holes 405. In some embodiments, the projection of the first groove on the substrate 401 can completely cover the projection of the corresponding first through hole 405 on the substrate 401.

[00270] As shown in FIGs. 81A and 81B, the nitride layer of the first mask layer 404 can be removed. In some embodiments, the nitride layer of the first mask layer 404 can be removed by using an etching process.

[00271] As shown in FIGs. 82A and 82B, the surface of the first insulating connection layer 403 can be planarized by any suitable techniques, such as backside grinding, and/or chemical mechanical polishing (CMP). A portion of the first insulating connection layer 403 can be removed to form a plurality of first grooves that penetrate the first insulating connection layer 403. An area of the projection of each of the plurality of first grooves on the substrate 401 can be larger than an area of the projection of each of the plurality of first through holes 405 on the substrate 401.

[00272] In some embodiments, a depth of the first groove 412 can be equal to or less than the thickness of the planarized first insulating connection layer 403, as shown in FIG. 82A. For example, the depth of the first groove 412 can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 403 is about 90nm, while the depth of the first groove is about 60nm.

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[00273] In some alternative embodiments, the depth of the first groove 412 can be greater than the thickness of the planarized first insulating connection layer 403, as shown in FIG. 82B. That is, a portion of the top nitride layer in the first stacked layer 402 can also be removed to form the first groove. For example, the depth of the first groove 412 can be in a range between 50nm and 70nm. In one embodiment, the thickness of the planarized first insulating connection layer 403 is about 30nm, while the depth of the first groove is about 60nm.

[00274] At S407, a third channel structure 413 can be formed in each of the plurality of first grooves 412. As shown in FIGs. 83A and 83B, the third channel structure 413 can be in contact with the second channel structure in each of the plurality of first through holes 405. In some embodiments, the third channel structure 413 can be a polycrystalline silicon player formed by using a deposition process.

[00275] A thickness of each third channel structure 413 can be equal to the depth of each first groove 412. As described above, in some embodiments, a thickness of each third channel structure 413 can be equal to or less than the thickness of the planarized first insulating connection layer 403, as shown in FIG. 83A. For example, the thickness of each third channel structure 413 can be in a range between 50nm and 70nm, preferably about 60nm. In some alternative embodiments, the thickness of each third channel structure 413 can be greater than the thickness of the planarized first insulating connection layer 403, as shown in FIG. 83B. For example, the thickness of each third channel structure 413 can be in a range between 60nm and 80nm, preferably about 70nm.

[00276] Referring to FIG. 103B, at S408, a second stacked layer 414 and a second insulating connection layer 415 can be sequentially formed on the plurality of third channel structures 413. As shown in FIG. 84, the second stacked layer 414 can include a plurality of oxide/nitride layer pairs, such as silicon oxide layers and silicon nitride layers. Similar to the first stacked layer 402 as described above, the multiple oxide layers (shown in the areas with dotes) and multiple nitride layers (shown in the areas with meshes) in the second stacked layer 414 alternate in a vertical direction. The second stacked layer 414 can include any suitable number of layers of the oxide layers and the nitride layers. In some embodiments, a total number of layers of the oxide layers and the nitride layers in the second stacked layer 414 is equal to or larger than 64.

[00277] In some embodiments, the second insulating connection layer 415 can be made by any suitable insulating material and/or dielectric material, such as silicon oxide. It is

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noted that, the material of the second insulating connection layer 415 can be different from the material of the nitride layer in the second stacked layer 414.

[00278] Further, in some embodiments, a second mask layer 416 can be formed on the surface of the second insulating connection layer 415. The second mask layer 416 can include a nitride layer on the surface of the second insulating connection layer 415, and an oxide layer on the surface of such nitride layer.

[00279] At S409, one or more second through holes 417 are formed in each of the first region 100, the second region 200, and the third region 300. As shown in FIG. 85, each of the plurality of second through holes 417 can completely penetrate the second stacked layer 414, the second insulating connection layer 415, and the second mask layer 416, and can extend into the surface of the corresponding third channel structure 413. The projection of each second through hole 417 on the substrate 401 can at least partially overlap with the projection of the corresponding first through hole 405 on the substrate 401.

[00280] In some embodiments, the second stacked layer 414, the second insulating connection layer 415, the second mask layer 416, and the third channel structures 413 can be etched to form the plurality of second through holes 417 that penetrate the second stacked layer 414 and the second insulating connection layer 415. The second stacked layer 414, the second insulating connection layer 415, the second mask layer 416, and/or the third channel structure 413 can be etched by using a dry etching process, a wet etching process, or a combination thereof. A cleaning process can then be performed to clean the plurality of second through holes 417.

[00281] It is noted that, each second through hole 417 can extend to the surface of the corresponding third channel structure 413, or can extend into the corresponding third channel structure 413. As such, a fourth channel structure formed subsequently in each second through hole 417 can directly contact the corresponding third channel structure.

[00282] In some embodiments, a maximum difference between the radius of the top aperture of each second through hole 417 and the radius of the bottom aperture of the second through hole 417 can be 15nm. That is, as shown in FIG. 85, a distance "a" between the boundary line of the top surface of each second through hole 417 and the boundary of the bottom surface of the second through hole 417 can be no more than 15 nm.

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[00283] At S4010, a second functional layer can be formed on the sidewall of each second through hole 417. In some embodiments, the second functional layer can include a second tunneling layer 418, a second storage layer 419, a second barrier layer 420, and a second passivation layer 421.

[00284] As shown in FIG. 86, the second tunneling layer 418 can be formed on the sidewall of each second through hole 417 and the surface of the corresponding third channel structure 413. The second tunneling layer 418 can be used for generating electronic charges. In some embodiments, the second tunneling layer 418 can be an oxide layer formed by using a deposition process.

[00285] The second storage layer 419 can be formed on the surface of the second tunneling layer 418. The second storage layer 419 can be used for storing electronic charges. In some embodiments, the second storage layer 419 can be a nitride layer formed by using a deposition process.

[00286] The second barrier layer 420 can be formed on the surface of the second storage layer 419. The second barrier layer 420 can be used for blocking the outflow of the electronic charges in the second storage layer 419. In some embodiments, the second barrier layer 420 can be an oxide layer formed by using a deposition process.

[00287] As shown in FIG. 87, a second passivation layer 421 can be formed on the surface of the second barrier layer 420. The second passivation layer 421 can be used for protecting the second barrier layer 420 from being damaged in a subsequent removal process. In some embodiments, the second passivation layer 421 can be an amorphous silicon layer formed by using a deposition process.

[00288] As shown in FIG. 87, the portions of the second passivation layer 421, the second barrier layer 420, the second storage layer 419, the second tunneling layer 418, and the third channel structure 413 between each second through hole 417 and the corresponding first through hole 405 can be removed. In some embodiments, the removal process can include an etching process and a cleaning process. In some embodiments, the portions of the second passivation layer 421, the second barrier layer 420, the second storage layer 419, the second tunneling layer 418, the oxide layer of the second mask layer 416 that are located on the nitride layer of the second mask layer 416 can also be removed by the same removal process. As such, the second functional layer can be formed on the sidewall of each second through hole 417, and each second through hole 417 and the corresponding first through hole 405 can be interconnected with each other.

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[00289] In some embodiments, the portions of the second barrier layer 420, the second storage layer 419, and the second tunneling layer 418 that are located under the second passivation layer 421, as shown in the dashed circle in FIG. 88, can also be removed by using an etching process.

[00290] At S4011, the second tunneling structure, the third tunneling structure, the second passivation layer 421, and the first passivation layer 410 can be removed. In some embodiments, the second tunneling structure, the third tunneling structure, the second passivation layer 421, and the first passivation layer 410 can be removed by using one or more etching processes. As such, a plurality of third through holes 422 can be formed in the first region 100, the second region 200, and the third region 300 by interconnecting each first through hole and the corresponding second through hole, as shown in FIG. 89.

[00291] At S4012, a fourth channel structure can be formed on the sidewall of the second functional layer and the exposed surface of the third channel structure in each third through hole 422 in the first region 100. Further, a first filling structure can be formed in each of the plurality of third through holes 422 in the first region 100, the second region 200, and the third region 300. In some embodiments, the top surface of the fourth channel structure can be higher than the top surface of the first filling structure.

[00292] As shown in FIG. 90, a fourth channel layer 428 can be formed to cover the sidewall and the bottom surface of each of the plurality of third through holes 422 in the first region 100, the second region 200, and the third region 300. In some embodiments, the fourth channel layer 428 can also cover the top surface of the nitride layer of the second mask layer 416. In some embodiments, the fourth channel layer 428 can be an amorphous silicon layer formed by using a deposition process. In some embodiments, the fourth channel structure 428 includes a joint channel structure that is sandwiched between the first stacked layer 402 and the second stacked layer 414, and covers the exposed surface of the first insulating connection layer 403.

[00293] As shown in FIG. 91, a second filling layer 429 can be formed to cover the fourth channel layer 428. In some embodiments, the second filling layer 429 can include one or more airgaps in each third through hole 417. In some embodiments, the second filling layer 429 can be an oxide layer formed by using a deposition process.

[00294] As shown in FIG. 92, a third mask layer 430 can be formed on the top surface of the second filling layer 429 in the first region 100. Using the third mask layer 430 as

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a mask, the portions of the second filling layer 429 located in the second region 200 and the third region 300 can be removed by using an etching process.

[00295] As shown in FIG. 93, the third mask layer 430 can be removed. Using the remaining second filling layer 429 in the first region 100 as a mask, the fourth channel layer 428 located in the second region 200 and the third region 300 can be removed by using an etching process. As such, one or more fourth through holes 431 can be formed in the second region 200 and the third region 300.

[00296] As shown in FIG. 94, a third filling layer 432 can be formed to cover the sidewall and the bottom of the one or more fourth through holes 431 in the second region 200 and the third region 300. The third filling layer 432 can also cover the exposed surface of the first insulating connection layer 403 in each fourth through hole 431 in the second region 200 and the third region 300. In some embodiments, the third filling layer 432 can enclose one or more airgap in one or more fourth through holes 431. In some embodiments, the filling performance of the third filling layer 432 can be better than the filling performance of the second filling layer 429. That is, in a same removing process, the removal rate of the third filling layer 432 can be less than the removal rate of the second filling layer 429.

[00297] As shown in FIG. 95, the second filling layer 429 on the surface of the fourth channel layer 428 in the first region 100 can be removed by using an etching process. As such, one or more fifth through holes 433 can be formed in the first region 100. It is noted that, a portion of the third filling layer 432 can also be removed by the same etching process.

[00298] As shown in FIG. 96, a first filling layer 434 can be formed in each fifth through hole 433 in the first region 100, and in each fourth through hole 431 in the second region 200 and the third region 300. The material of the first filling layer 434 can be the same material of the third filling layer 432.

[00299] As shown in FIG. 97, a portion of the first filling layer 434 can be removed by using an etching process, such that the top surface of the first filling layer 434 in each fifth through hole 433 or fourth through hole 431 is lower than the top surface of the second insulating connection layer 415. The remaining portion of the first filling layer 434 in each fourth through hole 431 or fifth through hole 433 can form the first filling structure.

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[00300] Further, the portion of the fourth channel layer 428 located on the surface of the second insulating connection layer 415 or the surface of the second mask layer 416 can be removed by using an etching process. The remaining portion of the fourth channel layer 428 in each fifth through hole 433 can form the fourth channel structure. The top surface of the fourth channel structure can be higher than the top surface of the first filling structure. As such, a second groove can be formed on the fourth channel structure and the first filling structure in each fifth through hole 433 in the first region 100, and on the first filling structure in each fourth through hole 431 in the second region 200 and the third region 300.

[00301] It is noted that, the top surface of the fourth channel structure can be higher than the top surface of the second stacked layer 414, or can be lower than the top surface of the second stacked layer 414. The top surface of the fourth channel structure is not lower than the top surface of the top oxide layer in the second stacked layer 414. In some embodiments, the top surface of the fourth channel structure can be in a same plane of the top surface of the top oxide layer in the second stacked layer 414.

[00302] At S4013, a fifth channel structure can be formed in the second groove of each fifth through hole 433 in the first region 100 and each fourth 431 in the second region 200 and third region 300. The fifth channel structure can be in contact with the fourth channel structure in each fifth through hole 433 in the first region 100.

[00303] As shown in FIG. 99, the fifth channel structure 435 can be formed in the second groove that is on the fourth channel structure and the first filling structure in each fifth through hole 433 in the first region 100. The fifth channel structure 435 can also be formed in the second groove that is on the first filling structure in each fourth through hole 431 in the second region 200 and the third region 300.

[00304] As shown in FIG. 100, the nitride layer of the second mask layer 416 can be then removed by an etching process. As shown in FIGs. 101A and 101B, the top surface of the second insulating connection layer 415 and the top surface of the plurality of fifth channel structures 435 can be planarized by any suitable techniques, such as backside grinding, and/or chemical mechanical polishing (CMP).

[00305] Accordingly, the disclosed method as shown in FIGs. 101A and 101B can form another joint opening structure of a three-dimensional (3D) memory device by combining two through hole formation processes. As such, the formed channel holes having the joint opening structure can have a large aspect ratio and a limited top-bottom aperture

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error. Further, the disclosed method of forming a joint opening structure in a 3D memory device can simultaneously form a plurality of channel holes, staircase dummy holes, and through array contact barriers, resulting in an efficient process capability control, a simplified process complexity, and a reduced cost.

[00306] In some embodiments, the present disclosure also provides another three-dimensional memory device formed by using the above disclosed method as shown in FIGs. 101A and 101B. The three-dimensional memory device can include a first region for forming a plurality of channel holes, a second region for forming a plurality of staircase structure (SS) dummy holes, and a third region for forming a plurality of through array contact (TAC) barriers. Along a direction perpendicular to the surface of the three-dimensional memory device, the three-dimensional memory device can include the following components.

[00307] A first stacked layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs, is formed on a substrate. A first insulating connection layer is formed on the first stacked layer. A plurality of first through holes penetrating the first stacked layer and the first insulating connection layer and extending into the surface of the substrate are formed in the first region, the second region, and the third region.

[00308] A first channel structure is formed on the surface of the substrate exposed by each first through hole. A first functional layer is formed on the sidewall of each first through hole. A second channel structure is formed on the sidewall of the first functional layer and the surface of the first channel structure in each first through hole. A first filling structure is formed on the sidewall and the surface of the second channel structure to fill each of the plurality of first through holes. In some embodiments, an airgap can be enclosed in the first filling structure in each first through hole. The top surfaces of the second channel structure and the first filling structure are lower than the top surfaces of the first insulating connection layer.

[00309] A first groove is formed in the first insulating connection layer, and above the first functional layer, the second channel structure and the first filling structure in each first through hole. A projection of each of the plurality of first grooves on the substrate completely covers a projection of the corresponding first through hole on the substrate. A third channel structure in contact with the second channel structure in the corresponding first through hole is formed in each first groove.

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[00310] A second stack layer including a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs, is formed on the top surfaces of the first insulating connection layer and the plurality of third channel structures. A second insulating connection layer is formed on the second stack layer. A plurality of second through holes penetrating through the second stacked layer and the second insulating connection layer and extending into a surface of the third channel structure are formed in the first region, the second region, and the third region. A projection of each of the plurality of second through holes on the substrate at least partially overlaps the projection of the corresponding first through hole on the substrate.

[00311] A second functional layer is formed on the sidewall of each second through hole. A fourth channel structure is formed on the sidewall of the second functional layer and the bottom surface of each second through hole in the first region. A second filling is formed to fill each of the plurality of second through holes in the first region, the second region, and the third region. In some embodiments, an airgap can be enclosed in the second filling structure. The top surface of the fourth channel structure is higher than the top surface of the second filling structure in each second through hole in the first region.

[00312] In the first region, a fifth channel structure in contact with the fourth channel structure is formed in a second groove in each second through hole that is surrounded by the second functional layer, and above the fourth channel structure and the second filling structure. And in the second region and the third region, a fifth channel structure is formed in a second groove in each second through hole that is surrounded by the second functional layer, and above the second filling structure.

[00313] Due to the fourth channel structures being formed in the second through holes in the first region rather than the third region, the fifth channel structure in each second through hole in the first region can be electronically connected with the first channel structure in the corresponding first through hole, while the fifth channel structure in each second through hole in the third region can be electronically insulated with the first channel structure in the corresponding first through hole. Thus, in the three-dimensional memory device, a plurality of channel holes can be formed in the first region, and a plurality of through array contact (TAC) barriers can be formed in the third region. The plurality of staircase structure dummy holes in the second region can have a supporting function of the staircase structure.

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[00314] In some embodiments, as shown in FIG. 101A, in each channel hole in the first region, a thickness "b" of the first insulating connection layer, which is the distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 80nm and 100nm, preferably about 90nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00315] In some alternative embodiments, as shown in FIG. 101B, in each channel hole in the first region, a thickness "b" of the first insulating connection layer, which is the distance between the top nitride layer of the first stacked layer and the bottom nitride layer of the second stacked layer can be in a range between 20nm and 40nm, preferably about 30nm. A thickness "c" of the third channel structure can be in a range between 50nm and 70nm, preferably about 60nm.

[00316] Further, the difference between the radiuses of the top aperture and the bottom aperture of the second channel structure, and the difference between the radiuses of the top aperture and the bottom aperture of the fourth channel structure can be within 15nm. Accordingly, the disclosed channel hole having a joint opening structure can have a large aspect ratio and a limited top-bottom aperture error.

[00317] In some embodiments, a replacement process can be performed to replace each of the plurality of nitride layers in the first stacked layer 402 and the second stacked layer 414 with a conductive layer 440, as shown in FIGs. 102A and 102B. The conductive layer can include any suitable material that is electronically conductive, including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof.

[00318] In some embodiments, the replacement process can be performed in one or more of the first region 100, the second region 200, and the third region 300. In one embodiments, the replacement process is performed in the first region 100 and the second region 200, but not in the third region 300. That is, the first stacked layer and the second stacked layer in the first region and the second region can be alternating conductive/dielectric stack, while the first stacked layer and the second stacked layer in the third region can be alternating oxide/nitride stack.

[00319] In some embodiments, during the replacement process, a portion of the third channel structure 413 that is adjacent with the bottom nitride layer of the second stacked layer 414, or is adjacent with the top nitride layer of the first stacked layer 402 can be

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converted to an oxide layer by an oxidation process. That is, as shown in FIGs. 102A and 102B, a thickness "c" of the third channel structure can be reduced after the replacement process. For example, the thickness "c" of the third channel structure can be reduced to a range between 30nm and 50nm, preferably about 40nm.

[00320] The provision of the examples described herein (as well as clauses phrased as "such as," "e.g.," "including," and the like) should not be interpreted as limiting the claimed subject matter to the specific examples; rather, the examples are intended to illustrate only some of many possible aspects.

[00321] Further, the words "first", "second" and the like used in this disclosure do not denote any order, quantity or importance, but are merely intended to distinguish between different constituents. The words "comprise" or "include" and the like mean that the elements or objects preceding the word can cover the elements or objects listed after the word and their equivalents, without excluding other elements or objects. The words "connect" or "link" and the like are not limited to physical or mechanical connections, but can include electrical connections, either directly or indirectly.

[00322] Although the present disclosure has been described and illustrated in the foregoing illustrative embodiments, it is understood that the present disclosure has been made only by way of example, and that numerous changes in the details of embodiment of the present disclosure can be made without departing from the spirit and scope of the present disclosure, which is only limited by the claims which follow. Features of the disclosed embodiments can be combined and rearranged in various ways. Without departing from the spirit and scope of the present disclosure, modifications, equivalents, or improvements to the present disclosure are understandable to those skilled in the art and are intended to be encompassed within the scope of the present disclosure.

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