**UNITED STATES PATENT AND TRADEMARK OFFICE**

---

**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

---

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

---

Case Nos.: IPR2025-00244, IPR2025-00294
U.S. Patent No. 10,886,291
Issue Date: January 5, 2021

Title: JOINT OPENING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME

---

# DECLARATION OF DR. SANJAY K. BANERJEE IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 10,886,291



**Micron Ex. 1003, p. 1**
**Micron v. YMTC**
**IPR2025-00244**

## TABLE OF CONTENTS

**I. INTRODUCTION ..... 12**

**II. BACKGROUND AND EXPERT QUALIFICATIONS ..... 12**

**III. ASSIGNMENT AND MATERIALS CONSIDERED ..... 17**

**IV. UNDERSTANDING OF THE LAW ..... 19**

**V. LEVEL OF SKILL IN THE ART ..... 23**

**VI. TECHNOLOGICAL BACKGROUND ..... 25**

**VII. THE '291 PATENT ..... 32**

A. Effective Filing Date ..... 32

B. Overview ..... 32

C. Prosecution History ..... 34

D. Claims ..... 37

**VIII. CLAIM CONSTRUCTION ..... 46**

**IX. UNPATENTABILITY ANALYSIS ..... 50**

A. Overview of the Prior Art ..... 51

1. Costa ..... 51

2. Liu ..... 57

3. Lee ..... 58

4. Toyama ..... 60

B. *Ground 1 (IPR2025-00244)*: Claims 1-5, 8-9, 11-12, and 14-19 Are Obvious Over Costa ..... 61

1. Claim 1 ..... 61

*[1.Pre] "A method of forming a joint opening structure in a three-dimensional (3D) memory device, comprising:" ..... 61*



**Micron Ex. 1003, p. 2**
**Micron v. YMTC**
**IPR2025-00244**

*[1.A] "forming a first stacked layer and forming a first insulating connection layer on the first stacked layer;" .....62*

*[1.B] "forming a first through hole that penetrates the first stacked layer and the first insulating connection layer;" .....66*

*[1.C] "forming a first channel structure overlaying the surface of the substrate that is exposed by the first through hole;".....68*

*[1.D] "forming a first functional layer on the sidewall of the first through hole;" .....70*

*[1.E] "forming a second channel structure and forming a first filling structure on the sidewall of the first functional layer and the exposed surface of the first channel structure;".....74*

*[1.F] "forming a third channel structure in contact with the second channel structure above the first through hole, wherein a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate;" .....79*

*[1.G] "forming a second stacked layer and forming a second insulating connection layer on the first insulating connection layer;" .....89*

*[1.H] "forming a second through hole that penetrates the second stacked layer and the second insulating connection layer, wherein a projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate;" .....93*

*[1.I] "forming a second functional layer on the sidewall of the second through hole;" .....97*

*[1.J] "forming a fourth channel structure and forming a second filling structure on the sidewall of the second functional layer and the exposed surface of the third channel structure; and" .99*

*[1.K] "forming a fifth channel structure in contact with the fourth channel structure above the second through hole." ....102*

2. Claim 2 .....107



**Micron Ex. 1003, p. 3**
**Micron v. YMTC**
**IPR2025-00244**

*[2.PRE] "The method of claim 1, wherein:" .....107*

*[2.A] "the first stacked layer includes a first number of oxide/nitride layer pairs; and" [2.B] "the second stacked layer includes a second number of oxide/nitride layer pairs." .....107*

3. Claim 3 .....108

*[3] "The method of claim 2, wherein: the first number and the second number are not less than 32." .....109*

4. Claim 4 .....109

*[4.PRE] "The method of claim 1, wherein forming the first functional layer comprises:" [4.A] "forming a first tunneling layer on the sidewall of the first through hole and the exposed surface of the first channel structure, wherein the first tunneling layer is configured, in operation, to generate charges;" .....109*

*[4.B] "forming a first storage layer on the surface of the first tunneling layer to store the charges generated by the first tunneling layer;" .....111*

*[4.C] "forming a first barrier layer on the surface of the first storage layer to block the outflow of charges in the first storage layer;" .....113*

*[4.D] "forming a first passivation layer on the surface of the first barrier layer to protect the first barrier layer from being damaged in a subsequent removal process; and" .....115*

*[4.E] "removing portions of the first passivation layer, the first barrier layer, the first storage layer, and the first tunneling layer on the surface of the first channel structure, wherein remaining portions of the first passivation layer, the first barrier layer, the first storage layer, and the first tunneling layer on the sidewall of the first through hole to form the first functional layer." .....117*

5. Claim 5 .....118

*[5.PRE] "The method of claim 4, wherein forming the second channel structure and the first filling structure comprises:"*



**Micron Ex. 1003, p. 4**
**Micron v. YMTC**
**IPR2025-00244**

*[5.A] "forming a second channel layer that covers the sidewall of the first passivation layer and the exposed surface of the first channel layer;* .....*118*

*[5.B] "forming the first filling layer that covers the surface of the second channel layer;"* .....*118*

*[5.C] "removing a portion of the first filling layer to form the first filling structure, wherein the top surface of the first filling structure is lower than the top surface of the first insulating connection layer; and [5.D] "removing a portion of the second channel layer to form the second channel structure, wherein a top surface of the second channel structure is lower than a top surface of the first insulating connection layer."* .....*118*

6. Claim 8 .....125

*[8.PRE] "The method of claim 1, further comprising:" [8.A] "forming a first mask layer overlaying the first insulating connection layer before forming the first through hole; and"* .....*126*

*[8.B] "removing the first mask layer after forming the first filling structure;"* .....*126*

*[8.C] "forming a second mask layer on the second insulating connection layer before forming the second through hole; and"* .....*126*

*[8.D] "removing the second mask layer after forming the second filling structure."* .....*127*

7. Claim 9 .....127

*[9.PRE] "The method of claim 1, wherein forming the fourth channel structure and the second filling structure comprises:" [9.A] "forming a fourth channel layer that covers the sidewall of a second functional layer and the exposed surface of the third channel layer;"* .....*127*

*[9.B] "forming a second filling layer that covers the surface of the fourth channel layer;"* .....*127*



**Micron Ex. 1003, p. 5**
**Micron v. YMTC**
**IPR2025-00244**

*[9.C] "removing a portion of the second filling layer to form the second filling structure, wherein the top surface of the second filling structure is lower than the top surface of the second insulating connection layer; and"* .....*128*

*[9.D] "removing a portion of the fourth channel layer to form the fourth channel structure, wherein a top surface of the fourth channel structure is lower than a top surface of the second insulating connection layer."*.....*129*

8. Claim 11 .....130

*[11.PRE] "A joint opening structure of a three-dimensional (3D) memory device, comprising:"* .....*130*

*[11.A] "a first stacked layer disposed overlaying a substrate;"* .....*130*

*[11.B] "a first insulating connection layer disposed on the first stacked layer;"* .....*130*

*[11.C] "a first through hole penetrating the first stacked layer and the first insulating connection layer;"*.....*130*

*[11.D] "a first channel structure disposed at the bottom of the first through hole and overlaying the substrate;"* .....*131*

*[11.E] "a first functional layer disposed on the sidewall of the first through hole;"* .....*131*

*[11.F] "a second channel structure in contact with the first channel structure disposed on the sidewall of the first functional layer;"*.....*131*

*[11.G] "a third channel structure in contact with the second channel structure disposed over the first through hole, wherein a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate;"* .....*132*

*[11.H] "a second stacked layer disposed on the third channel structure;"*.....*132*



**Micron Ex. 1003, p. 6**
**Micron v. YMTC**
**IPR2025-00244**

*[11.I] "a second insulating connection layer disposed on the second stacked layer;"* ..... *132*

*[11.J] "a second through hole penetrating the second stacked layer and the second insulating connection layer, wherein a projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate;"* ..... *132*

*[11.K] "a second functional layer disposed on the sidewall of the second through hole;"* ..... *132*

*[11.L] "a fourth channel structure in contact with the third channel structure disposed on the sidewall of the second functional layer; and"* ..... *133*

*[11.M] "a fifth channel structure in contact with the fourth channel structure disposed over the second through hole."* .. *133*

9. Claim 12 ..... 133

*[12.PRE] "The joint opening structure of claim 11, further comprising:" [12.A] "a first filling structure covering the surface of the second channel structure; and"* ..... *133*

*[12.B] "a second filling structure covering the surface of the fourth channel structure;"* ..... *133*

*[12.C] "wherein the first through hole is non-interconnected with the second through hole."* ..... *134*

10. Claim 14 ..... 135

*[14.PRE] "The joint opening structure of claim 11, wherein:" [14.A] "the first stacked layer includes a first number of conductor/dielectric layer pairs; and" [14.B] "the second stacked layer includes a second number of conductor/dielectric layer pairs."* ..... *136*

11. Claim 15 ..... 136

*[15] "The joint opening structure of claim 14, wherein: the first number and the second number are not less than 32."* ..... *136*



**Micron Ex. 1003, p. 7**
**Micron v. YMTC**
**IPR2025-00244**

12. Claim 16 ..... 136

*[16.PRE]-[16.B] "The joint opening structure of claim 11, wherein: the first stacked layer includes a first number of oxide/nitride layer pairs; and the second stacked layer includes a second number of oxide/nitride layer pairs.* ..... *136*

13. Claim 17 ..... 136

*[17] "The joint opening structure of claim 16, wherein: the first number and the second number are not less than 32."* ..... *136*

14. Claim 18 ..... 137

*[18] "The joint opening structure of claim 11, wherein: a thickness of the third channel structure is in a range between 30 nm and 70 nm."* ..... *137*

15. Claim 19 ..... 137

*[19.PRE] "The joint opening structure of claim 11, wherein:"* ..... *137*

*[19.A] "a size difference between a top aperture and a bottom aperture of the first through hole is equal to or less than 30 nm; and"* ..... *137*

*[19.B] "a size difference between a top aperture and a bottom aperture of the second through hole is equal to or less than 30 nm."* ..... *139*

C. *Ground 1 (IPR2025-00294)*: Dependent Claims 6 and 7 Are Obvious Over Costa in View of Liu ..... 139

1. Motivation to Combine ..... 139

2. Claim 6 ..... 146

*[6.PRE] "The method of claim 1, wherein forming the third channel structure comprises:" [6.A] "etching the first insulating connection layer to form a first groove, wherein a projection of the first groove on the substrate covers the projection of the first through hole on the substrate;"* ..... *146*



**Micron Ex. 1003, p. 8**
**Micron v. YMTC**
**IPR2025-00244**

*[6.B] "forming a third channel layer in the first groove, wherein the third channel layer is in contact with the second channel structure; and"* ..... *151*

*[6.C] "planarizing the top surfaces of the first insulating connection layer and the third channel layer to form the third channel structure."* ..... *152*

3. Claim 7 ..... 154

*[7.PRE] "The method of claim 1, wherein forming the third channel structure comprises:" [7.A] "etching the first insulating connection layer and at least a portion of the top nitride layer of the first stacked layer to form a first groove, wherein a projection of the first groove on the substrate covers the projection of the first through hole on the substrate;"* ..... *154*

*[7.B] "forming the third channel structure in the first groove, wherein the third channel structure is in contact with the second channel structure; and"* ..... *154*

*[7.C] "planarizing the top surfaces of the first insulating connection layer and the third channel structure."* ..... *155*

D. *Ground 2 (IPR2025-00294):* Dependent Claim 10 Is Obvious Over Costa in View of Lee ..... 155

1. Motivation to Combine ..... 155

2. Claim 10 ..... 158

*[10.PRE] "The method of claim 1, wherein forming the fifth channel structure comprises:" [10.A] "etching the second insulating connection layer to form a second groove, wherein a projection of the second groove on the substrate covers the projection of the second through hole on the substrate;"* ..... *158*

*[10.B] "forming a fifth channel layer in the second groove, wherein the fifth channel layer is in contact with the fourth channel structure; and"* ..... *162*



**Micron Ex. 1003, p. 9**
**Micron v. YMTC**
**IPR2025-00244**

*[10.C] "planarizing the top surfaces of the second insulating connection layer and the fifth channel layer to form the fifth channel structure."* ..... *163*

E. *Ground 3 (IPR2025-00294)*: Independent Claim 20 Is Obvious Over Costa in View of Toyama ..... 165

1. Motivation to Combine ..... 165

2. Claim 20: ..... 170

*[20.PRE] "A joint opening structure of a three-dimensional (3D) memory device, comprising:"* ..... *170*

*[20.A] "a first stacked layer disposed overlaying a substrate;"* ..... *170*

*[20.B] "a first insulating connection layer disposed on the first stacked layer;"* ..... *170*

*[20.C] "a second stacked layer disposed on the first insulating connection layer;"* ..... *170*

*[20.D] "a second insulating connection layer disposed on the second stacked layer;"* ..... *170*

*[20.E] "a plurality of channel holes in a first region of the 3D memory device;"* ..... *170*

*[20.F] "a plurality of staircase structure dummy holes in a second region of the 3D memory device; and"* ..... *171*

*[20.G] "a plurality of through array contact barriers in a third region of the 3D memory device;"* ..... *172*

*[20.H] "wherein each of the plurality of channel holes includes: a first through hole penetrating the first stacked layer and the first insulating connection layer,"* ..... *174*

*[20.I] "a first channel structure disposed at the bottom of the first through hole and overlaying the substrate,"* ..... *174*



**Micron Ex. 1003, p. 10**
**Micron v. YMTC**
**IPR2025-00244**

*[20.J] "a first functional layer disposed on the sidewall of the first through hole,"* .....175

*[20.K] "a second channel structure in contact with the first channel structure disposed on the sidewall of the first functional layer,"* .....175

*[20.L] "a third channel structure in contact with the second channel structure disposed over the first through hole, wherein a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate,"* .....175

*[20.M] "a second through hole penetrating the second stacked layer and the second insulating connection layer, wherein a projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate,"* .....175

*[20.N] "a second functional layer disposed on the sidewall of the second through hole,"* .....176

*[20.O] "a fourth channel structure in contact with the third channel structure disposed on the sidewall of the second functional layer, and"* .....176

*[20.P] "a fifth channel structure in contact with the fourth channel structure disposed over the second through hole."* ..176

F. Secondary Considerations of Non-Obviousness.....176



**Micron Ex. 1003, p. 11**
**Micron v. YMTC**
**IPR2025-00244**

I, Dr. Sanjay K. Banerjee, declare as follows:

## I. INTRODUCTION

1. I have been retained by Micron Technology, Inc. ("Micron") as an independent expert consultant in this proceeding before the United States Patent and Trademark Office ("PTO"). I am not an employee of Micron or any affiliate or subsidiary of Micron.

2. I have been asked to consider whether certain references disclose or teach the features recited in the claims of U.S. Patent No. 10,886,291, which I refer to herein as the '291 patent.

3. My opinions and the bases for my opinions are set forth below.

4. I am being compensated at my standard consulting rate of $650 per hour for my time. My compensation is based solely on the amount of time that I devote to activity related to this case and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

## II. BACKGROUND AND EXPERT QUALIFICATIONS

5. My *curriculum vitae* ("CV") accompanies this declaration as Ex. 1004 and provides an accurate identification of my background, experience, and qualifications as an expert in electronics and three-dimensional memory technology.

6. I currently serve as the Cockrell Family Regents Chair Professor of Electrical and Computer Engineering and Director of the Microelectronics Research Center at the University of Texas at Austin ("UT"). Prior to this position, I was first an Assistant Professor (September 1987-August 1990) and later an Associate Professor (September 1990-August 1993) at UT, before being named a Professor in September 1993. Prior to starting my academic work at UT, I was a member of the technical staff at Texas Instruments (Corporate R&D) from the time I completed my doctoral studies in 1983 until August 1987. I worked on vertical 3D Dynamic Random Access Memory (DRAM) cells (see S. Banerjee and M. Bordelon, "A Model for the Trench Transistor," IEEE Trans. Elec. Dev., 34 (12), 2485-2493, December 1987).

7. In addition to my academic work at UT, I was also the Director of the SouthWest Academy of Nanoelectronics, one of three centers created by the Semiconductor Research Corporation Nanoelectronics Research Initiative in 2006 to research and develop a replacement for conventional metal oxide semiconductor field effect transistors ("MOSFETs") during the entire program.

8. I received my Ph.D. in Electrical Engineering from the University of Illinois in 1983. I also received an M.S. in Electrical Engineering from the University of Illinois in 1981. I received a B. Tech. in Electronics from the Indian Institute of Technology at Kharagpur in 1979.



**Micron Ex. 1003, p. 13**
**Micron v. YMTC**
**IPR2025-00244**

9. As described in my CV (Ex. 1004), I have more than 40 years of experience in the field of electrical engineering, including extensive experience in semiconductor development and fabrication including that of 3-Dimensional Dynamic Random Access Memory ("DRAM") cells, MOSFETs, flash memory, and beyond-complementary metal-oxide-semiconductor ("CMOS") transistors. My work in these fields has resulted in thirty-five United States patents related to methods of forming polysilicon and novel transistors, flash memory, and vertical DRAM cells. I have been elected a Fellow of the National Academy of Inventors.

10. Much of my research and experience has been related to methods for MOSFET fabrication and design, including deposition of thin films by chemical vapor deposition (CVD), atomic layer deposition (ALD), physical vapor deposition (PVD), patterning using photolithography and etching using plasma-based Reactive Ion Etching (RIE) which are some of the processing techniques used to make 3D NAND flash. I have worked extensively on polysilicon thin film transistors similar to the ones used in the channel of NAND flash memory cells, high-k and other dielectrics used for charge storage, and for tunneling. A number of the sponsored research grants on which I have been a principal or coinvestigator have related to chemical deposition methods and/or ultra-shallow source/drain junction technology, including "Transport in MOSFETs" (Motorola, August 1993-August 1994), "Ultra Shallow Junction Technology" (SEMATECH January 1994-December 1996), and

"Vertical Si-Ge-C MOSFETS" (Semiconductor Research Corporation September 2000-August 2003). In addition, I am an author on over forty publications relating to flash memory cells, including vertical 3D memory that can be used in NAND flash (e.g., Sarkar J, Dey S, Shahrjerdi D, Banerjee SK, Vertical Flash memory cell with nanocrystal floating gate for ultradense integration and good retention, IEEE ELECTRON DEVICE LETTERS 28 (5): 449-451 MAY 2007.) One of my papers on flash memory was given a Best Paper Award by the SRC.

11. I am a Fellow of the Institute of Electrical and Electronics Engineers ("IEEE"), the American Physical Society ("APS"), and the American Association for the Advancement of Science ("AAAS"). I have served on numerous professional and government committees in the electrical engineering field, including chairing multiple IEEE committees, meetings, and programs, serving on Morgan & Claypool's editorial board, and serving as a member on the International Technology Roadmap for Semiconductors ("ITRS").

12. I have taught courses in Semiconductor Physics, Solid State Electronic Devices, and Microelectronic and VLSI Device Fabrication at UT. In addition, I have delivered many courses to industry on Semiconductor Devices and Memory and Semiconductor Processing. I have taught courses that cover 3D memories, such as 3D NAND (Ultra Large Scale Integration Techniques and Solid State Electronic



**Micron Ex. 1003, p. 15**
**Micron v. YMTC**
**IPR2025-00244**

Devices). As a principal investigator, I have been the advisor to over 80 Doctoral and Masters students.

13. I am the co-author of several books and invited book chapters covering the area of electronic and semiconductor devices, including: Dopant Diffusion, Solid State Electronic Devices (three editions), Silicon-germanium Devices, and Novel 3D CMOS. I have authored or co-authored more than 1,000 papers and presentations in the areas of semiconductor devices and electronics development over the course of my career.

14. I have been the recipient of fifty grants to fund my research from a variety of funding agencies including the National Science Foundation ("NSF"), DARPA, the Department of Energy, Semiconductor Research Corporation, the Department of Defense-Multidisciplinary University Research Initiative, and the Office of Naval Research.

15. I have received numerous awards for my work, including the NSF Presidential Young Investigator Award. The NSF Presidential Young Investigator Award was[1] a highly competitive honor and grant bestowed annually upon

[1] The NSF Presidential Young Investigator Award was an award given out by the NSF until 1991, at which time it was replaced with the NSF Young Investigator Awards and Presidential Faculty Fellows Program.



Micron Ex. 1003, p. 16
Micron v. YMTC
IPR2025-00244

recognized young academic leaders in science and engineering. I have received numerous other awards, including some the highest honors for semiconductor devices such as the Andrew Grove Award from the IEEE, and the Semiconductor Industry Association/Semiconductor Research Corporation University Researcher Award, for my work in semiconductor memory and transistors, which are described in more detail in my CV (Ex. 1004).

## III. ASSIGNMENT AND MATERIALS CONSIDERED

16. I have been asked to provide analysis and explain the subject matter of the ’291 patent, including the state of the art when the application underlying the ’291 patent was filed. I have also been asked to consider, analyze, and explain certain prior art to the ’291 patent including how that art relates to the challenged claims of the ’291 patent and to provide my opinions regarding whether that art invalidates the claimed subject matter.

17. The opinions expressed in this declaration are not exhaustive of opinions I may offer in the future regarding the unpatentability of the claims of the ’291 patent. Therefore, the fact that I do not address a particular point should not be understood to indicate an agreement on my part that any claim complies with the requirements of any other applicable rule.

18. I reserve the right to amend and supplement this declaration in light of additional evidence, arguments, or testimony presented during this IPR or related proceedings on the ’291 patent.

19. In forming the opinions set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, knowledge of scientific and engineering principles, and my experience. I have also reviewed and considered the ’291 patent (Ex. 1001), its prosecution history (Ex. 1002), and the following additional materials:

| EXHIBIT | DESCRIPTION |
|---|---|
| 1005 | U.S. Patent Publication No. 2018/0182771 A1 to Costa et al. (“Costa”) |
| 1006 | U.S. Patent Publication No. 2016/0204117 A1 to Liu et al. (“Liu”) |
| 1007 | U.S. Patent Publication No. 2015/0060979 A1 to Lee et al. (“Lee”) |
| 1008 | U.S. Patent Publication No. 2017/0179026 A1 to Toyama et al. (“Toyama”) |
| 1009 | Aritome, “NAND Flash Memory Technologies” (2016) |
| 1010 | Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017 |
| 1011 | Micheloni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018) |
| 1012 | U.S. Patent No. 10,475,737 to Tang et al. |
| 1013 | Micheloni, “3D Flash Memories” (2016) |

| EXHIBIT | DESCRIPTION |
|---|---|
| 1014 | U.S. Patent No. 9,853,046 to Lu et al. |
| 1015 | Excerpt from YMTC's Exemplary Infringement Claim Chart for U.S. Patent No. 10,886,291 (Ex. C-1 to Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024) ("Ex. C-1, YMTC's Contentions") [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL] |
| 1016 | U.S. Patent No. 9,245,962 to Yang et al. |
| 1017 | U.S. Patent No. 10,283,518 to Lee et al. |
| 1018 | Stavitski et al., "Specific contact resistance measurements of metal-semiconductor junctions," *2006 IEEE International Conference on Microelectronic Test Structures*, Austin, TX, USA, 2006, pp. 13-17 |
| 1019 | Fasoli et al., "Overview and status of bottom-up silicon nanowire electronics," *Materials Science in Semiconductor Processing*, Vol. 15, Issue 6, 2012, pp. 601-614 |
| 1020 | U.S. Patent Publication No. 2015/0264548 A1 to Lee et al. ("Lee 548") |
| 1021 | U.S. Patent No. 9,530,866 to Zhang et al. |
| 1022 | Plummer et al., "Silicon VLSI Technology: Fundamentals, Practice and Modeling" (2000) |
| 1023 | Certified Translation of KR 101487746 B1 to Lee et al. (including original Korean patent document) |
| 1024 | U.S. Patent Publication No. 2017/0154892 to Oh |

## IV. UNDERSTANDING OF THE LAW

20. I am not an attorney, but have been instructed in and applied the law as described in this section.

21. I understand that the first step in comparing an asserted claim to the prior art is for the claim to be properly construed. I address how a person of ordinary skill in the art (POSITA) would have understood the claims of the alleged invention in Section V below.

22. I have been further instructed and understand that a patent claim is unpatentable and invalid as obvious if the subject matter of the claim as a whole would have been obvious to a POSITA of the claimed subject matter as of the time of the invention at issue. I understand that when assessing the obviousness of claimed subject matter, the following factors are evaluated: (1) the scope and content of the prior art; (2) the difference or differences between each claim of the patent and the prior art; and (3) the level of ordinary skill in the art at the time the patent was filed.

23. I understand that claimed subject matter may be obvious in view of more than one item of prior art. I understand, however, that it is not enough to show simply that all the limitations of the claimed subject matter are spread throughout the prior art. Instead, for claimed subject matter to be obvious over multiple references, there must be some reason or motivation for a POSITA to combine the prior art references to arrive at the claimed subject matter.

24. I have been informed that, in seeking to determine whether an invention that is a combination of known elements would have been obvious to a POSITA at

the time of the invention, one must consider the references in their entirety to ascertain whether the disclosures in those references render the combination obvious to such a person.

25. I have been informed and understand that, while not required, the prior art references themselves may provide a teaching, suggestion, motivation, or reason to combine. The motivation linking two or more prior art references can also come from other sources, including, for instance, economic or market demand or the common sense of a POSITA at the time of the invention.

26. I understand that a particular combination may be proven obvious by showing that it was obvious to try the combination. I have been informed that, if a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

27. I further understand that an obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references also may be supplied by the direction of the marketplace. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a POSITA has good reason to pursue the known options within his or her technical

grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

28. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. Thus, where all the elements of a claim are used in substantially the same manner, in devices in the same field of endeavor, the claim is likely obvious.

29. Additionally, I understand that a patent is likely to be invalid for obviousness if a POSITA can implement a predictable variation or if there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. Therefore, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.

30. I further understand that combining embodiments related to each other in a single prior art reference would not ordinarily require a leap of inventiveness.

31. I also understand that a POSITA must have had a reasonable expectation of success when combining references for claimed subject matter to be obvious.

32. I have been informed and I understand that factors referred to as "objective indicia of non-obviousness" or "secondary considerations" are also to be

considered when assessing obviousness when such evidence is available. I understand that these factors can include: (1) commercial success; (2) long-felt but unresolved needs; (3) copying of the invention by others in the field; (4) initial expressions of disbelief by experts in the field; (5) failure of others to solve the problem the claimed subject matter solved; and (6) unexpected results.

33. I also understand that evidence of objective indicia of non-obviousness must be commensurate in scope with the claimed subject matter. I further understand that there must be a relationship, sometimes referred to as a "nexus," between any such secondary indicia and the claimed invention.

34. Finally, I have been informed that one cannot use hindsight to determine that an invention was obvious.

35. I provide my opinions in this declaration based on the guidelines set forth above.

## V. LEVEL OF SKILL IN THE ART

36. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA may have for combining references.

37. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the

inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the relevant field. I have been further informed and understand that a person of ordinary skill in the art (POSITA) is also a person of ordinary creativity.

38. In my opinion, a POSITA in the field of the ’291 patent would have had had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).

39. In my opinion, this POSITA would have been aware of and generally knowledgeable about 3D NAND’s structure, how it is manufactured, and its component parts.

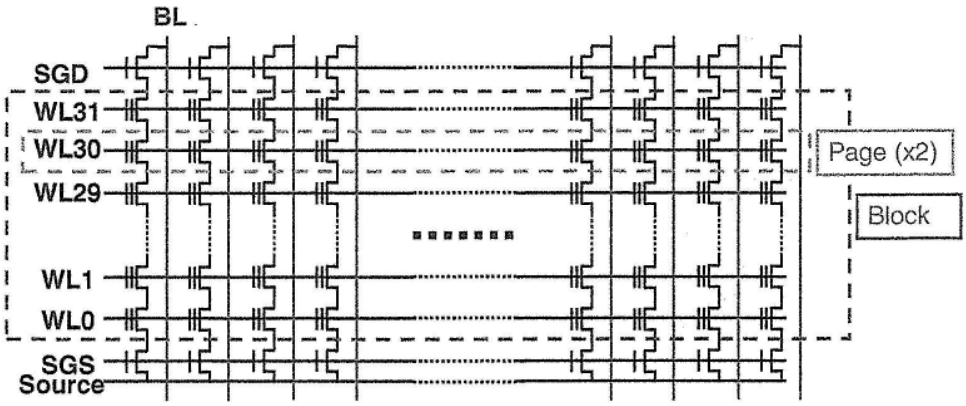
40. In view of my educational background and work experience, I was a person of more than the ordinary level of skill in the art as of March 2017. In forming my opinion, I have drawn on my academic background and professional experiences. My opinions herein, however, were formed by taking into account the perspective of an ordinarily skilled artisan.

## VI. TECHNOLOGICAL BACKGROUND

41. Before addressing the ’291 patent in detail, some background on the technology of the ’291 patent should be considered.

42. The ’291 patent and the prior art references discussed in this Declaration relate to methods of fabricating three-dimensional (3D) memory devices, such as 3D NAND memory devices.

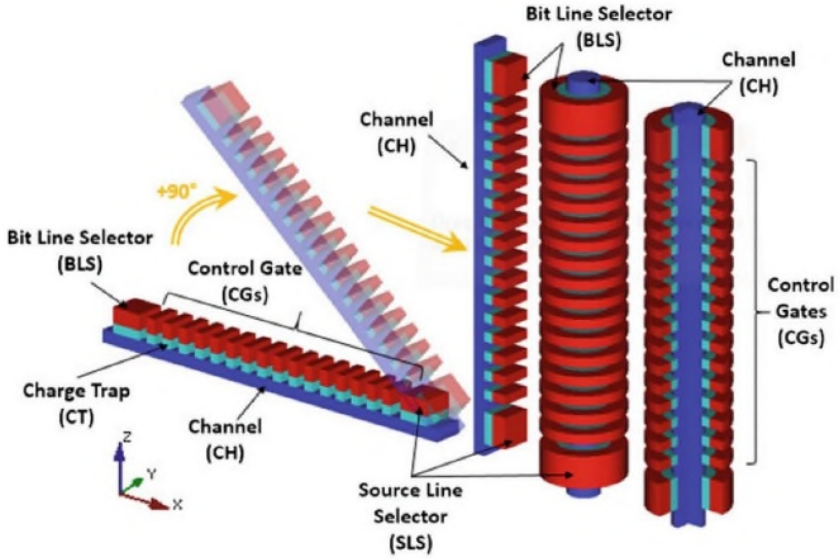
43. Central to NAND memory devices is a “memory cell,” which stores information as electrical charge. In these devices, NAND memory cells are arranged in “strings” having multiple cells “connected in series.” Ex. 1009, 38. Early NAND memory devices were formed as two-dimensional arrays of cells on a substrate surface. *Id.*, 58.



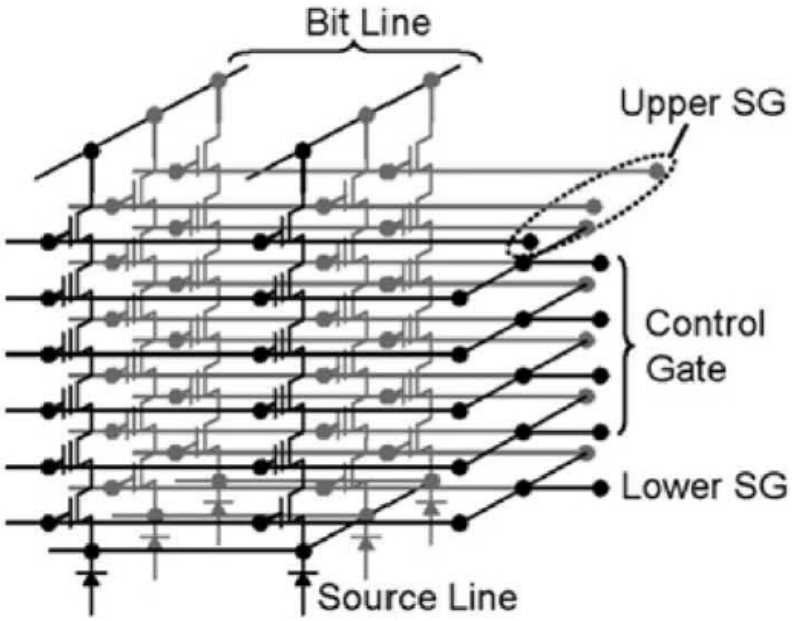

*Id.*, 40 (Fig. 2.4).

44. “[T]o further scale down the memory cell size,” “three-dimensional (3D) NAND flash cells” were developed. Ex. 1009, 292. “Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string

building block" and "turning the 2D NAND string upside," "resulting" in a "3D structure" with a "vertical channel." Ex. 1010, 3.




Ex. 1011, 122 (Fig. 5.2) (colors in the original). Multiple such vertical channels are repeated in a three-dimensional array:



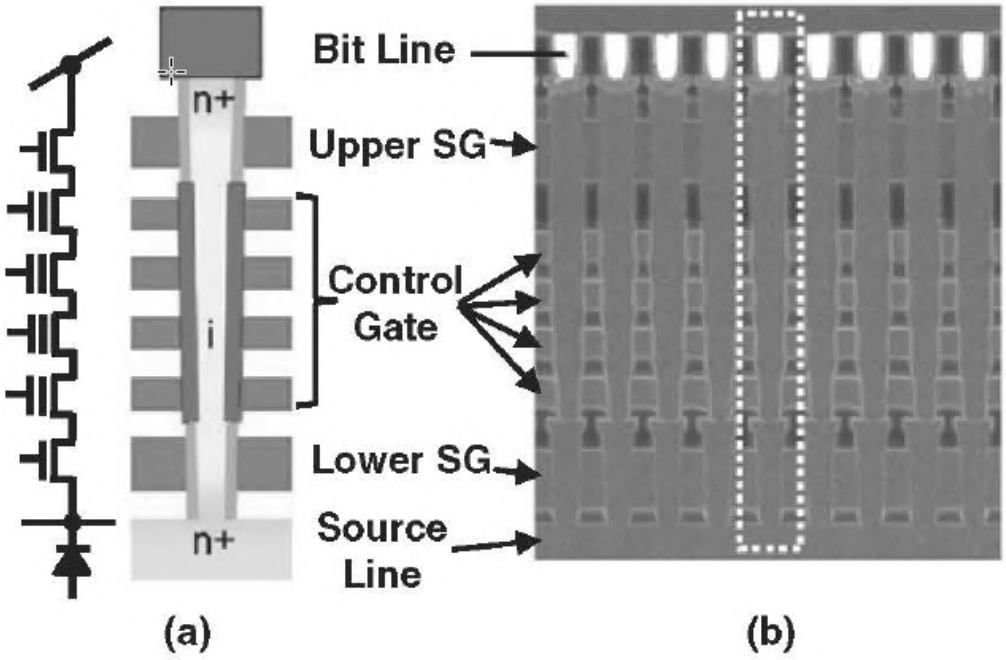

Ex. 1009, 296 (portion of Fig. 7.7).

45. A voltage applied on the control gate (which is also known as the word line) of each cell and the information stored in the cell (*e.g.*, binary 0 or 1 for a one-bit memory cell) determine whether the cell turns on or off. Specifically, the electrical charge (representing information) stored in the cell determines a threshold voltage of the cell, and the cell turns on when the control gate voltage is greater than the threshold voltage. Electrical current can only flow through a string when all cells in the string are turned on. Therefore, by applying a control gate voltage sufficient to turn on all but one cell (the selected cell) in a string and applying a suitable voltage to the control gate of the selected cell, the information stored in the selected cell may be determined using the amount of current flow through the string. This process is repeated by selecting a different cell to read (as an example operation) in the next cycle, eventually retrieving the requested information from the cells that store it.

46. A particular vertical memory cell "string is selected by a bit line and an upper select gate (upper SG)." Ex. 1009, 295-96. A memory cell "is located in the intersection of a control gate plate" and the channel of the string. *Id.* The lowest layer is a "select gate (lower SG)," which allows the strings to connect to a lower "common source." *Id.*, 295, 297. An example 3D NAND vertical memory cell string is shown below:

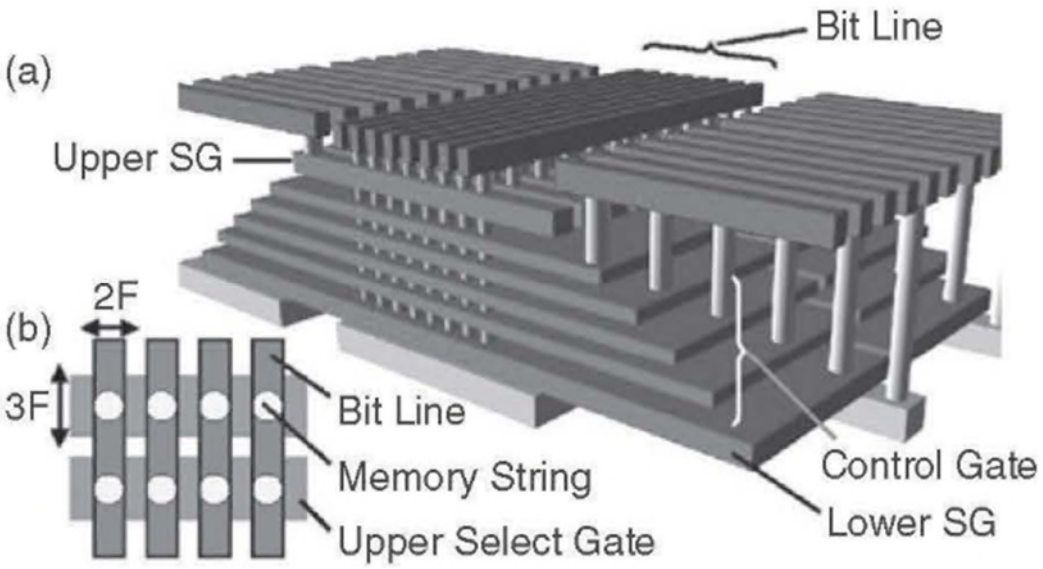


**Micron Ex. 1003, p. 27**
**Micron v. YMTC**
**IPR2025-00244**




*Id.*, 296 (Fig. 7.5).

47. 3D NAND memory devices include "multi-stacked layers of [control] gate (plate)" material alternated with "dielectric" (insulator of direct current) in a "[s]tack." Ex. 1009, 294. A "through-hole[]" channel (which is also known as a channel structure) "filled by memory film … and channel poly-Si" passes through the layers to form a string of vertically arranged memory cells. *Id.*, 295. "Each" layer of "electrode plate acts as a control gate." *Id.* "[T]he control gates … are connected … [in a] stair-like gate structure." *Id.*, 295-97.




Ex. 1009, 296 (Fig. 7.6).

48. Vertical conductive structures couple the control gates to control voltages. The steps of the staircase structure provide landing areas for the vertical conductive structures to contact the control gates. Ex. 1009, 298.

49. An example of one such staircase structure is shown in the figure below from Ex. 1012 (U.S. Pat. No. 10,475,737). To access each memory cell via its control gate (also known as a word line), contacts (item 60 in the figure) are connected to landing pads at the end of each of the different control gates:

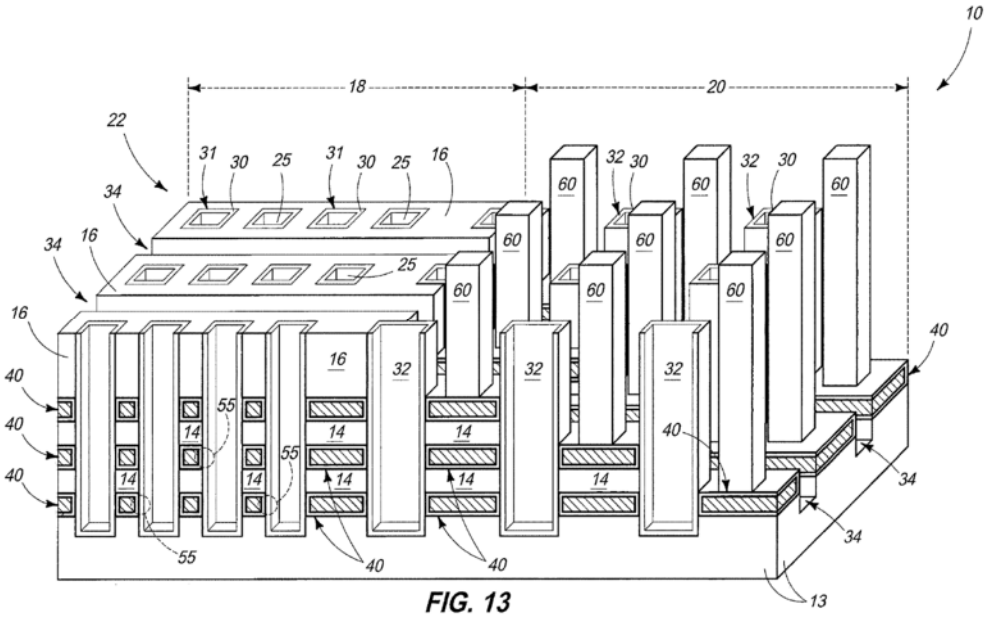



FIG. 13

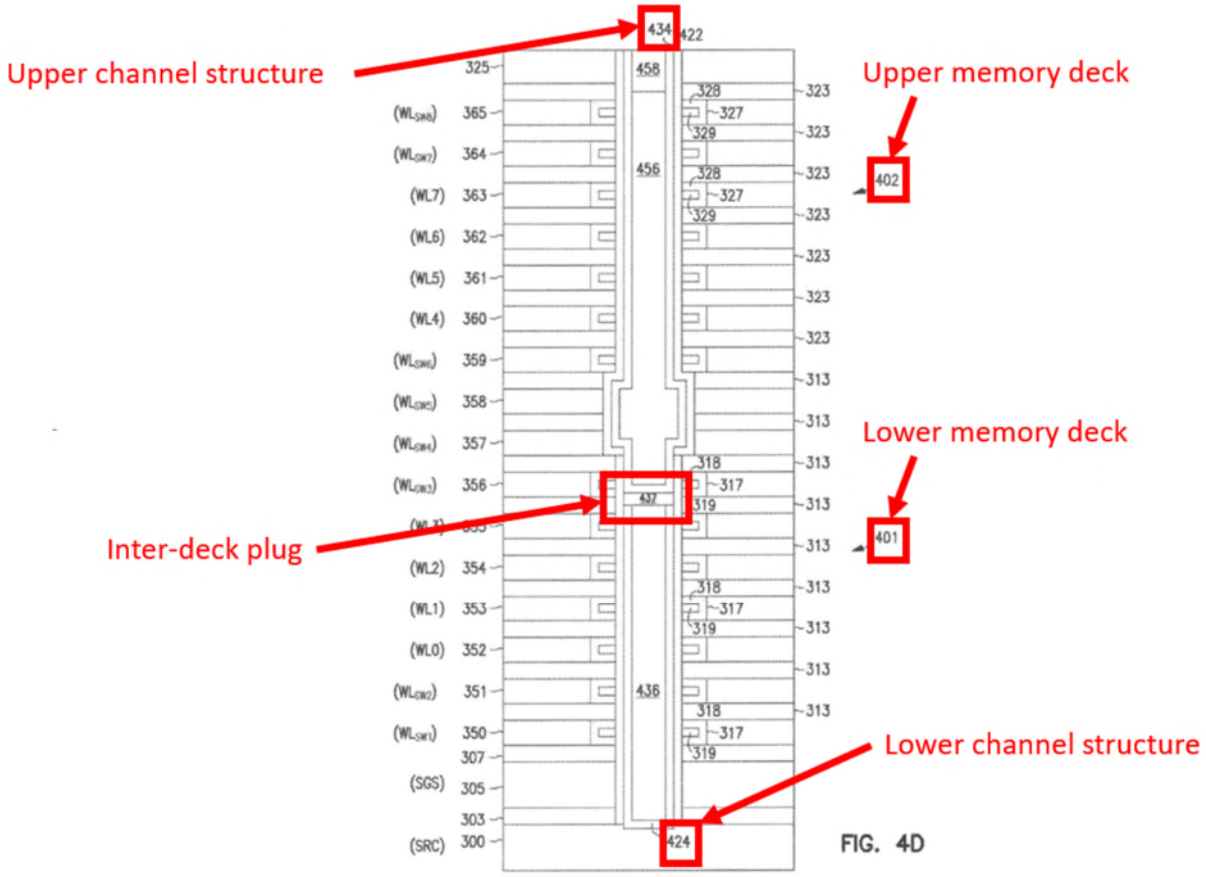
*Id.*, Fig. 13, 4:56-64, 8:45-56.

50. At the time the ’291 patent was filed, multi-deck 3D memory devices were also well-known. A “multi-deck” device is one that includes two memory stacks one on top of the other.

51. A POSITA would have recognized that the motivation behind the use of such a multi-deck structures is the difficulty in etching high aspect ratio channel holes of increased depth. This challenge became a limiting factor to memory density: as more layers are added it becomes more difficult to etch the channel holes. Ex. 1013, 211-215.

52. A multi-deck structure, however, avoids this problem and enables high aspect ratio channel holes to be more readily formed. In such a structure, the first deck is formed first and a hole is etched through the first deck. Then the second

deck is formed on top of the first deck, and another hole is etched through the second deck. The resulting structure includes two channel structures (each also known as a sub-channel structure) that connect via an interface, e.g., inter-deck plug. Because the two sub-channels were created via separate etching steps—that passed through only a subset of layers—etching can be more readily accomplished. An example one such structure is shown below:




Ex. 1014 (U.S. Pat. 9,853,046), Fig. 4D (annotated).

## VII. THE ’291 PATENT

### A. Effective Filing Date

53. I understand that the application leading to the ’291 patent was filed on July 26, 2018.

54. Based on my review of the ’291 patent, I note that it identifies itself as a continuation of a PCT application filed March 1, 2018. It also identifies two foreign applications filed March 8, 2017.

55. For purposes of this declaration, I have been instructed to use March 8, 2017 as the effective filing date of the ’291 patent. My opinions in this declaration were formed from the perspective of a POSITA as of March 8, 2017, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the prior art.

### B. Overview

56. The ’291 Patent is entitled “Joint opening structures of three-dimensional memory devices and methods for forming the same.” Ex. 1001, Title.

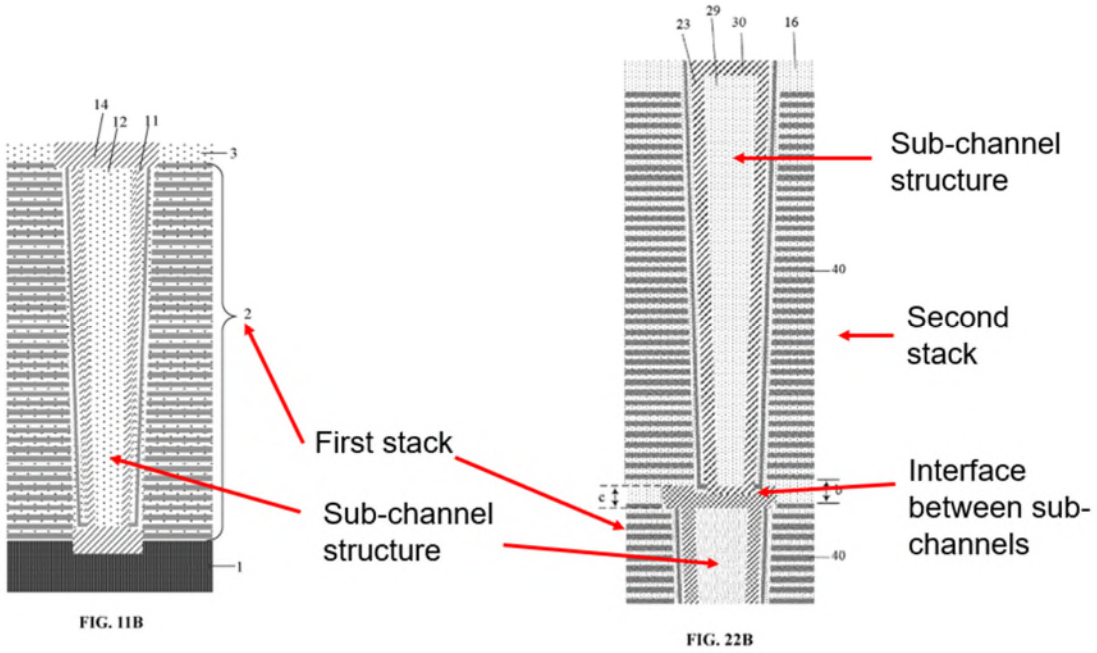
57. The patent relates generally to multiple-stack three-dimensional (3D) memory devices, *e.g.* 3D multiple-stack NAND devices. Ex. 1001, 1:15-35.

58. The patent explains that “3D NAND memory devices [] keep scaling more oxide/nitride (ON) layers” due to advances in semiconductor technology, creating difficulty in “us[ing] a single etching process to form the channel holes” as

the depth (i.e., number of layers) increases. *Id.* "Thus, a single etching method may not be efficient in both cost and process capability." *Id.*, 1:34-35.

59. The patent then goes on to propose a multiple-stack structure employing certain joint opening structures, and methods for forming the same. *See generally* Ex. 1001.

60. More particularly, the '291 patent proposes a first memory stack (*e.g.*, the stack shown in Figure 11B reproduced below), forming a sub-channel structure therein, forming a second memory stack on the first stack (*e.g.*, the upper stack shown in Figure 22B), and forming a sub-channel structure therein that connects to the first sub-channel via an interface:




Ex. 1001, Figs. 11B (annotated), 22B (annotated).

61. As I will discuss in greater detail below when comparing the claims to the prior art, the ’291 patent’s claims refer to the features that comprise the above sub-channels and interface therebetween as the first, second, third, fourth, and fifth channel structures, the first and second functional layers, and the first and second filling structures.

### C. Prosecution History

62. As noted above, I have reviewed the ’291 patent’s prosecution history.

63. During prosecution of the application underlying the ’291 patent, claims 11 and 13-19 were rejected as obvious over a reference to U.S. Pub. 2013/0109158 (“Lee ’158) in view of U.S. Pub. 2013/0203227 (“Huo”). Ex. 1002, 682, 684.

64. On April 1, 2020, Applicant made numerous arguments against Examiner’s rejections to independent claim 11. Specifically, Applicant argued that “claim 11 recites at least the below features that distinguish over the applied references:



Micron Ex. 1003, p. 34
Micron v. YMTC
IPR2025-00244

> a third channel structure in contact with the second channel structure disposed over the first through hole, wherein **a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate**;
>
> …
>
> **a fifth channel structure in contact with a fourth channel structure disposed over the second through hole**,

Ex. 1002, 706 (emphasis in original).

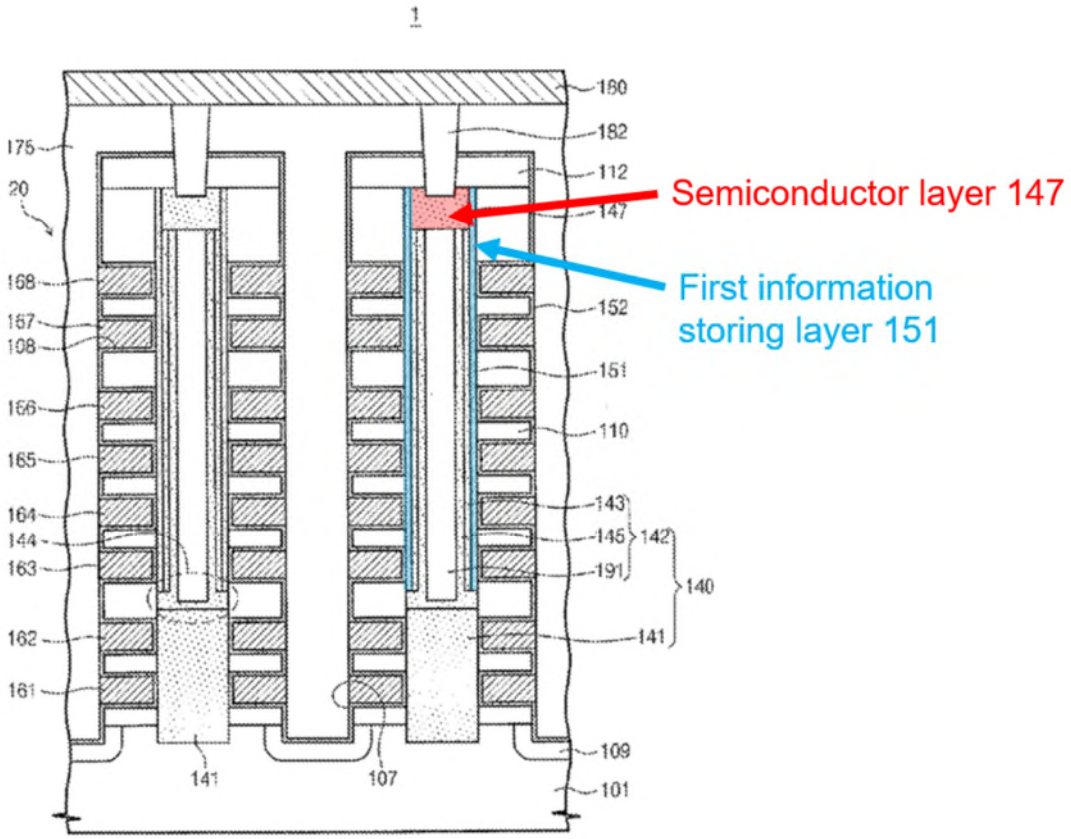
65. Applicant went on to elaborate that in Lee ’158, semiconductor layer 147 does not “cover [the] projection of the first through hole” as the claim requires because it is “within” the first through hole (channel hole 103) and “encircled by” the first information storing layer 151. Ex. 1002, 707.

66. In other words, as shown in the below annotated version of Figure 1P of Lee ’158, semiconductor layer 147 (annotated red) does not—according to the applicant—“cover” the “through hole” because it is within, does not meet the walls of, and is separated from the walls of the through hole by layer 151 (annotated blue):



**Micron Ex. 1003, p. 35**
**Micron v. YMTC**
**IPR2025-00244**

Fig. 1P




Ex. 1002, 708 (Fig. 1P) (annotated).

67. Regarding the claimed fifth channel structure, Applicant argued that Huo—the secondary reference relied on by the Examiner—does not disclose a fifth channel structure in contact with the fourth channel structure. Moreover, because the lower and upper sub-channels are distinct and different structures in Huo, the Examiner improperly assumed that there would be an element of the lower sub-channel on the upper sub-channel. Ex. 1002, 708-09.

68. This then led the Examiner to allow the claims. In so doing, the Examiner pointed to the same claim language cited by the applicant. Ex. 1002, 722-23.

**D. Claims**

69. For reference, claims 1-12, and 14-20 of the ’291 patent are reproduced below:

> **1**. A method of forming a joint opening structure in a three-dimensional (3D) memory device, comprising:
>
> forming a first stacked layer and forming a first insulating connection layer on the first stacked layer;
>
> forming a first through hole that penetrates the first stacked layer and the first insulating connection layer;
>
> forming a first channel structure overlaying the surface of the substrate that is exposed by the first through hole;
>
> forming a first functional layer on the sidewall of the first through hole;
>
> forming a second channel structure and forming a first filling structure on the sidewall of the first functional layer and the exposed surface of the first channel structure;
>
> forming a third channel structure in contact with the second channel structure above the first through hole, wherein a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate;



**Micron Ex. 1003, p. 37**
**Micron v. YMTC**
**IPR2025-00244**

forming a second stacked layer and forming a second insulating connection layer on the first insulating connection layer;

forming a second through hole that penetrates the second stacked layer and the second insulating connection layer, wherein a projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate;

forming a second functional layer on the sidewall of the second through hole;

forming a fourth channel structure and forming a second filling structure on the sidewall of the second functional layer and the exposed surface of the third channel structure; and

forming a fifth channel structure in contact with the fourth channel structure above the second through hole.

**2**. The method of claim **1**, wherein:

the first stacked layer includes a first number of oxide/nitride layer pairs; and

the second stacked layer includes a second number of oxide/nitride layer pairs.

**3**. The method of claim **2**, wherein:

the first number and the second number are not less than 32.

**4**. The method of claim **1**, wherein forming the first functional layer comprises:



**Micron Ex. 1003, p. 38**
**Micron v. YMTC**
**IPR2025-00244**

forming a first tunneling layer on the sidewall of the first through hole and the exposed surface of the first channel structure, wherein the first tunneling layer is configured, in operation, to generate charges;

forming a first storage layer on the surface of the first tunneling layer to store the charges generated by the first tunneling layer;

forming a first barrier layer on the surface of the first storage layer to block the outflow of charges in the first storage layer;

forming a first passivation layer on the surface of the first barrier layer to protect the first barrier layer from being damaged in a subsequent removal process; and

removing portions of the first passivation layer, the first barrier layer, the first storage layer, and the first tunneling layer on the surface of the first channel structure, wherein remaining portions of the first passivation layer, the first barrier layer, the first storage layer, and the first tunneling layer on the sidewall of the first through hole to form the first functional layer.

**5**. The method of claim **4**, wherein forming the second channel structure and the first filling structure comprises:

forming a second channel layer that covers the sidewall of the first passivation layer and the exposed surface of the first channel layer;

forming the first filling layer that covers the surface of the second channel layer;



**Micron Ex. 1003, p. 39**
**Micron v. YMTC**
**IPR2025-00244**

removing a portion of the first filling layer to form the first filling structure, wherein the top surface of the first filling structure is lower than the top surface of the first insulating connection layer; and

removing a portion of the second channel layer to form the second channel structure, wherein a top surface of the second channel structure is lower than a top surface of the first insulating connection layer.

**6**. The method of claim **1**, wherein forming the third channel structure comprises:

etching the first insulating connection layer to form a first groove, wherein a projection of the first groove on the substrate covers the projection of the first through hole on the substrate;

forming a third channel layer in the first groove, wherein the third channel layer is in contact with the second channel structure; and

planarizing the top surfaces of the first insulating connection layer and the third channel layer to form the third channel structure.

**7**. The method of claim **1**, wherein forming the third channel structure comprises:

etching the first insulating connection layer and at least a portion of the top nitride layer of the first stacked layer to form a first groove, wherein a projection of the first groove on the substrate covers the projection of the first through hole on the substrate;

forming the third channel structure in the first groove, wherein the



**Micron Ex. 1003, p. 40**
**Micron v. YMTC**
**IPR2025-00244**

third channel structure is in contact with the second channel structure; and

planarizing the top surfaces of the first insulating connection layer and the third channel structure.

**8**. The method of claim **1**, further comprising:

forming a first mask layer overlaying the first insulating connection layer before forming the first through hole; and

removing the first mask layer after forming the first filling structure;

forming a second mask layer on the second insulating connection layer before forming the second through hole; and

removing the second mask layer after forming the second filling structure.

**9**. The method of claim **1**, wherein forming the fourth channel structure and the second filling structure comprises:

forming a fourth channel layer that covers the sidewall of a second functional layer and the exposed surface of the third channel layer;

forming a second filling layer that covers the surface of the fourth channel layer;

removing a portion of the second filling layer to form the second filling structure, wherein the top surface of the second filling structure is lower than the top surface of the second insulating connection layer; and



**Micron Ex. 1003, p. 41**
**Micron v. YMTC**
**IPR2025-00244**

removing a portion of the fourth channel layer to form the fourth channel structure, wherein a top surface of the fourth channel structure is lower than a top surface of the second insulating connection layer.

**10**. The method of claim **1**, wherein forming the fifth channel structure comprises:

etching the second insulating connection layer to form a second groove, wherein a projection of the second groove on the substrate covers the projection of the second through hole on the substrate;

forming a fifth channel layer in the second groove, wherein the fifth channel layer is in contact with the fourth channel structure; and

planarizing the top surfaces of the second insulating connection layer and the fifth channel layer to form the fifth channel structure.

**11**. A joint opening structure of a three-dimensional (3D) memory device, comprising:

a first stacked layer disposed overlaying a substrate;

a first insulating connection layer disposed on the first stacked layer;

a first through hole penetrating the first stacked layer and the first insulating connection layer;

a first channel structure disposed at the bottom of the first through hole and overlaying the substrate;

a first functional layer disposed on the sidewall of the first through



**Micron Ex. 1003, p. 42**
**Micron v. YMTC**
**IPR2025-00244**

hole;

a second channel structure in contact with the first channel structure disposed on the sidewall of the first functional layer;

a third channel structure in contact with the second channel structure disposed over the first through hole, wherein a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate;

a second stacked layer disposed on the third channel structure;

a second insulating connection layer disposed on the second stacked layer;

a second through hole penetrating the second stacked layer and the second insulating connection layer, wherein a projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate;

a second functional layer disposed on the sidewall of the second through hole;

a fourth channel structure in contact with the third channel structure disposed on the sidewall of the second functional layer; and

a fifth channel structure in contact with the fourth channel structure disposed over the second through hole.

**12**. The joint opening structure of claim **11**, further comprising:

a first filling structure covering the surface of the second channel structure; and

a second filling structure covering the surface of the fourth channel



**Micron Ex. 1003, p. 43**
**Micron v. YMTC**
**IPR2025-00244**

structure;

wherein the first through hole is non-interconnected with the second through hole.

**14**. The joint opening structure of claim **11**, wherein:

the first stacked layer includes a first number of conductor/dielectric layer pairs; and

the second stacked layer includes a second number of conductor/dielectric layer pairs.

**15**. The joint opening structure of claim **14**, wherein:

the first number and the second number are not less than 32.

**16**. The joint opening structure of claim **11**, wherein:

the first stacked layer includes a first number of oxide/nitride layer pairs; and

the second stacked layer includes a second number of oxide/nitride layer pairs.

**17**. The joint opening structure of claim **16**, wherein:

the first number and the second number are not less than 32.

**18**. The joint opening structure of claim **11**, wherein:

a thickness of the third channel structure is in a range between 30 nm and 70 nm.

**19**. The joint opening structure of claim **11**, wherein:

a size difference between a top aperture and a bottom aperture of the first through hole is equal to or less than 30 nm; and

a size difference between a top aperture and a bottom aperture of the second through hole is equal to or less than 30 nm.

**20**. A joint opening structure of a three-dimensional (3D) memory device, comprising:

a first stacked layer disposed overlaying a substrate;

a first insulating connection layer disposed on the first stacked layer;

a second stacked layer disposed on the first insulating connection layer;

a second insulating connection layer disposed on the second stacked layer;

a plurality of channel holes in a first region of the 3D memory device;

a plurality of staircase structure dummy holes in a second region of the 3D memory device; and

a plurality of through array contact barriers in a third region of the 3D memory device;

wherein each of the plurality of channel holes includes:

a first through hole penetrating the first stacked layer and the first insulating connection layer,

a first channel structure disposed at the bottom of the first through hole and overlaying the substrate,



**Micron Ex. 1003, p. 45**
**Micron v. YMTC**
**IPR2025-00244**

a first functional layer disposed on the sidewall of the first through hole,

a second channel structure in contact with the first channel structure disposed on the sidewall of the first functional layer,

a third channel structure in contact with the second channel structure disposed over the first through hole, wherein a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate,

a second through hole penetrating the second stacked layer and the second insulating connection layer, wherein a projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate,

a second functional layer disposed on the sidewall of the second through hole,

a fourth channel structure in contact with the third channel structure disposed on the sidewall of the second functional layer, and

a fifth channel structure in contact with the fourth channel structure disposed over the second through hole.

## VIII. CLAIM CONSTRUCTION

70. I am not a legal expert or an attorney and offer no opinions on the law. I understand that claim construction is a matter of law. However, I have been informed by counsel of the legal standards that apply to claim construction in an *inter partes* review, and I have applied them in forming my opinions. I understand

that during an *inter partes* review, the same claim construction standard used in federal district court is applied when addressing the meaning of claim terms.

71. I have been informed that the words of a claim are generally given their plain and ordinary meaning that the term or phrase would have to POSITA at the time of the invention in view of the surrounding claim language, the specification and the file history (collectively, the "intrinsic evidence" or "intrinsic record").

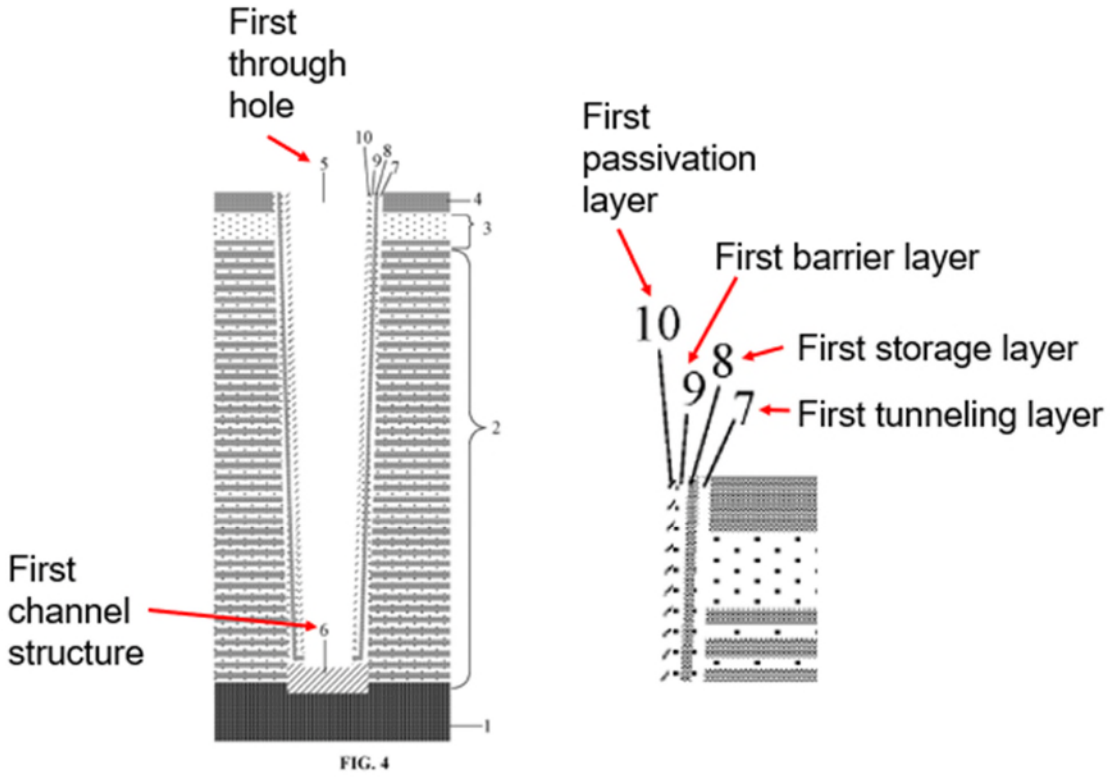
72. I also understand that courts may consider extrinsic evidence, such as expert and inventor testimony, dictionaries, and learned treatises (collectively, the "extrinsic evidence" or the "extrinsic record"), but that such extrinsic evidence should be given less weight than the intrinsic evidence.

73. In my opinion, the terms of the '291 patent's claims do not require further construction and can—with the exception of claim 4 as discussed in the following paragraphs—be afforded their plain and ordinary meaning for purposes of the analysis of the prior art that I am conducting in this declaration. I have provided further discussion of how a POSITA would have understood the '291 patent's claim terms in the sections below.

74. Claim 4 requires that the step of "forming" the "first functional layer" of claim 1 entail "forming" a series of ordered layers, including: (1) "a first tunneling layer on the sidewall of the first through hole and the exposed surface of the first channel structure;" (2) "a first storage layer on the surface of the first tunneling

layer;" (3) "a first barrier layer on the surface of the first storage layer;" and (4) "a first passivation layer on the surface of the first barrier layer."

75. The ordering of this "first the functional layer" of claim 4 is shown in the below annotated version of Figure 4 (first tunneling layer 7 is immediately adjacent to the sidewall of the through hole while all the other layers are located sequentially inside layer 7):




Ex. 1001, Fig. 4 (full and partial) (annotated).

76. This same layer ordering is discussed in the specification. First, tunneling layer (7) is formed on the sidewall of first through hole (5) and on the top surface of first channel structure (6). Ex. 1001, 10:44-55. Then, the storage layer

(8) is formed on the surface of the tunneling (7), the barrier layer (9) is formed on the surface of the storage layer (8), the passivation layer (10) is formed on the surface of the storage layer (8), and portions of (7)-(10) on the first channel structure (6) are removed. *Id.*, 10:44-11:17.

77. Claim 4's "functional layer" requires Figure 4's ordering of layers because it requires "forming a ***first tunneling layer*** **<u>on</u>** the ***sidewall of the first through hole***," "forming a ***first storage layer*** **<u>on</u>** the ***surface of the first tunneling layer***," etc. Ex. 1001, Claim 4 (emphasis added).

78. Put another way, the claim itself requires (just as the '291 patent's specification shows and its specification describes) that the tunneling layer must be formed on outside of the hole (*i.e.*, nearest the gate layers). If this were not the case, this layer would not be formed "on the sidewall of the first through hole." Nor would the storage layer be formed "on the surface of the first tunneling layer." The same is true for the following barrier and passivation layers.

79. I understand that YMTC interprets claim 4 such that it embraces forming the three outer layers (*i.e.*, outer being towards the gate layers) in the reverse order, such that from outside of the hole (*i.e.*, nearest the gate layers) to the inside of the hole the layers are formed in the following order: barrier layer, storage layer, tunneling layer, and passivation layer. *See, e.g.*, Ex. 1015, Ex. C-1, YMTC's Contentions, 31-33.

80. Put another way, I understand that as YMTC interprets claim 4, (1) the claimed steps may be performed out of order, and (2) a layer X can be considered to be formed on a layer Y even if when layer X is formed, layer Y does not yet exist. *See, e.g.,* Ex. 1015, Ex. C-1, YMTC's Contentions, 31-33 (showing that in the accused product, when the alleged "first storage layer" is formed, the "tunneling layer" has yet to be deposited).

81. In my opinion, this interpretation is contrary to the plain and ordinary meaning of claim 4: it reads out the requirement of "forming" particular layers "on" on other layers or the through hole. Moreover, there is nothing about the specification that would lead to any different claim construction: just like the claims, the specification uses the phrase "forming … on" in its ordinary sense.

82. Nevertheless, and while I believe YMTC's construction is wrong, I have employed the construction in this declaration. As I explain below, Costa discloses the exact ordering (and forming thereof) of layers that YMTC asserts falls within the scope of claim 4.

## IX. UNPATENTABILITY ANALYSIS

83. For the reasons I explain in greater detail below, it is my opinion that as of the effective filing date of the '291 patent, a POSITA would have considered Claims 1-12 and 14-20 of the '291 patent to be unpatentable as obvious over the prior art discussed in this declaration.

## A. Overview of the Prior Art

84. The following paragraphs provide an overview of the main prior art references I discuss throughout this declaration.

### 1. Costa

85. Costa (Ex. 1005) indicates on its face that it was filed February 28, 2017. *See* Costa, Cover. In view of this date filing, which is before the '291 patent's own March 2017 effective filing date, I understand that Costa is prior art under 35 U.S.C. § 102(a)(2).

86. Costa relates generally to "multi-tier three-dimensional memory devices containing dummy memory cells for providing inter-tier connection and methods of making the same. Costa, [0002].

87. Costa discloses forming a vertical memory channel (shown in green in the annotated version of Figure 21G below) in a multi-tier three-dimensional memory structure:

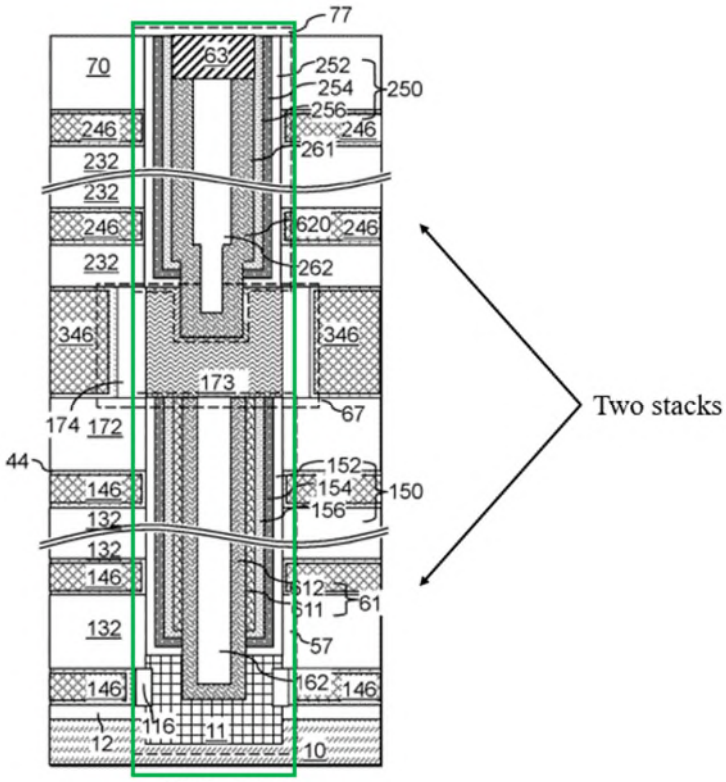


FIG. 21G

Costa, Fig. 21G (annotated).

88. Costa also explains "challenges for fabricating a multi-tier memory stack structure include formation of memory openings having high aspect ratios and alleviation of effects of misalignment of tier-level memory openings formed in different tier structures." Costa, [0003].

89. Because of this, Costa provides methods "for providing a reliable connection between vertically neighboring memory stack structures." Costa, [0003].

90. Specifically, Costa discloses forming "first alternating stack (132, 142)" on substrate 10. Costa, [0126]-[0127].

91. First-tier insulating cap layer 172 is formed over the first alternating stack (132, 142) to form the first-tier structure (132, 142, 172), which can be patterned to form "a first terrace region" located in a contact region of the device. Costa, [0134]-[0135].

92. First-tier openings (149, 119) are then formed for example by lithographic patterning and an anisotropic etch process. Costa, [0137]. This is shown in Figure 3B below:

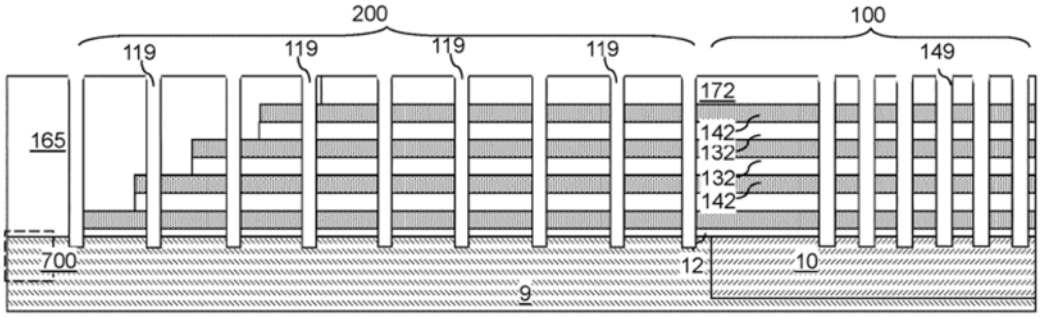



FIG. 3B

*Id.*, Fig. 3B.

93. A memory channel is formed in first-tier memory openings 149 by first forming epitaxial channel portion 11 in the bottom of each hole and subsequently forming a memory film 150, first outer and inner semiconductor channel layers (611, 612), and filling the remainder of the opening with dielectric core 162. Costa, [0141]-[0160]. Figure 4B shows one such memory channel:



Micron Ex. 1003, p. 53
Micron v. YMTC
IPR2025-00244

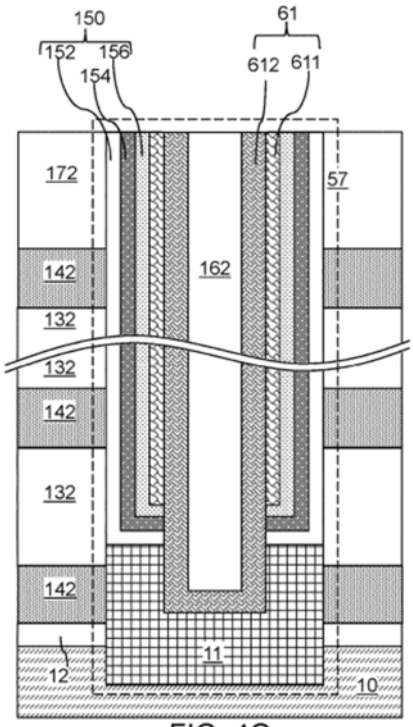


FIG. 4G

*Id.*, Fig. 4G.

94. In one embodiment, a joint-level doped semiconductor layer 173L is formed over the first-tier structure (*e.g.*, shown above in Fig. 4G) and subsequently patterned, removing the portions not over first-tier openings (149, 119), leaving joint-level doped semiconductor portion 173. Costa, [0263]-[0266], Figs. 20A-B.

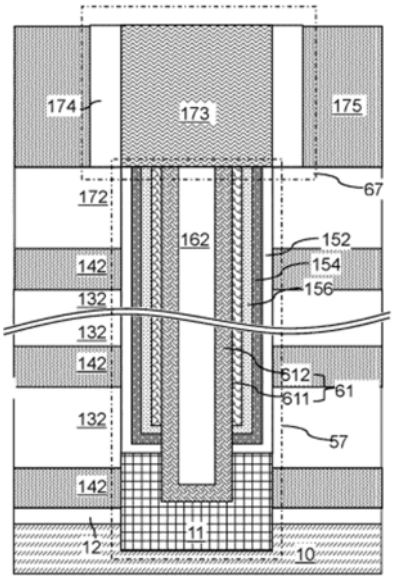
95. Costa states that "[i]n one embodiment, the bottom surface of each joint-level doped semiconductor portion 173 can contact an entire top surface of an underlying first memory opening fill structure 57." Costa, [0265].

96. Exposed portions of semiconductor portion 173 can be oxidized, converting those portions to dielectric material 174'. Costa, [0266], Fig. 20C. An annular dielectric spacer is formed by removing the top portion of 174'. *Id.*, [0268],

[0266] ("In an alternative embodiment shown in the dashed line inset in FIG. 20C, only the sidewalls of the joint-level doped semiconductor portions 173 are oxidized to form a first annular dielectric spacer 174."), Fig. 20C.

97. Joint-level spacer material 175 is then deposited over the first-tier structure and around semiconductor portion 173 and dielectric spacer 174. Costa, [0268]. This completed structure is shown below in Figure 20D:

FIG. 20D




*Id.*, Fig. 20D.

98. Per Costa, a second-tier structure and memory channel are formed in much the same way as the first-tier structure.

99. A second alternating stack (232, 242) is formed over joint level spacer 175, joint-level doped semiconductor portion 173, and dielectric spacer 174. Costa, [270], [0178]-[0180]. Second-tier insulating cap layer 70 is formed over the second

alternating stack and second-tier memory holes 249 are formed by a similar process to that of first-tier memory holes 149. *Id*., [0183]-[0192].

100. A memory channel is formed in second-tier memory openings 249 by forming a memory film 250 (comprised of layers 252, 254, 256), second outer and inner semiconductor channel layers (621, 622), and then filling the remainder of the opening with dielectric core 262. Costa, [0272]-[0276].

101. Drain region 63 is then formed in a recess etched into dielectric core 262 and second inner semiconductor channel layer 622). Costa, [0277]. Drain region 63 is deposited in and above the dielectric core cavity, and overlying material is planarized. *Id.*, [0212], [0277] (referring to [0212] description).

102. This results in a multi-tiered vertical memory channel (shown in green in Figure 21G below). Costa, [0278].



**Micron Ex. 1003, p. 56**
**Micron v. YMTC**
**IPR2025-00244**

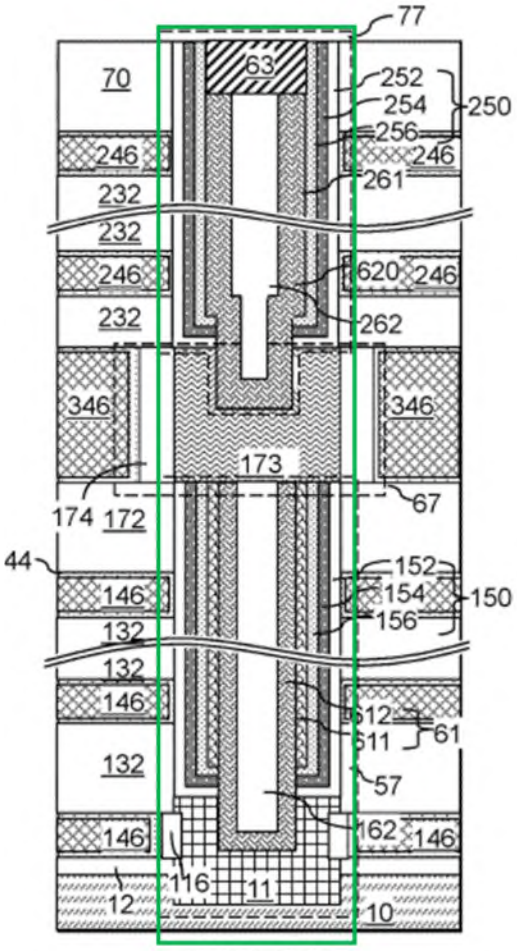


FIG. 21G

*Id*., Fig. 21G (annotated).

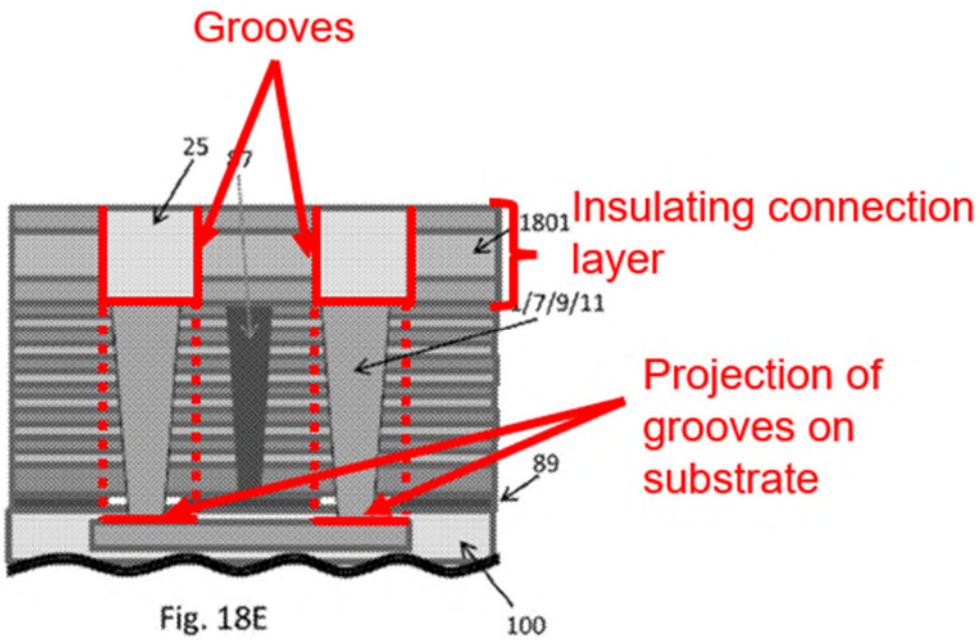
**2. Liu**

103. Liu (Ex. 1006) indicates on its face that was filed in the U.S. on March 24, 2016. Liu, Cover. In view of this date of filing, which pre-date the ’291 patent’s own March 2017 filing, I understand that Liu is prior art under AIA § 102(a)(2).

104. Liu relates to “three dimensional vertical NAND strings” and, more specifically, to facilitating “[a]lignment between memory openings through multiple tier structures [by] employing a temporary landing pad” with “a greater area than the

horizontal cross-section[]" of the first-tier memory opening. Liu, Abstract, Title, [0002].

105. In this regard, Liu discloses a process which entails depositing insulating layer 121A, boosting layer 1801, and insulating layer 121B over the first memory stack and subsequently creating a groove over the lower-level memory holes by an etching process. Liu, [0173]. This is shown in figure 18E below:




*Id.*, Fig. 18E (annotated).

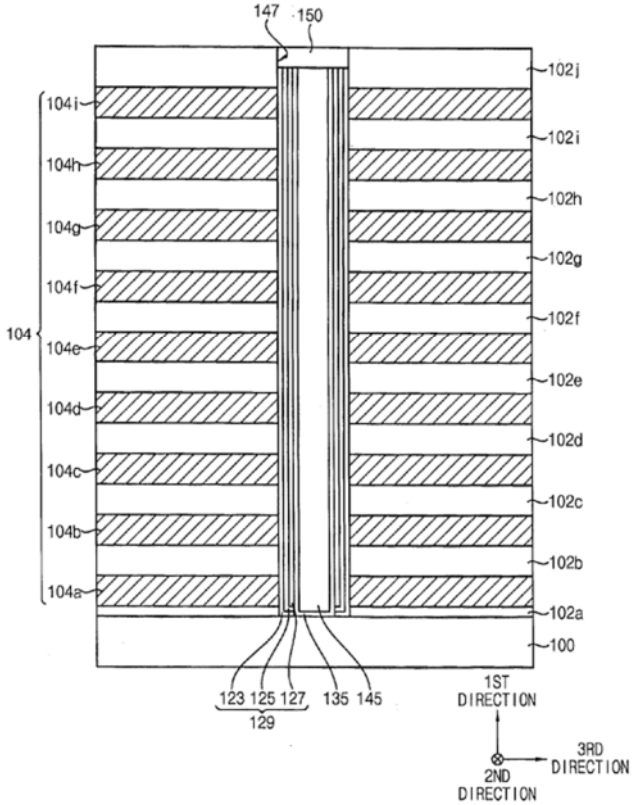
### 3. Lee

106. Lee (Ex. 1007) indicates on its face that it was filed in the U.S. on August 28, 2014 and published March 5, 2015. Lee, Cover. In view of these dates of filing and publication, both of which pre-date the '291 patent's own March 2017 filing, I understand that Lee is prior art under AIA §§ 102(a)(1) and 102(a)(2).

107. Lee relates to "[v]ertical memory devices and methods of manufacturing the same." Lee, Title.

108. Among other things, Lee discloses forming a doped polysilicon recessed pad 150 by forming a recessed groove atop the memory through hole. Lee, [0093]. Figure 8 below shows this pad 150:

FIG. 8



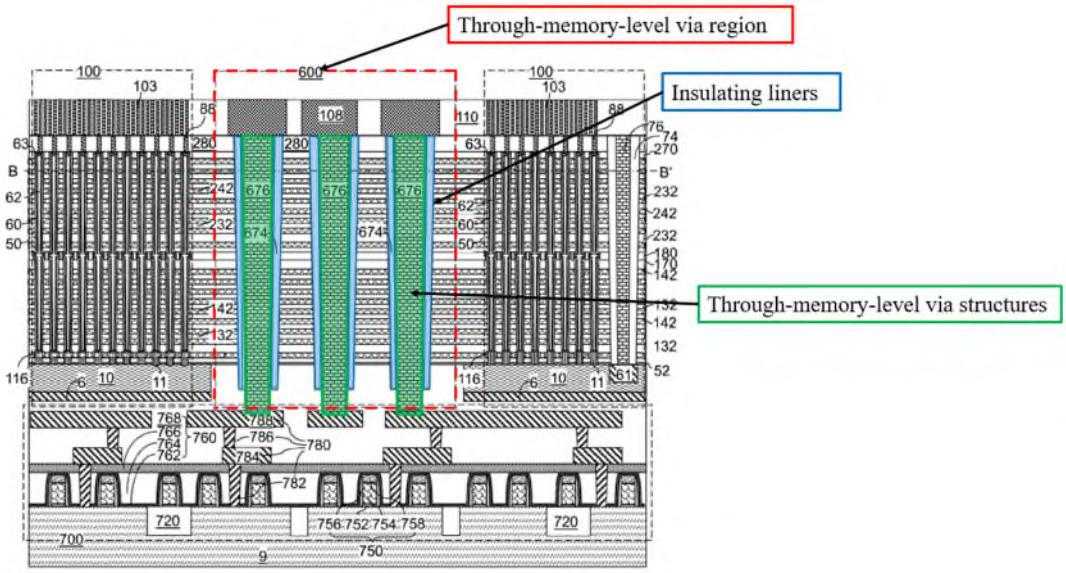

*Id.*, Fig. 8.

### 4. Toyama

109. Toyama (Ex. 1008) indicates on its face that it was filed in the U.S. on September 19, 2016. Toyama, Cover. As this date of filing pre-dates the '291 patent's own March 2017 filing, I understand that Toyama is prior art under AIA §102(a)(2).

110. Toyama relates to "three-dimensional non-volatile memory devices" and, like the '291 Patent, discloses a multi-tier memory structure. Toyama, Abstract, [0002], Figs. 49-50.

111. Toyama's device includes "through-memory-level via regions 600" that contain "through-memory-level via structures 676" (*i.e.*, through array contacts) and "insulating liners 674." Toyama, [0333], [0340]-[0342]. Figure 49 below shows this:




*Id.*, Fig. 49 (annotated).

### B. *Ground 1 (IPR2025-00244)*: Claims 1-5, 8-9, 11-12, and 14-19 Are Obvious Over Costa

112. In my opinion, a POSITA would have considered Costa to be within the scope of the prior art and highly relevant to the patentability of the ’291 patent’s claims.

113. In my opinion, when viewed and considered in light of the knowledge of a POSITA, Costa renders claims 1-5, 8-9, 11-12, and 14-19 of the ’291 patent obvious.

#### 1. Claim 1

***[1.Pre] “A method of forming a joint opening structure in a three-dimensional (3D) memory device, comprising:”***

114. In my opinion, to the extent the preamble is limiting it is taught by Costa.

115. Before summarizing Costa’s pertinent disclosures, I will walk through how the ’291 patent uses the term “joint opening structure.”

116. In the ’291 patent, “joint opening structure” refers to an opening structure of a three-dimensional (3D) memory device created by “combining two through hole formation processes.” Ex. 1001, 15:38-40.

117. In other words, this is simply a reference to the well-known technique of forming channel structures in multi-tier memory devices using two etch processes.

118. Moving on to Costa, Costa teaches forming a joint opening structure by etching a first memory through hole in a first stack (and forming a channel structure

therein), forming a second stack on the first stack, and etching a second memory through hole in the second stack (and forming a channel structure therein).

119. For instance, Costa explains that "[t]he present disclosure relates generally to the field of three-dimensional memory devices and specifically to multi-tier three-dimensional memory devices … and methods of making the same." Costa, [0002]. Likewise, it notes that it discusses "fabricating a multi-tier memory stack structure" and "providing a reliable connection between vertically neighboring memory stack structures." *Id.*, [0003]; *see also* Figs. 4A-4G, 10A-11F (showing first-tier opening (149, 119), and second-tier openings (249, 219)).

***[1.A] "forming a first stacked layer and forming a first insulating connection layer on the first stacked layer;"***

120. This, in my opinion, is taught by Costa.

121. According to the '291 patent, "the first stacked layer 2 can be formed on the substrate 1 [and] can include a plurality of oxide/nitride layer pairs." Ex. 1001, 9:26-28, Fig. 1.

122. "The first insulating connection layer 3 can be formed on the first stacked layer 2 [and] can be made by [sic] any suitable insulating material and/or dielectric material, such as silicon oxide." Ex. 1001, 9:61-65, Fig. 1.

123. The below annotated version of Figure 1 shows both the "first stacked layer" and "first insulating connection layer":

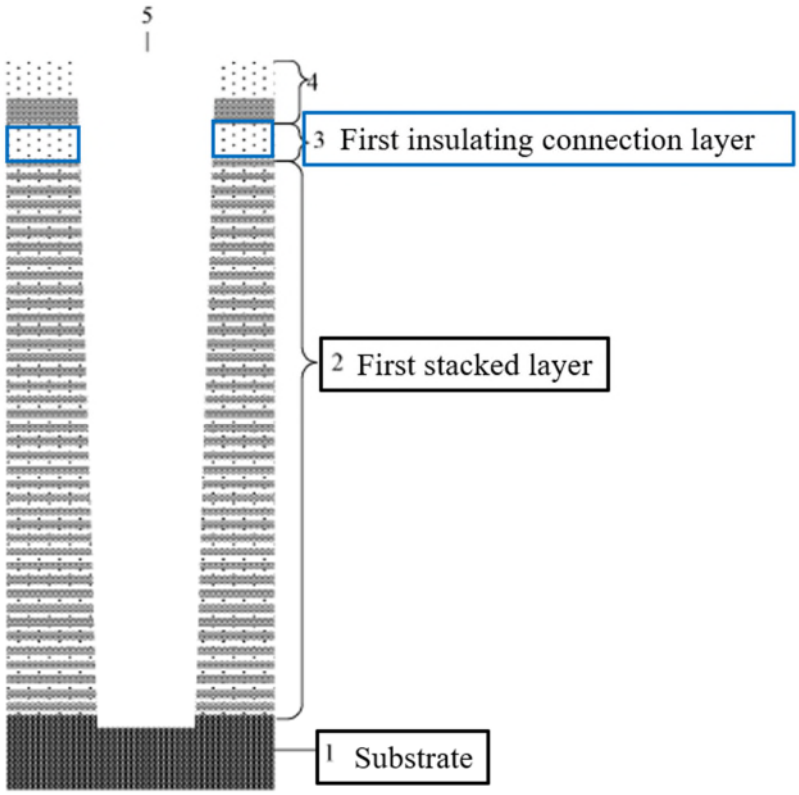
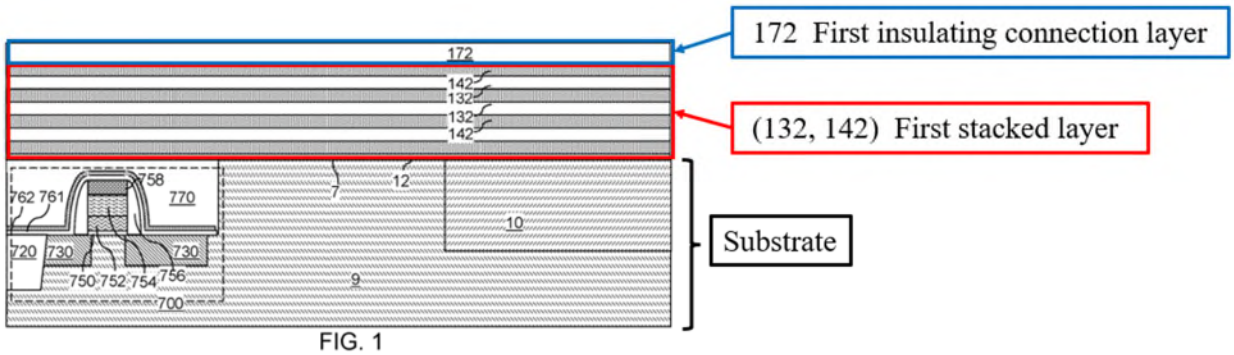



FIG. 1

Ex. 1001, Fig. 1 (annotated).

124. A POSITA would have recognized that the ’291 patent refers to the “first insulating connection layer” as a “connection layer” because in later steps, “a second stacked layer” is formed “on the first insulating connection layer.” Thus the “first insulating connection layer” serves at the “connection” layer between the two stacks. This is discussed in greater detail in connection with limitation [1.I] below.

125. Costa discloses the same layers and process. In particular, Costa forms a first stacked layer (“first alternating stack” 132, 142) and then forms a first insulating connection layer (“first insulating cap layer 172”) on the first stacked layer. Costa, [0134].




*Id*., Fig. 1 (annotated).

126. According to Costa, "[a]n alternating stack of first material layers and second material layers is subsequently formed. Each first material layer [132] can include a first material, and each second material layer [142] can include a second material that is different from the first material." Costa, [0126].

127. The first material layer 132 can be an insulating material, such as "silicon oxide … [or] dielectric metal oxides … commonly known as high dielectric constant (high-k) dielectric oxides…." Costa, [0126], [0129].

128. The second material layers 142 can be a "sacrificial material," such as "silicon nitride," that "can be subsequently replaced with electrically conductive electrodes…." Costa, [0129]-[0131].

129. As described by Costa, "first-tier insulating cap layer 172" is deposited on the first alternating stack (132, 142), "collectively constitut[ing] a first tier structure (132, 142, 172)." Costa, [0134], Figs. 1, 2B. Note that paragraph [0134] of Costa includes a typographical error. This paragraph refers to the insulating layer

being formed on the second stack. A POSITA would have understood, however, that this layer is actually formed on the first stack. *Id.*, [0134], Fig. 2B. This is what is shown in Costa's figures.

130. According to Costa, the first-tier insulating cap layer 172 is comprised of dielectric material such as silicon oxide. Costa, [0134].

131. While Costa's insulating layer 172 is directly on the first stacked layer, this is not required by the claim. The '291 patent explains that the term "on" includes simply being over: "intermediate feature[s]" could be between the layer 172 and the first stacked layer. Ex. 1001, 8:3-8.

132. The second stacked layer is then formed "on" this "first insulating cap layer 172," i.e., it is a connection layer between the two stacks made of dielectric. This is discussed in greater detail below in connection with limitation [1.I].

133. Patent Owner may argue that the claimed "first insulating connection layer" must directly contact the second stack.

134. In my opinion, this would be an incorrect understanding of claim 1.

135. Claim 1 requires only that the second stack be formed on the "first insulating connection layer."

136. Further, as I have explained, the '291 patent states that the term "on" broadly embraces layers that are either indirectly or directly on. This is consistent with the claim language itself, which uses the term "on" instead of "directly on."

137. Again, in my opinion it would be improper to limit the claim to require the second stack to be directly on and in contact with the "first insulating connection layer."

***[1.B] "forming a first through hole that penetrates the first stacked layer and the first insulating connection layer;"***

138. This, in my opinion, is taught by Costa.

139. According to the '291 patent, the first through hole 5 is formed by overlaying a mask layer 4 on the first insulating connecting layer 3 and performing an etching process to form the first through hole. Ex. 1001, 10:1-5, 10:16-29.

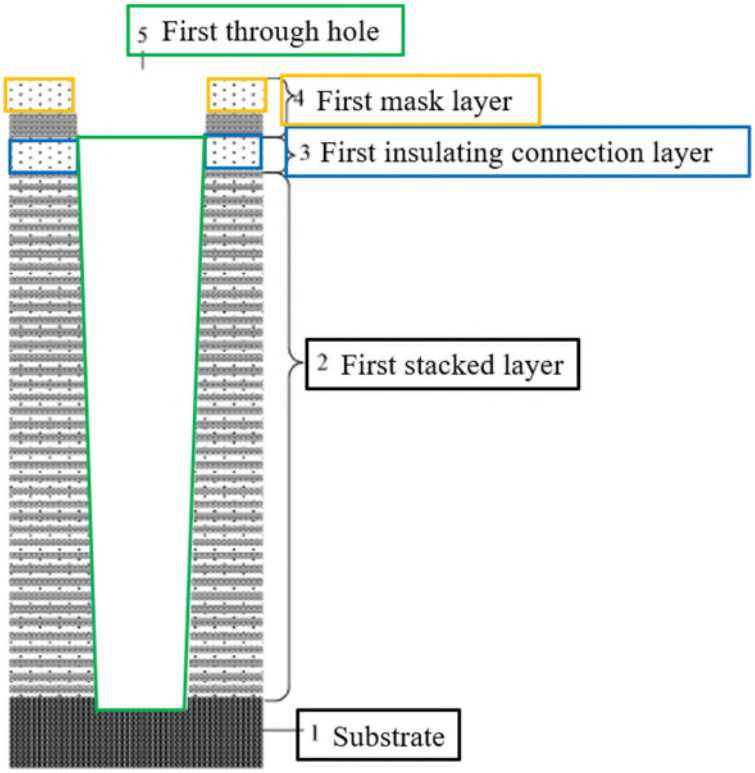


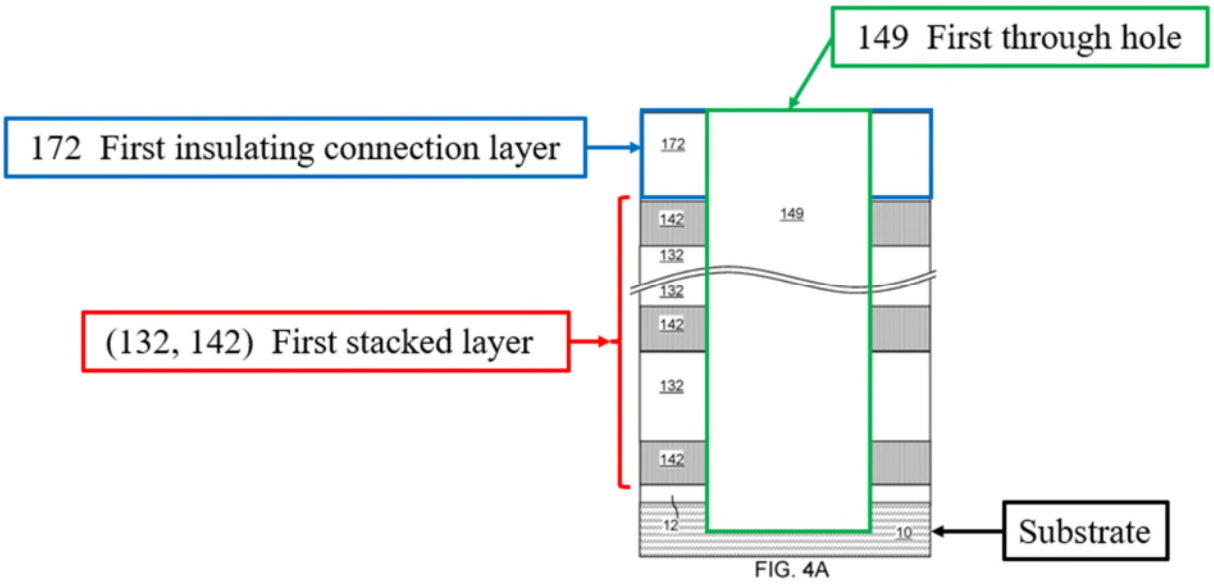

FIG. 1

*Id.*, Fig. 1 (annotated).

140. Costa teaches this same process. In particular, Costa forms a first through hole ("first-tier memory opening[]" 149) that penetrates the first stacked layer ("first alternating stack" 132, 142) and the first insulating connection layer ("first-tier insulating cap layer 172").

141. In particular, in Costa "first-tier openings (149, 119) extending to a top surface of the substrate (9, 10) are formed through the first tier structure (132, 142, 172, 165)." Costa, [0137]; *see also id.* (similarly discussing forming first-tier openings by lithographic patterning and etching, *i.e.*, masking).

142. As shown in the below annotated version of Figure 4A, Costa's first-tier memory opening 149 penetrates the first tier structure (132, 142, 172) exposing substrate 10:




Costa, Fig. 4A (annotated); *see also id.*, Fig. 3B.

***[1.C] "forming a first channel structure overlaying the surface of the substrate that is exposed by the first through hole;"***

143. This, in my opinion, is taught by Costa.

144. In the '291 patent, the claimed first channel structure is formed by depositing material "on the surface of the substrate 1 that is exposed by the first through hole 5" (i.e. at the bottom of the first through hole). Ex. 1001, 10:30-32, Fig. 2.

145. "[T]he first channel structure … can be a polycrystalline silicon (polysilicon) layer formed by using a selective epitaxial process." Ex. 1001, 10:32-34.

146. This is shown in Figure 2 below:

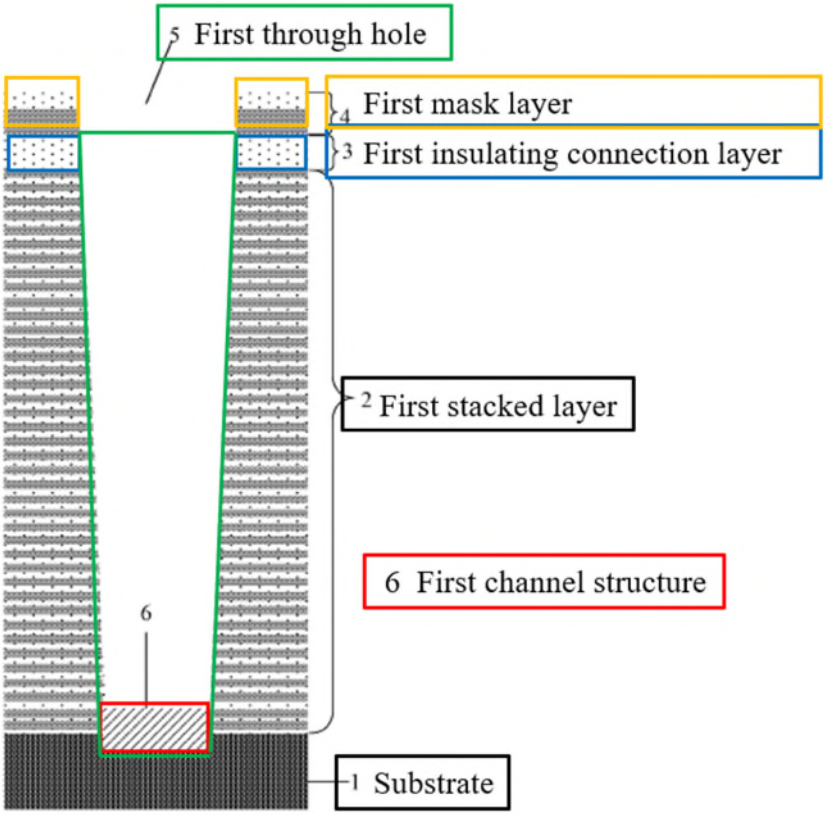



FIG. 2

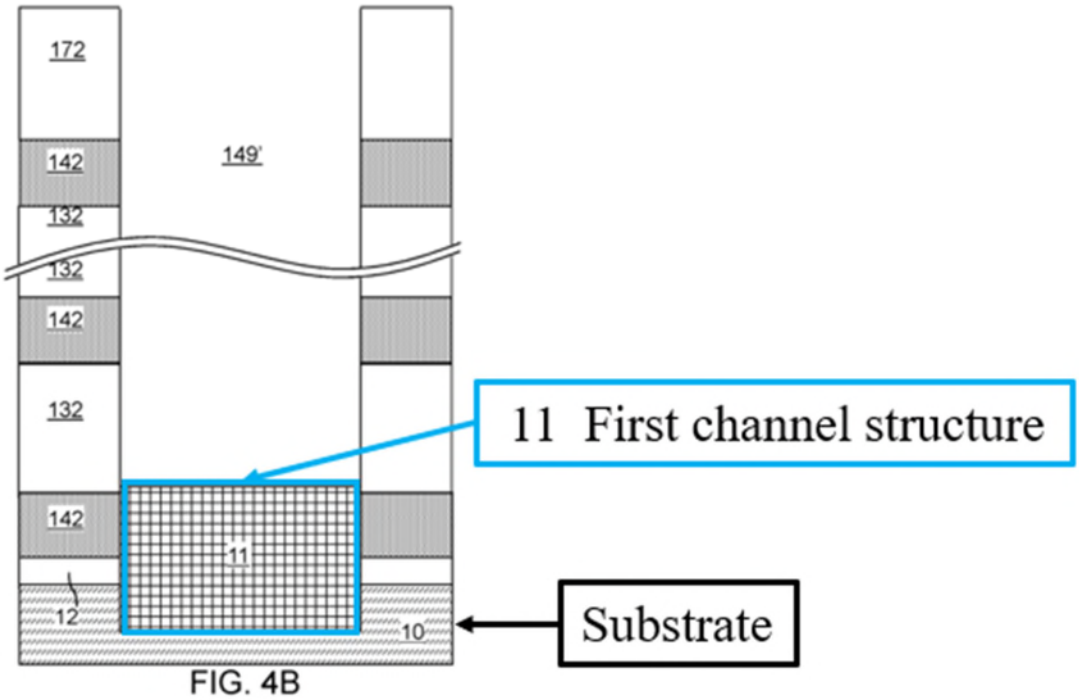
Ex. 1001, Fig. 2 (annotated).

147. In my opinion, Costa teaches this same process and structure.

148. In particular, Costa forms a first channel structure ("epitaxial channel portion 11") overlaying the surface of the substrate ("substrate 10") that is exposed by the first through hole ("first-tier memory opening" 149).

149. More particularly, an "epitaxial channel portion (*e.g.*, an epitaxial pedestal) 11 can be formed at the bottom portion of each first-tier memory opening 149…." Costa, [0143]; *see also id.*, [0137] ("substrate" includes portions 9 and 10).

150. As shown in Figure 4B below, Costa's epitaxial channel portion 11 overlays the surface of the substrate 10 that is exposed by the first-tier memory opening 149:




Costa, Fig. 4B (annotated).

***[1.D] "forming a first functional layer on the sidewall of the first through hole;"***

151. This, in my opinion, is taught by Costa.

152. In the '291 patent, the "functional layer" refers to a layer that performs a function. In the patent's embodiments, that function is data storage. Ex. 1001, 10:40-43 (functional layer including data storage layer and oxide layers to interject charge thereon).

153. The ’291 patent also explains that in one embodiment, “first functional layer can be formed on the sidewall of the first through hole 5 [and] can include a first tunneling layer 7, a first storage layer 8, a first barrier layer 9, and a first passivation layer 10.” Ex. 1001, 10:40-43, Fig. 3; *see also id.*, 8:34-51 (“A layer can include multiple layers.”).

154. Further, in the ’291 patent, portions of these layers “located on the top surface of the first channel structure 6 and the bottom of the first through hole 5 can be removed” (*i.e.*, leaving only the portions on the sidewall of first through hole 5). Ex. 1001, 11:3-24, Fig. 4.

155. Dependent claim 4 separately requires that “functional layer” of claim 1 includes each of the exemplary layers set forth in the ’291 patent specification (i.e., layers 7-10). As discussed, Costa includes the same layers. But more broadly, a POSITA would have understood that the claimed “functional layer” of claim 1 simply means a layer that functions, *e.g.*, to store data.

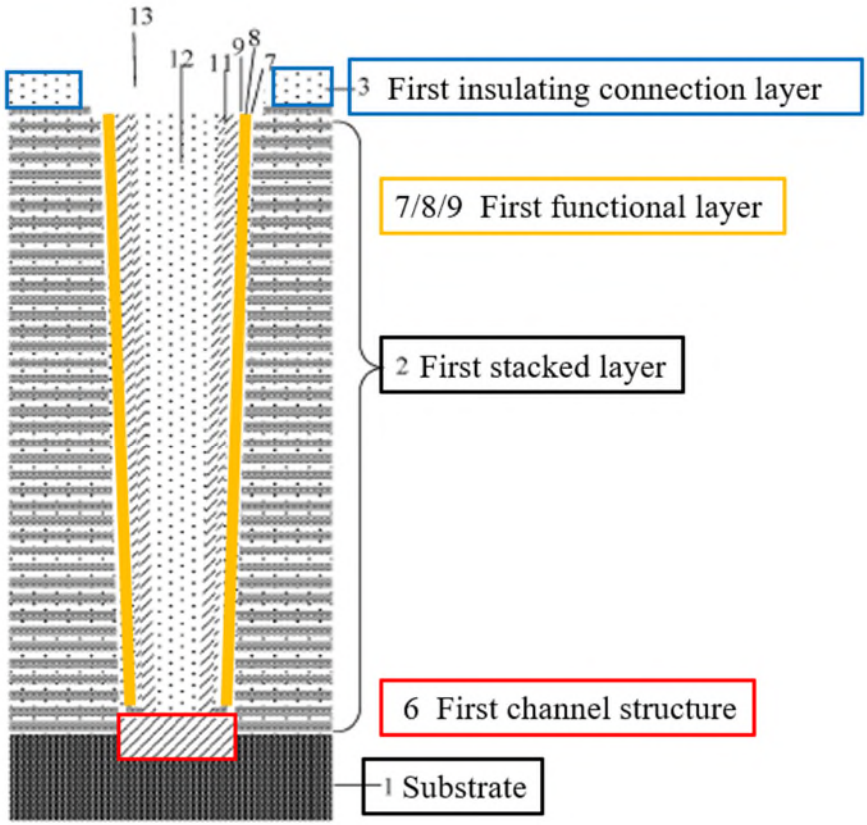



FIG. 10B

Ex. 1001, Fig. 10B (annotated).

156. This is what Costa discloses. In particular, Costa forms a first functional layer ("first memory film 150" with or without the optional semiconductor channel layer 611) on the sidewall of the first through hole ("first-tier memory opening 149").

157. More specifically, Costa explains that its first memory film 150 comprises "a stack of layers including a first blocking dielectric layer 152, a first charge storage layer 154, a first tunneling dielectric layer 156…." Costa, [0144], Figs. 4D-E.

158. This "stack of layers" consisting of memory film 150 is deposited in the first-tier memory opening 149 and subsequently etched to remove the portions above first-tier insulating cap layer 172 and at the bottom of first-tier memory opening 149, as shown in Figures 4C and 4D below. Costa, [0144], [0153].

159. While present in the figure below, Costa explains that outer semiconductor channel layer 611 is an optional layer. Costa, [0144], [0153].

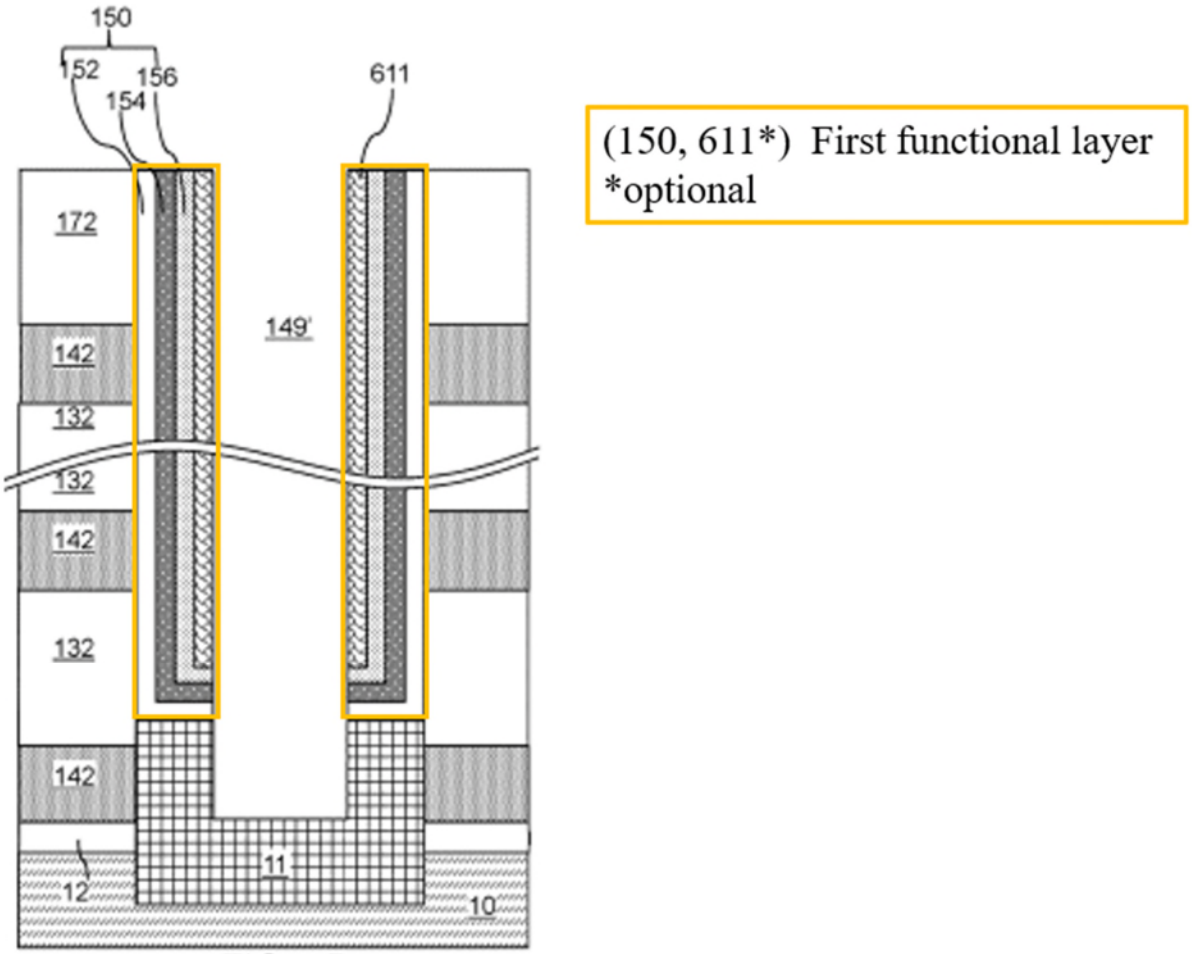


FIG. 4D

*Id*., Fig. 4D (annotated).

***[1.E] "forming a second channel structure and forming a first filling structure on the sidewall of the first functional layer and the exposed surface of the first channel structure;"***

160. This, in my opinion, is taught by Costa.

161. Here, the '291 patent discusses "sequentially form[ing a second channel structure and a first filling structure] on the sidewall of the first functional layer and the exposed surface of the first channel structure 6." Ex. 1001, 11:25-44; *see also id.*, Figs. 5-6, 11:45-12:23 (describing process of removing portions of first filling layer 12 and second channel layer 11 that are above first insulating connection layer 3), Figs. 7A-8B.

162. Per the '291 patent, the "second channel structure" can be amorphous silicon, while the "first filling structure" can be an oxide layer. Ex. 1001, 19:40-43, 19:46-48.

163. In sum, a POSTIA would have recognized that the claimed channel structure is, for example, the semiconductive layer of the channel structure while the filling structure is, for example, the core of the channel structure.

164. The annotated version of Figure 10B below shows these two structures (along with the surrounding structure):

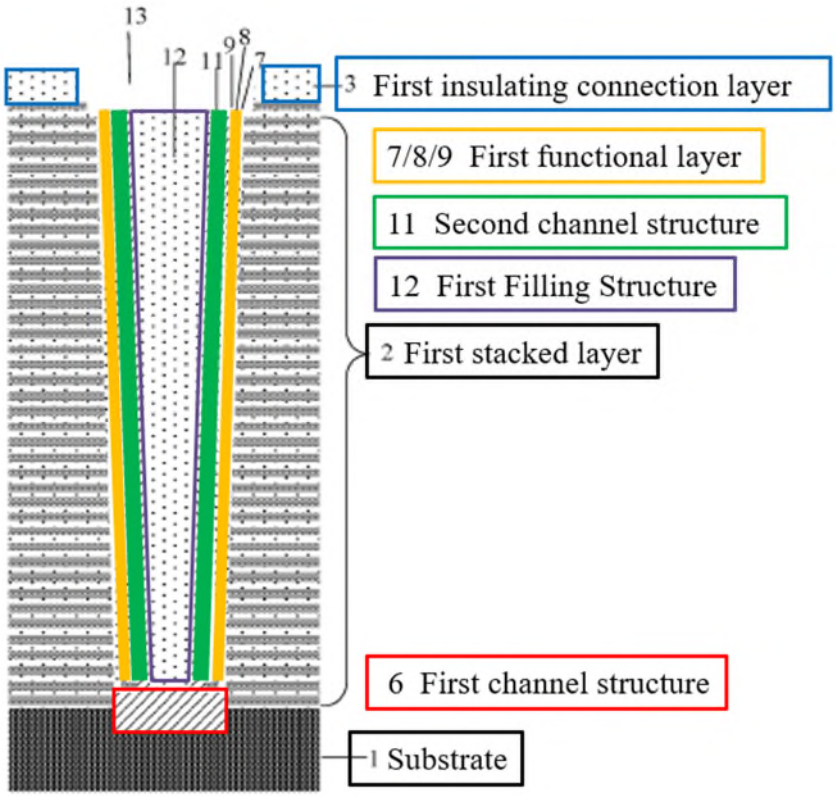



FIG. 10B

Ex. 1001, Fig. 10B (annotated).

165. This, in my opinion, is also what Costa teaches. In particular, Costa forms a second channel structure ("first inner semiconductor channel layer 612") and forming a first filling structure ("dielectric core 162") on the sidewall of the first functional layer ("stack of layers" 152, 154, 156, 611) and the exposed surface of the first channel structure ("epitaxial channel portion 11").

166. More specifically, with respect to the claimed "second channel structure," Costa teaches "a first inner semiconductor channel layer 612 can be deposited directly on the semiconductor surface of the epitaxial channel portion 11 … and directly on the [optional] first outer semiconductor channel layer 611."

Costa, [0156]. The 611 and 612 layers are "amorphous silicon or polysilicon." *Id.*, [0152], [0156]. "The materials of the first outer semiconductor channel layer 611 and the first inner semiconductor channel layer 612 are collectively referred to as a first semiconductor channel material." *Id.*, [0157].

167. With respect to the claimed "filling structure," Costa teaches that the cavity it forms need not be completely filled with semiconductor channel material. Costa, [0158], Fig. 4E. Then, a "dielectric core layer 162L" is formed. *Id.*, [0158], Fig. 4F. In other words a portion of "first dielectric core layer 162L" that is "above the top surface of the first-tier insulating cap layer 172" is removed leaving "dielectric core 162" within the memory cavity 149. *Id.*, [0159], Fig. 4G.

168. Again, as noted above, the "outer semiconductor channel layer 611" is optional. Costa, [0144].

169. These structures are shown in the below annotated version of Figure 4G:



**Micron Ex. 1003, p. 76**
**Micron v. YMTC**
**IPR2025-00244**

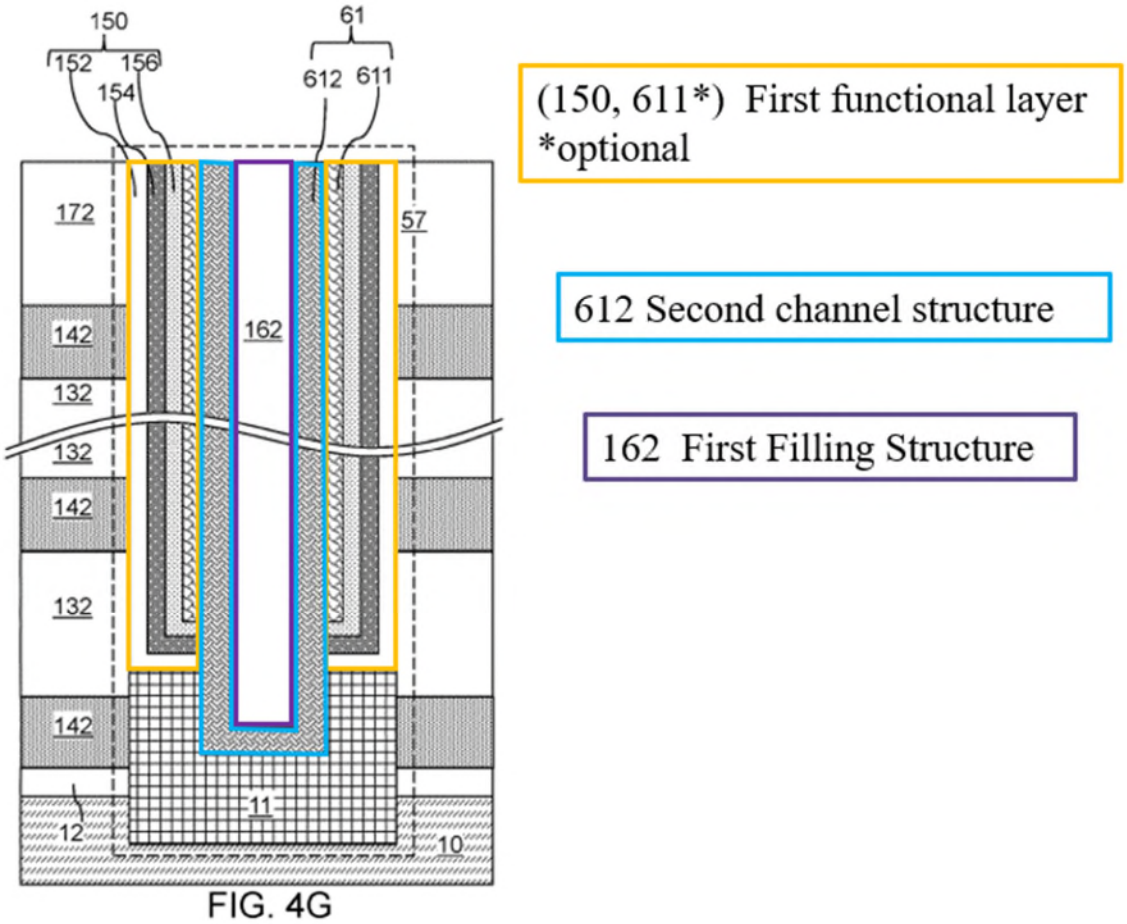


FIG. 4G

Costa, Fig. 4G (annotated).

170. It is possible that Patent Owner may attempt to argue that Costa does not teach what this limitation requires because its filling structure (162) is not "on" the "exposed surface of this first channel structure." This, in my opinion, is not how a POSITA would have applied the claims.

171. First, even if the "filling structure" must be "on" "the exposed surface of the first channel structure," Costa's layers are so structured because in the '291 patent, the term "on" does not require "directly contacting" (*i.e.*, there can be an intervening layer). Ex. 1001, 8:3-8.

172. Second, a POSITA would have recognized that this understanding is confirmed by the claim language itself. The claim phrase "on the sidewall of the first functional layer and the exposed surface of the first channel structure" does not modify "a first filling structure," even though this phrase appears immediately after "a first filling structure," because "a first filling structure," as described by the '291 patent, is not on the sidewall of the first functional layer (see above).

173. Nor would a POSITA understand the claim to require specifically that the "second channel structure" be formed "on the sidewall of the first functional layer" and that "a filling structure" be formed on "the exposed surface of the first channel structure," because the claim does not use the term "respectively" to differentiate these positional relationships. Instead, the claims require that the two structures collectively ("second channel structure" and "filling structure") in some way contact the "sidewalls" and "exposed surface of the first channel structure."

174. Third, this limitation parallels limitation [1.J] discussed below. As I explain when discussing that limitation, while the claim recites "forming a fourth channel structure and forming a second filling structure on the sidewall of the second functional layer and the exposed surface of the third channel structure," the '291 patent does not depict the filling structure directly on "the exposed surface of the third channel structure." Thus, a POSITA would have understood that layers that are indirectly on another layer are also claimed and covered.

***[1.F] "forming a third channel structure in contact with the second channel structure above the first through hole, wherein a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate;"***

175. This, in my opinion, is taught (or at least rendered obvious) by Costa.

176. To begin, the '291 patent forms its third channel structure by first removing a "[a] portion of the first insulating connection layer 3 … to form the first groove [13] that penetrates the first insulating connection layer 3." Ex. 1001, 12:35-40. "[A] third channel structure 14 can be formed in the first groove 13" that "can be a polycrystalline silicon []layer formed by using a deposition process." *Id*., 12:59-64. "A projection of the first groove [13] on the substrate completely covers a projection of the first through hole on the substrate" or, in other embodiments, "[a]n area of the projection 'x' of the first groove on the substrate 1 can be larger than an area of the projection 'y' of the first through hole 5 on the substrate 1." *Id*., 12:38-40, 16:5-7.

177. Additionally, the patent explains that "[i]n some embodiments … a portion of the third channel structure 14 that is adjacent with the bottom nitride layer of the second stacked layer 15, or is adjacent with the top nitride layer of the first stacked layer 2 can be converted to an oxide layer by an oxidation process." Ex. 1001, 16:65-17:2.

178. The '291 patent's third channel structure 14 is illustrated in the annotated version of Figure 11B below:

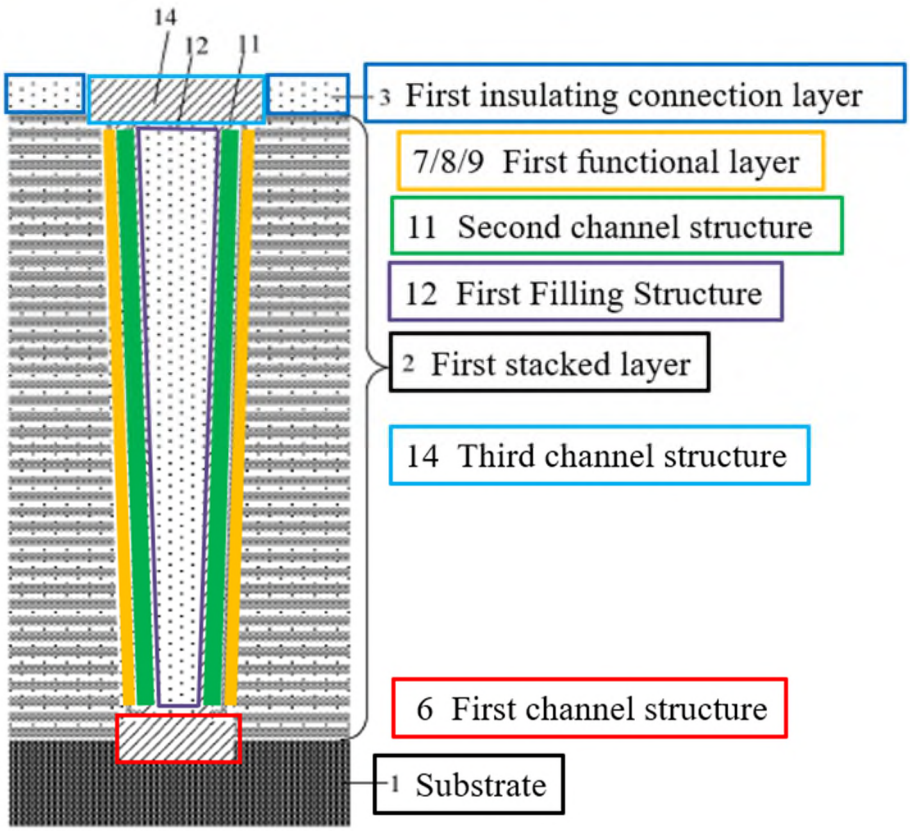



FIG. 11B

Ex. 1001, Fig. 11B (annotated).

179. Costa teaches this limitation or at the very least renders it obvious.

180. In particular, Costa forms a third channel structure ("joint-level doped semiconductor portion 173") in contact with the second channel structure ("first inner semiconductor channel layer 612") above the first through hole ("first-tier memory opening 149"), wherein a projection of the third channel structure ("joint-level doped semiconductor portion 173") on the substrate covers a projection of the first through hole ("first-tier memory opening 149") on the substrate.

181. Costa goes on to reference another "exemplary structure" that modifies the "first exemplary structure" discussed throughout limitations [1.Pre] through [1.E] above.

182. In particular, the interface between the two tiers can be modified. Costa, [0263]. This modification results in the rest of what this claim requires.

183. Per Costa, a "joint-level doped semiconductor layer 173L" is deposited over the first tier structure (i.e., over first insulating cap layer 172). Costa, [0265], Fig. 20A.

184. Lithographic patterning and subsequent etching are performed, leaving joint-level doped semiconductor portion 173 that "covers and protects the underlying first vertical semiconductor channel 61 from oxidation during a subsequent oxidation process." Costa, [0265], Figs. 20A-B.

185. "In one embodiment, the bottom surface of each joint-level doped semiconductor portion 173 can contact an entire top surface of an underlying first memory opening fill structure 57." Costa, [0265].

186. As shown in Figures 20B and 20C below, Costa's joint-level doped semiconductor portion 173 covers the entire first-tier memory opening 149 (i.e., a projection of 173 on the substrate covers a projection of 149 on the substrate) and is in contact with the second channel structure:

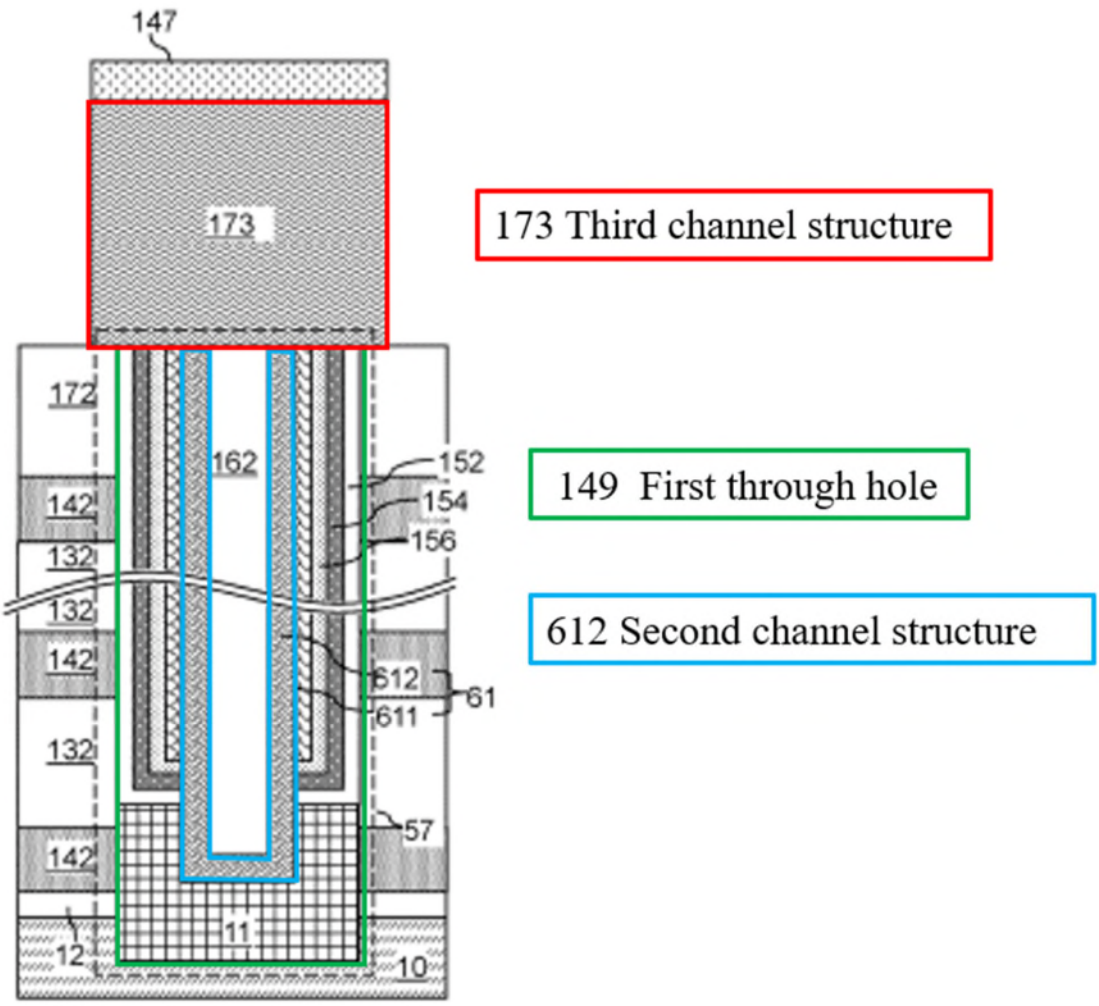



FIG. 20B

Costa, Fig. 20B (annotated).

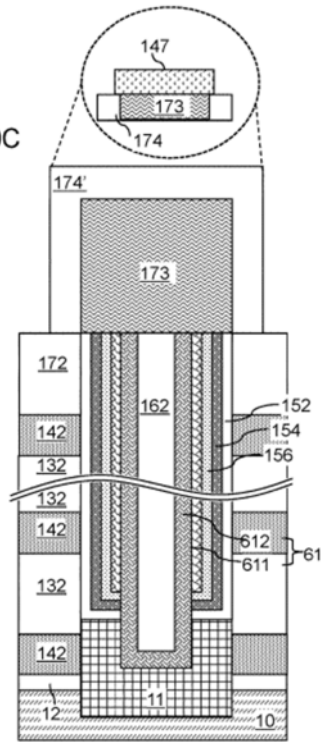
187. This is confirmed by other portions of Costa. In particular, Costa explains that the mask to preserve the final structure 173 will "cover each of the first memory opening fill structures 57." Costa, [0265]. Further, "[i]n one embodiment, the bottom surface of each joint-level doped semiconductor portion 173 can contact an entire top surface of an underlying first memory opening fill structure 57." *Id.*, [0265]. Because of this, a POSITA would have understood that the third channel

structure 173 will fully cover—and would in fact be wider than—the fill structure 57.

188. I note that Costa includes an embodiment with a further oxidation step. Costa, [0266].

189. Even in this embodiment, however, after oxidizing the exposed surfaces of semiconductor portion 173, Figure 20C shows that the remaining portion of doped semiconductor portion 173—this is the portion that was not oxidized—has an aperture at least the same size as that of fill structure 57 (or the structures filling first-tier memory opening 149). Costa, [0266], Fig. 20C. Figure 20C is reproduced below for reference:

FIG. 20C




*Id.*, Fig. 20C.



Micron Ex. 1003, p. 83
Micron v. YMTC
IPR2025-00244

190. It is possible that Patent Owner may attempt to argue that Costa does not teach what this limitation requires because in Figure 20C joint-level doped semiconductor portion 173 (*i.e.*, the portion of the structure that was not oxidized) has the same size as that of fill structure 57 (*i.e.*, the diameter of "the first through hole"). In my opinion, this would be incorrect.

191. First, Costa employs the oxidation step in only one embodiment, not all embodiments. Costa, [0266].

192. Second, in my opinion, a POSITA would have understood that Costa's joint-level doped semiconductor portion 173 shown in Figure 20C would have a projection on the substrate that "covers" a projection of the fill structure 57 in a way entirely consistent with how the '291 patent uses the term "cover."

193. The '291 patent's specification explains that "[i]n some embodiments, the projection of the first groove on the substrate 201 can completely cover the projection of the corresponding first through hole 205 on the substrate 201." *E.g.*, Ex. 1001, 20:33-38. Claim 1, however, just uses the word "cover." It does not say that the projection "completely cover." Because of this, in my opinion a POSITA would not read "cover" in the claim to mean "completely cover" (e.g., cover the entirety of the underlying object). The Patentee knew how to explain what complete coverage is required (as shown by the language choice in the specification) but purposefully chose not to limit the claims in this way.

194. Next, in my opinion, a POSITA would have understood the plain meaning of "cover" to include circumstances where the "covering" object is the same size as the object being "covered." In other words, the "covering" object need not be larger than another object to "cover" it. For example, if two quarters were stacked one atop the other, one would describe the top quarter as covering the bottom quarter even though the quarters are exactly the same size.

195. As shown in Figure 20C of Costa, joint-level doped semiconductor portion 173 is at least the same size as fill structure 57 (the first hole). Costa, Fig. 20C. Because of this, a projection of semiconductor portion 173 (even in the post-oxidation embodiment) "cover[s]" a projection of first-tier memory opening 149 on the substrate because it has the same size as that opening. *Id.*

196. Regardless, even if not already taught by Costa for the reasons explained above, in my opinion a POSITA would have found it obvious to ensure that Costa's joint-level doped semiconductor portion 173 is wider than the first hole (more than covers a projection of first-tier memory opening 149 on the substrate).

197. For example, Costa teaches that one purpose of doped semiconductor portion 173 is to "protect[] the underlying first vertical semiconductor channel 61 from oxidation during a subsequent oxidation process." Costa, [0265].

198. To do so, Costa forms portion 173 to "contact an entire top surface of an underlying first memory opening fill structure 57." Costa, [0265].

199. In my opinion, this protective function would have motivated a POSITA to ensure that doped semiconductor portion 173 does more than completely cover the underlying fill structure 57—i.e., extends beyond the margins of—to ensure it accomplishes the protection function, particularly given process variations during fabrication. Costa, [0266].

200. During fabrication, variations in the oxidation process could result in oxidation occurring around the boundary of areas protected by portion 173. By increasing the size of this portion—and thus creating a buffer or margin around the structure to be protected by making the portion 173 wider than fill structure 57—these processing issues would be avoided.

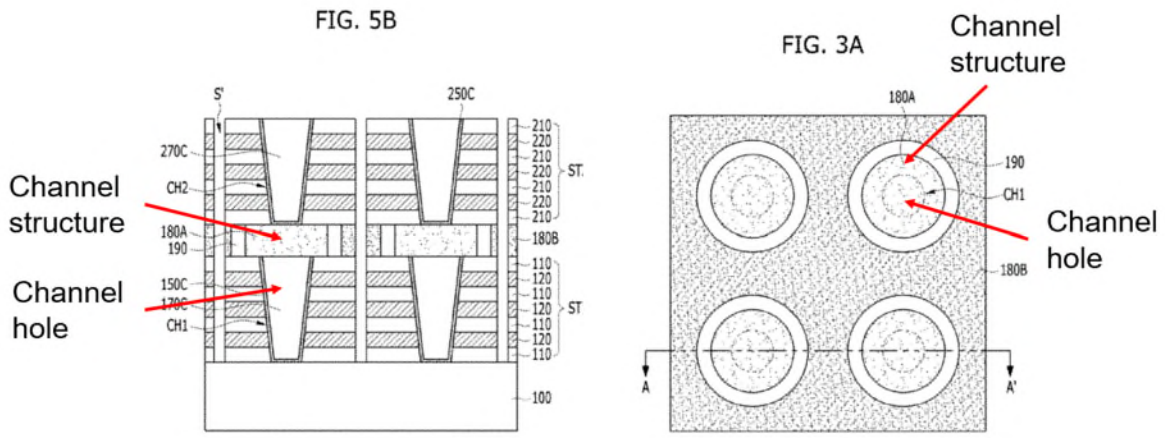
201. In addition, Costa describes a process that is not self-aligned. That is, even though Costa's figures show perfect alignment between, for example, portion 173 and the underlying fill structure 57, there would be some misalignment. This is because the process steps for, e.g., forming the third channel, does not include structures that naturally force alignment of the structures, e.g., the third channel structure. Precise mask alignment to features already formed is necessary. Process variations during fabrication, which were well known, would make perfect alignment in such a process for each device nearly impossible. *See* Ex. 1022 (Plummer), 20-21; Ex. 1021 (U.S. Pat. 9,530,866), 2:60-3:6 ("Importantly, using this prior art process flow, the gate structures 14 are not self-aligned in that the lateral

width 14L of the gate structure 14 is approximately defined by the lateral width 15L of the patterned features of the top spacer layer 15T. Since these features are defined by a patterning process, e.g., masking and etching, the control of the exact size and exact positioning of these patterned features is subject to the problems generally encountered when defining features using patterning processes such as, for example, positional accuracy relative to other structures (like the structures 12A), pattern transfer variations, etc. These types of issues are only expected to be more problematic as device dimensions continue to decrease with advancing technology.”).

202. Thus, a POSITA would have found it obvious to ensure an electrical connection (alignment) between the upper and lower deck memory channels by including a third channel structure with a larger diameter than that of the underlying memory hole. This concept of including margin in a semiconductor structure was generally well known. *E.g.*, Ex. 1023, [0023] (“The lateral extension portion (135) may have a larger cross-sectional area than the first and second semiconductor pillars (130a, 130b) based on a cross section parallel to the substrate (105).”), [0086] (“[B]y arranging the lateral extension portion (135) between the first semiconductor pillar (130a) and the second semiconductor pillar (130b), the alignment margin is increased when the second through holes (120b) are formed….”); Liu, [0058] (“[M]emory opening alignment challenges may be reduced or avoided by adding a

landing pad between the memory stack portions … [that is] is wider (e.g., had a larger diameter) than the channel in the horizontal direction.”).

203. In Costa, the third channel structure serves as an interface between the channels in the upper and lower channel structures (in the first and second through holes). For the same reasons as above, in this context, it was known to account for potential misalignment of the channel holes (and the third channel structure itself). This can be seen below:




Ex. 1024 (U.S. Pat. Pub. 2017/0154892), Fig. 5B (annotated) and 3A (annotated). As can be seen, a channel structure interface (180A) is made larger to account for potential misalignment. *Id.*, [0061] (“[C]hannel connection pattern 180A may have an island shape which overlaps the first channel holes CH1 … [T]o secure an overlap margin between the channel connection pattern 180A and the first channel hole CH1, the channel connection pattern 180A may have a larger width than the top surface of the first channel hole CH1.”). Thus, conventional semiconductor design practice

is to provide margin to address these issues when fabricating structures in processes that are not self-aligned. If the holes and/or third channel structure becomes unaligned to the degree that the upper and lower channel structures do not physically contact one another (which enables an electrical coupling), the memory string will be non-functional (e.g., because a channel through the string would not form). While memories often account for defective memory cells with redundant cells, too many defective cells render an entire device defective (or not to sellable standards). In short, not accounting for misalignment issues will result in more defective devices, also known as decreasing yield. Reducing yield reduces profit margin due to the waste in silicon and fabrication time. In sum, it is my opinion that a POSITA would have found it obvious to make portion 173 in Costa wider than fill structure 57 to account for process variations and ensure alignment between the first and second memory holes.

204. Patent Owner may argue that Costa does not satisfy this limitation because its joint-level doped semiconductor portion 173 is not formed in a groove of the first insulating cap layer 172.

205. This, in my opinion, would be incorrect. There is no such requirement in claim 1. And if there were, dependent claim 6 would be rendered superfluous.

***[1.G] "forming a second stacked layer and forming a second insulating connection layer on the first insulating connection layer;"***

206. This, in my opinion, is taught by Costa.



**Micron Ex. 1003, p. 89**
**Micron v. YMTC**
**IPR2025-00244**

207. According to the ’291 patent, “a second stacked layer 15 and a second insulating connection layer 16 can be sequentially formed on the third channel structure 14…. [T]he second stacked layer 15 can include a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs.” Ex. 1001, 13:11-16, Fig. 12, 13:16-21. This is shown in Figure 13 below:

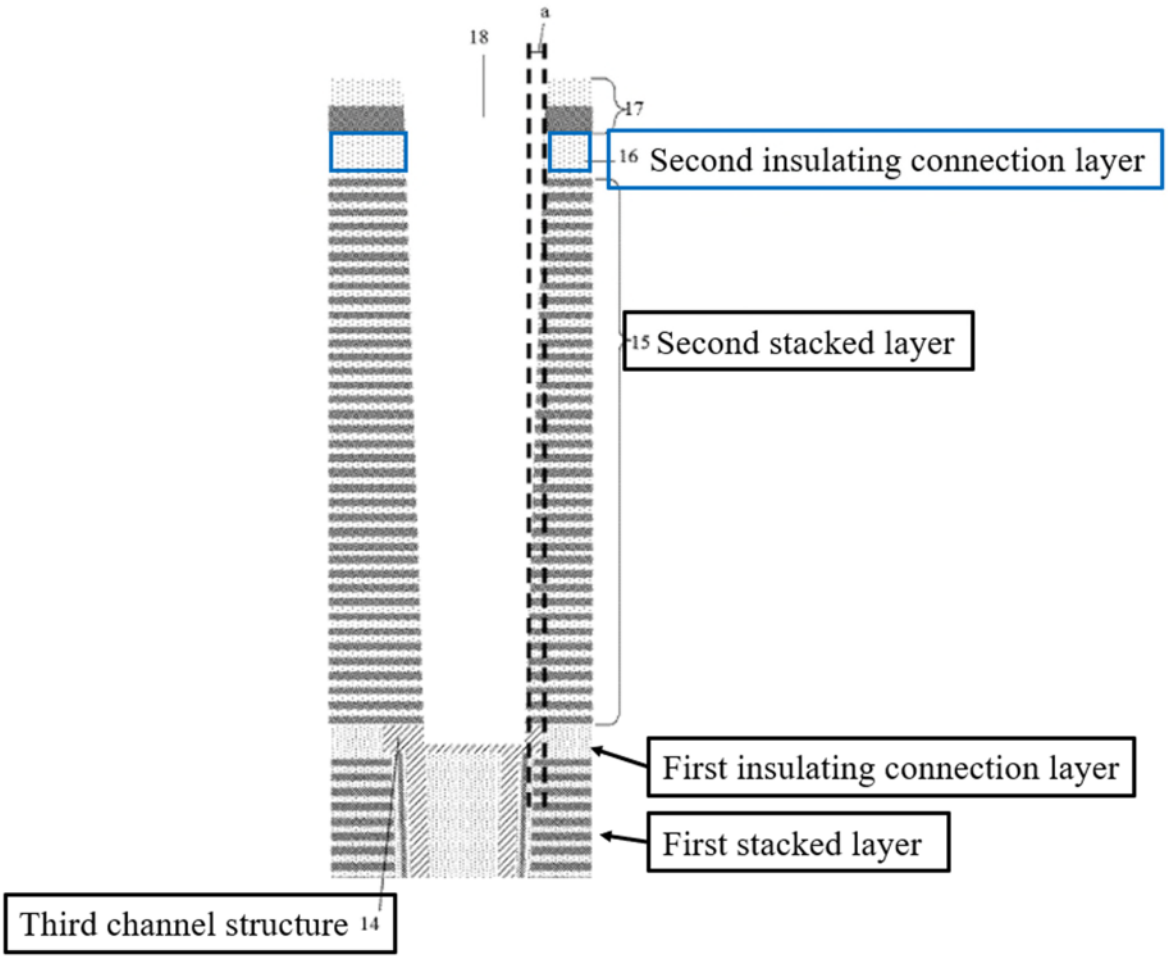



FIG. 13

*Id*., Fig. 13 (annotated).

208. This is what Costa teaches. In particular, Costa forms a second stacked layer (“second alternating stack” 232, 242) and second insulating connection layer

("insulating cap layer 70") on the first insulating connection layer ("first insulating cap layer 172").

209. As shown in Figure 21A reproduce in annotated form below, "second alternating stack (232, 242) of material layers is subsequently formed on the top surface of the joint-level material layers…." Costa, [0178] (describing the process of Figs. 8A-B), [0270] (referring to "the processing steps of" Figs. 7A-10B using the third exemplary structure's single joint-level doped semiconductor portion 173), [0263], Figs. 8A-B, Fig. 21A.

210. Per Costa, "[a]n insulating cap layer 70 can be subsequently formed over the second alternating stack (232, 242)." Costa, [0183].

211. Thus, second alternating stack (232, 242) and insulating cap layer 70 are formed "on" first-tier insulating cap layer 172. As I have repeatedly explained, the '291 patent does not use the word "on" such that a layer must be directly on another layer. Ex. 1001, 8:3-8.

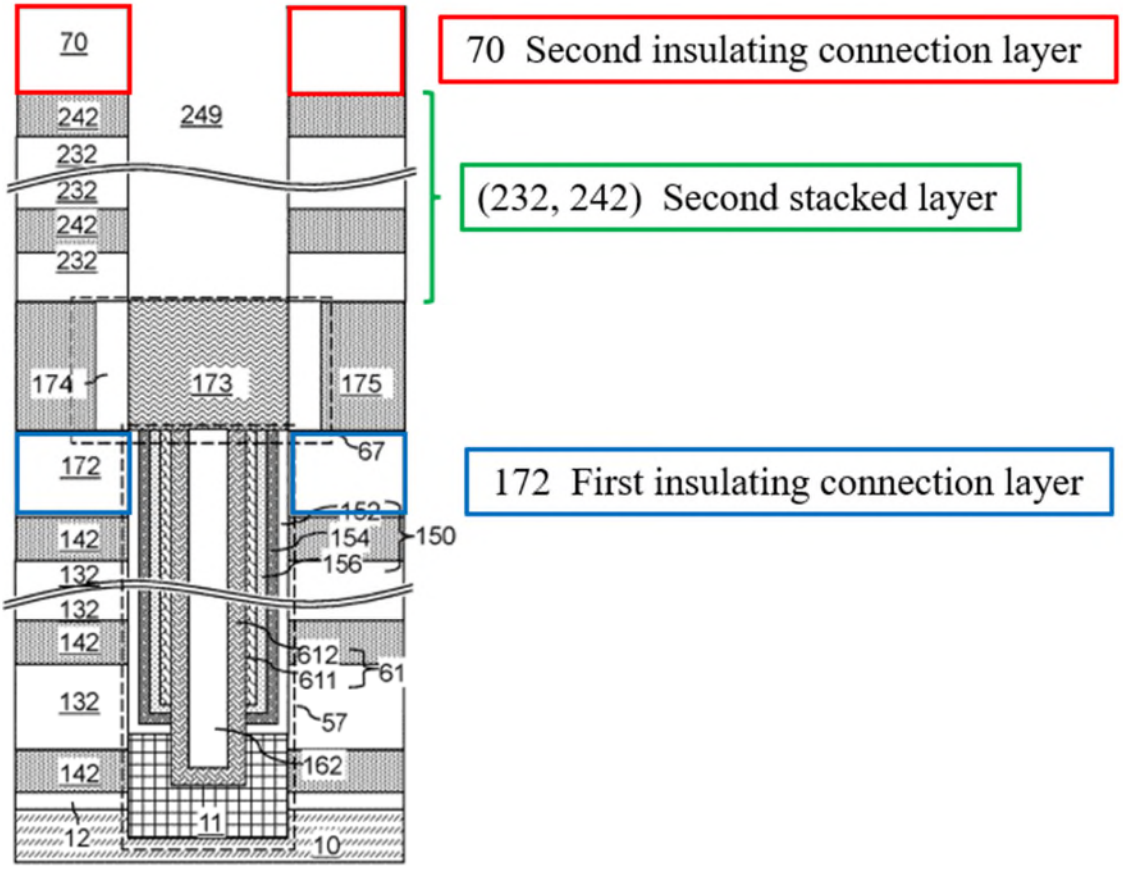



FIG. 21A

Costa, Fig. 21A (annotated).

212. As shown above, and also like the ’291 patent, Costa’s connection layer 70 is between the second tier and the overlying layers (e.g., for interconnects). *Compare* Ex. 1001, Fig. 22A-B (layer at top of second tier) *with* Costa, Fig. 22A-B (same).

***[1.H] "forming a second through hole that penetrates the second stacked layer and the second insulating connection layer, wherein a projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate;"***

213. This, in my opinion, is taught (or at the very least rendered obvious) by Costa.

214. In the '291 patent, the second through hole is formed similarly to the first through hole: "[A] second through hole 18 is formed [that] can completely penetrate the second stacked layer 15 and the second insulating connection layer 16, and can extend into the surface of the third channel structure 14." Ex. 1001, 13:38-42.

215. Further, "[t]he projection of the second through hole 18 on the substrate 1 can at least partially overlap with the projection of the first through hole 5 on the substrate 1." Ex. 1001, 13:42-45.

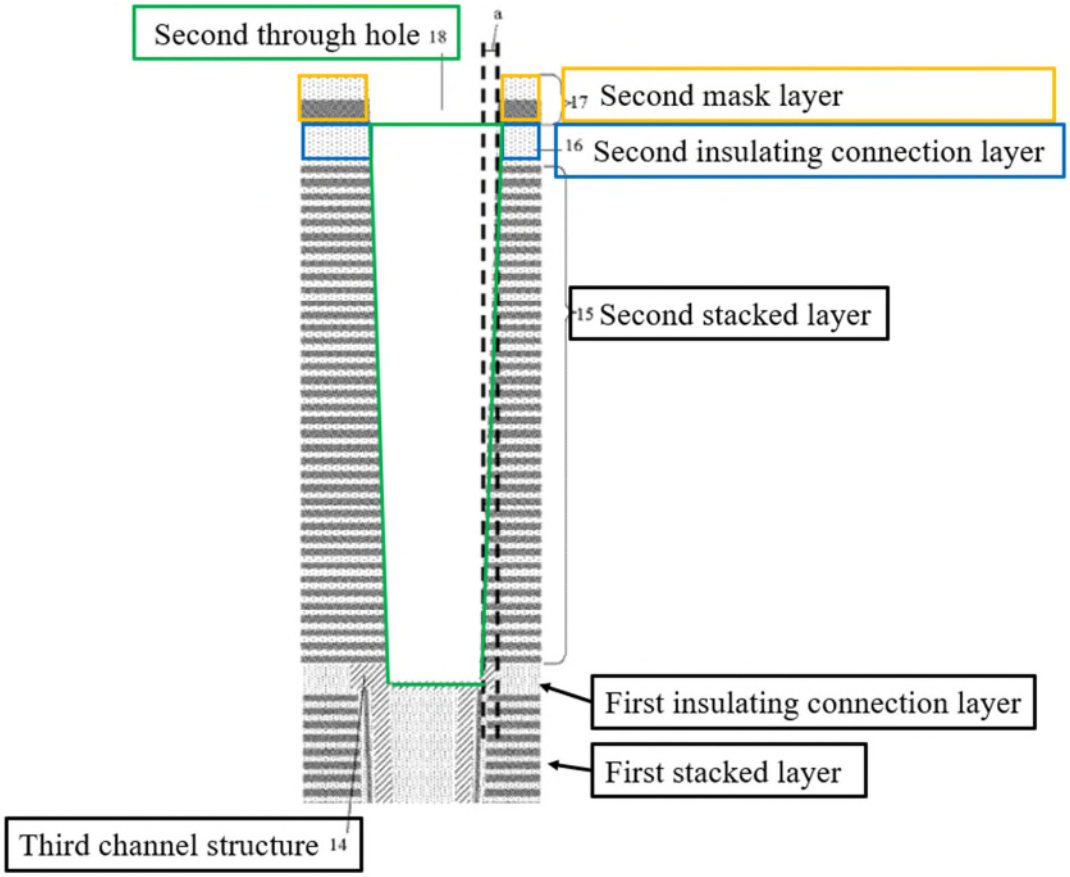



FIG. 13

*Id.*, Fig. 13 (annotated).

216. Costa similarly forms a second through hole ("second-tier memory opening 249") that penetrates the second stacked layer ("second alternating stack" 232, 242) and the second insulating connection layer ("insulating cap layer 70"), wherein a projection of the second through hole ("second-tier memory opening 249") on the substrate ("substrate 10") at least partially overlaps with the projection of the first through hole ("first-tier memory opening 149") on the substrate.

217. According to Costa, after forming the second alternating stack (232, 242), "second-tier [memory] openings" 249 "are formed through the second tier

structure (232, 242, 265, 70)." Costa, [0190], [0192] ("second-tier openings (249, 219) can be formed by a combination of lithographic patterning and an anisotropic etch").

218. As shown in the annotated version of Figure 21A reproduced below, second-tier memory opening 249 penetrates the second stacked layer (second alternating stack (232, 242)) and the second insulating connecting layer (insulating cap layer 70):

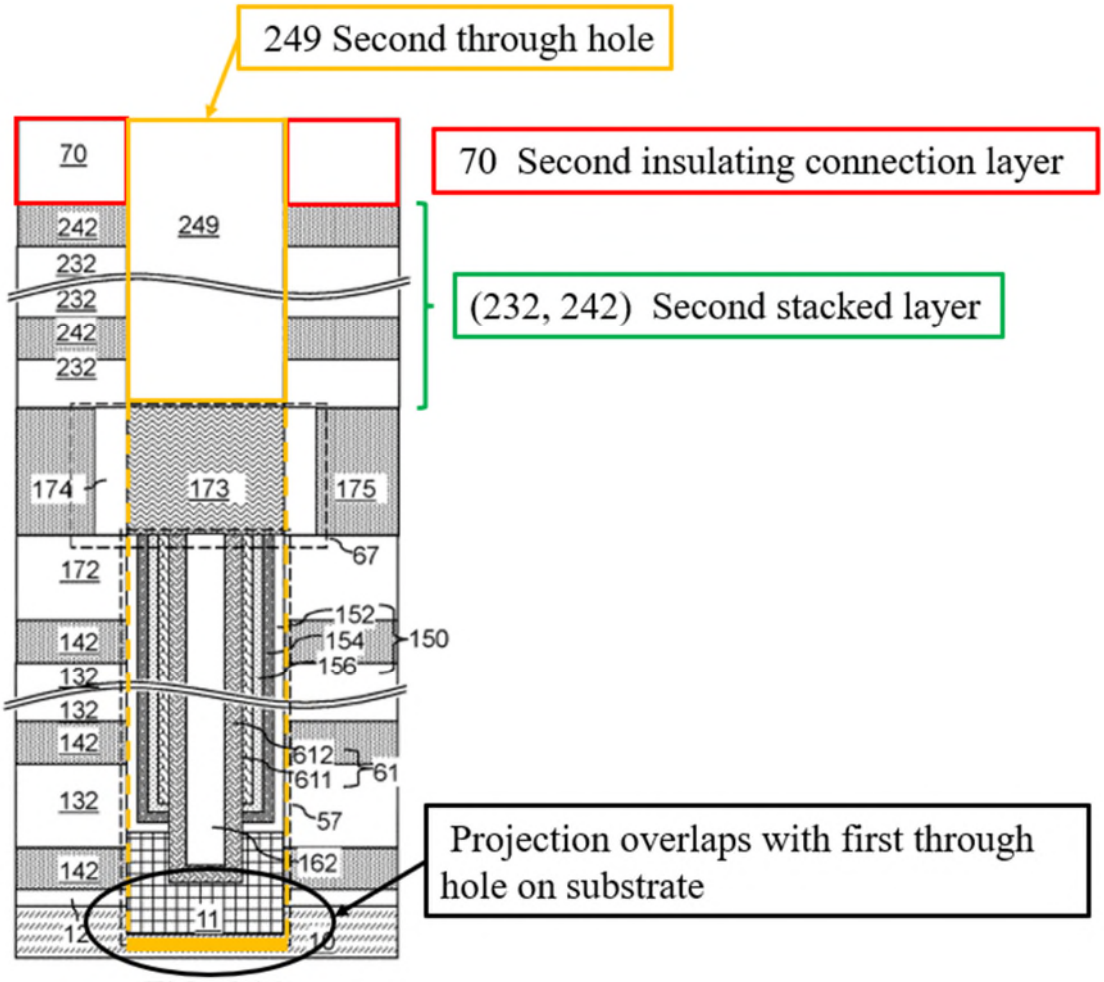



FIG. 21A

Costa, Fig. 21A (annotated).

219. Per Costa, "second-tier memory openings 249 are formed through the second-tier structure … in areas that overlap with the joint-level memory opening fill structures 67…." Costa, [0191], Fig. 21A.

220. Thus, in Costa, a projection of the second through hole (second-tier memory opening 249) on the substrate overlaps—either completely or partially—with a projection of the first through hole (first-tier memory opening 149) on the substrate. Consistent with this, Costa repeatedly explains that the two tiers form a "joint" or "collective[]" memory opening. *E.g.*, Costa, [0190] ("Each adjoining combination of a first-tier memory opening 149, a joint-level memory opening, and a second-tier memory opening 249 collectively constitutes a memory opening, or an inter-tier memory opening."), [0191] ("[E]ach second-tier memory opening 249 can be formed on top of a respective joint-level memory opening fill structure 67. In one embodiment, the bottom surface of each second-tier memory opening 249 … can have an areal overlap with the top surface of the underlying joint-level memory opening fill structure 67."), Fig. 21A.

221. This is also shown in Costa's figures. For instance, in Figure 21A above, Costa attempts to perfectly align the channel structures.

222. In my opinion, a POSITA would have found it obvious that the normal fabrication would largely align the channel structures, such that the holes almost completely overlap (as Costa depicts and describes), as Costa's goal is to align the



**Micron Ex. 1003, p. 96**
**Micron v. YMTC**
**IPR2025-00244**

structures for purposes of creating a joint or collective memory opening. Costa, [0191], Fig. 21A.

***[1.I] "forming a second functional layer on the sidewall of the second through hole;"***

223. This, in my opinion, is taught by Costa.

224. As per the '291 patent, a "second functional layer can be formed on the sidewall of second through hole 18." Ex. 1001, 14:1-2, Figs. 14-15.

225. The '291 patent's "second functional layer" is the same (albeit differently located) as the first functional layer. Ex. 1001, 14:3-5. This layer is shown in Figure 19 below:

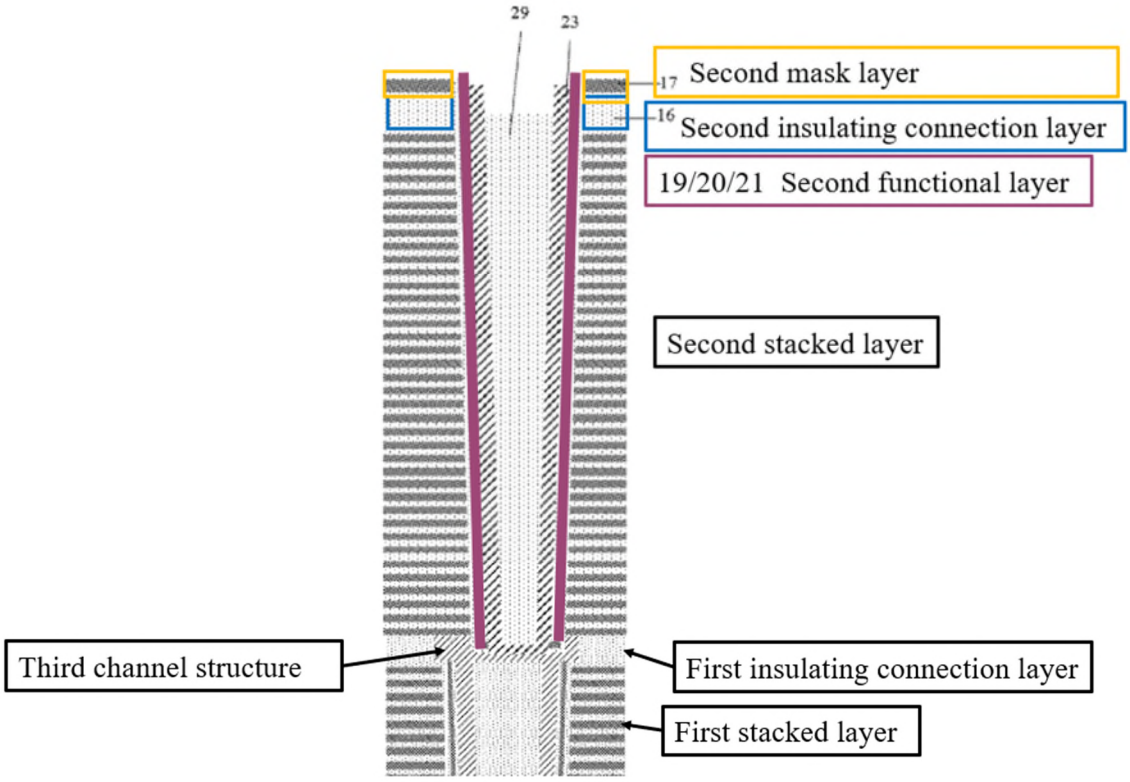



FIG. 19

*Id.*, Fig. 19 (annotated).

226. Costa teaches the formation of a second functional layer ("second memory film 250" with or without optional "second outer semiconductor channel layer 621") on the sidewall of the second through hole ("second-tier memory opening 249"). Costa, [0273].

227. In particular, Costa's second memory film 250 comprises "a stack of layers including a second blocking dielectric layer 252, a second charge storage layer 254, a second tunneling dielectric layer 256…." Costa, [0273], Figs. 21B-C.

228. An "optional second outer semiconductor channel layer 621" can also be "deposited into the second-tier memory opening[] 249." Costa, [0273].

229. This "stack of layers" is deposited in the second-tier memory opening 249 and subsequently etched to remove the portions above second-tier insulating cap layer 70 and at the bottom of second-tier memory opening 249, as shown in Figures 21B and 21C reproduced in annotated form below. Costa, [0273]-[0274].

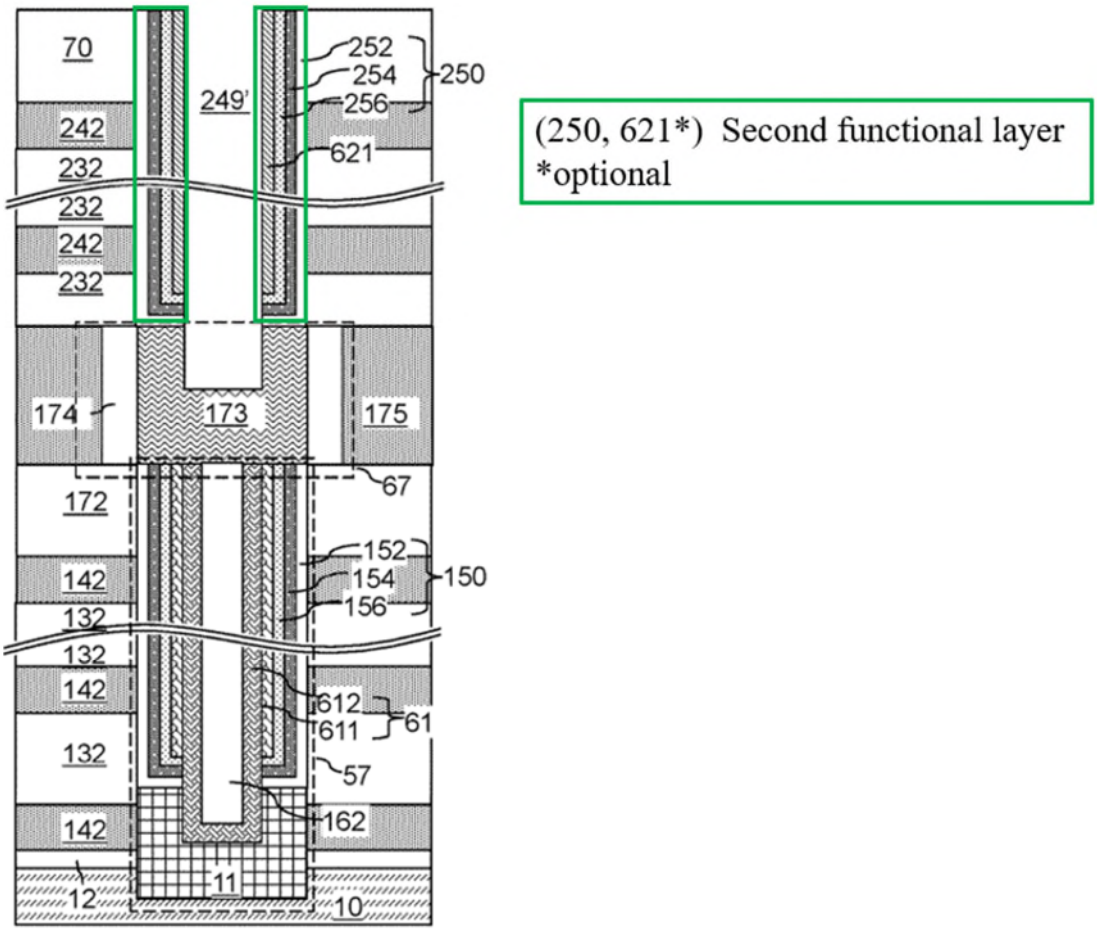



FIG. 21C

*Id.*, Figs. 21C (annotated).

230. For the same reasons that Costa's first functional layer is a functional layer, its second functional layer is a functional layer: both these layers perform a data storage function.

***[1.J] "forming a fourth channel structure and forming a second filling structure on the sidewall of the second functional layer and the exposed surface of the third channel structure; and"***

231. This, in my opinion, is taught by Costa.

232. In the ’291 patent, “a fourth channel structure and a second filling structure can be sequentially formed on the sidewall of the second functional layer and the exposed surface of the third channel structure” as shown in Figure 19 below. Ex. 1001, 14:44-47, Figs. 16-19.

233. This fourth channel structure can be composed of amorphous silicon and the second filling structure can be an oxide layer. Ex. 1001, 14:56-58, 14:61-63. Figure 19 below provides an example:

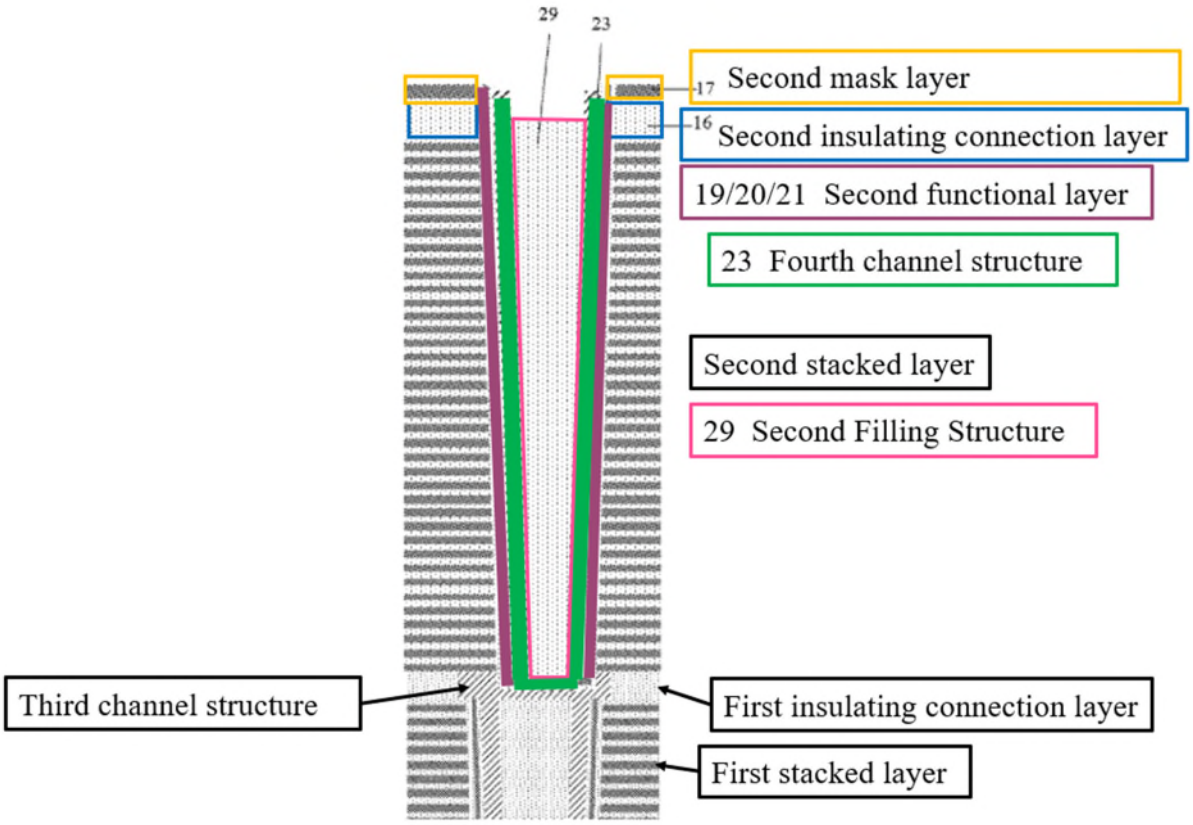



FIG. 19

*Id.*, Fig. 19 (annotated).

234. Costa likewise teaches forming a fourth channel structure ("second inner semiconductor channel layer 622" with or without the optional layer 621) and forming a second filling structure ("second dielectric core 262") on the sidewall of the second functional layer ("stack of layers" 252, 254, 256, 621) and the exposed surface of the third channel structure.

235. More particularly, in Costa, "a second inner semiconductor channel layer 622 can be deposited directly on the semiconductor surface of the second joint-level doped semiconductor portion 179." Costa, [0275] (and directly on optional semiconductor channel layer 621).

236. Again, as was the case with the first-tier structure, "an optional second outer semiconductor channel layer 621" can be deposited. Costa, [0273].

237. As shown in Figure 21D, the second inner semiconductor channel layer 622 can be deposited on the inner surface of functional layer (layers 250) and the exposed portion of the first joint-level doped semiconductor portion 173. Costa, [0275], Fig. 21D.

238. Costa also explains that "second dielectric core layer 262L" may be deposited as a core. Costa, [0275], Fig. 21.D.

239. A subsequent etching process removes "the horizontal portion of the second dielectric core layer 262L," leaving second dielectric core 162 within the second memory cavity 249'. Costa, [0276].

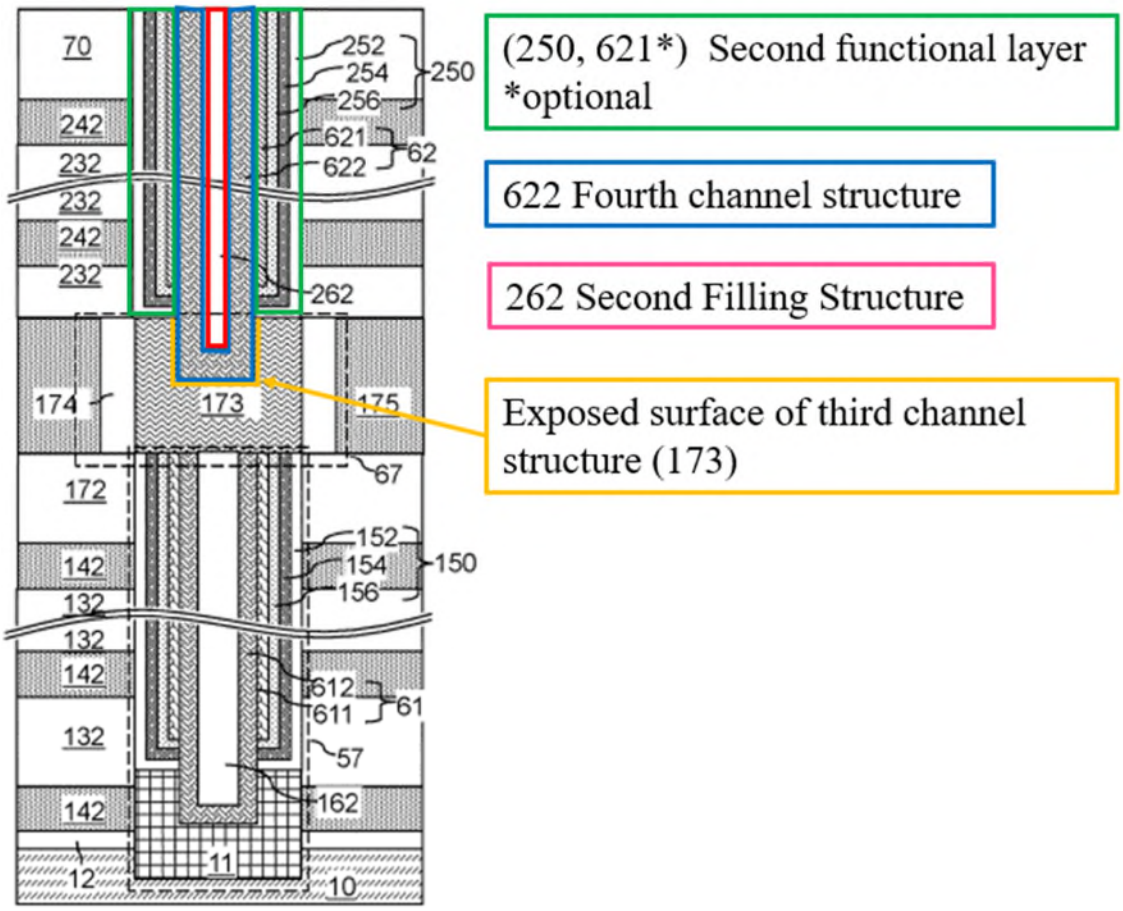



FIG. 21E

*Id.*, Fig. 21E (annotated).

240. Like Costa's second channel structures, layers 621 and 622 may be "amorphous silicon or polysilicon," and thus function as a channel. Costa, [0202], [0207].

***[1.K] "forming a fifth channel structure in contact with the fourth channel structure above the second through hole."***

241. This, in my opinion, is taught by Costa.

242. Per the '291 patent, the fifth channel structure is formed in a manner similar to that of the third channel structure (described above): "a second groove can

be formed on the fourth channel structure and the second filling structure, and in the second through hole 18." Ex. 1001, 15:12-14.

243. The "fifth channel structure can be formed in the second groove" and "the top surface of the second insulating connection layer 16 and the top surface of the fifth channel structure 30 can be planarized by any suitable techniques…." Ex. 1001, 15:24-36. This is shown in Figure 22B below:

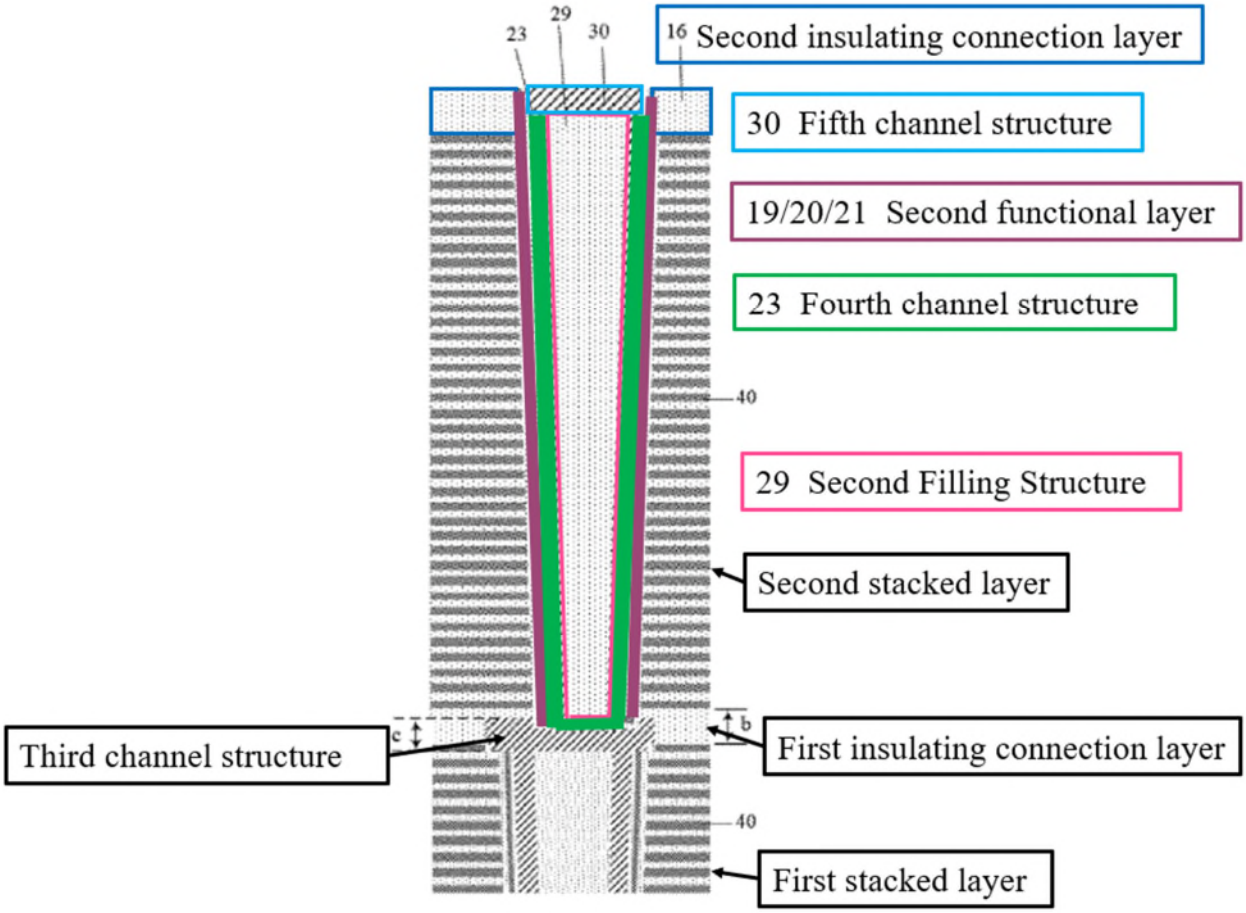



FIG. 22B

*Id.*, Fig. 22B (annotated).

244. This is also what Costa teaches. In Costa, a fifth channel structure ("drain region 63") in contact with the fourth channel structure ("second inner semiconductor channel layer 622") is formed above the second through hole ("second-tier memory opening 249"). Costa, [0277].

245. As shown in Figure 21F below, drain region 63 can be formed in a recess etched into second dielectric core 262 below the top surface of insulating cap layer 70:

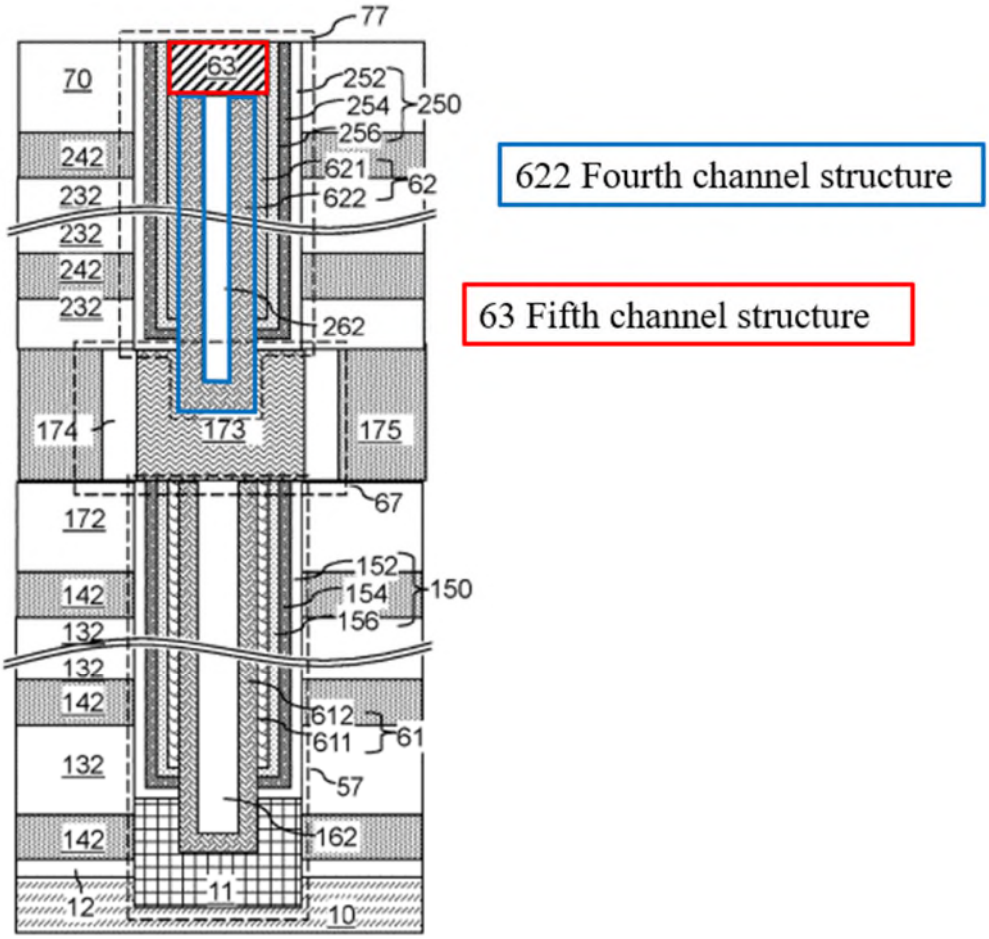



FIG. 21F

Costa, Fig. 21F (annotated), [0277].

246. As shown above, drain region 63 is in contact with second inner semiconductor channel layer 621 (and optional layer 622). Costa, Fig. 21F.

247. Further, as required, the drain regions are formed "above the second through hole."

248. Specifically, Costa's "second through hole" starts at the top of insulating layer 70. Costa describes forming drain regions in more detail with respect to its first embodiment, and then references back to this discussion regarding the conductive drains in later embodiments. *E.g.*, Costa, [0277].

249. As Costa describes, forming conductive regions first involves etching the groove for the conductive drain and then depositing polysilicon for the drain. Costa, [0212].

250. Next, "[e]xcess portions of the deposited semiconductor material can be removed from above the top surface of the insulating cap layer 70, for example, by chemical mechanical planarization (CMP) or a recess etch to form the drain regions 63." Costa, [0212].

251. So, in Costa the conductive drain (or "fifth channel structure") is initially above hole, and CMP levels the plug to the same height as the connection layer.

252. Patent Owner may attempt to argue that Costa's drain region 63 is not "form[ed] … above the second through hole" (second-tier memory opening 249)

because after completion of forming drain region 63, the top of drain region 63 is at the top of "the second through hole" (Costa's hole 249). Such an argument, in my opinion, would be incorrect.

253. First, Costa describes forming drain region 63 in exactly the same manner as the '291 patent describes its fifth channel structure in the '291 patent. In the '291 patent, "a fifth channel structure" is "above the second through hole" when it is at the same height as the connection layer 16. As shown in Figure 13, however, the '291 Patent depicts the top of "second through hole" 18 as being at the top of mask layer 17, which is above first insulating layer 16. Thus, this limitation cannot require that the "fifth channel structure" be fully above the "second through hole" after completing the method. Otherwise, it would not embrace what the '291 patent discloses.

254. Second, independent claim 1 recites a method, not an apparatus. Thus, any argument that Costa's drain region 63 is not "above" the second-tier memory opening 249 in its finished configuration is irrelevant. This limitation requires nothing more than that the fifth channel structure be "form[ed] … above the second through hole." Costa meets this limitation as written: its fifth channel structure is in fact "form[ed] … above" the then existing hole.

255. Moreover, independent claims 11 and 20, both of which are directed to "[a] joint opening structure of a three-dimensional (3D) memory device," reference



**Micron Ex. 1003, p. 106**
**Micron v. YMTC**
**IPR2025-00244**

"a fifth channel structure … disposed ***over*** the second through hole," not "a fifth channel structure … disposed ***above*** the second through hole." *See* Ex. 1001, cls. 11, 20.

256. The '291 patent's specification also does not describe any configuration where the "fifth channel structure" is above the fully completed hole. In each embodiment, the fifth channel structure is just like shown in Figure 22B above: the fifth channel structure is located at the top of the second through hole, its top surface planarized with the top surface of the second insulating connection layer. *E.g.*, Ex. 1001, 15:24-36, 24:21-38, 32:6-16, 40:39-58, Figs. 21A-B, 22A-B, 23B, 48A-B, 49A-B, 50B, 72A-B, 73A-B, 74B, 101A-B, 102A-B, 103B.

257. Claims 11 and 20, and the embodiments in the '291 patent's specification, make clear that what is claimed is not a fifth channel structure that is "above" the second through hole in its final configuration. Rather, the claims require only that the fifth channel structure be "form[ed] … above the second through hole" at the time of formation.

### 2. Claim 2

258. Claim 2 depends on claim 1 and further requires:

***[2.PRE] "The method of claim 1, wherein:"***
***[2.A] "the first stacked layer includes a first number of oxide/nitride layer pairs; and"***
***[2.B] "the second stacked layer includes a second number of oxide/nitride layer pairs."***

259. Costa, in my opinion, teaches what these limitations require.

260. Per Costa, "[t]he number of repetitions of the pairs of a first insulating layer 132 and a first sacrificial material layer 142 can be in a range from 2 to 1,024, and typically from 8 to 256." Costa, [0133]. And the same is true of the second alternating stack. *Id.*, [0182].

261. As I explained when discussing limitations [1.A] and [1.G] above, these stacked layers can be comprised of oxide/nitride layer pairs.

262. Patent Owner may argue that the claimed "first number" and "second number" must be different. This, in my opinion, would be incorrect.

263. Nothing in the '291 patent's claims or specification would require such an interpretation. Indeed, the patent explains that the words "first" and "second" are just meant to denote different physical stacks. *See* Ex. 1001, cl. 2, 43:18-21 ("[T]he words 'first', 'second' and the like used in this disclosure do not denote any order, quantity or importance, but are merely intended to distinguish between different constituents.") So, the "first number" is just the number of oxide/nitride layer pairs in the first stack, while the "second number" is just the number of oxide/nitride layer pairs in the second stack.

**3. Claim 3**

264. Claim 3 depends on claim 2 and further requires:

***[3] "The method of claim 2, wherein: the first number and the second number are not less than 32."***

265. In my opinion, this is taught by Costa for the same reasons discussed in connection with claim 2: Costa teaches the use of a number of layers that exceeds 32.

**4. Claim 4**

266. Claim 4 depends on claim 1 and further requires:

***[4.PRE] "The method of claim 1, wherein forming the first functional layer comprises:"***
***[4.A] "forming a first tunneling layer on the sidewall of the first through hole and the exposed surface of the first channel structure, wherein the first tunneling layer is configured, in operation, to generate charges;"***

267. Again, as I have explained, in discussing this claim I have applied YMTC's interpretation of this limitation as embracing layers formed in the opposite order as referenced in the claim and described in the '291 patent. *See supra* Section VIII.

268. Costa teaches what this claim requires when YMTC's interpretation is applied: in Costa, a first tunneling layer ("first tunneling dielectric layer 156") is formed on the sidewall of the first through hole (149') and exposed surface of the first channel structure (11):

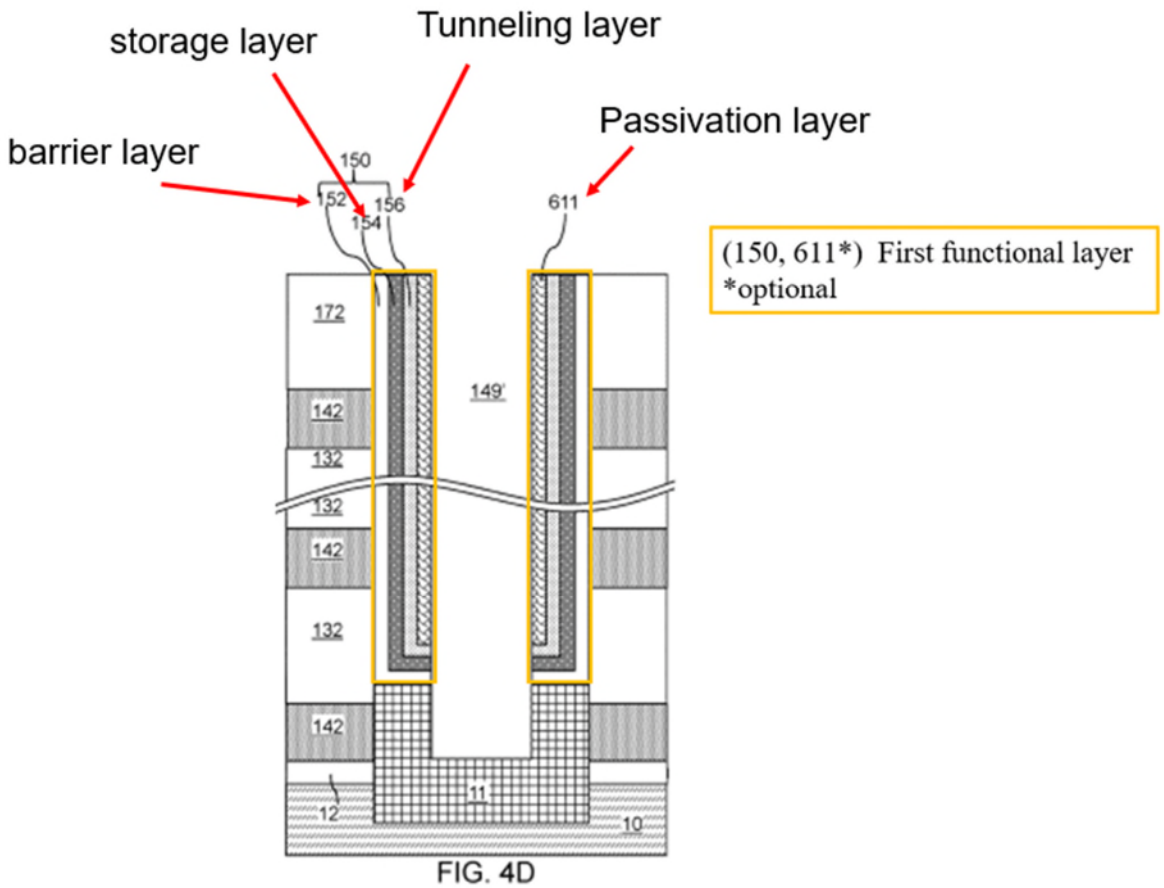


FIG. 4D

Costa, Fig. 4D (annotated), [0144] (sequentially forming layers 152, 154, 156, and 611).

269. This limitation also requires that the "first tunneling layer" be configured to "generate charges." Here, the '291 patent explains that "[t]he first tunneling layer 7 can be used for generating electronic charges (electrons or holes). In some embodiments, the first tunneling layer 7 can be an oxide layer formed by using a deposition process." Ex. 1001, 10:46-50.

270. An oxide layer does not "generate" charge by itself. So, this claim and the '291 patent, are apparently using the term "generate" to refer to the fact that

electronic charges tunnel through this layer (as an oxide layer does not "generate" charges by itself), and hence the layer "generates" charges for the data storage layer.

271. Costa teaches that its tunneling layer operates the same way by allowing electrons to tunnel for storage purposes: "first tunneling dielectric layer 156 includes a dielectric material through which charge tunneling can be performed under suitable electrical bias conditions." Costa, [0151].

***[4.B] "forming a first storage layer on the surface of the first tunneling layer to store the charges generated by the first tunneling layer;"***

272. In my opinion, when YMTC's understanding of this claim is applied, Costa teaches forming a first storage layer ("first charge storage layer 154") on the first tunneling layer ("first tunneling dielectric layer 156").

273. These layers are shown in Figure 4D below:



**Micron Ex. 1003, p. 111**
**Micron v. YMTC**
**IPR2025-00244**

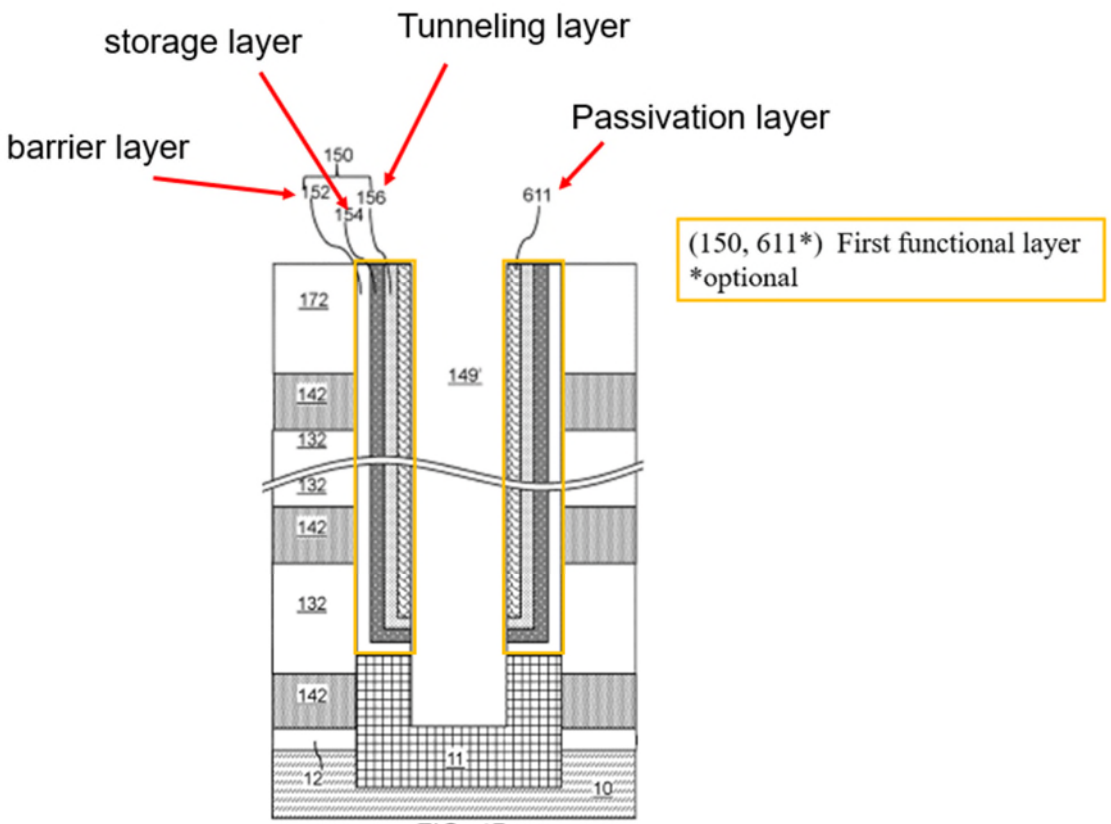


FIG. 4D

Costa, Fig. 4D (annotated), [0144] (sequentially forming layers 152, 154, 156, and 611).

274. This limitation also references "stor[ing] the charges generated by the first tunneling layer."

275. Again, Costa explains that "first tunneling dielectric layer 156 includes a dielectric material through which charge tunneling can be performed under suitable electrical bias conditions." Costa, [0151].

276. Costa's "first charge storage layer 154" stores the charges that tunnel through "first tunneling dielectric layer 156": "[t]he first charge storage layer 154

can comprise a charge trapping material or a floating gate material." Costa, [0154]; *id.*, [0148] ("first charge storage layer 154 can be a continuous layer or patterned discrete portions of a charge trapping material including a dielectric charge trapping material").

***[4.C] "forming a first barrier layer on the surface of the first storage layer to block the outflow of charges in the first storage layer;"***

277. In my opinion, when YMTC's understanding of this claim is applied, Costa teaches forming a first barrier layer ("first blocking dielectric layer 152") on the surface of the first storage layer ("first charge storage layer 154").

278. This is shown in Figure 4D below:



**Micron Ex. 1003, p. 113**
**Micron v. YMTC**
**IPR2025-00244**

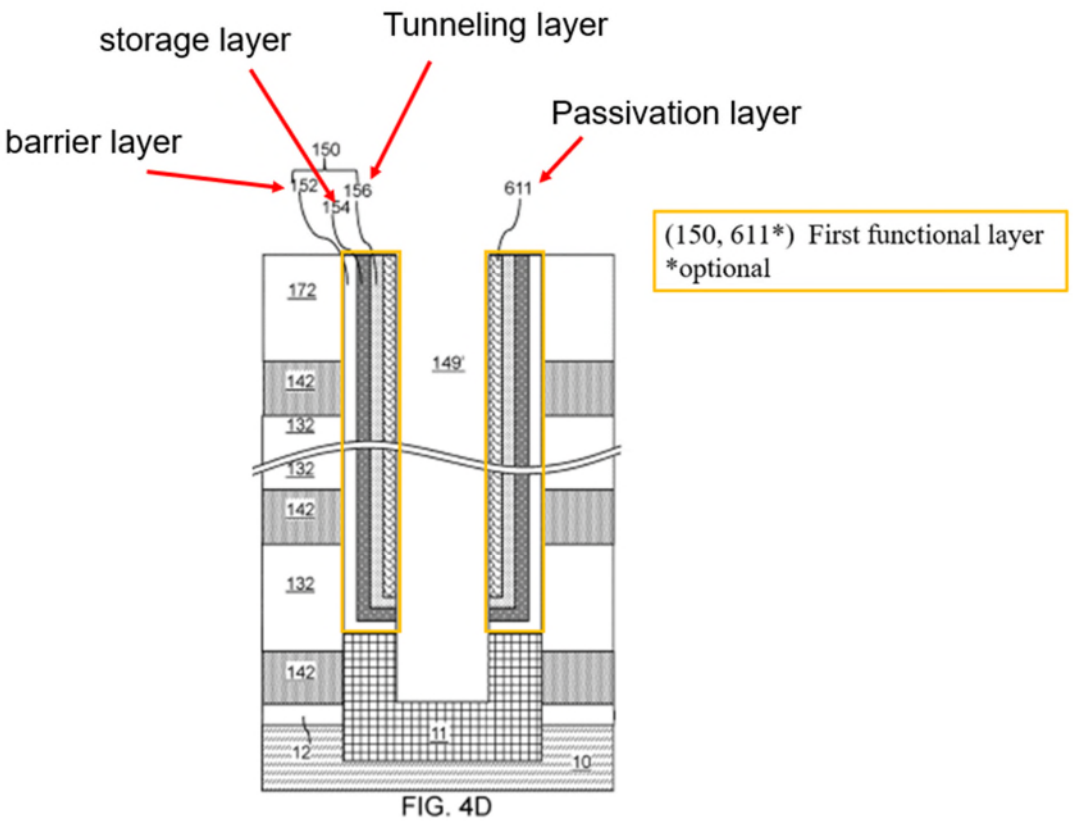


FIG. 4D

Costa, Fig. 4D (annotated), [0144] (sequentially forming layers 152, 154, 156, and 611).

279. This limitation also requires that the layer "block the outflow of charges in the first storage layer."

280. Here, Costa teaches that its "first blocking dielectric layer 152 can include a single dielectric material layer or a stack of a plurality of dielectric material layers." Costa, [0145].

281. This blocking layer is a barrier layer because it "block[s]" the outflow of charges from the storage layer into the gate layers. Costa, [0145].

***[4.D] "forming a first passivation layer on the surface of the first barrier layer to protect the first barrier layer from being damaged in a subsequent removal process; and"***

282. In my opinion, when YMTC's understanding of this claim is applied, Costa teaches forming a first passivation layer ("first outer semiconductor channel layer 611") on the surface of the barrier layer ("first blocking dielectric layer 152").

283. This is also shown in Figure 4D:

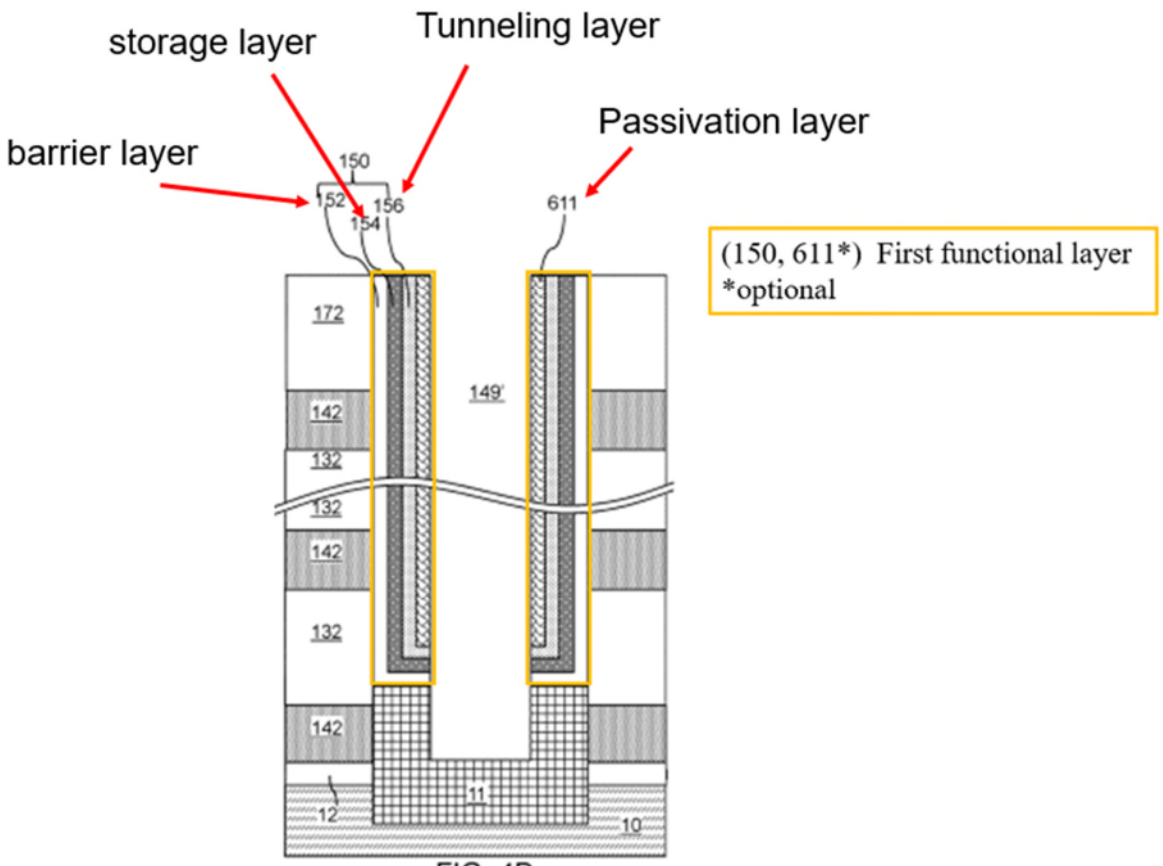


FIG. 4D

Costa, Fig. 4D (annotated), [0144] (sequentially forming layers 152, 154, 156, and 611).

284. This limitation also requires that the claimed layer be configured "to protect the first barrier layer from being damaged in a subsequent removal process."

285. Per the '291 patent, the "passivation layer" protects the barrier layer during removal of the bottom portion of the functional layer. Ex. 1001, 11:3-17.

286. The patent also explains that the first passivation layer may comprise "amorphous silicon" i.e., a semiconductor material. Ex. 1001, 11:7-9.

287. This is what Costa teaches. In Costa, "optional first outer semiconductor channel layer 611 includes … semiconductor materials known in the art." Costa, [0152].

288. After this layer is deposited, a subsequent etching process removes portions of the layer and the other layers of the first functional layer. This process is discussed in greater detail below in connection with limitation [4.E]

289. In my opinion, a POSITA would have considered layer 611 to be "passivation layer" because it protects the data storage layer during the removal of the bottom portion of layers 152, 154, 156, and 611.

290. Further, just like the '291 patent's passivation layer, Costa's passivation layer is "amorphous silicon" i.e., a semiconductor material. Costa, [0152].

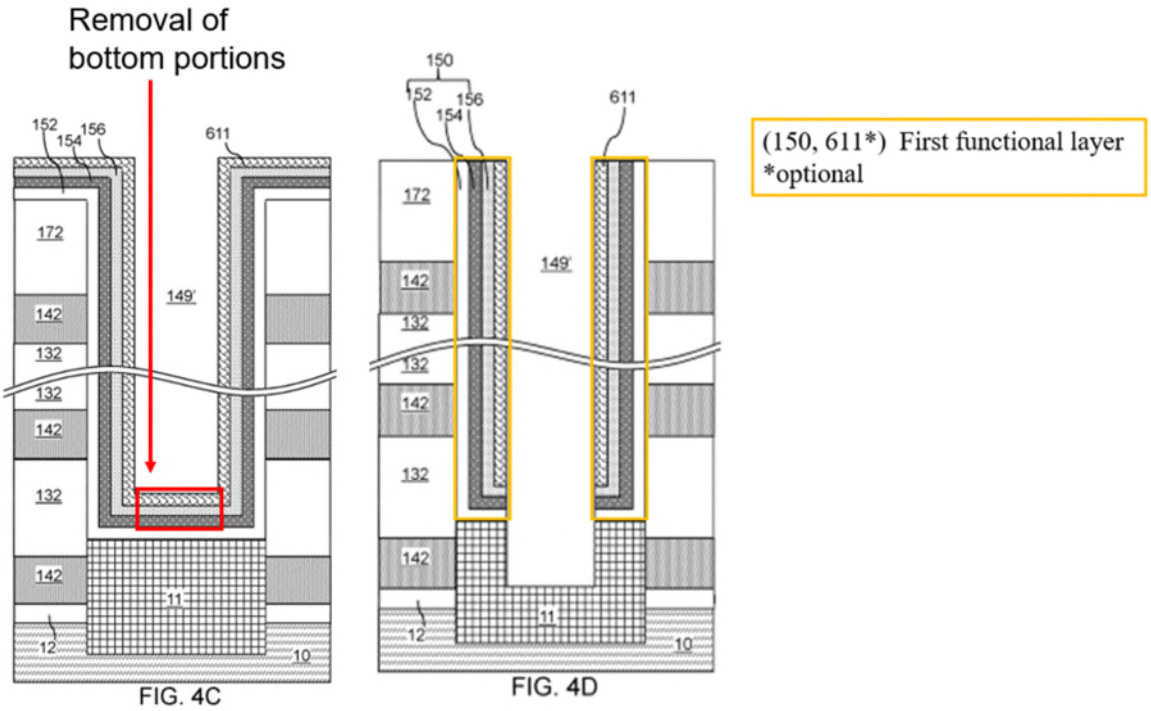


**Micron Ex. 1003, p. 116**
**Micron v. YMTC**
**IPR2025-00244**

***[4.E] "removing portions of the first passivation layer, the first barrier layer, the first storage layer, and the first tunneling layer on the surface of the first channel structure, wherein remaining portions of the first passivation layer, the first barrier layer, the first storage layer, and the first tunneling layer on the sidewall of the first through hole to form the first functional layer."***

291. In my opinion, when YMTC's understanding of this claim is applied, Costa teaches what this limitation requires.

292. As the annotated versions of Figures 4C and 4D below show, Costa removes the bottom portions of its functional layers to expose the first channel structure:




Costa, Figs. 4C, 4D (annotated), [0153] ("portions of the first outer semiconductor channel layer 611, the first tunneling dielectric layer 156, the first charge storage

layer 154, and the first blocking dielectric layer 152 at a bottom of each first memory cavity 149′ can be removed”).

### 5. Claim 5

293. Claim 5 depends on claim 4 and further requires:

***[5.PRE] “The method of claim 4, wherein forming the second channel structure and the first filling structure comprises:” [5.A] “forming a second channel layer that covers the sidewall of the first passivation layer and the exposed surface of the first channel layer;***

294. This, in my opinion, is taught by Costa.

295. As I discussed above in greater detail in connection with limitation [1.E], in Costa “a first inner semiconductor channel layer 612 can be deposited directly on the semiconductor surface of the epitaxial channel portion 11 … and directly on the first outer semiconductor channel layer 611.” Costa, [0156].

***[5.B] “forming the first filling layer that covers the surface of the second channel layer;”***

296. This is also taught by Costa.

297. Again, as I discuss above in connection with limitation [1.E], in Costa “a first dielectric core layer 162L can be deposited in the first memory cavity 149' to fill any remaining portion….” Costa, [0158], Fig. 4F.

***[5.C] “removing a portion of the first filling layer to form the first filling structure, wherein the top surface of the first filling structure is lower than the top surface of the first insulating connection layer; and [5.D] “removing a portion of the second channel layer to form the second channel structure, wherein a top surface of the second channel structure is lower than a top surface of the first insulating connection layer.”***

298. This is all either taught or rendered obvious by Costa.

299. Collectively, these limitations require recessing the filling layer and second channel layer to form a filling structure and second channel structure in which the top surface of both are below the first insulating connection layer.

300. In my opinion, a POSITA would have considered it obvious to recess the structures below the insulating connection layer (layer 172) in Costa.

301. There are a number of reasons for this. To begin, Costa expressly recognizes the desire to reduce the height of the device: "Referring to FIG. 22A, an alternate embodiment of the third exemplary structure after formation of the second memory opening fill structures 77, which is derived from the third exemplary structure by reducing the thicknesses of each joint-level doped semiconductor portions 173, each single annular dielectric spacer 174, and the joint-level spacer material layer 175, for example, to a range from 20 nm to 150 nm, although lesser and greater thicknesses can also be employed." Costa, [0281].

302. This reduction can be seen by comparing Figures 21B and 22A below:

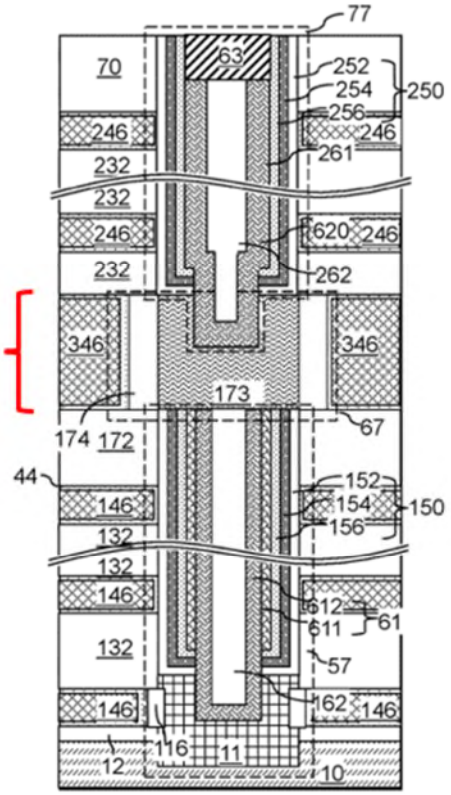



FIG. 21G

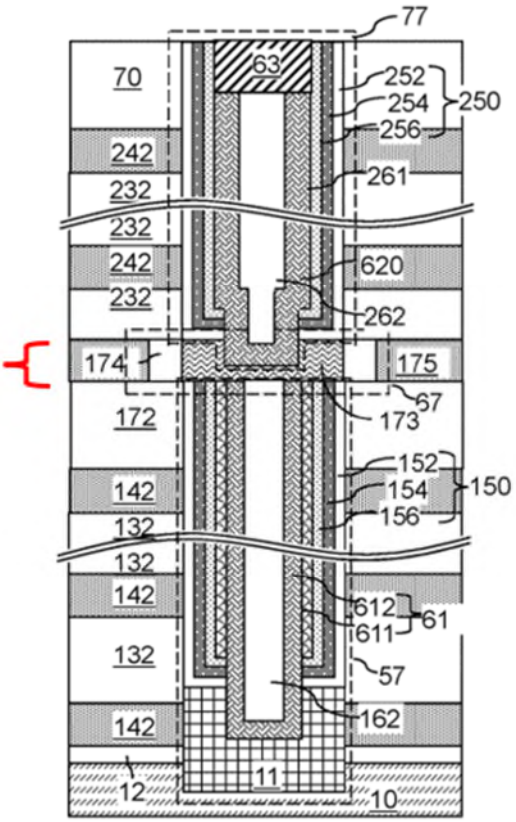


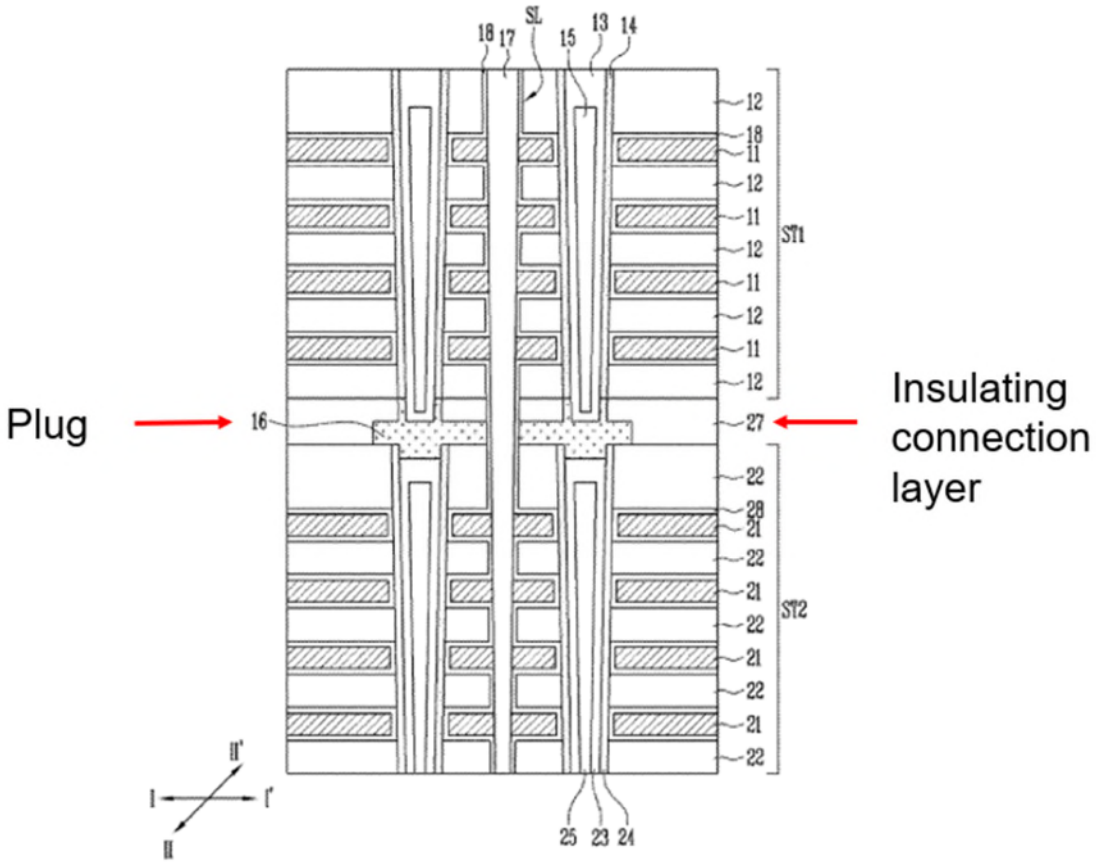

FIG. 22A

Costa, Figs. 21G (annotated), 22A (annotated).

303. It was also well-known that the height of a multi-tiered memory structure could be reduced by simply recessing the interface plug into the insulating connection layer.

304. The below figure from U.S. Patent No. 9,245,962 (Ex. 1016) provides an example of this:

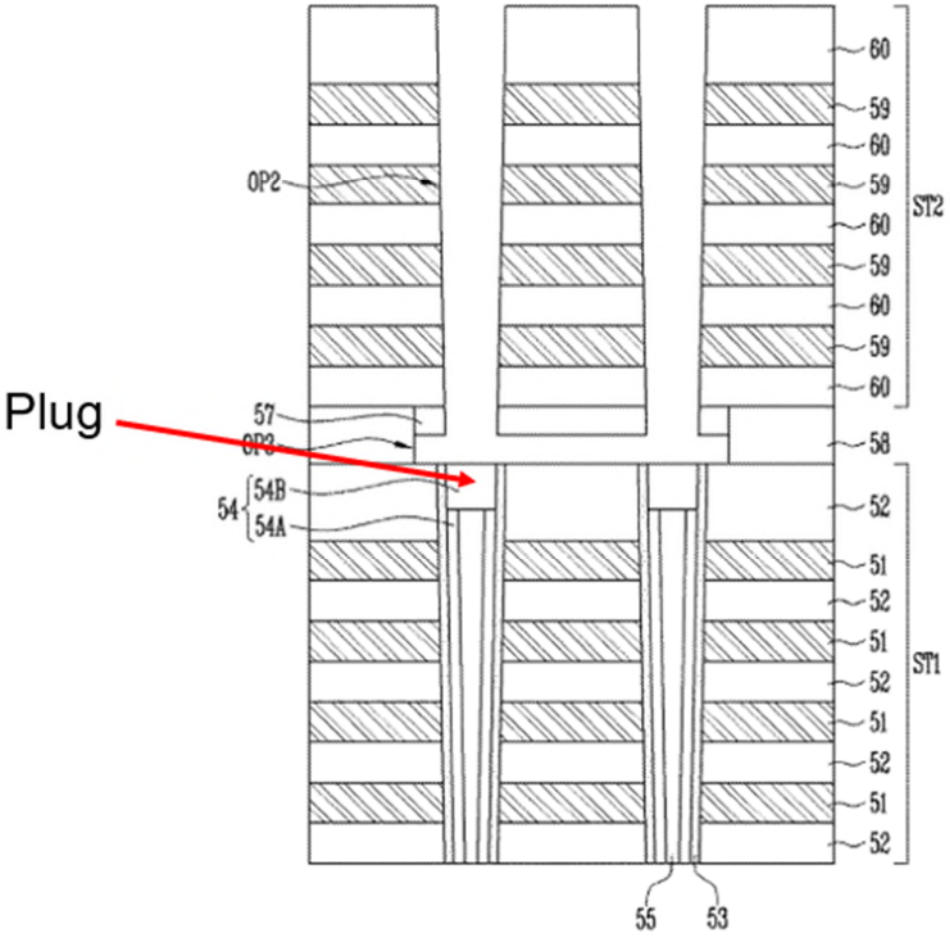
FIG. 4B




Ex. 1016, Fig. 4B (annotated), 4:63-5:9 (discussing insulating layer 27 and connection pattern 16).

305. This design involves recessing the channel structure and dielectric core into the insulating layer to reduce the height and then placing the plug in the recess:

FIG. 5B




Ex. 1017, Fig. 5B (annotated), 9:44-61 (forming recessed plug).

306. Applying this to Costa results in the following:

Original

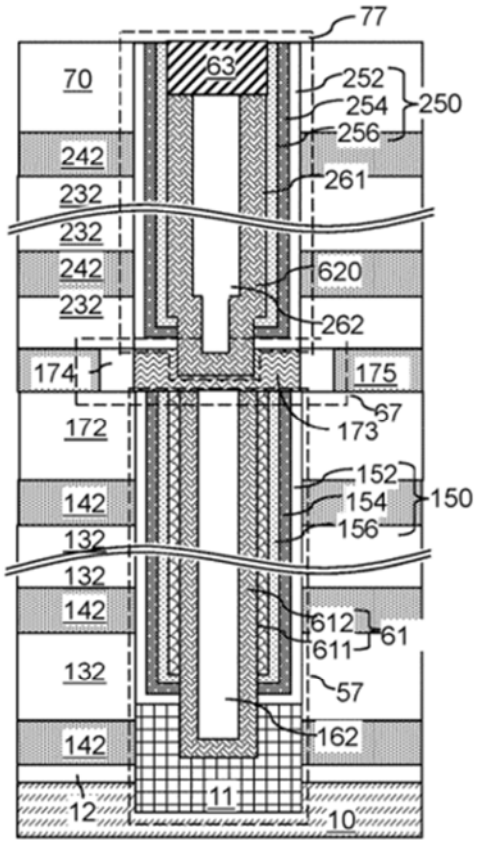



FIG. 22A

Modified

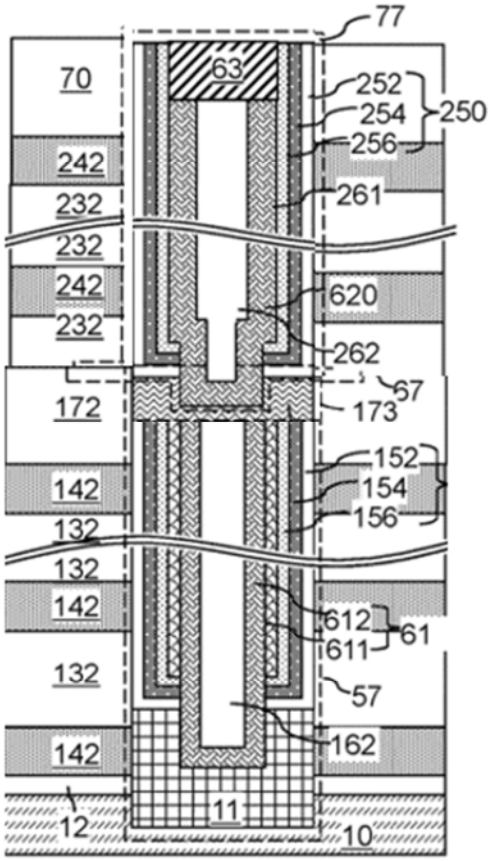



FIG. 22A

Costa, Figs. 22A (original), 22A (modified).

307. Again, a POSITA would have considered it highly obvious to recess the interface plug into the insulating connection layer because doing so would further—as shown above—the expressed goal of reducing the overall height of Costa's structure. The height would be reduced because the recessed plug would obviate layers 174/175.

308. In addition to further Costa's express goal to lower the height of the device (the height of a device impacts fabrication in multiple ways, e.g., requires

longer etching time to form holes through the stack), a POSITA would have understood that recess techniques improve contact resistance.

309. It was well known when the ’291 patent was filed that increasing the contact area decreases the contact resistance. *See, e.g.*, Ex. 1018 (Stavitski), 1 (“the contact resistance depends on the contact area[]”); Ex. 1019 (Fasoli), 10 (“small contact area tends to give rise to high contact resistance.”).

310. In fact, a POSITA would have understood that Costa itself implicitly recognizes this via the design of the lower and upper channel structures.

311. As shown in Fig. 21F below, Costa etches portions of first channel structure 11 and third channel structure 173 to expose the sidewall channels. Then, Costa deposits the second channel structure 162 and fourth channel structure 620 therein, thereby increasing the contact area between these structures.

312. But, Costa did not follow a similar procedure when forming the interface between the sub-channels.

313. A POSITA would have recognized that by employing well-known recessing techniques, the conductive third channel structure 173 would be formed in a further recess of 162. This would not only decrease the height of the structure, but would decrease contact resistance.

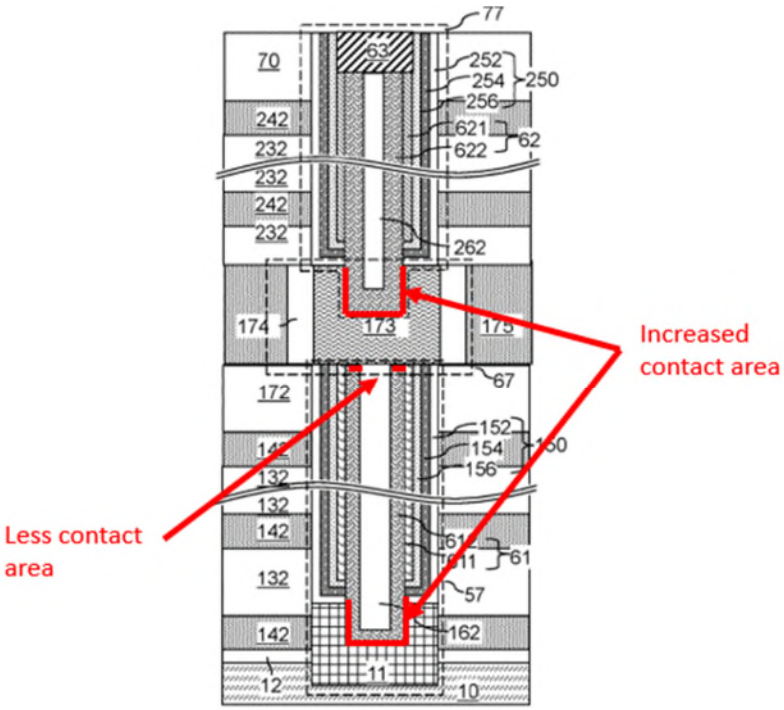



FIG. 21F

Costa, Fig. 21F (annotated).

314. In my opinion, a POSITA would have had a reasonable expectation of success when employing a recess with Costa.

315. First, as shown above, it was well-known in the art to form a recess to reduce height and improve contact resistance. Indeed, Costa itself already discusses the formation of recesses and then the provision of materials into the recess.

316. Moreover, a POSITA would have recognized that a recess can be formed via masking and anisotropic etch, manufacturing techniques that Costa already employs.

**6. Claim 8**

317. Claim 8 depends on claim 1 and further requires:

***[8.PRE] "The method of claim 1, further comprising:" [8.A] "forming a first mask layer overlaying the first insulating connection layer before forming the first through hole; and"***

318. This, in my opinion, is taught by Costa.

319. As I discuss above when discussing limitation [1.B], Costa explains that "[t]o form the first-tier openings (149, 119), a lithographic material stack (not shown) including at least a photoresist layer can be formed over the first tier structure (132, 142, 172, 165), and can be lithographically patterned to form openings within the lithographic material stack." Costa, [0137] ("The pattern in the lithographic material stack can be transferred through the entirety of the first tier structure (132, 142, 172, 165) by at least one anisotropic etch that employs the patterned lithographic material stack as an etch mask.").

***[8.B] "removing the first mask layer after forming the first filling structure;"***

320. In my opinion, Costa teaches what this limitation requires.

321. In particular, in Costa "the patterned lithographic material stack can be subsequently removed, for example, by ashing." Costa, [0138].

***[8.C] "forming a second mask layer on the second insulating connection layer before forming the second through hole; and"***

322. In my opinion, Costa teaches what this limitation requires.

323. As I explained above when discussing limitation [1.H], in Costa "a lithographic material stack (not shown) including at least a photoresist layer can be formed over the second tier structure (232, 242, 265, 70), and can be lithographically

patterned to form openings within the lithographic material stack." Costa, [0192] ("The pattern in the lithographic material stack can be transferred through the entirety of the second tier structure (232, 242, 265, 70) by at least one anisotropic etch that employs the patterned lithographic material stack as an etch mask.").

***[8.D] "removing the second mask layer after forming the second filling structure."***

324. In my opinion, Costa teaches what this limitation requires.

325. Once again, Costa explains that after the mask is employed "[s]ubsequently, the patterned lithographic material stack can be subsequently removed, for example, by ashing." Costa, [0194]

**7. Claim 9**

326. Claim 9 depends on claim 1 and further requires:

***[9.PRE] "The method of claim 1, wherein forming the fourth channel structure and the second filling structure comprises:" [9.A] "forming a fourth channel layer that covers the sidewall of a second functional layer and the exposed surface of the third channel layer;"***

327. In my opinion, Costa teaches what this limitation requires.

328. As discussed in greater detail above in connection with limitation [1.J], Costa teaches that its second inner semiconductor channel layer 622 (the fourth channel structure) can be deposited on the inner surface of second outer semiconductor channel layer 621 and the exposed portion of the first joint-level doped semiconductor portion 173. Costa, [0275], Fig. 21D.

***[9.B] "forming a second filling layer that covers the surface of the fourth channel layer;"***

329. In my opinion, Costa teaches what this limitation requires.

330. As discussed in greater detail above when addressing limitation [1.J], when Costa's second-tier memory opening 249 is not completely filled, the cavity is filled with "second dielectric core layer 262L." Costa, [0275], Fig. 21D.

***[9.C] "removing a portion of the second filling layer to form the second filling structure, wherein the top surface of the second filling structure is lower than the top surface of the second insulating connection layer; and"***

331. In my opinion, Costa teaches what this limitation requires.

332. As discussed in greater detail above when addressing limitation [1.J], Costa removes the horizontal portions of dielectric core layer 262L located above second-tier insulating cap layer 70. Costa, [0276].

333. Further, as discussed above in connection with limitation [1.K], Costa's dielectric core 262 is recess etched "below the top surface of the insulating cap layer 70," creating a groove in which drain region 63 is deposited. Costa, [0277], Fig. 21F.

334. The below annotated version of Figure 21F shows this:

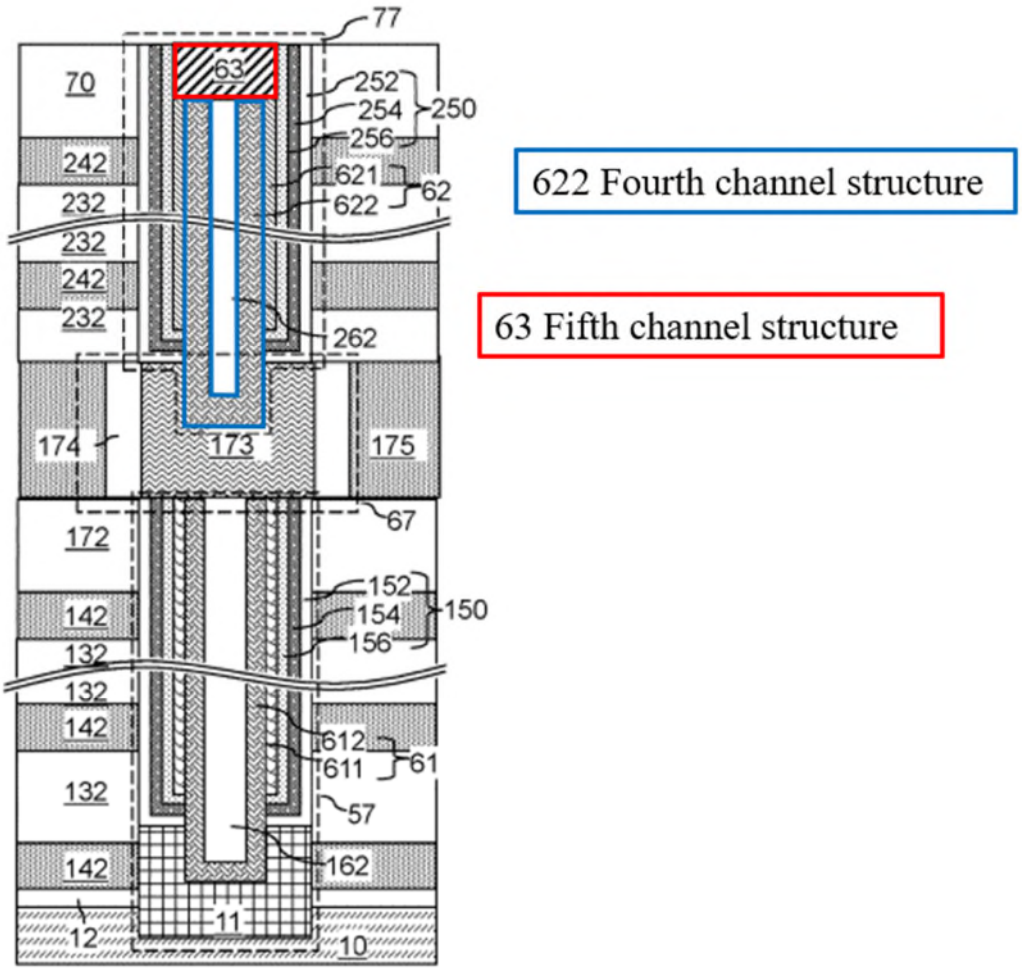



FIG. 21F

Costa, Fig. 21F (annotated).

***[9.D] "removing a portion of the fourth channel layer to form the fourth channel structure, wherein a top surface of the fourth channel structure is lower than a top surface of the second insulating connection layer."***

335. In my opinion, Costa teaches what this limitation requires.

336. As discussed above in connection with limitation [1.J], Costa removes the horizontal portions of second inner semiconductor channel layer 622 located above second-tier insulating cap layer 70. Costa, [0276]

337. Further, as I discussed above when addressing limitation [1.K], dielectric core 162 is recess etched "below the top surface of the insulating cap layer 70," creating a groove in which drain region 63 is deposited. Costa, [0277], Fig. 21F.

### 8. Claim 11

338. Claim 11 is another independent claim.

***[11.PRE] "A joint opening structure of a three-dimensional (3D) memory device, comprising:"***

339. To the extent this preamble is limiting, in my opinion it is taught for the same reasons explained above for the preamble of claim 1. Substantively, this preamble is identical to [1.PRE]: while claim 1 is directed to a method, the method of that claim forms the memory device joint opening structure this claim requires.

***[11.A] "a first stacked layer disposed overlaying a substrate;"***

340. This limitation is present in and thus is taught by Costa for the same reasons I describe above for limitation [1.A].

***[11.B] "a first insulating connection layer disposed on the first stacked layer;"***

341. This limitation is present in and thus is taught by Costa for the same reasons I describe above for limitation [1.A].

***[11.C] "a first through hole penetrating the first stacked layer and the first insulating connection layer;"***

342. This limitation is present in and thus is taught by Costa for the same reasons I describe above for limitation [1.B].



**Micron Ex. 1003, p. 130**
**Micron v. YMTC**
**IPR2025-00244**

***[11.D] "a first channel structure disposed at the bottom of the first through hole and overlaying the substrate;"***

343. This limitation is substantively the same as limitation [1.C] discussed above. The only difference is that it uses the phrase "disposed at the bottom of the first through hole" and omits "that is exposed by the first through hole." As a result, in my opinion it is taught by Costa for the same reasons I explained for limitation [1.C].

***[11.E] "a first functional layer disposed on the sidewall of the first through hole;"***

344. This limitation is substantively the same as limitation [1.D] discussed above. The only difference is that it uses the phrase "disposed on" instead of "on." As a result, in my opinion it is taught by Costa for the same reasons I explained for limitation [1.D].

***[11.F] "a second channel structure in contact with the first channel structure disposed on the sidewall of the first functional layer;"***

345. This limitation is present in and thus is taught by Costa for the same reasons I describe above for limitation [1.E].

346. More particularly, as I have explained, in Costa a second channel structure (vertical semiconductor channel) is in connect with a first channel structure (epitaxial pedestal at bottom) and first functional layer ("first memory film 150" with or without the optional semiconductor channel layer 611).



**Micron Ex. 1003, p. 131**
**Micron v. YMTC**
**IPR2025-00244**

***[11.G] "a third channel structure in contact with the second channel structure disposed over the first through hole, wherein a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate;"***

347. This limitation is substantively the same as limitation [1.F] discussed above. The only difference is that it uses the phrase "disposed over" instead of "form[ed] … above." As a result, in my opinion it is taught (or at least rendered obvious) by Costa for the same reasons I explained for limitation [1.F].

***[11.H] "a second stacked layer disposed on the third channel structure;"***

348. This limitation is present in and thus is taught by Costa for the same reasons I describe above for limitation [1.G].

***[11.I] "a second insulating connection layer disposed on the second stacked layer;"***

349. This limitation is present in and thus is taught by Costa for the same reasons I describe above for limitation [1.G].

***[11.J] "a second through hole penetrating the second stacked layer and the second insulating connection layer, wherein a projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate;"***

350. This limitation is present in and thus is taught by Costa for the same reasons I describe above for limitation [1.H].

***[11.K] "a second functional layer disposed on the sidewall of the second through hole;"***

351. This limitation is substantively the same as limitation [1.I] discussed above. The only difference is that it uses the phrase "disposed on" instead of "on."

As a result, in my opinion it is taught (or at least rendered obvious) by Costa for the same reasons I explained for limitation [1.I].

***[11.L] "a fourth channel structure in contact with the third channel structure disposed on the sidewall of the second functional layer; and"***

352. This limitation is present in and thus is taught by Costa for the same reasons I describe above for limitation [1.J].

***[11.M] "a fifth channel structure in contact with the fourth channel structure disposed over the second through hole."***

353. This limitation is substantively the same as limitation [1.K] discussed above. The only difference is that it uses the phrase "disposed over" instead of "form[ed] … above." As a result, in my opinion it is taught (or at least rendered obvious) by Costa for the same reasons I explained for limitation [1.K].

**9. Claim 12**

354. Claim 12 depends on claim 11 and further requires:

***[12.PRE] "The joint opening structure of claim 11, further comprising:" [12.A] "a first filling structure covering the surface of the second channel structure; and"***

355. This limitation is present in and thus is taught by Costa for the same reasons I describe above for limitation [1.E].

***[12.B] "a second filling structure covering the surface of the fourth channel structure;"***

356. This limitation is present in and thus is taught by Costa for the same reasons I describe above for limitation [1.J].

***[12.C] "wherein the first through hole is non-interconnected with the second through hole."***

357. In my opinion, Costa teaches what this limitation requires.

358. More particularly, when forming second-tier memory openings 249, Costa explains that "second-tier memory openings 249 are formed through the second tier structure (232, 242, 70, 265) in areas that overlap with the joint-level memory opening fill structures 67, i.e., with the joint-level memory openings." Costa, [0191]; Figs. 10A-10B.

359. Costa also explains that "FIG. 21A" (and the figures that follow) "illustrate a region of the second exemplary structure at the processing steps of FIGS. 10A and 10B, i.e., after formation of the second-tier memory openings 249…." *Id.*, [0272]; Fig. 21A.

360. As illustrated in Fig. 21F, in Costa, first-tier memory openings (filled in Fig. 21F with first memory opening fill structures 57) are non-interconnected with second-tier memory openings 249 (filled in Fig. 21F with second memory open opening fill structures 77). As shown below, there are joint-level doped semiconductor portions 173 interposed between the first-tier and second-tier memory openings:

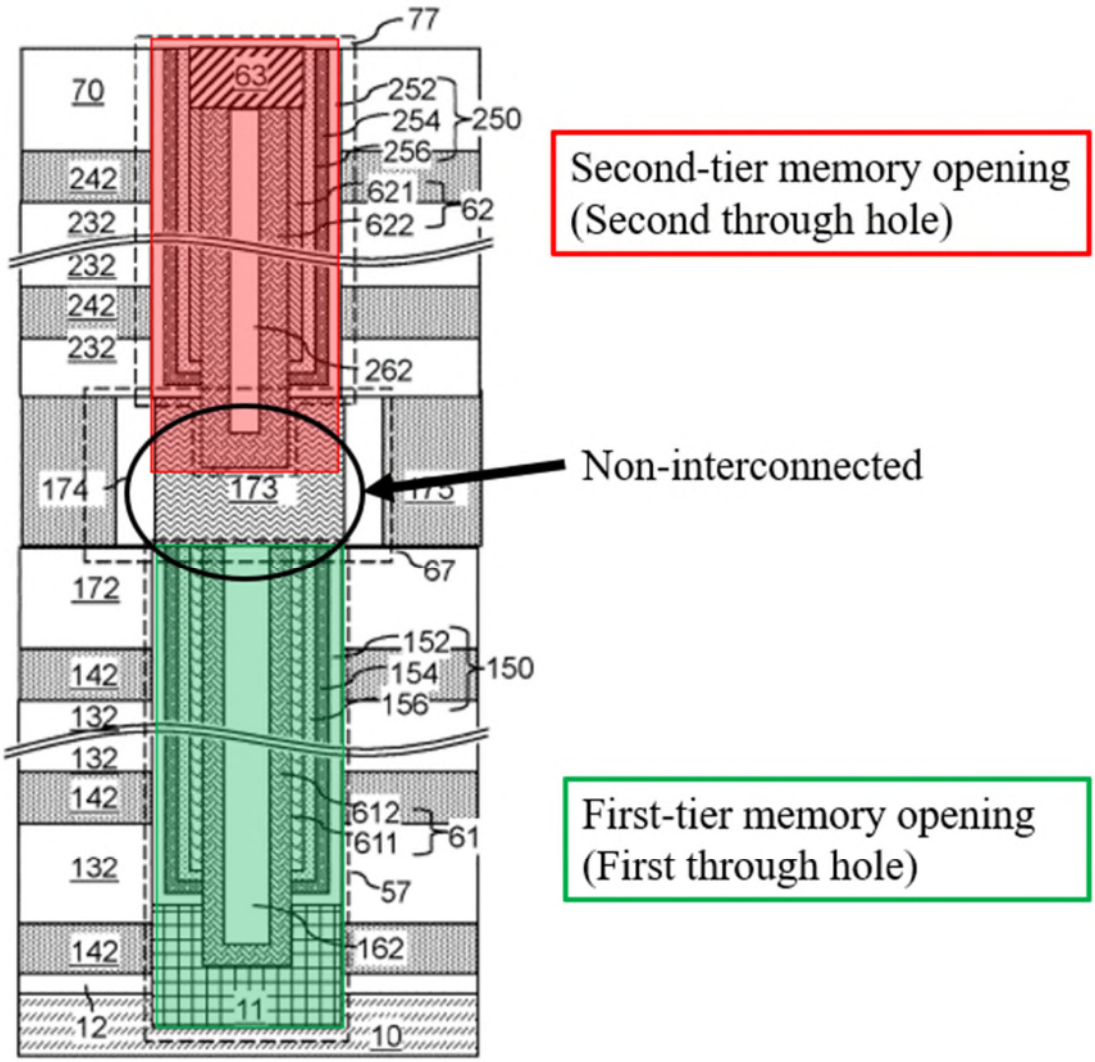



FIG. 21F

Costa, Fig. 21F (annotated).

### 10. Claim 14

361. Claim 14 depends on claim 11 and further requires:

***[14.PRE] "The joint opening structure of claim 11, wherein:" [14.A] "the first stacked layer includes a first number of conductor/dielectric layer pairs; and" [14.B] "the second stacked layer includes a second number of conductor/dielectric layer pairs."***

362. These limitations are the same as [2.A-B] and thus are taught by Costa for the same reasons I describe above for those limitations.

**11. Claim 15**

363. Claim 15 depends on claim 14 and further requires:

***[15] "The joint opening structure of claim 14, wherein: the first number and the second number are not less than 32."***

364. This limitation is the same as [3] and thus is taught by Costa for the same reasons I describe above for that limitation.

**12. Claim 16**

365. Claim 16 depends on claim 11 and further requires:

***[16.PRE]-[16.B] "The joint opening structure of claim 11, wherein: the first stacked layer includes a first number of oxide/nitride layer pairs; and the second stacked layer includes a second number of oxide/nitride layer pairs.***

366. These limitations are the same as [2.A-B] and thus are taught by Costa for the same reasons I describe above for those limitations.

**13. Claim 17**

367. Claim 17 depends on claim 16 and further requires:

***[17] "The joint opening structure of claim 16, wherein: the first number and the second number are not less than 32."***

368. This limitation is the same as [3] and thus is taught by Costa for the same reasons I describe above for that limitation.

### 14. Claim 18

369. Claim 18 depends on claim 11 and further requires:

***[18] "The joint opening structure of claim 11, wherein: a thickness of the third channel structure is in a range between 30 nm and 70 nm."***

370. In my opinion, Costa teaches that this limitation requires.

371. Per Costa, "[t]he thickness of the first joint-level doped semiconductor layer 173L can be in a range from 20 nm to 100 nm, although lesser and greater thicknesses can also be employed." Costa, [0163].

372. A POSITA would have understood that Costa teaches use of range of layer thickensses—overlapping the claimed range—because the other elements of Costa's stack also have ranges of thicknesses. The ranges are simply meant to reflect the fact that reflect that different processes may be employed to fabricate the device. *E.g.*, Costa, [0139], [0146]-[0147], [0150], [0182].

373. I also note that the '291 patent, like Costa, similarly discloses ranges for various layers. *E.g.*, Ex. 1001, 9:38-44.

### 15. Claim 19

374. Claim 19 depends on claim 11 and further requires:

***[19.PRE] "The joint opening structure of claim 11, wherein:"***
***[19.A] "a size difference between a top aperture and a bottom aperture of the first through hole is equal to or less than 30 nm; and"***

375. In my opinion, Costa teaches what this limitation requires.

376. In Costa, "[t]he lateral dimensions (e.g., a diameter) of the first-tier openings (149, 119) can be from about 20 nm to 200 nm at an upper portion of each first-tier opening (149, 119), and can be about 10 nm to 150 nm at a lower portion of each first-tier opening (149, 119)." Costa, [0139].

377. In other words, a POSITA would have recognized not only that there is a size difference between the top and bottom "aperture" of first-tier memory opening 149 in Costa, but that this side difference can be less than or equal to 30 nm as the claim requires.

378. This size difference is the necessary result of the etching process used to create the opening: more etching will occur at the top of the hole while less etching will occur at the hole's bottom resulting in a tapered structure.

379. Again, the range of opening diameters contemplated by Costa correspond with and teach the claimed range here. For instance, if the opening has a diameter of 20 nm at its top and 10 nm at its bottom, there would only be a 10 nm difference in diameter from top to bottom.

380. Not only is this consistent with what Costa actually discloses: Costa depicts only minimal taper (and thus minimal diameter difference from the opening top to bottom), a POSITA would have considered it obvious to etch in a way that minimizes (as opposed to maximizes) the amount of taper from top to bottom of the

opening naturally leading to a "size difference" that is well within the range of the claim here.

***[19.B] "a size difference between a top aperture and a bottom aperture of the second through hole is equal to or less than 30 nm."***

381. In my opinion, Costa also teaches what this limitation requires.

382. According to Costa, the second through hole employs the same lateral dimensions as the first through hole. Costa, [0194].

383. Because of this, in my opinion a POSITA would have understood that for the same reasons I just explained for limitation [19.A] a size difference between the top and bottom "aperture" of second-tier memory opening 149 would also obviously be less than or equal to 30 nm.

### C. *Ground 1 (IPR2025-00294)*: Dependent Claims 6 and 7 Are Obvious Over Costa in View of Liu

384. In my opinion, a POSITA would have considered both Costa and Liu to be within the scope of the prior art and highly relevant to the patentability of the '291 patent's claims.

385. In my opinion, when viewed and considered in light of the knowledge of a POSITA, Costa and Liu render claims 6 and 7 of the '291 patent obvious.

#### 1. Motivation to Combine

386. In my opinion, a POSITA would have been motivated to follow Liu's teachings and form a groove in Costa's insulating connection layer when forming third channel structure (173).

387. As I explain above, Liu teaches multi-tiered memory designed to facilitate "[a]lignment between memory openings through multiple tier structures [by] employing a temporary landing pad" with "a greater area than the horizontal cross-section[]" of the first-tier memory opening. Liu, Abstract, Title, [0002].

388. To do so, Liu deposits insulating layer 121A, boosting layer 1801, and insulating layer 121B over the first memory stack and subsequently creates a groove over the lower-level memory holes by an etching process. Liu, [0173].

389. A POSITA, in my opinion, would have recognized that utilizing Liu's groove to widen an insulating connection layer was a known technique in the art that was applicable to and usable with Costa's third channel structure.

390. A POSITA would have recognized that use of Liu's etch would have created a recess for Costa's third channel structure, and electrically coupled the third and second channel structures.

391. As a result, Liu's conductive plug (and the etching process that allows for this plug) serves the same purpose as Costa's insulating connection layer 172 and third channel structure thereon. Thus, a POSITA would have considered it a known, viable design option suitable for use with Costa.

392. Next, a POSITA would have been motivated to employ Liu's design and process.

393. Like Costa, Liu relates to a multi-tier structure. Liu, Abstract. Liu explains that such multi-tier structures often encounter difficulties when aligning the structures. This is a problem that Liu specifically addresses. *Id.*

394. Costa similarly seeks to address alignment issues: "Some of the challenges for fabricating a multi-tier memory stack structure include formation of memory openings having high aspect ratios and alleviation of effects of misalignment of tier-level memory openings formed in different tier structures. Thus, methods are desired for providing a reliable connection between vertically neighboring memory stack structures." Costa, [0003].

395. Because Costa teaches that it is often challenging to align memory openings, a POSITA would have been highly motivated to employ Liu's teachings with Costa. Doing so would have improved Costa by reducing the possibility of encountering alignment problems.

396. Costa also explains that it is desirable to reduce the height of its memory device: "Referring to FIG. 22A, an alternate embodiment of the third exemplary structure after formation of the second memory opening fill structures 77, which is derived from the third exemplary structure by reducing the thicknesses of each joint-level doped semiconductor portions 173, each single annular dielectric spacer 174, and the joint-level spacer material layer 175, for example, to a range from 20 nm to

150 nm, although lesser and greater thicknesses can also be employed." Costa, [0281].

397. A POSITA would have recognized that reduced device height produces numerous benefits. For example, it can reduce the amount of time needed to etch through the stack when forming through holes (as etching time is a function of, among other things, the height of the stack).

398. Again, this reduction can be seen by comparing Figures 21G and 22A (an intermediate layer in Figure 22A has reduced thickness resulting in an overall reduction of device height):

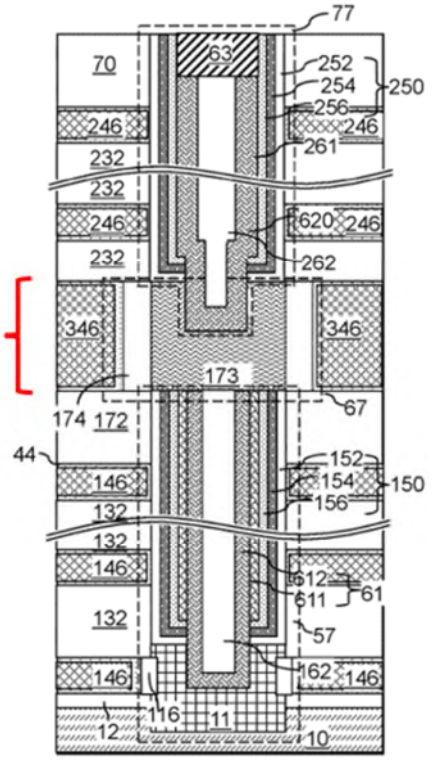


FIG. 21G

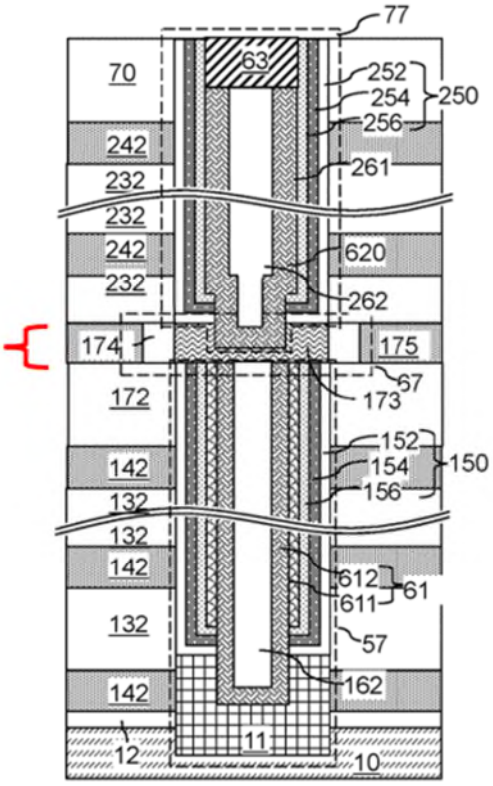


FIG. 22A

Costa, Figs. 21G (annotated), 22A (annotated).

399. A POSITA would have recognized that applying Liu's teachings to Costa furthers this goal. By forming a groove directly in insulating connection layer 172 of Costa (as Liu teaches), additional layers can be eliminated resulting in a further reduction in device height as shown below:

Original

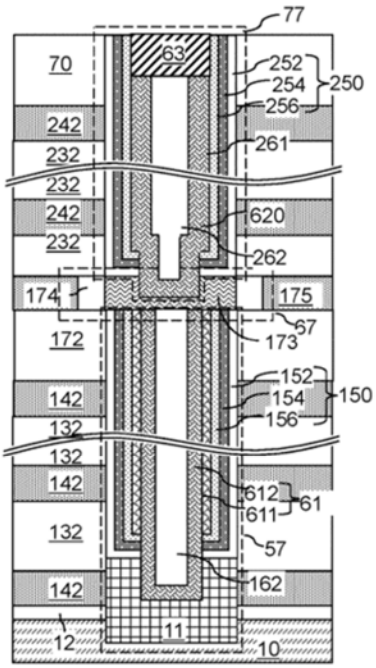



FIG. 22A

Modified

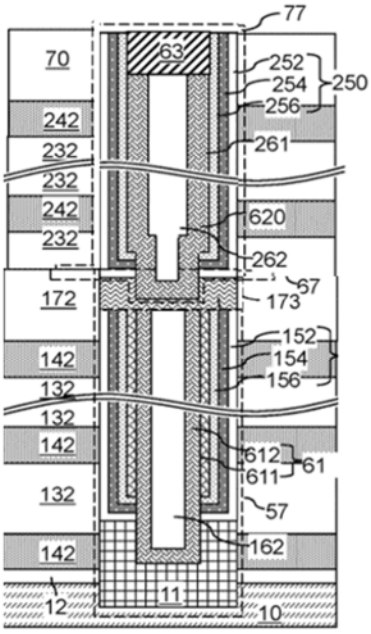



FIG. 22A

Costa, Fig. 22A (original), 22A (modified).

400. A POSITA also would have known that increasing the contact area decreases the contact resistance. *See, e.g.*, Ex. 1018 (Stavitski), 1 ("the contact resistance depends on the contact area[]"); Ex. 1019 (Fasoli), 10 ("small contact area tends to give rise to high contact resistance.").

401. Costa already designs its device with this in mind. As shown in Fig. 21F below, Costa etches portions of first channel structure 11 and third channel structure 173 to expose a larger portion of the channel sidewalls. Then, it deposits the second channel structure 162 and fourth channel structure 620 within this etched portion. This has the effect of increasing the contact area between these structures.

402. But, as shown, Costa did not employ a similar design in dielectric core 162:

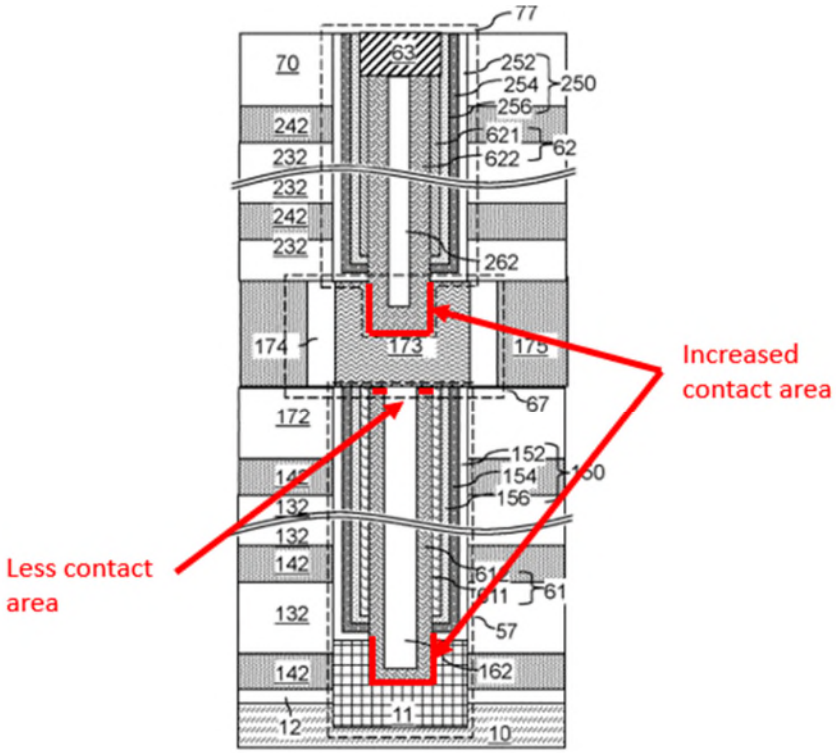



FIG. 21F

Costa, Fig. 21F (annotated).

403. In my opinion, a POSITA would have recognized that forming a recess into the insulating connection layer would allow the dielectric core 162 to be

recessed to a lower level then second channel structure 162, creating the same additional contact area as Costa has done above and below that interface.

404. This, in my opinion, would have further motivated application of Liu's teachings. A POSITA would have recognized that forming Costa's device this way would have improved the device by decreasing contact resistance.

405. A POSITA would have also understood that forming portion 173 in a groove of layer 172 would further Costa's goal of attaining alignment between structures. Costa, [0191]. Liu teaches forming a groove that is wider than the channel hole (see claim [6.B]). Costa is not a self-aligned process, because no structure naturally aligns the third channel structure (or the first and second channel through holes). Accordingly, natural misalignment results from process variations. Ex. 1021 , 2:60-3:6 (noting process variation issues in non self-aligned processes). Thus, Liu's approach addresses process variations that result in misalignment, because the groove can be wider than the channel hole. This simply involves an etch that was wider than the channel hole. This ensures electrical coupling between upper and lower channel structures, increasing yield. Ex. 1023, [0086].

406. In my opinion, a POSITA would also have had a reasonable expectation of success.

407. As I have explained, it was well known in the art that an upper structure in a memory device could be recessed into a lower structure. Moreover, it was also

known that such a recess could be readily achieved by masking and anisotropic etching. These are techniques that Costa already discloses.

408. Moreover, as shown above, Costa already discloses recessing layers, such as layer 70, for purposes of improving contacts resistance. Thus, a POSITA would have considered application of Liu to be nothing more than extension of Costa's existing teachings.

### 2. Claim 6

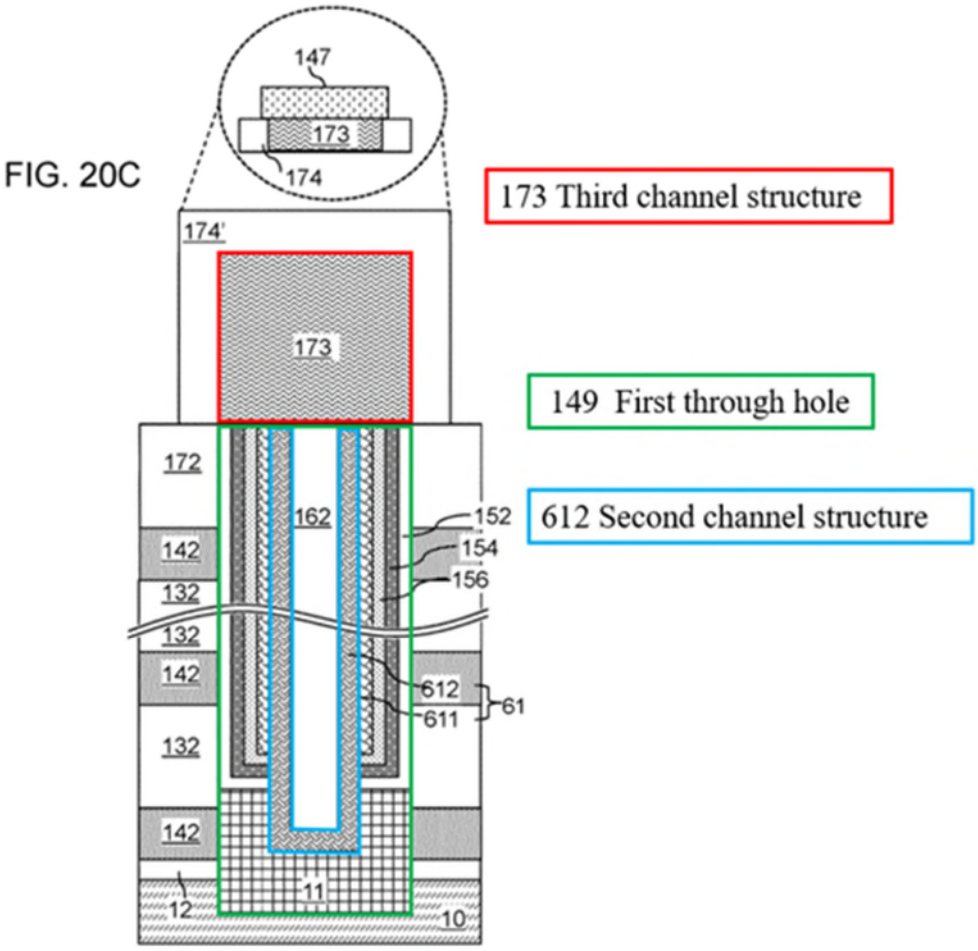
***[6.PRE] "The method of claim 1, wherein forming the third channel structure comprises:" [6.A] "etching the first insulating connection layer to form a first groove, wherein a projection of the first groove on the substrate covers the projection of the first through hole on the substrate;"***

409. In my opinion, this is obvious in view of Costa and Liu.

410. As I have explained, Costa teaches a first insulating connection layer (*i.e.*, first-tier insulating cap layer 172) and a third channel structure (*i.e.*, joint-level doped semiconductor portion 173) on the first insulating connection layer.



**Micron Ex. 1003, p. 146**
**Micron v. YMTC**
**IPR2025-00244**




Costa, Fig. 20C (annotated).

411. In my opinion, and for the reasons I explained above, a POSITA would have been motivated to etch a groove in Costa's first insulating connection layer 172 (effectively widening the aperture in which to form 173) for connecting the third channel structure 173 and the second channel structure 612.

412. Again, this would have both reduced device height and decreased contact resistance (consistent with both Liu's and Costa's goal).

413. Moreover, forming the third channel structure (173) with a wider aperture would also ensuring alignment between vertically neighboring channels. Again, this is one of Costa's design goals. Costa, [0003]. It is also the point of Liu's disclosure. *See* Liu, Abstract.

414. As I have explained, in Liu, a first insulating connection layer (insulating layer 121B, 1801, and insulating layer 121A) is etched to form a first groove (shown in annotated Fig. 18E below), wherein a projection of the first groove on the substrate covers the projection (also shown in annotated Fig. 18E below) of the first through hole (i.e. holes filled with 1/7/9/11) on the substrate (substrate 100).

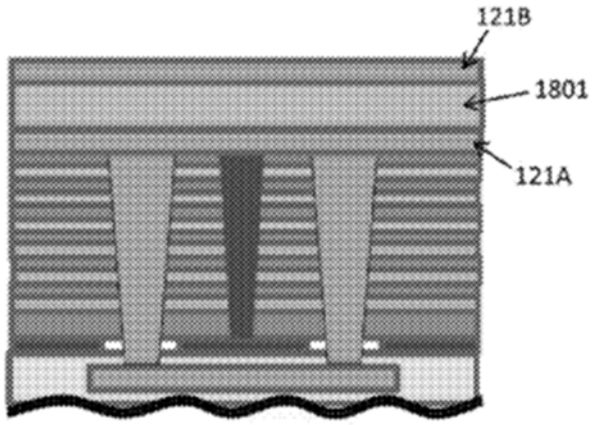
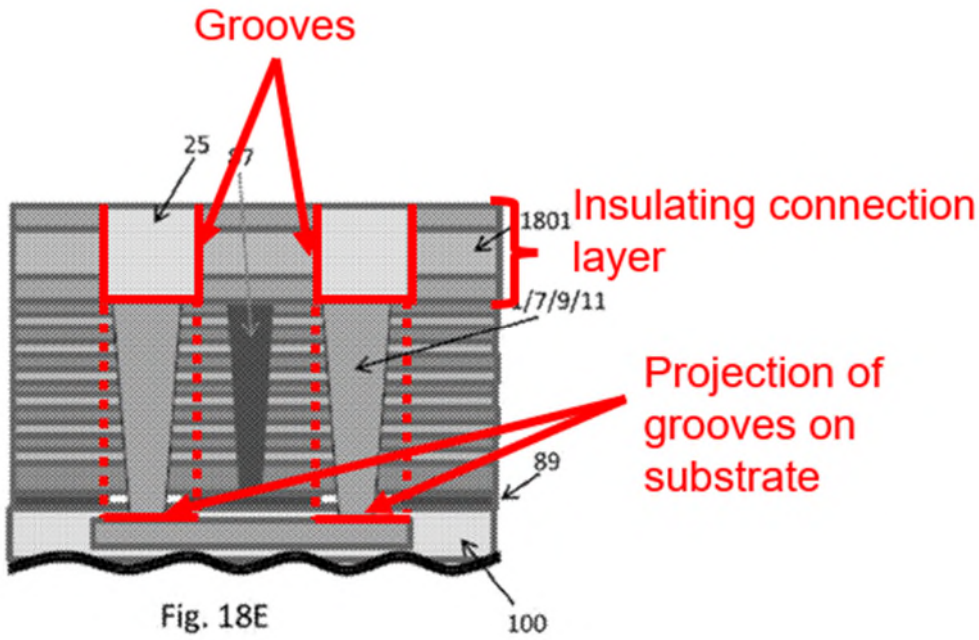



Fig. 18D




Liu, Figs. 18D, 18E (annotated).

415. To achieve this structure, Liu deposits the insulating layer 121A, then boosting layer 1801, and then insulating layer 121B. Liu, [0173].

416. Then, Liu creates grooves over the lower-level memory holes by an etching process: "[a]s illustrated in FIG. 18E, a mask, such as a photoresist mask, may be applied to the surface of the second insulating layer 121B and patterned. Portions of the second insulating layer 121B, the current boosting layer 1801 and the first insulating layer 121A located over the memory holes may be removed by etching." Liu, [0173].

417. A POSITA would have recognized that in Costa, both first insulating connection layer 172 and the dielectric filler 162 can be made out of a silicon oxide.

Costa [0134] (layer 172 can be silicon oxide), [0158]-[0159] (layer 162L can be silicon oxide).

418. A POSITA would further recognize that Layer 142 underlying layer 172 can be silicon nitride. Costa [0181].

419. Because layer 172 is made from silicon oxide insulating material and underlying layer 142 is made from a different silicon nitride sacrificial material, a groove in layer 172 would be created using an etch preferential to silicon oxide with layer 142 employed as an etch stop.

420. As a result, just as in Liu, when a groove is formed in Costa, a wider opening will be etched through layer 172. The etch will stop when it penetrates the underlying layer, i.e., silicon nitride layer 142.

421. This modification of Costa in view of Liu is shown in the below demonstrative (which was created using Costa's embodiment that attempts to shorten the stack height):

Original

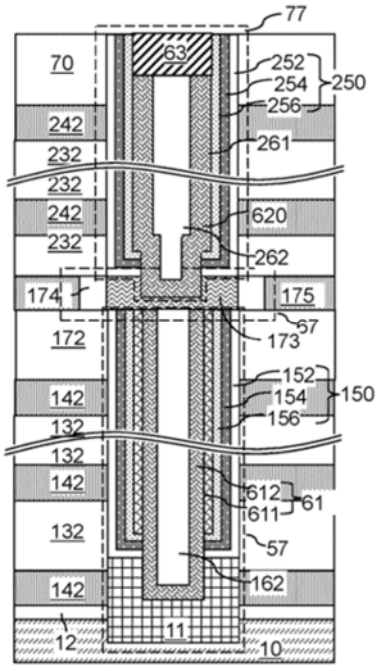



FIG. 22A

Modified

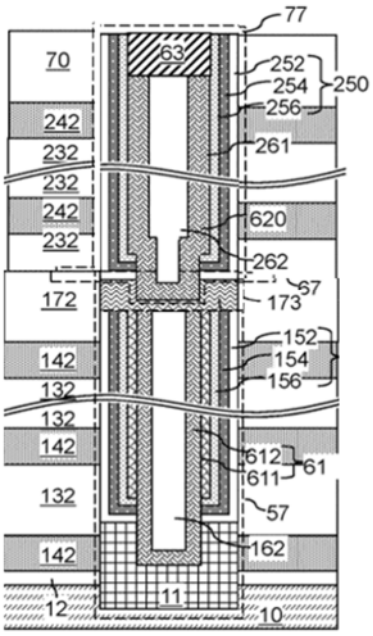



FIG. 22A

Costa, Fig. 22A (original), Fig. 22A (modified).

***[6.B] "forming a third channel layer in the first groove, wherein the third channel layer is in contact with the second channel structure; and"***

422. This, in my opinion, is rendered obvious by the combination of Costa and Liu.

423. In the combination, a third channel layer (173) is formed in the first groove. This third channel layer (173) is in contact with the second channel structure (612) as shown in modified version of Fig. 22A above.

***[6.C] "planarizing the top surfaces of the first insulating connection layer and the third channel layer to form the third channel structure."***

424. This, in my opinion, is obvious in view of the combination of Costa and Liu.

425. In my opinion, a POSITA would have considered it obvious to planarize the top surfaces of the first insulating connection layer and third channel structure.

426. When the '291 patent was filed, it was well known that the typical deposition of a plug interface requires planarizing the top surface because the deposition results in material above the target height.

427. Showing this, Costa explains that "[e]xcess portions of the deposited semiconductor material can be removed from above the top surface of the insulating cap layer 70, for example, by chemical mechanical planarization (CMP)." Costa, [0212].

428. Similarly, Liu explains that "The landing pad 55 formation may comprise epitaxially growing a 'mushroom head' shaped overgrown silicon 56 on exposed portions 1L of the channels 1. This silicon overgrowth 56 is then covered by an insulating gap fill layer (e.g., silicon oxide or nitride). The silicon mushroom head 56 and the gap fill layer are then planarized (e.g., by CMP) to form planar landing pads 55 on each pillar 1L." Liu, [0100].

429. Yet another reference to Lee discloses "[a]n upper portion of the pad layer may be planarized until the top surface of the uppermost insulating interlayer 102 j is exposed to obtain the pad 150. In example embodiments, the pad layer may be formed using polysilicon or doped polysilicon. In one example embodiment, a preliminary pad layer may be formed using amorphous silicon, and then a crystallization process may be performed thereon to form the pad layer. The planarization process may include a CMP process." Lee, [0094].

430. And still another reference to Lee 548 discloses "[u]pper portions of the first insulation layer patterns 148, the oxide layer 141, the charge storage layer 142, the tunnel insulation layer 144 and the channel pattern 146 in each channel hole 130 may be removed to form a recess and a pillar structure in each channel hole 130. A polysilicon layer may be formed to fill the recesses, and an upper portion of the polysilicon layer may be planarized until a top surface of the insulating interlayer 110 may be exposed to form a plurality of pads 150 on the pillar structures, respectively." Ex. 1020, [0100].

431. Because planarization steps were routinely employed after the deposition of a plug (indeed, such steps were taken after the formation of many types of structures), a POSITA would have considered it obvious to employ a step after forming the plug of Liu and Costa. Doing so would ensure that layers located above

the plug are properly formed and not misaligned due to the presence of unwanted, non-planar material below.

### 3. Claim 7

***[7.PRE] "The method of claim 1, wherein forming the third channel structure comprises:" [7.A] "etching the first insulating connection layer and at least a portion of the top nitride layer of the first stacked layer to form a first groove, wherein a projection of the first groove on the substrate covers the projection of the first through hole on the substrate;"***

432. This, in my opinion, is rendered obvious by the combination of Liu and Costa.

433. This Limitation [7.A] is substantively identical to limitation [6.A] discussed above, except that the etching requires "etching the first insulating connection layer and at least a portion of the top nitride layer of the first stacked layer to form a first groove."

434. As discussed above, etching a groove directly on layer 172 would remove portions of the silicon nitride layer—albeit small portions—as part of the etch that stops on layer 142.

***[7.B] "forming the third channel structure in the first groove, wherein the third channel structure is in contact with the second channel structure; and"***

435. This limitation is the same as [6.B] and thus is taught by Costa for the same reasons I describe above for that limitation.

***[7.C] "planarizing the top surfaces of the first insulating connection layer and the third channel structure."***

436. This limitation is the same as [6.C] and thus is taught by Costa for the same reasons I describe above for that limitation.

### D. *Ground 2 (IPR2025-00294):* Dependent Claim 10 Is Obvious Over Costa in View of Lee

437. In my opinion, a POSITA would have considered both Costa and Lee to be within the scope of the prior art and highly relevant to the patentability of the '291 patent's claims.

438. In my opinion, when viewed and considered in light of the knowledge of a POSITA, Costa and Liu render claim 10 of the '291 patent obvious.

#### 1. Motivation to Combine

439. As explained in greater detail below, Lee teaches that the entire width of a through hole can be employed when forming a conductive pad at the top of that hole.

440. In my opinion, a POSITA would have been motivated to apply this teaching to Costa and utilize the entire width of the through hole when forming the fifth channel structure 63 of Costa for several reasons.

441. First, as shown by both Costa and Lee, it was known that a conductive drain at the top of a channel structure can fill either all (as taught by Lee) or part (as taught by Costa) of the hole containing that channel structure. A POSITA would

have considered use of a conductive drain that fills all of the channel structure to be a known, viable option and nothing more than a routine design choice.

442. Moreover, a POSITA would have recognized that Lee's etch creates a recess for Costa's conductive drain, and electrically couples the conductive drain to Costa's fourth channel structure in the same way Costa already teaches (albeit with increased physical extent such that it fills all instead of just part of the hole).

443. A POSITA also would have recognized that Lee's approach increases the width of the conductive drain. As a result, the conductive drain is wider.

444. Per Costa, the conductive drain serves as a connection point of a bit line. *E.g.*, Costa, [0233].

445. A POSITA would have recognized that Lee's approach provides a wider landing area for this bit line connection. This would increase manufacturability by increasing the margin around the connection area. It would also reduce the occurrence of manufacturing defects in the event the bit line interconnect inadvertently extends beyond the edges of a too small landing area. The same is true with respect to the bottom of the conductive drain. The conductive drain, on the bottom side, connects to the fourth channel structure. As I explain in my analysis under claim [1.F], Costa's process is not self-aligned. Thus, process variations lead to misalignment. Including margin ensure the conductive drain properly physically contacts the relevant structures, ensuring the correct electric

coupling. E.g., Ex. 1021, 2:60-3:6 (noting process variation issues in non self-aligned processes); Ex. 1022, 20-21; Ex. 1023, [0023], [0086]; Liu, [0058]; Ex. 1024, Fig. 2F, [0061]. The margin reduces the number of defective memory strings, i.e., if the conductive drain does not properly contact the underlying channel structure (fourth channel structure) and above interconnects (ultimately, the bit line), the memory string will be defective. Including this margin reduces defective memory strings and increases yield.

446. In my opinion, a POSITA would also have had a reasonable expectation of success in employing Lee's teachings.

447. Costa already employs a conductive drain. Lee simply increases the size of this structure such that it fills the entirety of the through hole in which it is contained. A POSITA would have recognized that this could be readily accomplished via a straight forward etching process.

448. Moreover, both Costa and Lee employ the same, routinely used etching step: an anisotropic etch. *E.g.*, Lee, [0093]-[0094] ("Referring to FIG. 8, upper portions of the dielectric layer structure 129, the channel 135 and the first filling layer pattern 145 may be partially removed to form a recess 147, and then a pad 150 capping the recess 147 may be formed. In example embodiments, an upper portion of the multi-stacked structure may be removed by an etch-back process to form the recess 147.")

449. Thus, a POSITA would have recognized that Costa's existing processes could readily be applied to carry out Lee's teachings.

### 2. Claim 10

***[10.PRE] "The method of claim 1, wherein forming the fifth channel structure comprises:" [10.A] "etching the second insulating connection layer to form a second groove, wherein a projection of the second groove on the substrate covers the projection of the second through hole on the substrate;"***

450. This, in my opinion, is rendered obvious by Costa and Lee.

451. Costa does not expressly disclose what this limitation requires. In Costa, a fifth channel structure 63 is deposited in a recess. Costa, [0212], [0260]. While Costa states that the dielectric core can be recessed (*id.*), Costa depicts recessing the dielectric core and the semiconductor layers 622 and 621:

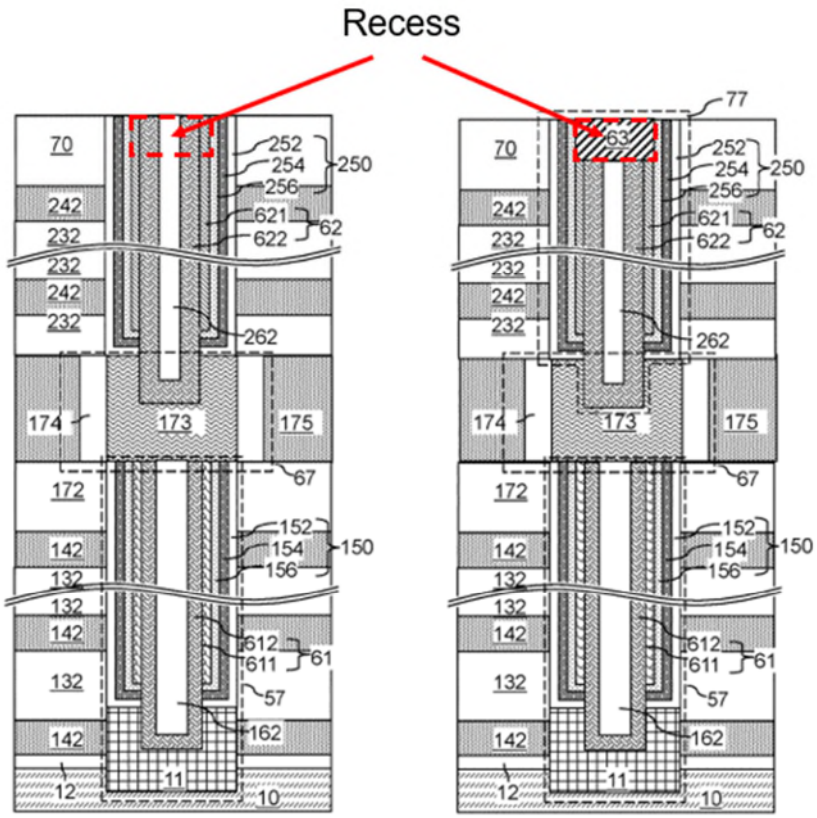


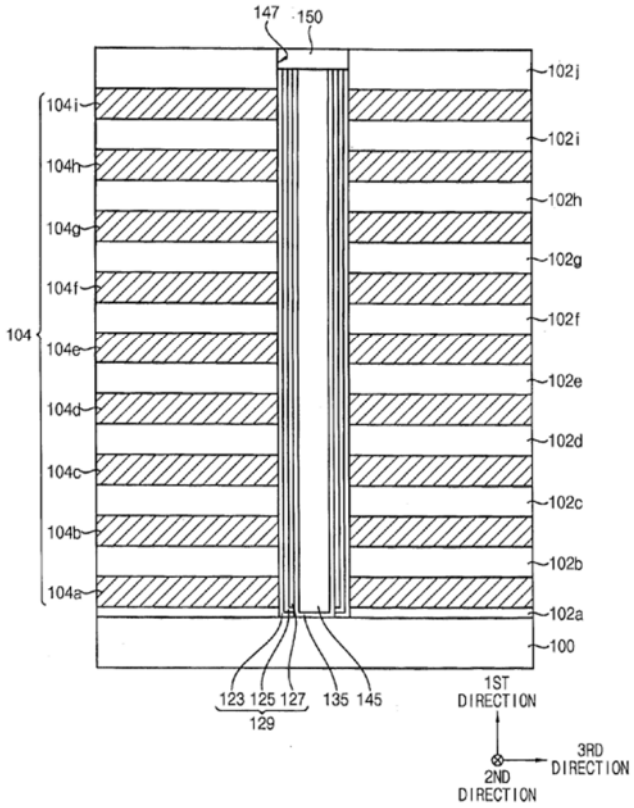

FIG. 21E FIG. 21F

*Id.*, Figs. 21E, F (annotated).

452. Because Costa contemplates recessing a variety of layers (some are discussed in the specification while others are shown in the figures), a POSITA would have understood that the exact width of the recess is not critical to Costa, but only that the recess enables the conductive drain to be formed under the top surface of the insulating layer 70. Put another way, Costa is open to and allows its conductive drain to have different physical extents.

453. Lee teaches an "etch-back process" to form the recess (i.e. groove) 147 that utilizes the entire width of the through hole and a recessed pad 150, e.g., of "doped polysilicon" (i.e. a fifth channel structure) that fills the groove. An example of pad 150 is shown in Figure 8 below.

FIG. 8




Lee, Fig. 8.

454. According to Lee, "upper portions of the dielectric layer structure 129, the channel 135 and the first filling layer pattern 145 may be partially removed to form a recess 147, and then a pad 150 capping the recess 147 may be formed. In



Micron Ex. 1003, p. 160
Micron v. YMTC
IPR2025-00244

example embodiments, an upper portion of the multi-stacked structure may be removed by an etch-back process to form the recess 147." Lee, [0093]-[0094].

455. As explained above, a POSITA would have been motivated to apply Lee's recess etch to form a second groove in Costa such that it removes layers 250, 62, and 262 (such that "a projection of the second groove on the substrate covers the projection of the second through hole on the substrate"). Again, this would have improved Costa by increasing the contact area for interconnection to the bit line.

456. Application of this second groove to Costa results in the following structure corresponding to this claim limitation:

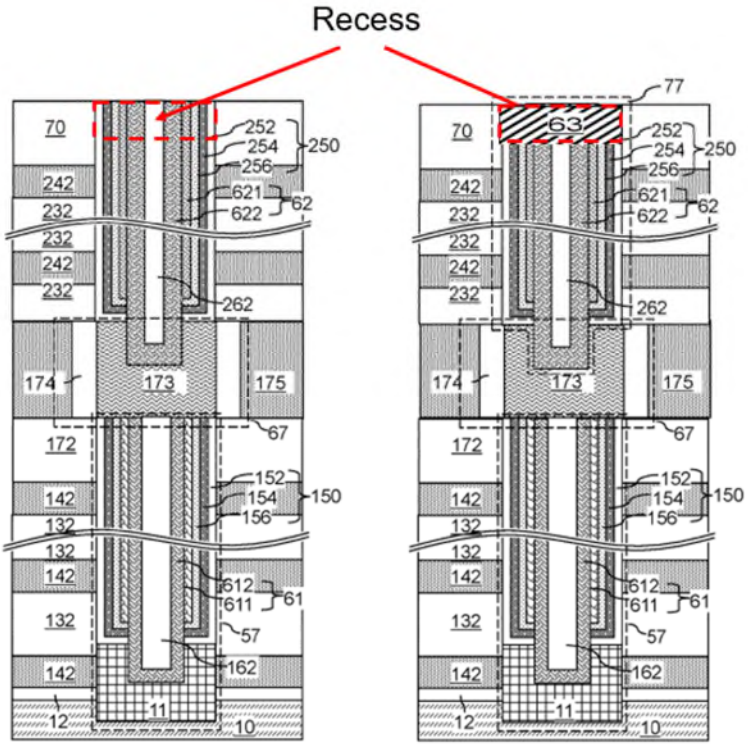



FIG. 21E FIG. 21F

Costa, Figs. 21E (annotated), 21F (annotated).

***[10.B] "forming a fifth channel layer in the second groove, wherein the fifth channel layer is in contact with the fourth channel structure; and"***

457. This, in my opinion, is obvious over Lee and Costa.

458. A POSITA would have considered it obvious—following Lee's teachings—to form the second groove through all the channel structure materials (*i.e.*, as wide as the entire second through hole), and then form the fifth channel layer therein.

459. Lee, for example, teaches "[a] pad layer sufficiently filling the recess 147 may be formed on the uppermost insulating interlayer 102j." Lee, [0094].

460. Similarly, Costa teaches forming its drain region in the recess. Costa, [0260].

461. A POSITA would have understood that this is necessary: the conductive drain must electrically couple to the semiconductor layer 622 (and optional layer 621).

462. Application of this second groove to Costa (widened following Lee's teachings) followed deposition of the conductive drain results in the following structure corresponding to this claim limitation:

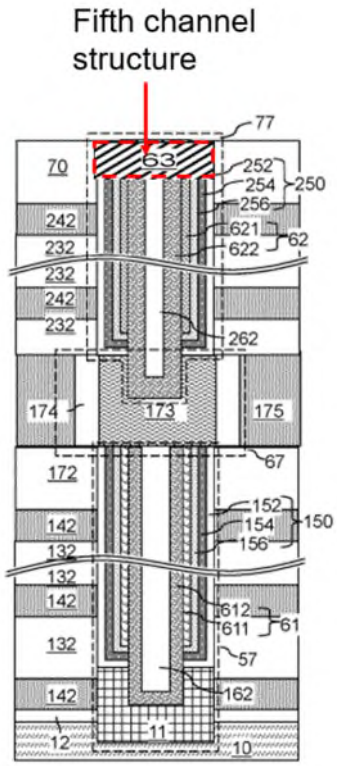



FIG. 21F

Costa, Figs. 21F (annotated).

***[10.C] "planarizing the top surfaces of the second insulating connection layer and the fifth channel layer to form the fifth channel structure."***

463. This, in my opinion, is obvious in view of Costa and Lee.

464. Again, Lee teaches forming the second groove through all of the channel structure materials (i.e., as wide as the entire second through hole). Both Costa and Lee then fill that groove with a conductive drain.

465. A POSITA also would have considered it obvious to planarize the top surfaces of the second insulating connection layer and fifth channel structure. It was well known that the typical deposition of a conductive drain requires than

planarizing the top surface because the deposition results in material above the target height.

466. For example, Lee explains that after "[a] pad layer sufficiently filling the recess 147 may be formed on the uppermost insulating interlayer 102j" then "[a]n upper portion of the pad layer may be planarized until the top surface of the uppermost insulating interlayer 102j is exposed to obtain the pad 150…. The planarization process may include a CMP process." Lee, [0093]-[0094].

467. Similarly, Costa explains that "[e]xcess portions of the deposited semiconductor material can be removed from above the top surface of the insulating cap layer 70, for example, by chemical mechanical planarization (CMP)." Costa, [0212].

468. Not only was planarization routinely performed after the deposition of material, but a POSITA would have recognized that planarization would still be necessary to ensure that the conductive drain is at the same level as insulating layer 70 and remove excess polysilicon above insulating layer 70 (on the fifth channel structure and insulating layer 70) because, for example, subsequently overlaid metal layers require planar surfaces for deposition.



**Micron Ex. 1003, p. 164**
**Micron v. YMTC**
**IPR2025-00244**

### E. *Ground 3 (IPR2025-00294)*: Independent Claim 20 Is Obvious Over Costa in View of Toyama

469. In my opinion, a POSITA would have considered both Costa and Toyama to be within the scope of the prior art and highly relevant to the patentability of the ’291 patent’s claims.

470. In my opinion, when viewed and considered in light of the knowledge of a POSITA, Costa and Toyama render claim 20 of the ’291 patent obvious.

#### 1. Motivation to Combine

471. As noted above, Toyama (Ex. 1008) teaches a multi-tiered three-dimensional memory device that includes “through-memory-level via regions 600” that contain “through-memory-level via structures 676” (*i.e.*, through array contacts) and “insulating liners 674.” Toyama, [0333], [0340]-[0342].

472. In my opinion, a POSITA would have been motivated to combine Costa with Toyama’s through-array contact teachings for several reasons.

473. As an initial matter, the focus of Costa’s disclosure is on its memory’s memory cell array and staircase region. It only mentions peripheral devices once. Costa, [0124].

474. A POSITA would have recognized, however, that memory devices require supporting logic to function. These logic devices (which are typically formed from CMOS devices) control access to support memory operations and are located outside of the memory array and staircase region.



Micron Ex. 1003, p. 165
Micron v. YMTC
IPR2025-00244

475. Toyama depicts one well-known architecture—known as CMOS under the array—the that provides for CMOS devices under the memory array. Figure 49 from Toyama, which is reproduced in annotated version below, shows the location of the CMOS logic:

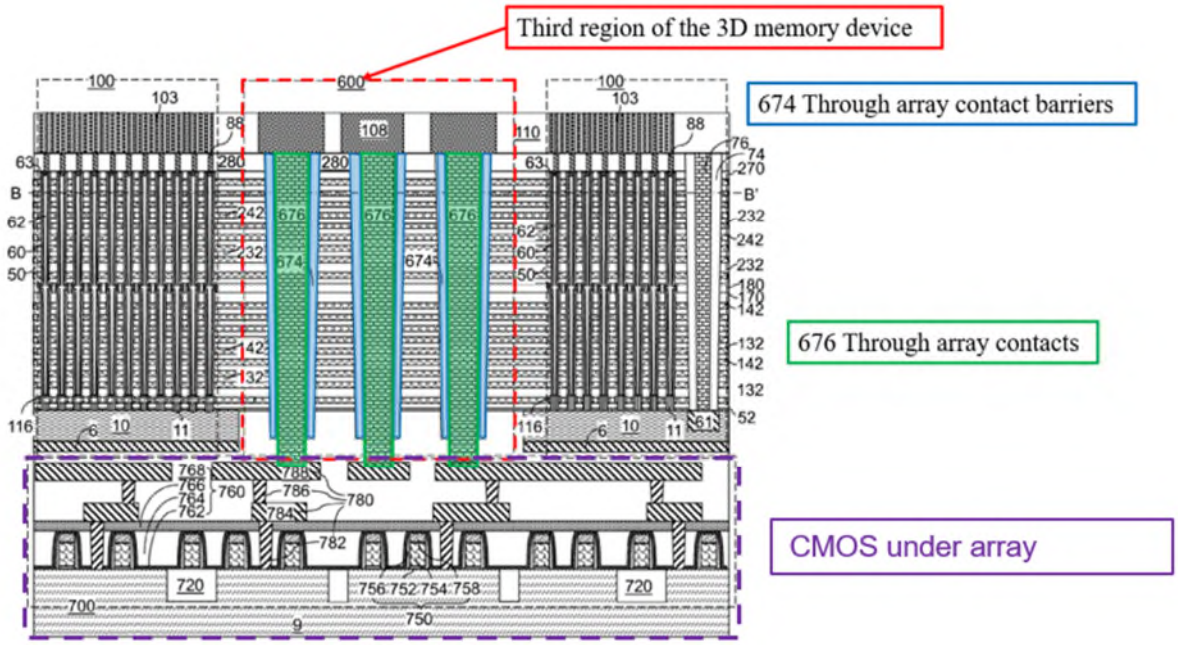



FIG. 49

Toyama (annotated), Fig. 49.

476. Toyama explains that placing the required controlling logic outside of the memory stack, *i.e.*, on the device's peripheral area, unnecessarily consumes space and increases the device's physical footprint: "As three-dimensional memory devices scale to smaller device dimensions, the device area for peripheral devices can take up a significant portion of the total chip area. Thus, a method of providing

various peripheral devices, such as word line driver circuits, without significantly increasing the total chip size is desired." Toyama, [0003].

477. To avoid consuming space in this way, Toyama teaches a "through-memory-level via region comprises through-memory-level via structures that vertically extend at least from a first horizontal plane including a topmost surface of the memory-level assembly to a second horizontal plane including a bottommost surface of the memory-level assembly." Toyama, [0005].

478. As shown in the annotated version of Figure 49A above, these through-memory level via structures (676) are contacts (with insulating spacers) that extend through the stack, thereby enabling the placement of CMOS under the array. The CMOS electrically interconnects with the remainder of the memory array. This accomplishes Toyama's goal of reducing the footprint of the memory device.

479. A POSITA would have been motivated to structure Costa's device in a similar fashion. By placing the required controlling CMOS circuitry under Costa's array rather than at its periphery, the physical footprint of Costa's device could be reduced. This would in turn result in a smaller, more compact memory device. Alternatively, there would be additional space to increase the size of the memory array (as less space would be consumed peripheral circuitry).



**Micron Ex. 1003, p. 167**
**Micron v. YMTC**
**IPR2025-00244**

480. Next, a POSITA would have recognized that forming the required memory controlling logic under the memory array provides another benefit: it brings that logic circuitry closer to the array.

481. Toyama explains that this is beneficial because it allows for a more "efficient power distribution network in the array of memory stack structures [that] can increase performance of three-dimensional memory devices." Toyama, [0003].

482. Further, a POSITA would also have understood that positioning the controlling logic closer to the array decreases the distance between—and the overall extent of—various metal layer connections. For instance, the total conductive path from the CMOS logic to upper interconnects and back into the memory array would be shortened. This would in turn reduce line resistance, improve speed, and reduce the possibility of interference, noise, or spurious signals. It would also position voltage drivers closer to, for instance, the wordlines reducing power needs.

483. In my opinion, a POSITA would also have had a reasonable expectation of success in implementing Toyama's CMOS under-array logic with through-array contacts (and the corresponding barrier layers).

484. To begin, the positioning of CMOS logic under the array was well-known and routinely done in the prior art. *See, e.g.*, Ex. 1013, 175 ("Because the entire stack is built above the silicon, the area under the array is used for circuits, thus saving silicon area and improving bit density. There are 4 metal layers: 2 at the



**Micron Ex. 1003, p. 168**
**Micron v. YMTC**
**IPR2025-00244**

bottom for connecting CMOS circuits underneath the array, and two at the top, one for bitline and one for power and global interconnects, respectively."), 180 (citing "K. Parat, C. Dennison, A floating gate based 3D NAND technology with CMOS under array in Conference on International Electron Devices Meeting (IEDM), San Francisco (USA), Dec 2015."

485. Given the routine use of this type of structure, a POSITA would have had every reason to believe that Costa would have been able to successfully employ it.

486. Next, a POSITA would have recognized that Costa already teaches etching through its stack for various purposes. For example, it forms memory structures and staircase support pillars contacts. *E.g.*, Costa, Fig. 3B. Costa also references creation of a contact, along with a barrier layer, through its stack. *Id.*, [0229]-[0231], Fig. 16B (insulating spacer 74 and contact via structure 76).

487. Given this, a POSITA would have understood that application of Toyama amounts to nothing more than employing a process Costa already uses—etching through the stack—to form a structure much like that already present in Costa—a contact that proceeds through the memory array. Moreover, etching and conformal deposition were textbook material.

488. Further, as shown by Toyama, a memory device formed as a multi-deck stack is able to successfully employ CMOS logic located under the array just like

any other type of memory device. Toyama, Fig. 49, [0016] (first tier), [0055] (second tier).

### 2. Claim 20:

***[20.PRE] "A joint opening structure of a three-dimensional (3D) memory device, comprising:"***

489. To the extent limiting, this preamble language is substantively identical to [1.PRE] and thus is taught by Costa for the same reasons I describe above when discussing claim 1.

***[20.A] "a first stacked layer disposed overlaying a substrate;"***

490. This limitation is present in and thus is taught by Costa for the same reasons I describe above for limitation [1.A].

***[20.B] "a first insulating connection layer disposed on the first stacked layer;"***

491. This limitation is present in and thus is taught by Costa for the same reasons I describe above for limitation [1.A].

***[20.C] "a second stacked layer disposed on the first insulating connection layer;"***

492. This limitation is present in and thus is taught by Costa for the same reasons I describe above for limitation [1.G].

***[20.D] "a second insulating connection layer disposed on the second stacked layer;"***

493. This limitation is present in and thus is taught by Costa for the same reasons I describe above for limitation [1.G].

***[20.E] "a plurality of channel holes in a first region of the 3D memory device;"***

494. This, in my opinion, is taught by Costa.

495. Costa's device includes channel holes in a first region (memory array region 100) of the 3D memory device. Costa, [0124], Figs. 3A-B, 10A-B.

496. As I explained in greater detail above when discussing limitations [1.A]-[1.K], Costa discloses forming a plurality of first-tier memory openings 149 and second-tier memory openings 249 in memory array region 100, which are subsequently filled to form an active memory channel. *See* Costa, [0135], [0161], [0190].

***[20.F] "a plurality of staircase structure dummy holes in a second region of the 3D memory device; and"***

497. This, in my opinion, is taught by Costa.

498. Per Costa, its device includes a plurality of staircase structure dummy holes in a second region (contact region 200) of the 3D memory device. Costa, [0124], Figs. 3A-B, 10A-B (staircase region 200).

499. More particularly, Costa forms first-tier support openings 119 and second-tier support openings 219 in contact region 200. Costa, [0137], [0190], Figs. 3A-B, 10A-B. Support openings 119 and 219 are subsequently filled to form support fill structures 17 and 27. *Id.*, [0160], [0177].

500. Costa explains that these support members support the memory stack during the gate replacement process. Costa, [0226].

501. The holes therefore are "dummy" holes because the structures are dummy structures, that is, they do not form memory cells and instead are present

merely for purposes of providing stack support during the gate replacement process. are merely support members. The dummy structures in the ’291 patent perform the same function. Ex. 1001, 26:2-4 (“The plurality of staircase structure dummy holes in the second region can have a supporting function of the staircase structure.”).

***[20.G] “a plurality of through array contact barriers in a third region of the 3D memory device;”***

502. This, in my opinion, is rendered obvious by Costa and Toyama.

503. Costa does not discuss through array contacts. Again, as I note above, it mentions its peripheral circuitry only once.

504. Toyama, however, teaches a memory device with a plurality of through array contact barriers (“insulating liners 674”) in a third region of the 3D memory device (“through-memory-level via regions 600”), as shown in Figure 49 below. Toyama, [0333], Figs. 45A, 48A, 49.

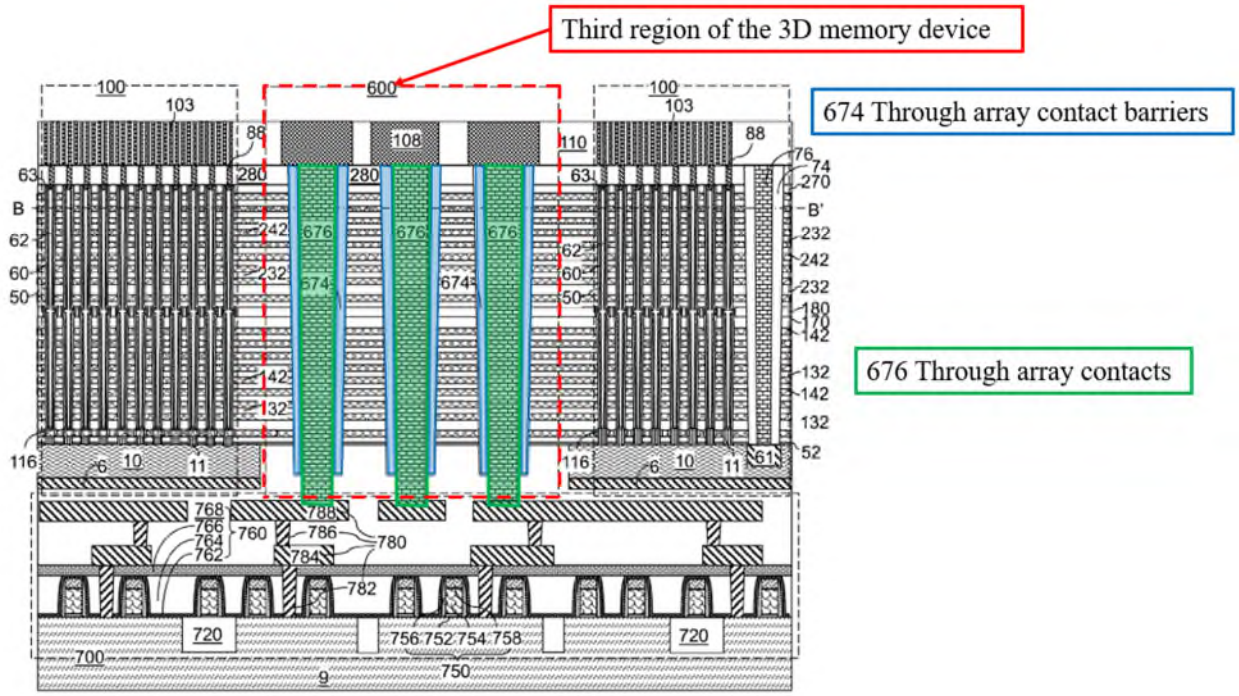



FIG. 49

*Id.*, Fig. 49 (annotated).

505. Toyama forms "insulating liners 674" by depositing "a conformal insulating material layer" in "through-memory-level openings 679." Toyama, [0338]-[0340], [0233] ("[a]n insulating spacer 74 including a dielectric material"), [0381] ("insulating liner 674 having a same material composition and a same thickness as the insulating spacer 74").

506. Although paragraph 338 of Toyama refers to "through-memory-level openings 689," that appears to be a typographical error. All relevant figures (*e.g.*, Figs. 47A-B to 49) and other textual descriptions refer to the elements as "through-memory-level openings 679," *see, e.g.*, Toyama, [0339]-[0341]. Thus, a POSITA would have understood the openings to correspond to item 679, not 689.

507. According to Toyama, the remaining portion of through-memory-level opening 679 is filled with "at least one conductive material" to form "through-memory-level via structure 676." Toyama, [0341]-[0342].

508. In my opinion, a POSITA would have understood these conductive through-memory-level via structures 676 to constitute through array contacts: they pass through the array portion of Toyama's memory and are meant to electrically interconnect the CMOS circuitry to the array.

509. Further, a POSITA also would have recognized that the insulating liners 674 form dielectric barriers between the through array contacts in a third region of the 3D memory device: the barriers allow the contacts to pass through the array without shorting out the array's various conductive layers.

***[20.H] "wherein each of the plurality of channel holes includes: a first through hole penetrating the first stacked layer and the first insulating connection layer,"***

510. This limitation is present in and thus is taught by Costa for the same reasons I describe above for limitation [1.B].

***[20.I] "a first channel structure disposed at the bottom of the first through hole and overlaying the substrate,"***

511. This limitation is substantively the same as limitation [1.C] discussed above. The only difference is that it uses the phrase "disposed at the bottom of the first through hole" instead of "on." As a result, in my opinion it is taught by Costa for the same reasons I explained for limitation [1.C].

***[20.J] "a first functional layer disposed on the sidewall of the first through hole,"***

512. This limitation is substantively the same as limitation [1.D] discussed above. The only difference is that it uses the phrase "disposed on" instead of "on." As a result, in my opinion it is taught by Costa for the same reasons I explained for limitation [1.D].

***[20.K] "a second channel structure in contact with the first channel structure disposed on the sidewall of the first functional layer,"***

513. This limitation is present in and thus is taught by Costa for the same reasons I describe above for limitation [1.E].

***[20.L] "a third channel structure in contact with the second channel structure disposed over the first through hole, wherein a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate,"***

514. This limitation is substantively the same as limitation [1.F] discussed above. The only difference is that it uses the phrase "disposed over" instead of "form[ed] … above." As a result, in my opinion it is taught by Costa for the same reasons I explained for limitation [1.F].

***[20.M] "a second through hole penetrating the second stacked layer and the second insulating connection layer, wherein a projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate,"***

515. This limitation is present in and thus is taught by Costa for the same reasons I describe above for limitation [1.H].

***[20.N] "a second functional layer disposed on the sidewall of the second through hole,"***

516. This limitation is substantively the same as limitation [1.I] discussed above. The only difference is that it uses the phrase "disposed on" instead of "on." As a result, in my opinion it is taught by Costa for the same reasons I explained for limitation [1.I].

***[20.O] "a fourth channel structure in contact with the third channel structure disposed on the sidewall of the second functional layer, and"***

517. This limitation is present in and thus is taught by Costa for the same reasons I describe above for limitation [1.J].

***[20.P] "a fifth channel structure in contact with the fourth channel structure disposed over the second through hole."***

518. This limitation is substantively the same as limitation [1.K] discussed above. The only difference is that it uses the phrase "disposed over" instead of "form[ed] … above." As a result, in my opinion it is taught by Costa for the same reasons I explained for limitation [1.K]

### F. Secondary Considerations of Non-Obviousness

519. Based on my review of the '291 patent's prosecution history, I note that no secondary considerations of non-obviousness were identified in connection with the patent's Claims.

520. I am not separately aware of any evidence of commercial success, skepticism, failure of others, industry praise, unexpected results, or the like. Instead, as discussed above, it is my opinion that the subject matter embraced by

the ’291patent’s claims was known in and obvious over the prior art. Moreover, it is also my opinion that the teachings of the prior art would have been expected to successfully function as or be usable with working 3D memory devices.



**Micron Ex. 1003, p. 177**
**Micron v. YMTC**
**IPR2025-00244**

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Date: December 13, 2024

Location: Austin, Texas

Signature: Sanjay Banerjee

Dr. Sanjay K. Banerjee



Micron Ex. 1003, p. 178
Micron v. YMTC
IPR2025-00244