



Review

Overview and status of bottom-up silicon nanowire electronics

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ARTICLE INFO

Available online 23 June 2012

Keywords:

Silicon nanowire
Bottom-up
Top-down
Synthesis
Doping
Electrical transport

ABSTRACT

This review summarises the recent advances in the field of silicon nanowire electronics from bottom-up assembled materials. The aim is to draw a comparison between bottom-up and top-down approaches, examining respective achievements and evaluating advantages and disadvantages of each methodology. Existing techniques for synthesis and doping are discussed to provide the framework in which practical electronic applications can be developed. Next, key device categories are reviewed, emphasising current challenges and proposed solutions. Finally, field perspectives are outlined.

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1. Introduction

The purpose of this paper is to convey a realistic view of the current status of research on bottom-up silicon nanowire (Si NW) electronics. The “bottom-up” class encompasses chemically synthesised nanostructures, assembled atom-by-atom from their fundamental components, as opposed to “top-down” approaches where materials in bulk form are shaped down to nanoscale via etching strategies. The turn of the millennium witnessed fast-growing interest towards bottom-up approaches for nanoelectronic applications, sparked by reports on relatively accessible methods for high yield production of self-assembled Si nanomaterials [1]. The discovery was particularly timely, because the techniques of choice for parallel top-down fabrication of the ubiquitous Si transistors were expected to fall short as characteristic device lengths hit the tens of nanometres scale. Envisaged limitations of top-down technology drove the search for alternative implementation approaches. Si NWs were seen as a more realistic solution than carbon nanotubes, at least in the short-term, because they avoided the tremendous paradigm shift required for changing the actual functional material. In principle, existing machinery, methods, and know-how could be readily applied to the novel Si structures.

The main motivation for pursuing bottom-up Si NW technology was essentially geometrical, residing in the 1D or quasi 1D morphology of these nanostructures. It has long been known that further improvement of transistor performance would be achieved by coupling the scaling of critical device dimensions with efficient gate control over charge flow. Under these conditions, low off-state currents and fast device response are obtained. Tight gate control is best realised in wrap-around (or all-around) geometries, i.e., in devices where the gate electrode surrounds the channel from all directions (see Fig. 3 for the FETs classification according to the number of gates). Thus, it was only natural for cylindrically-shaped nanostructures combining the advantages of small size and ideal geometry to be regarded as appealing building blocks for transistor assembly. However, while bottom-up strategies were being investigated, industrial top-down technologies were similarly being developed in the pursuit of further scaling so that, to date, fabrication of transistors with minimum features on the order of 20 nm became sufficiently reliable and cost-effective to meet industrial standards [2]. Serial top-down techniques such as electron beam lithography can be used to pattern even smaller features (down to few nanometres) but are not scalable, although they retain their usefulness for prototype studies. In comparison, bottom-up techniques can routinely produce nanostructures of extremely small size (with a remarkable record of 1 nm-diameter NWs [3]) yet questions remain on whether these methods will ever find practical application in nanoelectronics, properly addressing issues such as reproducibility, wide property distribution, and deterministic assembly. With further improvement of top-down methods within reach [2], bottom-up approaches towards Si nanodevice fabrication may not manage to retain their competitive edge for long.

This paper reviews the major achievements of bottom-up Si NW technology, with a critical eye on their near-future outlook. The first section outlines the most common synthesis techniques. The aim is to define the framework in which current NW based electronic is developing, describing the available tools for NW synthesis and discussing their relative advantages and limitations. With similar spirit, the following section deals with the methods for NW doping. In the third and main section several key device categories are introduced and discussed in comparison with their top-down counterpart.

2. Synthesis

2.1. Chemical vapour deposition (CVD)

CVD is a widely used technique for Si NW growth. The main reason of its popularity lies in the versatility: controlling a variety of parameters allows synthesis of NWs with broad range of morphologies and compositions. Different parameters include reaction time, temperature, pressure but also size of catalyst, substrate orientation, and, notably, gas mixture. CVD growth is carried out in a reactor where Si atoms are supplied by Si-rich gaseous sources such as silane (SiH_4) [4], disilane (Si_2H_6) [5], or silicon tetrachloride (SiCl_4) [6,7]. As temperature is raised, gas dissociation occurs at the surface of metal catalytic particles. These are prepared via thin film deposition and annealing or, alternatively, synthesised separately as individual colloids and dispersed on a supporting substrate. The particles act as catalyst and promote the unidirectional elongation (axial growth), their size roughly defining the diameter of the resulting NWs. Radial NW growth may occur when synthesis conditions favour surface adsorption over desorption, resulting in further deposition at the NW sidewalls and thus in the tapering or thickening of the NWs. Catalyst migration and droplet instabilities can also severely affect the growth and contribute in determining the NW length, shape, and sidewall profiles [8]. Additional material deposited on the sidewalls is often regarded as a growth by-product which can severely alter NW properties, especially in situations when dopants are introduced during growth (see Section 3). Yet, tapered NWs are best suited for specific applications including field-emission [9] and photovoltaics [10] and methods have been developed to control these overgrown layers [11]. As regards the axial growth, temperatures higher than the eutectic temperature (T_E) characteristic of the Si-metal system under consideration allow the formation of a liquid alloy. As more Si atoms are supplied to the droplet from the gas phase, supersaturation is obtained, whereupon Si precipitates, giving rise to epitaxial NW growth (as in, e.g., Fig. 2(a)). This process is referred to as the vapour-liquid-solid (VLS) mechanism and was first proposed in the 60s to explain the growth of micrometre-size Si whisker [12]. Au has historically been the metal of choice for VLS growth [13,14] but other catalysts have also been tested, including In [15], Sn [15], Al [16], and Ga [17]. The motivations behind the preferential choice of Au as catalyst for Si NW growth are better understood by looking at the Au–Si phase diagram in Fig. 1(a): Au does not form a silicide, it is characterised by the formation of an alloy at $T_E = 363^\circ\text{C}$, a low T compared to

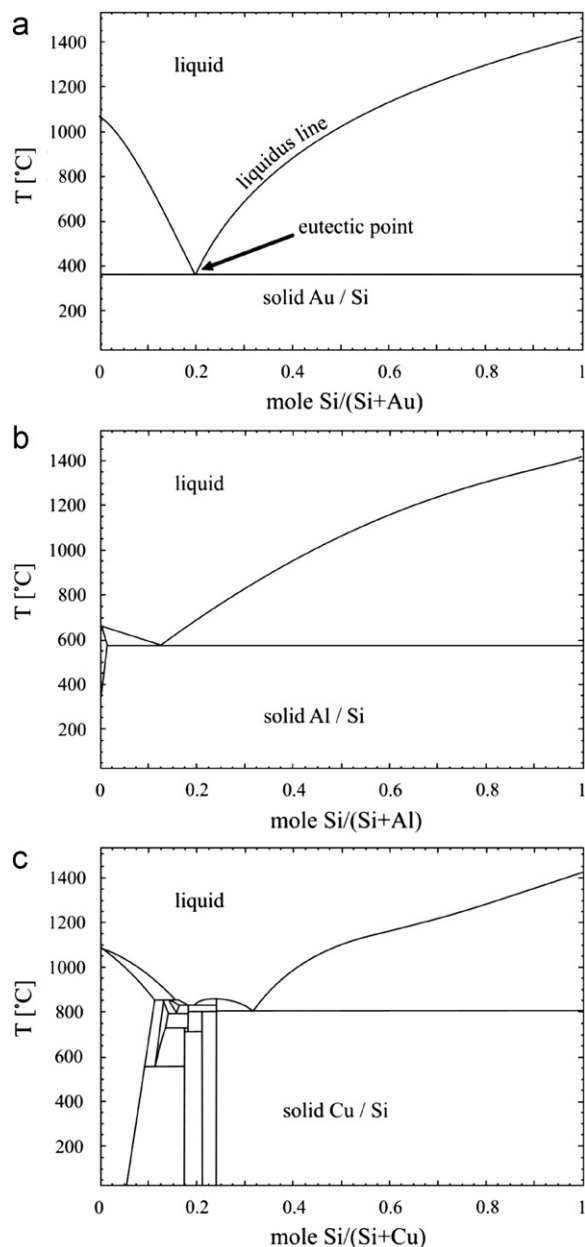


Fig. 1. Phase diagrams of (a) Au–Si, (b) Al–Si, (c) Cu–Si [18].

many other metal–Si alloys (see Fig. 1(b,c)), and the *liquidus line*, which in the diagram needs to be crossed moving towards higher Si concentrations to give rise to precipitation and therefore to VLS growth, extends over a wide range of temperatures [18]. In summary, Si NW VLS growth with Au is relatively simple, allowing for large flexibility in the choice of synthesis parameters. Unfortunately, Au is at the same time considered undesirable as far as electronic and optoelectronic applications are concerned. The main issue is associated with its incorporation into the NW during growth [19]. Au is known to act as a deep level impurity in semiconductors [20], thus it can be potentially being detrimental for the NW

electrical properties and increase non-radiative recombination. Even though the mechanism of metal incorporation in semiconductor NW growth has not been clarified yet and, interestingly, the effect such incorporation was shown to be negligible in some instances [19–21], concerns remain. In addition, Au usage poses a serious contamination problem in Complementary Metal Oxide Semiconductor (CMOS) technology, as the metal diffusion in Si and Si oxide is known to degrade device performances (e.g., by increasing p–n junction leakage or decreasing dielectric strength). These concerns pushed forward investigations of alternative catalysts. It is worth noting that VLS is not the only possible mechanism for Si NW growth. Even at temperatures below T_E , NW formation can be driven by surface or bulk diffusion into a solid droplet, by a mechanism known as vapour–solid–solid (VSS) growth. In fact, the boundary between VLS and VSS growth is not always easily determined, as size effects in nanoparticles can modify the phase diagram, effectively lowering T_E [22]. VSS growth has attracted a lot of interest in recent years mainly because it would allow using metals, such as Cu [23,24] or Al [25], more compatible with CMOS processing. As an additional advantage, the low solubility of Si in the solid metal should allow the fabrication of more abrupt heterojunctions than via VLS [26]. Yet, for the good yield and high control over morphology and composition achieved so far, VLS-based CVD remains to date the most investigated and utilised technique for Si NW synthesis, especially as far as prototype device fabrication is concerned. Given the current research trend though, this preference may change in the near future. By changing synthesis conditions, the growth rate of VLS CVD Si NWs can be tuned over a wide range, from 10^{-2} to 10^3 nm/min [27,28]. As mentioned above, the NWs diameter is related to the size of the catalyst particle. Very remarkably, this simple principle holds for an impressive range of Si NWs diameters, from as thin as 2 nm [29] up to several hundreds of micrometre thick [12]. The NWs length can be defined by simply adjusting the growth time and temperature. Notably, CVD also allows for in-situ NW doping (see Section 3), on the one hand, and axial or radial heterostructuring, on the other hand, achieved via careful balancing of the gas mixture.

2.2. Laser ablation (LA)

In the LA process, a mixed Si/catalyst target is heated at high temperature in a furnace environment, and ablated by means of a high-power pulsed laser beam. This results in the production of Si/catalyst material which is condensed into nanodroplets by an inert gas stream and carried by the gas itself to the desired substrate [1,30]. Large amount of Si NWs can be synthesised at a fast rate via this approach, which also allows a certain degree of control over NW morphology, achieved by varying the composition of the original target or by changing carrier gas [30,31]. NWs with crystalline Si cores as thin as 5 nm have been achieved via a modified LA process [32]. Remarkably, doping of Si NWs via LA has been recently achieved by ablating doped Si targets [33]. However, the need for complex, expensive equipment has so far limited this technique utilisation.

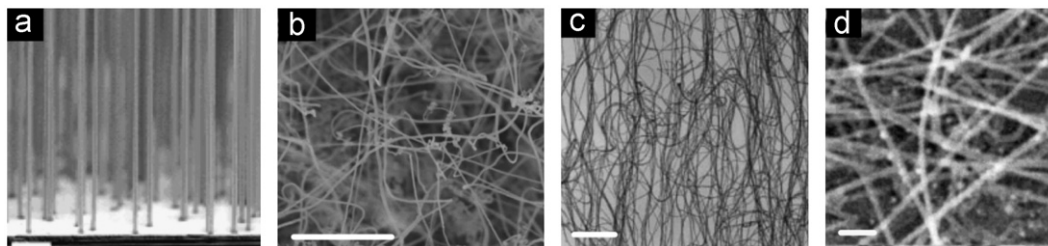


Fig. 2. Si NW synthesised via (a) CVD from SiCl_4 at 800 °C. Adapted with permission [7]; (b) thermal evaporation of Si powder at 800 °C substrate temperature; (c) OAG at 900 °C. Adapted with permission [136]; (d) solution-phase from diphenylsilane at 500 °C. Adapted with permission [137]. Scalebars: (a–c) 1 μm , (d) 200 nm.

2.3. Powder thermal evaporation

Si NWs VLS growth can also be achieved in a furnace by evaporating at high temperature ($> 1000\text{ °C}$) pure grade Si powders. The Si vapours then diffuse in the reactor tube and condense in a lower temperature region (700–800 °C) [34]. A carrier gas can also be used to facilitate the vapour transport process. A catalyst-coated substrate is placed within the condensation region. VLS growth takes place in the way previously described in Section 2.1, the only notable difference being the high substrate temperature. As a consequence, the as-grown Si NWs tend to develop curly-like morphologies (Fig. 2(b)), resembling much more the LA products than the stiff NWs obtained via CVD. This technique suffers from the same limitation of LA, in that in-situ controllable doping is, in practice, hardly achievable.

Alternatively, SiO powder can also be thermally evaporated, at even higher temperatures ($> 1300\text{ °C}$). This can give rise to Si NW growth via a completely different mechanism which goes under the name of Oxide Assisted Growth (OAG). OAG is based on the disproportionation of the evaporated SiO at the substrate position. The outcome consists of Si NWs characterised by a relatively thick SiO_2 shell (Fig. 2(c)) [34,35]. The advantage of this technique is twofold. First, use of metal catalyst is optional and growth conditions can be tuned to promote Si NW synthesis totally free of metal contamination to therefore produce CMOS compatible material. Second, metal-free growth does not require the use of substrates which, combined with the high growth rate, allows for exceptional throughput. Si NWs with diameter down to 10 nm can be synthesised via OAG [34]. Other nanostructure morphologies like nanochains can also be obtained [34,36]. Similarly to LA, the absence of an in-situ doping technique, along with a certain difficulty in achieving morphological uniformity, has thus far prevented the widespread utilisation of these materials for electronic application.

2.4. Solution-based synthesis

Another approach is based on growth of Si NWs in a liquid environment. Pioneered by Holmes et al. [37], this method utilises highly pressurised supercritical organic fluids enriched with metal particles and a liquid Si precursor to promote the one-dimensional (1D) growth of Si NWs (Fig. 2(d)). The mechanism resembles VLS in

many aspects: the synthesis is carried out above T_E , with the Si precursor decomposing at the particles surface. Si atoms then diffuse into the droplet forming an alloy. Precipitation begins when the droplet becomes supersaturated with Si. Growth of NWs as thin as 4 nm has been demonstrated using Au or Ni as catalyst [37,38]. Growth below T_E (thus via a mechanism similar to VSS) was also demonstrated by means of Cu nanoparticles at a temperature of about 500 °C [39]. Alternatively, organic solvents at atmospheric pressure and below T_E can be used to growth micrometre long Si NW about 25 nm in diameter [40]. This method is appealing in that it provides a very high yield of high quality, thin Si NWs by means of low cost equipment. Unlike CVD though, it requires ex-situ doping for use in CMOS applications.

2.5. Other methods

Amongst other methods, ultrahigh vacuum Molecular Beam Epitaxy (MBE) offers excellent control over the synthesis conditions, allowing for example fabrication of heterostructures with abrupt interfaces. In MBE, a heated solid Si source provides a gaseous beam of Si atoms. This is directed onto a substrate where metal particles initiate the growth via the VLS mechanism previously described. Notice that, unlike CVD, the metal does not crack the precursor. It promotes the growth by forming an alloy with the semiconductor. Also, the flow of Si atoms diffusing from the Si substrate to the metal can affect the growth dynamics. MBE allows growth of highly crystalline and pure Si NWs [41], as well as controlled in-situ doping [42]. However, the NW growth rate is very low, only few nm/min [41], NW yield is low as well, and the minimum NW diameter achievable appears to be fundamentally limited to about 40 nm [43].

Additional methods include annealing of Si in a reactive atmosphere, which consists of annealing metal-contaminated Si wafers in reactive gases such as H_2 or I_2 [44], and hydrothermal growth, a metal-free method carried out in a liquid media and based on the OAG mechanism [45].

3. Doping

3.1. Introduction

Semiconductor technology relies on the ability to precisely tune the number of charge carriers, n or p, contributing to the conduction in the active layer of a device. For NW

bottom-up approaches to be considered a realistic option in electronics, techniques capable of introducing a deterministic amount of impurities into 1D structures need to be developed. One choice would be to try to adapt the existing, standardised, post-synthesis methods for bulk and thin-film doping, the two most popular being diffusion from solid phase [46] and ion-implantation [47]. Alternatively, in-situ approaches based on the idea of introducing dopants during the nanostructures self-assembling can be pursued. This method resembles the diffusion from the gas phase approach which has been long used by semiconductor industry [48,49]. In recent years, a lot of effort has been devoted to the investigations of both approaches for NW doping [50].

The challenges faced are manifold: on one side, NWs represent a completely different system from bulk or thin-films. In particular, high surface-to-volume ratio, vicinity of the surface to the channel, use of vertical device geometries, and even the NW cylindrical shape itself, all contribute to make standard post-growth techniques considerably more difficult to be implemented in 1D structures. On the other hand, it has been shown that in-situ doping affects the growth dynamics, generally leading to degradation of NW morphology and yield when high impurities concentrations are required [51,52]. In both the case of post-growth and in-situ doping, collecting information on impurities or carrier concentrations is frustrated by the impracticability, from geometrical considerations on 1D systems, of Hall measurements, a limitation which makes proper dopants characterisation challenging. As additional requirements, an effective doping technique should also enable high levels of doping concentrations and good control over the spatial distribution of dopants, which may dramatically affect performances as device dimensions are shrunk [20]. Finally, it needs to be, of course, reproducible, scalable and cost-effective.

3.2. Ion implantation

Ion implantation is a mature technology for top-down semiconductor processing [53]. It was first employed in relation to the bottom-up NW field to investigate the damage caused by Ga^+ ions implantation in GaN NWs [54,55]. As far as NW doping is concerned, the first reported experiment [56] utilised implantation of phosphorus atoms to fabricate conventional-like Si NW FETs (see Section 4.2). This was achieved by doping the NWs regions below the source and drain contacts, effectively implementing two junctions and an n/intrinsic/n-Si channel [56]. It is important to notice that in this experiment the fluence, i.e. the number of ions delivered per unit area, was kept to 4×10^{12} ions/cm², well below the full amorphization threshold of crystalline Si under P bombardment (2×10^{14} ions/cm²) [57]. Amorphization of the crystalline phase is a well known consequence of the damage caused to the lattice by ions irradiation. In conventional wafers, full recrystallisation can be achieved via high temperature annealing, with the bulk Si substrate acting as a seed for the recovery of the crystallographic structure. On the other hand, full amorphization can be a major concern for NWs. If this occurs, the lack of a

crystalline seed may in principle prevent the structure recrystallisation. This issue was investigated in more detail by Colli et al. [58] by implanting thin (10–20 nm core diameter) Si NWs with P or B ions at fluences as high as 10^{15} ions/cm². Electrical measurements of the Si NW FETs fabricated from as-implanted NWs confirmed the n and p-doping. Surprisingly, Raman spectroscopy measurements showed partial or no amorphization of the crystalline core, thus allowing a full recovery of the ordered structure upon furnace annealing at 800 °C. The authors speculated that this effect may be attributed to dynamic annealing, i.e. defects removal within the thermal spike generated in the vicinity of the ion impact region by the energy transferred to phonons by the implanted ions themselves [59], as previously observed for the Ga^+ implantation of GaN NWs [54]. The annealing would be a consequence of morphology-dependent properties such as high diffusivity of mobile point defects [54] and limited thermal conductivity of thin Si NWs [60]. Alternatively, NW partial amorphization can also be achieved by tuning the energy of the impinging ions and decreasing the implantation depth, thus retaining in the NWs portions of crystalline phase [61]. All these findings imply the feasibility of NW implantation at fluences higher than in the bulk, provided that care is taken in tailoring the recovery thermal annealing step [62]. An additional issue associated with ion implantation doping is the sputtering (or ion milling), i.e. the removal of atoms from the target structure due to collision with an impinging dopant [59]. Sputtering is enhanced for steep angle incidence and it is therefore particularly prominent at the sides of cylindrical NWs, which can experience severe reductions in lateral diameter and shape modifications as consequences of this effect. On the other hand, vertical NWs, whose top-surface is perpendicular to the ion beam, are not significantly affected by sputtering, as showed in demonstrations of vertical p–n junctions [63,64]. In summary, ion implantation can be considered a promising technique for NW doping, yet questions remain concerning the intrinsic limits to practical device implementation.

3.3. Solid-phase diffusion

NW doping can also be achieved post-growth via solid phase diffusion techniques. For example, B doping of Si NW can be achieved by Spin-On Dopant (SOD) proximity diffusion of dopants from a source to a nearby Si NW forest, followed by a “drive-in” step to distribute the dose uniformly into the NWs [65]. Alternatively, both n and p-type doping NWs were obtained by diffusion from an oxide layer doped via Plasma Enhanced CVD [66]. Both techniques are capable of doping NWs uniformly but lack control over the axial distribution of dopants. Controlled doping was also achieved via a self-limiting “monolayer doping (MLD) strategy” based on the self-assembly on the NWs surface of dopant-containing molecules followed by an RTA step to break the molecular structure and diffuse the dopants into the NWs [67]. This allowed for implementation of Si NW devices with doped contact regions. However, the suitability of this technique for fabrication of abrupt p–n junctions is questionable.

3.4. Gas-phase diffusion

In situ techniques have been so far the most popular means for doping bottom-up NWs. As far as Si NWs are concerned, both n- and p-type doping were first demonstrated in an LA process by Cui et al. [68] employing phosphorus or boron as sources of dopants. Nowadays, synthesis of doped Si NWs is more often pursued in CVD reactors, a more accessible set-up than LA. Typically, PH_3 is utilised for n-type doping [69–73], and B_2H_6 for p-type doping [51,68,74], but several alternative precursors have also been explored [75,76]. MBE in-situ doping of Si NW has also been reported [42], obtained via co-evaporation of Si and B precursors.

In VLS, two important factors controlling the dynamics of dopant incorporation during axial growth are the solubility of impurities in the catalytic metal particle and their segregation coefficient (i.e., the ratio between the concentration of impurities in the solid NW and in the liquid alloy, at equilibrium). Low solubility and high segregation coefficient result in fast migration of dopants from the metal seed into the NW. Therefore, the largest part of the impurities supplied to the droplet from the vapour phase will be transferred to the solid. The opposite scenario of high solubility and low segregation is less favourable for incorporation of impurities in NWs, as it promotes the buildup of a high concentration of dopants in the metal droplet and, consequently, their re-evaporation and loss. The former scenario is the case, for example, of P incorporation from Au seeds into Si NWs [50]. It was found that the P concentration could be gradually raised by increasing the $\text{PH}_3:\text{SiH}_4$ ratio up to $1.5 \times 10^{20} \text{ cm}^{-3}$ [52]. Reaching the limit of P solubility in solid Si was made possible by the swift transport of dopants from the melted Si-metal alloy to the solid Si phase. At this point, further increments in PH_3 molar fraction could no longer alter the dopants concentration in Si [52]. On the other hand, incorporation of B has not been systematically investigated so far but the general finding is that B is incorporated to a lesser extent (concentrations as high as $4 \times 10^{19} \text{ cm}^{-3}$ have been reported [75]). This phenomenon may be related to the lower solubility of B in Si [77].

The solubility and segregation coefficient also contribute in determining the sharpness of the dopant gradient as the source of Si atoms is switched on/off. The lower the solubility, the lower the number of dopants stored in the metal seed. The higher the segregation coefficient, the faster the impurities will be depleted into the solid phase. Thus, P incorporation should be capable of providing sharp doping profile while B is expected to give rise to somewhat less abrupt gradients. In fact, modulated doping of Si NW with P impurities achieved doped NW sections as thin as 30 nm [52,78]. Interestingly, due to the low solubility of dopants in the solid phase, growth via VSS is expected to give even better results in terms of abruptness [79].

As previously mentioned, introduction of dopants can affect the NW growth rate and morphology. For example, it has been reported that addition of B_2H_6 can promote instabilities and nanofaceting [51]. Non uniform radial incorporation of dopants has also been reported [80]. Finally, it is often found for growth to be hindered when

high impurity concentrations are targeted [52]. All these issues may limit the selection of suitable doping sources and the range of achievable doping levels, but the potential and demonstrated capabilities of in-situ doping techniques are certainly remarkable [52,69,70].

4. Electrical transport and devices

4.1. Current challenges

In a famous publication dating back to 1965, Gordon Moore predicted that the number of transistors on a chip would experience exponential growth in the following years (his initial estimate of a doubling every year [81], based on the previous six years data, was later adjusted to a doubling every two years [82]). Moore's law, as it came to be known the prediction, eventually turned into a self-fulfilling prophecy which challenged (and keeps challenging to date) semiconductor industry to meet the target it set. Increase in transistor density is primarily achieved by shrinking device dimensions. The device gate length, L_G , is often used as synthetic parameter to describe the scaling (in conventional MOSFETs the effective channel length is about 50% of L_G). The natural outcome of size reduction is the capability to pack more functionality per unit chip area. In addition, size scaling lowers power dissipation and increases switching speed, especially when coupled with same-scale reduction of supply (V_{DD}) and threshold voltage (V_{TH}) [83]. However, as dimensions hit the nanoscale domain further reduction becomes challenging as short channel effects (SCEs) increasingly affect device properties.

In bulk, planar MOSFET, SCEs are a consequence of the extension into the channel of the drain and source depletion regions associated with the corresponding p–n junctions. The electric field generated at the junctions penetrates into the channel and competes for charge control with that of the gate electrode. At L_G comparable with the field penetration, SCEs become significant. SCEs can be limited by increasing dopant concentration either in the whole channel region or, more effectively, locally at the junctions (e.g., with so called halo or pocket implants). However, as device dimension keeps shrinking, the amount of dopant required to balance SCEs becomes unfeasible, both in terms of dopant concentration (which becomes too high, exceeding 10^{19} cm^{-3} , for proper device operation) and dopant gradient (which imposes severe limitations on the processing thermal budget to minimise dopants diffusion, as in a typical junction doping must be switched from 10^{19} cm^{-3} n-type to more than 10^{18} cm^{-3} p-type within few nanometres).

MOSFETs based on fully depleted Silicon-on-insulator (FDSOI) technology represent a step forward from planar MOSFETs. In FDSOI devices most of the field lines propagate through the buried oxide (BOX) before crossing the channel region. Thus, SCEs can be mitigated by using a thin buried oxide and an underlying ground plane or, alternatively, a double-gate configuration.

Yet, ultra short channel devices require even more efficient gating solutions [2]. These are provided by multi-gate approaches [84]. Unlike planar MOSFETs where the

gate only lies on top of the channel region, multi-gate devices benefit from a gate wrapped around multiple sides of the channel. This category include fin field-effect transistors (FinFETs) [85], tri-gate [86], π -gate [87], Ω -gate [88], and wrap-around MOSFETs [89], all named after the shape of their respective gate electrodes (see Fig. 3). For the reasons expressed below, these devices improve gate control and limit SCEs, therefore allowing for further device scaling.

SCEs affect electronic transport in several ways, the most notable being: (1) reduction in V_{TH} occurring when the potential barrier between source and channel is lowered by an increase in drain voltage (and thus field penetration). The barrier is present in the subthreshold region of the drain current–gate voltage (I_D – V_G) characteristic (weak inversion regime). The V_{TH} shift tends to increase off-state current I_{OFF} at zero gate voltage. This effect is known as drain-induced barrier lowering (DIBL, or surface DIBL). (2) Increase in I_{OFF} due to similar barrier reduction occurring farther from the channel-dielectric interface, where the gate control is poorer (punchthrough or subsurface DIBL). (3) Degradation of the subthreshold swing, i.e., the rate at which in the subthreshold region drain–source current can be varied by means of the gate voltage; this is directly related to the competition between drain and source fields, on the one hand, and gate field, on the other hand.

A more quantitative approach to predict the appearance of SCEs is based on a 1D modified Poisson equation, used to describe the potential at the channel-dielectric interface $\Phi_f(x)$ (alternatively, $\Phi_c(x)$, the potential at the centre of the channel, is sometimes utilised, leading to similar results and considerations). Assuming the channel

extends along the x -direction, the relation is given by [90,91]:

$$\frac{d^2 \Phi_f(x)}{dx^2} - \frac{\Phi_f(x) - \Phi_{gs} - \Phi_{bi}}{\lambda^2} = -\frac{q\rho(x)}{\epsilon_{Si}} \quad (1)$$

where $\Phi_{gs}(x)$ and $\Phi_{bi}(x)$ are the gate and built-in potential, respectively, ρ is the carrier density, and ϵ_{Si} is the silicon permittivity. λ is termed the “natural length” and is a measure of the extension of the electric field lines from the source and the drain into the channel region. It has been shown that in order to prevent SCEs, the effective gate length of a MOS device must be larger than 5–10 times λ [91]. For a single-gate device of square section, the natural length λ_1 is calculated by [91]:

$$\lambda_1 = \sqrt{\frac{\epsilon_{Si}}{\epsilon_{ox}}} t_{Si} t_{ox} \quad (2)$$

This remarkably simple relation suggests that to minimised SCEs, one can either decrease the gate oxide thickness t_{ox} or reduce the thickness t_{Si} of the silicon film. It must be noted however that in single-gate devices these solutions have already been pushed to their limits [84]. Alternatively, use of insulating materials of higher dielectric constant would also improve (decrease) λ_1 by affecting the gate oxide term ϵ_{ox} in Eq. (2).

By choosing appropriate sets of coordinates and boundary conditions, a set of equations retaining the same form of Eq. (1) can be written to describe single-, double-, triple-, π -, and Ω -gate devices as well as wrap-around MOSFETs, of square or circular section (see Table 1). Interestingly, it turns out that for square section channels, λ_N (defined as λ in a N -gate device) simply scales as $\lambda_1/\sqrt{N}$, indicating that tighter gate control is obtained as the number of gates increases, effectively allowing further scaling of transistor dimensions.

It was previously mentioned that in the ideal scenario a reduction of V_{TH} would accompany size scaling, to promote maximum improvement of performance. In practice, lowering of V_{TH} has significantly slowed down in recent years. This is consequence of the limits on the subthreshold slope (SS). SS is the inverse of the subthreshold swing and is defined as:

$$SS = \frac{dV_G}{d(\log(I_D))} \quad (3)$$

where V_G is the gate voltage and I_D the drain current. Any device relying on injection of carriers from a thermally broadened Fermi distribution (thus including all the aforementioned MOSFETs) experiences a room temperature lower limit for SS of about 60 mV/dec. This fundamental limitation arises from the properties of electron transport in the subthreshold regime. The diffusion current between drain and source depends on the height of the barrier. At the source electrode, the electron density n is determined by the well known relation:

$$n \approx N_C e^{-(E_C - E_F)/KT} \quad (4)$$

where N_C is the effective density of states, E_C the conduction band energy, E_F the Fermi energy, K the Boltzmann constant and T the temperature in Kelvin. This arises from the convolution of the Density of States (assumed

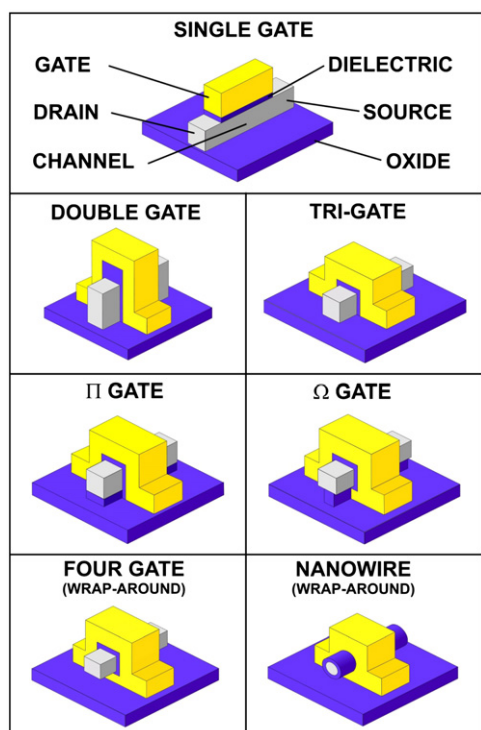


Fig. 3. Schematic representation of different gating strategies.

Table 1

Natural length in FETs with various gate configurations and channel sections.

	Square section	Ref.	Circular section	Ref.
Single gate	$\lambda_1 = \sqrt{\frac{\epsilon_{\text{Si}}}{\epsilon_{\text{ox}}} t_{\text{Si}} t_{\text{ox}}}$	[91]		
Single planar back-gate			$\lambda'_1 = \sqrt{\frac{\epsilon_{\text{Si}}}{\epsilon_{\text{ox}}} t_{\text{Si}} t_{\text{ox}}}$	[93]
Double gate	$\lambda_2 = \sqrt{\frac{\epsilon_{\text{Si}}}{2\epsilon_{\text{ox}}} t_{\text{Si}} t_{\text{ox}}} = \frac{\lambda_1}{\sqrt{2}}$	[91]	$\lambda'_2 = \sqrt{\frac{\epsilon_{\text{Si}}}{2\epsilon_{\text{ox}}} (1 + \frac{t_{\text{ox}} t_{\text{Si}}}{4\epsilon_{\text{Si}} t_{\text{ox}}}) t_{\text{Si}} t_{\text{ox}}}$	[95]
Tri-gate	$\lambda_3 = \sqrt{\frac{\epsilon_{\text{Si}}}{3\epsilon_{\text{ox}}} t_{\text{Si}} t_{\text{ox}}} = \frac{\lambda_1}{\sqrt{3}}$	[92]		
Π - and Ω -gate	$\lambda_z = \sqrt{\frac{\epsilon_{\text{Si}}}{2\epsilon_{\text{ox}}} t_{\text{Si}} t_{\text{ox}}} = \frac{\lambda_1}{\sqrt{2}} \quad 3 < z < 4 (z_{\Pi} \neq z_{\Omega})$	[84]		
Wrap-around (four gates)	$\lambda_4 = \sqrt{\frac{\epsilon_{\text{Si}}}{4\epsilon_{\text{ox}}} t_{\text{Si}} t_{\text{ox}}} = \frac{\lambda_1}{\sqrt{4}}$	[93]	$\lambda'_4 = \sqrt{\frac{2\epsilon_{\text{Si}} t_{\text{Si}}^2 \ln(1 + \frac{2t_{\text{ox}}}{t_{\text{Si}}}) + \epsilon_{\text{ox}} t_{\text{ox}}^2}{16\epsilon_{\text{ox}}}}$	[96]

3-dimensional) with the Fermi–Dirac distribution. As the source-channel barrier is lowered by applying a gate potential, the density of electrons with sufficient energy to overcome the barrier will therefore increase exponentially for a linear decrease in channel potential. The maximum current variation (proportional to n) will be therefore limited, at $T=300$ K, to:

$$SS \approx \ln(10) \frac{KT}{q} \approx 60 \text{ mV/dec} \quad (5)$$

In practice, the electrostatic coupling between the gate voltage V_G and the channel potential ϕ_f is not perfect. Therefore, the thermodynamic lower limit on SS increases by a factor of $n=dV_G/d\phi_f$ with $n>1$, because a larger variation of V_G is needed to vary ϕ_f (and thus the current).

Interestingly, several devices that are not limited to 60 mV/dec have also been proposed [97–102]. These would in principle allow further reduction of V_{TH} . Some of these have been realised by using nanowires and will be discussed in the following section.

4.2. SS-limited nanowire devices

Geometry itself makes NWs an ideal system for the implementation of multi-gate devices and realise the much needed tight gate control over carriers transport by minimising SCEs. It has been predicted that multi-gate MOSFETs will manage to push the scaling of L_G down to the 3 nm node [103]. NW-FETs can be assembled in radically different architectures. Planar geometries based on horizontal NWs are usually easier to implement because they provide more freedom in the choice of the synthesis technique, not requiring growth of vertically aligned nanostructures. In addition, they allow for post-synthesis transfer of the NWs onto an arbitrary substrate therefore expanding the available set of substrates for both growth and device implementation. As a consequence planar NW-FETs have been, and still are, the most extensively studied. It must be noted that in the context of this section and hereafter in the text, “planar” refers to the parallel direction of the NWs with respect to the substrate and characterises the devices dimensionality, 1D or 2D. This is unlike conventional MOSFETs where planar is often synonymous with single-gate. In contrast, planar NW devices are in the vast majority of cases multi-gate devices.

On the basis of their electrical behaviour, one can distinguish three types of NW-FET whose injection mechanism limits their room temperature SS to 60 mV/dec: “conventional-like”, Schottky-barrier (SB), and junctionless (JL) devices. In their simplest implementation, they all rely on establishing electrical connections to multiple or individual, horizontal Si NWs. Channel conductance is modulated by means of capacitive coupling of one or more gate electrodes. There exists a certain confusion regarding the boundaries between these three categories. For example, a NW-FET assembled from a uniform intrinsic Si NW and operated by means of a combination of bottom and top-gates may be characterised by Schottky barriers at the metal/NW junctions. Yet, its transport behaviour would be comparable to that of a conventional MOSFET. Moreover, the fabrication process of such a NW-FET may be remarkably similar to that of a JL NW-FET, the only difference being in the properties and/or physical size of the NW used as building block. Nevertheless, the two devices would operate very differently. The following sections will try to dispel these and other sources of ambiguity.

4.2.1. “Conventional-like” Si NW-FETs

“Conventional-like” NW-FETs resemble the standard single-gate MOSFET in terms of operational behaviour: charge flow is regulated by the potential barriers arising at the semiconductor/semiconductor junctions. Such junctions can be realised in two distinct ways. On the one hand, they are obtained by physically doping the area below the drain–source metal contacts (see Fig. 4(a)). This naturally corresponds to the standard solution widely adopted by semiconductor industry. Interestingly, as discussed in Section 3, doping strategies for bottom-up NWs are not limited to ion-implantation [56,58,104] but alternative methods like in-situ doping [105] or solid-phase post-growth doping [66] are also available. On the other hand, by using a dual gate configuration¹ (see Fig. 4(b)) it is possible to induce in the channel the formation of separate sections with variable “electrostatic doping”.

¹ Dual-gate FET is not to be confused with the previously mentioned double-gate FET. The former refers to the physical presence of two independent gate electrodes while the latter reflects the number of channel sides affected by the electric field of a single, or common, gate electrode (two sides, in a double-gate FET).

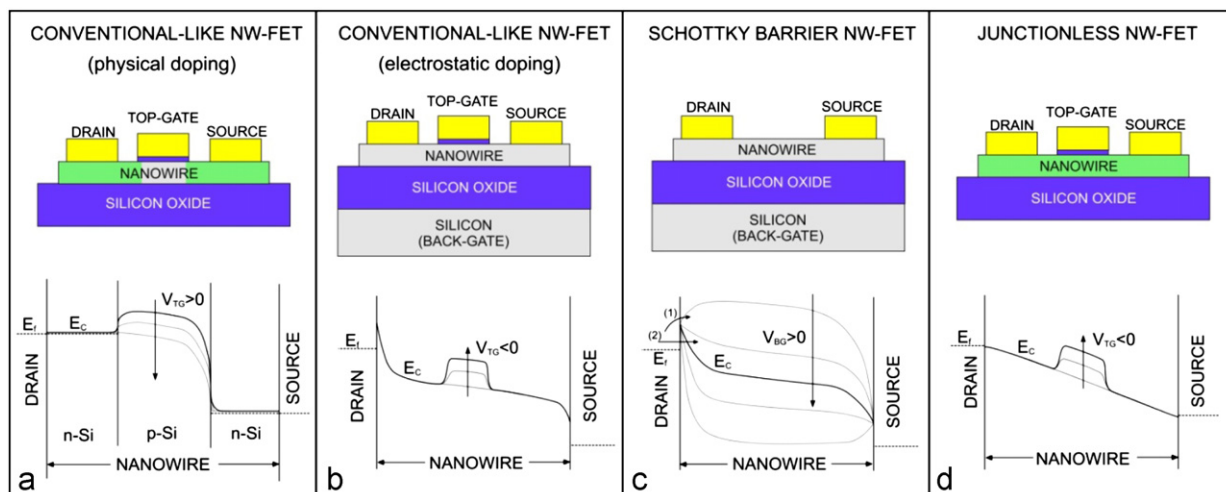


Fig. 4. NW-FET classification and band structure. As an example, the case of electron injection is represented, under $V_{DS} < 0$. Bands at different gate voltage (either V_{TG} or V_{BG}) are shown. The arrows over the bands points in the direction of increasing gate voltage (in modulus). Only the conduction band is shown in the diagrams. (a) Conventional-like NW-FET with p–n junctions formed by doping drain and source regions with opposite dopant type than in the channel. (b) Conventional-like device obtained via electrostatic doping in dual-gate configuration. V_{BG} sets the injection through the SBs, V_{TG} modulates the conductance. (c) SB device controlled via a global back-gate. Injection occurs over the barrier (thermal excitation, case 1) or through the barrier (tunnelling, case 2). (d) JL NW-FET from a highly doped NW. Tight gate control is needed to deplete the channel.

Most commonly, a back-gate electrode is utilised to shift the bands in the channel to accumulate carriers and set the barrier at the metal contacts. This selects whether n or p carriers are injected into the channel and correspondingly “dopes” the NW portion affected by the back-gate field. A top-gate electrode partially screens the field of the back-gate, allowing us to reverse the doping in the region underlying the electrode itself. The outcome of this process is the formation of two junctions approximately located at the top-gate sides. If the device is operated by varying the top-gate voltage at constant back-gate voltage, it should in principle tend to mimic the behaviour of a NW-FET realised with physical doping.

Examples of “conventional-like” tri-gate NW-FETs using bottom-up Si NW and relying on the physical doping of the channel have been demonstrated via low-fluence ion-implantation [56], in-situ VLS doping using PH_3 [105], and local phase-diffusion from a doped SiO_x layer [66]. In addition, Cohen et al. achieved similar results by heavily doping a Si buffer layer overgrown on top of a Si NW at the drain and source locations [104]. Other groups investigated dual-gate devices obtained using bottom-up grown NWs [106,107]. General findings are I_{ON}/I_{OFF} ratio above 10^6 and high drive currents ($10\text{--}100\text{ }\mu\text{A }\mu\text{m}^{-1}$) (see Fig. 5). Yet, scattered value for SS were reported, all remaining well above the theoretical minimum of 60 mV/dec. The most likely explanation for this limitation is the presence of Si/SiO_x interface states, which lower the penetration of gate field lines into the channel, thus affecting the gate-coupling efficiency ($dV_G/d\phi_f > 1$). Au contamination has also been suggested as a source of non-ideality but the effect of in-growth metal incorporation into Si nanostructures remains controversial to date (as discussed in Section 2). Estimated mobilities were generally lower than in bulk Si [56,104,105]. On one side, this may be related to the errors introduced

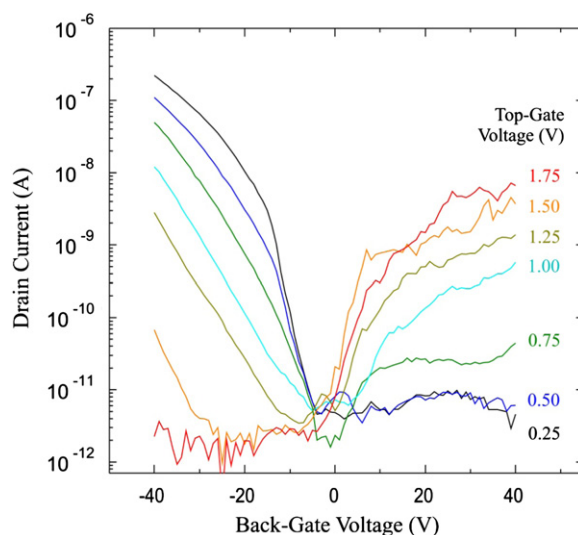


Fig. 5. I_D – V_{BG} transfer curves of a dual-gate bottom-up Si NW-FET, at $V_{DS} = 1$ V. By varying V_{TG} from 0.25 to -1.75 V, a progressive enhancement (suppression) of electron (hole) conduction and, consequently, unipolar behaviour are obtained. Adapted with permission [107].

by incorrect approximation of quantities such as the oxide capacitance or the channel charge, commonly evaluated on the basis of simplified models [20]. Interestingly, Appenzeller et al. [94,106] pointed out the complexity of ruling out contact effects in electrostatically doped FETs, reporting an unexpected variation in mobility upon contact annealing. In principle, annealing should improve carrier injection at the lateral Schottky barriers but have no effect on the transport as regulated by the gate electrode. This discrepancy may cause incorrect estimation of transport parameters in such devices.

It must be noted that even earlier reports on tri-gate and wrap-around Si NW-FETs with NW diameter down to 5 nm and implemented using top-down technologies [108,109] demonstrated, along with similar I_{ON}/I_{OFF} ratios, even higher drive currents (up to 1.5 mA/ μ m), low DIBL (10–20 mV/V) and almost ideal SS (63–80 mV/dec). Although these devices were fabricated using non-scalable electron beam lithographic techniques, the comparison shows the powerfulness of standardised techniques for device processing and integration, appearing to be well ahead of bottom-up methods.

4.2.2. Schottky barrier Si NW-FETs

The concept of a SB MOSFET was first proposed and developed in the 60s [110,111]. In this device, metal/semiconductor junctions are implemented in place of the standard semiconductor/semiconductor junctions, at source and drain, introducing two SBs of height ϕ_B . The height of the barrier for electrons ($\phi_{B,e}$) and holes ($\phi_{B,h}$) depends on the magnitude of the metal workfunction and on the arrangement of the chemical bonds at the metal/semiconductor interface, the latter being responsible for the so called Fermi level pinning. Typically, metals forming silicides upon annealing are used as they allow for atomically abrupt junction formation. Common silicides are platinum silicide ($\phi_{B,h}=0.15\text{--}0.27$ eV [112,113]), erbium silicide ($\phi_{B,e}=0.36$ eV [114]), ytterbium silicide ($\phi_{B,e}=0.27$ eV [115]) and nickel silicide ($\phi_{B,e}=0.66$ eV, $\phi_{B,h}=0.46$ eV [116]). Motivations for developing SB technology include inherent scalability to sub-10 nm L_G due to the extreme junction abruptness, lower parasitic resistance, and lower processing temperature.

Electronic transport in SB MOSFETs fundamentally differs from their conventional MOSFETs counterparts. Carrier injection into the channel occurs via emission above the SB (thermal emission) and tunnelling through the SB (thermionic emission and field-emission). The gate voltage regulates the current in a non-linear fashion. As an example, in n-type devices, varying V_G to control the channel potential ϕ_f when the condition $\phi_f > \phi_B$ is satisfied, leads to injection behaviour similar to conventional MOSFETs (with $dV_G/d\phi_f=1$, assuming ideal gate-channel coupling). As gate voltage is increased and bands are bent further, ϕ_f will drop below ϕ_B . Thus, with the SB getting thinner, injection will be progressively more and more dominated by tunnelling. Consequently, the control of V_G over ϕ_f is reduced ($dV_G/d\phi_f > 1$) and an increase in SS is experienced. A modified natural length λ can be introduced to account for both thermal emission and tunnelling to obtain a synthetic parameter to estimate the channel length at which SCEs are significant [94].

As far as research on bottom-up NWs is concerned, SB NW-FETs benefit from the simplest fabrication process and were the first to be studied [68,117]. The basic device is obtained by simple drain and source patterning and metal deposition on a Si NW transferred on a thermally oxidised Si wafer (Fig. 4(c)). The wafer itself can be used to apply the back-gate, in a single-gate fashion. The gate field affects the channel and both junctions at the same time. Alternatively, a top-gate extending over both SBs can be utilised, the thinner dielectric significantly

improving gate-coupling. While in principle various metals can be used to form SB on Si [68,117,118], contact is greatly improved if silicide formation can be promoted via annealing. This is particularly crucial in NW devices, where the small contact area tends to give rise to high contact resistance. For the nickel case, a popular metal for SB NW-FET fabrication, sufficient temperature and annealing time promotes the silicide intrusion into the NW body, effectively shortening the channel length [106]. This effect has been used to tune the channel length to the desired value [118]. The transfer characteristic $I_D\text{--}V_G$ of back-gated, planar SB NW-FETs with nickel contacts usually shows ambipolar behaviour, i.e., both electrons and holes can be injected in the channel by selecting a positive or negative V_G , respectively [58,106] (see Fig. 6). Ambipolarity is result of the alignment of the nickel silicide Fermi level close to the middle of the silicon bandgap and the comparable $\phi_{B,e}$ and $\phi_{B,h}$ that are formed as a consequence. In practice, $\phi_{B,e} > \phi_{B,h}$ is usually the case, therefore hole injection is favoured and current density is higher for holes rather than for electrons.

Reported SB NW-FETs demonstrated an I_{ON}/I_{OFF} ratio $> 10^6$ and drive currents as high as 50 μ A/ μ m [58,106,119]. When operated via a back-gate (through the thermally grown Si oxide layer of thickness > 100 nm) it is not unusual for these devices to show very poor SS, on the order of 1 V/dec [58,106,119]. This is attributed to inefficient coupling between gate and junctions but the injection mechanism plays an important role as well. In fact, controlling the channel conductance with a top-gate separated by few nanometres of dielectric was shown to dramatically improve SS, to 110 mV/dec in the thermal emission regime, and 200 mV/dec in the tunnelling dominated regime [120]. Nevertheless, these values are far from those achieved in “conventional-like” NW-FETs because of inherent injection limitations.

Very recently, Heinzig et al. proposed a novel design for SB Si NW-FETs for reconfigurable transistor implementation [121]. The devices are based on intrinsic Si NWs with NiSi₂ contacts and make use of their ambipolar behaviour: the type of carriers contributing to the conductance can be selected at will by proper choice of the voltage at the two top-gates, each of them independently controlling one of the SBs. The use of two gates also

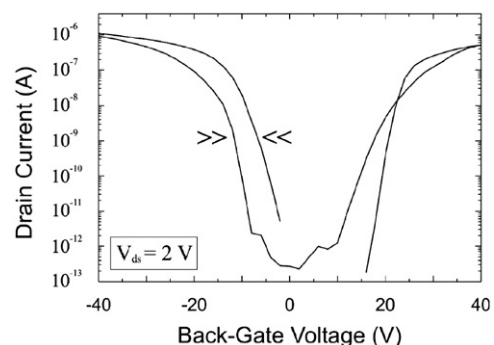


Fig. 6. $I_D\text{--}V_{BG}$ transfer curve of a SB NW-FET based on an intrinsic Si NW with annealed Ni contacts, showing ambipolar behaviour. Arrows indicate the V_{BG} scan direction, which shows a strong hysteresis effect.

suppresses leakage currents, raising the I_{ON}/I_{OFF} ratio to 10^9 . Application in reprogrammable circuits is envisaged.

Fabrication of top-down devices mostly focused on single-gate devices. While achieving control of the channel proved to be more challenging than in conventional MOSFETs, excellent results were obtained with a 2.5 nm gate dielectric and forming a 10 nm thick interfacial layer between drain and source [122]. The device reported had $> 1 \text{ mA}/\mu\text{m}$ drive current, I_{ON}/I_{OFF} ratio $> 10^6$ and SS $< 100 \text{ mV}/\text{dec}$ [122].

4.2.3. Junctionless Si NW-FETs

In contrast to conventional and SB FETs, JL FETs have no potential barrier engineered *a priori* [123,124]. In practice, the JL FET is a multigate device coinciding with a gated transistor (i.e., a resistor in which the gate electric field can modulate the current flow). The JL FET state is normally on but by virtue of the small size of the conductive channel and the tight gate control, conductance can be switched off by electrostatically depleting channel carriers.

Fabrication-wise, JL NW-FETs resemble in many aspects the “conventional-like” NW FETs with electrostatic doping (the dual-gate FETs) previously discussed in Section 4.2.1 (Fig. 4(d)). Both fabrication processes involve deposition of drain, source, and top-gate electrodes, although an additional back-gate is present in dual-gate FETs. This similarity may generate certain confusion between the two categories. In a sense, the JL NW-FET can be considered evolving from its “conventional-like” counterpart: the main differences reside in the limitations imposed over JL NW-FETs on doping level and channel dimensions. In a JL FET the whole channel is uniformly heavily doped. On one side, this ensures metal/semiconductor junctions do not develop SBs but ohmic contacts. Equally important, high drive currents can then be obtained without the need of promoting carrier accumulation by using the global back-gate. Carriers can travel through the whole section of the NW, not being confined to a relatively thin layer in close proximity to the surface. Thus, to vary the current flow, extreme control of the gate over the channel is required. This requires the use of multigate configurations and as well as ultra-thin channels, usually on the order of 10 nm. Increasing doping in devices with larger channels progressively lowers I_{ON}/I_{OFF} , eventually resulting in the loss of current modulation.

JL FETs are expected to allow extreme L_C scaling [103]. Perhaps surprisingly, there is no report to date of JL FETs assembled from bottom-up Si NWs. Yet, considering the achievements in NW synthesis and doping, fabrication would be certainly within reach, and more complex geometries including for example highly doped Si p–n junctions have in fact been pursued. Instead, the potential of JL FETs was first recognised and investigated in top-down fabricated Si NWs [123,124] which reported, for a $(10 \times 30.5) \text{ nm}^2$ rectangular section NW, I_{ON}/I_{OFF} ratio greater than 10^6 , drive current of $1 \text{ mA}/\mu\text{m}$ at $V_D = 1 \text{ V}$, SS = $64 \text{ mV}/\text{dec}$ thus very close to the theoretical limit, and mobilities comparable to doped bulk Si [124]. These results confirm that electrostatic depletion of channel carriers is at least as efficient in turning off the device as using a reverse-biased junction.

4.3. Steep-SS nanowire devices

“Conventional-like”, SB, and JL MOSFETs are inherently limited in the steepness of SS and to the minimum value at room temperature of $60 \text{ mV}/\text{dec}$. This is because all these devices share the carrier injection process, the previously mentioned injection from a thermally broadened Fermi distribution. As a consequence of this limit, V_{TH} scaling could not keep up with the pace of scaling of the physical dimensions of transistors, because for a given I_{ON}/I_{OFF} ratio, SS sets the minimum voltage variation needed to switch the device on or off.

However, other devices are conceivable which do not rely on the same injection mechanism and are therefore not subject to the aforementioned limits. In this regard, two architectures are of particular interest: the Impact Ionisation (II) MOSFET and the tunnel FET.

Impact Ionisation (II) is the phenomenon by which energetic carriers travelling in a material lose energy and generate other carriers. In semiconductors, under high electric fields, II can give rise to a cascade of carrier multiplication and to the consequent avalanche breakdown. Interestingly, devices based on this process achieve much steeper SS, with a significant improvement over the room temperature limit of $60 \text{ mV}/\text{dec}$. In order to induce II in a MOSFET architecture, a p–i–n structure is implemented, with a top-gate partially covering the intrinsic section of the channel [125] (Fig. 7(a)). The partial covering is crucial to obtain sufficient band bending for the

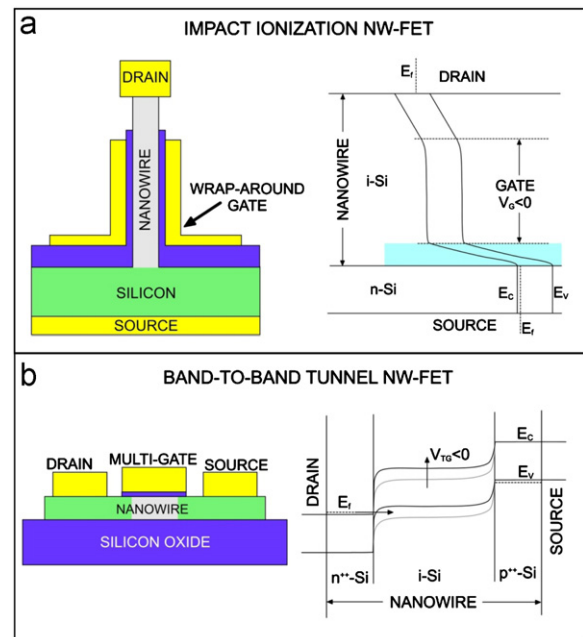


Fig. 7. Schematic and band structure of steep-SS FETs. (a) Example of II MOSFET as demonstrated in Ref. [126]. Positive energy axis points left and negative V_{DS} is taken. Planar configuration is also possible. At sufficiently negative V_G , strong band bending (highlighted region in the band diagram) generates II and avalanche breakdown. The device can also be operated at positive V_G , with II occurring near the drain. (b) Tunnel FET from doped NW. Here, $V_{DS} > 0$. A negative V_{TG} shifts the bands upwards and allows tunnelling from the n^{++} doped section into the channel.

associated electric field to promote II and avalanche breakdown under reverse gate bias (Fig. 7(a)). Bjork et al. [126] demonstrated implementation of an II MOSFET from a vertical, CVD-synthesised Si NW in wrap-around geometry. The device showed extremely steep SS for both positive and negative gate bias, 5 mV/dec and 14 mV/dec respectively, at I_{ON}/I_{OFF} ratios greater than 10^4 . In addition, the geometry utilised allowed the minimisation of one of the major concerns associated with II MOSFET: degradation due to hot carrier injection in the gate dielectric and the related reliability issues [125]. Yet, the main limitation of these devices remains the relatively high voltage required for their operation: the high electric field needed to induce II is reflected in a high drain-source voltage (around 4 V in Ref. [126] and to date no solution has been offered to this problem.

Another interesting steep-SS device is the tunnel FET (T-FET) [127,128]. Its working principle is based on the band-to-band tunnelling of carriers. This is made possible by proper band engineering, achieved in top-gated FET operated in reverse bias, with p-i-n⁺ [74,129] or p-n-n⁺ [130] channel doping (Fig. 7(b)). In contrast to II-MOSFETs, the top-gate in T-FETs covers and affects the whole channel length. Tunnelling as a mechanism for carrier injection has the potential to greatly improve the steepness of the SS, yet it is in practice a difficult result to achieve. SS smaller than 60 mV/dec was first demonstrated in a carbon nanotube-based T-FET (40 mV/dec) [127] and few years later in silicon, in a top-down device (52.8 mV/dec) [128]. To date, these results could not be replicated in wrap-around NW T-FET where the reported SS remained well above the theoretical limit [74,129,130].

4.4. Complex architectures

Potential applications of Si NWs are far from being limited to the fabrication of individual nanodevices. On the other hand, implementation of complex architectures is now actively pursued. First, existing circuitry can be reproduced by using bottom-up NWs as core device components. For example, demonstration of basic logic-gate assembly and operation dates back to more than a decade ago [131]. Yet, current research efforts try to overcome this simple approach by targeting applications for which bottom-up NWs would be better suited than their top-down counterpart. This is achieved by either taking advantage of the NW morphology to implement devices on large area, or by packing additional functionalities in a single building block.

An interesting example of the first approach is the crossbar architecture [132,33]. In this structure, arrays of parallel Si NWs are overlapped in crossed geometry and form active devices at each intersection. The design offers the benefits of high density device packing as well as those of a defect-tolerant computational architecture. More importantly, based on such NW arrangement, programmable logic arrays can be built to realise advanced computational functions [133].

On the other hand, complex functionalities can be integrated in NW devices by means of simple process flows and elementary building blocks. This is the case of

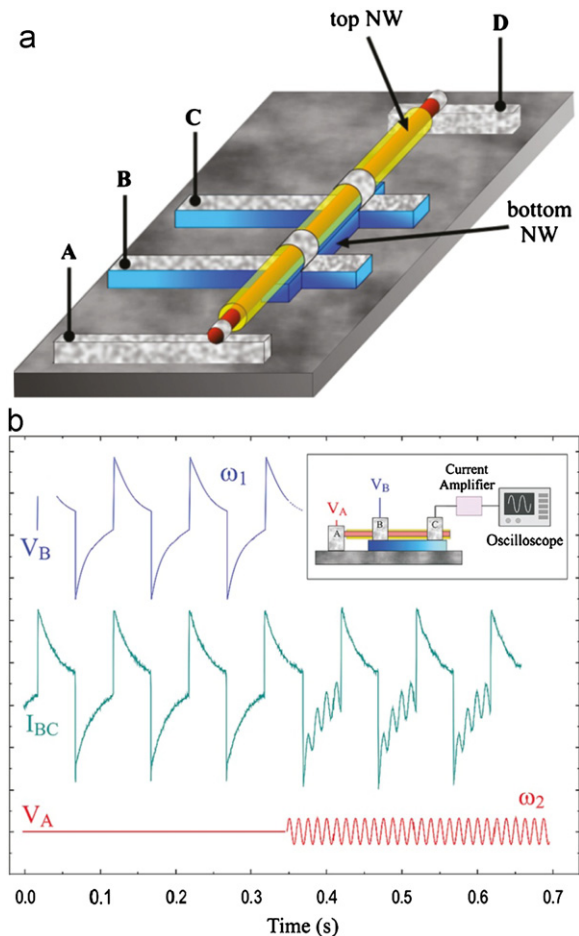


Fig. 8. Realisation of a complex architecture: the Couple Nanowire Transistor (CWT). (a) Schematic of the double NW structure, a bottom-up NW lying on top of another NW etched in an SOI layer. NWs are mutually interacting and allows for non-trivial computation. (b) Demonstration of advanced AC signal processing with the CWT. Adapted with permission [134].

the recently demonstrate Coupled Nanowire Transistor [134] which exploits the interaction of components in close proximity to each other (see Fig. 8(a)). To assemble the device, chemically synthesised Si NWs are transferred onto ultrathin SOI. By following a Nanowire Lithography approach [135], the lateral morphology of the NW is replicated in the underlying layer, with the NW itself acting as mask in a dry etching step. The process results in two overlapping Si NWs (Fig. 8(a)) which, once individually contacted, are capable of mutual interaction and, consequently, of complex signal processing (Fig. 8(b)).

5. Conclusions

The contrast between bottom-up and top-down Si NW transistors is stark, with the top-down approach almost inevitably ending up winning. Even achieving high control on NW synthesis and doping did not succeed in pushing device performances significantly ahead of those obtained via top-down methods. It now looks probable that within a decade or so conventional parallel techniques will reach

the level of sophistication needed for implementing and standardise Si NW devices down to the scale where their properties will be affected by quantum-confinement, the point at which approaches for further scaling will have to be rethought.

On top of this, practical device implementation would also require a CMOS compatible assembly technique for the transferring, deposition, alignment, and registration of billions of Si NWs grown separately of the final substrate. Alternatively, capability to grow in predetermined locations in a contamination-free environment by means of a scalable, parallel technique to define the NW nucleation sites is needed. Despite all the efforts, the hurdle of NW assembly, which has plagued the bottom-up concept since its very inception, has not been convincingly solved to date and it remains a bottleneck for the field.

It is therefore clear that the potential of the bottom-up world lies elsewhere, not in direct competition with top-down approaches but, perhaps as a complement to the current platform and used for fundamental studies via the possible implementation of devices of much more complex or even impossible realisation via top-down approaches. For example, devices based on axial or radial heterostructures, such as Ge/Si core/shell NWs, or attempts towards III–V integration on Si attracted lot of attention in recent years. Whether current challenges will be addressed and bottom-up solutions will eventually hit the market remains to be seen.

Acknowledgements

A.F. acknowledges funding from Emmanuel College.

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