

iled on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: May 12, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00244
Patent 10,886,291

PATENT OWNER'S PRELIMINARY RESPONSE

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Exhibit List

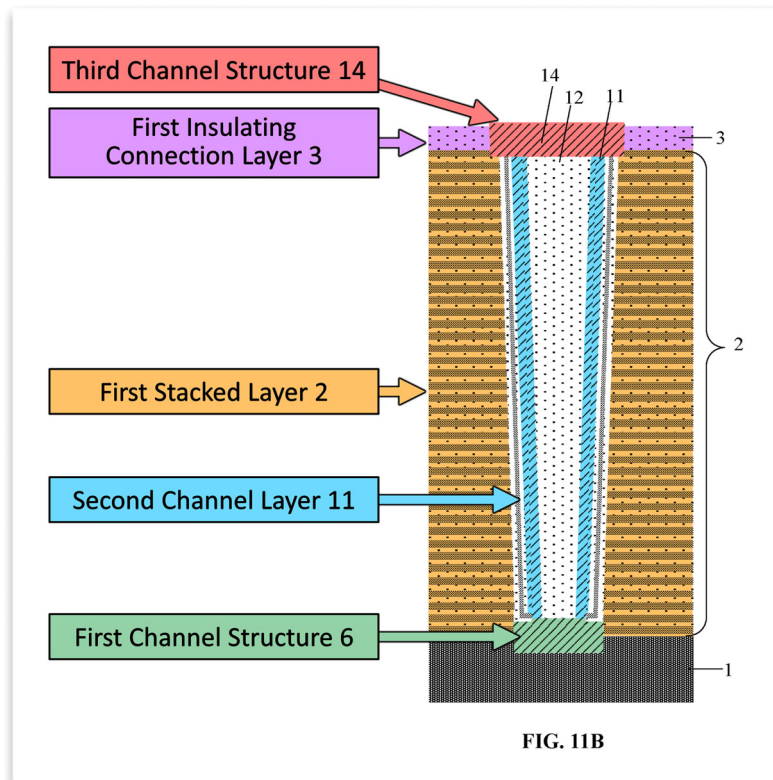
Exhibit	Description
2001	Defendants' Preliminary Invalidity Contentions and Document Production Accompanying Invalidity Contentions re YMTC II Asserted Patents (Patent Local Rules 3-3 and 3-4), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv- 05792-RFL (N.D. Cal. Nov. 25, 2024) (excerpts)
2002	Civil Minutes, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Sept. 18, 2024), ECF No. 141
2003	Order Granting Stipulation to Extend Certain Deadlines Pursuant to Patent L.R. 4-2 and the Scheduling Order (ECF No. 141) Pursuant to Civil Local Rule 6-1(b), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Jan. 8, 2025), ECF No. 194
2004	Order Granting Motion to Stay Case Pending <i>Inter Partes</i> Review, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Mar. 14, 2025), ECF No. 243
2005	Plaintiff/Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.'s and Counterclaim Defendant Yangtze Memory Technologies, Inc.'s Opposition to Micron's Motion to Stay Case Pending Inter Partes Review and Post-Grant Proceedings, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Feb. 3, 2025), ECF No. 221
2006	Declaration of Dr. Sunil P. Khatri, Ph.D In Support Of Patent Owner's Preliminary Response ("Khatri")
2007	Curriculum Vitae of Dr. Sunil P. Khatri
2008	Disclaimer in Patent Under 37 C.F.R. § 1.321(a), filed May 9, 2025

Exhibit	Description
2009	Redline comparison of Petitions filed in Case Nos. IPR2005-00244 and IPR2005-00294
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2018	Order Granting Motion to Consolidate, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Aug. 21, 2024), ECF No. 106

I. Introduction

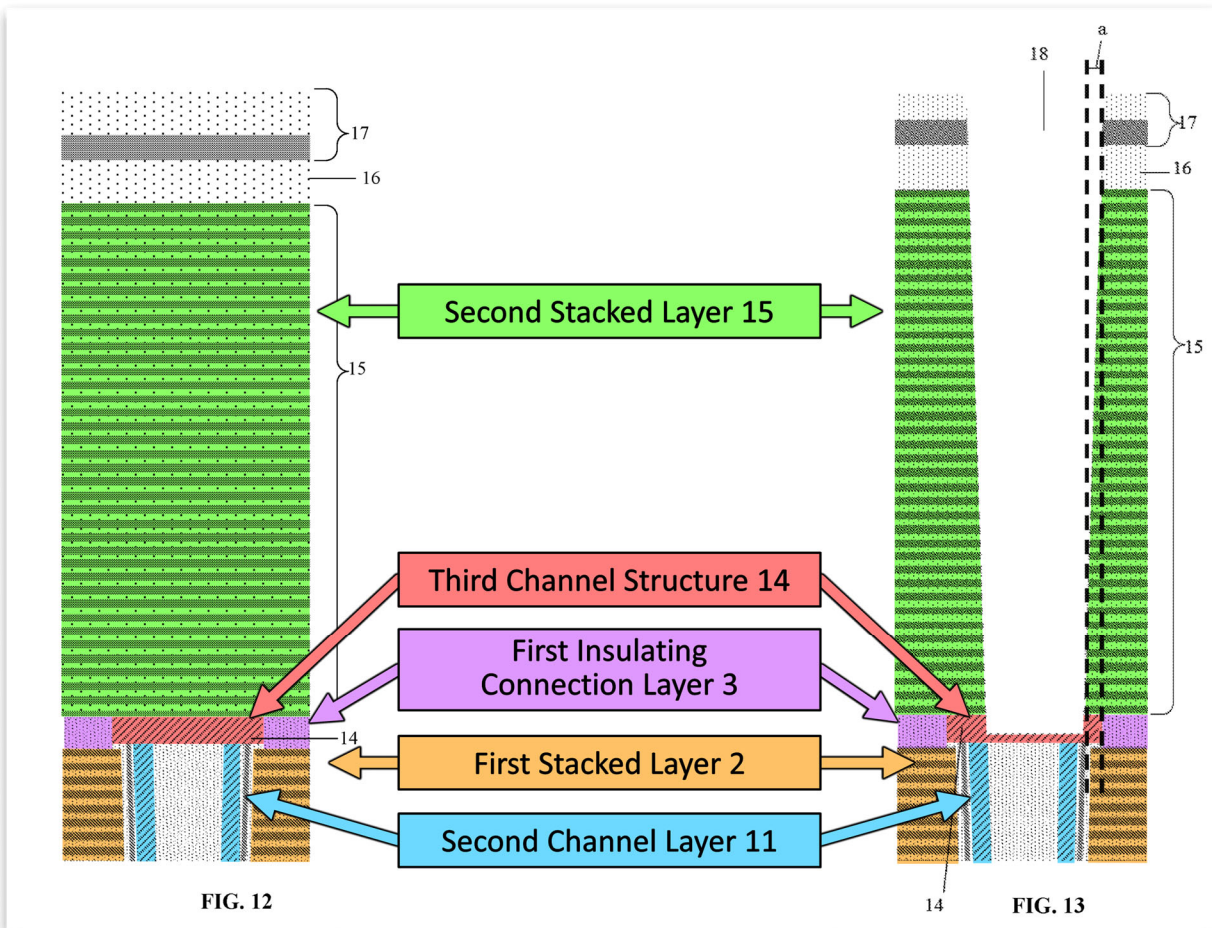
The Board should deny the Petition for *inter partes* review of Patent Owner Yangtze Memory Technology Company, Ltd.'s ("YMTC's" or "Patent Owner's") U.S. Patent No. 10,886,291 ("’291 Patent" (Ex. 1001)), because it fails to show a reasonable likelihood of prevailing as to any claim. Petitioner's only ground fails because the sole prior art reference relied upon does not disclose or render obvious the independent claim. Indeed, Petitioner, Micron Technology, Inc., fails to even assert that the prior art discloses or renders obvious each limitation of the claims.

The ’291 Patent describes a novel joint opening structure for a three-dimensional memory device, designed to improve electrical continuity between a top and bottom stack of layers including oxide/nitride layer pairs. The ’291 Patent describes forming the joint opening structure on top of a first stacked layer 2 (orange), by forming a first insulating connection layer 3 (purple) and a conductive third channel structure 14 (red) that is wider than the through hole in the first stacked layer 2.

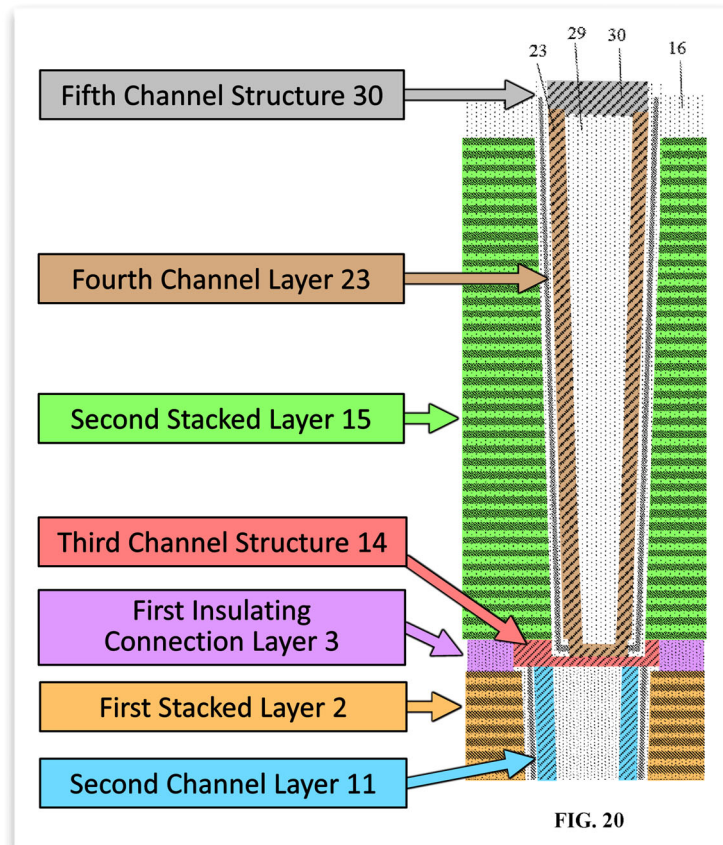


Ex. 1001, Fig. 11B,¹ 9:26-27, 9:61-62, 10:30-39, 11:31-33, 12:59-64, 21:8-10; Ex. 2006 (“Khatri”) ¶44. The conductive third channel structure 14 (red) extends electrical contact from both conductive first channel structure 6 (above in green) and conductive second channel layer 11 (above in blue). Ex. 1001, 10:30-39, 11:25-44, 11:45-12:23, 12:59-64, 19:40-43; Khatri ¶44. To further form the joint opening structure to facilitate electrical connection between a first stacked layer 2 (below in orange) and a second stacked layer 15 (below in green), the second stacked layer 15 is *disposed on* the conductive third channel structure 14 (below in red).

¹ Annotations to figures are added by Patent Owner unless stated otherwise.



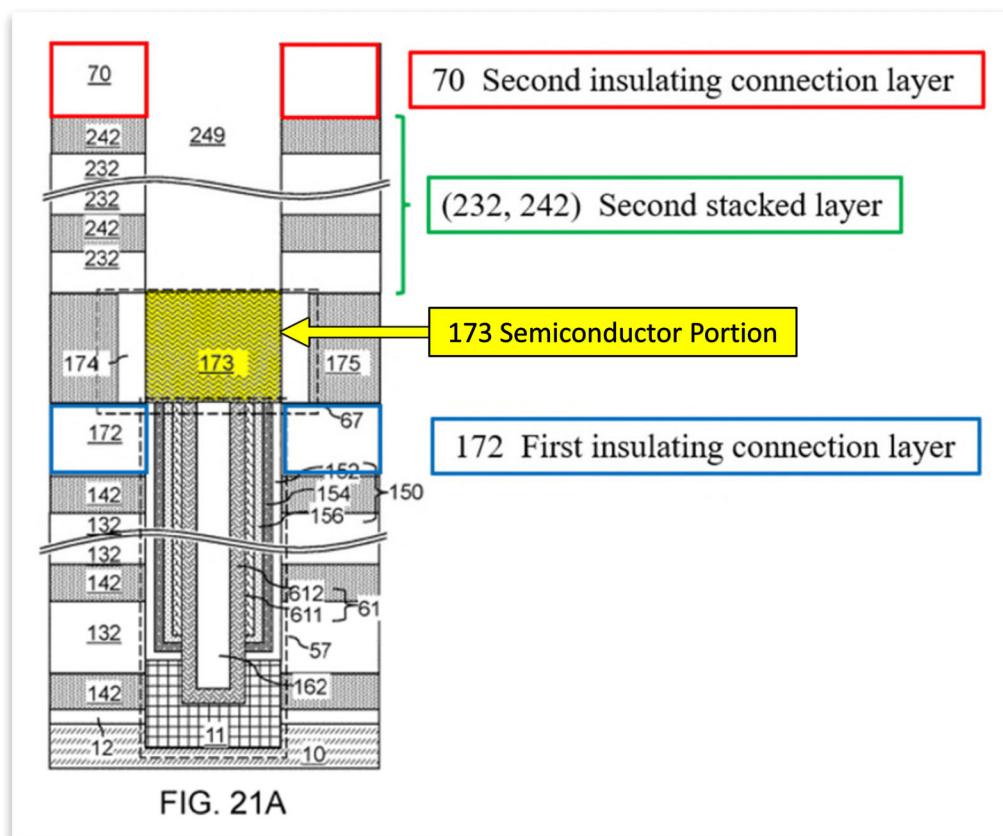
Ex. 1001, Figs. 12, 13, 13:11-20; Khatri ¶45. Next, as seen above in Figure 13, a through hole 18 is formed through the second stacked layer 15 (green) to the third channel structure 14 (red). Ex. 1001, 13:11-21, 13:38-42, Fig. 13; Khatri ¶45. Further, conductive fourth channel layer 23 (below in brown) is deposited into through hole 18 and conductive fifth channel structure 30 (below in grey) is added on top to complete the electrical connection through the two stacks. Ex. 1001 at 14:44-58, 15:12-14, 15:24-31; Khatri ¶46.



Ex. 1001, Fig. 20. As such, a joint opening structure is formed in the dual-stack 3D memory that connects conductive channel structures formed in through holes of two separate stacks. *Id.* at 15:24-31, 13:57-59, 12:59-62, 12:8-10; Khatri ¶46. Because the third channel structure 14 is wider than and covers the first through hole below it, the third channel structure 14 acts as an alignment pad that will necessarily overlap with the through hole in the second stack to provide a margin for alignment of the two through holes. *See* Ex. 1001, 32:17-26, 1:57-59, 1:63-66, 13:42-45; Khatri ¶47. In other words, the components of the joint opening structure limit “top-bottom aperture error” by providing a landing pad for connection between stacks (e.g., third channel structure 14 (red)), resulting in “an efficient process capability control, a

simplified process complexity, and a reduced cost.” Ex. 1001, 32:17-26, 1:57-59, 1:63-66, 13:42-45; Khatri ¶47.

The Petition presents one ground of purported invalidity based on Costa (Ex. 1005). It fails because Costa does not teach or suggest a “second stacked layer *disposed on* the third channel structure,” as recited in independent claim 11 (Limitation [11.H] by Petitioner’s nomenclature). Instead, as shown below in Figure 21A, Costa’s “second stacked layer” (which the Petition identifies as second alternating stack 232, 242; green) *is not disposed on* the “third channel structure” (which the Petition identifies as semiconductor portion 173; yellow).



Costa, Fig. 21A (red, blue, and green annotations added by Petitioner at Pet. 56; yellow annotations added by Patent Owner); Khatri ¶¶73-81.

Tellingly, the Petition does not even assert that Costa's second alternating stack 232, 242 is "disposed on" the semiconductor portion 173, as claimed in an apparatus, nor does it assert that such an arrangement would have been obvious. *See* Pet. 92, 54-57. Petitioner does not even make these bare-bone assertions simply because Costa cannot substantiate them. As clearly shown in Figure 21A, Costa's "second stacked layer" does not laterally overlap with semiconductor portion 173. Consequently, Costa's "second stacked layer" is not "disposed on" the semiconductor portion 173, which Petitioner identifies as the "third channel structure."

Because independent claim 11 requires a "second stacked layer disposed on the third channel structure" and Costa fails to disclose that arrangement—and Petitioner does not even contend it would have been obvious to modify Costa in some way to meet this limitation—Petitioner fails to show a reasonable likelihood of success for any challenged claim. As a result, the Board should deny institution.

II. Background

A. Only Claims 11, 12, and 14-19 Are At Issue

Although Petitioner presents one ground based on Costa to challenge claims 1-5, 8-9, 11-12, and 14-19 of the '291 Patent (Pet. 9), YMTC disclaimed claims 1-5

and 8-9. Ex. 2008 (Disclaimer in Patent Under 37 C.F.R. § 1.321(a)); Khatri ¶¶35-37. As a result, only independent claim 11 and its dependent claims 12 and 14-19 are at issue. Since Petitioner exclusively relies on Costa in its challenges to independent claim 11, if the Board finds that Costa fails to disclose or suggest at least one limitation present in claim 11 based on Petitioner's arguments, then the Board should deny institution.

B. Technical Background

Memory cells are the fundamental building blocks of digital storage devices, responsible for storing and retrieving data in electronic systems. Khatri ¶38. Each memory cell is capable of holding at least a bit of information, each bit represented as either a 0 or a 1, through the manipulation of electrical quantities such as charges. *Id.* In traditional, two-dimensional memory, often referred to as planar memory, these cells exist in a flat, horizontal layout. Ex. 1009 pt. 1, 38-40; Khatri ¶38. However, as the demand for higher storage capacities and improved performance has grown, the limitations of two-dimensional memory, such as limited scalability, lithography/patterning, random dopant fluctuations, capacitive coupling interference, reduced number of electrons, and increased power consumption, have driven the development of more advanced memory architectures, such as three-dimensional memory. Ex. 1009 pt. 1, 150; Khatri ¶38.

Three-dimensional NAND (3D NAND) memory cells represent a significant advancement in data storage technology, offering increased storage capacity and efficiency compared to traditional two-dimensional memory. *See* Ex. 1011, 120-121; Khatri ¶39. Unlike their two-dimensional counterparts, 3D NAND memory cells can be stacked vertically, allowing for greater density and storage capacity within the same physical footprint. *See* Ex. 1011, 120-125; Khatri ¶39.

These 3D stacks can comprise alternating layers of insulating and charge-trapping materials, such as silicon oxide and silicon nitride, which allow the individual memory cells to remain isolated from each other. *See* Ex. 1011, 127-128; Khatri ¶40. These layers are penetrated by channel holes, which allow for the creation of 3D NAND strings and interconnectivity between the layers, allowing for the reading and writing of data to the memory cells. *See* Ex. 1011, 121-123; Khatri ¶40. The creation of channel holes is a critical step in the fabrication of 3D NAND memory, as the channel holes must be precisely aligned and uniformly etched to ensure optimal performance and connectivity between each stack. *See* Ex. 1011, 121-123, 130; Khatri ¶40.

C. The '291 Patent (Ex. 1001)

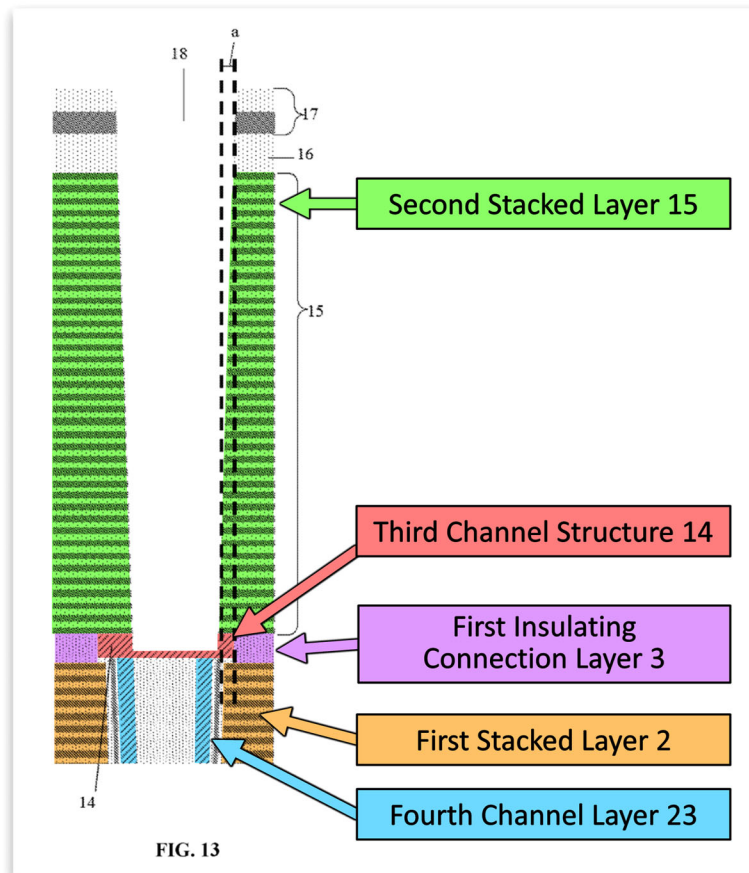
The '291 Patent, filed on January 5, 2021 and claiming priority to March 8, 2017, relates to “the field of semiconductor technology, and more particularly, to joint opening structures of three-dimensional [] memory devices.” Ex. 1001 at 1:17-

20; Khatri ¶41. In particular, the disclosure of the '291 Patent addresses issues that arise because “three-dimensional [] memory devices . . . keep scaling more oxide/nitride [] layers.” Ex. 1001 at 1:24-26; Khatri ¶41. As the number of layers increases, it becomes more difficult to use a single etching process to form the channel holes (i.e., akin to drilling a hole through the many layered three-dimensional memory), both because increasing the depth of the channel holes makes the etching process “exponentially slower” and because it increases the risk of improperly formed holes, which typically are wider at the top and narrower at the bottom. Ex. 1001 at 1:26-35; Khatri ¶42.

To address this issue, the '291 Patent discloses three-dimensional memory devices made from two stacks of oxide/nitride layers. Ex. 1001, 1:45-56, 1:59-63; Khatri ¶43. Each stack of nitride/oxide layers includes a channel hole, also called a through hole. Ex. 1001, 1:45-49, 1:61-63; Khatri ¶43. The stacks can then be placed one atop the other with the through holes aligned. Ex. 1001, 1:66-2:5; Khatri ¶43. Specifically, the '291 Patent discloses structures for such three-dimensional memory devices that allow the stacks to be placed atop each other while improving electrical connectivity between the stacks. Ex. 1001, 1:57-59, 1:63-66, 1:43-2:5; Khatri ¶43.

One embodiment disclosed by the '291 Patent involves forming the second stacked layer “on the third channel structure.” Ex. 1001, 13:11-20; Khatri ¶45. The second through hole is then formed to penetrate the second stacked layer 15 and

extend into the surface of the third channel structure, allowing for electrical connectivity. Ex. 1001, 13:38-45; Khatri ¶45. This can be seen in Figure 13 below, in which the second stacked layer 15 (green) is first formed on third channel structure 14 (red) before a through hole 18 is formed through the second stacked layer 15.



Ex. 1001, Fig. 13, 13:11-21, 13:38-45; Khatri ¶45.

D. Prosecution History

For brevity, YMTC does not address the prosecution history in this Preliminary Response as it does not impact any of the arguments herein. YMTC's decision not to address the prosecution history here should not be understood as

agreement or acquiescence with the statements made by Petitioner regarding the prosecution history. *See* Pet. 18-20; Khatri ¶48.

E. Person of Ordinary Skill in the Art

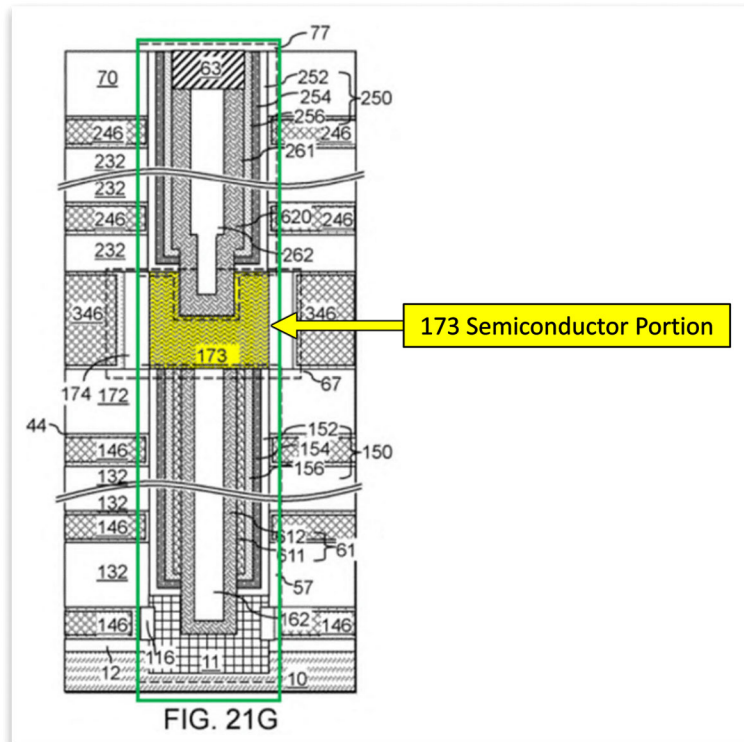
Petitioner asserts that a person of ordinary skill in the art (“POSITA”) in the field of the ’291 Patent “would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).” Pet. 24; Khatri ¶¶31-33. Petitioner also asserts that this “POSITA would have been aware of and generally knowledgeable about 3D NAND’s structure, how it is manufactured, and its component parts.” Pet. 24; Khatri ¶33.

YMTC takes no position on the level of ordinary skill in the art in this Preliminary Response only, as Petitioner has failed to establish a reasonable likelihood of prevailing under any reasonable definition for a POSITA. Khatri ¶34.

F. Costa (Ex. 1005)

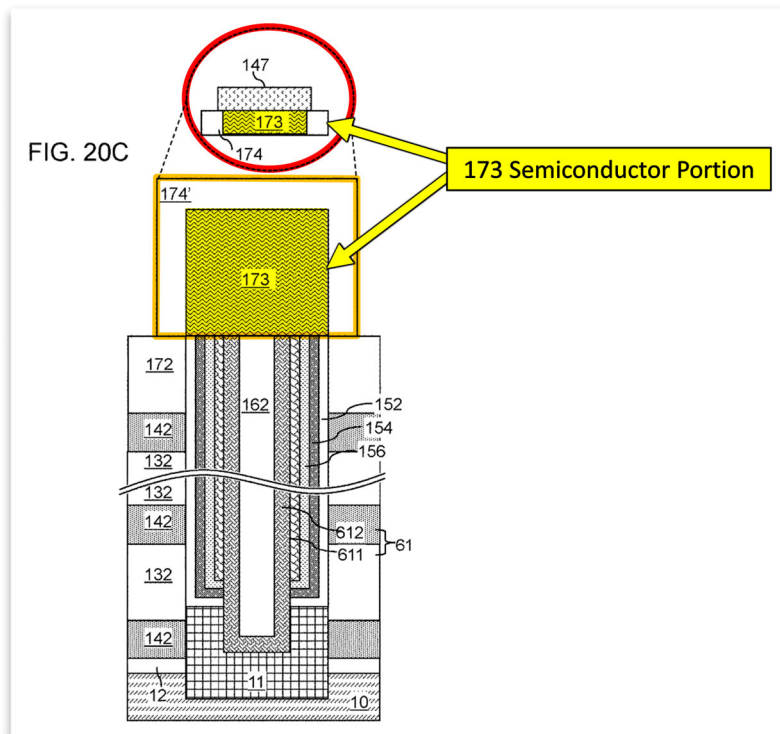
Costa is a U.S. Patent Publication titled “Three-Dimensional Memory Devices Containing Inter-Tier Dummy Memory Cells and Methods of Making the Same,” which was filed on February 28, 2017 and published on June 28, 2018. Costa discloses a memory device with two stacks of alternating insulation and electrically

conductive layers. Costa, Abstract; Khatri ¶49. Costa further discloses a “joint-level doped semiconductor portion 173” (yellow below) as part of a vertical memory channel (green below) that electrically connects the first and second stacks, as shown in Figure 21G.



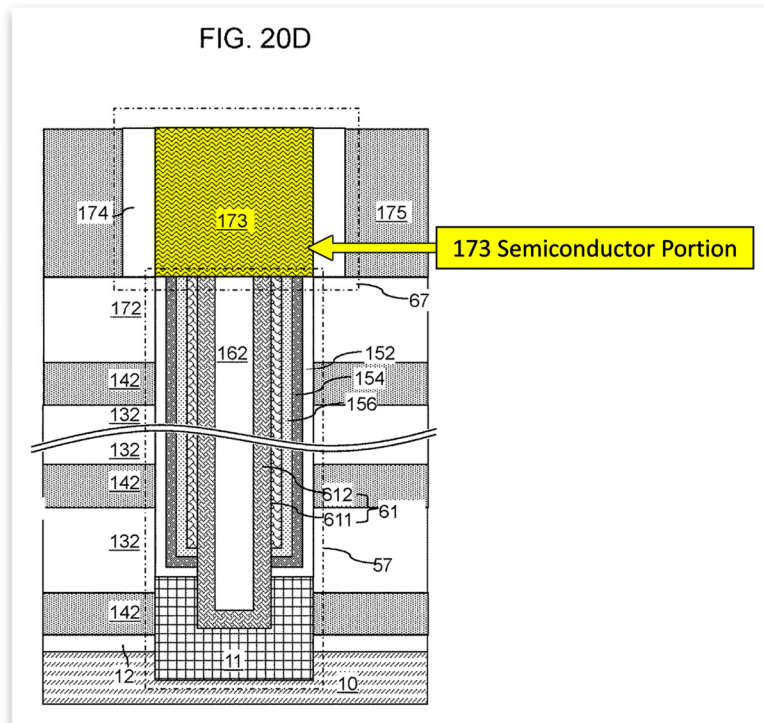
Costa, Fig. 21G (green annotations by Petitioner at Pet. 29; yellow annotation added by Patent Owner), ¶¶272-280; Khatri ¶49. However, Costa describes several processing steps before reaching the final configuration shown above. During the manufacturing of the 3D memory, a “joint-level doped semiconductor layer 173L” is placed atop the first stack and oxidized, either with a mask 147 (in red circle below) or without mask 147 (in orange square below), as seen below in Figure 20C. Ex. 1005, ¶¶264-266; Khatri ¶50. During the oxidation process, the exposed

surfaces of portion 173 are converted into dielectric oxide material (174 or 174') and the lateral dimension of portion 173 is reduced, as seen below in Figure 20C. Ex. 1005, ¶266; Khatri ¶50.



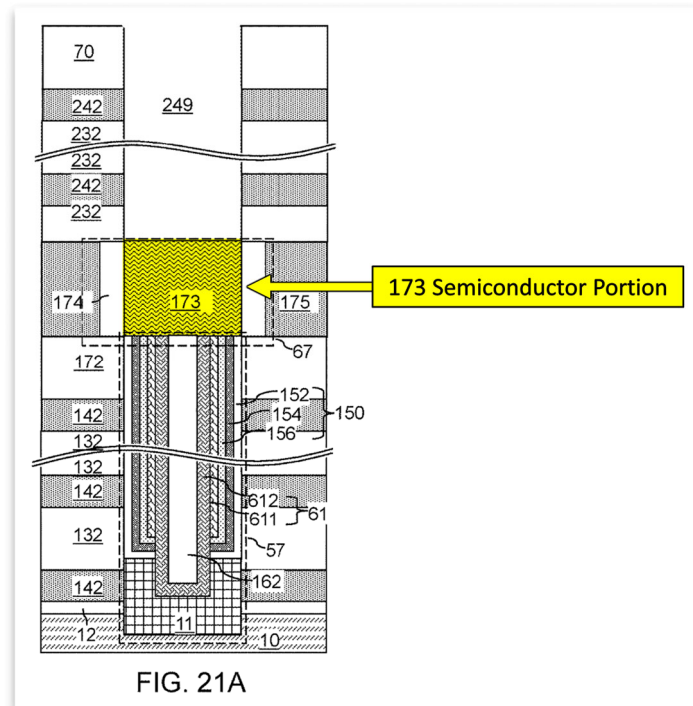
Costa, Fig. 20C.

Next, the top portion of the dielectric material is removed to form an annular dielectric spacer 174, and joint-level spacer material 175 is then deposited over the first tier-structure and around semiconductor portion 173 and dielectric spacer 174. Ex. 1005, ¶266-268, Fig. 20D; Khatri ¶51.



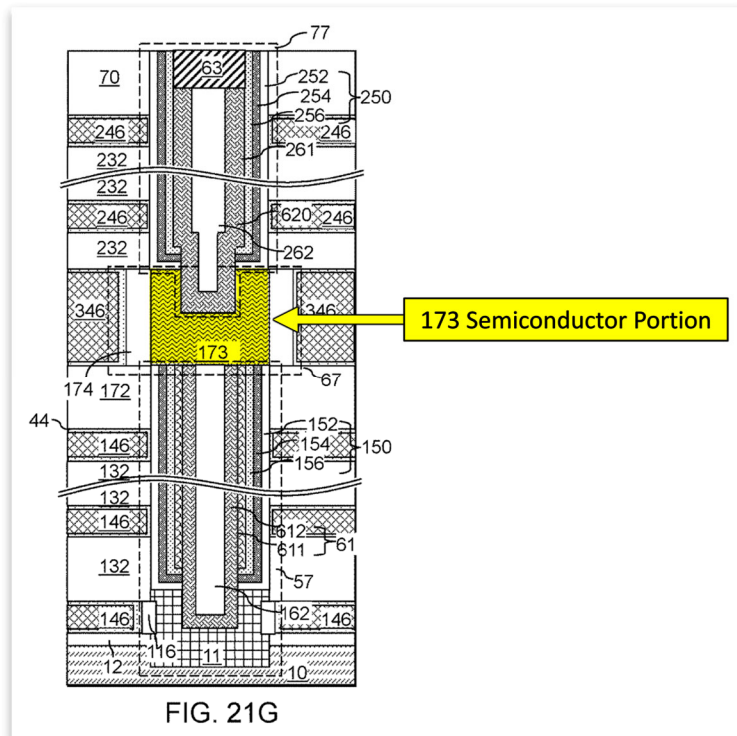
Costa, Fig. 20D.

Next, second tier structure 232, 242 is formed above layers 173, 174, and 175, and a second-tier memory opening 249 is formed over the semiconductor portion 173 exposing the semiconductor portion 173. *Id.* ¶¶272, 190, Figs. 10A, 10B, 21A; Khatri ¶52.



Costa, Fig. 21A.

As seen below in Fig. 21G, additional processing steps are performed to fill in second-tier memory opening 249 with multiple layers, including second inner semiconductor channel layer 622, and drain region 63 is formed into a recess etched into second dielectric core 262. *Id.* ¶¶274-275, 212, 277; Khatri ¶53.



Costa, Fig. 21G.

G. Claim Construction

The prior art relied on in the Petition fails to disclose the subject matter of the challenged claims under any reasonable construction, including plain and ordinary meaning.² Khatri ¶¶54-59.

In Petitioner's claim construction section, Petitioner alleges "the '291 Patent's claims do not require further construction and should receive their plain and ordinary meaning." Pet. 21; Khatri ¶¶60. For claim 4—not at issue in this Preliminary

² Patent Owner reserves the right to advocate for claim constructions if the Board institutes review.

Response—Petitioner states that “Micron applies YMTC’s claim interpretation that is evident from its infringement contentions in the Co-Pending Litigation.” Pet. 21-24; Khatri ¶¶60. Petitioner represents that all other claims, including claim 11 and its dependents at issue in this Preliminary Response, “should receive their plain and ordinary meaning.” Pet. 21; Khatri ¶¶60.

However, when analyzing the ’291 Patent claims, Petitioner and its expert argue that “the ’291 Patent does not limit ‘on’ to ‘directly contacting’ (*i.e.*, there can be intervening layers).” Pet. 43 (citing Ex. 1001, 8:3-12); Banerjee (Ex. 1003) ¶¶171; *see also* Pet. 33-34, 56; Banerjee ¶¶136, 171; Khatri ¶¶61.

The inventors of the ’291 Patent acted as their own lexicographers and defined the term “on” in the specification:

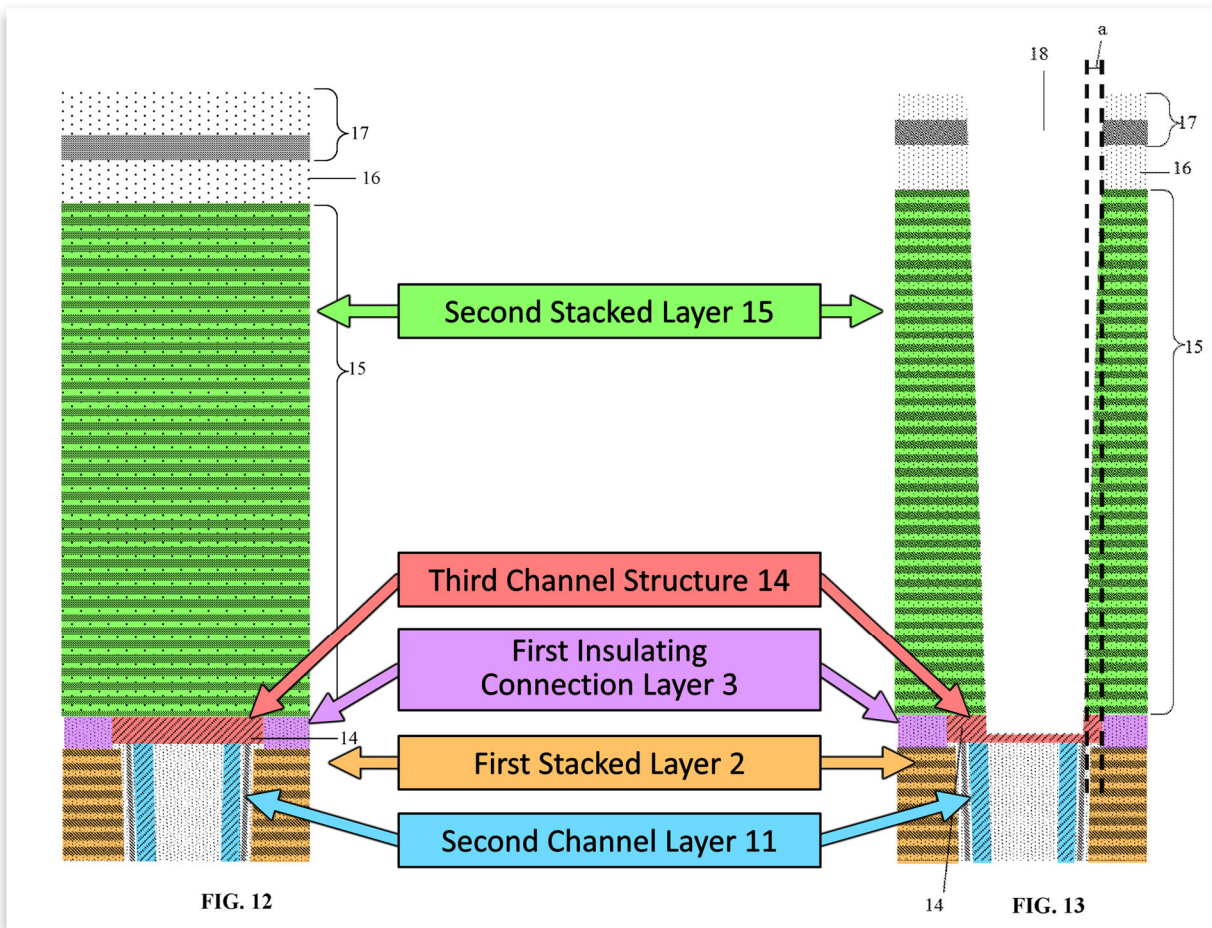
It should be readily understood that the meaning of “on,” “above,” and “over” in the present disclosure should be interpreted in the broadest manner such that **“on” not only means “directly on” something but also includes the meaning of “on” something with an intermediate feature or a layer therebetween**, and that “above” or “over” not only means the meaning of “above” or “over” something but can also include the meaning it is “above” or “over” something with no intermediate feature or layer therebetween (*i.e.*, directly on something).

Ex. 1001, 8:3-12 (emphasis added);³ *see Thorner v. Sony Computer Ent. Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012) (“To act as its own lexicographer, a patentee must clearly set forth a definition of the disputed claim term other than its plain and

³ All emphasis added unless stated otherwise.

ordinary meaning” and “clearly express an intent to redefine the term”) (citation omitted); Khatri ¶62. Here, the '291 Patent inventors offset the term “on” with quotations, and clearly expressed intent to redefine it by stating it “not only means ... but also includes the meaning of” See Ex. 1001, 8:3-12; *Sinorgchem Co., Shandong v. Int’l Trade Comm’n*, 511 F.3d 1132, 1136 (Fed. Cir. 2007) (citation omitted) (recognizing a term “set off by quotation marks” is “often a strong indication that what follows is a definition”); see, e.g., *Abbott Lab’ys v. Andrx Pharms., Inc.*, 473 F.3d 1196, 1210 (Fed. Cir. 2007) (holding ‘as used herein, means’ as definitional); *Meds. Co. v. Mylan, Inc.*, 853 F.3d 1296, 1306 (Fed. Cir. 2017) (holding ‘refers to’ and ‘as defined herein’ as definitional); *Kyocera Senco Indus. Tools Inc. v. Int’l Trade Comm’n*, 22 F.4th 1369, 1378 (Fed. Cir. 2022) (holding ‘referred to herein’ as definitional); Khatri ¶62. Based on this lexicography, “on” should be construed as “directly on or on with an intermediate feature or layer therebetween.” Khatri ¶62.

The specification is consistent with and supports the lexicography in the '291 Patent. As discussed above, the specification shows an example of a “second stacked layer ... formed on the third channel structure.” Ex. 1001 at 13:11-17; Khatri ¶63. It explains that this arrangement is “shown in FIG. 12.” Ex. 1001 at 13:11-17; Khatri ¶63. As can be seen in Figure 12 below on the left, the second stacked layer 15 (green) is disposed directly on the third channel structure 14 (red).



Ex. 1001, Figs. 12, 13; Khatri ¶63. As seen in Figure 13 above on the right, after the creation of the “second through hole 18”, the second stacked layer 15 (green) is still on the third channel structure 14 (red). Khatri ¶63.

Further, there is no basis for asserting—and Petitioner does not assert—that “on” should be interpreted more broadly to simply mean “over.” The specification and lexicography therein do not suggest that “on” means “over.” Ex. 1001, 8:3-12; Khatri ¶64. To the contrary, the specification distinguishes “on” and “over” by providing distinct lexicography for each term. Ex. 1001, 8:3-12 (“[O]ver’ not only means the meaning of ... ‘over’ something but can also include the meaning it is ...

‘over’ something with no intermediate feature or layer therebetween (i.e., directly on something)”); Khatri ¶64. If “on” meant the same thing as “over,” a first element that is higher than a second element could be interpreted as “on” the second element (e.g., the top of the dome of the U.S. Capitol could be interpreted as “on” the USPTO’s James Madison Building). Khatri ¶65; *see* Ex. 1001, 8:3-12; *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 801, 810 (Fed. Cir. 2021) (“It is highly disfavored to construe terms in a way that renders them void, meaningless, or superfluous.”).

To be clear, YMTC does not believe any terms require construction for the Board to deny institution. To the extent that the Board does not agree with the above lexicography, Patent Owner submits that the Petition still fails if the claim term “on” receives its plain and ordinary meaning—e.g., physically in contact with or directly on top of with intervening objects therebetween. Khatri ¶66.

III. Claims 11-12 and 14-19 Are Not Obvious Over Costa

The Petition is fatally flawed because Petitioner failed to demonstrate that Costa teaches each and every claim element of independent claim 11.⁴ As a result,

⁴ The Board cannot institute an IPR on disclaimed claims 1-5 and 8-9. *See* Ex. 2008; 37 C.F.R. § 42.107(e); *Intuitive Surgical, Inc. v. Ethicon LLC*, IPR2018-01248, Paper 7 at 2 n.1, 9-10 (PTAB Feb. 7, 2019).

Petitioner similarly fails to meet its burden with respect to claims 12 and 14-19, each of which depend from claim 11. Khatri ¶¶67-68.

A. Costa Does Not Disclose “A Second Stacked Layer Disposed On The Third Channel Structure” (Limitation [11.H])

Claim 11 recites, in part, “[a] joint opening structure of a three-dimensional (3D) memory device, comprising ... a second stacked layer disposed on the third channel structure.” Ex. 1001, 45:52-53, 46:4-5; Khatri ¶69. Petitioner addresses limitation [11.H] with a single sentence: “This limitation is present in [1.G] and Costa discloses it for the same reasons.” Pet. 92. But limitation [11.H] is not present in limitation [1.G]. The two limitations are different and the Petition does not address the structure claimed in apparatus limitation [11.H] when addressing method limitation [1.G]. Khatri ¶70.

1. A “Joint Opening Structure” With “A Second Stacked Layer Disposed On The Third Channel Structure” (Limitation [11.H]) Is Not Present In Method Limitation [1.G]

Method limitation [1.G] and apparatus limitation [11.H] are not coextensive. Method limitation [1.G] recites “forming a second stacked layer and forming a second insulating connection layer on the first insulating connection layer.” Ex. 1001, 43:43-44:10; Khatri ¶71. Method limitation [1.G] does not require that the “second stacked layer” is “disposed on the third channel structure,” as recited in apparatus limitation [11.H]. Ex. 1001, 43:43-44:10, 45:52-46:20; Khatri ¶71.

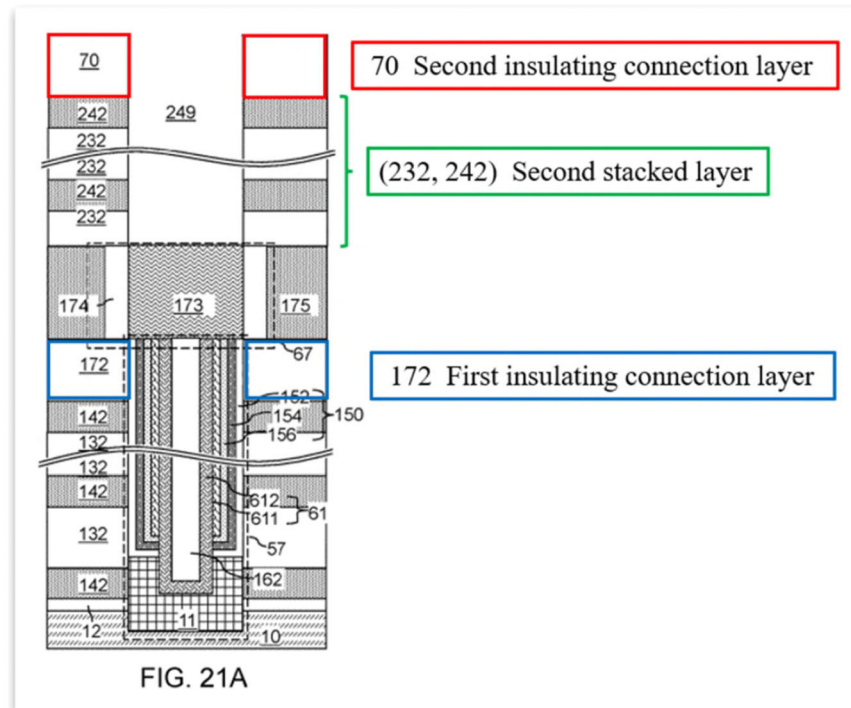
The Petition's fatal flaw is that it ignores the distinction between the method and apparatus claims, citing steps in Costa's method but ignoring the final apparatus that Petitioner alleges meets the claim limitations. Rather than method claim 1 which simply recites “[a] *method of forming* a joint opening structure” and limitation [1.G] which recites the method step of “forming a second stacked layer ... on the first insulating connection layer,” the apparatus claim 11 recites “[a] *joint opening structure* of a three-dimensional (3D) memory device” and limitation [11.H] recites the required feature of “a second stacked layer disposed on the third channel structure.” Ex. 1001, 43:43-44:10, 45:52-53, 46:4-5, 45:52-46:20; *see* Pet. 70 (Petitioner recognizing the method-apparatus distinction in the context of claim 1, stating that any argument regarding Costa's “finished configuration is irrelevant” to the method step in limitation [1.K]); Pet. 90 (recognizing the “joint opening structure” recited in [11.PRE] and that “claim 1 recites a method for forming the same”); Khatri ¶72. The Petition points to Costa to address “forming a second stacked layer” as recited in method claim limitation [1.G], while ignoring the distinctive limitation “a second stacked layer disposed on the third channel structure” as recited in apparatus claim limitation [11.H].

2. Petitioner's Cited Costa Disclosure For Method Limitation [1.G] Does Not Disclose A “Joint Opening Structure” With “A Second

**Stacked Layer Disposed On The Third Channel Structure”
(Limitation [11.H])**

Petitioner's ground addressing apparatus claim 11 fails because it relies exclusively on Costa, and Costa does not teach “a second stacked layer disposed on the third channel structure” as recited in limitation [11.H]. Instead, as explained below, Costa's “second stacked layer” (i.e., second alternating stack 232, 242 according to Petitioner) is not “disposed on” the “third channel structure” (i.e., semiconductor portion 173 according to Petitioner). Khatri ¶73.

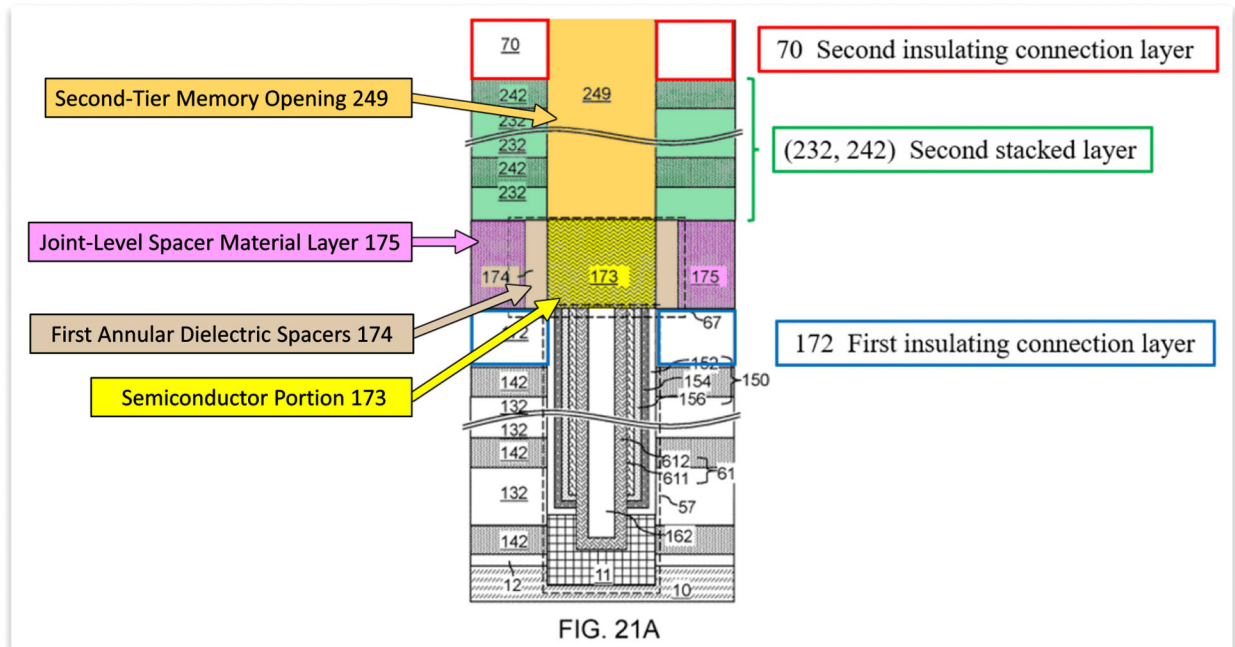
Petitioner addresses apparatus limitation [11.H] by referring back to method limitation [1.G] (Pet. 92), but Petitioner's reliance on Costa to address method limitation [1.G] fails to address how the “second stacked layer” is “disposed on the third channel structure,” as recited in apparatus limitation [11.H]—mainly because Costa does not disclose it. To address limitation [1.G], Petitioner relies on Costa's Figure 21A reproduced below, stating that Costa discloses “forming a second stacked layer (‘second alternating stack’ 232, 242) [in green below] and forming a second insulating connection layer (‘insulating cap layer 70’) [in red below] on the first insulating connection layer (‘first insulating cap layer 172’) [in blue below].” Pet. 55.



Costa, Fig. 21A (Petitioner's annotations at Pet. 56); Khatri ¶74.

Tellingly, the Petition does not even assert that Costa's second alternating stack 232, 242 is "disposed on" the semiconductor portion 173, as claimed in apparatus limitation [11.H]. *See* Pet. 54-57; Khatri ¶¶75-76. Instead, Petitioner appears to argue that Costa discloses method limitation [1.G]—which recites "forming a second stacked layer and forming a second insulating connection layer on the first insulating connection layer"—by forming a second stacked layer ("second alternating stack" 232, 242; green below) above the third exemplary structure's single joint-level doped semiconductor portion 173 (what Petitioner calls the "third channel structure" (Pet. 46), yellow below), annular dielectric spacers 174 (brown below), and joint-level spacer material layer 175 (pink below). *See* Pet. 55-

56 (citing Costa ¶¶270 (noting that processing steps shown in Figures 8A, 8B, 10A, and 10B apply to the third exemplary structure), 178 (noting second alternating stack (232, 242) is formed on the top surface of the joint-level material layers (175, 176, 177) as in Figures 8A and 8B)); Khatri ¶77.



Costa Fig. 21A (red, blue, and green annotations added by Petitioner at Pet. 56; orange, pink, brown, and yellow annotations added by Patent Owner); *see* Costa ¶75 (noting Figure 21A illustrates the third exemplary structure after forming second-tier opening 249 (above in orange) as depicted in Figures 10A and 10B). Petitioner relies on Figure 21A, which depicts the step of forming a through hole (above in orange) through “second alternating stack” 232, 242 (above in green). Pet. 56; Khatri ¶77. Later in the Petition, for a different limitation (i.e., not [1.G] or [11.H]), Petitioner depicts Figure 21A showing a “second memory through hole in the second

stack” above the semiconductor portion 173. Pet. 59; *see also id.* at 30 (Petitioner addressing [1.PRE] by describing how Costa forms a “joint opening structure” by “etching a second memory through hole in the second stack (and forming a channel structure therein”), 90 (addressing [11.PRE] by referring to [1.PRE]). Unsurprisingly, Petitioner’s citations relying on Costa’s Figure 21A to address limitation [1.G] focus on the *process for forming* the apparatus, not on the apparatus itself. *See* Pet. 54-57; Khatri ¶78.

Petitioner’s Costa disclosure to address method limitation [1.G] does not disclose apparatus limitation [11.H], which requires a “joint opening structure” with “a second stacked layer disposed on the third channel structure.” Because claim 11 is an apparatus claim, not a method claim, the process for forming the apparatus is not relevant—the ultimate apparatus itself is. And as seen above in Figure 21A, the “second stacked layer” (i.e., 232, 242 according to Petitioner) is not “disposed on” the “third channel structure” (i.e., semiconductor portion 173 according to Petitioner). Khatri ¶79. Instead, Costa describes a second-tier memory opening 249 (in orange above) that is formed above the semiconductor portion 173, as shown in Figure 21A. Costa, at ¶¶191 (describing process of forming second-tier memory opening 249 over opening fill structure 67 as shown in Figures 10A and 10B regarding a “first exemplary structure”), 269 (joint-level memory opening fill structure 67 includes semiconductor portion 173), 270 (stating this process can be

performed for the “third exemplary structure” that Petitioner relies on), 272 (Figure 21A illustrates the third exemplary structure after formation of the second-tier memory opening 249 as shown in Figures 10A and 10B);⁵ Khatri ¶80.

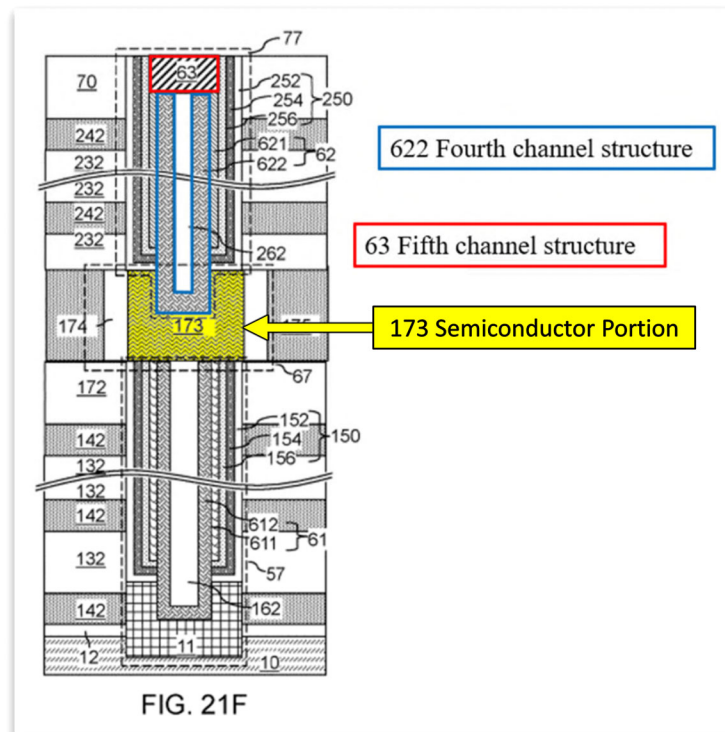
As a result, Petitioner errs in relying on Costa to disclose apparatus limitation [11.H] because it does not disclose “a second stacked layer” (i.e., 232, 242 according to Petitioner) “disposed on” the “third channel structure” (i.e., 173 according to Petitioner). Khatri ¶81. The Board should deny institution.

3. Costa Does Not Disclose A “Joint Opening Structure” With “A Second Stacked Layer Disposed On The Third Channel Structure” (Limitation [11.H])

None of the other figures of Costa disclose “a second stacked layer disposed on the third channel structure” as recited by apparatus limitation [11.H]. Khatri ¶¶82-83. Costa’s later configuration depicted in Figure 21F does not disclose it. And Costa’s final configuration in Figure 21G likewise fails to disclose limitation [11.H].

⁵ Costa has a typo in Paragraph 272 where it states that “FIG. 21A illustrate [sic] a region of the second exemplary structure at the processing steps of FIGS. 10A and 10B,” instead of the “third exemplary structure” described in the series of Figures 20A-21G. See Costa ¶¶272, 263, 71-81.

Costa’s later configuration in Figure 21F—the one Petitioner relies on for other limitations of apparatus claim 11 besides [11.H]—does not disclose “a second stacked layer disposed on the third channel structure,” as recited in limitation [11.H]. Rather than Figure 21A, Petitioner relies on the later configuration of Costa seen below in Figure 21F.



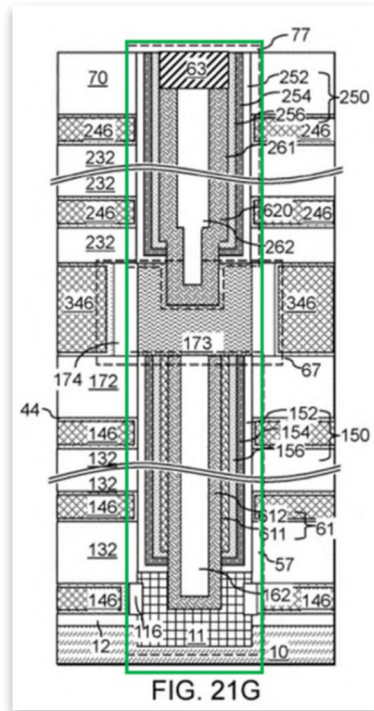
Costa, Fig. 21F (Petitioner addressing method limitation [1.K] by relying on Costa's Figure 21F as annotated at Pet. 68); Pet. 92 (Petitioner addressing apparatus limitation [11.M] by referring to method limitation [1.K]); Khatri ¶84. As seen above, numerous layers 252, 254, 256, 621, 622, and 262 are deposited in the second-tier memory opening 249 above the semiconductor portion 173, some of which establish electrical conductivity in a vertical channel. Costa ¶¶273-275, Figs

21B-21D (describing adding layers 252, 254, 256, 621, 622, and 262L into second-tier memory opening 249); 276 (describing second vertical channel 62, which includes layers 621 and 622, as conducting electrical current); 277 (describing adding drain region 63); *see also* Pet. 93 (recognizing “second-tier memory openings 249” are “filled in Fig. 21F with second memory open [sic] opening fill structures 77”). In the configuration in Figure 21F, as in Figure 21A, Costa does not disclose “a second stacked layer disposed on the third channel structure,” as recited in limitation [11.H]. Khatri ¶84.

Costa's final configuration of the third exemplary structure shown in Figure 21G below—one that Petitioner does not rely on in the Petition to address method claim 1 or apparatus claim 11—similarly fails to disclose limitation [11.H]. Figure 21G shows the iterative step of replacing both sacrificial material layers 142, 242 and joint-level spacer material layer 175 with electrically conductive layers 146, 246, 346. Costa ¶¶280 (describing Figure 21G shows the third exemplary structure after the processing steps of Figures 14A and 14B),⁶ 217-219 (describing removal

⁶ Costa has a typo in Paragraph 280 where it states that “FIG. 21G illustrates the second exemplary structure at the processing steps of FIG. 14B,” instead of the “third exemplary structure” described in the series of Figures 20A-21G. *See* Costa ¶¶280, 71-81.

of sacrificial material layers 142, 242 and joint-level spacer material layer 175), 222-224 (describing deposit of electrically conductive layers 146, 246, 346); Khatri ¶85.



Costa, Fig. 21G (annotated by Petitioner at Pet. 29 in overview of Costa). As seen in the above final configuration, Costa's "second stacked layer" (i.e., 232, 242 according to Petitioner) is still not "disposed on the third channel structure" (i.e., 173 according to Petitioner). In fact, Costa's "second stacked layer" (i.e., 232, 242 according to Petitioner) no longer exists because layer 242 has been replaced by electrically conductive layer 246. Compare Costa Fig. 21F with *id.* at Fig. 21G; Khatri ¶85. Like the prior intermediate configurations of Figures 21A and 21F, Costa's final configuration in Figure 21G fails to disclose a "second stacked layer disposed on the third channel structure," as recited in limitation [11.H].

4. Petitioner Does Not Argue Costa Renders Obvious A “Joint Opening Structure” With “A Second Stacked Layer Disposed On The Third Channel Structure” (Limitation [11.H])

Notably, Petitioner's position is that Costa discloses limitation [11.H], not that Costa renders it obvious. In particular, Petitioner argues for limitation [11.H] that “Costa discloses it,” not that Costa renders it obvious. Pet. 92; Khatri ¶86. Petitioner similarly states that Costa discloses limitation [1.G], not that Costa renders it obvious. Pet. 54-57. And Petitioner is clear in other instances when it relies on obviousness. *See, e.g.*, Pet. 92 (arguing for limitations [11.J], [11.K], and [11.M] that “Costa discloses it, *or renders it obvious*”); Khatri ¶86. Petitioner cannot change its position after filing the Petition. *See Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (“In an IPR, the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.”) (citing 35 U.S.C. § 312); *Intelligent Bio-Systems, Inc. v. Illumina Cambridge LTD., Inc.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) (“It is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement that the initial petition identify ‘with particularity’ the ‘evidence that supports the grounds for the challenge to each claim.’”) (quoting 35 U.S.C. § 312(a)(3)). And as explained above, Petitioner fails to meet its burden to show that “Costa discloses it,” i.e., limitation [11.H]. Khatri ¶86.

Any post-filing argument cannot remedy this fatal failure in the Petition. “It would be unfair,” and impermissible, “to expect the Patent Owner to conjure up arguments against its own patent and just as inappropriate for the Board to take the side of the Petitioner to salvage an inadequately expressed ground.” *Liberty Mut. Ins. Co. v. Progressive Cas. Ins. Co.*, CBM2012-00003, Paper 8 at 14 (PTAB Oct. 25, 2012).

Thus, Petitioner failed to demonstrate that the art teaches each and every claim element of independent claim 11, and the Petition is fatally flawed as a result. Khatri ¶¶87. The Board should deny institution because Costa does not disclose limitation [11.H] for the reasons above.

B. Dependent Claims 12 and 14-19 Are Not Obvious Over Costa

Because independent claim 11 is not disclosed by or rendered obvious over Costa, the Board should also deny institution of the Petition on claims 12 and 14-19, which depend from claim 11. *See Neptune Generics, LLC v. Eli Lilly & Co.*, 921 F.3d 1372, 1378 (Fed. Cir. 2019); Khatri ¶¶88.

IV. Any New Obviousness Argument Regarding Limitation [11.H] Would Be Improper And Hindsight Driven

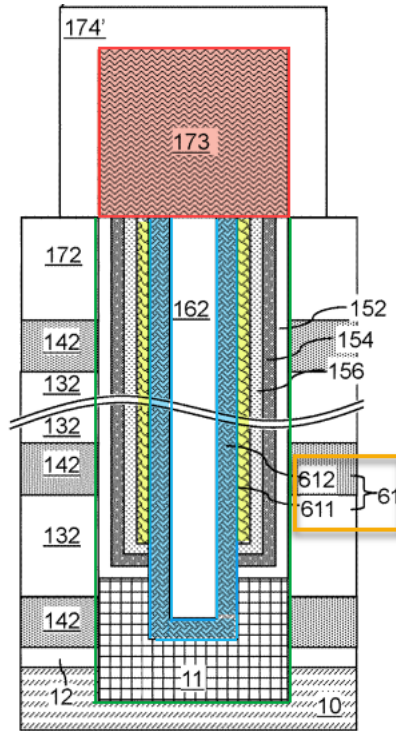
As mentioned above in Section III.A.4, Petitioner's position is that Costa discloses limitation [11.H]—not that Costa renders it obvious. Pet. 92; Khatri ¶¶86, 89. Petitioner similarly states that Costa discloses limitation [1.G], not that Costa renders it obvious. Pet. 54-57. Moreover—because Petitioner does not provide an

obviousness position for limitations [11.H] or [1.G]—Petitioner unsurprisingly presents no evidence or expert testimony to support a motivation to modify Costa to render obvious limitations [11.H] or [1.G]. Khatri ¶89.

Even if Petitioner did try to modify Costa to render obvious limitations [11.H] or [1.G] (which Petitioner did not), it would be based on hindsight.⁷ Khatri ¶¶90-92. For example, a POSITA would not modify Costa's semiconductor portion 173 to be wider than the through hole below it because Costa's semiconductor portion 173 already provides significant margin for its purpose at its current width. Khatri ¶¶90-92; *see, .* That is, semiconductor portion 173 is already wide enough to facilitate electrical contact between the upper and lower stacked layers. Khatri ¶90. As seen below in Figure 20C, the semiconductor portion 173 (red) “covers and protects the underlying first vertical semiconductor channel 61,” consisting of first

⁷ The Board should deny any attempt by Petitioner to rewrite its petition. *See, e.g., Intelligent Bio-Systems*, 821 F.3d at 1369 (“It is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement that the initial petition identify ‘with particularity’ the ‘evidence that supports the grounds for the challenge to each claim.’”) (quoting 35 U.S.C. § 312(a)(3)); *Liberty Mut, Ins. Co.*, CBM2012-00003, Paper 8 at 14. Patent Owner reserves the right to respond to any arguments to this effect.

outer semiconductor channel layer 611 (yellow) and first inner semiconductor channel layer 612 (blue). Costa ¶¶160, 265, 285; Khatri ¶90.



Costa at Fig. 20C. As illustrated above, the first-tier memory opening 149 (outlined in green) is significantly wider than the first vertical semiconductor channel 61 (layers 611 and 612) which conducts electricity through the multi-tier stack. Costa at ¶¶160 (“Each adjoining pair of a first outer semiconductor channel layer 611 and a first inner semiconductor channel layer 612 can collectively form a first vertical semiconductor channel 61 through which electrical current can flow.”), 137 (describing first-tier opening 149 formed in the first tier structure); Khatri ¶90. Moreover, Figure 20C above shows the semiconductor portion 173 covers the first

vertical semiconductor channel 61 (layers 611 and 612) by a significant margin. Khatri ¶¶90.

As seen below in Figure 21E, Costa's semiconductor portion 173 is designed to be wider than first vertical semiconductor channel 61 (orange box identifying blue and yellow layers) and second vertical semiconductor channel 62 (brown box identifying purple and green layers) to form an electrical channel between lower and upper stacks. Costa, ¶¶275-276 (describing second vertical semiconductor channel 62 for the upper stack "through which electrical current can flow"), 278 (describing second vertical semiconductor channel as "an upper portion of the vertical semiconductor channel"); Khatri ¶¶91.

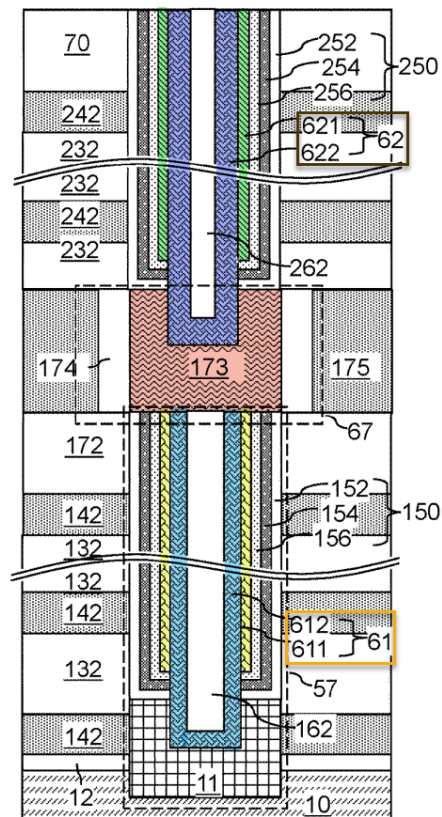


FIG. 21E

Costa, Fig. 21E. Costa even describes that “[t]he at least one doped semiconductor portion [173] ... provide[s] a robust alignment and connection scheme between each pair of a first memory opening fill structure 57 and a second memory opening fill structure 77.” Costa, ¶324; Khatri ¶¶91.

Any attempt by Petitioner to widen semiconductor portion 173 beyond the aperture of the through hole below it would be an exercise in hindsight. Khatri ¶¶91-92. Doing so would “use the challenged patent as a roadmap to reconstruct the claimed invention using disparate elements from the prior art—i.e., the

impermissible ex post reasoning and hindsight bias that KSR warned against.” *TQ Delta, LLC v. Cisco Sys., Inc.*, 942 F.3d 1352, 1361 (Fed. Cir. 2019).

In sum, Petitioner fails to make any obviousness allegations for limitations [11.Hs] and [1.G]. *See supra* Section III.A.4. Petitioner also presents no evidence or expert testimony to support a motivation to modify Costa to render obvious limitations [11.H] or [1.G]. Even if Petitioner did try to modify Costa to render obvious limitations [11.H] or [1.G] to make semiconductor portion 173 wider (which Petitioner did not), it would be based on hindsight, using the '291 Patent as a roadmap. A POSITA would not modify Costa to widen semiconductor portion 173 absent hindsight, at least because “[t]he at least one doped semiconductor portion [173] ... provide[s] a robust alignment and connection scheme between each pair of a first memory opening fill structure 57 and a second memory opening fill structure 77.” Costa, ¶324; Khatri ¶¶89-92.

V. Conclusion

For the reasons set forth above, the Board should deny the Petition for *Inter Partes* Review.

Respectfully submitted,

Dated: May 12, 2025

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CERTIFICATE OF COMPLIANCE WITH 37 C.F.R. § 42.24

I hereby certify that this Patent Owner's Preliminary Response complies with the word count limitation of 37 C.F.R. § 42.24(b)(1) because the Patent Owner's Preliminary Response contains 6,115 words using Microsoft Word's counting feature, excluding the cover page, signature block, and the parts of the Patent Owner's Preliminary Response exempted by 37 C.F.R. § 42.24(b)(1).

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 12th day of May, 2025, a true and correct copy of the foregoing **Patent Owner's Preliminary Response and all Exhibits** were served by electronic mail on Petitioner's lead and backup counsel at the following email addresses:

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