Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: May 12, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00244
Patent 10,886,291

DECLARATION OF DR. SUNIL P. KHATRI, PH.D
IN SUPPORT OF PETITIONER'S REPLY

YMTC
Exhibit 2006
Micron v. YMTC
IPR2025-00244
Ex. 2006-001

TABLE OF CONTENTS

Page

I. Introduction....1

II. Qualifications....1

III. Summary Of Materials Reviewed And Considered....13

IV. Understanding of Legal Standards....14

V. Level of Ordinary Skill in the Art....18

VI. Background....19

A. Only Claims 11, 12, and 14-19 Are At Issue....19

B. Technical Background....20

C. The '291 Patent (Ex. 1001)....21

D. Prosecution History....26

E. Costa (Ex. 1005)....26

F. Claim Construction....31

VII. Claims 11-12 and 14-19 Are Not Obvious Over Costa....36

A. Costa Does Not Disclose "A Second Stacked Layer Disposed On The Third Channel Structure" (Limitation [11.H])....37

1. A "Joint Opening Structure" With "A Second Stacked Layer Disposed On The Third Channel Structure" (Limitation [11.H]) Is Not Present In Method Limitation [1.G]....37

2. Petitioner's Cited Costa Disclosure For Method Limitation [1.G] Does Not Disclose A "Joint Opening Structure" With "A Second Stacked Layer Disposed On The Third Channel Structure" (Limitation [11.H])....39

3. Costa Does Not Disclose A "Joint Opening Structure" With "A Second Stacked Layer Disposed On The Third Channel Structure" (Limitation [11.H])....44

4. Petitioner Does Not Argue Costa Renders Obvious A "Joint Opening Structure" With "A Second Stacked Layer Disposed On The Third Channel Structure" (Limitation [11.H])....48

B. Dependent Claims 12 and 14-19 Are Not Obvious Over Costa....48

VIII. Any New Obviousness Argument Regarding Limitation [11.H] Would Be Improper And Hindsight Driven....49

IX. Conclusion....53

I. Introduction

1. I have been retained on behalf of YMTC ("YMTC"), and its counsel, Latham & Watkins, LLP, to provide expert opinions relating to U.S. Patent 10,886,291 ("Asserted Patent" or "'291 Patent") in connection with Micron's Petition for *inter partes* review. I am personally knowledgeable about the matters stated herein and am competent to make this declaration.

2. I am being compensated for my time at my standard hourly rate of $800 per hour.

3. This declaration, including the exhibits hereto and cited materials, identifies my opinions to date, although I may provide further testimony and opinions if asked to testify in court or at a deposition. I also reserve the right to supplement or amend my opinions, as well as the bases for those opinions, if I receive additional relevant information or to respond to opinions offered by other experts in this case. I may rely on demonstrative exhibits, including pictures, figures, and drawings that appear in this declaration and the referenced exhibits and materials.

II. Qualifications

4. I have over thirty-five years of experience with electronics, electrical engineering, and computer engineering. A copy of my latest curriculum vitae (CV)

is attached hereto as Ex. 2007 and provides further details regarding my background and qualifications.

5. During my career, I have acquired extensive knowledge and experience with VLSI circuits, computer architecture, testing, computer-aided design (CAD) algorithms and algorithm acceleration, logic synthesis, semiconductor memory, redundancy, synchronous and asynchronous circuits, and related software and hardware topics. Most relevant to the Asserted Patent my technical expertise includes extensive work with semiconductor memory devices such as DRAM, SRAM and flash. My work with semiconductor memory devices has included work on 3D integration and novel ring-based memory architectures, power and speed tradeoffs using selective body bias, architectures and circuit approaches for processing-in-memory, radiation hardening analysis for memories, the use of flash transistors for designing logic circuits (such as ternary Content-addressable Memories (CAMs), Field Programmable Gate Arrays (FPGAs), and traditional binary-valued as well as ternary-valued digital logic, secure logic circuits, analog circuits like Finite Impulse Response (FIR) filters, Discrete Fourier Transform (DFT) circuits, and in-memory mixed-signal computing architectures like Convolutional Neural Networks (CNNs)), large language models (LLMs) and clocking and source-synchronous design. I recently was awarded a research grant

by the Air Force Research Laboratory (AFRL) in Rome, NY, to conduct research in secure digital circuits using flash-based digital design approaches.

6. Another recent research grant from the National Science Foundation (NSF) will fund research on the use of flash transistors for general purpose mixed-signal arithmetic. Additionally, I have led-authored a book chapter on the use of flash transistors in novel Very Large Scale Integrated (VLSI) design applications. My MS thesis involved designing a memory interface for a multi-threaded Reduced Instruction Set Computing (RISC) microprocessor.

7. The following describes some of my relevant experience. I earned my Bachelor of Science in Electrical Engineering in 1987 from the Indian Institute of Technology, Kanpur, India. After graduating with my B.S. degree, I was a candidate for a Master of Science degree in Electrical and Computer Engineering at the University of Texas from 1987–89. At the University of Texas, I held the Microelectronics and Computer Development (MCD) Fellowship from 1987–89. I also conducted my M.S. research and wrote my thesis on the design of the METRIC memory interface and memory system. METRIC was one of the first super-scalar processors that was developed in the world. I earned an M.S. degree in 1989 from the University of Texas, Austin.

8. After leaving the University of Texas, I worked at Motorola Inc. from 1989–93 as a design engineer for the MC88110 reduced instruction set computing

(RISC) microprocessor team. My duties included the design of digital and analog circuitry, test logic and circuits, JTAG boundary scan design, input/output driver design, and clock phase-locked loop (PLL) logic. During my time at Motorola, I was independently responsible for the design of the factory test controller of the MC88110 microprocessor. I performed all attendant tasks in a "vertical" VLSI design methodology, which included high-level modeling, circuit and layout design and verification, as well as global and detailed routing. I also helped in the design of the Translation Lookaside Buffer (TLB) unit, which included a static random-access memory (SRAM) block.

9. In 1999, I earned a Doctor of Philosophy degree in Electrical Engineering and Computer Sciences from the University of California, Berkeley. While at Berkeley, I held the California Microelectronics (MICRO) Fellowship in 1993.

10. I joined the faculty at the University of Colorado, Boulder, in 2000 as an Assistant Professor of Electrical and Computer Engineering. At the University of Colorado my research focused on VLSI logic design automation, VLSI layout design automation, and VLSI design methodologies to address Deep Submicron (DSM) issues such as crosstalk and power.

11. I joined the faculty at Texas A&M University in 2004 as an Assistant Professor in Electrical and Computer Engineering. In 2010 I was promoted to

Associate Professor in Electrical and Computer Engineering. In 2015, I was promoted to full Professor in Electrical and Computer Engineering. My research focuses on three primary areas: the first is computer systems, including computer architecture from the circuits up, and algorithm acceleration using GPUs, FPGAs and custom ICs. The second is logic and its applications, while the third area consists of interdisciplinary extensions of the first two. Some specific recent research topics include circuit design using floating gate (flash) devices, wireless power delivery and battery-less electronic systems, machine learning architectures, secure computing approached from both a hardware and software perspective, a formal framework for designing and verifying cryptographic hash functions, and extreme high-speed serial interfaces for Artificial Intelligence / Machine Learning (AI/ML) systems such as those used in Large Language Models (LLMs) like ChatGPT. One of my new focus areas is intelligent and secure computing viewed from the hardware (circuit) as well as the software levels. I have conducted research on tamper-proof memory techniques, as well as multi-row read architectures for SRAM, DRAM and flash memory arrays.

12. At Texas A&M I teach classes that cover memories extensively, featuring thorough discussion of sense amplifiers, row and column decoders, and different types of memory circuits. For example, in Electrical and Computer Engineering (ECEN) 752 "Advances in VLSI Circuit Design," a graduate level

course, I cover all aspects of VLSI design, including memory design for various types of memories. In this course, (and also in ECEN 449/749 "Microprocessor System Design,"), I cover memories, including flash memories, the design of flash memory cells, the organization of memories into multiple banks, and the division of data across multiple banks of memory, as well as other design techniques that can be used to optimize and manage memories. The ECEN 449/749 course is attended by both undergraduate (ECEN 449) and graduate (ECEN 749) students. In ECEN 454 "Digital Circuit Design," a senior undergraduate course, I cover circuit design techniques for memory in detail. The Ph.D. thesis dissertation topic for 3 of my current Ph.D. students covers the use of flash memory transistors for analog and digital applications. The Ph.D. thesis of one of my recent doctoral students dealt with the use of flash transistors to design logic circuits. The research of a recent M.S. student entailed a new ring-based source synchronous architecture for 3D DRAM technologies, which has been published at a conference and in a journal and is being submitted for dissemination as a research monograph. In the past, I have conducted research into new topologies for efficient memory redundancy as part of a course project for my graduate course.

13. Since 2000, I have earned at least 24 research contracts from funders including Intel, the National Science Foundation, the National Security Agency, Altera Corporation, the National Center for Atmospheric Research, National

Semiconductor Corporation, and several private sources. The total amount for these research grants is at least $17.53 million, of which my portion is at least $2.85 million.

14. I have a total of over 289 peer-reviewed publications. Among these papers, five received a best paper award, while seven others received best paper nominations (including one journal best paper nomination). An additional six journal papers and three conference paper are currently undergoing peer review. I have co-authored nine research monographs, one edited research monograph, and four book chapters. Additionally, I have seven awarded U.S. Patents (two of which were filed during my tenure at Texas A&M), two filed provisional U.S. Patents, and another U.S. Patent which is currently under review and was also submitted during my tenure at Texas A&M. I have co-authored one invited journal paper and 13 invited conference or workshop papers (including one from Design Automation Conference (DAC) and one from Allerton). Moreover, I was invited to serve as a panelist at a conference seven times and have presented four conference tutorials. I received the "Outstanding Professor Award" in the ECE Department at Texas A&M University in 2007 and also in 2020. In 2009 and in 2019, I received a university-level and a college-level teaching award respectively, at Texas A&M. My H-index is 36 (per Google Scholar).

15. Since 2003, I have published numerous research monographs, journal papers, and conference papers on flash transistors and memory systems, as detailed in my CV attached in Appendix A. A few papers on relevant subject areas authored or co-authored by me include:

- *"Flash - A "Forgotten" Technology in VLSI Design,*" Khatri, Vrudhula, Abusultan, Bharathi, Chu, Lee, Scott, Singh, Wagle. Appears "Frontiers of Quality Electronic Design (QED)". Springer publishers, Sept 2022. Pages 67-136. Ali Iranmanesh, Ed. ISBN: 978-3-031-16344-9;
- *"Flash – An Overlooked Technology in VLSI Design,"* Khatri, Vrudhula. Monday Tutorial to be presented at the ACM/CEDA Design Automation Conference (DAC), San Francisco, CA, June 2024;
- *"A Mixed-Signal Quantized Neural Network Accelerator Using Flash Transistors,"* Scott, Lee, Khatri, Vrudhula. IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 71, no. 3, pp. 1025-1038, March 2024;
- *"An ASIC Accelerator for QNN With Variable Precision and Tunable Energy-Efficiency,"* Wagle, Singh, Khatri Vrudhula. IEEE

Transactions on Computer-Aided Design of Integrated Circuits and Systems, Jan 2024;

- *"A Digital Low Dropout (LDO) Voltage Regulator Using Pseudoflash Transistors,"* Lee, Khatri. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 31, no. 12, pp. 1960-1969, Dec. 2023;
- *"A Novel ASIC Design Flow using Weight-tunable Binary Neurons as Standard Cells,"* Wagle, Singh, Khatri, Vrudhula. IEEE Transactions on Circuits and Systems I (Regular Papers), 69(7): 2968-2981 (Sept 2022);
- *"CIDAN-XE: Computing in DRAM with Artificial Neurons,"* Singh, Wagle, Khatri, Vrudhula. Frontiers in Electronics, section Integrated Circuits and VLSI. vol. 3, Feb 2022;
- *"An Extremely Low-Voltage Floating Gate Artificial Neuron",* Scott, Khatri. 2023 IEEE International Conference on Circuits and Systems (ISCAS), May 21-25, 2023. Monterey, CA;
- *"A Novel Pseudo-Flash Based Digital Low Dropout (LDO) Voltage Regulator,"* Lee, Khatri, Vrudhula. 2023 International Symposium on Quality Electronic Design (ISQED), April 5-7 2023. San Francisco, CA;

- *"A Flash-based Digital to Analog Converter for Low Power Applications,"* Scott, Khatri. IEEE 40th International Conference on Computer Design (ICCD), October 2022. Lake Tahoe, CA. pp 1-8;
- *"A Flash-based Current-mode IC to Realize Quantized Neural Networks,"* Scott, Lee, Khatri, Vrudhula. IEEE Design Automation and Test in Europe Conference, Mar 2022, Antwerp, Belgium. pp 1029-1034;
- *"CIDAN: Computing in DRAM with Artificial Neurons,"* Singh, Wagle, Vrudhula, Khatri. 39th IEEE International Conference on Computer Design (ICCD) 2021, pp 349-356, Oct 2021, virtual conference;
- *"A Statistical Methodology for Post-Fabrication Weight Tuning in a Binary Perceptron,"* Azari, Wagle, Khatri, Vrudhula. IEEE 21st International Symposium on Quality Electronic Design (ISQED) 2020. Mar 25-26, 2020, Santa Clara, CA. pp 141-148;
- *"Threshold Logic in a Flash,"* Wagle, Singh, Yang, Khatri, Vrudhula. 37th IEEE International Conference on Computer Design (ICCD), 2019. Abu Dhabi, UAE, pp 550-558. Nov 17-20, 2019;
- *"Fast, Ring-based Design of 3D Stacked DRAM,"* IEEE Transactions on Very Large Scale Integrated Circuits (TVLSI), IEEE Transactions

on Very Large Scale Integration (VLSI) Systems. Vol 27 number 8, Aug 2019. pp 1731-1741.;

- *"Fast, Ring-Based Design of 3D Stacked DRAM,"* IEEE International Conference on Computer Design 2017: pp 665-672;
- *"Selective Forward Body Bias for High Speed and Low Power SRAMs,"* Journal of Low Power Electronics, Vol. 5, No. 2, Aug. 2009, pp. 185-95;
- *"Low Power and High Performance SRAM Design using Bank-based Selective Forward Body Bias,"* IEEE/ACM Great Lakes Symposium on VLSI, May 10-12, 2009, Boston, MA, pp. 441-44;
- *"Modeling Dynamic Stability of SRAMs in the Presence of Single Event Upsets (SEUs),"* IEEE International Symposium on Circuits and Systems, May 18-21, 2008, Seattle, WA, pp. 1788-91;
- *"Design of a Flash-based Circuit for Multi-valued Logic,"* Proceedings of the Great Lakes Symposium on VLSI (GLSVLSI) 2017, pp 41-46, May 10-12, 2017. Banff, Canada.
- *"SAT-Based Optimization for Flash-Based Digital Designs,"* IEEE/ACM Design Automation Conference (DAC), Jun 18-22 2017, Austin, TX.

- *"A Flash-based Digital Circuit Design Flow,"* IEEE/ACM International Conference on Computer-Aided Design (ICCAD) 2016, Austin, TX, Nov 2016.
- *"Implementing low power digital circuits using flash devices,"* 2016 IEEE 34th International Conference on Computer Design (ICCD), pp 109-116, Oct 3-5, 2016, Phoenix, AZ.
- *"Exploring Flash Devices to Implement Digital Circuits,"* IEEE/ACM Design Automation Conference (DAC), June 2016, Austin, TX.
- *"FTCAM: An Area-efficient Flash-based Ternary CAM Design,"* IEEE Transactions on Computers, Vol. 65, No. 8, Aug. 2016, pp. 2652-58;
- *"An Area-efficient Ternary CAM Design Using Floating Gate Transistors,"* IEEE International Conference on Computer Design, Oct. 19-22, 2014, Seoul, S. Kor., pp. 55-60; and
- *"A Fast Ternary CAM Design for IP Networking Applications, International Conference on Computer Communications and Networks,"* October 22, 2003, Dallas, TX, pp. 434-39 (awarded best paper).

16. In addition to my work on the papers listed above, I have also served as an editor for IEEE Transactions on Computers, ACM Transactions on Design Automation of Electronic Systems, and MDPI Journal of Electronics.

17. I have served as EDA Track Co-Chair for ICECS 2014, Panel Chair for TexasWISE 2014, Track Co-Chair (VLSI Systems, Applications and Computer Aided Design track) for ICECS 2013, Poster Session Chair for TexasWISE 2013, Advisory Committee for HotPI 2013, Panel Session Chair for SLiP 2013, Track Chair (Logic track) for ICCAD 2009-10, 2015-17, Track Chair (logic track) for DAC 2016-17, General Chair for IWLS 2009, Technical Program Chair for IWLS 2008, Track Co-Chair, Computer Aided Network Design (CANDE) Track, for ISCAS 2008-10, Track Co-Chair, Test and Methodologies Track, for ICCD 2007, Panel Chair for ITSW 2009, Publicity Co-Chair for GLS-VLSI 2009, and as a member of the TPC for several conferences.

III. Summary Of Materials Reviewed And Considered

18. All of the opinions contained in this Declaration are based on the documents I reviewed and my knowledge and professional judgment. In forming the opinions expressed in this Declaration, while drawing on my experience in the field of semiconductor circuit design, I reviewed the Petition and all exhibits attached thereto, and all exhibits cited herein.

19. My opinions are guided by my appreciation of how a person of ordinary skill in the art (defined in Section V) would have understood the claims of the '291 patent at the time of the invention, which I have been asked to assume is March 8, 2017.

IV. Understanding of Legal Standards

20. I am not an attorney, and in this Declaration, I do not opine on matters of law. For the purposes of this Declaration, I have been informed about certain aspects of the law that are relevant to my analysis and opinions. My understanding of these principles is set forth below.

21. I have been informed by Counsel that the validity analysis is a two-step process. First, the patent claims are construed to ascertain their proper scope. Second, the construed claims are compared to the identified prior art to determine if the claims are valid over the prior art.

22. I have been informed by Counsel that there are different types of patent claims, including method claims and apparatus claims. I understand that method claims focus on the steps or processes involved in an invention, while apparatus claims focus on the physical structure and components of a device. Method claims describe the actions taken to achieve a result, while apparatus claims, on the other hand, describe the physical device itself. For example, a method claim may recite a process for forming a chair comprising attaching at least

two legs to a seat. An apparatus claim, for example, may recite a chair structure comprising a seat, four legs, and a back, regardless of the method of making it.

23. I also understand that to be considered prior art, a reference must be enabling, meaning it provides sufficient detail for a POSITA to make and use the invention without undue experimentation.

24. I have been informed by Counsel that patent claims can be deemed invalid if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. It is not sufficient that a collection of prior art references merely recites the various elements of a challenged patent claim. Rather, as I have been informed by Counsel, the prior art must present the elements in a manner that is consistent with their arrangement or use in the challenged claims. I have been informed by Counsel that obviousness cannot be based on the hindsight-driven combination of components selectively culled from the prior art.

25. I have been informed by Counsel that a POSITA is a hypothetical person who is presumed to have known the relevant art at the time the invention was made. I have been informed by Counsel that the condition "at the time the invention was made" is imposed to rule out impermissible hindsight. I also have been informed by Counsel that an expert is to analyze the prior art from the

perspective of a POSITA at the time the invention was made, and not simply to provide his/her own personal conclusions.

26. I also have been informed by Counsel that an obviousness determination includes several factual inquiries, including (1) determining the scope and content of the prior art; (2) ascertaining the differences between the claimed invention and the prior art; (3) resolving the level of ordinary skill in the pertinent art; and (4) taking into consideration any objective indicia of nonobviousness.

27. I have been informed by Counsel that obviousness must be determined as of the date of the invention (i.e., the effective filing date). In considering the reason or motivation to combine references, it is essential to avoid using hindsight. For example, the problem examined when considering obviousness is the general problem that confronted the inventor before the invention was made, not the specific problem solved by the invention. Defining the problem in terms of its solution leads to improper hindsight in the selection of the prior art relevant to obviousness. Further, an overly narrow statement of the problem can represent a form of hindsight, because often the inventive contribution lies in defining the problem in a new revelatory way. Similarly, a conclusory assertion that a POSITA could combine the references, rather than a showing why they would have been motivated to do so, is an impermissible form of hindsight.

Moreover, knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references to reach the particular claimed invention.

28. I have been informed by Counsel that a motivation to solve a problem (or issue) is not the same as a motivation to combine references.

29. I have been informed by Counsel that the analysis of the motivation to combine should be explicit. Additionally, it must include articulated reasoning with rational underpinnings to support the conclusion of obviousness. Providing a full explanation of the motivation to combine the references and the reasonable expectation of success is a necessary component of the obviousness inquiry, as inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known. However, conclusory statements fail to adequately explain why POSITA would have a motivation to combine the potential prior art references.

30. I also have been informed by Counsel that evidence suggesting reasons to combine cannot be viewed apart from evidence suggesting reasons not to combine. In analyzing motivation, both advantages and disadvantages must be considered. Teaching away, for example, is a statement in the prior art that either (i) discourages one from following the path of the claimed invention, or (ii)

encourages one to follow a path that diverges from the path of the claimed invention. The concept of teaching away bears directly on whether there was a reason to combine prior art.

V. Level of Ordinary Skill in the Art

31. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA may have for combining references.

32. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the relevant field. I have been further informed and understand that a POSITA is also a person of ordinary creativity.

33. Petitioner's expert Dr. Banerjee defines a POSITA as a person having "a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree

may replace some of the professional experience)." Ex. 1003 ¶38. Dr. Banerjee further states that "this POSITA would have been aware of and generally knowledgeable about 3D NAND's structure, how it is manufactured, and its component parts." *Id.* ¶39.

34. For the purposes of this declaration, I have not been asked to provide an opinion on the level of ordinary skill in the art, or to opine on Dr. Banerjee's definition on this issue. In view of my educational background and work experience, I surpass Dr. Banerjee's definition of a POSITA. In forming my opinion, I have drawn on my academic background and professional experiences. My opinions herein, however, were formed taking into account the perspective of an ordinarily skilled artisan using Dr. Banerjee's definition of a POSITA. Under this definition of a POSITA, the Petition does not show the challenged claims are obvious. I reserve the right to opine as to an alternative level of a POSITA in other proceedings or if the Board institutes review in this proceeding.

VI. Background

A. *Only Claims 11, 12, and 14-19 Are At Issue*

35. Petitioner presents one ground based on Costa (Ex. 1005) to challenge claims 1-5, 8-9, 11-12, and 14-19 of the '291 Patent. Pet. 9.

36. I understand that YMTC has disclaimed claims 1-5 and 8-9. Ex. 2008. As a result, only independent claim 11 and its dependent claims 12 and 14-19 are at issue.

37. In my opinion, the Board should deny institution of the Petition because Costa fails to disclose or suggest at least one limitation present in claim 11 (limitation [11.H]).

B. *Technical Background*

38. Memory cells are the fundamental building blocks of digital storage devices, responsible for storing and retrieving data in electronic systems. Each memory cell is capable of holding at least a bit of information, each bit represented as either a 0 or a 1, through the manipulation of electrical quantities such as charges. In traditional, two-dimensional memory, often referred to as planar memory, these cells exist in a flat, horizontal layout. Ex. 1009 pt. 1, 38-40. However, as the demand for higher storage capacities and improved performance has grown, the limitations of two-dimensional memory, such as limited scalability, lithography/patterning, random dopant fluctuations, capacitive coupling interference, reduced number of electrons, and increased power consumption, have driven the development of more advanced memory architectures, such as three-dimensional memory. Ex. 1009 pt. 1, 150.

39. Three-dimensional NAND (3D NAND) memory cells represent a significant advancement in data storage technology, offering increased storage capacity and efficiency compared to traditional two-dimensional memory. *See* Ex. 1011, 120-121. Unlike their two-dimensional counterparts, 3D NAND memory cells can be stacked vertically, allowing for greater density and storage capacity within the same physical footprint. *See* Ex. 1011, 120-125.

40. These 3D stacks can comprise alternating layers of insulating and charge-trapping materials, such as silicon oxide and silicon nitride, which allow the individual memory cells to remain isolated from each other. *See* Ex. 1011, 127-128. These layers are penetrated by channel holes, which allow for the creation of 3D NAND strings and interconnectivity between the layers, allowing for the reading and writing of data to the memory cells. *See* Ex. 1011, 121-123. The creation of channel holes is a critical step in the fabrication of 3D NAND memory, as the channel holes must be precisely aligned and uniformly etched to ensure optimal performance and connectivity between each stack. *See* Ex. 1011, 121-123, 130.

C. *The '291 Patent (Ex. 1001)*

41. The '291 Patent, filed on January 5, 2021 and claiming priority to March 8, 2017, relates to "the field of semiconductor technology, and more particularly, to joint opening structures of three-dimensional [] memory devices."

Ex. 1001 at 1:17-20. In particular, the disclosure of the '291 Patent addresses issues that arise because "three-dimensional [] memory devices . . . keep scaling more oxide/nitride [] layers." *Id.* at 1:24-26.

42. As the number of layers increases, it becomes more difficult to use a single etching process to form the channel holes (i.e., akin to drilling a hole through the many layered three-dimensional memory), both because increasing the depth of the channel holes makes the etching process "exponentially slower" and because it increases the risk of improperly formed holes, which typically are wider at the top and narrower at the bottom. *See id.* at 1:26-35.

43. To address this issue, the '291 Patent discloses three-dimensional memory devices made from two stacks of oxide/nitride layers. Ex. 1001, 1:45-56, 1:59-63. Each stack of nitride/oxide layers includes a channel hole, also called a through hole. Ex. 1001, 1:45-49, 1:61-63. The stacks can then be placed one atop the other with the through holes aligned. Ex. 1001, 1:66-2:5. Specifically, the '291 Patent discloses structures for such three-dimensional memory devices that allow the stacks to be placed atop each other while improving electrical connectivity between the stacks. Ex. 1001, 1:57-59, 1:63-66, 1:43-2:5.

44. The '291 Patent describes forming the joint opening structure on top of a first stacked layer 2 (orange), by forming a first insulating connection layer 3

(purple) and a conductive third channel structure 14 (red) that is wider than the through hole in the first stacked layer 2.

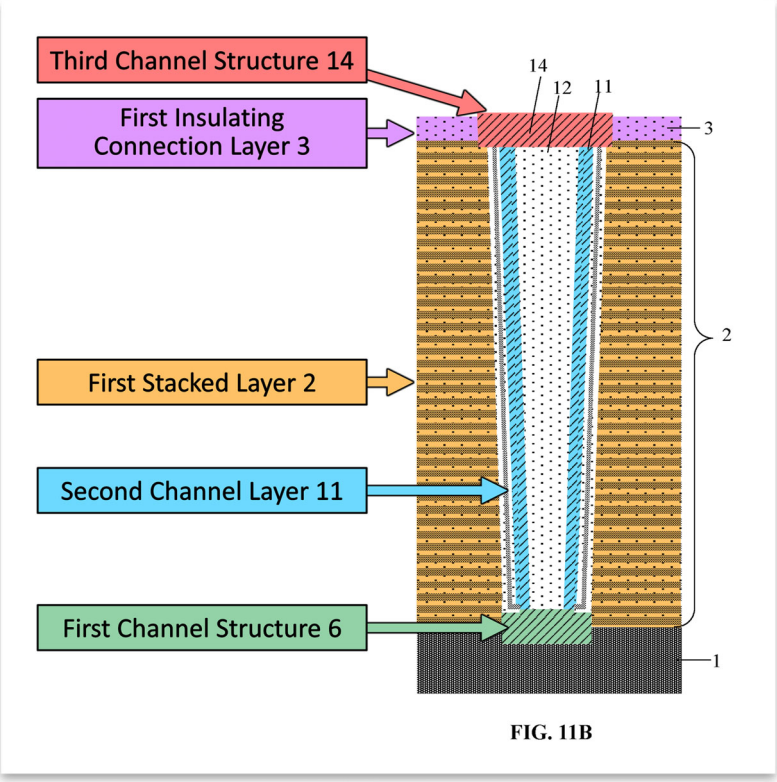


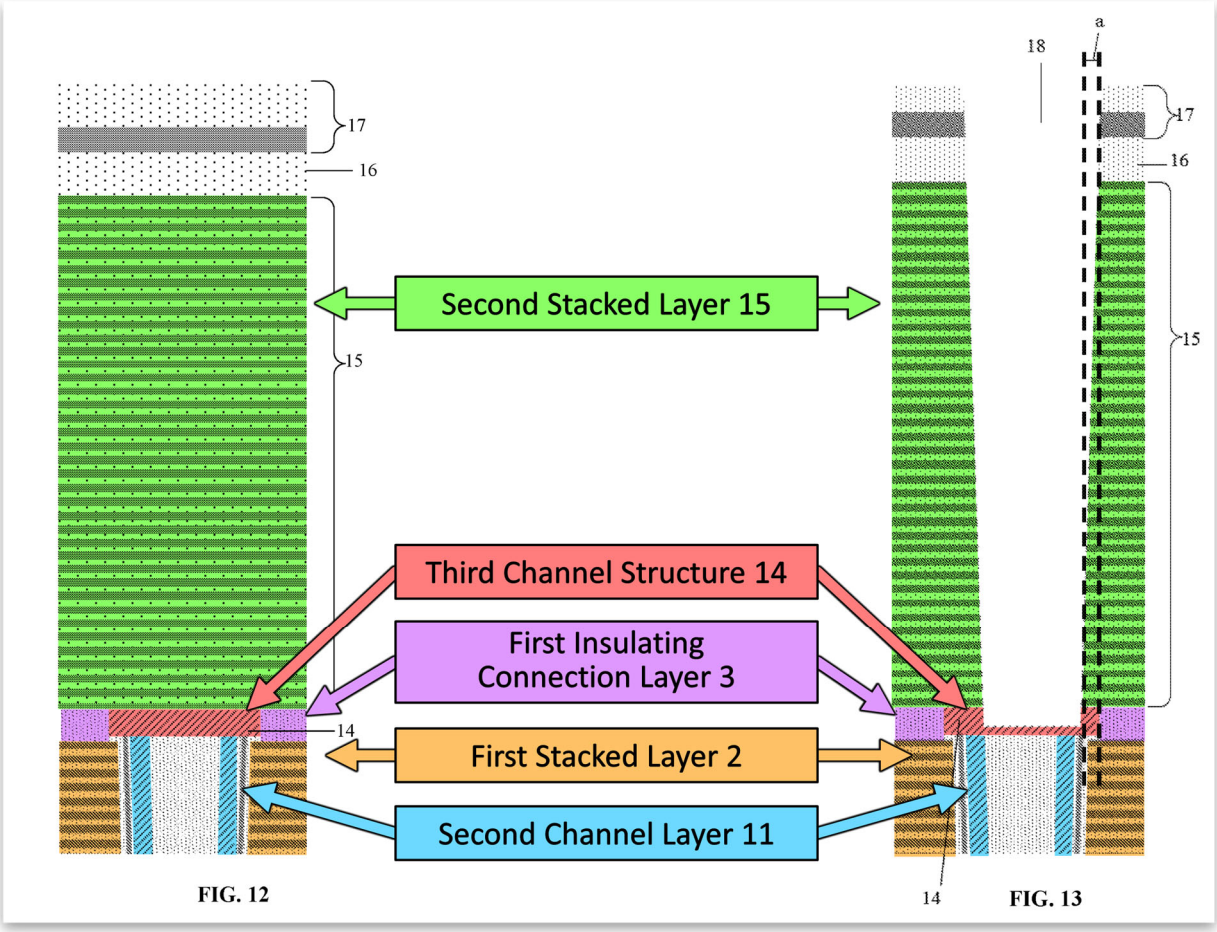
FIG. 11B

Ex. 1001, Fig. 11B,[1] 9:26-27, 9:61-62, 10:30-39, 11:31-33, 12:59-64, 21:8-10. The conductive third channel structure 14 (red) extends electrical contact from both conductive first channel structure 6 (above in green) and conductive second channel layer 11 (above in blue). Ex. 1001, 10:30-39, 11:25-44, 11:45-12:23, 12:59-64, 19:40-43.

45. To further form the joint opening structure to facilitate electrical connection between a first stacked layer 2 (below in orange) and a second stacked

[1] Annotations to figures are added unless stated otherwise.

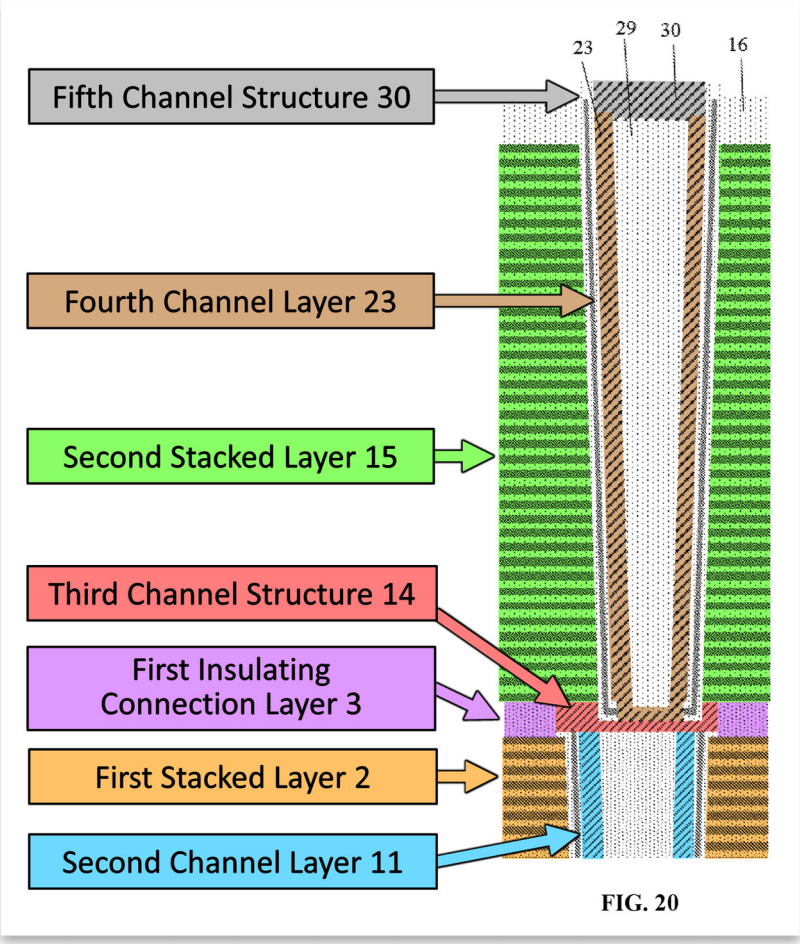
layer 15 (below in green), the second stacked layer 15 is ***disposed on*** the conductive third channel structure 14 (below in red).



Ex. 1001, Figs. 12, 13, 13:11-20. Next, as visible above in Figure 13, a through hole 18 is formed through the second stacked layer 15 (green) to the third channel structure 14 (red). Ex. 1001, 13:11-21, 13:38-45, Fig. 13.

46. Further, conductive fourth channel layer 23 (below in brown) is deposited into through hole 18 and conductive fifth channel structure 30 (below in

grey) is added on top to complete the electrical connection through the two stacks. *Id.* at 14:44-58, 15:12-14, 15:24-31.



Ex. 1001, Fig. 20. As a result, a joint opening structure is formed in the dual-stack 3D memory that connects conductive channel structures formed in through holes of two separate stacks. *Id.* at 15:24-31, 13:57-59, 12:59-62, 12:8-10.

47. Because the third channel structure 14 is wider than and covers the first through hole below it, the third channel structure 14 acts as an alignment pad that will necessarily overlap with the through hole in the second stack to provide a

margin for alignment of the two through holes. *See* Ex. 1001, 32:17-26, 1:57-59, 1:63-66, 13:42-45. The components of the joint opening structure limit "top-bottom aperture error" by providing a landing pad for connection between stacks (e.g., third channel structure 14 (red)), resulting in "an efficient process capability control, a simplified process complexity, and a reduced cost." Ex. 1001, 32:17-26, 1:57-59, 1:63-66, 13:42-45.

D. *Prosecution History*

48. I have reviewed the prosecution history of the '291 Patent. I do not address the prosecution history in detail in this declaration as it does not impact any of my opinions herein. However, I do not acquiesce to any statements or positions by Petitioner or its expert regarding the prosecution history, and I reserve the right to respond to any analysis by Petitioner or its expert on the prosecution history.

E. *Costa (Ex. 1005)*

49. Costa is a U.S. Patent Publication titled "Three-Dimensional Memory Devices Containing Inter-Tier Dummy Memory Cells and Methods of Making the Same," which was filed on February 28, 2017 and published on June 28, 2018. Costa discloses a memory device with two stacks of alternating insulation and electrically conductive layers. Costa, Abstract. Costa further discloses a "joint-level doped semiconductor portion 173" (yellow below) as part of a vertical

memory channel (green below) that electrically connects the first and second stacks, as shown in Figure 21G.

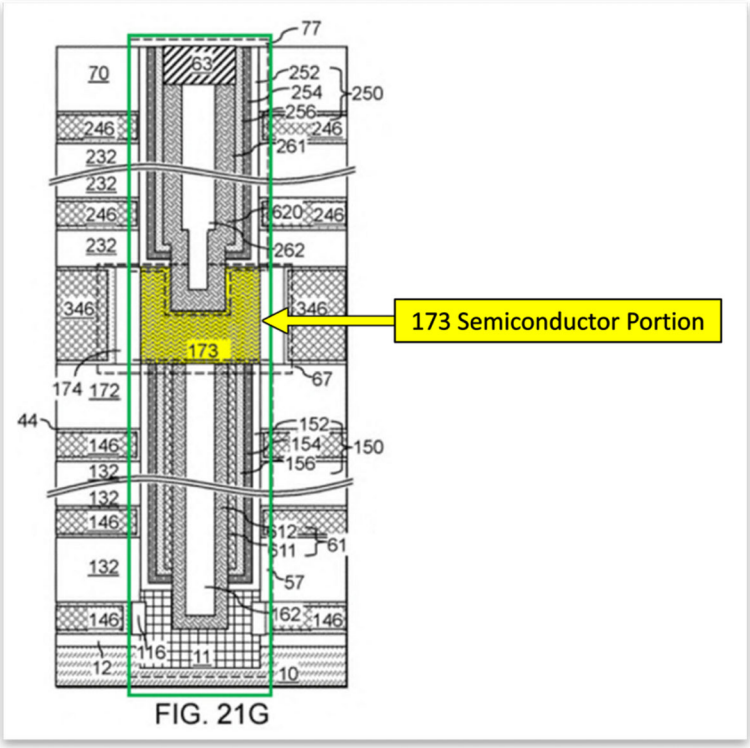
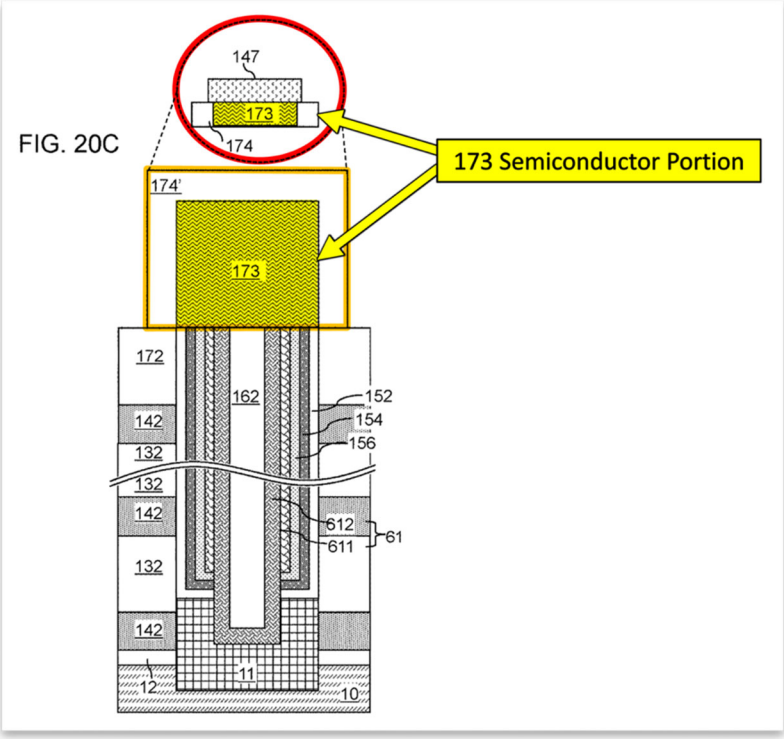


FIG. 21G

Costa, Fig. 21G (green annotations by Petitioner at Pet. 29; yellow annotation added by Patent Owner), ¶¶272-280.

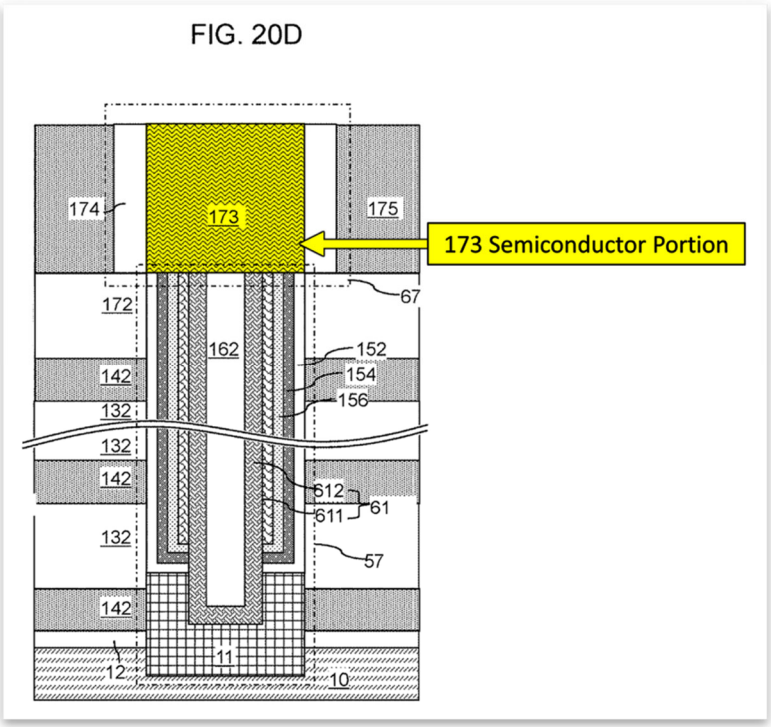
50. However, Costa describes several processing steps before reaching the final configuration shown above. During the manufacturing of the 3D memory, a "joint-level doped semiconductor layer 173L" is placed atop the first stack and oxidized, either with a mask 147 (in red circle below) or without mask 147 (in orange square below), as seen below in Figure 20C. Costa, ¶¶264-266. During the oxidation process, the exposed surfaces of portion 173 are converted into dielectric

oxide material (174 or 174') and the lateral dimension of portion 173 is reduced, as seen below in Figure 20C. *Id.* at ¶266.



Costa, Fig. 20C.

51. Next, the top portion of the dielectric material is removed to form an annular dielectric spacer 174, and joint-level spacer material 175 is then deposited over the first tier-structure and around semiconductor portion 173 and dielectric spacer 174. Costa, ¶¶266-268, Fig. 20D.



Costa, Fig. 20D.

52. Next, second tier structure 232, 242 is formed above layers 173, 174, and 175, and a second-tier memory opening 249 is formed over the semiconductor portion 173 exposing the semiconductor portion 173. *Id.* ¶¶272, 190, Figs. 10A, 10B, 21A.

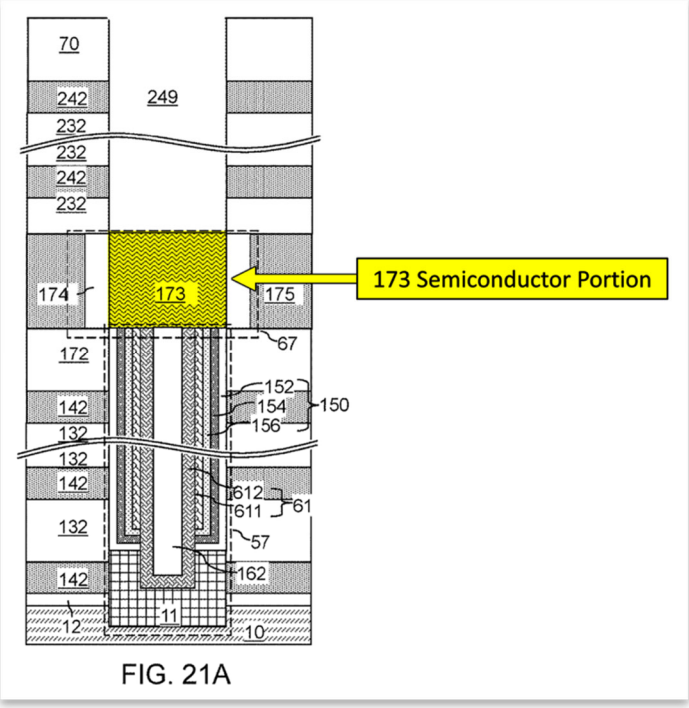


FIG. 21A

Costa, Fig. 21A.

53. As seen below in Fig. 21G, additional processing steps are performed to fill in second-tier memory opening 249 with multiple layers, including second inner semiconductor channel layer 622, and drain region 63 is formed into a recess etched into second dielectric core 262. *Id.* ¶¶274-275, 212, 277.

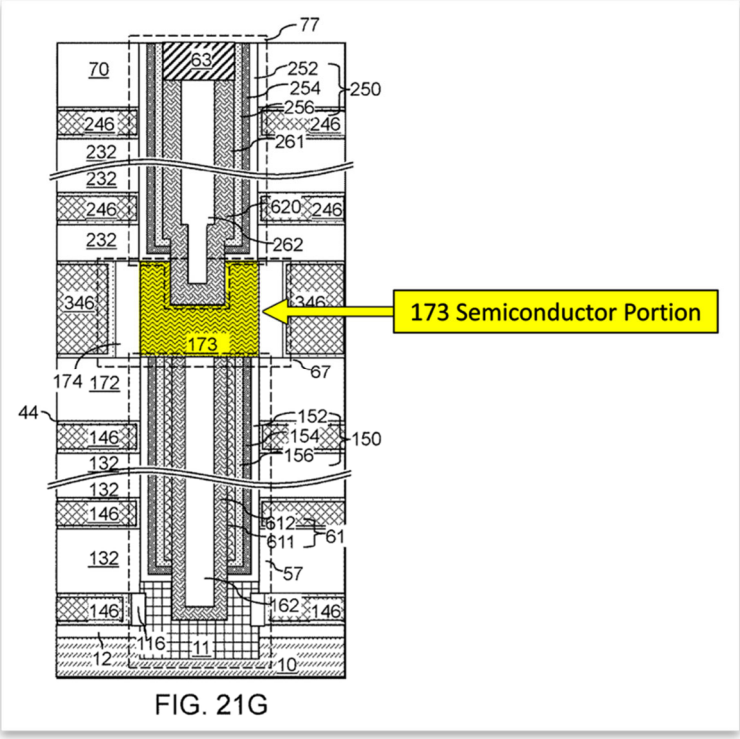


FIG. 21G

Costa, Fig. 21G.

F. *Claim Construction*

54. I am not a legal expert or an attorney and offer no opinions on the law. I understand that claim construction is a matter of law. However, I have been informed by Counsel of the legal standards that apply to claim construction in an inter partes review, and I have applied them in forming my opinions. I understand that during an inter partes review, the same claim construction standard used in federal district court is applied when addressing the meaning of claim terms.

55. I understand that claims must be construed in light of and consistent with the intrinsic evidence. In this context, intrinsic evidence includes the claims themselves, the written disclosure in the specification including all figures, and the

patent's prosecution history, including prior art that was considered by the United States Patent and Trademark Office ("USPTO"), and references cited on the patent itself. I understand that extrinsic evidence may also be considered when construing claims and may include, for example, technical dictionaries, technical publications and books, treatises, and expert testimony, but that such extrinsic evidence should be given less weight than the intrinsic evidence. I also understand that extrinsic evidence can be used in claim construction when the intrinsic evidence does not clearly provide the meaning of a claim term. However, I understand that extrinsic evidence cannot contradict the intrinsic evidence.

56. I understand that claim terms are assigned their ordinary and customary meaning to a POSITA, unless the specification or prosecution history provides a special, different meaning. I further understand that a POSITA is expected to read each claim term in the context of the entire patent, including the specification, which is always highly relevant and the single best guide to the meaning of a disputed term.

57. I further understand that the plain and ordinary meaning of a claim term can be overcome when an inventor clearly and expressly acts as his or her own lexicographer by defining a claim term. An inventor acts as his or her own lexicographer by explicitly setting forth a definition of a claim term distinct from its ordinary meaning.

58. I further understand that the relevant timeframe for assessing the '291 Patent for purposes of this declaration is around March 8, 2017, the earliest priority date. If I refer to the time of the invention in this declaration, I am referring to this timeframe.

59. In my opinion, the prior art relied on in the Petition (i.e., Costa) fails to disclose the subject matter of the challenged claims under any reasonable construction, including plain and ordinary meaning.[2]

60. In Petitioner's claim construction section, Petitioner alleges "the '291 Patent's claims do not require further construction and should receive their plain and ordinary meaning." Pet. 21. For claim 4—not at issue in this Preliminary Response—Petitioner states that "Micron applies YMTC's claim interpretation that is evident from its infringement contentions in the Co-Pending Litigation." Pet. 21-24. Petitioner represents that all other claims, including claim 11 and its dependents at issue in this Preliminary Response, "should receive their plain and ordinary meaning." Pet. 21.

61. When analyzing the '291 Patent claims, however, Petitioner and its expert Dr. Banerjee argue that "the '291 Patent does not limit 'on' to 'directly

[2] I reserve the right to advocate for claim constructions if the Board institutes review.

contacting' (*i.e.*, there can be intervening layers)." Pet. 43 (citing Ex. 1001, 8:3-12); Banerjee ¶171; *see also* Pet. 33-34, 56; Banerjee ¶¶136, 171.

62. The inventors of the '291 Patent acted as their own lexicographers and defined the term "on" in the specification:

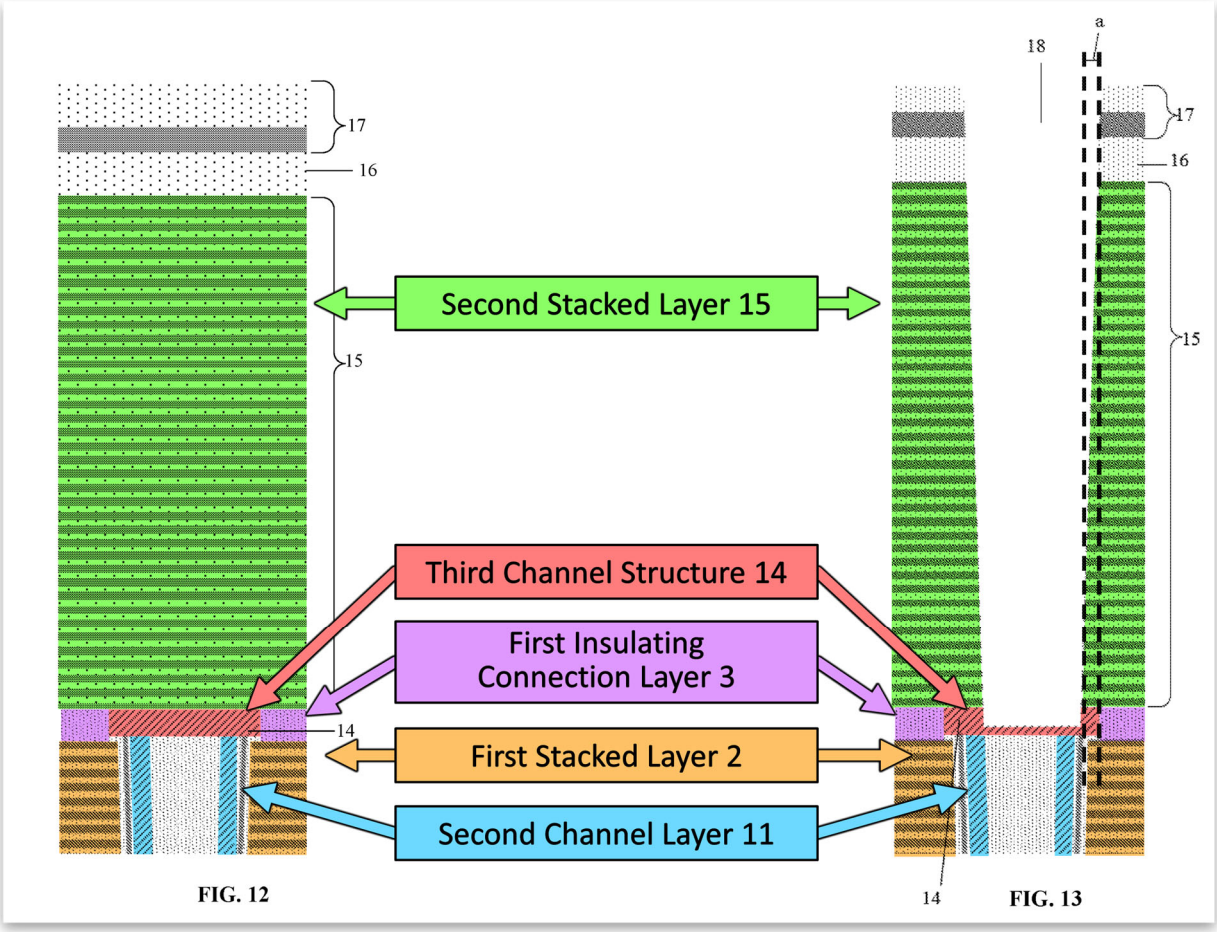
> It should be readily understood that the meaning of "on," "above." and "over" in the present disclosure should be interpreted in the broadest manner such that ***"on" not only means "directly on" something but also includes the meaning of "on" something with an intermediate feature or a layer therebetween***, and that "above" or "over" not only means the meaning of "above" or "over" something but can also include the meaning it is "above" or "over" something with no intermediate feature or layer therebetween (i.e., directly on something).

Ex. 1001, 8:3-12 (emphasis added).[3] As seen above, the '291 Patent inventors offset the term "on" with quotations, and clearly expressed intent to redefine it by stating it "not only means … but also includes the meaning of …." *See* Ex. 1001, 8:3-12. Based on this lexicography, "on" should be construed as "directly on or on with an intermediate feature or layer therebetween."

63. The rest of the specification is consistent with and supports the lexicography in the '291 Patent. As discussed above, the specification shows an example of a "second stacked layer … formed on the third channel structure." Ex. 1001 at 13:11-17. It explains that this arrangement is "shown in FIG. 12." *Id.* As

[3] Emphasis added unless stated otherwise.

can be seen in Figure 12 below on the left, the second stacked layer 15 (green) is disposed directly on the third channel structure 14 (red).



Ex. 1001, Figs. 12, 13. As seen in Figure 13 above on the right, after the creation of the "second through hole 18", the second stacked layer 15 (green) is still on the third channel structure 14 (red).

64. The specification and lexicography therein do not suggest that "on" means "over." Ex. 1001, 8:3-12. To the contrary, the specification distinguishes "on" and "over" by providing distinct lexicography for each term. Ex. 1001, 8:3-12 ("'[O]ver' not only means the meaning of … 'over' something but can also

include the meaning it is … 'over' something with no intermediate feature or layer therebetween (i.e., directly on something)").

65. If "on" meant the same thing as "over," a first element that is higher than a second element could be interpreted as "on" the second element (e.g., the top of the dome of the U.S. Capitol could be interpreted as "on" the USPTO's James Madison Building).

66. To clarify, I do not believe any terms require construction for the Board to deny institution. To the extent that the Board does not agree with the above lexicography, it is my opinion that the Petition still fails if the claim term "on" receives its plain and ordinary meaning—e.g., physically in contact with or directly on top of with intervening objects therebetween.

VII. Claims 11-12 and 14-19 Are Not Obvious Over Costa

67. In my opinion, the Petition is fatally flawed because Petitioner failed to demonstrate that Costa teaches each and every claim element of independent claim 11. As a result, Petitioner similarly fails to meet its burden with respect to claims 12 and 14-19, each of which depend from claim 11.

68. Because limitation [11.H] of independent claim 11 requires "second stacked layer disposed on the third channel structure" and Costa fails to disclose that arrangement—and Petitioner does not even contend it would have been obvious to modify Costa in some way to meet this limitation—Petitioner fails to

show a reasonable likelihood of success for any challenged claim. In my opinion, the Board should deny institution as a result.

A. *Costa Does Not Disclose "A Second Stacked Layer Disposed On The Third Channel Structure" (Limitation [11.H])*

69. Claim 11 recites, in part, "[a] joint opening structure of a three-dimensional (3D) memory device, comprising … a second stacked layer disposed on the third channel structure." Ex. 1001, 45:52-53, 46:4-5.

70. Petitioner addresses limitation [11.H] with a single sentence: "This limitation is present in [1.G] and Costa discloses it for the same reasons." Pet. 92. But apparatus limitation [11.H] is not present in method limitation [1.G]. The two limitations are different and the Petition does not address the structure claimed in apparatus limitation [11.H] when addressing method limitation [1.G]. Nor can the Petitioner do this, since Costa does not disclose the structure claimed in apparatus claim [11.H].

1. *A "Joint Opening Structure" With "A Second Stacked Layer Disposed On The Third Channel Structure" (Limitation [11.H]) Is Not Present In Method Limitation [1.G]*

71. Method limitation [1.G] and apparatus limitation [11.H] are not coextensive—that is, they do not have the same recited elements. Method limitation [1.G] recites "forming a second stacked layer and forming a second insulating connection layer on the first insulating connection layer." Ex. 1001, 43:43-44:10. Method limitation [1.G] does not require that the "second stacked

layer" is "disposed on the third channel structure," as recited in apparatus limitation [11.H]. *Id.* at 43:43-44:10, 45:52-46:20.

72. In my opinion, the Petition's fatal flaw is that it ignores the distinction between the method and apparatus claims, citing steps in Costa's method but ignoring the final apparatus that Petitioner alleges meets the claim limitations. Rather than method claim 1 which recites "***[a] method of forming*** a joint opening structure" and limitation [1.G] which recites the method step of "forming a second stacked layer … on the first insulating connection layer," the apparatus claim 11 recites "***[a] joint opening structure*** of a three-dimensional (3D) memory device" and limitation [11.H] recites the required feature of "a second stacked layer disposed on the third channel structure." Ex. 1001, 43:43-44:10, 45:52-53, 46:4-5, 45:52-46:20; *see* Pet. 70 (Petitioner recognizing the method-apparatus distinction in the context of claim 1, stating that any argument regarding Costa's "finished configuration is irrelevant" to the method step in limitation [1.K]); Pet. 90 (recognizing the "joint opening structure" recited in [11.PRE] and that "claim 1 recites a method for forming the same"). The Petition points to Costa to address "***forming*** a second stacked layer" as recited in method claim [1.G], while ignoring the distinctive limitation "a second stacked layer ***disposed on the third channel structure***" as recited in apparatus claim [11.H].

2. *Petitioner's Cited Costa Disclosure For Method Limitation [1.G] Does Not Disclose A "Joint Opening Structure" With "A Second Stacked Layer Disposed On The Third Channel Structure" (Limitation [11.H])*

73. Petitioner's ground addressing apparatus claim 11 fails because it relies exclusively on Costa, and Petitioner's disclosures from Costa do not teach "a second stacked layer disposed on the third channel structure" as recited in limitation [11.H]. Nor can Petitioner show this, since, as I explain below, Costa's "second stacked layer" (i.e., second alternating stack 232, 242 according to Petitioner) is not "disposed on" the "third channel structure" (i.e., semiconductor portion 173 according to Petitioner).

74. Petitioner addresses apparatus limitation [11.H] by referring back to method limitation [1.G] (Pet. 92), but Petitioner's reliance on Costa to address method limitation [1.G] fails to address how the "second stacked layer" is "disposed on the third channel structure," as recited in apparatus limitation [11.H]—mainly because Costa does not disclose it. To address limitation [1.G], Petitioner relies on Costa's Figure 21A reproduced below, stating that Costa discloses "forming a second stacked layer ('second alternating stack' 232, 242) [in green below] and forming a second insulating connection layer ('insulating cap layer 70') [in red below] on the first insulating connection layer ('first insulating cap layer 172') [in blue below]." Pet. 55.

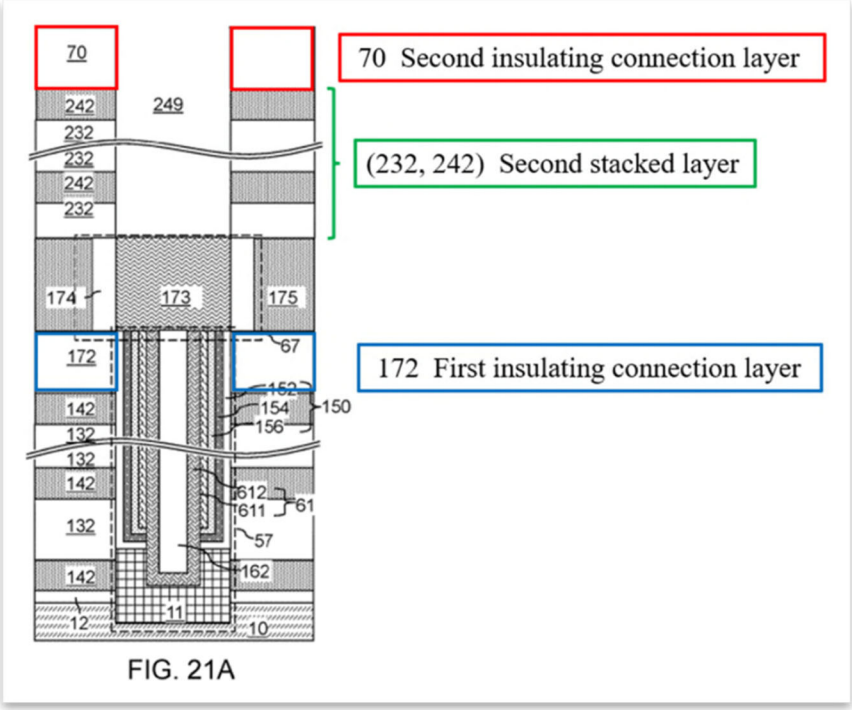


FIG. 21A

Costa, Fig. 21A (Petitioner's annotations at Pet. 56).

75. Therefore in its analysis of [1.G], Petitioner does not address whether the "second stacked layer disposed on the third channel structure," as required by [11.H]. *See* Pet. 54-57. Petitioner gets it wrong by relying on [1.G] to address [11.H], stating "This limitation is present in [1.G] and Costa discloses it for the same reasons." Pet. 92.

76. Further, even if Petitioner tried, it would not be able to show that the "second stacked layer [is] disposed on the third channel structure," because the "second stacked layer" in Costa is not "disposed on" "the third channel structure."

77. In other words, Petitioner appears to argue that Costa discloses method limitation [1.G]—which recites "forming a second stacked layer and

forming a second insulating connection layer on the first insulating connection layer"—by forming a second stacked layer ("second alternating stack" 232, 242; green below) above the third exemplary structure's single joint-level doped semiconductor portion 173 (what Petitioner calls the "third channel structure" (Pet. 46), yellow below), annular dielectric spacers 174 (brown below), and joint-level spacer material layer 175 (pink below). *See* Pet. 55-56 (citing Costa ¶¶270 (noting that processing steps shown in Figures 8A, 8B, 10A, and 10B apply to the third exemplary structure), 178 (noting second alternating stack (232, 242) is formed on the top surface of the joint-level material layers (175, 176, 177) as in Figures 8A and 8B)).

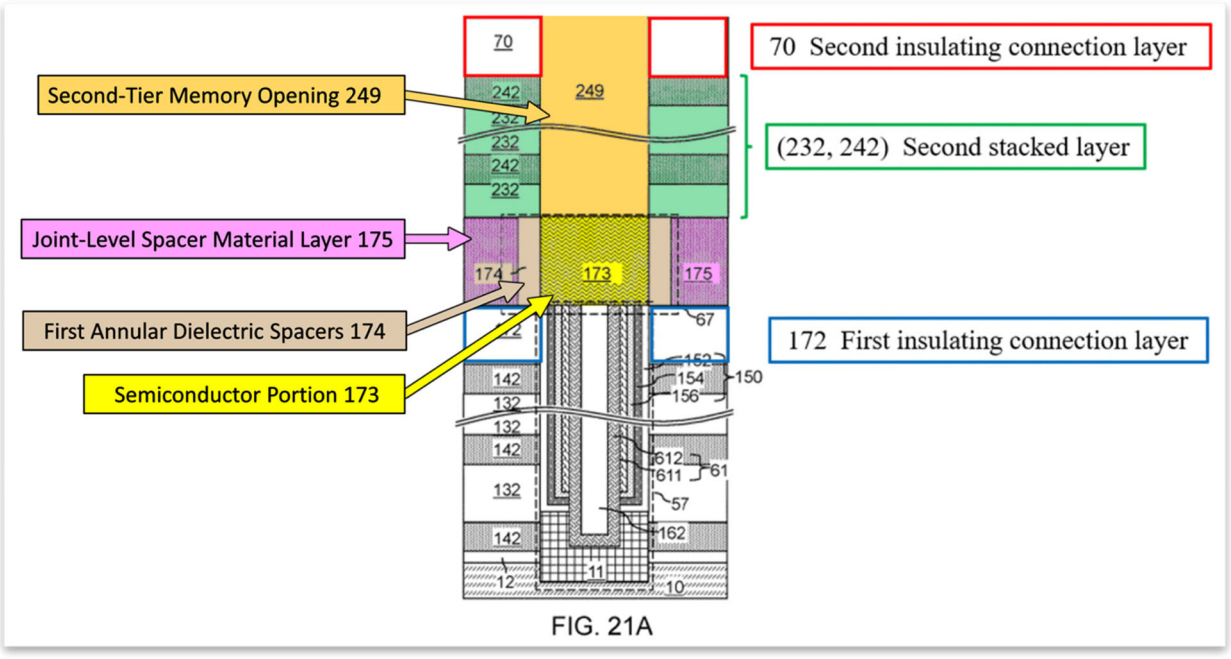


FIG. 21A

Costa Fig. 21A (red, blue, and green annotations added by Petitioner at Pet. 56; orange, pink, brown, and yellow annotations added by Patent Owner); *see* Costa

¶75 (noting Figure 21A illustrates the third exemplary structure after forming second-tier opening 249 (above in orange) as depicted in Figures 10A and 10B). Petitioner relies on Figure 21A, which depicts the step of forming a through hole (above in orange) through "second alternating stack" 232, 242 (above in green). Pet. 56.

78. Later in the Petition, for a different limitation (not [1.G] or [11.H]) Petitioner depicts Figure 21A showing a "second memory through hole in the second stack" above the semiconductor portion 173. Pet. 59; *see also id.* at 30 (Petitioner addressing [1.PRE] by describing how Costa forms a "joint opening structure" by "etching a second memory through hole in the second stack (and forming a channel structure therein)"), 90 (addressing [11.PRE] by referring to [1.PRE]). As would be expected, Petitioner's citations to Costa's Figure 21A to address limitation [1.G] focus on the ***process for forming*** the apparatus, not on the apparatus itself. *See* Pet. 54-57.

79. Petitioner's Costa disclosure to address method limitation [1.G] does not disclose apparatus limitation [11.H], which requires a "joint opening structure" with "a second stacked layer disposed on the third channel structure." Because claim 11 is an apparatus claim, not a method claim, the process for forming the apparatus is not relevant—the ultimate apparatus itself is. And as seen above in Figure 21A, ***the "second stacked layer"*** (i.e., 232, 242 according to Petitioner) ***is***

not "disposed on" the "third channel structure" (i.e., semiconductor portion 173 according to Petitioner).

80. Instead, Costa describes ***a second-tier memory opening 249*** (in orange above) ***that is formed above the semiconductor portion 173***, as shown in Figure 21A. *Id.* at ¶¶191 (describing process of forming second-tier memory opening 249 over opening fill structure 67 as shown in Figures 10A and 10B regarding a "first exemplary structure"), 269 (joint-level memory opening fill structure 67 includes semiconductor portion 173), 270 (stating this process can be performed for the "third exemplary structure" that Petitioner relies on), 272 (Figure 21A illustrates the third exemplary structure after formation of the second-tier memory opening 249 as shown in Figures 10A and 10B).[4] In this figure , ***the "second stacked layer"*** (i.e., 232, 242 according to Petitioner) ***is not "disposed on" the "third channel structure"*** (i.e., semiconductor portion 173 according to Petitioner).

81. As a result, in my opinion, Petitioner errs in relying on Costa to disclose apparatus limitation [11.H] because it does not disclose "a second stacked

[4] Costa has a typo in Paragraph 272 where it states that "FIG. 21A illustrate [sic] a region of the ***second exemplary structure*** at the processing steps of FIGS. 10A and 10B," instead of the "***third exemplary structure***" described in the series of Figures 20A-21G. *See* Costa ¶¶272, 263, 71-81.

layer" (i.e., 232, 242 according to Petitioner) "disposed on" the "third channel structure" (i.e., 173 according to Petitioner).

3. *Costa Does Not Disclose A "Joint Opening Structure" With "A Second Stacked Layer Disposed On The Third Channel Structure" (Limitation [11.H])*

82. None of the figures of Costa (including figures that Petitioner does not refer to in the context of [11.H]) disclose "a second stacked layer disposed on the third channel structure" as recited by apparatus limitation [11.H]. Costa's final configuration in Figure 21G fails to disclose apparatus limitation [11.H].

83. Petitioner does not rely on Figure 21F to address apparatus limitation [11.H], but I will also discuss Costa's configuration depicted in Figure 21F and show that it does not disclose apparatus limitation [11.H].

84. In my opinion, Costa's later configuration depicted in Figure 21F—the one Petitioner relies on for other limitations of apparatus claim 11—does not disclose "a second stacked layer disposed on the third channel structure," as recited in limitation [11.H]. Rather than Figure 21A, Petitioner relies on the later configuration of Costa seen below in Figure 21F.

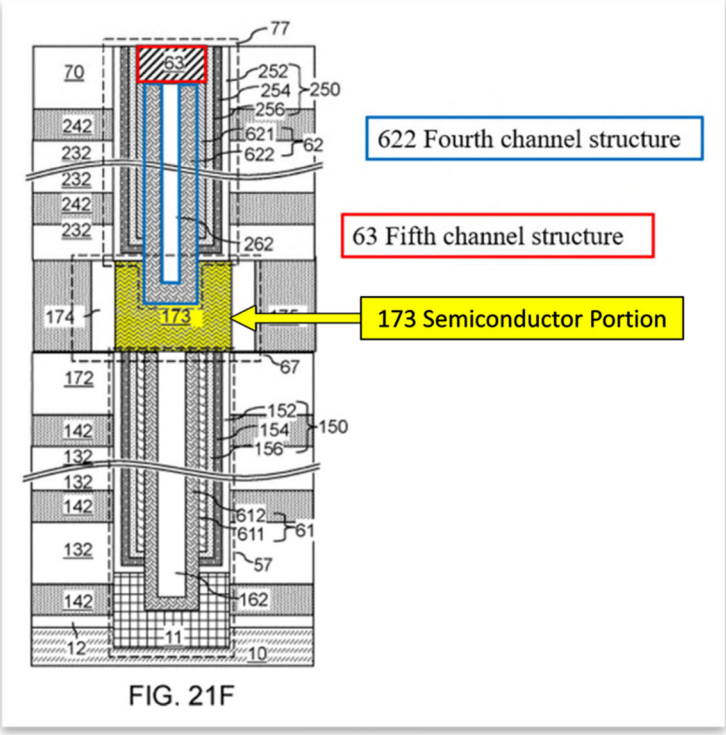


FIG. 21F

Costa, Fig. 21F (Petitioner addressing method limitation [1.K] by relying on Costa's Figure 21F as annotated at Pet. 68); Pet. 92 (Petitioner addressing apparatus limitation [11.M] by referring to method limitation [1.K]). As seen above, numerous layers 252, 254, 256, 621, 622, and 262 are deposited in the second-tier memory opening 249 above the semiconductor portion 173, some of which establish electrical conductivity in a vertical channel. Costa ¶¶273-275, Figs 21B-21D (describing adding layers 252, 254, 256, 621, 622, and 262L into second-tier memory opening 249); *id.* at ¶276 (describing second vertical channel 62, which includes layers 621 and 622, as conducting electrical current); *id.* at ¶277 (describing adding drain region 63); *see also* Pet. 93 (recognizing "second-tier memory openings 249" are "filled in Fig. 21F with second memory open [sic]

opening fill structures 77"). In the configuration in Figure 21F, as in Figure 21A, Costa does not disclose "a second stacked layer disposed on the third channel structure," as recited in limitation [11.H].

85. Costa's final configuration of the third exemplary structure shown in Figure 21G below—one that Petitioner does not rely on in the Petition to address method claim 1 or apparatus claim 11—similarly fails to disclose limitation [11.H]. Figure 21G shows the iterative step of replacing both sacrificial material layers 142, 242 and joint-level spacer material layer 175 with electrically conductive layers 146, 246, 346. Costa ¶¶280 (describing Figure 21G shows the third exemplary structure after the processing steps of Figures 14A and 14B),[5] 217-219 (describing removal of sacrificial material layers 142, 242 and joint-level spacer material layer 175), 222-224 (describing deposit of electrically conductive layers 146, 246, 346).

[5] Costa has a typo in Paragraph 280 where it states that "FIG. 21G illustrates the ***second exemplary structure*** at the processing steps of FIG. 14B," instead of the "***third exemplary structure***" described in the series of Figures 20A-21G. *See* Costa ¶¶280, 71-81.

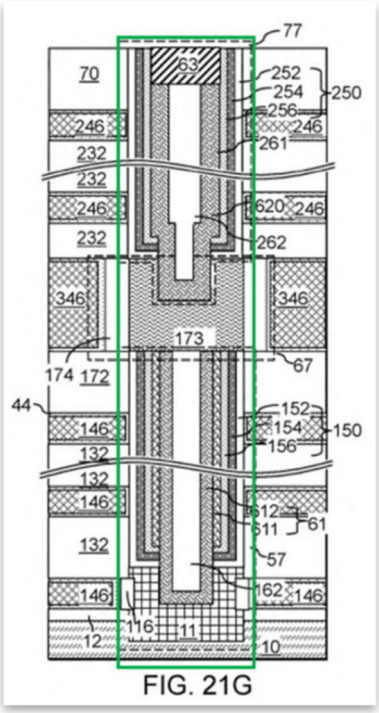


FIG. 21G

Costa, Fig. 21G (annotated by Petitioner at Pet. 29 in overview of Costa). As seen in the above final configuration, Costa's "second stacked layer" (i.e., 232, 242 according to Petitioner) is still not "disposed on the third channel structure" (i.e., 173 according to Petitioner). In fact, Costa's "second stacked layer" (i.e., 232, 242 according to Petitioner) no longer exists because layer 242 has been replaced by electrically conductive layer 246. This can be seen by comparing Costa's Figure 21F with Costa's Figure 21G. Like the prior intermediate configurations of Figures 21A and 21F, Costa's final configuration in Figure 21G fails to disclose a "second stacked layer disposed on the third channel structure," as recited in limitation [11.H].

4. *Petitioner Does Not Argue Costa Renders Obvious A "Joint Opening Structure" With "A Second Stacked Layer Disposed On The Third Channel Structure" (Limitation [11.H])*

86. In my opinion, it is important to note that for limitation [11.H], Petitioner's position is that Costa discloses limitation [11.H], not that Costa renders it obvious. Specifically, Petitioner says that "Costa discloses it," and does not say that Costa renders it obvious. Pet. 92. Petitioner similarly states that Costa discloses limitation [1.G], and does not say that Costa renders it obvious. Pet. 54-57. In other instances, however, Petitioner is clear when it relies on obviousness. *See, e.g.*, Pet. 92 (arguing for limitations [11.J], [11.K], and [11.M] that "Costa discloses it, ***or renders it obvious***"). And as explained above, Petitioner fails to meet its burden to show that "Costa discloses it," i.e., limitation [11.H].

87. In sum, Petitioner failed to demonstrate that the art teaches each and every claim element of independent claim 11, and the Petition is fatally flawed as a result. The Board should deny institution because Costa does not disclose limitation [11.H] for the reasons above.

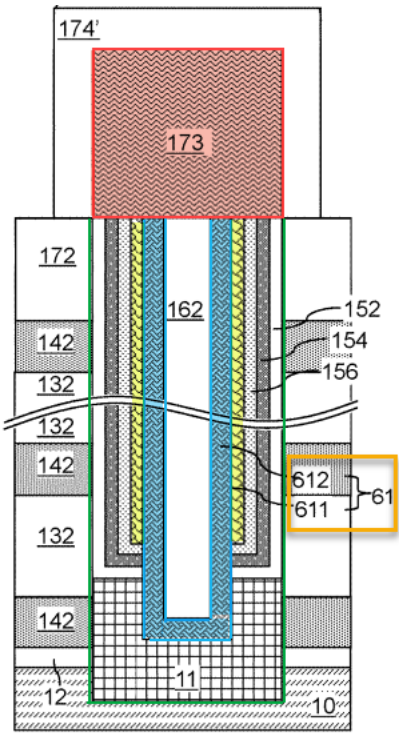
B. *Dependent Claims 12 and 14-19 Are Not Obvious Over Costa*

88. Because independent claim 11 is not disclosed by or rendered obvious over Costa, the Board should also deny institution of the Petition on claims 12 and 14-19, which depend from claim 11.

VIII. Any New Obviousness Argument Regarding Limitation [11.H] Would Be Improper And Hindsight Driven

89. As mentioned above in Section VII.A.4, Petitioner's position is that Costa discloses limitation [11.H], not that Costa renders it obvious. Pet. 92. Petitioner similarly states that Costa discloses limitation [1.G], not that Costa renders it obvious. Pet. 54-57. Moreover—because Petitioner does not provide an obviousness position for limitations [11.H] or [1.G]—Petitioner also presents no evidence or expert testimony to support a motivation to modify Costa to render obvious limitations [11.H] or [1.G].

90. Even if Petitioner did try to modify Costa to render obvious limitations [11.H] or [1.G] (which Petitioner did not), it would be based on hindsight. For example, a POSITA would not modify Costa's semiconductor portion 173 to be wider than the through hole below it because Costa's semiconductor portion 173 already provides significant margin for its purpose at its current width. That is, semiconductor portion 173 is already wide enough to facilitate electrical contact between the upper and lower stacked layers. As seen below in Figure 20C, the semiconductor portion 173 (red) "covers and protects the underlying first vertical semiconductor channel 61," consisting of first outer semiconductor channel layer 611 (yellow) and first inner semiconductor channel layer 612 (blue). Costa ¶¶160, 265, 285.



Costa at Fig. 20C. As illustrated above, the first-tier memory opening 149 (outlined in green) is significantly wider than the first vertical semiconductor channel 61 (layers 611 and 612) which conducts electricity through the multi-tier stack. Costa at ¶¶160 ("Each adjoining pair of a first outer semiconductor channel layer 611 and a first inner semiconductor channel layer 612 can collectively form a first vertical semiconductor channel 61 through which electrical current can flow."), 137 (describing first-tier opening 149 formed in the first tier structure). Moreover, Figure 20C above shows the semiconductor portion 173 covers the first vertical semiconductor channel 61 (layers 611 and 612) by a significant margin.

91. As seen below in Figure 21E, Costa's semiconductor portion 173 is designed to be wider than first vertical semiconductor channel 61 (orange box

identifying blue and yellow layers) and second vertical semiconductor channel 62 (brown box identifying purple and green layers) to form an electrical channel between lower and upper stacks. Costa, ¶¶275-276 (describing second vertical semiconductor channel 62 for the upper stack "through which electrical current can flow"), 278 (describing second vertical semiconductor channel as "an upper portion of the vertical semiconductor channel").

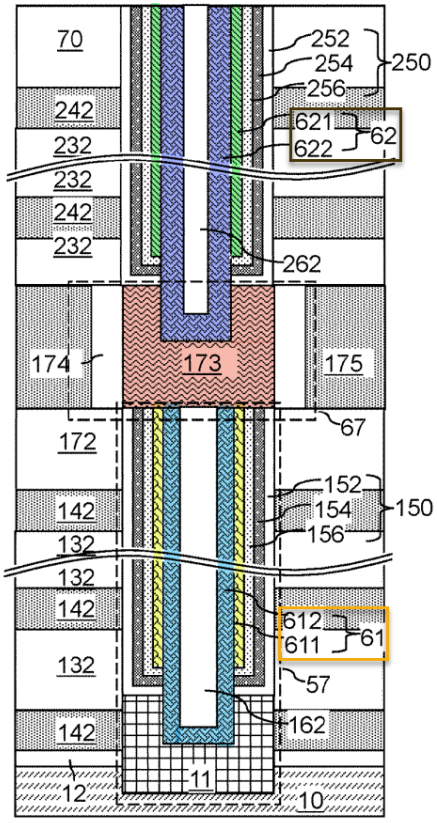


FIG. 21E

Costa, Fig. 21E. Costa even describes that "[t]he at least one doped semiconductor portion [173] … provide[s] a robust alignment and connection scheme between each pair of a first memory opening fill structure 57 and a second memory opening

fill structure 77." Costa, ¶324. Any attempt by Petitioner to widen semiconductor portion 173 beyond the aperture of the through hole below it would be an exercise in hindsight.

92. In sum, Petitioner fails to make any obviousness allegations for limitations [11.H] and [1.G]. *See supra* Section VII.A.4. Petitioner also presents no evidence or expert testimony to support a motivation to modify Costa to render obvious limitations [11.H] or [1.G]. Even if Petitioner did try to modify Costa to render obvious limitations [11.H] or [1.G] to make semiconductor portion 173 wider (which Petitioner did not), it would be based on hindsight, using the '291 Patent as a roadmap. In my opinion, a POSITA would not modify Costa to widen semiconductor portion 173 absent hindsight, at least because "[t]he at least one doped semiconductor portion [173] … provide[s] a robust alignment and connection scheme between each pair of a first memory opening fill structure 57 and a second memory opening fill structure 77." Costa, ¶324.

IX. Conclusion

All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. Further, I am aware that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001. I declare under penalty of perjury that the foregoing is true and correct.

Executed May 12, 2025 in College Station, Texas.



Dr. Sunil Khatri