

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner
v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00244
U.S. Patent No. 10,886,291

**PETITIONER'S OPPOSITION TO PATENT OWNER'S BRIEF ON
DISCRETIONARY DENIAL**

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1001	U.S. Patent No. 10,886,291 to Lu et al. (“the ’291 Patent”)
1002	File History of U.S. Patent No. 10,886,291 (“the ’291 FH”)
1003	Declaration of Dr. Sanjay K. Banerjee (“Banerjee”)
1004	<i>Curriculum Vitae</i> of Dr. Sanjay K. Banerjee
1005	U.S. Patent Publication No. 2018/0182771 A1 to Costa et al. (“Costa”)
1006	U.S. Patent Publication No. 2016/0204117 A1 to Liu et al. (“Liu”)
1007	U.S. Patent Publication No. 2015/0060979 A1 to Lee et al. (“Lee”)
1008	U.S. Patent Publication No. 2017/0179026 A1 to Toyama et al. (“Toyama”)
1009	Aritome, “NAND Flash Memory Technologies” (2016)
1010	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
1011	Micheloni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)
1012	U.S. Patent No. 10,475,737 to Tang et al.
1013	Micheloni, “3D Flash Memories” (2016)
1014	U.S. Patent No. 9,853,046 to Lu et al.
1015	Excerpt from YMTC’s Exemplary Infringement Claim Chart for U.S. Patent No. 10,886,291 (Ex. C-1 to Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024) (“Ex. C-1, YMTC’s Contentions”) [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]
1016	U.S. Patent No. 9,245,962 to Yang et al.
1017	U.S. Patent No. 10,283,518 to Lee et al.

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1018	Stavitski et al., “Specific contact resistance measurements of metal-semiconductor junctions,” <i>2006 IEEE International Conference on Microelectronic Test Structures</i> , Austin, TX, USA, 2006, pp. 13-17
1019	Fasoli et al., “Overview and status of bottom-up silicon nanowire electronics,” <i>Materials Science in Semiconductor Processing</i> , Vol. 15, Issue 6, 2012, pp. 601-614
1020	U.S. Patent Publication No. 2015/0264548 A1 to Lee et al. (“Lee 548”)
1021	U.S. Patent No. 9,530,866 to Zhang et al.
1022	Plummer et al., “Silicon VLSI Technology: Fundamentals, Practice and Modeling” (2000)
1023	Certified Translation of KR 101487746 B1 to Lee et al. (including original Korean patent document)
1024	U.S. Patent Publication No. 2017/0154892 to Oh
1025	Minute Order (case schedule), Dkt. No. 141, dated September 18, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1026	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1027	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, LTD.’s Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
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1029	Declaration of Jared Bobrow in Support of Petitioner’s Motion for Admission <i>Pro Hac Vice</i>
1030	Press Release, Micron, Micron and Intel Unveil New 3D NAND Flash Memory (Mar. 26, 2015) (“Micron ‘3D NAND Flash Memory’ Press Release”)
1031	Press Release, Micron, <i>Micron and WekaIO Win Best of Show Award at the Flash Memory Summit 2019</i> (Aug. 29, 2019) (“Micron ‘Best of Show Award’”)
1032	Micron Technology, Inc., Annual Report (Form 10-K) (Oct. 4, 2024)
1033	Ministry of Industry and Information Technology, <i>The Ministry of Industry and Information Technology Officially Announced the “National Integrated Circuit Industry Development Promotion Outline”</i> (Jun. 26, 2014) (https://www.cac.gov.cn/2014-06/26/c_1111325916.htm) (“National IC Development Promotion Outline”)
1034	Certified English Translation of Ex. 1033 (National IC Development Promotion Outline)
1035	Karen M. Sutter et al., Cong. Rsch. Serv., R47558, <i>Semiconductors and the CHIPS Act: The Global Context</i> (2023)
1036	Alex He, <i>Case Study: From Paper Tiger to Real Tiger? The Development of China’s Semiconductor Industry</i> , CENTRE FOR INT’L GOVERNANCE INNOVATION 14 (2021)
1037	State-Owned Assets Supervision and Administration Commission of the State Council (SASAC), <i>Definition of “State-Owned Enterprise”</i> (July 4, 2019) (https://www.sasac.gov.cn/n2588040/n2590387/n9854212/c11647665/content.html) (“SASAC Definition”)
1038	Certified English Translation of Ex. 1037 (SASAC Definition)

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1039	China’s State Council, <i>Notice of the State Council on Issuing “Made in China 2025”</i> (May 19, 2015) (https://www.gov.cn/zhengce/content/2015-05/19/content_9784.htm) (“Made in China 2025”)
1040	Certified English Translation of Ex. 1039 (Made in China 2025)
1041	Karen M. Sutter, Cong. Rsch. Serv., R46767, <i>China’s New Semiconductor Policies: Issues for Congress</i> (2021)
1042	Liu Yuanchun et al., <i>Accelerating the Realization of High-Level Scientific and Technological Self-Reliance</i> , PEOPLE (July 15, 2024) (http://paper.people.com.cn/zgjjzk/html/2024-07/15/nw.zgjjzk_20240715_1-05.htm) (“People’s Paper Article”)
1043	Certified English Translation of Ex. 1042 (<i>People’s Paper Article</i>)
1044	YMTC, <i>Yangtze Memory Technologies Co. Ltd. Officially Established</i> (Aug. 1, 2016) (https://www.ymtc.com/cn/news/28.html) (“YMTC Press Release”)
1045	Certified English Translation of Ex. 1044 (YMTC Press Release)
1046	Testimony of Stephen Ezell (VP, Global Innovation Policy – Information Technology & Innovation Foundation) Before the U.S.-China Economic and Security Review Commission (Apr. 14, 2022)
1047	Yahoo! Finance, South China Morning Post, Tech War: China’s Top Memory Chip Maker YMTC Gets US\$7 Billion From State-Backed Investors (Mar. 2, 2023) (“Yahoo! Article”)
1048	Baidu, <i>Yangtze Memory Increases Capital and Expands Capacity to RMB 100 Billion, Big Fund Phase II Forms a Partnership with Local Hubei State-owned Assets</i> (Mar. 2, 2023) (https://baijiahao.baidu.com/s?id=1759256650733024656&wfr=spider&for=pc) (“Baidu Article”)
1049	Certified English Translation of Ex. 1048 (<i>Baidu Article</i>)

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1050	YMTC’s Rule 7.1 Corporate Disclosure Statement, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , Case No. 5:23-cv-05792-VKD (N.D. Cal. Nov. 9, 2023)
1051	Lianhe Credit Rating Co., Ltd., Wuhan Optics Valley Financial Holding Group Co., Ltd., 2024 Tracking Rating Report (Jun. 28, 2024) (“2024 Tracking Rating Report”)
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1055	Sina Finance, <i>Yangtze Memory’s “Double 11 Performance” Surpassed Samsung’s for the First Time</i> (Nov. 12, 2024) (https://finance.sina.com.cn/roll/2024-11-12/doc-incvupap6483110.shtml) (“Sina Finance Article”)
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1059	Wuhan University of Science and Technology, <i>Yangtze Memory Technologies Co., Ltd.</i> 2020 Campus Recruitment Introduction (Sept. 10, 2019) (https://wust.91wllm.cn/teachin/view/id/97310) (“Wuhan Univ. of Sci. and Tech., YMTC 2020 Campus Recruitment Introduction”)
1060	Certified English Translation of Ex. 1059 (Wuhan Univ. of Sci. and Tech., YMTC 2020 Campus Recruitment Introduction)
1061	China University of Petroleum, <i>Yangtze Memory 2025 Campus Recruitment</i> (Feb. 20, 2025) (https://career.cup.edu.cn/job/view/id/618140) (“China Univ. Of Petroleum, YMTC 2025 Campus Recruitment”)
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1063	Yoko Kubota et al., <i>U.S. Chip Equipment Suppliers Suspend Business Activities at Yangtze Memory</i> , WALL STREET JOURNAL CHINA (Oct. 13, 2022) (https://cn.wsj.com/articles/美国供应商暂停在中国长江存储科技的业务活动-11665617406) (“WSJ China Article”)
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1065	Letter from Michael T. McCaul, Member of Congress, and Bill Hagerty, U.S. Senator, to the Honorable Gina Raimondo, U.S. Commerce Secretary (July 12, 2021)
1066	Demetri Sevastopulo, <i>Bipartisan Group Urges US Blacklist for “Beijing-Directed” Chipmaker</i> , FINANCIAL TIMES (Sept. 20, 2022) (https://www.ft.com/content/173eb5b7-c211-4fa8-af8e-93382ed12836) (“Financial Times Article”)
1067	U.S. Senator Charles E. Schumer, <i>With Chinese Chip Companies Threatening National Security And Jobs, Schumer Announces President Has Heeded His Call And Will Add YMTC - One Of China’s Leading Chip Makers - To A Trade Blacklist; Administration Action Will Strengthen National Security And Protect The Domestic Chip Industry</i> (Dec. 16, 2022) (“Schumer Statement”)

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1068	U.S. Department of Defense, <i>DOD Releases List of People’s Republic of China (PRC) Military Companies in Accordance with Section 1260H of the National Defense Authorization Act for Fiscal Year 2021</i> (Jan. 31, 2024) (https://www.defense.gov/News/Releases/Release/article/3661985/dod-releases-list-of-peoples-republic-of-china-prc-military-companies-in-accord/)
1069	U.S. Department of Defense, <i>Entities Identified as Chinese Military Companies Operating in the United States in accordance with Section 1260H of the William M. (“Mac”) Thornberry National Defense Authorization Act for Fiscal Year 2021 (Public Law 116-283)</i> (https://media.defense.gov/2024/Jan/31/2003384819/-1/-1/0/1260H-LIST.PDF)
1070	<i>Oversight of the USPTO: Hearing Before the Subcomm. On Intellectual Property</i> , 118th Cong. (2023) (Testimony of Katherine Vidal, Undersecretary of Commerce for IP and Director of USPTO)
1071	China’s State Council, <i>Notice of the State Council on Issuing Policies to Promote the High-quality Development of the Integrated Circuit Industry and Software Industry in the New Era</i> (Aug. 4, 2020) (https://www.gov.cn/zhengce/content/2020-08/04/content_5532370.htm) (“State Council Notice on Policies to Promote Development of IC”)
1072	Certified English Translation of Ex. 1071 (State Council Notice on Policies to Promote Development of IC)
1073	Declaration of Karen Lee, Translator (Mar. 10, 2025)
1074	Declaration of Fei-Xue Qian, Translator (Mar. 10, 2025)
1075	Order Granting Motion to Stay Case Pending <i>Inter Partes</i> Review, <i>Yangtze Memory Techs. Co., Ltd. v. Micron Tech., Inc. et al.</i> , Case No. 3:23-cv-05792-RFL, Docket No. 243 (N.D. Cal. Mar. 14, 2025)

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1076	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.'s Disclosure of YMTC I Asserted Claims and Infringement Contentions, <i>Yangtze Memory Techs. Co., Ltd. v. Micron Tech., Inc. et al.</i> , Case no. 23-cv-05792-RFL (N.D. Cal. May 6, 2024)
1077	U.S. Patent No. 11,482,532 to Lu et al.
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I. INTRODUCTION

Petitioner Micron submits this opposition to Patent Owner YMTC's Brief on Discretionary Denial (Paper 14, "DD Brief"). This IPR—along with all the other still-pending IPRs/PGR Micron filed against YMTC's patents—should proceed to a merits decision.

The public has a strong interest in reviewing the patents that YMTC has asserted. Micron—the target of YMTC's infringement allegations—is a U.S.-based semiconductor memory innovator and manufacturer. Indeed, it is the only such U.S. manufacturer. YMTC is a Chinese-state owned entity that operates to further the Chinese government's goal of expanding its global influence in the semiconductor field. IPR here is not only appropriate, but necessary to ensure that an entity operating at the behest of a foreign state is not asserting invalid patents to improperly suppress, undermine, and capture an important part of the U.S. economy.

YMTC argues that the mere fact that it chose to assert 19 patents against Micron in district court somehow warrants denial of IPR. The Board, however, routinely handles more than a thousand post grant filings a year. Micron's filings represent only a very small percentage of this. Moreover, this is a problem of YMTC's own making. If it did not want its patents subject to post-grant proceedings, it should have been more circumscribed when selecting which patents to assert in the first place. Instead, YMTC chose to assert 19 patents. YMTC's complaint that

Micron cannot invoke the AIA to defend itself against this type of onslaught rings hollow. Asserting numerous patents does not (and cannot) operate as a get-out-of-the-PTAB free card. Holding otherwise will incentivize other patent holders to flood district courts with excessive numbers of patent infringement allegations.

The *Fintiv* factors also heavily favor institution. The district court stayed the parallel district court action at least until the completion of all Micron IPRs/PGR. Thus, no trial (or any other district court work) will take place until well after the IPRs/PGR conclude. Moreover, Micron's IPRs/PGR will undeniably simplify the complex issues before the district court. The number of asserted YMTC patents is likely to be substantially reduced. And the Board's findings—regardless of whether they favor Micron or YMTC—will inform the district court's later analysis. Among other things, the IPR/PGR proceedings will prevent YMTC from making the type of ambiguous, overbroad, and tenuous allegations that currently permeate its complaint and infringement contentions. Indeed, the likelihood of issue simplification motivated the district court to stay the case in the first place.

Additionally, the mere fact that Petitioner submitted an expert declaration does not merit denial of IPR. The Petition's grounds are so clear and straightforward that they can be understood without expert testimony. The testimony accompanying the Petition simply serves to confirm that the Petition properly interpreted the prior art. Petitioner's expert testimony is no different from the testimony accompanying

almost every filed IPR/PGR: it discusses a POSITA's background knowledge and explains the motivations a POSITA would have had in view of the prior art's teachings.

For the reasons explained in this paper—and in the Petition itself—the Director should refer the petition to the merits panel for an institution decision.

II. ARGUMENT

No good reason exists for the Director to exercise its discretion to deny institution. In fact, the Director has every reason to reject YMTC's arguments and institute this proceeding.

A. Compelling Economic and National Security Interests Favor Institution

As explained in recent guidance, the Director considers “[c]ompelling economic, public health, or nationality security interests” when deciding whether to exercise its institution discretion. *See* March 26, 2025 Interim Processes for PTAB Workload Management (“March 26, 2025 Processes”). This case presents just such issues.

1. *Factual Background*

a) Micron Is a Pioneer in NAND Flash Memory

The '291 patent—just like the most of the other YMTC patents¹ that Micron challenges—relates generally to 3D NAND flash memory. *See* Ex. 1001, 1:24-29. NAND flash memory is a crucial component in the semiconductor ecosystem. It is a type of memory that does not lose data when it loses power. Conventional NAND stores data in memory cells laid out in an array of rows and columns. Historically, NAND arrays were laid out two-dimensionally in a single level. But, as demand for data storage grew, the semiconductor industry developed multi-level NAND devices, in which multiple levels of NAND memory cells are stacked vertically on top of each other. This is 3D NAND. By stacking levels vertically, 3D NAND dramatically increases memory storage capacity compared to conventional NAND. Connection with the stacked levels is typically accomplished using a staircase structure.

Micron—headquartered in Boise, Idaho—began its pioneering work in developing 3D NAND products more than fifteen years ago. Micron invested

¹ The '941 patent relates more generically to NAND, but does include 3D NAND embodiments (IPR2025-00190), and the '164 patent relates to ESD circuitry generally (IPR2025-00118).

billions of dollars and years of effort towards researching, developing, and manufacturing 3D NAND technology. As part of this effort, Micron filed for (and later obtained) thousands of U.S. patents on this technology starting at least by 2010. This culminated in Micron launching its first 3D NAND product on March 26, 2015. *See* Ex. 1030 at 1-2.

Since 2015, Micron has continued to innovate its 3D NAND technology by developing memory products with more and more capacity and capabilities. Micron has received numerous awards and widespread recognition for its innovation (*see, e.g.*, Ex. 1031 at 1), and is a leading innovator—both in the U.S. and globally—of semiconductor memory devices, with over 57,000 patents (*see* Ex. 1032 at 2). In fact, Micron remains the only U.S.-based manufacturer of semiconductor memory devices.

YMTC did not file the earliest application identified on the face of '291 patent until 2017. *See* Ex. 1001, Cover.

b) The Chinese Government's Control of Its Semiconductor Industry

YMTC's role in the global semiconductor industry (and the strategic, state-backed initiative of which it is part) contrasts sharply with that of Micron. For more than a decade, the Chinese government has invested heavily in the semiconductor industry within its borders and set policies for Chinese semiconductor companies. In June 2014, China's State Council announced its "National Integrated Circuit

Industry Development Outline” with the “goal of establishing a world-leading semiconductor industry in all areas of the integrated circuit supply chain.” *See* Ex. 1034 at 1; Ex. 1035 at 19-20. It sought to remove “bottleneck[s] of industrial development,” establish “a national integrated circuit industry development leading group ... for the overall coordination of the integrated circuit industry,” and create “a financing platform and policy environment.” Ex. 1034 at 1-2; Ex. 1035 at 19-23.

The Chinese government then created the “National Integrated Circuit Industry Investment Fund” (or “Big Fund”) and raised 138.7 billion yuan from multiple government and state-owned enterprises,² including China’s Ministry of Finance. Ex. 1036 at 5; *see id.* at 3-7. The Big Fund aimed to “***support[] the integrated circuit manufacturing field,***” “implement mergers,” and “***standardize***

² According to China’s State Council, the term “state-owned enterprise” includes “state-owned enterprises, state-owned companies and state-owned capital holding companies that the State Council and local people’s governments respectively perform the duties of investors on behalf of the state, including enterprises supervised by central and local state-owned assets supervision and administration agencies and other departments at the same level and enterprises formed by their investment at each level.” Ex. 1038.

corporate governance.”³ Ex. 1034 at 2.

In May 2015, China’s State Council launched its “Made in China 2025” initiative. *See* Ex. 1040. The initiative set an ambitious ten-year roadmap for China to become a global leader in high-tech industries and officially solidified the semiconductor industry as one of the Chinese government’s targets. *Id.* at 1-13 (e.g., “[W]e must seize the current rare strategic opportunities, actively respond to challenges, strengthen overall planning, highlight innovation-driven, formulate special policies, give full play to institutional advantages, mobilize the whole society to work hard, rely more on Chinese equipment and Chinese brands, ... and complete the strategic task of transforming Chinese manufacturing from big to strong.”), 30.

The “Made in China 2025” initiative also outlined a comprehensive set of strategic goals, emphasizing the government’s central role in control and financing.⁴ *Id.* at 8-9 (e.g., “Market-led, **government-guided**. Comprehensively deepen reform, give full play to the decisive role of the market in resource allocation, strengthen the dominant position of enterprises, and stimulate the vitality and creativity of

³ All emphases added unless otherwise noted.

⁴ *See also* Ex. 1072 at 4-5 (“Strengthen services and guidance for the construction of major integrated circuit projects [and] orderly guide and regulate the development of the integrated circuit industry”), 8-9.

enterprises. ***Actively transform government functions, strengthen strategic research and planning guidance***, improve relevant support policies, and create a good environment for enterprise development.”), 37, 39, 41-44 (e.g., “***Deepen the reform of state-owned enterprises [and] improve the corporate governance structure....***”).

The Chinese government has aggressively sought foreign (including U.S.) patent protection in support of its goal to increase its control over the global semiconductor market. Indeed, the U.S. Congressional Research Service (CRS) explained:

China’s policies feature ***a substantial and central role for the government in directing and financing Chinese businesses to obtain foreign IP*** related to semiconductors. The Chinese government uses production targets; subsidies; tax preferences; trade and investment barriers (including pressure to engage in joint ventures); and discriminatory antitrust, IP, procurement, and standards practices. The policies seek to leverage China’s central role in global consumer electronics manufacturing and potential as a semiconductor production hub to incentivize and pressure foreign companies to localize production, share technology, and partner with the Chinese government and affiliated entities.

Ex. 1041 at 6; *see also id.* at 7-11.

c) YMTC Is China’s State-Owned NAND Memory Company

In pursuit of its “Made in China 2025” initiative, the Chinese government tasked Tsinghua Unigroup, a state-controlled company, with leading the country’s memory chip development. *See* Ex. 1043 at 2; Ex. 1046 at 7. On July 26, 2016, Tsinghua Unigroup—jointly with the Big Fund and municipal governments—founded YMTC to develop NAND memory. Ex. 1045 at 1. This joint venture initially invested more than \$24 billion (USD) in YMTC. *See* Ex. 1046 at 7. Since then, the Chinese government has continued to invest heavily in YMTC. In 2023, for example, the Chinese government invested another \$7 billion (USD) through various investment vehicles, such as the second phase of its Big Fund. Ex. 1047 at 1; Ex. 1049 at 1-2.

The Chinese government not only invests heavily in YMTC, but it also owns and controls YMTC. YMTC is wholly owned by one parent corporation: Yangtze Memory Technologies Holding Co., Ltd. (“YMTC Holding”). *See* Ex. 1050 at 2. And YMTC Holding is owned by the following state-owned enterprises (as of March 12, 2025):

Shareholder	Ownership
Hubei Changsheng Development Co., Ltd. (湖北长晟发展有限责任公司), a state-owned enterprise	~29%

Shareholder	Ownership
Wuhan Xinfei Technology Investment Co., Ltd. (武汉芯飞科技投资有限公司), a state-owned enterprise	~27%
National IC Industry Investment Fund Co., Ltd. (国家集成电路产业投资基金股份有限公司), a state-owned enterprise	~13%
National IC Industry Investment Fund Phase II Co., Ltd. (国家集成电路产业投资基金二期股份有限公司), a state-owned enterprise	~12%
Hubei Science & Technology Investment Group Co., Ltd. (湖北省科技投资集团有限公司), a state-owned enterprise	~10%
Hubei Guoxin Industry Investment Fund Partnership (L.P.) (湖北国芯产业投资基金合伙企业 (有限合伙)), a state-owned enterprise	~6%
Yangtze Industrial Investment Group Co., Ltd. (长江产业投资集团有限公司), a state-owned enterprise	~3%
Total	100%

See Ex. 1052 at 9-10; Ex. 1056 at 1 (“Yangtze Memory is a state-controlled enterprise ... [where] all seven shareholders of Yangtze Memory Technologies Holdings Co., Ltd. are state-owned assets.”); Ex. 1049 at 1-2 (“Hubei Changsheng Development Co., Ltd. is held by Hubei Integrated Circuit Industry Investment Fund, Wuhan Optics Valley Finance and Yangtze River Industrial Investment Group”—with the actual “controller behind the scenes [being the governmental] Administration of Wuhan East Lake High-tech Development Zone.... [The] actual

controller of Yangtze River Industrial Investment Group is the Hubei Provincial State-owned Assets Supervision and Administration Commission.... [The] actual controller of Hubei Guoxin Industry Investment Fund Partnership (Limited Partnership) is the Wuhan State-owned Assets Supervision and Administration Commission, and the actual controller of Hubei Science [&] Technology Investment Group Co., Ltd. is the [governmental] Administration of Wuhan East Lake High-tech Development Zone.”). All shareholders (listed above) are state-owned enterprises and, therefore, YMTC Holding and YMTC are state owned. See Ex. 1052 at 9-10; Ex. 1056 at 1; Ex. 1049 at 1-2.

This ownership structure and the Chinese government’s significant investment (*i.e.*, tens of billions of U.S. dollars) clearly show that YMTC serves the Chinese government’s semiconductor strategy and operates under the direction and control of the Chinese government. Indeed, China’s State Council has described YMTC as a “state-owned enterprise.” Ex. 1054 at 2. And Chinese media outlets and Chinese universities identify YMTC as a “state-owned enterprise” or “state-controlled enterprise.” Ex. 1056 at 1 (***“Yangtze Memory [Technologies, Inc.] is a state-controlled enterprise”***); *see also, e.g.*, Ex. 1058 at 1 (***“Nature of [YMTC]: State-owned enterprise”***); Ex. 1060 at 1 (same); Ex. 1062 at 1 (same); Ex. 1064 at 1-2 (***“China’s state-owned enterprise Yangtze Memory Technologies Co. Ltd.... Yangtze Memory is controlled by the Hubei Provincial Government and the China***

National Integrated Circuit Industry Investment Fund.”).

d) Bipartisan U.S. Policymakers Agree That the Chinese Government Controls YMTC

U.S. policymakers consistently highlight the Chinese government’s ownership and control over YMTC. In July 2021, U.S. Senator Bill Hagerty and U.S. Representative Michael McCaul urged the U.S. Commerce Secretary to add YMTC to the Department of Commerce’s Entity List⁵ because it “has clear ties to the Party-state and military and plays a significant role in CCP plans to control the supply chain for a strategic dual-use sector.” Ex. 1065 at 1-2. They explained that:

YMTC is the PRC’s state-owned national champion for memory chips — a type of semiconductor with defense, artificial intelligence, and aerospace applications. YMTC was created as a joint-venture by the National Integrated Circuit (IC) Industry Investment Fund, Tsinghua Unigroup (a state investment firm that is one of the IC Fund’s shareholders), the Hubei IC Industry Fund (a regional branch of the national IC Fund), and the Hubei Science and Technology Investment Group (an investment vehicle of the Wuhan Municipal Government

⁵ The “Entity List” identifies persons—including corporate entities—reasonably believed to be involved, or pose a significant risk of being or becoming involved, in activities contrary to the national security or foreign policy interests of the United States. See <https://www.bis.gov/licensing/guidance-on-end-user-and-end-use-controls-and-us-person-controls#End-usercontrols>

that provides capital investment, infrastructure and services for the PRC's strategic industries, including semiconductors).

Id.; see also Ex. 1066 at 2 (“The White House has described YMTC as a Chinese ‘national champion.’”).

In April 2022, Mr. Stephen Ezell, Vice President of Global Innovation Policy at the Information Technology and Innovation Foundation, testified before the U.S.-China Economic and Security Review Commission (which is a bipartisan legislative commission created by the U.S. Congress) on “U.S.-China Innovation, Technology, and Intellectual Property Concern.” Ex. 1046 at 1, 3. In his testimony, he explained:

[YMTC] is a Chinese state-controlled joint venture stood up from whole cloth by the National IC Industry Investment Fund, the state university-controlled fabless semiconductor firm Tsinghua Unigroup, and the Hubei Science and Technology Investment Group, supported by \$24 billion in initial government funding allocated for its initial Wuhan factory alone. In effect, YMTC is China's state-owned national champion for memory chips.

Id. at 7. Similarly, in September 2022, U.S. Senator Mark Warner stated it “has been clear for some time now that YMTC is ... a key part of the Chinese Communist party's goal of shifting control of global microelectronics to the PRC.” Ex. 1066 at 2. Similarly, in December 2022, U.S. Senator Charles E. Schumer called YMTC a “CCP-backed technology compan[y].” Ex. 1067 at 1.

Next, pursuant to Section 1260H of the William M. (Mac) Thornberry National Defense Authorization Act, the Secretary of Defense must identify entities that the Secretary “determines” to be a “Chinese military company” “based on the most recent information available.” H.R. 6395, 116th Cong. §1260H(a), (d) (2021). A “Chinese military company” refers to any entity that is “directly or indirectly owned, controlled, or beneficially owned by, or in an official or unofficial capacity acting as an agent of or on behalf of, the People’s Liberation Army or any other organization subordinate to the Central Military Commission of the Chinese Communist Party”—i.e., an entity that is owned and/or controlled by the Chinese government. *Id.* §1260H(d). On January 31, 2024, the Department of Defense identified YMTC as a “Chinese military compan[y].” Ex. 1068 at 1; Ex. 1069 at 1, 3; *see also* 90 Fed. Reg. 1105 (Jan. 7, 2025) (same).

2. *YMTC’s State-Owned Status Weighs in Favor of Institution*

The USPTO’s regulations governing IPR/PGR proceedings—including those controlling IPR/PGR institution—are intended to account for “the effect ... on the economy” and “the integrity of the patent system....” 35 U.S.C. §316(b). Consistent with this, as the former USPTO Director explained to Congress in 2023, “the USPTO is committed to an all-of-Government approach to leveraging IP rights to catalyze U.S. economic competitiveness and national security.” Ex. 1070 at 9. She further testified, “[t]he USPTO is working globally to strengthen the innovation, creativity,

and entrepreneurship ecosystem, to hold competitors to their agreements, to curb abuses and unfair practices, and to directly assist stakeholders facing IP issues abroad.” *Id.*

Proceeding to a merits decision in this IPR will further these goals. Accepting YMTC’s arguments, however, will frustrate them. Micron is the sole U.S.-based semiconductor memory manufacturer. Micron is currently the target of an expansive district court patent infringement action brought by YMTC involving 19 patents. YMTC is a Chinese-state owned and controlled company. As explained above, China has publicly explained that it intends to, among other things, leverage foreign intellectual property rights to increase its control over the global semiconductor market. Engaging in a full, comprehensive, and substantive review of YMTC’s patents will ensure that China is not improperly using U.S. patents—through its proxy YMTC—to target, impose costs on, and potentially extract monetary concessions on invalid and unenforceable patents from U.S.-based companies like Micron. This in turn furthers U.S. economic interests by ensuring continued, fair competition in the semiconductor field. Relatedly, it will ensure that the U.S. patent system operates to further U.S. economic and national security interests, as opposed to those of a foreign state and its proxy YMTC. This all weighs heavily in favor of institution.

B. The Large Number of Patents Asserted by YMTC Does Not Weigh Against Institution

None of YMTC's other arguments even remotely suggests any other course of action, and a merits decision is appropriate here.

YMTC begins its brief by discussing the supposedly "substantial burden" imposed on both it and the Board by Micron's "barrage" of IPR and PGR petitions. DD Brief, 1. According to YMTC, these petitions are meant to provide Micron with a "tactical advantage in district court" and somehow operate only to "harass[]" and "punish[]" YMTC. *Id.* Further, YMTC complains that instituting would unnecessarily consume the Board's "finite resources." *Id.*

As an initial matter, the Board handles over a thousand IPRs and PGRs every year. Micron's filings represent only a very, very small percentage of this total. This falls well short of imposing anything that could even remotely be characterized as a "substantial burden" on the Board.

Next, in complaining that it will be burdened by Micron's filings, YMTC has it backwards. Micron filed the number of IPRs/PGRs it did only because YMTC chose to assert an excessive number of patents (19 in total) and claims (more than 200) in district court. Thus, it was YMTC—not Micron—that improperly sought a "tactical advantage." By arguing for discretionary denial due to the large number of Micron IPRs/PGR, YMTC is attempting to prevent meaningful review of its many (and non-meritorious) patent allegations simply by asserting a large number of

patents. Micron, unsurprisingly, sought to defend itself against YMTC’s “barrage” both in district court and in the USPTO. The district court also refused to become bogged down by YMTC’s excessive assertions and instead stayed the case pending resolution of Micron’s IPR/PGR filings. *See* Ex. 1075 at 2 (noting that a stay will “simplify the issues” by reducing the number of “infringement, validity, and claim construction issues”). If YMTC did not want to defend multiple patents in IPR/PGR, it should have been more careful when selecting which patents to assert in the first place. This would have both allowed for more expeditious district court proceedings and reduced the number of IPR petitions Micron filed. Once again, YMTC made its bed and must lie in it.

Nor does the fact that Micron occasionally filed multiple petitions against certain YMTC patents have any bearing on whether institution is appropriate here. This—like the total number of filed IPRs/PGRs—was necessitated by YMTC’s actions. Rather than asserting only a single claim (or small number of claims) per patent, YMTC chose to assert many claims. Indeed, even as the district court action progressed from the pleadings stage into early fact discovery, YMTC continued to expand the total number of asserted claims. *See, e.g.*, Ex. 1027 at 2 (asserting more than 150 claims across 11 patents); Ex. 1076 at 2 (asserting more than 50 claims across 8 patents). It was this expansion that necessitated additional IPR/PGR filings.

Declining to address Micron’s petitions on the grounds that YMTC asserted numerous patents would serve little purpose besides improperly rewarding YMTC for its chosen litigation tactic. Even more perniciously, however, were the Board to agree with YMTC, the Board would incentivize other patent owners to behave similarly. Rather than limiting and focusing their district court assertions, patent owners will be motivated to assert even more patents in district court in the hopes of similarly avoiding Board review. The Director should discourage this type of gamesmanship and forum shopping—which has the potential to further burden district courts with reams of unnecessary allegations. The most straightforward way to do so is to strongly and unambiguously reject YMTC’s argument here: the volume of IPRs filed does not (and cannot) have any bearing on whether institution is appropriate, particularly when that volume was patent owner’s own creation.

C. The District Court Has Deferred to the PTAB

YMTC next argues that this IPR is “unlikely to result in a commensurate simplification of the issues before the District Court.” DD Brief, 12. Relatedly, it posits that the district court—and not the Board—is better situated to “manag[e]” the scope of the parties’ dispute. *See id.* at 15-16.

The district court arrived at the opposite conclusion when it stayed the co-pending district court case. In particular, the district court explained that “staying the case pending IPR will simplify the issues.” Ex. 1075 at 2. Among other things,

the district court noted that Micron’s IPRs/PGR will likely entirely eliminate patents from the case, resulting in simplification of the “infringement, validity, and claim construction issues” confronting the court. *Id.* at 2. Moreover, the district court noted that many of YMTC’s patents embrace “overlapping subject matter.” *Id.* So each Board decision has the potential to resolve issues spanning across multiple patents. *See id.*

While the district court did issue a series of orders requiring YMTC to reduce the number of asserted claims as YMTC notes in its brief (*see* DD Brief, 12), this fact alone does not merit a discretionary denial of IPR/PGR. Micron’s IPRs/PGR cover a larger number of claims than will ultimately be at issue in district court because YMTC itself chose to assert these claims in the first instance in its district court infringement contentions. Moreover, most of the independent claims addressed by Micron’s IPRs/PGR—which will likely be the focus of any disputes between the parties if the Board institutes this and Micron’s other proceedings—currently remain at issue in district court. YMTC’s argument is also self-contradictory. If Micron had waited to file until after the district court had narrowed the number of asserted claims, YMTC presumably would have argued that Micron’s petitions should be discretionarily denied because they were filed too late. Given this, it cannot now argue that filing early (and addressing the claims at issue at the time when doing so) somehow also merits a discretionary denial. Agreeing with

YMTC would be nonsensical: both early and late IPR/PGR filings would be deemed unworthy of review on the merits.

D. The *Fintiv* Factors Weigh Strongly In Favor of Institution

The Director also continues to evaluate “the discretionary considerations enumerated in existing Board precedent” including *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper No. 11 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv*”). March 26, 2025 Processes at 2. These considerations make it abundantly clear that Micron’s IPR petition should be reviewed on the merits. In particular: the district court has stayed the parallel district court case, no trial is currently scheduled, no substantive district court work has occurred, the stay ensures that there will be little overlap, and the petition is substantively strong.

1. *The District Court Litigation Is Stayed*

The district court has stayed the case pending IPR/PGR. *See* Ex. 1075. By issuing a stay, the district court indicated that it prefers the Board to address unpatentability of YMTC’s patents in the first instance. This weighs strongly in favor of institution. *See Fintiv* at 12.

Patent Owner argues that if the Director declines to institute, it “intends to seek to lift the District Court stay and resume the litigation.” DD Brief, 17. No basis exists for doing so any time soon. The district court ordered that the case be stayed until “the completion of all IPR proceedings.” Ex. 1075 at 1, 3. The PTAB has

already instituted several Micron IPRs. *See, e.g.*, IPR2024-00788, -00789, -00790, -00791, -00792, -00794, -00795, -00909, -00911, and IPR2025-00034. The most recent of these will not reach final decision until May 2026. *See* IPR2025-00034, Paper 19. Other IPRs are still in the pre-institution phase, with institution decisions not due for several months. *See, e.g.*, IPR2025-00117, -00118, -00119, -00189, -00191, -00190, -00228, -00244, -00294, and -00245. Given this, IPRs/PGR involving YMTC's patents will be ongoing for quite some time. The district court's stay will remain in place throughout this process. Any suggestion by YMTC to the contrary is pure speculation. This factor weighs heavily in favor of institution.

2. *No Trial Is Scheduled*

Next, because the district court case is stayed, no trial date is currently scheduled. As a result, if IPR is instituted, proceedings before the Board will be completed long before any potential district court trial. YMTC references the district court's previously scheduled June 2026 filing date. *See* DD Brief, 17. But the district court vacated that date, and it no longer applies. *See generally* Ex. 1075. And as the case is currently stayed, once the stay is eventually lifted, it will take more than a year (if not years) of further work before the parties will be ready for trial. This also weighs strongly in favor of institution.

3. *Little Substantive Progress Has Been Made*

Here, YMTC chooses to argue about when this case would have gone to trial had the district court not stayed the case (DD Brief, 14-17), however this hypothetical is irrelevant as the district court case is stayed until the completion of all IPR/PGR proceedings. Ex. 1075 at 1, 3. As explained in its stay order, “the litigation is in an early stage.” *Id.* at 1. “Fact discovery” remained open and “the parties had not yet taken a single deposition.” *Id.* “Claim construction briefs [had] not yet been filed....” *Id.* So, while the parties had engaged in some fact discovery, almost all substantive work—including depositions, claim construction briefing, expert discovery, and dispositive motion briefing—remained to be done. None of this work will occur until after the district court’s stay is lifted. This also weighs in favor of institution. *See Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative).

While YMTC makes much of the fact that it was “forced to defend against” various discovery motions (*e.g.*, DD Brief, 17-19), this was also a problem of its own making. YMTC aggressively pursued overbroad, extraordinarily burdensome, and irrelevant discovery from Micron. At the same time, it largely refused to provide any meaningful productions of its own. This lopsided approach predictably led to discovery briefing. Moreover, the parties’ briefing focused on the scope of discovery. The fact that back-and-forth briefing regarding discovery scope was still

ongoing at the time of the stay (*see, e.g.*, Ex. 1075 at 2-3 (referencing still pending motions)) further evinces the parties' lack of meaningful progress and the amount of work that remains in district court. Rather than finishing the discovery process, the parties were still in the process of debating what fact discovery would entail.

The Board also has explained that institution is appropriate where "the petitioner filed the petition expeditiously...." *Fintiv* at 11. Here, Petitioner proceeded with diligence, filing only months after being served with the complaint. *See* Ex. 1028. This, just like the early stage of the district court action, also weighs in favor of institution.

4. *The Stay Minimizes Any Issue Overlap*

YMTC argues that "[t]here is substantial overlap" between this proceeding and the district court action. DD Brief, 20. This, however, entirely ignores that the impact of the district court's stay. The district court action will not resume until all of Micron's IPRs conclude. Because of this, in the event the Board institutes and renders a final written decision, Micron will be prevented from asserting the petition's grounds (or grounds it reasonably could have included in the petition) in district court. There will be no overlap at all. Moreover, even if the district court were to lift the stay for some reason (it will not be), Micron stipulated in the Petition that it will not advance the Petition's grounds in district court. *See* Petition at 11. This all weighs in favor of institution. *See Sand Revolution*, 11-12.

5. *Party Overlap*

Both Petitioner and Patent Owner are parties in the parallel proceeding. This, however, is of little moment as parallel proceedings often result in party overlap.

6. *Other Circumstances*

Petitioner submits that its petition has significant substantive merit. It is premised on clear, understandable prior art that the Patent Office did not previously consider. *See generally* Pet.

E. Expert Testimony Accompanying the Petition

YMTC argues that the Petition’s “extensive reliance on expert testimony indicates that its assertions are better resolved in district court.” DD Brief, 23. Once again, the district court disagreed: it deferred to the Board and stayed the district court case. *See* Ex. 1075. In doing so, the district court signaled its belief that it is more appropriate for the **Board** to assess Micron’s arguments first.

Petitioner recognizes that, after it filed its IPR, the Board recently issued guidance stating that the “extent of the petition’s reliance on expert testimony” may play a role in the Board’s institution decision. March 26, 2025 Processes at 2. As the below demonstrates, the IPR does not use expert testimony in a way that favors denial.

To start, the Petition demonstrates how Costa discloses the claim limitations in an incredibly straightforward way: for each limitation of the independent claims, it annotates the corresponding structure of a ’291 embodiment and then demonstrates

that Costa discloses (or renders obvious) the same. Pet., 90-92 (analyzing the limitations of claim 11 by reference to claim 1); Pet., 29-71 (analyzing the limitations of claim 1 by including disclosure from the specification for each limitation). Thus, the Petition alone demonstrates unpatentability. The expert declaration supplements this clear showing, for example, with focused technical explanation of how certain issues would have been understood, e.g., that Costa does not employ a self-aligned process. Pet., 51-53 (“Costa describes a non self-aligned process that would produce some degree of misalignment between, e.g., the target placement of the third channel structure and actual placement of the third channel structure ... a POSITA would have understood and found it obvious to ensure alignment ...”). But even there, the expert declaration cites specific disclosures in Costa, and other prior art, that support this. EX.1003, ¶¶ 197-203.

Patent Owner argues that the Board should discretionarily deny the petition because Petitioner and its expert rely “in part on a presumptive claim construction that the ’291 Patent’s use of ‘cover’ does not mean ‘completely cover.’” DD Brief, 23. Patent Owner makes this argument of view of limitation [11.G] of the ’291 patent, which requires “a third channel structure on the substrate covers a projection of the first through hole.” This argument fails.

The Petition merely states the obvious: “cover” does not mean “completely cover” because “cover”—without the qualifier “completely”—is broader than

“completely cover.” Indeed, the specification states “[i]n some embodiments, the projection of the first groove on the substrate 201 can completely cover the projection of the corresponding first through hole 205 on the substrate 201.” Ex. 1001, 20:33-38. In other words, the specification demonstrates that the applicant uses the phrase completely cover or similar language when that is what it means. *See also* Ex. 1077 (’532 Patent), claim 1 (“a size of the third channel structure along a lateral direction is larger than a top aperture of the first through hole”). What’s more, by using the phrase “[i]n some embodiments,” the specification embraces other embodiments, such as those that simply “cover.” Tellingly, PO does not even propose a different meaning of “cover.”

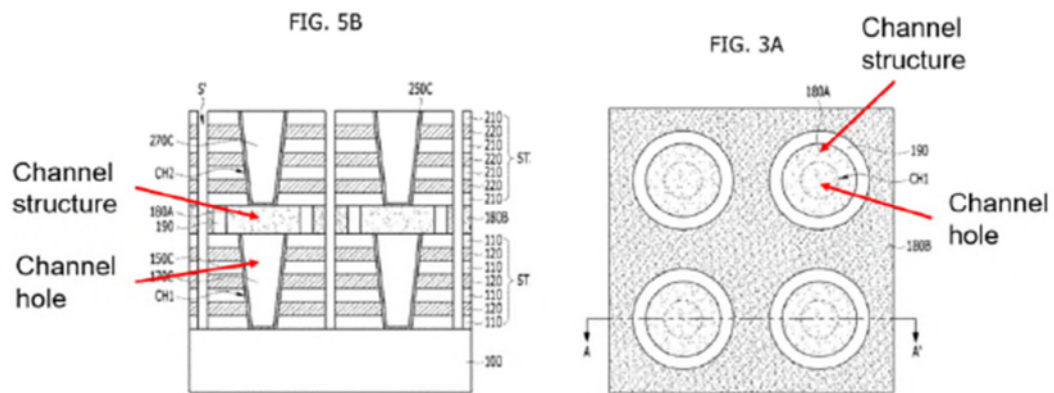
Next, Patent Owner argues that the Petition should be denied because “[p]etitioner relies on contradictory assumptions of its expert that are not based on the prior art asserted in Ground 1[.]” DD Brief, 24. In sum, Patent Owner faults Dr. Banerjee’s testimony because he recognizes that Costa’s goal is to align the channel structures, but that in practice, there will be misalignment. Patent Owner’s argument fails, and indeed, defies logic.

First, PO’s argument that Costa does not express as a goal to align structures (DD Brief, 24) is incorrect. As both the Petition and accompanying declaration recognize, Costa explains that “[t]he second-tier memory openings 249 are formed through the second tier structure (232, 242, 70, 265) in areas that **overlap** with the

joint-level memory opening fill structures 67, i.e., with the joint-level memory openings.” Pet., 60; Ex. 1003, ¶ 222 (both citing EX1005, [0191]) (emphasis added). Indeed, as Dr. Banerjee explains, Costa describes these openings as “joint” or “collective[]” because the goal is they overlap, as otherwise the two structures would not function. Ex. 1003, ¶¶ 202 (explaining the structures must electrically couple) 220 (explaining Costa’s references to “joint” and “collective[]”). Finally, PO’s assertion that Dr. Banerjee cites no support for this explanation is incorrect. DD Brief, 24. In addition to his citations to Costa, he explains with citation to prior art that while one can attempt to use “[p]recise mask alignment” to align structures, “[p]rocess variation” prevent perfect alignment. Ex. 1003, ¶ 201 (citing Exs. 1021-22).

Second, PO’s argument that Costa’s goal of aligning the structures contradicts that would be some misalignment (DD Brief, 24) fails because it contradicts Costa itself. Dr. Banerjee explains that Costa’s process is not self-aligned, meaning it relies on “[p]recise mask alignment” instead of structures that effectively force perfect alignment. Ex. 1003, ¶ 201. Fatal to PO’s argument is that Costa expressly recognizes the need to mitigate for “misalignment.” Ex. 1005, [0164]. As the Petition and the supporting expert declaration explain, accounting for this misalignment even when attempting to use precise mask alignment is exactly what the ’291 patent, Costa (¶ [0164]), and the other cited prior art do. Pet., 45-54 (citing,

e.g., Ex. 1024, [0061], “[T]o secure an overlap margin between the channel connection pattern 180A and the first channel hole CH1, the channel connection pattern 180A may have a larger width than the top surface of the first channel hole CH1.”); Ex. 1003 ¶¶ 175-205, 222, 405. The result is a wider structure, e.g., third channel structure, in which another structure, e.g., the second stacked layer, laterally overlaps such that when misalignment occurs, the structures still overlap and allow electrical coupling:



Pet., 53 (citing Ex. 1024, Figs., 5B, 3A); Ex. 1003 ¶ 203 (same). Accordingly, there is nothing contradictory about the Petition's expert declaration because it is well-known to add margin (i.e. additional overlap) to account for misalignment when you want to perfectly align structures in different tiers of a 3D NAND memory device.

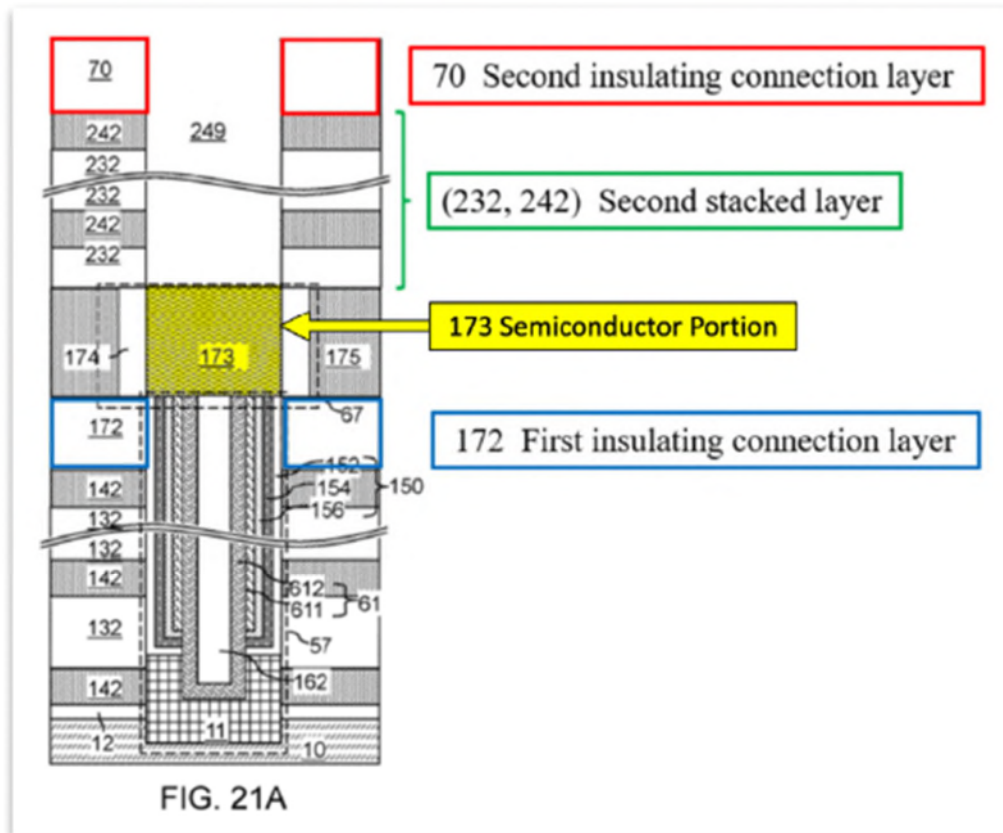
F. Petitioner Presents Strong Prior Art Positions That Favor Institution

The Patent Owner (“PO”) cannot legitimately dispute Petitioner’s strong showing that claims 1-5, 8-9, 11-12, and 14-19 are obvious over Costa. *See* Pet., 9-97. Indeed, in the face of this showing, PO disclaimed claims 1-5 and 8-9, implicitly acknowledging that the Costa prior art reference discloses or renders obvious the alleged invention of claim 1 along with many of its dependent claims. *See* POPR, 7. PO focuses only on whether Costa discloses a minor orientation detail of independent claim 11, namely, whether Costa discloses that the “second stacked layer” (a structure that PO admits Costa discloses) physically resides “**on**” the “third channel structure” (a structure that PO also admits Costa discloses). *Id.*, 21-36. To advance this argument, PO relies on an implicit construction of “on” as meaning “laterally overlapping.” POPR, 5-6. The Director should reject PO’s argument because it ignores the Petition’s showing about Costa’s disclosure of this limitation and relies on a legally erroneous claim construction. Even if the Director accepts PO’s characterization of the Petition and adopts PO’s erroneous construction, Costa still discloses the limitation.

1. *PO’s Argument Ignores the Petition’s Actual Showing*

PO’s entire argument relies on its illogical assertion that Costa’s “second stacked layer (232, 242 in green below) is not “**on**” the “third channel structure” (173 in yellow below) because the second stack layer allegedly does not laterally

overlap with the third channel structure. POPR, 4-6. What this means, of course, is that if Costa's "third channel structure" were a little wider, PO's entire argument would fall apart.



POPR, 5 (citing Costa, Fig. 21A).

Fall apart it does, because the Petition shows that the third channel structure (element 173) is wider in some embodiments and that it would have been obvious to widen Costa's third channel structure. Claim 11 recites as element [11.H]: "a second stacked layer disposed on ***the third channel structure.***" Element [11.H] refers back to element [11.G]: "***a third channel structure*** in contact with the second channel

structure disposed over the first through hole, ***wherein a projection of the third channel structure on the substrate covers a projection of the first through hole.***

The Petition's showing for [11.G] refers back to [1.F], arguing that Costa discloses or renders obvious "a third channel structure." Pet., 91. Notably, the Petition's analysis in [1.F] details that the "third channel structure" would have been understood, or at least it would have been obvious, to be wider than the hole ("covers a projection of the first through hole," i.e., 57, in the above figure) on which it sits. Pet., 47-54.

By way of example, the Petition's analysis in [1.F] explains that Costa discloses that the oxidation step that creates element 174, see Figure 21A above, is optional. Pet., 50 (citing Costa, [0266]). As a result, Costa's "third channel structure" 173 may include regions 174. The Petition illustrates this Costa embodiment:

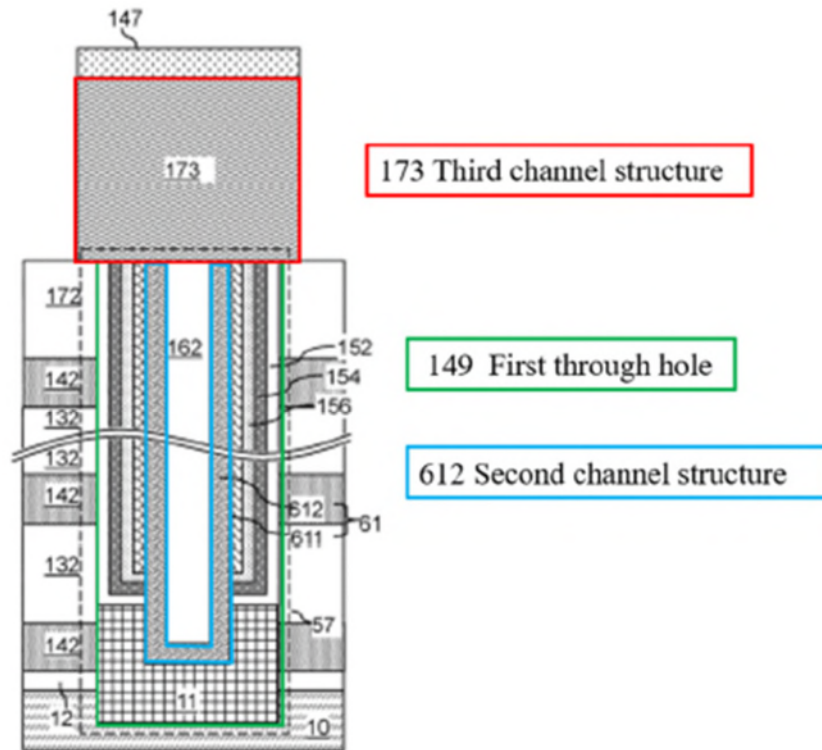
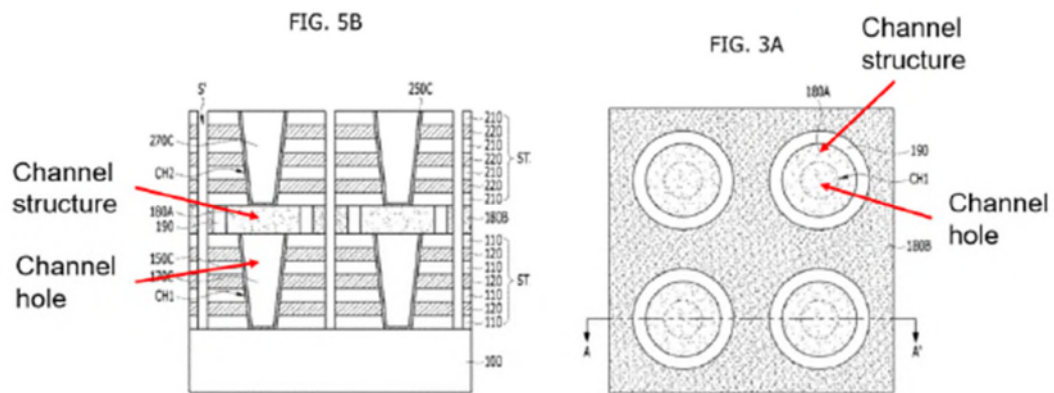


FIG. 20B

Pet., 48-49 (citing Costa, Fig. 20B). As can be seen in POPR Figure 21A above, the “second stack layer” would then laterally overlap with the “third channel structure.”

By way of another example, the Petition’s analysis in [1.F] explains why, at a minimum, a POSITA would have found obvious extending the third channel structure wider than the underlying hole (in which the channel structure reside), namely, (1) in the embodiments with the oxidation step, to protect the underlying channel structure from oxidation, and (2) in all embodiments, to improve processing margins and thereby ensure electrical coupling between the third channel structure and channel structure. Pet., 51-53. What’s more, with citations to prior art, the Petition demonstrates that using a wider structure to protect underlying structures

and enhance processing margins was conventional and routine. Pet., 52-53 (citing, e.g., Ex. 1024, [0061], “[T]o secure an overlap margin between the channel connection pattern 180A and the first channel hole CH1, the channel connection pattern 180A may have a larger width than the top surface of the first channel hole CH1.”). The result is a wider third channel structure in which the second stacked layer laterally overlaps the third channel structure, as the Petition demonstrates from an exemplary reference:



Pet., 53 (citing Ex. 1024, Figs., 5B, 3A).

The POPR conveniently ignores all of this for a simple reason: with Costa disclosing or rendering obvious that the “third channel structure” shown in Fig. 21A can be wider, there can be no dispute that Costa discloses, or at least renders obvious, that the “second stacked layer” is **“on”** the “third channel structure” even under PO’s incorrect implicit construction that “on” means “laterally overlapping.”

2. PO's Bases Its Argument on a Legally Erroneous Claim Construction

The Director also should reject PO's argument because it is based on inconsistent—and legally erroneous—claim constructions for the term “on.”

On the one hand, PO's argument implicitly construes “on” to mean “laterally overlapping”: “As clearly shown in Figure 21A, Costa's ‘second stacked layer’ does not **laterally overlap** with semiconductor portion 173. **Consequently**, Costa's ‘second stacked layer’ **is not ‘disposed on’** the semiconductor portion 173, which Petitioner identifies as the ‘third channel structure.’” POPR, 6. In other words, PO is construing “on” to require a special restriction in the Z direction (“overlap”). On the other hand, in the POPR's claim construction section, PO offers a different construction of “on”: “[b]ased on this lexicography, ‘on’ should be construed as ‘directly on or on with an intermediate feature or layer therebetween.’” POPR, 18. These constructions are inconsistent: the second construction does not require lateral overlap in the Z direction, but the first one does. To illustrate, under the second construction, a house would have siding “on” it (the siding touches the house), but under the first construction, the siding would not be “on” the house (because the siding does not vertically overlap any other portion of the house).

Under the '291 patent's mandate that “on” be construed in its broadest sense, the second stacked layer is plainly “on” the third channel structure. To start, the plain meaning of “on” includes both objects that are merely touching (in any

dimension) **and** objects that are in proximity to each other but not touching.⁶ The specification does not narrow this plain and ordinary meaning—if anything, it broadens it. The specification states:

It should be readily understood that ***the meaning of “on,” “above.” and “over” in the present disclosure should be interpreted in the broadest manner*** such that “on” not only means “directly on” something but also includes the meaning of “on” something with an intermediate feature or a layer therebetween, and that “above” or “over” not only means the meaning of “above” or “over” something but can also include the meaning it is “above” or “over” something with no intermediate feature or layer therebetween (i.e., directly on something).

Ex. 1001, 8:3-12 (emphasis added). As noted above, plain meaning of “on” includes objects that at are merely touching and that are in proximity to each other but not touching. The specification instructs that “on” “should be interpreted in the broadest manner.” *Id.* The specification then recites that a structure can be “on” another structure (i.e. “something”) even if there is a structure that intervenes. *Id.* Nothing about that narrows the meaning of “on” to exclude an object that is proximate to another, and nothing about that requires that one object laterally overlap another. Tellingly, when the claims require overlap, they use different words than “on”:

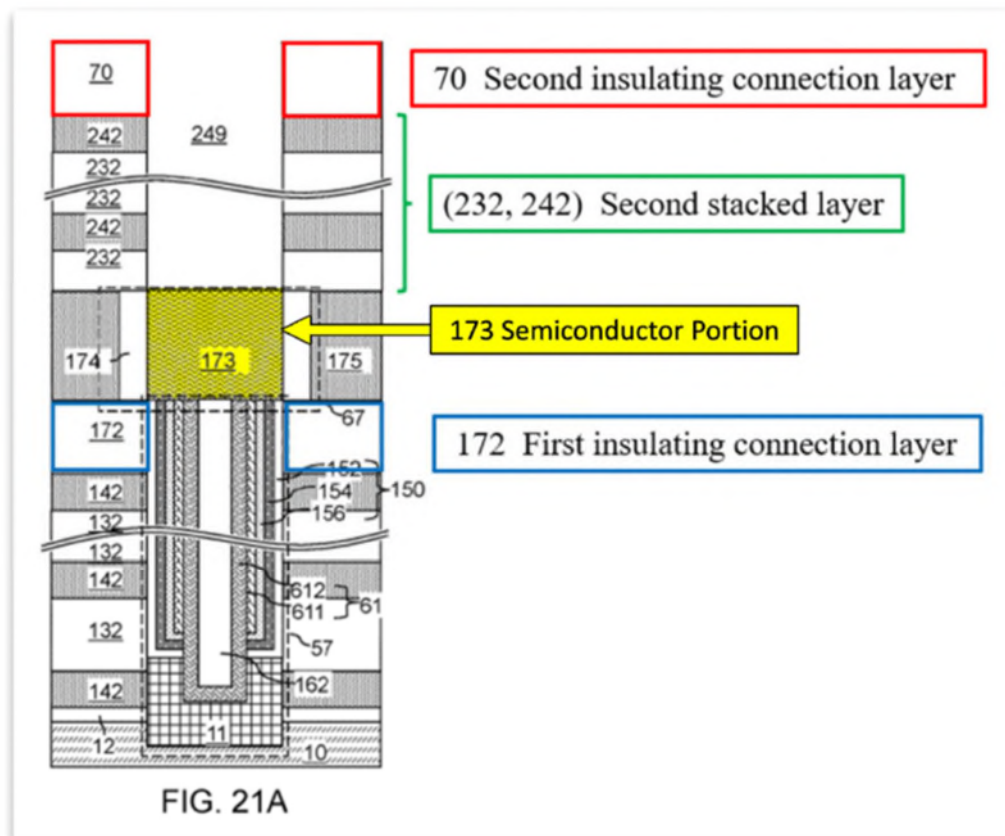
⁶ Ex. 1078, 1 (<https://www.merriam-webster.com/dictionary/on>) (“c used as a function word to indicate position in close proximity with”).

“wherein a projection of the third channel structure on the substrate ***covers*** a projection of the first through hole on the substrate.” Ex. 1001, Claim 1.

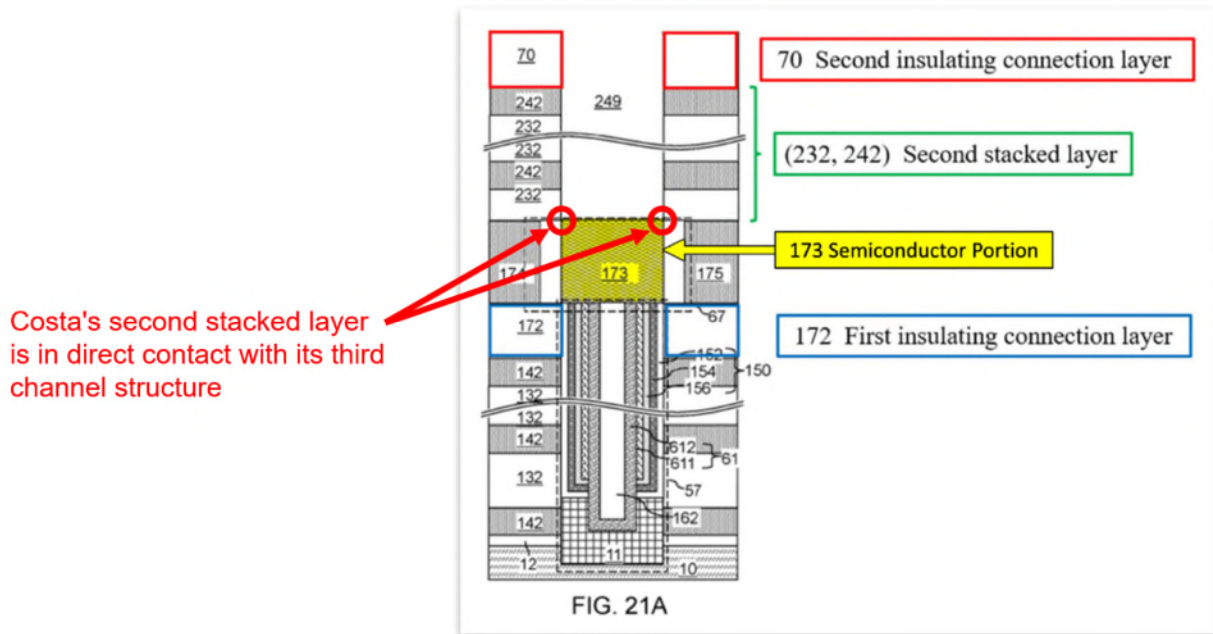
Because all of PO’s arguments rely on an erroneous interpretation of “on” that requires “lateral overlap,” the Director should reject them. POPR, 16-31.

3. *Under PO’s Express Claim Construction of “On,” PO’s Arguments Fail Even Ignoring the Petition’s “Third Channel Structure” Showing*

Under the construction of “on” in the POPR’s claim construction section (“directly on or on with an intermediate feature or layer therebetween”), Costa’s Fig. 21A plainly discloses the limitation, even ignoring Costa’s teaching that the “third channel structure” can be wider than shown in the Figure. POPR, 18. PO depicts these elements as follows:



POPR, 5-6 (citing Costa, Fig. 21A). As this figure illustrates, Costa's second stacked layer (232, 242) and third channel structure (element 173) are "directly on" each other, because their edges are directly touching each other:

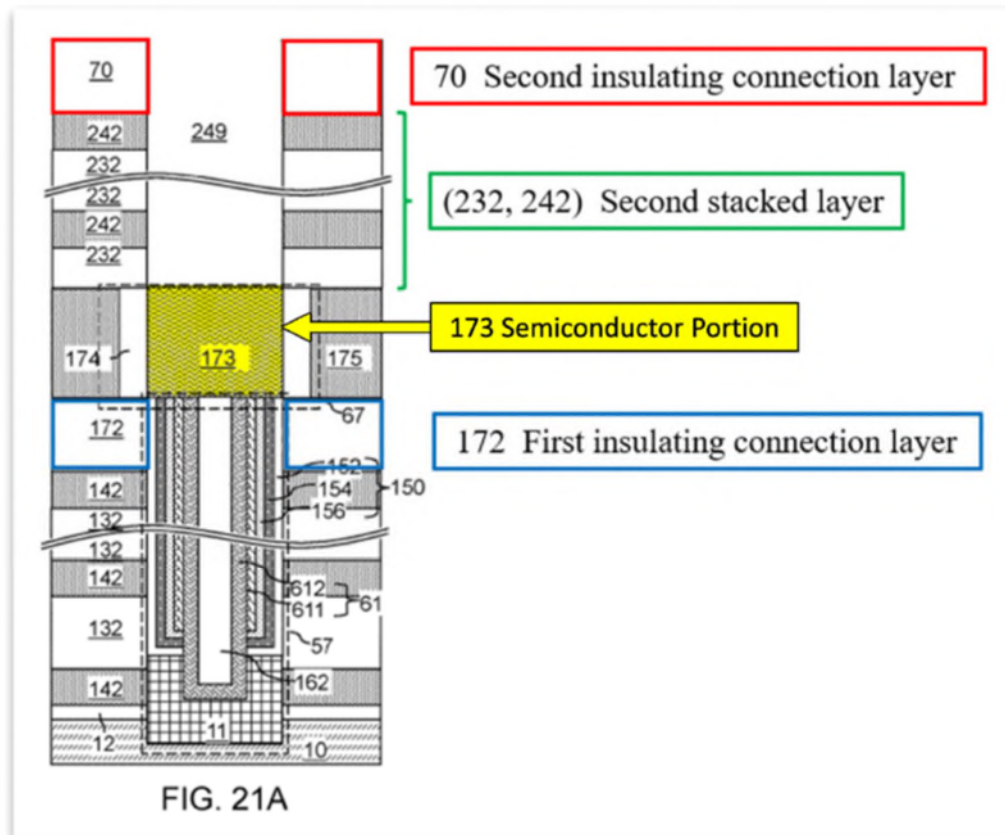


Costa, Fig. 21A (annotated); *see also* POPR, 24-26. This is yet another independent reason to reject all of PO's arguments.

4. *PO's Arguments to the Board Are Misleading*

Throughout the POPR, which ignores the Petitioner's showing (*see supra* §II.F.1) and relies on a legally erroneous implicit construction of "on" (*see supra* §II.F.2-3), PO makes misleading strawman arguments. All should be rejected.

First, PO faults Petitioner for referencing [1.G] in its analysis of [11.H] because [1.G] does not expressly recite the "on" limitation. POPR, 21. This argument fails because the [1.G] analysis describes the formation of the "second stack structure," and demonstrates that it is formed "on" the "third channel structure." Pet., 45-57. Indeed, PO reproduces the relevant mapping itself from the annotated Fig. 21A shown in the [1.G] analysis:



POPR, 5-6 (citing Costa, Fig. 21A).

Second, PO argues that because claim 11 is an apparatus claim, and claim 1 is a method claim, the Petition cannot refer back to claim 1 for disclosure of claim 11. POPR, 22. The Petition itself addresses this and explains the obvious: “claim 1 recites a method for forming the same,” i.e., a method for forming the “same” apparatus of claim 11. Pet., 90. And as PO correctly points out, the Petition’s analysis of claim 1 expressly details what the apparatus—after fabrication—

includes, thereby clearly setting forth the basis for claim 11's reliance on claim 1's analysis. POPR, 22.

Third, PO argues that the Petition does not even allege that the "on" limitation is met because that word "on" does not appear in the [11.H] analysis. POPR, 23-24. This makes no sense, because under the heading that recites the claim language which includes the word "on," the Petition states: "Costa discloses it," that is, Costa discloses the "on" limitation. Pet., 92. The POPR's focus on the relevant structures for the Petition's claim mapping itself demonstrates that the Petition's claim mapping is clear.

Fourth, PO argues that Petitioner did not advance an obviousness theory for limitation [11.H] and any attempt to do so would be hindsight, effectively arguing that the Petition did not advance an obviousness theory that the "third channel structure" would be wider than shown in POPR Figure 21A. POPR, 31-37. This is incorrect. The Petition expressly argues that it would have been obvious for the "third channel structure" to be wider than the underlying hole. Pet., 51 ("Regardless, a POSITA would have found it obvious to ensure that Costa's joint-level doped semiconductor portion 173 is wider than the first hole (more than covers a projection of first-tier memory opening 149 on the substrate)."); *see also* Pet., 45-52, 91. This analysis is part of [11.G] because the [11.G] limitation introduces "a third channel structure." Thus, limitation [11.H], which refers to "the third channel structure,"

incorporates the Petition’s showing with respect to [11.G], including that it would have been obvious for it to be wider than the underlying hole. *See* §II.F.1. Tellingly, PO expressly addresses this part of the Petition’s analysis, which makes clear that PO had no confusion over its relevance to limitation [11.H]. POPR, 35-37. Indeed, PO concedes here that “margin” was a motivating factor to make a third channel structure wider—as the Petition demonstrates—and only asserts that Costa had enough margin. POPR, 33-34. PO’s assertion fails because it contradicts the art of record, which states: “[T]o secure an overlap margin between the channel connection pattern 180A and the first channel hole CH1, the channel connection pattern 180A may have ***a larger width than the top surface of the first channel hole CH1***”—that is, the third channel structure should laterally overlap with the second stack structure. Pet., 53 (citing Ex. 1024, [0061]).

III. CONCLUSION

Institution is appropriate for the reasons outlined above and in the Petition.

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PETITIONER’S OPPOSITION TO PATENT OWNER’S BRIEF ON DISCRETIONARY DENIAL complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system’s word count, the paper—excluding the caption, table of contents, table of exhibits, certificate of word count, and certificate of service—contains 8,171 words.

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