

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00245
U.S. Patent No. 11,482,532
Issue Date: October 25, 2022

Title: JOINT OPENING STRUCTURES OF THREE-DIMENSIONAL
MEMORY DEVICES AND METHODS FOR FORMING THE SAME

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 11,482,532
PURSUANT TO 35 U.S.C. §§311-319 AND 37 C.F.R. §42**

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LISTING OF EXHIBITS

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1001	U.S. Patent No. 11,482,532 to Lu et al. (“the ’532 Patent”)
1002	File History of U.S. Patent No. 11,482,532 (“the ’532 FH”)
1003	Declaration of Dr. Sanjay Banerjee (“Banerjee”)
1004	<i>Curriculum Vitae</i> of Dr. Sanjay Banerjee
1005	U.S. Patent Publication No. 2018/0182771 A1 to Costa et al. (“Costa”)
1006	U.S. Patent Publication No. 2017/0154892 A1 to Oh (“Oh”)
1007	U.S. Patent Publication No. 2015/0155296 A1 to Yoon
1008	Aritome, “NAND Flash Memory Technologies” (2016)
1009	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
1010	Micheloni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)
1011	U.S. Patent No. 10,475,737 to Tang et al.
1012	Micheloni, “3D Flash Memories” (2016)
1013	U.S. Patent No. 9,853,046 to Lu et al.
1014	U.S. Patent No. 9,530,866 to Zhang et al.
1015	Plummer et al., “Silicon VLSI Technology: Fundamentals, Practice and Modeling” (2000)
1016	Certified Translation of KR 101487746 B1 to Lee et al. (including original Korean patent document)
1017	U.S. Patent Publication No. 2016/0204117 A1 to Liu et al.

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EXHIBIT NO.	DESCRIPTION
1018	U.S. Patent Publication No. 2016/0284728 A1 to Lu et al.
1019	U.S. Patent No. 9,401,371 to Lee et al.
1020	U.S. Patent No. 9,570,460 to Kanakamedala et al.
1021	U.S. Patent No. 9,496,381 to Lee et al.
1022	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1023	Minute Order (case schedule), Dkt. No. 141, dated September 18, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1024	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, LTD.'s Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1025	Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:24-cv-04223-RFL which has been consolidated with Case No. 3:23-cv-05792-RFL

LISTING OF CHALLENGED CLAIMS

Ref. #	Listing of Challenged Claims
Claim 1:	
[1.PRE]	A method of forming a joint opening structure in a three-dimensional (3D) memory device, comprising:
[1.A]	forming a first stacked layer on a substrate;
[1.B]	forming a first through hole penetrating the first stacked layer to expose the substrate;
[1.C]	forming a first channel structure at a bottom of the first through hole and in contact with the substrate;
[1.D]	forming a second channel structure in the first through hole and in contact with the first channel structure;
[1.E]	forming a third channel structure above the first through hole and in contact with the second channel structure, wherein a size of the third channel structure along a lateral direction is larger than a top aperture of the first through hole;
[1.F]	forming a second stacked layer over the third channel structure;
[1.G]	forming a second through hole penetrating the second stacked layer to expose the third channel structure;
[1.H]	forming a fourth channel structure in the second through hole and in contact with the third channel structure; and
[1.I]	forming a fifth channel structure above the second through hole and in contact with the fourth channel structure.

Ref. #	Listing of Challenged Claims
Claim 2:	
[2.PRE]	The method of claim 1, wherein:
[2.A]	the first stacked layer includes a first number of oxide/nitride layer pairs; and
[2.B]	the second stacked layer includes a second number of oxide/nitride layer pairs.
Claim 3:	
[3.PRE]	The method of claim 2, wherein:
[3.A]	the first number and the second number are not less than 32.
Claim 11:	
[11.PRE]	A joint opening structure of a three-dimensional (3D) memory device, comprising:
[11.A]	a first through hole penetrating a first stacked layer along a vertical direction;
[11.B]	a first channel structure disposed at the bottom of the first through hole;
[11.C]	a second channel structure in contact with the first channel structure disposed in the first through hole;
[11.D]	a third channel structure in contact with the second channel structure disposed over the first through hole, wherein a size of the third channel structure along a lateral direction is larger than a top aperture of the first through hole;
[11.E]	a second stacked layer disposed on the third channel structure;
[11.F]	a second through hole penetrating the second stacked layer along the vertical direction;

Ref. #	Listing of Challenged Claims
[11.G]	a fourth channel structure in contact with the third channel structure disposed in the second through hole;
[11.H]	a fifth channel structure in contact with the fourth channel structure disposed over the second through hole.
Claim 13:	
[13.PRE]	The joint opening structure of claim 11, further comprising:
[13.A]	a first filling structure covering the surface of the second channel structure; and
[13.B]	a second filling structure covering the surface of the fourth channel structure;
[13.C]	wherein the first through hole is non-interconnected with the second through hole.
Claim 15:	
[15.PRE]	The joint opening structure of claim 11, wherein:
[15.A]	the first stacked layer includes a first number of conductor/dielectric layer pairs;
[15.B]	the second stacked layer includes a second number of conductor/dielectric layer pairs; and
[15.C]	the first number and the second number are not less than 32.
Claim 16:	
[16.PRE]	The joint opening structure of claim 11, wherein:
[16.A]	a thickness of the third channel structure is in a range between 30 nm and 70 nm.
Claim 17:	
[17.PRE]	The joint opening structure of claim 11, wherein:

Ref. #	Listing of Challenged Claims
[17.A]	a size difference between the top aperture and a bottom aperture of the first through hole is equal to or less than 30 nm; and
[17.B]	a size difference between a top aperture and a bottom aperture of the second through hole is equal to or less than 30 nm.
Claim 18:	
[18.PRE]	A joint opening structure of a three-dimensional (3D) memory device, comprising:
[18.A]	a first stacked layer disposed on a substrate;
[18.B]	a second stacked layer disposed on the first stacked layer; and
[18.C]	a plurality of channel structures penetrating the first stacked layer and the second stacked layer;
[18.D]	wherein each of the plurality of channel structures includes:
[18.E]	a first through hole penetrating the first stacked layer,
[18.F]	a first channel structure disposed at the bottom of the first through hole and in contact with the substrate,
[18.G]	a second channel structure disposed in the first through hole and in contact with the first channel structure,
[18.H]	a third channel structure disposed over the first through hole and in contact with the second channel structure, wherein a size of the third channel structure along a lateral direction is larger than a top aperture of the first through hole;
[18.I]	a second through hole penetrating the second stacked layer,
[18.J]	a fourth channel structure disposed in the second through hole and in contact with the third channel structure, and
[18.K]	a fifth channel structure disposed over the second through hole and in contact with the fourth channel structure.

Ref. #	Listing of Challenged Claims
Claim 20:	
[20.PRE]	The joint opening structure of claim 18, wherein:
[20.A]	a thickness of the third channel structure is in a range between 30 nm and 70 nm.

I. INTRODUCTION

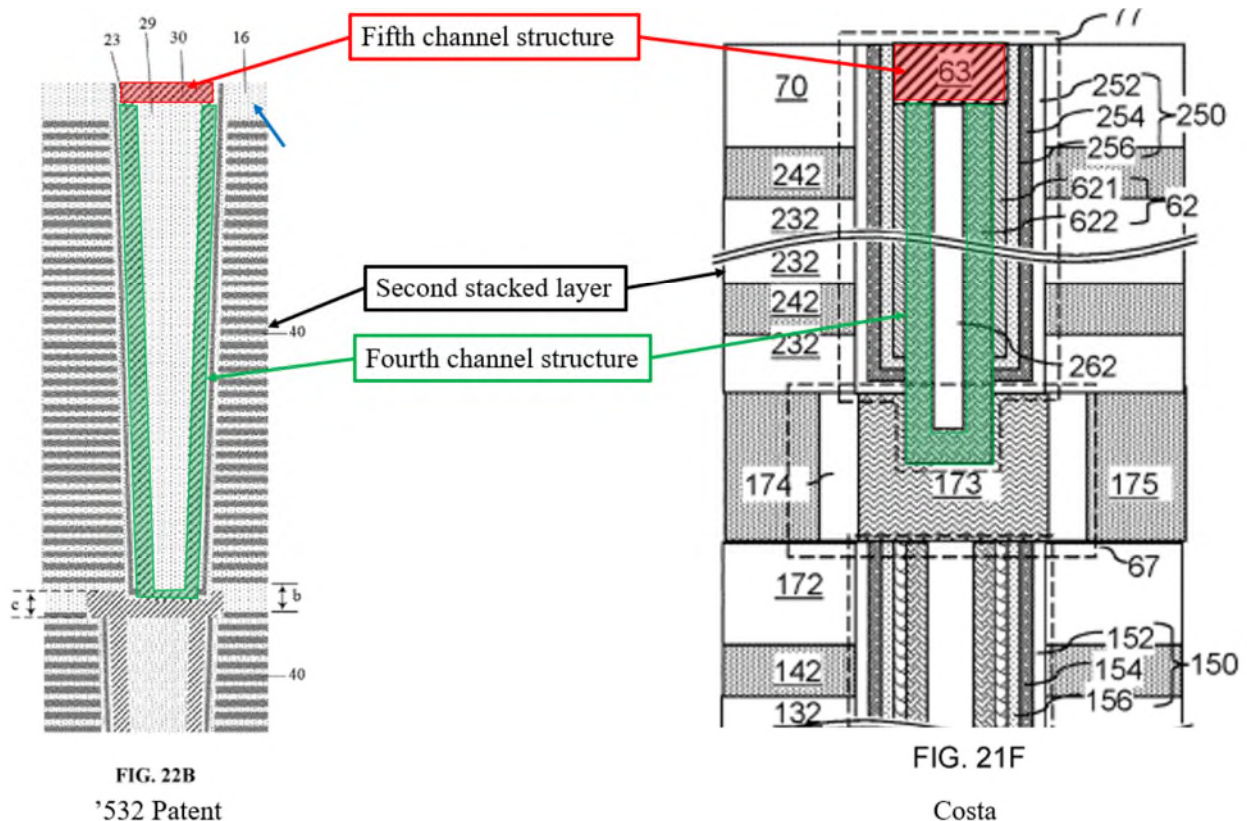
Petitioner Micron Technology, Inc. (“Petitioner”) respectfully requests inter partes review of claims 1-3, 11, 13, 15-18, and 20 (the “Challenged Claims”) of U.S. Patent No. 11,482,532 (the “’532 Patent”) assigned to Yangtze Memory Technologies Co., Ltd. (“Patent Owner” or “PO”).

The ’532 Patent relates to joint opening structures in 3D memory devices in which a first memory structure is formed in a first deck followed by a second memory structure in a second deck. The two structures electrically connect to form a continuous vertical memory channel. *E.g.*, Ex. 1001, Figs. 11B, 22B. The ’532 Patent admits that such structures were known in the prior art. *Id.*, 1:26-37. Forming a continuous vertical channel requires ensuring that the first and second memory structures are vertically aligned such that the channel structures therein (e.g., separate semiconductive layers) electrically couple. The Challenged Claims cover a specific method and configuration of doing so.

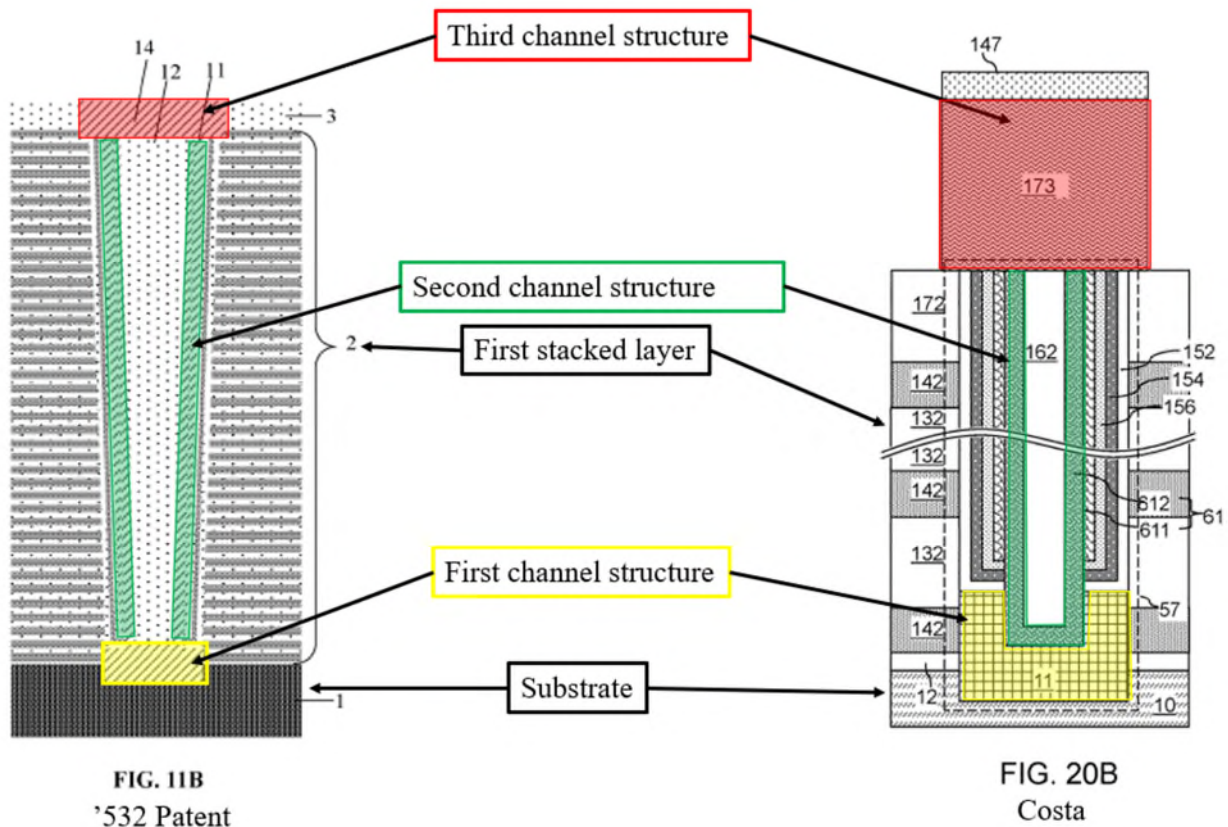
The ’532 Patent describes a structure that includes an inter-tier channel structure (the claimed “third channel structure”) that is “sandwiched” between the upper and lower decks. Ex. 1001, 2:44-56, Fig. 16 (element 14). The third channel structure can have a dimension (or area) that is larger than that of the underlying first through hole. *Id.*, 12:34-36, 12:55-60, Fig. 10A. Further, the claimed “fifth channel structure” is disposed over a second tier through hole. *Id.*, 3:10-18, Fig. 21A

(element 30). These elements, along with the two channel structures in the respective memory decks, create a continuous vertical memory channel. That the claims require the third channel structure (“wherein a size of the third channel structure along a lateral direction is larger than a top aperture of the first through hole”) was the reason for allowance. Ex. 1002, 642.

None of this, however, was new or nonobvious. The Costa prior art reference was not before the Examiner during prosecution of the ’532 Patent. Costa discloses, or at least renders obvious, each and every element of claim 1. The figure below maps each claim element in the top deck portion of Costa with the corresponding elements shown in the ’532 Patent for comparison.



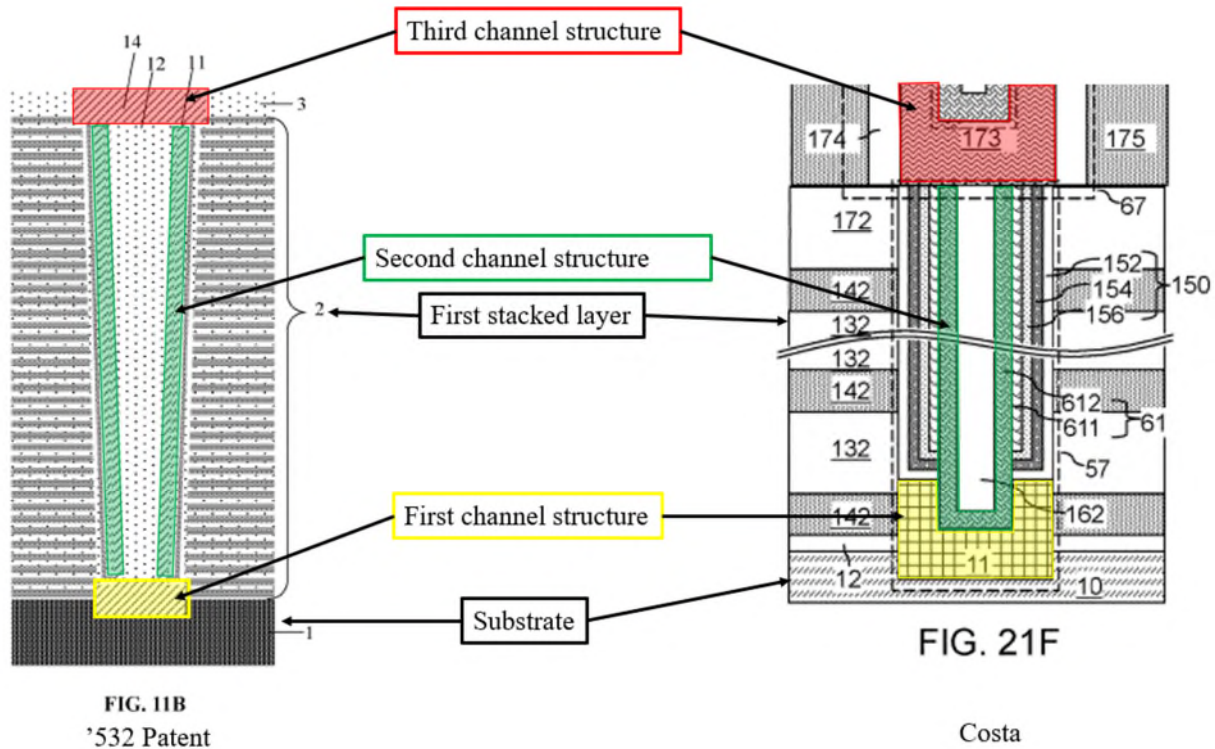
Ex. 1001, Fig. 22B (annotated, left); Ex. 1005 (“Costa”), Fig. 21F (excerpted, annotated, right). The figure below maps each claim element in the bottom deck portion of Costa with the corresponding elements shown in the ’532 Patent for comparison. As can be seen, in some of Costa’s figures, e.g., Figure 20B, Costa depicts the third channel structure being wider than the underlying channel hole:



Ex. 1001, Fig. 11B (annotated, left); Costa, Fig. 20B (annotated, right).

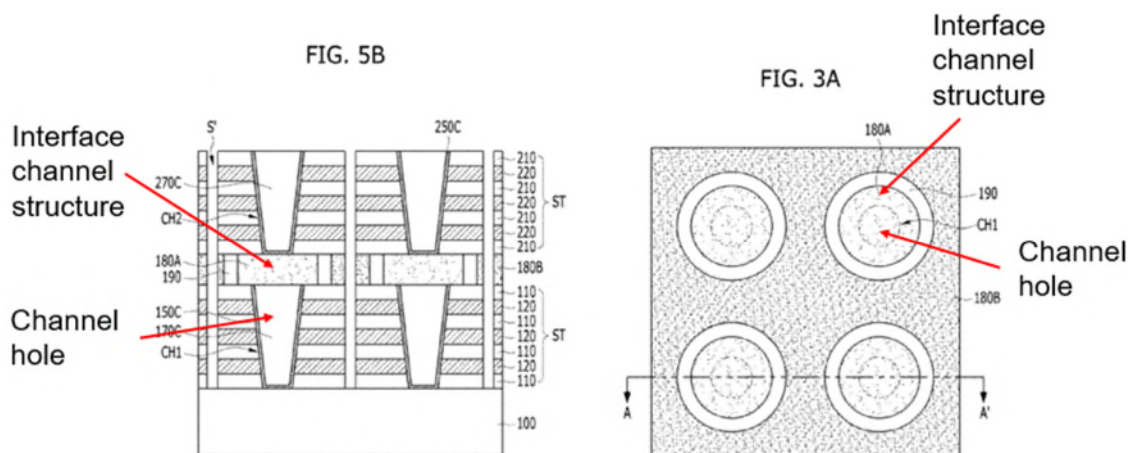
In other figures, Costa illustrates the third channel structure being the same width as the underlying channel hole, after performing an optional oxidation step to create 174’ spacers. These figures, however, do not take into account the well-

known margin (added width added to account for, e.g., misalignment and process variations) that would have been obvious to apply even in these embodiments.



Ex. 1001, Fig. 11B (annotated, left); Costa, Fig. 21F (excerpted, annotated, right).

Critically, the Examiner was not made aware of a vast amount of prior art demonstrating that—in this very context—it was known to increase the width of the third channel structure, *i.e.*, provide an alignment margin, to mitigate alignment issues. To preview just one example, Oh discloses an interface channel structure between two memory decks that is wider than the underlying channel hole:



Ex. 1006 (“Oh”), Figs. 5B, 3A (annotated). Oh also explains why the third channel structure should be wider than the underlying hole: “[T]o secure an overlap margin between the channel connection pattern 180A and the first channel hole CH1, the channel connection pattern 180A may have a larger width than the top surface of the first channel hole CH1.” *Id.*, [0061]. This Petition demonstrates that (1) Costa’s express teachings would have been understood to apply this margin, and separately, (2) it would have at least been obvious to include this “overlap margin,” because, for example, the top and bottom channels can then “be easily connected.” Ex. 1007, [0037]-[0038].

The dependent claims recite well known structures (and methods for forming such structures) that Costa discloses or were well within the knowledge of a POSITA. Petitioner requests that the Board institute trial and find the Challenged Claims unpatentable under §103.

II. MANDATORY NOTICES

A. Real Party-in-Interest

Petitioner Micron Technology, Inc., and its subsidiaries, including Micron Consumer Products Group LLC, are the real parties-in-interest.

B. Related Matters

On July 12, 2024, YMTC asserted the '532 Patent and U.S. Patent Nos. 10,672,711, 10,879,164, 10,879,254, 10,886,291, 11,101,276, 11,145,666, 11,450,604, 11,568,941, 11,581,322, and 12,010,838 against Micron. On August 21, 2024, the litigation was consolidated with *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023) (“Co-Pending Litigation”). U.S. Patent Nos. 10,658,378, 10,861,872, 10,868,031, 10,937,806, 10,950,623, 11,468,957, 11,501,822, and 11,600,342 were asserted by Patent Owner in the first filed case, leading to a total of 19 patents-at-issue in the now consolidated Co-Pending Litigation.

In addition to this Petition, Petitioner is filing (or has filed) petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation:

Patent	PTAB Proceeding	Wave
10,658,378 (claims 15-17 and 19-20)	IPR2024-00788	Wave 1 Petitions
10,861,872 (claims 1-6 and 11-13)	IPR2024-00789	

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Patent	PTAB Proceeding	Wave
10,868,031	IPR2024-00790	
10,937,806 (claims 8-9 and 11-12)	IPR2024-00791	
10,950,623	IPR2024-00794	
11,468,957	IPR2024-00792	
11,501,822	IPR2024-00795	
11,600,342 (claims 1-6 and 8-20)	IPR2024-00793	
10,658,378 (claims 1-7 & 18)	IPR2024-00909	Wave 2 Petitions
10,861,872 (claims 7-10)	IPR2024-00910	
10,937,806 (claim 10)	IPR2024-00911	
11,600,342 (claim 7)	IPR2024-00912	
10,672,711	IPR2025-00117	Wave 3 Petitions
10,879,164	IPR2025-00118	
10,879,254	IPR2025-00034	
10,879,254	IPR2025-00119	
10,886,291 (claims 1-5, 8-9, 11-12, & 14-19)	IPR2025-00244	
10,886,291 (claims 6-7, 10, & 20)	IPR2025-00294	
11,101,276	IPR2025-00228	
11,145,666	IPR2025-00189	
11,450,604	IPR2025-00035	
11,568,941	IPR2025-00190	
11,581,322	IPR2025-00191	

Patent	PTAB Proceeding	Wave
12,010,838	IPR2025-00229	

The Director and the Board should allow this Petition under 35 U.S.C. §314(a), 35 U.S.C. §325(d), and/or 37 C.F.R. §42.108(a).

C. Counsel, Service, and Fee Information

Petitioner designates the following counsel:

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Petitioner consents to service by electronic mail at the following addresses:
PTABDocketJJL2@orrick.com, PTABDocketT6J1@orrick.com,

PTABDocketJ3B3@orrick.com, and micron-ymtc_ohs@orrick.com. Pursuant to 37 C.F.R. §42.10(b), Petitioner's Power of Attorney is attached.

The USPTO is authorized to charge the filing fee and any other fees incurred by Petitioner to the deposit account of Orrick, Herrington, & Sutcliffe LLP:15-0665.

III. REQUIREMENTS FOR *INTER PARTES* REVIEW

A. Grounds for Standing

Petitioner certifies that the '532 Patent is available for IPR, and that Petitioner is not barred or estopped from requesting this IPR. Petitioner was served with a complaint alleging infringement of the '532 Patent on July 12, 2024.

B. Identification of Challenged Claims and Statement of Precise Relief Requested

Petitioner requests IPR of claims 1-3, 11, 13, 15-18, and 20. This Petition is supported by the accompanying Declaration of Dr. Sanjay K. Banerjee (Ex. 1003, "Banerjee"), a leading expert in the 3D NAND field.

For purposes of this Petition only, it is assumed that the '532 Patent is entitled to the benefit of the earliest-listed priority documents: March 8, 2017 date. Ex. 1001.

Petitioner relies on the following references under the ground presented in the following table:

Ground	Claim(s)	Prior Art Asserted
1	1-3, 11, 13, 15-18, and 20	Obvious under §103 based on U.S. App. Pub. No. 2018/0182771 (Ex. 1005, “Costa”) ¹
2	1-3, 11, 13, 15-18, and 20	Obvious under §103 based on Costa and U.S. App. Pub. No. 2017/0154892 (Ex. 1006, “Oh”) ²

IV. INSTITUTION SHOULD BE GRANTED

Petitioner has established a reasonable likelihood of success on the merits. All other requirements for IPR have been met. The Board should institute IPR.

A. There are No Grounds for a § 314 Discretionary Denial in this Case

Petitioner submits that it presents a “compelling” case, and thus the Board should not “discretionarily deny institution in view of [the] parallel district court litigation.” 6/21/22 Interim Procedure, 2, 4-5.

Petitioner also notes that the factors considered by the Board when assessing whether to institute IPR in light of a parallel proceeding collectively weigh in favor of institution. *See Apple Inc. v. Fintiv, Inc.*, Case No. IPR2020-00019, Paper No. 11 (Mar. 20, 2020) (precedential) (“*Fintiv*”). In particular: the district court may stay the case, any potential trial will occur years from now, little district court work has

¹ Costa was filed on February 28, 2017 and is prior art under at least AIA § 102(a)(2).

² Oh was filed June 10, 2016 and is prior art under at least AIA § 102(a)(2).

occurred, petitioner diligently prepared this petition, and the petition is substantively strong.

1. Possibility of a Stay

Petitioner intends to seek a stay. This factor is neutral.

2. Proximity of the Court's Trial Date

The average time to trial for civil cases in the Northern District of California is 48.9 months. *See* Ex. 1022. Assuming that average holds, and IPR is instituted, IPR should conclude before trial. On September 18, 2024, the district court entered a scheduling order which set a trial date of June 15, 2026. *See* Ex. 1023. Assuming no stay, delay, or continuance, the FWD will issue proximate with the trial date. This weighs in favor of institution.

3. Investment in the Parallel Proceeding

To date, the parties and Court have invested very little in the parallel proceeding. Indeed, beyond engaging in some motion practice regarding the pleadings and consolidation, little substantive progress has been made. Virtually no progress has been made in connection with the later asserted YMTC patents. This includes the '532 Patent and other "Wave 3" patents discussed above. *See supra* § II.B. The parties only recently completed the exchange of contentions for the Wave 3 patents but have not taken any depositions regarding any of the patents in the Co-Pending Litigation. Fact discovery is in its infancy. No claim-construction positions have been exchanged for the Wave 3 patents except an initial exchange of

terms, no claim-construction order has issued, no infringement or invalidity expert discovery has occurred, and no summary judgment motions have been filed. This weighs in favor of institution. *See Sand Revolution*, 10-11.

The Board also has explained that institution is appropriate where “the petitioner filed the petition expeditiously....” *Fintiv*, 11. Here, on July 12, 2024, PO asserted eleven Wave 3 patents against Petitioner and subsequently asserted 149 claims across those Wave 3 patents. Ex. 1024. Petitioner proceeded with diligence, starting the filing of eleven petitions approximately three months after being served with the July 12, 2024 complaint. Ex. 1025. This also weighs strongly in favor of institution.

4. Issue Overlap

Should the Board institute, Micron stipulates that it will not advance in District Court any of the grounds in this Petition. Micron submits that this eliminates any potential overlap in issues between the proceedings here and in District Court. The Board has found that such stipulations weigh in favor of institution. *Sand Revolution*, 11-12.

5. Party Overlap

Both Petitioner and Patent Owner are parties in the parallel proceeding. This, however, is of little moment as there is often party overlap when there is a parallel proceeding.

6. Other Circumstances

Here, Petitioner submits that its petition has significant substantive merit. It is premised on clear, understandable prior art that plainly teaches the claimed subject matter. Thus, this factor also weighs in favor of institution.

B. Denial Under §325(d) Would Be Inappropriate

The Examiner did not consider Costa or Oh³, and thus denial under §325(d) would be inappropriate. Moreover, the apparent point of novelty of the independent claims is the “third channel structure.” See §VI.B. Costa would have been understood to disclose, or at least render obvious, the “third channel structure.” See §X.A.6. Importantly, the Examiner apparently was unaware of the prior art (such as Oh) that teaches both (1) a third channel structure that is wider than the underlying through hole and (2) the exact reasons for (and corresponding benefits of) widening the third channel structure to be wider than the underlying through hole. See §VI.B. Similarly, the Examiner did not have the benefit of expert testimony explaining a POSITA’s understanding of the alignment issues. Both the prior art and the expert testimony demonstrate that widening the third channel structure to be wider than the underlying through hole was in line with basic semiconductor fabrication practices. Banerjee, ¶¶ 155-57. At the very least, the Examiner overlooked, or did not

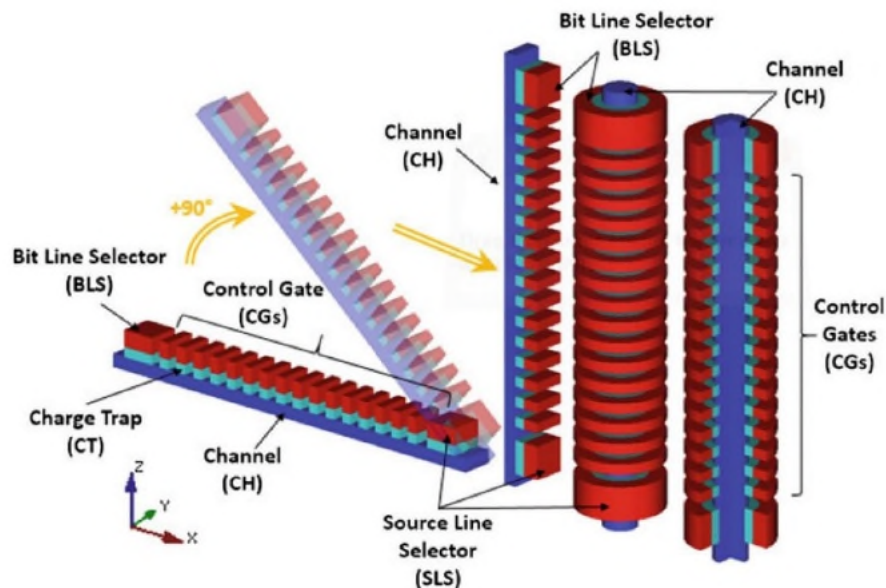
³ The ’532 Patent cites an unrelated Oh patent on its face.

appreciate, such teachings and knowledge of a POSITA.

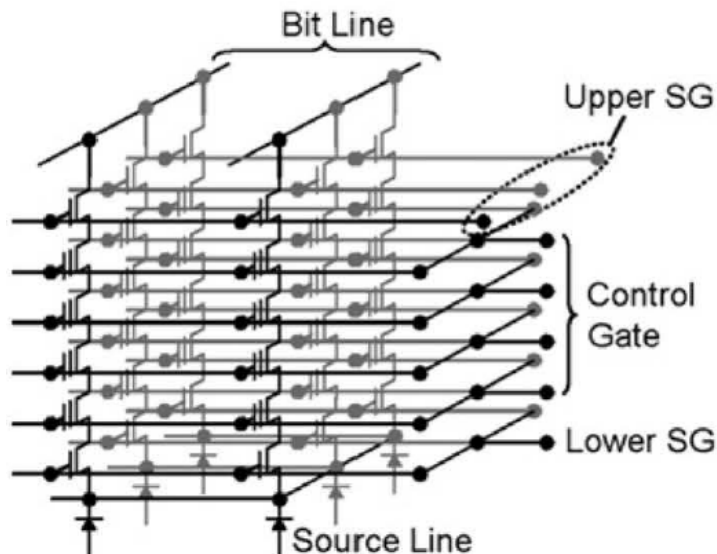
V. TECHNOLOGY BACKGROUND

The '532 Patent and the prior art discussed in this Petition relate to three-dimensional (3D) memory devices, e.g., 3D NAND memory devices. Banerjee, ¶¶ 41-42.

In NAND memory devices, NAND cells are arranged in “strings” with multiple cells “connected in series.” Ex. 1008, 38. Early NAND devices were formed as two-dimensional arrays. *Id.*, 58. “Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block” and “turning the 2D NAND string upside,” “resulting” in a “3D structure” with a “vertical channel.” Ex. 1009, 3; Banerjee ¶ 43.

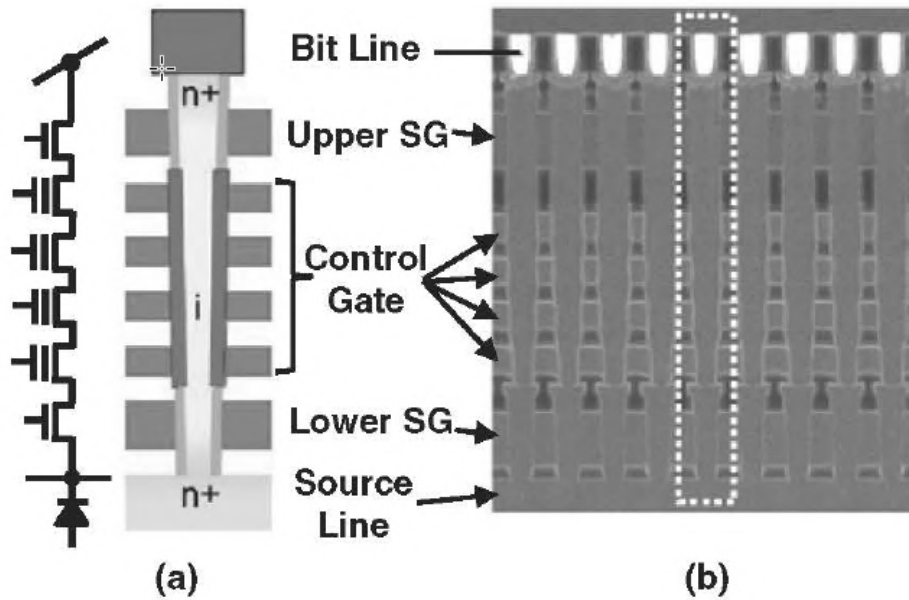


Ex. 1010, 122. Multiple such vertical channels are then repeated in a three-dimensional array:



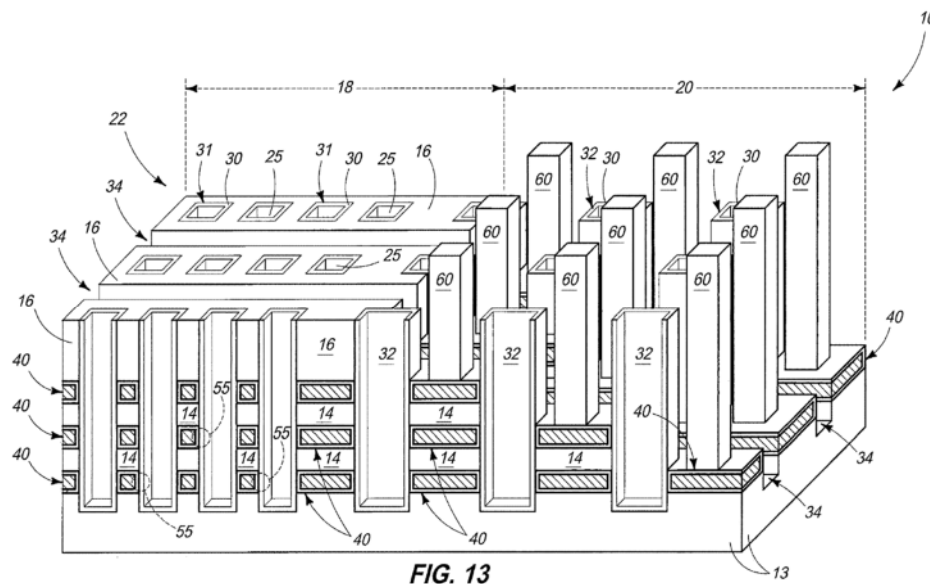
Ex. 1008, 296; Banerjee, ¶ 44.

3D NAND includes “multi-stacked layers of gate (plate)” material alternated with “dielectric” in a “[s]tack.” Ex. 1008, 294. These stacks are known as “memory stacks.” A “through-hole[]” channel (also known as a channel structure) “filled by memory film ... and channel poly-Si” passes through the layers of the memory stack to form the string of vertically arranged memory cells. *Id.*, 295. “Each” layer of “electrode plate acts as a control gate.” *Id.* A particular vertical memory cell “string is selected by a bit line and an upper select gate (upper SG).” *Id.*, 295-296. A memory cell “is located in the intersection of a control gate plate” and the memory film/poly-Si channel. *Id.* The lowest layer is a “select gate (lower SG)” allowing the strings to connect to a lower “common source.” *Id.*, 295, 297. An example 3D NAND vertical memory cell string is shown below:



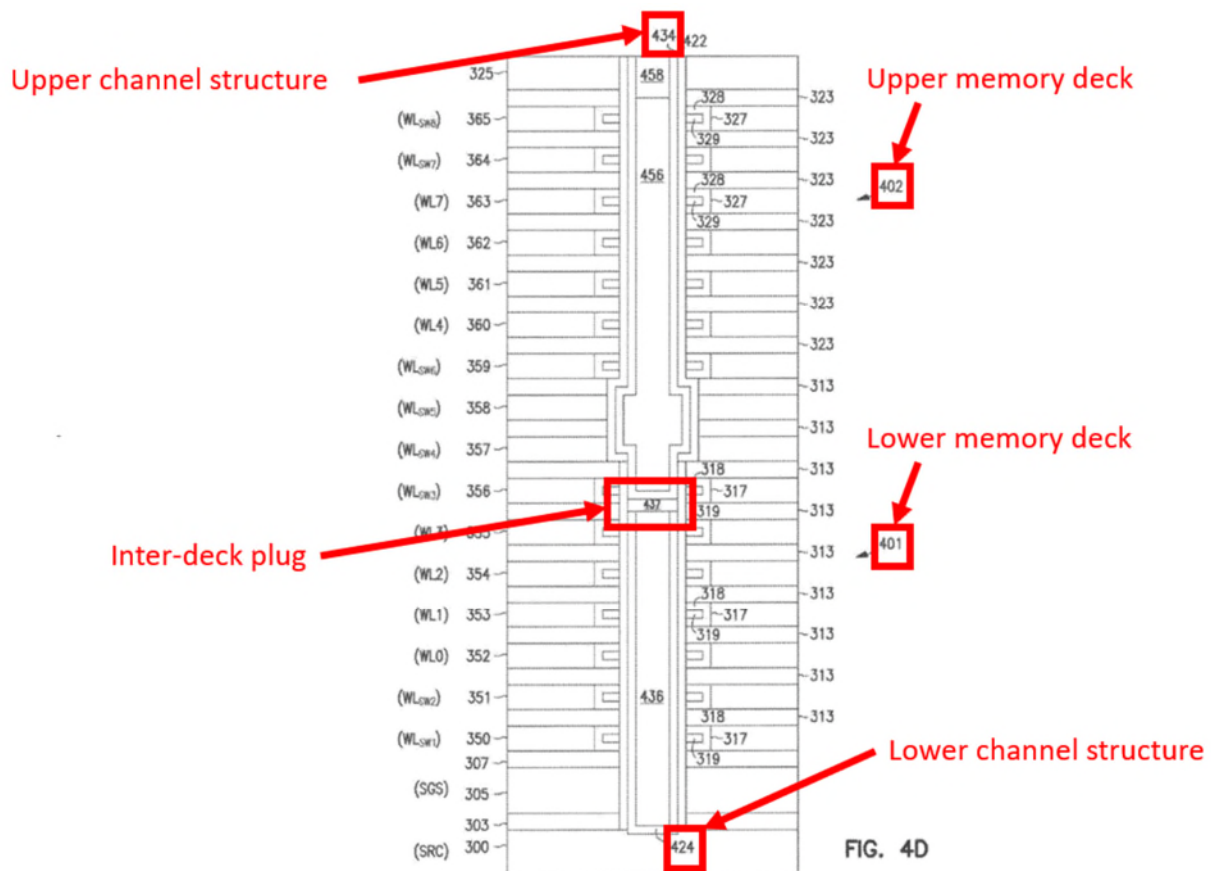
Id., 296; Banerjee, ¶¶ 45-46.

To access each memory cell via its control gate (also known as a word line), it was well known to use staircase structures, which provide landing areas on the control gates for contacts (below, the contacts 60 connect to different control gates):



Ex. 1011 (U.S. Pat. 10,475,737), Fig. 13, 4:56-64, 8:45-56; Banerjee, ¶¶ 47-50.

Multi-deck 3D memory devices became well known before 2017, i.e., a device that includes two memory stacks: one on top of the other. The driving motivation for multi-deck structures is the difficulty in etching high aspect ratio channel holes. Ex. 1012, 211-215. A multi-deck structure, however, enables the formation of high aspect ratio channel holes by forming the first deck, etching a hole through the first deck, forming the second deck, and then etching another hole through the top deck. The resulting structure includes two channel structures (each also known as a sub-channel structure) that connect via an interface:



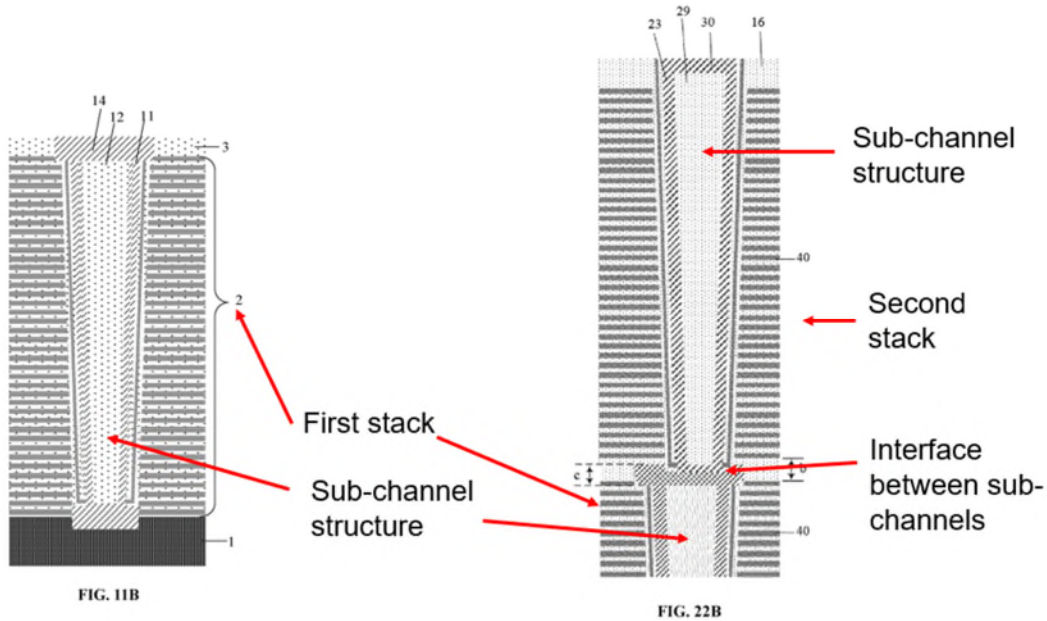
Ex. 1013 (U.S. Pat. 9,853,046), Fig. 4D (annotated); Banerjee, ¶¶ 51-52.

VI. THE '532 PATENT AND ITS PROSECUTION HISTORY

A. '532 Patent Summary

The '532 Patent primarily relates to multiple-stack three-dimensional (3D) memory devices, *e.g.* multiple-stack 3D NAND devices. Ex. 1001, 1:17-37. According to the '532 Patent specification, “3D NAND memory devices[] keep scaling more oxide/nitride (ON) layers” due to advances in semiconductor technology, creating difficulty in “us[ing] a single etching process to form the channel holes” as the depth (i.e., number of layers) increases. *Id.* “Thus, a single etching method may not be efficient in both cost and process capability.” *Id.*, 1:36-37.

To mitigate these purported problems, the '532 Patent proposes a multiple-stack structure employing certain joint opening structures and methods for forming the same. *See generally* Ex. 1001. In short, the '532 Patent relates to forming a first memory stack, forming a sub-channel structure therein, forming a second memory stack on the first stack, and forming a sub-channel structure therein that connects to the first sub-channel.



Id., Figs. 11B, 22B. The '532 Patent claims refer to the features that comprise the sub-channels and the interface therebetween as the first, second, third, fourth, and fifth channel structures, the first and second functional layers, and the first and second filling structures. *See generally id.* Petitioner describes each claimed feature below in mapping the claims to the prior art to aid in understanding the '532 Patent's disclosure and respective claim elements.

B. '532 Patent File History

On March 29, 2022, the Examiner rejected claims 11-12 and 14-20 as obvious over U.S. Pub. No. 2013/0109158 ("Lee '158") in view of U.S. Pub. No.

2013/0203227 (“Huo”). Ex. 1002, 591.⁴ The Examiner provisionally rejected claims 11-20 on non-statutory double patenting grounds, finding that they were patentably indistinct over the corresponding claims in then co-pending application number 16/046,847 (now U.S. Patent No. 10,886,291 (“the ’291 Patent”). *Id.*, 597-98.

On May 27, 2022, Applicant made numerous arguments against the Examiner’s rejections of independent claim 11.⁵ Specifically, Applicant argued that “claim 11 recites at least the below features that distinguish over the applied references:

⁴ An Office Action dated March 3, 2022 required Applicant to make an election between claims 1-10 (method claims) and claims 11-20 (apparatus claims). Ex. 1002, 578. Applicant elected claims 11-20, without traverse. *Id.*, 583. However, the Examiner later withdrew the requirement for election and allowed claims 1-10. *Id.*, 641.

⁵ On May 27, 2022, Applicant also filed a terminal disclaimer, which was approved on June 2, 2022. Ex. 1002, 614, 635.

a third channel structure in contact with the second channel structure disposed over the first through hole, wherein **a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate;**

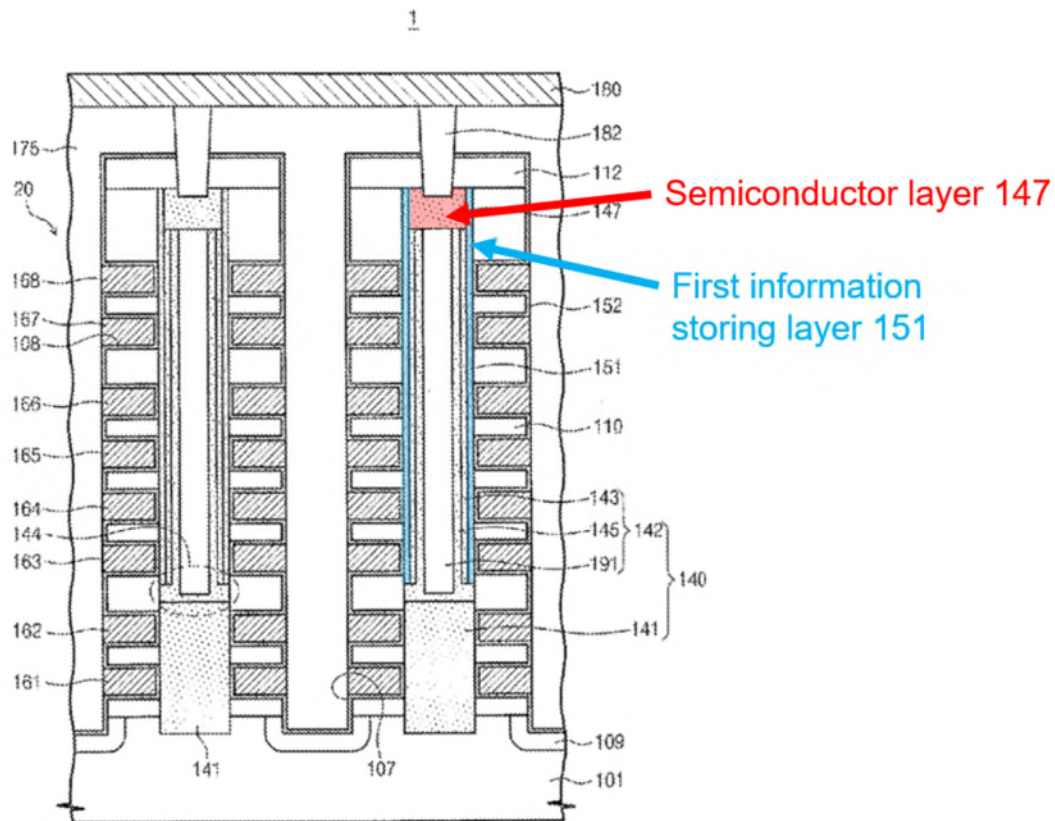
...

a fifth channel structure in contact with the fourth channel structure disposed over the second through hole,

Ex. 1002, 622 (emphasis in original). Applicant appears to have mistakenly quoted language from claim 11 of the '291 Patent with respect to the third channel structure limitation. On June 20, 2022, the Examiner allowed the claims, citing the same “third channel structure” limitation Applicant cited as the reason for allowance. *Id.*, 642. The Examiner, however, quoted the correct language and found that the prior art did not teach that “a size of the third channel structure along a lateral direction is larger than a top aperture of the first through hole.” *Id.*

In further regard to Lee '158 and the third channel structure, Applicant argued that “a diameter of [Lee '158's] semiconductor layer 147 in the lateral direction must be **less than** an inner diameter of the channel hole 103” because it is “**within** the channel hole 103 and **encircled by** first information storing layer 151[.]” Ex. 1002, 623 (emphasis in original). In other words, as shown below, the semiconductor layer 147 is not wider than the through hole of Lee '158:

Fig. 1P



Id., 624, Lee '158, Fig. 1P (annotated).

Regarding the fifth channel structure, Applicant argued that Huo does not disclose any fifth channel structure in contact with the fourth channel structure, and that because the lower and upper sub-channels are distinct and different structures, the Examiner's assumption that an element of the lower sub-channel would be on the upper sub-channel and satisfy the fifth channel structure element was incorrect. Ex. 1002, 624-25.

VII. CLAIM CONSTRUCTION

For purposes of this Petition, Petitioner submits that the '532 Patent's claims do not require further construction and should receive their plain and ordinary meaning.

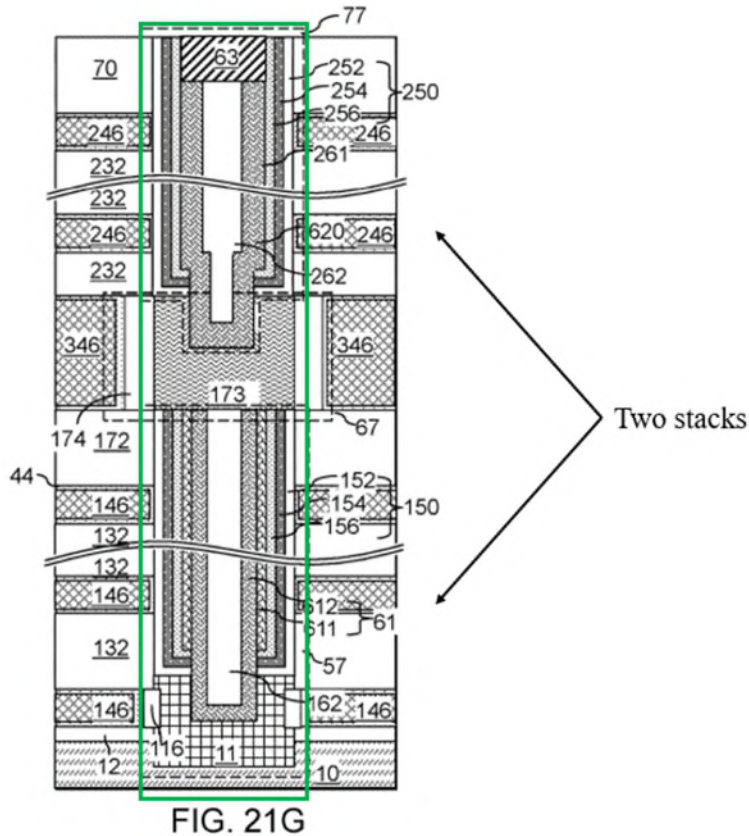
VIII. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA in the field of the '532 Patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience). This POSITA would have been aware of and generally knowledgeable about 3D NAND's structure, how it is manufactured, and its component parts. See Banerjee, ¶¶ 36-40.

IX. DESCRIPTION OF THE PRIOR ART

A. Costa

Costa relates to “multi-tier three-dimensional memory devices containing dummy memory cells for providing inter-tier connection and methods of making the same.” Costa, [0002]. As explained below, just like the '532 Patent, Costa discloses forming a vertical memory channel (shown in green below) in a multi-tier three-dimensional memory structure:



Id., Fig. 21G (annotated); Banerjee, ¶¶ 77-79. And Costa identifies the same problem to be overcome as does the '532 Patent—namely, that forming channel holes becomes more difficult as the aspect ratio of the holes increases due to the increased number of layers. Compare Costa, [0003] (“Some of the challenges for fabricating a multi-tier memory stack structure include formation of memory openings having high aspect ratios and alleviation of effects of misalignment of tier-level memory openings formed in different tier structures.”) with Ex. 1001, 1:26-37 (“As semiconductor technology advances, three-dimensional (3D) memory devices ... keep scaling more oxide/nitride (ON) layers [and] it becomes difficult to use a single etching process to form the channel holes in the 3D memory devices that have

a substantial depth. As the channel hole aspect ratio increases, channel hole etching becomes exponentially slower.”). Thus, Costa provides methods “for providing a reliable connection between vertically neighboring memory stack structures.” Costa, [0003]; Banerjee, ¶¶ 80-81.

Specifically, Costa discloses forming “first alternating stack (132, 142)” on substrate 10. Costa, [0126]-[0127]. First-tier insulating cap layer 172 is formed over the first alternating stack (132, 142) to form the first tier structure (132, 142, 172), which can be patterned to form “a first terrace region” located in a contact region of the device. *Id.*, [0134]-[0135]. First-tier openings (149, 119) are then formed for example by lithographic patterning and an anisotropic etch process. *Id.*, [0137]; Banerjee, ¶¶ 82-83.

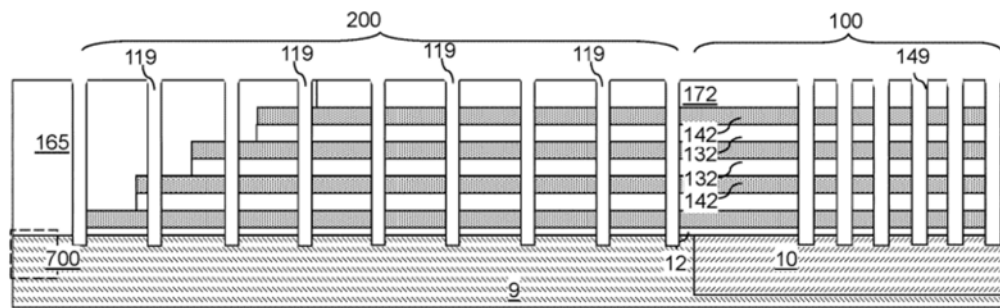


FIG. 3B

Costa, Fig. 3B; Banerjee, ¶ 84. A memory channel is formed in first-tier memory openings 149 by first forming epitaxial channel portion 11 in the bottom of each hole, subsequently forming a memory film 150 and first outer and inner

semiconductor channel layers (611, 612), and filling the remainder of the opening with dielectric core 162. Costa, [0141]-[0160].

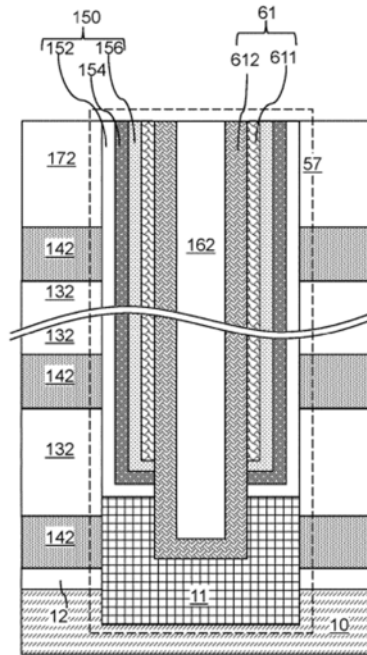
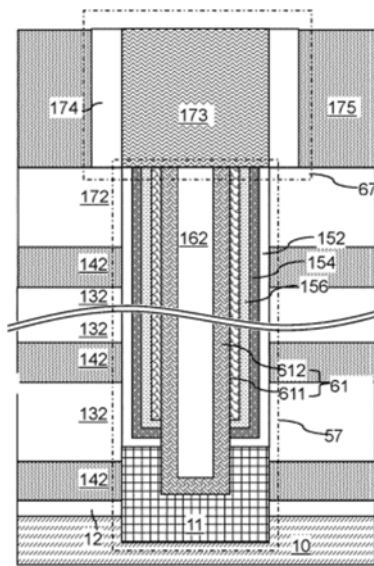


FIG. 4G

Id., Fig. 4G; Banerjee, ¶ 85. In one embodiment, a joint-level doped semiconductor layer 173L is formed over the first-tier structure (*e.g.*, shown above in Fig. 4G) and subsequently patterned, removing the portions not over first-tier openings (149, 119), leaving joint-level doped semiconductor portion 173. Costa, [0263]-[0266], Figs. 20A-B. Costa states that “[i]n one embodiment, the bottom surface of each joint-level doped semiconductor portion 173 can contact an entire top surface of an underlying first memory opening fill structure 57.” *Id.*, [0265]. Exposed portions of semiconductor portion 173 can be oxidized, converting those portions to dielectric material 174’. *Id.*, [0266], Fig. 20C. An annular dielectric spacer is formed by removing the top portion of 174’. *Id.*, [0268], [0266] (“In an alternative embodiment

shown in the dashed line inset in FIG. 20C, only the sidewalls of the joint-level doped semiconductor portions 173 are oxidized to form a first annular dielectric spacer 174.”), Fig. 20C. Joint-level spacer material 175 is then deposited over the first-tier structure and around semiconductor portion 173 and dielectric spacer 174. *Id.*, [0268]; Banerjee, ¶¶ 86-89.

FIG. 20D



Costa, Fig. 20D; Banerjee, ¶ 89.

A second-tier structure and memory channel are formed in much the same way as the first-tier structure. A second alternating stack (232, 242) is formed over joint level spacer 175, joint-level doped semiconductor portion 173, and dielectric spacer 174. Costa, [270], [0178]-[0180]. Second-tier insulating cap layer 70 is formed over the second alternating stack, and second-tier memory holes 249 are formed over the second alternating stack, and second-tier memory holes 249 are formed by a similar process to that of first-tier memory holes 149. *Id.*, [270], [0183]-

[0192]. A memory channel is formed in second-tier memory openings 249 by forming a memory film 250 (comprised of layers 252, 254, 256) and second outer and inner semiconductor channel layers (621, 622), and filling the remainder of the opening with dielectric core 262. *Id.*, [0272]-[0276]. Drain region 63 is then formed in a recess etched into dielectric core 262 and second inner semiconductor channel layer 622). *Id.*, [0277]. Drain region 63 is deposited in and above the dielectric core cavity, and overlying material is planarized. *Id.*, [0212], [0277] (referring to [0212] description); Banerjee, ¶¶ 90-93.

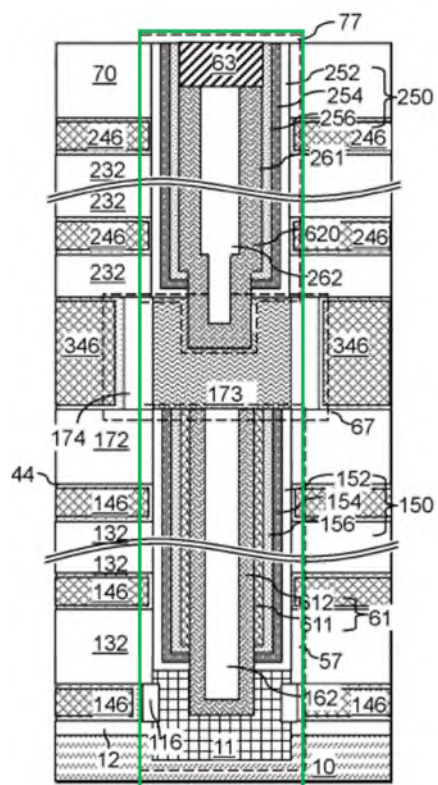


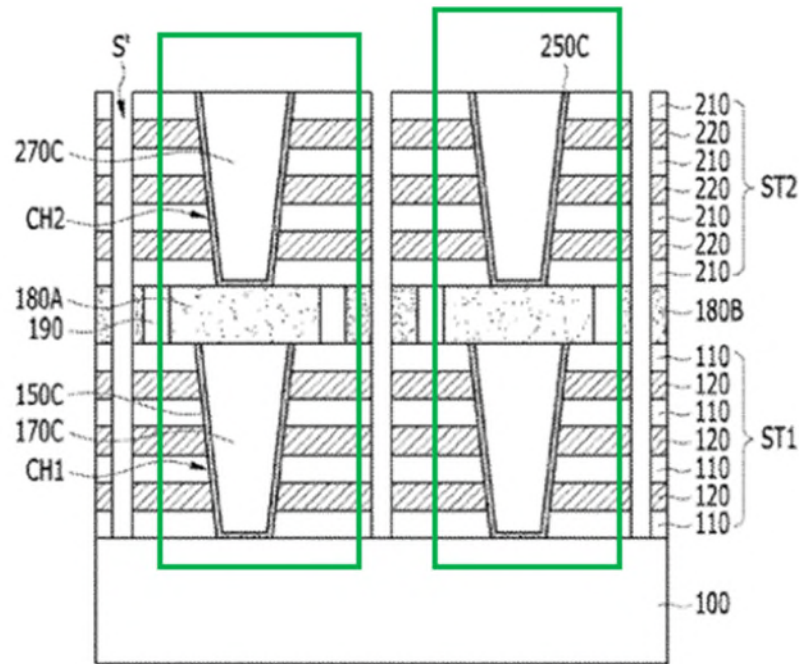
FIG. 21G

Costa, Fig. 21G (annotated); Banerjee, ¶ 94. Thus, a vertical memory channel (shown in green above) is formed. Costa, [0278]; Banerjee, ¶ 94.

B. Oh

Much like Costa, Oh relates to forming a vertical memory channels (shown in green) through two separate decks:

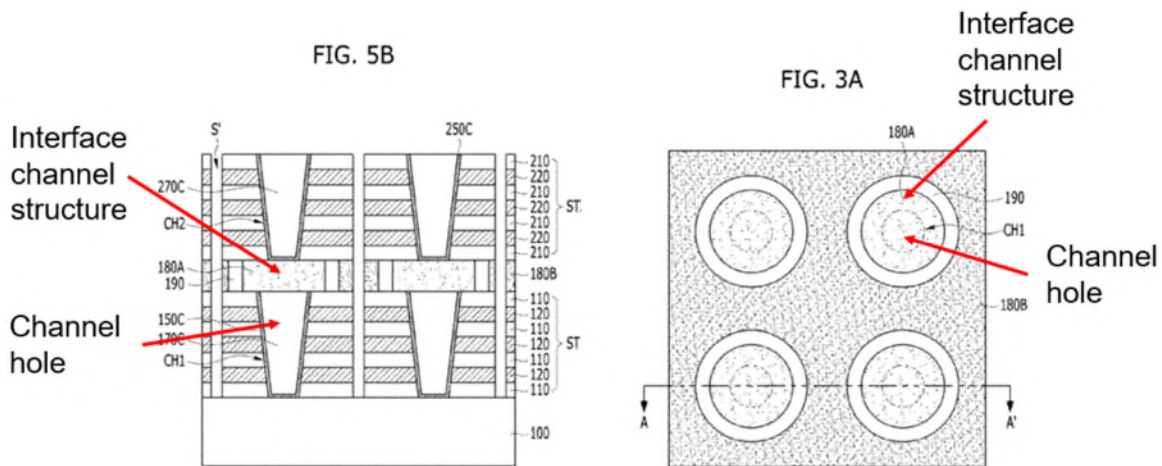
FIG. 5B



Oh, Fig. 5B (annotated); Banerjee, ¶¶ 95-96.

Oh addresses alignment issues in multi-stack structures. First, in the context of slit structures, Oh discusses the difficulty in aligning the slit structures that are separately formed through each stack. Oh, [0047]. In particular, Oh discloses that slits have a small width, magnifying alignment issues. *Id.* As such, Oh teaches: “Thus, an overlap margin is low and a manufacturing process is likely to fall.” *Id.*; Banerjee, ¶ 97.

In view of this well-known processing issue, when turning to Oh's channel structures, Oh teaches: "Referring to FIG. 3A the channel connection pattern 180A may have an island shape which overlaps the first channel holes CH1 [in] order to secure an overlap margin between the channel connection pattern 180A and the first channel hole CH1, the channel connection pattern 180A may have a larger width than the top surface of the first channel hole CH1." Oh, [0061]. This "overlap margin" is shown below:



Id., Figs. 3A, 5B. In other words, the "overlap margin" ensures that even if misalignment occurs, the channel interface structure will contact the channel semiconductor film in the first, underlying memory hole. *Id.*; Banerjee, ¶ 98.

Oh teaches another benefit of providing a wider interface channel structure. Specifically, the bottom of the top hole will have a smaller width than the channel interface structure, likewise providing an "overlap margin" when forming the second, overlying hole. Oh, [0060]; Banerjee, ¶ 98.

X. GROUND 1: INDEPENDENT CLAIMS 1, 11, AND 18, AND DEPENDENT CLAIMS 2, 3, 13, 15-17, AND 20, ARE OBVIOUS OVER COSTA

A. Claim 1:

- 1. [1.PRE] “A method of forming a joint opening structure in a three-dimensional (3D) memory device, comprising:”**

To the extent the preamble is limiting, Costa discloses it.

To start, when the '532 Patent uses the term “joint opening structure,” it is referring to an opening structure of a three-dimensional (3D) memory device created by “combining two through hole formation processes.” Ex. 1001, 15:33-36. That is, it is referring to the well-known technique of forming channel structures in multi-tier memory devices using two etch processes. Banerjee, ¶¶ 102-04.

Costa discloses forming a joint opening structure by etching a first memory through hole in a first stack (and forming a channel structure therein), forming a second stack on the first stack, and etching a second memory through hole in the second stack (and forming a channel structure therein). Costa, [0002] (“[t]he present disclosure relates generally to the field of three-dimensional memory devices and specifically to multi-tier three-dimensional memory devices ... and methods of making the same.”), [0003] (“fabricating a multi-tier memory stack structure” and “providing a reliable connection between vertically neighboring memory stack structures”), Figs. 4A-4G, 10-11 (first-tier opening (149, 119), and second-tier openings (249, 219)); Banerjee, ¶¶ 105-06.

2. [1.A] “forming a first stacked layer on a substrate;”

As described by the '532 Patent, “the first stacked layer 2 can be formed on the substrate 1 [and] can include a plurality of oxide/nitride layer pairs.” Ex. 1001, 9:23-25, Fig. 1.

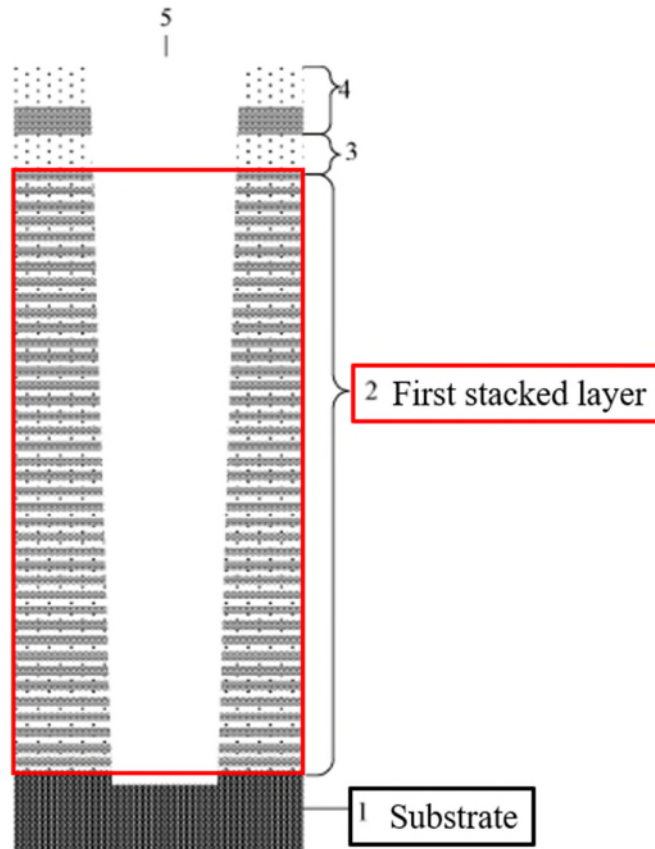
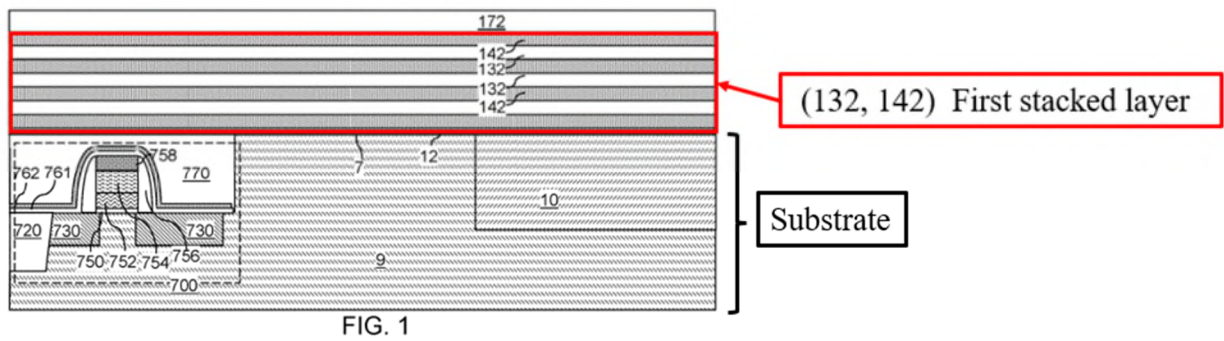


FIG. 1

Id., Fig. 1 (annotated); Banerjee, ¶ 108.

Costa discloses the same process, namely, forming a first stacked layer (“first alternating stack” 132, 142) on a substrate. Costa, [0134]; Banerjee, ¶¶ 107, 109.



Costa, Fig. 1 (annotated); Banerjee, ¶ 109.

Specifically, “[a]n alternating stack of first material layers and second material layers is subsequently formed. Each first material layer [132] can include a first material, and each second material layer [142] can include a second material that is different from the first material.” Costa, [0126]. The first material layer 132 can be an insulating material, such as “silicon oxide ... [or] dielectric metal oxides ... commonly known as high dielectric constant (high-k) dielectric oxides....” *Id.*, [0126], [0129]. The second material layers 142 can be a “sacrificial material,” such as “silicon nitride,” that “can be subsequently replaced with electrically conductive electrodes....” *Id.*, [0129]-[0131]; Banerjee, ¶¶ 110-12.

3. [1.B] “forming a first through hole penetrating the first stacked layer to expose the substrate;”

The '532 Patent describes forming the first through hole 5 by overlaying a mask layer 4 and performing an etching process to form the first through hole.

Ex. 1001, 9:65-10:2, 10:12-25.

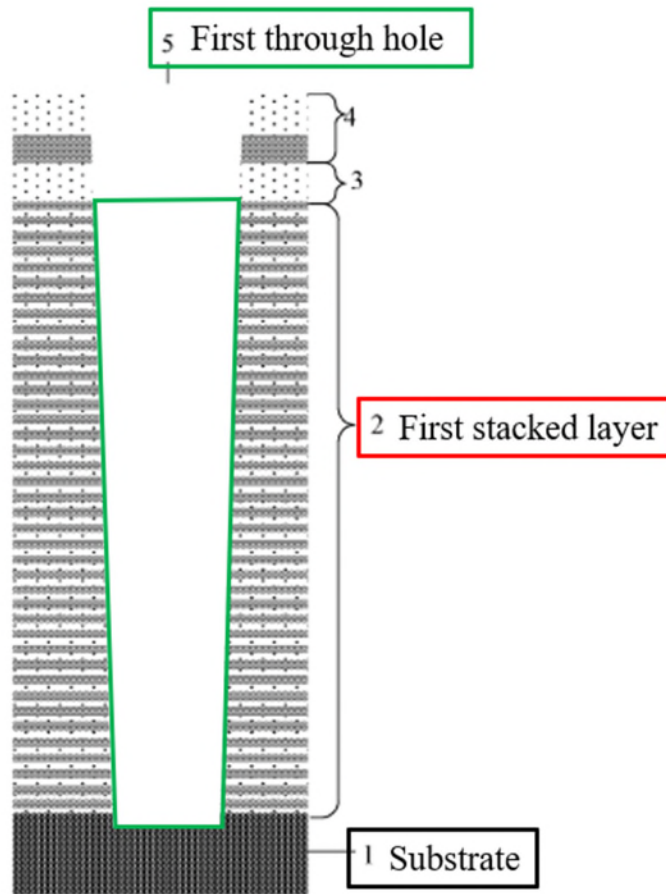
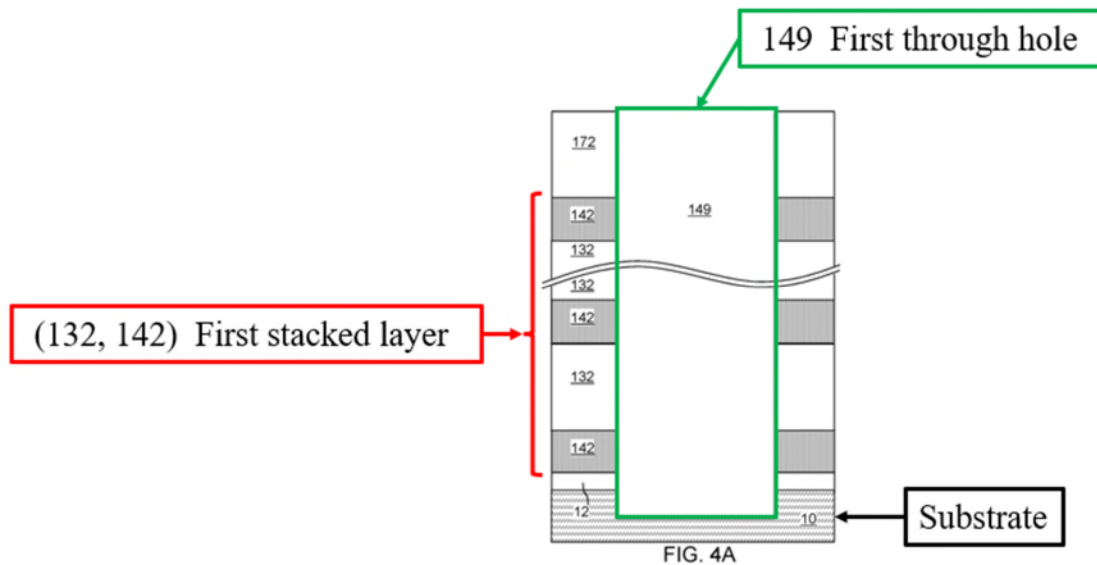


FIG. 1

Id., Fig. 1 (annotated); Banerjee, ¶ 114. The “first through hole” could map to include the hole portion that extends through the connection layer 3 as well, similar to the analysis set forth in [1.F] with respect to the “second through hole.” The difference is immaterial to Costa, because Costa’s third channel structure is above the “first through hole” regardless of whether that hole includes a portion through the connection layer in Costa.

As demonstrated below, Costa discloses the same process, namely, forming a first through hole (“first-tier memory opening[]” 149) that penetrates the first

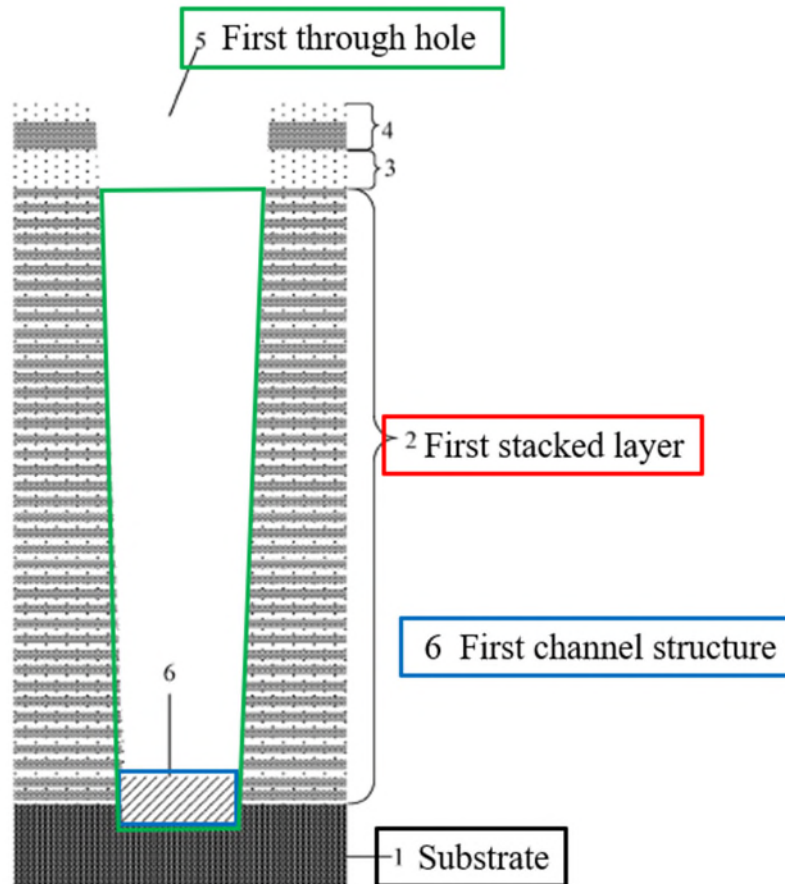
stacked layer (“first alternating stack” 132, 142). Costa discloses that “first-tier openings (149, 119) extending to a top surface of the substrate (9, 10) are formed through the first tier structure (132, 142, 172, 165).” Costa, [0137]; Banerjee, ¶¶ 113, 115; *see also* Costa, [0137] (describing forming first-tier openings by lithographic patterning and etching, i.e., masking). As shown below, first-tier memory opening 149 penetrates the first alternating stack (132, 142) to expose substrate 10:



Id., Fig. 4A (annotated); Banerjee, ¶¶ 116-17; *see also* Costa, Fig. 3B. The “second through hole” could exclude the portion through the connection layer 172. That difference is immaterial, because Costa’s third channel structure is above the through-hole under either interpretation (the “second hole” including the connection layer or not). *See* limitation [1.E].

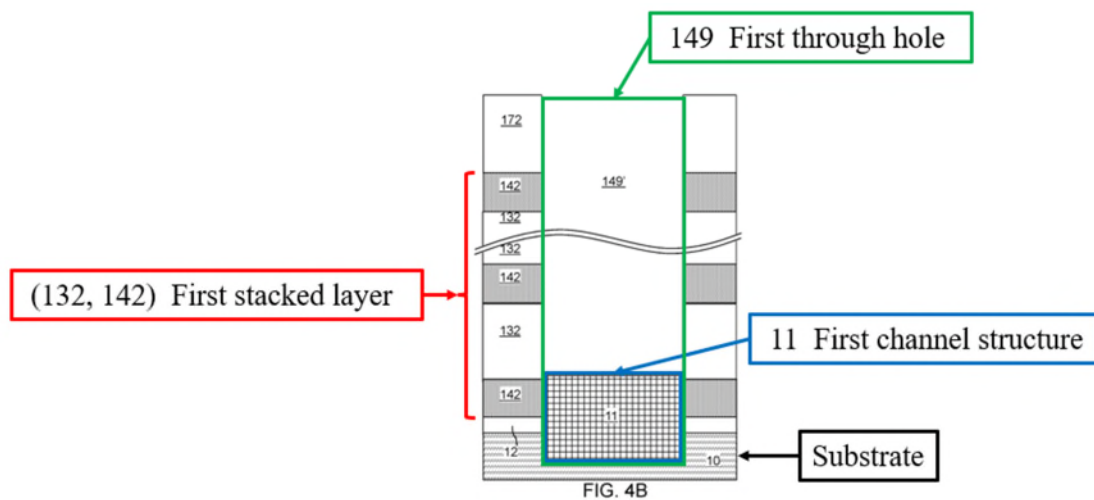
4. [1.C] “forming a first channel structure at a bottom of the first through hole and in contact with the substrate;”

The '532 Patent describes forming the claimed first channel structure by depositing material “on the surface of the substrate 1 that is exposed by the first through hole 5” (i.e. at the bottom of the first through hole). Ex. 1001, 10:26-30, Fig. 2. As described by the '532 Patent, “the first channel structure [] can be a polycrystalline silicon (polysilicon) layer formed by using a selective epitaxial process.” *Id.* 10:28-30; Banerjee, ¶¶ 119-20.



Ex. 1001, Fig. 2 (annotated); Banerjee ¶ 121.

Costa discloses the same, namely, forming a first channel structure (“epitaxial channel portion 11”) overlaying the surface of the substrate (“substrate 10”) that is exposed by the first through hole (“first tier memory opening” 149). Costa, [0143] (“[E]pitaxial channel portion (*e.g.*, an epitaxial pedestal) 11 can be formed at the bottom portion of each first-tier memory opening 149...”); Banerjee, ¶¶ 118, 122; *see also* Costa, [0137] (“substrate” includes portions 9 and 10). Epitaxial channel portion 11 overlays the surface of the substrate 10 that is exposed by the first-tier memory opening 149:



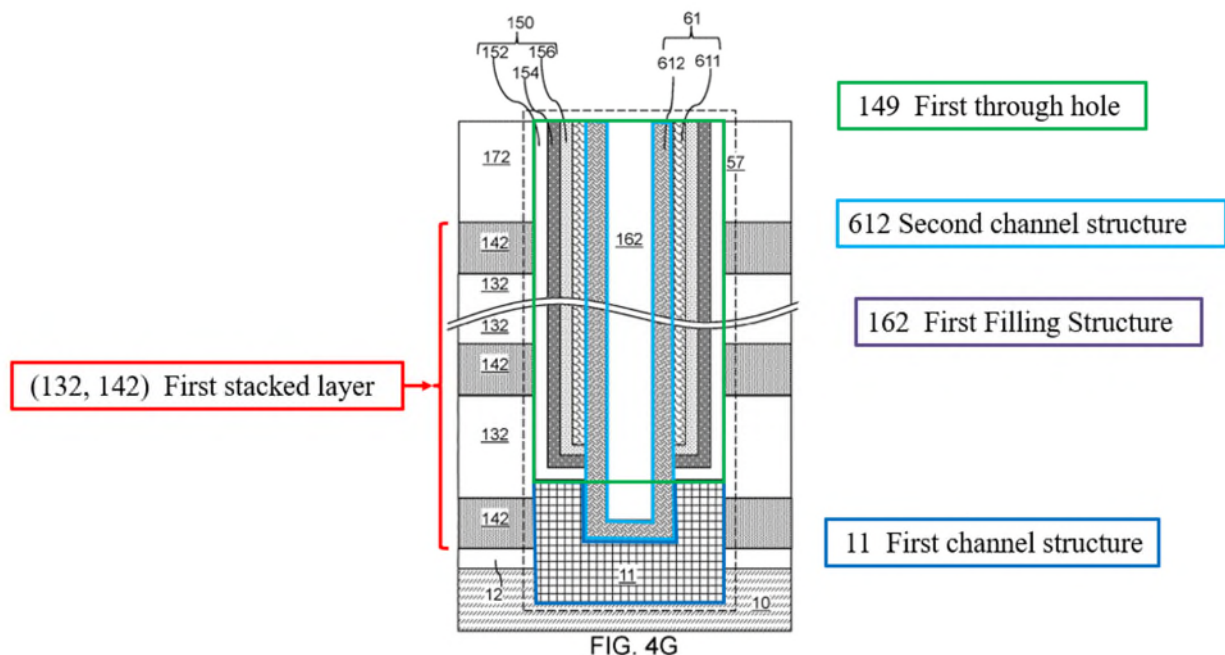
Id., Fig. 4B (annotated); *see also* Banerjee, ¶¶ 123-25.

5. [1.D] “forming a second channel structure in the first through hole and in contact with the first channel structure;”

The '532 Patent describes “form[ing a second channel structure] on the sidewall of the first functional layer and the exposed surface of the first channel structure 6.” Ex. 1001, 11:21-40; *see also id.*, Figs. 5-6, 11:41-12:19 (describing

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Costa discloses that “a first inner semiconductor channel layer 612 can be deposited directly on the semiconductor surface of the epitaxial channel portion 11 ... and directly on the [optional] first outer semiconductor channel layer 611.” Costa, [0156]. In other words, first inner semiconductor channel layer 612 is formed in first-tier memory opening 149. The 611 and 612 layers are “amorphous silicon or polysilicon.” *Id.*, [0152], [0156]. “The materials of the first outer semiconductor channel layer 611 and the first inner semiconductor channel layer 612 are collectively referred to as a first semiconductor channel material.” *Id.*, [0157].



Id., Fig. 4G (annotated); Banerjee, ¶ 132.

6. **[1.E] “forming a third channel structure above the first through hole and in contact with the second channel structure, wherein a size of the third channel structure along a lateral direction is larger than a top aperture of the first through hole;”**

The '532 Patent describes forming the claimed third channel structure in a groove 13 formed in the first insulating connection layer 3. Ex. 1001, 12:31-36, 12:55-56. “[T]he third channel structure can be a polycrystalline silicon [l]ayer formed by using a deposition process.” *Id.*, 12:58-60. “An area of the projection ‘x’ of the first groove on the substrate 1 can be larger than an area of the projection ‘y’ of the first through hole 5 on the substrate 1.” *Id.*, 12:34-36, Fig. 10A. The '532 Patent further describes that, “[i]n some embodiments ... a portion of the third channel structure 14 that is adjacent with the bottom nitride layer of the second stacked layer 15, or is adjacent with the top nitride layer of the first stacked layer 2 can be converted to an oxide layer by an oxidation process.” *Id.*, 16:60-64. The third channel structure 14 is illustrated in Figure 11B below:

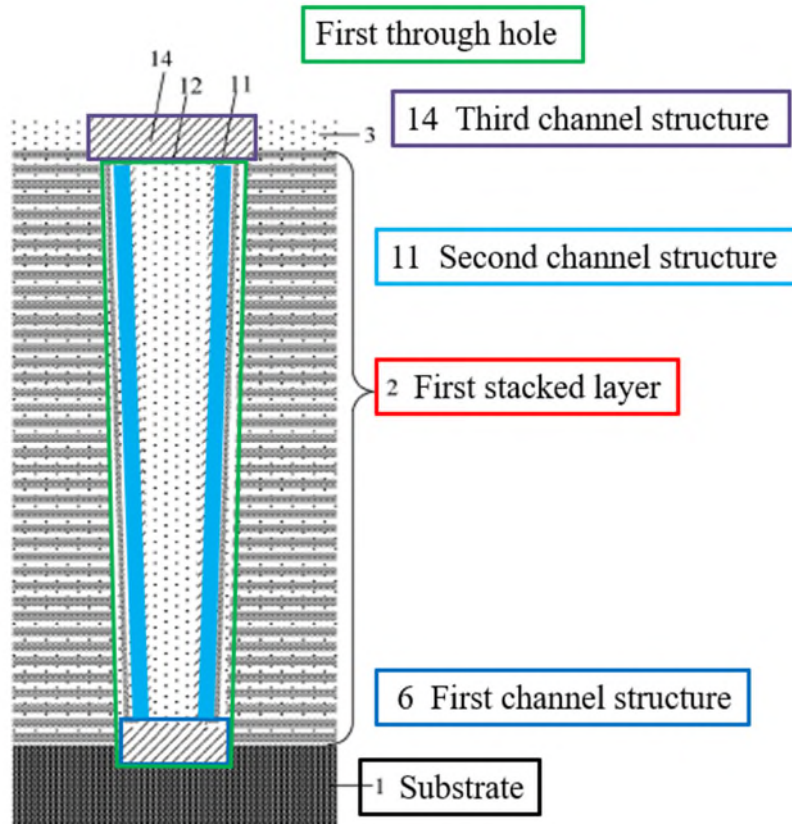


FIG. 11B

Id., Fig. 11B (annotated); Banerjee, ¶¶ 134-36.

Costa discloses, or at least renders obvious, this limitation. Banerjee, ¶¶ 133, 137.

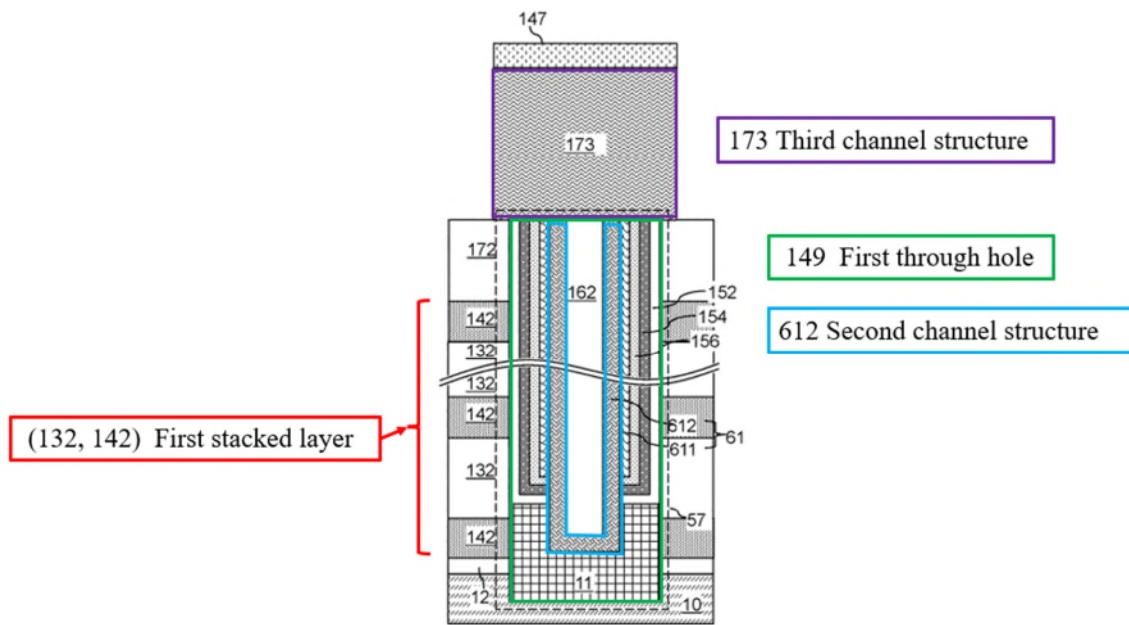
a. Costa's Disclosures as Understood by a POSITA

Costa discloses forming a third channel structure (“joint-level doped semiconductor portion 173”) above the first through hole (“first-tier memory opening 149”) and in contact with the second channel structure (“first inner semiconductor channel layer 612”), where the third channel structure (173) completely covers the underlying first memory opening fill structure 57. Costa,

[0265]. As explained below, a POSITA would have understood this to mean that the third channel structure in Costa is wider than the underlying first through hole to account for alignment margin and, thus, a size of the third channel structure along a lateral direction is larger than a top aperture of the first through hole (“first-tier memory opening 149”) on the substrate. In other words, to ensure that the third channel structure (173) completely covers the underlying first memory opening fill structure 57 and protects all portions thereof, it would be made wider than the underlying fill structure to ensure it completely covers the fill structure even if the third channel structure (173) is not perfectly aligned over the fill structure 57. Indeed, as demonstrated below, Costa illustrates that the third channel structure 173 is wider than the fill structure in Figure 20B. Banerjee, ¶ 138.

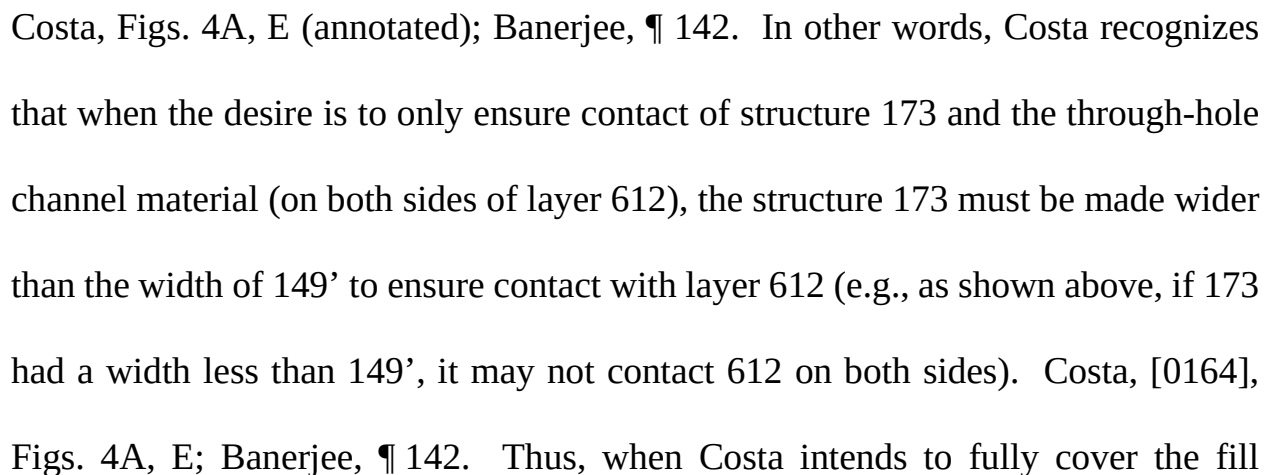
Costa’s “third exemplary structure” modifies the “first exemplary structure” (which this Ground maps to the claim limitations to this point) by modifying the interface between the two tiers. Costa, [0263]. In particular, as shown below before an optional oxidation step in both embodiments (*see infra*), Costa’s “third exemplary structure” modifies the interface (including structure 173) between the two decks. *Compare id.*, Figs. 6A-H with Figures 20A-D.

memory opening fill structure 57.” Costa, [0265]. As illustrated in Figure 20B below, Costa’s joint-level doped semiconductor portion 173 not only covers the entire first-tier memory opening 149 (i.e., a projection of 173 on the substrate covers a projection of 149 on the substrate), but is wider than the first-tier memory opening and is in contact with the second channel structure.



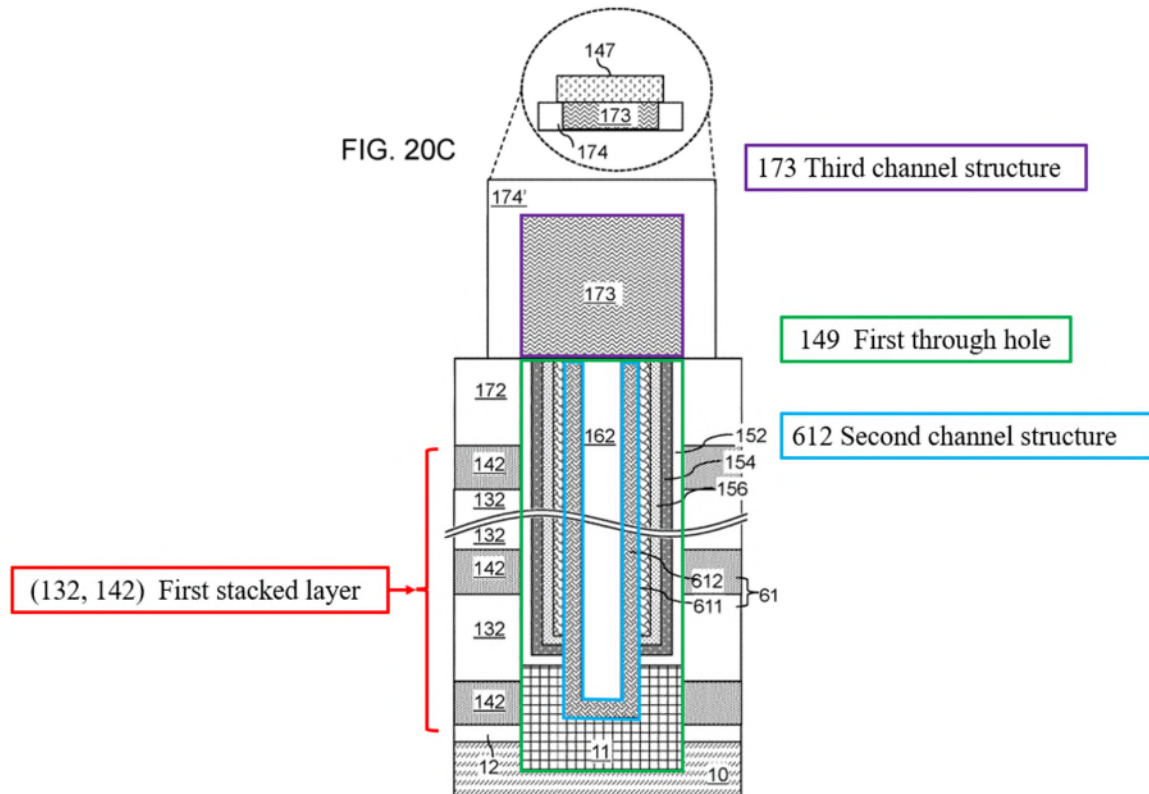
Id., Fig. 20B; Banerjee, ¶ 141.

That Costa discloses the above additional margin, i.e., more than fully covering the fill structure 57, is hardly surprising, because in other embodiments, Costa expressly recognizes the need “to account for misalignment” when forming a channel interface structure over the first channel structure. Costa, [0164]; Banerjee, ¶ 142. Specifically, in the first exemplary embodiment, Costa states: “The width



structure as it does in the third exemplary embodiment, consistent with accounting for misalignment, a POSITA would have understood that structure 173 would be made wider than the fill structure. Banerjee, ¶ 143. Indeed, as discussed below, this provides the additional benefit of protecting the entire fill structure and surrounding layers during both oxidation and formation of the second through hole. Banerjee, ¶ 145.

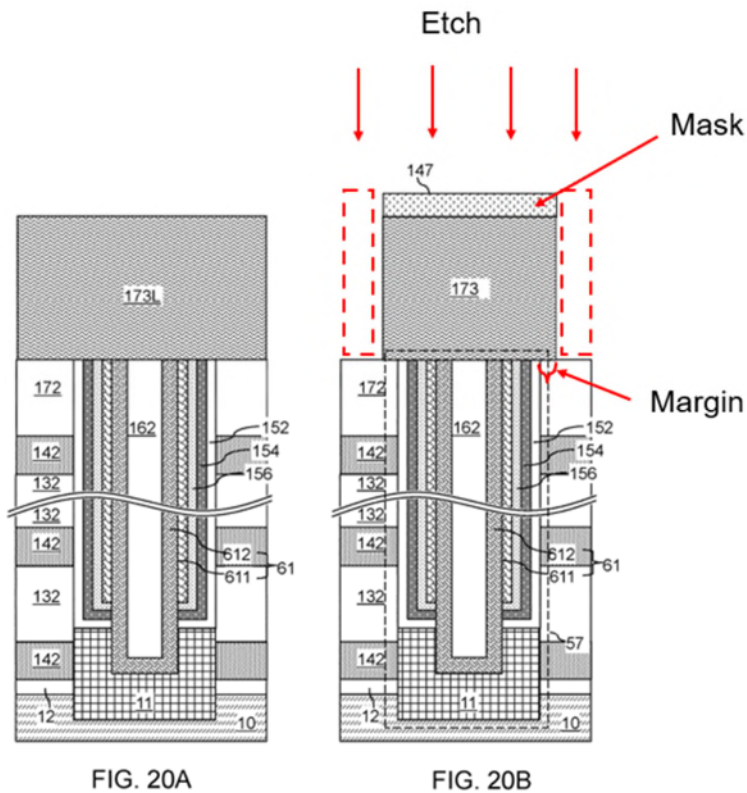
Next, in the third exemplary embodiment, Costa discloses an optional step that oxidizes and forms 174' (it is an optional step in the first exemplary embodiment as well). Costa, [0266] (“in one embodiment”). Costa makes clear that this step is optional because, when it refers to 174' portions, it states “if present.” *Id.*, [0268] (“Each remaining annular portion of the dielectric oxide portions 174' (if present) constitutes an annular dielectric spacer 174.”); *see also id.*, [0172] (same). Without the oxidation, the third channel structure below would be significantly wider than the top aperture of fill structure 57 (first hole), as shown below. Banerjee, ¶ 144. And because claim 1 is a method claim, even with this optional oxidation, an initial third channel structure has been formed that is clearly wider than the underlying through hole.



Costa, Fig. 20C (annotated), [0268] (referring to 174' and noting "if present"); Banerjee, ¶ 144.

Even with the oxidation step, Costa's description confirms that the third channel structure 173 will be, in practice, wider than the top aperture of fill structure 57 (first hole), because to achieve Costa's express goal of covering the fill structure, a POSITA would have understood that it is necessary to implement a margin that increases the width of the third channel structure (which, alternatively, certainly would have been obvious). Banerjee, ¶ 145. To start, Costa's description in the third exemplary embodiment consistently teaches that the third channel structure 173 "can contact an entire top surface of an underlying first memory opening fill

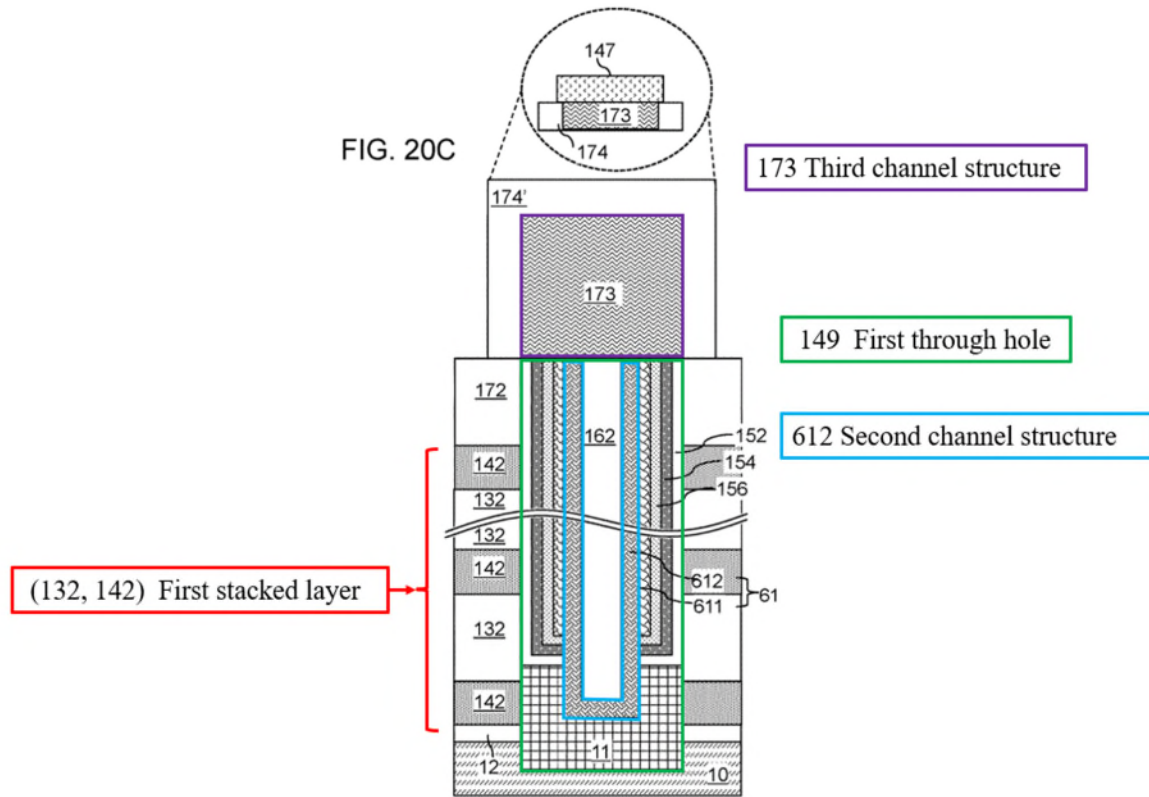
structure 57.” Costa, [0265]. But Costa’s process for forming channel structure 173 is not self-aligned, and in fact, multiple steps require unaligned processing. Costa masks the top of 173L (with 147) to remove portions of 173L. Costa, [0265], Figs. 20A, B. In doing so, Costa shows mask 147 as being wider than the entire fill structure 57, *i.e.*, Costa applies a margin, ensuring that the final structure 173 will fully cover fill structure 57 because the width of 147 is not self-aligned to the underlying fill structure 57:



Id., Figs. 20A, B (annotated); Banerjee, ¶ 146. Put simply, the mask is made wider than the fill structure, because there will be process variations and misalignment in some devices. Thus, a POSITA would have known that, to compensate for such

misalignment and still cover the entire fill structure 57, the third channel structure 173 must be designed to be wider than fill structure 57. Banerjee, ¶ 146; Costa, [0265] (“each joint-level doped semiconductor portion 173 can contact an entire top surface of an underlying first memory opening fill structure 57”).

Additional process variations also would lead a POSITA to understand that Costa’s third structure 173 would be wider than the through hole. Take for example the Costa embodiment that uses an additional oxidation step (an embodiment of the third exemplary embodiment, that is, an option applicable to the third exemplary embodiment). Costa, [0266]. Even in this embodiment, after oxidizing the exposed surfaces of semiconductor portion 173, Figure 20C (reproduced below) shows that the remaining portion of doped semiconductor portion 173 (i.e., the portion not oxidized) is at least as wide as fill structure 57 (i.e., the structures filling first-tier memory opening 149). *Id.*, [0266], Fig. 20C.



Id., Fig. 20C (annotated); Banerjee, ¶ 147. Critically, were the oxidation to extend too far, the interface would become non-conductive in areas approaching the semiconductor films (*see infra*), thereby disadvantageously increasing contact resistance and damaging the data storage and blocking layers (*see infra*). Here, too, a POSITA would have applied a margin for the same reasons. Banerjee, ¶ 147.

b. Costa in View of the Knowledge of a POSITA Renders This Limitation Obvious

To the extent PO argues that Costa fails to disclose this limitation because Figure 20C, above, shows joint-level doped semiconductor portion 173 (i.e. the portion not oxidized) having the same size as that of fill structure 57 (i.e., the

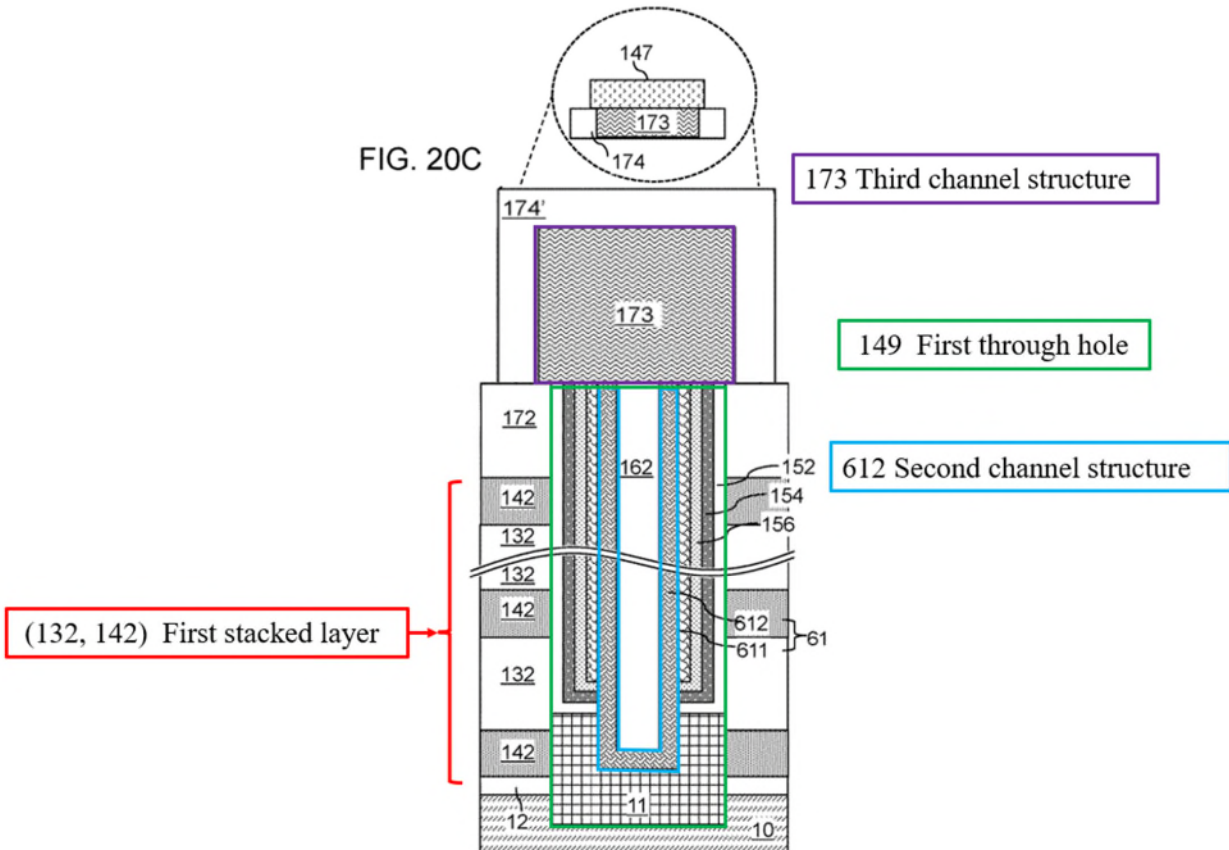
“aperture” of “the first through hole”), PO would be incorrect for all of the reasons above (including that element 173 is shown as wider than the fill structure in Figure 20B, that the oxide portions are optional, and the margins that Costa describes in the first exemplary embodiment). Regardless, a POSITA would have found it obvious to ensure that Costa’s joint-level doped semiconductor portion 173 is wider than the top aperture of the first through hole. Again, Costa teaches that one purpose of doped semiconductor portion 173 is to “protect[] the underlying first vertical semiconductor channel 61 from oxidation during a subsequent oxidation process.” Costa, [0265]. To serve this purpose, Costa discloses forming portion 173 to “contact an entire top surface of an underlying first memory opening fill structure 57.” *Id.* This purpose alone would have motivated a POSITA to ensure that doped semiconductor portion 173 is wider than the underlying fill structure 57 to ensure it accomplishes the protection function, particularly given process variations during fabrication. *Id.*, [0266]; Banerjee, ¶ 148.

It was further well known to protect the entire fill structure, not just the vertical channel layer. Banerjee, ¶ 149. For example, U.S. Pat. No. 9,401,371 discloses using a select sacrificial dielectric material surrounding the fill structures such that subsequent processing removes “a very minimal amount of the oxide of the memory layer” that includes “a tunneling layer 1132, the charge storage layer 1131, and the blocking layer 1130.” Ex. 1019, 16:60-17:14, 17:50-56. By way of

another example, U.S. Pat. No. 9,570,460 discloses a “cover layer” that protects “memory film 7, 9, 11” during subsequent processing, i.e., the blocking layer, tunneling layer, and charge storage layer. Ex. 1020, 11:22-40; Banerjee, ¶¶ 149-50. Costa’s fill structure may comprise a variety of different material compositions, e.g., the blocking layer may be metal oxide, silicon nitride, or a combination of silicon oxynitride and silicon nitride, and the charge storage layer may be titanium or semiconductor material (floating gate) or silicon nitride (continuous charge trap layer). *E.g.*, Costa, [0145]-[0147], [0150]. These layers (and horizontally adjacent layers of the stack) are subject to damage during the subsequent optional oxidation step and the subsequent etch that forms the overlying second through hole. And if the processing damages even the top most memory cell, this compromises the entire memory string, given how read and write operations occur in 3D NAND. Banerjee, ¶ 151.

As to the optional oxidation step, it was well known that inadvertently oxidizing the blocking layer may change its material composition, e.g., changing the target dielectric constant for this material and changing the coupling capacitance that may lead to malfunction. Banerjee, ¶ 152. A POSITA also knew that inadvertently oxidizing the charge storage layer would damage its storage function. Banerjee, ¶ 153. It was well known that when performing an oxidation process, “other material” (than the target material) may be “unintentionally oxidized.” Ex. 1021,

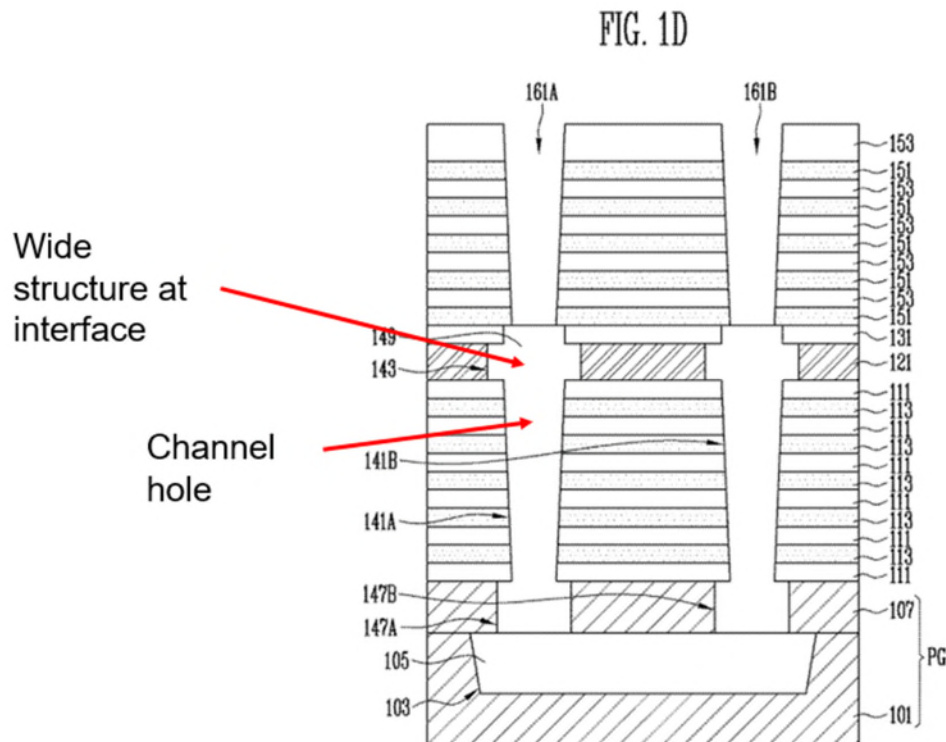
12:37-45; Banerjee, ¶ 152. Unlike Costa's first exemplary embodiment that does not intend to cover the entire fill structure, Costa's embodiment of Figure 20 provides additional protection. Thus, as shown below, a POSITA would have been motivated to form Costa's third channel structure wider than the fill structure such that the optional oxidation does not oxidize any materials near (e.g., over) any part of the fill structure, thereby ensuring that oxidation does not extend to the fill structure. Banerjee, ¶ 154.



Costa, Fig. 20C (modified and annotated); Banerjee, ¶ 155.

As to the second etch, it was well known that an interface structure (here, third channel structure) may provide protection for the underlying layers during etching

of the second through hole. Yoon, for example, discloses: “In addition, according to the first embodiment of the present invention, since the overlay margins between the second through-areas 161A and 161B and the first through-areas 141A and 141B may be enlarged, damage of the first and second material layers 111 and 113 around the first through-areas 141A and 141B due to the etching process for forming the second through- areas 161A and 161B may be prevented.” Ex. 1007, [0037]. As can be seen below, the wide structure over the underlying channel hole protects everything under 149 even if the etch to form hole 161A does not perfectly align above the underlying hole:



Ex. 1007, Fig. 1D (annotated); Banerjee, ¶ 156. In view of these teachings, a POSITA would have been motivated to form Costa’s third-channel structure wider

than the fill structure. Costa discloses an anisotropic etch that is selective towards alternating stack layers 232/242 and dielectric material portion 265. Costa, [0193]. These layers and dielectric portion may comprise, e.g., silicon oxide and silicon nitride. *Id.*, [0181]; Banerjee, ¶ 157. As can be seen below, if the third channel structure is the same width as the underlying fill structure, the etch that forms the overlying memory hole must perfectly align or the etch will not terminate on structure 173:

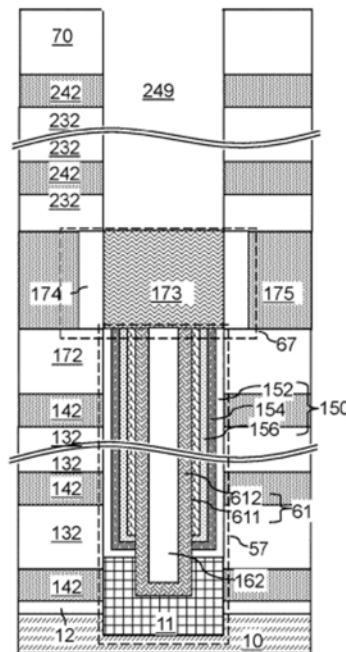
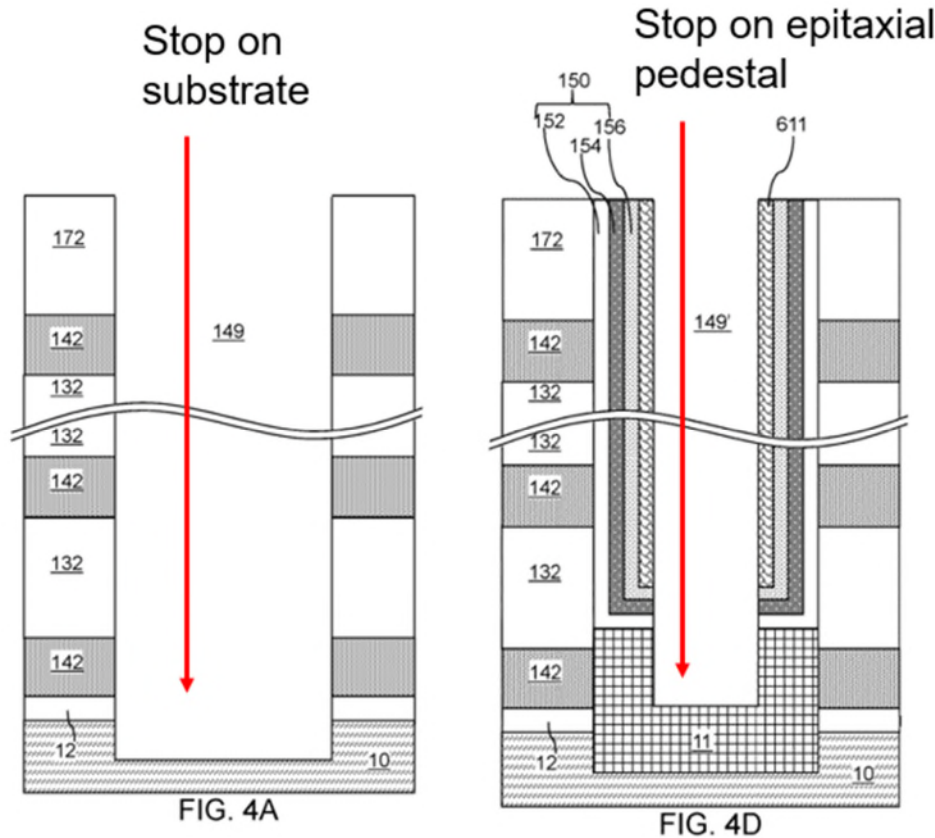


FIG. 21A

Costa, Fig. 21A; Banerjee, ¶ 157. In other words, in the oxidation embodiment, even a little misalignment would etch 174. Banerjee, ¶ 157. Because if the etch targets oxide, the etch would quickly etch 174 and risk damage to underlying layers. In short, a wide 173 acts as a protective etch stop when forming the second channel

hole. Banerjee, ¶ 158. This greatly simplifies Costa's first exemplary embodiment, in which Costa uses a series of selective etches to etch down to 173 because it does not have a wider structure 173 to terminate the etch. Costa, [0171], Fig. 6F-G; Banerjee, ¶ 158.

Also note that employing structure 173 to terminate the etch is consistent with other Costa disclosures. Costa, for example, teaches using substrate 9/10 as the "stopping layer" for the anisotropic etch that forms the first through hole. Costa, [0139]. Similarly, Costa discloses anisotropic etches that are selective towards the memory fill portions, which stop on the epitaxial pedestal (11), when removing the horizontal portions of the fill layers above epitaxial pedestal. *Id.*, [0153]; Banerjee, ¶ 159.

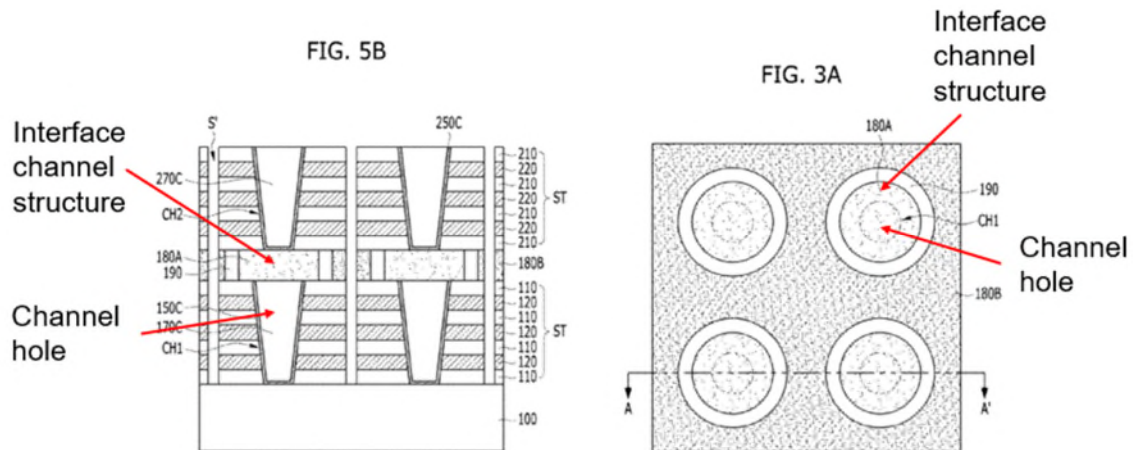


Costa, Figs. 4A (annotated), 4D (annotated).

Moreover, as discussed above, Costa describes a non-self-aligned process that would produce some degree of misalignment between, e.g., the target placement of the third channel structure and actual placement of the third channel structure (and more generally, the first and second memory holes) due to process variations during fabrication. Banerjee, ¶ 160; Ex. 1014, 2:60-3:6 (noting process variation issues in non-self-aligned processes); Ex. 1015, 20-21. And a POSITA would have understood and found it obvious to ensure alignment (i.e., electrical contact between upper and lower deck memory channels) by including a third channel structure with a larger diameter than the underlying memory hole. This was a basic concept known

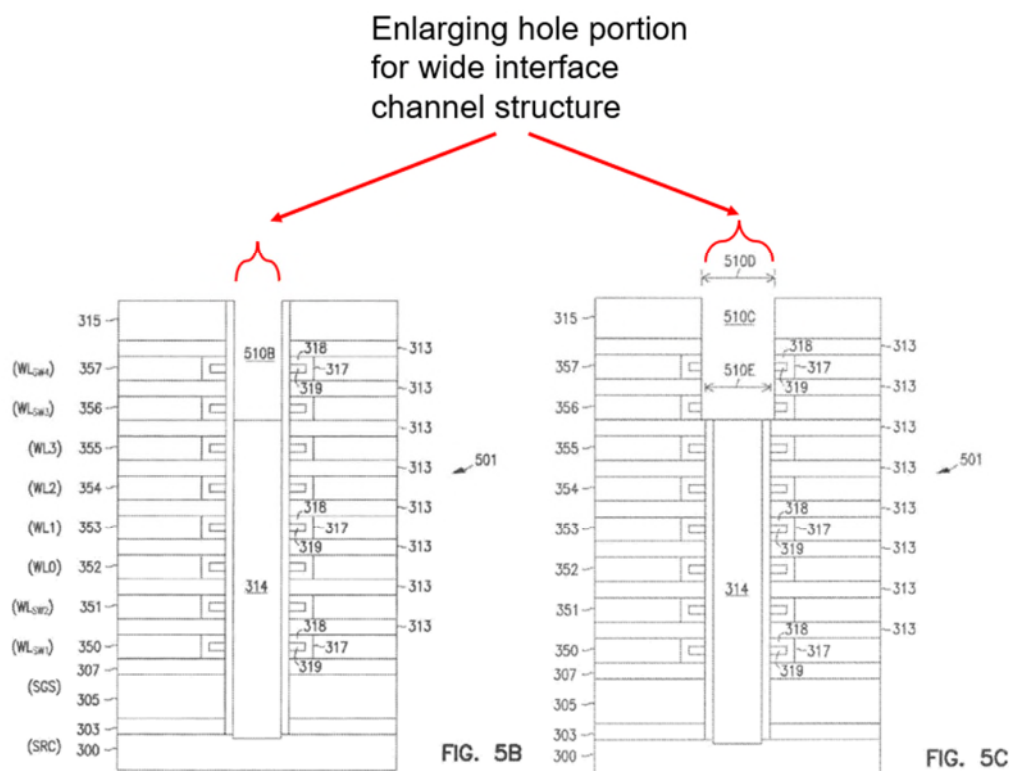
in the fabrication of memory devices. Banerjee, ¶ 160; *see also e.g.*, Ex. 1016, [0023] (“The lateral extension portion (135) may have a larger cross-sectional area than the first and second semiconductor pillars (130a, 130b) based on a cross section parallel to the substrate (105).”), [0086] (“[B]y arranging the lateral extension portion (135) between the first semiconductor pillar (130a) and the second semiconductor pillar (130b), the alignment margin is increased when the second through holes (120b) are formed....”); Ex. 1017, [0058] (“[M]emory opening alignment challenges may be reduced or avoided by adding a landing pad between the memory stack portions [that is] is wider (e.g., had a larger diameter) than the channel in the horizontal direction.”).

Indeed, in this specific context of an interface between channel holes, it was well known to address these alignment and process issues by making the channel interface structure (e.g., third channel structure) wider than the channel hole. For example, Oh discloses:



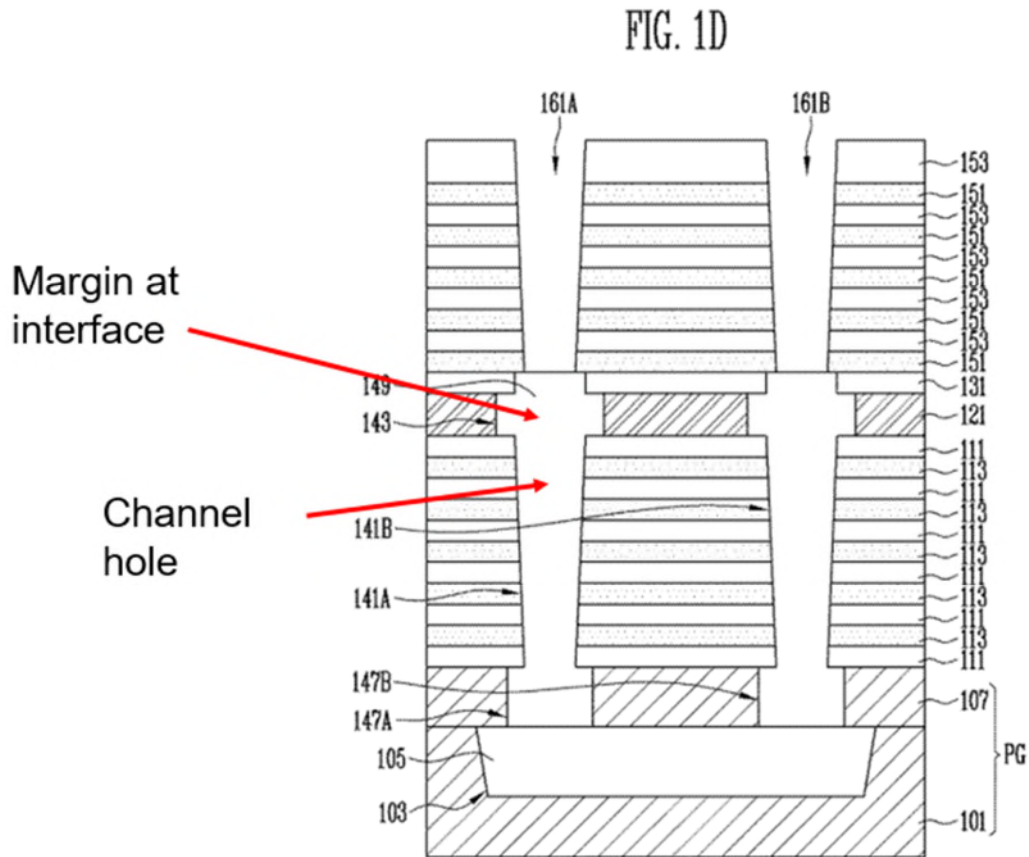
Oh, Figs. 5B, 3A (annotated), [0061] (“[C]hannel connection pattern 180A may have an island shape which overlaps the first channel holes CH1 ... [T]o secure an overlap margin between the channel connection pattern 180A and the first channel hole CH1, the channel connection pattern 180A may have a larger width than the top surface of the first channel hole CH1.”); Banerjee, ¶ 161.

By way of another example, Lu discloses:



Ex. 1018, Fig. 5B, C (annotated), [0118]-[0119] (“Enlarged hole portion 510C can have a diameter 510D that is greater than a diameter 510E (e.g., a diameter of an unenlarged portion of hole 510). The value of diameter 510D can be selected based on an alignment margin for forming a conducting channel in an additional deck (e.g., similar to deck 302 in FIG. 3S) directly over enlarged hole portion 510C.”); Banerjee, ¶ 162.

By way of another example, Yoon discloses employing margin:



Ex. 1007, Fig. 1D (annotated), [0037]-[0038] (“The above-described second through-areas 161A and 161B are formed in a state in which parts of the first through-areas 141A and 141B are widened by the first protrusions 143. According to the first embodiment of the present invention, overlay margins between the second through-areas 161A and 161B and the first through- areas 141A and 141B are enlarged, and thereby the second through-areas 161A and 161B may be easily connected to the first through- areas 141A and 141B.”), Fig. 1E; Banerjee, ¶ 163.

In sum, a POSITA would have understood that the conventional approach to fabricating Costa’s memory device would have added a margin to portion 173 to

make it wider than fill structure 57 to account for process variations and ensure alignment—as shown in Figure 20B of Costa. At the very minimum, this would have been obvious. As demonstrated above, doing so results in the “alignment margin [being] increased” (Ex. 1016, [0086]), i.e., provides an “overlap margin” (Oh [0061]). As a result, “memory opening alignment challenges may be reduced or avoided.” Ex. 1017, [0058]. This enables first and second channels to “be easily connected.” Ex. 1007, [0037]-[0038]. Similarly, it ensures that the interface channel structure and the lower channel are properly connected. *E.g.*, Oh, [0061] (“[C]hannel connection pattern 180A may have an island shape which overlaps the first channel holes CH1 ... [T]o secure an overlap margin between the channel connection pattern 180A and the first channel hole CH1); *see also* Banerjee, ¶ 164. At bottom, providing this margin increases yield, because the margin allows for unaligned structures to still electrically couple. A POSITA would have been highly motivated to consider these similar structures to address the alignment issues of Costa and reap the benefits of increasing alignment margin, providing easy connections, and improving yield. Banerjee, ¶ 165.

A POSITA would have had a high expectation of success in providing this overlap margin. Banerjee, ¶ 166. First, as demonstrated above, providing such a margin was a conventional and basic best practice in semiconductor fabrication. Banerjee, ¶ 167. Second, as the above annotations to Costa’s figures 20A and B

demonstrate, Costa already discloses providing some margin in forming mask 147, and providing additional margin simply involves increasing the width of mask 147 (and less oxidation in the optional oxidation embodiment). *Id.*, ¶ 168. Third, applying a margin actually simplifies the overall fabrication process, because it accounts for misalignment. *Id.* ¶ 169.

Furthermore, to the extent PO argues that Costa fails to meet this limitation because Costa's joint-level doped semiconductor portion 173 is not formed in a groove of the first insulating cap layer 172, PO would be incorrect. First, the claim includes no such requirement. Second, such a requirement would render Claim 7 superfluous. *See* Ex. 1001, Claim 7 (adding additional limitation of "connection layer" and "groove" therein); Banerjee, ¶ 170.

7. [1.F] "forming a second stacked layer over the third channel structure;"

As described by the '532 Patent, "a second stacked layer 15 ... can be ... formed on the third channel structure 14 [and] can include a plurality of oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs." Ex. 1001, 13:7-20, Fig. 12.

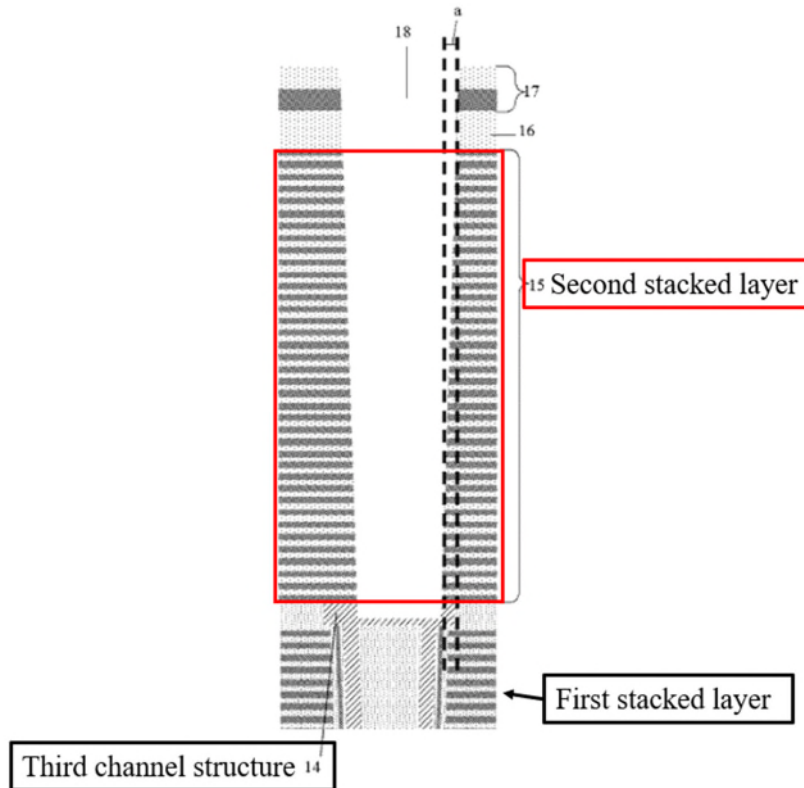
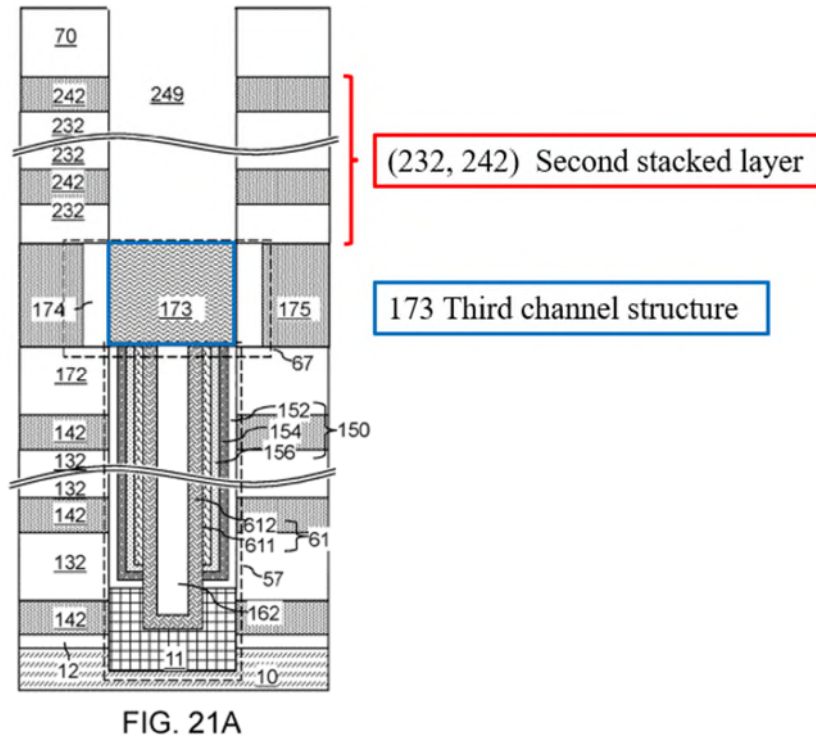


FIG. 13

Id., Fig. 13 (annotated); Banerjee, ¶¶ 172-73.

Costa discloses the same, namely, forming a second stacked layer (“second alternating stack” 232, 242) over the third channel structure (“joint-level doped semiconductor portion 173”). Banerjee, ¶¶ 171, 174. As shown in Figure 21A below, “second alternating stack (232, 242) of material layers is subsequently formed on the top surface of the joint-level material layers....” Costa, [0178] (describing the process of Figs. 8A-B), [0270] (referring to “the processing steps of” Figs. 7A-10B using the third exemplary structure’s single joint-level doped semiconductor portion 173), [0263], Figs. 8A-B, Fig. 21A; Banerjee, ¶ 175. Thus,

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Costa, Fig. 21A (annotated); Banerjee, ¶ 175; *see also* Costa, Fig. 8B.

8. [1.G] “forming a second through hole penetrating the second stacked layer to expose the third channel structure;”

The '532 Patent describes the second through hole similarly to the first through hole: “[A] second through hole 18 is formed [that] can completely penetrate the second stacked layer 15 and the second insulating connection layer 16, and can extend into the surface of the third channel structure 14.” Ex. 1001, 13:33-49.

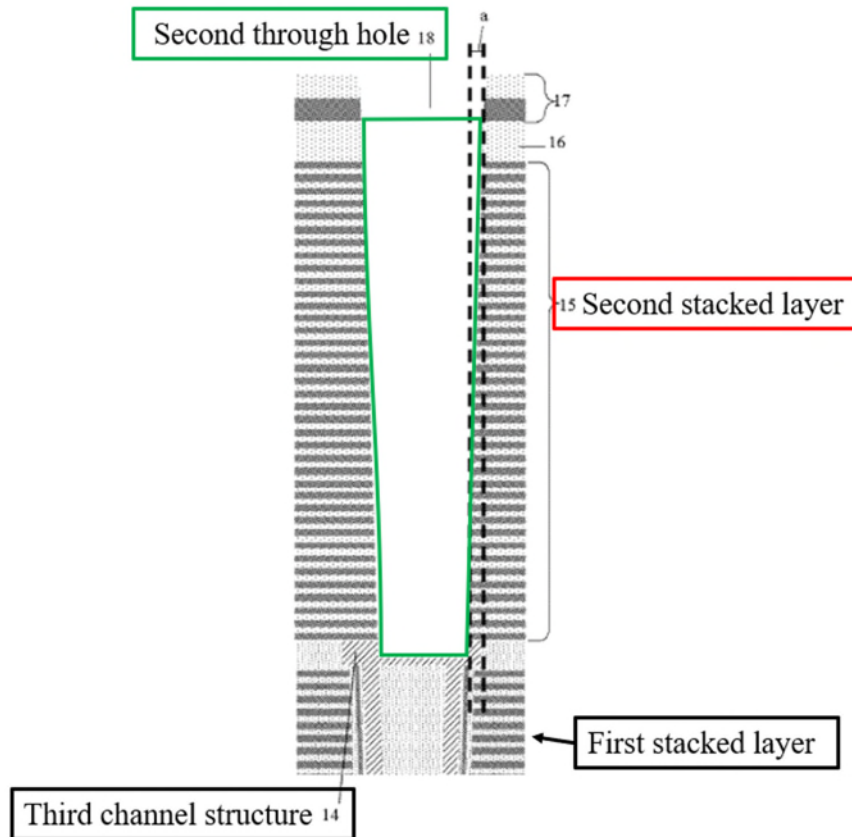


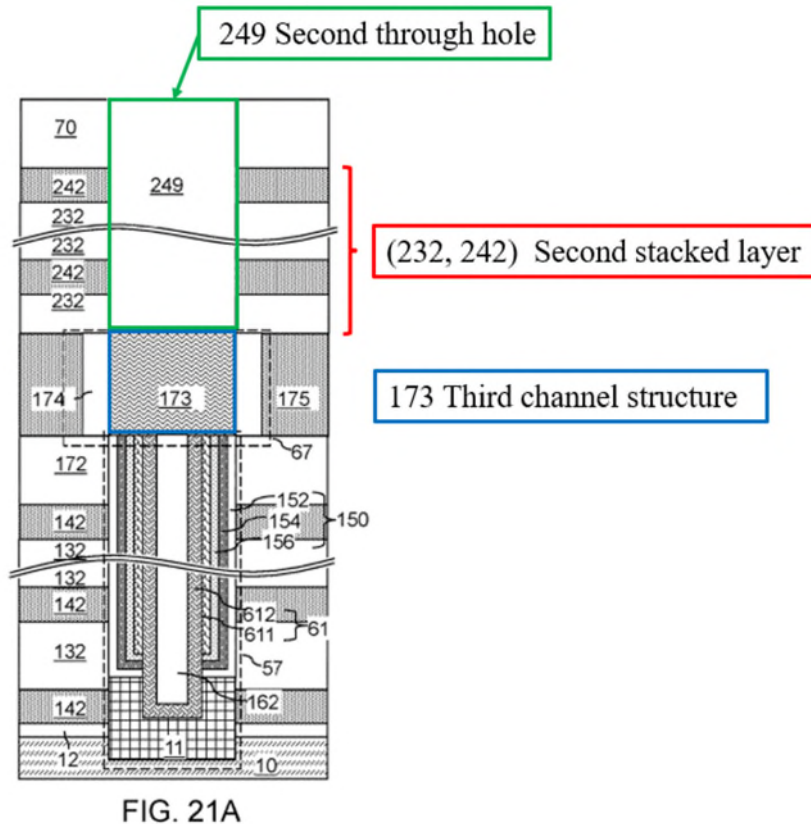
FIG. 13

Id., Fig. 13 (annotated); Banerjee, ¶ 177. The “second through hole” also maps to Figure 13 such that the top of the through hole is at the top of second stack 15, because the claim recites “a second through hole penetrating the second stacked layer to expose the third channel structure.” The analysis under [1.I] addresses each interpretation, and Costa discloses the limitations regardless of how one construes “second through hole.” In other words, the hole may include the portion of the hole that extends through connection layer 16 or exclude that portion. Banerjee, ¶ 178.

Costa discloses the same, namely, forming a second through hole (“second-tier memory opening 249”) that penetrates the second stacked layer (“second

alternating stack” 232, 242) and exposes the third channel structure (“joint-level doped semiconductor portion 173”). Banerjee, ¶¶ 176, 179.

Specifically, after forming the second alternating stack (232, 242), Costa teaches that “second-tier memory opening[] 249 ... are formed” “through the second tier structure (232, 242, 265, 70).” Costa, [0190], [0192] (“second-tier openings (249, 210) can be formed by a combination of lithographic patterning and an anisotropic etch”). As shown in Figure 21A below, second-tier memory opening 249 penetrates the second stacked layer (second alternating stack (232, 242)) and exposes the third channel structure (doped semiconductor portion 173):



Id., Fig. 21A (annotated); Banerjee, ¶ 179. As the analysis under [1.I] demonstrates, Costa’s “second through hole” also maps to the hole that extends from the top of the second stacked layer to the third channel structure, consistent with the claim language requiring a hole “penetrating the second stacked layer.”

9. [1.H] “forming a fourth channel structure in the second through hole and in contact with the third channel structure; and”

The ’532 Patent describes forming a fourth channel structure in the second through hole in much the same manner as the second channel structure, as shown in Figure 19 below. Ex. 1001, 14:39-42, Figs. 16-19. As described by the ’532 Patent, the fourth channel structure can be composed of amorphous silicon. *Id.*, 14:51-53.

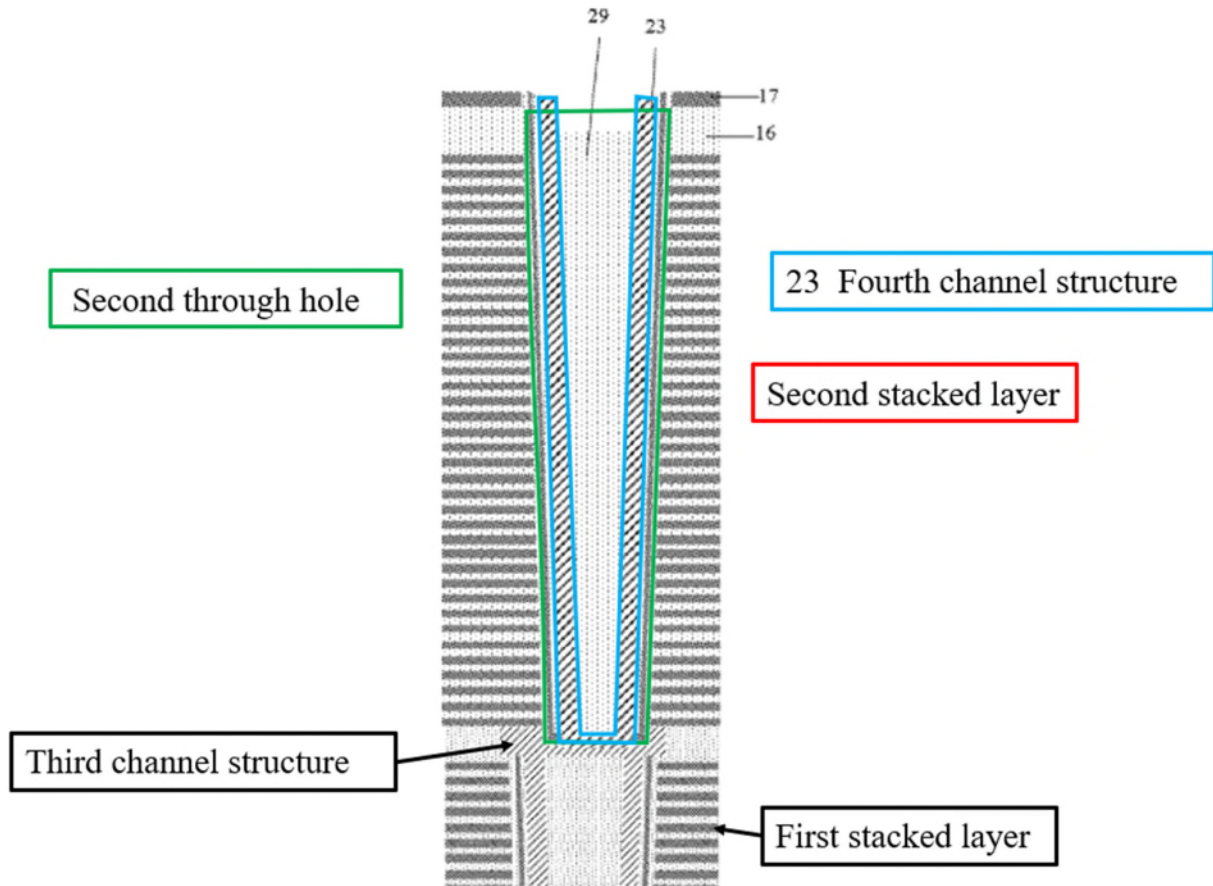
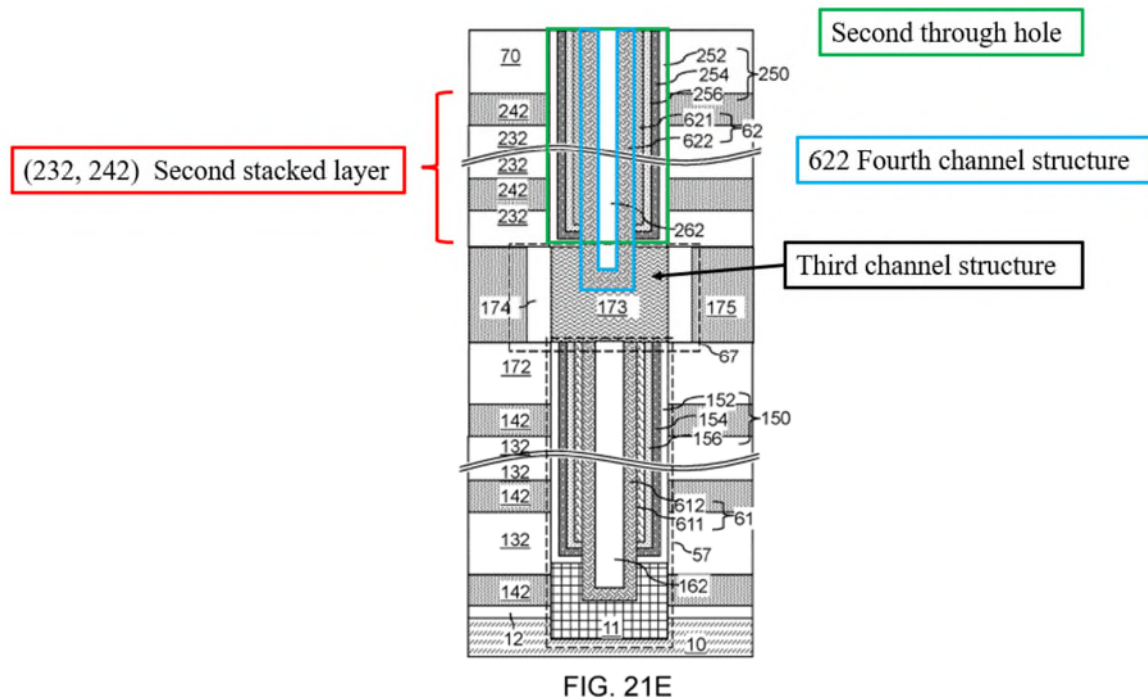


FIG. 19

Id., Fig. 19 (annotated); Banerjee, ¶¶ 181-82.

Costa discloses the same, namely, forming a fourth channel structure (“second inner semiconductor channel layer 622” with or without the optional layer 621) in the second through hole (“second-tier memory opening 249”) and in contact with the third channel structure (“joint-level doped semiconductor portion 173”). Banerjee, ¶¶ 180, 183. Specifically, “a second inner semiconductor channel layer 622 can be deposited directly on the semiconductor surface of the second joint-level doped semiconductor portion 179.” Costa, [0275] (and directly on optional

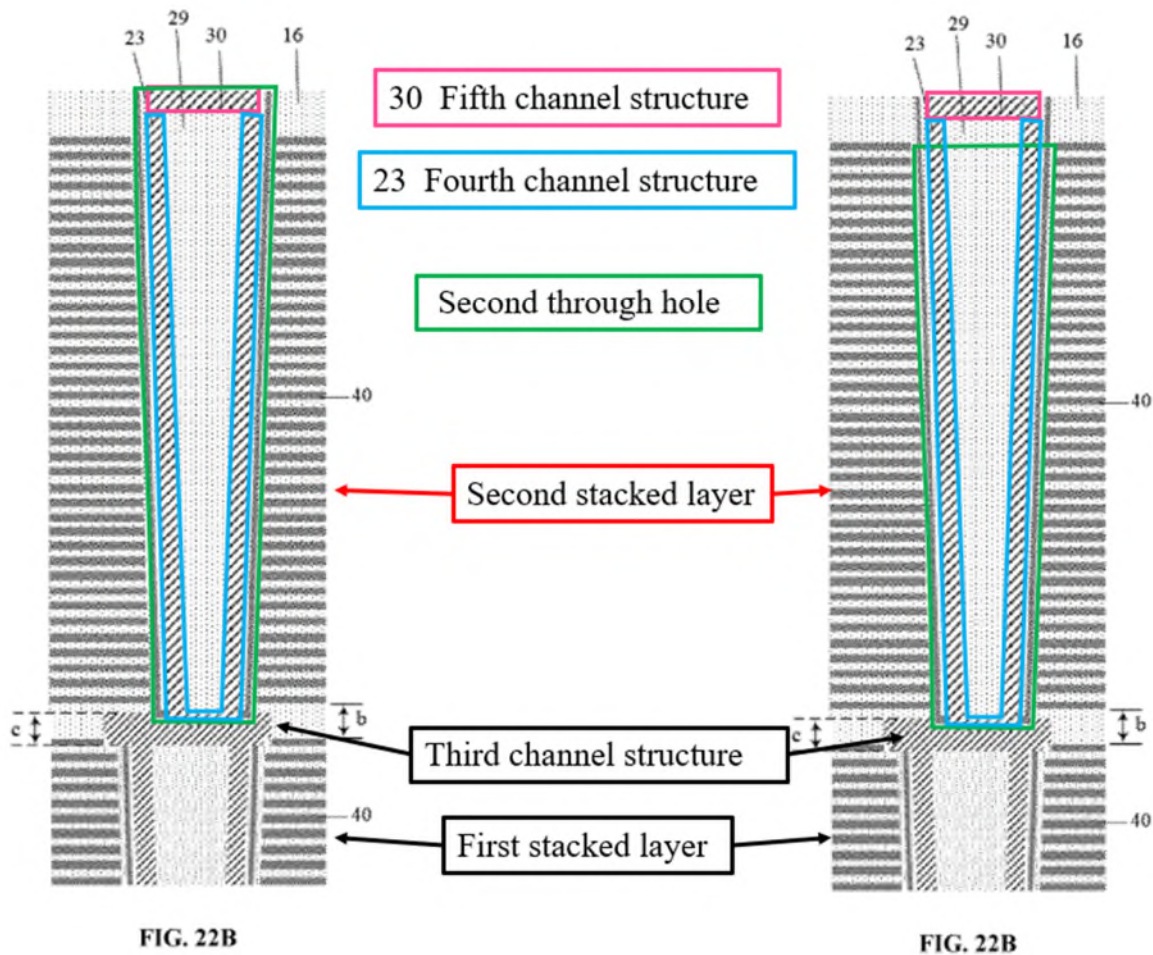
semiconductor channel layer 621). Again, “an optional second outer semiconductor channel layer 621” can be deposited. *Id.*, [0273]. Figure 21D illustrates that second inner semiconductor channel layer 622 can be deposited on the inner surface of the second through hole and in contact with the exposed portion of the first joint-level doped semiconductor portion 173. *Id.*, [0275], Fig. 21D.



Costa, Fig. 21E (annotated); Banerjee, ¶ 184. Like Costa’s second channel structures, layers 621 and 622 may be “amorphous silicon or polysilicon,” and thus function as a channel. Costa, [0202], [0207], Banerjee, ¶ 184. As the analysis under [1.I] demonstrates, Costa’s “second through hole” also maps to the hole that extends from the top of the second stacked layer to the third channel structure, consistent with the claim language requiring a hole “penetrating the second stacked layer.”

10. [1.I] “forming a fifth channel structure above the second through hole and in contact with the fourth channel structure.”

As described by the '532 Patent, the fifth channel structure is formed in a manner similar to that of the third channel structure (described above). “[A] second groove can be formed on the fourth channel structure and the second filling structure, and in the second through hole 18.” Ex. 1001, 15:7-9. The “fifth channel structure can be formed in the second groove” and “the top surface of the second insulating connection layer 16 and the top surface of the fifth channel structure 30 can be planarized by any suitable techniques....” *Id.*, 15:19-31. As [1.G] explains, the “second through hole” maps to two different hole sizes.



Id., Fig. 22B (annotated); Banerjee, ¶ 186.

Regardless of the mapping of “second through hole,” Costa discloses the same, namely, forming a fifth channel structure (“drain region 63”) above the second through hole (“second-tier memory opening 249”) and in contact with the fourth channel structure (“second inner semiconductor channel layer 622”). Costa, [0277]; Banerjee, ¶¶ 185, 187.

“The Second Through Hole” Extending Through the Connection Layer

As shown in Figure 21F below, drain region 63 can be formed in a recess etched into second dielectric core 262 below the top surface of insulating cap layer 70:

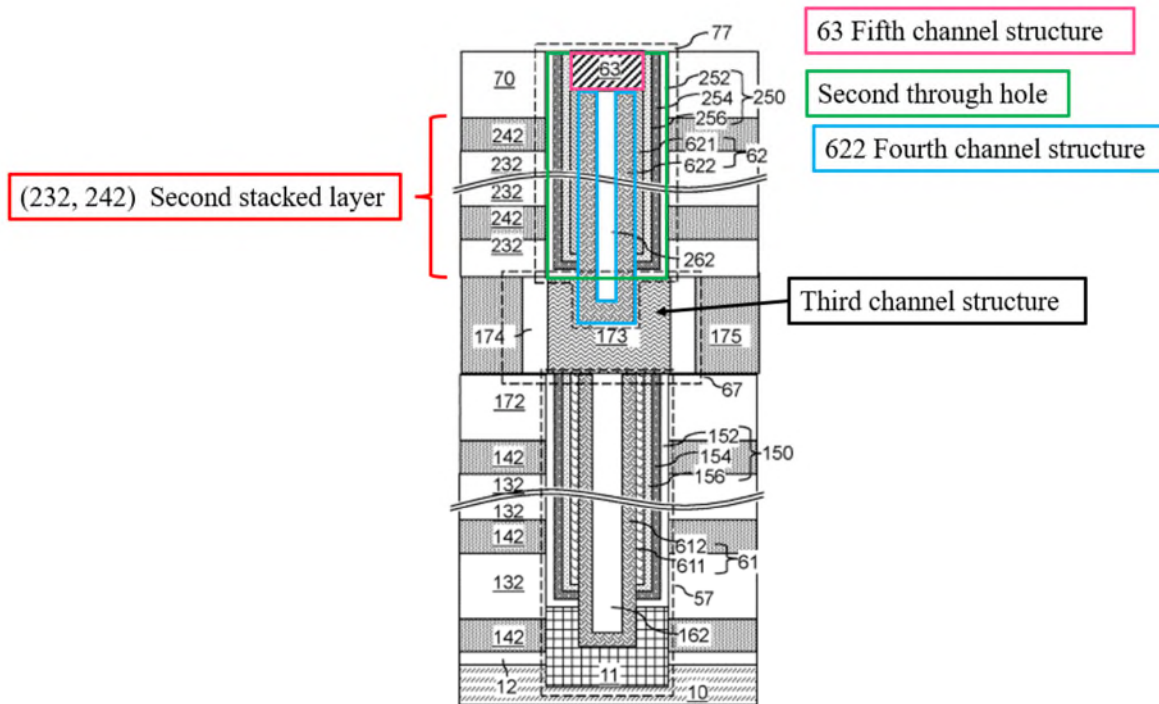


FIG. 21F

Costa, Fig. 21F (annotated), [0277]; Banerjee, ¶ 188. Drain region 63 is in contact with second inner semiconductor channel layer 622 (and optional layer 621). Costa, Fig. 21F; Banerjee, ¶ 189.

Costa’s drain regions are formed “above the second through hole.” Specifically, Costa’s full hole starts at the top of insulating layer 70. Banerjee, ¶ 190; *see also* §X.A.8. Costa describes forming drain regions in more detail with respect to the first embodiment, which Costa specifically references in the third embodiment

regarding the conductive drains. Costa, [0277]. As Costa describes, forming conductive regions first involves etching the groove for the conductive drain and then depositing polysilicon for the drain. *Id.*, [0212]. Next, Costa discloses: “[e]xcess portions of the deposited semiconductor material can be removed from above the top surface of the insulating cap layer 70, for example, by chemical mechanical planarization (CMP) or a recess etch to form the drain regions 63.” *Id.* In other words, the conductive drain (“fifth channel structure”) is initially above the Costa hole that extends through the connection layer, and CMP planarizes the plug to the same height as the connection layer. Banerjee, ¶ 191.

To the extent PO argues that Costa’s drain region 63 is not “form[ed] ... above the second through hole” (second-tier memory opening 249) because after drain region 63 is formed, drain region 63 is in “the second through hole” and not “above” (Costa’s hole 249), PO would be incorrect for several reasons. Banerjee, ¶ 192.

First, Costa describes forming drain region 63 in exactly the same manner as the fifth channel structure in the ’532 Patent, i.e., the “fifth channel structure” is not completely “above” the “second through hole” after fabrication of the memory has been completed unless the “second through hole” is defined to be only the part of the hole that extends through the stack (and not the portion that extends through the connection layer). As to the ’532 Patent, the top of the “second through hole” is at

the top of layer 16 (excluding the mask layer 17 given that mask is temporary), i.e., it also extends through the connection layer:

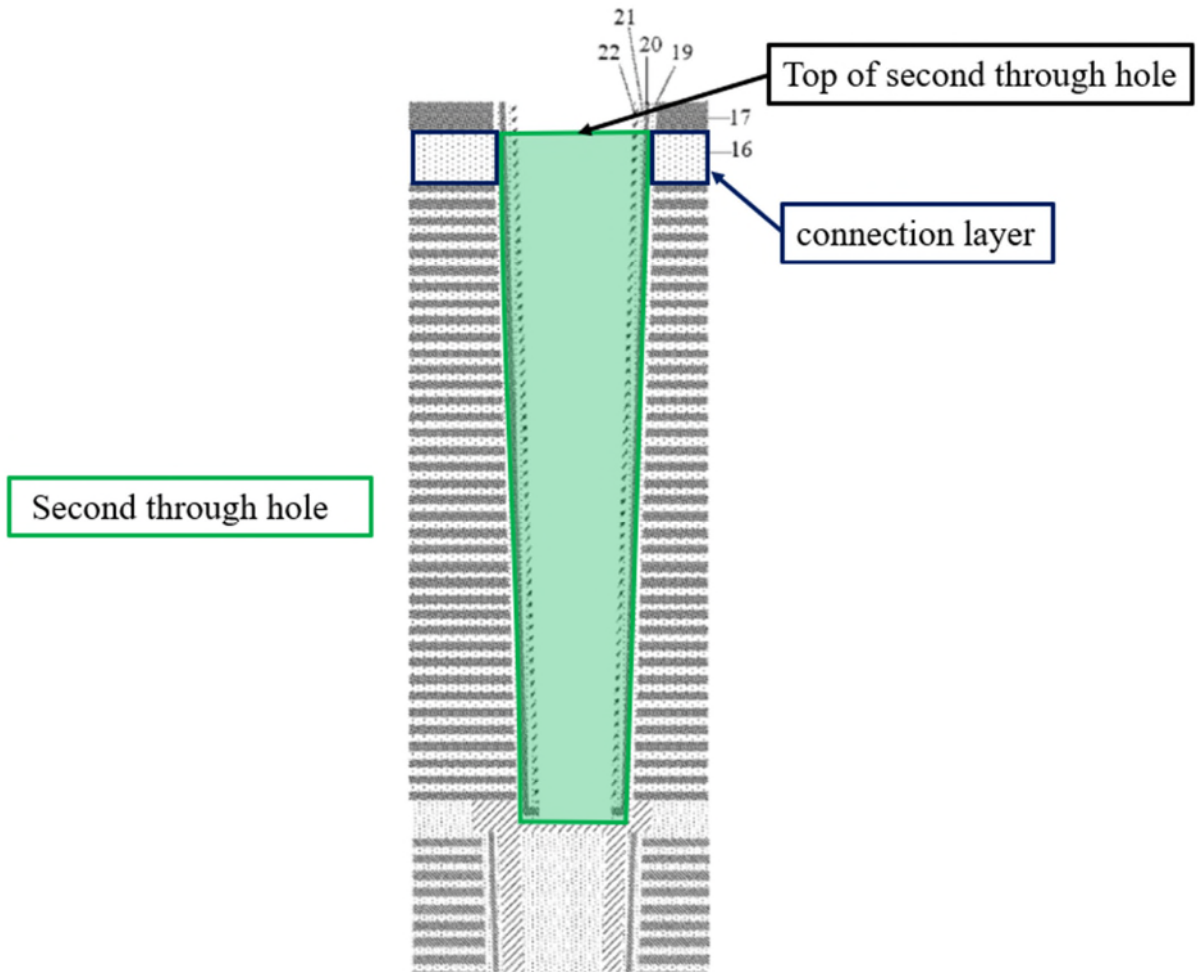
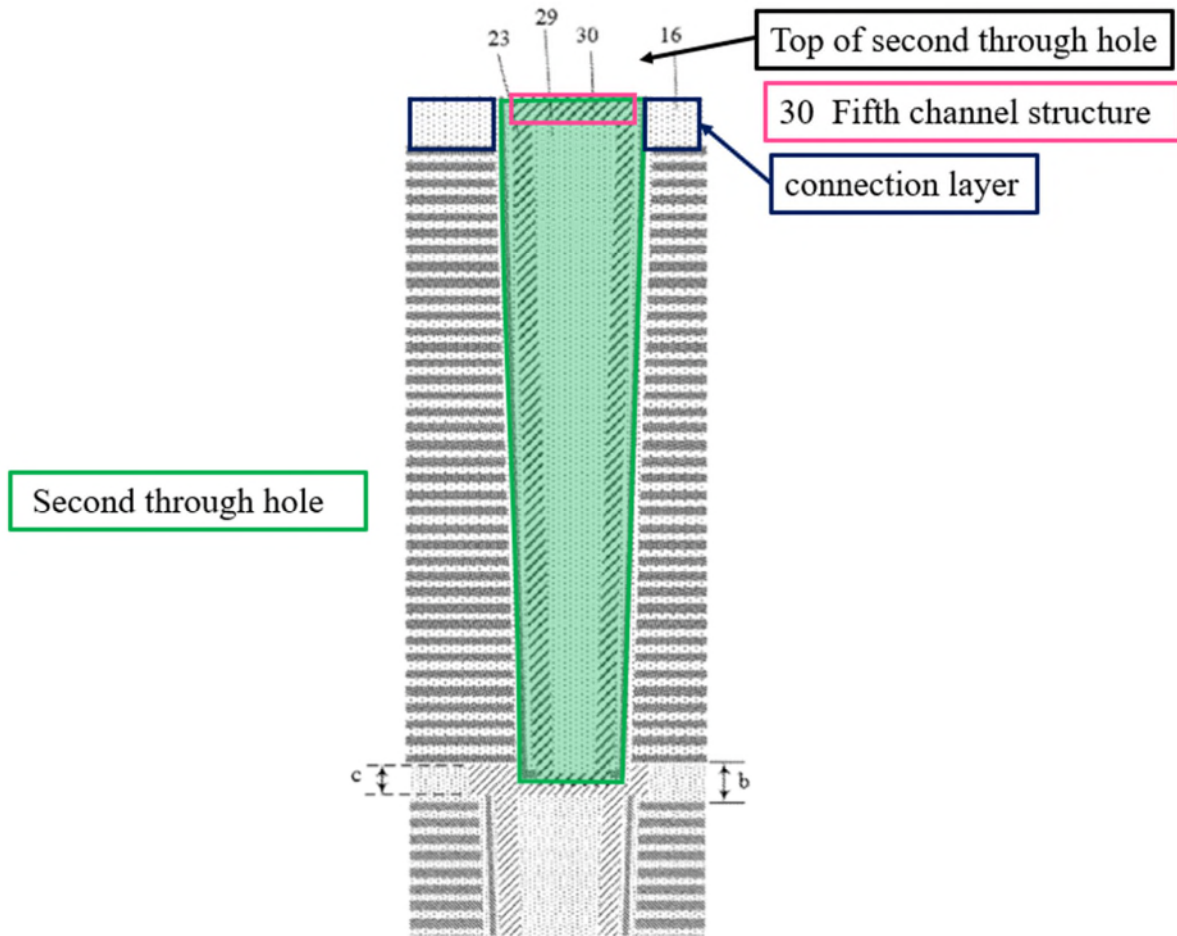


FIG. 15

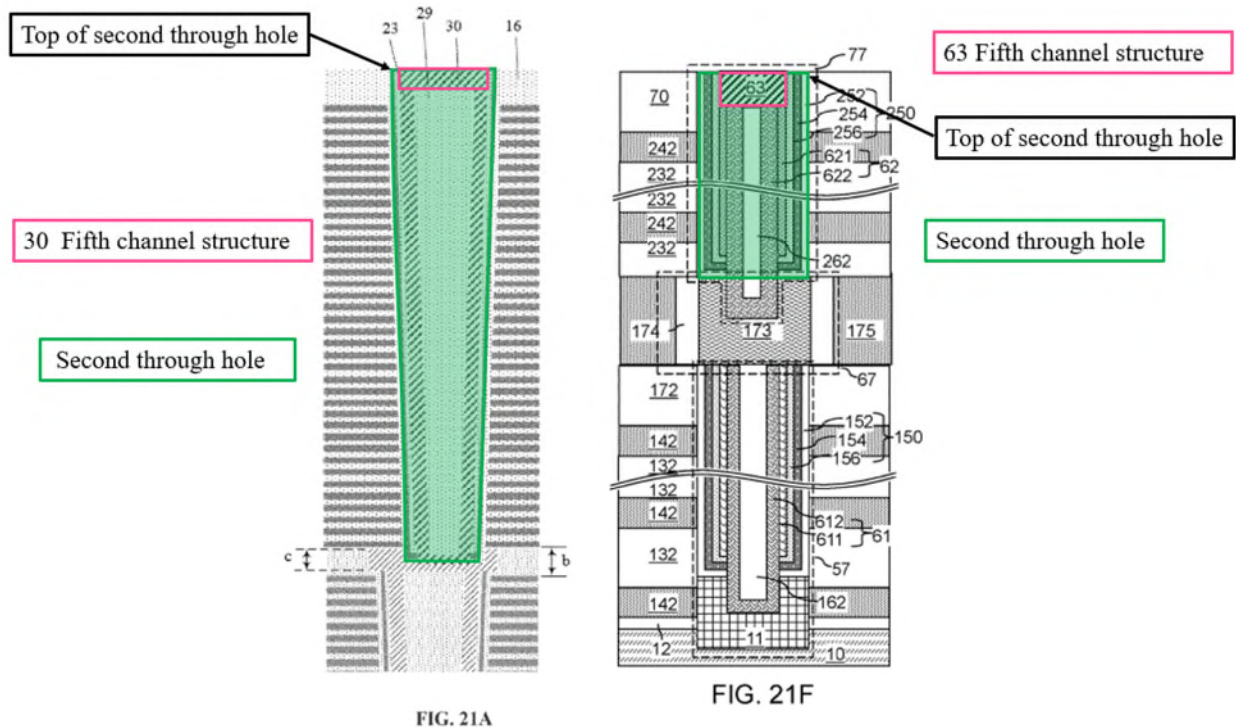
Ex. 1001, Fig. 15 (annotated); Banerjee, ¶ 193.

After fabrication, however, the fifth channel structure is not above layer 16, but sits flush with layer 16 because of the CMP process:



Ex. 1001, Fig. 21A (annotated), 15:27-31 (CMP to make flush with layer 16); Banerjee, ¶ 194.

As demonstrated above, after fabrication, Costa's fifth channel structure sits within the original hole through the connection layer with the top of the fifth structure being at the same level as the top of the original hole, whereas the fifth channel structure of the '532 patent has the same orientation.



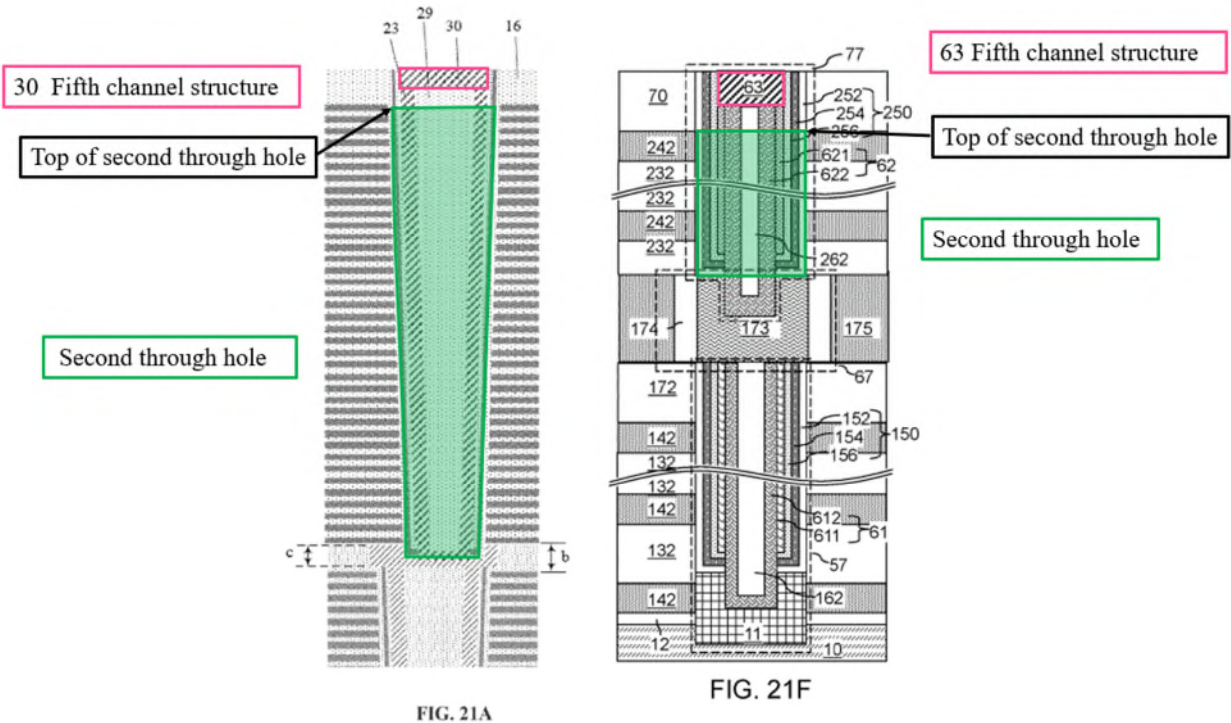
Ex.1001, Fig. 21A (left, annotated); Costa, Fig. 21F (right, annotated); Banerjee, ¶ 195.

Finally, independent claim 1 recites a method, not an apparatus. Thus, any argument by PO that Costa’s drain region 63 is not “above” the second-tier memory opening 249 in its finished configuration is irrelevant. This limitation requires nothing more than that the fifth channel structure be “form[ed] ... above the second through hole.” Based on the plain language, Costa meets this limitation, because its deposition of the fifth channel structure requires CMP to reduce its height to be commensurate with the top of the original hole. Costa, [0212], [0277]. Moreover, independent claims 11 and 18 (directed to “[a] joint opening structure of a three-dimensional (3D) memory device”) recite “a fifth channel structure ... ***disposed over***

the second through hole,” Ex. 1001, cls. 11, 18, **not** “a fifth channel structure ... ***disposed above*** the second through hole.” Nor does the specification describe any such configuration—each embodiment describes a fifth channel structure just like that of Figure 22B (see above)—that is, a fifth channel structure located at the top of the second through hole, its top surface planarized with the top surface of the second insulating connection layer. *E.g., id.*, 15:19-31, 24:18-31, 31:66-32:9, 40:38-51, Figs. 21A-B, 22A-B, 23B, 48A-B, 49A-B, 50B, 72A-B, 73A-B, 74B, 101A-B, 102A-B, 103B; Banerjee, ¶ 196-197. Claims 11 and 18, and the embodiments described in the specification, make clear that what is claimed is not a fifth channel structure that is “above” the second through hole in its final configuration. Rather, what is claimed is a fifth channel structure that is “form[ed] ... above the second through hole” and is “disposed above the second through hole in its final configuration. *Id.*, ¶ 197.

“The Second Through Hole” Extending Only Through the Stack

Alternatively, if one were to define the “second through hole” as being only the hole that extends from the top of the second stacked layer to the bottom of that layer (consistent with the claim language “a second through hole penetrating the second stacked layer”), then both the ’532 Patent and Costa disclose the fifth channel structure being above the shorter hole:



Ex. 1001, Fig. 21A (left, annotated); Costa, Fig. 21F (right, annotated); Banerjee, ¶ 198.

B. Claim 2:

1. [2.PRE] “The method of claim 1, wherein:” [2.A] “the first stacked layer includes a first number of oxide/nitride layer pairs; and” [2.B] “the second stacked layer includes a second number of oxide/nitride layer pairs.”

Costa discloses these limitations.

Costa teaches that “[t]he number of repetitions of the pairs of a first insulating layer 132 and a first sacrificial material layer 142 can be in a range from 2 to 1,024, and typically from 8 to 256.” Costa, [0133]. And the same is true of the second alternating stack. *Id.*, [0182]. And as discussed in [1.A] and [1.F], these stacked layers can be comprised of oxide/nitride layer pairs. Banerjee, ¶¶ 201-02.

To the extent PO argues that Costa fails to disclose this limitation by arguing that the “first number” and “second number” must be different, PO would be incorrect. Nothing in the ’532 Patent’s claims or specification would require such an interpretation. To the contrary, in the specification, “first” and “second” just denote different physical stacks. *See* Ex. 1001, cl. 2, 43:10-13 (“[T]he words ‘first’, ‘second’ and the like used in this disclosure do not denote any order, quantity or importance, but are merely intended to distinguish between different constituents.”); Banerjee, ¶¶ 203-04.

C. Claim 3:

1. **[3.PRE] “The method of claim 2, wherein:” [3.A] “the first number and the second number are not less than 32.”**

The analysis in [2] demonstrates that Costa discloses this limitation.

D. Claim 11:

1. **[11.PRE] “A joint opening structure of a three-dimensional (3D) memory device, comprising:”**

This limitation is substantively identical to [1.PRE] and Costa discloses it for the same reasons (claim 1 recites a method for forming the same).

2. **[11.A] “a first through hole penetrating a first stacked layer along a vertical direction;”**

This limitation is substantively identical to [1.B], and is present in [1.A], and Costa discloses it for the same reasons.

3. **[11.B] “a first channel structure disposed at the bottom of the first through hole;”**

This limitation is present in [1.C] and Costa discloses it for the same reasons.

4. **[11.C] “a second channel structure in contact with the first channel structure disposed in the first through hole;”**

This limitation is substantively identical to [1.D] and Costa discloses it for the same reasons.

5. **[11.D] “a third channel structure in contact with the second channel structure disposed over the first through hole, wherein a size of the third channel structure along a lateral direction is larger than a top aperture of the first through hole;”**

This limitation is substantively the same as [1.E] (but recites “disposed over” instead of “form[ed] ... above”) and Costa renders it obvious for the same reasons. Banerjee, ¶ 212.

6. **[11.E] “a second stacked layer disposed on the third channel structure;”**

This limitation is substantively identical to [1.F] and Costa discloses it for the same reasons.

7. **[11.F] “a second through hole penetrating the second stacked layer along the vertical direction;”**

This limitation is substantively the same as [1.G] and Costa discloses it for the same reasons.

8. [11.G] “a fourth channel structure in contact with the third channel structure disposed in the second through hole;”

This limitation is substantively identical to [1.H] and Costa discloses it for the same reasons.

9. [11.H] “a fifth channel structure in contact with the fourth channel structure disposed over the second through hole.”

This limitation is substantively the same as [1.I] (but recites “disposed over” instead of “form[ed] ... above”) and Costa discloses it, or renders it obvious, for the same reasons. Banerjee, ¶ 216.

E. Claim 13:

1. [13.PRE] “The joint opening structure of claim 11, further comprising:” [13.A] “a first filling structure covering the surface of the second channel structure; and”

The '532 Patent describes the claimed first filling structure in conjunction with the second channel structure discussed in [1.D]. Specifically, “a first filling layer 12 can be formed to cover the second channel layer 11 and fill the first through hole 5.” Ex. 1001, 11:35-37, Fig. 6. A subsequent etching process removes “a portion of the first filling layer 12” such that “the remaining portion of the first filling layer 12 in the first through hole 5 can form the first filling structure” as shown in Figure 10B below. *Id.*, 11:41-51, Figs. 7A-B. As described by the '532 Patent, the first filling layer can be an oxide layer. *Id.*, 19:40-42. Put simply, the filling structure is, e.g., the core of the channel structure. Banerjee, ¶ 219.

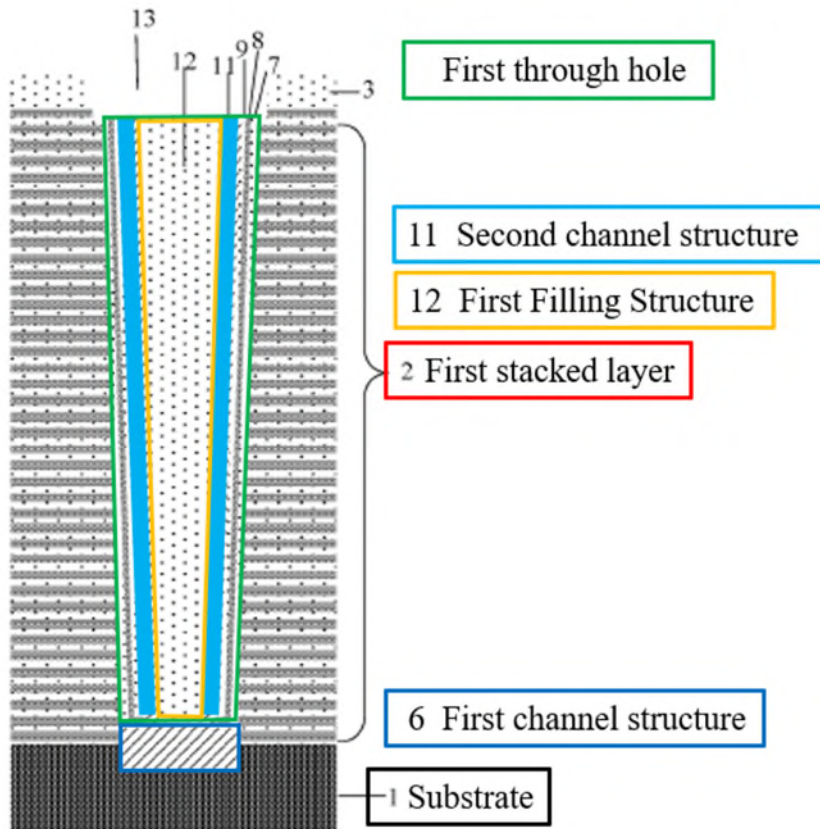


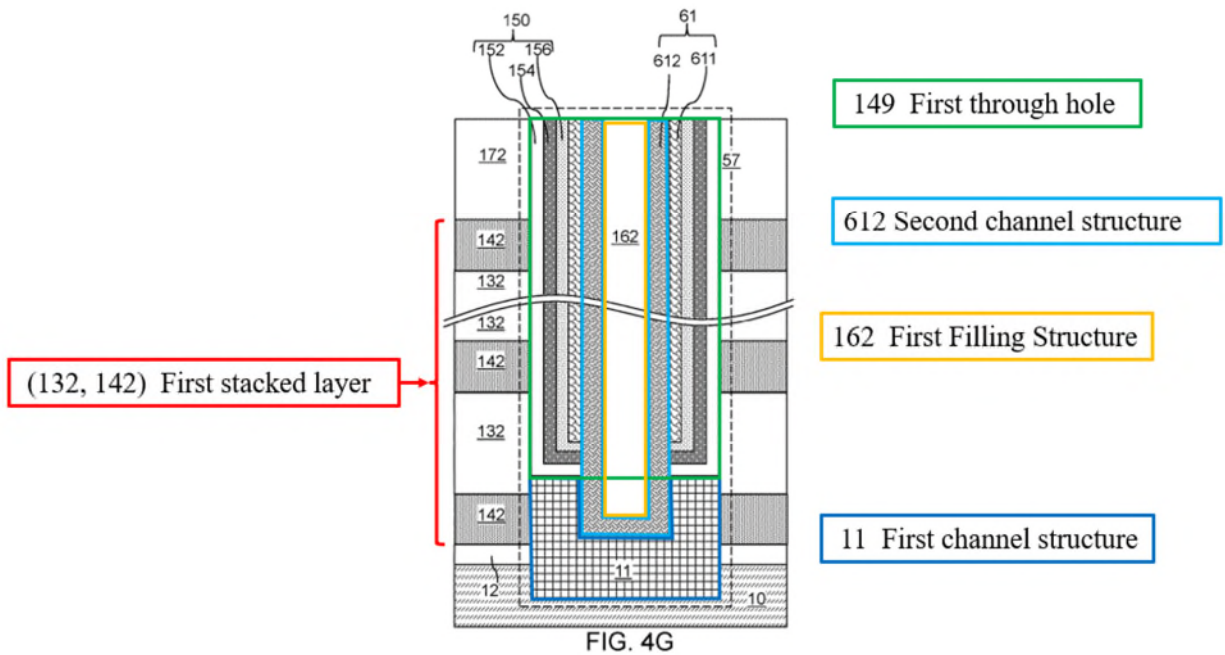
FIG. 10B

Ex. 1001, Fig. 10B (annotated); Banerjee, ¶ 220.

As demonstrated below, Costa discloses the same, namely, a first filling structure (“dielectric core 162”) that covers the surface of the second channel structure (“inner semiconductor channel layer 612”). The “outer semiconductor channel layer 611,” shown below, is optional. Costa, [0144]. Banerjee, ¶¶ 218, 221.

Costa discloses not completely filling the cavity with semiconductor channel material. Costa, [0158], Fig. 4F. In such cases, Costa discloses forming a “dielectric core layer 162L.” *Id.*, [0158], Fig. 4F; *see also id.*, [0159], Fig. 4G (removing portion of “first dielectric core layer 162L” that is “above the top surface of the first-

tier insulating cap layer 172” and leaving “dielectric core 162” within the memory cavity 149’); Banerjee, ¶ 221. Moreover, Costa’s dielectric core covers the surface of the second channel structure (“inner semiconductor channel layer 612”) as is apparent from the Figure below:



Costa, Fig. 4G (annotated); Banerjee, ¶ 222.

To the extent Patent Owner argues that Costa fails to meet this limitation because dielectric core 162 fails to “cover the surface of the second channel structure,” Patent Owner would be incorrect. A POSITA would have understood that Costa’s dielectric core 162 “cover[s] the surface of” inner semiconductor channel layer 612 given the ’532 Patent’s use of “cover.” The ’532 Patent’s specification uses the term “completely covering” and “completely cover” when total coverage is described, whereas Claim 13 simply recites “covering.” *E.g.*, Ex.

1001, Fig. 23A (“the projection of the first groove on the substrate completely covering the projection of the first through hole on the substrate”), 12:21-23 (“In some embodiments, the projection of the first groove on the substrate 1 can completely cover the projection of the first through hole 5 on the substrate 1.”). Thus, a POSITA would not read “covering” to mean “completely covering,” e.g., covering the entirety of the underlying object. Banerjee, ¶¶ 223-24. Moreover, as Figure 4G above demonstrates, dielectric core 162 is in direct contact with each inner surface (relative to the channel hole) of inner semiconductor channel layer 612. Costa, Fig. 4G. Thus, dielectric core 162 is “covering the surface of” inner semiconductor channel layer 612. *Id.*; Banerjee, ¶ 225.

2. [13.B] “a second filling structure covering the surface of the fourth channel structure;”

The ’532 Patent describes the claimed second filling structure in conjunction with the fourth channel structure discussed in [1.H]. Specifically, “a second filling layer 29 can be formed to cover the fourth channel layer 23 and to fill the second through hole 18.” Ex. 1001, 14:54-56, Fig. 17. A subsequent etching process removes “a portion of the second filling layer 29” such that “[t]he remaining portions of the second filling layer 29 in the second through hole 18 can form the second filling structure.” *Id.*, 14:63-65, Fig. 18. As described by the ’532 Patent, the second filling structure can be an oxide layer. *Id.*, 14:56-58. Just like the first filling structure, the second filling structure is, e.g., the core of the channel structure.

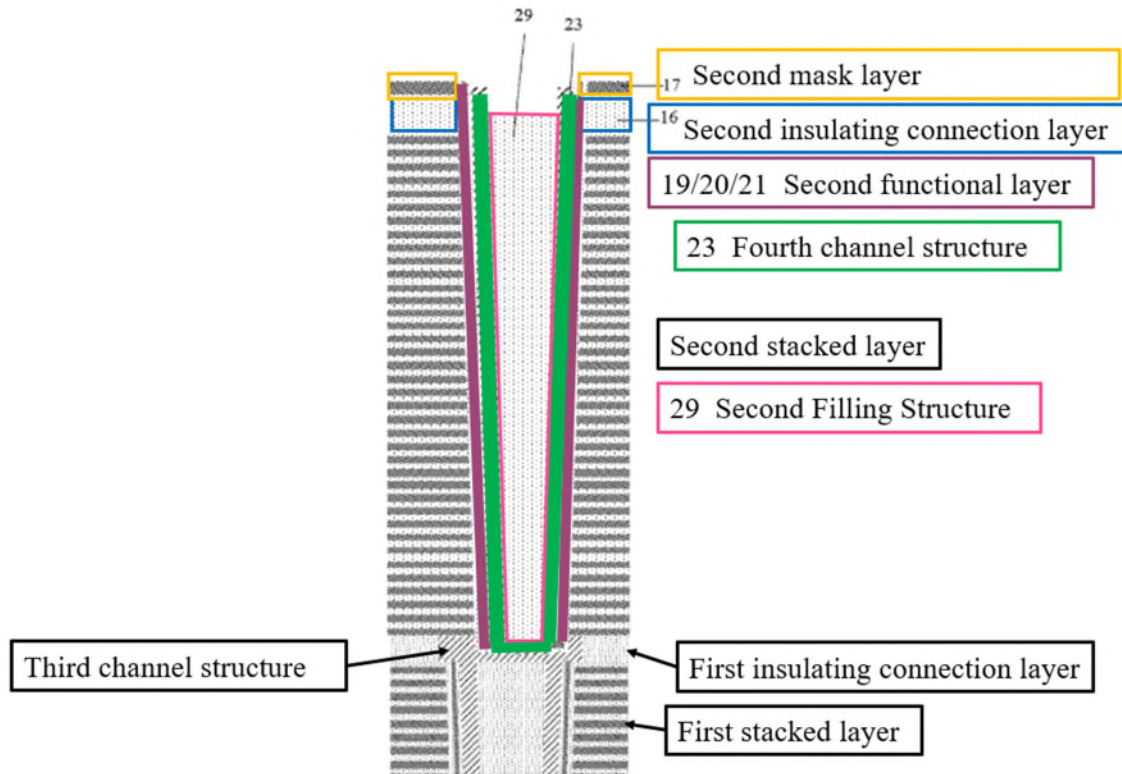
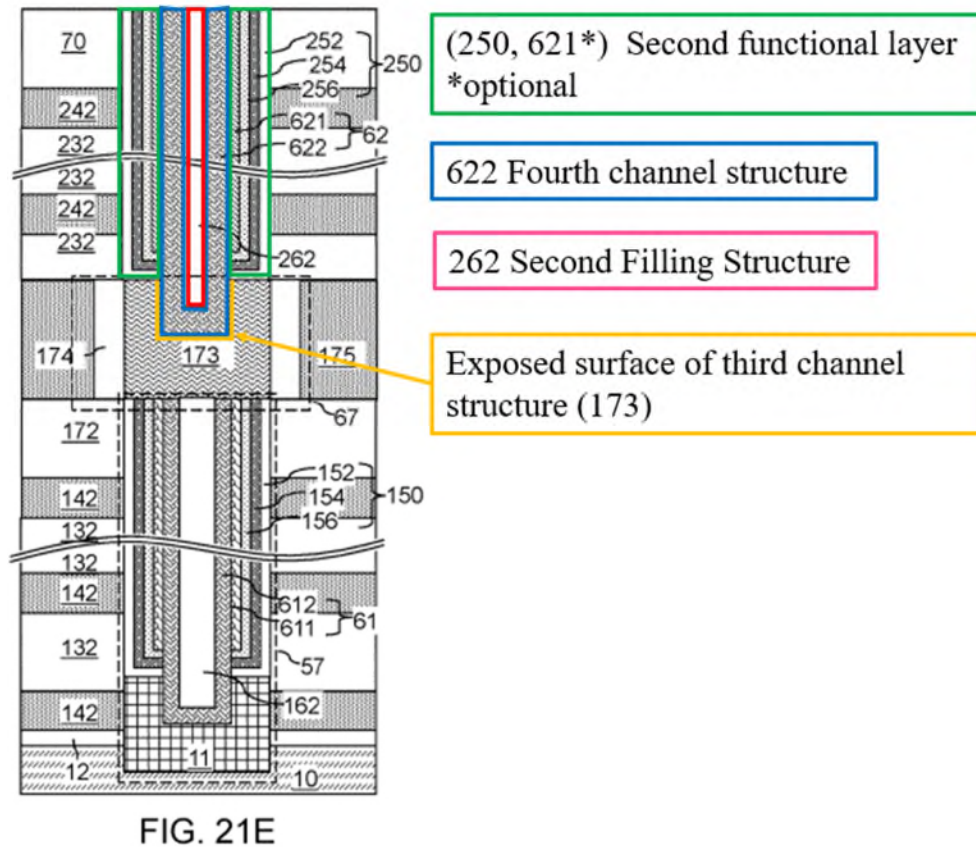


FIG. 19

Id., Fig. 19 (annotated); Banerjee, ¶ 227.

As demonstrated below, Costa discloses the same, namely, a second filling structure (“dielectric core 262”) that covers the surface of the second channel structure (“inner semiconductor channel layer 622”). Banerjee, ¶¶ 226, 228. The “outer semiconductor channel layer 621,” shown below, is optional. Costa, [0196]. Costa discloses that a “second dielectric core layer 262L” may be deposited as a core. *Id.*, [0275], Fig. 21D. A subsequent etching process removes “the horizontal portion of the second dielectric core layer 262L,” leaving second dielectric core 262 within the second memory cavity 249’. *Id.*, [0276].



Id., Fig. 21E (annotated); Banerjee, ¶ 229.

To the extent Patent Owner argues that Costa fails to meet this limitation because dielectric core 262 does not “cover the surface of the fourth channel structure,” Patent Owner would be incorrect for the same reasons discussed above in [13.A] with respect to dielectric core 162. Banerjee, ¶ 230.

3. [13.C] “wherein the first through hole is non-interconnected with the second through hole.”

Costa discloses this limitation.

For example, when forming second-tier memory openings 249, Costa teaches that “second-tier memory openings 249 are formed through the second tier structure

(232, 242, 70, 265) in areas that overlap with the joint-level memory opening fill structures 67, i.e., with the joint-level memory openings.” Costa, [0191]; Figs. 10A-10B, 21A; *see also id.*, [0272] (“FIG. 21A illustrate a region of the second exemplary structure at the processing steps of FIGS. 10A and 10B, i.e., after formation of the second-tier memory openings 249...”). As illustrated in Fig. 21F, a POSITA would have understood that Costa discloses that first-tier memory openings (filled in Fig. 21G with first memory opening fill structures 57) are non-interconnected with second-tier memory openings 249 (filled in Fig. 21G with second memory opening fill structures 77) because joint-level doped semiconductor portions 173 are interposed between the first-tier and second-tier memory openings:

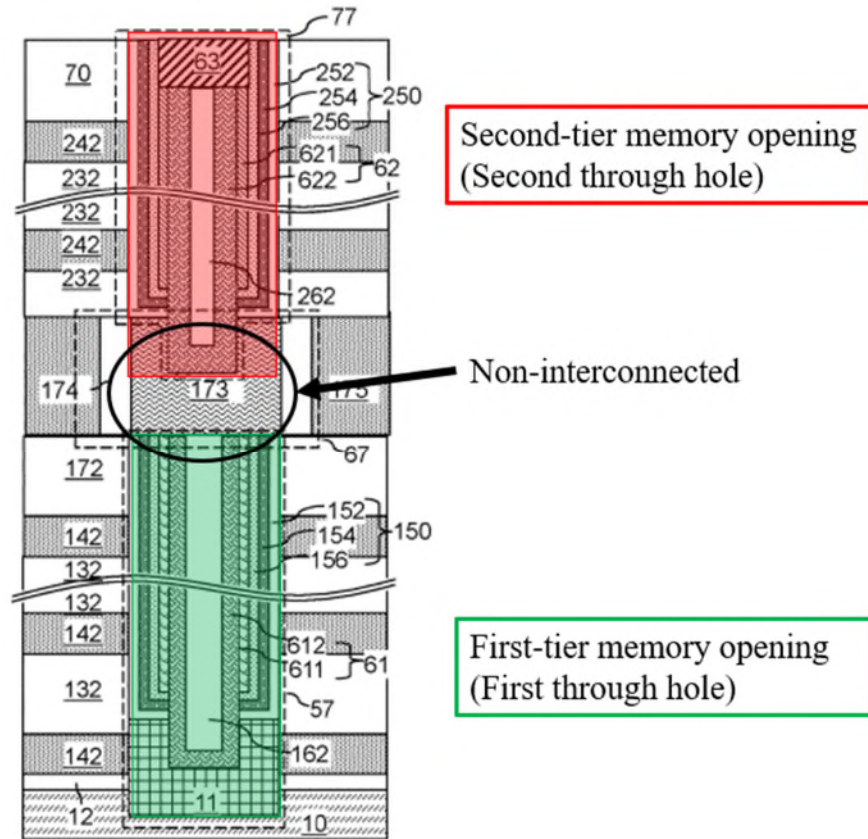


FIG. 21F

Id., Fig. 21F (annotated); Banerjee, ¶¶ 232-34.

F. Claim 15:

1. [15.PRE] “The joint opening structure of claim 11, wherein:” [15.A] “the first stacked layer includes a first number of conductor/dielectric layer pairs;” [15.B] “the second stacked layer includes a second number of conductor/dielectric layer pairs; and”

These limitations are identical to [2.A -2.B] and met for the same reasons.

2. [15.C] “the first number and the second number are not less than 32.”

This limitation is identical to [3] and met for the same reasons.

G. Claim 16:

1. **[16.PRE] “The joint opening structure of claim 11, wherein:” [16.A] “a thickness of the third channel structure is in a range between 30 nm and 70 nm.”**

Costa discloses this limitation.

Specifically, Costa discloses that “[t]he thickness of the first joint-level doped semiconductor layer 173L can be in a range from 20 nm to 100 nm, although lesser and greater thicknesses can also be employed.” Costa, [0163]. Thus, Costa discloses the full range of claim 18. Costa’s range accounts for the fact that Costa discloses the elements of stacks also have ranges, and the ranges simply reflect that depending on process generation that is employed to fabricate the device, different feature sizes are available. *E.g., id.*, [0139], [0146]-[0147], [0150], [0182]; Banerjee, ¶¶ 240-41. The ’532 Patent similarly discloses ranges for various layers. *E.g.*, Ex. 1001, 9:35-41; Banerjee, ¶ 242.

H. Claim 17:

1. **[17.PRE] “The joint opening structure of claim 11, wherein:” [17.A] “a size difference between the top aperture and a bottom aperture of the first through hole is equal to or less than 30 nm; and”**

Costa discloses this limitation.

Costa discloses that “[t]he lateral dimensions (e.g., a diameter) of the first-tier openings (149, 119) can be from about 20 nm to 200 nm at an upper portion of each first-tier opening (149, 119), and can be about 10 nm to 150 nm at a lower portion

of each first-tier opening (149, 119).” Costa, [0139]; Banerjee, ¶¶ 245-46. Thus, a POSITA would have understood that a size difference between the top and bottom “aperture” of first-tier memory opening 149 can be less than or equal to 30 nm, e.g., taking the two lower ranges, the size difference in Costa would be 10nm. *Id.*, ¶¶ 247-49 (explaining that tapering creates this difference).

2. **[17.B] “a size difference between a top aperture and a bottom aperture of the second through hole is equal to or less than 30 nm.”**

Costa discloses this limitation.

Costa teaches the same difference for the second through hole. Costa, [0194]. Thus, a POSITA would have understood that a size difference between the top and bottom “aperture” of second-tier memory opening 249 can be less than or equal to 30 nm, e.g., taking the two lower ranges, the size difference in Costa would be 10nm. Banerjee, ¶¶ 251-52.

I. Claim 18:

1. **[18.PRE] “A joint opening structure of a three-dimensional (3D) memory device, comprising:”**

This limitation is substantively identical to [1.PRE] and Costa discloses it for the same reasons (claim 1 recites a method for forming the same).

2. **[18.A] “a first stacked layer disposed on a substrate;”**

This limitation is substantively identical to [1.A], and Costa discloses it for the same reasons.

3. [18.B] “a second stacked layer disposed on the first stacked layer; and”

This limitation is substantively identical to [1.F] and Costa discloses it for the same reasons. Here, the claim recites “on the first stacked layer” (instead of on the “third channel structure). The second stacked layer is “disposed on the first stacked layer” in Costa (and the ’532 Patent), because the ’532 Patent does not use “on” to mean “directly on,” i.e., the second stacked layer need not physically contact the first stacked layer. Ex. 1001, 8:1-11; *see also* Banerjee, ¶¶ 257-58.

4. [18.C] “a plurality of channel structures penetrating the first stacked layer and the second stacked layer;”

Costa discloses a plurality of channel structures in a first region (memory array region 100) of the 3D memory device. Costa, [0124], Figs. 3A-B, 10A-B. As discussed in [1.A]-[1.I], Costa discloses forming a plurality of first-tier memory openings 149 and second-tier memory openings 249 in memory array region 100, which are subsequently filled to form active memory channels. *See* Section X.A; Costa, [0135], [0161], [0190]; Banerjee, ¶ 260-61.

5. [18.D] “wherein each of the plurality of channel structures includes:” [18.E] “a first through hole penetrating the first stacked layer,”

This limitation is substantively identical to [1.B] and Costa discloses it for the same reasons.

6. **[18.F] “a first channel structure disposed at the bottom of the first through hole and in contact with the substrate,”**

This limitation is present in [1.C] and Costa discloses it for the same reasons.

7. **[18.G] “a second channel structure disposed in the first through hole and in contact with the first channel structure,”**

This limitation is substantively identical to [1.D] and Costa discloses it for the same reasons.

8. **[18.H] “a third channel structure disposed over the first through hole and in contact with the second channel structure, wherein a size of the third channel structure along a lateral direction is larger than a top aperture of the first through hole;”**

This limitation is substantively the same as [1.E] (but recites “disposed over” instead of “form[ed] ... above”) and Costa renders it obvious for the same reasons. Banerjee, ¶ 266.

9. **[18.I] “a second through hole penetrating the second stacked layer,”**

This limitation is substantively identical to [1.G] and Costa discloses it for the same reasons.

10. **[18.J] “a fourth channel structure disposed in the second through hole and in contact with the third channel structure, and”**

This limitation is substantively identical to [1.H] and Costa discloses it for the same reasons.

11. [18.K] “a fifth channel structure disposed over the second through hole and in contact with the fourth channel structure.”

This limitation is substantively the same as [1.I] (but recites “disposed over” instead of “form[ed] ... above”) and Costa discloses it, or renders it obvious, for the same reasons. Banerjee, ¶ 271.

J. Claim 20:

1. [20.PRE] “The joint opening structure of claim 18, wherein:” [20.A] “a thickness of the third channel structure is in a range between 30 nm and 70 nm.”

This limitation is identical to [16.PRE]-[16A] and Costa discloses it for the same reasons.

XI. GROUND 2: INDEPENDENT CLAIMS 1, 11, AND 18, AND DEPENDENT CLAIMS 2, 3, 13, 15-17, AND 20, ARE OBVIOUS OVER COSTA IN VIEW OF OH

To the extent that PO argues that Ground 1 is deficient because it does not expressly combine Costa with a secondary reference, PO would be incorrect, because obviousness always takes into account the knowledge of a POSITA. Regardless, Ground 2 expressly combines Costa with Oh (and the knowledge of a POSITA particularly with respect to alignment issues). Ground 2 applies the same claim mapping as Ground 1, and therefore Ground 2 does not repeat the claim mapping and incorporates that mapping fully herein. See Banerjee, ¶ 276.

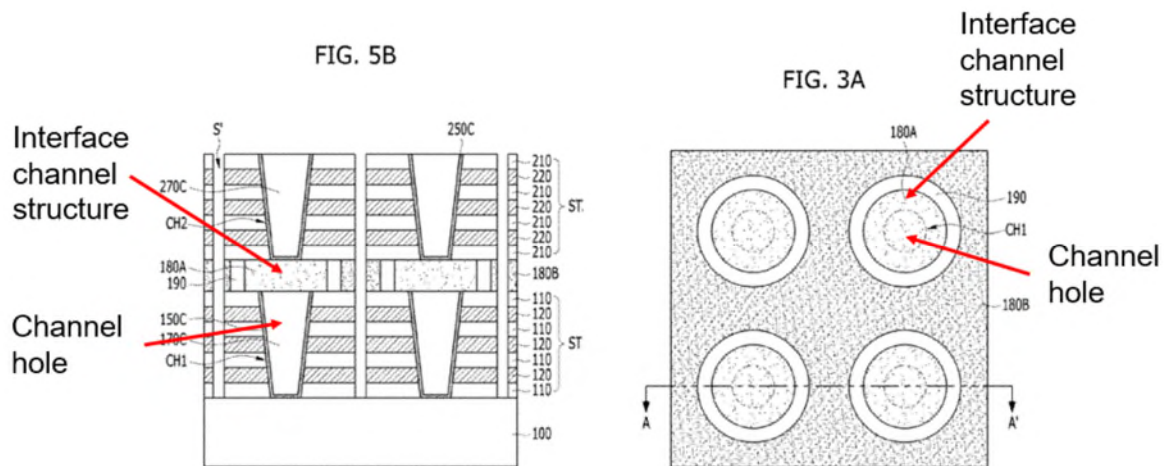
A. Motivation to Combine

A POSITA would have been motivated, with a reasonable expectation of success, in view of Oh's teaching and the knowledge of a POSITA to ensure that Costa's third channel structure is wider than the underlying, first through hole for several reasons.

To start, recall that Costa discloses that the third channel structure 173 "can contact an entire top surface of an underlying first memory opening fill structure 57" (Costa, [0265]) to protect the lower deck channel structure during processing. *Id.*; §X.A.6. Further, recall that Costa's process is not self-aligned and subject to misalignment. Costa, [0265], Figs. 20A, B (using mask 147 to form third channel structure). Next, Costa expressly recognizes, and seeks to mitigate, the risk of misalignment with structure 173. For example, Costa recognizes the need "to account for misalignment" when forming a channel interface structure over the first channel structure. *Id.*, [0164]. There, Costa recognizes that to only ensure contact between structure 173 and the through-hole semiconductive channel material (versus the entire fill structure), the structure 173 must be made wider than the width of 149' to ensure contact. *Id.*; Banerjee, ¶ 277. Thus, when Costa intends to fully cover the fill structure, consistent with accounting for misalignment, a POSITA would have understood that structure 173 would be made wider than the fill structure. *Id.* Indeed, Costa specifically discloses that a reason to use structure 173 is to address

“misalignment.” Costa, [0324]. Thus, a POSITA reading Costa would have been highly motivated to consider similar teachings, such as Oh (see §IX.B), that address misalignment of multi-stack structures with interface channel structures. Banerjee, ¶ 278.

Next, Oh discloses a very similar interface structure to Costa, and specifically teaches that it addresses the very alignment issues that are of concern to Costa. Oh teaches: “Referring to FIG. 3A the channel connection pattern 180A may have an island shape which overlaps the first channel holes CH1 order to secure an overlap margin between the channel connection pattern 180A and the first channel hole CH1, the channel connection pattern 180A may have a larger width than the top surface of the first channel hole CH1.” Oh, [0061]. This “overlap margin” is shown below:



Id., Figs. 3A, 5B. In other words, the “overlap margin” ensures that even if misalignment occurs, the channel interface structure will contact the channel semiconductor film in the first underlying memory hole. *Id.*; Banerjee, ¶¶ 279-80.

Importantly, a POSITA would have been motivated to consider Oh's widening of the third channel structure to increase "alignment margin" (Ex. 1016, [0086]), i.e., provide an "overlap margin" (Oh, [0061]). As a result, "memory opening alignment challenges may be reduced or avoided." Ex. 1017, [0058]. This enables first and second channels to "be easily connected." Ex. 1007, [0037]-[0038]. Similarly, it ensures that the interface channel structure and the lower channel are properly connected. *E.g.*, Oh, [0061] ("[C]hannel connection pattern 180A may have an island shape which overlaps the first channel holes CH1 ... [T]o secure an overlap margin between the channel connection pattern 180A and the first channel hole CH1). At bottom, providing this margin increases yield, because the margin allows for unaligned structures to still electrically couple. Banerjee, ¶¶ 280-83.

A POSITA would have had a high expectation of success in adapting Costa to include this overlap margin. First, the above demonstrates that providing such margin was a conventional and basic best practice in semiconductor fabrication. Second, as the above annotations to Costa's figures 20A and B demonstrate, Costa already discloses providing some margin in forming mask 147, and providing additional margin simply involves increasing the width of mask 147 (and less oxidation in the optional oxidation embodiment). Third, applying a margin actually simplifies the overall fabrication process, because it accounts for misalignment. Banerjee, ¶¶ 284-87.

XII. SECONDARY CONSIDERATIONS

Petitioner is unaware of any applicable secondary considerations of nonobviousness. None were identified during prosecution. *See generally* Ex. 1002. Even if such considerations existed, none would overcome the strong *prima facie* showing of obviousness.

XIII. CONCLUSION

Petitioner respectfully requests that the Board enter a final written decision finding the Challenged Claims unpatentable.

Respectfully submitted,

December 31, 2024

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing Petition for *Inter Partes* Review complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 13,884 words.

Dated: December 31, 2024

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Petition for *Inter Partes* Review and associated documents and exhibits were caused to be served on December 31, 2024 via overnight courier upon the following counsel of record for Patent Owner:

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Copies of this Petition and accompanying documents and exhibits were also served via electronic mail on Patent Owner's counsel of record for related PTAB proceedings and in the related district court litigation – ROPES & GRAY LLP and LATHAW & WATKINS LLP:

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Petition for *Inter Partes* Review of U.S. Patent No. 11,482,532

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