

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00245
U.S. Patent No. 11,482,532
Issue Date: October 25, 2022

Title: JOINT OPENING STRUCTURES OF THREE-DIMENSIONAL MEMORY
DEVICES AND METHODS FOR FORMING THE SAME

**DECLARATION OF DR. SANJAY K. BANERJEE IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 11,482,532**

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I, Dr. Sanjay K. Banerjee, declare as follows:

I. INTRODUCTION

1. I have been retained by Micron Technology, Inc. (“Micron”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”). I am not an employee of Micron or any affiliate or subsidiary of Micron.

2. I have been asked to consider whether certain references disclose or teach the features recited in the claims of U.S. Patent No. 11,482,532, which I refer to herein as the ’532 patent.

3. My opinions and the bases for my opinions are set forth below.

4. I am being compensated at my standard consulting rate of \$650 per hour for my time. My compensation is based solely on the amount of time that I devote to activity related to this case and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

II. BACKGROUND AND EXPERT QUALIFICATIONS

5. My *curriculum vitae* (“CV”) accompanies this declaration as Ex. 1004 and provides an accurate identification of my background, experience, and qualifications as an expert in electronics and three-dimensional memory technology.

6. I currently serve as the Cockrell Family Regents Chair Professor of Electrical and Computer Engineering and Director of the Microelectronics Research Center at the University of Texas at Austin (“UT”). Prior to this position, I was first an Assistant Professor (September 1987-August 1990) and later an Associate Professor (September 1990-August 1993) at UT, before being named a Professor in September 1993. Prior to starting my academic work at UT, I was a member of the technical staff at Texas Instruments (Corporate R&D) from the time I completed my doctoral studies in 1983 until August 1987. I worked on vertical 3D Dynamic Random Access Memory (DRAM) cells (see S. Banerjee and M. Bordelon, “A Model for the Trench Transistor,” IEEE Trans. Elec. Dev., 34 (12), 2485-2493, December 1987).

7. In addition to my academic work at UT, I was also the Director of the SouthWest Academy of Nanoelectronics, one of three centers created by the Semiconductor Research Corporation Nanoelectronics Research Initiative in 2006 to research and develop a replacement for conventional metal oxide semiconductor field effect transistors (“MOSFETs”) during the entire program.

8. I received my Ph.D. in Electrical Engineering from the University of Illinois in 1983. I also received an M.S. in Electrical Engineering from the University of Illinois in 1981. I received a B. Tech. in Electronics from the Indian Institute of Technology at Kharagpur in 1979.

9. As described in my CV (Ex. 1004), I have more than 40 years of experience in the field of electrical engineering, including extensive experience in semiconductor development and fabrication including that of 3-Dimensional Dynamic Random Access Memory (“DRAM”) cells, MOSFETs, flash memory, and beyond-complementary metal-oxide-semiconductor (“CMOS”) transistors. My work in these fields has resulted in thirty-five United States patents related to methods of forming polysilicon and novel transistors, flash memory, and vertical DRAM cells. I have been elected a Fellow of the National Academy of Inventors.

10. Much of my research and experience has related to methods for MOSFET fabrication and design, including deposition of thin films by chemical vapor deposition (CVD), atomic layer deposition (ALD), physical vapor deposition (PVD), patterning using photolithography and etching using plasma-based Reactive Ion Etching (RIE) which are some of the processing techniques used to make 3D NAND flash. I have worked extensively on polysilicon thin film transistors similar to the ones used in the channel of NAND flash memory cells, high-k and other dielectrics used for charge storage, and for tunneling. A number of the sponsored research grants on which I have been a principal or coinvestigator have related to chemical deposition methods and/or ultra-shallow source/drain junction technology, including “Transport in MOSFETs” (Motorola, August 1993-August 1994), “Ultra Shallow Junction Technology” (SEMATECH January 1994-December 1996), and

“Vertical Si-Ge-C MOSFETS” (Semiconductor Research Corporation September 2000-August 2003). In addition, I am an author on over forty publications relating to flash memory cells, including vertical 3D memory that can be used in NAND flash (e.g., Sarkar J, Dey S, Shahrjerdi D, Banerjee SK, Vertical Flash memory cell with nanocrystal floating gate for ultradense integration and good retention, IEEE Electron Device Letters 28 (5): 449-451 May 2007). One of my papers on flash memory was given a Best Paper Award by the SRC.

11. I am a Fellow of the Institute of Electrical and Electronics Engineers (“IEEE”), the American Physical Society (“APS”), and the American Association for the Advancement of Science (“AAAS”). I have served on numerous professional and government committees in the electrical engineering field, including chairing multiple IEEE committees, meetings, and programs, serving on Morgan & Claypool’s editorial board, and serving as a member on the International Technology Roadmap for Semiconductors (“ITRS”).

12. I have taught courses in Semiconductor Physics, Solid State Electronic Devices, and Microelectronic and VLSI Device Fabrication at UT. In addition, I have delivered many courses to industry on Semiconductor Devices and Memory and Semiconductor Processing. I have taught courses that cover 3D memories, such as 3D NAND (Ultra Large Scale Integration Techniques and Solid State Electronic

Devices). As a principal investigator, I have been the advisor to over 80 Doctoral and Masters students.

13. I am the co-author of several books and invited book chapters covering the area of electronic and semiconductor devices, including: Dopant Diffusion, Solid State Electronic Devices (three editions), Silicon-germanium Devices, and Novel 3D CMOS. I have authored or co-authored more than 1,000 papers and presentations in the areas of semiconductor devices and electronics development over the course of my career.

14. I have been the recipient of fifty grants to fund my research from a variety of funding agencies including the National Science Foundation (“NSF”), DARPA, the Department of Energy, Semiconductor Research Corporation, the Department of Defense-Multidisciplinary University Research Initiative, and the Office of Naval Research.

15. I have received numerous awards for my work, including the NSF Presidential Young Investigator Award. The NSF Presidential Young Investigator Award was¹ a highly competitive honor and grant bestowed annually upon

¹ The NSF Presidential Young Investigator Award was an award given out by the NSF until 1991, at which time it was replaced with the NSF Young Investigator Awards and Presidential Faculty Fellows Program.

recognized young academic leaders in science and engineering. I have received numerous other awards, including some the highest honors for semiconductor devices such as the Andrew Grove Award from the IEEE, and the Semiconductor Industry Association/Semiconductor Research Corporation University Researcher Award, for my work in semiconductor memory and transistors, which are described in more detail in my CV (Ex. 1004).

III. ASSIGNMENT AND MATERIALS CONSIDERED

16. I have been asked to provide analysis and explain the subject matter of the '532 patent, including the state of the art when the application underlying the '532 patent was filed. I have also been asked to consider, analyze, and explain certain prior art to the '532 patent including how that art relates to the challenged claims of the '532 patent and to provide my opinions regarding whether that art invalidates the claimed subject matter.

17. The opinions expressed in this declaration are not exhaustive of opinions I may offer in the future regarding the unpatentability of the claims of the '532 patent. Therefore, the fact that I do not address a particular point should not be understood to indicate an agreement on my part that any claim complies with the requirements of any other applicable rule.

18. I reserve the right to amend and supplement this declaration in light of additional evidence, arguments, or testimony presented during this IPR or related proceedings on the '532 patent.

19. In forming the opinions set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, knowledge of scientific and engineering principles, and my experience. I have also reviewed and considered the '532 patent (Ex. 1001), its prosecution history (Ex. 1002), and the following additional materials:

Exhibit	Description
1005	U.S. Patent Publication No. 2018/0182771 A1 to Costa et al. ("Costa")
1006	U.S. Patent Publication No. 2017/0154892 A1 to Oh ("Oh")
1007	U.S. Patent Publication No. 2015/0155296 A1 to Yoon
1008	Aritome, "NAND Flash Memory Technologies" (2016)
1009	Silvagni, "3D NAND Flash Based on Planar Cells," Computers 2017
1010	Micheloni et al., "Inside Solid State Drives (SSDs)" (2 nd Ed. 2018)
1011	U.S. Patent No. 10,475,737 to Tang et al.
1012	Micheloni, "3D Flash Memories" (2016)
1013	U.S. Patent No. 9,853,046 to Lu et al.
1014	U.S. Patent No. 9,530,866 to Zhang et al.

Exhibit	Description
1015	Plummer et al., “Silicon VLSI Technology: Fundamentals, Practice and Modeling” (2000)
1016	Certified Translation of KR 101487746 B1 to Lee et al. (including original Korean patent document)
1017	U.S. Patent Publication No. 2016/0204117 A1 to Liu et al.
1018	U.S. Patent Publication No. 2016/0284728 A1 to Lu et al.
1019	U.S. Patent No. 9,401,371 to Lee et al.
1020	U.S. Patent No. 9,570,460 to Kanakamedala et al.
1021	U.S. Patent No. 9,496,381 to Lee et al.

IV. UNDERSTANDING OF THE LAW

20. I am not an attorney, but have been instructed in and applied the law as described in this section.

21. I understand that the first step in comparing an asserted claim to the prior art is for the claim to be properly construed. I address how a person of ordinary skill in the art (POSITA) would have understood the claims of the alleged invention in Section V below.

22. I have been further instructed and understand that a patent claim is unpatentable and invalid as obvious if the subject matter of the claim as a whole would have been obvious to a POSITA of the claimed subject matter as of the time of the invention at issue. I understand that when assessing the obviousness of claimed subject matter, the following factors are evaluated: (1) the scope and content

of the prior art; (2) the difference or differences between each claim of the patent and the prior art; and (3) the level of ordinary skill in the art at the time the patent was filed.

23. I understand that claimed subject matter may be obvious in view of more than one item of prior art. I understand, however, that it is not enough to show simply that all the limitations of the claimed subject matter are spread throughout the prior art. Instead, for claimed subject matter to be obvious over multiple references, there must be some reason or motivation for a POSITA to combine the prior art references to arrive at the claimed subject matter.

24. I have been informed that, in seeking to determine whether an invention that is a combination of known elements would have been obvious to a POSITA at the time of the invention, one must consider the references in their entirety to ascertain whether the disclosures in those references render the combination obvious to such a person.

25. I have been informed and understand that, while not required, the prior art references themselves may provide a teaching, suggestion, motivation, or reason to combine. The motivation linking two or more prior art references can also come from other sources, including, for instance, economic or market demand or the common sense of a POSITA at the time of the invention.

26. I understand that a particular combination may be proven obvious by showing that it was obvious to try the combination. I have been informed that, if a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

27. I further understand that an obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references also may be supplied by the direction of the marketplace. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a POSITA has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

28. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. Thus, where all the elements of a claim are used in substantially the same manner, in devices in the same field of endeavor, the claim is likely obvious.

29. Additionally, I understand that a patent is likely to be invalid for obviousness if a POSITA can implement a predictable variation or if there existed

at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. Therefore, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.

30. I further understand that combining embodiments related to each other in a single prior art reference would not ordinarily require a leap of inventiveness.

31. I also understand that a POSITA must have had a reasonable expectation of success when combining references for claimed subject matter to be obvious.

32. I have been informed and I understand that factors referred to as "objective indicia of non-obviousness" or "secondary considerations" are also to be considered when assessing obviousness when such evidence is available. I understand that these factors can include: (1) commercial success; (2) long-felt but unresolved needs; (3) copying of the invention by others in the field; (4) initial expressions of disbelief by experts in the field; (5) failure of others to solve the problem the claimed subject matter solved; and (6) unexpected results.

33. I also understand that evidence of objective indicia of non-obviousness must be commensurate in scope with the claimed subject matter. I further understand that there must be a relationship, sometimes referred to as a "nexus," between any such secondary indicia and the claimed invention.

34. Finally, I have been informed that one cannot use hindsight to determine that an invention was obvious.

35. I provide my opinions in this declaration based on the guidelines set forth above.

V. LEVEL OF SKILL IN THE ART

36. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA may have for combining references.

37. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the relevant field. I have been further informed and understand that a person of ordinary skill in the art (POSITA) is also a person of ordinary creativity.

38. In my opinion, a POSITA in the field of the '532 patent would have had had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an

equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).

39. In my opinion, this POSITA would have been aware of and generally knowledgeable about 3D NAND's structure, how it is manufactured, and its component parts.

40. In view of my educational background and work experience, I was a person of more than the ordinary level of skill in the art as of March 2017. In forming my opinion, I have drawn on my academic background and professional experiences. My opinions herein, however, were formed by taking into account the perspective of an ordinarily skilled artisan.

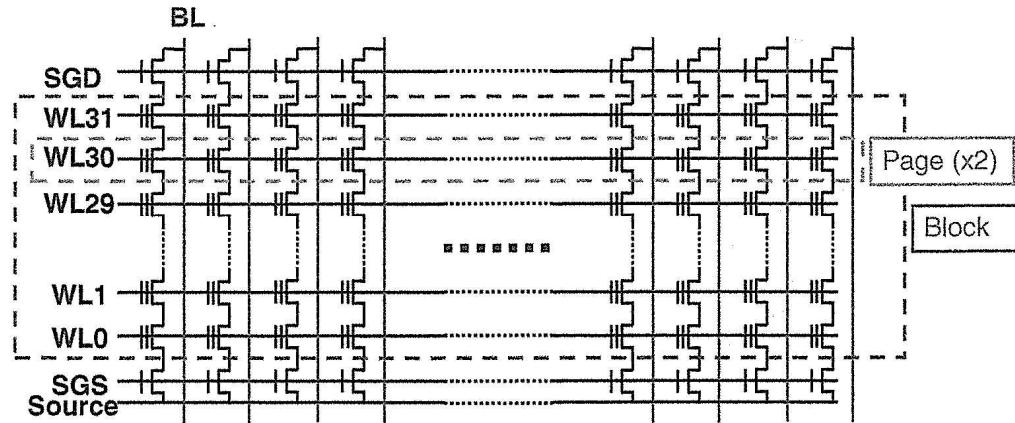
VI. TECHNOLOGICAL BACKGROUND

41. Before addressing the '532 patent in detail, some background on the technology of the '532 patent should be considered.

42. The '532 patent and the prior art references discussed in this Declaration relate to methods of fabricating three-dimensional (3D) memory devices, such as 3D NAND memory devices.

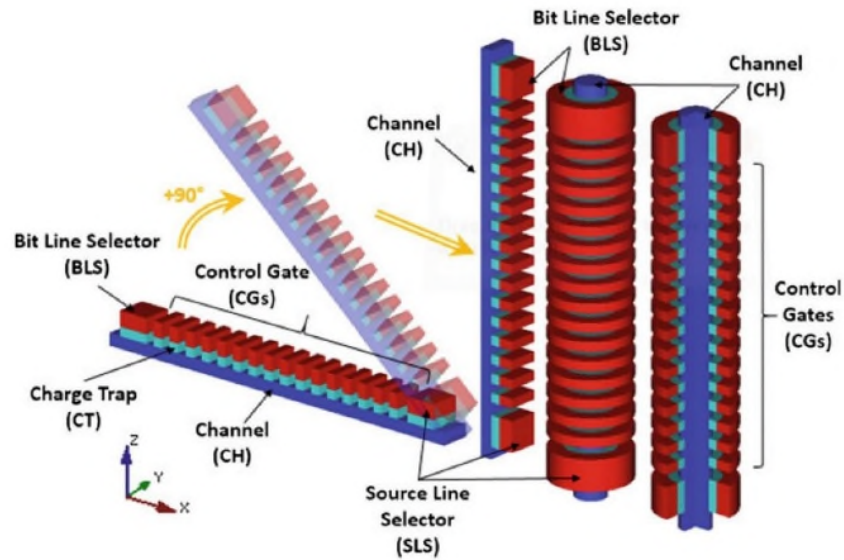
43. Central to NAND memory devices is a "memory cell," which stores information as electrical charge. In these devices, NAND memory cells are arranged in "strings" having multiple cells "connected in series." Ex. 1008, 38. Early NAND

memory devices were formed as two-dimensional arrays of cells on a substrate surface. *Id.*, 58.

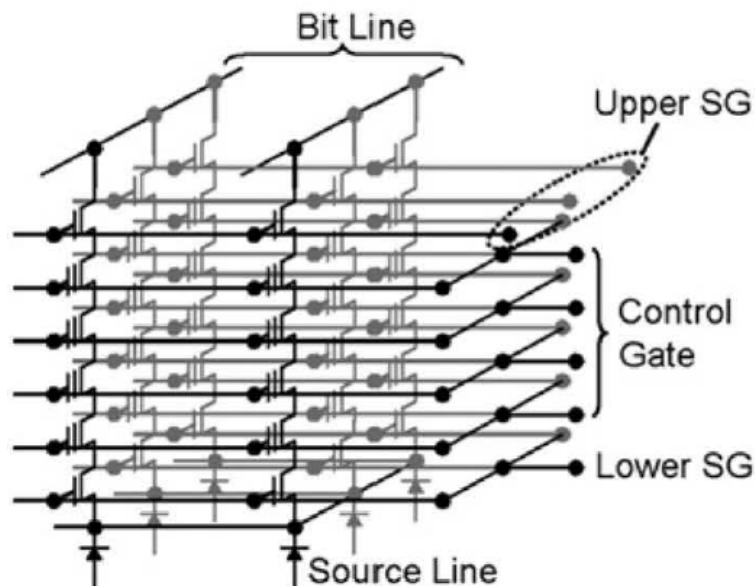


Id., 40 (Fig. 2.4).

44. “[T]o further scale down the memory cell size,” “three-dimensional (3D) NAND flash cells” were developed. Ex. 1008, 292. “Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block” and “turning the 2D NAND string upside,” “resulting” in a “3D structure” with a “vertical channel.” Ex. 1009, 3.



Ex. 1010, 122 (Fig. 5.2) (colors in the original). Multiple such vertical channels are repeated in a three-dimensional array:

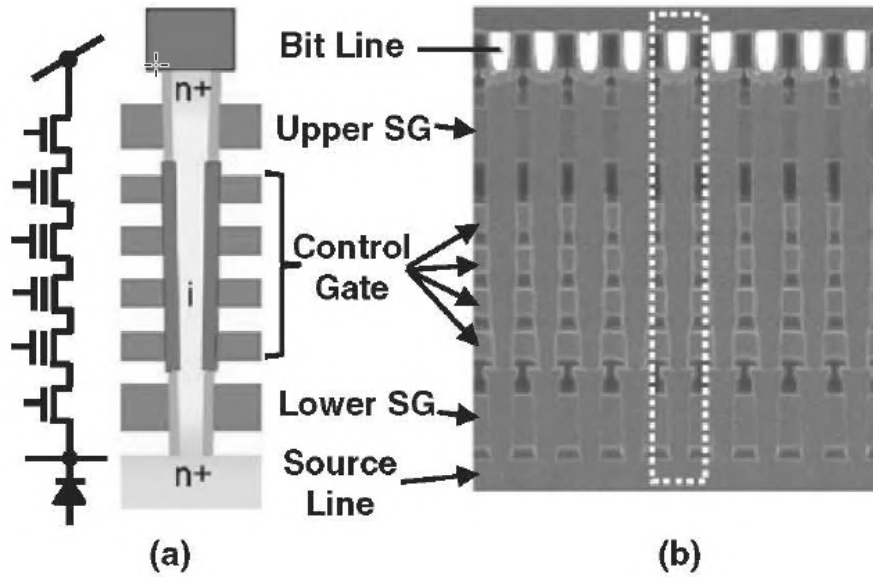


Ex. 1008, 296 (portion of Fig. 7.7).

45. A voltage applied on the control gate (which is also known as the word line) of each cell and the information stored in the cell (*e.g.*, binary 0 or 1 for a one-

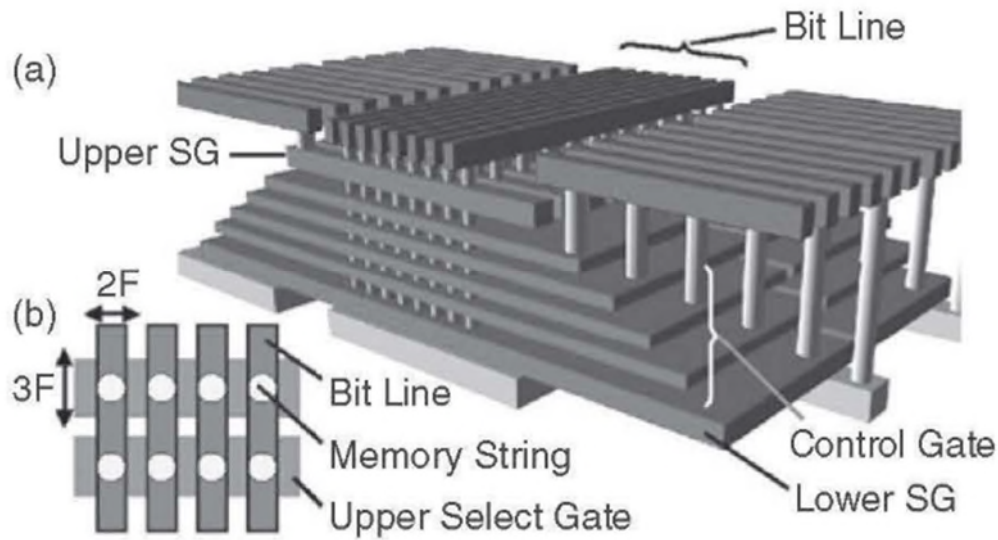
bit memory cell) determine whether the cell turns on or off. Specifically, the electrical charge (representing information) stored in the cell determines a threshold voltage of the cell, and the cell turns on when the control gate voltage is greater than the threshold voltage. Electrical current can only flow through a string when all cells in the string are turned on. Therefore, by applying a control gate voltage sufficient to turn on all but one cell (the selected cell) in a string and applying a suitable voltage to the control gate of the selected cell, the information stored in the selected cell may be determined using the amount of current flow through the string. This process is repeated by selecting a different cell to read (as an example operation) in the next cycle, eventually retrieving the requested information from the cells that store it.

46. A particular vertical memory cell “string is selected by a bit line and an upper select gate (upper SG).” Ex. 1008, 295-96. A memory cell “is located in the intersection of a control gate plate” and the channel of the string. *Id.* The lowest layer is a “select gate (lower SG),” which allows the strings to connect to a lower “common source.” *Id.*, 295, 297. An example 3D NAND vertical memory cell string is shown below:



Id., 296 (Fig. 7.5).

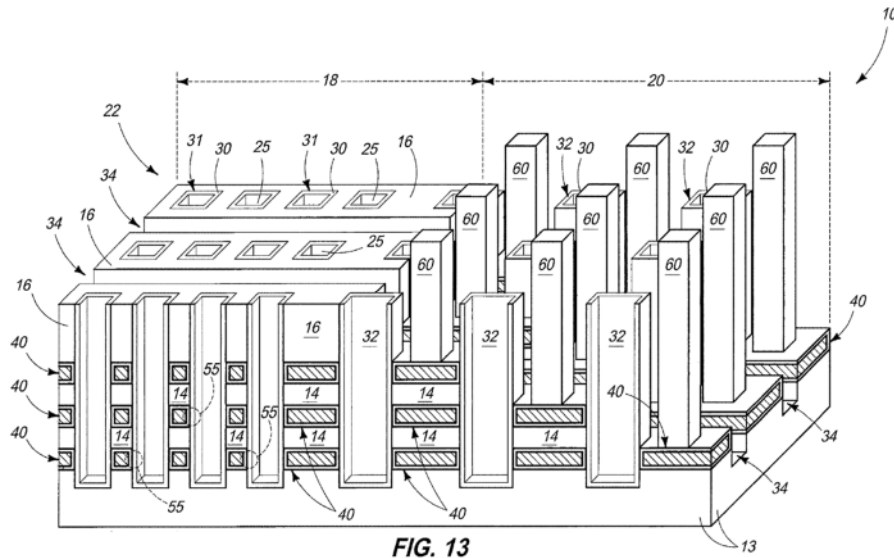
47. 3D NAND memory devices include “multi-stacked layers of [control] gate (plate)” material alternated with “dielectric” (insulator of direct current) in a “[s]tack.” Ex. 1008, 294. A “through-hole[.]” channel (which is also known as a channel structure) “filled by memory film ... and channel poly-Si” passes through the layers to form a string of vertically arranged memory cells. *Id.*, 295. “Each” layer of “electrode plate acts as a control gate.” *Id.* “[T]he control gates ... are connected ... [in a] stair-like gate structure.” *Id.*, 295-97.



Id., 296 (Fig. 7.6).

48. Vertical conductive structures couple the control gates to control voltages. The steps of the staircase structure provide landing areas for the vertical conductive structures to contact the control gates. Ex. 1008, 298.

49. An example of one such staircase structure is shown in the figure below from Ex. 1011 (U.S. Pat. No. 10,475,737). To access each memory cell via its control gate (also known as a word line), contacts (item 60 in the figure) are connected to landing pads at the end of each of the different control gates:



Id., Fig. 13, 4:56-64, 8:45-56.

50. At the time the '532 patent was filed, multi-deck 3D memory devices were also well-known. A “multi-deck” device is one that includes two memory stacks one on top of the other.

51. A POSITA would have recognized that the motivation behind the use of such a multi-deck structures is the difficulty in etching high aspect ratio channel holes of increased depth. This challenge became a limiting factor to memory density: as more layers are added it becomes more difficult to etch the channel holes. Ex. 1012, 211-215.

52. A multi-deck structure, however, avoids this problem and enables high aspect ratio channel holes to be more readily formed. In such a structure, the first deck is formed first and a hole is etched through the first deck. Then the second deck is formed on top of the first deck, and another hole is etched through the second

[illegible]

VII. THE '532 PATENT

53. I understand that the application leading to the '532 patent was filed on
 mber 18, 2020.

54. Based on my review of the '532 patent, I note that it identifies itself as a continuation of application No. 16/046,847 filed on July 26, 2018, which was issued as U.S. Patent No. 10,886,291, which claims priority to a PCT application filed March 1, 2018. It also identifies two foreign applications filed March 8, 2017.

55. For purposes of this declaration, I have been instructed to use March 8, 2017, as the effective filing date of the '532 patent. My opinions in this declaration were formed from the perspective of a POSITA as of March 8, 2017, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the prior art.

B. Overview

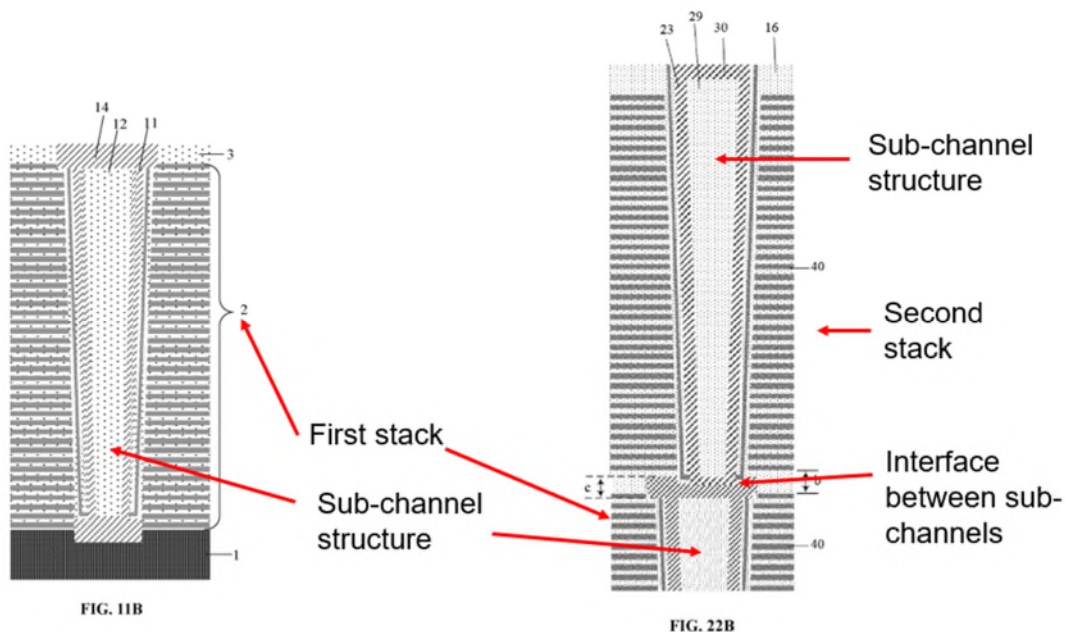
56. The '532 patent is entitled "Joint opening structures of three-dimensional memory devices and methods for forming the same." Ex. 1001, Title.

57. The patent relates generally to multiple-stack three-dimensional (3D) memory devices, *e.g.* 3D multiple-stack NAND devices. Ex. 1001, 1:17-37.

58. The patent explains that "3D NAND memory devices[] keep scaling more oxide/nitride (ON) layers" due to advances in semiconductor technology, creating difficulty in "us[ing] a single etching process to form the channel holes" as the depth (i.e., number of layers) increases. Ex. 1001, 1:17-37. "Thus, a single etching method may not be efficient in both cost and process capability." *Id.*, 1:36-37.

59. The patent then goes on to propose a multiple-stack structure employing certain joint opening structures, and methods for forming the same. See *generally* Ex. 1001.

60. More particularly, the '532 patent proposes a first memory stack (*e.g.*, the stack shown in Figure 11B reproduced and annotated below), forming a sub-channel structure therein, forming a second memory stack on the first stack (*e.g.*, the upper stack shown in Figure 22B), and forming a sub-channel structure therein that connects to the first sub-channel via an interface:



Ex. 1001, Figs. 11B (annotated), 22B (annotated).

61. As I will discuss in greater detail below when comparing the claims to the prior art, the '532 patent's claims refer to the features that comprise the above sub-channels and interface therebetween as the first, second, third, fourth, and fifth

channel structures, the first and second functional layers, and the first and second filling structures.

C. Prosecution History

62. As noted above, I have reviewed the '532 patent's prosecution history.

63. On March 3, 2022, the Office determined that the 20 claims are subject to a restriction requirement and determined that claims 1-10 are drawn to a method of forming a joint opening in a three-dimensional memory device whereas claims 11-20 are drawn to a joint opening in a three-dimensional memory device. Ex. 1002, 578. On March 16, 2022, the applicant elected to continue prosecution on the second group of claims (claims 11-20) drawn to a joint opening in a three-dimensional memory device. *Id.*, 583.

64. On March 29, 2022, the Office rejected claims 11-12 and 14-20 as obvious over a reference to Lee '158 (U.S. Pub. No. 2013/0109158) in view of Huo (U.S. Pub. No. 2013/0203227). Ex. 1002, 591. The Office also rejected claims 11-20 on the ground of non-statutory double patenting as being unpatentable over claims 11-15 and 18-20 of co-pending Application No. 16/046,847 (which was issued as U.S. Pat. No. 10,886,291 (the "'291 patent")). *Id.*, 597-98.

65. The applicant responded and filed a terminal disclaimer on May 27, 2022, as to the '291 patent. The applicant further amended claim 18 and made several arguments against the Examiner's rejections to the claims. Specifically,

Applicant argued that “claim 11 recites at least the below features that distinguish over the applied references:

a third channel structure in contact with the second channel structure disposed over the first through hole, wherein **a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate;**

...

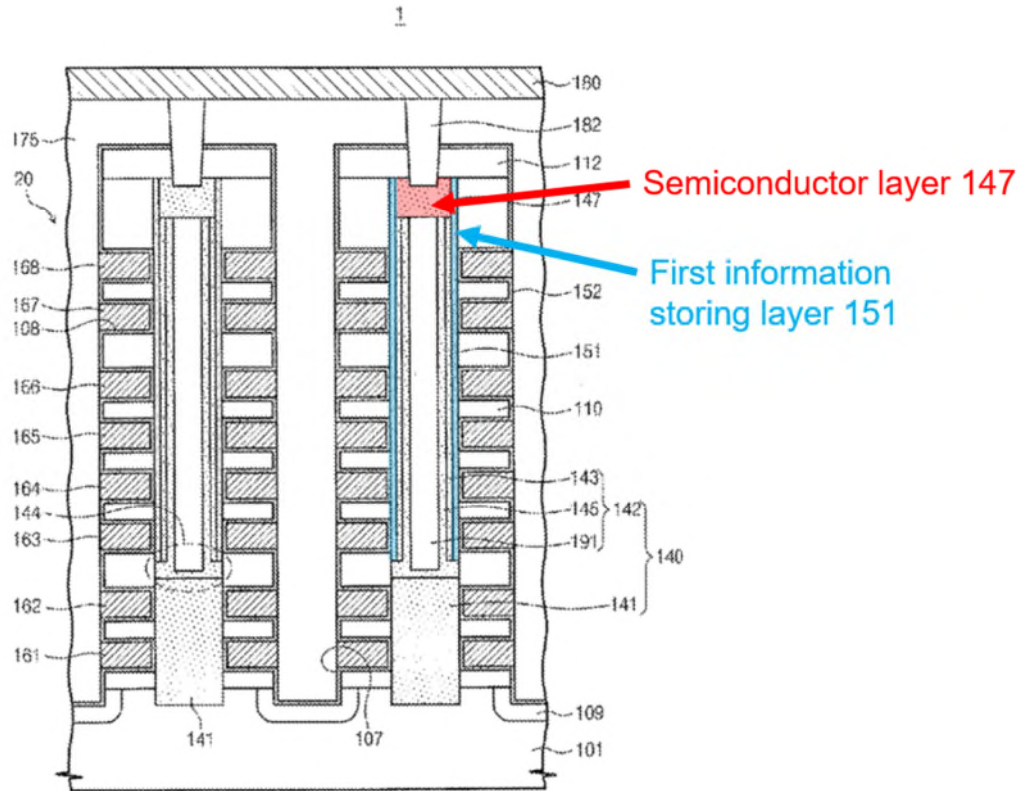
a fifth channel structure in contact with the fourth channel structure disposed over the second through hole,

Ex. 1002, 622 (emphasis in original). I note that the quoted language appears to have been mistakenly taken from claim 11 of the '291 patent.

66. Applicant went on to elaborate that in Lee, semiconductor layer 147 does not “cover[] the projection of the first through hole” as the claim requires because it is “within” and “encircled by” the first information storing layer 151. Ex. 1002, 623.

67. In other words, as shown in the below annotated version of Figure 1P of Lee, semiconductor layer 147 (annotated red) does not—according to the applicant—“cover” the “through hole” because it is within, does not meet the walls of, and is separated from the walls of the through hole by layer 151 (annotated blue):

Fig. 1P



Ex. 1002, 624, Lee '158, Fig. 1P (annotated).

68. Regarding the claimed fifth channel structure, Applicant argued that Huo—the secondary reference relied on by the Examiner—does not disclose a fifth channel structure in contact with the fourth channel structure. Moreover, because the lower and upper sub-channels are distinct and different structures in Huo, the Examiner improperly assumed that there would be an element of the lower sub-channel on the upper sub-channel. Ex. 1002, 624-25.

69. This then led the Examiner to allow the claims. In so doing, the withdrawn claims 1-10 were rejoined, examined, and allowed along with claims 11-

20. Ex. 1002, 641. The Examiner stated that the prior art did not teach or render obvious the limitation of forming a size of the third channel structure along a lateral direction is larger than a top aperture of the first through hole. *Id.*, 642.

D. Claims

70. For reference, claims 1-3, 11, 13, 15-18, and 20 of the '532 patent are reproduced below:

1. A method of forming a joint opening structure in a three-dimensional (3D) memory device, comprising:

forming a first stacked layer on a substrate;

forming a first through hole penetrating the first stacked layer to expose the substrate;

forming a first channel structure at a bottom of the first through hole and in contact with the substrate;

forming a second channel structure in the first through hole and in contact with the first channel structure;

forming a third channel structure above the first through hole and in contact with the second channel structure, wherein a size of the third channel structure along a lateral direction is larger than a top aperture of the first through hole;

forming a second stacked layer over the third channel structure;

forming a second through hole penetrating the second stacked layer to expose the third channel structure;

forming a fourth channel structure in the second through hole and in

contact with the third channel structure; and
forming a fifth channel structure above the second through hole and
in contact with the fourth channel structure.

2. The method of claim 1, wherein:

the first stacked layer includes a first number of oxide/nitride layer
pairs; and

the second stacked layer includes a second number of oxide/nitride
layer pairs.

3. The method of claim 2, wherein:

the first number and the second number are not less than 32.

11. A joint opening structure of a three-dimensional (3D) memory
device, comprising:

a first through hole penetrating a first stacked layer along a vertical
direction;

a first channel structure disposed at the bottom of the first through
hole;

a second channel structure in contact with the first channel structure
disposed in the first through hole;

a third channel structure in contact with the second channel structure
disposed over the first through hole, wherein a size of the third
channel structure along a lateral direction is larger than a top
aperture of the first through hole;

a second stacked layer disposed on the third channel structure;

a second through hole penetrating the second stacked layer along the vertical direction;

a fourth channel structure in contact with the third channel structure disposed in the second through hole;

a fifth channel structure in contact with the fourth channel structure disposed over the second through hole.

13. The joint opening structure of claim **11**, further comprising:

a first filling structure covering the surface of the second channel structure; and

a second filling structure covering the surface of the fourth channel structure;

wherein the first through hole is non-interconnected with the second through hole.

15. The joint opening structure of claim **11**, wherein:

the first stacked layer includes a first number of conductor/dielectric layer pairs;

the second stacked layer includes a second number of conductor/dielectric layer pairs; and

the first number and the second number are not less than 32.

- 16.** The joint opening structure of claim **11**, wherein:
a thickness of the third channel structure is in a range between 30 nm and 70 nm.
- 17.** The joint opening structure of claim **11**, wherein:
a size difference between the top aperture and a bottom aperture of the first through hole is equal to or less than 30 nm; and
a size difference between a top aperture and a bottom aperture of the second through hole is equal to or less than 30 nm.
- 18.** A joint opening structure of a three-dimensional (3D) memory device, comprising:
a first stacked layer disposed on a substrate;
a second stacked layer disposed on the first stacked layer; and
a plurality of channel structures penetrating the first stacked layer and the second stacked layer;
wherein each of the plurality of channel structures includes:
a first through hole penetrating the first stacked layer,
a first channel structure disposed at the bottom of the first through hole and in contact with the substrate,
a second channel structure disposed in the first through hole and in contact with the first channel structure,
a third channel structure disposed over the first through hole and in

contact with the second channel structure, wherein a size of the third channel structure along a lateral direction is larger than a top aperture of the first through hole;

a second through hole penetrating the second stacked layer,

a fourth channel structure disposed in the second through hole and in contact with the third channel structure, and

a fifth channel structure disposed over the second through hole and in contact with the fourth channel structure.

20. The joint opening structure of claim **18**, wherein:

a thickness of the third channel structure is in a range between 30 nm and 70 nm.

VIII. CLAIM CONSTRUCTION

71. I am not a legal expert or an attorney and offer no opinions on the law. I understand that claim construction is a matter of law. However, I have been informed by counsel of the legal standards that apply to claim construction in an *inter partes* review, and I have applied them in forming my opinions. I understand that during an *inter partes* review, the same claim construction standard used in federal district court is applied when addressing the meaning of claim terms.

72. I have been informed that the words of a claim are generally given their plain and ordinary meaning that the term or phrase would have to POSITA at the

time of the invention in view of the surrounding claim language, the specification, and the file history (collectively, the “intrinsic evidence” or “intrinsic record”).

73. I also understand that courts may consider extrinsic evidence, such as expert and inventor testimony, dictionaries, and learned treatises (collectively, the “extrinsic evidence” or the “extrinsic record”), but that such extrinsic evidence should be given less weight than the intrinsic evidence.

74. In my opinion, the terms of the ’532 patent’s claims do not require further construction and can be afforded their plain and ordinary meaning for purposes of the analysis of the prior art that I am conducting in this declaration. I have provided further discussion of how a POSITA would have understood the ’532 patent’s claim terms in the sections below.

IX. UNPATENTABILITY ANALYSIS

75. For the reasons I explain in greater detail below, it is my opinion that as of the effective filing date of the ’532 patent, a POSITA would have considered Claims 1-3, 11, 13, 15-18, and 20 of the ’532 patent to be unpatentable as obvious over the prior art discussed in this declaration.

A. Overview of the Prior Art

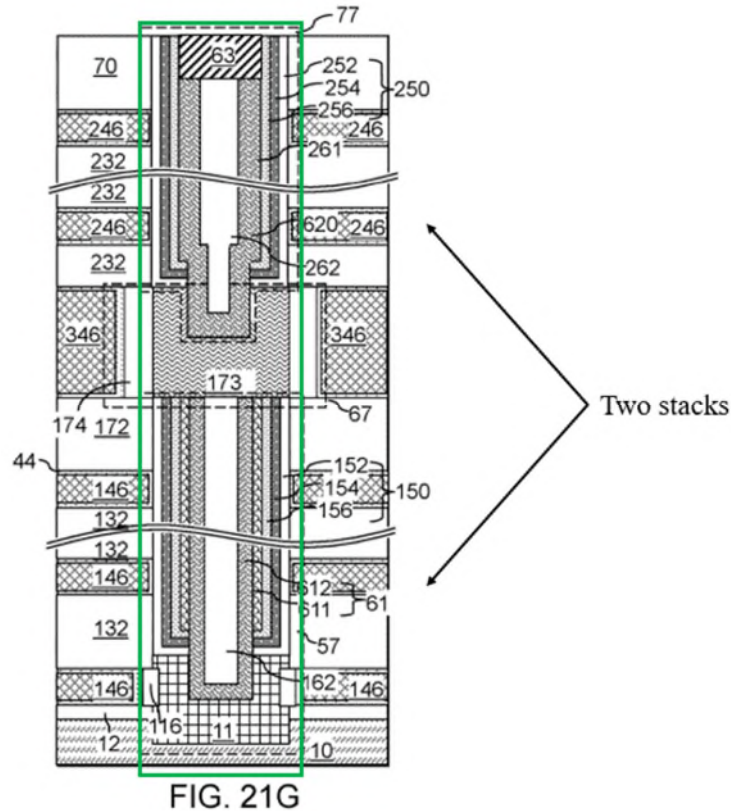
76. The following paragraphs provide an overview of the main prior art references I discuss throughout this declaration.

1. Costa

77. Costa (Ex. 1005) indicates on its face that it was filed February 28, 2017. *See* Costa, Cover. In view of this date filing, which is before the '532 patent's own March 2017 priority date, I understand that Costa is prior art under 35 U.S.C. § 102(a)(2).

78. Costa relates generally to “multi-tier three-dimensional memory devices containing dummy memory cells for providing inter-tier connection and methods of making the same.” Costa, [0002].

79. Costa discloses forming a vertical memory channel (shown in green in the annotated version of Figure 21G below) in a multi-tier three-dimensional memory structure:



Costa, Fig. 21G (annotated).

80. Costa also explains “challenges for fabricating a multi-tier memory stack structure include formation of memory openings having high aspect ratios and alleviation of effects of misalignment of tier-level memory openings formed in different tier structures.” Costa, [0003].

81. Because of this, Costa provides methods “for providing a reliable connection between vertically neighboring memory stack structures.” Costa, [0003].

82. Specifically, Costa discloses forming “first alternating stack (132, 142)” on substrate 10. Costa, [0126]-[0127].

83. First-tier insulating cap layer 172 is formed over the first alternating stack (132, 142) to form the first-tier structure (132, 142, 172), which can be patterned to form “a first terrace region” located in a contact region of the device. Costa, [0134]-[0135].

84. First-tier openings (149, 119) are then formed for example by lithographic patterning and an anisotropic etch process. Costa, [0137]. This is shown in Figure 3B below:

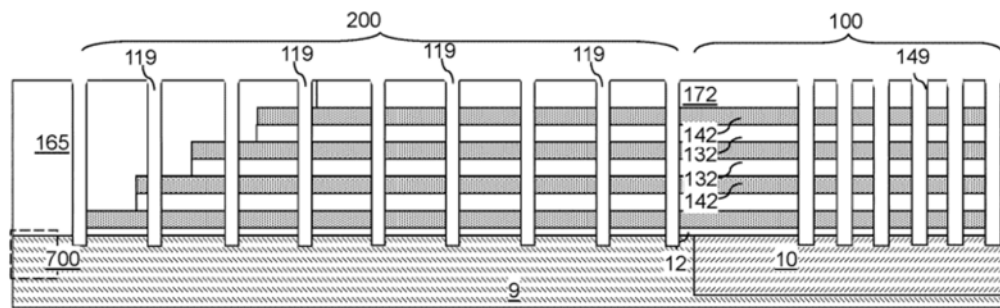
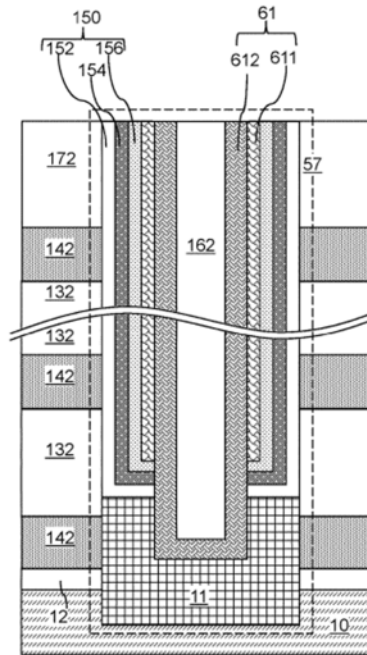


FIG. 3B

Id., Fig. 3B.

85. A memory channel is formed in first-tier memory openings 149 by first forming epitaxial channel portion 11 in the bottom of each hole and subsequently forming a memory film 150, first outer and inner semiconductor channel layers (611, 612), and filling the remainder of the opening with dielectric core 162. Costa, [0141]-[0160]. Figure 4B shows one such memory channel:



Id., Fig. 4G.

86. In one embodiment, a joint-level doped semiconductor layer 173L is formed over the first-tier structure (*e.g.*, shown above in Fig. 4G) and subsequently patterned, removing the portions not over first-tier openings (149, 119), leaving joint-level doped semiconductor portion 173. Costa, [0263]-[0266], Figs. 20A-B.

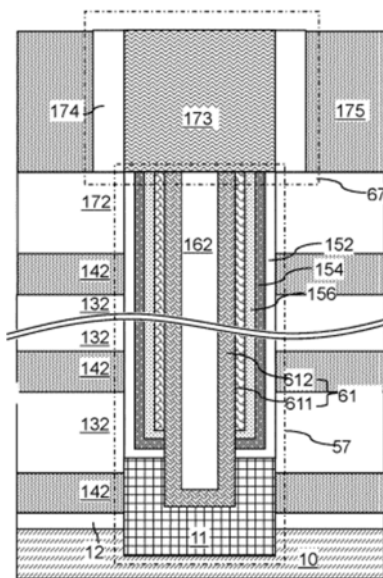
87. Costa states that “[i]n one embodiment, the bottom surface of each joint-level doped semiconductor portion 173 can contact an entire top surface of an underlying first memory opening fill structure 57.” Costa, [0265].

88. Exposed portions of semiconductor portion 173 can be oxidized, converting those portions to dielectric material 174'. Costa, [0266], Fig. 20C. An annular dielectric spacer is formed by removing the top portion of 174'. *Id.*, [0268],

[0266] (“In an alternative embodiment shown in the dashed line inset in FIG. 20C, only the sidewalls of the joint-level doped semiconductor portions 173 are oxidized to form a first annular dielectric spacer 174.”), Fig. 20C.

89. Joint-level spacer material 175 is then deposited over the first-tier structure and around semiconductor portion 173 and dielectric spacer 174. Costa, [0268]. This completed structure is shown below in Figure 20D:

FIG. 20D



Id., Fig. 20D.

90. Per Costa, a second-tier structure and memory channel are formed in much the same way as the first-tier structure.

91. A second alternating stack (232, 242) is formed over joint level spacer 175, joint-level doped semiconductor portion 173, and dielectric spacer 174. Costa, [270], [0178]-[0180]. Second-tier insulating cap layer 70 is formed over the second

alternating stack and second-tier memory holes 249 are formed by a similar process to that of first-tier memory holes 149. *Id.*, [270], [0183]-[0192].

92. A memory channel is formed in second-tier memory openings 249 by forming a memory film 250 (comprised of layers 252, 254, 256), second outer and inner semiconductor channel layers (621, 622), and then filling the remainder of the opening with dielectric core 262. Costa, [0272]-[0276].

93. Drain region 63 is then formed in a recess etched into dielectric core 262 and second inner semiconductor channel layer 622). Costa, [0277]. Drain region 63 is deposited in and above the dielectric core cavity, and overlying material is planarized. *Id.*, [0212], [0277] (referring to [0212] description).

94. This results in a multi-tiered vertical memory channel (shown in green in Figure 21G below). Costa, [0278].

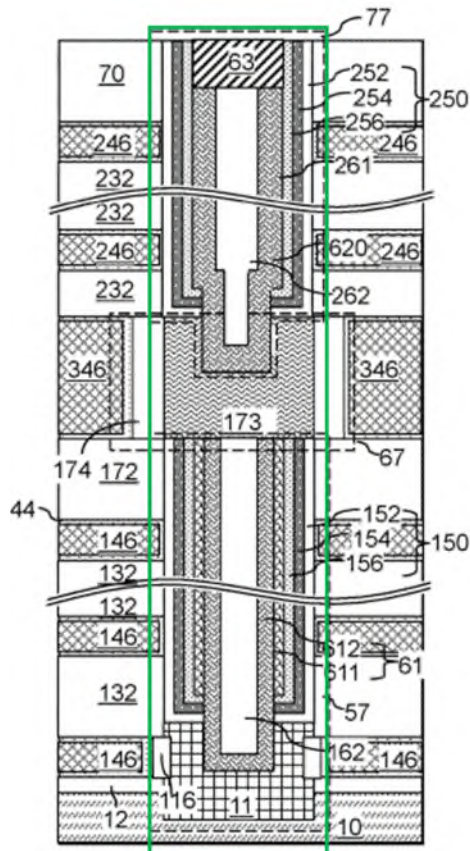


FIG. 21G

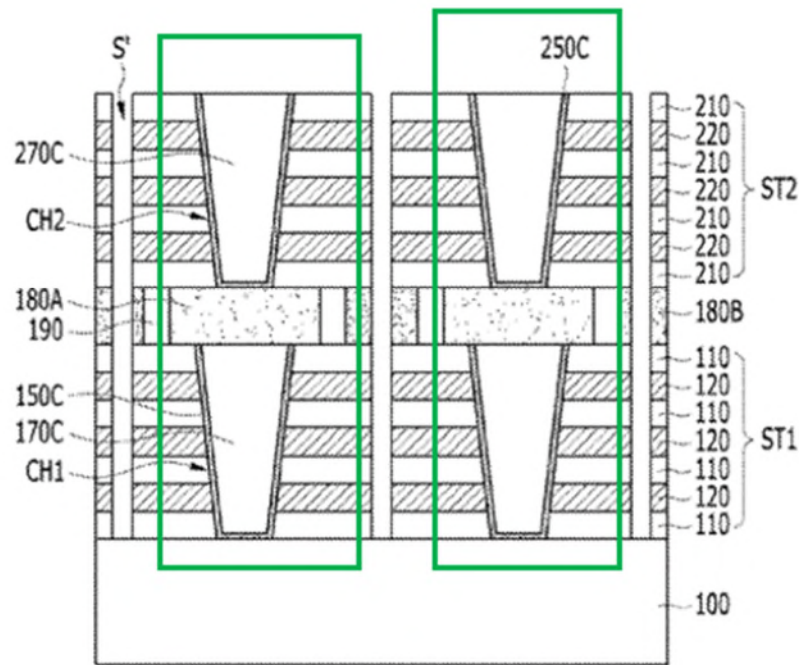
Id., Fig. 21G (annotated).

2. Oh

95. Oh (Ex. 1006) indicates on its face that it was filed June 10, 2016. See Oh, Cover. In view of this date filing, which is before the '532 patent's own March 2017 priority date, I understand that Oh is prior art under 35 U.S.C. § 102(a)(2).

96. Oh and Costa both relate to multi-deck channel structures. As shown below, Oh discloses an interface structure (180A):

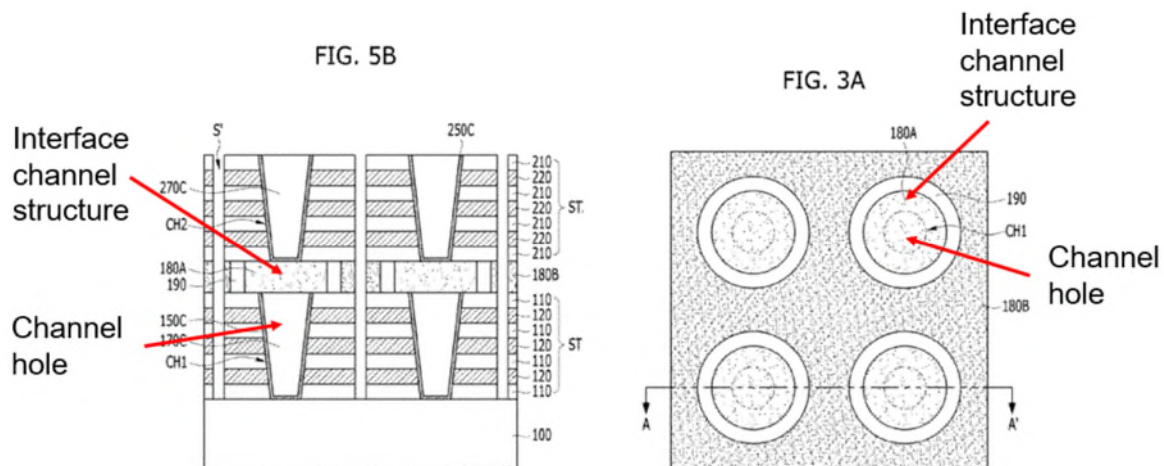
FIG. 5B



Oh, Fig. 5B (annotated).

97. Oh discusses various alignment issues in multi-stack structures. For example, Oh addresses alignment issues in forming slit structures, that is, structures that extend laterally throughout the array. As Oh discloses, these alignment issues arise when forming slit structures separately through each stack. Oh, [0047]. Oh discloses that slits have a small width. As a result, the alignment issues are more challenging. *Id.* Oh discloses: “Thus, an overlap margin is low and a manufacturing process is likely to fall.” *Id.* This refers to the fact that if the width is smaller, there is less margin for misalignment.

98. Oh also addresses alignment issues with respect to the channel structures. Oh discloses a channel interface structure to address this issue (180A below). Oh discloses: “Referring to FIG. 3A the channel connection pattern 180A may have an island shape which overlaps the first channel holes CH1 order to secure an overlap margin between the channel connection pattern 180A and the first channel hole CH1, the channel connection pattern 180A may have a larger width than the top surface of the first channel hole CH1.” Oh, [0061]. This “overlap margin” is shown below. As can be seen below, even if the top channel structure does not perfectly align to the middle of 180A, because of the width of 180A, there is margin that allows for misalignment. The top and bottom channel structures must electrically couple to form a continuous channel. That coupling occurs through 180A, and 180A allows this electrical coupling even if there is misalignment.



bottom sub-channel and the top channel structure need not be formed perfectly over 180A. The process for forming both (180A and the top channel structure) is not self-aligned, and thus this overlap margin accounts for standard misalignment and process variations.

B. Ground 1: Claims 1-3, 11, 13, 15-18, and 20 Are Obvious Over Costa

99. In my opinion, a POSITA would have considered Costa to be within the scope of the prior art and highly relevant to the patentability of the '532 patent's claims.

100. In my opinion, when viewed and considered in light of the knowledge of a POSITA, Costa renders claims 1-3, 11, 13, 15-18, and 20 of the '532 patent obvious.

1. Claim 1

[1.Pre] “A method of forming a joint opening structure in a three-dimensional (3D) memory device, comprising:”

101. In my opinion, to the extent the preamble is limiting it is taught by Costa.

102. Before summarizing Costa's pertinent disclosures, I will walk through how the '532 patent uses the term “joint opening structure.”

103. In the '532 patent, “joint opening structure” refers to an opening structure of a three-dimensional (3D) memory device created by “combining two through hole formation processes.” Ex. 1001, 15:33-35.

104. In other words, this is simply a reference to the well-known technique of forming channel structures in multi-tier memory devices using two etch processes.

105. Moving on to Costa, Costa teaches forming a joint opening structure by etching a first memory through hole in a first stack (and forming a channel structure therein), forming a second stack on the first stack, and etching a second memory through hole in the second stack (and forming a channel structure therein).

106. For instance, Costa explains that “[t]he present disclosure relates generally to the field of three-dimensional memory devices and specifically to multi-tier three-dimensional memory devices ... and methods of making the same.” Costa, [0002]. Likewise, it notes that it discusses “fabricating a multi-tier memory stack structure” and “providing a reliable connection between vertically neighboring memory stack structures[.]” *Id.*, [0003]; *see also* Figs. 4A-4G, 10-11 (showing first-tier opening (149, 119), and second-tier openings (249, 219)).

[1.A] “forming a first stacked layer on a substrate;”

107. This, in my opinion, is taught by Costa.

108. According to the ’532 patent, “the first stacked layer 2 can be formed on the substrate 1 [and] can include a plurality of oxide/nitride layer pairs.” Ex. 1001, 9:23-25, Fig. 1.

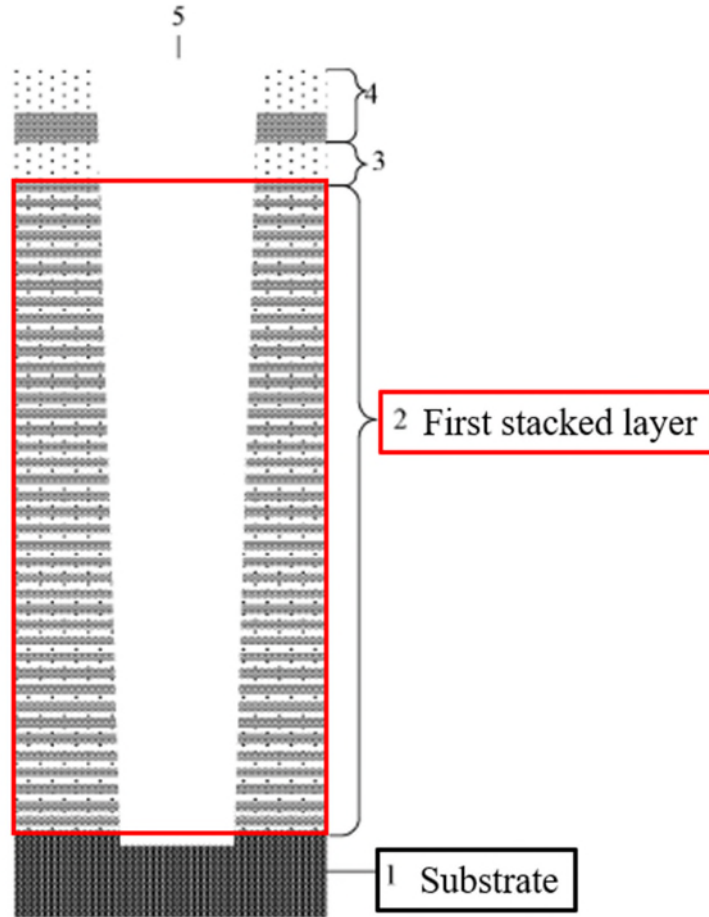
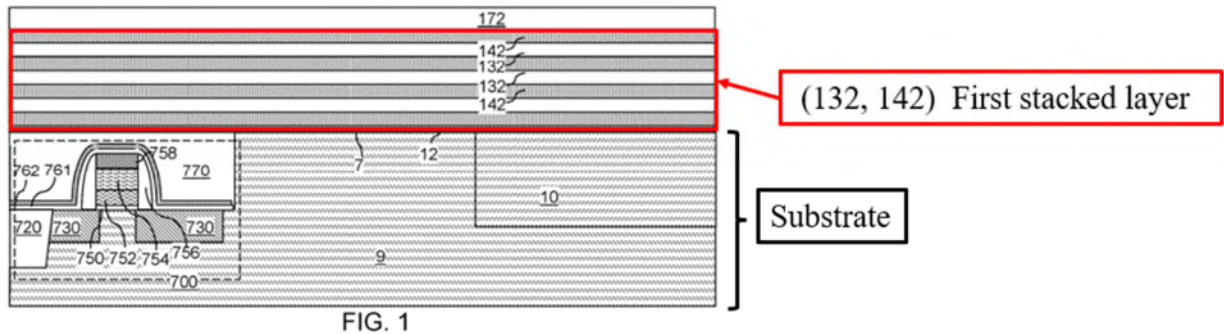


FIG. 1

Id., Fig. 1 (annotated).

109. Costa discloses the same layers and process. In particular, Costa forms a first stacked layer (“first alternating stack” 132, 142) and then forms a first insulating connection layer (“first insulating cap layer 172”) on the first stacked layer. Costa, [0134].



Id., Fig. 1 (annotated).

110. According to Costa, “[a]n alternating stack of first material layers and second material layers is subsequently formed. Each first material layer [132] can include a first material, and each second material layer [142] can include a second material that is different from the first material.” Costa, [0126].

111. The first material layer 132 can be an insulating material, such as “silicon oxide ... [or] dielectric metal oxides ... commonly known as high dielectric constant (high-k) dielectric oxides....” Costa, [0126], [0129].

112. The second material layers 142 can be a “sacrificial material,” such as “silicon nitride,” that “can be subsequently replaced with electrically conductive electrodes....” Costa, [0129]-[0131].

[1.B] “forming a first through hole penetrating the first stacked layer to expose the substrate;”

113. This, in my opinion, is taught by Costa.

114. According to the '532 patent, the first through hole 5 by overlaying a mask layer 4 and performing an etching process to form the first through hole. Ex. 1001, 9:65-10:2, 10:12-25.

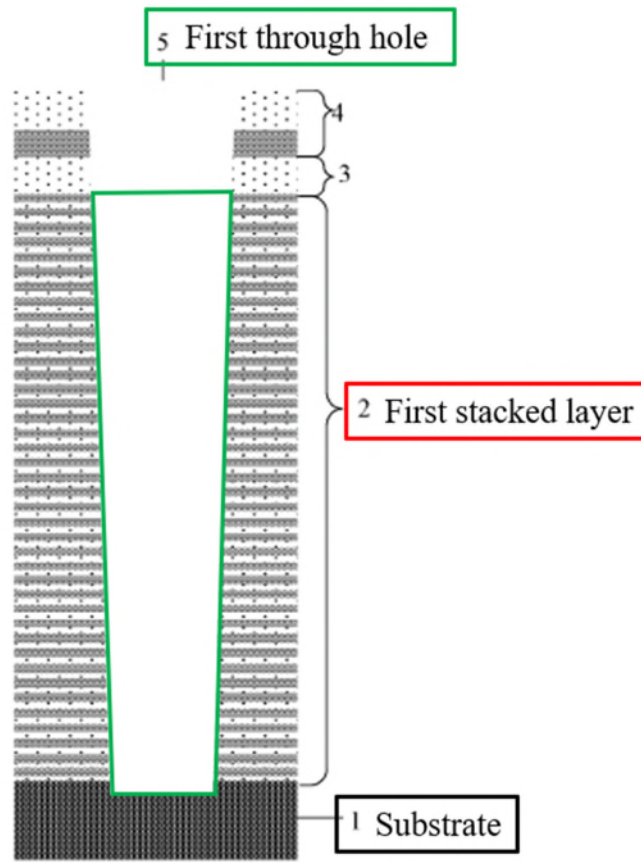


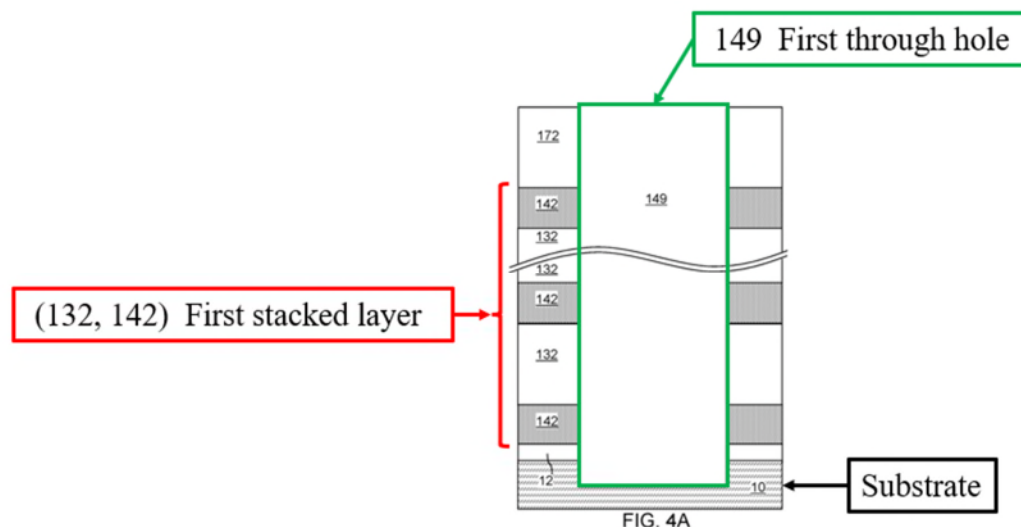
FIG. 1

Id., Fig. 1 (annotated). The above identifies the “first through hole” through the first stack. But the “first through hole” could map to include the hole portion that extends through the connection layer 3 as well, similar to my analysis in [1.F] for the “second through hole.” This distinction is irrelevant, because Costa’s third channel structure is above the “first through hole” under either interpretation, namely, Costa’s third channel structure is above its connection layer.

115. Costa teaches this same process. In particular, Costa forms a first through hole (“first-tier memory opening[.]” 149) that penetrates the first stacked layer (“first alternating stack” 132, 142) and the first insulating connection layer (“first-tier insulating cap layer 172”).

116. In particular, in Costa “first-tier openings (149, 119) extending to a top surface of the substrate (9, 10) are formed through the first tier structure (132, 142, 172, 165).” Costa, [0137]; *see also id.* (similarly discussing forming first-tier openings by lithographic patterning and etching, *i.e.*, masking).

117. As shown in the below annotated version of Figure 4A, Costa’s first-tier memory opening 149 penetrates the first tier structure (132, 142, 172) exposing substrate 10:



Costa, Fig. 4A (annotated); *see also Id.*, Fig. 3B. The “second through hole” in Costa could include only the portion through the first stack, excluding the portion through

the connection layer 172 shown above. Again, the distinction is irrelevant to claim 1, because Costa's third channel structure is above the through-hole under either interpretation. See limitation [1.E].

[1.C] “forming a first channel structure at a bottom of the first through hole and in contact with the substrate;”

118. This, in my opinion, is taught by Costa.

119. In the '532 patent, the claimed first channel structure is formed by depositing material “on the surface of the substrate 1 that is exposed by the first through hole 5” (i.e. at the bottom of the first through hole). Ex. 1001, 10:26-30, Fig. 2.

120. “[T]he first channel structure [] can be a polycrystalline silicon (polysilicon) layer formed by using a selective epitaxial process.” Ex. 1001, 10:28-30.

121. This is shown in Figure 2 below:

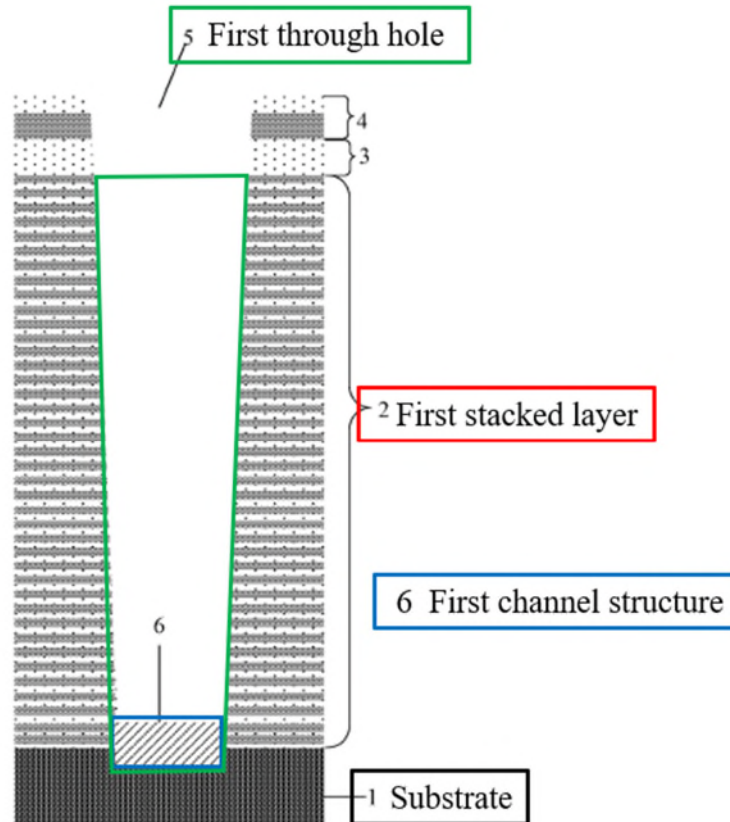


FIG. 2

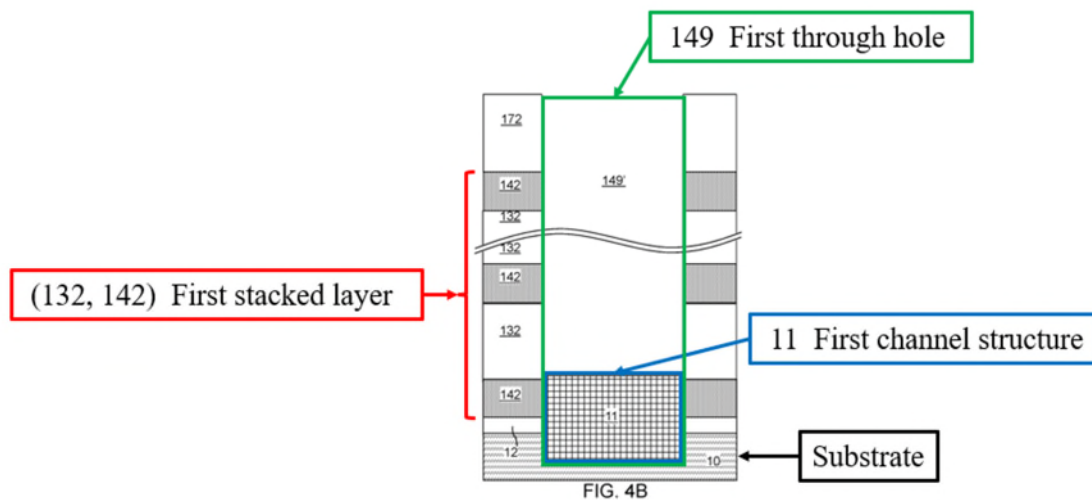
Ex. 1001, Fig. 2 (annotated).

122. In my opinion, Costa teaches this same process and structure.

123. In particular, Costa forms a first channel structure (“epitaxial channel portion 11”) overlaying the surface of the substrate (“substrate 10”) that is exposed by the first through hole (“first-tier memory opening” 149). Costa, [0143].

124. More particularly, an “epitaxial channel portion (*e.g.*, an epitaxial pedestal) 11 can be formed at the bottom portion of each first-tier memory opening 149....” Costa, [0143]; *see also id.*, [0137] (“substrate” includes portions 9 and 10).

125. As shown in Figure 4B below, Costa's epitaxial channel portion 11 overlays the surface of the substrate 10 that is exposed by the first-tier memory opening 149:



Costa, Fig. 4B (annotated).

[1.D] “forming a second channel structure in the first through hole and in contact with the first channel structure;”

126. This, in my opinion, is taught by Costa.

127. The '532 patent claims “form[ing a second channel structure] on the sidewall of the first functional layer and the exposed surface of the first channel structure 6.” Ex. 1001, 11:21-40; *see also id.*, Figs. 5-6, 11:41-12:19 (describing process of removing portions of second channel layer 11), Figs. 7A-8B.

128. In the '532 patent, the second channel structure can be comprised of amorphous silicon. Ex. 1001, 19:34-37. Said differently, the second channel structure is, e.g., the semiconductive layer of the channel structure.

129. This is shown in Figure 10B:

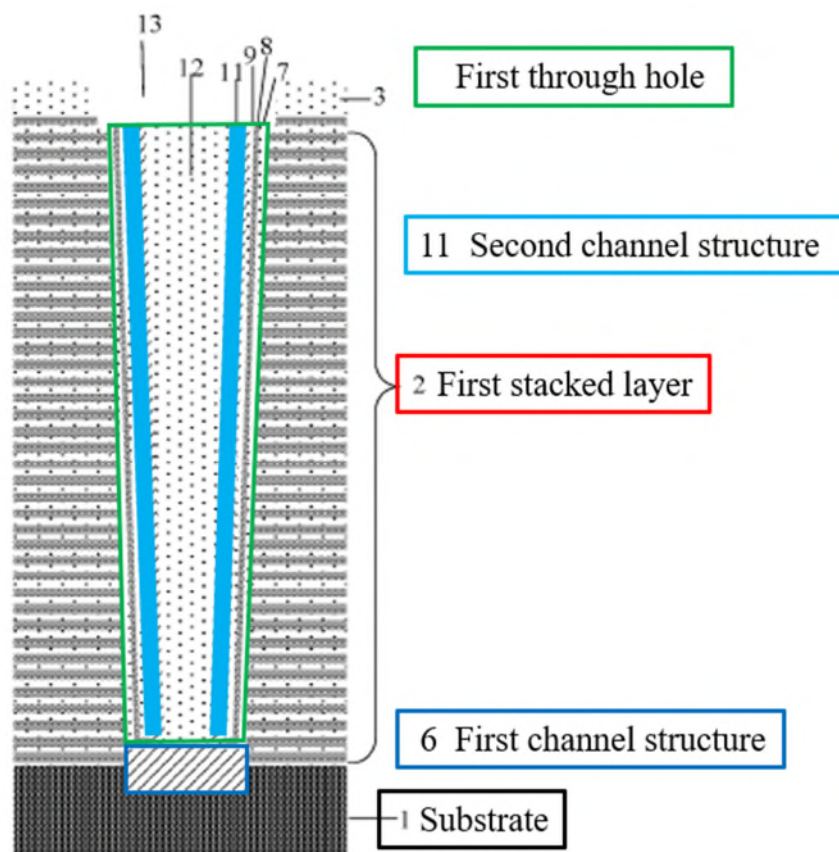


FIG. 10B

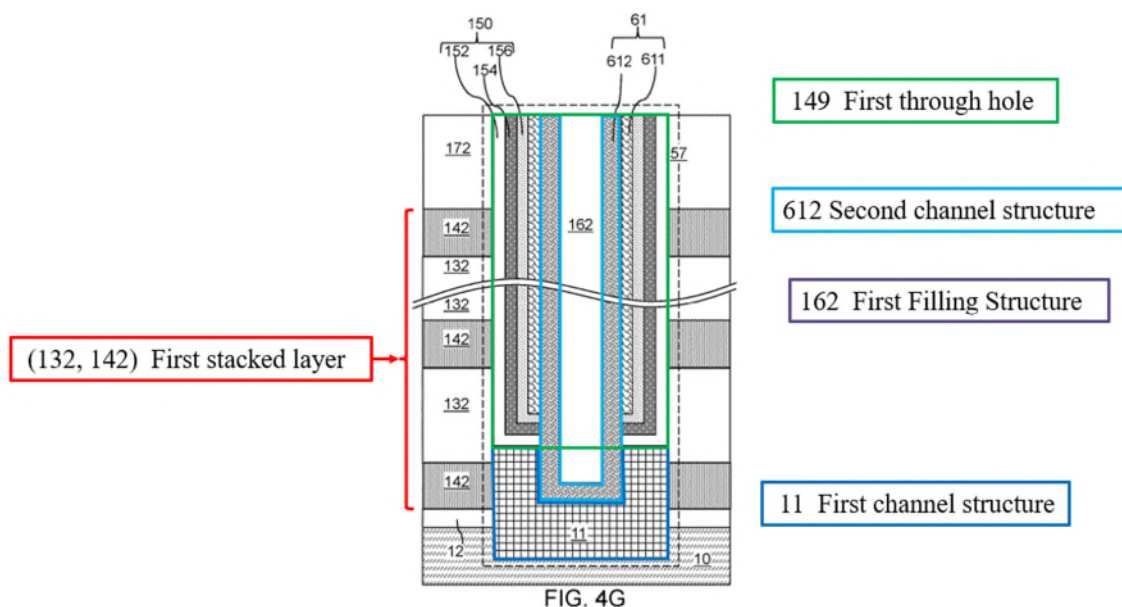
Ex. 1001, Fig. 10B (annotated).

130. In my opinion, Costa teaches this same process and structure.

131. Costa discloses forming a second channel structure (“first inner semiconductor channel layer 612”) in the first through hole (“first-tier memory opening[]” 149). The “outer semiconductor channel layer 611,” shown below, is optional. Costa, [0144].

132. Costa discloses that “a first inner semiconductor channel layer 612 can be deposited directly on the semiconductor surface of the epitaxial channel portion

11 ... and directly on the [optional] first outer semiconductor channel layer 611.” Costa, [0156]. In other words, first inner semiconductor channel layer 612 is formed in first-tier memory opening 149.. The 611 and 612 layers are “amorphous silicon or polysilicon.” *Id.*, [0152], [0156]. “The materials of the first outer semiconductor channel layer 611 and the first inner semiconductor channel layer 612 are collectively referred to as a first semiconductor channel material.” *Id.*, [0157].



Id., Fig. 4G (annotated).

[1.E] “forming a third channel structure above the first through hole and in contact with the second channel structure, wherein a size of the third channel structure along a lateral direction is larger than a top aperture of the first through hole;”

133. This, in my opinion, is taught by Costa or is at least rendered obvious in view of the knowledge of a POSITA.

134. The '532 patent claims forming the claimed third channel structure in a groove 13 formed in the first insulating connection layer 3. Ex. 1001, 12:31-36, 12:55-56.

135. “[T]he third channel structure can be a polycrystalline silicon [l]ayer formed by using a deposition process.” Ex. 1001, 12:58-60. “[T]he projection of the first groove [13] on the substrate 1 can completely cover the projection of the first through hole 5 on the substrate 1” or, in other embodiments, “[a]n area of the projection ‘x’ of the first groove on the substrate 1 can be larger than an area of the projection ‘y’ of the first through hole 5 on the substrate 1.” *Id.*, 12:21-23, 12:34-36.

136. This third channel structure 14 is illustrated in Figure 11B below:

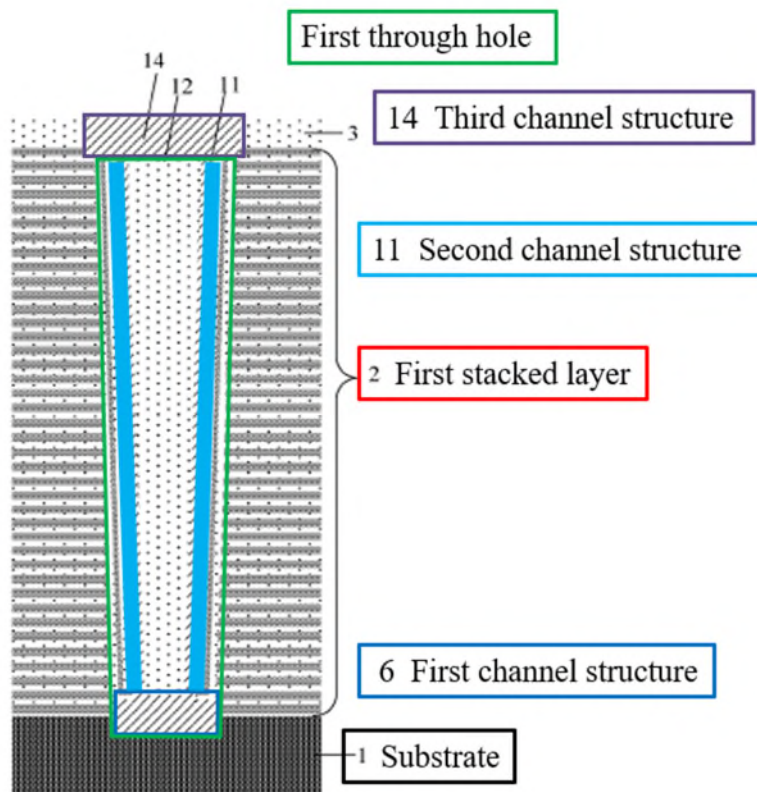


FIG. 11B

Ex. 1001, Fig. 11B (annotated).

137. In my opinion, Costa teaches this same process and structure or at least renders it obvious in view of the knowledge of a POSITA.

138. Costa states that the third channel structure (“joint-level doped semiconductor portion 173”) above the first through hole (“first-tier memory opening 149”) completely covers the underlying first memory opening fill structure 57 to protect that structure. Costa, [0265]. A POSITA would have understood (and certainly found obvious) this to mean that the third channel structure in Costa is wider than the underlying first through hole to account for margin. As a result, a

size of the third channel structure along a lateral direction would be larger than a top aperture of the first through hole (“first-tier memory opening 149”) on the substrate. As result, even if the third channel structure is not perfectly aligned over the underlying channel structure, it would still completely cover the underlying first memory opening fill structure 57 because of margin from it being wider than the fill structure 57. This understood margin is consistent with Costa’s Figure 20B that I discuss further below.

139. Costa’s “third exemplary structure” modifies the “first exemplary structure” by modifying the interface between the two tiers, and applies that modification to the remaining claim limitations. Costa, [0263]. More specifically, before Costa’s optional oxidation step in both embodiments, Costa’s “third exemplary structure” changes the interface between the two memory decks, including structure 173:

First Exemplary
Structure

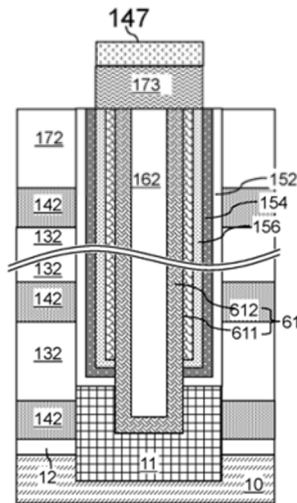


FIG. 6B

Third Exemplary
Structure

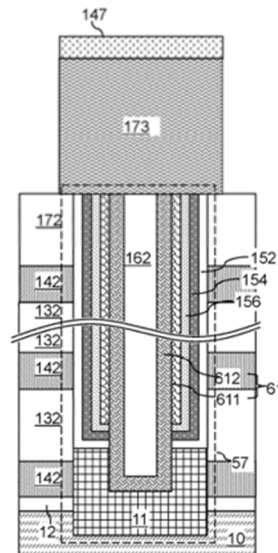


FIG. 20B

Costa, Figs. 6B, 20B (annotated). I will use this third embodiment for the rest the claim mapping.

140. Costa discloses depositing “joint-level doped semiconductor layer 173L” over the first tier structure (i.e., over first insulating cap layer 172). Costa, [0265], Fig. 20A. Costa discloses patterning and subsequent etching on layer 173L to form joint-level doped semiconductor portion 173 that “covers and protects the underlying first vertical semiconductor channel 61 from oxidation during a subsequent oxidation process.” *Id.*, [0265], Figs. 20A-B. The mask defines the width of portion 173 because it defines etch pattern.

141. Unlike the earlier embodiment (see Fig. 6B-C) Costa discloses: “In one embodiment, the bottom surface of each joint-level doped semiconductor portion

173 can contact an entire top surface of an underlying first memory opening fill structure 57.” Costa, [0265]. However, as shown below, Costa depicts joint-level doped semiconductor portion 173 to not only cover the entire first-tier memory opening 149 (i.e., a projection of 173 on the substrate covers a projection of 149 on the substrate), but depicts the structure to be wider than the first-tier memory opening.

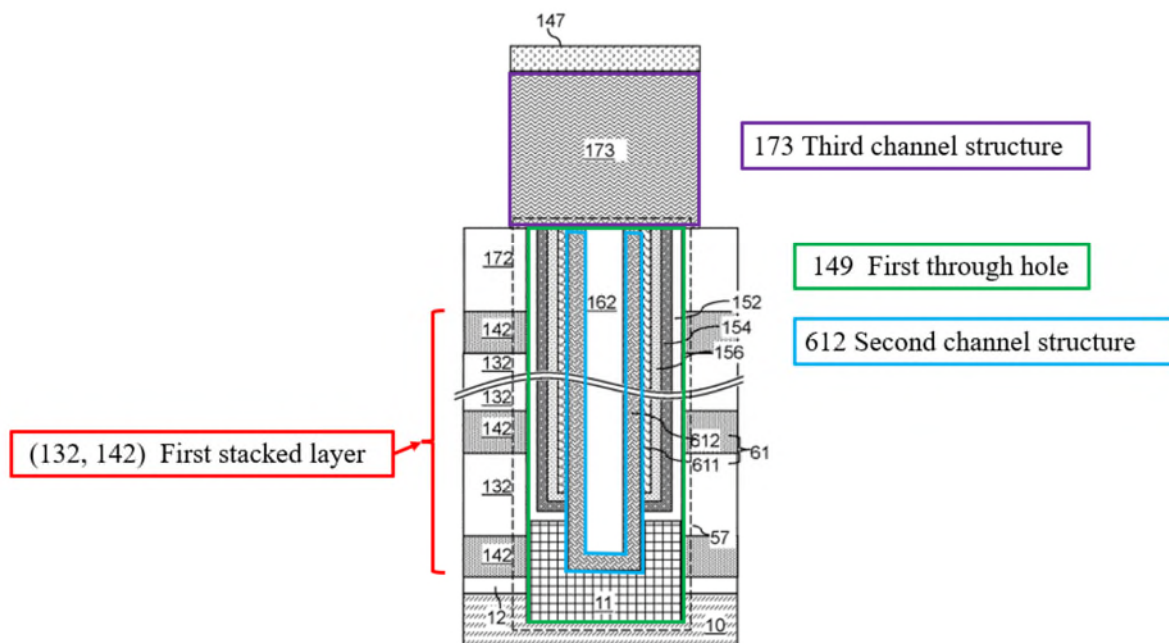
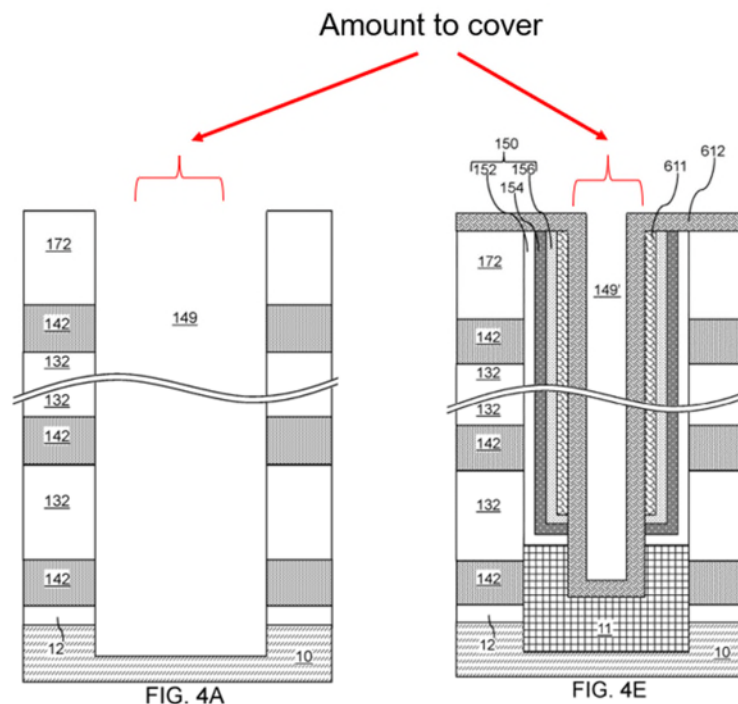


FIG. 20B

Id., Fig. 20B (annotated).

142. A POSITA would have understood that Costa is depicting margin in Figure 20B. In other words, even if structure 173 doesn’t perfectly align over the fill structure 57, it will still completely cover the fill structure 57. In another embodiment, Costa recognizes the need “to account for misalignment” when

forming a channel interface structure over the first channel structure. Costa, [0164]. In that embodiment, Costa's goal was to ensure contact of structure 173 and the through-hole channel material. But to realize this goal, Costa teaches that structure 173 should be made wider than the width of 149', because then structure 173 will contact layer 612 even if the alignment is not perfect. *Id.* ("The width (e.g., diameter) of the doped semiconductor portion 173 can be smaller than that of the first memory opening 149 (e.g., 20-25 nm smaller than a 100 nm first memory opening 149) but larger than that of the first memory cavity 149' (e.g., about 20 nm larger than a 60 nm first memory cavity 149') to account for misalignment of the layers (e.g., about 10 nm misalignment).").



Costa, Figs. 4A, E (annotated). Thus, Costa recognizes that when the desire is to only ensure contact of structure 173 and the through-hole channel material (layer 612), the structure 173 must be made wider than the width of 149' to ensure contact with layer 612 (e.g., as shown above, if 173 had a width less than 149', it may not contact 612).

143. Applying this well-known principle (accounting for misalignment) to Costa's third exemplary structure, a POSITA would have understood that structure 173 would be made wider than the underlying fill structure.

144. In Figure 20C, Costa discloses a step that oxidizes and forms 174'. Costa discloses that this step is optional. Costa, [0266], [0268] (referring to '174 portions and noting "if present"). The third channel structure below would be

FIG. 20C

147

173

174

173 Third channel structure

174'

173

149 First through hole

172

142

132

132

142

132

142

162

152

154

156

612 Second channel structure

612

611

61

(132, 142) First stacked layer

11

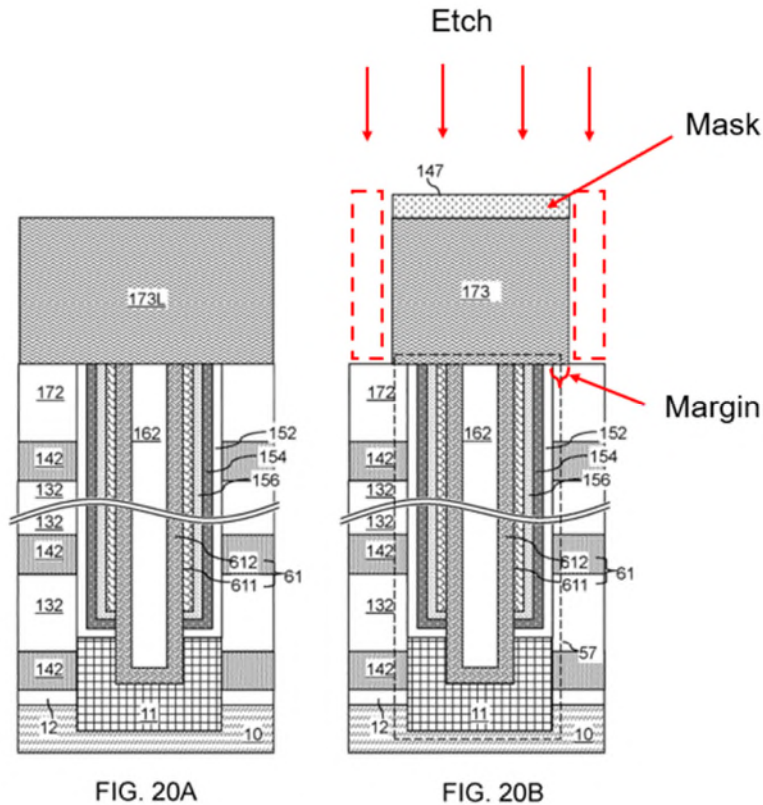
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10

145. A POSITA would have understood Costa's description to confirm that the third channel structure 173 would be wider than the top aperture of fill structure 57 (first hole) because of the understood margin that would apply in its design (consistent with Figure 20B), even with the optional oxidation step. Costa discloses that the third channel structure 173 "can contact an entire top surface of an underlying first memory opening fill structure 57." Costa, [0265]. This is because Costa teaches that structure 173 protects for the lower deck channel structure during

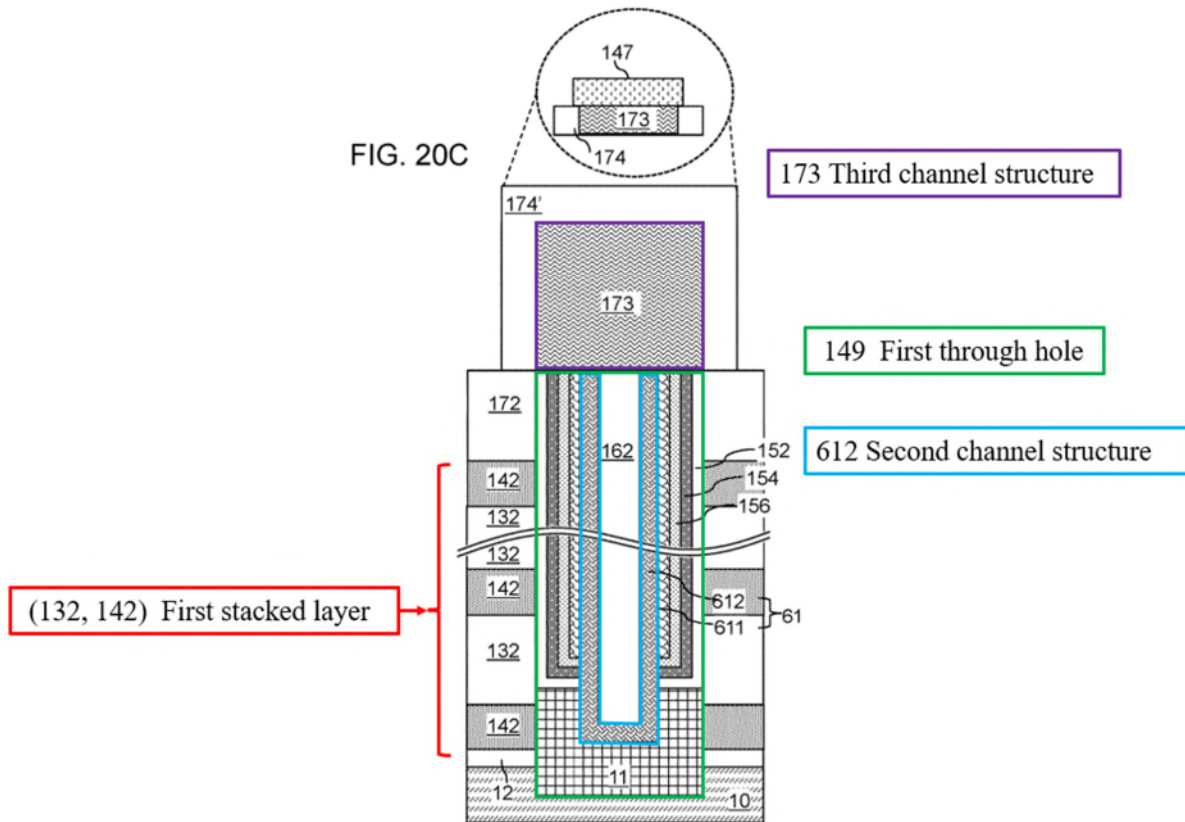
processing. *Id.* Subsequent processing, e.g., forming the oxidation portions or other isolation techniques, may inadvertently damage the fill structure. The third channel structure, however, effectively provides a barrier of the fill structure to protect it. This is in contrast to Costa's earlier embodiment (see Fig. 6B-C) and the additional protection would have been understood to be an improvement.

146. But Costa does not provide a self-aligned technique to forming channel structure 173 or the overlying channel structure on channel structure 173. For example, Costa masks the top of 173L (with 147) to remove portions of 173L, ultimately forming channel structures 173 over respective lower channel structures. Costa, [0265], Figs. 20A, B. An etch will remove portions of 173L that do not include an overlying mask. As can be seen below, Costa depicts the mask being wider than the entire fill structure 57. Semiconductor processing involves patterns on reticles and perfectly aligning those reticles to perfectly replicate a pattern on a wafer is incredibly challenging. Series of reticles and process steps ultimately form the semiconductor patterns. As a result of potential misalignment, it was the normal to provide margin when forming structures. Applying that here, Costa depicts the mask, which defines the width of fill structure 173, being wider than the fill structure:



Id., Figs. 20A, B (annotated). The result is a semiconductor structure that is wider than the fill structure. But this accounts for process variations and misalignment. While the medium case would be as shown in Figure 20B above, from wafer to wafer (even substrate to substrate), there may be some misalignment. The additional width accounts for those variations, so that even with these variations, semiconductor structure 173 will fully cover the fill structure.

147. Also recall that Costa discloses an embodiment that uses an additional oxidation step. Costa, [0266].



Id., Fig. 20C (annotated). A POSITA would have understood that providing for margin in this embodiment would be important as well. The oxidation renders the semiconductor material into an oxide, that is, non-conductive. Were the oxidation process to start to oxide semiconductor materials in the channel fill structure, it would negatively its function (and possibly render it defective), because that fill structure must ultimately function as a channel. In addition, as I discuss below, inadvertent oxidization may damage other portions of the memory fill structure. Thus, a POSITA, even in this embodiment, would have understood that it was important and advantageous to account for margin in the oxidation process as well.

148. In my opinion, a POSITA would have found it obvious to apply a margin to the width of semiconductor portion 173, such that it is wider than the top aperture of the first through hole, to ensure that it fully covers the underlying fill structure. Costa teaches expressly teaches that one purpose of doped semiconductor portion 173 is to “protect[] the underlying first vertical semiconductor channel 61 from oxidation during a subsequent oxidation process.” Costa, [0265]. Thus, Costa discloses forming portion 173 to “contact an entire top surface of an underlying first memory opening fill structure 57.” *Id.* That is, to perform this protection function, it fully covers the fill structure. However, as I discuss above and below, perfectly aligning structure 173 of the fill structure is challenging. Thus, it would have been obvious to simply make the fill structure 173 wider than the fill structure, such that even if not perfectly aligned, structure 173 will still fully cover the fill structure.

149. I also note that a POSITA understood that it is beneficial to protect the entire fill structure, not just the vertical channel layer (as in Costa’s earlier embodiment of Fig. 6C). By way of example, U.S. Pat. No. 9,401,371 discloses a sacrificial dielectric material such that subsequent processing removes “a very minimal amount of the oxide of the memory layer” that includes “a tunneling layer 1132, the charge storage layer 1131, and the blocking layer 1130.” Ex. 1019, 16:60-17:14. In other words, the goal here was to preserve the structure of the memory layer. By way of another example, U.S. Pat. No. 9,570,460 discloses a “cover layer”

that protects “memory film 7, 9, 11” during subsequent processing, i.e., the blocking layer, tunneling layer, and charge storage layer. Ex. 1020, 11:22-40. Again, the goal here was to preserve the structure of the memory film.

150. It is imperative to protect the entire NAND memory string structure, including the topmost layer. Assuming *arguendo* that just the very top cell was damaged due to misalignment and overetch. It would mean that the rest of the string would be compromised because all the cells are in series. During READ or WRITE, one must apply a PASS voltage to all the cells, except the one that is being READ or written into. A defective cell at the top would not allow the READ or WRITE voltages be applied properly to the rest of the cells. What is worse is that if this were due to misalignment of the top stack and overetch, this failure mechanism would apply to all the cells. One cannot use the redundancy of rows or columns to overcome this problem.

151. As to Costa, Costa’s fill structure may comprise a variety of different material compositions, e.g., the blocking layer may be metal oxide, silicon nitride, or a combination of silicon oxynitride and silicon nitride and the charge storage layer may be titanium or semiconductor material (floating gate) or silicon nitride (charge trap layer). *E.g.*, Costa, [0145]-[0147], [0150]. These layers (and horizontally adjacent layers of the stack) are subject to damage during subsequent processing

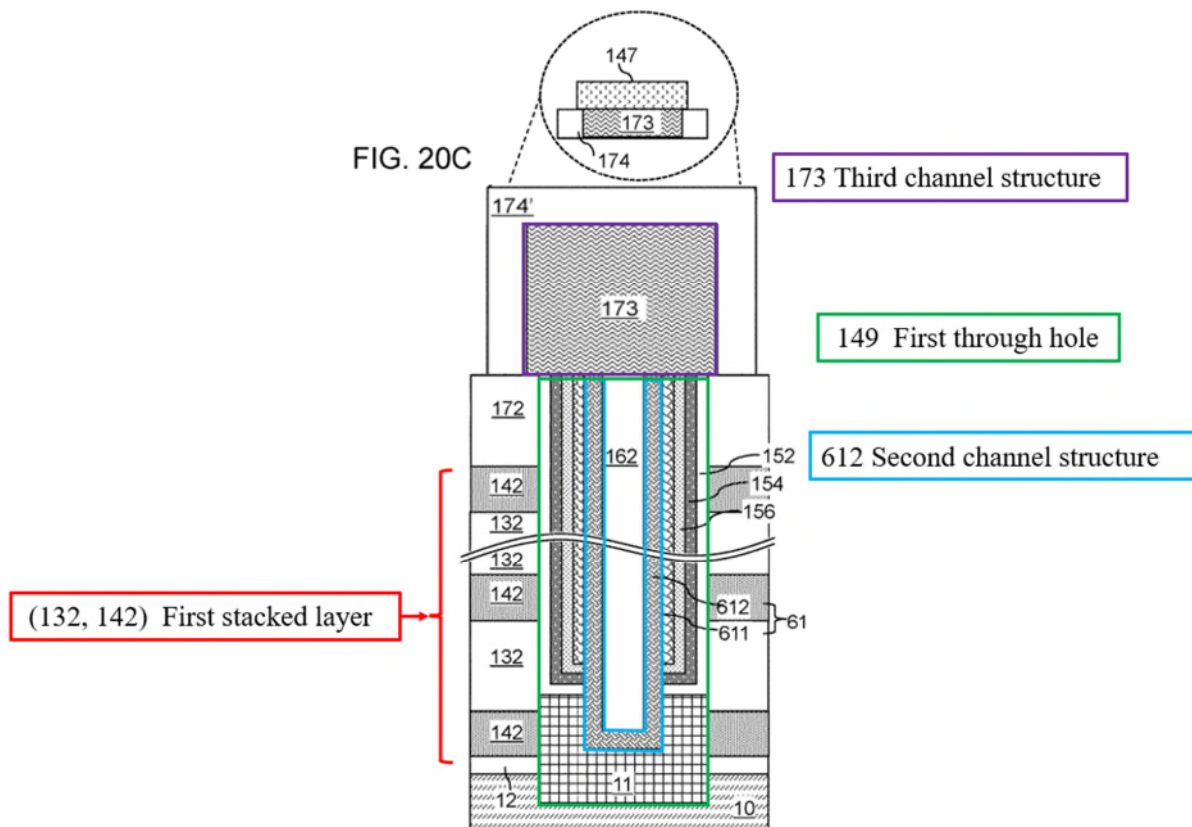
during the optional oxidation step and etch to form overlying second through hole. Depending on the layer composition, different oxidation concerns will be present.

152. Controlling the extent of oxidation of a material, e.g., the depth of oxidation, has been an area of study for decades before the filing of the '532 Patent. And for processes that involve oxidation, consideration must be given to ensure that inadvertent oxidation does not occur. For example, when oxidizing a given material, e.g., polysilicon, "other material" may be "unintentionally oxidized." Ex. 1021, 12:37-46.

153. Applying this knowledge to Costa, a POSITA would have understood that inadvertently oxidizing the blocking layer may have deleterious effects. For example, if the memory design assumes a dielectric constant for the blocking layer, inadvertent oxidizing the blocking layer may change this constant. Also, it would lead to a thickness increase, leading to a decrease of the coupling capacitance between the storage node to the channel and to the wordline. This would lead to different programming conditions of the cell, and lead to malfunction. More problematic would be inadvertently oxidizing the charge storage layer. Take the example of a silicon nitride charge trap layer. Oxidizing this layer, for example, would impact its ability to trap charge.

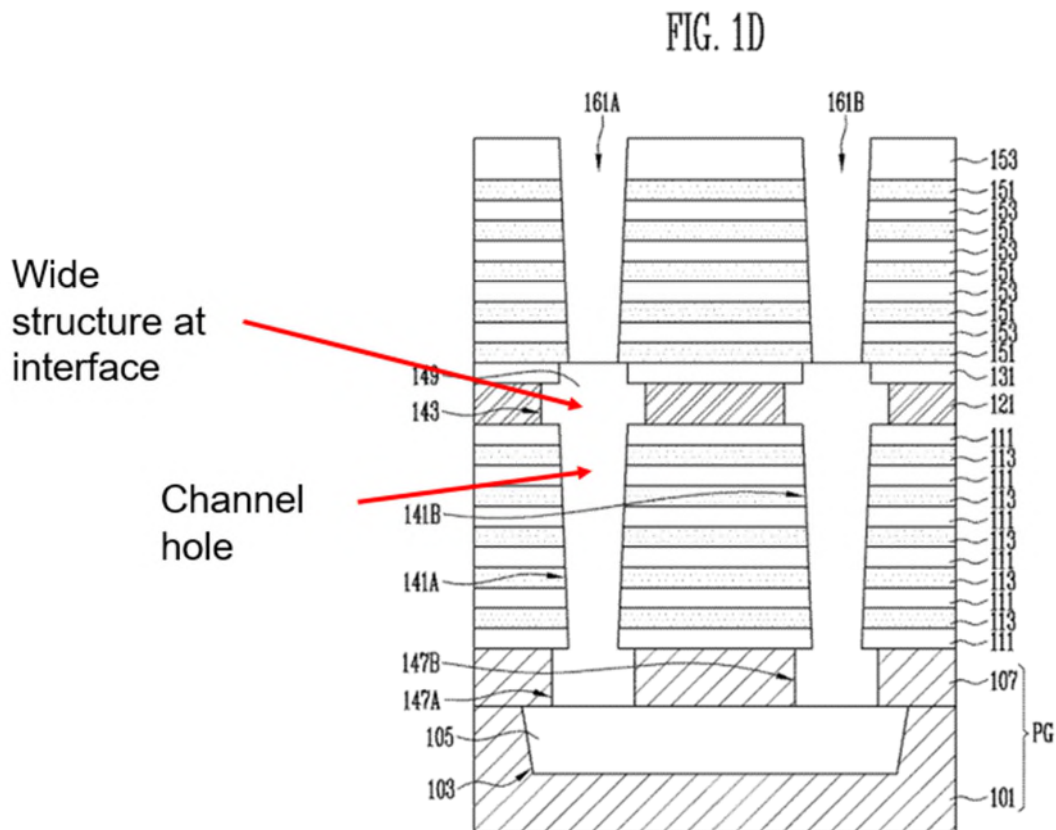
154. A POSITA would have understood unlike Costa's earlier embodiment that does not intend to cover the entire fill structure, Costa's embodiment of Figure 20 provides additional protection to the issues above.

155. Thus, in light of these consideration, a POSITA would have been motivated to form Costa's third channel structure wider than the fill structure, such that after oxidation, oxidation did not occur near (e.g., over) any part of the fill structure, thereby ensuring that inadvertent oxidation does not impact any structures of the memory fill portion:



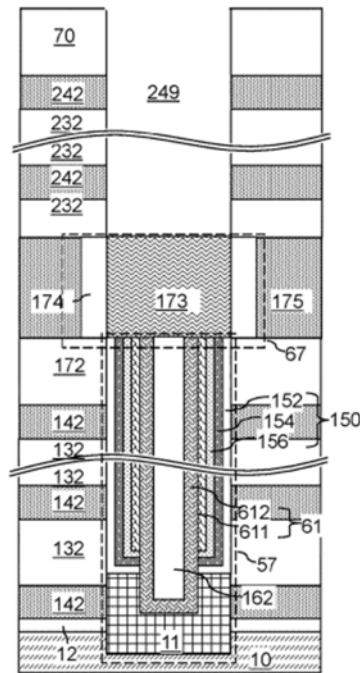
Costa, Fig. 20C (modified and annotated).

156. Importantly, it was also known that an interface structure between two decks may provide protection for the underlying layers during etching of the second through hole (through the top deck, such that the etch terminates on the interface structure). Yoon teaches a sacrificial interface structure for this purpose: “In addition, according to the first embodiment of the present invention, since the overlay margins between the second through-areas 161A and 161B and the first through-areas 141A and 141B may be enlarged, damage of the first and second material layers 111 and 113 around the first through-areas 141A and 141B due to the etching process for forming the second through- areas 161A and 161B may be prevented.” Ex. 1007, [0037]. As can be seen below, the wide structure over the underlying channel hole protects everything under 149 even if the etch to form hole 161A does not perfectly align above the underlying hole:



Ex. 1007, Fig. 1D (annotated).

157. Applying this knowledge to Costa, first note that Costa discloses an anisotropic etch that is selective towards alternating stack layers 232/242 and dielectric material portion 265. Costa, [0193]. These layers and dielectric portion may comprise, e.g., silicon oxide and silicon nitride. *Id.*, [0181]. If the third channel structure is the same width of the underlying fill structure, the etch that forms the overlying memory hole must perfectly align or the etch would not terminate on structure 173 (e.g., shifting 249 to left slightly exposes 174’):

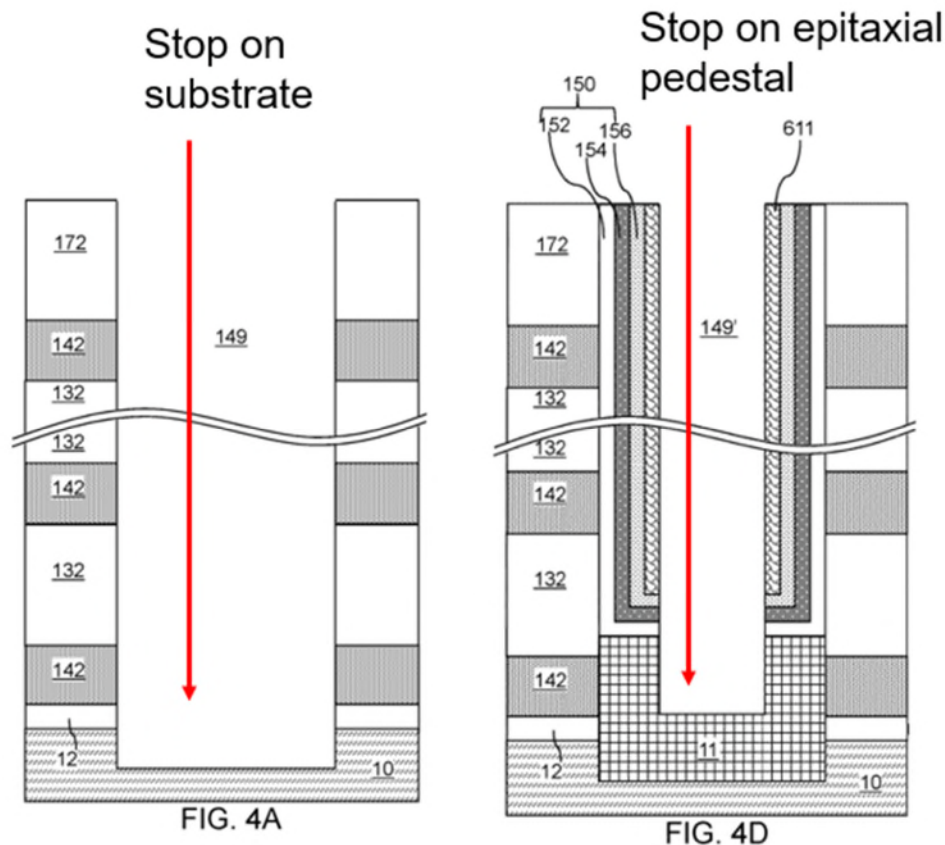


Id., Fig. 21A. Put simply, in Costa's optional oxidation step, even a slight misalignment would lead to etching annular spacer 174.

158. If the etch selectivity ratio results in significantly etching oxide, however, the etch would quickly etch 174 and risk damage to underlying layers. But employing a wide interface structure 173 prevent this, because even with a little misalignment, the etch will terminate on 173. Structure 173 serves as an etch stop and the etch will slow down at 173. A comparison of Costa's earlier embodiment demonstrates that employing a wide 173 simplifies the etch process for the second through hole. In Costa's earlier embodiment, Costa discloses a series of selective etches. Costa, [0171], Figs. 6F-G. This is because Costa recognizes that the final etch chemistry will also contact 174' (if present) in the earlier embodiment. Thus, a

series of different etch chemistries is necessary to avoid employing an etch that is selective towards 174’.

159. That Costa is using structure 173 as an etch stop is consistent with other Costa’s etches. When forming the first through hole, Costa teaches using substrate 9/10 as the “stopping layer” for the anisotropic etch that form the first through hole. Costa, [0139]. Similarly, Costa discloses anisotropic etches that are selective towards the memory fill portions, which stop on the epitaxial pedestal (11), when removing the horizontal portions of the fill layers above epitaxial pedestal. *Id.*, [0153]. Costa is recognizing the problems with using an etch chemistry that is not selective towards semiconductor material for these etches and the etch stopping on polysilicon. This same technique is seen when Costa is disclosing the wider version of interface structure 173.

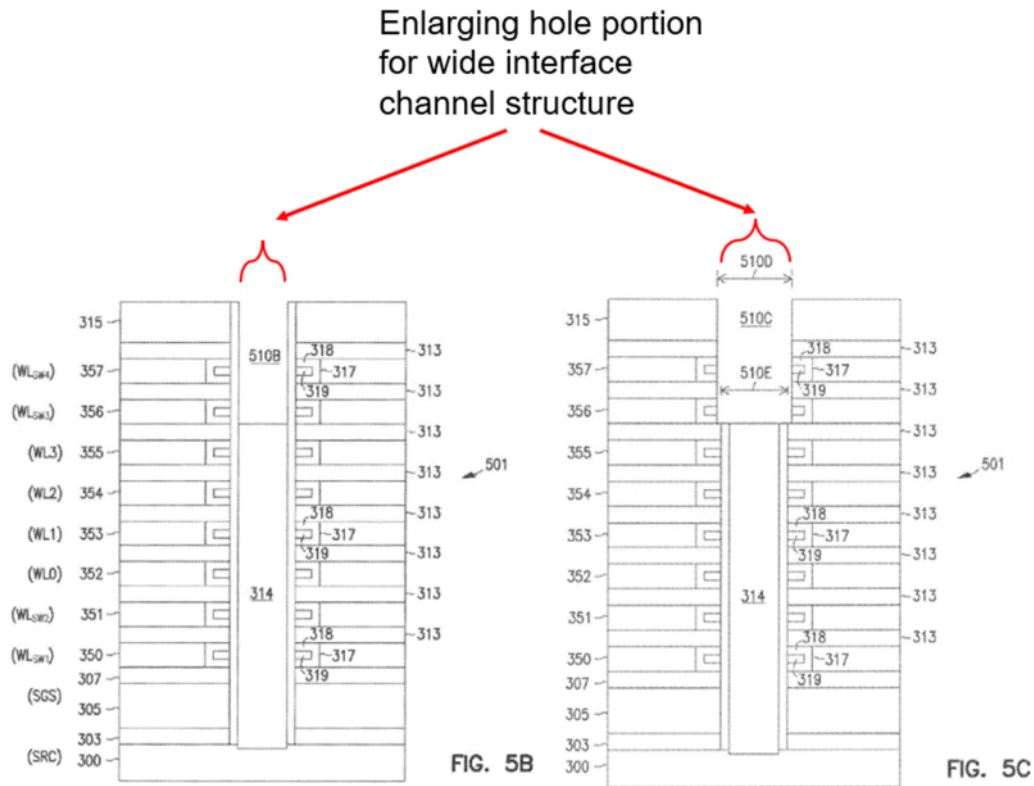


Id., Figs. 4A (annotated), 4D (annotated).

160. I describe above that Costa's process is not self-aligned. It was textbook material that these processes result in misalignment issues. *E.g.*, Ex. 1014, 2:60-3:6 (noting process variation issues in non-self-aligned processes); Ex. 1015, 20-21. In simple terms, this means that if the goal and design is for the middle of the channel structure to be over the middle of the fill structure, the actual fabricated products may result in variance in which some of the fabricated structures 173 are not perfectly aligned over the middle. A simple way to view this is that a structure may have an intended "landing" structure or target. When that structure is fabricated, perfecting aligning it on the landing target is difficult. As a result, it was

well known to simply make that landing area wider. *E.g.*, Ex. 1016, [0023] (“The lateral extension portion (135) may have a larger cross-sectional area than the first and second semiconductor pillars (130a, 130b) based on a cross section parallel to the substrate (105).”), [0086] (“[B]y arranging the lateral extension portion (135) between the first semiconductor pillar (130a) and the second semiconductor pillar (130b), the alignment margin is increased when the second through holes (120b) are formed....”); Ex. 1017, [0058] (“[M]emory opening alignment challenges may be reduced or avoided by adding a landing pad between the memory stack portions [that is] is wider (e.g., had a larger diameter) than the channel in the horizontal direction.”).

161. Accounting for margin was specifically known in the context of interface structure between channel structure in a multi-deck structure. Oh, for example, discloses interface structure 180A:



Ex. 1018, Fig. 5B, C (annotated), [0118]-[0119] (“Enlarged hole portion 510C can have a diameter 510D that is greater than a diameter 510E (e.g., a diameter of an un-enlarged portion of hole 510). The value of diameter 510D can be selected based on an alignment margin for forming a conducting channel in an additional deck (e.g., similar to deck 302 in FIG. 3S) directly over enlarged hole portion 510C.”). As can be seen above, in one embodiment, Lu makes the interface wider, providing the same benefit that Oh teaches.

163. Yoon discloses a similar technique:

This diagram shows a cross-sectional view of a semiconductor device. It features a central channel hole (141B) and a margin at the interface (149). The device includes a substrate (101) with a trench (103) and a gate structure (105). The channel hole is defined by a gate (147A) and a gate (147B). The margin at the interface is indicated by a red arrow pointing to the region between the gate and the channel. The channel hole is labeled 141B, and the margin at the interface is labeled 149. The device also includes a gate (141A) and a gate (141B). The channel hole is defined by a gate (147A) and a gate (147B). The margin at the interface is indicated by a red arrow pointing to the region between the gate and the channel. The channel hole is labeled 141B, and the margin at the interface is labeled 149. The device also includes a gate (141A) and a gate (141B).

164. Making the third channel structure wider increases the “alignment margin” (Ex. 1016, [0086]), i.e., provides an “overlap margin” (Oh [0061]). This

means that even if not perfectly aligned, the structures will still overlap. Put another way, there is “margin” in the process for aligning the structures, such that the correct electrical coupling will occur despite potential misalignment. The result of applying these margin techniques is that “memory opening alignment challenges may be reduced or avoided.” Ex. 1017, [0058]. For example, this lessens the degree of accuracy that the third channel structure must be formed over the middle of the underlying channel structure and the degree of accuracy that the upper channel structure must be formed on the third channel structure (effectively, where it must land). Applying this margin was known to simplify the forming of the upper and lower channels. Ex. 1007, [0037]-[0038] (margin allows for channel structures to “be easily connected”); Oh, [0061] (“[C]hannel connection pattern 180A may have an island shape which overlaps the first channel holes CH1 ... [T]o secure an overlap margin between the channel connection pattern 180A and the first channel hole CH1).

165. If misalignment results in the channel structures not electrically coupling, the memory channel will be non-functional. For many decades, it has been standard to include redundant memory cells or channel structures to account for defective memory cells or channel structures. But if there are too many defects, the entire device is considered defective, e.g., the device does not have a pre-defined memory capacity. These devices are then not sold. The percentage of good or

salable devices is known as the yield. In short, providing overlap margin for structures that are subject to misalignment increases yield, because it reduces the defective components. Yield is very important, because fabs are typically run nearly 24 hours a day, 7 days a week. The sellable output therefore is driven by process time and yield. Increasing yield increase the sellable output and directly correlates to profitability.

166. In my opinion, a POSITA would have had a high expectation of success in providing this overlap margin for several reasons.

167. First, providing margin is a standard, advantageous practice in semiconductor fabrication. A POSITA readily understood for any process design that is not self-aligned, misalignment issues must be considered. And margin, for example, may be as simple as designing a structure wider by a certain percentage than what its minimum, functional width must be. Semiconductor processes for forming channels, e.g., an anisotropic etch through a stack, were well known, and as a result, the associated margin that should be provided were also understood by a POSITA.

168. Second, as I discuss above, Costa already recognizes that alignment issues may occur with its process. Naturally, Costa accounts for this by making channel structure wider than its target width in those embodiments, as shown in the annotations to Costa's Figures 20A-B above. A POSITA would have understood

this simply involves making the mask that defines the width of channel structure 173 wider.

169. Third, applying a margin simplifies the overall fabrication process. This is because it eases how precise other steps must be. Take for example the etch to form the overlying channel (top) structure. If that channel structure must be perfectly aligned over channel structure 173, that etch step would have no margin for error, requiring perfect alignment for the corresponding mask.

170. I also note that Patent Owner might argue that Costa fails to meet this limitation because Costa's joint-level doped semiconductor portion 173 is not formed in a groove of the first insulating cap layer 172. This would be incorrect for at least two reasons. First, the claim language includes no such requirement. And second, to import such a requirement would render Claim 7 superfluous. *See* Ex. 1001, Claim 7 (describing forming the third channel structure by "forming a first insulating connection layer" and depositing the third channel structure in a "groove" formed in the connection layer).

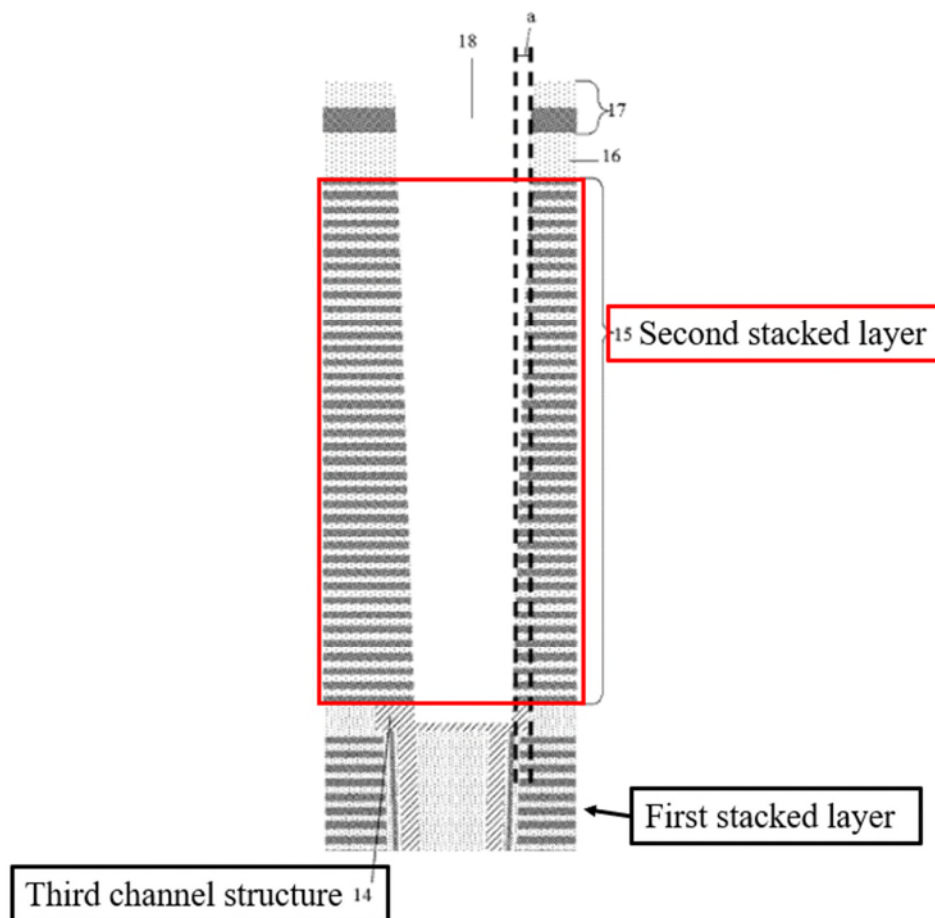
[1.F] "forming a second stacked layer over the third channel structure;"

171. This, in my opinion, is taught by Costa.

172. According to the '532 patent, "a second stacked layer 15 ... can be ... formed on the third channel structure 14 [and] can include a plurality of oxide/nitride

layer pairs, such as silicon oxide layer and silicon nitride layer pairs.” Ex. 1001, 13:7-20, Fig. 12.

173. This is shown in Figure 13 below:



Id., Fig. 13 (annotated).

174. This is what Costa teaches. Specifically, Costa forms a second stacked layer (“second alternating stack” 232, 242) over the third channel structure (“joint-level doped semiconductor portion 173”).

175. As shown in Figure 21A below, “second alternating stack (232, 242) of material layers is subsequently formed on the top surface of the joint-level material layers....” Costa, [0178] (describing the process of Figs. 8A-B), [0270] (referring to “the processing steps of” Figs. 7A-10B using the third exemplary structure’s single joint-level doped semiconductor portion 173), [0263], Figs. 8A-B, Fig. 21A. In this way, second alternating stack (232, 242) is formed “on” doped semiconductor portion 173. This is shown in Figure 21A below:

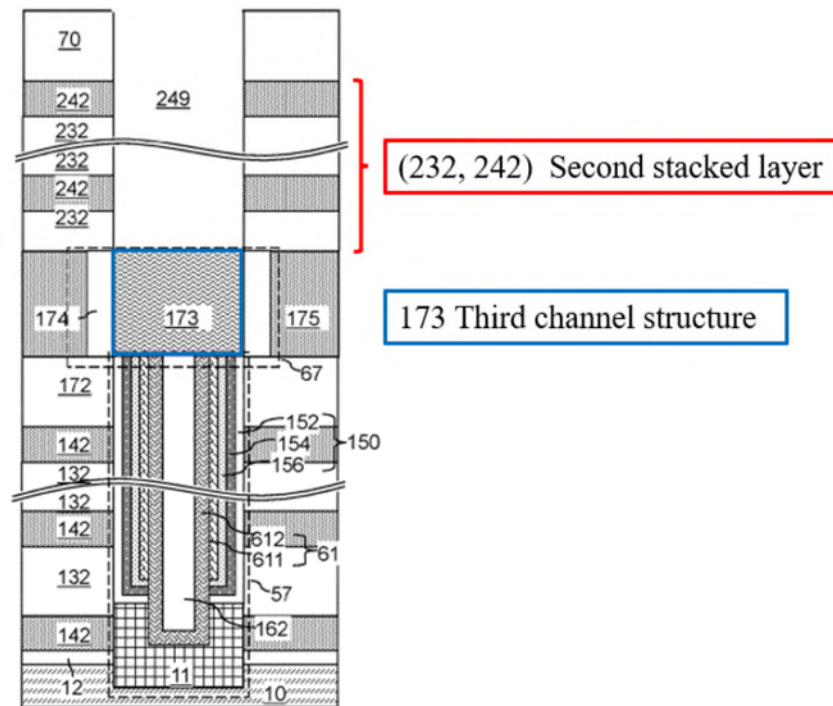


FIG. 21A

Costa, Fig. 21A (annotated).

[1.G] “forming a second through hole penetrating the second stacked layer to expose the third channel structure;”

176. This, in my opinion, is taught by Costa or is at least rendered obvious in view of the knowledge of a POSITA.

177. In the '532 patent, the second through hole is formed similarly to the first through hole: “[A] second through hole 18 is formed [that] can completely penetrate the second stacked layer 15 ..., and can extend into the surface of the third channel structure 14.” Ex. 1001, 13:33-49.

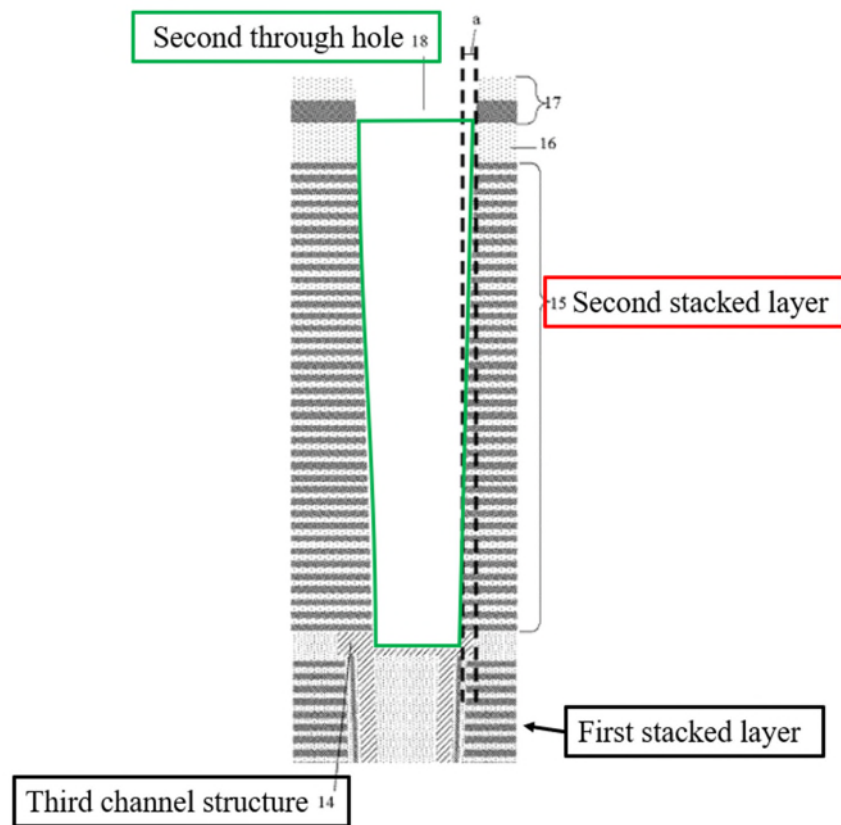


FIG. 13

Id., Fig. 13 (annotated).

178. One could also map the top of the “second through hole” to the topmost layer of the second stacked layer 15 as shown in Figure 13. Claim 1 recites “a second through hole penetrating the second stacked layer to expose the third channel structure.” Regardless of how one defines the “second through hole,” Costa discloses these limitations, as I explain below in limitation [1.I] when addressing both interpretations. Simply stated, the second through hole may either include the portion of the hole that extends through connection layer 16 or not.

179. This is what Costa teaches. Specifically, Costa discloses that after forming the second alternating stack (232, 242), “second-tier memory opening[] 249 ... are formed” “through the second tier structure (232, 242, 265, 70).” Costa, [0190], [0192] (“second-tier openings (249, 210) can be formed by a combination of lithographic patterning and an anisotropic etch”). As shown in Figure 21A below, second-tier memory opening 249 penetrates the second stacked layer (second alternating stack (232, 242)) and exposes the third channel structure (doped semiconductor portion 173):

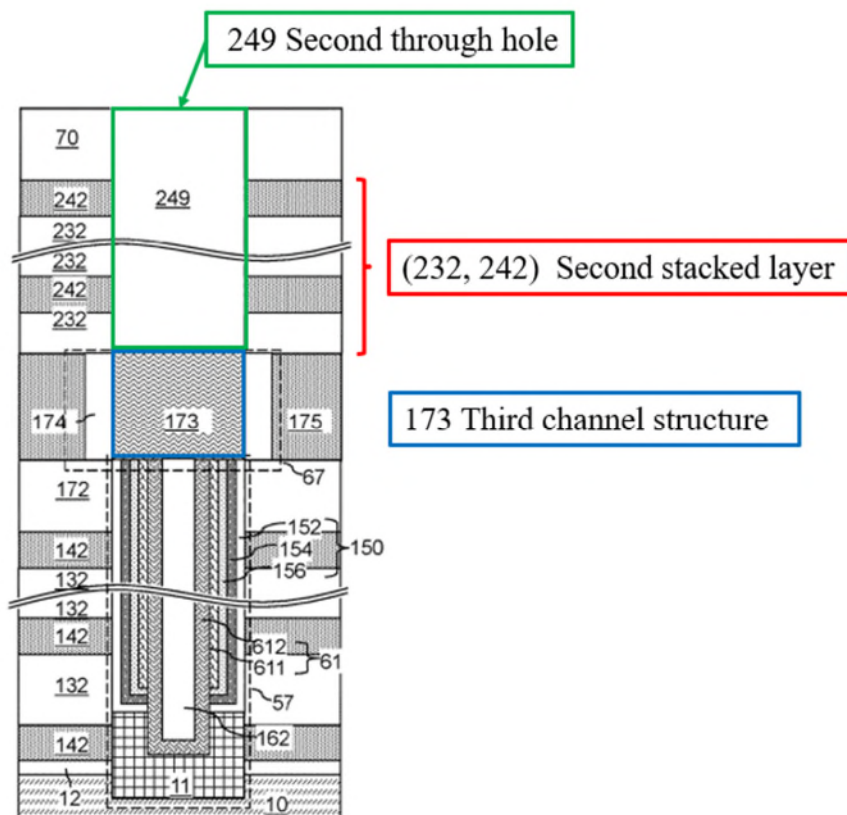


FIG. 21A

Id., Fig. 21A (annotated). As I discuss in the final limitation, the “second through hole” also maps to the hole portion through the second stack (232/242 layers) as well.

[1.H] “forming a fourth channel structure in the second through hole and in contact with the third channel structure; and”

180. This, in my opinion, is taught by Costa.

181. In the '532 patent, a fourth channel structure is formed in the second through hole, in much the same manner as that of the second channel structure, as shown in Figure 19 below. Ex. 1001, 14:39-42, Figs. 16-19.

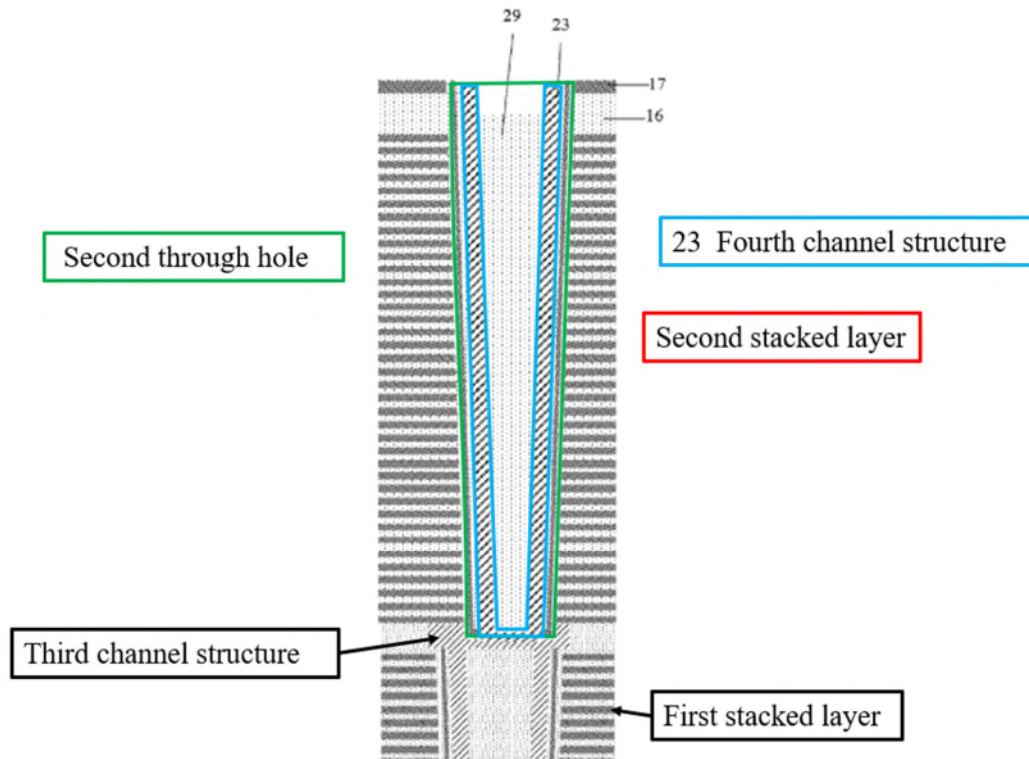


FIG. 19

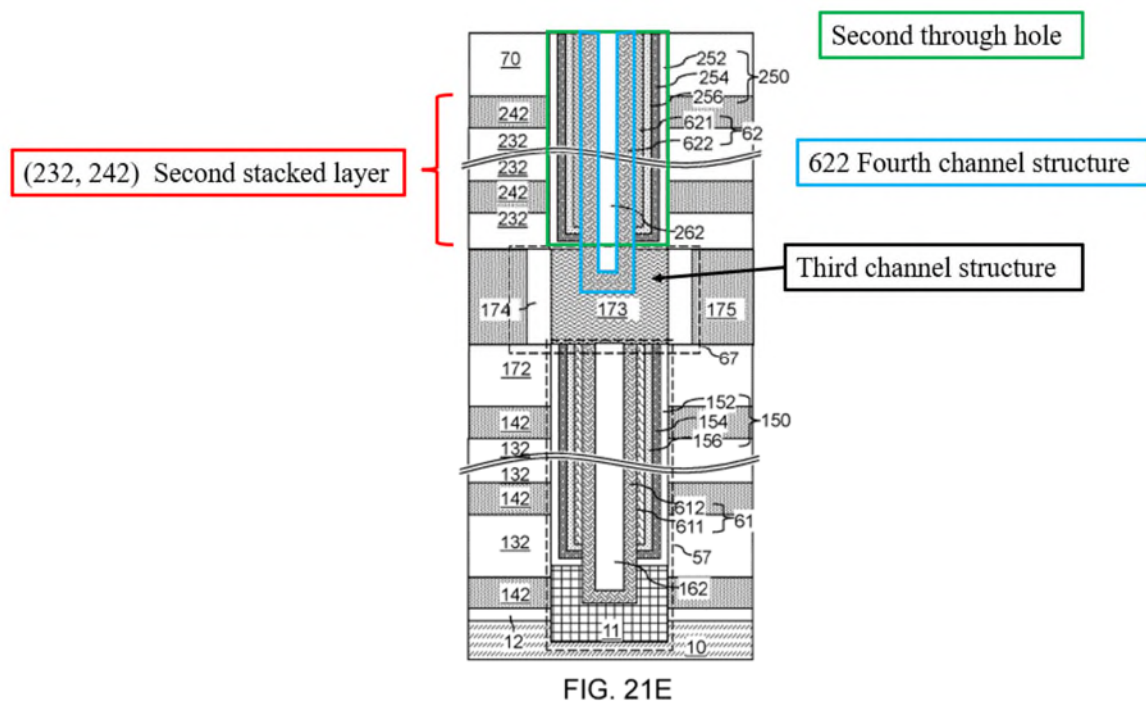
Id., Fig. 19 (annotated).

182. The '532 patent describes that the fourth channel structure can be composed of amorphous silicon. Ex. 1001, 14:51-53.

183. This is what Costa teaches. Specifically, Costa discloses forming a fourth channel structure (“second inner semiconductor channel layer 622” with or without the optional layer 621) in the second through hole (“second-tier memory opening 249”) and in contact with the third channel structure (“joint-level doped semiconductor portion 173”).

184. Specifically, Costa discloses that “a second inner semiconductor channel layer 622 can be deposited directly on the semiconductor surface of the

second joint-level doped semiconductor portion 179.” Costa, [0275] (and directly on optional semiconductor channel layer 621). Again, “an optional second outer semiconductor channel layer 621” can be deposited. *Id.*, [0273]. Figure 21D illustrates that second inner semiconductor channel layer 622 can be deposited on the inner surface of the second through hole and in contact with the exposed portion of the first joint-level doped semiconductor portion 173. *Id.*, [0275], Fig. 21D.

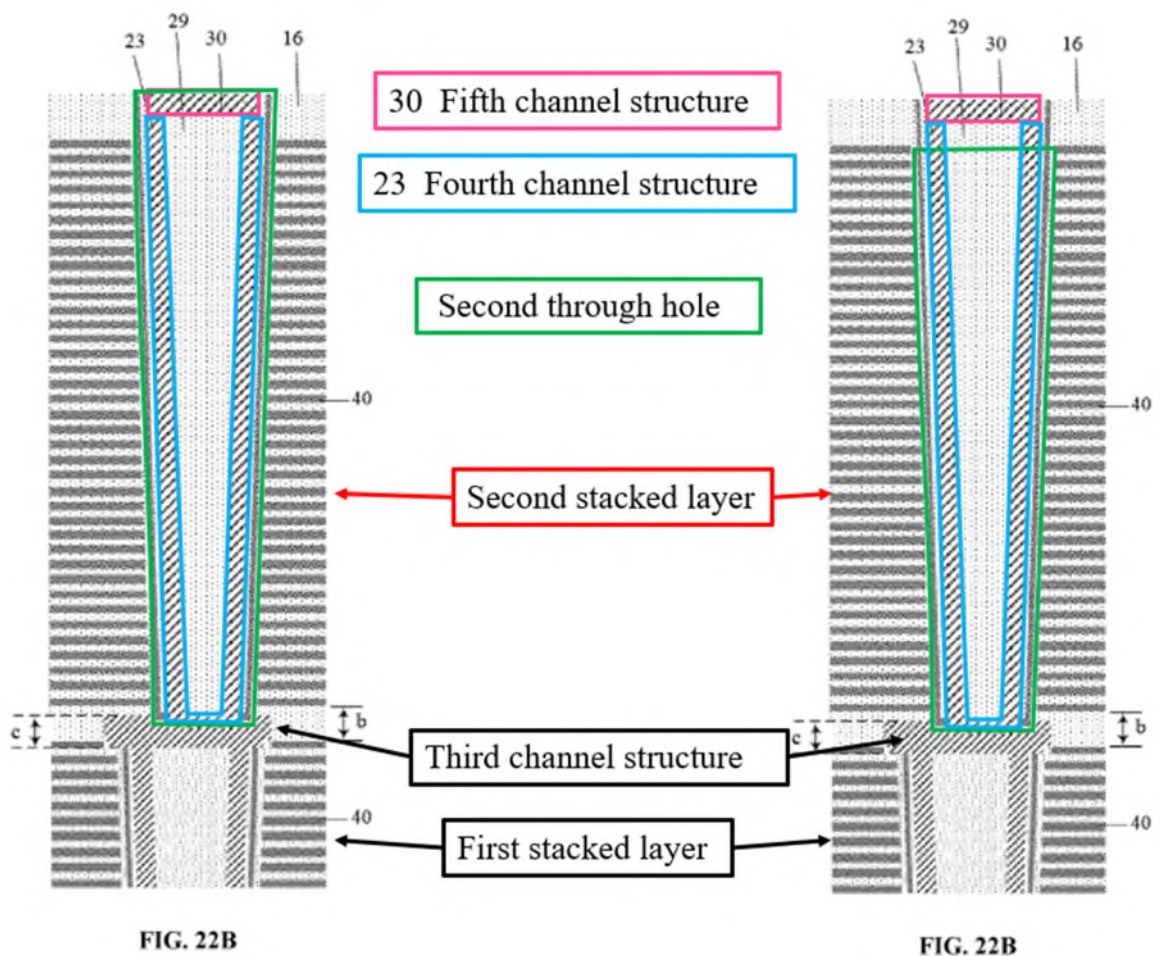


Id., Fig. 21E (annotated). Like Costa’s second channel structures, layers 621 and 622 may be “amorphous silicon or polysilicon,” and thus function as a channel. *Id.*, [0202], [0207].

[1.I] “forming a fifth channel structure above the second through hole and in contact with the fourth channel structure.”

185. This, in my opinion, is taught by Costa.

186. In the '532 patent, the fifth channel structure is formed in a manner similar to that of the third channel structure (described above). The '532 patent states that “a second groove can be formed on the fourth channel structure and the second filling structure, and in the second through hole 18.” Ex. 1001, 15:7-9. The “fifth channel structure can be formed in the second groove” and “the top surface of the second insulating connection layer 16 and the top surface of the fifth channel structure 30 can be planarized by any suitable techniques....” *Id.*, 15:19-31. As I stated above, the “second through hole” could be mapped to two different hole sizes:



Id., Fig. 22B (annotated).

187. Regardless of how one maps the “second through hole,” Costa discloses this limitation. Specifically, Costa discloses forming a fifth channel structure (“drain region 63”) above the second through hole (“second-tier memory opening 249”) and in contact with the fourth channel structure (“second inner semiconductor channel layer 622”). Costa, [0277].

188. Figure 21F reproduced and annotated below shows that drain region 63 can be formed in a recess etched into second dielectric core 262 below the top surface of insulating cap layer 70:

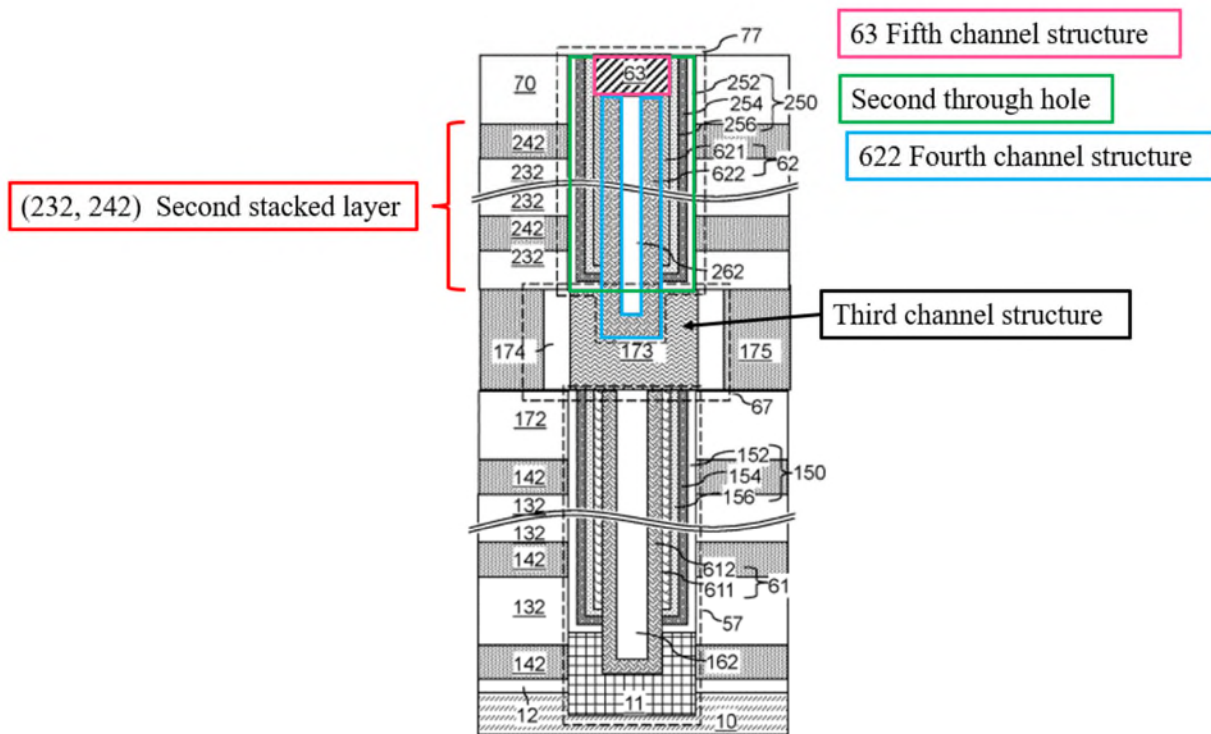


FIG. 21F

Costa, Fig. 21F (annotated), [0277].

189. As seen in this figure, drain region 63 is in contact with second inner semiconductor channel layer 621 (and optional layer 622). Costa, Fig. 21F.

190. The drain regions are formed “above the second through hole.” Specifically, Costa’s full “second through hole” starts at the top of insulating layer 70.

191. Costa also discloses forming drain regions in more detail with respect to the first embodiment, which Costa specifically references in the third embodiment regarding the conductive drains. Costa, [0277]. As Costa describes, forming conductive regions first involves etching the groove for the conductive drain and then depositing polysilicon for the drain. *Id.*, [0212]. Next, Costa discloses: “[e]xcess portions of the deposited semiconductor material can be removed from above the top surface of the insulating cap layer 70, for example, by chemical mechanical planarization (CMP) or a recess etch to form the drain regions 63.” *Id.* In other words, the conductive drain (“fifth channel structure”) is initially above hole, and CMP levels the plug to the same height as the connection layer.

192. In my opinion, if PO argues that Costa’s drain region 63 is not “form[ed] ... above the second through hole” (second-tier memory opening 249) because after drain region 63 is formed, the top of drain region 63 is at the top of “the second through hole” (Costa’s hole 249), I disagree for several reasons.

193. First, Costa describes forming drain region 63 in exactly the same manner as the fifth channel structure in the '532 patent, i.e., the “fifth channel structure” is not completely “above” the “second through hole” after fabrication of the memory has been completed unless the “second through hole” is defined to be only the part of the hole that extends through the stack (and not the portion that extends through the connection layer). This is true in viewing the “second through hole” in two different ways. As to the '532 patent, the top of the full “second through hole” is at the top of layer 16, i.e., it also extends through the connection layer:

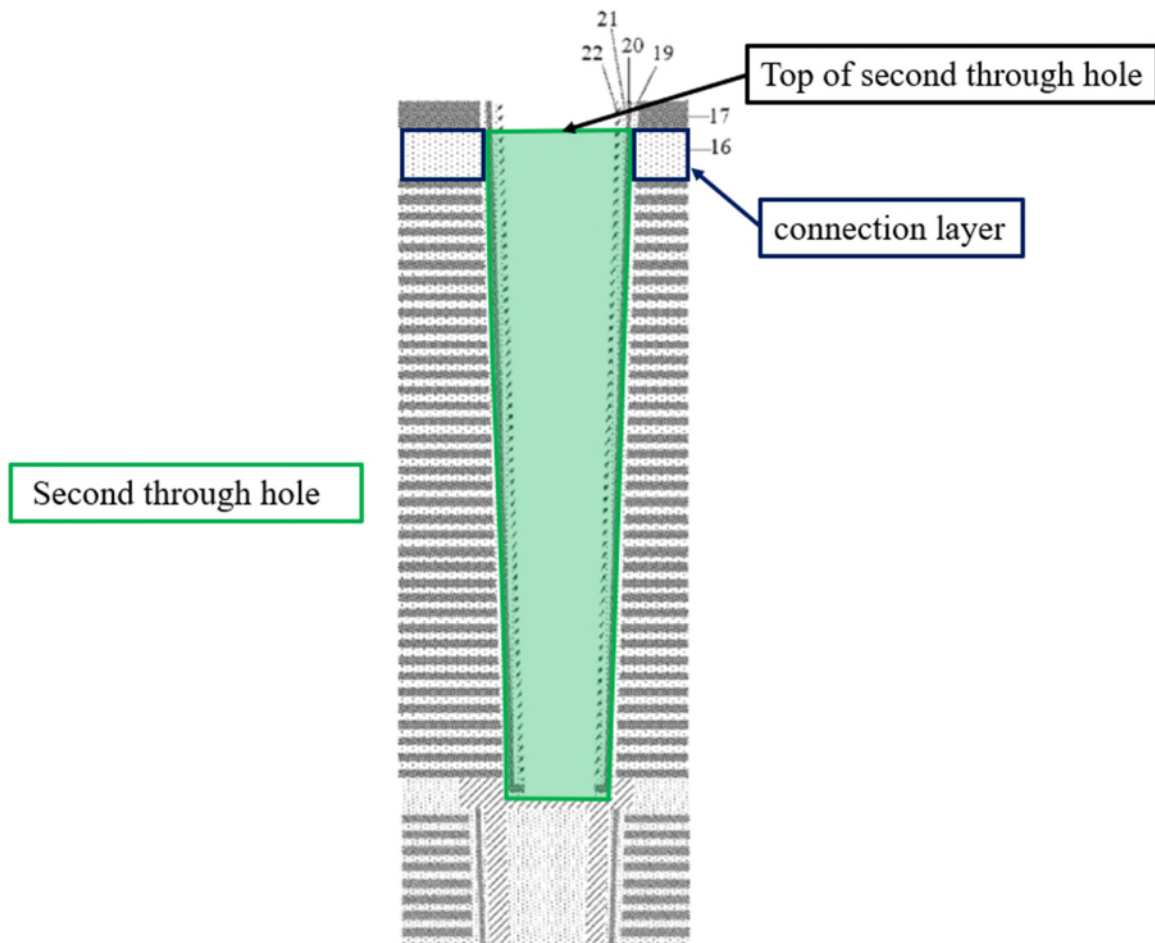


FIG. 15

Ex. 1001, Fig. 15 (annotated).

194. As seen below, however, the fifth channel structure is flush with layer 16 and sits within the “second through hole” under this reading of “second through hole”:

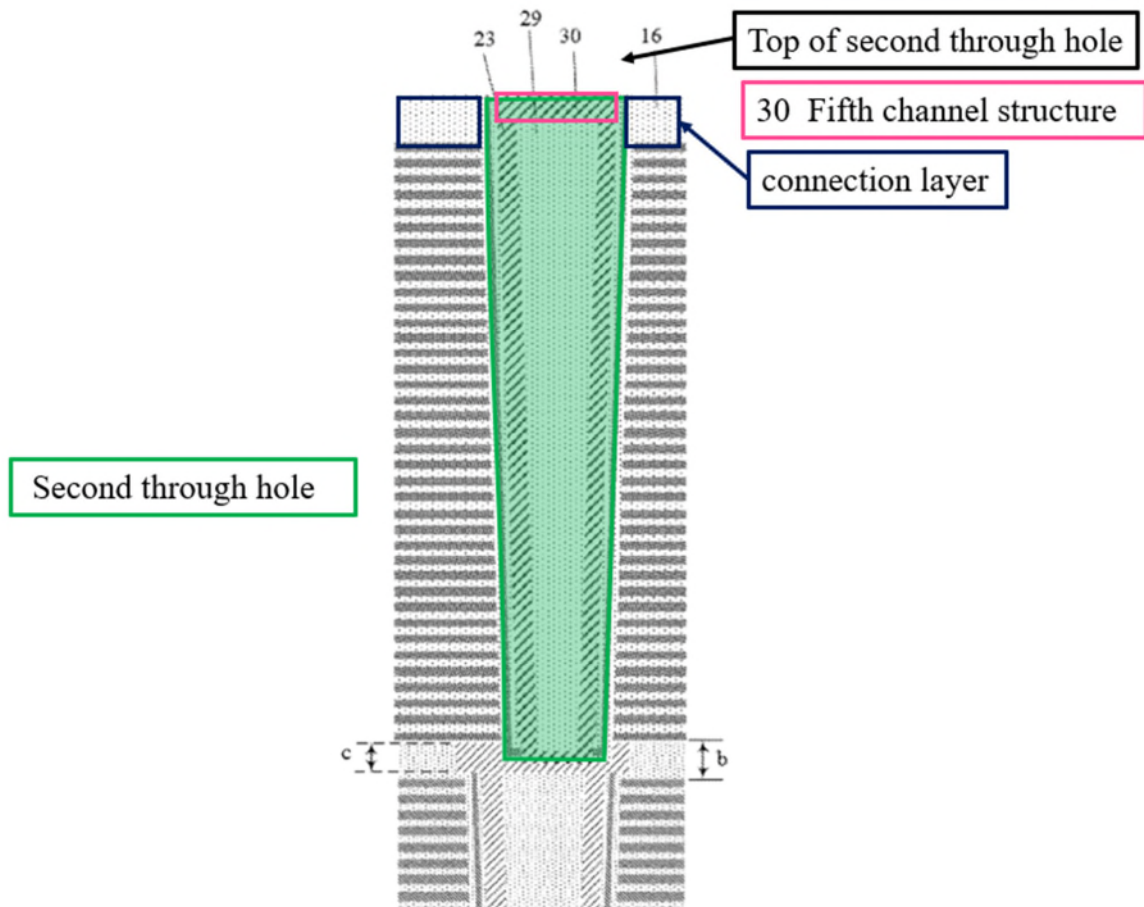
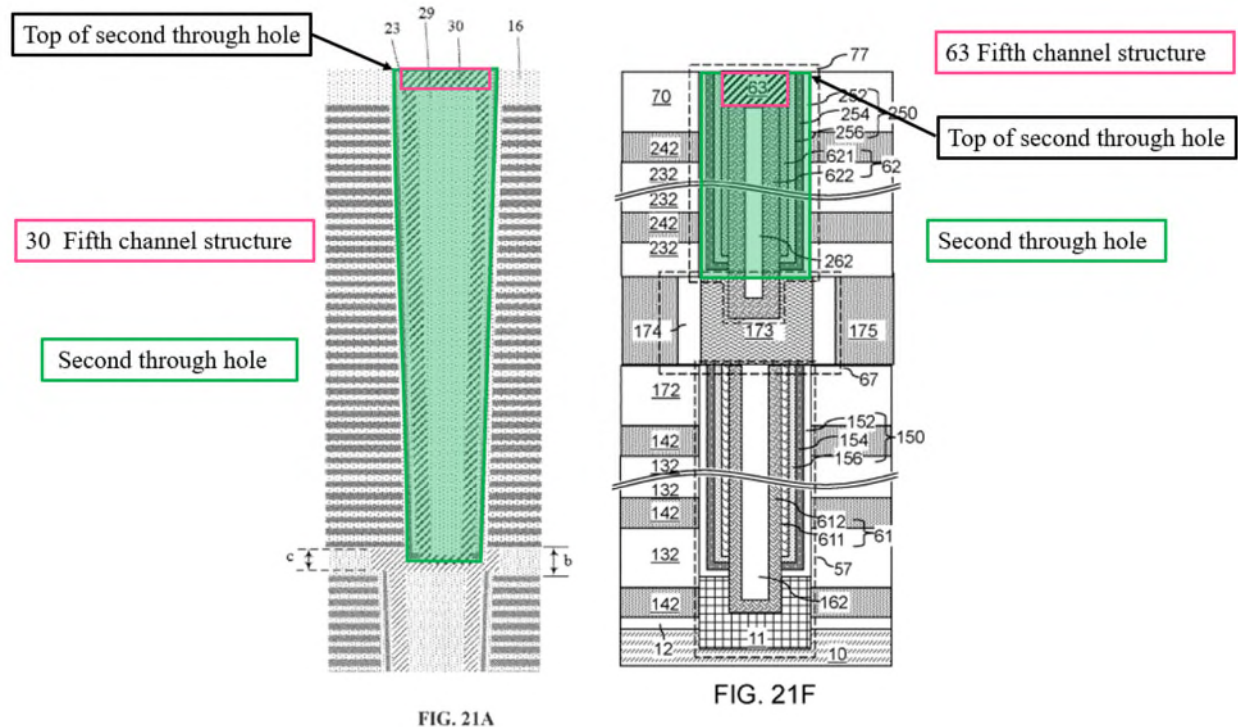


FIG. 21A

Id., Fig. 21A (annotated).

195. Costa's fifth channel structure sits flush within its hole through the stack and connection layer just like the '532 patent:



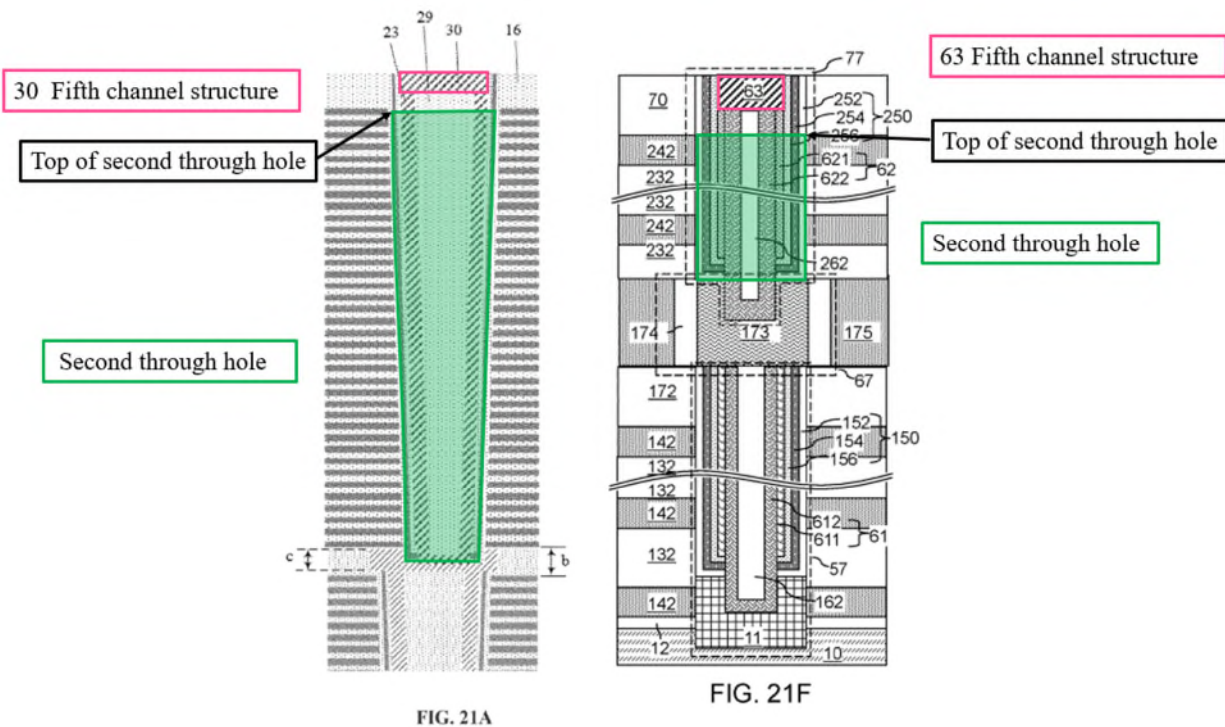
Ex.1001, Fig. 21A (left, annotated); Costa, Fig. 21F (right, annotated).

196. I also note that claim 1 recites a method, and this limitation requires a fifth channel structure that is “form[ed] ... above the second through hole.” Costa deposits the drain semiconductor material above the hole because Costa further teaches CMP to planarize the conductive material (downwards) to its final height of being at the top of the hole. Costa, [0212], [0277]. CMP refers to chemical mechanical planarization. This is a standard process. After filling a recess, the material will be higher than the recess, and the CMP process planarizes the material downward, flush with, in Costa, layer 70.

197. I also note that independent claims 11 and 18 (directed to “[a] joint opening structure of a three-dimensional (3D) memory device”) recite “a fifth

channel structure ... ***disposed over*** the second through hole,” Ex. 1001, cls. 11, 18, ***not*** “a fifth channel structure ... ***disposed above*** the second through hole.” And the specification does not describe any configuration where the fifth channel structure is above the full hole length. *E.g., id.*, 15:19-31, 24:18-31, 31:66-32:9, 40:38-51, Figs. 21A-B, 22A-B, 23B, 48A-B, 49A-B, 50B, 72A-B, 73A-B, 74B, 101A-B, 102A-B, 103B. Thus, this further supports that the claim would have been understood not to require a fifth channel structure that is above the full length of the hole.

198. One could also view the “second through hole” as being the hole that only extends through the stack, because the claim language defines the hole as being through the “stack.” Under this reading, both the ’532 patent and Costa disclose the fifth channel structure being above the shorter hole:



Ex. 1001, Fig. 21A (left, annotated); Costa, Fig. 21F (right, annotated).

2. Claim 2

199. Claim 2 depends on claim 1 and further requires:

[2.PRE] “The method of claim 1, wherein:”

[2.A] “the first stacked layer includes a first number of oxide/nitride layer pairs; and”

[2.B] “the second stacked layer includes a second number of oxide/nitride layer pairs.”

200. Costa, in my opinion, teaches what these limitations require.

201. Per Costa, “[t]he number of repetitions of the pairs of a first insulating layer 132 and a first sacrificial material layer 142 can be in a range from 2 to 1,024, and typically from 8 to 256.” Costa, [0133]. And the same is true of the second alternating stack. *Id.*, [0182].

202. As I explained when discussing limitations [1.A] and [1.E] above, these stacked layers can be comprised of oxide/nitride layer pairs.

203. Patent Owner may argue that the claimed “first number” and “second number” must be different. This, in my opinion, would be incorrect.

204. Nothing in the ’532 patent’s claims or specification would require such an interpretation. Indeed, the patent explains that the words “first” and “second” are just meant to denote different physical stacks. *See* Ex. 1001, cl. 2, 43:10-13 (“[T]he words ‘first’, ‘second’ and the like used in this disclosure do not denote any order, quantity or importance, but are merely intended to distinguish between different constituents.”). So, the “first number” is just the number of oxide/nitride layer pairs in the first stack, while the “second number” is just the number of oxide/nitride layer pairs in the second stack.

3. Claim 3

205. Claim 3 depends on claim 2 and further requires:

[3] “The method of claim 2, wherein: the first number and the second number are not less than 32.”

206. In my opinion, this is taught by Costa for the same reasons discussed in connection with claim 2: Costa teaches the use of a number of layers that exceeds 32.

4. Claim 11

207. Claim 11 is another independent claim.

[11.Pre] “A joint opening structure of a three-dimensional (3D) memory device, comprising:”

208. To the extent this preamble is limiting, in my opinion it is taught for the same reasons explained above for the preamble of claim 1. Substantively, this preamble is identical to [1.PRE]: while claim 1 is directed to a method, the method of that claim forms the memory device joint opening structure this claim requires.

[11.A] “a first through hole penetrating a first stacked layer along a vertical direction;”

209. This limitation is present in and thus is taught by Costa for the same reasons I describe above for limitations [1.A] and [1.B].

[11.B] “a first channel structure disposed at the bottom of the first through hole;”

210. This limitation is present in and thus is taught by Costa for the same reasons I describe above for limitation [1.C].

[11.C] “a second channel structure in contact with the first channel structure disposed in the first through hole;”

211. This limitation is present in and thus is taught by Costa for the same reasons I describe above for limitation [1.D].

[11.D] “a third channel structure in contact with the second channel structure disposed over the first through hole, wherein a size of the third channel structure along a lateral direction is larger than a top aperture of the first through hole;”

212. This limitation is substantively the same as limitation [1.E] discussed above. The only difference is that it uses the phrase “disposed over” instead of

“form[ed] ... above.” As a result, in my opinion it is taught by Costa for the same reasons I explained for limitation [1.E].

[11.E] “a second stacked layer disposed on the third channel structure;”

213. This limitation is substantively the same as limitation [1.F] discussed above. As a result, in my opinion it is taught by Costa for the same reasons I explained for limitation [1.F].

[11.F] “a second through hole penetrating the second stacked layer along the vertical direction;”

214. This limitation is substantively the same as limitation [1.G] discussed above. As a result, in my opinion it is taught by Costa for the same reasons I explained for limitation [1.G].

[11.G] “a fourth channel structure in contact with the third channel structure disposed in the second through hole;”

215. This limitation is substantively the same as limitation [1.H] discussed above. As a result, in my opinion it is taught by Costa for the same reasons I explained for limitation [1.H].

[11.H] “a fifth channel structure in contact with the fourth channel structure disposed over the second through hole.”

216. This limitation is substantively the same as limitation [1.I] discussed above. The only difference is that it uses the phrase “disposed over” instead of “form[ed] ... above.” As a result, in my opinion it is taught by Costa for the same reasons I explained for limitation [1.I].

5. Claim 13

217. Claim 13 depends on claim 11 and further requires:

[13.Pre] “The joint opening structure of claim 11, further comprising:” [13.A] “a first filling structure covering the surface of the second channel structure; and”

218. This, in my opinion, is taught by Costa.

219. Here, the '532 patent describes the claimed first filling structure in conjunction with the second channel structure discussed in [1.D]. Specifically, “a first filling layer 12 can be formed to cover the second channel layer 11 and fill the first through hole 5.” Ex. 1001, 11:35-37, Fig. 6. A subsequent etching process removes “a portion of the first filling layer 12” such that “the remaining portion of the first filling layer 12 in the first through hole 5 can form the first filling structure” as shown in Figure 10B below. *Id.*, 11:41-51, Figs. 7A-B. As described by the '532 patent, the first filling layer can be an oxide layer. *Id.*, 19:40-42. Put simply, the filling structure is, e.g., the core of the channel structure.

220. The annotated version of Figure 10B below shows these two structures (along with the surrounding structure):

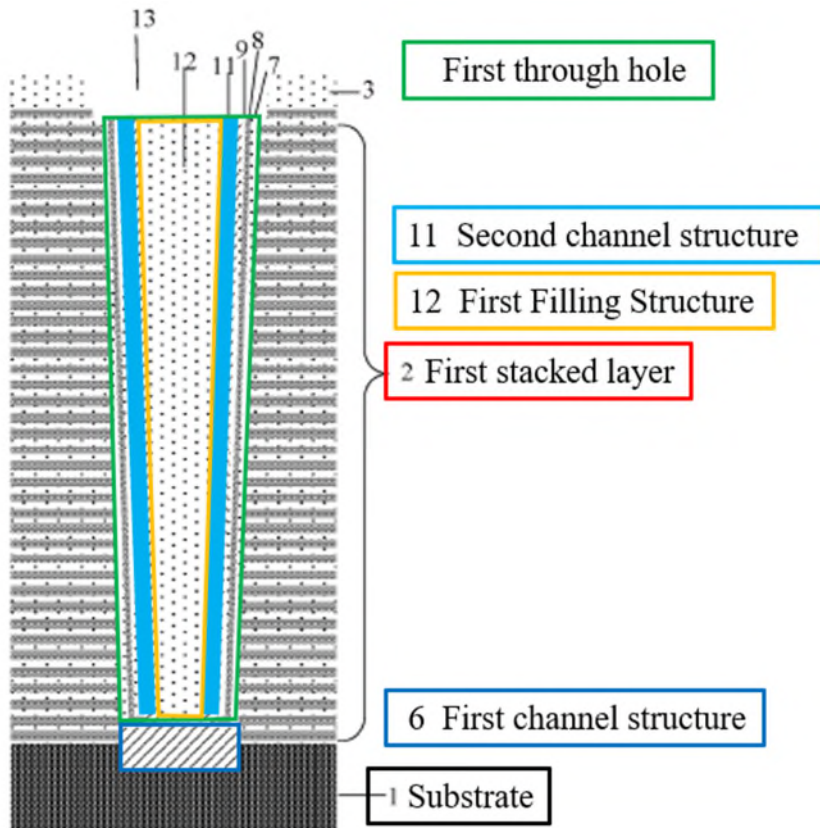


FIG. 10B

Ex. 1001, Fig. 10B (annotated).

221. This, in my opinion, is also what Costa teaches. Costa teaches that the cavity it forms need not be completely filled with semiconductor channel material. Costa, [0158], Fig. 4F. Then, a “dielectric core layer 162L” is formed. *Id.*, [0158], Fig. 4F. In other words a portion of “first dielectric core layer 162L” that is “above the top surface of the first-tier insulating cap layer 172” is removed leaving “dielectric core 162” within the memory cavity 149. *Id.*, [0159], Fig. 4G.

222. These structures are shown in the below annotated version of Figure 4G:

embodiments, the projection of the first groove on the substrate 1 can completely cover the projection of the first through hole 5 on the substrate 1.”).

225. Thus, it is my opinion that a POSTIA would not read “covering” to mean “completely covering,” *e.g.*, covering the entirety of the underlying object. Moreover, as Figure 4G above demonstrates, dielectric core 162 is in direct contact with each inner surface (relative to the channel hole) of inner semiconductor channel layer 612. Costa, Fig. 4G. Thus, dielectric core 162 is “covering the surface of” inner semiconductor channel layer 612. *Id.*

[13.B] “a second filling structure covering the surface of the fourth channel structure;”

226. This, in my opinion, is taught by Costa.

227. In the ’532 patent, “a second filling layer 29 can be formed to cover the fourth channel layer 23 and to fill the second through hole 18.” Ex. 1001, 14:54-56, Fig. 17. A subsequent etching process removes “a portion of the second filling layer 29” such that “[t]he remaining portions of the second filling layer 29 in the second through hole 18 can form the second filling structure.” *Id.*, 14:63-65, Fig. 18. As described by the ’532 patent, the second filling structure can be an oxide layer. *Id.*, 14:56-58. Just like the first filling structure, the second filling structure is, *e.g.*, the core of the channel structure. This is shown in Figure 19:

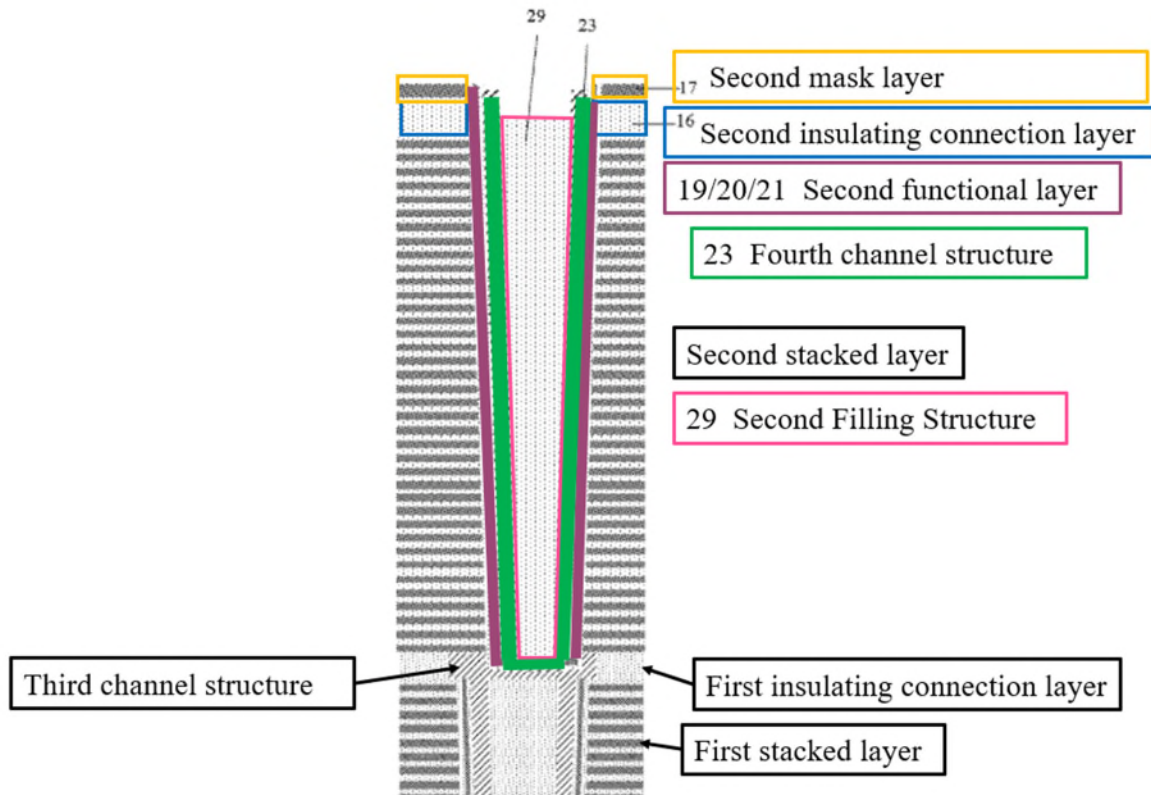


FIG. 19

Id., Fig. 19 (annotated).

228. Costa likewise teaches a second filling structure (“dielectric core 262”) that covers the surface of the second channel structure (“inner semiconductor channel layer 622”). The “outer semiconductor channel layer 621,” shown below, is optional. Costa, [0196].

229. Costa discloses that a “second dielectric core layer 262L” may be deposited as a core. Costa, [0275], Fig. 21D. A subsequent etching process removes “the horizontal portion of the second dielectric core layer 262L,” leaving second dielectric core 162 within the second memory cavity 249’. *Id.*, [0276].

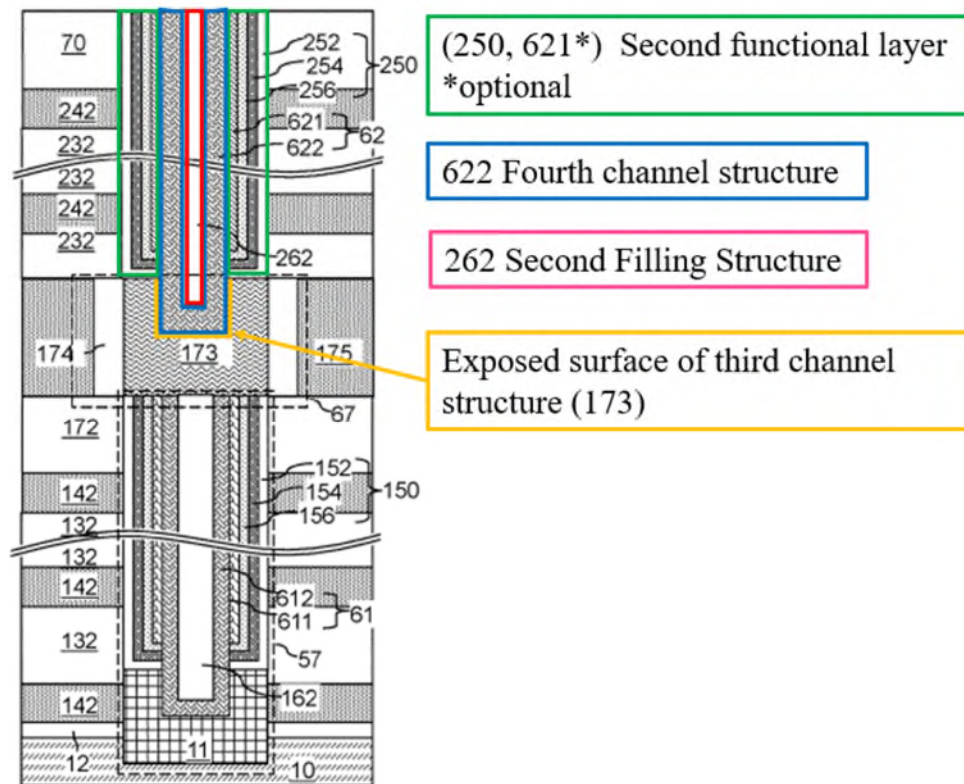


FIG. 21E

Id., Fig. 21E (annotated).

230. If Patent Owner argues that Costa fails to meet this limitation because dielectric core 262 does not “cover the surface of the fourth channel structure,” Patent Owner is mistaken for the same reasons described in [13.A] regarding dielectric core 162.

[13.C] “wherein the first through hole is non-interconnected with the second through hole.”

231. In my opinion, Costa teaches what this limitation requires.

232. More particularly, when forming second-tier memory openings 249, Costa explains that “second-tier memory openings 249 are formed through the

second tier structure (232, 242, 70, 265) in areas that overlap with the joint-level memory opening fill structures 67, i.e., with the joint-level memory openings.” Costa, [0191]; Figs. 10A-10B.

233. Costa also explains that “FIG. 21A” (and the figures that follow) “illustrate a region of the second exemplary structure at the processing steps of FIGS. 10A and 10B, i.e., after formation of the second-tier memory openings 249....” Costa, [0272]; Fig. 21A.

234. As illustrated in Fig. 21F, in Costa, first-tier memory openings (filled in Fig. 21F with first memory opening fill structures 57) are non-interconnected with second-tier memory openings 249 (filled in Fig. 21F with second memory opening fill structures 77). As shown below, there are joint-level doped semiconductor portions 173 interposed between the first-tier and second-tier memory openings:

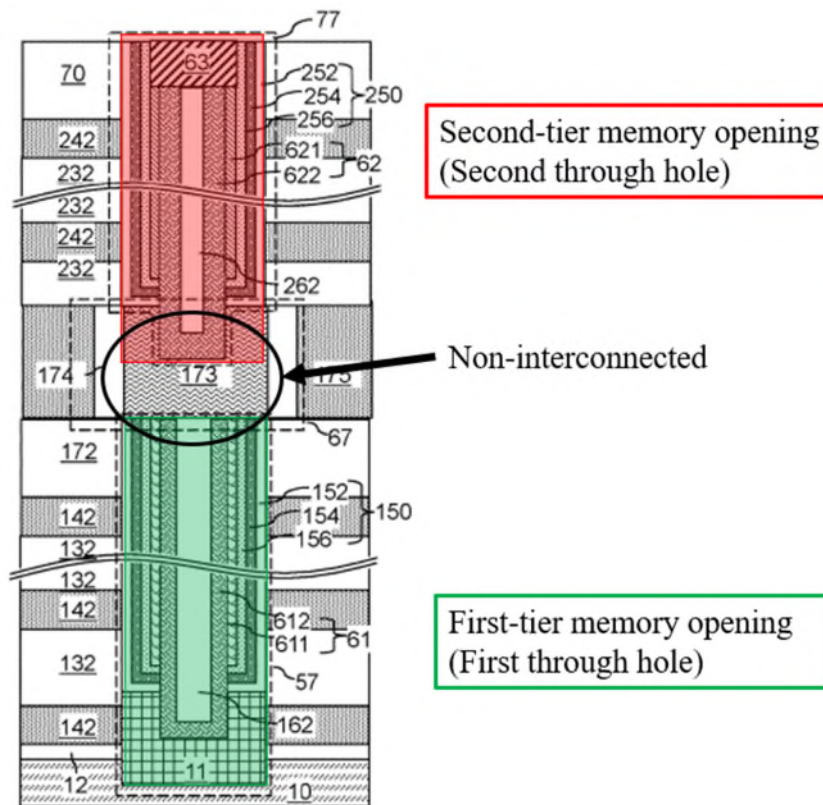


FIG. 21F

Costa, Fig. 21F (annotated).

6. Claim 15

235. Claim 15 depends on claim 11 and further requires:

[15.Pre] “The joint opening structure of claim 11, wherein:” [15.A] “the first stacked layer includes a first number of conductor/dielectric layer pairs;” [15.B] “the second stacked layer includes a second number of conductor/dielectric layer pairs; and”

236. These limitations are the same as [2.A]-[2.B] and thus it is my opinion that they are taught by Costa for the same reasons I describe above for those limitations.

[15.C] “the first number and the second number are not less than 32.”

237. This limitation is the same as claim 3 and thus it is my opinion that it is taught by Costa for the same reasons I describe above for that claim.

7. Claim 16

238. Claim 16 depends on claim 11 and further requires:

[16.Pre]-[16.A] “The joint opening structure of claim 11, wherein: a thickness of the third channel structure is in a range between 30 nm and 70 nm”

239. In my opinion, this is taught by Costa.

240. Per Costa, “[t]he thickness of the first joint-level doped semiconductor layer 173L can be in a range from 20 nm to 100 nm, although lesser and greater thicknesses can also be employed.” Costa, [0163].

241. A POSITA would have understood that Costa teaches use of range of layer thicknesses—overlapping the claimed range—because the other elements of Costa’s stack also have ranges of thicknesses. The ranges are simply meant to reflect the fact that reflect that different processes may be employed to fabricate the device. *E.g.*, Costa, [0139], [0146]-[0147], [0150], [0182].

242. I also note that the ’532 patent, like Costa, similarly discloses ranges for various layers. *E.g.*, Ex. 1001, 9:35-41.

8. Claim 17

243. Claim 17 depends on claim 11 and further requires:

[17.Pre] “The joint opening structure of claim 11, wherein:” [17.A] “a size difference between the top aperture and a bottom aperture of the first through hole is equal to or less than 30 nm; and”

244. In my opinion, Costa teaches what this limitation requires.

245. In Costa, “[t]he lateral dimensions (e.g., a diameter) of the first-tier openings (149, 119) can be from about 20 nm to 200 nm at an upper portion of each first-tier opening (149, 119), and can be about 10 nm to 150 nm at a lower portion of each first-tier opening (149, 119).” Costa, [0139].

246. In other words, a POSITA would have recognized not only that there is a size difference between the top and bottom “aperture” of first-tier memory opening 149 in Costa, but that this size difference can be less than or equal to 30 nm as the claim requires.

247. This size difference is the necessary result of the etching process used to create the opening: more etching will occur at the top of the hole while less etching will occur at the hole’s bottom resulting in a tapered structure.

248. Again, the range of opening diameters contemplated by Costa correspond with and teach the claimed range here. For instance, if the opening has a diameter of 20 nm at its top and 10 nm at its bottom, there would only be a 10 nm difference in diameter from top to bottom.

249. Not only is this consistent with what Costa actually discloses: in Costa depicts only minimal taper (and thus minimal diameter difference from the opening top to bottom), a POSITA would have considered it obvious to etch in a way that minimizes (as opposed to maximizes) the amount of taper from top to bottom of the opening naturally leading to a “size difference” that is well within the range of the claim here.

[17.B] “a size difference between a top aperture and a bottom aperture of the second through hole is equal to or less than 30 nm.”

250. In my opinion, Costa also teaches what this limitation requires.

251. According to Costa, the second through hole employs the same lateral dimensions as the first through hole. Costa, [0194].

252. Because of this, in my opinion a POSITA would have understood that for the same reasons I just explained for limitation [17.A] a size difference between the top and bottom “aperture” of second-tier memory opening 149 would also obviously be less than or equal to 30 nm.

9. Claim 18

253. Claim 18 is another independent claim.

[18.Pre] “A joint opening structure of a three-dimensional (3D) memory device, comprising:”

254. This limitation is substantively the same as [1.Pre] and thus it is my opinion that it is taught by Costa for the same reasons I describe above for that limitation.

255. The only difference is that Claim 1 recites a method of forming a joint opening structure in a three-dimensional (3D) memory device, but this difference is inconsequential to the disclosure of this limitation because a disclosure of forming something necessarily discloses the thing formed.

[18.A] “a first stacked layer disposed on a substrate;”

256. This limitation is substantively the same as [1.A] and thus it is my opinion that it is taught by Costa for the same reasons I describe above for that limitation.

[18.B] “a second stacked layer disposed on the first stacked layer; and”

257. This limitation is substantively the same as [1.F] and thus it is my opinion that it is taught by Costa for the same reasons I describe above for that limitation.

258. As I have explained, the '532 patent does not use the term “on” to mean “directly on.” Ex. 1001, 8:1-11. In other words, the second stacked layer does not need to be in physical contact with the first stacked layer to be “on” it (i.e., there can be one or more layers between the first and second stacked layers).

[18.C] “a plurality of channel structures penetrating the first stacked layer and the second stacked layer;”

259. In my opinion, Costa also teaches what this limitation requires.

260. Costa discloses a plurality of channel structures in a first region (memory array region 100) of the 3D memory device. Costa, [0124], Figs. 3A-B, 10A-B.

261. As I explained regarding [1.A]-[1.I], Costa discloses forming a plurality of first-tier memory openings 149 and second-tier memory openings 249 in memory array region 100, which are subsequently filled to form an active memory channel. See Section IX.B.1; Costa, [0135], [0161], [0190].

[18.D] “wherein each of the plurality of channel structures includes:” [18.E] “a first through hole penetrating the first stacked layer,”

262. This limitation is substantively the same as [1.B] and thus it is my opinion that it is taught by Costa for the same reasons I describe above for that limitation.

[18.F] “a first channel structure disposed at the bottom of the first through hole and in contact with the substrate,”

263. This limitation is substantively the same as [1.C] and thus it is my opinion that it is taught by Costa for the same reasons I describe above for that limitation.

[18.G] “a second channel structure disposed in the first through hole and in contact with the first channel structure,”

264. This limitation is substantively the same as [1.D] and thus it is my opinion that it is taught by Costa for the same reasons I describe above for that limitation.

[18.H] “a third channel structure disposed over the first through hole and in contact with the second channel structure, wherein a size of the third channel structure along a lateral direction is larger than a top aperture of the first through hole;”

265. This limitation is substantively the same as [1.E] and thus it is my opinion that it is taught by Costa for the same reasons I describe above for that limitation.

266. The only difference between this limitation and [1.E] is an inconsequential change in language. This limitation recites “disposed over” whereas [1.E] recites “form[ed] ... above.” This is inconsequential because if something is formed over it is necessarily, once formed, “disposed over.”

[18.I] “a second through hole penetrating the second stacked layer,”

267. This limitation is included as a part of [1.G] (“forming a second through hole penetrating the second stacked layer”) and is substantively similar to that part of [1.G] and thus it is my opinion that it is taught by Costa for the same reasons I describe above for that limitation.

268. The only difference between this limitation and [1.G] is an inconsequential change in language. [1.G] recites “forming” whereas this limitation does not. This is inconsequential because if something is “formed” it would then exist and thus satisfy this limitation.

[18.J] “a fourth channel structure disposed in the second through hole and in contact with the third channel structure, and”

269. This limitation is substantively the same as [1.H] and thus it is my opinion that it is taught by Costa for the same reasons I describe above for that limitation.

[18.K] “a fifth channel structure disposed over the second through hole and in contact with the fourth channel structure.”

270. This limitation is substantively the same as [1.I] and thus it is my opinion that it is taught by Costa for the same reasons I describe above for that limitation.

271. The only difference between this limitation and [1.I] is an inconsequential change in language. This limitation recites “disposed over” whereas [1.I] recites “form[ed] ... above.” This is inconsequential because if something is formed over it is necessarily, once formed, “disposed over.”

10. Claim 20

272. Claim 20 depends on claim 18 and further requires:

[20.Pre] “The joint opening structure of claim 18, wherein:” [20.A] “a thickness of the third channel structure is in a range between 30 nm and 70 nm.”

273. These limitations are the same as [16.Pre]-[16.A] and thus it is my opinion that they are taught by Costa for the same reasons I describe above for those limitations.

C. Ground 2: Claims 1-3, 11, 13, 15-18, and 20 Are Obvious Over Costa in view of Oh

274. In my opinion, a POSITA would have considered both Costa and Oh to be within the scope of the prior art and highly relevant to the patentability of the '532 patent's claims. Both Costa and Oh, for example, relate to multi-deck structures. See §IX.A.

275. I have been asked to separately consider Costa in view of Oh. In my opinion, when viewed and considered in light of the knowledge of a POSITA, Costa and Oh render claims 1-3, 11, 13, 15-18, and 20 of the '532 patent obvious.

276. For Ground 2, I apply the same claim mapping as Ground 1 and not repeat that analysis here. Below, I specifically address whether a POSITA would have been motivated, with a reasonable expectation of success, to widen Costa's third channel structure in view of Oh's teachings. In my opinion, a POSITA would have been motivated to do so.

1. Motivation to Combine

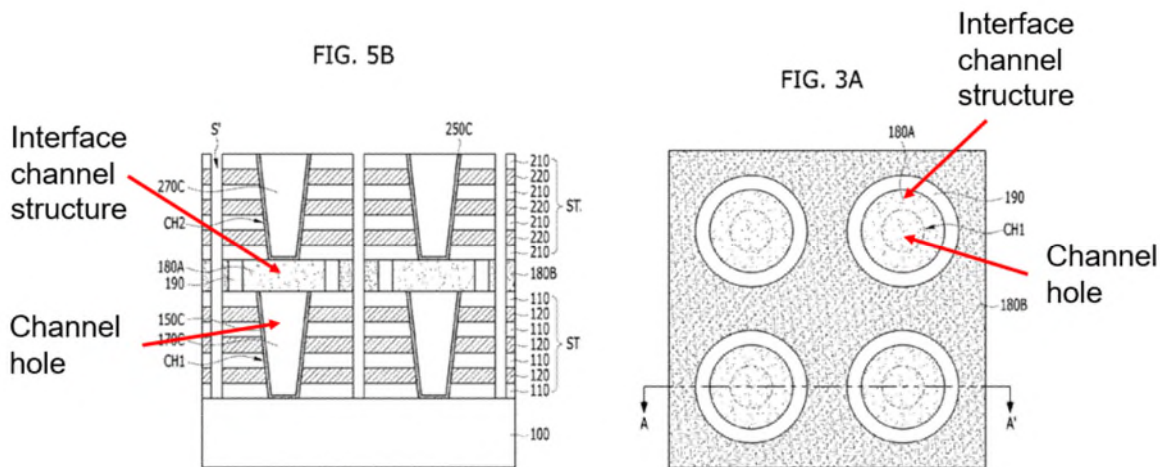
277. As an initial matter, Costa recognizes that because its process is not self-aligned, the process is subject to misalignment. In one embodiment, for example, Costa recognizes the need "to account for misalignment" when forming a channel interface structure over the first channel structure. Costa, [0164]. This is because the process for forming the third channel structure is not self-aligned. By way of example, take the example of forming a source and drain region after forming

the gate of a CMOS transistor in a gate-first process. After forming the gate, the gate, in simple terms, provides a structural reference point for the process that forms the source and drain regions (via, e.g., implantation of dopants). Unlike this process, the formation of channel structure 173 does not have a similar reference point to fix its location. As a result, Costa teaches accounting for this margin. *Id.* In this embodiment, Costa is intending to ensure that channel structure 173 physically contacts the through-hole channel material (149'). But in view of these alignment issues, Costa states that structure 173 must be made wider than the width of 149', because even if there is some misalignment, then channel structure 173 will still contact 149'. *Id.*

278. In other embodiments, Costa discloses that the third channel structure 173 “can contact an entire top surface of an underlying first memory opening fill structure 57,” which protects the lower deck channel structure during processing. Costa, [0265]. This means, for example, the optional oxidation step will not inadvertently damage any portions of fill structure 57. A POSITA would have understood that to ensure the third channel structure 173 fully contacts the entire top surface of fill structure 57, the design would be that the width is wider than the top of fill structure 57, consistent with Costa’s recognition of these well-known alignment issues. Given that Costa expressly recognizes these alignment issues, in viewing Costa, a POSITA would have been motivated to consider other teachings

that also address alignment issues, particularly with respect to alignment of channel structures in a multi-deck structure.

279. Oh addresses these alignment issues for channels in a multi-deck structure. Oh's channel interface structure, like Costa's third channel structure, is the interface between channel structures in a multi-deck structure. Oh discloses: "Referring to FIG. 3A the channel connection pattern 180A may have an island shape which overlaps the first channel holes CH1 order to secure an overlap margin between the channel connection pattern 180A and the first channel hole CH1, the channel connection pattern 180A may have a larger width than the top surface of the first channel hole CH1." Oh, [0061].



Id., Figs. 3A, 5B. Oh's "overlap margin" ensures that even if misalignment occurs, the width of 180A accounts for that misalignment. For example, if 180A is not formed perfectly over the underlying channel structure, 180A can still contact the channel structure's semiconductor channel layer. Likewise, if the second, overlying

channel does not perfectly align to the middle of 180A, the overlying channel structure's semiconductive channel layer will still contact 180A. As a result, the width of 180A enables electrically coupling between the two channel structures even if misalignment occurs, creating a continuous channel between the upper and lower channel structures.

280. A POSITA would have understood that Costa is attempting to address the same issue of Oh, because as I discuss above, Costa expressly recognizes that misalignment may occur. Thus, a POSITA would have been motivated to consider other teachings that also address this same issue, such as Oh. Specifically, a POSITA would have been motivated to consider increasing “alignment margin” (Ex. 1016, [0086]), i.e., provide an “overlap margin” (Oh, [0061]). This “margin” means that even if misalignment occurs (within the margin), the overlap margin accounts for it, and the proper electrical coupling occurs.

281. It was well known that overlap margin accounts for misalignment, including in this specific context. Ex. 1017, [0058] (“memory opening alignment challenges may be reduced or avoided”). Perfectly aligning structures, such as the channel structures or a third interface structure, in a process that is not self-aligned is very challenging. For example, the masks would have to be perfectly formed and placed. By way of another example, the planarity of the structure itself can impact alignment, e.g., because that planarity impacts whether the etch is perfectly vertical.

Providing margin accounts for misalignment, in simple terms, reduces the requirement to perfectly align the structures. In view of a sufficient margin, for example, and using relative terms, it can be said that first and second channels are “easily connected” (again, this is in relative terms, as semiconductor fabrication is not often thought of as “easy”). Ex. 1007, [0037]-[0038].

282. A requirement in a multi-deck structure is that there is a continuous channel between the upper and lower channel structures. Each channel structure will include, for example, a layer of semiconductor film (often known as the channel). The interface structure ensures an electrical coupling between these layers. The channel structure (the top and bottom together) will not function unless there is this electrical coupling. Recall that a channel structure is a memory string of multiple memory cells, i.e., transistors. A read operation is instructive as an example. A read operation involves applying various threshold voltages to a target memory cell to determine whether that memory cell (a transistor) turns on or off. A pass voltage is applied to all other memory cells (to turns those transistors on). The entire channel structure operates as the channel. If the top and bottom channel structures did not electrically couple, there would be no channel to detect whether the target memory cell is turning on.

283. As can be seen from above, if misalignment results in the channel structures not electrically coupling, the memory channel will be non-functional. For

many decades, it has been standard to include redundant memory cells or channel structures to account for defective memory cells or channel structures. But if there are too many defects, the entire device is considered defective, e.g., the device does not have a pre-defined memory capacity. These devices are then not sold. The percentage of good or salable devices is known as the yield. In short, providing overlap margin for structures that are subject to misalignment increases yield, because it reduces the defective components. Yield is very important, because fabs are typically run nearly 24 hours a day, 7 days a week. The sellable output therefore is driven by process time and yield. Increasing yield increase the sellable output and directly correlates to profitability.

284. In my opinion, a POSITA would have had a high expectation of success in providing this overlap margin for several reasons.

285. First, providing margin is a standard, advantageous practice in semiconductor fabrication. A POSITA readily understood for any process design that is not self-aligned, misalignment issues must be considered. And margin, for example, may be as simple as designing a structure wider by a certain percentage than what its minimum, functional width must be. Semiconductor processes for forming channels, e.g., an anisotropic etch through a stack, were well known, and as a result, the associated margin that should be provided were also understood by a POSITA.

286. Second, as I discuss above, Costa already recognizes that alignment issues may occur with its process. Naturally, Costa accounts for this by making channel structure wider than its target width in those embodiments. A POSITA would have understood this simply involves making the mask that defines the width of channel structure 173 wider.

287. Third, applying a margin simplifies the overall fabrication process. This is because it eases how precise other steps must be. Take for example the etch to form the overlying channel (top) structure. If that channel structure must be perfectly aligned over channel structure 173, that etch step would have no margin for error, requiring perfect alignment for the corresponding mask.

D. Secondary Considerations of Non-Obviousness

288. Based on my review of the '532 patent's prosecution history, I note that no secondary considerations of non-obviousness were identified in connection with the patent's Claims.

289. I am not separately aware of any evidence of commercial success, skepticism, failure of others, industry praise, unexpected results, or the like. Instead, as discussed above, it is my opinion that the subject matter embraced by the '532 patent's claims was known in and obvious over the prior art. Moreover, it is also my opinion the teachings of the prior art would have been expected to successfully function as or be usable with working 3D memory devices.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Executed this 31st day of December 2024 at Austin, Texas.



Sanjay Banerjee, Ph.D.