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(12) **United States Patent**
Kanakamedala et al.

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(54) **SPACER PASSIVATION FOR HIGH-ASPECT RATIO OPENING FILM REMOVAL AND CLEANING**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(65) **Prior Publication Data**

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Related U.S. Application Data

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(51) **Int. Cl.**
H01L 21/336 (2006.01)
H01L 27/115 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ... ***H01L 27/11582*** (2013.01); ***H01L 21/02063*** (2013.01); ***H01L 21/28273*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC H01L 27/11556; H01L 27/1157; H01L 27/11582; H01L 29/66825; H01L 29/7889; H01L 21/28273; H01L 21/28282; H01L 21/76224; H01L 21/764; H01L 21/8221; H01L 21/8239; H01L 27/088; H01L 27/10805
See application file for complete search history.

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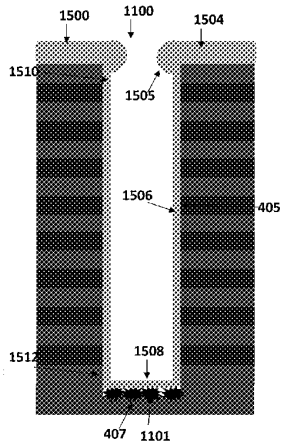
(57) **ABSTRACT**

A method of making a semiconductor device includes forming a stack of alternating layers of a first material and a second material over a substrate, etching the stack to form at least one opening in the stack such that a damaged region is located on a bottom surface of the at least one opening, forming a masking layer on a sidewall of the at least one opening while the bottom surface of the at least one opening is not covered by the masking layer, and further etching the bottom surface of the at least one opening remove the damaged region.

21 Claims, 22 Drawing Sheets



(51) **Int. Cl.**
H01L 21/311 (2006.01)
H01L 21/28 (2006.01)
H01L 21/02 (2006.01)

(52) **U.S. Cl.**
CPC .. ***H01L 21/28282*** (2013.01); ***H01L 21/31116*** (2013.01); ***H01L 21/31144*** (2013.01); ***H01L 27/1157*** (2013.01); ***H01L 27/11524*** (2013.01); ***H01L 27/11556*** (2013.01)

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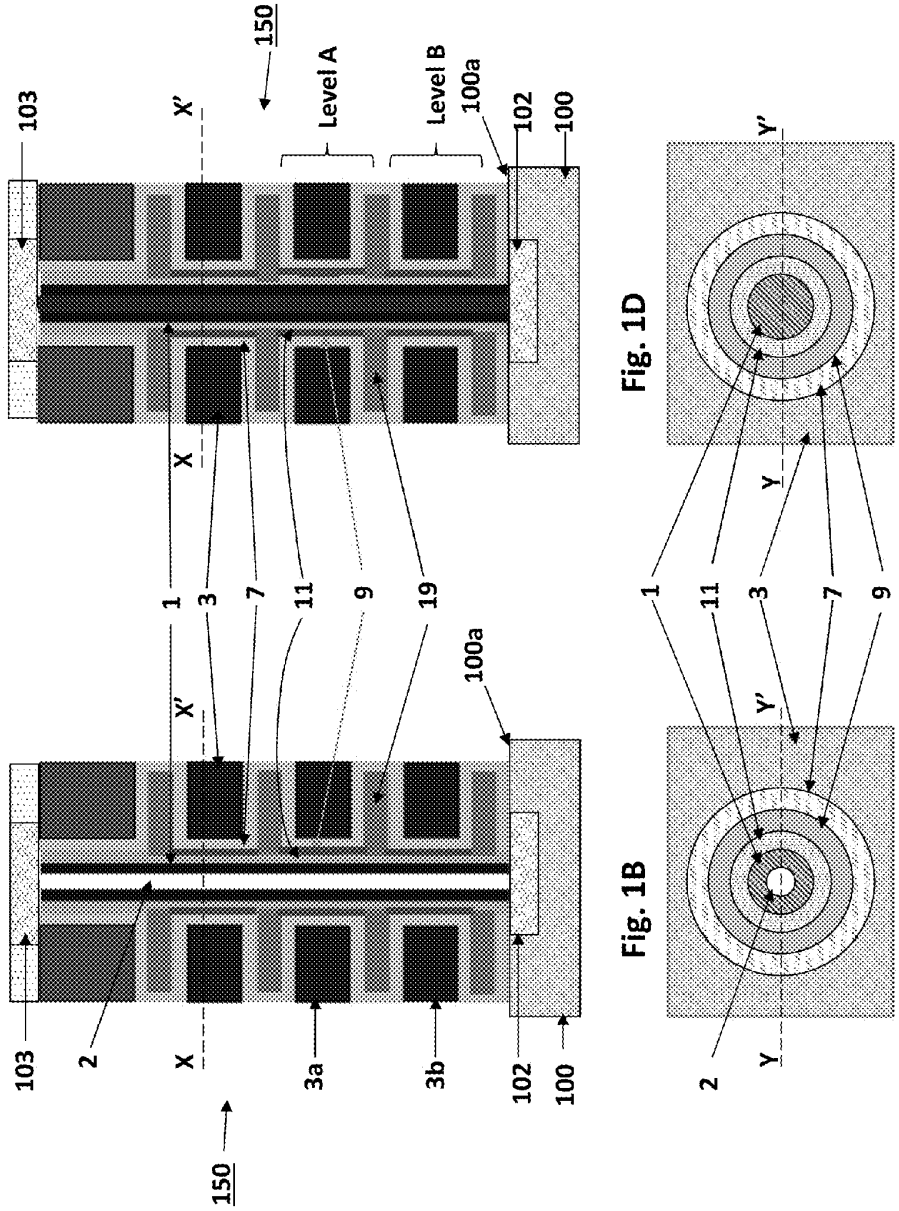
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Fig. 1B
Fig. 1C
Fig. 1D
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Level A
Level B
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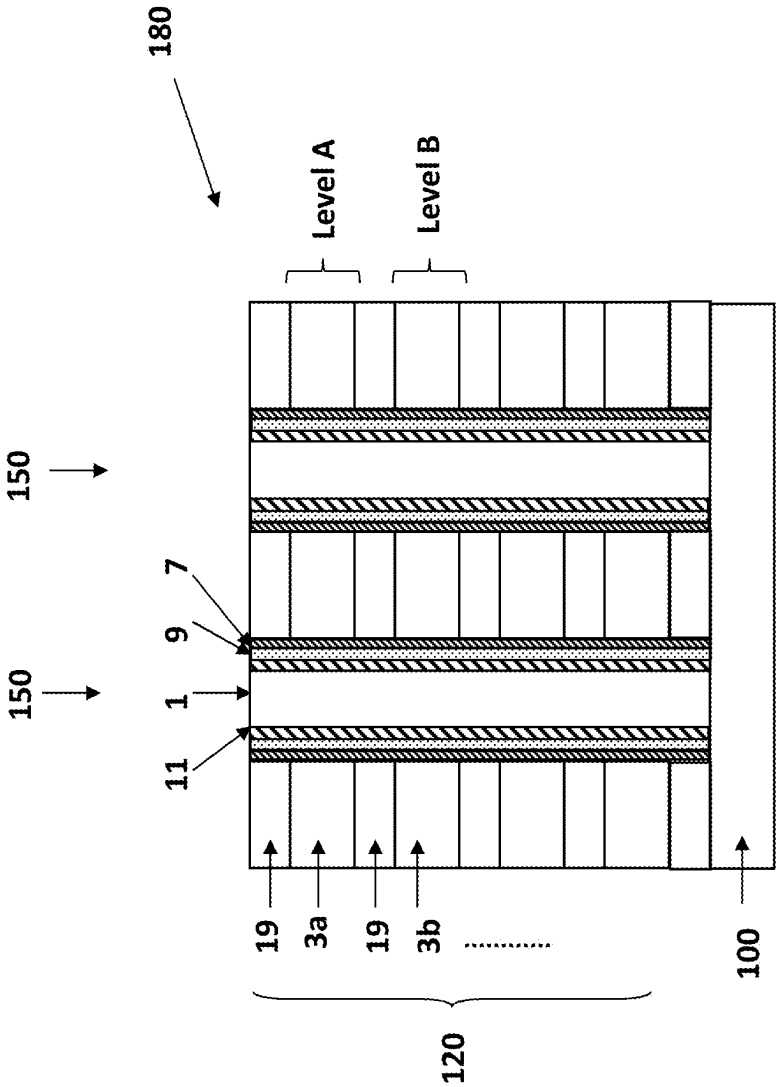
Y'



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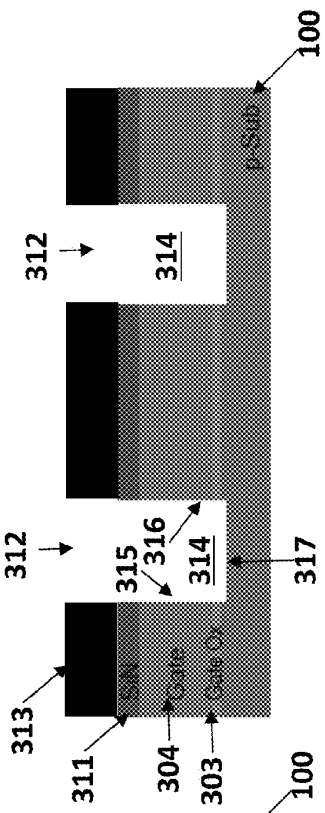

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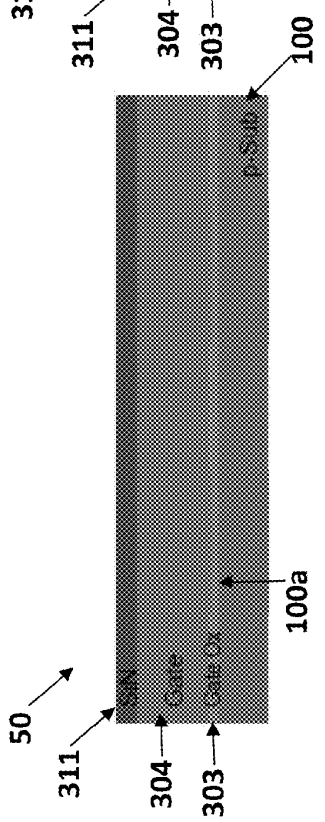

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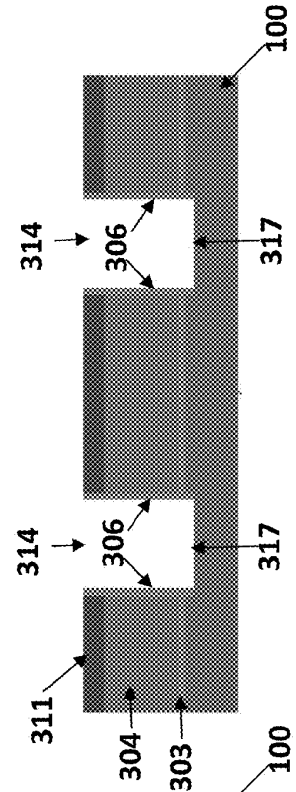

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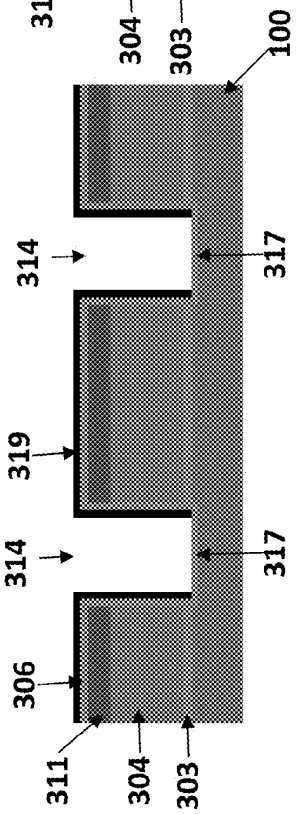
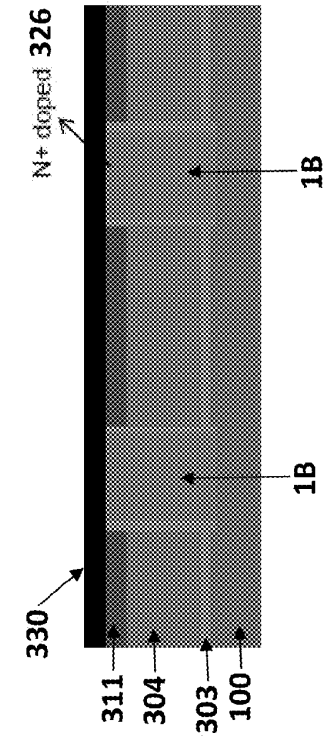


Fig. 3C



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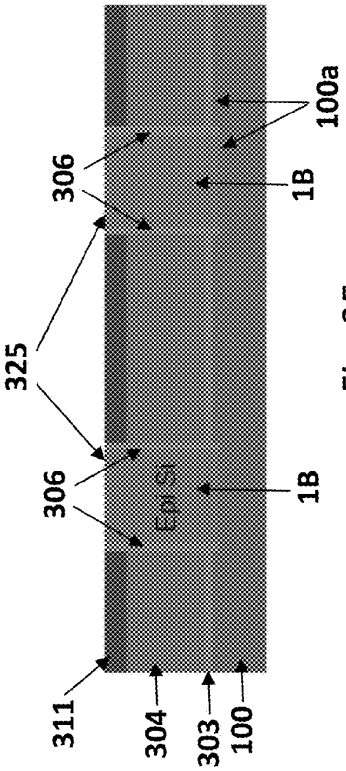

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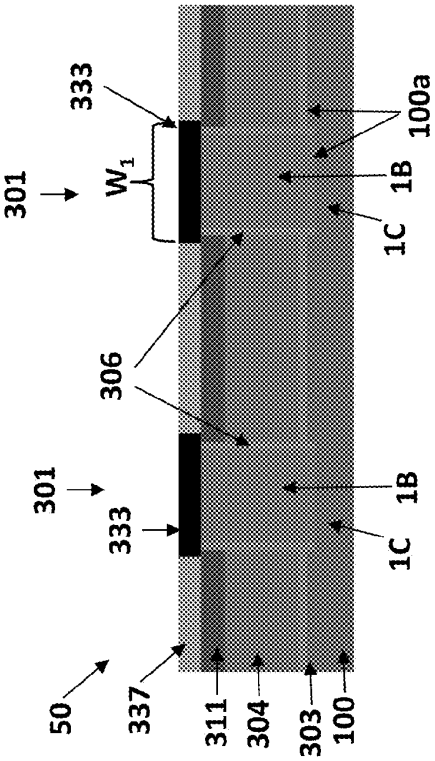

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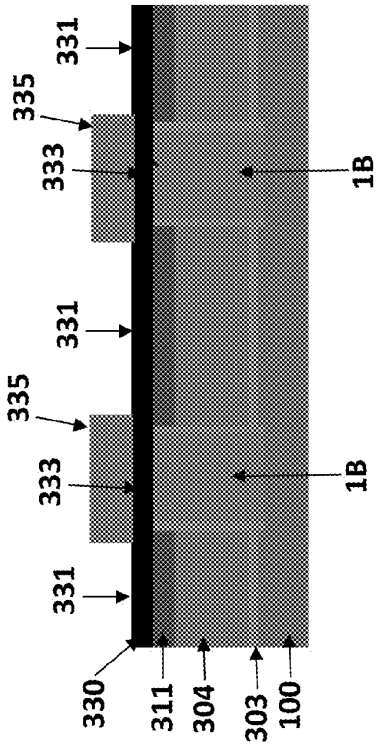

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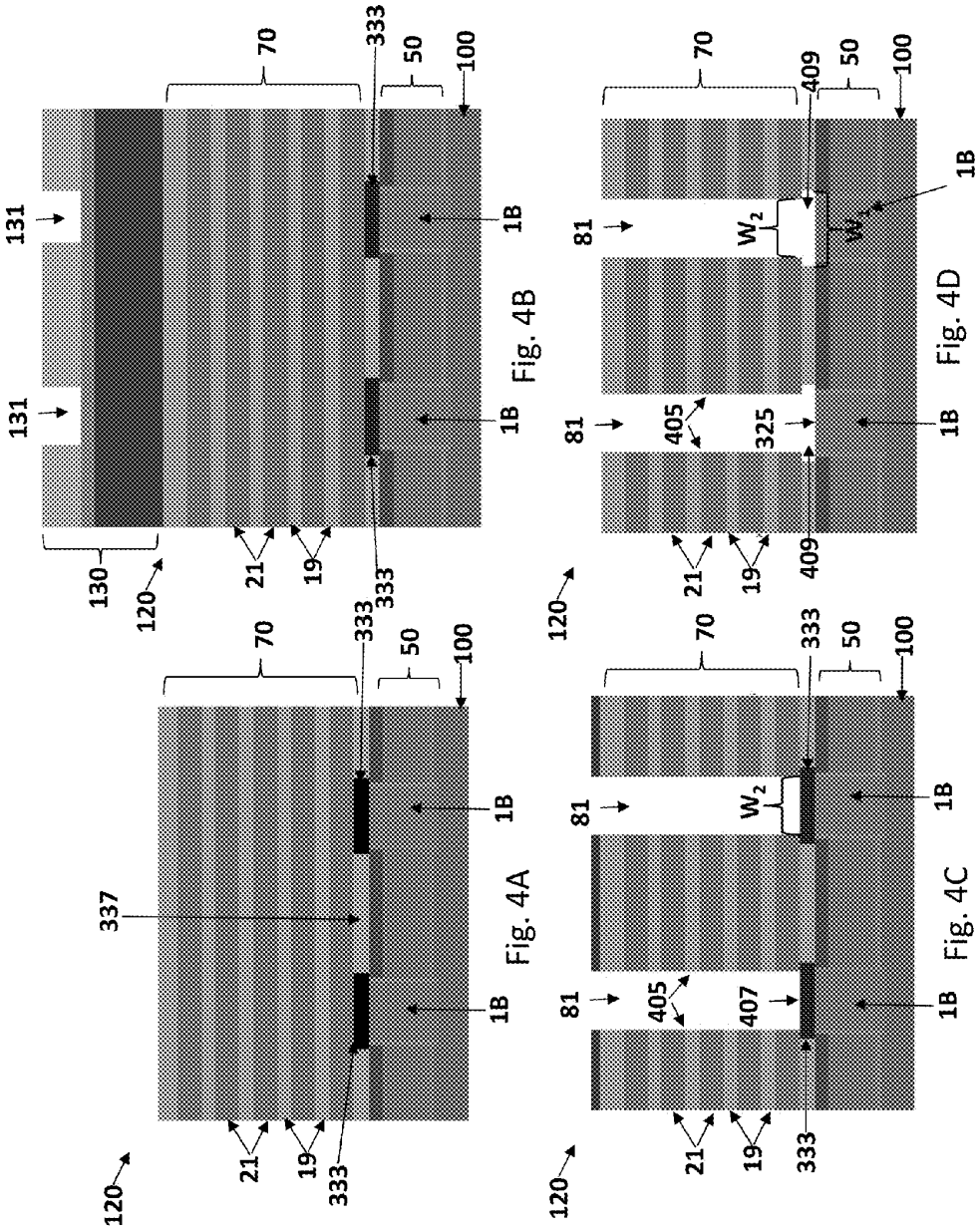
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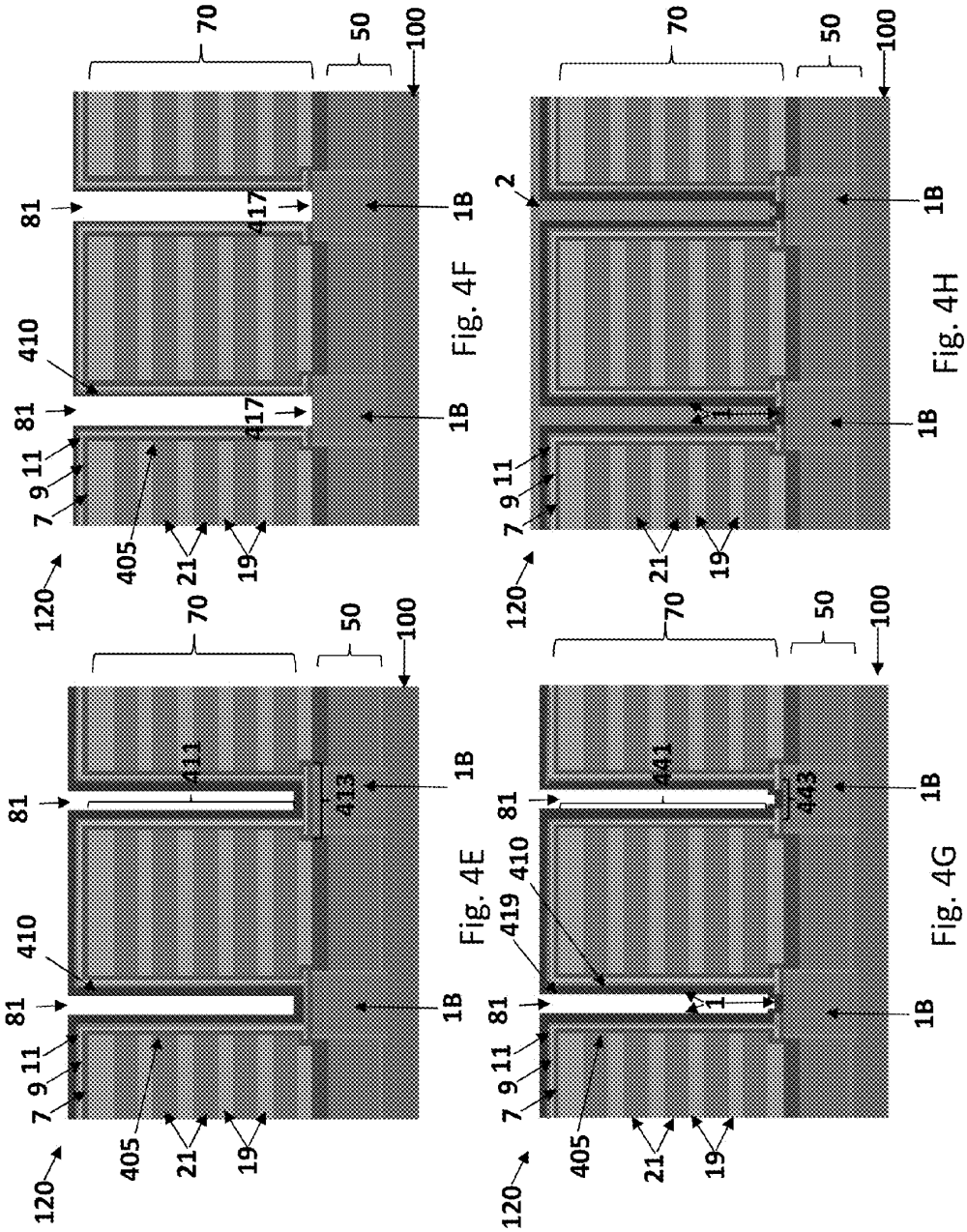
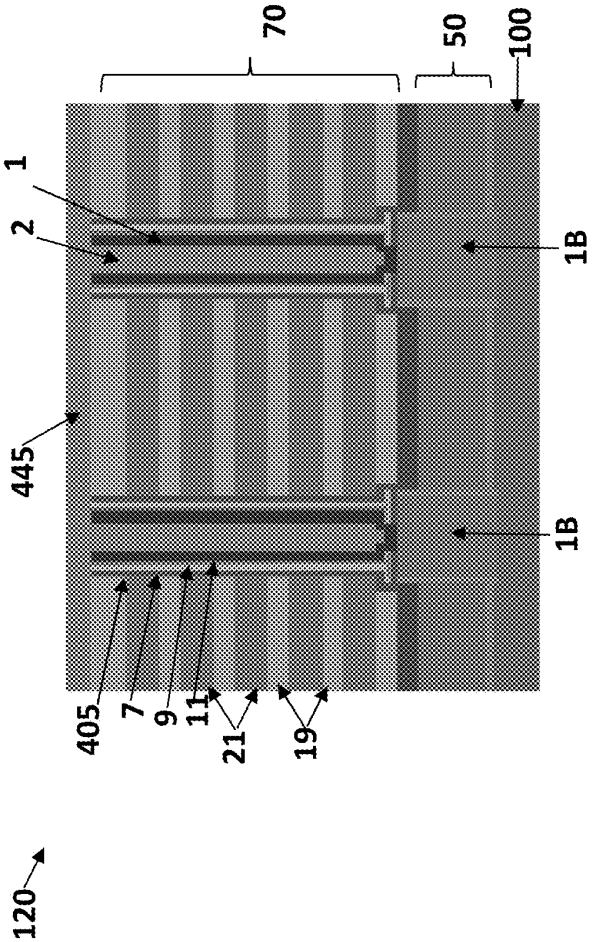


Fig. 4E

Fig. 4F

Fig. 4G

Fig. 4H



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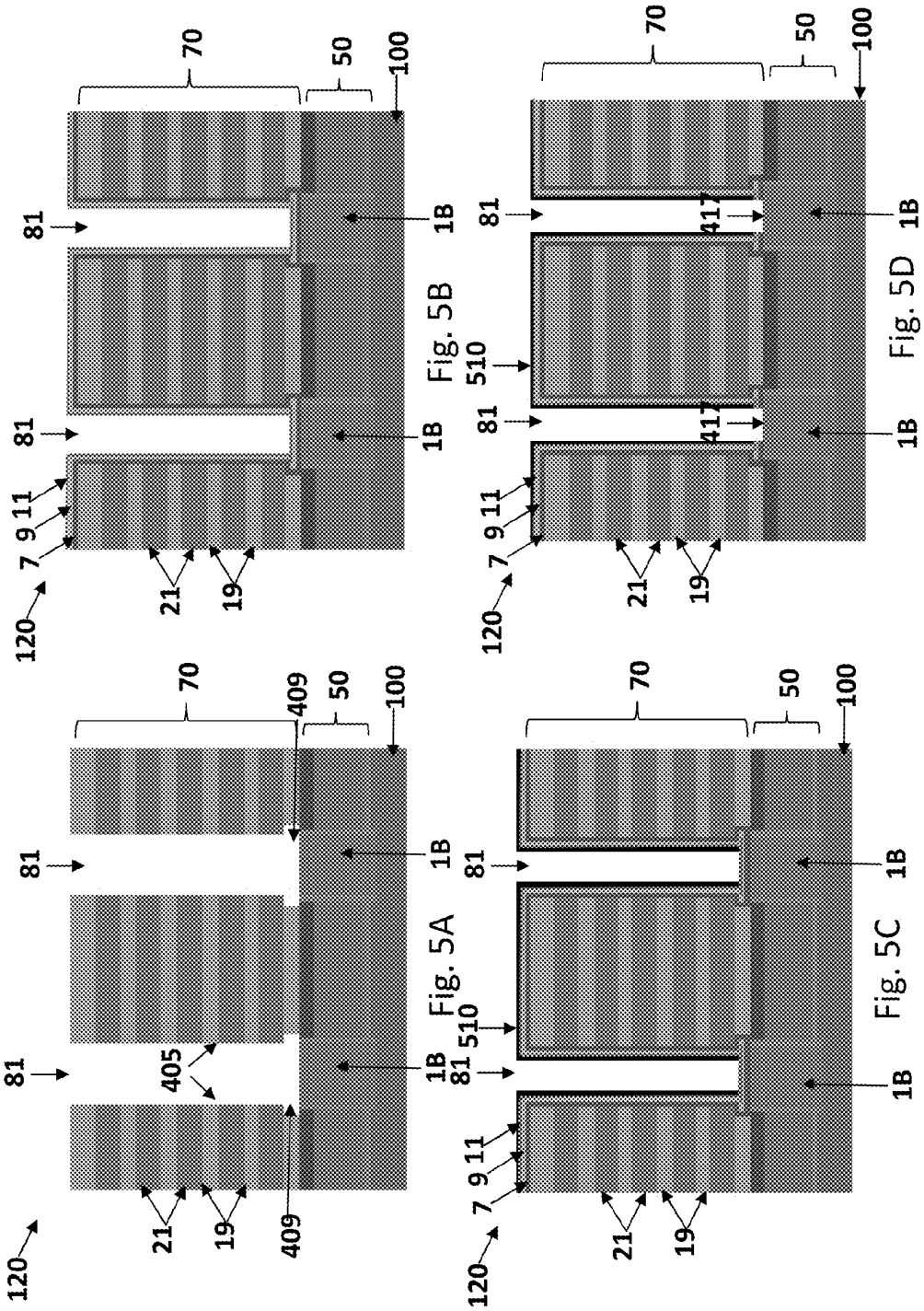
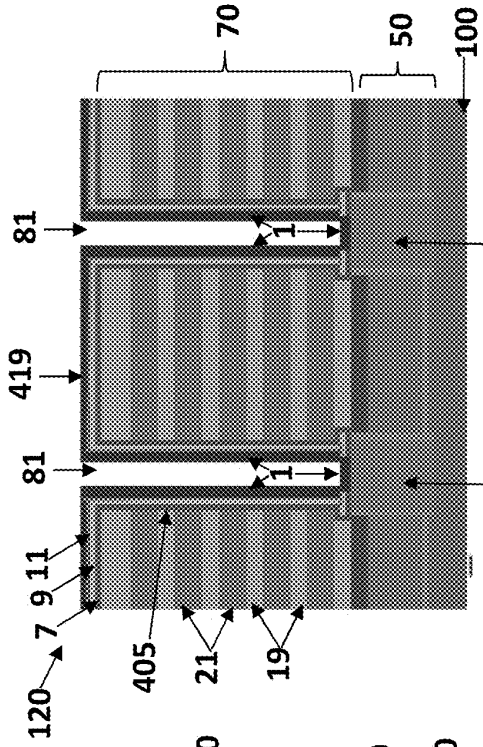


Fig. 5B

Fig. 5D

Fig. 5A

Fig. 5C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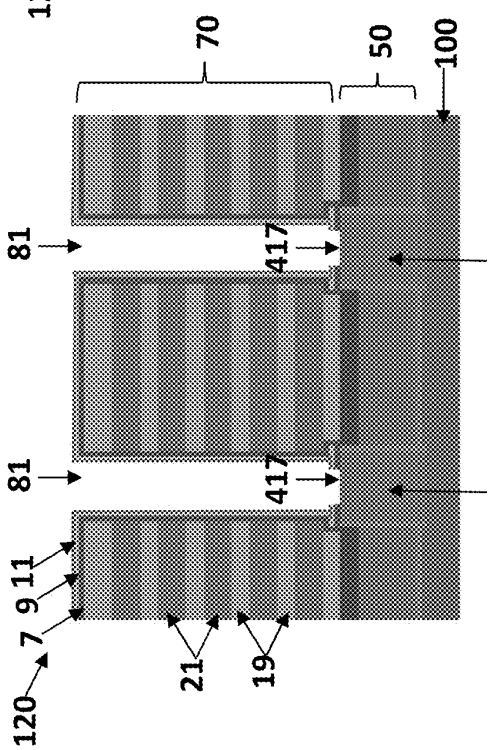
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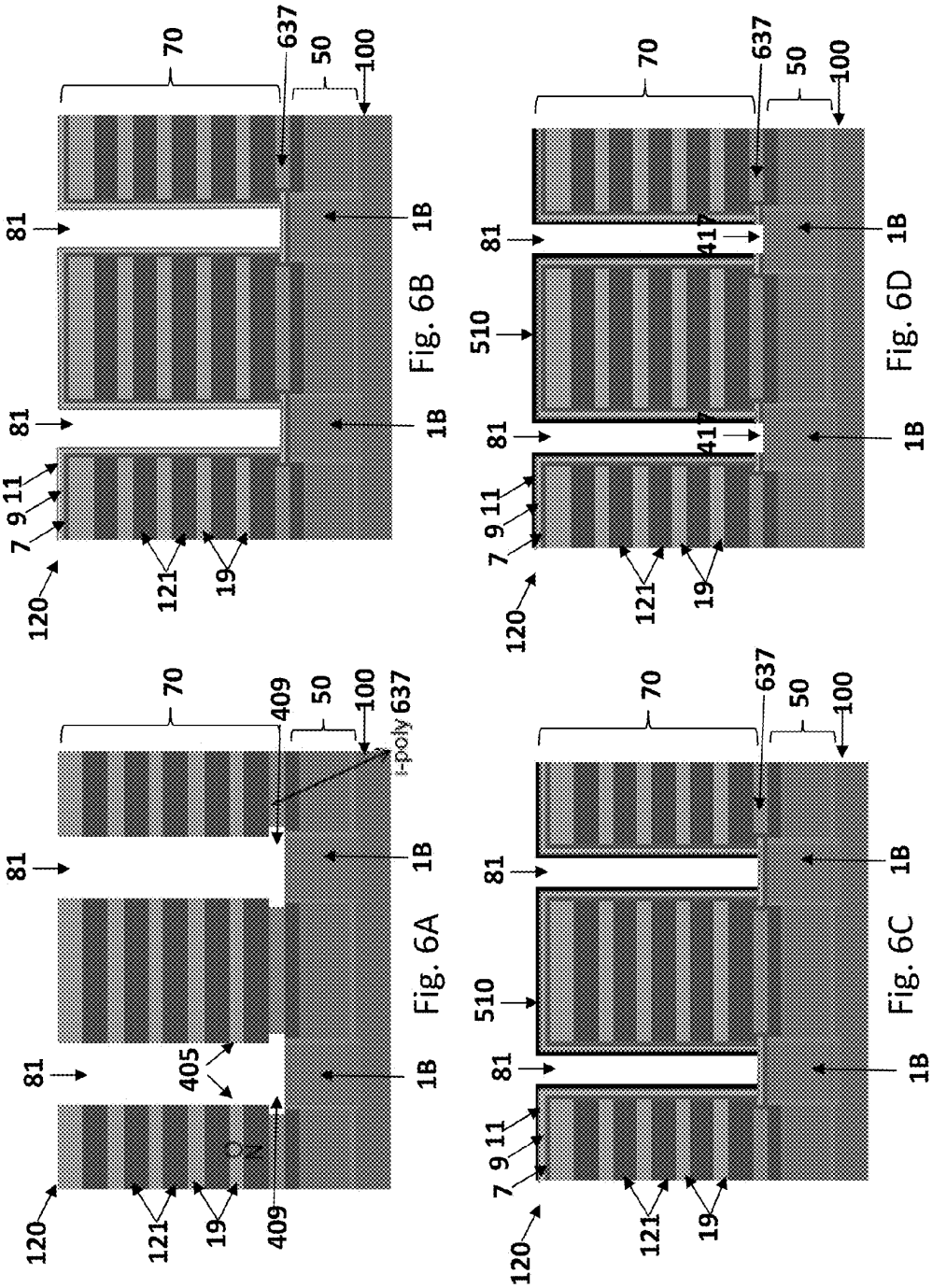
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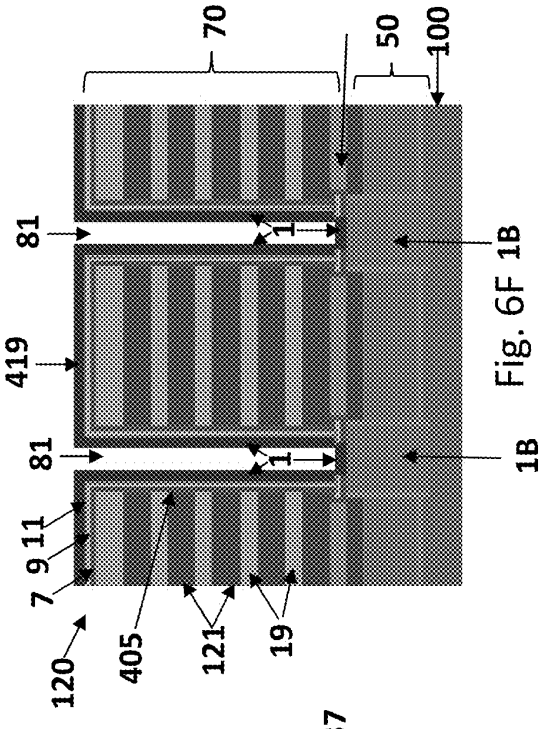
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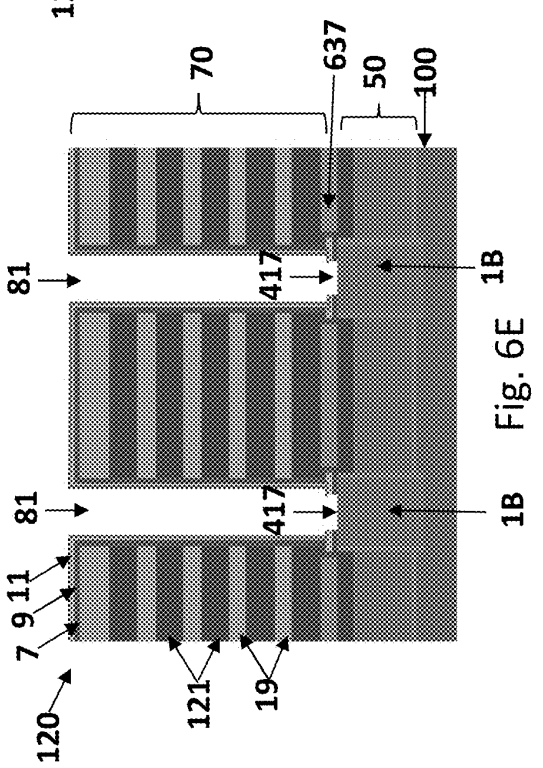
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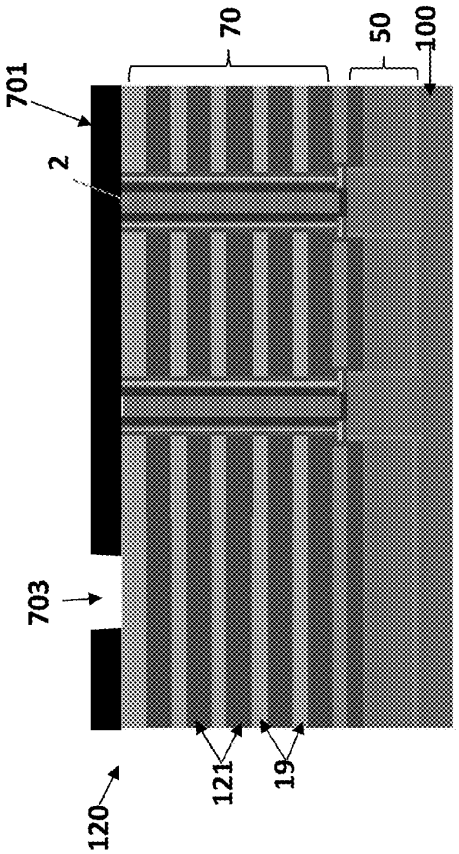
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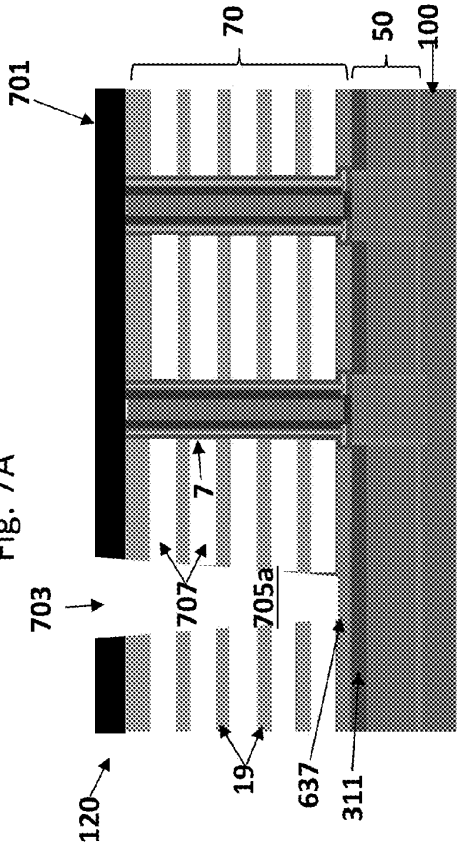
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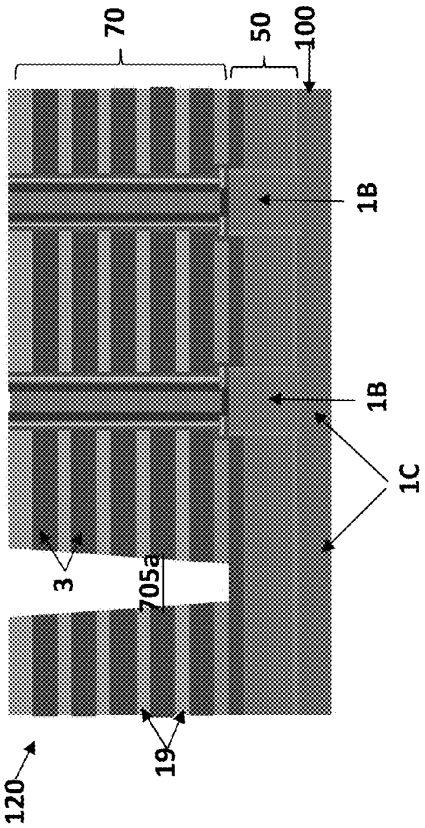
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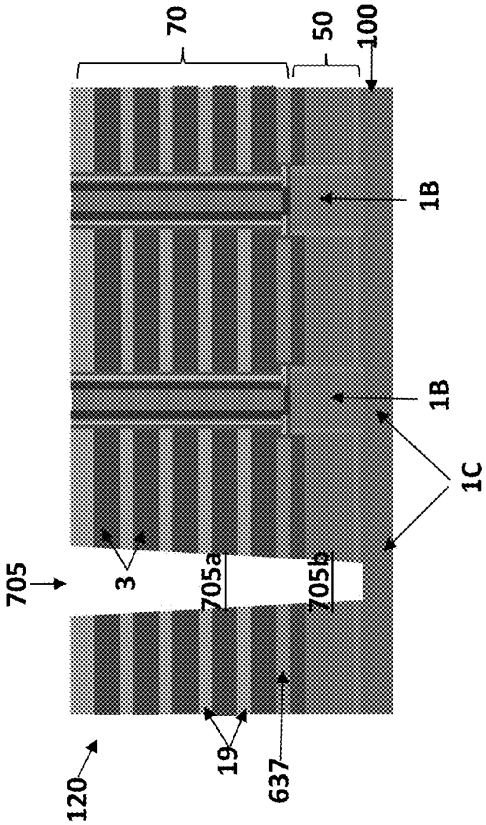
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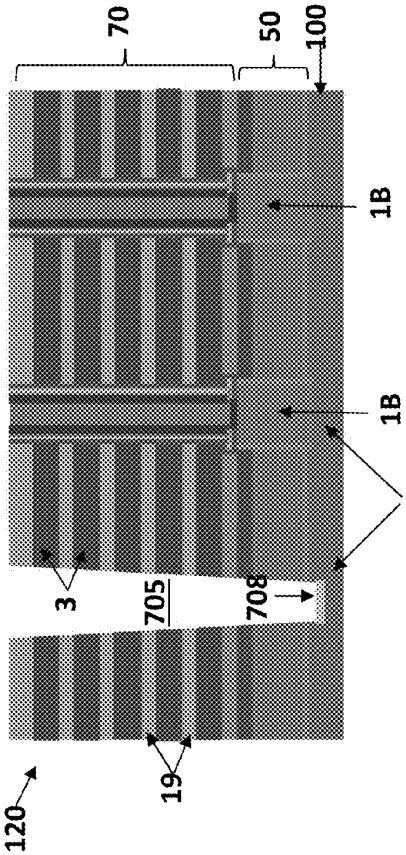
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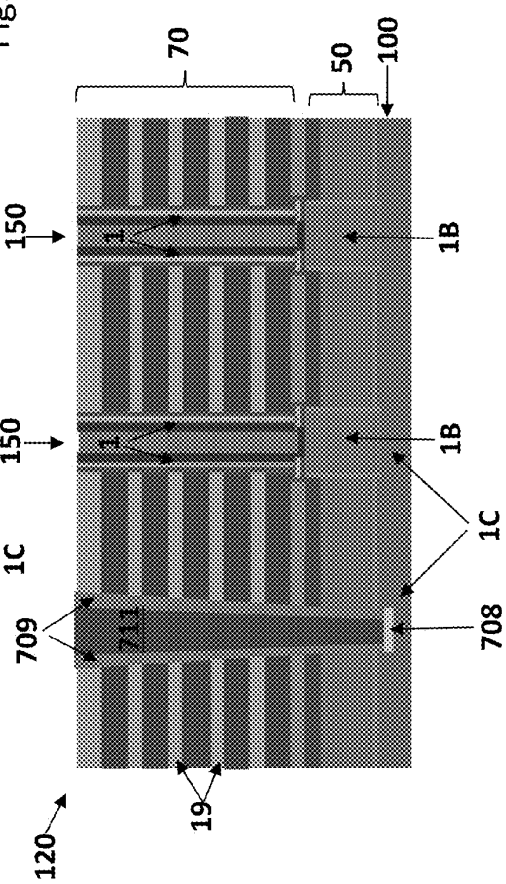
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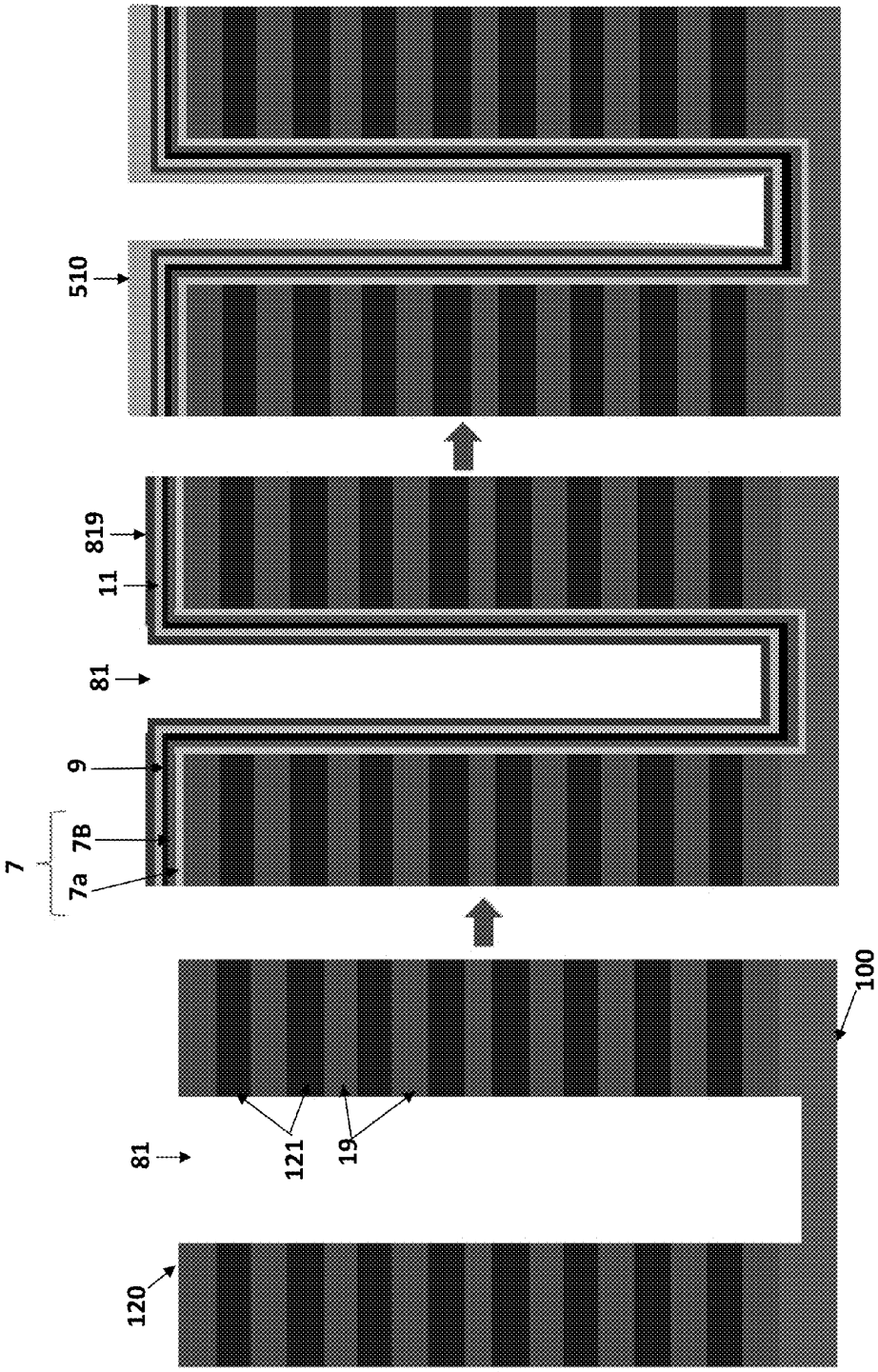

Fig. 8C

Fig. 8B

Fig. 8A

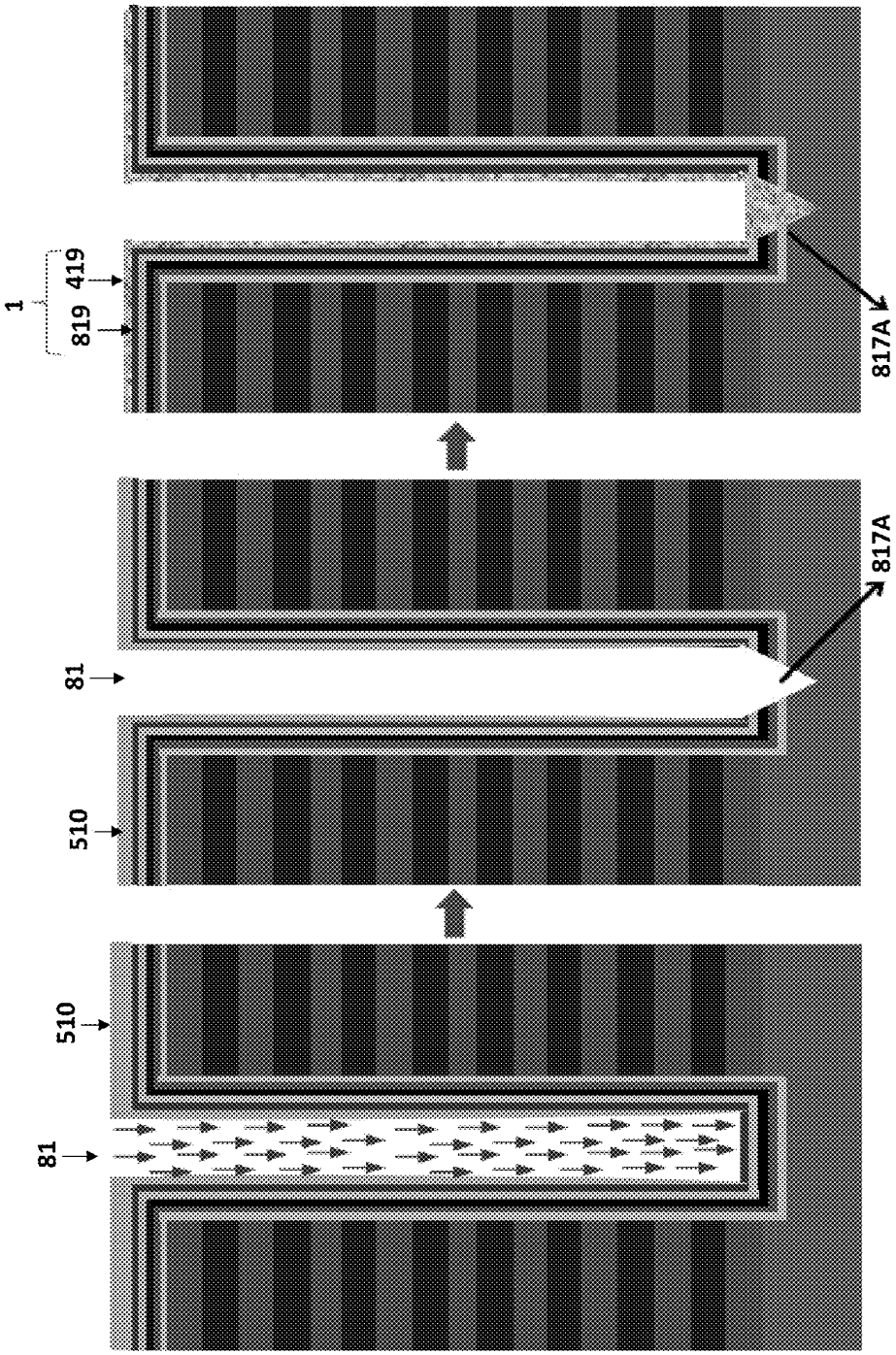

Fig. 8F

Fig. 8E

Fig. 8D

Fig. 10

Fig. 9

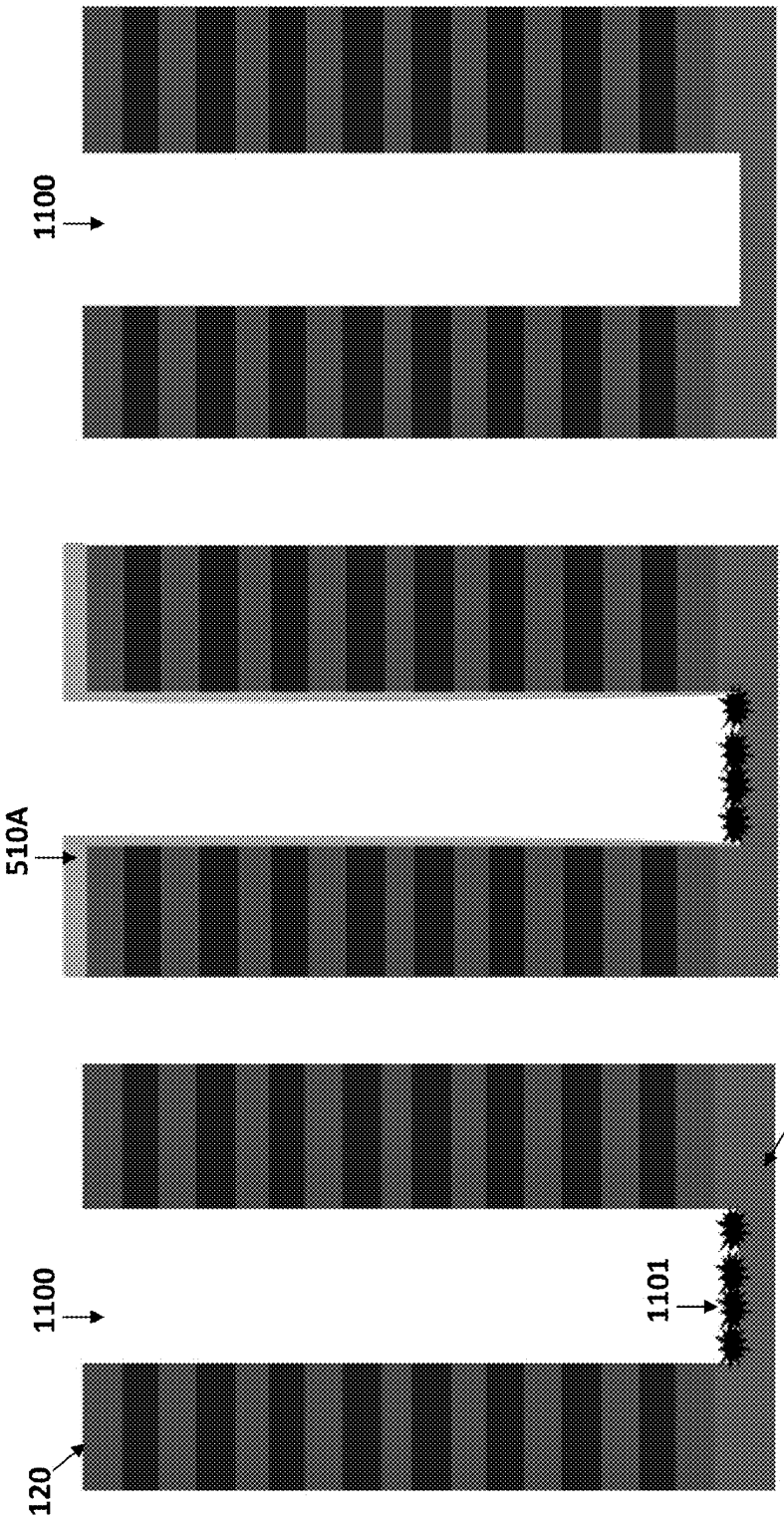

Fig. 11C

Fig. 11B

Fig. 11A

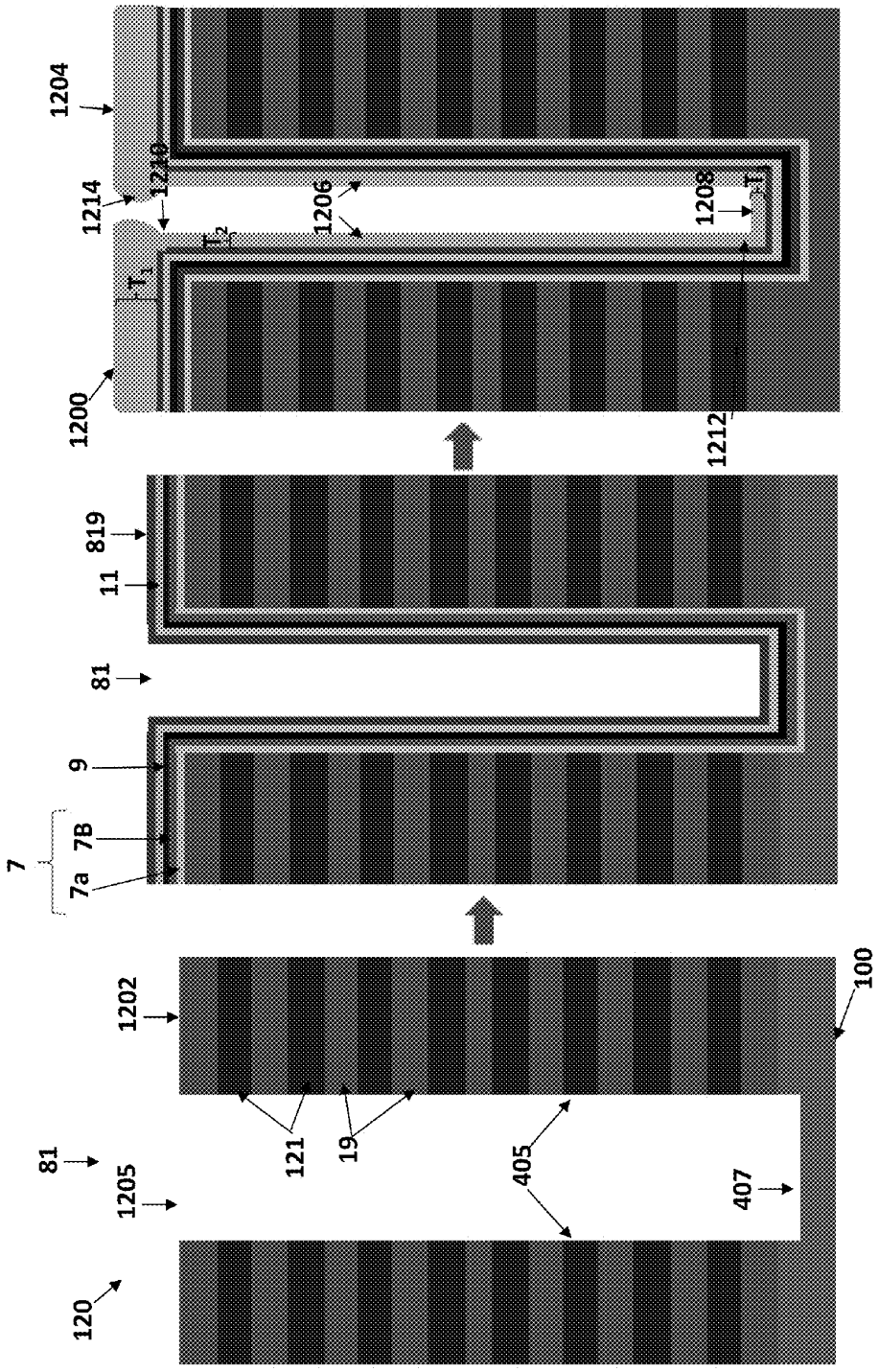

Fig. 12C

Fig. 12B

Fig. 12A

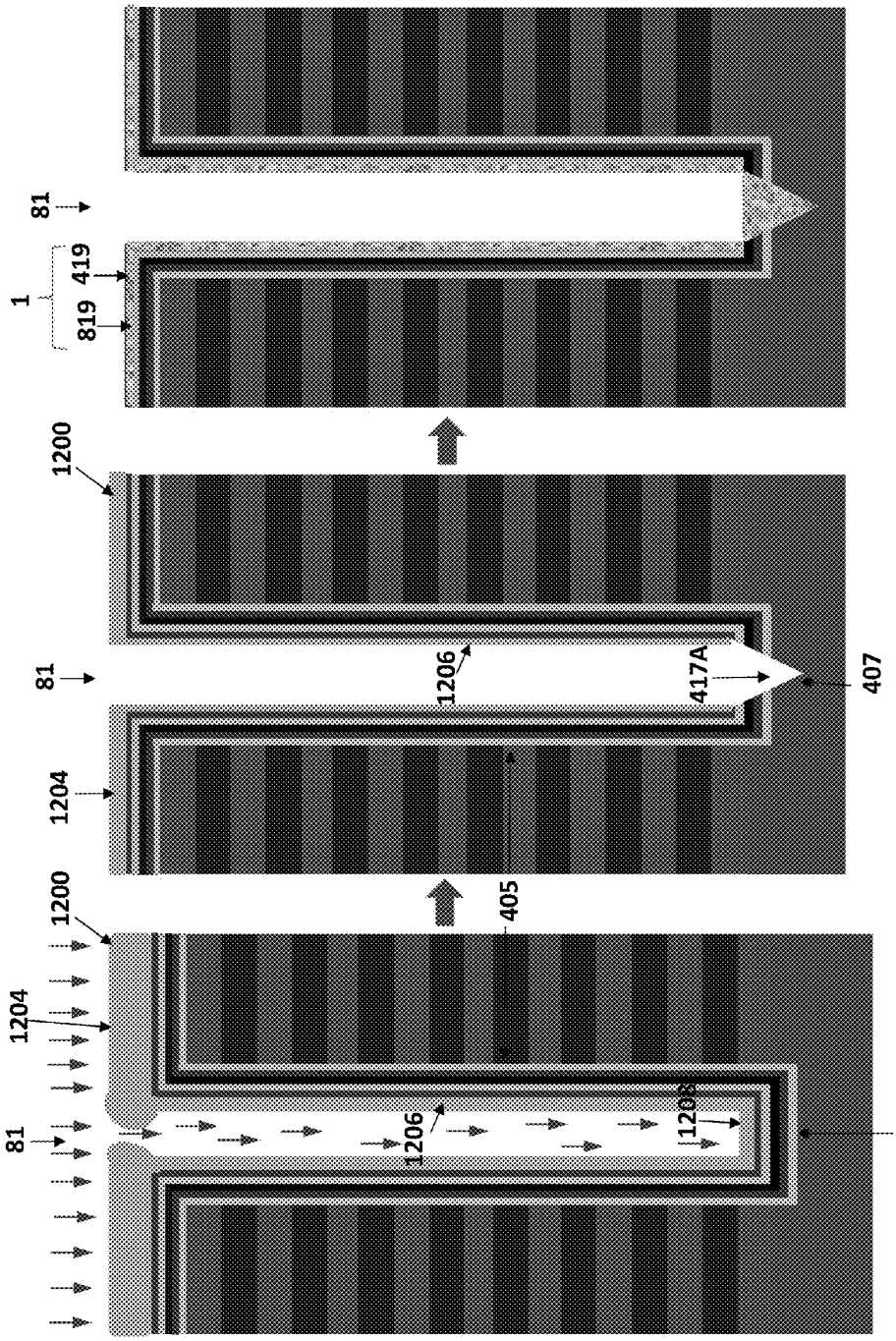

Fig. 12D

Fig. 12E

Fig. 12F

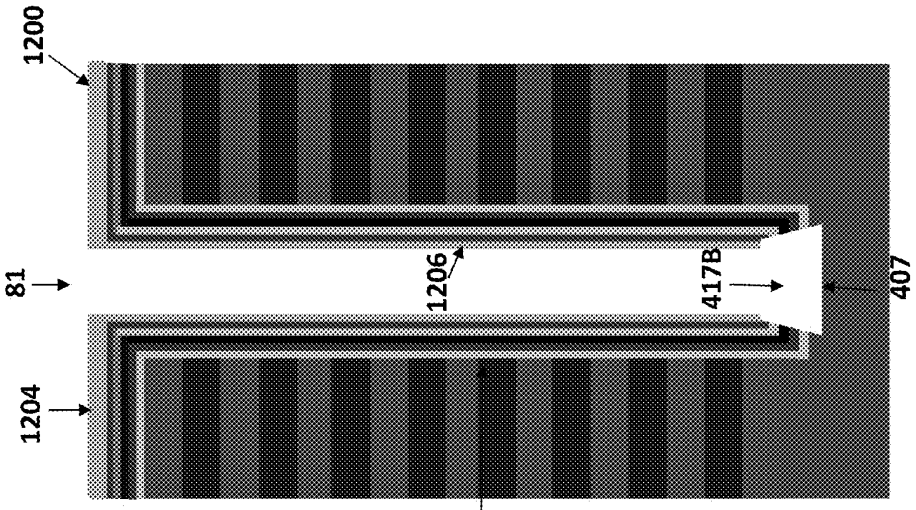

Fig. 14

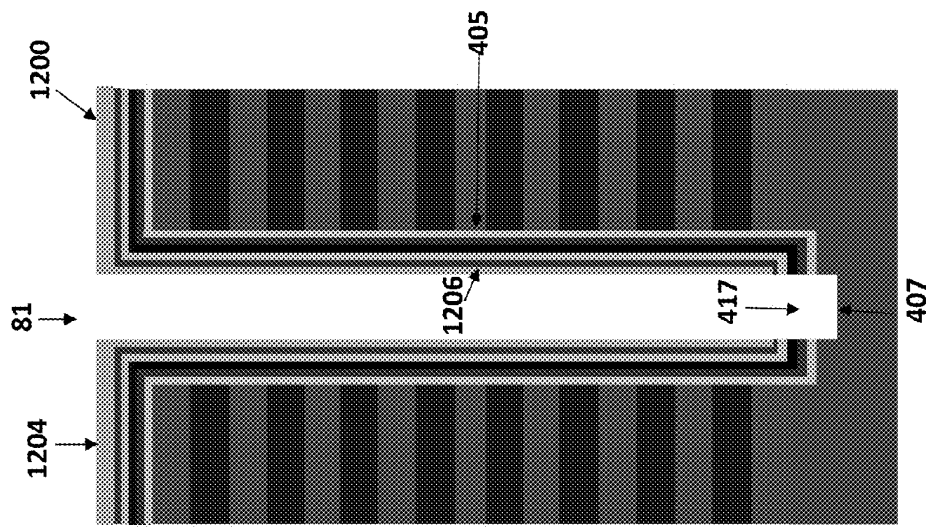

Fig. 13

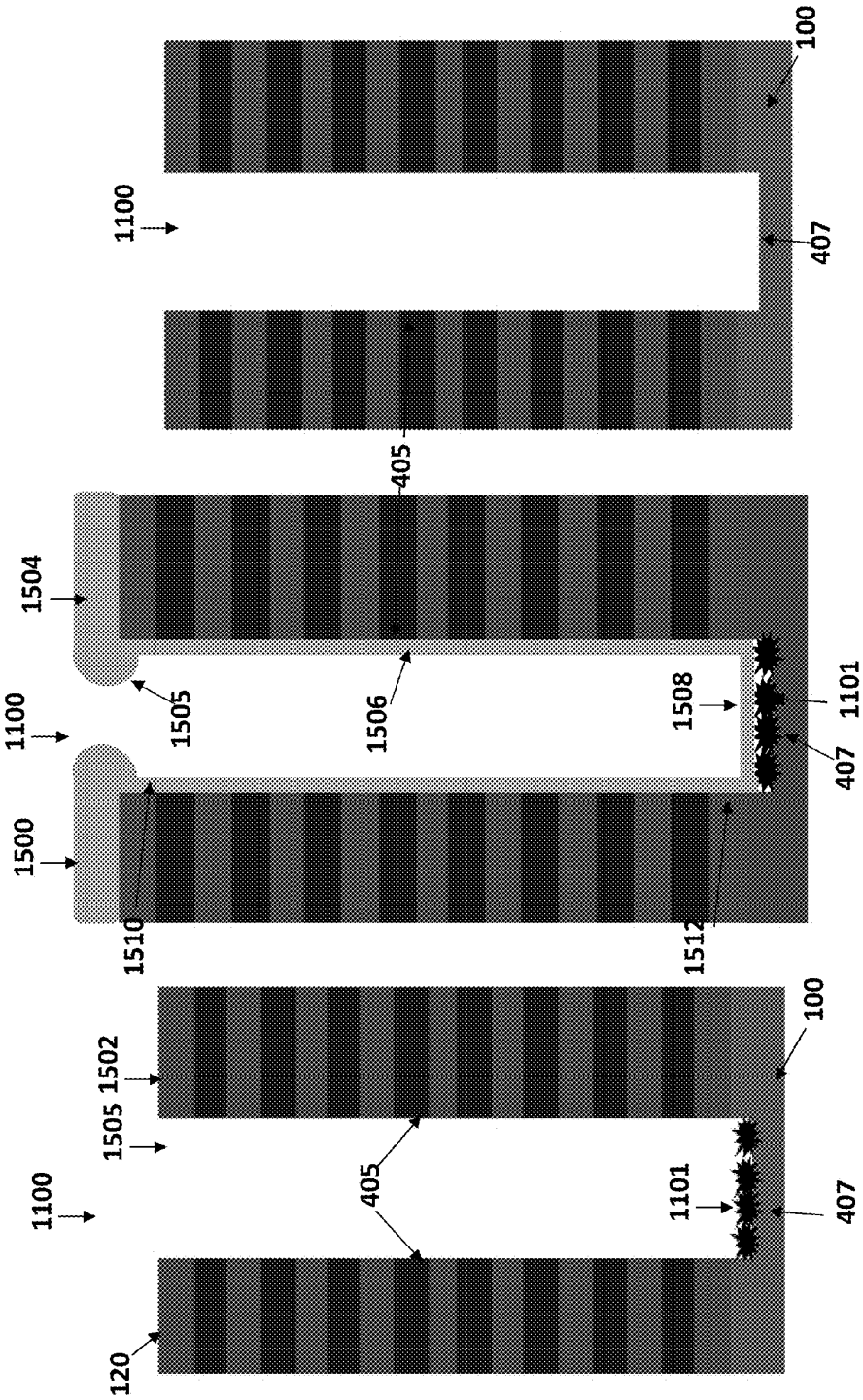

Fig. 15A

Fig. 15B

Fig. 15C

SPACER PASSIVATION FOR HIGH-ASPECT RATIO OPENING FILM REMOVAL AND CLEANING

RELATED APPLICATION

This application claims the benefit of priority to U.S. Provisional Application No. 62/030,351, filed Jul. 29, 2014, the entire contents of which are incorporated herein by reference.

FIELD

The present disclosure relates generally to the field of semiconductor devices and specifically to three dimensional non-volatile memory, such as vertical NAND strings, and other three dimensional devices and methods of making thereof.

BACKGROUND

Recently, ultra high density storage devices have been proposed using a three-dimensional (3D) stacked memory structure sometimes referred to as a Bit Cost Scalable (BiCS) architecture. For example, a 3D NAND stacked memory device can be formed from an array of alternating conductive and dielectric layers. A memory hole is formed through the layers to define many memory layers simultaneously. A NAND string is then formed by filling the memory hole with appropriate materials. A straight NAND string extends in one memory hole, while a pipe- or U-shaped NAND string (p-BiCS) includes a pair of vertical columns of memory cells. Control gates of the memory cells may be provided by the conductive layers.

SUMMARY

Embodiments relate to a method of making a semiconductor device including forming a stack of alternating layers of a first material and a second material over a semiconductor material, etching the stack to form at least one front side opening in the stack, forming a memory film over a sidewall and bottom surface of the at least one front side opening, forming a sacrificial cover layer over the memory film such that the sacrificial cover layer is deposited so that it preferentially forms over a sidewall portion of the memory film located over a sidewall of the at least one front side opening but not over a bottom portion of the memory film located over a bottom of the at least one front side opening, etching the bottom portion of the memory film at the bottom of the at least one front side opening to expose an upper surface of the semiconductor material while the sacrificial material layer protects the sidewall portion of the memory film during the etching step, removing the sacrificial cover layer, and forming a semiconductor channel material in the at least one front side opening.

In embodiments, the method further includes at least one of (a), (b) or (c):

(a) the memory film comprises a composite blocking dielectric comprising a high-k dielectric layer and a silicon oxide layer; and/or

(b) forming a semiconductor cover layer between the memory film and the sacrificial cover layer and etching a bottom portion of the semiconductor cover layer at the bottom of the at least one front side opening to expose the upper surface of the semiconductor material while the sacrificial material layer protects a sidewall portion of the semiconductor channel material during the etching step; and/or

(c) etching the bottom portion of the memory film at the bottom of the at least one front side opening forms either a tapered opening or a reverse tapered opening.

Another embodiment relates to a method of making a semiconductor device which includes forming a stack of alternating layers of a first material and a second material over a substrate, etching the stack to form at least one opening in the stack such that a damaged region is located on a bottom surface of the at least one opening, forming a masking layer on a sidewall of the at least one opening while the bottom surface of the at least one opening is not covered by the masking layer, and further etching the bottom surface of the at least one opening remove the damaged region.

Another embodiment relates to a method of making a semiconductor device that includes forming a stack of alternating layers of a first material and a second material over a semiconductor material, etching the stack to form at least one front side opening in the stack, the at least one front side opening including a top opening defined by a top surface of the stack, a bottom surface opposite the top surface, and a sidewall defined at least in part by the alternating layers of the stack and extending between the top opening and the bottom surface, forming a memory film over the sidewall and bottom surface of the at least one front side opening, forming a sacrificial cover layer over the stack such that the sacrificial cover layer is deposited so that it forms a first portion over the top surface of the stack and at least partially covering the top opening of the at least one front side opening and a second portion over a sidewall portion of the memory film located over the sidewall of the at least one front side opening, wherein the first portion has a thickness that is greater than the thickness of the second portion, etching the bottom portion of the memory film at the bottom of the at least one front side opening to expose an upper surface of a semiconductor material while the sacrificial cover layer protects the sidewall portion of the memory film during the etching step, removing the sacrificial cover layer, and forming a semiconductor channel in the at least one front side opening.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1**A-**1**B are respectively side cross sectional and top cross sectional views of a NAND string of one embodiment. FIG. **1**A is a side cross sectional view of the device along line Y-Y' in FIG. **1**B, while FIG. **1**B is a side cross sectional view of the device along line X-X' in FIG. **1**A.

FIGS. **1**C-**1**D are respectively side cross sectional and top cross sectional views of a NAND string of another embodiment. FIG. **1**C is a side cross sectional view of the device along line Y-Y' in FIG. **1**D, while FIG. **1**D is a side cross sectional view of the device along line X-X' in FIG. **1**C.

FIG. **2** is a partial side cross-sectional view of a memory device comprising a plurality of NAND strings formed in a stack of material layers over a substrate.

FIGS. **3**A-**3**H are partial side cross-sectional views of a stack of material layers over a substrate and illustrate a method of forming a select gate level of a memory device according to an embodiment.

FIGS. **4**A-**4**I are partial side cross-sectional views of a material layer stack over a substrate that illustrate a method of fabricating NAND memory strings according to one embodiment.

FIGS. **5**A-**5**F are partial side cross-sectional views of a material layer stack over a substrate that illustrate a method of fabricating NAND memory strings according to another embodiment.

FIGS. **6**A-**6**F are partial side cross-sectional views of a material layer stack over a substrate that illustrate a method of fabricating NAND memory strings according to another embodiment.

FIGS. **7**A-**7**F are partial side cross-sectional views of a material layer stack that illustrate a method of forming control gate electrodes and a select line for a plurality of NAND memory strings.

FIGS. **8**A-**8**F are partial side cross-sectional views of a material layer stack over a substrate that illustrate a method of fabricating NAND memory strings according to another embodiment.

FIGS. **9** and **10** are partial side cross-sectional views of a material layer stack over a substrate that illustrate a method of fabricating NAND memory strings according to alternative embodiments.

FIGS. **11**A-**11**C are partial side cross-sectional views of a material layer stack over a substrate that illustrate a method of fabricating NAND memory strings according to another embodiment.

FIGS. **12**A-**12**F are partial side cross-sectional views of a material layer stack over a substrate that illustrate a method of fabricating NAND memory strings according to another embodiment.

FIGS. **13** and **14** are partial side cross-sectional views of a material layer stack over a substrate that illustrate a method of fabricating NAND memory strings according to alternative embodiments.

FIGS. **15**A-**15**C are partial side cross-sectional views of a material layer stack over a substrate that illustrate a method of fabricating NAND memory strings according to another embodiment.

DETAILED DESCRIPTION

The embodiments of the invention provide a method for fabricating a semiconductor device, such as a three dimensional monolithic memory array comprising a plurality of NAND memory strings.

A monolithic three dimensional memory array is one in which multiple memory levels are formed above a single substrate, such as a semiconductor wafer, with no intervening substrates. The term "monolithic" means that layers of each level of the array are directly deposited on the layers of each underlying level of the array. In contrast, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device. For example, non-monolithic stacked memories have been constructed by forming memory levels on separate substrates and adhering the memory levels atop each other, as in Leedy, U.S. Pat. No. 5,915,167, titled "Three Dimensional Structure Memory." The substrates may be thinned or removed from the memory levels before bonding, but as the memory levels are initially formed over separate substrates, such memories are not true monolithic three dimensional memory arrays.

In some embodiments, a monolithic three dimensional NAND string **150** comprises a semiconductor channel **1** having at least one end portion extending substantially perpendicular to a major surface **100***a* of a substrate **100**, as shown in FIGS. **1**A, **1**C and **2**. For example, the semiconductor channel **1** may have a pillar shape extending through a plurality of memory device levels (Level A, Level B, etc.) and the entire pillar-shaped semiconductor channel in the memory device levels extends substantially perpendicularly to the major surface **100***a* of the substrate **100**, as shown in FIGS. **1**A, **1**C and **2**. The channels **1** may be electrically connected to first and second (e.g., source and drain) electrodes **102**, **103** which are schematically shown in FIGS. **1**A and **1**C. The first (e.g., source) electrode **102** may connect to the bottom of the channel **1** and the second (e.g., drain electrode **103**) may connect to the top of the channel **1**. The NAND string **150** may further include drain-side and source-side select or access transistors (not shown in FIGS. **1**A-**2** for clarity) which may be located above and below the memory levels of the NAND string **150**, respectively.

In some embodiments, the semiconductor channel **1** may be a filled feature, as shown in FIGS. **1**C and **1**D. In some other embodiments, the semiconductor channel **1** may be hollow, for example a hollow cylinder filled with an insulating fill material **2**, as shown in FIGS. **1**A and **1**B. In these embodiments, an insulating fill material **2** may be formed to fill the hollow part surrounded by the semiconductor channel **1**.

A memory device **180** may comprise a plurality of NAND strings **150** formed in a stack **120** of material layers over the substrate **100**, as shown in FIG. **2**. The substrate **100** can be any semiconducting substrate known in the art, such as monocrystalline silicon, IV-IV compounds such as silicon-germanium or silicon-germanium-carbon, III-V compounds, II-VI compounds, epitaxial layers over such substrates, or any other semiconducting or non-semiconducting material, such as silicon oxide, glass, plastic, metal or ceramic substrate. The substrate **100** may include integrated circuits fabricated thereon, such as driver circuits for a memory device.

Any suitable semiconductor materials can be used for semiconductor channel **1**, for example silicon, germanium, silicon germanium, or other compound semiconductor materials, such as III-V, II-VI, or conductive or semiconductive oxides, etc. The semiconductor material may be amorphous, polycrystalline or single crystal. The semiconductor channel material may be formed by any suitable deposition methods. For example, in one embodiment, the semiconductor channel material is deposited by low pressure chemical vapor deposition (LPCVD). In some other embodiments, the semiconductor channel material may be a recyrstallized polycrystalline semiconductor material formed by recrystallizing an initially deposited amorphous semiconductor material.

The insulating fill material **2** may comprise any electrically insulating material, such as silicon oxide, silicon nitride, silicon oxynitride, or other high-k insulating materials.

The monolithic three dimensional NAND strings **150** further comprise a plurality of control gate electrodes **3** as shown in FIGS. **1**A-**2**. The control gate electrodes **3** may comprise a portion having a strip shape extending substantially parallel to the major surface **100***a* of the substrate **100**. The plurality of control gate electrodes **3** comprise at least a first control gate electrode **3***a* located in a first device level (e.g., memory device level A) and a second control gate electrode **3***b* located in a second device level (e.g., memory device level B) located over the major surface **100***a* of the substrate **100** and below the device level A. The control gate material may comprise any one or more suitable conductive or semiconductor control gate material known in the art, such as doped polysilicon, tungsten, tungsten nitride, copper, aluminum, tantalum, titanium, cobalt, titanium nitride, alloys thereof or combination of these materials. For example, the control gate material in FIGS. **1**A-**1**D may

comprise a conductive metal or metal alloy, such as tungsten, titanium nitride, and/or tungsten nitride, while the control gate material in FIG. **2** may comprise doped polysilicon.

A blocking dielectric **7** is located adjacent to the control gate(s) **3** and may surround the control gate **3**, as shown in FIGS. **1**A and **1**C. Alternatively, a straight blocking dielectric layer **7** may be located only adjacent to an edge (i.e., minor surface) of each control gate **3**, as shown in FIG. **2**. The blocking dielectric **7** may comprise one or more layers having plurality of blocking dielectric segments located in contact with a respective one of the plurality of control gate electrodes **3**. Alternatively, the blocking dielectric **7** may comprise one or more continuous layers which extend the entire length of the memory cell portion of the NAND string **150**, as shown in FIG. **2**.

The monolithic three dimensional NAND string also comprise a charge storage region **9**. The charge storage region **9** may comprise one or more continuous layers which extend the entire length of the memory cell portion of the NAND string as shown in FIG. **2**. For example, the charge storage region **9** may comprise an insulating charge trapping material, such as a silicon nitride layer. Alternatively, the charge storage region may comprise a plurality of discrete charge storage regions or segments **9** located between the blocking dielectric **7** and the channel **1**, as shown in FIGS. **1**A and **1**C. The discrete charge storage regions **9** may comprise a plurality of vertically spaced apart, conductive (e.g., metal such as tungsten, molybdenum, tantalum, titanium, platinum, ruthenium, and alloys thereof, or a metal silicide such as tungsten silicide, molybdenum silicide, tantalum silicide, titanium silicide, nickel silicide, cobalt silicide, or a combination thereof), or semiconductor (e.g., polysilicon) floating gates. Alternatively, the discrete charge storage regions **9** may comprise an insulating charge trapping material, such as silicon nitride segments. Alternatively, the charge storage region **9** may comprise conductive nanoparticles, such as metal nanoparticles, for example ruthenium nanoparticles.

The tunnel dielectric **11** of the monolithic three dimensional NAND string is located between charge storage region **9** and the semiconductor channel **1**.

The blocking dielectric **7** and the tunnel dielectric **11** may be independently selected from any one or more same or different electrically insulating materials, such as silicon oxide, silicon nitride, silicon oxynitride, or other insulating materials, such as metal oxide materials, for example aluminum oxide or hafnium oxide. The blocking dielectric **7** and/or the tunnel dielectric **11** may include multiple layers of silicon oxide, silicon nitride and/or silicon oxynitride (e.g., ONO layers).

In various embodiments, the three-dimensional NAND string **150** may have a generally pillar shape that extends substantially perpendicular to the major surface of the substrate **100**, with a first (e.g., drain) electrode **103** that connects to the NAND string **150** at the top of the NAND string **150** (i.e., distal to the substrate **100**) and a second (e.g., source) electrode **102** that connects to the NAND string **150** at the bottom of the NAND string **150** (i.e., proximate to the substrate **100**). In embodiments, each NAND string **150** may have a first select or access transistor (e.g., a drain-side select gate transistor) located above the memory levels of the NAND string **150**, and a second select or access transistor (e.g., a source-side select gate transistor) located below the memory levels of the NAND string **150**. Since the second or source-side select gate transistor is located below the memory levels of the NAND string **150**, forming effective contact between the semiconductor channel **1** of the NAND string **150** and the underlying select gate region of the device has proven challenging, particularly for high aspect ratio NAND strings **150**.

Various embodiments include methods of making a memory device such as a monolithic three-dimensional NAND string memory device. FIGS. **3**A-**3**H illustrate a method of making a memory device according to a first, non-limiting embodiment of the invention. The method of FIGS. **3**A-**3**H may result in a higher quality gate insulating layer **306** for the source side select gate transistor **301**. Specifically, a select gate electrode **304** may be formed over a first gate insulating layer **303** over a major surface **100***a* of the substrate **100**. Then, the select gate electrode **304** and the first gate insulating layer **303** are etched through a mask to form one or more openings **314** having vertically-extending sidewalls **315**, **316** and a horizontally-extending bottom surface **317** that exposes the surface of the substrate **100**. A second gate insulating layer **306** is formed on the sidewalls **315**, **316** and bottom surface **317** of the openings **314**, and a sacrificial carbon spacer layer **319** is formed over the second gate insulating layer **306** on the sidewalls **315**, **316** of the opening **314**, but not over the bottom surface **317** of the opening **314**. Then, the second gate insulating layer **306** is etched over the bottom surface **317** of the opening **314** to expose the substrate, and the sacrificial carbon spacer layer **319** is removed (such as by ashing) to expose the gate insulating layer **306** over the sidewalls **315**, **316** of the opening **314**. A protrusion comprising a semiconductor material, which later forms a channel portion **1**B of the NAND string **150**, is then formed in the opening **314**, with the gate insulating layer **306** on the sidewalls **315**, **316** of the opening **314** being located between the select gate electrode **304** and first and second side surfaces of the protrusion. The gate insulating layer **306** is not subject to processing damage because it is protected by the sacrificial carbon spacer layer **319** while the bottom surface of the opening **314** is etched to expose the surface of the semiconductor substrate **100**. Further, in some embodiments the sacrificial carbon spacer layer **319** may be removed using a process (e.g., ashing) that does not damage or degrade the gate insulating layer **306**. Thus, the vertical portions of the gate insulating layer **306** are not subjected to etching damage and may be higher quality than in prior art devices.

FIG. **3**A illustrates a select gate portion **50** of a NAND string memory device according to one embodiment. To form the select gate portion **50** of FIG. **3**A, a first gate insulating layer **303** (e.g., an oxide layer) may be formed over the surface of a semiconductor substrate **100**. The first gate insulating layer **303** may be formed by oxidation of the exposed surface of the semiconductor (e.g., silicon) substrate **100**. Any suitable oxidation process may be used, such as radical oxidation, dry oxidation, wet oxidation, etc to form a silicon oxide layer **303**. Alternatively, rather than oxidizing the exposed surface, a layer **303** of insulating material, such as silicon oxide, may be deposited by chemical vapor deposition ("CVD") or sputtering.

A select gate electrode **304** may be formed over the first gate insulating layer **303**. The select gate electrode **304** may comprise any suitable conductive material(s), such as a doped semiconductor material, a metal and/or metal alloy, and may be formed using any suitable process, such as via physical or chemical vapor deposition processes. An upper layer **311** of an insulating material (e.g., silicon nitride) may be provided over the select gate electrode **304**.

A mask layer **313** is then formed over the upper layer **311** of insulating material. The mask layer **313** may comprise

any suitable mask layer, such as photoresist or a hard mask material, such as amorphous carbon, silicon nitride, metal, etc., and may be patterned using photolithography. As shown in FIG. **3**B, the mask layer **313** is patterned into a mask pattern defining open portions **312** in which layer **311** is exposed. The upper layer **311** of insulating material, the select gate electrode **304** and the first gate insulating layer **303** are etched through the mask **313** to the substrate **100** to form openings **314** corresponding to the locations of the open portions **312** in the mask **313** as shown in FIG. **3**B. The layers **311**, **304**, **306** may be etched using reactive ion etching (RIE), for example. The select gate electrode **304** and the first gate insulating layer **306** may form at least a portion of the sidewalls **315**, **316** of each opening **314**, and the substrate **100** (e.g., surface **100***a*) may form the bottom surface **317** of each opening **314**. The sidewalls **315**, **316** may be opposite sides on one sidewall of a cylindrical opening **314**. The mask layer **313** may be removed, as shown in FIG. **3**C. A second gate insulating layer **306** may be formed over the upper layer **311** of insulating material and in the openings **314** over the sidewalls **315**, **316** and bottom surface **317** of each opening **314**, as shown in FIG. **3**C. The second gate insulating layer **306** may comprise an insulating material, such as silicon oxide, and may be deposited using a suitable process, such as by chemical vapor deposition ("CVD") or sputtering. The mask layer **313** may be removed, as shown in FIG. **3**C.

A sacrificial carbon spacer layer **319** may then be formed such that the sacrificial carbon spacer layer **319** preferentially forms over the second gate insulating layer **306** on the sidewalls **315**, **316** but not on the bottom surface **317** of the openings **314**. The sacrificial carbon spacer layer **319** may comprise a carbon material that is deposited by any suitable process, such as CVD. The selective formation of the sacrificial carbon spacer layer **319** on the sidewalls **315**, **316** but not on the bottom surface **317** may be promoted by controlling the parameters of the carbon deposition, such as the carbon deposition temperature, the thickness of the carbon layer **319** and the aspect ratio of the openings **314**. The deposition parameters may otherwise be similar to non-conformal deposition processes.

In FIG. **3**D, the second gate insulating layer **306** may be etched on the bottom surface **317** of the openings **314** to expose the surface of the semiconductor substrate **100**. In embodiments, the second gate insulating layer **306** may be etched using a dry etch process, such as RIE. During the etching, the sacrificial carbon spacer layer **319** may protect the vertically extending portions of the second gate insulating layer **306** over the sidewalls **315**, **316** of the openings **314** from etching damage. Following the etching, the sacrificial carbon spacer layer **319** may be removed, such as by ashing, to expose the vertically extending portions of the second gate insulating layer **306** as shown in FIG. **3**D. The second gate insulating layer **306** may remain over the upper layer of insulating material **311** (not shown for clarity).

In FIG. **3**E, protrusions **1**B comprising a semiconductor material are formed within the openings **314** and contact the surface (e.g., surface **100***a*) of the semiconductor substrate **100**. As shown in FIG. **3**E, an epitaxial single crystal semiconductor layer, such as a single crystal silicon layer may be epitaxially grown on the exposed major surface **100***a* of the substrate **100** over the bottom surfaces **317** of the openings **314**. The epitaxial single crystal semiconductor layer may optionally be planarized, such as by chemical mechanical polishing (CMP) or an etch-back process, to remove any portions of the protrusion **1**B extending above the top of the openings **314** and to define a top surface **325** of the protrusions **1**B, which may be made planar with the top surface of the upper layer of insulating material **311**, as shown in FIG. **3**E. The second gate insulating layer **306** may also be removed from above the upper layer of insulating material **311** during planarization (e.g., CMP), and layer **311** may act as a polish stop. The protrusions **1**B may optionally be implanted to form doped regions **326** (e.g., N+ doped regions) proximate the top surfaces **325** of the protrusions **1**B, as shown in FIG. **3**F.

In alternative embodiments, the protrusions **1**B may be formed by forming an epitaxial single crystal semiconductor (e.g., silicon) layer on the exposed surface of the substrate to partially fill the openings **314**, and forming at least one layer of a second material, such as a second semiconductor material (e.g., a polycrystalline semiconductor material, such as polysilicon), a metal and/or a metal nitride, over the epitaxial single crystal semiconductor layer within each of the openings **314**. Alternatively, a polycrystalline semiconductor (e.g., silicon) layer (doped or undoped) may be formed to fill all or a portion of the opening **314** and may then be recrystallized by thermal treatment or by laser annealing to form a single crystal or large grain polycrystalline semiconductor material.

A carbon layer **330** may be formed over the top surfaces **325** of the protrusions **1**B and over the upper layer of insulating material **311**, as shown in FIG. **3**F. The carbon layer **330** may comprise a carbon material that is deposited by any suitable process, such as CVD, PECVD, MBE, ALD, etc. The carbon layer **330** may comprise a carbon material that has a relatively low etch rate using a first etch process (e.g., a reactive ion etch process). In embodiments, the carbon layer **330** may be formed over the entire surface of the upper layer of insulating material **311** and the protrusions **1**B, as shown in FIG. **3**F. The carbon layer **330** may be patterned such that selected portions **331** of the layer **330** are removed while portions **333** of the layer **330** located above the protrusions **1**B remain. For example, as shown in FIG. **3**G, portions **333** of the layer **300** located above the protrusions **1**B may be protected by a patterned mask **335** while exposed portions **331** of the layer **330** are removed via a suitable process, such as by etching or selective ashing. Removing the selected portions **331** of the layer **330** leaves discrete carbon etch stop layers **333** above each of the protrusions **1**B, as shown in FIG. **3**H. The carbon etch stop layers **333** may have a first width dimension, W_1, and may completely cover the top surfaces **325** of the protrusions **1**B. In one embodiment, the first width dimension, W_1, may be greater than the width of the protrusions **1**B. Following the formation of the discrete carbon etch stop layers **333**, the patterned mask **335** may be removed.

In FIG. **3**H, a layer **337** of dielectric material (e.g., an oxide material, such as silicon oxide, or a nitride material, such as silicon nitride) may be provided over the upper layer of insulating material **311** and adjacent to each of the carbon etch stop layers **333**. In embodiments, the dielectric layer **337** may be formed over the upper layer of insulating material **311** and the carbon etch stop layers **333**, and may be planarized (e.g., by CMP or etch-back) to remove the dielectric material from above the carbon etch stop layers **333** and to make the dielectric layer **337** planar with the carbon etch stop layers **333**, as shown in FIG. **3**H.

FIG. **3**H illustrates a portion of a completed lower (e.g., source) select gate device level **50** comprising lower (e.g. source) select gate transistors **301** for a NAND string memory device. The select gate device level **50** includes a conductive select gate electrode **304** that extends generally parallel to the major surface **100***a* of the substrate **100** and

a plurality of protrusions **1**B that extend in a generally vertical direction from the major surface **100***a* of the semiconductor substrate **100** and are located adjacent to the select gate electrode **304**. The protrusions **1**B may comprise a semiconductor material and may form channel portions that extend generally perpendicular to the major surface of the substrate **100**. The semiconductor channel portions **1**B may comprise pillar- or rail-shaped protrusions that extend in a generally vertical direction from the semiconductor substrate **100**, and may comprise epitaxial single crystal silicon, for example. Additional semiconductor channel portions **1**C may be located on or in the substrate **100** and may extend in a direction that is generally parallel to the major surface of the substrate **100** (e.g., to the left and right or into and out of the page in FIG. **3**H). The additional semiconductor channel portions **1**C may electrically couple the semiconductor channel portions of the protrusions **1**B to a conductive source line outside of the view of FIG. **3**H. A first gate insulating layer **303** may extend generally parallel to the major surface of the substrate **100** and may be located between the select gate electrode **304** and the substrate **100**. A second gate insulating layer **306** may extend generally perpendicular to the major surface of the substrate **100**, and may be located between the select gate electrode **304** and first and second opposing side surfaces of each of the protrusions **1**B. Discrete carbon etch stop layers **333** are located above each of the protrusions **1**B and may function as a stopper to prevent punch through to the protrusions **1**B during an etching process to form memory openings for NAND strings above the lower (e.g., source) select gate device level **50** as described further below.

A monolithic three-dimensional NAND string memory device may be fabricated by providing a stack **120** of alternating layers of a first material **19** and a second material **21** different from the first material **19** over the substrate **100**, and forming one or more memory openings **81** in the stack **120** that extend through the layers in a direction that is substantially perpendicular to the major surface of the substrate **100**. FIGS. **4**A-**4**I illustrate one method of forming NAND strings **150** in a stack **120** over a substrate **100**. In this embodiment, the stack **120** includes a lower (e.g., source) select gate device level **50** located below the future location of the memory device levels **70**, as shown in FIG. **4**A. The select gate device level **50** may be formed as described above and shown in FIGS. **3**A-**3**H. Other fabrication methods and/or select gate device level **50** configurations may be used. For example, a lower select gate device level **50** may be fabricated as described in U.S. patent application Ser. No. 14/133,979, filed on Dec. 19, 2013, U.S. patent application Ser. No. 14/225,116, filed on Mar. 25, 2014, and/or U.S. patent application Ser. No. 14/225,176, filed on Mar. 25, 2014, all of which are incorporated by reference herein for all purposes.

In embodiments, discrete carbon etch stop layers **333** may be provided above the semiconductor protrusions **1**B, and may be separated from one another by a dielectric material layer **337**, as described above in connection with FIG. **3**H. The carbon etch stop layers **333** may have a relatively low etch rate using a first etch process (e.g., a reactive ion etch process).

The three dimensional memory device levels **70** may be fabricated over the carbon etch stop layers **333** and the dielectric material layer **337** by depositing a plurality of alternating layers **19**, **21** of a first material and a second material different than the first material as shown in FIG. **4**A. Layers **19**, **21** may be deposited by any suitable deposition method, such as sputtering, CVD, PECVD, MBE, ALD, etc. The layers **19**, **21** may be 6 to 100 nm thick.

In this embodiment, the first layers **19** comprise an electrically insulating material. Any suitable insulating material may be used, such as silicon oxide, silicon nitride, silicon oxynitride, a high-k dielectric (e.g., aluminum oxide, hafnium oxide, etc. or an organic insulating material). The second layers **21** may comprise a semiconductor material (e.g., silicon, such as polysilicon). In one embodiment, layers **19** comprise silicon oxide and layers **21** comprise polysilicon.

The deposition of layers **19**, **21** is followed by etching the stack **120** to the carbon etch stop layers **333** to form a plurality of front side openings **81** in the stack **120**. An array of a front side openings **81** (e.g., cylindrical memory openings or holes) may be formed in locations where vertical channels of NAND strings **150** will be subsequently formed, as shown in FIGS. **4**E-**4**G.

The openings **81** may be formed by photolithography and etching, as follows. First, a memory hole mask **130** is formed over the stack and patterned to form openings **131** exposing the stack **120**, as shown in FIG. **4**B. Mask **130** may comprise any suitable material, such as one or more layer of photoresist and/or hard mask material (e.g., photoresist over silicon nitride and amorphous carbon layers). Then, the stack **120** may be etched (e.g., using reactive ion etching (RIE)) to form the openings **81** in the stack through the openings **131** in mask **130**, stopping the etch at the carbon etch stop layers **333**, as shown in FIG. **4**C. As discussed above, carbon etch stop layer **333** may have a lower RIE etch rate than the materials of the alternating layers **19**, **21** of the stack **120**. Thus, the layers **19**, **21** may be more easily etched using RIE than the etch stop layer **333**. The etching process used to form the front side memory openings **81** may be stopped at the carbon etch stop layer **333** without exposing the surface of the protrusions **1**B in the openings **81**, as shown in FIG. **4**C.

Each of the front side openings **81** (e.g., cylindrical memory openings or holes) may include a sidewall **405** that extends substantially perpendicular to the major surface of the substrate **100** and is defined by the exposed surfaces of the alternating layers **19**, **21** of the first insulating material and the second semiconductor material, and a bottom **407** defined by the carbon etch stop layer **333**. The front side opening **81** may include a second width dimension (e.g., a diameter), W_2, at the bottom of the opening **81** proximate to the carbon etch stop layer **333**, as shown in FIG. **4**C. The second width dimension, W_2, at the bottom of the opening **81** may be smaller than the first width dimension, W_1, of the adjacent carbon etch stop layer **333** (see FIG. **3**H).

In FIG. **4**D, the carbon etch stop layers **333** may be removed to provide void areas **409** between the bottom of the memory openings **81** and the top surfaces of the protrusions **1**B. The void areas **409** may have the same width dimensions, W_1, as the carbon etch stop layers **33** (see FIG. **3**H), and may thus have larger width dimensions than the width dimensions W_2 at the bottoms of the memory openings **81**. In other words, the void area **409** formed by the removal of the carbon etch stop layer **333** exposes a larger area of the top surface **325** of the protrusion **1**B than would be exposed if the front side opening **81** were extended to the top surface **325** of the protrusion **1**B (i.e., if the carbon etch stop layer **333** were not present, and the front side memory opening **81** was formed by etching the stack **120** until the top surface **325** of the protrusion **1**B is reached at the bottom of the opening **81**). By exposing a larger surface area at the top surface **325** of the protrusion **1**B, a more effective electrical

contact may be made with the future channel **1** of the NAND string **150** formed in the opening **81** while providing a high aspect ratio of the opening **81**, as described in further detail below. In embodiments, the carbon etch stop layers **333** may be removed by ashing.

FIGS. **4**E-H illustrate a method of forming the NAND memory strings **150** within the front side memory openings **81**. As shown in FIG. **4**E, at least one memory film **7**, **9**, **11** is formed in the memory openings **81**, including over the sidewalls **405** of the memory openings **81**, into the void areas **409** and over the exposed surfaces of the protrusions **1**B at the bottoms of the memory openings **81**. The at least one memory film **7**, **9**, **11** may also be formed over the top of the stack **120**, as shown in FIG. **4**E. The at least one memory film includes one or more functional layers such as a blocking dielectric layer **7**, a charge storage layer **9**, and/or a tunneling dielectric layer **11** as described above in connection with FIGS. **1**A-**2**. The blocking dielectric layer **7** may be formed over the sidewall **405** and within the void area **409** of the memory opening **81** and over the exposed surface **325** of the protrusion **1**B at the bottom of the memory opening **81**. The charge storage layer **9** may be formed over the blocking dielectric layer **7**, and the tunneling dielectric **11** may be formed over the charge storage layer **9** in the memory opening **81**, as shown in FIG. **4**E.

Then, a cover layer **410** may be formed over the at least one memory film **7**, **9**, **11** in the memory openings **81** and over the stack **120**, as shown in FIG. **4**E. A purpose of the cover layer **410** is to protect the memory film **7**, **9**, **11** over the sidewall **405** of the memory opening **81** from damage during a subsequent etching step. The cover layer **410** may be a semiconductor material, such as amorphous silicon or polysilicon that may form a portion of the future semiconductor channel **1** of the NAND string, as discussed below. Alternatively, the cover layer **410** may comprise a sacrificial material, such as amorphous silicon, polysilicon, silicon nitride or carbon, that protects the memory film **7**, **9**, **11** over the sidewall **405** during an etching step and is then removed from the memory opening **81** prior to formation of the semiconductor channel **1**.

As shown in FIG. **4**E, the at least one memory film **7**, **9**, **11** and the cover layer **410** may each comprise a first portion **411** that extends over the sidewall **405** of the memory opening **81** in a direction that is substantially perpendicular to the major surface of the substrate **100** and a second portion **413** that extends over the top surface **325** of the protrusion **1**B in a direction that is substantially parallel to the major surface of the substrate **100**.

As shown in FIG. **4**F, portions of the at least one memory film **7**, **9**, **11** and the cover layer **410** may be removed in the horizontally-extending second portion **413** (see FIG. **4**E) to define a generally cylindrically-shaped opening **417** through the second portion **413** of the at least one memory film **7**, **9**, **11** and the cover layer **410** that exposes the top surface of the protrusion **1**B. The at least one memory film **7**, **9**, **11** and cover layer **410** may be etched using RIE or another suitable anisotropic wet or dry etching method to form the opening **417**. The cover layer **410** protects the at least one memory film **7**, **9**, **11** along the sidewalls **405** of the memory openings **81** from etching damage. The etching may be performed through a patterned mask (not shown) that covers the top of the stack **120** to protect the rest of the stack form etching damage. Alternatively, the mask may be omitted and a sidewall spacer anisotropic etch may be used to remove the horizontal portions of layers **7**, **9**, **11** and **410** while leaving the vertical portions of these layers in place as sidewall spacers.

In some embodiments, after the openings **417** are formed to expose the surface of the protrusions **1**B, at least a portion of the cover layer **410** may be removed from the openings **81**, including from over the sidewalls **405** of the openings **81**. For example, the cover layer **410** may be removed by a selective wet etch. Where the cover layer **410** comprises carbon, the cover layer **410** may be removed by ashing. In embodiments where the cover layer comprises a sacrificial material (e.g., amorphous silicon, silicon nitride, carbon, etc.), the cover layer **410** may be completely removed from the openings **81** prior to the formation of a channel **1** in the openings **81** (FIG. **4**G). In embodiments where the cover layer **410** comprises a semiconductor material (e.g., amorphous silicon or polysilicon) all or a portion of the cover layer **410** may remain in the memory opening **81** and may form a portion of a semiconductor channel of a NAND string, as described below. In such cases, a separate cover layer **410** removal step may be omitted.

In FIG. **4**G, a semiconductor channel material **419** is formed in the memory openings **81** and within the opening **417** such that the semiconductor channel material **419** makes contact with the top surface **325** of the semiconductor channel protrusions **1**B. The semiconductor channel material **419** may comprise, for example, amorphous silicon or polysilicon. Where all or a portion of the cover layer **410** remains in the opening **81**, the semiconductor channel material **419** may be formed over the cover layer **410**, and the semiconductor channel material **419** and the cover layer **410** may together form the semiconductor channel **1** as illustrated in FIGS. **1**A-**2**. Alternatively, where the cover layer **410** has been removed, the semiconductor channel material **419** may be formed directly over the at least one memory film (e.g., the tunnel oxide layer **11**) along the sidewall **405** of the memory opening **81**, and may form the vertically extending semiconductor channel **1** as illustrated in FIGS. **1**A-**2**. In either case, the at least one memory film **7**, **9**, **11** may be located between the semiconductor channel **1** and the sidewall **405** of the memory opening **81**.

In embodiments, the cover layer **410** and/or the semiconductor channel material **419** may be initially deposited as an amorphous semiconductor material, and may be converted to a polycrystalline semiconductor material (e.g., polysilicon) by a recrystallization process, such as by a thermal treatment or laser annealing, to provide a polycrystalline semiconductor material channel **1**.

As shown in FIG. **4**G, a first portion **441** of the semiconductor channel **1** extends in the substantially vertical direction substantially perpendicular to the major surface of the substrate **100** over the at least one memory film **7**, **9**, **11** along the sidewall **405** of the memory opening **81** and a bottom second portion **443** of the semiconductor channel **1** extends in the substantially horizontal direction substantially parallel to the major surface of the substrate **100** over the memory film **7**, **9**, **11** and into the opening (e.g., open region **417**) at the bottom portion of the memory opening **81** to electrically contact the top surface of the protrusion **1**B.

An optional core insulating layer **2**, such as a silicon oxide layer may be deposited in the openings **81** and over the stack **120** as shown in FIG. **4**H. Layer **2** is also shown in FIGS. **1**A and **1**B. The stack **120** may then be planarized (e.g., by CMP) as shown in FIG. **4**I to remove the channel, core insulating layer and the at least one memory film (e.g., layers **2**, **419**, **410**, **11**, **9** and **7**) from the top of the stack **120**. Alternately, a dry etch process (e.g., RIE) may be used to remove layers **2**, **419**, **410**, **11**, **9** and **7** from the top of the stack **120**. An optional cover layer **445**, such as a silicon oxide layer deposited by CVD using a tetraethyl orthosili-

cate (TEOS) source, may be formed over the stack as shown in FIG. **4**I. Doped semiconductor layers **21** function as control gate electrodes of the NAND strings.

FIGS. **5**A-**5**F illustrate an alternative method of forming NAND strings **150** in a stack **120** over a substrate **100**. FIG. **5**A corresponds to FIG. **4**D, and shows the stack **120** after formation of the memory openings **81** and removal of the carbon etch stop layers **333** to form void areas **409** that expose the surfaces of the protrusions **1**B at the bottoms of the memory openings **81**. FIG. **5**B shows the at least one memory film **7**, **9**, **11** formed over the stack **120** and in the memory openings **81**, including over the sidewalls **405**, within the void areas **409** and over the exposed surfaces of the protrusions **1**B at the bottoms of the memory openings **81**. Then, a cover layer **510** may be formed over the at least one memory film **7**, **9**, **11** in the memory openings **81** and over the stack **120**, as shown in FIG. **5**C. The cover layer **510** of FIG. **5**C differs from layer **410** of FIG. **4**E in that cover layer **510** is formed such that the cover layer **510** preferentially forms over the sidewall **405** of the memory opening **81** but not over the surface of the protrusion **1**B at the bottom of the memory opening **81**, as shown in FIG. **5**C (i.e., the cover layer **510** lacks the horizontally extending portion **413** of the cover layer **410** shown in FIG. **4**E). In this embodiment, the cover layer **510** may comprise a carbon material that is deposited by any suitable process, such as CVD. The selective formation of the carbon cover layer **510** over the sidewalls **405** but not over the bottom surface of the memory opening **81** may be promoted by controlling the parameters of the carbon deposition, such as the carbon deposition temperature, the thickness of the carbon cover layer **510** and the aspect ratio of the memory openings **81**. The deposition parameters may otherwise be similar to non-conformal deposition processes.

FIG. **5**D corresponds to FIG. **4**F, and shows portions of the at least one memory film **7**, **9**, **11** removed (e.g., etched, such as via RIE) to define a generally cylindrically-shaped opening **417** that exposes the top surface of the protrusion **1**B. In this embodiment, the carbon cover layer **510** does not extend over the horizontally-extending portions of the memory film **7**, **9**, **11** at the bottom of the memory hole **81**, and thus the carbon cover layer **510** does not need to be etched to expose the top surface of the protrusion **1**B. The carbon cover layer **510** extends over the memory film **7**, **9**, **11** along the sidewall **405** of the memory opening **81**, and may protect the memory film **7**, **9**, **11** over the sidewall **405** from etching damage while the portions of the memory film **7**, **9**, **11** at the bottom of the memory opening **81** are etched to expose the surface of the protrusion **1**B. The carbon cover layer **510** may then be removed, such as by ashing, as shown in FIG. **5**E.

FIG. **5**F shows a semiconductor channel material **419** formed in the memory openings **81** and within the opening **417** such that the semiconductor channel material **419** makes contact with the top surface of the semiconductor channel protrusions **1**B. The semiconductor channel material **419** in this embodiment is formed directly over the at least one memory film (e.g., the tunnel oxide layer **11**) along the sidewall **405** of the memory opening **81**, and may form the vertically extending semiconductor channel **1** as illustrated in FIGS. **1**A-**2**. The at least one memory film **7**, **9**, **11** is located between the semiconductor channel **1** and the sidewall **405** of the memory opening **81**.

An optional core insulating layer **2** may be formed as shown in FIG. **4**H, and the stack may be planarized with an optional cover layer **445** formed over the stack as shown in FIG. **4**I.

FIGS. **6**A-**6**F illustrate an alternative method of forming NAND strings **150** in a stack **120** over a substrate **100**. FIG. **6**A corresponds to FIGS. **4**D and **5**A, and shows the stack **120** after formation of the memory openings **81** and removal of the carbon etch stop layers **333** to form void areas **409** that expose the surfaces of the protrusions **1**B at the bottoms of the memory openings **81**. The stack **120** in FIGS. **6**A-**6**F differs from the stack **120** in FIGS. **4**A-**4**I and **5**A-**5**F in that instead of alternating layers of a first insulating (e.g., an oxide, such as silicon oxide) material and a second semiconductor (e.g., silicon, such as polysilicon) material **21** (e.g., an OPOP stack), the stack **120** of FIGS. **6**A-**6**F includes alternating layers of a first insulating (e.g., an oxide, such as silicon oxide) material **19** and a second sacrificial (e.g., a nitride, such as silicon nitride) material **121** (e.g., an ONON stack). In addition, as shown in FIG. **6**A, a layer of semiconductor material **637** (e.g., intrinsic polysilicon) rather than dielectric material **337** is formed planar with and is located between each of the carbon etch stop layers **333** at the bottom of the memory openings **81**. FIG. **6**A depicts the stack **120** following removal of the carbon etch stop layers **333** as described above, such that the void areas **409** are defined within the semiconductor material layer **637**.

In an alternative embodiment, the layer of intrinsic polysilicon **637** may serve as an etch stop layer for high aspect ratio memory hole etching. The stack **120** may be etched to form the memory openings **81** as described above, stopping the etch at the intrinsic polysilicon layer **637**. A selective wet etch (e.g., using tetramethyl ammonium hydroxide) may be used to preferentially etch the intrinsic polysilicon layer **637** to widen the bottom width of the memory openings **81** (e.g., to a larger width dimension W_1 as described above) but not the surface of the protrusion **1**B. The bottom lateral width of the opening **409** may be controlled by wet etch time.

The NAND strings **150** may be formed as described above in FIG. **4**E-**4**I or **5**B-**5**F. For example, similar to the method shown in FIGS. **5**B-**5**F, at least one memory film **7**, **9**, **11** may be formed over the stack **120** and in the memory openings **81**, including over the sidewalls **405**, within the void areas **409** and over the exposed surfaces of the protrusions **1**B at the bottoms of the memory openings **81**, as shown in FIG. **6**B. Then, a cover layer **510** is formed such that the cover layer **510** preferentially forms over the sidewall **405** of the memory opening **81** but not over the surface of the protrusion **1**B at the bottom of the memory opening **81**, as shown in FIG. **6**C (i.e., the cover layer **510** lacks the horizontally extending portion **413** of the cover layer **410** shown in FIG. **4**E). As described above, the cover layer **510** may comprise a carbon material that is deposited by any suitable process, such as CVD. The selective formation of the carbon cover layer **510** over the sidewalls **405** but not over the bottom surface of the memory opening **81** may be promoted by controlling the parameters of the carbon deposition, such as the carbon deposition temperature, the thickness of the carbon cover layer **510** and the aspect ratio of the memory openings **81**. The deposition parameters may otherwise be similar to non-conformal deposition processes.

In FIG. **6**D, portions of the at least one memory film **7**, **9**, **11** may be removed (e.g., etched, such as via RIE) to define a generally cylindrically-shaped opening **417** that exposes the top surface of the protrusion **1**B, while the carbon cover layer **510** protects the at least one memory film **7**, **9**, **11** from etching damage. Then, the carbon cover layer **510** may be removed, such as by ashing, as shown in FIG. **6**E.

FIG. **6**F shows a semiconductor channel material **419** formed in the memory openings **81** and within the opening

417 such that the semiconductor channel material 419 makes contact with the top surface of the semiconductor channel protrusions 1B. The semiconductor channel material 419 in this embodiment is formed directly over the at least one memory film (e.g., the tunnel oxide layer 11) along the sidewall 405 of the memory opening 81, and may form the vertically extending semiconductor channel 1 as illustrated in FIGS. 1A-2. The at least one memory film 7, 9, 11 is located between the semiconductor channel 1 and the sidewall 405 of the memory opening 81.

An optional core insulating layer 2 may be formed as shown in FIG. 4H, and the stack may be planarized with an optional cover layer 445 formed over the stack as shown in FIGS. 4I and 7A.

FIGS. 7A-7F illustrate additional processing steps that may be performed to remove the layers of sacrificial material 121 from the stack 120 and form control gate electrodes 3 for a vertical NAND memory string 150. The processing steps of FIGS. 7A-7F may be used to replace the alternating layers of sacrificial material 121 with a conductive gate electrode material in a stack 120 as shown in FIGS. 6A-6F (e.g., an ONON stack 120). In other embodiments, the processing steps of FIGS. 7A-7F may also be used to partially or completely replace the alternating layers of a semiconductor material 21 with a conductive gate electrode material in a stack 120 such as shown in FIGS. 4A-4I and 5A-5F (e.g., an OPOP stack 120). As shown in FIG. 7A, a mask 701 may be formed over the top of the stack 120. The mask 701 may be a photoresist and/or hard mask. At least one back side mask opening 703 is formed in the mask. Then, as shown in FIG. 7B, the stack 120 is etched through the opening(s) 703 in the mask to form one or more back side openings (e.g., trenches) 705*a* in the stack 120. In this embodiment, the back side opening (e.g., trench) 705*a* stops at the intrinsic polysilicon layer 637 which functions as an etch stop layer for a first trench etch.

Then, at least a portion of the sacrificial second material layers 121 may be removed through the back side openings 705*a* to form back side recesses 707 between the first material layers 19, as shown in FIG. 7B. Layers 121 may be removed by selective etching, such as a silicon nitride selective etching which removes silicon nitride layers 121 but does not remove the silicon oxide layers 19. The intrinsic polysilicon layer 637 may protect the upper layer of insulating material 311 (e.g., silicon nitride) in the lower select gate level 50 from being etched. The selective etch may stop on the oxide blocking dielectric 7, such as a silicon oxide blocking dielectric, that extends vertically in the memory openings 81.

If desired, back side opening 705*a* may be etched further at this time to extend the back side opening 705*a* through the intrinsic polysilicon layer 637 to the insulating layer 311. Alternatively, this step may be omitted at this time and combined with the etching step shown in FIG. 7D.

Electrically conductive control gate electrodes 3 may then be formed in the back side recesses 707 through the back side opening 705*a*, as shown in FIG. 7C. The control gate electrode 3 material may comprise any suitable material described above with respect to FIGS. 1A-2. For example, the material may comprise a TiN liner and tungsten gate material. The electrodes 3 may be formed by forming the electrically conductive control gate electrode material to partially or completely fill the back side opening 705*a* and to fill the back side recesses 707 such that the control gate electrode 3 material contacts the dielectric film 7 along the sidewalls of the memory openings 81. The electrode material may then be removed from the back side opening 705*a* (e.g., using anisotropic etching) without removing the material forming the electrodes 3.

In FIG. 7D, the stack 120 may be etched through a mask (not shown) or by using the top layer of the stack as a mask to form a second trench 705*b* that is continuous with the back side opening 705*a*. Together, the back side opening 705*a* and the second trench 705*b* may form a continuous trench 705 through the stack 120 to the substrate 100. The second trench 705*b* may be formed by etching through the intrinsic polysilicon layer 637 and the layers of the lower select gate level 50 (e.g., upper layer of insulating material 311, select gate electrode 304 and first gate insulating layer 303 as described above with respect to FIGS. 3A-3I) to the substrate 100. An optional doped source region 708 may be implanted into channel region 1C in the substrate 100 through the continuous trench 705, as shown in FIG. 7E. The source region 708 may be doped opposite conductivity type (e.g., n-type) from the conductivity type (e.g., p-type) of the channel region 1C.

Then, as shown in FIG. 7F, an insulating layer 709, such as a silicon oxide or silicon nitride layer is formed on the sidewalls of the backside opening 705 such that the bottom surface of the backside opening 705 (e.g., the upper major surface of the semiconductor substrate 100) is exposed. A conductive source line 711 (e.g., a metal or metal nitride line, such as W, Ti, TiN, etc.) is then formed over the insulating layer 709 in the backside opening 705 such that the source line 711 contacts the source region 708 which in turn contacts the channel region 1C in the substrate 100. This forms an electrical connection between the source line and the channel portions 1, 1B and 1C. An upper (e.g., drain side) select gate electrode and transistor (not shown for clarity) may also be formed above the memory levels 70 of each NAND string 150.

Another embodiment is illustrated in FIGS. 8A-8F. The embodiment of FIGS. 8A-8F is similar to the embodiment illustrated in FIGS. 6A-6F. However, in the embodiment of FIGS. 8A-8F, the use of the carbon etch stop layer 333 shown in FIGS. 3H and 4A-4C and the resulting void area 409 formed when layer 333 is removed as shown in FIGS. 4D, 5A and 6A may be omitted. Likewise, the protrusions 1B shown in FIGS. 4A, 5A and 6A may optionally also be omitted.

As shown in FIG. 8A, the front side opening 81 (e.g., cylindrical memory opening or hole) sidewall lacks the void area 409 in its bottom portion. Therefore, as shown in FIG. 8B, when the memory film 7, 9, 11 is formed in the opening 81, it is not formed in the void area 409 since the void area is not present.

Likewise, as shown in FIG. 8A, the bottom of the front side opening 81 may expose an upper surface of a silicon substrate 100 or a silicon layer located over the substrate rather than the surface of the protrusion 1B. However, if desired, the protrusions 1B may be retained in this embodiment if desired.

Preferably, the blocking dielectric 7 in the embodiment of FIGS. 8A-8C comprises a multi-layer film, such as a high-k dielectric layer 7A and a silicon oxide dielectric layer 7B, as shown in FIG. 8B. The high-k dielectric layer 7A has a dielectric constant greater than that of silicon oxide (e.g., greater than 3.9). Examples of high-k materials include metal oxide materials, such as aluminum oxide. Other high-k materials may also be used. Preferably, layer 7A is formed in the opening 81 first, followed by forming layer 7B over layer 7A in the opening. However, other blocking dielectrics may be used.

Preferably, a semiconductor cover layer **819** is formed over the tunnel dielectric **11** of the memory film in the front side opening **81** prior to forming the carbon cover layer **510**, as shown in FIG. **8**B. The semiconductor cover layer **819** may comprise amorphous silicon or polysilicon. Layer **819** may comprise an outer portion of the semiconductor channel **1** in the opening **81**.

As described above, the cover layer **510** may comprise a carbon layer that is selectively formed over the sidewalls over layer **819** but not over the bottom surface of layer **819** in the front side opening **81**, as shown in FIG. **8**C. However, if desired, layer **819** may be omitted and the cover layer **510** may be formed over the sidewall but not the bottom tunnel dielectric **11** portion of the memory film.

Layer **510** may be formed by CVD, such as by plasma enhanced CVD. Layer **510** deposition parameters can be tuned so that the layer deposits until the desired depth in the opening **81** without covering the bottom of the opening **81**.

FIGS. **8**D-**8**F show similar steps to those shown in FIGS. **6**D-**6**E. In FIGS. **8**D-**8**E, portions of the at least one memory film **7**, **9**, **11** and the semiconductor cover layer **819** on the bottom of the front side opening **81** are etched, such as via direction RIE, as shown by arrows in FIG. **8**D, to be removed from the bottom of the front side opening **81**. This defines an opening **817**A in the memory film and in layer **819** that exposes the top surface of the semiconductor substrate **100** (or of the protrusion **1**B, if present), while the carbon cover layer **510** protects the at least one memory film **7**, **9**, **11** and the semiconductor cover layer **819** from etching damage, as shown in FIG. **8**E.

The directional dry etch removes the bottom of the memory film, including the high-k layer **7**A, such as AlOx, which is difficult to etch without also etching layers **819**, **11**, **9** and **7**A/**7**B at the top and shoulder of the opening **81**. The spacer cover layer **510** helps in tuning the opening **81** bottom etch profile without the etching medium attacking the layers **819**, **11**, **9** and **7**B at the top, shoulder and/or sidewall of the opening **81**. Layer **510** also protects the bottom of layer **819** from resputtered AlOx deposition during the dry etch.

Then, the carbon cover layer **510** may be removed, such as by ashing, as shown in FIG. **8**F, and a semiconductor channel material **419** is formed (as shown in FIG. **8**F) in the opening **81** over layer **819** and in contact with the exposed portion of the substrate **100** (or protrusion **1**B if present) in the opening **417**A. Layers **419** and **819** together form at least a vertical portion or the entirety of the semiconductor channel **1**. An optional core insulating layer **2** may be formed as shown in FIG. **4**H, and the stack may be planarized with an optional cover layer **445** formed over the stack as shown in FIGS. **4**I and **7**A. The method then may proceed as described above with respect to FIGS. **7**A-**7**F to form the control gate electrodes **3** and the conductive source line **711**.

The opening **817**A may be tapered (e.g., roughly conical), as shown in FIG. **8**E, such that the top of the opening **817**A is wider than the bottom of the opening **817**A. The bottom of the channel **1**/**419** is also tapered in shape, as shown in FIG. **8**F. In an alternative embodiment shown in FIG. **9**, instead of the tapered opening **417**A, the cylindrical opening **417** described above having substantially vertical rather than non-vertical, angled sidewalls may be formed. The bottom of the channel **1**/**419** is also cylindrical in shape to correspond to the opening **417** shape.

In another alternative embodiment shown in FIG. **10**, instead of the tapered opening **417**A, a reverse tapered opening **417**B may be formed. The walls of the reverse tapered opening **417**B are angled in a non-vertical direction such that the top of the opening **417**B is narrower than the bottom of the opening **417**B. The bottom of the channel **1**/**419** is also reverse tapered in shape to correspond to the opening **417**B shape. The shape of the opening **417**, **417**A and **417**B may be controlled by the selecting the appropriate etching parameters.

In another embodiment shown in FIGS. **11**A-**11**C, the semi-conformal carbon cover layer **510**A is used as a spacer mask during repair/clean up of the damage at the bottom of one or more openings **1100**, such as the front side opening **81** and/or the back side (slit trench) opening **705***a*. As shown in FIG. **11**A, after formation of the opening **1100** (e.g., front and/or back side opening), there is a damaged region **1101** that is located at the bottom of the opening **1100**. The damaged region **1101** may comprise an upper surface of the silicon substrate **100** that is damaged during the etching of the opening **1100**. Alternatively, region **1101** may comprise the upper surface of a silicon layer or a silicon protrusion **1**B exposed in the opening **1100**.

As shown in FIG. **11**B, the carbon cover layer **510**A is formed by PECVD over the sidewalls of the opening **1100** (e.g., in the front side opening **81** prior to deposition of the memory film **7**, **9**, **11** and/or in the back side opening **705***a* prior to formation of layer **709**). Layer **510**A is semi-conformal and exposes the damaged region **1101** at the bottom of the opening **1100**.

Then, as shown in FIG. **11**C, the damaged region **1101** is removed (e.g., "cleaned") using a dry etch to expose an undamaged portion of the silicon substrate **100** (or protrusion **1**B or silicon layer located over the substrate) at the bottom of the opening **1100**. Layer **510**A protects the sidewalls of the opening from lateral ions/radical attack during the dry etch to prevent the opening width or diameter from being enlarged during the dry etch. After removal of the damaged region **1101**, the cover layer **510**A is removed by ashing, such as oxygen plasma ashing.

The method then proceeds as in any embodiment described above. The removal of the damaged region **1101** allows a high quality silicon channel layer **1** (e.g., epitaxial silicon channel) to formed on the exposed bottom surface of the front side opening **81** and/or a high quality conductive source line **711** contact with the source region **708**.

Another embodiment is illustrated in FIGS. **12**A-**12**F. The embodiment of FIGS. **12**A-**12**F is similar to the embodiment illustrated in FIGS. **8**A-**8**F. However, in the embodiment of FIGS. **12**A-**12**F, the sacrificial cover layer is formed over the top surface of the stack, the sidewall of the front side opening and optionally over the bottom surface of the front side opening. In the embodiment of FIGS. **12**A-**12**F, the use of the carbon etch stop layer **333** shown in FIGS. **3**H and **4**A-**4**C and the resulting void area **409** formed when layer **333** is removed as shown in FIGS. **4**D, **5**A and **6**A may be omitted. Likewise, the protrusions **1**B shown in FIGS. **4**A, **5**A and **6**A may optionally also be omitted.

FIG. **12**A corresponds to FIG. **8**A described above, and illustrates the front side opening **81** (e.g., cylindrical memory opening or hole) which lacks the void area **409** in its bottom portion. Therefore, as shown in FIG. **12**B, when the memory film **7**, **9**, **11** is formed in the opening **81**, it is not formed in the void area **409** since the void area is not present.

Likewise, as shown in FIG. **12**A, the bottom **407** of the front side opening **81** may expose an upper surface of a silicon substrate **100** or a silicon layer located over the substrate rather than the surface of the protrusion **1**B. However, if desired, the protrusions **1**B may be retained in this embodiment if desired.

The blocking dielectric **7** in the embodiment of FIGS. **12**A-**12**C may comprise a multi-layer film, such as a high-k dielectric layer **7**A and a silicon oxide dielectric layer **7**B, as shown in FIG. **12**B. The high-k dielectric layer **7**A has a dielectric constant greater than that of silicon oxide (e.g., greater than 3.9). Examples of high-k materials include metal oxide materials, such as aluminum oxide. Other high-k materials may also be used. Layer **7**A may be formed in the opening **81** first, followed by forming layer **7**B over layer **7**A in the opening. However, other blocking dielectrics may be used.

A semiconductor cover layer **819** may formed over the tunnel dielectric **11** of the memory film in the front side opening **81** prior to forming a sacrificial cover layer, as shown in FIG. **12**B. The semiconductor cover layer **819** may comprise amorphous silicon or polysilicon. Layer **819** may comprise an outer portion of the semiconductor channel **1** in the opening **81**.

Referring to FIG. **12**C, a sacrificial cover layer **1200** may be formed over the stack **120**, including over the top surface **1202** of the stack **120**, and over layer **819** on the sidewall **405** and bottom surface **407** of the front side opening **81**. The sacrificial cover layer **1200** may comprise a carbon layer as described above. Alternately, the cover layer **1200** in this embodiment may comprise one or more of an oxide, a nitride or a high-k dielectric material that may be deposited semi-conformally and may be subsequently selectively removed without damaging the underlying layers (e.g., layers **819**, **7**, **9** and **11**) on at least the sidewall **405** of the front side opening **81**.

In the embodiment of FIG. **12**C, the sacrificial cover layer **1200** may be deposited so that it forms a first portion **1204** over the top surface **1202** of the stack **120** and at least partially covering the top opening **1205** of the front side opening **81**. The sacrificial cover layer **1200** may also form a second portion **1206** over layers **819**, **7**, **9** and **11** on the sidewall **405** of the front side opening **81**. The sacrificial cover layer **1200** may optionally also form a third portion **1208** over layers **819**, **7**, **9** and **11** on the bottom surface **407** of the front side opening **81**, as shown in FIG. **12**C.

The second portion **1206** of the sacrificial cover layer **1200** may be formed with a thickness (T_2) that is substantially constant or gradually tapers between a first end **1210** proximate the top opening **1205** of the front side opening **81** and a second end **1212** proximate to the bottom surface **407** of the front side opening **81**. In embodiments, the thickness of the second portion **1206** may vary by less than 120% (e.g., 0-100%, such as 10-75%) between the first end **1210** and the second end **1212**.

As shown in FIG. **12**C, the first portion **1204** of the sacrificial cover layer **1200** may have a thickness (T_1) that is greater than the thickness (T_2) of the second portion **1206**. In embodiments, the thickness of the first portion **1204** may be more than 225% (e.g., 225-500%) of the maximum thickness of the second portion **1206**. When a third portion **1208** of the sacrificial cover layer **1200** is present over the bottom surface **407** of the front side opening **81**, the thickness (T_3) of the third portion **1208** may be less than the thicknesses of the first portion **1204** and the second portion **1206**.

Referring again to FIG. **12**C, the first portion **1204** of the sacrificial cover layer **1200** may include a region **1214** that overhangs the top opening **1205**, i.e., extends radially inwards from the first end **1210** of the second portion **1206** of the sacrificial cover layer **1200** to at least partially cover the top opening **1205** of the front side opening **81**.

The sacrificial cover layer **1200** may be formed by CVD, such as by plasma enhanced CVD. The deposition parameters can be tuned so that the layer **1200** deposits to the desired depths in the first **1204**, second **1206** and (optional) third portions **1208** of the layer **1200**.

FIGS. **12**D-**12**F show similar steps to those shown in FIGS. **8**D-**8**F. In FIGS. **12**D-**12**E, portions of the at least one memory film **7**, **9**, **11** and the semiconductor cover layer **819** are etched, such as via a directional dry etch (e.g., RIE), schematically illustrated by arrows in FIG. **12**D, to remove the portions from over the bottom surface **407** of the front side opening **81**. The etching may also remove some of the first portion **1204** of the sacrificial cover layer **1200** from over the top surface **1202** of the stack and from over the top opening **1205** of the front side opening **81**. The etching may also remove the optional third portion **1208** (if present) of the sacrificial cover layer **1200** in addition to the memory film and semiconductor cover layer **819** from the bottom surface **407** of the front side opening **81** to define an opening **417**A that exposes the top surface of the semiconductor substrate **100** (or of the protrusion **1**B, if present). The second portion **1206** of the sacrificial cover layer **1200** may protect the at least one memory film **7**, **9**, **11** and the semiconductor cover layer **819** on the sidewall **405** of the front side opening **81** from etching damage, as shown in FIG. **12**E.

The directional dry etch removes the bottom of the memory film, including the high-k layer **7**A, such as AlOx, which is difficult to etch without also etching layers **819**, **11**, **9** and **7**B at the top and shoulder of the opening **81**. The sacrificial cover layer **1200** may help in tuning the opening **81** bottom etch profile without the etching medium attacking the layers **819**, **11**, **9** and **7**B at the top, shoulder and/or sidewall of the opening **81**. The relatively thick first portion **1204** of the layer **1200**, including the radially-inward extending region **1214** at the top opening **1205** of the front side opening **81**, may further protect layers **819**, **11**, **9** and **7**A/**7**B from being etched at the top and shoulder of the opening **81**. The directional nature of the etch may enable the relatively thin, generally horizontally-extending third portion **1208** of layer **1200** to be removed during the etching while the generally vertically-extending second portion **1206** of layer **1200** may protect the sidewall **405** of the opening **81** against etching damage. The second portion **1206** of layer **1200** may also protect the bottom of layer **819** from resputtered AlOx deposition during the dry etch.

Referring to FIG. **12**F, the sacrificial cover layer **1200** may then be removed from the stack **120**. The sacrificial cover layer **1200** may be selectively removed from over the top surface **1202** of the stack **120** and the sidewall **405** of the front side opening **81** without damaging the memory film and semiconductor cover layer **819**. When the sacrificial cover layer **1200** comprises carbon, the layer **1200** may be removed by ashing (e.g., using an oxygen plasma ashing process). In other embodiments, the sacrificial cover layer **1200** may be removed via selective etching.

A semiconductor channel material **419** may then be formed in the opening **81** over layer **819** and in contact with the exposed portion of the substrate **100** (or protrusion **1**B if present) in the opening **417**A, as shown in FIG. **12**F. The semiconductor material of layers **419** and **819** may together form a semiconductor channel **1** as described above. An optional core insulating layer **2** may be formed as shown in FIG. **4**H, and the stack may be planarized with an optional cover layer **445** formed over the stack as shown in FIGS. **4**I and **7**A. The method then may proceed as described above

with respect to FIGS. **7**A-**7**F to form the control gate electrodes **3** and the conductive source line **711**.

The opening **417**A may be tapered (e.g., roughly conical), as shown in FIG. **12**E, such that the top of the opening **417**A is wider than the bottom of the opening **417**A. The bottom of the channel **1**/**419** is also tapered in shape, as shown in FIG. **12**F. In an alternative embodiment shown in FIG. **13**, instead of the tapered opening **417**A, the cylindrical opening **417** described above having substantially vertical rather than non-vertical, angled sidewalls may be formed. The bottom of the channel **1**/**419** may also be cylindrical in shape to correspond to the opening **417** shape.

In another alternative embodiment shown in FIG. **14**, instead of the tapered opening **417**A, a reverse tapered opening **417**B may be formed. The walls of the reverse tapered opening **417**B are angled in a non-vertical direction such that the top of the opening **417**B is narrower than the bottom of the opening **417**B. The bottom of the channel **1**/**419** may also be reverse tapered in shape to correspond to the opening **417**B shape. The shape of the opening **417**, **417**A and **417**B may be controlled by the selecting the appropriate etching parameters.

In another embodiment shown in FIGS. **15**A-**15**C, a sacrificial cover layer may be used as a spacer mask during repair/clean up of the damage at the bottom of one or more openings **1100**, such as the front side opening **81** and/or the back side (slit trench) opening **705***a*. FIG. **15**A corresponds to FIG. **11**A described above, and shows the stack **120** after forming an opening **1100** (e.g., front and/or back side opening) such that a damaged region **1101** is located on the bottom surface **407** of the opening **1100**. The damaged region **1101** may comprise an upper surface of the silicon substrate **100** that is damaged during the etching of the opening **1100**. Alternatively, region **1101** may comprise the upper surface of a silicon layer or a silicon protrusion **1**B exposed in the opening **1100**.

Referring to FIG. **15**B, a masking layer **1500** may be formed on the stack **120**, such as by PECVD. The masking layer **1500** may comprise a carbon layer as described above. Alternately, the masking layer **1500** may comprise one or more of an oxide, a nitride or a high-k dielectric material that may be deposited semi-conformally and then selectively removed from the stack **120**. The masking layer **1500** may be deposited so that it forms a first portion **1504** on a top surface **1502** of the stack **120** and a second portion **1506** on a sidewall **405** of the opening **1100**. The masking layer **1500** may optionally be deposited so that it also forms a third portion **1508** over the damaged region **1101** on the bottom surface **407** of the opening **1100**.

The second portion **1506** may have a thickness that is substantially constant or gradually tapers between a first end **1510** proximate to the top **1501** of the opening **1100** and a second end **1512** proximate to the bottom surface **407** of the opening **1100**. In embodiments, the thickness of the second portion **1506** may vary by less than 120% (e.g., 0-100%, such as 10-75%) between the first end **1510** and the second end **1512**. The first portion **1504** may have a thickness that is greater than the thickness of the second portion **1506**. For example, the thickness of the first portion **1504** may be more than 225% (e.g., 225-500%) of the maximum thickness of the second portion **1506**. The third portion **1508** of the masking layer **1500** may have a thickness that is less than the thicknesses of the first portion **1504** and the second portion **1506**.

The first portion **1504** of the masking layer **1500** may overhang and at least partially cover the top **1505** of the opening **1100**. As shown in FIG. **15**B, the first portion **1504** may extend radially inward from the first end **1510** of the second portion **1506** of the masking layer **1500** to at least partially cover the top **1501** of the opening **1100**.

Referring to FIG. **15**C, the damaged region **1101** may be removed (e.g., "cleaned") using a dry etch to expose an undamaged portion of the silicon substrate **100** (or protrusion **1**B or silicon layer located over the substrate) at the bottom of the opening **1100**. The masking layer **1500** protects the top, shoulder and sidewall of the opening from lateral ions/radical attack during the dry etch to prevent the opening width or diameter from being enlarged during the dry etch. The directional dry etch may initially remove the third portion **1508** of the masking layer **1500** (if present) from the bottom of the opening **1100** to expose the damaged region **1101**, and may also remove the damaged region **1101** from the bottom surface **407** of the opening **1100**. After removal of the damaged region **1101**, the masking layer **1500** may be selectively removed by a suitable process, such as by ashing (e.g., oxygen plasma ashing) or one or more additional etching steps.

The method then proceeds as in any embodiment described above. The removal of the damaged region **1101** allows a high quality silicon channel layer **1** (e.g., epitaxial silicon channel) to formed on the exposed bottom surface of the front side opening **81** and/or a high quality conductive source line **711** contact with the source region **708**.

Although the foregoing refers to particular preferred embodiments, it will be understood that the disclosure is not so limited. It will occur to those of ordinary skill in the art that various modifications may be made to the disclosed embodiments and that such modifications are intended to be within the scope of the disclosure. All of the publications, patent applications and patents cited herein are incorporated herein by reference in their entirety.

What is claimed is:

1. A method of making a semiconductor device, comprising:

forming a stack of alternating layers of a first material and a second material over a semiconductor material;

etching the stack to form at least one front side opening in the stack;

forming a memory film over a sidewall and bottom surface of the at least one front side opening;

forming a sacrificial cover layer over the memory film such that the sacrificial cover layer is deposited so that the sacrificial cover layer is formed over a sidewall portion of the memory film located over the sidewall of the at least one front side opening, but not over a bottom portion of the memory film located over the bottom of the at least one front side opening, wherein the sacrificial cover layer comprises carbon and the semiconductor material comprises a semiconductor substrate;

etching the bottom portion of the memory film at the bottom of the at least one front side opening to expose an upper surface of the semiconductor material while the sacrificial material layer protects the sidewall portion of the memory film during the etching step;

removing the sacrificial cover layer;

forming a semiconductor channel in the at least one front side opening;

etching a back side opening through the stack to the substrate;

removing the second material layers from the stack through the back side opening to form back side recesses between the first material layers in the stack;

forming control gate electrodes in the back side recesses through the back side opening;

forming a source region in the substrate through the back side opening;

forming an insulating layer on sidewalls of the back side opening such that a major surface of the substrate is exposed in the back side opening; and

forming a conductive source line in the back side opening over the insulating layer and in contact with the source region in the substrate;

wherein the method further comprises at least one of (a), (b) or (c):

(a) the memory film comprises a composite blocking dielectric comprising a high-k dielectric layer and a silicon oxide layer; and/or

(b) forming a semiconductor cover layer between the memory film and the sacrificial cover layer and etching a bottom portion of the semiconductor cover layer at the bottom of the at least one front side opening to expose the upper surface of the semiconductor material while the sacrificial material layer protects a sidewall portion of the semiconductor channel during the etching step; and/or

(c) etching the bottom portion of the memory film at the bottom of the at least one front side opening forms either a tapered opening or a reverse tapered opening.

2. The method of claim **1**, wherein the carbon sacrificial cover layer is removed from the at least one front side opening by ashing.

3. The method of claim **1**, further comprising depositing a dielectric material in a core of the at least one front side opening such that the semiconductor channel concentrically surrounds the dielectric material.

4. The method of claim **1**, wherein the memory film comprises a charge trapping layer or floating gate and a tunnel dielectric, and the tunnel dielectric is located between the charge trapping layer or floating gate and the semiconductor channel.

5. The method of claim **4**, wherein the memory film further comprises a blocking dielectric.

6. The method of claim **1**, wherein:

the semiconductor device comprises a monolithic three dimensional NAND string in an array of monolithic three dimensional NAND strings located over a silicon substrate;

the monolithic three dimensional NAND string comprises at least one memory cell in the first device level located over another memory cell in the second device level of the three dimensional array of NAND strings; and

the silicon substrate contains an integrated circuit comprising a driver circuit for the memory device located thereon.

7. The method of claim **1**, wherein the method further comprises (a) the memory film comprises the composite blocking dielectric comprising the high-k dielectric layer and the silicon oxide layer.

8. The method of claim **1**, wherein the method further comprises (b) forming the semiconductor cover layer between the memory film and the sacrificial cover layer and etching the bottom portion of the semiconductor cover layer at the bottom of the at least one front side opening to expose the upper surface of the semiconductor material while the sacrificial material layer protects a sidewall portion of the semiconductor channel during the etching step.

9. The method of claim **1**, wherein the method further comprises (c) etching the bottom portion of the memory film at the bottom of the at least one front side opening forms either the tapered opening or the reverse tapered opening.

10. A method of making a semiconductor device, comprising:

forming a stack of alternating layers of a first material and a second material over a semiconductor material;

etching the stack to form at least one front side opening in the stack, the at least one front side opening comprising a top opening defined by a top surface of the stack, a bottom surface opposite the top surface, and a sidewall defined at least in part by the alternating layers of the stack and extending between the top opening and the bottom surface;

forming a memory film over the sidewall and bottom surface of the at least one front side opening;

forming a sacrificial cover layer over the stack such that the sacrificial cover layer is deposited so that it forms a first portion over the top surface of the stack and at least partially covering the top opening of the at least one front side opening and a second portion over a sidewall portion of the memory film located over the sidewall of the at least one front side opening, wherein the first portion has a thickness that is greater than the thickness of the second portion;

etching the bottom portion of the memory film at the bottom of the at least one front side opening to expose an upper surface of a semiconductor material while the sacrificial cover layer protects the sidewall portion of the memory film during the etching step;

removing the sacrificial cover layer; and

forming a semiconductor channel in the at least one front side opening.

11. The method of claim **10**, wherein the sacrificial cover layer is deposited so that it forms a third portion over the bottom surface of the at least one front side opening, and the third portion of the sacrificial cover layer is etched with the bottom portion of the memory film to expose the upper surface of the semiconductor material while the second portion of the sacrificial cover layer remain over the sidewall portion of the memory film.

12. The method of claim **11**, wherein a thickness of the third portion is less than the thicknesses of the first and second portions.

13. The method of claim **10**, wherein the second portion has a thickness that varies by less than 120% between a first end proximate to the top opening and a second end proximate to the bottom surface of the at least one memory opening.

14. The method of claim **10**, wherein the thickness of the first portion is more than 225% of a maximum thickness of the second portion.

15. The method of claim **10**, wherein:

the first portion of the sacrificial cover layer extends radially inward from the first end of the second portion of the sacrificial cover layer to at least partially cover the top opening of the at least one front side opening; and

the second portion has a thickness that is substantially constant or gradually tapers between a first end proximate to the top opening and a second end proximate to the bottom surface of the at least one memory opening.

16. The method of claim **10**, wherein the method further comprises at least one of (a), (b) or (c):

(a) the memory film comprises a composite blocking dielectric comprising a high-k dielectric layer and a silicon oxide layer; and/or

(b) forming a semiconductor cover layer between the memory film and the sacrificial cover layer and etching a bottom portion of the semiconductor cover layer at the bottom of the at least one front side opening to expose the upper surface of the semiconductor material while the sacrificial cover layer protects a sidewall portion of the semiconductor channel during the etching step; and/or

(c) etching the bottom portion of the memory film at the bottom of the at least one front side opening forms either a tapered opening or a reverse tapered opening.

17. The method of claim **10**, wherein the sacrificial cover layer comprises carbon and the semiconductor material comprises a semiconductor substrate, and the carbon sacrificial cover layer is removed from the at least one front side opening by ashing.

18. The method of claim **17**, wherein the memory film comprises a charge trapping layer or floating gate and a tunnel dielectric, and the tunnel dielectric is located between the charge trapping layer or floating gate and the semiconductor channel.

19. The method of claim **18**, wherein:

the memory film further comprises a blocking dielectric; and

a dielectric material is located in a core of the at least one front side opening such that the semiconductor channel concentrically surrounds the dielectric material.

20. The method of claim **17**, further comprising:

etching a back side opening through the stack to the substrate;

removing the second material layers from the stack through the back side opening to form back side recesses between the first material layers in the stack;

forming control gate electrodes in the back side recesses through the back side opening;

forming a source region in the substrate through the back side opening;

forming an insulating layer on sidewalls of the back side opening such that a major surface of the substrate is exposed in the back side opening; and

forming a conductive source line in the back side opening over the insulating layer and in contact with the source region in the substrate.

21. The method of claim **10**, wherein:

the semiconductor device comprises a monolithic three dimensional NAND string in an array of monolithic three dimensional NAND strings located over a silicon substrate;

the monolithic three dimensional NAND string comprises at least one memory cell in the first device level located over another memory cell in the second device level of the three dimensional array of NAND strings; and

the silicon substrate contains an integrated circuit comprising a driver circuit for the memory device located thereon.

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