Specific Contact Resistance Measurements of Metal-Semiconductor Junctions

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ABSTRACT

Our research comprises the manufacturing of test structures to characterize the metal-semiconductor junctions with a number of techniques and materials. An extensive subsequent physical and electrical testing of the junctions is carried out. We present our first results on specific silicide-to-diffusion contact resistance characterization using the known Scott's Transmission Line Model (TLM) and our approach, considering particular geometry, with NiSi and PtSi as the silicides.

INTRODUCTION

Future improvements of IC technology demand the introduction of many new materials i.e. for metal-semiconductor junctions in particular and studying both the technology and properties of such junctions in a broad sense. Metal-semiconductor junctions are essential to any electronic system containing semiconductors. These junctions have always been a topic of research [1-3].

The performance of MOS circuits depends strongly on transistor drive current. The drive current of the transistor is determined by the total device resistance, which consists of the channel resistance and the parasitic resistances associated with diffusions and contacts. As device dimensions shrink in each new technology generation, contact resistance scales as a power of the reciprocal dimensions [4]. It is expected that the contact resistance between silicide and source/drain region will dominate the total series resistance. This has serious consequences for current drive and device speed.

The silicide must provide low contact resistance to the doped silicon regions. The reduction of this contact resistance and the corresponding specific contact resistance is a large issue in order to not compromise the device performance. Thus the ability to accurately measure the contact resistance is essential to contact process development. For this purpose, a set of test structures was fabricated and specific contact resistance was derived using the Scott model of TLM [5] and a correction for the current distribution.

DESCRIPTION OF THE MEASUREMENT TECHNIQUES

A. *Transmission Line Model*

The theoretical expression of the contact resistance contribution to the series source and drain resistance is expressed as [5]:

$$\left(R_c\right)_{\text{Transistor}} = R_{cs} + R_{cd} = \frac{2\sqrt{\rho_c R_s}}{W \tanh\left(L/L_c\right)} \qquad (1)$$

where ρ_c is the specific contact resistance from the silicide to diffusion. The diffusion layer under the silicide is characterized by R_s, the sheet resistance under the silicide, W is the transistor width and L is the length of the silicide contact. L_c is the transfer length defined as $L_c = \sqrt{\rho_c / R_s}$.

The current tends to stay in the silicide as long as possible before moving into the silicon over a distance corresponding to the transfer length L_c. Two limiting cases for the contact resistance could be expressed. For $L >> L_c$, (1) is reduced to:

$$R_{cs} + R_{cd} = \frac{2\sqrt{\rho_c R_s}}{W} = R_0 \qquad (2)$$

The limit expressed by (2) corresponds to the ideal case when the contact contribution of the source and drain to the series resistance is independent of the silicided contact length (L). For $L << L_c$, (1) is reduced to:

$$R_{cs} + R_{cd} = \frac{2\rho_c}{LW} \qquad (3)$$

The limit (3) denotes the case when the contact resistance depends on the contact area. The extraction of the contact resistance contribution to the series source and drain resistance cannot be done using transistor measurements; appropriate test structures are necessary for contact resistance evaluation. The transmission line structure [5] is a useful and simple method to accurately describe the behavior of the silicide contact resistance.

Silicide to silicon contact resistance is investigated using a set of dedicated test structures with silicided segments of varying lengths based on the Scott model

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of the Transmission Line Model (TLM) [6]. The TLM structure consists of alternating silicided and unsilicided segments formed by using a silicide-blocking mask (Fig. 1).

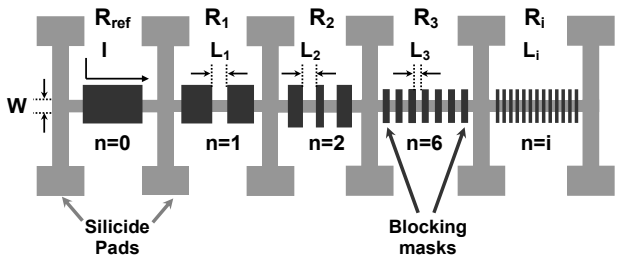

Fig. 1. Example of a TLM layout structure (top view).

The measurement technique involves forcing the current through the reference structure not interrupted by silicide segments in series with the structures interrupted by one, two or n silicided segments and measuring the voltage drop across each structure. As the structures have been designed to have equal silicided and non-silicided segments lengths, the difference between the reference resistance and the other resistances is attributed to the contact resistance contribution. Thus, the contact resistance of each structure measured experimentally is expressed as:

$$\left(R_{\mathrm{c}}\right)_{\mathrm{meas}} W = \left(\frac{R_{\mathrm{i}} - R_{\mathrm{ref}}}{n}\right) W \tag{4}$$

where R_{i} is the resistance of the structure interrupted by n silicided segments, R_{ref} is the resistance of the reference structure and W is the structure width. The theoretical expression of the silicide-to-silicon contact resistance for the test structure as stated by Scott is given as:

$$\left(R_{\mathrm{c}}\right)_{\mathrm{meas}} = \frac{2\sqrt{\rho_{\mathrm{c}} R_{\mathrm{s}}}\,\tanh(L/2L_{\mathrm{c}})}{W} \tag{5}$$

where $\rho_c = L_c R_0 W/2$ is the specific contact resistance, R_{s} is the sheet resistance under the silicide, W is the structure width and L is the length of the silicided segment. L_{c} is the transfer length. Once more, two limiting cases for the contact resistance can be expressed, for $L >> L_{\mathrm{c}}$ equation (5) reduces to

$$\left(R_{\mathrm{c}}\right)_{\mathrm{meas}} = \frac{2\sqrt{\rho_{\mathrm{c}} R_{\mathrm{s}}}}{W} = R_0 \tag{6}$$

The limit expressed by (6) corresponds to low contact resistance thus all the current flows through the silicide contact. The value of $R_0 W$ obtained with the transmission line structure using the long silicided segments equals to limit (2) achieved with a transistor with long silicided contact. For $L << L_{\mathrm{c}}$ equation (5) reduces to:

$$\left(R_{\mathrm{c}}\right)_{\mathrm{meas}} = \frac{L}{W} R_{\mathrm{s}} \tag{7}$$

The limit of (7) shows the case when only a fraction of the current will flow in the silicided segment of the TLM. In the transistor all the current has to enter the silicide, resulting in lower drive current when $L << L_{\mathrm{c}}$. By plotting $(R_{\mathrm{c}})_{\mathrm{meas}} W$ as a function of silicided length L, the contact resistance saturates for $L >> L_{\mathrm{c}}$ to the maximum value $R_0 W$.

The TLM contact resistance given by the equation (5) can be expressed as:

$$\frac{R_0 + (R_{\mathrm{c}})_{\mathrm{meas}}}{R_0 - (R_{\mathrm{c}})_{\mathrm{meas}}} = \exp\left(\frac{L}{L_{\mathrm{c}}}\right) \tag{8}$$

Plotting $\ln((R_0+R_{\mathrm{c}})/(R_0-R_{\mathrm{c}}))$ as function of L allows to extract the transfer length L_{c}. Using extracted L_{c} and R_0 values, the resistance of the test structure $(R_{\mathrm{c}})_{\mathrm{meas}}$ can be plotted to fit the theoretical curve and, therefore, the specific contact resistance ρ_{c} can be calculated.

B. *Current direction influence*

The TLM derivation as shown in [6] requires the assumption of the electric current through the interface between the silicide and diffusion areas to be vertical. This corresponds to the first extreme case depicted in Fig. 2a. Although, using the modern method of growing silicide, it is known that the structures are built in into the diffusion area, so the assumption of the current to be vertical is not accurate. Considering the second extreme case, we can assume a horizontal current injection, for a better description of the realized structures with embedded silicide areas (Fig. 2c).

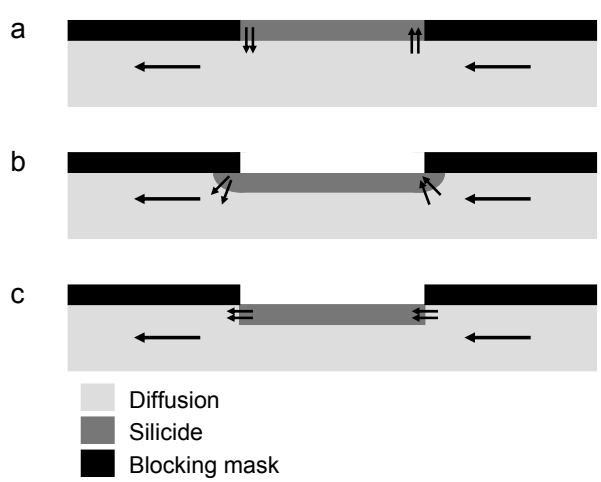

Fig. 2. Current directions for different cases of silicide formation: (a) Scott model; (b) realized structure; (c) first approach to horizontal current distribution.

The realized structure (see the TEM image in Fig 5 and the schematic representation in Fig 2b) can be

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described using a resistor network depicted in Fig. 3. Such a network should especially be applied to the rounded corners of the silicide-to-diffusion transition regions. Using this approach, one can calculate 2D current distributions in different materials. The number of horizontal sub-layers in such a scheme (i.e. horizontal resistor lines; note that only two sub-layers are shown in Fig 3) to be varied depending on actual dimensions and accuracy requirements.

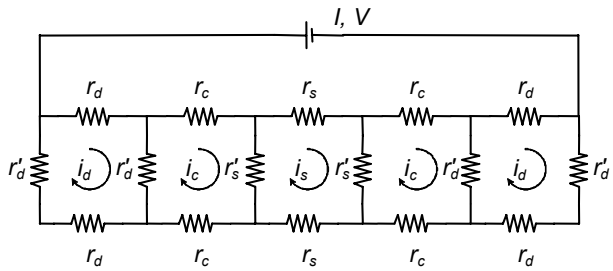

Fig. 3. Schematic representation of the realized structure with one silicide fragment only (Fig. 2b); r_d and r'_d – are diffusion resistances, r_s and r'_s – silicide resistances, r_c – silicide to diffusion contact resistance and i_s ,i_c, i_d are currents for the corresponding loops.

In terms of the proposed loop-current model, using Kirchoff's laws for current and voltage and Ohm's law it can be shown that:

$$\begin{aligned} &2(I-i_d)r_d + 2(I-i_c)r_c + (I-i_s)r_s = V \\ &2i_d(r_d + r'_d) - Ir_d - i_c r'_d = 0 \\ &(2r_c + r'_d + r'_s)i_c - Ir_c - r'_d i_d - r'_s i_s = 0 \\ &2i_s(r_s + r'_s) - Ir_s - 2i_c r'_s = 0. \end{aligned} \tag{9}$$

The loop currents do not change for the same regions (e.g. for all diffusion regions) due to the symmetry of the structure. This approach based on a variable resistor network will be developed in our future work. In this paper we will only consider the simplest case shown in Fig 2c.

The input current I and voltage drop across the structure V can be measured using R_{ref} and R_1 from the TLM layout, which eliminates the diffusion resistance (r_d and r'_d) contribution:

$$V/I = R = R_1 - R_{ref} \tag{10}$$

As the resistance of the diffusion area is eliminated, the resistor network can be simplified to the network depicted in Fig 4. Here we assume that the horizontal current distribution is uniform in the vertical direction inside the silicide. The current can only flow inside the silicide and not in the diffusion area under the silicide.

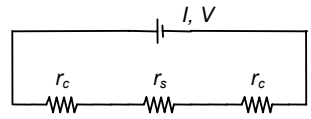

Fig. 4. Schematic representation of one-silicide fragment shown in Fig. 2c.

The silicide resistance r_s can be calculated from the measured silicide sheet resistance $r_{s(sheet)}$ on the same wafer using one of the sheet resistance measurement techniques and silicide geometry factors - the length (L) and the width (W):

$$r_s = r_{s(sheet)} L/W \tag{11}$$

The contact resistance r_c can then be calculated from Ohm's law:

$$I(2r_c + r_s) = V \tag{12}$$

EXPERIMENTAL RESULTS

For the contact resistance study (100) p-type Si wafers were used as starting material on which active areas were defined by Shallow Trench Isolation. Channels were defined by I-line lithography and doping concentrations were achieved by low-dose well implantations B (180 keV) and P (380 keV) for the P-well and N-well respectively. Highly Doped Drain (HDD) implantations were carried out for corresponding wells: As (20 keV) for NHDD and B (2keV) for PHDD. For the TLM, a silicide blocking layer (SiO_2/Si_3N_4) was deposited and patterned using I-line lithography. The segment lengths range from 0.05 to 3 µm and have a width of 8 µm. The smaller segments (0.25 µm to 50 nm) were defined with e-beam lithography. Each of the four structures has n silicided segments, where n equals 1, 2, 6, 12, 15, 20, 30, 40 and 60 (Fig. 1). Finally, a 10-nm thick Ni layer or a 13-nm Pt was deposited and silicide was formed by either a two-step anneal (300 ^oC for 30 s + 470 ^oC for 30 s) for NiSi or a one-step anneal (500 ^oC for 30 sec) for PtSi. In both cases the unreacted metal was selectively removed by wet etching.

Silicide profiles and lengths for the smaller segments were verified by TEM-analysis (see e.g. Fig. 5). The samples were prepared by a combination of mechanical polishing and FIB200 technique (Focused Ion Beam), depositing a layer of low-temperature PECVD silicon nitride prior to preparation as a protection layer and a thin Pt layer to avoid charging. In the FIB equipment a 1.5 µm thick Pt layer is deposited on each structure to protect the sample during FIB milling. The TEM-analysis was performed on a FEI Tecnai F30ST TEM operated at 300 kV. The silicide profiles are in agreement with structure (b) in Fig. 2. The actual segment lengths are always larger

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than the defined ones due to lateral expansion of silicide, ranging from 10 to 20 nm on each side.

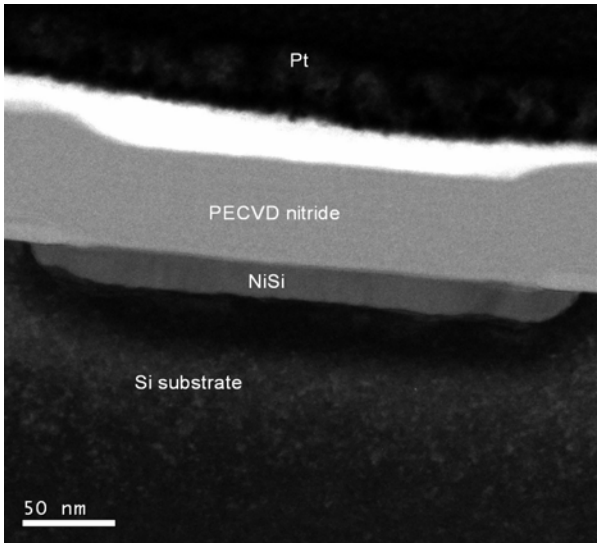

Fig. 5. Example of a X-section TEM image of NiSi profile for n=12, showing the lateral silicide formation.

According to the Scott model the transfer length (L_c) value was extracted using expression (8) and the actual silicide lengths derived from TEM (Fig. 6).

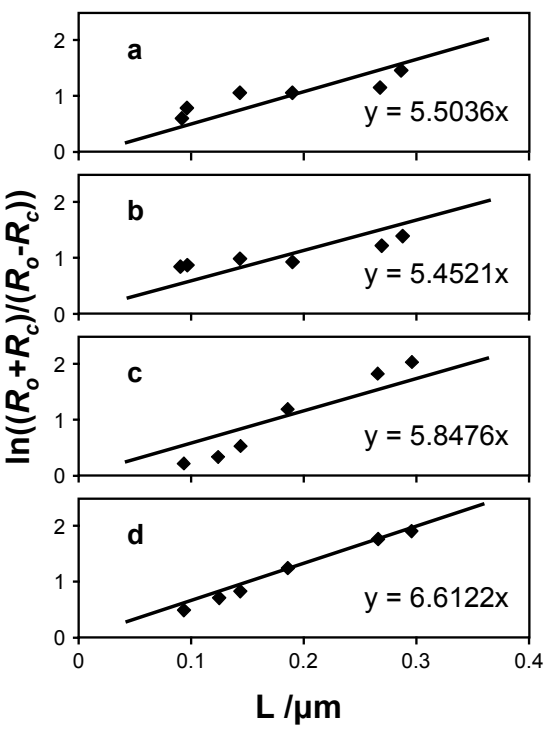

Fig. 6. $\ln((R_0+R_c)/(R_0-R_c))$ as a function of silicided segment length. The slope equals to $1/L_c$ reveals L_c extraction for (a) NiSi/n-type silicon (b) NiSi/p-type silicon (c) PtSi/n-type silicon (d) PtSi/p-type silicon

Using extracted L_c and R_0 values, the specific contact resistance for NiSi is calculated to be 1.8×10^{-8} $\Omega\cdot cm^2$ (to n-type silicon) and 3.9×10^{-8} $\Omega\cdot cm^2$ (to p-type silicon) and for PtSi is 5.3×10^{-8} $\Omega\cdot cm^2$ (to n-type silicon) and 9.3×10^{-8} $\Omega\cdot cm^2$ (to p-type silicon).

The fit of experimental data for NiSi and PtSi with the Scott model for R_c (5) when the values extracted for L_c and R_0 are implemented may be found on Fig. 7-8 respectively.

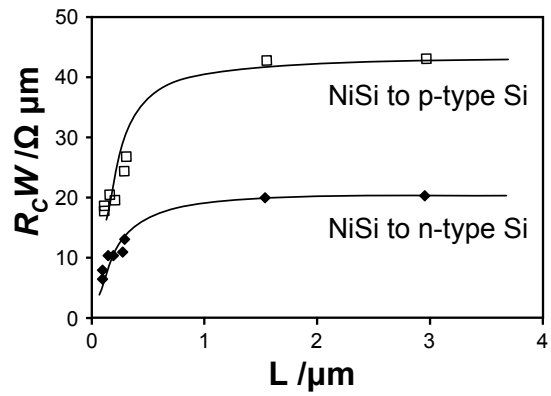

Fig. 7. Contact resistance values for NiSi, measured (dots) vs. calculated (lines) using the Scott model

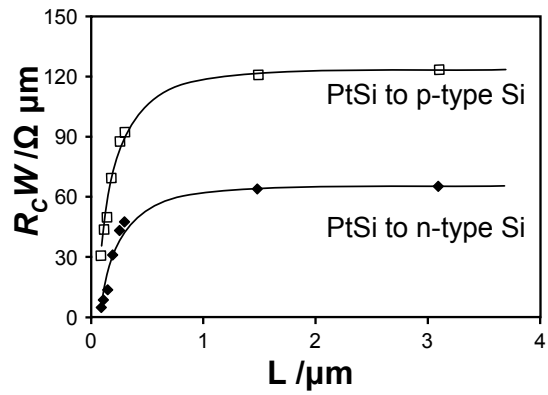

Fig. 8. Comparison of the curve fit values with the measured values for PtSi

The values of $r_{s(sheet)}$ were measured using Van der Pauw structures. From the equations (10)-(12), values of r_c were extracted. The specific contact resistance can be calculated as a product of r_c and the interface contact area between the silicide and diffusion regions. The specific contact resistance was found to be 0.20×10^{-8} $\Omega\cdot cm^2$ for NiSi (to p-type silicon) and 0.59×10^{-8} $\Omega\cdot cm^2$ for PtSi (to p-type silicon). The values for the n-type case are lower compared to the p-type silicon. However, the dimensions L and W were not known with sufficient precision to compute a reliable value of specific contact resistance on n-type silicon.

DISCUSSION & CONCLUSIONS

The contact resistance between NiSi and PtSi and highly doped silicon regions (N and P) was studied making use of the TLM test structure. The results were analyzed using two methods – the Scott Model (assuming vertical current flow through the diffusion/silicide interface) and the approach modified for the case of a horizontal current flow through the

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interface. Specific contact resistances obtained by the two methods are different. This significant difference is explained by different assumptions for the geometrical factors of the structures and consequently different current distributions. The Scott Model assumes vertical current distribution while our approach ultimately assumes a horizontal distribution. According to TEM analyses the real structure and therefore the current distribution is more complicated. Here we present only the two boundary cases (as depicted in Fig. 2). Future research will focus on a model with a 2D current distribution for the realized structures. The results will be compared also with different measurement techniques like Kelvin Cross-Bridge Resistor (KCBR) [7, 8].

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REFERENCES

[1] C. Wang, J.P. Snyder, and J.R. Tucker, Appl. Phys. Letters, vol. 74, no.8, pp.1174-1176, 1999.

[2] J. Kedzierski, M.Ieong, X. Peiqi, J. Bokor, T.J. King, and C. Hu, in 2001 IEEE Int. SOI Conf. Proc., pp. 21-22, 2001

[3] A.Y. C. Yu, Solid-stat. Electron, vol.13, pp. 239-247, 1970.

[4] C.M. Osburn, K.R. Bellur, Thin Solid Films, vol.332, pp. 428-436, 1998

[5] D.B. Scott, R. A. Chapman, C. Wei, S. S. Mahant-Shetti, R.A. Haken and T.C. Holloway, IEEE Trans. on Electron Devices, pp. 562-574, 1987

[6] D.B. Scott, W.R. Hunter, and H. Shichijo, IEEE Trans. Electron Devices, vol. Ed-29, pp.651-661, 1982.

[7] W. M. Loh, K. Saraswat, and R.W. Dutton, IEEE Electron Device Lett., vol. EDL-6, no.3, pp. 105-108, 1985.

[8] W. M. Loh, S.E. Swirhun, E. Crabbe, K. Saraswat, and R.M. Swanson, IEEE Electron Device Lett., vol. EDL-6, no.3, pp. 105-108, 1985

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