UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00294
U.S. Patent No. 10,886,291
Issue Date: January 5, 2021

Title: JOINT OPENING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 10,886,291
PURSUANT TO 35 U.S.C. §§311-319 AND 37 C.F.R. §42

YMTC
Exhibit 2009
Micron v. YMTC
IPR2025-00294
Ex. 2009-001

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X. GROUND 1: ~~IN~~DEPENDENT CLAIMS ~~1~~**6** AND ~~11~~**7** A~~ND~~**RE OBVIOUS OVER COSTA IN VIEW OF LIU** **29**

~~**DEPENDENT CLAIMS 2-5, 8-9, 12, 14-19 ARE OBVIOUS OVER COSTA** ..... **29**~~

A. Claim 1 29

1. [1.Pre] "A method of forming a joint opening structure in a three-dimensional (3D) memory device, comprising:" 29

2. [1.A] "forming a first stacked layer and forming a first insulating connection layer on the first stacked layer;". 30

3. [1.B] "forming a first through hole that penetrates the first stacked layer and the first insulating connection layer;" 34

4. [1.C] "forming a first channel structure overlaying the surface of the substrate that is exposed by the first through hole;" 35

5. [1.D] "forming a first functional layer on the sidewall of the first through hole;" 37

6. [1.E] "forming a second channel structure and forming a first filling structure on the sidewall of the first functional layer and the exposed surface of the first channel structure;" 40

7. [1.F] "forming a third channel structure in contact with the second channel structure above the first through hole, wherein a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate;" ..... 4~~5~~**4**

8. [1.G] "forming a second stacked layer and forming a second insulating connection layer on the first insulating connection layer;" .....

5~~4~~2

9. [1.H] "forming a second through hole that penetrates the second stacked layer and the second insulating connection layer, wherein a projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate;" ..... 5~~7~~5

10. [1.I] "forming a second functional layer on the sidewall of the second through hole;" ..... ~~61~~58

11. [1.J] "forming a fourth channel structure and forming a second filling structure on the sidewall of the second functional layer and the exposed surface of the third channel structure; and" ..... 6~~4~~1

12. [1.K] "forming a fifth channel structure in contact with the fourth channel structure above the second through hole." ..... 6~~6~~3

B. ~~Claim 2~~**Motivation to Combine** ..... ~~71~~68

~~1. [2.PRE] "The method of claim 1, wherein:" [2.A] "the first stacked layer includes a first number of oxide/nitride layer pairs; and" [2.B] "the second stacked layer includes a second number of oxide/nitride layer pairs."~~ ..... ~~71~~

C. Claim ~~3~~6 ..... 7~~2~~4

~~1. [3] "The method of claim 2, wherein: the first number and the second number are not less than 32."~~ ..... ~~72~~

~~D. Claim 4~~ ..... ~~72~~

~~1. [4.PRE] "The method of claim 1, wherein forming the first functional layer comprises:" [4.A] "forming a first tunneling layer on the sidewall of the first through hole and the exposed~~

~~surface of the first channel structure, wherein the first tunneling layer is configured, in operation, to generate charges;"~~ ..... ~~72~~

~~2. [4.B] "forming a first storage layer on the surface of the first tunneling layer to store the charges generated by the first tunneling layer;"~~ ..... ~~74~~

~~3. [4.C] "forming a first barrier layer on the surface of the first storage layer to block the outflow of charges in the first storage layer;"~~ ..... ~~75~~

~~4. [4.D] "forming a first passivation layer on the surface of the first barrier layer to protect the first barrier layer from being damaged in a subsequent removal process; and". 77~~

~~5. [4.E] "removing portions of the first passivation layer, the first barrier layer, the first storage layer, and the first tunneling layer on the surface of the first channel structure, wherein remaining portions of the first passivation layer, the first barrier layer, the first storage layer, and the first tunneling layer on the sidewall of the first through hole to form the first functional layer."~~ ..... ~~78~~

~~E. Claim 5~~ ..... ~~80~~

~~1. [5.PRE] "The method of claim 4, wherein forming the second channel structure and the first filling structure comprises:" [5.A] "forming a second channel layer that covers the sidewall of the first passivation layer and the exposed surface of the first channel layer;~~ ..... ~~80~~

~~2. [5.B] "forming the first filling layer that covers the surface of the second channel layer;"~~ ..... ~~80~~

~~3. [5.C] "removing a portion of the first filling layer to form the first filling structure, wherein the top surface of the first filling structure is lower than the top surface of the first insulating connection layer; and [5.D] "removing a portion of the second channel layer to form the second channel~~

~~structure, wherein a top surface of the second channel structure is lower than a top surface of the first insulating connection layer."~~ ..... ~~80~~

~~F. Claim 8~~ ..... ~~87~~

1. [~~8~~6.PRE] "The method of claim 1, ~~further~~**wherein forming the third channel structure** comprisi~~ng~~**es**:" [~~8~~6.A] "~~forming a first mask layer overlaying~~**etching** the first insulating connection layer ~~before forming~~**to form a first groove, wherein a projection of the first groove on the substrate covers the projection of** the first through hole **on the substrate**;~~ and~~" ..... ~~8~~7**4**

1. [6.B] "forming a third channel layer in the first groove, wherein the third channel layer is in contact with the second channel structure; and" **78**

2. [6.C] "planarizing the top surfaces of the first insulating connection layer and the third channel layer to form the third channel structure." **78**

D. Claim 7 ..... **80**

1. [7.PRE] "The method of claim 1, wherein forming the third channel structure comprises:" [7.A] "etching the first insulating connection layer and at least a portion of the top nitride layer of the first stacked layer to form a first groove, wherein a projection of the first groove on the substrate covers the projection of the first through hole on the substrate;" **80**

2. [~~8~~7.B] "~~removing the first mask layer after~~ forming the ~~first filling~~**third channel structure in the first groove, wherein the third channel structure is in contact with the second channel** structure; **and**" ..... 8~~7~~**0**

3. [~~8~~7.C] "~~forming a second mask layer on the second~~**planarizing the top surfaces of the first** insulating connection layer ~~before forming the second through hole; and~~**and the third channel structure.**" ..... 8~~7~~**0**

~~4. [8.D] "removing the second mask layer after forming the second filling structure." 88~~

XI. GROUND 2: DEPENDENT CLAIM 10 IS OBVIOUS OVER COSTA IN VIEW OF LEE 81

A. Motivation to Combine 81

~~C~~**B**. Claim ~~9~~**10** 8~~8~~**3**

1. [~~9~~**10**.PRE] "The method of claim 1, wherein forming the ~~fourth~~**fifth** channel structure ~~and the second filling structure~~ comprises:" [~~9~~**10**.A] "~~forming a fourth channel layer that covers the sidewall of a second functional layer and the exposed surface of the third chanel layer~~**etching the second insulating connection layer to form a second groove, wherein a projection of the second groove on the substrate covers the projection of the second through hole on the substrate**;" 8~~8~~**3**

2. [~~9~~**10**.B] "forming a ~~second filling layer that covers the surface of~~**fifth channel layer in the second groove, wherein the fifth channel layer is in contact with** the fourth channel ~~layer~~**structure**; **and**" 8~~8~~**6**

~~1. [9.C] "removing a portion of the second filling layer to form the second filling structure, wherein the top surface of the second filling structure is lower than the top surface of the second insulating connection layer; and" 89~~

~~2. [9.D] "removing a portion of the fourth channel layer to form the fourth channel structure, wherein a top surface of the fourth channel structure is lower than a top surface of the second insulating connection layer." 90~~

[10.C] "planarizing the top surfaces of the second insulating connection layer and the fifth channel layer to form the fifth channel structure." 88

XII. GROUND 3: INDEPENDENT CLAIM 20 IS OBVIOUS OVER COSTA IN VIEW OF TOYAMA **89**

A. Motivation to Combine **89**

~~H~~**B**. Claim ~~11~~**20** ..... 9~~0~~**2**

1. [~~11~~**20**.PRE] "A joint opening structure of a three-dimensional (3D) memory device, comprising:" ..... 9~~0~~**2**

2. [~~11~~**20**.A] "a first stacked layer disposed overlaying a substrate;" ..... 9~~0~~**3**

3. [~~11~~**20**.B] "a first insulating connection layer disposed on the ..... first stacked layer;" ..... 9~~0~~**3**

4. [20.C] "a second stacked layer disposed on the first insulating connection layer;" **93**

5. [20.D] "a second insulating connection layer disposed on the second stacked layer;" **93**

6. [20.E] "a plurality of channel holes in a first region of the ..... 3D memory device;" **93**

7. [20.F] "a plurality of staircase structure dummy holes in a second region of the 3D memory device; and" **93**

8. [20.G] "a plurality of through array contact barriers in a third region of the 3D memory device;" **94**

~~4~~**9**. [~~11~~**20**.~~C~~**H**] "**wherein each of the plurality of channel holes includes:** a first through hole penetrating the first stacked layer and the first insulating connection layer~~;~~**,**"9~~0~~**6**

~~5~~**10**. [~~11~~**20**.~~D~~**I**] "a first channel structure disposed at the bottom of the first through hole and overlaying the substrate~~;~~**,**" ..... 9~~1~~**6**

~~6.~~ ~~[~~11.~~E~~**[20.J**] "a first functional layer disposed on the sidewall of the firs

~~7~~**12**. [~~11~~**20**.~~F~~**K**] "a second channel structure in contact with the first channel structure disposed on the sidewall of the first functional layer~~;~~**,**" ..... 9~~1~~**6**

~~8~~**13**. [~~11~~**20**.~~G~~**L**] "a third channel structure in contact with the

second channel structure disposed over the first through hole, wherein a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate~~;~~,” ..... 9~~1~~7

~~9. [11.H] “a second stacked layer disposed on the third channel structure;” ..... 92~~

~~10. [11.I] “a second insulating connection layer disposed on the second stacked layer;” ..... 92~~

1~~1~~4. [~~11~~20.~~J~~M] “a second through hole penetrating the second stacked layer and the second insulating connection layer, wherein a projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate~~;~~,” ..... 9~~2~~7

1~~2~~5. [~~11~~20.~~K~~N] “a second functional layer disposed on the sidewall of the second through hole~~;~~,” ..... 9~~2~~7

1~~3~~6. [~~11~~20.~~L~~O] “a fourth channel structure in contact with the third channel structure disposed on the sidewall of the second functional layer~~;~~, and” ..... 9~~2~~7

1~~4~~7. [~~11~~20.~~M~~P] “a fifth channel structure in contact with the fourth channel structure disposed over the second through hole.” ..... 9~~2~~8

~~I. Claim 12 ..... 93~~

~~1. [12.PRE] “The joint opening structure of claim 11, further comprising:” [12.A] “a first filling structure covering the surface of the second channel structure; and” ..... 93~~

~~2. [12.B] “a second filling structure covering the surface of the fourth channel structure;” ..... 93~~

~~3. [12.C] “wherein the first through hole is non-interconnected with the second through hole.” ..... 93~~

~~J. Claim 14 ..... 95~~

~~1. [14.PRE] "The joint opening structure of claim 11, wherein:" [14.A] "the first stacked layer includes a first number of conductor/dielectric layer pairs; and" [14.B] "the second stacked layer includes a second number of conductor/dielectric layer pairs." ..... 95~~

~~K. Claim 15 ..... 95~~

~~1. [15] "The joint opening structure of claim 14, wherein: the first number and the second number are not less than 32." ..... 95~~

~~L. Claim 16 ..... 95~~

~~1. [16.PRE]-[16.B] "The joint opening structure of claim 11, wherein: the first stacked layer includes a first number of oxide/nitride layer pairs; and the second stacked layer includes a second number of oxide/nitride layer pairs ..... 95~~

~~M. Claim 17 ..... 95~~

~~1. [17] "The joint opening structure of claim 16, wherein: the first number and the second number are not less than 32." ..... 95~~

~~N. Claim 18 ..... 95~~

~~1. [18] "The joint opening structure of claim 11, wherein: a thickness of the third channel structure is in a range between 30 nm and 70 nm." ..... 95~~

~~O. Claim 19 ..... 96~~

~~1. [19.PRE] "The joint opening structure of claim 11, wherein:" [19.A] "a size difference between a top aperture and a bottom aperture of the first through hole is equal to or less than 30 nm; and" ..... 96~~

~~2. [19.B] "a size difference between a top aperture~~

~~**and a bottom aperture of the second through hole is equal to or less than 30 nm."**~~ ~~**97**~~

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35 U.S.C. §314(a) 6

35 U.S.C. §325(d) ..... 6, 1~~1~~2

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37 C.F.R. §42.10(b) 7

37 C.F.R. §42.108(a) 6

LISTING OF EXHIBITS

EXHIBIT	DESCRIPTION
1001	U.S. Patent No. 10,886,291 to Lu et al. ("the '291 Patent")
1002	File History of U.S. Patent No. 10,886,291 ("the '291 FH")
1003	Declaration of Dr. Sanjay K. Banerjee ("Banerjee")
1004	*Curriculum Vitae* of Dr. Sanjay K. Banerjee
1005	U.S. Patent Publication No. 2018/0182771 A1 to Costa et al. ("Costa")
1006	U.S. Patent Publication No. 2016/0204117 A1 to Liu et al. ("Liu")
1007	U.S. Patent Publication No. 2015/0060979 A1 to Lee et al. ("Lee")
1008	U.S. Patent Publication No. 2017/0179026 A1 to Toyama et al. ("Toyama")
1009	Aritome, "NAND Flash Memory Technologies" (2016)
1010	Silvagni, "3D NAND Flash Based on Planar Cells," Computers 2017
1011	Micheloni et al., "Inside Solid State Drives (SSDs)" (2nd Ed. 2018)
1012	U.S. Patent No. 10,475,737 to Tang et al.
1013	Micheloni, "3D Flash Memories" (2016)
1014	U.S. Patent No. 9,853,046 to Lu et al.

EXHIBIT	DESCRIPTION
1015	Excerpt from YMTC's Exemplary Infringement Claim Chart for U.S. Patent No. 10,886,291 (Ex. C-1 to Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024) ("Ex. C-1, YMTC's Contentions") [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]
1016	U.S. Patent No. 9,245,962 to Yang et al.
1017	U.S. Patent No. 10,283,518 to Lee et al.
1018	Stavitski et al., "Specific contact resistance measurements of metal-semiconductor junctions," *2006 IEEE International Conference on Microelectronic Test Structures*, Austin, TX, USA, 2006, pp. 13-17
1019	Fasoli et al., "Overview and status of bottom-up silicon nanowire electronics," *Materials Science in Semiconductor Processing*, Vol. 15, Issue 6, 2012, pp. 601-614
1020	U.S. Patent Publication No. 2015/0264548 A1 to Lee et al. ("Lee 548")
1021	U.S. Patent No. 9,530,866 to Zhang et al.
1022	Plummer et al., "Silicon VLSI Technology: Fundamentals, Practice and Modeling" (2000)
1023	Certified Translation of KR 101487746 B1 to Lee et al. (including original Korean patent document)
1024	U.S. Patent Publication No. 2017/0154892 to Oh
1025	Minute Order (case schedule), Dkt. No. 141, dated September 18, 2024 in *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL

EXHIBIT	DESCRIPTION
1026	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1027	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, LTD.'s Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024 in *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL
1028	Docket from *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:24−cv−04223−RFL which has been consolidated with Case No. 3:23-cv-05792-RFL

LISTING OF CHALLENGED CLAIMS

Ref. #	Listing of Challenged Claims
Claim 1:	
[1.PRE]	A method of forming a joint opening structure in a three-dimensional (3D) memory device, comprising:
[1.A]	forming a first stacked layer and forming a first insulating connection layer on the first stacked layer;
[1.B]	forming a first through hole that penetrates the first stacked layer and the first insulating connection layer;
[1.C]	forming a first channel structure overlaying the surface of the substrate that is exposed by the first through hole;
[1.D]	forming a first functional layer on the sidewall of the first through hole;
[1.E]	forming a second channel structure and forming a first filling structure on the sidewall of the first functional layer and the exposed surface of the first channel structure;
[1.F]	forming a third channel structure in contact with the second channel structure above the first through hole, wherein a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate;
[1.G]	forming a second stacked layer and forming a second insulating connection layer on the first insulating connection layer;
[1.H]	forming a second through hole that penetrates the second stacked layer and the second insulating connection layer, wherein a projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate;
[1.I]	forming a second functional layer on the sidewall of the second through hole;

Ref. #	Listing of Challenged Claims
[1.J]	forming a fourth channel structure and forming a second filling structure on the sidewall of the second functional layer and the exposed surface of the third channel structure; and
[1.K]	forming a fifth channel structure in contact with the fourth channel structure above the second through hole.
Claim ~~2~~6:	
[~~2~~6.PRE]	The method of claim 1, wherein **forming the third channel structure comprises**:
~~[2.A]~~	~~**the first stacked layer includes a first number of oxide/nitride layer pairs; and**~~
~~[2.B]~~	~~**the second stacked layer includes a second number of oxide/nitride layer pairs.**~~
~~**Claim 3:**~~	
~~[3]~~	~~**The method of claim 2, wherein: the first number and the second number are not less than 32.**~~
~~**Claim 4:**~~	
~~[4.PRE]~~	~~**The method of claim 1, wherein forming the first functional layer comprises:**~~
[~~4~~6.A]	~~**forming a first tunneling layer on the sidewall of the**~~**etching the first insulating connection layer to form a first groove, wherein a projection of the first groove on the substrate covers the projection of the** first through hole ~~**and the exposed surface of the first channel structure, wherein the first tunneling layer is configured, in operation, to generate charges**~~**on the substrate**;
[~~4~~6.B]	forming a ~~**first storage layer on the surface of the first tunneling layer to store the charges generated by the first tunneling layer**~~**third channel layer in the first groove, wherein the third channel layer is in contact with the second channel structure; and**

~~[4.C]~~	~~forming a first barrier layer on the surface of the first storage layer to block the outflow of charges in the first storage layer;~~

~~Ref. #~~	~~Listing of Challenged Claims~~
~~[4.D]~~	~~forming a first passivation layer on the surface of the first barrier layer to protect the first barrier layer from being damaged in a subsequent removal process; and~~
[~~4~~6.~~E~~C]	~~removing portions~~planarizing the top surfaces of the first ~~passivation layer, the first barrier layer, the first storage layer, and the first tunneling layer on the surface of the first channel structure, wherein remaining portions of the first passivation layer, the first barrier layer, the first storage layer, and the first tunneling layer on the sidewall of the first through hole to form the first functional layer~~insulating connection layer and the third channel layer to form the third channel structure.
Claim ~~5~~7:	
[~~5~~7.PRE]	The method of claim ~~4~~1, wherein forming the ~~second~~third channel structure ~~and the first filling structure~~ comprises:
~~[5.A]~~	~~forming a second channel layer that covers the sidewall of the first passivation layer and the exposed surface of the first channel layer;~~
~~[5.B]~~	~~forming the first filling layer that covers the surface of the second channel layer;~~
[~~5~~7.~~C~~A]	~~removing~~etching the first insulating connection layer and at least a portion of the top nitride layer of the first ~~filling~~stacked layer to form ~~the~~a first ~~filling structure~~groove, wherein ~~the top surface~~a projection of the first ~~filling structure is lower than the top surface~~groove on the substrate covers the projection of the first ~~insulating connection layer~~through hole on the substrate;~~ and~~
[~~5~~7.~~D~~B]	~~removing a portion of the second~~forming the third channel ~~layer to form~~structure in the first groove, wherein the third channel structure is in contact with the second channel structure~~, wherein a top surface of the second channel structure is lower than a top surface of the first insulating~~

	~~connection layer.~~; and
~~Claim 8:~~	
~~[8.PRE]~~	~~The method of claim 1, further comprising:~~
[~~8~~7.~~A~~C]	~~forming a first mask layer overlaying~~planarizing the top surfaces of the first insulating connection layer ~~before forming the first through hole; and~~and the third channel structure.

Ref. #	Listing of Challenged Claims
~~[8.B]~~	~~removing the first mask layer after forming the first filling structure;~~
~~[8.C]~~	~~forming a second mask layer on the second insulating connection layer before forming the second through hole; and~~
~~[8.D]~~	~~removing the second mask layer after forming the second filling structure.~~
Claim ~~9~~10:	
[~~9~~10.PRE]	The method of claim 1, wherein forming the ~~fourth~~**fifth** channel structure ~~and the second filling structure~~ comprises:
[~~9~~10.A]	~~forming a fourth channel layer that covers the sidewall of a second functional layer and the exposed surface of the third channel layer~~**etching the second insulating connection layer to form a second groove, wherein a projection of the second groove on the substrate covers the projection of the second through hole on the substrate**;
[~~9~~10.B]	forming a ~~second filling layer that covers the surface of~~**fifth channel layer in the second groove, wherein the fifth channel layer is in contact with** the fourth channel ~~layer~~**structure**; **and**
[~~9~~10.C]	~~removing a portion of the second filling layer to form the second filling structure, wherein~~**planarizing** the top surface**s** ~~of the second filling structure is lower than the top surface~~ of the second insulating connection layer~~;~~ and **the fifth channel layer to form the fifth channel structure.**
~~[9.D]~~	~~removing a portion of the fourth channel layer to form the fourth channel structure, wherein a top surface of the fourth channel structure is lower than a top surface of the second insulating connection layer.~~
Claim ~~11~~20:	
[~~11~~20.PRE]	A joint opening structure of a three-dimensional (3D) memory device, comprising:
[~~11~~20.A]	a first stacked layer disposed overlaying a substrate;

[~~11~~20.B]	a first insulating connection layer disposed on the first stacked layer;
[20.C]	**a second stacked layer disposed on the first insulating connection layer;**
[20.D]	**a second insulating connection layer disposed on the second stacked layer;**
[20.E]	**a plurality of channel holes in a first region of the 3D memory device;**
[20.F]	**a plurality of staircase structure dummy holes in a second region of the 3D memory device; and**
[20.G]	**a plurality of through array contact barriers in a third region of the 3D memory device;**

Ref. #	Listing of Challenged Claims
[~~11~~20.~~C~~H]	**wherein each of the plurality of channel holes includes:** a first through hole penetrating the first stacked layer and the first insulating connection layer~~;~~,
[~~11~~20.~~D~~I]	a first channel structure disposed at the bottom of the first through hole and overlaying the substrate~~;~~,
[~~11~~20.~~E~~J]	a first functional layer disposed on the sidewall of the first through hole~~;~~,
[~~11~~20.~~F~~K]	a second channel structure in contact with the first channel structure disposed on the sidewall of the first functional layer~~;~~,
[~~11~~20.~~G~~L]	a third channel structure in contact with the second channel structure disposed over the first through hole, wherein a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate~~;~~,
~~[11.H]~~	~~a second stacked layer disposed on the third channel structure;~~
~~[11.I]~~	~~a second insulating connection layer disposed on the second stacked layer;~~
[~~11~~20.~~J~~M]	a second through hole penetrating the second stacked layer and the second insulating connection layer, wherein a projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate~~;~~,
[~~11~~20.~~K~~N]	a second functional layer disposed on the sidewall of the second through hole~~;~~,
[~~11~~20.~~L~~O]	a fourth channel structure in contact with the third channel structure disposed on the sidewall of the second functional layer~~;~~, and
[~~11~~20.~~M~~P]	a fifth channel structure in contact with the fourth channel structure disposed over the second through hole.
~~Claim 12:~~	
~~[12.PRE]~~	~~The joint opening structure of claim 11, further comprising:~~

~~Ref. #~~	~~Listing of Challenged Claims~~

~~[12.A]~~	~~a first filling structure covering the surface of the second channel structure; and~~
~~[12.B]~~	~~a second filling structure covering the surface of the fourth channel structure;~~
~~[12.C]~~	~~wherein the first through hole is non-interconnected with the second through hole.~~
~~Claim 14:~~	
~~[14.PRE]~~	~~The joint opening structure of claim 11, wherein:~~
~~[14.A]~~	~~the first stacked layer includes a first number of conductor/dielectric layer pairs; and~~
~~[14.B]~~	~~the second stacked layer includes a second number of conductor/dielectric layer pairs.~~
~~Claim 15:~~	
~~[15]~~	~~The joint opening structure of claim 14, wherein: the first number and the second number are not less than 32.~~
~~Claim 16:~~	
~~[16.PRE]~~	~~The joint opening structure of claim 11, wherein:~~
~~[16.A]~~	~~the first stacked layer includes a first number of oxide/nitride layer pairs; and~~
~~[16.B]~~	~~the second stacked layer includes a second number of oxide/nitride layer pairs.~~
~~Claim 17:~~	
~~[17]~~	~~The joint opening structure of claim 16, wherein: the first number and the second number are not less than 32.~~

~~Ref. #~~	~~Listing of Challenged Claims~~
~~Claim 18:~~	

~~[18]~~	~~**The joint opening structure of claim 11, wherein: a thickness of the third channel structure is in a range between 30 nm and 70 nm.**~~
~~**Claim 19:**~~	
~~**[19.PRE]**~~	~~**The joint opening structure of claim 11, wherein:**~~
~~**[19.A]**~~	~~**a size difference between a top aperture and a bottom aperture of the first through hole is equal to or less than 30 nm; and**~~
~~**[19.B]**~~	~~**a size difference between a top aperture and a bottom aperture of the second through hole is equal to or less than 30 nm.**~~

I. INTRODUCTION

Petitioner Micron Technology, Inc. ("Petitioner") respectfully requests *inter partes* review of claims ~~1~~6-~~5~~7, ~~8-9, 11-12~~10, and ~~14-19~~20 (the "Challenged Claims") of

U.S. Patent No. 10,886,291 (the "'291 Patent") assigned to Yangtze Memory Technologies Co., Ltd. ("Patent Owner" or "PO"). Concurrently filed herewith, Micron's Explanation for and Ranking of Two Petitions explains the basis for filing ~~the~~this second Petition~~ (IPR2025-00294) challenging~~. **Challenged Claims 6-7 and 10 depend on claim 1, and claim 20 closely mirrors many of claim 1's limitations. This Petition relies on the same Ground 1 (the "Costa Ground") from IPR2025-00244 to demonstrate that the elements of** claims 6-7, 10, and 20 ~~of the '291 Patent~~**are disclosed or rendered obvious**.

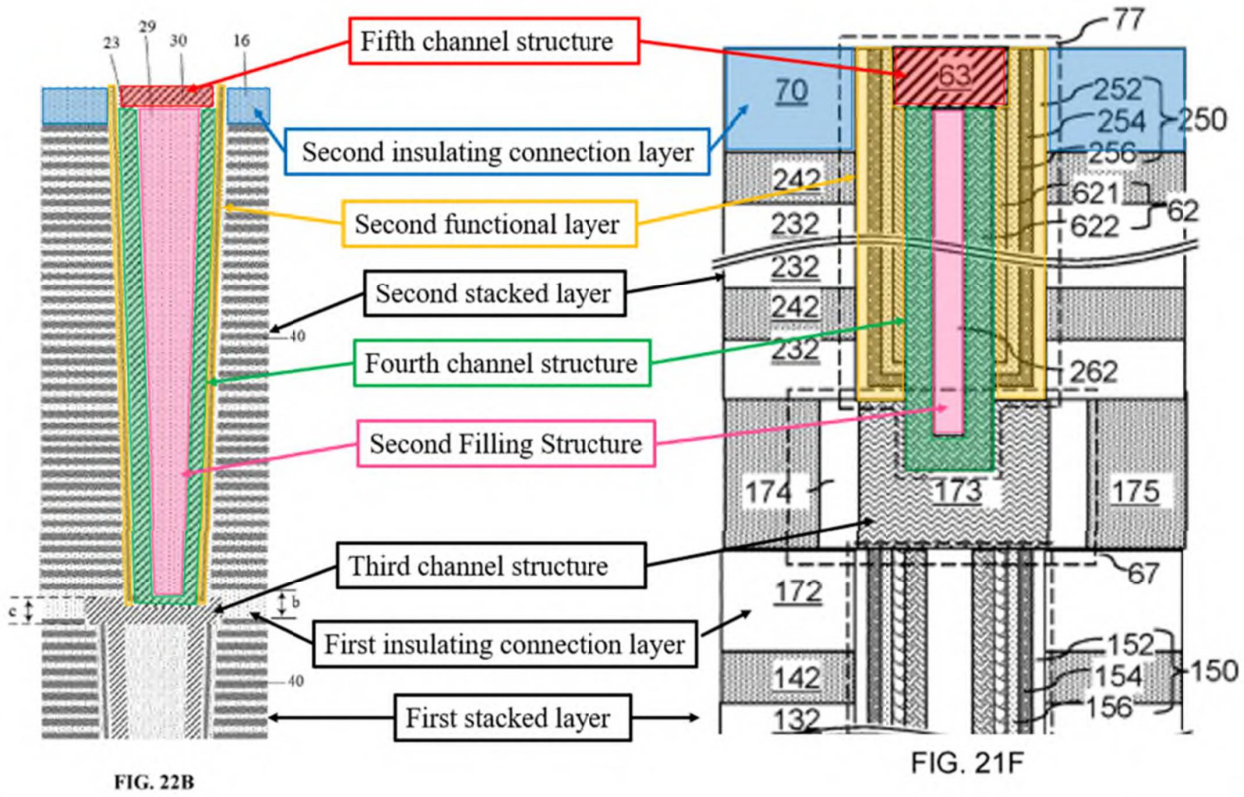
The '291 Patent relates to joint opening structures in 3D memory devices—that is, memory structures formed in two steps: a first memory structure formed in a first deck followed by a second deck in which a second memory structure is formed. The two structures connect to form a continuous vertical memory channel. *E.g.*, Ex. 1001, Figs. 11B, 22B. The '291 Patent admits that such structures were known in the prior art. *Id.*, 1:24-35. Forming a continuous vertical channel requires ensuring that the first and second memory structures are vertically aligned such that the channel therein (e.g., a semiconductive layer) electrically

couple. The challenged claims cover a specific method and configuration of doing so.

The ’291 Patent describes a structure that includes an inter-tier channel structure (the claimed “third channel structure”) that “covers” the first-tier memory through hole, *i.e.*, this third channel structure is “sandwiched” between the upper

and lower decks. Ex. 1001, 2:42-54, Fig. 16 (element 14). Further, the claimed "fifth channel structure" is disposed over a second tier through hole that overlaps with the first through hole. *Id.*, 3:8-16, Fig. 21A (element 30). These elements, along with the two channel structures in respective memory decks, create a continuous vertical memory channel. That the claims require these features (the third and fifth channel structures) was the reason for allowance. Ex. 1002, 722-23.

None of this, however, was new or nonobvious. The Costa prior art reference was not before the Examiner during prosecution of the '291 Patent. Costa discloses each and every structure of claim 1. The figure below maps each claim element in the top deck portion to Costa with the corresponding elements shown in the '291 Patent for comparison.



Ex. 1001, Fig. 11B (annotated, left); Costa, Fig. 21F (excerpted, annotated, right).

The figure below maps each claim element in the bottom deck portion to Costa with the corresponding elements shown in the ’291 Patent for comparison.

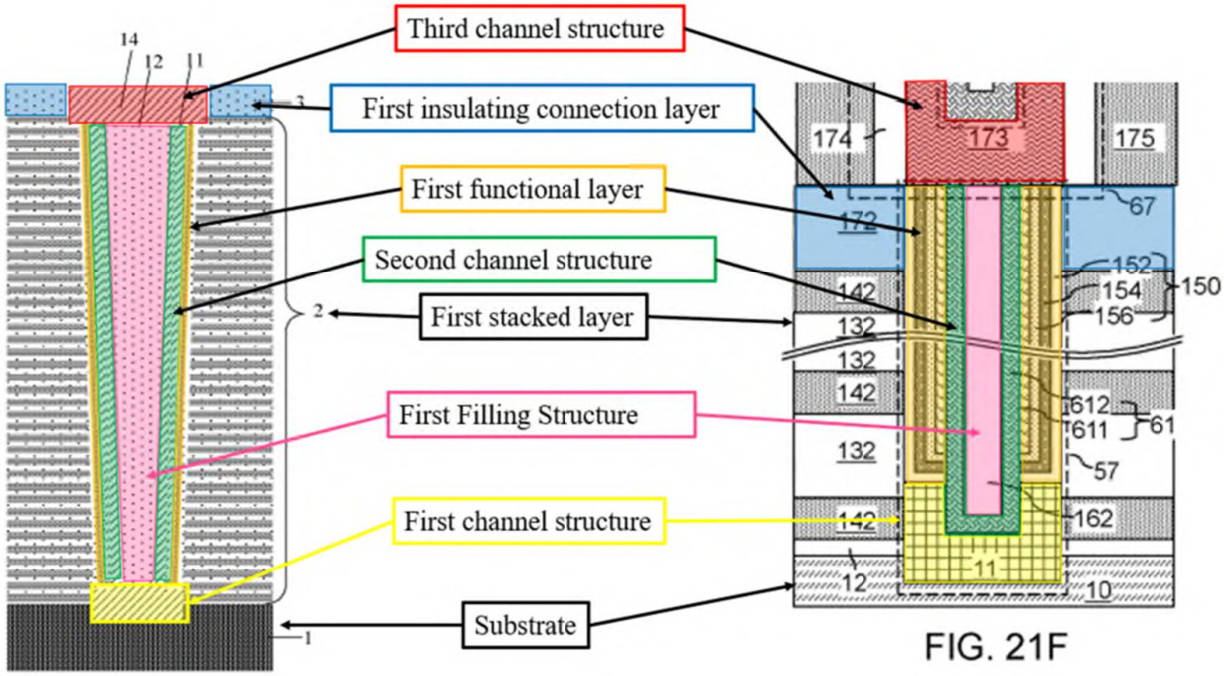


FIG. 11B

Id., Fig. 22B (annotated, left); Costa, Fig. 21F (excerpted, annotated, right).

The dependent claims recite well known structures (and methods for forming such structures) that ~~Costa discloses or~~ were well within the knowledge of a POSITA**, as the secondary references demonstrate**. Petitioner requests that the Board institute trial and find the Challenged Claims unpatentable under §103.

II. MANDATORY NOTICES

A. Real Parties-in-Interest

Petitioner Micron Technology, Inc. and its subsidiaries, including Micron Consumer Products Group LLC, are the real-parties in interest.

B. Related Matters

On July 12, 2024, YMTC asserted the ’291 Patent and U.S. Patent Nos. 10,672,711, 10,879,164, 10,879,254, 11,101,276, 11,145,666, 11,450,604,
11,482,532, 11,568,941, 11,581,322, and 12,010,838 against Micron. On August 21, 2024 the litigation was consolidated with *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023) (“Co- Pending Litigation”). U.S. Patent Nos. 10,658,378, 10,861,872, 10,868,031,
10,937,806, 10,950,623, 11,468,957, 11,501,822, and 11,600,342 were asserted by Patent Owner in the first filed case, leading to a total of 19 patents-at-issue in the now consolidated Co-Pending Litigation.

In addition to this Petition, Petitioner is filing (or has filed) petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation:

Patent	PTAB Proceeding	Wave
10,658,378 (claims 15-17 and 19-20)	IPR2024-00788	Wave 1 Petitions
10,861,872 (claims 1-6 and 11-13)	IPR2024-00789	
10,868,031	IPR2024-00790	
10,937,806 (claims 8-9 and 11-12)	IPR2024-00791	

10,950,623	IPR2024-00794	
11,468,957	IPR2024-00792	

Patent	PTAB Proceeding	Wave
11,501,822	IPR2024-00795	
11,600,342 (claims 1-6 and 8-20)	IPR2024-00793	
10,658,378 (claims 1-7 & 18)	IPR2024-00909	Wave 2 Petitions
10,861,872 (claims 7-10)	IPR2024-00910	
10,937,806 (claim 10)	IPR2024-00911	
11,600,342 (claim 7)	IPR2024-00912	
10,672,711	IPR2025-00117	Wave 3 Petitions
10,879,164	IPR2025-00118	
10,879,254	IPR2025-00034	
10,879,254	IPR2025-00119	
11,101,276	IPR2025-00228	
11,145,666	IPR2025-00189	
11,450,604	IPR2025-00035	
11,482,532	IPR2025-00245	
11,568,941	IPR2025-00190	
11,581,322	IPR2025-00191	
12,010,838	IPR2025-00229	
10,886,291 (claims ~~6~~1-~~7~~5, ~~10~~8-9, ~~& 20)~~11-12, & 14-19)	IPR2025-002~~9~~44	

The Director and the Board should allow this Petition under 35 U.S.C. §314(a), 35 U.S.C. §325(d), and/or 37 C.F.R. §42.108(a). Concurrently filed herewith, Micron's Explanation for and Ranking of Two Petitions explains the

basis for filing ~~the~~this second Petition ~~(IPR2025-00294)~~ challenging a different set of claims ~~6-7, 10, and 20~~ of the '291 Patent.

C. Counsel, Service, and Fee Information

Petitioner designates the following counsel:

Lead Counsel	Back-Up Counsel
Jeremy Jason Lang Registration No. 73,604 (jlang@orrick.com) Postal & Hand-Delivery Address: Orrick, Herrington & Sutcliffe LLP 1000 Marsh Road Menlo Park, CA 94025-1015 T: 650-614-7400; F: 650-614-7401	Thomas James Registration No. 74,109 PTABDocketT6J1@orrick.com. Postal & Hand-Delivery Address: Orrick, Herrington & Sutcliffe LLP 353 N Clark Street Suite 3600 Chicago, IL 60654 T: 312-924-9800 F: 312-924-9899 Jared Bobrow *Pro Hac Vice* to be submitted (jbobrow@orrick.com) Postal & Hand-Delivery Address: Orrick, Herrington & Sutcliffe LLP 1000 Marsh Road Menlo Park, CA 94025-1015 T: 650-614-7400; F: 650-614-7401

Petitioner consents to service by electronic mail at the following addresses: PTABDocketJJL2@orrick.com, PTABDocketT6J1@orrick.com, PTABDocketJ3B3@orrick.com, and micron-ymtc_ohs@orrick.com. Pursuant to 37 C.F.R. §42.10(b), Petitioner's Power of Attorney is attached.

The USPTO is authorized to charge the filing fee and any other fees

incurred by Petitioner to the deposit account of Orrick, Herrington, & Sutcliffe LLP: 15-0665.

III. REQUIREMENTS FOR *INTER PARTES* REVIEW

A. Grounds for Standing

Petitioner certifies that the '291 Patent is available for IPR, and that Petitioner is not barred or estopped from requesting this IPR. Petitioner was served with a complaint alleging infringement of the '291 Patent on July 12, 2024. This petition was filed within 1 year of this date.

B. Identification of Challenged Claims and Statement of Precise Relief Requested

Petitioner requests IPR of claims ~~1~~6-~~5~~7, ~~8-9, 11-12~~10, and ~~14-19~~20. This petition ~~discusses claim construction, explains why the claims are unpatentable, provides details regarding where the various claim limitations are found in the prior art, and~~ is supported by the accompanying Declaration of Dr. Sanjay K. Banerjee (Ex. 1003, "Banerjee"), a leading expert in the 3D NAND field.

The application for the '291 Patent was filed on July 26, 2018 and claims priority to an earlier filed PCT publication No. PCT/CN2018/077785, filed March 1, 2018, which claims priority to Chinese Patent Application No. 201710134782.1, filed March 8, 2017, and Chinese Patent Application No. 201710134783.6, filed March 8, 2017. This Petition assumes that March 8, 2017

is the priority date for the ’291 Patent (the “Priority Date”).

Petitioner relies on the following references under the grounds presented in the following table:

Ground	Claim(s)	Prior Art Asserted
1	~~1~~6-~~5~~7~~, 8-9, 11-~~	Obvious under §103 based on U.S. App. Pub. No. 2018/0182771 (Ex. 1005, "Costa")[1] in view of U.S. App. Pub. No. 2016/0204117 (Ex. 1006, "Liu")[2]
2	1~~2~~0~~, 14-19~~	Obvious under §103 based on Costa in view of U.S. App. Pub. No. 201~~8~~5/~~0182771~~0060979 (Ex. 100~~5~~7, "~~Costa~~Lee")[~~1~~3]
3	20	Obvious under §103 based on Costa in view of U.S. App. Pub. No. 2017/0179026 (Ex. 1008, "Toyama")[4]

IV. INSTITUTION SHOULD BE GRANTED

Petitioner has established a reasonable likelihood of success on the merits. All other requirements for IPR have been met. The Board should institute IPR.

A. There are No Grounds for a § 314 Discretionary Denial in this Case

Petitioner submits that it presents a "compelling" case and thus the Board should not discretionarily deny. 6/21/22 Interim Procedure, 2, 4-5.

[1] Costa was filed on February 28, 2017 and is prior art under at least AIA § 102(a)(2).

[2] Liu was filed on March 24, 2016 and is prior art under at least AIA § 102(a)(2).

[3] Lee was filed on August 28, 2014 and published on March 5, 2015 and is prior art under at least AIA § 102(a)(2).

[4] Toyama was filed on September 19, 2016 and is prior art under at least AIA

§ 102(a)(2).

Petitioner also notes that the discretionary denial factors collectively weigh in favor of institution. See *Apple Inc. v. Fintiv, Inc.,* Case No. IPR2020-00019, Paper No. 11 (Mar. 20, 2020) (precedential) ("Fintiv").

1. Possibility of a Stay

Petitioner intends to seek a stay if the Board institutes IPR. This factor is neutral.

~~[1] Costa was filed on February 28, 2017 and is prior art under at least AIA § 102(a)(2).~~

2. Proximity of the Court's Trial Date

On September 18, 2024, the district court entered a scheduling order which set a trial date of June 15, 2026. *See* Ex. 1025. If IPR proceedings are instituted, they should be completed well before the scheduled trial date. *See also* Ex. 1026 (statistics indicating that it takes on average 48.9 months to reach trial in district). This weighs strongly in favor of institution.

3. Investment in the Parallel Proceeding

Regarding the Co-Pending Litigation, to date, the parties and the district court have invested very little in the parallel proceeding. Indeed, beyond engaging in some motion practice regarding the pleadings and consolidation, little substantive progress has been made. Virtually no progress has been made in connection with the later asserted YMTC patents. This includes the '291 patent and other "Wave 3" patents discussed above. *See supra* § II.D. The parties only just completed the exchange of contentions for the Wave 3 patents but have not taken any depositions regarding any of the patents in the Co-Pending Litigation. Fact discovery is in its infancy. No claim-construction positions have been exchanged for the Wave 3 patents, no claim- construction order has issued, no infringement or invalidity expert discovery has occurred, and no summary judgment motions have been filed. This weighs in favor of institution. *See Sand Revolution* at 11.

The Board also has explained that institution is appropriate where "the

petitioner filed the petition expeditiously…." *Fintiv* at 11. Here, on July 12, 2024, PO asserted eleven Wave 3 patents against Petitioner, and subsequently asserted 149 claims across those patents. Ex. 1027. Petitioner proceeded with diligence, starting the filing of eleven petitions approximately three months after being served with the YMTC2 complaint. Ex. 1028. This also weighs strongly in favor of institution.

4. Issue Overlap

Should the Board institute, Micron stipulates that it will not advance in District Court any of the grounds in this Petition. Micron submits that this eliminates any potential overlap in issues between the proceedings here and in District Court. The Board has found that such stipulations weigh in favor of institution. *Sand Revolution* at 11-12.

5. Party Overlap

Both Petitioner and Patent Owner are parties in the parallel proceeding. This, however, is of little moment as there is often party overlap when there is a parallel proceeding.

6. Other Circumstances

Here, Petitioner submits that its petition has significant substantive merit. It is premised on clear, understandable prior art that plainly teaches the claimed subject matter. Thus, this factor also weighs in favor of institution.

B. Denial Under §325(d) Would Be Inappropriate

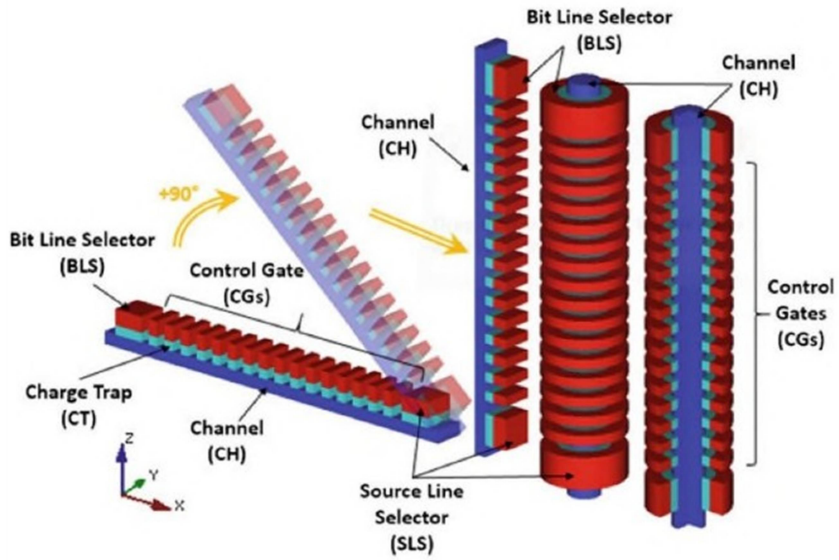
The Examiner did not consider Costa, and thus denial under §325(d) would be inappropriate. Moreover, the apparent point of novelty of the independent claims is the "third channel structure" covering the first through hole and the "fifth channel structure" in contact with the fourth channel structure. *See* §VI.B. Costa squarely discloses these limitations. *See* §X.A.7, 12.

V. TECHNOLOGY BACKGROUND

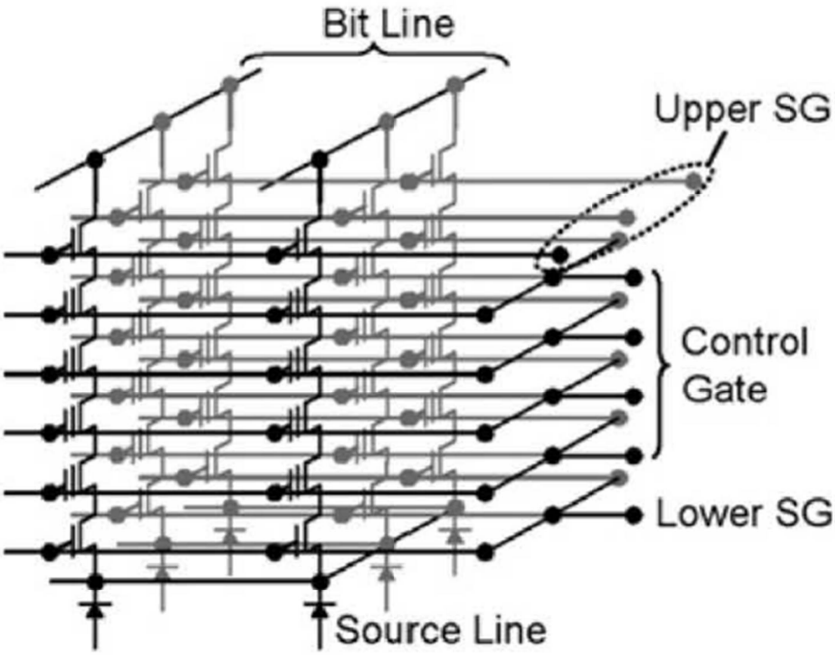
The '291 Patent and the prior art discussed in this Petition relate to three-dimensional (3D) memory devices, e.g., 3D NAND memory devices. Banerjee, ¶¶ 41-42.

In NAND memory devices, NAND cells are arranged in "strings" with multiple cells "connected in series." Ex. 1009, 38. "[T]o further scale down the memory cell size," "three-dimensional (3D) NAND flash cells" were developed. *Id.*,

292. "Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block" and "turning the 2D NAND string upside," "resulting" in a "3D structure" with a "vertical channel." Ex. 1010, 3.



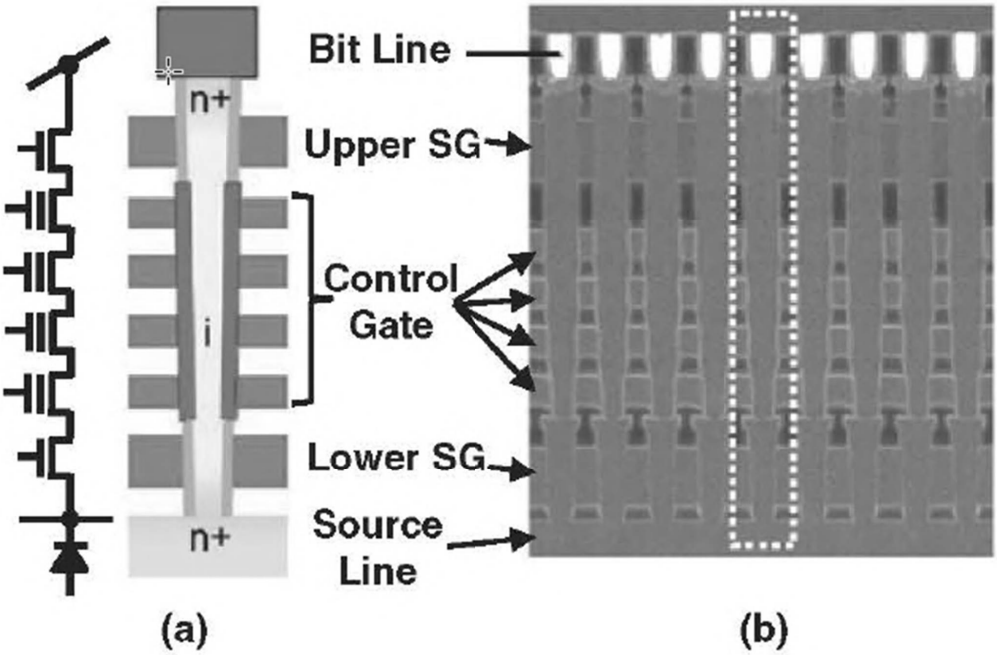
Ex. 1011, 122. Multiple such vertical channels are then repeated in a three-dimensional array:



Ex. 1009, 296~~:~~; Banerjee ¶¶ 43-44.

3D NAND includes "multi-stacked layers of gate (plate)" material alternated

with "dielectric" in a "[s]tack." Ex. 1009, 294. These stacks are known as "memory stacks." A "through-hole[]" channel (also known as a channel structure) "filled by memory film … and channel poly-Si" passes through the layers of the memory stack to form the string of vertically arranged memory cells. *Id.*, 295. "Each" layer of "electrode plate acts as a control gate." *Id.* **A memory cell "is located in the intersection of a control gate plate" and the memory film/poly-Si channel. *Id.*** An example 3D NAND vertical memory cell string is shown below:



Id., 296; Banerjee, ¶¶ 45-46.

To access each memory cell via its control gate (also known as a word line), it was well known to use staircase structures ~~(20~~**, which provide landing areas on the control gates for contacts (below, the contacts 60 connect to different control gates**):

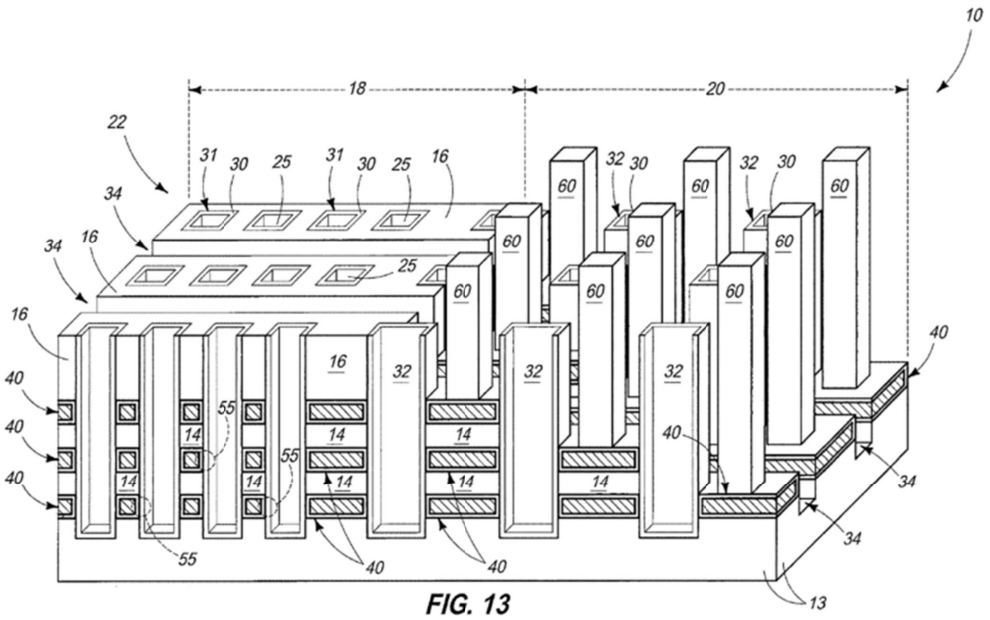


FIG. 13

Ex. 1012 (U.S. Pat. 10,475,737), Fig. 13, 4:56-64, 8:45-56; Banerjee, ¶¶ 47-49.

Multi-deck 3D memory devices became well known before 2017, i.e., a device that includes two memory stacks: one on top of the other. The driving motivation for multi-deck structures is the difficulty in etching high aspect ratio channel holes. This challenge became a limiting factor to memory density. Ex. 1013, 211-215. A multi-deck structure, however, enables the formation of high aspect ratio channel holes by forming the first deck, etching a hole through the first deck, forming the second deck, and then etching another hole through the top deck. The resulting structure includes two channel structures (each also known as a sub- channel structure) that connect via an interface, e.g., inter-deck plug. ~~**An example is shown below:**~~

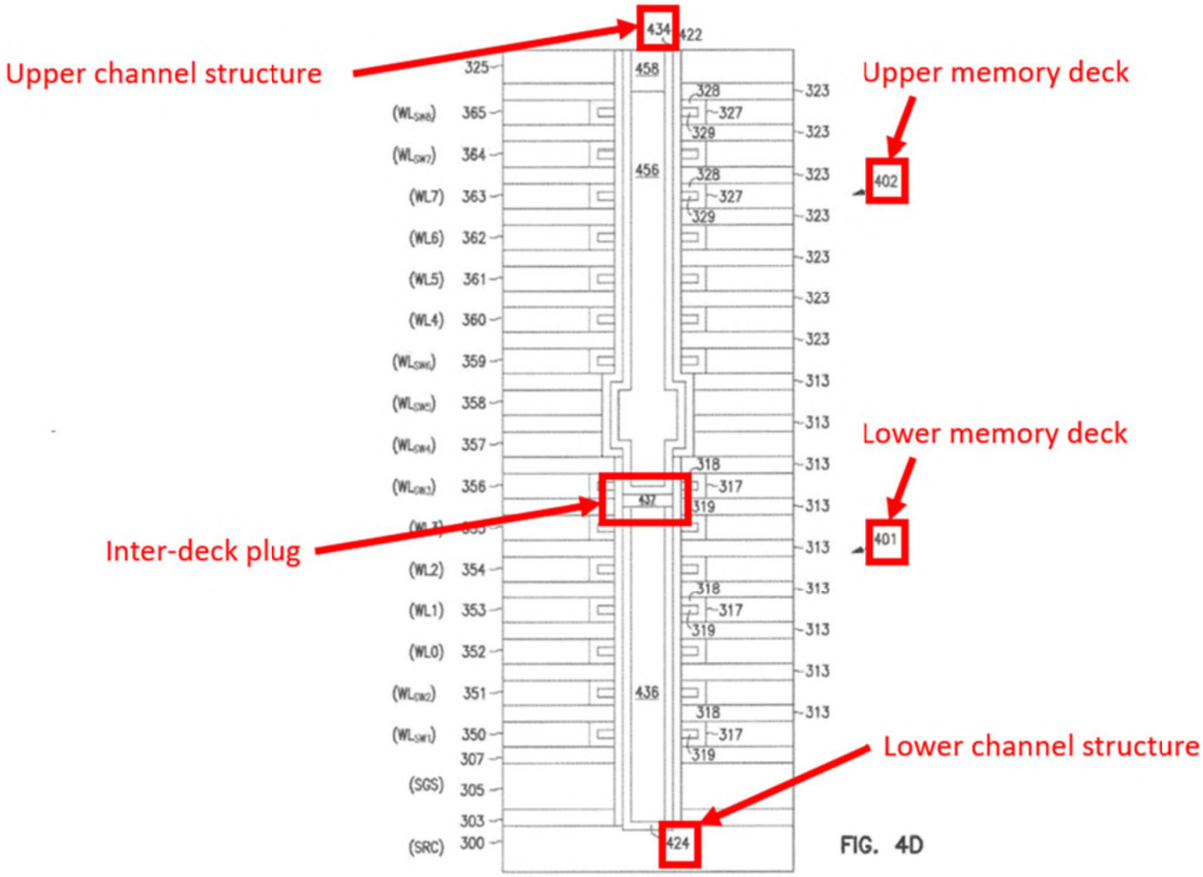


FIG. 4D

Ex. 1014 (U.S. Pat. 9,853,046), Fig. 4D (annotated); Banerjee ¶¶ 50-52.

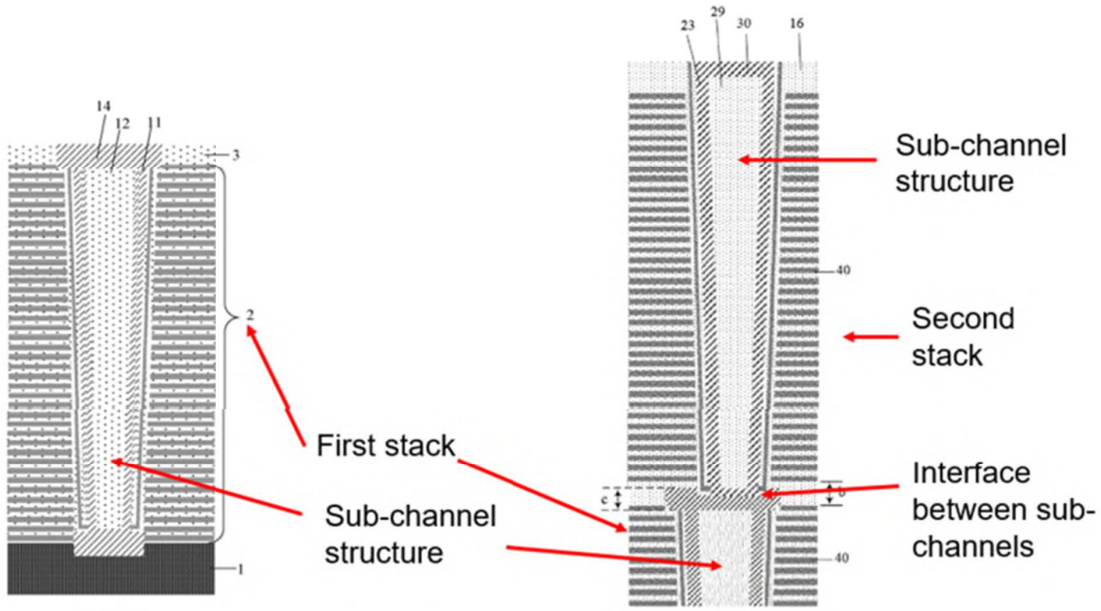
VI. THE '291 PATENT AND ITS PROSECUTION HISTORY

A. '291 Patent Summary

The '291 Patent ~~primarily~~ relates to multiple-stack three-dimensional (3D) memory devices**, *e.g.* 3D multiple-stack NAND devices**. Ex. 1001, 1:15-35. According to the '291 Patent **specification**, "3D NAND memory devices[] keep scaling more oxide/nitride (ON) layers" due to advances in semiconductor technology, creating difficulty in "us[ing] a single etching process to form the channel holes" as the depth

(i.e., number of layers) increases. *Id.* "Thus, a single etching method may not be efficient in both cost and process capability." *Id.*, 1:34-35.

~~To mitigate these purported problems,~~ The '291 Patent proposes a ~~multiple- stack~~**multiple-stack** structure employing certain joint opening structures~~, and methods for forming the same~~. *See generally* Ex. 1001. In short, the '291 Patent relates to forming a first memory stack, forming a sub-channel structure therein, forming a second memory stack on the first stack, and forming a sub-channel structure therein that connects to the first sub-channel.



Id., Figs. 11B (annotated), 22B (annotated). The '291 Patent claims refer to the features that comprise the above sub-channels and interface therebetween

as the first,

second, third, fourth, and fifth channel structures, the first and second functional

layers, and the first and second filling structures. *See generally id.* Petitioner describes each claimed feature below in mapping the claims to the prior art to aid in understanding the '291 Patent's disclosure and respective claim elements.

B. '291 Patent File History

On February 20, 2020, the Examiner rejected claims 11 and 13-19 as obvious over U.S. Pub. 2013/0109158 ("Lee '158) in view of U.S. Pub. 2013/0203227 ("Huo"). Ex. 1002, 682, 684. [25] On April 1, 2020, Applicant made numerous arguments against Examiner's rejections to independent claim 11. Specifically, Applicant argued that "claim 11 recites at least the below features that distinguish over the applied references:

> ~~**a third channel structure in contact with the second channel structure disposed over the first through hole, wherein a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate;**~~
>
> ~~...~~

---

[25] An Office Action dated October 10, 2019 required Applicant to make an election between claims 1-10 (method claims) and claims 11-20 (apparatus claims). Ex. 1002, 672-73. Applicant elected claims 11-20, without traverse. *Id.*, 676. However, the Examiner later withdrew the requirement for election and allowed claims 1-10. *Id.*, 722.

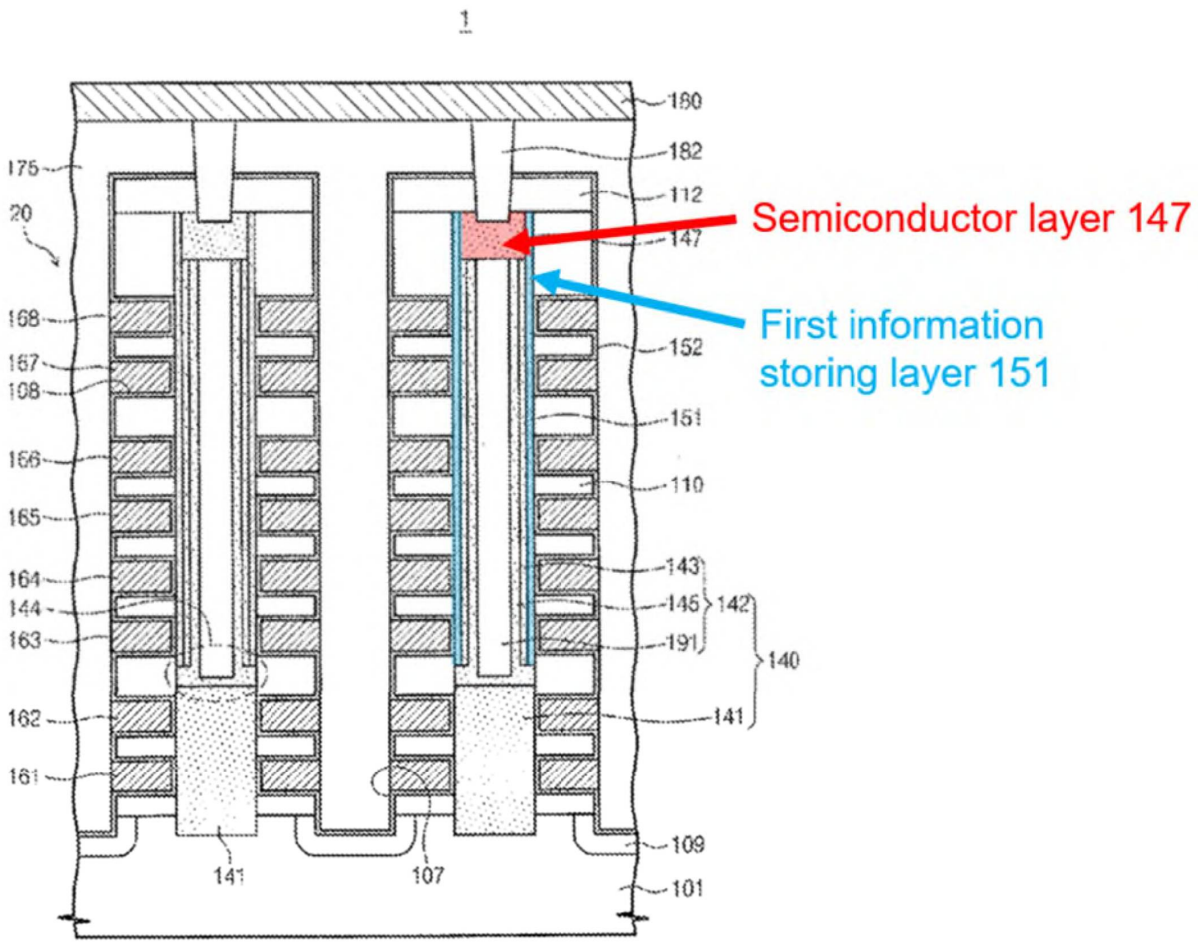
> **a third channel structure in contact with the second channel structure disposed over the first through hole, wherein a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate;**
>
> **…**
>
> **a fifth channel structure in contact with a fourth channel structure disposed over the second through hole**,

Id., 706 (emphasis in original). On July 16, 2020, the Examiner allowed the claims, citing the same claim language that Applicant cited as the reason for allowance. *Id.*, 722-23.

In further regard to Lee '158 and the third channel structure, Applicant argued that the semiconductor layer 147 of Lee '158 "cannot cover a projection of the first through hole" because it is "formed ***within*** the channel hole 103 and ***encircled by*** first information storing layer 151." Ex. 1002, 707 (emphasis in original). In other words, as shown below, the semiconductor layer 147 does not at

least meet the walls of the through hole of Lee ’158:

Fig. 1P



Ex. 1002, at 708 (Fig. 1P) (annotated).

Regarding the fifth channel structure, Applicant argued that Huo does not disclose any fifth channel structure in contact with the fourth channel structure, and that because the lower and upper sub-channels are distinct and different structures, the Examiner's assumption that an element of the lower sub-channel would be on the upper sub-channel and satisfy the fifth channel structure element is incorrect. Ex. 1002, 708-09.

VII. CLAIM CONSTRUCTION

For purposes of this Petition, Petitioner submits the '291 Patent's claims do not require further construction and should receive their plain and ordinary meaning. ~~**For claim 4, however, Micron applies YMTC's claim interpretation that is evident from its infringement contentions in the Co-Pending Litigation. This section addresses the plain and ordinary meaning of claim 4 and YMTC's incorrect claim interpretation.**~~

~~**In short, YMTC distorts the plain language of claim 4 such that it covers "the first functional layer" with an order of layers that is the opposite of what claim 4 requires. For context, the "first the functional layer" of claim 4 corresponds to Figure 4:**~~

~~**Ex. 1001, Fig. 4 (full and partial, annotated). The specification describes, first, forming the tunneling layer (7) on the sidewall of first through hole (5) and on the top surface of first channel structure (6). *Id.*, 10:44-55. Then, the storage layer (8) is formed on the surface of the tunneling layer (7), the barrier layer (9) is formed on the surface of the storage layer (8), the passivation layer (10) is formed on the surface of barrier layer (9), and portions of (7)-(10) on the first channel structure (6) are removed. *Id.*, 10:44-11:17.**~~

~~**Claim 4's "functional layer" requires Figure 4's ordering of layers**~~

~~**because it requires "forming a *first tunneling layer* on the *sidewall of the first through hole*,"**~~

~~**"forming a *first storage layer* on the *surface of the first tunneling layer*," etc. Ex. 1001, Claim 4. In short, the outer surface of the tunneling layer must be formed on the sidewall of the hole (i.e., nearest the gate layers), because claim 4 requires it to be formed "on the sidewall of the first through hole"; the storage layer must be formed to the inner surface of the tunneling layer, because claim 4 requires it to be formed "on the surface of the first tunneling layer." The same is true for the barrier and passivation layers.**~~

~~**YMTC, however, interprets the claim language to read on forming the three layers nearest the sidewall of the hole (i.e., nearest to the gate layers) in the reverse order, such that from the sidewall of the hole (i.e., nearest the gate layers) to the interior of the hole, the layers are formed in the following order: barrier layer, storage layer, tunneling layer, and passivation layer. Ex. 1015, Ex. C-1, YMTC's Contentions, 31-33. YMTC is apparently interpretating the claims to mean that (1) the steps may be performed out of order, and (2) X is formed on Y even if Y doesn't exist when X is formed. This is apparent, e.g., from YMTC's identification of the "first storage layer" in its contentions. Claim 4 requires: "forming a first storage layer on the surface of the first**~~

~~**tunneling layer." But in the accused product, when the alleged "first storage layer" is formed, the "tunneling layer" has yet to be deposited. *Id.*. Thus, YMTC is interpreting the claim such that the "first storage layer" is formed on the "tunneling layer" if the "tunneling layer" is subsequently**~~

~~**formed on the "first storage layer." This interpretation flies in the face of the plain and ordinary meaning of claim 4, because it reads out from the method steps that the particular layers must be formed ("forming") on specific layers. No lexicography exists in the specification to justify such a departure from the plain and ordinary meaning of claim 4. Nevertheless, Micron advances this interpretation only for claim 4, because Costa discloses the exact ordering (and forming) of layers that YMTC asserts falls within the scope of claim 4.**~~

VIII. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA in the field of the '291 Patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience). This POSITA would have been aware of

and generally knowledgeable about 3D NAND's structure, how it is manufactured, and its component parts. *See* Banerjee, ¶¶ 36-40.

IX. PRIOR ART OVERVIEW

A. Costa

Costa relates to "multi-tier three-dimensional memory devices containing dummy memory cells for providing inter-tier connection and methods of making the same." Costa, [0002]. As explained below, just like the '291 Patent, Costa discloses

forming a vertical memory channel (shown in green below) in a multi-tier three- dimensional memory structure:

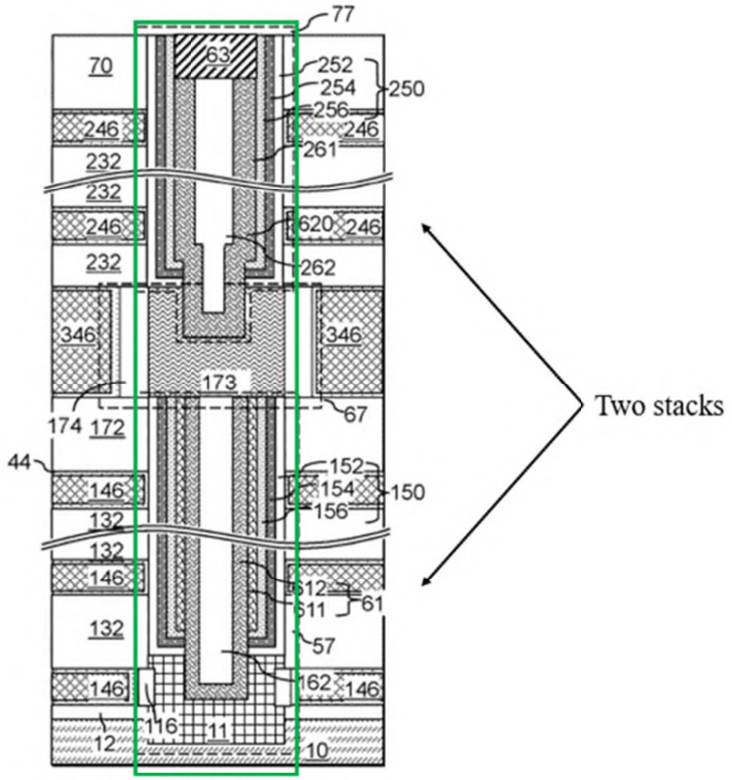


FIG. 21G

Id., Fig. 21G (annotated); Banerjee, ¶¶ 86-87. And Costa identifies the same problem to be overcome as does the '291 Patent—namely, that forming channel holes becomes more difficult as the aspect ratio of the holes increases due to the increased number of layers. Costa, [0003] ("Some of the challenges for fabricating a multi-tier memory stack structure include formation of memory openings having high aspect ratios and alleviation of effects of misalignment of tier-level memory openings formed in different tier structures."). Thus, Costa provides methods "for

providing a reliable connection between vertically neighboring memory stack structures." Costa, [0003].

Specifically, Costa discloses forming "first alternating stack (132, 142)" on substrate 10. Costa, [0126]-[0127]. First-tier insulating cap layer 172 is formed over the first alternating stack (132, 142) to form the first tier structure (132, 142, 172), which can be patterned to form "a first terrace region" located in a contact region of the device. *Id.*, [0134]-[0135]. First-tier openings (149, 119) are then formed for example by lithographic patterning and an anisotropic etch process. *Id.*, [0137].

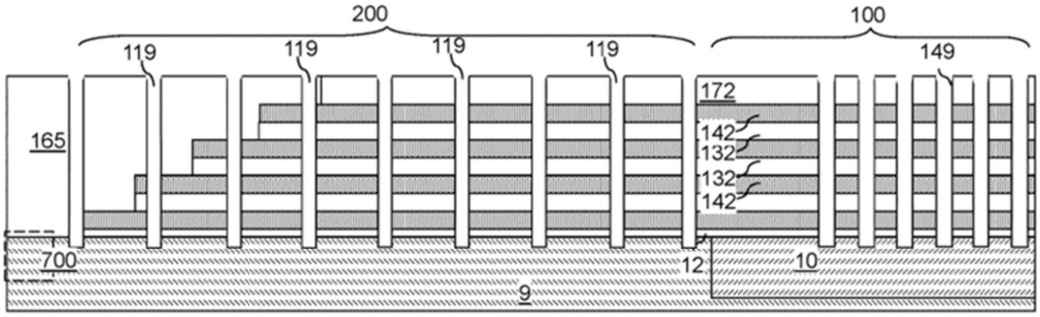


FIG. 3B

Id., Fig. 3B. A memory channel is formed in first-tier memory openings 149 by first forming epitaxial channel portion 11 in the bottom of each hole, subsequently forming a memory film 150 and first outer and inner semiconductor channel layers (611, 612), and filling the remainder of the opening with dielectric core 162. *Id.*, [0141]-[0160].

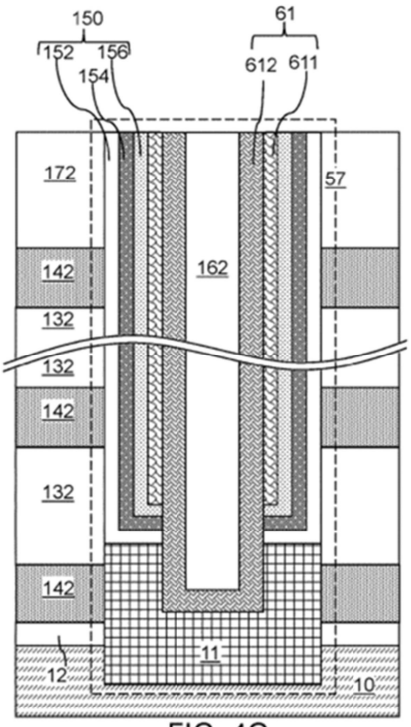


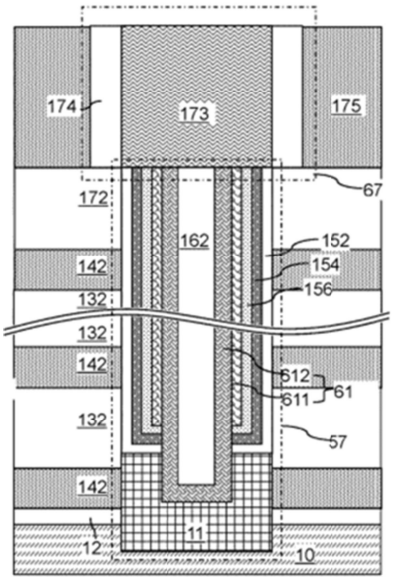
FIG. 4G

Id., Fig. 4G. In one embodiment, a joint-level doped semiconductor layer 173L is formed over the first-tier structure (*e.g.*, shown above in Fig. 4G) and subsequently patterned, removing the portions not over first-tier openings (149, 119), leaving joint-level doped semiconductor portion 173. *Id.*, [0263]-[0266], Figs. 20A-B. Costa states that "[i]n one embodiment, the bottom surface of each joint-level doped semiconductor portion 173 can contact an entire top surface of an underlying first memory opening fill structure 57." *Id.*, [0265]. ~~**Exposed portions of semiconductor portion 173 can be oxidized, converting those portions to dielectric material 174'. *Id.*, [0266], Fig. 20C. An annular dielectric spacer is formed by removing the top portion of 174'.**~~ *Id.*, [0268], [0266] **("In an alternative embodiment shown in the dashed line inset in FIG.**

20C, only the sidewalls of the joint-level doped semiconductor portions 173 are oxidized to form a first annular dielectric spacer 174."), Fig. 20C. Joint-level spacer material 175 is

then deposited over the first-tier structure and around semiconductor portion 173 and dielectric spacer 174. *Id.*, [0268].

FIG. 20D



Id., Fig. 20D.

A second-tier structure and memory channel are formed in much the same way as the first-tier structure. ~~**A second alternating stack (232, 242) is formed over joint level spacer 175, joint-level doped semiconductor portion 173, and dielectric spacer 174.**~~ Costa, [270], [0178]-[0180]~~**. Second-tier insulating cap layer 70 is formed over the second alternating stack and second-tier memory openings 249 are formed by a similar process to that of first-tier memory**~~

~~holes 149. *Id.*~~, [0183]-[0192], [0272]- [0276]. Drain region 63 is then formed in a recess etched into dielectric core 262 and second inner semiconductor channel layer 622). *Id.*, [**0277]. Drain region 63 is deposited in and above the dielectric core cavity, and overlying material is planarized. *Id.*, [**0212], [0277] **(referring to [0212] description)**.

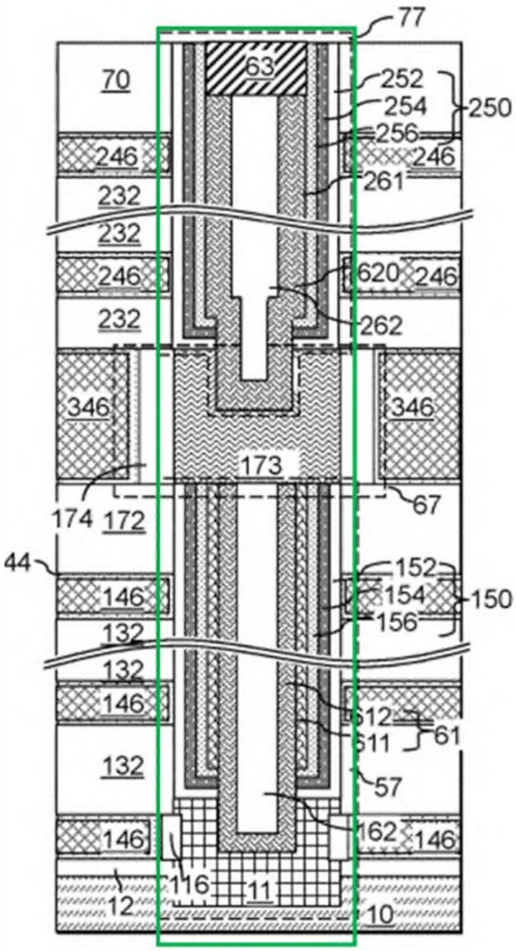


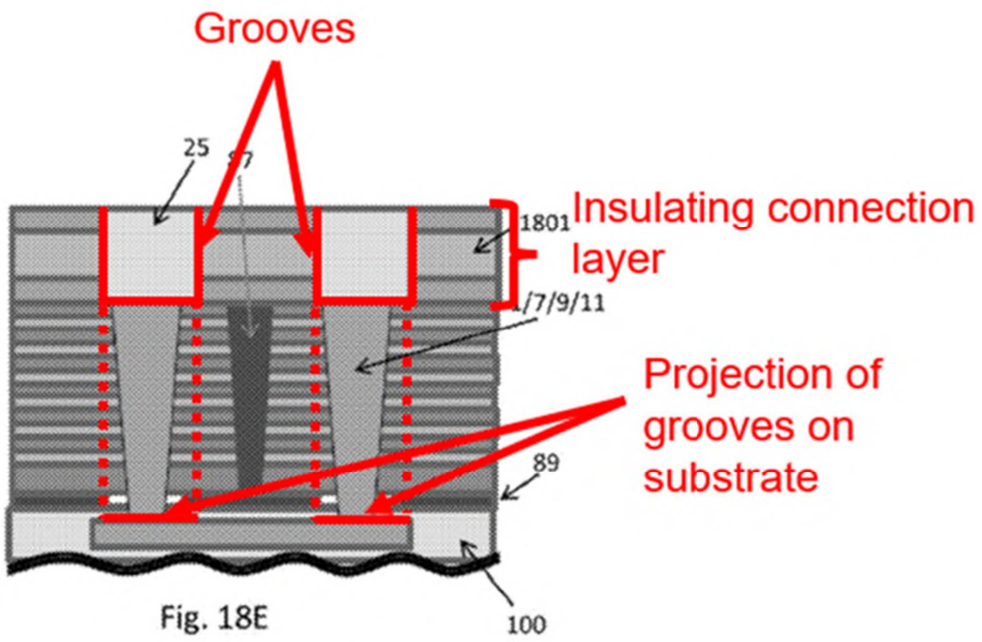
FIG. 21G

Id., Fig. 21G (annotated). Thus, a vertical memory channel (shown in green above) is formed. *Id.*, [0278].

B. Liu

Liu relates to "three dimensional vertical NAND strings" and, more specifically, to facilitating "[a]lignment between memory openings through multiple tier structures [by] employing a temporary landing pad" with "a greater area than the horizontal cross-section[]" of the first-tier memory opening. Liu, Abstract, [0002]. Liu discloses depositing insulating layer

121A, boosting layer 1801, and insulating layer 121B over the first memory stack and subsequently creating a groove over the lower-level memory holes by an etching process, as shown in Figure 18E below. *Id.*, [0173].

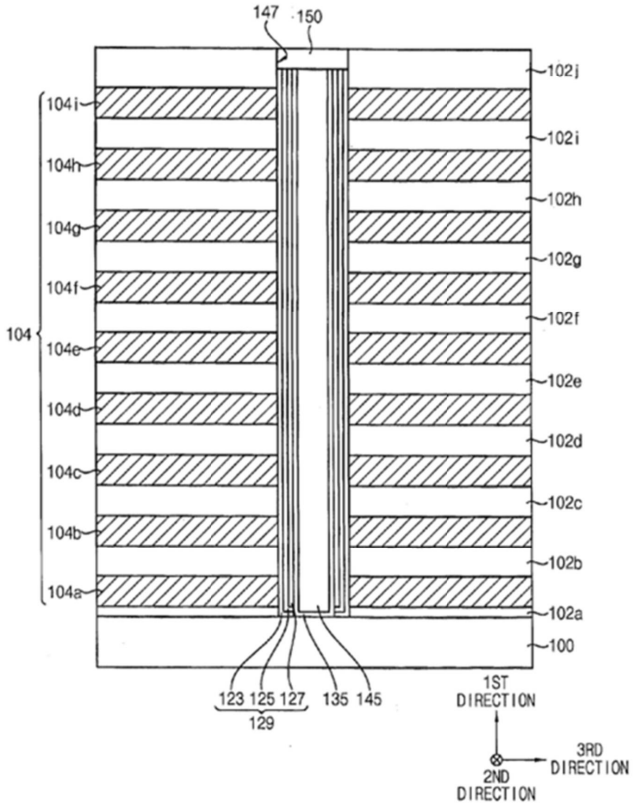


***Id.*, Fig. 18E (annotated); Banerjee ¶¶ 104-105.**

C. Lee

Lee relates to "[v]ertical memory devices and methods of manufacturing the same." Lee, Title. Lee discloses forming a doped polysilicon recessed pad 150 by forming a recessed groove atop the memory through hole wherein the groove is at least as wide as the original through hole for the memory structure. *Id.*, [0093]- [0094].

FIG. 8



***Id*, Fig. 8; Banerjee ¶¶ 107-108.**

D. Toyama

Toyama relates to "three-dimensional non-volatile memory devices" that comprise multiple tiers. Toyama, Abstract, [0002], Figs. 49, 50A, 50B. Toyama discloses "through-memory-level via regions 600" that contain "through-memory- level via structures 676" (*i.e.*, through array contacts) and "insulating liners 674." *Id.*, [0333], [0340]-[0342], Fig. 49.

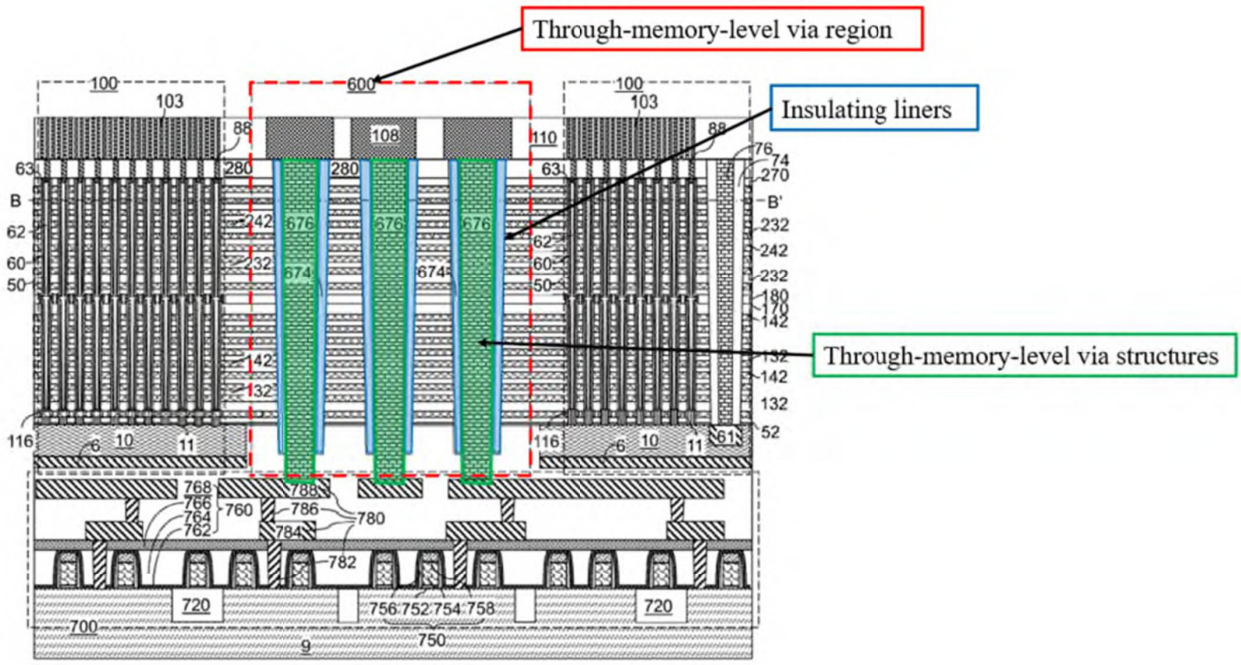


FIG. 49

***Id.*, Fig. 49 (annotated); Banerjee ¶¶ 110-111.**

X. GROUND 1: ~~INDEPENDENT CLAIMS 1 AND 11 AND~~ DEPENDENT CLAIMS ~~2-5, 8-9, 12, 14-19~~6 AND 7 ARE OBVIOUS OVER COSTA IN VIEW OF LIU

A. Claim 1:

1. [1.Pre] "A method of forming a joint opening structure in a three-dimensional (3D) memory device, comprising:"

To the extent the preamble is limiting, Costa discloses it. Banerjee ¶ 114.

To start, when '291 Patent uses the term "joint opening structure" it is referring to an opening structure of a three-dimensional (3D) memory device created by "combining two through hole formation processes." Ex. 1001, 15:38-40. That is, it is referring to the well-known technique of forming channel structures in multi- tier memory devices using two etch processes. Banerjee ¶ 115-17.

Costa discloses forming a joint opening structure by etching a first memory through hole in a first stack (and forming a channel structure therein), forming a second stack on the first stack, and etching a second memory through hole in the second stack (and forming a channel structure therein). Costa, [0002] ("multi-tier three-dimensional memory devices"), [0003] ("fabricating a multi-tier memory stack structure" and "providing a reliable connection between vertically neighboring memory stack structures"), Figs. 4A-4G, 10A-11F; Banerjee ¶¶ 118-119.

2. [1.A] "forming a first stacked layer and forming a first insulating connection layer on the first stacked layer;"

As described by the '291 Patent, "the first stacked layer 2 can be formed on the substrate 1 [and] can include a plurality of oxide/nitride layer pairs." Ex. 1001, 9:26-28, Fig. 1. "The first insulating connection layer 3 can be formed on the first stacked layer 2 [and] can be made by [sic] any suitable insulating material and/or dielectric material, such as silicon oxide."– Ex. 1001, 9:61-65, Fig. 1; Banerjee **¶ 121- 22.**

~~**¶¶ 121-22.**~~

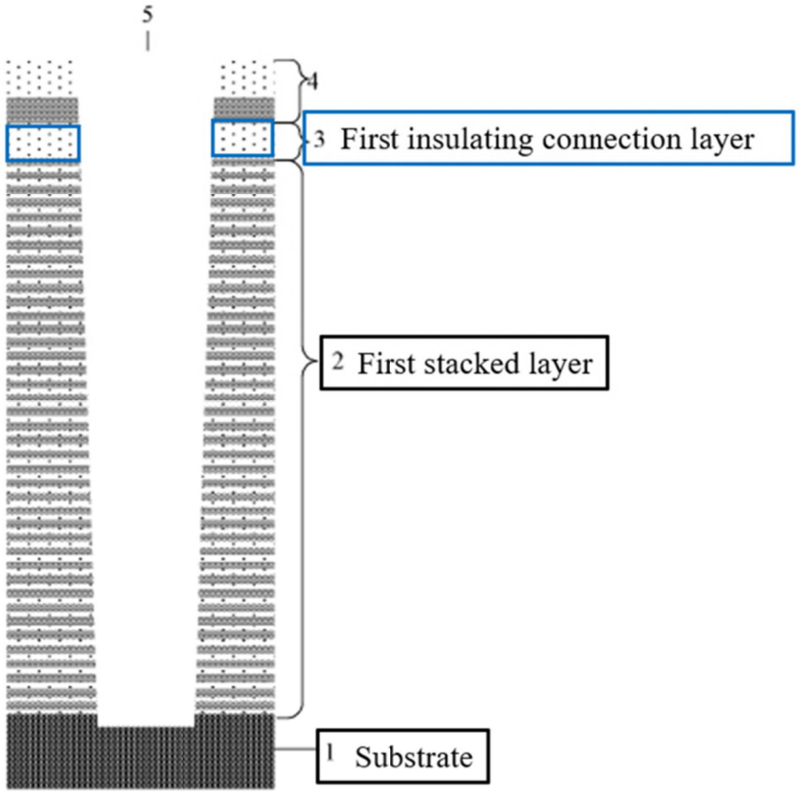
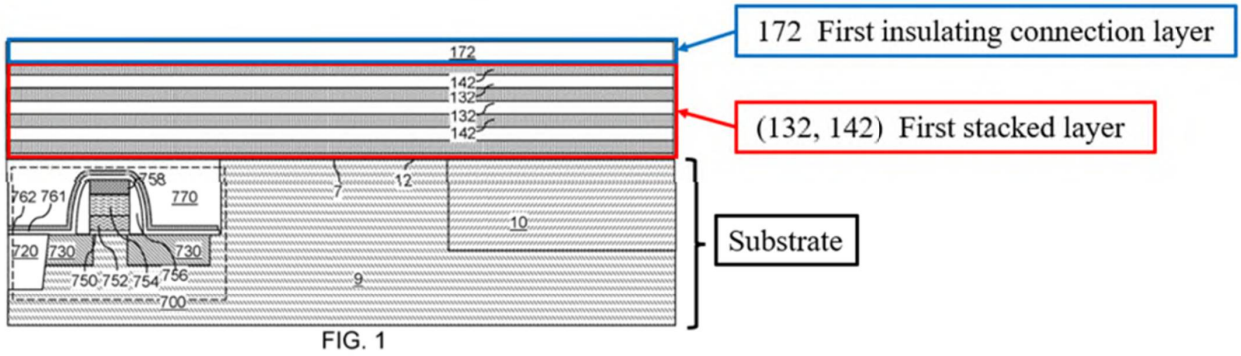


FIG. 1

Id., Fig. 1 (annotated)~~;~~: Banerjee ¶ 123. The '291 Patent apparently uses the term "connection" because "a second stacked layer" is formed "on the first insulating connection layer," that is, this "connection" layer is between the two stacks. ***See*** Banerjee ¶ 124.

Costa discloses the same process, namely, forming a first stacked layer ("first alternating stack" 132, 142) and forming a first insulating connection layer ("first

insulating cap layer 172") on~~3~~6 the first stacked layer. Costa, [0134]. Banerjee ¶ 120, 125.



Id., Fig. 1 (annotated); Banerjee ¶ 125.

Specifically, "[a]n alternating stack of first material layers and second material layers is subsequently formed. Each first material layer [132] can include a first material, and each second material layer [142] can include a second material that is different from the first material." Costa, [0126]; Banerjee ¶ 126. The first material layer 132 can be an insulating material, such as "silicon oxide … [or] dielectric metal oxides … commonly known as high dielectric constant (high-k) dielectric oxides…." *Id.*, [0126], [0129]. The second material layers 142 can be a

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[36] While Costa's insulating layer 172 is directly on the first stacked layer, the '291 Patent defines "on" to include being over, such that "intermediate feature[s]" could be between the layer 172 and the first stacked layer. Ex. 1001, 8:3-8.

"sacrificial material," such as "silicon nitride," that "can be subsequently replaced

with electrically conductive electrodes…." *Id.*, [0129]-[0131]; Banerjee ¶¶ 126-128.

As described by Costa, "first-tier insulating cap layer 172" is deposited on the first alternating stack (132, 142), "collectively constitut[ing] a first tier structure (132, 142, 172)." Costa, [0134][47], Figs. 1, 2B; Banerjee ¶ 129. Furthermore, the first-tier insulating cap layer 172 is comprised of dielectric material such as silicon oxide. Costa, [0134]; Banerjee ¶ 130. The second stacked layer is then formed "on" this "first insulating cap layer 172," i.e., it is a connection layer between the two stacks made of dielectric. Banerjee ¶¶ 124, 131-32; Ex. 1001, 8:3-8 ("on" does not require directly on).

To the extent that PO argues that the "first insulating connection layer" must directly contact the second stack, PO would be incorrect. Claim 1 requires only that the second stack be formed on the "first insulating connection layer." Because the '291 Patent defines "on" broadly to include not directly on, and the claim says "on" instead of "directly on," it would be improper to limit the claim to require the second

[47] Costa at [0134] includes a typographical error, because it refers to the insulating layer being formed on the second stack instead of the first. Costa, [0134], Fig. 2B;

Banerjee ¶ 129.

stack to be directly on and in contact with the "first insulating connection layer." Banerjee ¶¶ 133-137.

3. [1.B] "forming a first through hole that penetrates the first stacked layer and the first insulating connection layer;"

The '291 Patent describes forming the first through hole 5 by overlaying a mask layer 4 on the first insulating connecting layer 3 and performing an etching process to form the first through hole. Ex. 1001, 10:1-5, 10:16-29.

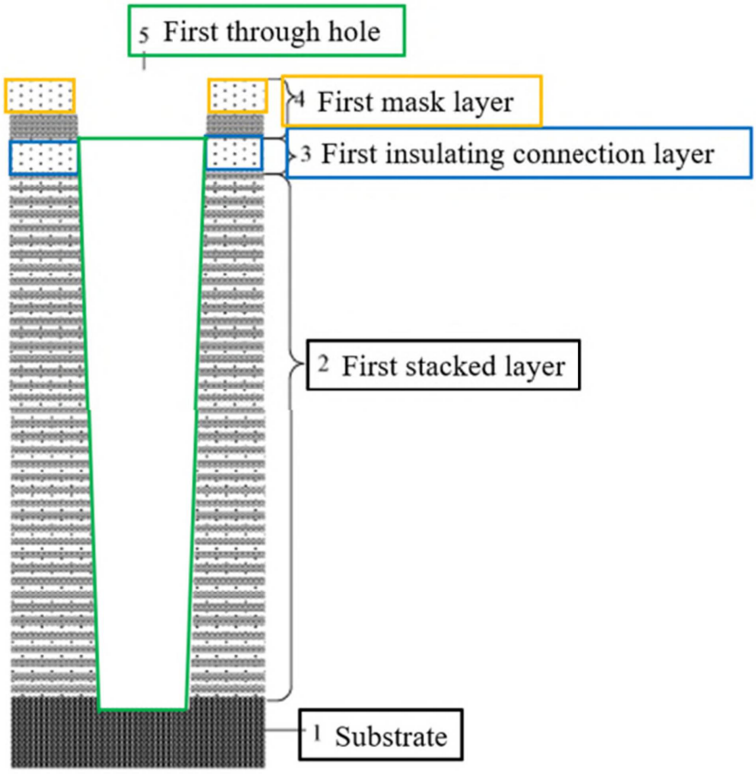


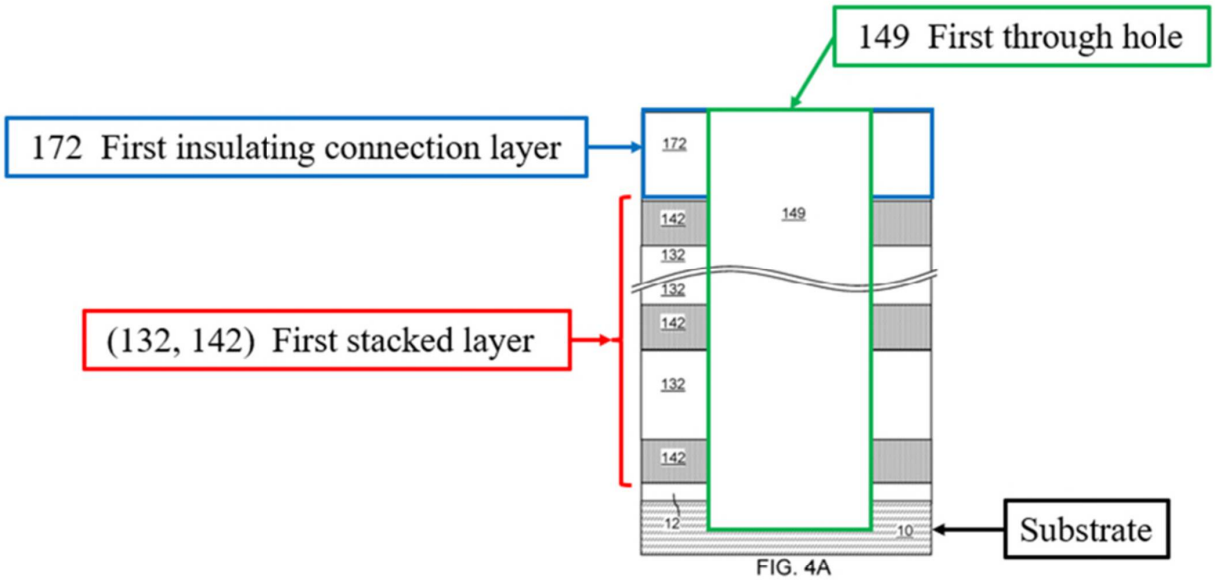
FIG. 1

Id., Fig. 1 (annotated); Banerjee ¶ 139.

As demonstrated below, Costa discloses the same process, namely, forming

a first through hole ("first-tier memory opening[]" 149) that penetrates the first

stacked layer ("first alternating stack" 132, 142) and the first insulating connection layer ("first-tier insulating cap layer 172"); Banerjee ¶¶ 138, 140. Costa discloses that "first-tier openings (149, 119) extending to a top surface of the substrate (9, 10) are formed through the first tier structure (132, 142, 172, 165)." Costa, [0137]; *see also id.* (describing forming first-tier openings by lithographic patterning and etching, i.e., masking); Banerjee ¶ 141. As shown below, first-tier memory opening 149 penetrates the first tier structure (132, 142, 172) exposing substrate 10:



Id., Fig. 4A (annotated); Banerjee ¶ 142; *see also* Costa, Fig. 3B.

4. [1.C] "forming a first channel structure overlaying the surface of the substrate that is exposed by the first through hole;"

The ’291 Patent describes forming the claimed first channel structure by depositing material “on the surface of the substrate 1 that is exposed by the first through hole 5” (i.e. at the bottom of the first through hole). Ex. 1001, 10:30-32,

Fig. 2; Banerjee ¶ 144. ~~As described by the ’291 Patent, “~~“[T]~~t~~he first channel structure

… can be a polycrystalline silicon (polysilicon) layer formed by using a selective epitaxial process.” *Id.* 10:32~~-34~~- 34; Banerjee ¶ 145.

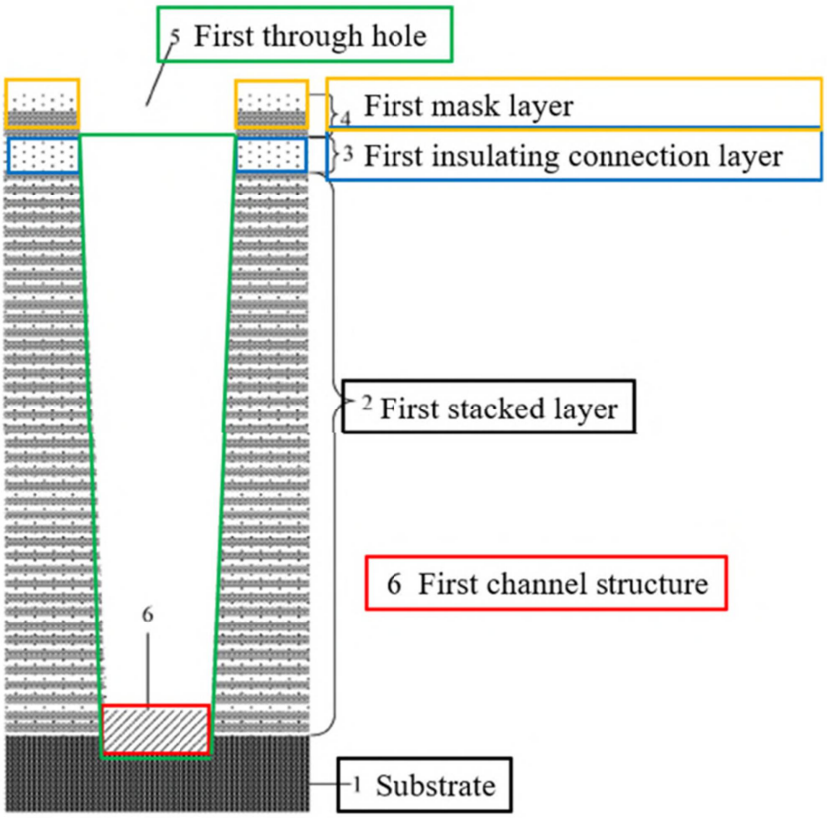


FIG. 2

Id., Fig. 2 (annotated); Banerjee ¶ 146.

Costa discloses the same, namely, forming a first channel structure

("epitaxial channel portion 11") overlaying the surface of the substrate ("substrate 10") that is exposed by the first through hole ("first-tier memory opening" 149). Costa, [0143] ("[E]pitaxial channel portion (*e.g.*, an epitaxial pedestal) 11 can be formed at the bottom portion of each first-tier memory opening 149…."); Banerjee ¶¶ 143, 147-

48; *see also* Costa, [0137] ("substrate" includes portions 9 and 10). Epitaxial channel portion 11 overlays the surface of the substrate 10 that is exposed by the first-tier memory opening 149:

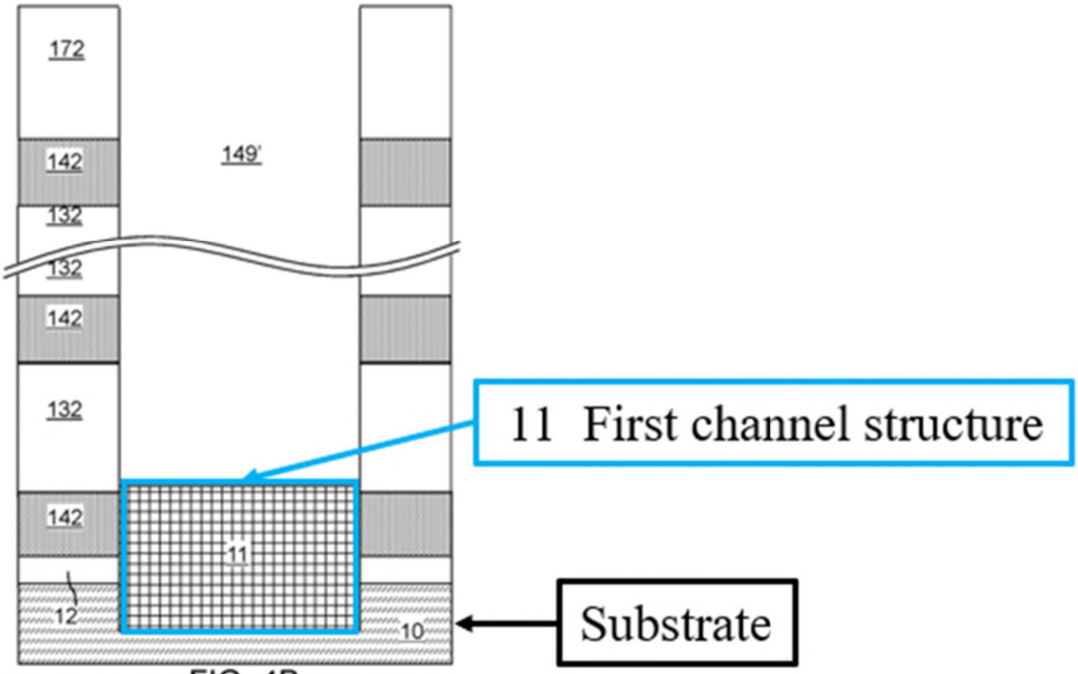


FIG. 4B

Id., Fig. 4B (annotated); *see also* Banerjee ¶¶ 148-150.

5. [1.D] "forming a first functional layer on the sidewall of the first through hole;"

As an initial matter, the '291 Patent uses "functional layer" to refer to a

layer that performs a function, and in the context of the embodiments, that function is a data storage function. Ex. 1001, 10:40-43 (functional layer including data storage layer and oxide layers to inject charge thereon); Banerjee ¶ 152. The '291 provides the ~~following~~**an** example~~:~~ **of the** "first functional layer~~ can be formed on the sidewall of the first through hole 5 [and] can include a first tunneling layer 7, a first storage layer 8,~~

" having multiple layers~~a first barrier layer 9, and a first passivation layer 10."~~**.** Ex. 1001, 10:40-43, Fig. 3; *see also id.*, 8:34-51 ("A layer can include multiple layers.")~~. Portions of these layers "located on the top surface of the first channel structure 6 and the bottom of the first through hole 5 can be removed" (*i.e.*, leaving only the portions on the sidewall of first through hole 5). *Id.*, 11:3-24, Fig. 4.~~

~~–~~Dependent claim 4 separately requires that "functional layer" includes each of these exemplary layers~~ (and Costa includes each of these layers, *see infra*)~~, and thus "functional layer" more broadly simply means a layer that functions, e.g., to store data (but regardless, **Costa** includes each of these four layers~~, *see infra*~~); Banerjee ¶¶ 153-55.

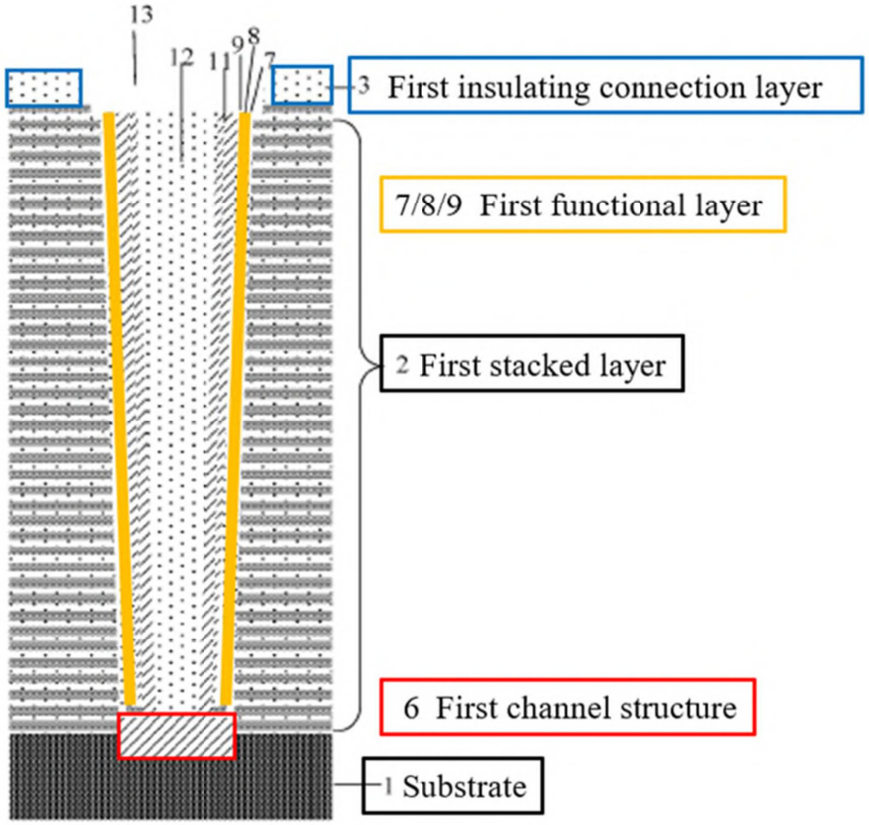


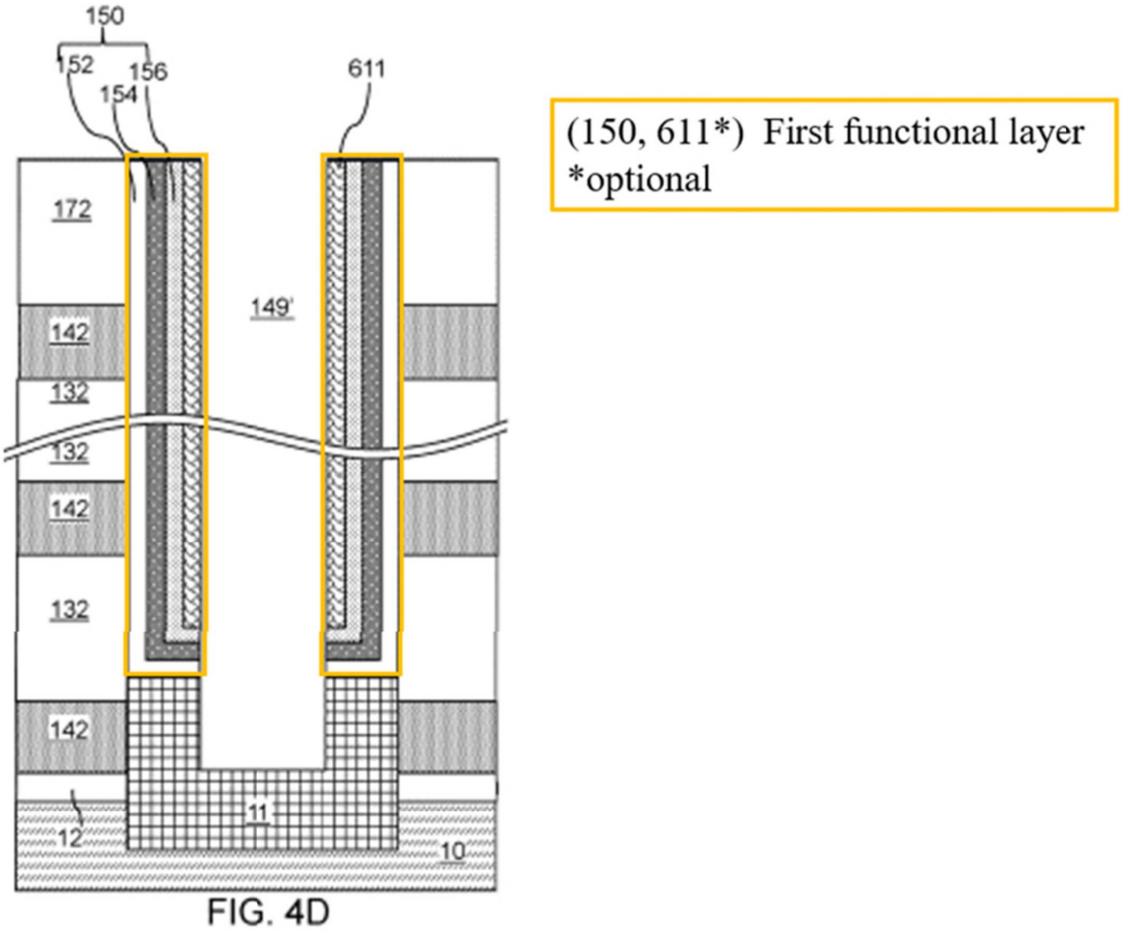
FIG. 10B

Id., Fig. 10B (annotated); Banerjee ¶ 155.

As demonstrated below, Costa discloses the same, namely, forming a first functional layer ("first memory film 150" with or without the optional semiconductor channel layer 611) on the sidewall of the first through hole ("first-tier memory opening 149"); Banerjee ¶¶ 151, 156. Specifically, Costa's first

memory film 150 comprises "a stack of layers including a first blocking dielectric layer 152, a first charge storage layer 154, a first tunneling dielectric layer 156…." Costa, [0144], Figs. 4D-E; Banerjee ¶ 157. This "stack of layers"

consisting of memory film 150 is deposited in the first-tier memory opening 149 and subsequently etched to remove the portions above first-tier insulating cap layer 172 and at the bottom of first-tier memory opening 149, as shown in Figures 4C and 4D below. *Id.*, [0144], [0153]; Banerjee ¶¶ 158. Note that outer semiconductor channel layer 611 is an optional layer. *Id.*; Banerjee ¶ 159



Costa, Fig. 4D (annotated); Banerjee ¶ 159.

6. [1.E] "forming a second channel structure and forming a first filling structure on the sidewall of the first functional layer and the exposed surface of the first channel structure;"

The '291 Patent describes "sequentially form[ing a second channel structure and a first filling structure] on the sidewall of the first functional layer and the exposed surface of the first channel structure 6." Ex. 1001, 11:25-44; Banerjee

¶ 161; *see also* Ex. 1001, Figs. 5-6, 11:45-12:23, Figs. 7A-8B~~. The second channel~~**, 19:40-43, 19:46-48;**
~~**structure can be comprised of amorphous silicon and the first filling layer can be an oxide layer. Ex. 1001, 19:40-43, 19:46-48; Banerjee ¶¶ 162-63.**~~

Banerjee ¶ 162. Put simply, the channel structure is, e.g., the semiconductive layer of the channel structure, and the filling structure is, e.g., the core of the channel structure. Banerjee ¶ 163.

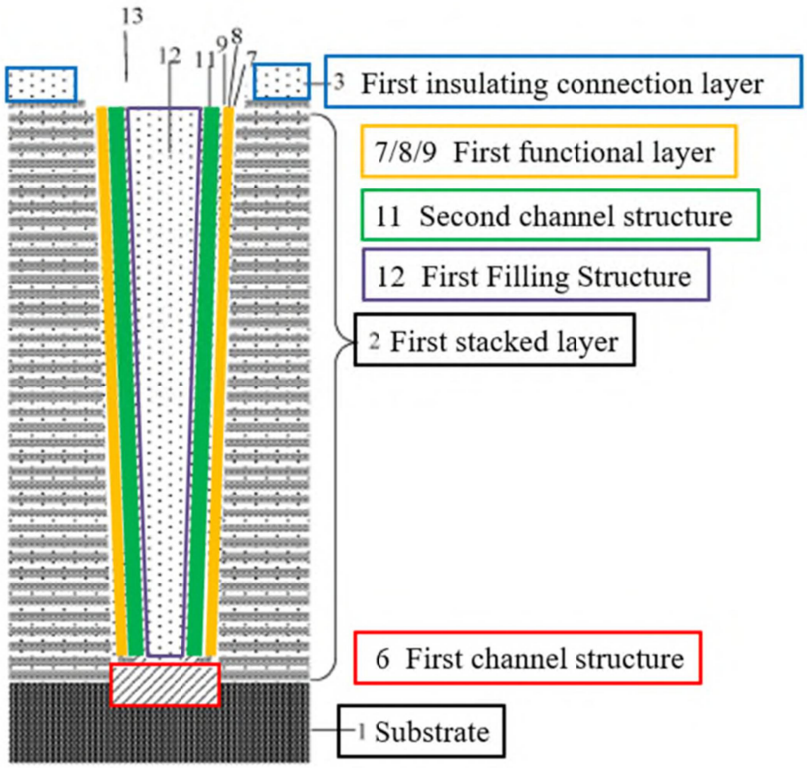


FIG. 10B

Ex. 1001, Fig. 10B (annotated); Banerjee ¶ 164.

As demonstrated below, Costa discloses the same, namely, forming a second channel structure ("first inner semiconductor channel layer 612") and forming a first filling structure ("dielectric core 162") on the sidewall of the first functional layer ("stack of layers" 152, 154, 156, 611) and the exposed surface of the first channel structure ("epitaxial channel portion 11"). Banerjee ¶¶ 160, 165. The "outer semiconductor channel layer 611," shown below, is optional. Costa, [0144]. Banerjee ¶ 166.

As to the "second channel structure," Costa discloses: "a first inner semiconductor channel layer 612 can be deposited directly on the semiconductor

surface of the epitaxial channel portion 11 … and directly on the [optional] first outer semiconductor channel layer 611." Costa, [0156]. The 611 and 612 layers are "amorphous silicon or polysilicon." *Id.*, [0152], [0156]. "The materials of the first outer semiconductor channel layer 611 and the first inner semiconductor channel layer 612 are collectively referred to as a first semiconductor channel material." *Id.*, [0157]; Banerjee ¶ 166.

As to the "filling structure," Costa discloses not completely filling the cavity with semiconductor channel material. Costa, [0158], Fig. 4E. In such cases, Costa discloses forming a "dielectric core layer 162L." *Id.*, [0158], Fig. 4F; *see also id.*, [0159], Fig. 4G (removing portion of "first dielectric core layer 162L" that is "above

the top surface of the first-tier insulating cap layer 172" and leaving "dielectric core 162" within the memory cavity 149'); Banerjee ¶ 167.

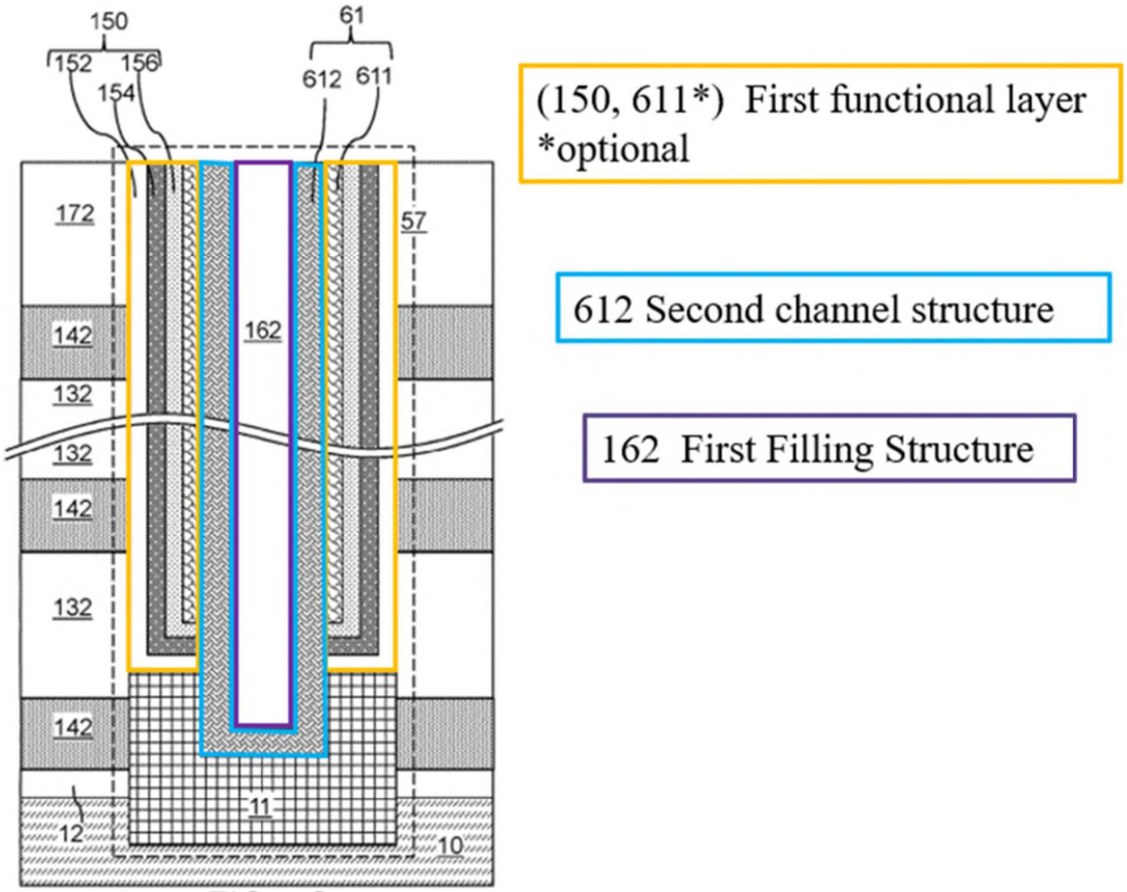


FIG. 4G

Costa, Fig. 4G (annotated); Banerjee ¶¶ 168-69.

To the extent that PO attempts to argue that Costa does not disclose this limitation because Costa's filling structure is not "on" the "exposed surface of this first channel structure," PO would be incorrect for three reasons. Banerjee ¶ 170.

First, even if the "filling structure" must be "on" "the exposed surface of the first channel structure," Costa discloses this, because the '291 Patent does not limit

–"on" to "directly contacting" (*i.e.*, there can be intervening layers). Ex. 1001, 8:3-8; Banerjee ¶ 171.

Second, the claim phrase "on the sidewall of the first functional layer and the exposed surface of the first channel structure" does not modify "a first filling structure," even though this phrase appears immediately after "a first filling structure," because "a first filling structure," as described by the '291 Patent, is not on the sidewall of the first functional layer but rather on the second channel structure (see above). Nor would a POSITA understand the claim to require specifically that the "second channel structure" be formed "on the sidewall of the first functional layer" and that "a filling structure" be formed on "the exposed surface of the first channel structure," because the claim does not use the term "respectively" to differentiate these positional relationships. Instead, the claims require that the two structures collectively ("second channel structure" and "filling structure") in some way contact the "sidewalls" and "exposed surface of the first channel structure." Banerjee ¶ 172-73.

Third, this limitation parallels limitation [1.J]. As seen there, while the limitation recites "forming a fourth channel structure and forming a second filling structure on the sidewall of the second functional layer and the exposed surface of the third channel structure," the '291 Patent does not depict the filling structure directly on "the exposed surface of the third channel structure." *See* Banerjee ¶ 174.

7. [1.F] "forming a third channel structure in contact with the second channel structure above the first through hole, wherein a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate;"

~~**The '291 Patent describes forming the claimed third channel structure by first removing a "[a] portion of the first insulating connection layer 3 … to form the first groove [13] that penetrates the first insulating connection layer 3." Ex. 1001, 12:35-**~~

~~**40.**~~**The '291 Patent describes forming** "~~**[**~~a~~**]**~~ third channel structure 14~~ **can be formed in the first groove 13**~~" that "can be a polycrystalline silicon []layer formed by using a deposition process." *Id.*, 12:59-

~~**64. "A projection of the first groove [13] on the substrate completely covers a projection of the first through hole on the substrate" or, in other embodiments, "[a]n area of the projection 'x' of the first groove on the substrate 1 can be larger than an area of the projection 'y' of the first through hole 5 on the substrate 1." *Id.*, 16:5-7, 12:38-40. The '291 Patent further describes that, "[i]n some embodiments … a portion of the third channel structure 14 that is adjacent with the bottom nitride layer of the second stacked layer 15, or is adjacent with the top nitride layer of the first stacked layer 2 can be converted to an oxide layer by an oxidation process." *Id.*, 16:65-17:2; Banerjee ¶¶ 176-77. The third channel**~~

~~structure 14 is illustrated in Figure 11B below:~~

64. The third channel structure 14 is illustrated in Figure 11B below:

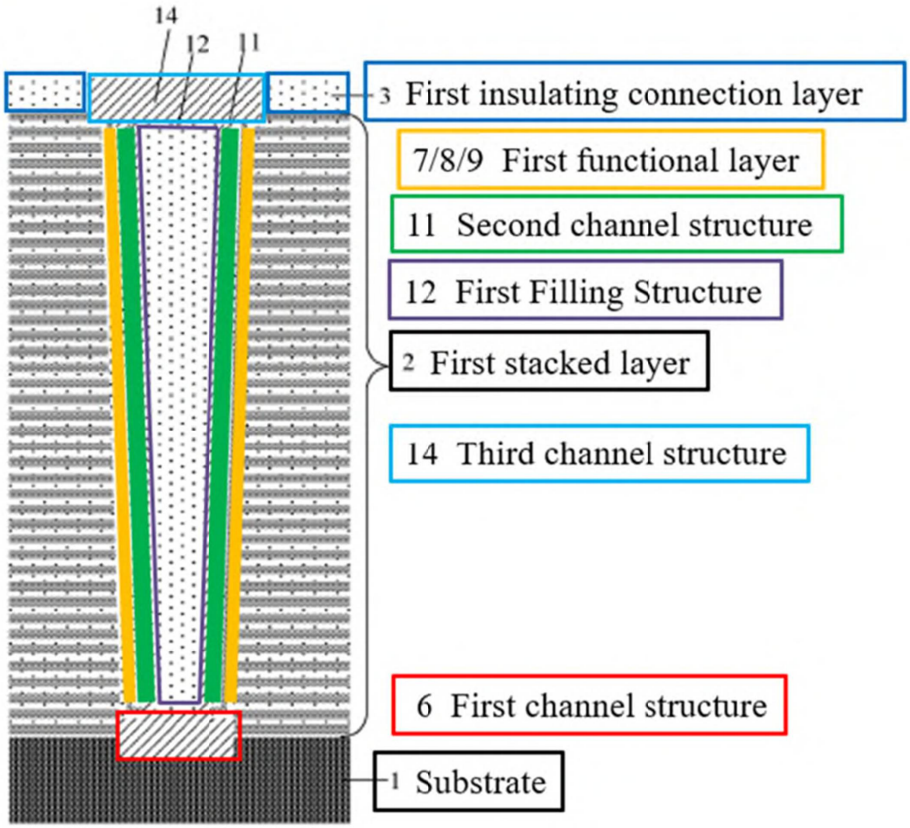


FIG. 11B

Id., Fig. 11B (annotated); Banerjee ¶ 178.

Costa discloses, or at least renders obvious in view of the knowledge of a POSITA, the same, namely, as demonstrated below, forming a third channel –structure ("joint-level doped semiconductor portion 173") in contact with the second channel structure ("first inner semiconductor channel layer 612") above the first through hole ("first-tier memory opening 149"), wherein a projection of the third channel structure ("joint-level doped semiconductor portion 173") on the

substrate covers a projection of the first through hole ("first-tier memory opening 149") on the substrate. Banerjee ¶¶ 175, 179-80.

Costa's "third exemplary structure" is derived from the "first exemplary structure" (this Ground maps the first exemplary structure to the claim limitations up to this point) by modifying the interface between the two tiers. Costa, [0263]. The rest of the claim mapping follows using the "third exemplary structure" embodiment. Here, Costa discloses depositing "joint-level doped semiconductor layer 173L" over the first tier structure (i.e., over first insulating cap layer 172). *Id.*, [0265], Fig. 20A. Lithographic patterning and subsequent etching are performed, leaving joint-level doped semiconductor portion 173 that "covers and protects the underlying first vertical semiconductor channel 61 from oxidation during a subsequent oxidation process." *Id.*, [0265], Figs. 20A-B. "In one embodiment, the bottom surface of each joint-level doped semiconductor portion 173 can contact an entire top surface of an underlying first memory opening fill structure 57." *Id.*, [0265]. As illustrated in Figures 20B and 20C below, Costa's joint-level doped semiconductor portion 173 covers the entire first-tier memory opening 149 (i.e., a

projection of 173 on the substrate covers a projection of 149 on the substrate) and is in contact with the second channel structure. Banerjee ¶¶ 181-86.

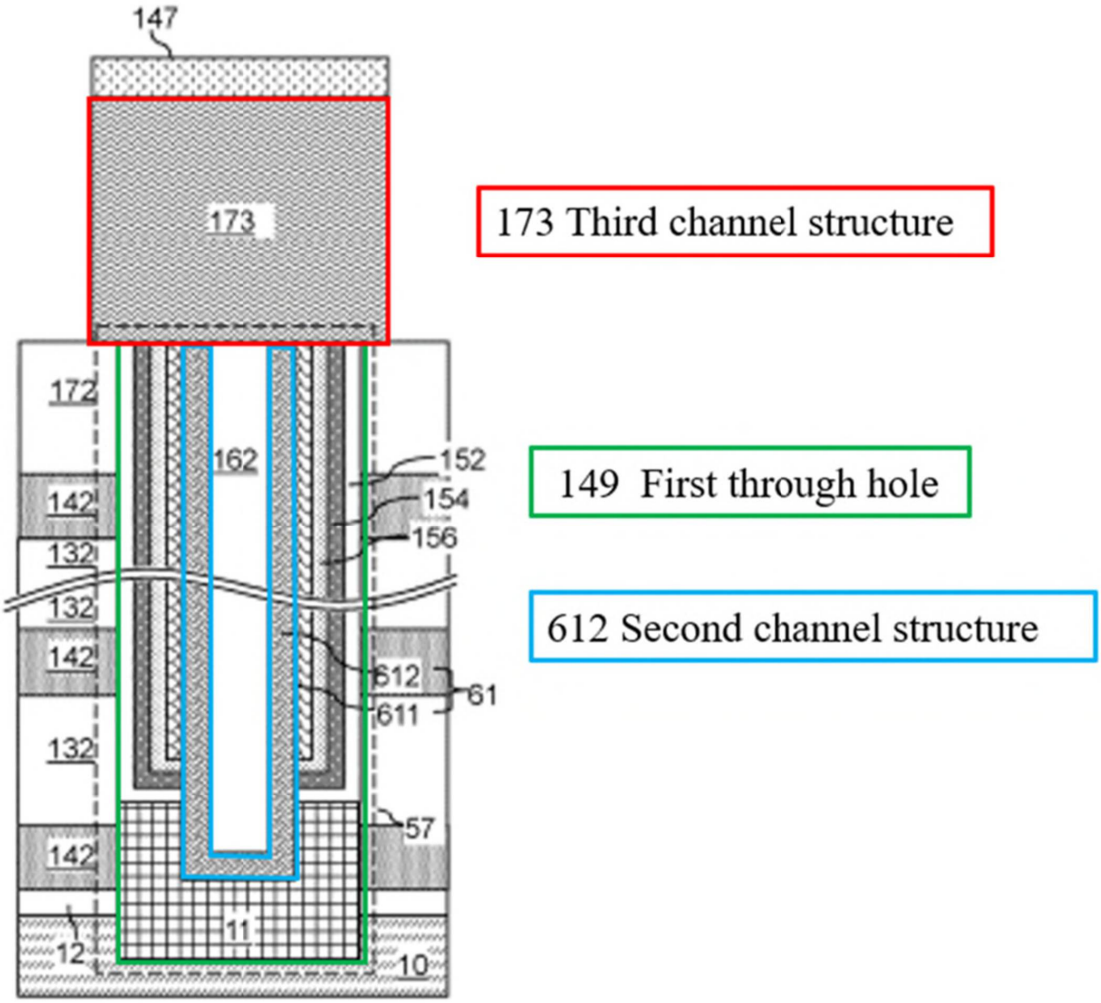
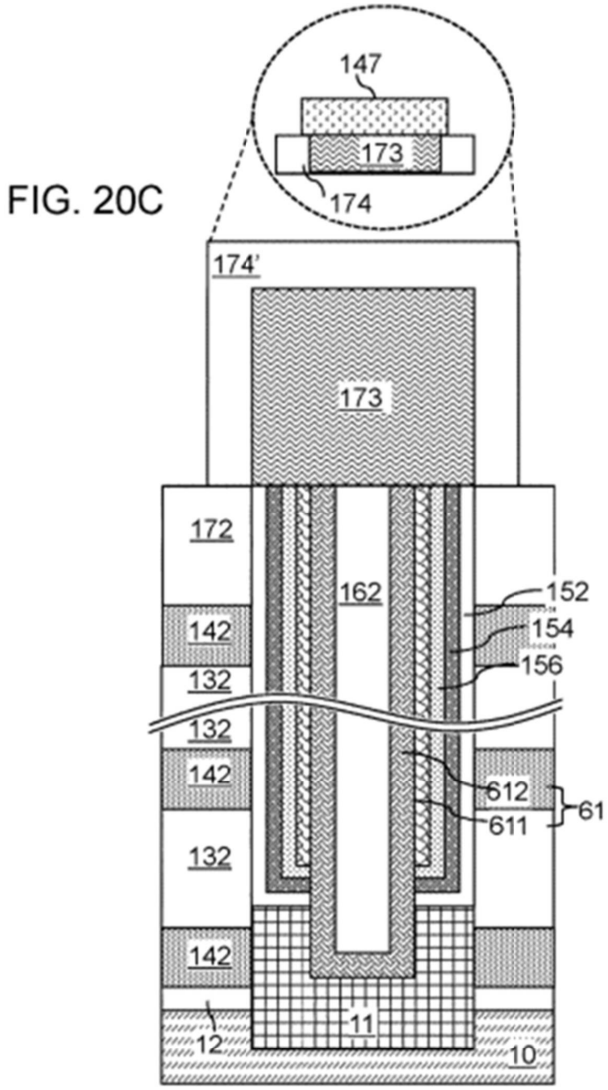


FIG. 20B

Id., Fig. 20B (annotated); Banerjee ¶ 186. Costa's description confirms the third channel structure 173 will fully cover (indeed, be wider than) the fill structure 57 (first hole), because Costa discloses that the mask to preserve the final structure 173 will "cover each of the first memory opening fill structures 57." Costa, [0265]; Banerjee ¶ 187. Indeed, Costa also discloses: "In one embodiment, the bottom

surface of each joint-level doped semiconductor portion 173 can contact an entire

top surface of an underlying first memory opening fill structure 57." Costa, [0265]. Costa describes an embodiment that further includes an oxidation step. Costa, [0266]; Banerjee ¶ 188. Even in this embodiment, after oxidizing the exposed surfaces of semiconductor portion 173, Figure 20C shows that the remaining portion of doped semiconductor portion 173 (i.e., the portion not oxidized) has an aperture at least the same size as that of fill structure 57 (i.e., the structures filling first-tier memory opening 149). Costa, [0266], Fig. 20C; Banerjee ¶ 189.



Id., Fig. 20C; Banerjee ¶ 189.

To the extent PO argues that Costa fails to disclose this limitation because the above Figure 20C shows joint-level doped semiconductor portion 173 (i.e. the portion not oxidized) having the same size as that of fill structure 57 (i.e., the diameter of "the first through hole"), PO would be incorrect. Banerjee ¶ 190.

First, the oxidation step is only in one embodiment in Costa, not all

embodiments. Costa, [0266]; Banerjee ¶ 191. Second, a POSITA would have understood that Costa's joint-level doped semiconductor portion 173 (as disclosed in Figure 20C) would have a projection on the substrate that "covers" a projection of the fill structure 57, i.e., the first hole, given the '291 Patent's use of "cover." The '291 Patent's specification uses the term "completely cover," while Claim 1 simply recites "cover." *E.g.*, Ex. 1001, 20:33-38 ("In some embodiments, the projection of the first groove on the substrate 201 can completely cover the projection of the corresponding first through hole 205 on the substrate 201."); *see also* Banerjee

¶ 192. Thus, a POSITA would not read "cover" to mean "completely cover," e.g., cover the entirety of the underlying object. Banerjee ¶ 193. Indeed, the plain meaning of "cover" includes where the "covering" object is the same size as the object being "covered." In other words, the "covering" object need not be larger than another object to "cover" it. For example, if two quarters were stacked one atop the other, one would describe the top quarter as covering the bottom quarter. Banerjee ¶ 194. As clearly demonstrated in Figure 20C, joint-level doped

semiconductor portion 173 is at least the same size as fill structure 57 (the first hole). Costa, Fig. 20C. Thus, a projection of semiconductor portion 173 (even in the post- oxidation embodiment) "cover[s]" a projection of first-tier memory

opening 149 on the substrate. *Id.*; Banerjee ¶ 195.

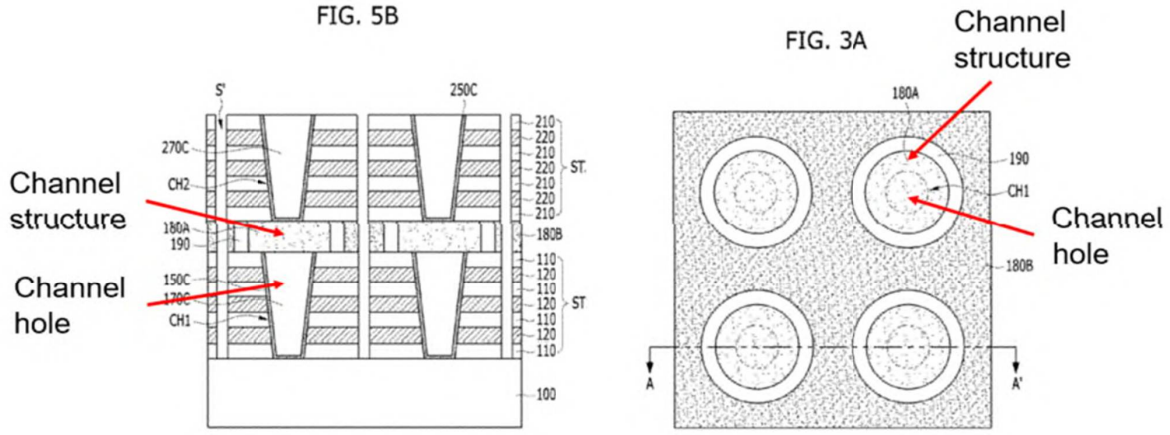
Regardless, a POSITA would have found it obvious to ensure that Costa's joint-level doped semiconductor portion 173 is wider than the first hole (more than covers a projection of first-tier memory opening 149 on the substrate). For example, Costa teaches that one purpose of doped semiconductor portion 173 is to "protect[] the underlying first vertical semiconductor channel 61 from oxidation during a subsequent oxidation process." Costa, [0265]. To serve this purpose, Costa discloses forming portion 173 to "contact an entire top surface of an underlying first memory opening fill structure 57." *Id.* This purpose alone would have motivated a POSITA to ensure that doped semiconductor portion 173 does more than completely cover the underlying fill structure 57 to ensure it accomplishes the protection function, particularly given process variations during fabrication. *Id.*, [0266]; Banerjee ¶ 196-200.

Moreover, Costa describes a non self-aligned process that would produce some degree of misalignment between, e.g., the target placement of the third channel structure and actual placement of the third channel structure (and more generally, the first and second memory holes) due to process variations during fabrication.

Banerjee ¶ 201; Ex. 1021, 2:60-3:6 (noting process variation issues in non self- aligned processes); Ex. 1022, 20-21. And a POSITA would have understood

and found it obvious to ensure alignment (i.e., electrical contact between upper and lower deck memory channels) by including a third channel structure with a larger diameter

–than the underlying memory hole. Banerjee ¶ 202; *see also, e.g.*, Ex. 1023, [0023] ("The lateral extension portion (135) may have a larger cross-sectional area than the first and second semiconductor pillars (130a, 130b) based on a cross section parallel to the substrate (105)."), [0086] ("[B]y arranging the lateral extension portion (135) between the first semiconductor pillar (130a) and the second semiconductor pillar (130b), the alignment margin is increased when the second through holes (120b) are formed…."); Liu, [0058] ("[M]emory opening alignment challenges may be reduced or avoided by adding a landing pad between the memory stack portions [that is] is wider (e.g., had a larger diameter) than the channel in the horizontal direction."). Indeed, in this specific context of an interface between channel holes, it was known to address these alignment and process issues by making the interface wider than the channel hole:



Ex. 1024, Fig. 5B (annotated), 3A (annotated), [0061] (~~"[C]hannel connection pattern 180A may have an island shape which overlaps the first channel holes CH1 …~~ [T]o secure an overlap margin between the channel connection pattern 180A and the first channel hole CH1,

~~-~~the channel connection pattern 180A may have a larger width than the top surface of the first channel hole CH1."); Banerjee ¶ 203. In simple terms, the conventional fabrication approach would include a margin such that the portion 173 is wider than fill structure 57 to account for process variations and ensure alignment, thereby beneficially increasing yield. Banerjee ¶ 203.

Furthermore, to the extent PO argues that Costa fails to meet this limitation because Costa's joint-level doped semiconductor portion 173 is not formed in a groove of the first insulating cap layer 172, PO would be incorrect. First, the claim

includes no such requirement. Second, such a requirement would render Claim 6 superfluous. Banerjee ¶¶ 204-05; ***see also infra*, §XI.B**.

8. **[1.G] "forming a second stacked layer and forming a second insulating connection layer on the first insulating connection layer;"**

As described by the '291 Patent, "a second stacked layer 15 and a second insulating connection layer 16 can be sequentially formed on the third channel structure 14…. [T]he second stacked layer 15 can include a plurality of

oxide/nitride layer pairs, such as silicon oxide layer and silicon nitride layer pairs." Ex. 1001, 13:11-16, Fig. 12, 13:16-21.

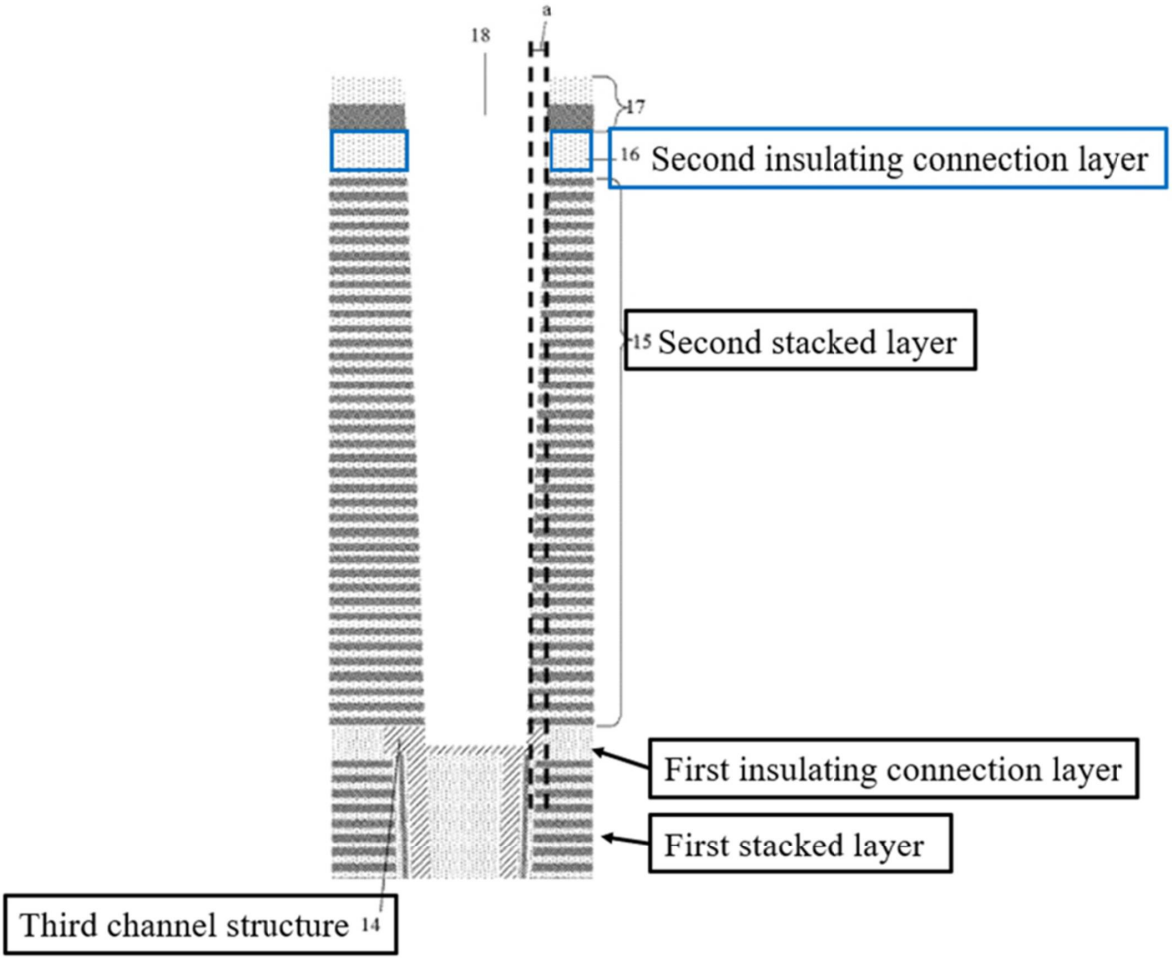


FIG. 13

Id., Fig. 13 (annotated); Banerjee ¶ 207.

Costa discloses the same, namely, forming a second stacked layer ("second alternating stack" 232, 242) and forming a second insulating connection layer ("insulating cap layer 70") on the first insulating connection layer ("first insulating cap layer 172"); Banerjee ¶¶ 206, 208. As shown in Figure 21A below, "second alternating stack (232, 242) of material layers is subsequently formed on the top surface of the joint-level material layers…." Costa, [0178] (describing the process of Figs. 8A-B), [0270] (referring to "the processing steps of" Figs. 7A-10B

using the

third exemplary structure's single joint-level doped semiconductor portion 173), [0263], Figs. 8A-B, Fig. 21A; Banerjee ¶ 209. "An insulating cap layer 70 can be subsequently formed over the second alternating stack (232, 242)." Costa, [0183]; Banerjee ¶ 210. Thus, second alternating stack (232, 242) and insulating cap layer 70 are formed "on" first-tier insulating cap layer 172. Banerjee ¶ 211; Ex. 1001, 8:3-8 ("on" does not require directly on).

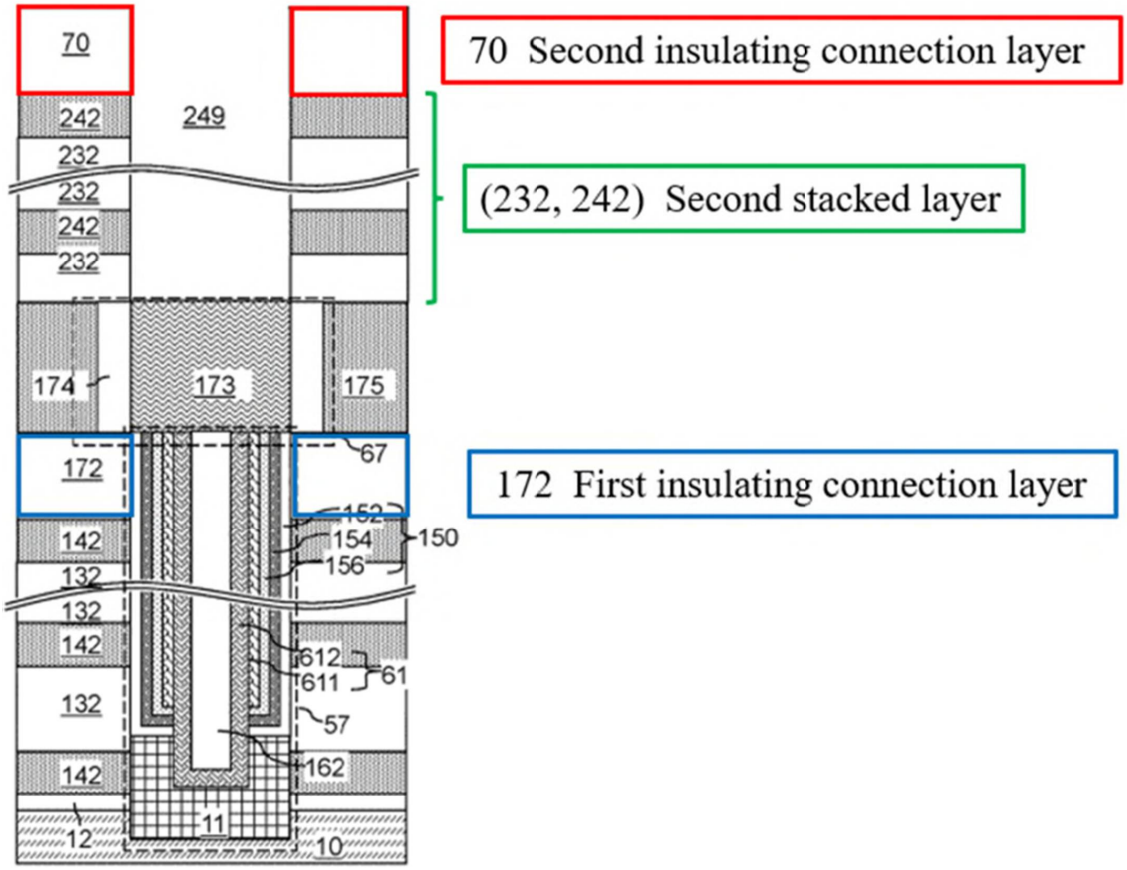


FIG. 21A

Costa, Fig. 21A (annotated); Banerjee ¶ 211. Note that like the '291 Patent, Costa's connection layer 70 is between the second tier and the overlying layers

(e.g., for

interconnects). *Compare* Ex. 1001, Fig. 22A-B (layer at top of second tier) *with* Costa, Fig. 22A-B (same); *see also* Banerjee ¶ 212.

9. [1.H] "forming a second through hole that penetrates the second stacked layer and the second insulating connection layer, wherein a projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate;"

The '291 Patent describes the second through hole similarly to the first through hole: "[A] second through hole 18 is formed [that] can completely penetrate the second stacked layer 15 and the second insulating connection layer 16, and can extend into the surface of the third channel structure 14." Ex. 1001, 13:38-42. Further, "[t]he projection of the second through hole 18 on the substrate 1 can at least partially overlap with the projection of the first through hole 5 on the substrate

1." *Id.*, 13:42-45; Banerjee ¶ 214.

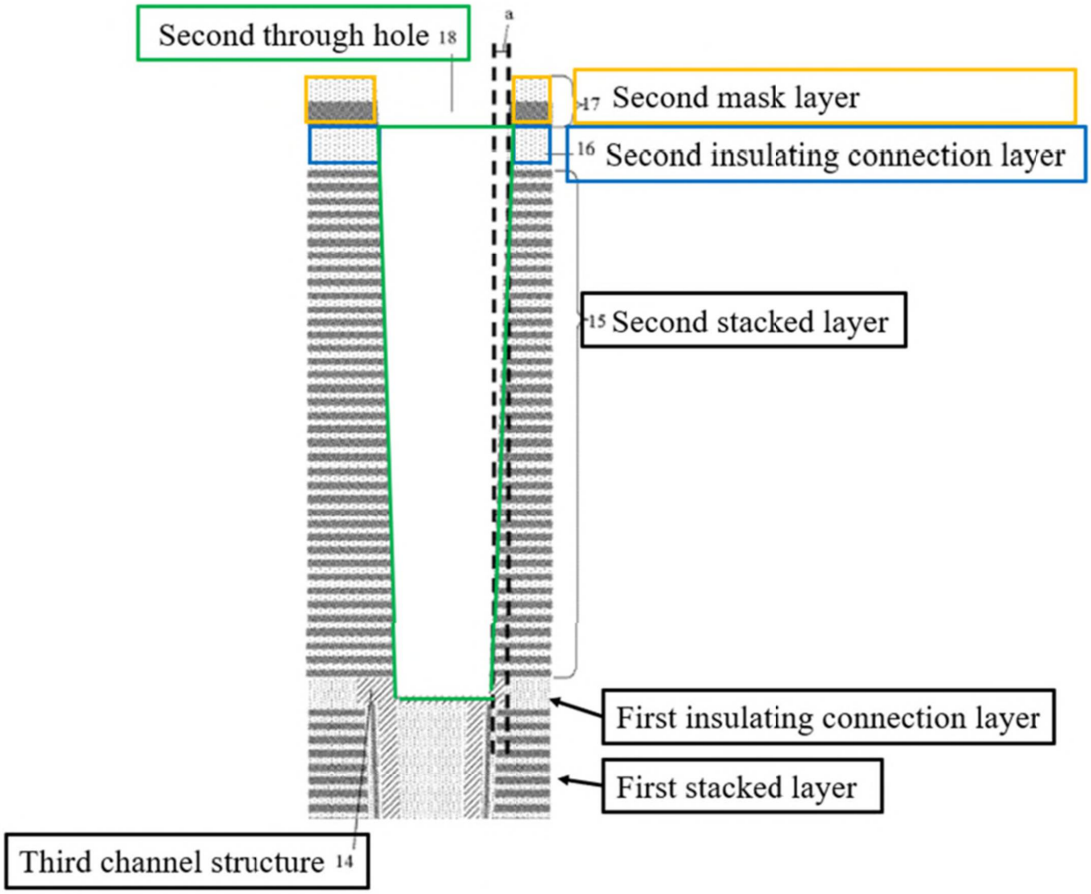


FIG. 13

Id., Fig. 13 (annotated); Banerjee ¶ 215.

Costa discloses, or at least renders obvious in light of the knowledge of a POSITA, the same, namely, forming a second through hole ("second-tier memory opening 249") that penetrates the second stacked layer ("second alternating stack" 232, 242) and the second insulating connection layer ("insulating cap layer 70"), wherein a projection of the second through hole ("second-tier memory opening 249") on the substrate ("substrate 10") at least partially overlaps with the projection of the first through hole ("first-tier memory opening 149") on the substrate. Banerjee

¶¶ 213, 216.

Specifically, after forming the second alternating stack (232, 242), Costa teaches that "second-tier [memory] openings" 249 "are formed through the second tier structure (232, 242, 265, 70)." Costa, [0190], [0192] ("second-tier openings (249, 219) can be formed by a combination of lithographic patterning and an anisotropic etch"); Banerjee ¶ 217. As shown in Figure 21A below, second-tier memory opening 249 penetrates the second stacked layer (second alternating stack (232, 242)) and the second insulating connecting layer (insulating cap layer 70):

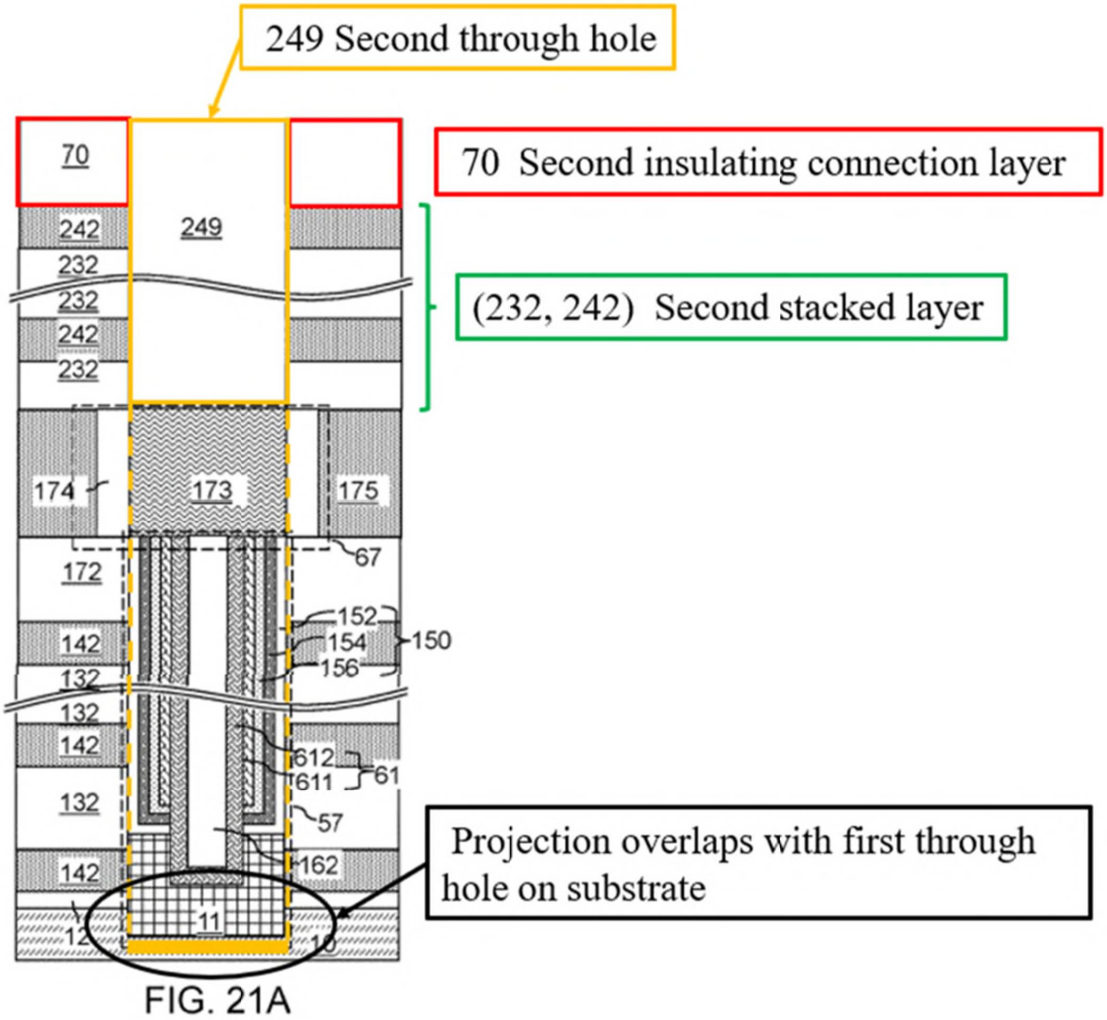


FIG. 21A

Id., Fig. 21A (annotated); Banerjee ¶ 218.

Costa explains that "second-tier memory openings 249 are formed through the second tier structure … in areas that overlap with the joint-level memory opening fill structures 67…." Costa, [0191], Fig. 21A; Banerjee ¶ 219. Thus, Costa teaches that a projection of the second through hole (second-tier memory opening 249) on the substrate overlaps—completely or partially—with a projection of the first through hole (first-tier memory opening 149) on the substrate. *Id.*, [0190] ("~~**Each adjoining combination of a first-tier memory opening 149, a joint-level memory opening, and a second-tier memory opening 249 collectively constitutes a memory opening, or an inter-tier memory opening.**~~**joint- level memory opening**"), [0191] ("[E]ach second-tier memory opening 249 can be formed on top of a respective joint-level memory opening fill structure 67. In one embodiment, the bottom surface of each second-tier memory opening 249 … can have an areal overlap with the top surface of the underlying joint-level memory opening fill structure 67."), Fig. 21A; Banerjee ¶ 220.

As can be seen in Costa's figures, e.g., figure 21A above, Costa attempts to perfectly align the channel structures. Banerjee ¶ 221. A POSITA would have found it obvious that the normal fabrication would largely align the channel structures, such that the holes almost completely overlap (as Costa depicts and describes), as Costa's goal is to perfectly align the structures. Costa, [0191], Fig.

21A; Banerjee

¶ 222.

10. [1.I] "forming a second functional layer on the sidewall of the second through hole;"

As described in the '291 Patent, the "second functional layer can be formed on the sidewall of second through hole 18." Ex. 1001, 14:1-2, Figs. 14-15; Banerjee

¶ 224. The '291 Patent describes the "second functional layer" in the same way as the first functional layer, except it is in the second through hole. *Id.*, 14:3-5.

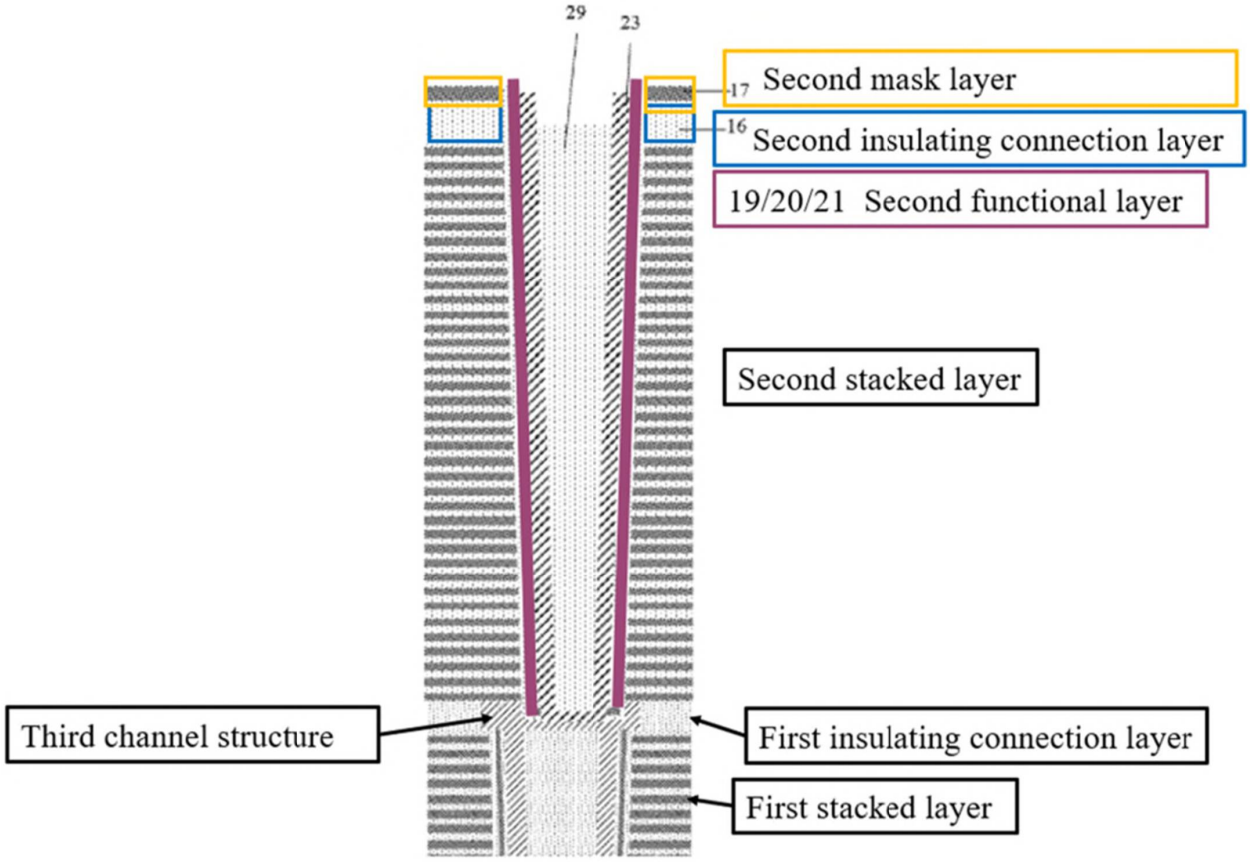


FIG. 19

Id., Fig. 19 (annotated); Banerjee ¶ 225.

Costa discloses forming a second functional layer ("second memory film 250" with or without optional "second outer semiconductor channel layer 621") on the

sidewall of the second through hole ("second-tier memory opening 249"). Banerjee

¶ 223, 226. Costa, [0273]. Costa's second memory film 250 comprises "a stack of layers including a second blocking dielectric layer 252, a second charge storage layer 254, a second tunneling dielectric layer 256…." Costa, [0273], Figs. 21B-C; Banerjee ¶ 227. An "optional second outer semiconductor channel layer 621" can also be "deposited into the second-tier memory opening[] 249." Costa, [0273; Banerjee ¶ 228]. This "stack of layers" is deposited in the second-tier memory opening 249 and subsequently etched to remove the portions above second-tier insulating cap layer 70 and at the bottom of second-tier memory opening 249, as shown in Figures 21B and 21C below. Costa, [0273]-[0274]; Banerjee ¶ 229.

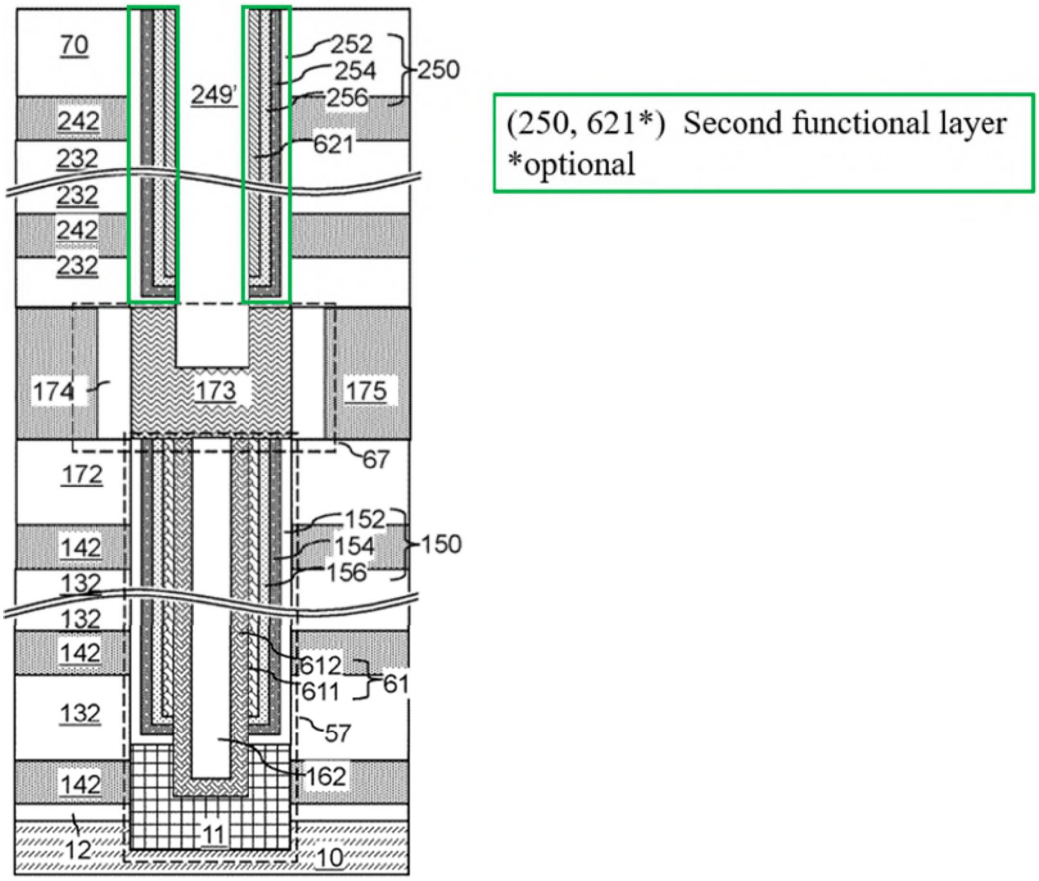


FIG. 21C

Id., Figs. 21C (annotated); Banerjee ¶ 229. For the same reasons that Costa's first functional layer is a functional layer, its second functional layer is a functional layer,

-namely, it performs a function, e.g., a data storage function. Banerjee ¶ 230; *see* §X.A.5.

11. [1.J] "forming a fourth channel structure and forming a second filling structure on the sidewall of the second functional layer and the exposed surface of the third channel structure; and"

The '291 Patent describes "a fourth channel structure and a second filling

structure~~ can be sequentially formed on the sidewall of~~" (like the second ~~functional layer and the exposed surface of the third~~ channel structure~~" as shown in Figure 19 below~~ and first filling structure). Ex. 1001, 14:44-47, 14:56-58, 14:61-63, Figs. 16-19; Banerjee ¶ 232.~~ As described by the '291 Patent, the fourth channel structure can be composed of amorphous silicon and the second filling structure can be an oxide layer. *Id.*, 14:56-58, 14:61-63.~~

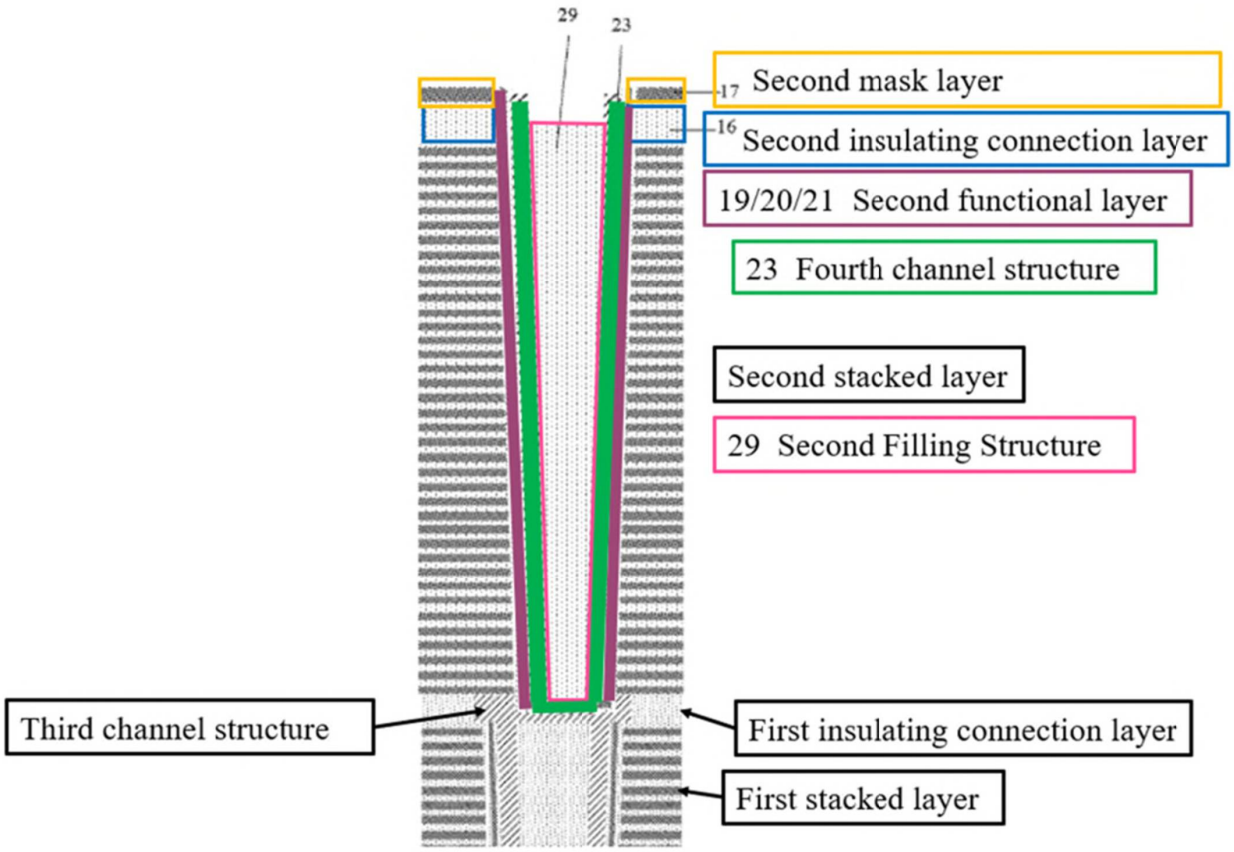


FIG. 19

Id., Fig. 19 (annotated); Banerjee ¶ 233.

Costa discloses the same, namely, forming a fourth channel structure ("second inner semiconductor channel layer 622" with or without the optional

layer 621) and forming a second filling structure ("second dielectric core 262") on the sidewall of the second functional layer ("stack of layers" 252, 254, 256, 621) and the exposed surface of the third channel structure. Banerjee ¶¶ 231, 234. Specifically, "a second inner semiconductor channel layer 622 can be deposited directly on the semiconductor surface of the second joint-level doped semiconductor portion 179." Costa, [0275] (and directly on optional semiconductor channel layer 621); Banerjee

¶ 235. Again, "an optional second outer semiconductor channel layer 621" can be deposited. Costa, [0273]; Banerjee ¶ 236. Figure 21D illustrates that second inner semiconductor channel layer 622 can be deposited on the inner surface of functional layer (layers 250) and the exposed portion of the first joint-level doped semiconductor portion 173. *Id.*, [0275], Fig. 21D; Banerjee ¶ 237.

Costa discloses that a "second dielectric core layer 262L" may be deposited as a core. Costa, [0275], Fig. 21.D; Banerjee ¶ 238. A subsequent etching process removes "the horizontal portion of the second dielectric core layer 262L," leaving second dielectric core 162 within the second memory cavity 249'. Costa, [0276]; Banerjee ¶ 239.

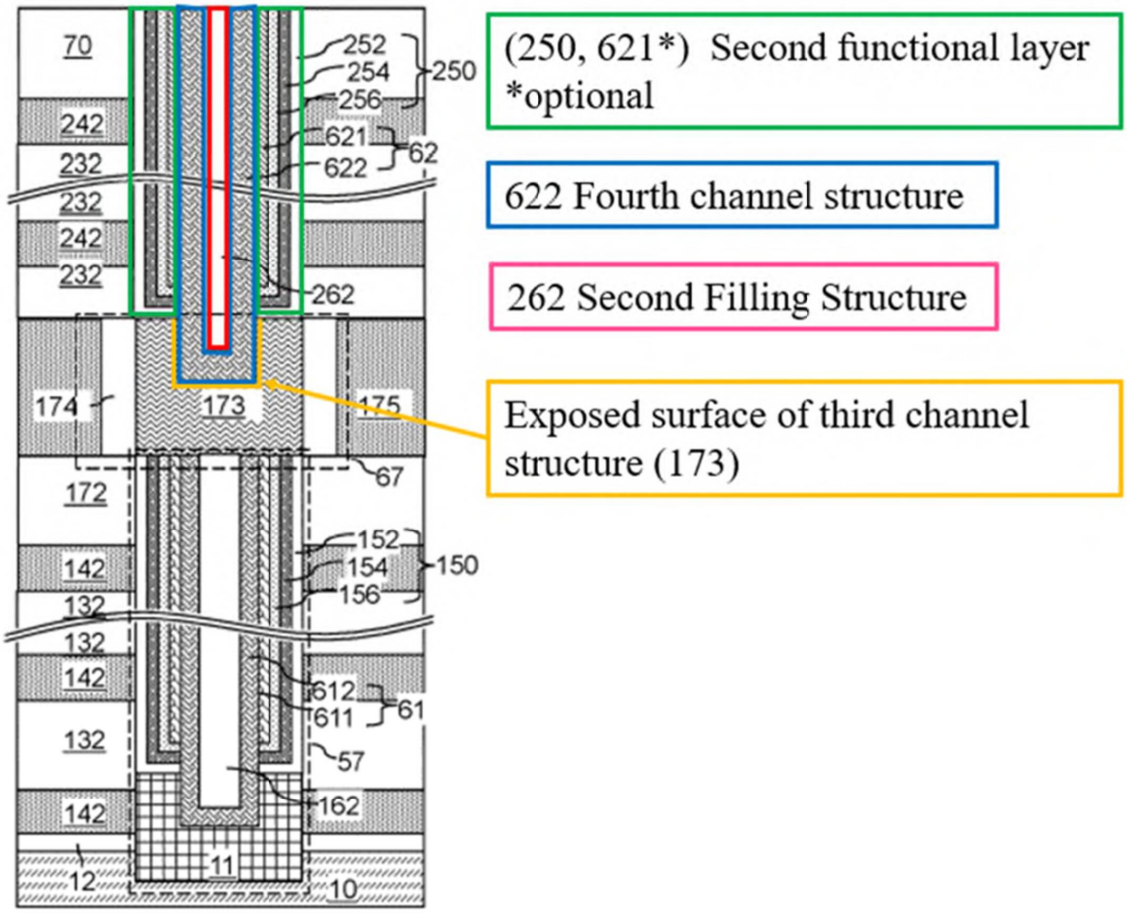


FIG. 21E

Id., Fig. 21E (annotated); Banerjee ¶ 239. Like Costa's second channel structures, layers 621 and 622 may be "amorphous silicon or polysilicon," and thus function as a channel. *Id.*, [0202], [0207]; Banerjee ¶ 240.

12. [1.K] "forming a fifth channel structure in contact with the fourth channel structure above the second through hole."

As described by the '291 Patent, the fifth channel structure is formed in a manner similar to that of the third channel structure (described above). "[A] second groove can be formed on the fourth channel structure and the second filling

structure, and in the second through hole 18." Ex. 1001, 15:12-14; Banerjee ¶ 242. The "fifth

channel structure can be formed in the second groove" and "the top surface of the second insulating connection layer 16 and the top surface of the fifth channel structure 30 can be planarized by any suitable techniques…." Ex. 1001, 15:24-36.

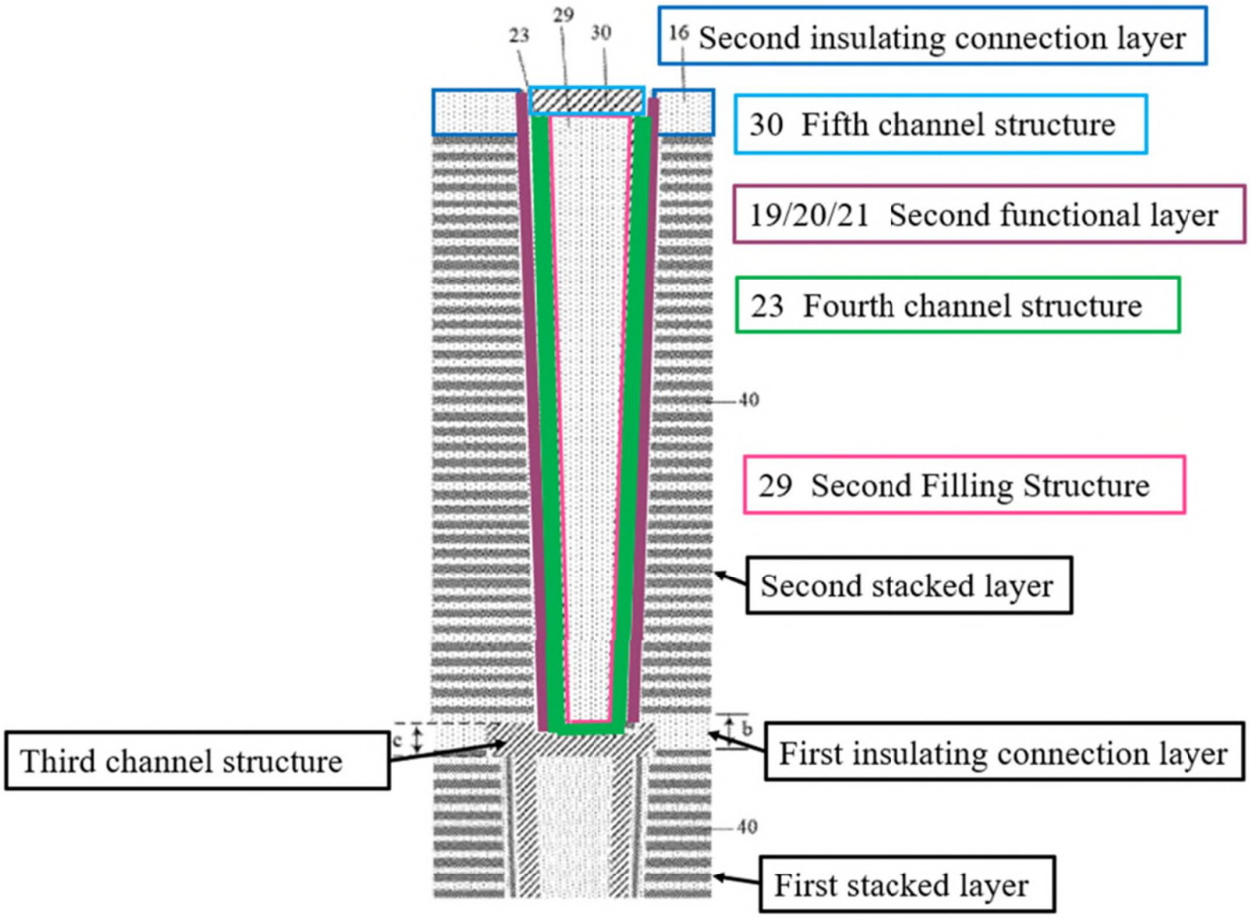


FIG. 22B

Id., Fig. 22B (annotated); Banerjee ¶ 243.

Costa discloses the same, namely, forming a fifth channel structure ("drain region 63") in contact with the fourth channel structure ("second inner

semiconductor channel layer 622") above the second through hole ("second-tier memory opening 249"). Costa, [0277]; Banerjee ¶¶ 241, 244. As shown in Figure

21F below, drain region 63 can be formed in a recess etched into second dielectric core 262 below the top surface of insulating cap layer 70:

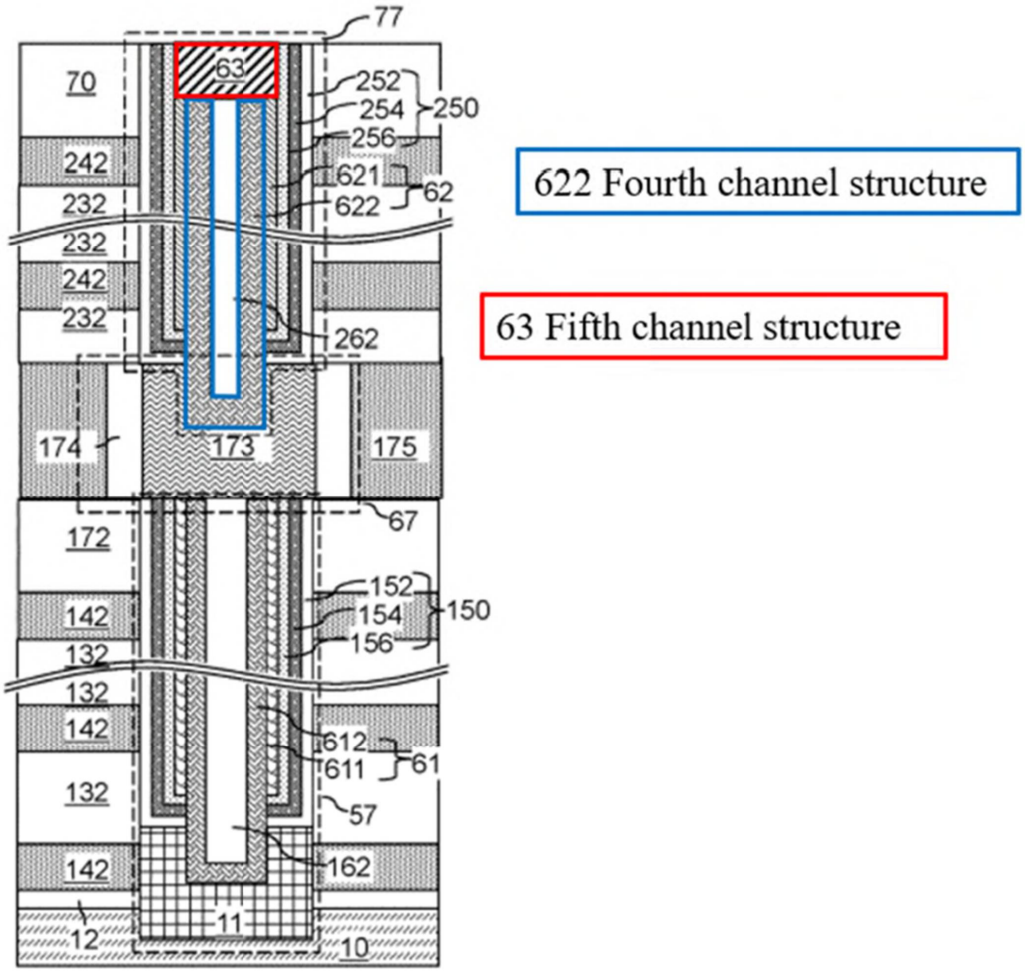


FIG. 21F

Id., Fig. 21F (annotated), [0277]; Banerjee ¶ 245. Drain region 63 is in contact with second inner semiconductor channel layer 621 (and optional layer 622).

Costa, Fig. 21F; Banerjee ¶ 246.

The drain regions are formed "above the second through hole." Banerjee ¶ 247. Specifically, Costa's "second through hole" starts at the top of insulating layer 70 (see [1.H] above). Banerjee ¶ 248. Costa describes forming drain regions in more detail with respect to the first embodiment, which Costa specifically references in the third embodiment regarding the conductive drains. Costa, [0277]; Banerjee ¶ 248. As Costa describes, forming conductive regions first involves etching the groove for the conductive drain and then depositing polysilicon for the drain. Costa, [0212]; Banerjee ¶ 249. Next, Costa discloses: "[e]xcess portions of the deposited semiconductor material can be removed from above the top surface of the insulating cap layer 70, for example, by chemical mechanical planarization (CMP) or a recess etch to form the drain regions 63." Costa, [0212]; Banerjee ¶ 250. In other words, the conductive drain ("fifth channel structure") is initially above hole, and CMP levels the plug to the same height as the connection layer. Banerjee

¶ 251.

To the extent PO argues that Costa's drain region 63 is not "form[ed] … above the second through hole" (second-tier memory opening 249) because after completion of forming drain region 63, the top of drain region 63 is at the top of "the second through hole" (Costa's hole 249), PO would be incorrect for at least two reasons. Banerjee ¶ 252.

First, Costa describes forming drain region 63 in exactly the same manner as the fifth channel structure in the '291 Patent, i.e., the "fifth channel structure" is not completely "above" the "second through hole" after fabrication of the memory has

been completed. As shown above, in the '291 Patent, "a fifth channel structure" is "above the second through hole" when it is at the same height as the connection layer 16. As shown in Figure 13, however, the '291 Patent depicts the top of "second through hole" 18 as being at the top of mask layer 17, i.e., above first insulating layer 16. Thus, this limitation cannot require that the "fifth channel structure" be fully above the "second through hole" after completing the method. Banerjee ¶ 253.

Second, independent claim 1 recites a method, not an apparatus. Thus, any argument by PO that Costa's drain region 63 is not "above" the second-tier memory opening 249 in its finished configuration is irrelevant. This limitation requires nothing more than that the fifth channel structure be "form[ed] … above the second through hole." Based on the plain language, Costa meets this limitation. Banerjee

¶ 254. Moreover, independent claims 11 and 20 (directed to "[a] joint opening structure of a three-dimensional (3D) memory device") recite "a fifth channel structure … ***disposed <u>over</u>*** the second through hole," Ex. 1001, cls. 11, 20, ***not*** "a

fifth channel structure … ***disposed <u>above</u>*** the second through hole." Nor does the

specification describe any such configuration—each embodiment describes a fifth channel structure just like that of Figure 22B (see above)—that is, a fifth channel structure located at the top of the second through hole, its top surface planarized with the top surface of the second insulating connection layer. *E.g.*, *id.*, 15:24-36, 24:21- 38, 32:6-16, 40:39-58, Figs. 21A-B, 22A-B, 23B, 48A-B, 49A-B, 50B, 72A-B, 73A-

B, 74B, 101A-B, 102A-B, 103B; Banerjee ¶ 256. Claims 11 and 20, and the embodiments described in the specification, make clear that what is claimed is not a fifth channel structure that is "above" the second through hole in its final configuration. Rather, what is claimed is a fifth channel structure that is "form[ed] … above the second through hole" and is "disposed above the second through hole in its final configuration. Banerjee ¶¶ 255-57.

B. ~~Claim 2:~~Motivation to Combine

A POSITA would have been motivated, with a reasonable expectation of success, in view of Liu's teachings to form a groove in Costa's insulating connection layer to form the third channel structure (173) therein for several reasons. Banerjee

~~1. [2.PRE] "The method of claim 1, wherein:" [2.A] "the first stacked layer includes a first number of oxide/nitride layer pairs; and" [2.B] "the second stacked layer includes a second number of oxide/nitride layer pairs."~~

~~**Costa discloses this limitation. Banerjee ¶ 259.**~~

~~**Costa teaches that "[t]he number of repetitions of the pairs of a first insulating layer 132 and a first sacrificial material layer 142 can be in a range from 2 to 1,024, and typically from 8 to 256." Costa, [0133]; Banerjee ¶ 260. And the same is true of the second alternating stack. *Id.*, [0182]. And as discussed in [1.A] and [1.G] above, these stacked layers can be comprised of oxide/nitride layer pairs. Banerjee**~~

¶ ~~**2**~~**38**6~~**1**~~.

~~**To the extent PO argues that Costa fails to disclose this limitation by arguing that the "first number" and "second number" must be different, PO would be incorrect. The "first" and "second" just denote different physical stacks. *See* Ex. 1001, cl. 2, 43:18-21 ("[T]he words 'first', 'second' and the like used in this disclosure do not denote any order, quantity or importance, but are merely intended to distinguish between different constituents."); *see also id.*, 2:6-10, 6:8-16; Banerjee ¶ 262-63.**~~

~~**C. Claim 3:**~~

~~**1. [3] "The method of claim 2, wherein: the first number and the second number are not less than 32."**~~

~~**The analysis in [2] demonstrates that Costa discloses this limitation. Banerjee**~~

First, utilizing Liu's groove in an insulating connection layer was a "known technique" that was at least "a suitable option" for Costa's third channel structure. *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023). Liu's etch creates a recess for Costa's third channel structure, and electrically couples the third and second channel structures by forming the two structures such that they physically contact each other. Banerjee ¶¶ 387-88. Liu's etch and conductive plug therein serves the same purpose as Costa's insulating connection layer 172 and third channel structure thereon, and was a known technique and suitable option for Costa. Banerjee ¶¶ 389-91.

~~**¶ 265.**~~

~~**D. Claim 4:**~~

~~**The claim 4 here mapping applies YMTC's interpretation of the claim limitations, namely, that the first three claimed layers may formed in the opposite order as claimed and described in the '291 Patent. Banerjee ¶ 267; *see* §VII.**~~

~~**1. [4.PRE] "The method of claim 1, wherein forming the first functional layer comprises:" [4.A] "forming a first tunneling layer on the sidewall of the first through hole and the exposed surface of the first channel structure, wherein the first tunneling layer is configured, in operation, to generate charges;"**~~

~~**Under YMTC's claim interpretation, Costa discloses forming a first**~~

~~tunneling layer ("first tunneling dielectric layer 156") on the sidewall of the first through hole (149') and exposed surface of the first channel structure (11):~~

Second, a POSITA would have been motivated to adopt Liu's teachings. Banerjee ¶ 392. Like Costa, Liu relates to a multi-tier structure. Banerjee ¶ 393; Liu, Abstract. As Liu recognizes, issues in multi-tier structures include aligning the structures, which Liu addresses. Liu, Abstract. Costa, too, seeks to address alignment issues: "Some of the challenges for fabricating a multi-tier memory stack structure include formation of memory openings having high aspect ratios and alleviation of effects of misalignment of tier-level memory openings formed in different tier structures. Thus, methods are desired for providing a reliable connection between vertically neighboring memory stack structures." Costa, [0003]; Banerjee ¶ 394. Thus, a POSITA would have been highly motivated to adopt Liu's teaching to address Costa's alignment issues. Banerjee ¶ 395.

~~Costa, Fig. 4D (annotated), [0144] (sequentially forming layers 152, 154, 156, and 611); Banerjee ¶ 267-68.~~

~~With respect to this limitation's "generate charges" requirement, the '291 Patent discloses: "The first tunneling layer 7 can be used for~~

~~**generating electronic charges (electrons or holes). In some embodiments, the first tunneling layer 7 can be an oxide layer formed by using a deposition process." Ex. 1001, 10:46-50. This apparently refers to the fact that electronic charges tunnel through this layer (as an oxide layer does not "generate" charges by itself), and in this sense the layer generates charges for the data storage layer under YMTC's interpretation. Banerjee**~~

~~**¶¶ 269-70. Costa discloses the same for its tunneling layer: "first tunneling dielectric layer 156 [that] includes a dielectric material through which charge tunneling can be performed under suitable electrical bias conditions." Costa, [0151]; Banerjee ¶ 271.**~~

~~**2. [4.B] "forming a first storage layer on the surface of the first tunneling layer to store the charges generated by the first tunneling layer;"**~~

~~**Under YMTC's claim interpretation, Costa discloses forming a first storage layer ("first charge storage layer 154") on the first tunneling layer ("first tunneling dielectric layer 156"):**~~

~~**Costa, Fig. 4D (annotated), [0144] (sequentially forming layers 152, 154, 156, and 611); Banerjee ¶ 273.**~~

~~**As to this limitation's requirement of "stor[ing] the charges**~~

~~**generated by the first tunneling layer," recall that Costa discloses "first tunneling dielectric layer 156 [that] includes a dielectric material through which charge tunneling can be performed under suitable electrical bias conditions." Costa, [0151]. Costa's "first charge storage layer 154" stores the charges that tunnel through "first tunneling dielectric layer 156": "[t]he first charge storage layer 154 can comprise a charge trapping material or a floating gate material." *Id.*, [0154]; *id.*, [0148] ("first charge storage layer 154 can be a continuous layer or patterned discrete portions of a charge trapping material including a dielectric charge trapping material"); Banerjee ¶ 272, 274-76.**~~

~~**3. [4.C] "forming a first barrier layer on the surface of the first storage layer to block the outflow of charges in the first storage layer;"**~~

~~**Under YMTC's claim interpretation, Costa discloses forming a first barrier layer ("first blocking dielectric layer 152") on the surface of the first storage layer ("first charge storage layer 154"):**~~

~~**Costa, Fig. 4D (annotated), [0144] (sequentially forming layers 152, 154, 156, and**~~

~~**611); Banerjee ¶ 277-78.**~~

~~**As to this limitation's requirement that the barrier is formed "to block the outflow of charges in the first storage layer," Costa discloses**~~

~~that "[t]he first blocking dielectric layer 152 can include a single dielectric material layer or a stack of a plurality of dielectric material layers." Costa, [0145]. In other words, the blocking layer is a barrier layer because, using dielectric material, it "block[s]" the outflow of charges from the storage layer into the gate layers. *Id.*; Banerjee ¶ 279-81.~~

~~4. [4.D] "forming a first passivation layer on the surface of the first barrier layer to protect the first barrier layer from being damaged in a subsequent removal process; and"~~

~~Under YMTC's claim interpretation, Costa discloses forming a first passivation layer ("first outer semiconductor channel layer 611") on the surface of the barrier layer ("first blocking dielectric layer 152"):~~

~~Costa, Fig. 4D (annotated), [0144] (sequentially forming layers 152, 154, 156, and~~

~~611); Banerjee ¶ 282-83.~~

~~As to this limitation's requirement "to protect the first barrier layer from being damaged in a subsequent removal process," the '291 Patent describes a "passivation~~

~~layer" as protecting the barrier layer during removal of the bottom portion of the functional layer. Ex. 1001, 11:3-17; Banerjee ¶ 284-85.~~

~~**The first passivation layer may comprise "amorphous silicon" i.e., a semiconductor material. Ex. 1001, 11:7–9; Banerjee ¶ 286.**~~

~~**Costa discloses the same. According to Costa, "optional first outer semiconductor channel layer 611 includes … semiconductor materials known in the art." Costa, [0152]; Banerjee ¶ 287. After this layer is deposited, a subsequent etching process removes portions of it and the other layers of the first functional layer. Banerjee ¶ 288; *see* [4.E], *infra*. Thus, layer 611 acts as a "passivation layer," because it protects the memory film during the removal of the bottom portion of layers 152,154, 156, and 611. Banerjee ¶ 289. Moreover, just like the '291 Patent, Costa's passivation layer is "amorphous silicon" i.e., a semiconductor material. Costa, [0152]; Banerjee ¶ 290.**~~

~~**5. [4.E] "removing portions of the first passivation layer, the first barrier layer, the first storage layer, and the first tunneling layer on the surface of the first channel structure, wherein remaining portions of the first passivation layer, the first barrier layer, the first storage layer, and the first tunneling layer on the sidewall of the first through hole to form the first functional layer."**~~

~~**Under YMTC's claim interpretation, Costa discloses this limitation. Banerjee**~~

~~**¶ 291.**~~

~~**Specifically, as the below illustrates, Costa removes the bottom portions of these layers to expose the first channel structure:**~~

~~Costa, Figs. 4C, 4D, [0153] ("portions of the first outer semiconductor channel layer 611, the first tunneling dielectric layer 156, the first charge storage layer 154, and the first blocking dielectric layer 152 at a bottom of each first memory cavity 149' can be removed"); Banerjee ¶ 292.~~

~~E. Claim 5:~~

~~1. [5.PRE] "The method of claim 4, wherein forming the second channel structure and the first filling structure comprises:" [5.A] "forming a second channel layer that covers the sidewall of the first passivation layer and the exposed surface of the first channel layer;~~

~~As discussed in [1.E], Costa discloses this limitation: "[A] first inner semiconductor channel layer 612 can be deposited directly on the semiconductor surface of the epitaxial channel portion 11 … and directly on the first outer semiconductor channel layer 611." Costa, [0156]; Banerjee ¶ 295 (recall that layer 611 is optional).~~

~~2. [5.B] "forming the first filling layer that covers the surface of the second channel layer;"~~

~~As discussed in [1.E], Costa discloses this limitation: "a first dielectric core layer 162L can be deposited in the first memory cavity 149' to fill any remaining portion…." Costa, [0158], Fig. 4F; Banerjee ¶¶ 296-97.~~

~~3. [5.C] "removing a portion of the first filling~~

> ~~layer to form the first filling structure, wherein the top surface of the first filling structure is lower than the top surface of the first insulating connection layer; and [5.D] "removing a portion of the second channel layer to form the second channel structure, wherein a top surface of the second channel structure is lower than a top surface of the first insulating connection layer."~~

~~Collectively, these limitations require recessing the filling layer and second channel layer to form a filling structure and second channel structure in which the top surface of both are below the first insulating connection layer. Banerjee ¶ 299.~~

~~The analysis below treats these two limitations together, because in view of the knowledge of a POSITA, it would have been obvious to recess both structures below the insulating connection layer (layer 172 of Costa) with a single etch. Banerjee~~

~~¶¶ 298, 300.~~

~~As an initial matter~~**Third**, Costa expressly recognizes the desire to reduce the height of the device: "Referring to FIG. 22A, an alternate embodiment of the third exemplary structure ~~…~~**after formation of the second memory opening fill structures 77, which** is derived from the third exemplary structure by reducing the thicknesses of each joint-level doped semiconductor portions 173, each single annular dielectric spacer 174, and the joint-level spacer material layer 175**, for example, to a range from 20 nm to 150 nm, although lesser and greater**

thicknesses can also be employed." Costa, [0281]; Banerjee ¶ ~~301~~**396-97**. This reduction is shown below:

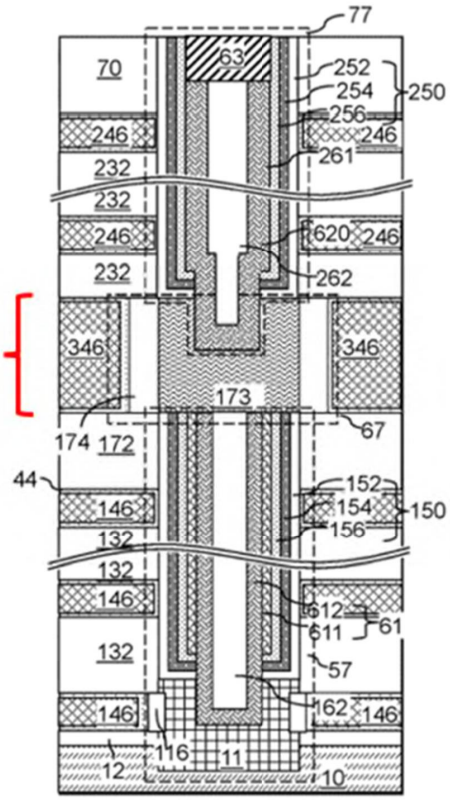


FIG. 21G

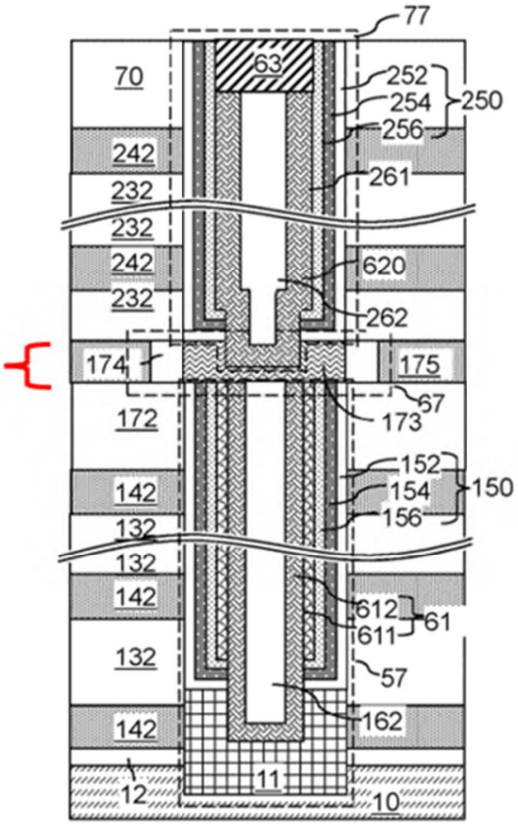


FIG. 22A

***Id.*, Figs. 21G, 22A (annotated); Banerjee ¶ 398. Liu furthers this goal by teaching to form the groove directly in insulating connection layer 172 of Costa, thereby further reducing the height as shown below (*see also* claim [6.B] *infra*):**

~~***Id.*, Figs. 21G, 22A (annotated); Banerjee ¶ 302.**~~

~~**Another well-known technique to reduce the height was simply to recess the interface plug into the insulating connection layer (as opposed to including the plug on top in an additional layer). The below figure demonstrates this knowledge of a POSITA:**~~

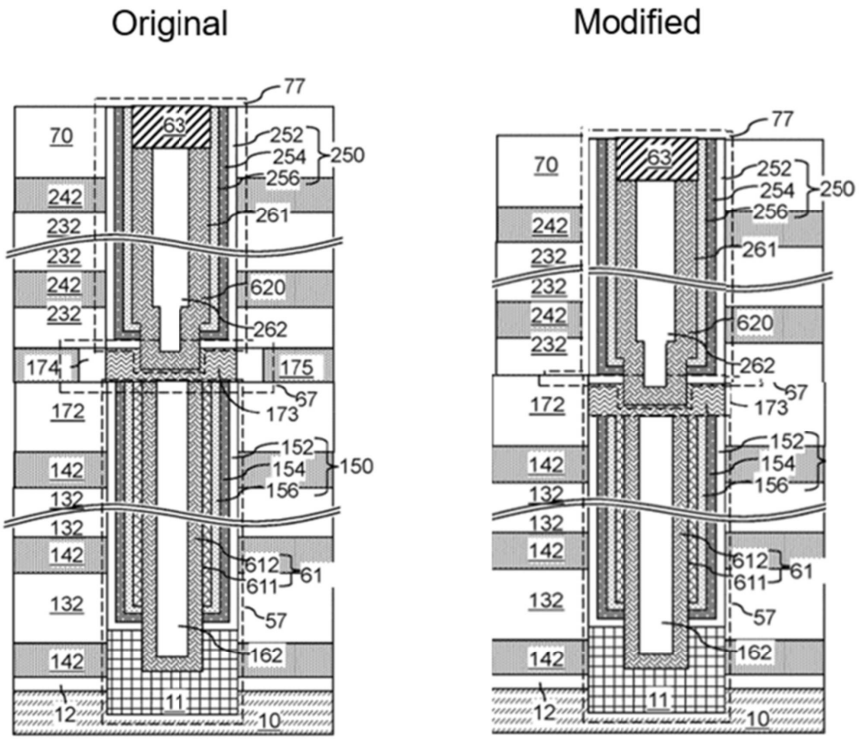


FIG. 22A FIG. 22A

~~**Ex. 1016, Fig. 4B (annotated), 4:63-5:9 (insulating layer 27 and connection pattern 16); Banerjee ¶ 303-04. Put another way, this design option may involve recessing the channel structure and dielectric core, providing space to place the plug in the recess. The figure below provides a further example of this well-known option:**~~

~~**Ex. 1017, Fig. 5B (annotated), 9:44-61 (forming recessed plug); Banerjee ¶ 305. Applying this knowledge of a POSITA to further the intent of Costa's embodiments that reduce device height results in the following modification, shown relative to Costa's short plug:**~~

~~Costa~~*Id.*, Fig. 22A (original), 22A (modified); Banerjee ¶ ~~306-07~~399.

Fourth, in addition to furthering Costa's ~~embodiments to reduce~~**express goal of lowering the** device**'s** height (~~the~~ height ~~of a device~~ impacts fabrication in multiple ways, e.g., ~~taller~~**higher** structures require longer etching time to form holes through the stack), recess techniques improve contact resistance. ~~Banerjee ¶ 308.~~ It was well known that increasing ~~the~~ contact area decreases ~~the~~ contact resistance. Banerjee ¶ ~~3~~**4**0~~9~~**0**; *see also, e.g.*, Ex. 1018 (Stavitski), 1 ("the contact resistance depends on the contact area[]"); Ex. 1019 (Fasoli), 10 ("small contact area tends to give rise to high contact resistance."). Costa implicitly recognizes this with his design of the lower and upper channel structures. Banerjee ¶ ~~3~~**40**1~~0~~. As shown in Fig. 21F below, Costa etches portions of

first channel structure 11 and third channel

structure 173 to expose sidewalls thereof, and then deposits the second channel structure 162 and fourth channel structure 620 therein, thereby increasing the contact area between these structures. ~~As~~ Costa ~~and the above prior art examples demonstrate~~**did not follow that design strategy in dielectric core 162.**

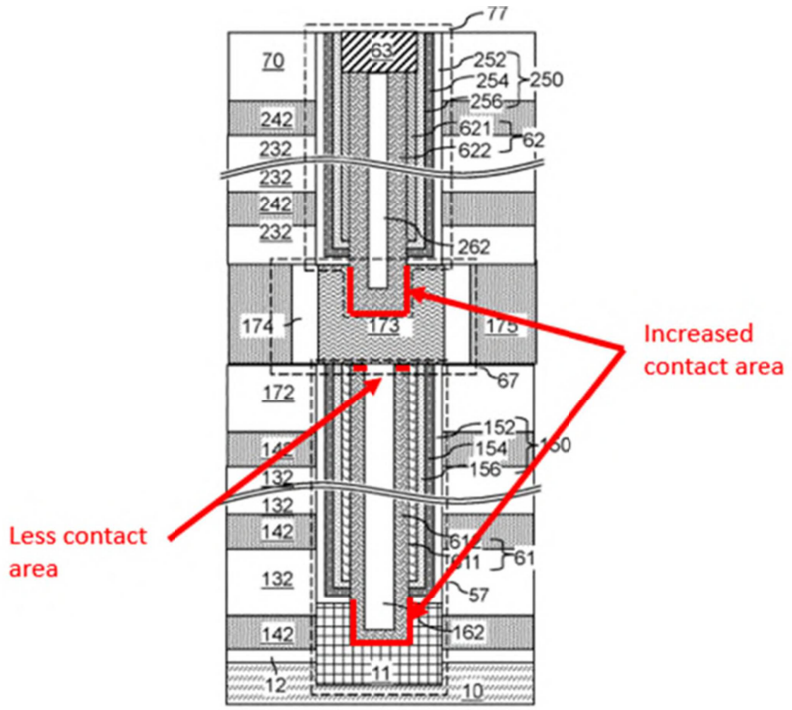


FIG. 21F

~~, recess techniques were well known, and employing those techniques would further allow recessing the conductive third~~**Costa, Fig. 21G (annotated); ¶ 402. A recess into insulating connection layer would allow additional recessing of the dielectric core 162 to a lower level than second** channel structure ~~173 in a further recess of 162~~**162, creating the same additional contact area as Costa has done above and below that interface**. This also provides the ~~known~~ benefit of decreasing contact resistance. **Banerjee ¶ 403-04.**

Fifth, a POSITA would have understood that forming Costa's portion 173 in a groove in layer 172 would further Costa's goal of aligning the structures. Costa,

[0191]; Banerjee ¶ 405. Consistent with Liu (see claim [6.B]), it was well

understood the groove can be larger than the channel hole, thereby accounting for alignment issues. In other words, simply forming the groove larger than the channel hole accounts for process variations that cause misalignment. *Id.* ; Ex. 1021, 2:60- 3:6 (noting process variation issues in non self-aligned processes). Thus, Liu's approach addresses process variations that result in misalignment, beneficially increasing yield. Banerjee ¶ 405; Ex. 1023, [0086].

~~**Costa, Fig. 21F (annotated); Banerjee ¶¶ 311-13.**~~

A POSITA would have had a reasonable expectation of success in implementing ~~**such recess techniques**~~**Liu's teaching** in Costa. Banerjee ¶ ~~**31**~~4**06**. First~~**, as the above illustrates**~~, recessing such structures was well known. **Banerjee ¶ 407.** It merely involves masking

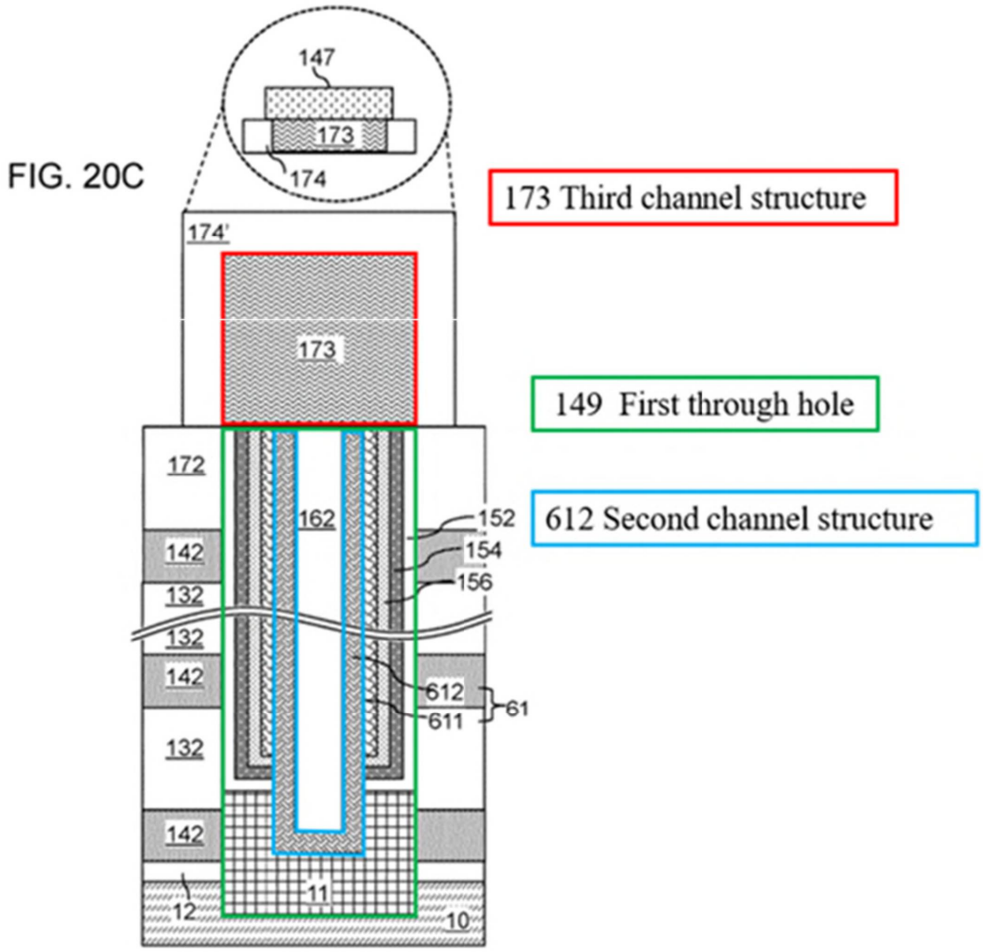
and, e.g., an anisotropic etch. These are techniques that Costa already discloses. ~~**Banerjee ¶ 315; *see,***~~ *E.g.*, Costa, [0137]-[0138]. Second, as ~~**demonstrated**~~**shown** above, Costa already discloses ~~**forming**~~ recess~~**es**~~**ing** ~~**and depositing material therein**~~**such layers, e.g., layer 70**, consistent with the goal of decreasing contact resistance. Banerjee ¶ ~~**316**~~**408**.

~~F~~C. Claim ~~8~~6:

1. [~~8~~6.PRE] "The method of claim 1, ~~further~~wherein forming the third channel structure comprisi~~ng~~es:" [~~8~~6.A] "~~forming a first mask layer overlaying~~etching the first insulating connection layer ~~before forming~~to form a first groove, wherein a projection of the first groove on the substrate covers the projection of the first through hole on the substrate; ~~and~~"

~~As discussed in [1.B], Costa discloses this limitation: "To form the first-tier openings (149, 119), a lithographic material stack (not shown) including at least a photoresist layer can be formed over the first tier structure (132, 142, 172, 165), and can be lithographically patterned to form openings within the lithographic material stack." Costa, [0137] (transferring pattern); Banerjee ¶¶ 318-19.~~

Recall that Costa discloses a first insulating connection layer (i.e. first-tier insulating cap layer 172) and a third channel structure (i.e. joint-level doped semiconductor portion 173) on the first insulating connection layer. Banerjee ¶ 410.



Costa, Fig. 20C (annotated); Banerjee ¶ 410.

At the '291 Patent's assumed effective filing date, a POSITA would have been motivated to etch a groove in the first insulating connection layer 172 (effectively widening the aperture in which to form 173) for connecting the third channel structure 173 and the second channel structure 612 in view of Liu to further Costa's express goal of reducing the device height and to decrease contact resistance. Banerjee ¶¶ 409, 411; *see also* §X.B. Moreover, forming the third channel structure

(173) with a wider aperture would further serve Costa's goal of ensuring

alignment between vertically neighboring channels. Costa, [0003]; Banerjee ¶ 412-13.

Liu discloses etching a first insulating connection layer (insulating layer 121B, 1801, and insulating layer 121A) to form a first groove (annotated on Fig. 18E below), wherein a projection of the first groove on the substrate covers the projection (annotated on Fig. 18E below) of the first through hole (i.e. holes filled with 1/7/9/11) on the substrate (substrate 100).

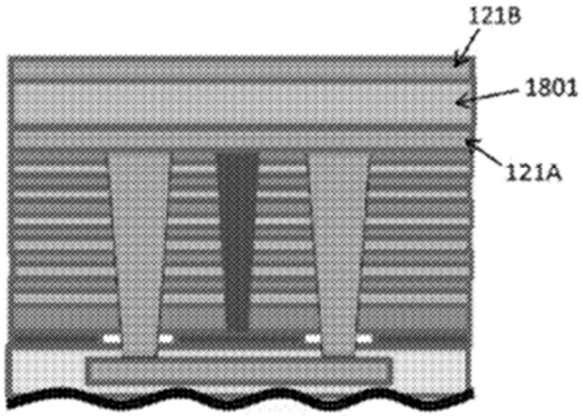


Fig. 18D

~~2. [8.B] "removing the first mask layer after forming the first filling structure;"~~

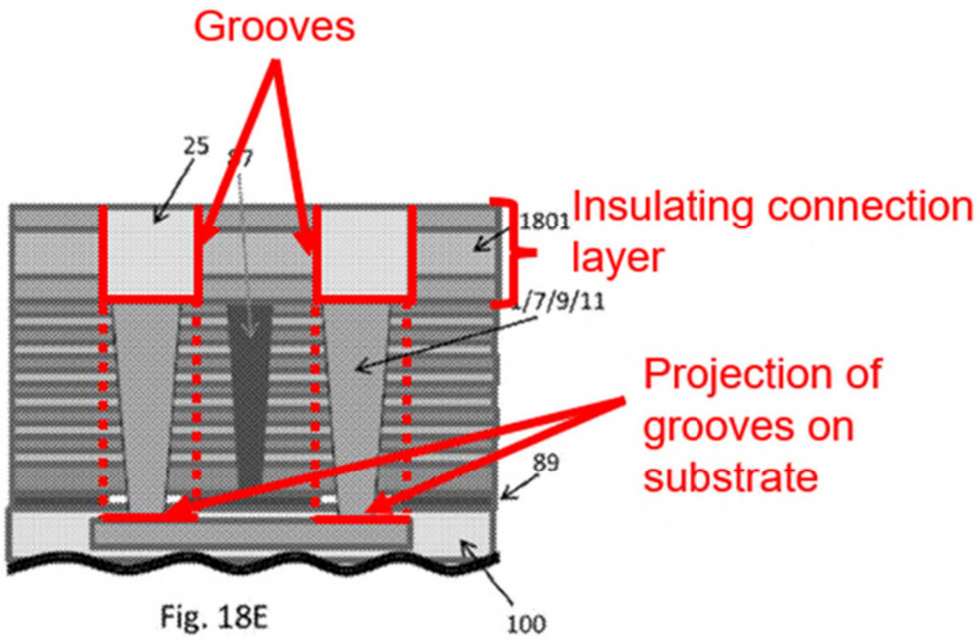


Fig. 18E

~~Costa discloses this limitation. Costa, [0138] ("Subsequently, the patterned lithographic material stack can be subsequently removed, for example, by ashing."). Banerjee ¶¶ 320-21.~~

Liu, Figs. 18D, 18E (annotated); Banerjee ¶ 414.

Specifically, Liu discloses depositing insulating layer 121A, then boosting layer 1801, and then insulating layer 121B. Liu, [0173]; Banerjee ¶ 415. Then, Liu creates grooves over the lower-level memory holes by an etching process: "[a]s illustrated in FIG. 18E, a mask, such as a photoresist mask, may be applied to the surface of the second insulating layer 121B and patterned. Portions of the second insulating layer 121B, the current boosting layer 1801 and the first insulating layer 121A located over the memory holes may be removed by etching." Liu, [0173]; Banerjee ¶ 416.

Applying this teaching to Costa, a POSITA would have recognized that

in Costa, both first insulating connection layer 172 and the dielectric filler 162 can be silicon oxide. Costa [0134] (layer 172 can be silicon oxide), [0158]-[0159] (layer

162L can be silicon oxide); Banerjee ¶ 417. A POSITA would further have recognized that layer 142 underlying layer 172 can be silicon nitride. Costa [0181]; Banerjee ¶ 418. As such, a POSITA would have understood that creating a groove in layer 172 of the combination would be done with an etch preferential to silicon oxide, using the layer underlying layer 172 as an etch stop. Banerjee ¶ 419. As a result, as Liu demonstrates, the practical groove involves etching a wider opening through layer 172 and stopping as the etch penetrates the underlying layer, i.e., silicon nitride layer 142. Banerjee ¶ 420. The modification of Costa in view of Liu is illustrated with reference to Costa's embodiment that attempts to shorten the stack height:

Original

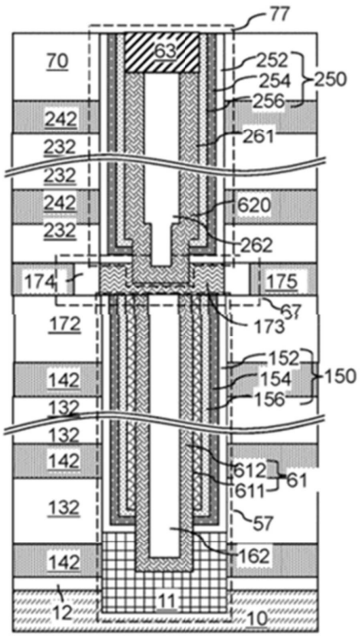


FIG. 22A

Modified

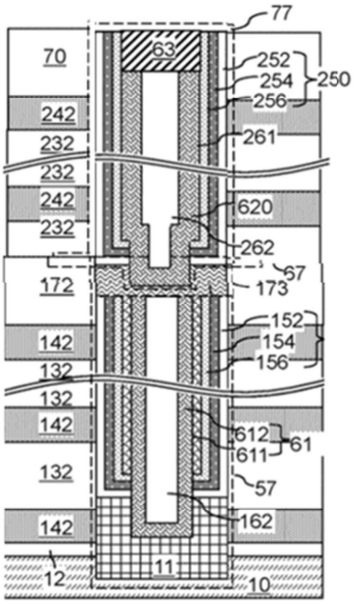


FIG. 22A

Costa, Fig. 22A (original), Fig. 22A (modified); Banerjee ¶ 421.

1. [6.B] "forming a third channel layer in the first groove, wherein the third channel layer is in contact with the second channel structure; and"

Costa in view of Liu's teaching discloses forming a third channel layer (173) in the first groove, wherein the third channel layer (173) is in contact with the second channel structure (612) as shown in modified Fig. 22A above. Banerjee ¶ 422-23.

~~3~~2. [~~8~~6.C] "~~forming a second mask layer on the second~~planarizing the top surfaces of the first insulating connection layer ~~before forming the second through hole; and~~and the third channel layer to form the third channel structure."

In view of Liu's teaching of forming the groove through the insulating connection layer, it would have been obvious to planarize the top surfaces of the first insulating connection layer and third channel structure. Banerjee ¶¶ 424-25. It was well known that the typical deposition of a plug interface requires planarizing the top surface because the deposition results in material above the target height. Banerjee ¶ 426. For example, Costa discloses that "[e]xcess portions of the deposited semiconductor material can be removed from above the top surface of the insulating cap layer 70, for example, by chemical mechanical planarization (CMP)." Costa, [0212]; Banerjee ¶ 427. Similarly, Liu recognizes the need to planarize in other embodiments: "The landing pad 55 formation may comprise epitaxially growing a 'mushroom head' shaped overgrown silicon 56 on exposed portions 1L of the channels 1.

This silicon overgrowth 56 is then covered by an insulating gap fill layer (e.g., silicon oxide or nitride). The silicon mushroom head 56 and the gap fill layer are then planarized (e.g., by CMP) to form planar landing pads 55 on each pillar 1L." Liu, [0100]; Banerjee ¶ 428.

By way of other examples, Lee discloses "[a]n upper portion of the pad layer may be planarized until the top surface of the uppermost insulating interlayer 102j is exposed to obtain the pad 150. In example embodiments, the pad layer may be formed using polysilicon or doped polysilicon. In one example embodiment, a preliminary pad layer may be formed using amorphous silicon, and then a crystallization process may be performed thereon to form the pad layer. The planarization process may include a CMP process." Lee, [0094]; Banerjee ¶ 429. And Lee 548 discloses "[u]pper portions of the first insulation layer patterns 148, the oxide layer 141, the charge storage layer 142, the tunnel insulation layer 144 and the channel pattern 146 in each channel hole 130 may be removed to form a recess and a pillar structure in each channel hole 130. A polysilicon layer may be formed to fill the recesses, and an upper portion of the polysilicon layer may be planarized until a top surface of the insulating interlayer 110 may be exposed to form a plurality of pads 150 on the pillar structures, respectively." Ex. 1020, [0100]; Banerjee ¶ 430. As such, in this modification of Costa, it would

have been understood, or obvious, that planarization would occur after the deposition of third channel structure 173. Such planarization was a textbook step in the deposition of such plugs. Banerjee ¶ 431.

~~**As discussed in [1.H], Costa discloses this limitation: "[A] lithographic material stack (not shown) including at least a photoresist layer can be formed over**~~

~~**the second tier structure (232, 242, 265, 70), and can be lithographically patterned to form openings within the lithographic material stack." Costa, [0192] (transferring pattern); Banerjee ¶¶ 322-23.**~~

~~**4. [8.D] "removing the second mask layer after forming the second filling structure."**~~

~~**Costa discloses this limitation. Costa, [0194] ("Subsequently, the patterned lithographic material stack can be subsequently removed, for example, by ashing."). Banerjee ¶¶ 324-25.**~~

~~G~~D. Claim ~~9~~7:

1. [~~9~~7.PRE] "The method of claim 1, wherein forming the ~~fourth~~third channel ~~structure and the second filling~~ structure comprises:" [~~9~~7.A] "~~forming a fourth channel layer that covers the sidewall of a second functional layer and the exposed surface of the third channel layer;"~~etching the first insulating connection layer and at least a portion of the top nitride layer of the first stacked layer to form a first groove, wherein a projection of the first groove on the substrate covers the projection of the first through hole on the substrate;"

~~**As discussed in [1.J], Costa discloses this limitation. Costa discloses that second inner semiconductor channel layer 622 (the fourth channel structure) can be deposited on the inner surface of second outer semiconductor channel layer 621 and the exposed portion of the first joint-level doped semiconductor portion 173. Costa, [0275], Fig. 21D; Banerjee ¶¶ 327-28.**~~

Limitation [7.A] is identical to [6.A] except that the etching requires "etching the first insulating connection layer *and at least a portion of the top nitride layer of the first stacked layer* to form a first groove," (emphasis added), and is otherwise disclosed or rendered obvious to the same reasons. Banerjee ¶¶ 432-33.

As discussed above, etching a groove directly on layer 172 would remove portions of the silicon nitride layer as part of the etch that stops on layer 142. Banerjee ¶ 434.

2. [~~9~~7.B] "forming ~~a second filling layer that covers the surface of the fourth channel layer;~~the third channel structure in the first groove, wherein the third channel structure is in contact with the second channel structure; and"

~~**As discussed in [1.J], Costa discloses this limitation. Recall that, where second-tier memory opening 249 is not completely filled, the cavity is filled with "second dielectric core layer 262L." Costa, [0275], Fig. 21D; Banerjee ¶¶ 329-30.**~~

Limitation [7.B] is identical to [6.B] and is disclosed or rendered obvious to the same reasons.

3. [7.C] "planarizing the top surfaces of the first insulating connection layer and the third channel structure."

Limitation [7.C] is substantively identical to [6.C] and is disclosed or rendered obvious to the same reasons.

XI. GROUND 2: DEPENDENT CLAIM 10 IS OBVIOUS OVER COSTA IN VIEW OF LEE

A. Motivation to Combine

A POSITA would have been motivated, with a reasonable expectation of success, to utilize the entire width of the through hole, as taught by Lee, when forming the fifth channel structure 63 of Costa for several reasons. Banerjee ¶¶ 439- 40.

To start, utilizing Lee's groove through the entire width of the through hole was a "known technique" that was at least "a suitable option" for Costa's conductive drain. *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023). Lee's etch creates a recess for Costa's conductive drain, and electrically couples the conductive drain to Costa's fourth channel structure. This serves the same purpose as Costa's conductive drain and was a known technique and suitable option for Costa. Banerjee ¶ 441.

In addition, Lee's approach increases the width of the conductive drain. As a result, the conductive drain is wider. Banerjee ¶ 442. As Costa recognizes, a bit line ultimately connects to the conductive drain. Costa, [0233]; Banerjee ¶ 444; §V. Thus, Lee's approach provides a wider landing area for the bit line connection (which may occur through another interconnect structure on the conductive drain). Banerjee ¶ 443. In short, Lee's approach beneficially increases the margin for the interconnection of

the conductive drain to upper-level interconnects. Banerjee ¶ 445. Likewise, Lee's approach increases the width of the bottom interface of the conductive drain, which connects to the fourth channel structure. As the analysis under claim [1.F] discusses in detail, Costa does not employ a self-aligned process. As a result, it was known to include margin in structures to account for misalignment. Banerjee ¶ 445; *see also, e.g.*, Ex. 1021, 2:60-3:6 (noting process variation issues in non self-aligned processes); Ex. 1022, 20-21; Ex. 1023, [0023], [0086]; Liu, [0058]; Ex. 1024, Fig. 2F, [0061]. Addressing this natural misalignment issue increases yield. Banerjee ¶ 445.

A POSITA would have had a reasonable expectation of success in employing Lee's teachings. Banerjee ¶ 446. As Lee demonstrates, such etching was routine. Lee, [0093]-[0094] ("Referring to FIG. 8, upper portions of the dielectric layer structure 129, the channel 135 and the first filling layer pattern 145 may be partially removed to form a recess 147, and then a pad 150 capping the recess 147 may be formed. In example embodiments, an upper portion of the multi-stacked structure may be removed by an etch-back process to form the recess 147."). Such etches were textbook material. And Costa already discloses etching to form a recess for the conductive drain and depositing said conductive drain (see [1.K] above).

Banerjee ¶¶ 447-49.

B. Claim 10:

1. [~~9~~10.~~C] "removing a portion of the second filling layer to form the second filling structure~~PRE] "The method of claim 1, wherein ~~the top surface of the second filling~~forming the fifth channel structure ~~is lower than the top surface of the~~comprises:" [10.A] "etching the second insulating connection layer~~; and~~ to form a second groove, wherein a projection of the second groove on the substrate covers the projection of the second through hole on the substrate;"

Costa does not expressly disclose the limitations of claim 10. *See* Banerjee ¶ 450-51. Costa discloses forming a fifth channel structure 63 by forming a recess and depositing 63 in that recess. Costa, [0212], [0260]; Banerjee ¶ 451. While Costa states that the dielectric core can be recessed (*id.*), Costa depicts recessing the dielectric core and the semiconductor layers 622 and 621:

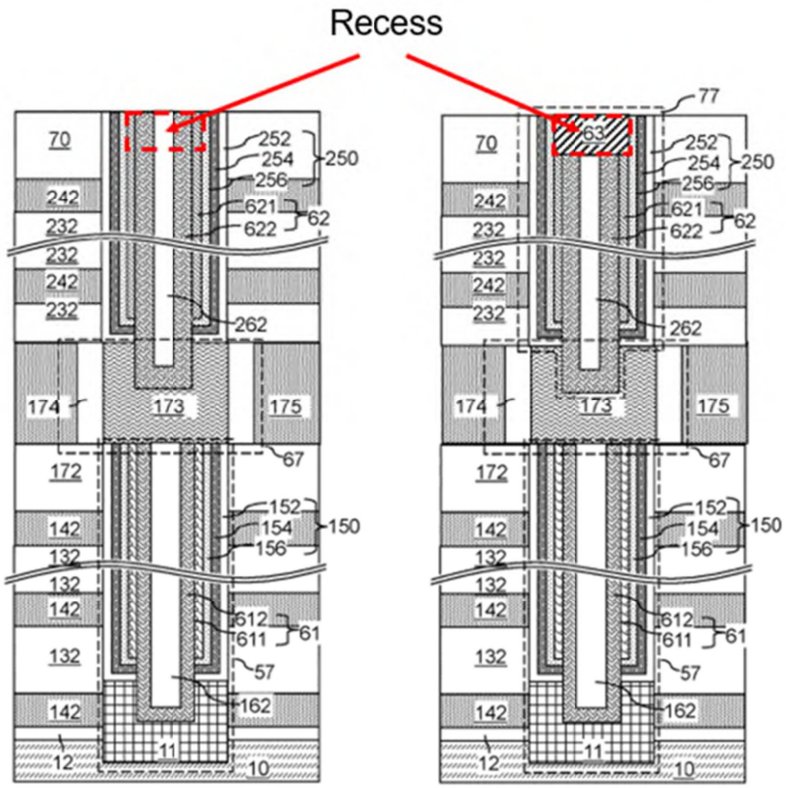


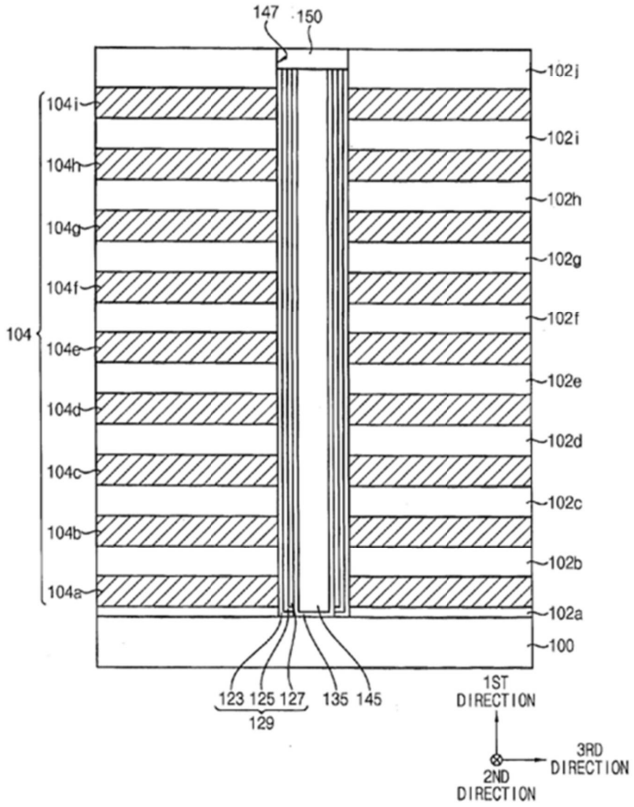
FIG. 21E FIG. 21F

~~As discussed in [1.J], Costa describes removing the horizontal portions of dielectric core layer 262L located above second-tier insulating cap layer 70. Costa, [0276]. And, as discussed in [1.K] above, dielectric core 262 is recess etched "below~~*Id.*, Figs. 21E, F (annotated); Banerjee ¶ 451. Accordingly, a POSITA would have understood that the exact width of the recess is not critical to Costa, but only that the recess enables the conductive drain to be formed under the top surface of the insulating ~~cap~~ layer 70~~," creating a groove in which drain region 63 is deposited. Costa, [0277], Fig. 21F;~~. Banerjee, ~~¶¶ 331-33~~ 452.

Lee discloses an "etch-back process" to form the recess (i.e. groove) 147

that utilizes the entire width of the through hole and a recessed pad 150, e.g., of "doped polysilicon" (i.e. a fifth channel structure) that fills the groove:

FIG. 8



Lee, Fig. 8, [0093]-[0094] ("Referring to FIG. 8, upper portions of the dielectric layer structure 129, the channel 135 and the first filling layer pattern 145 may be partially removed to form a recess 147, and then a pad 150 capping the recess 147 may be formed. In example embodiments, an upper portion of the multi-stacked structure may be removed by an etch-back process to form the recess 147."); Banerjee ¶ 453-54.

As §XI.A demonstrates, it would have been obvious to employ this recess etch to form a second groove in Costa such that it removes layers 250, 62, and

262 (such

that "a projection of the second groove on the substrate covers the projection of the second through hole on the substrate"). Banerjee ¶ 455. Application of this second groove to Costa results in the following structure:

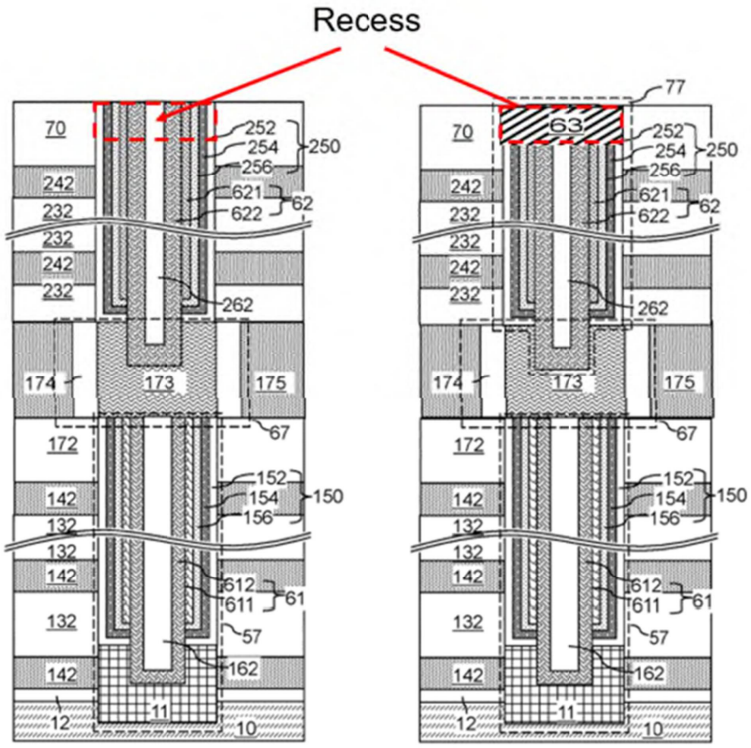


FIG. 21E FIG. 21F

Costa, Figs. 21E, 21F (annotated); Banerjee ¶ 456.

2. [10.B] "forming a fifth channel layer in the second groove, wherein the fifth channel layer is in contact with the fourth channel structure; and"

In view of Lee's teaching of forming the second groove through all the channel structure materials (i.e., as wide as the entire second through hole), it would have been obvious to form the fifth channel layer therein. Banerjee ¶

457-58. Lee, for example, discloses "[a] pad layer sufficiently filling the recess 147 may be

formed on the uppermost insulating interlayer 102j." Lee, [0094]. Similarly, Costa discloses forming the drain region in the recess. Costa, [0260]; Banerjee ¶¶ 459-60. This is necessary, because the conductive drain must electrically couple to the semiconductor layer 622 (and optional layer 621). Banerjee ¶ 461. Application of this second groove to Costa and resulting deposition of the conductive drain results in the following structure:

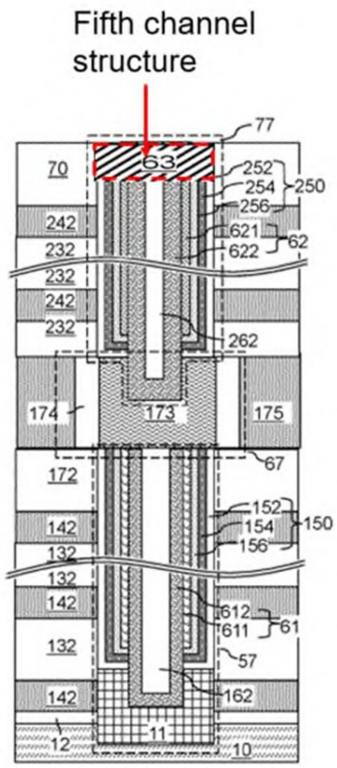


FIG. 21F

~~Costa,~~*Id.*, Figs. 21F (annotated); Banerjee ¶ ~~33~~462.

[10.C] "planarizing the top surfaces of the second insulating connection layer and the fifth channel layer to form the fifth channel structure."

In view of Lee's teaching of forming the second groove through all of the channel structure materials (i.e., as wide as the entire second through hole) and the teachings of Lee and Costa to fill that with a conductive drain, it would have been obvious to planarize the top surfaces of the second insulating connection layer and fifth channel structure. Banerjee ¶¶ 463-64. It was well known that the typical deposition of a conductive drain requires than planarizing the top surface because the deposition results in material above the target height. Banerjee ¶ 465. For example, Lee discloses that "[r]eferring to FIG. 8 … [a] pad layer sufficiently filling the recess 147 may be formed on the uppermost insulating interlayer 102j. An upper portion of the pad layer may be planarized until the top surface of the uppermost insulating interlayer 102j is exposed to obtain the pad 150…. The planarization process may include a CMP process." Lee, [0093]-[0094]; Banerjee ¶ 466. Similarly, Costa discloses "[e]xcess portions of the deposited semiconductor material can be removed from above the top surface of the insulating cap layer 70, for example, by chemical mechanical planarization (CMP)." Costa, [0212]; Banerjee ¶ 467. Thus, a POSITA would have understood that in view of Lee, this planarization would still be necessary to planarize the conductive drain

to the same level as insulating layer 70 and remove excess polysilicon above insulating layer 70

(on the fifth channel structure and insulating layer 70). Banerjee ¶ 468. Costa and Lee disclose planarization because it was well known that it was critical to form each layer in planar fashion, e.g., as the overlying metal layers require planar surfaces. *Id.*

XII. GROUND 3: INDEPENDENT CLAIM 20 IS OBVIOUS OVER COSTA IN VIEW OF TOYAMA

A. Motivation to Combine

A POSITA would have been motivated, with a reasonable expectation of success, to combine Costa with Toyama's through-array contact teachings for several reasons. Banerjee ¶¶ 471-72.

To start, Costa's focus is on the memory and staircase region, as Costa only mentions the peripheral devices once. Costa, [0124]; Banerjee ¶ 473. As was well known, however, memory devices require supporting logic, i.e., logic devices (typically CMOS) that control access to support memory operations. Banerjee,

¶ 474. Toyama depicts a well-known architecture, known as CMOS under the array, that provides for CMOS devices under the memory array.

~~2. [9.D] "removing a portion of the fourth channel layer to form the fourth channel structure, wherein a top surface of the fourth channel structure is lower than a top surface of the second insulating connection layer."~~

~~As discussed in [1.J], Costa describes removing the horizontal portions of second inner semiconductor channel layer 622 located above second-tier insulating cap layer 70. Costa, [0276]. And, as discussed in [1.K] above, dielectric core 162 is recess etched "below the top surface of the insulating cap layer 70," creating a groove in which drain region 63 is deposited. Costa, [0277], Fig. 21F; Banerjee~~

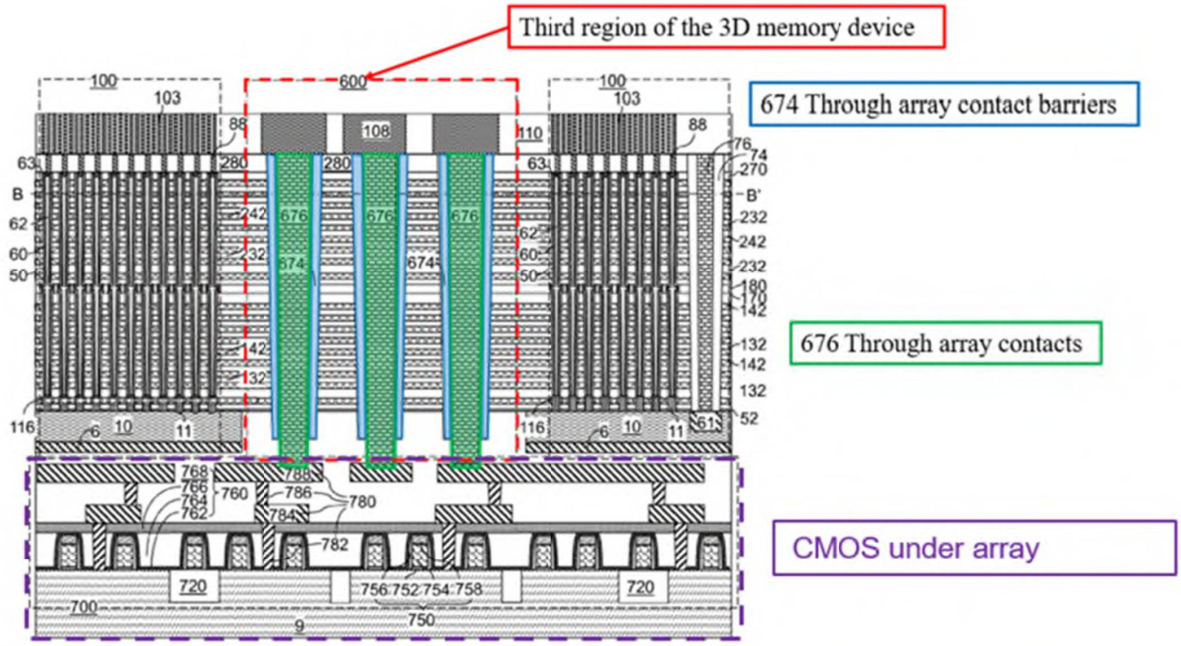


FIG. 49

Toyama (annotated), Fig. 49; Banerjee ¶ 475.

Toyama recognizes that placing devices outside the stack, i.e., on the peripheral area, unnecessarily takes up significant space: "As three-dimensional memory devices scale to smaller device dimensions, the

device area for peripheral devices can take up a significant portion of the total chip area. Thus, a method of providing various peripheral devices, such as word line driver circuits, without significantly increasing the total chip size is desired." Toyama, [0003]; Banerjee

¶ 476. Accordingly, Toyama teaches a "through-memory-level via region comprises through-memory-level via structures that vertically extend at least from a first horizontal plane including a topmost surface of the memory-level assembly to a second horizontal plane including a bottommost surface of the memory-level

assembly." Toyama, [0005]; Banerjee ¶ 477. As shown in Figure 49A above, these through-memory level via structures (676) are contacts (with insulating spacers) that extend through the stack, thereby enabling the placement of CMOS under the array. Banerjee, ¶ 478. This accomplishes Toyama's goal of saving footprint. *Id.* ¶¶ 478- 79.

Next, the placement of circuitry under the array brings the supporting logic closer to the array. Toyama describes one benefit of this, namely, "an efficient power distribution network in the array of memory stack structures [that] can increase performance of three-dimensional memory devices." Toyama, [0003]; Banerjee ¶ 480-81. A POSITA also understood that this placement decreases the distance between various metal layer connections

because, for example, certain connections are on top of the memory stack, e.g., to the wordlines. Thus, wordline drivers, which are now under the array, require shorter lateral connections to the wordlines. Banerjee, ¶ 482.

A POSITA would have had a reasonable expectation of success in implementing Toyama's CMOS under-array logic with through-array contacts (and the corresponding barrier layers). Banerjee ¶ 483. To start, CMOS under the array was textbook material before the '291 Patent's assumed effective filing date. Banerjee ¶ 484-85; Ex. 1013, 175 ("Because the entire stack is built above the silicon, the area under the array is used for circuits, thus saving silicon area and

improving bit density. There are 4 metal layers: 2 at the bottom for connecting CMOS circuits underneath the array, and two at the top, one for bitline and one for power and global interconnects, respectively."), 180 (citing "K. Parat, C. Dennison, A floating gate based 3D NAND technology with CMOS under array in Conference on International Electron Devices Meeting (IEDM), San Francisco (USA), Dec 2015."). Next, Costa already discloses etching through the stack, e.g., for the memory structures and staircase support pillar contacts. *E.g.*, Costa, Fig. 3B. Indeed, Costa already discloses creating a contact, along with a barrier layer, through the stack. *Id.*, Costa, [0229]-[0231], Fig. 16B (insulating spacer 74 and contact via structure 76).

Such etches and conformal deposition of a space were textbook material. Banerjee, ¶ 486-87. And as Toyama demonstrates, a multi-deck stack was fully compatible with a CMOS under the array design. Toyama, Fig. 49, [0016] (first tier), [0055] (second tier); Banerjee ¶ 488. Thus, a POSITA would have had a high expectation of success in implementing a CMOS under the array design that includes a third region for the through-array contact barriers in Costa. Banerjee,

¶ **~~335-37~~483**.

~~H~~B. Claim ~~11~~20:

1. [~~11~~20.PRE] "A joint opening structure of a three-dimensional (3D) memory device, comprising:"

This limitation is substantively identical to [1.PRE] and Costa discloses it for the same reasons (claim 1 **~~recites~~is** a method for forming the same).

2. [~~11~~20.A] "a first stacked layer disposed overlaying a substrate;"

This limitation is present in [1.A] and Costa discloses it for the same reasons.

3. [~~11~~20.B] "a first insulating connection layer disposed on the first stacked layer;"

This limitation is present in [1.A] and Costa discloses it for the same reasons.

4. [20.C] "a second stacked layer disposed on the first insulating connection layer;"

This limitation is present in [1.G] and Costa discloses it for the same reasons.

5. [20.D] "a second insulating connection layer disposed on the second stacked layer;"

This limitation is present in [1.G] and Costa discloses it for the same reasons.

6. [20.E] "a plurality of channel holes in a first region of the 3D memory device;"

Costa discloses a plurality of channel holes in a first region (memory array region 100) of the 3D memory device. Costa, [0124], Figs. 3A-B, 10A-B; Banerjee ¶¶ 494-95. As discussed in [1.A]-[1.K], Costa discloses forming a plurality of first- tier memory openings 149 and second-tier memory openings 249 in memory array region 100, which are subsequently filled to form an active memory channel. *See* §X.A; Costa, [0135], [0161], [0190]; Banerjee ¶ 496.

7. [20.F] "a plurality of staircase structure dummy holes in

a second region of the 3D memory device; and"

Costa discloses a plurality of staircase structure dummy holes in a second region (contact region 200) of the 3D memory device. Costa, [0124], Figs. 3A-B,

10A-B (staircase region 200); Banerjee ¶¶ 497-98. Specifically, Costa discloses forming first-tier support openings 119 and second-tier support openings 219 in contact region 200. Costa, [0137], [0190], Figs. 3A-B, 10A-B; Banerjee ¶ 499. Support openings 119 and 219 are subsequently filled to form support fill structures 17 and 27. Costa, [0160], [0177]. These support members support the memory stack during the gate replacement process. *Id.*, [0226]. The holes therefore are "dummy" holes because the structures are dummy structures, that is, they perform no function, such as being a functional contact, and instead are merely support members. *Id.*; Banerjee ¶ 500-01; *see* Ex. 1001, 26:2-4 ("The plurality of staircase structure dummy holes in the second region can have a supporting function of the staircase structure.").

8. [20.G] "a plurality of through array contact barriers in a third region of the 3D memory device;"

Costa does not disclose or otherwise discuss through array contacts. Banerjee

¶¶ 502-03; *see generally* Costa.

Toyama discloses a plurality of through array contact barriers

("insulating liners 674") in a third region of the 3D memory device ("through-memory-level via regions 600"), as shown in Figure 49 below. Toyama, [0333], Figs. 45A, 48A, 49.

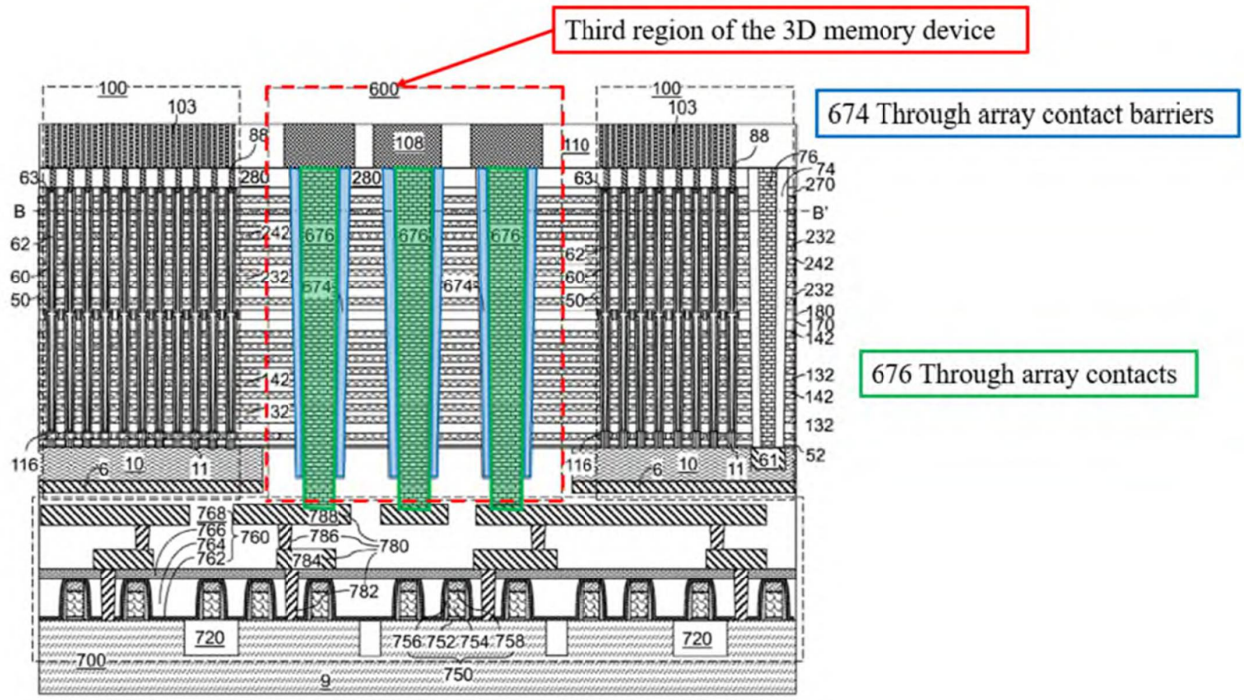


FIG. 49

Toyama, Fig. 49 (annotated); Banerjee ¶ 504. Toyama forms "insulating liners 674" by depositing "a conformal insulating material layer" in "through-memory-level openings 679." [8] Toyama, [0338]-[0340], [0233] ("[a]n insulating spacer 74 including a dielectric material"), [0381] ("insulating liner 674 having a same material composition and a same thickness as the insulating spacer 74"); Banerjee

¶ 505. The remaining portion of through-memory-level opening 679 is filled with

---

[8] Although paragraph 338 of Toyama refers to "through-memory-level openings 689," that appears to be a typographical error. All relevant figures

(*e.g.*, Figs. 47A- B to 49) and other textual descriptions refer to the elements as "through-memory- level openings 679," *see, e.g.*, Toyama, [0339]-[0341]; Banerjee, ¶ 506.

"at least one conductive material" to form "through-memory-level via structure 676." Toyama, [0341]-[0342]; Banerjee ¶ 507. A POSITA would have understood these conductive through-memory-level via structures 676 to constitute through array contacts. Banerjee ¶ 508. Thus, insulating liners 674 form dielectric barriers between the through array contacts in a third region of the 3D memory device. *Id.*

¶ 509.

~~4~~9. [~~11~~20.~~C~~H] "wherein each of the plurality of channel holes includes: a first through hole penetrating the first stacked layer and the first insulating connection layer~~;~~,"

This limitation is present in [1.B] and Costa discloses it for the same reasons.

~~5~~10. [~~11~~20.~~D~~I] "a first channel structure disposed at the bottom of the first through hole and overlaying the substrate~~;~~,"

This limitation is substantively the same as [1.C] (but recites "disposed at the bottom of the first through hole"), and Costa discloses it for the same reasons.~~-~~

~~**Banerjee ¶ 343.**~~

~~6.~~ ~~[~~11.~~E~~ [20.J] "a first functional layer disposed on the sidewall of the first through hole~~;~~,"

This limitation is substantively the same as [1.D] (but recites "disposed on"

instead of "on"), and Costa discloses it for the same reasons.

~~7~~12. [~~11~~20.~~F~~K] "a second channel structure in contact with the first channel structure disposed on the sidewall of the first functional layer~~;~~,"

This limitation is present in [1.E] and Costa discloses it for the same reasons.~~-~~ ~~**As that analysis explains, Costa's second channel structure (vertical semiconductor channel) is in connect with Costa's first channel structure (epitaxial pedestal at bottom) and first functional layer ("first memory film 150" with or without the optional semiconductor channel layer 611). Banerjee ¶¶ 345-46.**~~

~~8~~13. [~~11~~20.~~G~~L] "a third channel structure in contact with the second channel structure disposed over the first through hole, wherein a projection of the third channel structure on the substrate covers a projection of the first through hole on the substrate~~;~~,"

This limitation is substantively the same as [1.F] (but recites "disposed over" instead of "form[ed]…above"), and Costa discloses it, or renders it obvious, for the same reasons.

~~9. [11.H] "a second stacked layer disposed on the third channel structure;"~~

~~This limitation is present in [1.G] and Costa discloses it for the same reasons.~~

~~10. [11.I] "a second insulating connection layer disposed on the second stacked layer;"~~

~~This limitation is present in [1.G] and Costa discloses it for the same reasons.~~

1~~1~~4. [~~11~~20.~~J~~M] "a second through hole penetrating the second stacked layer and the second insulating connection layer, wherein a projection of the second through hole on the substrate at least partially overlaps with the projection of the first through hole on the substrate~~;~~,"

This limitation is substantively the same as [1.H] and Costa discloses it, or renders it obvious, for the same reasons.

1~~2~~5. [~~11~~20.~~K~~N] "a second functional layer disposed on the sidewall of the second through hole~~;~~,"

This limitation is substantively the same as [1.I] (but recites "disposed on" instead of "on"), and Costa discloses it, or renders it obvious, for the same reasons.

1~~3~~6. [~~11~~20.~~L~~O] "a fourth channel structure in contact with the third channel structure disposed on the sidewall of the

second functional layer~~;~~, and"

This limitation is present in [1.J] and Costa discloses it for the same reasons.

147. [~~11~~20.~~M~~P] "a fifth channel structure in contact with the fourth channel structure disposed over the second through hole."

This limitation is substantively the same as [1.K] (but recites "disposed over" instead of "form[ed]…above"), and Costa discloses it, or renders it obvious, for the same reasons.

~~**I. Claim 12:**~~

~~**1. [12.PRE] "The joint opening structure of claim 11, further comprising:" [12.A] "a first filling structure covering the surface of the second channel structure; and"**~~

~~**This limitation is present in [1.E] and Costa discloses it for the same reasons.**~~

~~**2. [12.B] "a second filling structure covering the surface of the fourth channel structure;"**~~

~~**This limitation is present in [1.J] and Costa discloses it for the same reasons.**~~

~~**3. [12.C] "wherein the first through hole is non-interconnected with the second through hole."**~~

~~**Costa discloses this limitation. Banerjee ¶ 357.**~~

~~**For example, when forming second-tier memory openings 249, Costa teaches that "second-tier memory openings 249 are formed through the second tier structure (232, 242, 70, 265) in areas that overlap with the joint-level memory opening fill structures 67, i.e., with the joint-level memory openings." Costa, [0191]; Figs. 10A- 10B, 21A;**~~

~~**Banerjee ¶ 358-59; *see also* Costa, [0272] ("FIG. 21A illustrate a region of the second exemplary structure at the processing steps of FIGS. 10A and 10B, i.e., after formation of the second-tier memory openings 249…."). As illustrated in Fig. 21F, a POSITA would have understood that Costa discloses that first-tier memory openings (filled in Fig. 21F with first memory opening fill structures 57) are non-interconnected with second-tier memory openings 249 (filled in Fig. 21F with second memory open opening fill structures 77) because joint-level doped semiconductor portions 173 are interposed between the first-tier and second-tier memory openings:**~~

~~***Id.*, Fig. 21F (annotated); Banerjee ¶ 360.**~~

~~**J. Claim 14:**~~

~~**1. [14.PRE] "The joint opening structure of claim 11, wherein:" [14.A] "the first stacked layer includes a first number of conductor/dielectric layer pairs; and" [14.B] "the second stacked layer includes a second number of conductor/dielectric layer pairs."**~~

~~**These limitations are identical to [2.A-B] and met for the same reasons.**~~

~~**K. Claim 15:**~~

~~**1. [15] "The joint opening structure of claim 14, wherein: the first number and the second number are not less than 32."**~~

~~**This limitation is identical to [3] and met for the same reasons.**~~

~~**L. Claim 16:**~~

~~1. [16.PRE]-[16.B] "The joint opening structure of claim 11, wherein: the first stacked layer includes a first number of oxide/nitride layer pairs; and the second stacked layer includes a second number of oxide/nitride layer pairs.~~

~~These limitations are identical to claim [2.A-B] and met for the same reasons.~~

~~M. Claim 17:~~

~~1. [17] "The joint opening structure of claim 16, wherein: the first number and the second number are not less than 32."~~

~~This claim is identical to claim [3] and met forth the same reasons.~~

~~N. Claim 18:~~

~~1. [18] "The joint opening structure of claim 11, wherein: a thickness of the third channel structure is in a range between 30 nm and 70 nm."~~

~~Costa discloses this limitation. Banerjee ¶ 370.~~

~~Specifically, Costa disclose that "[t]he thickness of the first joint-level doped semiconductor layer 173L can be in a range from 20 nm to 100 nm, although lesser and greater thicknesses can also be employed." Costa, [0163]. Thus, Costa discloses the full range of claim 18. Costa's range accounts for the fact that Costa discloses the elements of stacks also have ranges, and the ranges simply reflect that a different process generation may fabricate the device. *E.g.*, *id.*, [0139], [0146]-[0147], [0150], [0182]; Banerjee ¶ 371-72. The '291 Patent similarly discloses ranges for various layers. *E.g.*, Ex. 1001, 9:38-44; *see also* Banerjee ¶~~

~~373.~~

~~O. Claim 19:~~

~~1. [19.PRE] "The joint opening structure of claim 11, wherein:" [19.A] "a size difference between a top aperture and a bottom aperture of the first through hole is equal to or less than 30 nm; and"~~

~~Costa discloses this limitation. Banerjee ¶ 375.~~

~~Costa discloses that "[t]he lateral dimensions (e.g., a diameter) of the first-tier openings (149, 119) can be from about 20 nm to 200 nm at an upper portion of each first-tier opening (149, 119), and can be about 10 nm to 150 nm at a lower portion of each first-tier opening (149, 119)." Costa, [0139]; Banerjee ¶ 376. Thus, a POSITA would have understood that a size difference between the top and bottom "aperture" of first-tier memory opening 149 can be less than or equal to 30 nm, e.g., taking the two lower ranges, the size difference in Costa would be 10nm. Banerjee ¶ 377-80 (explaining that tapering creates this difference).~~

~~2. [19.B] "a size difference between a top aperture and a bottom aperture of the second through hole is equal to or less than 30 nm."~~

~~Costa discloses this limitation. Banerjee ¶ 381.~~

~~Costa teaches the same difference for the second through hole. Costa, [0194]; Banerjee ¶ 382. Thus, a POSITA would have understood that a size difference between the top and bottom "aperture" of second-tier memory opening 249 can be less than or equal to 30 nm, e.g., taking the two lower ranges, the size difference in Costa would be 10nm.~~

~~**Banerjee ¶ 383.**~~

XI~~I~~II. SECONDARY CONSIDERATIONS

Petitioner is unaware of any applicable secondary considerations of nonobviousness. ~~***See* generally Ex. 1002**~~**Even if such considerations existed, none would overcome the strong *prima facie* showing of obviousness**.

XI~~I~~IV. CONCLUSION

Petitioner respectfully requests that the Board enter a final written decision finding the Challenged Claims unpatentable.

Respectfully submitted,

Dated: December 13, 2024 ORRICK, HERRINGTON & SUTCLIFFE LLP

By: */Jeremy Jason Lang/*
Jeremy Jason Lang
Lead Counsel for Petitioner
Reg. No. 73,064
1000 Marsh Road
Menlo Park, CA 94025-1015
T: (650) 614-7400
F: (650) 614-7401
Email: PTABDocketJJL2@orrick.com

Attorneys for Petitioner Micron Technology, Inc.

CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system's word count, the petition— excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 13,~~5~~92~~1~~8 words.

Dated: December 13, 2024

By: */Jeremy Jason Lang/*

Jeremy Jason Lang
Lead Counsel for Petitioner
Reg. No. 73,064
1000 Marsh Road
Menlo Park, CA 94025-1015
T: (650) 614-7400
F: (650) 614-7401
Email: PTABDocketJJL2@orrick.com

Attorney for Petitioner Micron Technology, Inc..

CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Petition for *Inter Partes* Review and associated documents and exhibits were caused to be served on December 13, 2024 via overnight courier upon the following counsel of record for Patent Owner:

34431 - HANLEY, FLIGHT & ZIMMERMAN, LLC
10 S. WACKER DRIVE
SUITE 3500
CHICAGO, IL 60606
UNITED STATES

Copies of this Petition and accompanying documents and exhibits were also served via electronic mail on Patent Owner's counsel of record for related PTAB proceedings and in the related district court litigation – ROPES & GRAY LLP and LATHAW & WATKINS LLP:

Alexander E Middleton (alexander.middleton@ropesgray.com)
Allen S. Cross (allen.cross@ropesgray.com)
Hyun-Joong Kim (daniel.kim@ropesgray.com)
James R. Batchelder (james.batchelder@ropesgray.com)
James F. Mack (james.mack@ropesgray.com)
Nancy Attalla (nancy.attalla@ropesgray.com)
Rachael Bacha (rachael.bacha@ropesgray.com)
Stepan Starchenko (stepan.starchenko@ropesgray.com)
Andrew T. Radsch (andrew.radsch@ropesgray.com)
James L. Davis (James.L.Davis@ropesgray.com)
Christopher M. Bonny (Christopher.Bonny@ropesgray.com)
Nicole Pobre (nicole.pobre@ropesgray.com)
YMTC-Micron-IPRs-Ropes-Service@ropesgray.com

Benjamin J. Behrendt (benjamin.behrendt@lw.com)
Brenda L. Danek (brenda.danek@lw.com)
Brent Thomas Watson
(thomas.watson@lw.com) Brett M. Sandford

(brett.sandford@lw.com) Clement Naples
(clement.naples@lw.com) Elliott Greb
(elliott.greb@lw.com)
Kevin Wheeler (kevin.wheeler@lw.com)
Thomas Yeh (thomas.yeh@lw.com)
Richard A. Lowry (richard.lowry@lw.com)
Inge A. Osman (inge.osman@lw.com)
Steven W. Peters (steven.peters@lw.com)

/*Karen Johnson*/
Karen Johnson

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