

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION, LENOVO (UNITED STATES) INC., MOTOROLA
MOBILITY LLC,
Petitioners,

v.

COLLISION COMMUNICATIONS, INC.,
Patent Owner.

Case No. IPR2025-00303
U.S. Patent No. 7,463,703

**PATENT OWNER'S PRELIMINARY RESPONSE
PURSUANT TO 37 C.F.R. § 42.107(a)**

TABLE OF CONTENTS

	Page
I. Introduction.....	1
II. Wireless Communication Background.....	4
A. Material Differences between Coded Systems and Uncoded Systems.....	5
1. Uncoded Systems.....	6
2. Coded Systems.....	9
B. Soft Data Bit versus Hard Data Bit Decisions in Uncoded Systems.....	16
C. Successive Interference Cancellation vs. Parallel Interference Cancellation.....	18
III. The '703 Patent's Bank of Decoders with Feedback to a Joint Amplitude Estimator.....	21
A. Exemplary Architecture	22
A. The Challenged Claims	29
IV. The Petition and Deficiencies of the Asserted References.....	30
A. Grounds 1-3.....	31
1. <i>Brommer</i> is not § 102(e) Prior Art Because <i>Brommer</i> was Owned by BAE and the '703 Patent Inventor Was "Subject to an Obligation of Assignment" to BAE	31
2. None of the Asserted References for Ground 1 Concerns or Describes a Joint Amplitude Estimator, Much less a Bank of Decoders that Provides Feed Back to the Joint Amplitude Estimator	34
B. Grounds 4-5.....	37

1.	Neither <i>Frank</i> nor <i>Zha</i> Concern or Describe “a bank of decoders that produce symbol likelihood estimates for each user, wherein said symbol likelihood estimates are iteratively fed back to said symbol estimator and said joint amplitude estimator until a final condition is obtained”	37
V.	The Petition Should be Denied Because Each Asserted Ground Fails to Establish the Required Likelihood of Success	41
A.	Grounds 1-3.....	41
1.	<i>Brommer</i> is Not Prior Art	41
2.	The Petition fails to show that the combination of <i>Brommer</i> , <i>Lillieberg</i> , and <i>Hottinen</i> describe “a bank of decoders... producing a plurality of symbol likelihood estimates for each user, wherein said symbol likelihood estimates are iteratively fed back to said symbol estimator and said joint amplitude estimator” as required by claim 1.....	42
B.	Grounds 4-5.....	47
1.	The Petition admits that <i>Frank</i> does not disclose a bank of decoders and there is no evidence that a bank of decoders exists in <i>Zha</i>	47
2.	The Petition Provides No Explanation of <u>How</u> or <u>Why</u> One Would Combine <i>Zha</i> with <i>Frank</i> to Result in Claimed “Bank of Decoders”	49
3.	The Petition Provides No Explanation of <u>How</u> or <u>Why</u> One Would Combine <i>Zha</i> ’s Successive Interference Cancellation with <i>Frank</i> ’s Parallel Interference Cancellation	51
VI.	The <i>Fintiv</i> Factors Heavily Favor Discretionary Denial Of Institution Under § 314(A).....	54
A.	Factor 1: Whether a stay exists or is likely to be granted if a proceeding is instituted.....	54

B.	Factor 2: Proximity of the court’s trial date to the Board’s projected statutory deadline	55
C.	Factor 3: Investment in the parallel proceeding by the court and parties	57
D.	Factor 4: Overlap between issues raised in the petition and in the parallel proceeding	58
E.	Factor 5: Whether the petitioner and the defendant in the parallel proceeding are the same party.....	59
F.	Factor 6: Other circumstances that impact the Board’s exercise of discretion, including the merits / Compelling Merits	60
VII.	Conclusion	60

TABLE OF AUTHORITIES

	Page(s)
Federal Cases	
<i>Apple Inc. v. Fintiv, Inc.</i> , IPR2020- 00019, Paper 11 (PTAB Mar. 20, 2020).....	<i>passim</i>
<i>Comcast Cable Communications, LLC v. Touchstream Technologies, Inc.</i> , IPR2024-00324, Paper 13 (PTAB July 24, 2024).....	56, 58, 60
<i>Corning Inc. v. DSM IP Assets B.V.</i> , IPR2013-00053, Paper 66 (P.T.A.B. May 1, 2014)	34
<i>Limelight Networks, Inc., v. Akamai Techs., Inc.</i> , IPR2017-00349, Paper 7 (P.T.A.B. May 30, 2017)	34
<i>Sotera Wireless, Inc. v. Masimo Corp.</i> , IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020)	60
<i>Verizon Bus. Network Servs. LLC v. Huawei Techs. Co. Ltd.</i> , IPR2020-01292, Paper 13 (PTAB Jan. 25, 2021)	57
Regulations	
37 C.F.R. § 42.24(d)	62

TABLE OF EXHIBITS

Exhibit	Description
2001	Declaration of Dr. Giuseppe Caire
2002	CV of Dr. Giuseppe Caire
2003	U. Madhow, <i>Fundamentals of Digital Communication</i> , Cambridge University Press 2008
2004	R.G. Gallager, <i>Principles of Digital Communication</i> , Cambridge University Press 2008
2005	A. Goldsmith, <i>Wireless Communications</i> , Cambridge University Press 2005
2006	RESERVED
2007	Judge Rodney Gilstrap Motion to Stay Pending IPR Statistics
2008	June 30, 2024 Federal District Court Case Management Statistics
2009	Docket in <i>Collision Communications, Inc. v. Lenovo Group Ltd.</i> , No. 23-cv-00594 (E.D. Tex.)
2010	Scheduling Order in <i>Collision Communications, Inc. v. Lenovo Group Ltd.</i> , No. 23-cv-00594 (E.D. Tex.), Dkt. 44 (Aug. 5, 2024)
2011	USPTO Assignment Record, Reel/Frame: 013147/0391
2012	USPTO Assignment Record, Reel/Frame: 015999/0544
2013	Provisional Patent Application No. 60/462,657
2014	McElwain Employee Proprietary Information and Innovation Agreement dated September 16, 1996 (EPIIA)
2015	History of BAE Systems North America
2016	BAE SYSTEMS North America to Acquire Business from Lockheed Martin
2017	Declaration of Dr. Giuseppe Caire

This Petition is a copycat petition seeking to join the pending Petition in IPR2024-01500, for which PTAB has not yet issued an institution decision.¹ This Petition is substantively identical to that -01500 Petition, and it should be denied for the same reasons set forth in Patent Owner’s Preliminary Response to the -01500 Petition.

Accordingly, the following Preliminary Response is substantively identical to Patent Owner’s -01500 Preliminary Response and repeats all of those reasons for denial. In addition, Patent Owner has updated the following *Fintiv* section to address the present petitioners and align with the recission of the June 21, 2022, Director’s Memorandum entitled “Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation” (“Guidance Memo”).

I. Introduction

The Board should deny institution because (1) the Petition’s Grounds 1-5 do not establish the required reasonable likelihood of success; and (2) the ongoing proceedings establish that institution should be discretionally denied under *Fintiv*.

¹ Patent Owner has retained Giuseppe Caire, Ph.D. in this proceeding. (EX2017). Dr. Caire has adopted his prior opinions set forth in EX2001 (submitted in IPR2024-01500) and, for expediency, this Patent Owner Preliminary Response cites to Dr. Caire’s previously submitted declaration, also presented herein as EX2001.

Lack of Reasonable Likelihood of Success: The '703 Patent only has one independent claim: the apparatus of claim 1, which requires a bank of decoders for processing digital data that feedbacks data to other components in the apparatus, including a joint amplitude estimator.

But *none* of the asserted references describe or suggest a “bank of decoders” that feeds back data to a joint amplitude estimator.

Preliminarily, regarding Grounds 1-3, the Petition does not even rely on prior art. The primary reference for each of Grounds 1-3 is *Brommer*. But *Brommer* is not prior art under 35 U.S.C. § 103(c) due to *Brommer* and the '703 Patent being commonly owned by (or the inventors were under an obligation to assign to) BAE. Such facts are clear from the prosecution history and public assignment records, yet the Petitioners did not recognize this fundamental defect in Grounds 1-3. Moreover, submitted with this Patent Owner Preliminary Reply is a copy of the inventor employee agreement evidencing the obligation to assign. That *Brommer* is not prior art is fatal to grounds 1-3.

Even if *Brommer* was considered to be prior art, *Brommer* does not provide any element capable of providing feedback from a bank of decoders to anything the Petition alleges could be a joint amplitude estimator. *Brommer* fails to describe any iterations, looping, or other type of feedback from the bank of decoders to any alleged joint amplitude estimator. Rather, the Petition relies on *Lilleberg* and

Hottinen to describe a joint amplitude estimator. But the Petition fails to identify any “bank of decoders” in *Brommer* producing a plurality of symbol likelihood estimates for each user, wherein said symbol likelihood estimates are iteratively fed back to said symbol estimator and said joint amplitude estimator. Moreover, the Petition does not assert that *Lilleberg* describes a “bank of decoders” and, indeed, it does not.

The Petition fares worse for Grounds 4-5 as *Frank* and *Zha* do not describe a bank of decoders, much less any feedback mechanism or structure from the bank of decoders. Rather, the Petition simply points to a “data bit decision” made by a decision rule in *Zha* and assumes this describes a “bank of decoders”. (Pet. at 60). It does not. Any reasonable understanding of a “bank of decoders” requires an error correction coding technique in which additional redundancies are introduced into the sequence of bits at a transmitter end. The additional redundancies in the sequence of bits are utilized by the decoder at the receiver end for error identification and correction. But contrary to the Petition’s unexplained assumption, there is no use of error correction coding in *Zha* and therefore no decoder, let alone a “bank of decoders” feeding back any information.

For any and all of these reasons, the Petition fails to show the required reasonable likelihood of success under any asserted Ground, and the Petition should be denied.

Discretionary Fintiv Denial: The *Fintiv* factors heavily weigh in favor of discretionary denial. In an attempt to characterize every factor as either neutral or favoring institution, the Petition is rife with conclusory statements and misapplications of controlling PTAB precedent. Under the appropriate legal standards—and considering the totality of the record evidence—on balance, the *Fintiv* factors support discretionary denial of institution.

II. Wireless Communication Background

The challenged claims generally concern wireless communication systems with multiple signals. More specifically, the claims are directed to an improved apparatus that applies a bank of decoders to produce a plurality of symbol likelihood estimates for each user. Once symbol likelihood estimates are produced, the symbol likelihood estimates are fed back to the symbol estimator and a joint amplitude estimator until a final condition is reached.

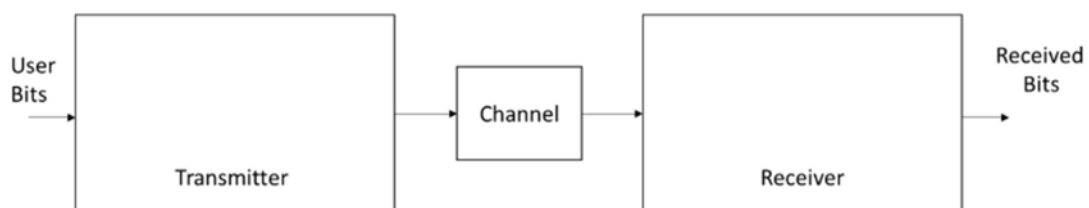
To provide context for the claimed subject matter and the Petition, the following brief background addresses the following topics:

- uncoded systems vs. coded systems;
- soft bit decisions vs. hard bit decisions; and
- successive interference cancellation vs. parallel interference cancellation.

A. Material Differences between Coded Systems and Uncoded Systems

A typical wireless transmission generally involves a transmitter and receiver at opposite ends of a wireless channel. An original signal is input at the transmitter and a recovered signal is calculated at the receiver.

As illustrated in the simplified figure below, an original information signal in the form of user bits (sequences of 0s and 1s) is input to the transmitter. The transmitter converts those bits into an analog carrier waveform and then transmits that carrier waveform over the wireless channel to the receiver. (EX2001 at ¶17; EX2003 at 2-4; EX2004 at 1-5, 95, 181-183, 208-209). The receiver receives the waveform and attempts to recover the original signal by converting the received waveform into received bits. (EX2001 at ¶17; EX2003 at 2-4; EX2004 at 3-5).



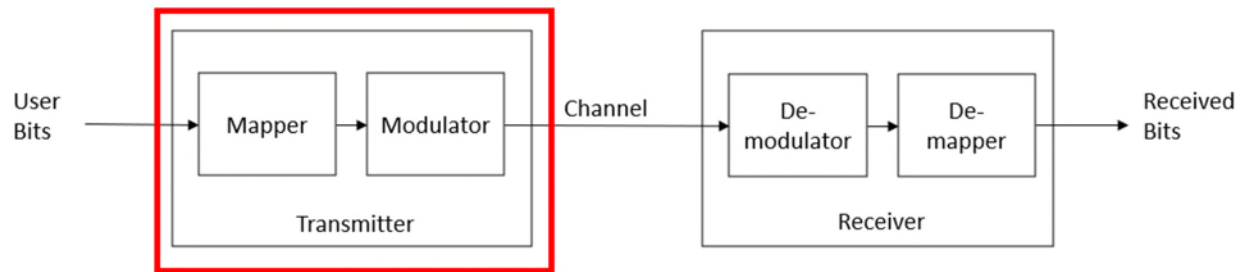
(EX2001 at ¶17, based on FIG. 1.1 of EX2003).

There are two classes of wireless transmission systems: uncoded systems and coded systems.

1. Uncoded Systems

An uncoded system transmits data without use of error correction coding. In an uncoded system, a transmitter includes a *mapper* that maps user bits to different symbols. (EX2001 at ¶18; EX2003 at 2-3, 7, 45-46, 107). As illustrated below, in a digital communication system, the transmitter typically includes this mapper along with a modulator. (EX2001 at ¶18; EX2003 at 2-3, 107; EX2004 at 3-5).

Uncoded System



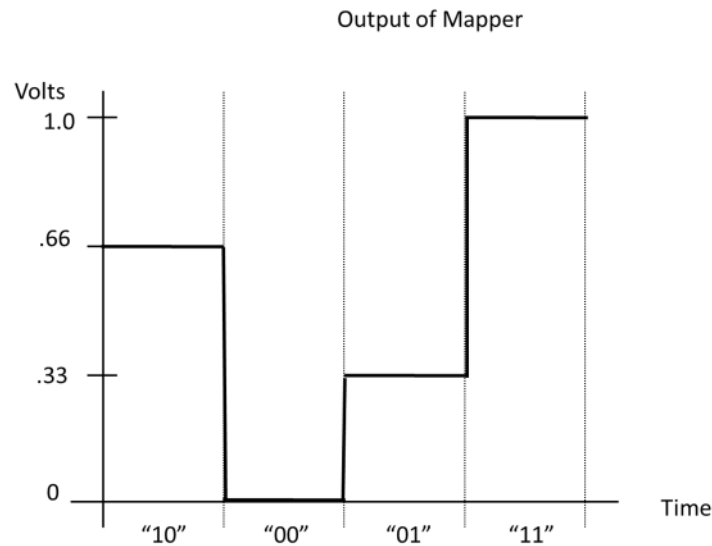
(EX2001 at ¶18; Based on FIG. 1.1 of EX2003).

The user bits are input to the *mapper*, which maps the user bits to symbols. (EX2001 at ¶19; EX2003 at 7; EX2004 at 181-209). For example, to send a user bit sequence of “10000111”, the mapper would take each 2-bit sequence, and map it to its corresponding symbol. Using a bit-and-symbol correlation identified below, the sequence “10000111” would be broken into its composite bit sequences 10, 00, 01, and 11, which would be mapped to the voltages .66, 0.0, .33, and 1.0 respectively.

2-Bit Sequence	Symbol
----------------	--------

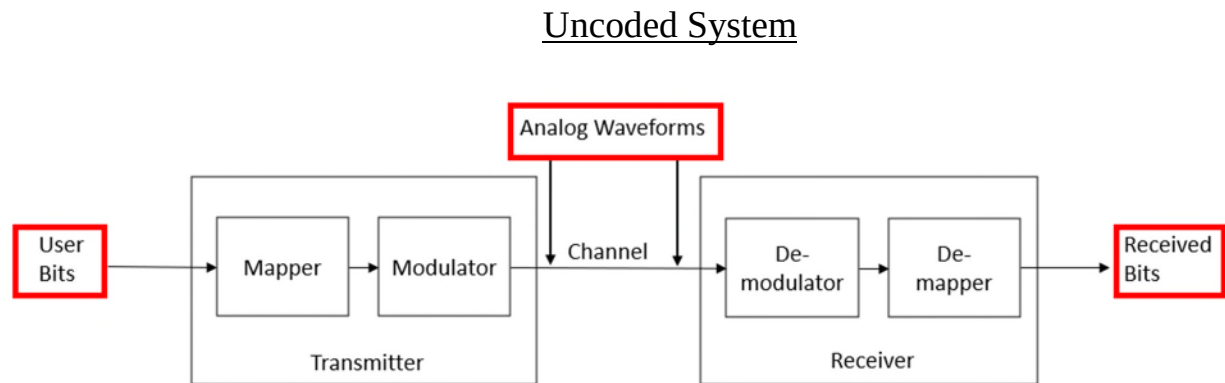
	(Waveform Amplitude)
“00”	0
“01”	.33
“10”	.66
“11”	1.0

The resulting output of the example mapper is the sequence 0.66, 0.0, 0.33, and 1.0 shown in the following figure, in which the y-axis represents voltage and the x-axis represents time. (EX2001 at ¶20). For reference, the transmitted bit sequence is shown for each time slot below the figure.



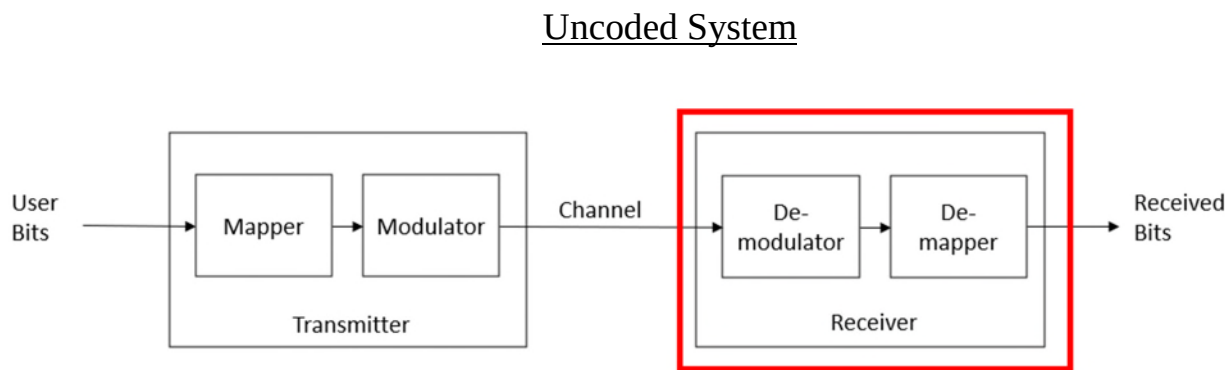
Next, the mapper provides these symbols to the transmitter’s *modulator*, which creates a waveform to be modulated to reflect the symbol values provided by the mapper and then be sent through the channel. (EX2001 at ¶21; EX2004 at 3, EX2004 at 6-7). There are numerous different ways for a modulator to apply such

information to a carrier waveform. (EX2001 at ¶21; EX2003 at 2-3; EX2004 at 181-209). For example, in our illustration, the modulator can modify (modulate) the amplitude of the carrier waveform so that the waveform’s different amplitudes will match the mapped symbols output by the mapper.



(EX2001 at ¶21; Based on FIG. 1.1 of EX2003).

The receiver in the uncoded system typically mirrors the transmitter and includes: a de-modulator and a demapper.



(EX2001 at ¶22; Based on FIG. 1.1 of EX2003).

The **demodulator** receives the modulated waveform via the channel and attempts to extract the waveform's symbol values (in our example, amplitude). (EX2001 at ¶23; EX2003 at 3-4; EX2004 at 4-7).

The extracted symbol values are then input to the **demapper**, which is used to help identify which bit sequence may correspond to the extracted symbol values. (EX2001 at ¶24; EX2003 at 3-4, 43-46; EX2004 at 4-7). But because of noise in the transmission, the demodulated symbol values signal may not be identical to the symbol values output from the demapper. (EX2001 at ¶24; EX2003 at 43-46). The demapper has two types of decision rules for handling variations in the symbol values: hard decisions and soft decisions (discussed more below). The hard decisions and soft decisions determine symbol estimates of the recovered user bits.

2. Coded Systems

A coded system is one that incorporates error correction coding to identify and correct errors introduced during transmission. (EX2001 at ¶25; EX2003 at 3; EX2005 at 228).

Error correction coding is a technique used for controlling errors in data transmissions over unreliable or noisy channels. (EX2001 at ¶26; EX2003 at 293; EX2005 at 228-229). The approach includes the transmitter taking the sequence of user bits that are input to the transmitter and encoding (e.g., modifying) the sequence to add redundancy, which increases the number of bits that are

transmitted from the transmitter to the receiver. (EX2001 at ¶26; EX2003 at 2-3, 293; EX2004 at 11; EX2005 at 229-231). The receiver takes the received signal, which includes the longer sequence of bits having redundancy, and decodes the signal to output the shorter sequence of bits representing the original user bits. (EX2001 at ¶26; EX2003 at 2-3, 293; EX2004 at 11; EX2005 at 228-229). Using error correction coding, the decoding process can identify, and in some cases correct, any bits that were corrupted during transmission due to noise. (EX2001 at ¶26; EX2003 at 293; EX2004 at 11; EX2005 at 228-229). By implementing error correction coding, increased system performance can be achieved. (EX2001 at ¶26; EX2003 at 3; EX2004 at 11; EX2005 at 228).

Consider the following simple example to illustrate the concept of error correction coding. Assuming a transmitter receives a sequence of 3 user bits: “010”. The example transmitter encodes the sequence by introducing 2 additional redundant bits for each user bit. (EX2001 at ¶27; EX2004 at 11). This simplified example includes repeating each input user bit such as encoding “010” to “000111000”. (EX2001 at ¶27; EX2004 at 11). This encoding (modification) triples the length of the user bit sequence that is transmitted from 3 user bits to 9 user bits. (EX2001 at ¶27; EX2004 at 11). Such an approach would be considered to have a code rate of 1/3 (indicating for every 1 bit input, 3 bits are output). (EX2001 at ¶27; EX2004 at 11; EX2005 at 228-229).

Continuing the simple example, the transmitter will modulate and transmit the longer encoded bit sequence (“000111000”) through the channel to the receiver. (EX2001 at ¶28; EX2004 at 11). After demodulation by the receiver, and because of noise introduced during transmission, the received bit sequence may not match the transmitted bit sequence. (EX2001 at ¶28; EX2004 at 11). For the purposes of the example, assume the receiver demodulates the wireless signal to “010011000”. Note that the 2nd and 4th received bits are different from their corresponding bits in the transmitted bit sequence. The decoder, knowing that the transmitted bit sequence was structured such that every 3 bits were identical, can process the received bit sequence “010011000” and identify that there is an error in the first 3 bits and another error in the second 3 bits. (EX2001 at ¶28; EX2004 at 11). Thus, the decoder can identify that errors are present in the received bit sequence. (EX2001 at ¶28; EX2004 at 11).

Further, the decoder in the example could correct the errors by determining which value of the bit (“0” or “1”) occurs more frequently in each set of 3 consecutive bits and choose that bit type as the final output bit type². (EX2001 at ¶29; EX2004 at 11). Thus, in the example, the decoder can identify that a “0”

² In the example, for simplicity of discussion, the decoder performs “hard” bit decisions. However, a decoder can be implemented to perform “soft” bit decisions that reflect a likelihood a given bit type (“0” or “1”) is correct.

occurs more frequently for the first 3 bits, a “1” occurs more frequently for the second set of 3 bits, and a “0” occurs more frequently for the third set of three bits and determine they are the most likely correct bits. In this instance, the receiver will output “010” as the final user bits. (EX2001 at ¶29; EX2004 at 11). Such error identification and correction is possible because of the redundancy and increase in the number of transmitted bits.

While the above example provides a simple error correction coding approach, there are a wide range of error correction coding approaches utilized in the field of communications that introduce redundancy into the bit sequence in different manners. (EX2001 at ¶30; EX2003 at 293; EX2004 at 11; EX2005 at 228-229). These examples include convolutional codes, soft-output Viterbi, Maximum A Posterior, Bahl-Cocke-Jelinis, Raviv (BCJR), and turbo codes. (EX2001 at ¶30; EX2003 at 293, 311; EX2004 at 11; EX2005 at 230-259).

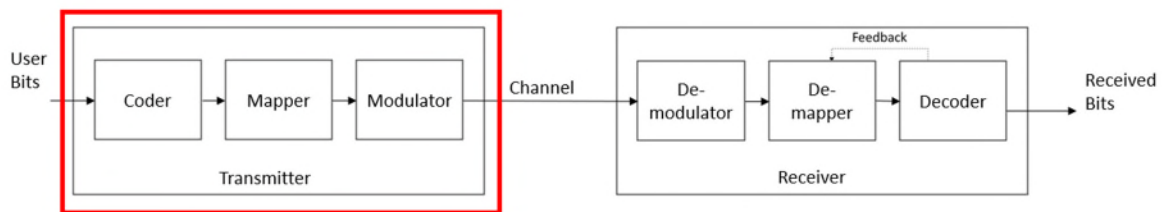
Notably, any error correction coding approach will necessarily involve the encoder increasing the number of bits to-be-transmitted, and the decoder will necessarily perform the inverse operation such that the number of final received user bits is decreased from what was transmitted over the channel. (EX2001 at ¶31; EX2003 at 293; EX2005 at 230). Processing units that do not involve the use of any error correction coding that adds redundancy in some form into the transmitted

bit sequence cannot reasonably be considered to be an encoder or decoder.

(EX2001 at ¶31; EX2003 at 2-3, 293; EX2005 at 230).

As described above, error correction coding is implemented using a **coder** at the transmitter, and a **decoder** at the receiver. As illustrated below, in a digital communication system, the transmitter typically includes the coder in the processing stream before the mapper and the modulator. (EX2001 at ¶32; EX2003 at 2-3, 107; EX2004 at 3-5).

Coded System



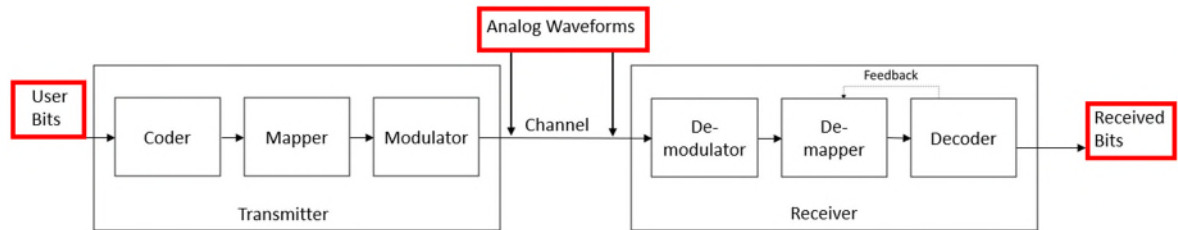
(EX2001 at ¶32; Based on FIG. 1.1 of EX2003).

The **coder** increases the number of user bits into a longer sequence of bits that includes redundancy and error-correcting features to enable error correction at the receiver. (EX2001 at ¶33; EX2003 at 2-4, 107; EX2004 at 6-7). This longer sequence of bits makes the transmission more robust against noise or disruptions in communication channels.

The resulting new bit sequence from the coder is input to the **mapper** which maps this new sequence to symbols. (EX2001 at ¶34; EX2003 at 7; EX2004 at 181-209). Similar to the uncoded system, the mapper in the coded system provides

these symbols to the transmitter's **modulator**, which creates a waveform that can be sent through the channel. (EX2001 at ¶34; EX2004 at 3, EX2004 at 6-7).

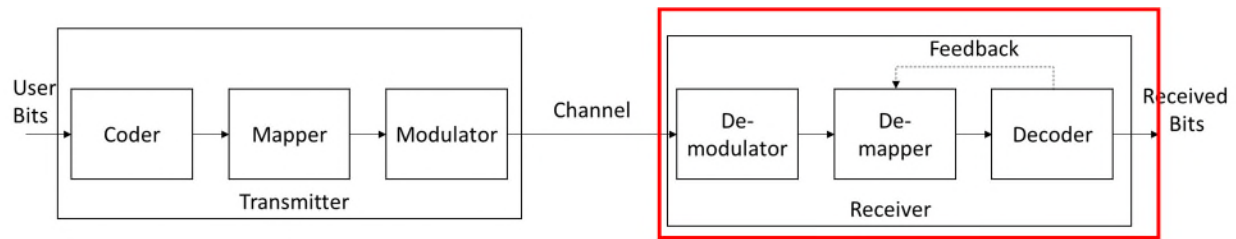
Coded System



(EX2001 at ¶34; Based on FIG. 1.1 of EX2003).

Like the uncoded system, the receiver in the coded system typically mirrors the transmitter and includes: a de-modulator, a demapper, and a decoder.

Coded System



(EX2001 at ¶35; Based on FIG. 1.1 of EX2003).

The **demodulator** receives the modulated waveform via the channel and attempts to extract the waveform's symbol values (in our example, amplitude).

(EX2001 at ¶36; EX2003 at 3-4; EX2004 at 4-7).

The extracted symbol values are then input to the **demapper**, which is used to help identify which bit sequence may correspond to the extracted symbol values.

(EX2001 at ¶37; EX2003 at 3-4, 43-46; EX2004 at 4-7). But because of noise in

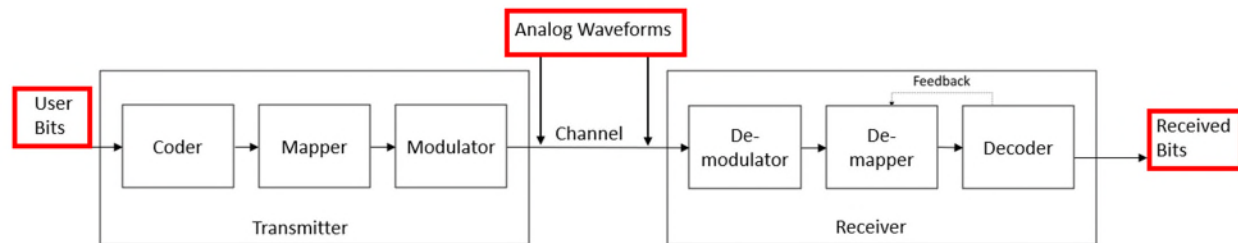
the transmission, the demodulated symbol values signal obtained from the demapper may not be identical to the symbol values output from the mapper at the transmitter side. (EX2001 at ¶37; EX2003 at 43-46). The demodulated symbol values may also include likelihood information that estimates whether a particular bit is 0 or 1.

The **decoder** implements the error correction coding technique, as described above, to identify and eliminate errors in the symbol values. In particular, the decoder reconstructs the original signal using the output of the demapper, applies the error correction coding, and reconstructs the original signal. (EX2001 at ¶38; EX2003 at 3-4; EX2004 at 11).

In light of the foregoing, an uncoded system and a coded system are not interchangeable. That is, one cannot merely add a decoder to an uncoded system to arrive at a coded system. (EX2001 at ¶39; EX2003 at 2-3; EX2005 at 228). Both types of systems have different methods of recovering user data. (EX2001 at ¶39; EX2003 at 75; EX2005 at 256-258). For example, the uncoded system applies decisions rules to obtained symbols to recover the user bits. (EX2001 at ¶39; EX2003 at 75). On the other hand, the coded system applies a coding scheme with an increased number of bits to eliminate errors and identify the appropriate bit sequences. (EX2001 at ¶39; EX2003 at 75; EX2004 at 11). The coding scheme is also determined prior to the transmission over the channel and is independent of

unique signal paths and their corresponding interference. (EX2001 at ¶39; EX2003 at 293; EX2004 at 11; EX2005 at 228-229).

Contrary to the Petition's unexplained presumption, the derivation of data bit decisions does not imply the existence of a coded system having a bank of decoders because the derivation of data bit decisions does not result in introduction of redundancy into the bit sequence to-be-transmitted. (EX2001 at ¶40; EX2003 at 107).



(EX2001 at ¶40; Based on FIG. 1.1 of EX2003).

B. Soft Data Bit versus Hard Data Bit Decisions in Uncoded Systems

As discussed, a demodulator extracts symbol values from the waveform and passes the extracted symbols to the **demapper**. (EX2001 at ¶41; EX2003 at 3-4; EX2004 at 4-7). The task of the demapper is to associate an observed symbol value with a reference point in a space of observations to form a bit sequence. (EX2001 at ¶41; EX2003 at 43-46 and 89, EX1012 at 85). That is, the demapper identifies a bit sequence corresponding to the extracted symbol values. (EX2001 at ¶41; EX2003 at 3-4, 43-46; EX2004 at 4-7).

But extracted symbol values signal may not be identical to the symbol values generated at the transmitter side due to noise in the channel. (EX2001 at ¶42; EX2003 at 43-46). To address variations in observed symbol values from extracted symbol values, the demapper applies **decision rules** to the extracted symbol values. (EX2001 at ¶42; EX2003 at 75; EX2005 at 81). Decisions may be divided into two categories: hard decisions or soft decisions. (EX2001 at ¶42; EX2003 at 75; EX2005 at 238). The demapper applies either hard decisions or soft decisions to the extracted symbol values. (EX2001 at ¶42; EX2003 at 75; EX2005 at 238).

Hard decisions include requiring the demapper to assume whether a particular bit is 0 or 1. (EX2001 at ¶43; EX2003 at 3; EX2005 at 238). For example, a demapper may observe a sequence of voltages having magnitudes of 0.66, 0.05, 0.48, and 1.05. The demapper may take each voltage from the sequence and map the voltage to a corresponding 2-bit sequence. (EX2001 at ¶43). Using the bit and symbol correlation identified below, an expected symbol value or expected sequence of voltages of 0.66, 0.0, 0.33, and 1.0 could be mapped to a bit sequence:

2-Bit Sequence	Symbol (Waveform Amplitude)
“00”	0
“01”	.33

“10”	.66
“11”	1.0

But some observed voltages (i.e., 0.05V, 0.48V and 1.05V) are not exact matches to a symbol in the mapping: although there is a deviation between the observed voltage amplitude and the desired voltage magnitude, the demapper may apply hard decisions that assume that the voltages having magnitudes of 0.05, 0.48, and 1.05 are to be mapped to bit sequences 00, 01, and 11. (EX2001 at ¶44).

But sometimes the assumptions of hard decisions are incorrect. (EX2001 at ¶45). For example, the observation of 0.48V received more channel interference than the other observed voltages. The transmitted voltage magnitude may have been 0.66V and the channel distorted the symbol to 0.48V. Applying the mapping of bit sequence “01” instead of bit sequence “10” for the observed voltage of 0.48V is an error due to the assumption made by the hard decision.

In contrast to hard decisions, soft decisions estimate the likelihood that a particular bit is 0 or 1. (EX2001 at ¶46; EX2003 at 3; EX2005 at 238).

C. Successive Interference Cancellation vs. Parallel Interference Cancellation

There are at least two distinct approaches to interference cancellation: (1) successive interference cancellation; and (2) parallel interference cancellation. (EX2001 at ¶47). The Petition highlights and relies on the material differences

between the two approaches because its sole argument for combining Grounds 4-5 *Frank* and *Zha* references is its assertion that they both use the successive approach to interference cancellation. (*E.g.*, Pet. at 50-54). Momentarily putting aside the baselessness of Petitioners' conclusion (which is akin to arguing it is obvious to import any and all features from a gas engine into an electric engine because they both drive a vehicle's wheels), the entire premise for this obviousness argument is demonstrably false: while *Zha* does indeed use successive interference cancellation, every *Frank* embodiment that Petitioners seek to combine with *Zha* is explicitly and expressly parallel interference cancellation. (*E.g.*, EX1006 at ¶¶ [0012]-[0015]). Unable to assert, much less support, how these disparate approaches would and could be combined, the Petition just pretends they both use successive interference cancellation and does not address the distinct differences between the two. The following provides that missing information.

Successive Interference Cancellation: As the name suggests, successive interference cancellation attempts to identify and isolate the channel's multiple signals one after the other. (EX2001 at ¶48). For example, if there were ten signals present in a channel's information stream, the receiver would first try to identify and isolate just one of those signals, ignoring the remaining nine signals as interfering noise. Once this first signal is recovered, its information is subtracted (cancelled) from the original information stream. (EX2001 at ¶48).

The receiver then attempts to recover a second signal from the resulting smaller residual information stream, again ignoring the remaining signals as interfering noise. Once this second signal is recovered, it, too is subtracted (cancelled) from the information stream. (EX2001 at ¶49).

This successive process continues, with a third signal being recovered and subtracted, a fourth signal being recovered and subtracted, *etc.*, until the information stream comprises only information for the last signal. This information is then used to recover that final signal, completing the successive interference cancellation process. (EX2001 at ¶50).

Parallel Interference Cancellation: In contrast, in a parallel interference cancellation process, the receiver does not attempt to recover signals one at a time, one after the other. Instead, the receiver attempts to recover all of the signals at the same time. (EX2001 at ¶51).

Consider again our example of ten user signals present in a single channel's information stream. In parallel interference cancellation, the receiver will attempt to isolate and recover all ten signals at the same time. For example, the receiver may try to simultaneously subtract from each signal the interfering information for the other nine signals. For each of the ten resulting sets of information, the receiver will then attempt to reconstruct its corresponding signal. (EX2001 at ¶52).

Because the reliability of these initial cancellations and reconstructions is typically low, the process will continue iteratively, with the receiver repeatedly recalculating and subtracting from each signal the interfering information for the other nine signals, until reliable cancellations, symbols, and signals are achieved. (EX2001 at ¶53).

III. The '703 Patent's Bank of Decoders with Feedback to a Joint Amplitude Estimator

The '703 Patent and its challenged claims generally concern wireless communication systems with multiple signals. More specifically, the claims are directed to an improved apparatus that applies a bank of decoders to produce a plurality of symbol likelihood estimates for each user. Once symbol likelihood estimates are produced, the symbol likelihood estimates are fed back to the symbol estimator for error correction and a joint amplitude estimator.

The '703 Patent addresses extracting the correct data for a given user following transmission with interference and multipaths. (EX1001 at 2:64-66). Extracting user data can be further complicated when the number of users exceeds the number of dimensions (*e.g.*, time slots, frequency slots, polarizations, *etc.*) in a system, resulting in an *overloaded condition*. (EX1001 at 2:66-3:2). Overloaded conditions can exist where the number of simultaneous users is doubled or tripled

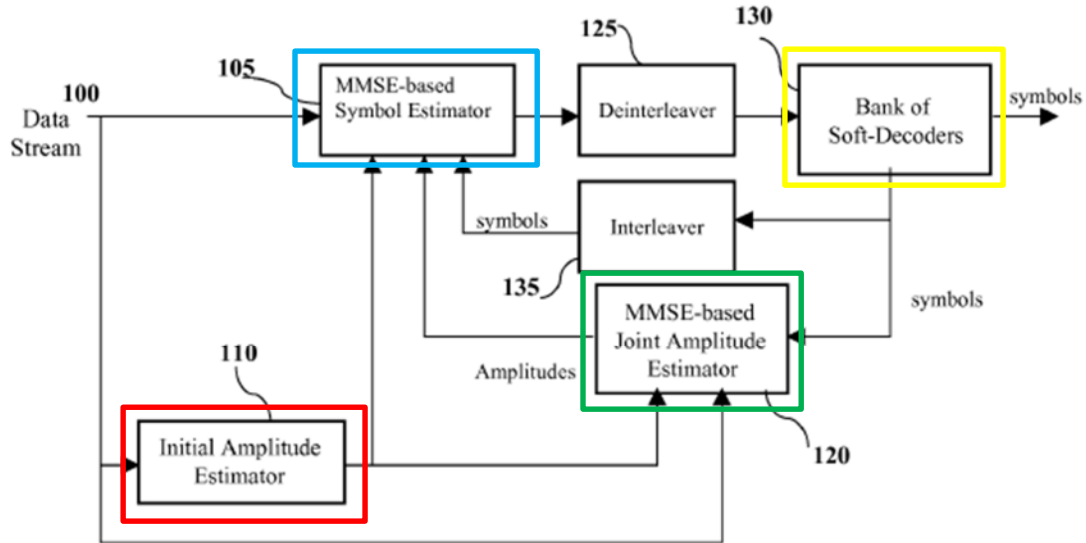
relative to the number of dimensions (e.g. time slots, frequency slots, polarizations, *etc.*). (EX1001 at 7:3-15).

The '703 Patent improves over prior systems by delivering better performance while accommodating *overloaded conditions*. (EX1001 at 5:50-52).

A. Exemplary Architecture

The '703 Patent describes overcoming the problems of *overloading* by providing turbo decoding based on an iterative decoding solution that exploits error correction codes. (EX1001 at Abstract). The methods and embodiments of the joint symbol estimator, the joint amplitude estimator, and the bank of decoders can provide high quality real-time processing for multiple access systems, including *overloaded situations*. (EX1001 at 11:33-37, 13:67-14:2). FIG. 2 of the '703 Patent illustrates an example system, which includes bank of decoders 130 providing feedback to both the symbol estimator 105 and joint amplitude estimator 120.

An exemplary receiver architecture illustrated in '703 Patent Figure 2 includes an initial amplitude estimator 110 (highlighted below in red), a symbol estimator 105 (blue), a bank of decoders 130 (yellow), and a joint amplitude estimator 120 (green).

**Figure 2**

(EX1001 at Figure 2; EX2001 at ¶58).

For a high-level overview (as illustrated above in Figure 2 and described in more detail below), this architecture works as follows:

(1) the received multi-user data stream 100 is provided to the initial amplitude estimator 110, which detects active users and calculates an initial estimate of the amplitude of each user signal in the stream (EX1001 at 15:25-44; EX2001 at ¶59);

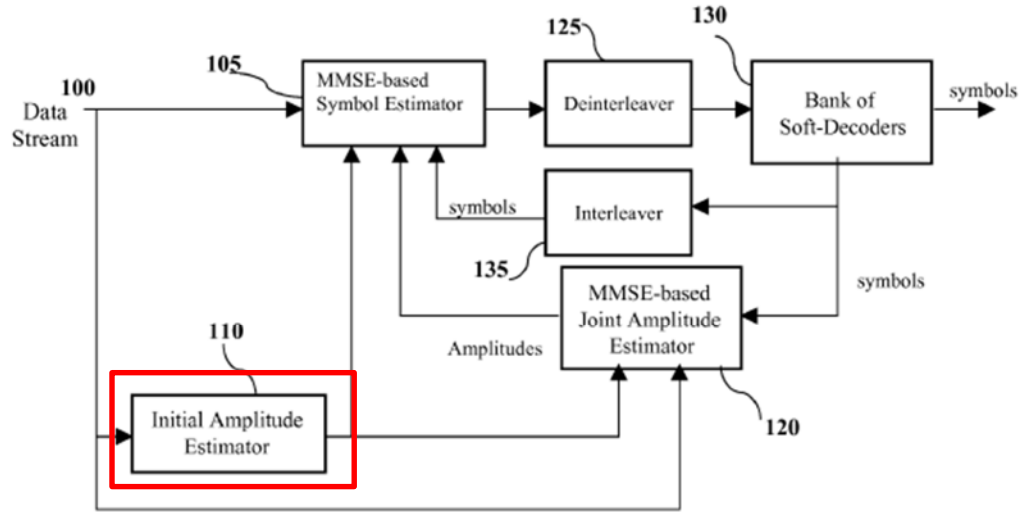
(2) these initial amplitude estimates are provided (along with the data stream) to the symbol estimator 105, which uses that data to estimate symbols for each user (EX1001 at 15:43-51, 16:3-7, 16:43-48; EX2001 at ¶59);

(3) those symbol estimates are provided to the bank of error-correcting decoders 130, which calculate probabilities for the symbol estimates (in other words, how likely those symbols are correct) (EX1001 at 8:65-9:1, 16:8-14, 16:39-42; EX2001 at ¶59);

(4) the symbol likelihoods from the decoder are passed to the joint amplitude estimator, which uses that information to calculate updated amplitude estimates, which are provided to the symbol estimator so that it can use them to calculate updated symbol estimates (EX1001 at 16:39-42, 18:65-20:52; EX2001 at ¶59); and

(5) the symbol estimator, decoders, and joint amplitude estimator continue this cycle to iteratively calculate and provide information to one another (the joint amplitude estimator providing updates amplitude estimates to the symbol estimator, which in turn provides updated symbol estimates to the decoders, which in turn provides symbol likelihoods to the joint amplitude estimator, starting the cycle all over again) until some criteria is met, such as reaching a maximum number of iterations or a desired error rate (EX1001 at 16:39-52, 20:41-52; EX2001 at ¶59).

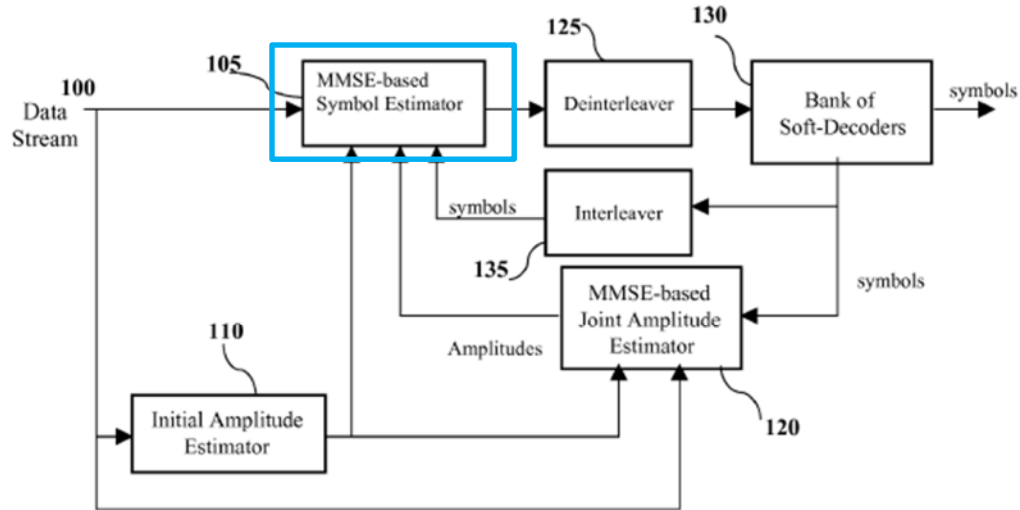
Initial Amplitude Estimator: As illustrated below, the exemplary initial amplitude estimator 110 receives the multi-user data stream 100:

**Figure 2**

(EX1001 at Figure 2, 15:25-27; EX2001 at ¶60). This initial amplitude estimator uses energy detection to identify which users are active within the channel's data stream. (EX1001 at 15:35-44). It then integrates the energy out of a filter for all active users to compute an initial estimate for the amplitude of each active user's signal. (EX1001 at 15:26-34).

As illustrated above, the initial amplitude estimates are passed to the exemplary symbol estimator 105 and to the joint amplitude estimator 120.

Symbol Estimator: During the first iteration of the process, exemplary symbol estimator 105 receives the data stream 100 and the initial amplitude estimator 110's initial amplitude estimates:

**Figure 2**

(EX1001 at Figure 2, 15:42-53; EX2001 at ¶63). The symbol estimator then uses that data to estimate symbols for each user. (*Id.*).

The symbol estimator uses the initial amplitude estimates to compute symbol estimates only during the first cycle/iteration. (EX1001 at 15:42-53). During all other iterations, the symbol estimator uses updated amplitude estimates from the joint amplitude estimator (along with other information, such as prior information on the symbols) to re-estimate the symbols. (EX1001 at 15:42-53, 16:43-52).

Decoders: The symbol estimates from the symbol estimator are routed to the exemplary decoders 130.³ (EX1001 at 16:3-7). The decoders calculate the likelihood for each estimated symbol and then routes those estimated symbols and their respective likelihoods to various units, including joint amplitude estimator 120:

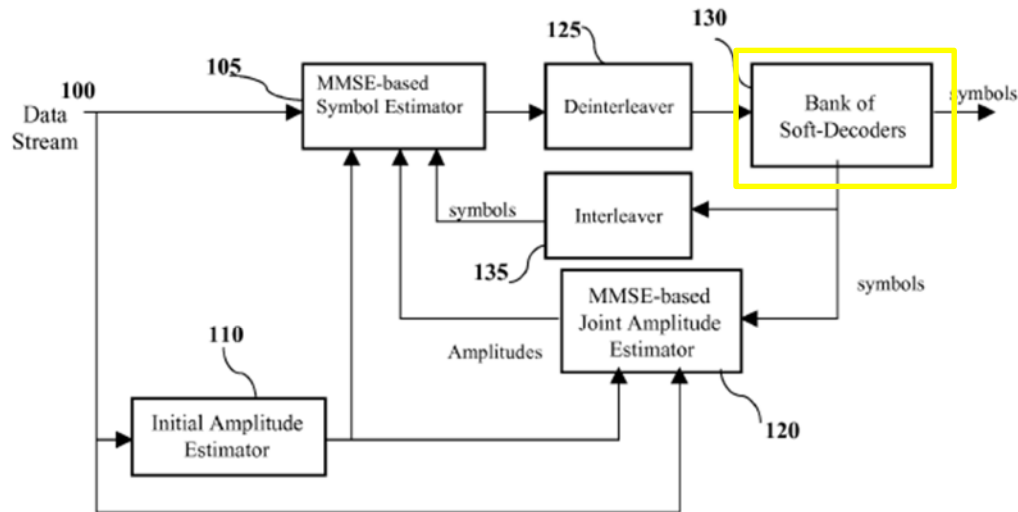


Figure 2

(EX1001 at Figure 2, 16:39-42, 18:65-20:52; EX2001 at ¶66).

Joint Amplitude Estimator: Disclosed architecture embodiments include a joint amplitude estimator (discussed in more detail in the following section) apart from the initial amplitude estimator, symbol estimator, and decoders. After the

³ For purposes of this general overview, details concerning other disclosed blocks, such as the deinterleaver 125 and interleaver 135 are omitted. (See, e.g., EX1001 at 16:15-28).

initial amplitude estimator provides the initial amplitude estimate, all updated amplitude estimates are computed and provided to the symbol estimator by and from exemplary joint amplitude estimator 120:

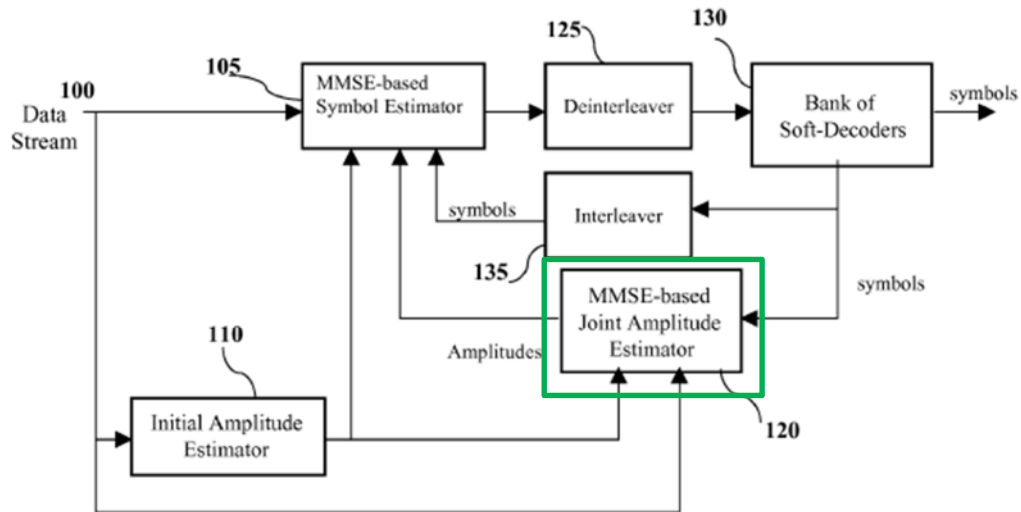


Figure 2

(EX1001 at Figure 2, 16:39-42, 18:65-20:52; EX2001 at ¶67).

These updated amplitude estimates are based on the symbol likelihoods from the decoders and are provided to the symbol estimator to start a new cycle of computations, which continues and repeats until a predefined condition is met:

The new symbol likelihoods from the decoders 130 are used to update previous amplitude estimates in the joint amplitude estimator 120. ... The new amplitude estimates from the joint amplitude estimator 120 are passed to the MMSE-based Symbol Estimator 105 that re-estimates the symbols based on prior information on the symbols and updated parameter estimates. These updated symbol estimates from the symbol estimator 105 are then re-routed to the bank of decoders 130. This process is repeated for either some fixed number of

iterations or until the estimates of the bit error rate or frame error rate achieve some desired level.

(EX1001 at 16:39-52).

The blocks involved in this exemplary iterative cycle are outlined in dotted blue below:

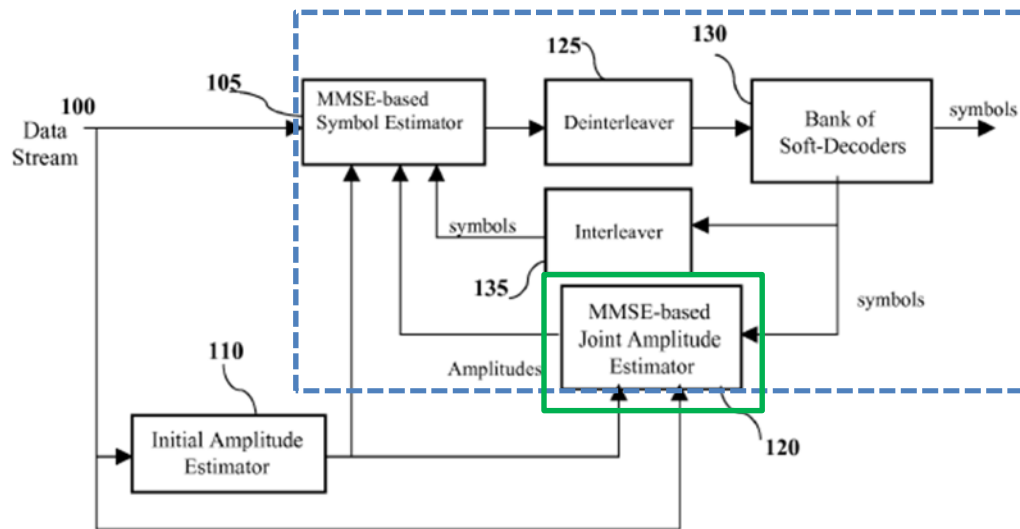


Figure 2

(EX1001 at Figure 2, 16:39-52; EX2001 at ¶69).

A. The Challenged Claims

The challenged claims cover at least parts of the foregoing innovative approaches, each of which requires a receiver having a bank of decoders that provides feedback to the joint amplitude estimator. (See, *e.g.*, EX1001 at claims 1-5).

And consistent with the foregoing, all of the challenged claims additionally include the following limitations:

- “a bank of decoders coupled to said symbol estimator, producing a plurality of symbol likelihood estimates for each user, wherein said symbol likelihood estimates are iteratively fed back to said symbol estimator and said joint amplitude estimator until a final condition is obtained.”

(See, e.g., EX1001 at claim 1).

For example, each of these limitations is present and highlighted in the following exemplary claim 1:

1. An apparatus for processing a digital data stream from multiple users, comprising:

an initial amplitude estimation unit processing said data stream and producing initial amplitude estimates on a first iteration;

a joint amplitude estimator coupled to said data stream and said initial amplitude estimator, wherein said joint amplitude estimator produces updated amplitude estimates;

a symbol estimator coupled to said data stream, said initial amplitude estimator, and said joint amplitude estimator, wherein said symbol estimator produces a plurality of symbols estimates for each user; and

a bank of decoders coupled to said symbol estimator, ***producing a plurality of symbol likelihood estimates*** for each user, wherein said symbol likelihood estimates are ***iteratively fed back to*** said symbol estimator and ***said joint amplitude estimator*** until a final condition is obtained.

(EX1001 at claim 1).

IV. The Petition and Deficiencies of the Asserted References

The Petition asserts the following Grounds:

Ground	References	Basis	Challenged Claims
1	<i>Brommer, Lilleberg, and Hottinen</i>	§ 103	1-3
2	<i>Brommer, Lilleberg, Hottinen, and Learned</i>	§ 103	4
3	<i>Brommer, Lilleberg, Hottinen, and ElGamal</i>	§ 103	5
4	<i>Frank and Zha</i>	§ 103	1-3, 5
5	<i>Frank, Zha, and Learned</i>	§ 103	4

The Petition relies on *Brommer, Lilleberg, and Hottinen* as allegedly rendering obvious claim 1 for grounds 1-3 and *Frank and Zha* as allegedly rendering obvious claim 1 for grounds 4-5. But both of these combinations fail to disclose all the required claim limitations of independent claim 1.

A. Grounds 1-3

Grounds 1-3 each rely on *Brommer, Lilleberg, and Hottinen*. But *Brommer* is not prior art. And even were *Brommer* considered to be prior art, none of the references, alone or in combination, describe the claimed “bank of decoders coupled to said symbol estimator, producing a plurality of symbol likelihood estimates for each user, wherein said symbol likelihood estimates are iteratively fed back to said symbol estimator and said joint amplitude estimator.”

1. *Brommer* is not § 102(e) Prior Art Because *Brommer* was Owned by BAE and the '703 Patent Inventor Was “Subject to an Obligation of Assignment” to BAE

The Petition alleges that *Brommer* applies as prior art under at least 35 U.S.C. § 102(e). (Pet. at 17). But *Brommer* is disqualified as prior art under 35

U.S.C. § 103(c) due to *Brommer* and the '703 Patent being commonly owned by BAE. *Brommer* is excluded as prior art under § 102(e) because at all relevant times, the subject matter of *Brommer* and the inventions claimed in the '703 patent were “owned by the same person or subject to an obligation of assignment to the same person.” 35 U.S.C. § 103(c) (pre-AIA). *Brommer* first published as US 2004-0037202 on February 26, 2004. (EX1004 at page 1).

In September 20, 2002, the inventors of *Brommer* assigned their entire right, title, and interest in and to the inventions described in *Brommer* to BAE. (EX2011).

Prior to *Brommer*, BAE Systems North America (“BAE NA”) (the parent of BAE) acquired Lockheed Martin Corporation’s (“Lockheed”) “Aerospace Electronics Systems Business,” including approximately 5,300 employees in 2000 (the “Acquisition”). (EX2016 at 1; EX2015 at 2). Following the Acquisition, former employees of the acquired Lockheed division, including the inventor of the '703 Patent, became employees of BAE Systems Information and Electronic Systems Integration Inc. (“BAE”). (EX2016 at 1).

Thomas McElwain (“McElwain”), the sole inventor of the '703 Patent, was employed by Lockheed beginning in 1996. (EX2014). During his employment with Lockheed, McElwain was “subject to an obligation of assignment” to Lockheed all “Innovations” (defined as “inventions, discoveries, improvements,

computer programs, mask works, works of authorship”) under the terms of the Employee Proprietary Information and Innovation Agreement dated September 16, 1996 (“EPIIA”). (EX2014). Specifically, under the EPIIA, McElwain agreed that all “Innovations and Work for Hire shall be the sole and exclusive property of Lockheed Martin and I hereby assign to the Corporation all of my right, title, and interest therein.” EX2014 at §3. McElwain’s employment, as well as his obligations under the EPIIA, were acquired by BAE in 2000 as part of the Acquisition. Accordingly, McElwain’s obligation to assign inventions to Lockheed was transferred to BAE in 2000 as part of the Acquisition.

Accordingly, prior to the April 14, 2003 filing of Provisional Patent Application No. 60/462,657 (the earliest priority claim of the ’703 Patent), McElwain, by virtue of his EPIIA, and the Acquisition, was subject to an obligation to assign to BAE the subject matter of the ’703 Patent. Additionally, prior to filing the 60/462,657 application, McElwain preemptively assigned his entire right, title, and interest in and to such subject matter of the ’703 Patent to BAE via the present tense assignment language of the 1996 EPIIA. EX2014, §3.

In furtherance of the EPIIA, on November 25, 2003, McElwain executed a recordable patent assignment agreement assigning his entire right, title, and interest in and to the inventions claimed in the ’703 Patent to BAE. (EX2012).

Employment agreements, like the EPIIA, are conclusive proof that an inventor was

subject to an obligation of assignment. *See Limelight Networks, Inc., v. Akamai Techs., Inc.*, IPR2017-00349, Paper 7 at 27–28 (P.T.A.B. May 30, 2017); *Corning Inc. v. DSM IP Assets B.V.*, IPR2013-00053, Paper 66 at 21 (P.T.A.B. May 1, 2014). Here, McElwain was subject to an obligation to assign his rights in the inventions described in the '703 Patent, which he in fact did. (EX2012).

The obligation to assign is further confirmed by the prosecution history of the priority application. For example, the transmittal of Provisional Patent Application No. 60/462,657 (the earliest priority claim of the '703 Patent) was filed using the BAE USPTO Customer number and BAE correspondence address. (EX2013 at 2).

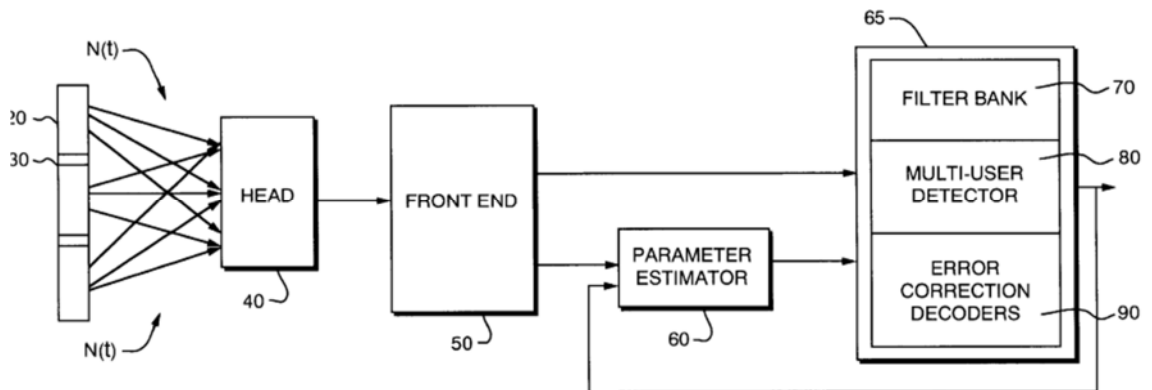
Accordingly, the subject matter of *Brommer* and the '703 Patent were commonly owned by BAE at the time of the invention and *Brommer* is not available to Petitioners to show the obviousness of the '703 Patent under § 103(c).

The failure of the Petition to rely upon a reference that is actually prior art is fatal to grounds 1-3.

2. None of the Asserted References for Ground 1 Concerns or Describes a Joint Amplitude Estimator, Much less a Bank of Decoders that Provides Feed Back to the Joint Amplitude Estimator

Brommer describes multiuser detection to separate tracks of data from neighboring tracks in a digital storage medium. (EX1004 at 15:9-35; EX2001 at

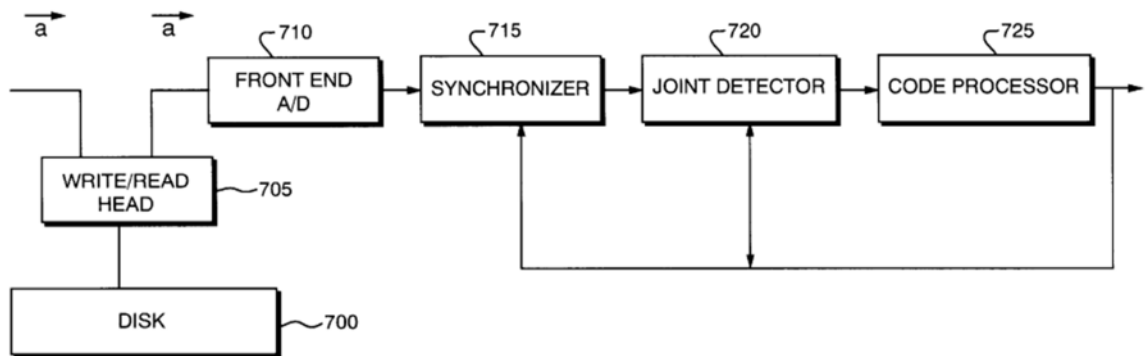
¶73). In FIG. 1 of *Brommer*, a head 40 extracts a plurality of signals from the tracks at the digital storage medium. (EX1004 at 15:9-35; EX2001 at ¶73). The signals are processed by parameter estimator 60 and MUD processing section 65. MUD processing section 65 includes bank of matched filters 70 for preprocessing the signals. (EX1004 at 15:9-35; EX2001 at ¶73). MUD processing section 65 also includes multi-user detector 80 that uses an algorithm to establish symbol estimates and a bank of decoders 90 to provide further processing. (EX1004 at 15:9-35; EX2001 at ¶73). FIG. 1 of *Brommer* does not describe a joint amplitude estimator.



(EX1004 at FIG. 1).

Brommer describes another embodiment used for reading and writing to neighboring tracks in a digital storage medium. In FIG. 8 of *Brommer*, a read head 705 extracts analog voltage signals from the data on the tracks of magnetic disk platter 700. (EX1004 at 25:48-26:12; EX2001 at ¶74). The analog voltage signals are converted to a digital stream of data by front end 710. (EX1004 at 25:48-26:12; EX2001 at ¶74). Front end 710 feeds digital samples of the analog waveform into

synchronizer 715. (EX1004 at 25:48-26:12; EX2001 at ¶74). Synchronizer 715 generates a track transfer function for each of the appropriate functions, including estimates of the pulse envelope for each track. (EX1004 at 25:48-26:12; EX2001 at ¶74). Using the track transfer functions and estimates of the pulse envelope, the joint detector makes preliminary estimates of the interfering digital signal values containing in the received signal. (EX1004 at 25:48-26:12; EX2001 at ¶74). The preliminary symbol estimates produced by joint detector 720 are send to code processor 725 to update the preliminary estimates. (EX1004 at 25:48-26:12; EX2001 at ¶74). Code processor 725 and joint detector 720 refine these estimates using iterations. (EX1004 at 25:48-26:12; EX2001 at ¶74). But FIG. 8 of *Brommer* does not describe a bank of decoders.



(EX1004 at FIG. 8).

FIG. 1 and FIG. 8 of *Brommer* have different components. (EX2001 at ¶75). FIG. 8 of *Brommer* does not include at least two elements of the MUD processing section 65: bank of matched filters 70 and bank of decoders 90. Additionally, FIG.

1 and FIG. 8 also have different dataflows. (EX2001 at ¶75). For example, front end 710 in FIG. 8 feeds all digital samples of the analog waveform into the synchronizer 715. In contrast, FIG. 1 of *Brommer* suggests the dataflow from the front end 50 may bypass parameter estimator 60 in route to MUD processing section 65. (EX2001 at ¶75).

B. Grounds 4-5

1. Neither *Frank* nor *Zha* Concern or Describe “a bank of decoders that produce symbol likelihood estimates for each user, wherein said symbol likelihood estimates are iteratively fed back to said symbol estimator and said joint amplitude estimator until a final condition is obtained”

Frank describes a communication system that includes an error correction decoder such as a turbo decoder. (EX1006 at ¶ [0010]). The Petition concedes that *Frank* does not disclose “a bank of decoders that produce symbol likelihood estimates for each user” and instead relies upon *Zha*. (Pet. at 60).

Zha describes successive interference cancellation in which individual user signals are first separated according to code division multiple access (CDMA), and then estimates of each user signal are used to successively cancel interference in the other user signals. (EX1010 at 743; EX2001 at ¶77). By successively cancelling (or subtracting) the contribution of one user’s signal from the other user signals, the accuracy of the detection process can be improved. (EX1010 at 743-744; EX2001 at ¶77). *Zha* notes that in certain circumstances while performing

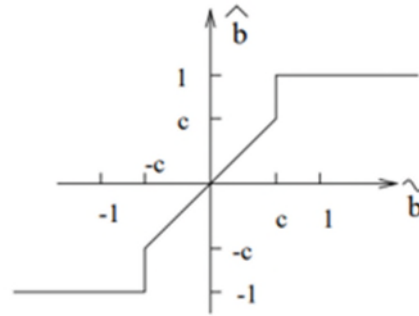
successive interference cancellation, performing “hard” decisions in the detection process can lead to reduced performance when the “hard” decision is incorrect. (EX1010 at 743; EX2001 at ¶77). This is because the incorrect “hard” decision error is propagated and impacts the detection of the other user’s signals. (EX1010 at 743; EX2001 at ¶77). *Zha* notes that in some instances, when performing the cancellation, it would be better to weigh a given bit-decision by a measure of confidence in the given bit. (EX1010 at 743; EX2001 at ¶77). Thus, if that decision is incorrect, it will have a smaller negative effect when canceling the given user’s signal from the other user signals. (EX1010 at 743; EX2001 at ¶77). In order to implement this approach, *Zha* describes a “soft decision rule” that may output, for a given bit, a weighted value rather than an explicit “hard” “0” or “1”. (EX1010 at 744; EX2001 at ¶77).

Zha shows that bit decisions are derived by applying the clipping function of Equation 7 to the soft data bit estimates.

$$\hat{b} = f_{dec}(\tilde{b}) = \begin{cases} 1, & \tilde{b} > c \\ \tilde{b}, & \tilde{b} \in [-c, c] \\ -1, & \tilde{b} < -c \end{cases} \quad (7)$$

The clipping function of Equation 7 treats soft data bit estimates with a probability above threshold c as hard data bit estimates. (EX1010 at 745; EX2001 at ¶79). Similarly, soft data bit estimates with a probability below threshold c

remain unchanged. (EX1010 at 745; EX2001 at ¶79). This clipping function can be depicted, as shown in figure 1(d):



(d) Proposed decision rule

Thus, while *Zha* describes soft bit decision rules, there is no mention of any decoder, let alone a “bank of decoders”.

Indeed, the “soft decision rule” of *Zha* involves no error correction codes. (EX2001 at ¶81). There is no encoder at the transmitter that encodes the user bits to introduce redundancy into the transmitted signal. (EX2001 at ¶81). Similarly, there is no decoder at the receiver that uses error correction codes to assess the structure of the received signal to identify and correct errors. (EX2001 at ¶81). Moreover, *Zha* only weights a given bit and does not involve a system that performs an encoding process that increases the number of bits-to-be-transmitted and a decoder that performs the opposite operation. (EX1010 at 744; EX2001 at ¶81). In contrast, in error correction coding, introduction of redundancy by the encoder at the transmitter increases the number of bits to be transmitted (*e.g.*, an error correction code with a code rate of 1/3 would increase the number of bits by a

factor of 3), while the decoder will effect the opposite operation (*e.g.*, the decoding process). (EX2001 at ¶81).

Zha's mere description of "data bit decisions" made by a decision rule—without any discussion of redundancy, iterations, or error correction—does not imply the existence of a bank of decoders. (Pet. at 60; EX2001 at ¶82).

Accordingly, this key claimed concept is missing from both *Frank* and *Zha*, and combining them does not and cannot result in the claimed apparatus of claim 1.

Further, grounds 4-5 rely on combining primary reference *Frank* with *Zha*. But the supposed basis for combining these references—that they both use successive interference cancellation—is demonstrably incorrect: *Zha* uses **successive** interference cancellation, but every *Frank* embodiment relied on in the Petition explicitly uses the incompatible **parallel** interference cancellation approach. (*E.g.*, Pet. at 48-54; EX1006 at ¶¶ [0012]-[0015]; EX2001 at ¶83). Indeed, the Petition does not even identify how the references could supposedly be combined, much less establish that this undisclosed combination was somehow obvious. Nor could it. The Petition does not acknowledge these material differences, nor does it try to explain how these incompatible approaches could somehow be combined.

V. The Petition Should be Denied Because Each Asserted Ground Fails to Establish the Required Likelihood of Success

The Petition should be denied because as established in the following sections, Grounds 1-5 all fail to establish the required reasonable likelihood of success.

A. Grounds 1-3

The Petition fails to show that *Brommer* in view of *Lilleberg* in further view of *Hottinen* discloses or renders obvious independent claim 1 of the '703 patent for at least two independent reasons: (1) *Brommer* is not prior art; and (2) the Petition is silent regarding how the asserted references teach or suggest feedback from a bank of decoders to a joint amplitude estimator, as required by independent claim 1.

1. *Brommer* is Not Prior Art

The Petition alleges that *Brommer* applies as prior art under at least 35 U.S.C. § 102(e). (Pet. at 17). But, as established above, *Brommer* is disqualified as prior art under 35 U.S.C. § 103(c) due to *Brommer* and the '703 Patent being commonly owned by, or subject to an obligation to assign to, BAE.

That *Brommer* is not prior art is clear and established on the face of the prosecution histories as well as the faces of the '703 patent and *Brommer* publication, but Petitioners just ignore this fact. (EX2013 at 2; EX1004 at page 1, EX1001 at page 1). They fail to identify or acknowledge the common ownership

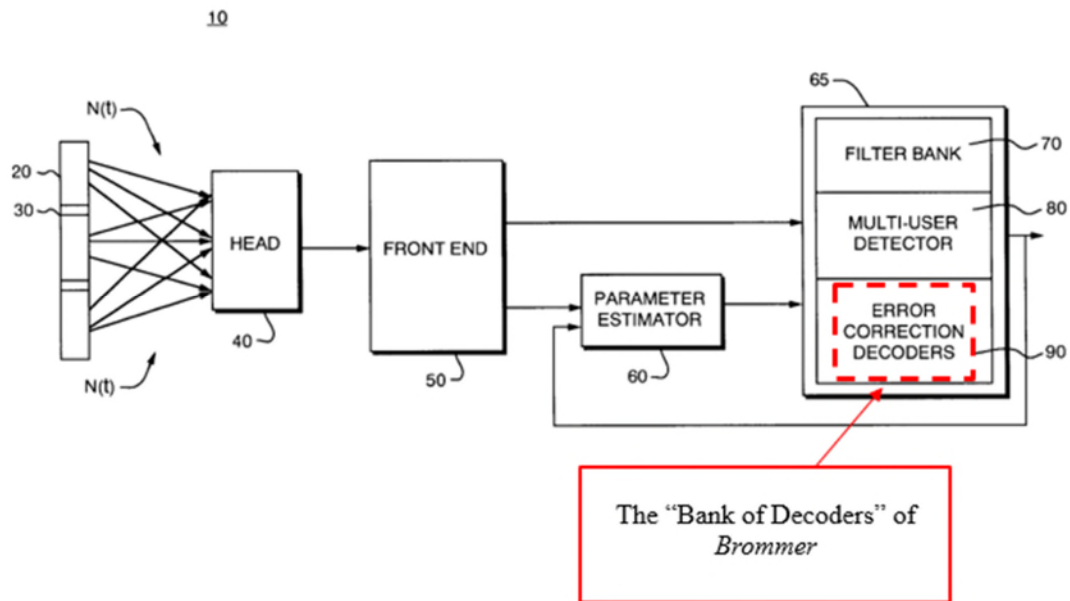
and fail to even try to explain how the reference is somehow prior art in light of that common ownership.

This failure of Grounds 1-3 to rely on prior art is fatal for Grounds 1-3.

2. **The Petition fails to show that the combination of *Brommer*, *Lillieberg*, and *Hottinen* describe “a bank of decoders... producing a plurality of symbol likelihood estimates for each user, wherein said symbol likelihood estimates are iteratively fed back to said symbol estimator and said joint amplitude estimator” as required by claim 1**

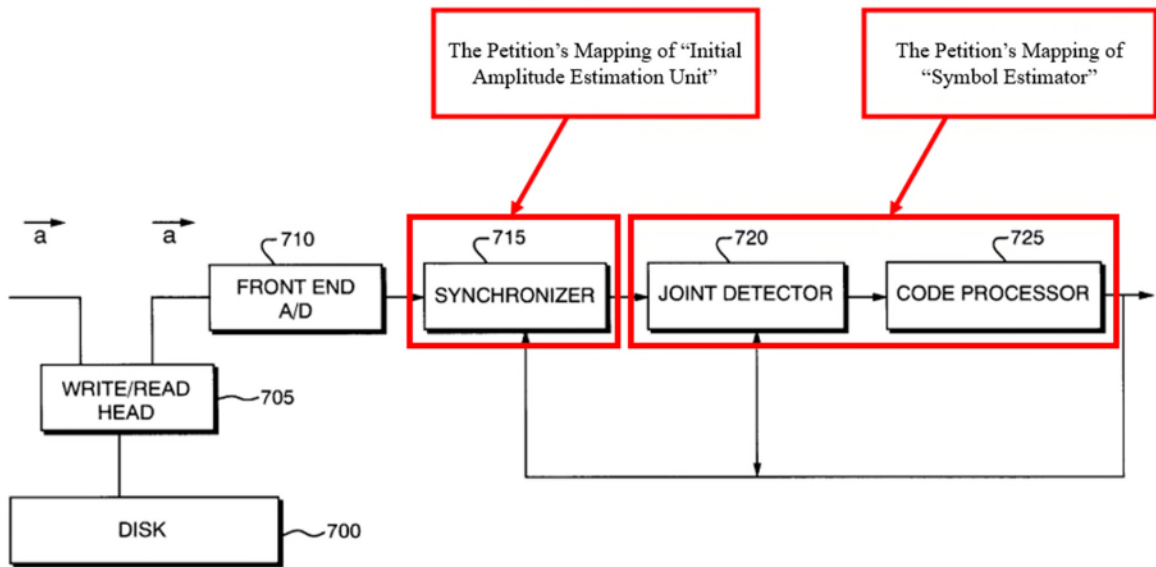
Even if *Brommer* were considered prior art (it is not), the Petition fails to demonstrate that *Brommer*, *Lillieberg*, and *Hottinen* describe “a bank of decoders... producing a plurality of symbol likelihood estimates for each user, wherein said symbol likelihood estimates are iteratively fed back to said symbol estimator and said joint amplitude estimator,” as required by claim 1.

In an attempt to show this requirement of claim 1, the Petition points to *Brommer*’s “bank of decoders 90” illustrated in FIG. 1:



(Pet. at 34-35; EX1004 at FIG. 1).

The Petition asserts that a POSITA would understand that, in combination with *Lilleberg*, the symbol likelihood estimates from bank of decoders 90 would be “fed back” to the symbol estimator (previously mapped to *Brommer*’s joint detector 720 and code processor 725 depicted in FIG. 8) and joint amplitude estimator. (Pet. at 34-35).

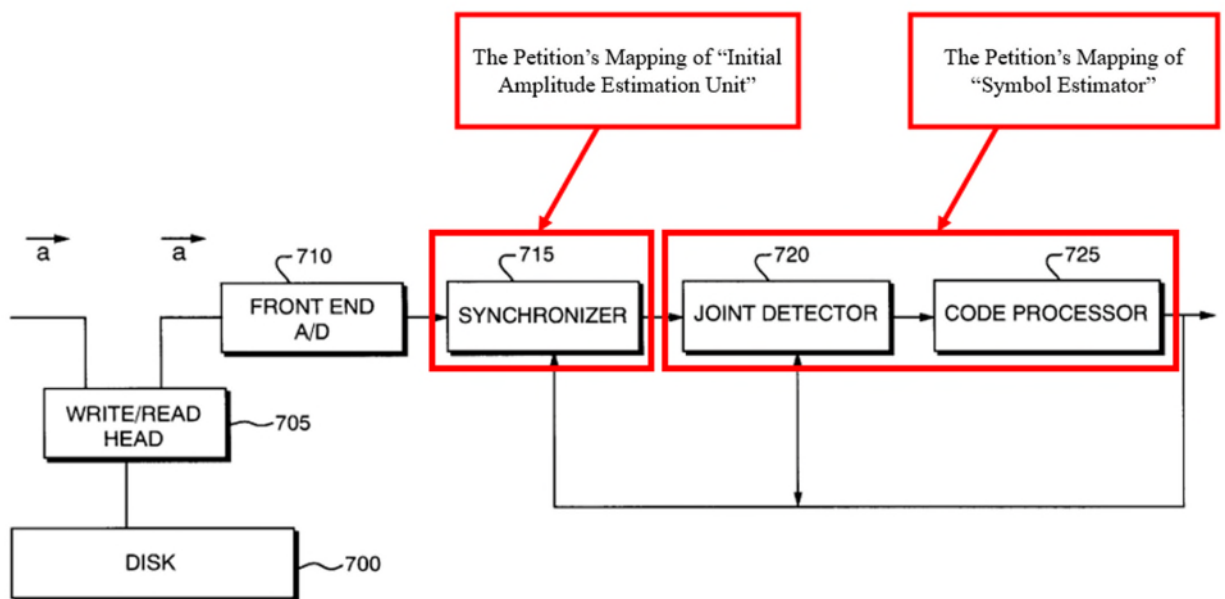


(Pet. at 34-35; EX1004 at FIG. 1⁴).

That is, the Petition only suggests modifying FIG. 8 of *Brommer* to include a joint amplitude estimator. But the Petition ignores that FIG. 8 only discloses a code processor 725 (which the Petition asserts is part of the claimed symbol estimator), and does not include the bank of decoders 90 of FIG. 1. The Petition refers to FIG. 8 as “provid[ing] additional detail regarding the implementation of *Brommer*’s system” but fails to connect the structure of the FIG. 1 embodiment and the FIG. 8 embodiment in any meaningful manner. (Pet. at 26-27).

⁴ Patent Owner has added notations to FIG. 8 in line with the mapping provided in the Petition.

The Petition provides no explanation of how *Brommer* discloses a bank of decoders in its FIG. 8 embodiment. Petitioners just assume the bank of decoders 90 in FIG. 1 of *Brommer* also is present in FIG. 8 without explaining how or why one would believe it is present in FIG. 8. Indeed, a POSITA would **not** think there is an additional component for a bank of decoders 90 in the embodiment of FIG. 8 as FIG. 8 already has a code processor 725 (already mapped by the Petition to the symbol estimator), which is responsible for implementing error correction coding. (EX2001 at ¶91).



(Pet. at 33-34; EX1004 at FIG. 1, annotated).

A POSITA would understand that because FIG. 8 already includes the code processor 725 implementing error correcting coding, there could not be an

additional bank of decoders, which would also implement error correcting codes, within the embodiment of FIG. 8. (EX2001 at ¶92).

The Petition does not identify a “bank of decoders” in *Lilleberg* because it cannot as *Lilleberg* is silent regarding any bank of decoders. (EX2001 at ¶93). Further, the Petition does not connect the description of feedback in *Lilleberg* to the bank of decoders in *Brommer* in any meaningful way to show that a “bank of decoders . . . producing a plurality of symbol likelihood estimates . . . iteratively fed back to . . . said joint amplitude estimator.” Accordingly, the Petition has failed to show any “bank of decoders . . . producing a plurality of symbol likelihood estimates for each user, wherein said symbol likelihood estimates are iteratively fed back to said symbol estimator and said joint amplitude estimator” as required by claim 1, even if a POSITA were to combine *Brommer*, *Lillieberg*, and *Hottinen* as proposed.

And further, a POSITA would not want to modify *Brommer*’s FIG. 8 embodiment to include a “bank of decoders 90” because *Brommer* already has a code processor 725 implementing an error correcting coding (and which the Petition alleges is the symbol estimator and therefore cannot be the claimed bank of decoders). (EX2001 at ¶94).

For this reason alone, the Petition fails to demonstrate that *Brommer* in view of *Lilleberg* in further view of *Hottinen* discloses or renders obvious claim 1 of the '703 patent.

B. Grounds 4-5

The Petition fails to show that *Frank* in view of *Zha* discloses or renders obvious claims 1-5 of the '703 patent for at least the reason that none of the asserted references disclose “a bank of decoders that produce symbol likelihood estimates for each user, wherein said symbol likelihood estimates are iteratively fed back to said symbol estimator and said joint amplitude estimator until a final condition is obtained,” as required by independent claim 1.

1. The Petition admits that *Frank* does not disclose a bank of decoders and there is no evidence that a bank of decoders exists in *Zha*

The Petition fails to demonstrate that *Frank* and *Zha* disclose the required “bank of decoders that produce symbol likelihood estimates for each user, wherein said symbol likelihood estimates are iteratively fed back to said symbol estimator and said joint amplitude estimator until a final condition is obtained.” The Petition admits that *Frank* does not disclose a bank of decoders and instead relies on *Zha*’s “soft decision rule” alleging that a POSITA would understand the “soft decision rule” to be a decoder. (Pet. at 60). The Petition relies solely on their expert Dr. Min

for this assertion and Dr. Min merely parrots the same statement as the Petition without explanation or support. (Pet at 60; EX1003 at 178).

But as explained above, any reasonable understanding of a decoder is one that implements an error correction coding approach. (EX2001 at ¶98; EX2003 at 3; EX2004 at 11; EX2005 at 228). A system utilizing error correction coding requires encoding, by an encoder at the transmitter, the user bits using error correction coding such as a convolution coding, soft-output Viterbi, Maximum A Posteriori, BCJR, or Turbo Coding. (EX2001 at ¶98; EX2003 at 293, 311; EX2004 at 11; EX2005 at 230-259). This approach also requires the decoder in the receiver to decode the received signal such that the receiver can output the decoded user bits. (EX2001 at ¶98; EX2003 at 293; EX2004 at 11; EX2005 at 228-229). Such an understanding is supported not only by Collision Communications expert Dr. Caire, but by numerous textbooks in the field, including Verdu, the text upon which the Petitioners rely. (EX2001 at ¶98; EX2003 at 3, 293; EX2004 at 11; EX2005 at 228; EX1012 at 37-38).

The “soft decision rule” of *Zha* involves no error correction coding. (EX2001 at ¶99). There is no encoder at the transmitter that encodes the user bits to introduce redundancy into the transmitted signal. (EX2001 at ¶99). Similarly, there is no decoder at the receiver that uses error correction codes to assess the structure of the received signal to identify and correct errors. (EX2001 at ¶99). *Zha*

only uses a soft decision rule to proportionally weigh a given bit and does not involve a system that uses an encoder to increase the number of bits-to-be-transmitted and a decoder that performs the opposite operation. (EX1010 at 743-744; EX2001 at ¶99). Accordingly, the “bit decision rule” in *Zha* has nothing to do with error correction coding and cannot reasonably be considered a decoder, let alone a bank of decoders. (EX2001 at ¶99). As a result, *Frank* and *Zha* fail to describe all elements of claim 1, and for this reason alone the Petition has not provided a reasonable expectation of success of showing at least one claim is unpatentable.

2. The Petition Provides No Explanation of How or Why One Would Combine *Zha* with *Frank* to Result in Claimed “Bank of Decoders”

The Petition admits *Frank* is silent to “a bank of decoders that produce symbol likelihood estimates for each user, wherein said symbol likelihood estimates are iteratively fed back to said symbol estimator and said joint amplitude estimator until a final condition is obtained” and asserts that a POSITA would modify *Frank* with *Zha*’s bit decision rule. (Pet. at 60). But the Petition ignores that *Frank* already describes a system using error correcting codes. (see, e.g., EX1006 at Abstract and ¶¶ [0010]; EX2001 at ¶100).

Because the Petition and Dr. Min ignore that *Frank* already describes a decoder utilizing error correcting codes, they are entirely silent as to how a

POSITA could make the proposed combination to result in “a bank of decoders that produce symbol likelihood estimates for each user, wherein said symbol likelihood estimates are iteratively fed back to said symbol estimator and said joint amplitude estimator until a final condition is obtained.” The Petition gives no explanation of how the “bit decision rule” of *Zha* is compatible with *Frank*’s error correcting codes or whether a wholesale substitution with further unexplained functional changes would be required. (EX2001 at ¶101). Indeed, expert Dr. Caire opines that it is unclear how a POSITA even could incorporate *Zha* into *Frank* to obtain the claimed “bank of decoders” as there would be many unexplained substantial functional changes to *Frank* for which the Petition is silent. (EX2001 at ¶101).

Moreover, even if a POSITA could make the proposed combination (they could not), the Petition does not adequately explain why a POSITA would implement the soft bit decision rule of *Zha* within *Frank*. (EX2001 at ¶102). *Frank* already utilizes error correcting codes. (EX2001 at ¶102). *Zha* states that the bit decision rule can “achieve a performance close to that of a single user bound”. (EX1010 at 743; Pet. at 52). But *Zha* is an uncoded system and this improvement is only applicable to a similar uncoded system. (EX2001 at ¶102). There is no explanation of how or why *Zha*’s bit decision rule for an uncoded system would improve or could be combined with *Frank*’s coded system, let alone that a

POSITA would understand and be motivated by the improvement. (EX2001 at ¶102).

This failure of the Petition to adequately explain how or why a POSITA would combine *Frank* and *Zha* to achieve the alleged advantage is another independent reason that the Petition has failed to show the challenged claims are unpatentable with respect to Grounds 4-5.

3. The Petition Provides No Explanation of How or Why One Would Combine *Zha*'s Successive Interference Cancellation with *Frank*'s Parallel Interference Cancellation

The Petition further fails to demonstrate that a POSITA would combine *Frank* and *Zha* because the Petition fails to explain how and why a POSITA would combine *Zha*'s improved amplitude averaging algorithm designed for a successive interference cancellation receiver with the ***parallel interference cancellation receiver*** disclosed in *Frank*.

First, the Petition's combination is entirely premised on combining *Zha*'s **successive** interference cancellation with *Frank*'s **successive** interference cancellation. (Pet. at 50-54). But all the *Frank* figures and embodiments relied by the Petition use **parallel** interference cancellation, not successive interference cancellation:

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. 1 is a block diagram illustrating a preferred receiver structure for MMSE equalization with parallel interference cancellation in accordance with the present invention.

[0013] FIG. 2 (divided into FIGS. 2A and 2B) is a combined block and flow diagram illustrating, in greater detail, a preferred receiver structure and method for MMSE equalization with parallel interference cancellation in accordance with the present invention.

[0014] FIG. 3 is a block diagram illustrating an apparatus embodiment of the preferred receiver structure for MMSE equalization with parallel interference cancellation in accordance with the present invention.

[0015] FIG. 4 (divided into FIGS. 4A and 4B) is a flow diagram illustrating a method embodiment for MMSE equalization with parallel interference cancellation in accordance with the present invention.

(EX1006 at ¶¶ [0012]-[0015]; EX2001 at ¶105).

And the Petition does not explain how a POSITA would combine the improved amplitude averaging algorithm designed for *Zha*'s successive interference cancellation with *Frank*'s parallel interference cancellation or how *Zha*'s successive interference cancellation teachings could be applied to *Frank*'s parallel interference cancellation. (See Pet. at 50-54). And for good reason—as established above but ignored by the Petition, a POSITA would understand that successive interference cancellation and parallel interference cancellation are fundamentally different cancellation techniques, and the two techniques cannot simply be mixed and matched as the Petition proposes. (EX2001 at ¶106).

Second, the *Frank* and *Zha* embodiments that Petitioners seek to combine are incompatible for additional reasons. For example, *Zha*'s time-based amplitude averaging algorithm (which the Petition vaguely proposes somehow using with *Frank*) requires that associated time delays are exactly known at the receiver. *Zha* states "[i]nitially, we assume that the time delays are exactly known at the receiver." (EX1010 at 743).

$$\mathbf{d}_k(i) = \delta_k \mathbf{c}_k(p_k + 1, i) + (1 - \delta_k) \mathbf{c}_k(p_k, i). \quad (5)$$

(EX1010 at 744). This known time delay— $\mathbf{d}_k(i)$ —is used in the amplitude averaging algorithm relied on by the Petition:

$$\bar{A}_k^{v+1} = \frac{1}{M} \sum_{i=1}^M \text{abs} \left(\text{Re} \left(e^{-j\theta_k} (\mathbf{d}_k(i))^H \bar{\mathbf{r}}_k^{v+1} \right) \right)$$

(Pet. at 50-54, 60; EX1010 at 744).

But *Zha* does not disclose how to achieve such required known time delays, nor does *Frank* disclose that time delays can be known in its disclosed wireless system as required by *Zha*'s amplitude averaging algorithm. (See EX1006; EX2001 at ¶108). The Petition does not explain how a POSITA would use an amplitude averaging algorithm that requires the time delays to be exactly known in a system where the time delays are not known. (See Pet. at 50-54, 60).

For these reasons alone, *Frank* in view of *Zha* fails to disclose or render obvious claim 1 of the '703 Patent.

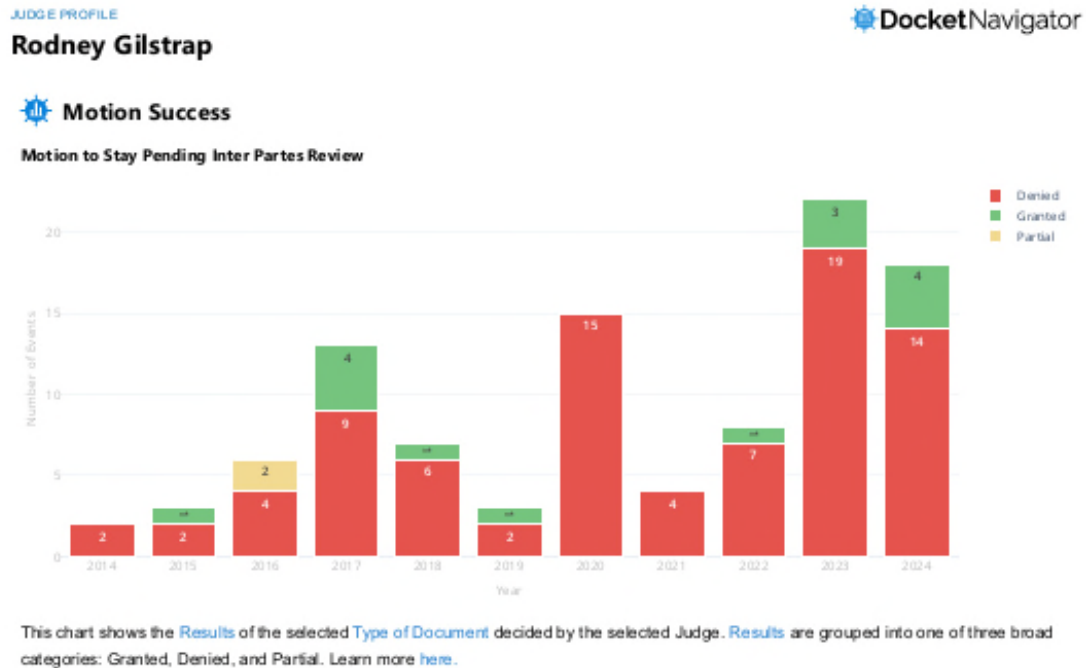
VI. The *Fintiv* Factors Heavily Favor Discretionary Denial Of Institution Under § 314(A)

Patent Owner is currently asserting the challenged patent against the parent company of Petitioners Lenovo (United States) Inc. and Motorola Mobility LLC in the Eastern District of Texas, which has set a trial date for January 5, 2026, which is over five months earlier than a final written decision in the requested IPR.

Accordingly (and as established below), the *Fintiv* factors heavily weigh in favor of discretionary denial. In an attempt to characterize every factor as either neutral or favoring institution, the Petition is rife with conclusory statements and misapplications of controlling PTAB precedent. Under the appropriate legal standards—and considering the totality of the record evidence—the *Fintiv* factors support discretionary denial of institution. PTAB’s recent rescission of the Guidance Memo only strengthens this support for a *Fintiv* discretionary denial.

A. Factor 1: Whether a stay exists or is likely to be granted if a proceeding is instituted

Petitioners admit that it has not sought a stay in the district court, and Patent Owner represents that it will not seek nor agree to a stay. Further, here other evidence exists that makes stay very unlikely. Over the past ten years, the presiding district court judge has denied over 83% of motions to stay pending *inter partes* review.



EX2007. Because the Petition does not even go as far to suggest that Petitioners will seek a stay, and because Judge Gilstrap has denied the overwhelming majority of motions to stay pending *inter partes* review, this factor weighs in favor of discretionary denial.

B. Factor 2: Proximity of the court’s trial date to the Board’s projected statutory deadline

Here, any final written decision would issue ***over five months*** after the trial date and a decision on the validity defenses presented therein. If the court’s trial date is earlier than the expected statutory deadline for the IPR’s final written decision, “the Board generally has weighed this fact in favor of exercising authority to deny institution.” *Fintiv*, IPR2020-00019, Paper 11 at 9. The trial date

is set for January 5, 2026, while the statutory final written decision, if the IPR was instituted, would be June 18, 2026.

Petitioners' suggestion that the PTAB should ignore this much earlier trial date in light of the Guidance Memo is improper because PTAB has withdrawn that Guidance Memo. *See* Pet. at 66-67. Moreover, there was no basis in the first place for Petitioners' speculation that "additional delays are likely." *See* Pet. at 67.

To the contrary, the evidence of record strongly supports the conclusion that trial will occur months before any final written decision would issue. According to the most recent statistics, the time to trial for the Eastern District of Texas is 21.6 months—squarely in line with the approximately 21-month schedule set by the district court. EX2008 (June 30, 2024 Federal District Court Case Management Statistics); EX2009 (Docket in *Collision Communications, Inc. v. Lenovo Group Ltd.*, No. 23-cv-00594 (E.D. Tex.) showing complaint filing date of Dec. 12, 2023); *see also Comcast Cable Communications, LLC v. Touchstream Technologies, Inc.*, IPR2024-00324, Paper 13 at 10 (PTAB July 24, 2024) ("Patent Owner's representation of median time-to-trial of twenty-one months is consistent with the most recent available data from the judiciary. . . . We find that the related district court litigation's trial date and the district court's median time-to-trial favor denial.") (discretionary denial granted upon rehearing); *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 9 (PTAB Mar. 20, 2020) (precedential) ("If the

court's trial date is earlier than the projected statutory deadline, the Board generally has weighed this fact in favor of exercising authority to deny institution under *NHK*.”).

Because any final written decision would issue substantially later than the district court trial, this factor weighs heavily in favor of discretionary denial. *See Verizon Bus. Network Servs. LLC v. Huawei Techs. Co. Ltd.*, IPR2020-01292, Paper 13 at 12 (PTAB Jan. 25, 2021) (trial date seven to eight months before expected final written decision deadline weighs in favor of discretionary denial).

C. Factor 3: Investment in the parallel proceeding by the court and parties

At best for Petitioners, this factor favors denial of institution or is neutral. Petitioners fail to evaluate the investment by both the court *and* the parties at the relevant time—at the deadline for institution. *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 9-10 (PTAB Mar. 20, 2020) (precedential). By the June 18, 2025, deadline for institution, the parties will have invested substantial resources in the following case events:

- Completion and service of invalidity contentions
- Completion of claim construction discovery
- Substantial completion of document production
- Exchange of privilege logs

- Filing of technical tutorials for claim construction
- Filing of opening claim construction brief
- Filing of responsive claim construction brief

EX2010 (Scheduling Order). Therefore, this case, particularly at the time of institution, will hardly be in the “very early stages of litigation” and discovery will not be in its preliminary stages. *See* Pet. at 67. The Parties will have expended significant resources on the district court litigation by the deadline for institution, which favors denial of institution. Finally, Petitioners provide no support for its contention that filing the Petition four months before the statutory deadline weighs against denying institution. *See id.* Conversely, filing the Petitions four months after receiving Patent Owner’s infringement contentions and notice of asserted claims weighs slightly in favor of denial of institution. *Comcast*, IPR2024-00324, Paper 13 at 15.

D. Factor 4: Overlap between issues raised in the petition and in the parallel proceeding

The Petition challenges the same claims as are asserted in the district court. Due to the substantial overlap in challenged claims and the similarity of Petitioners’ claims and theories, this factor weighs in favor of discretionary denial. *Fintiv*, IPR2020-00019, Paper 11 at 12-13 (“[I]f a petition involves the same prior art challenges but challenges claims in addition to those that are challenged in the

district court, it may still be inefficient to proceed because the district court may resolve validity of enough overlapping claims to resolve key issues in the petition.”).

Petitioners’ suggestion that this factor weighs in favor of institution if the Board addresses the overlapping validity issues before they are resolved by the district court is unfounded because the district court will resolve any overlapping validity issues several months before the Board issues its final written decision. *See* Pet. at 68. Institution will not thus preserve judicial resources; it will waste them by allowing Petitioners to challenge the same claims first in the district court and then again before the PTAB. The Board can save resources by discretionarily denying this petition and allowing the district court to adjudicate the validity of these claims under the same art nearly six months *before* the PTAB.

E. Factor 5: Whether the petitioner and the defendant in the parallel proceeding are the same party

Petitioners effectively concede that the parties materially overlap here. Two of the Petitioners (Lenovo and Motorola) admittedly manufacture the products accused of infringement in this district court and are subsidiaries of the named defendant. The products of the third petitioner (Intel) are likewise accused of infringement in the district court action. *See* Pet. at 68. Accordingly, this factor is not neutral as Petitioners argue without explanation, but instead favors denial. *See*

Sotera Wireless, Inc. v. Masimo Corp., IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020) (precedential as to § II.A); *see also Comcast*, IPR2024-00324, Paper 13 at 15.

F. Factor 6: Other circumstances that impact the Board’s exercise of discretion, including the merits / Compelling Merits

No other considerations warrant discretionary denial. As discussed above, Petitioner’ case does not even meet the “reasonable likelihood” standard for the statutory institution threshold. The Petition thus falls far short of showing “compelling merits.” *See* PTAB Director’s 2022 *Fintiv* Memorandum, 4 (“Compelling, meritorious challenges are those in which the evidence, if unrebutted in trial, would plainly lead to a conclusion that one or more claims are unpatentable by a preponderance of the evidence. . . . Where the information presented at the institution stage is merely sufficient to meet the statutory institution threshold, the PTAB has the authority, where warranted, to exercise discretion to deny institution in view of the other *Fintiv* factors.”). Accordingly, because the Petition fails to show compelling merits, and the *Fintiv* factors heavily support discretionary denial, the Board should deny institution.

VII. Conclusion

For the foregoing reasons, the Board should deny institution of the Petition.

Dated: March 18, 2025

Respectfully submitted,

/William A. Meunier/

William A. Meunier (Reg. No. 41,193)

Michael T. Renaud (Reg. No. 44,299)

Kevin C. Amendt (Reg. No. 69,361)

MINTZ, LEVIN, COHN, FERRIS,

GLOVSKY AND POPEO, P.C.

One Financial Center

Boston, MA 02111

Telephone: 617-542-6000

Facsimile: 617-542-2241

E-mails: WAMeunier@mintz.com;

MTRenaud@mintz.com;

KCAmendt@mintz.com

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Patent Owner hereby certifies, in reliance on the word count of the word-processing system (Microsoft Office Word 2010) used to prepare this preliminary response, that the number of words in this paper is 11,063. This word count excludes the tables of contents, tables of authorities, certificate of word count, certificate of service, and table of exhibits.

Dated: March 18, 2025

/William A. Meunier/

William A. Meunier (Reg. No. 41,193)

CERTIFICATE OF SERVICE

I certify that copies of Patent Owner's Preliminary Response and accompanying Collision Exhibits 2001 through 2017 are being served by electronic mail on the following counsel of record:

Vincent Y. Ling (Reg. No. 67,145)
vincent.ling@mto.com
MUNGER, TOLLES & OLSON LLP
350 South Grand Ave., 50th Floor
Los Angeles, CA 90071
Tel: (213) 683-9100
Fax: (213) 687-3702

Heather Takahashi (Reg. No. 78,418)
Adam Kwon (Reg. No. 75,653)
Zach Briers (pro hac vice pending)
Peter Gratzinger (pro hac vice pending)
MUNGER, TOLLES & OLSON LLP
350 South Grand Ave., 50th Floor
Los Angeles, CA 90071
Tel: (213) 683-9100
Fax: (213) 687-3702
lenovo-collision@mto.com

Timothy Riffe, Reg. No. 43,881
Jennifer Huang, Reg. No. 64,297
Whitney Reichel, Reg. No. 59,173
Lawrence Jarvis, Reg. No. 74,636
Fish & Richardson, P.C.
60 South Sixth Street, Suite 3200
Minneapolis, MN 55402
Tel: 202-783-5070
Fax: 877-769-7945
PTABInbound@fr.com
IPR55851-0026IP1@fr.com

Dated: March 18, 2025

/William A. Meunier/

William A. Meunier (Reg. No. 41,193)