

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS AMERICA, INC.,
SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

COLLISION COMMUNICATIONS, INC.
Patent Owner.

Case No. IPR2024-01500
U.S. Patent No. 7,463,703

**DECLARATION OF GIUSEPPE CAIRE REGARDING PATENT
OWNER'S PRELIMINARY RESPONSE FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 7,463,703**

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I, Dr. Giuseppe Caire, hereby declare as follows:

I. Introduction

1. My name is Giuseppe Caire. I have been retained in the above-referenced *inter partes* review proceeding by Collision Communications, Inc., to evaluate United States Patent No. 7,463,703 (the “’703 patent”) against certain references that are presented by the Petitioner. As detailed in this report, it is my opinion that the Petition does not establish that any of the challenged claims are anticipated or rendered obvious by the references presented by the Petitioner. If requested by the Patent Trial and Appeal Board, I am prepared to testify at trial about my opinions expressed herein.

II. Qualifications

2. I have over thirty years of experience in the field of electrical engineering. For the past nine years I have held a Full Professorship and faculty position as the Chair of Communications and Information Theory at Technische Universität Berlin. In my work and research, I have researched and written about Information Theory, Communication Theory and Coding Theory, Wireless Communication Systems, Signal Processing and Statistics.

3. Prior to my appointment at the Technische Universität, Berlin I was a tenured Full Professor at the University of Southern California, Los Angeles from 2005-2016. Although I am currently at the Technische Universität Berlin, I have

retained the title of Adjunct Research Professor at the University of Southern California, Los Angeles since 2016. Prior to my tenure at the University of Southern California, Los Angeles, I spent seven years as a Professor at Eurecom Institute, and held various Assistant Professorships from 1995-1998.

4. I studied Electrical Engineering and received my Ph.D. in 1994 from the Politecnico di Torino, my Master's Degree in 1992 from Princeton University, and my Bachelor of Science Degree in 1990 from the Politecnico di Torino. In addition to my studies at undergraduate and graduate levels and academic qualifications, I have held industrial research positions such as my current role as the Director of the Huawei-TU Berlin Joint Innovation Center, which has a focus on fundamental research in wireless technology.

5. I have authored or co-authored over four hundred publications in the areas of computer networks, and telecommunications. My publication and patents are listed on my curriculum vitae, which is attached hereto as EX2002.

6. In 2021, I was awarded the Leibniz Price, which is awarded to "exceptional scientists and academics for their outstanding achievements in the field of research" and known as the most important research award in Germany. In 2022, I was elected a Member of the Berlin Brandenburg Akademie der Wissenschaften (BBAW). Further, I served as President of the Institute of Electrical and Electronics Engineers (IEEE) Information Theory Society in 2011.

7. I am thanked in the preface of S. Verdu, *Multiuser Detection*, Cambridge University Press 1998, which is submitted by the Petitioner as EX1012.

8. As a result of my background in information and communication theory, I have extensive knowledge regarding the state of the technical art in this area at the time of filing of the '703 patent.

9. I am co-author of an article titled "Bit-Interleaved Coded Modulation" which was published in IEEE Transactions on Information Theory, Vol. 44, No. 3, May 1998 at pp. 927-946. This paper has been cited in other publications over thirty-three hundred (3300) times (Google Scholar).

10. In addition, I am co-author of an article titled "Iterative Multi-User Joint Decoding: Unified Framework and Asymptotic Analysis," which was published in IEEE Transactions on Information Theory 48, No. 7 (2002): 1772-1793. This paper has been cited 409 times, which makes it one of the most referenced papers on turbo multiuser joint decoding. In this paper, we presented the idea of feeding back to the MUD the soft-estimations of the symbols produced by the soft-output decoders and do partial interference cancellation in order to clean up the signal from interfering along the iterations.

III. Materials Considered

11. In preparing this declaration, I have reviewed the specification and claims of the '703 patent (EX1001) and the file history of the '703 patent (EX1002).

I understand the '703 patent was issued on December 9, 2008, from U.S. Patent Application No. 10/531,772.

12. I have also reviewed the Petition, declaration of Dr. Paul S. Min (EX1003) and all publications and exhibits cited in the Petition and declaration of Dr. Paul S. Min including:

- U.S. Patent No. 6,826,140 to Brommer et al (“Brommer” EX1004).
- U.S. Patent No. 7,190,743 to Learned (“Learned” EX1005).
- U.S. Patent Pub. No. 2003/0035469 to Frank et al. (“Frank” EX1006).
- U.S. Patent No. 5,905,946 to Lilleberg et al. (“Lilleberg” EX1007).
- U.S. Patent No. 6,898,248 to ElGamal et al. (“ElGamal” EX1008).
- U.S. Patent No. 5,995,499 to Hottinen et al. (“Hottinen” EX1009).
- Zha et al., “Soft-Decision Successive Interference Cancellation CDMA Receiver with Amplitude Averaging and Robust to Timing Errors,” in Proc. IEEE Global Telecommunications Conference, 2001 (GLOBECOM '01), vol. 2, 2001, pp. 743-747 (EX1010).
- S. Verdu, “Computational Complexity of Optimum Multiuser Detection,” *Algorithmica* (1989) (EX1011).
- S. Verdu, *Multiuser Detection*, Cambridge University Press 1998 (“Verdu” EX1012).

- Shimon Moshavi, “Multi-User Detection for DS-CDMA Communications,” in IEEE Communications Magazine, Oct. 1996, pp. 124-136 (EX1013).

13. I have also reviewed relevant parts of the publications and exhibits cited in this declaration, including the following publications:

- U. Madhow, *Fundamentals of Digital Communication*, Cambridge University Press 2008 (“Madhow” (EX2003));
- R.G. Gallager, *Principles of Digital Communication*, Cambridge University Press 2008 (“Gallagher” (EX2004)); and
- A. Goldsmith, *Wireless Communications*, Cambridge University Press 2005 (“Goldsmith” (EX2005)).

IV. Wireless Communication Background

14. The challenged claims generally concern wireless communication systems with multiple signals. More specifically, the claims are directed to an improved apparatus that applies a bank of decoders to produce a plurality of symbol likelihood estimates for each user. Once symbol likelihood estimates are produced, the symbol likelihood estimates are fed back to the symbol estimator and a joint amplitude estimator until a final condition is reached.

15. To provide context for the claimed subject matter and Samsung’s Petition, the following brief background addresses the following topics:

- uncoded systems vs. coded systems;

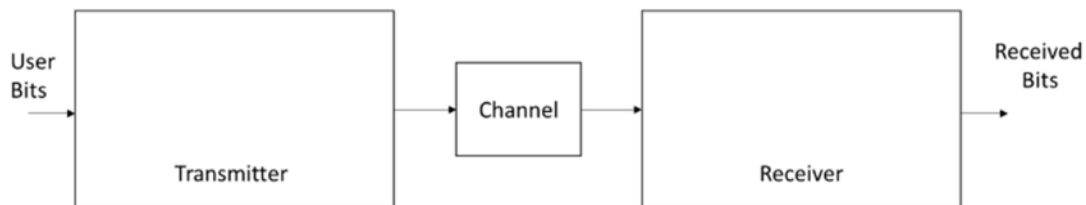
- soft bit decisions vs. hard bit decisions; and
- successive interference cancellation vs. parallel interference

cancellation.

A. Material Differences between Coded Systems and Uncoded Systems

16. A typical wireless transmission generally involves a transmitter and receiver at opposite ends of a wireless channel. An original signal is input at the transmitter and a recovered signal is calculated at the receiver.

17. As illustrated in the simplified figure below, an original information signal in the form of user bits (sequences of 0s and 1s) is input to the transmitter. The transmitter converts those bits into an analog carrier waveform and then transmits that carrier waveform over the wireless channel to the receiver. (EX2003 at 2-4; EX2004 at 1-5, 95, 181-183, 208-209). The receiver receives the waveform and attempts to recover the original signal by converting the received waveform into received bits. (EX2003 at 2-4; EX2004 at 3-5).



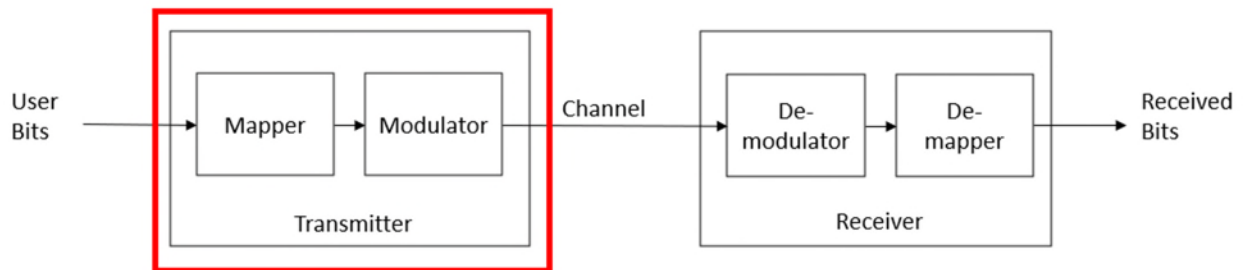
(Based on FIG. 1.1 of EX2003).

There are two classes of wireless transmission systems: uncoded systems and coded systems.

1. Uncoded Systems

18. An uncoded system transmits data without use of error correction coding. In an uncoded system, a transmitter includes a **mapper** that maps user bits to different symbols. (EX2003 at 2-3, 7, 45-46, 107). As illustrated below, in a digital communication system, the transmitter typically includes this mapper along with a modulator. (EX2003 at 2-3, 107; EX2004 at 3-5).

Uncoded System

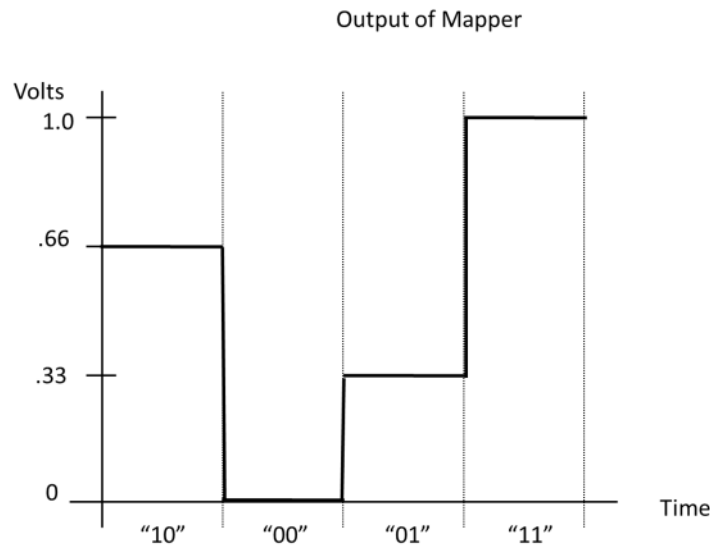


(Based on FIG. 1.1 of EX2003).

19. The user bits are input to the **mapper**, which maps the user bits to symbols. (EX2003 at 7; EX2004 at 181-209). For example, to send a user bit sequence of “10000111”, the mapper would take each 2-bit sequence, and map it to its corresponding symbol. Using a bit-and-symbol correlation identified below, the sequence “10000111” would be broken into its composite bit sequences 10, 00, 01, and 11, which would be mapped to the voltages .66, 0.0, .33, and 1.0 respectively.

2-Bit Sequence	Symbol (Wave Amplitude)
"00"	0
"01"	.33
"10"	.66
"11"	1.0

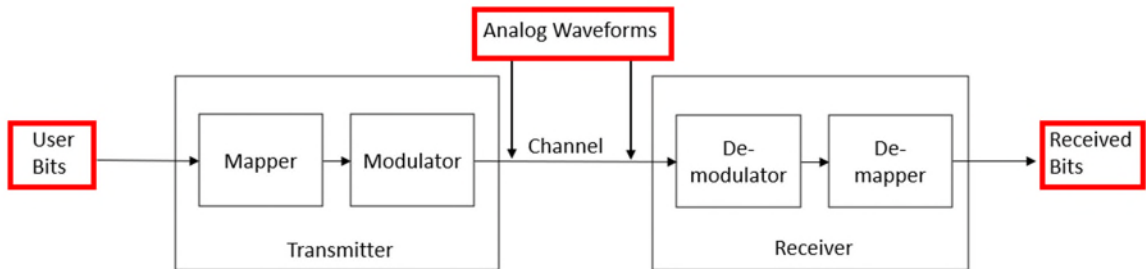
20. The resulting output of the example mapper is the sequence 0.66, 0.0, 0.33, and 1.0 shown in the following figure, in which the y-axis represents voltage and the x-axis represents time. For reference, the transmitted bit sequence is shown for each time slot below the figure.



21. Next, the mapper provides these symbols to the transmitter's **modulator**, which creates a waveform to be modulated to reflect the symbol values provided by the mapper and then be sent through the channel. (EX2004 at 3,

EX2004 at 6-7). There are numerous different ways for a modulator to apply such information to a carrier waveform. (EX2003 at 2-3; EX2004 at 181-209). For example, in our illustration, the modulator can modify (modulate) the amplitude of the carrier waveform so that the waveform's different amplitudes will match the mapped symbols output by the mapper.

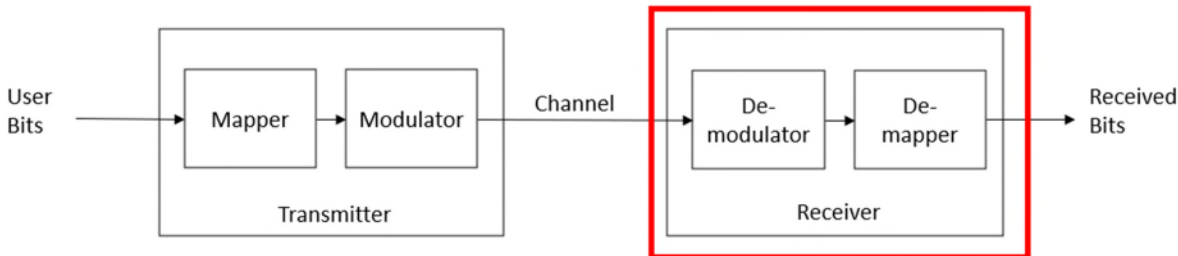
Uncoded System



(Based on FIG. 1.1 of EX2003).

22. The receiver in the uncoded system typically mirrors the transmitter and includes: a de-modulator and a demapper.

Uncoded System



(Based on FIG. 1.1 of EX2003).

23. The **demodulator** receives the modulated waveform via the channel and attempts to extract the waveform's symbol values (in our example, amplitude). (EX2003 at 3-4; EX2004 at 4-7).

24. The extracted symbol values are then input to the **demapper**, which is used to help identify which bit sequence may correspond to the extracted symbol values. (EX2003 at 3-4, 43-46; EX2004 at 4-7). But because of noise in the transmission, the demodulated symbol values signal may not be identical to the symbol values output from the demapper. (EX2003 at 43-46). The demapper has two types of decision rules for handling variations in the symbol values: hard decisions and soft decisions (discussed more below). The hard decisions and soft decisions determine symbol estimates of the recovered user bits.

2. Coded Systems

25. A coded system is one that incorporates error correction coding to identify and correct errors introduced during transmission. (EX2003 at 3; EX2005 at 228).

26. Error correction coding is a technique used for controlling errors in data transmissions over unreliable or noisy channels. (EX2003 at 293; EX2005 at 228-229). The approach includes the transmitter taking the sequence of user bits that are input to the transmitter and encoding (e.g., modifying) the sequence to add redundancy, which increases the number of bits that are transmitted from the

transmitter to the receiver. (EX2003 at 2-3, 293; EX2004 at 11; EX2005 at 229-231). The receiver takes the received signal, which includes the longer sequence of bits having redundancy, and decodes the signal to output the shorter sequence of bits representing the original user bits. (EX2003 at 2-3, 293; EX2004 at 11; EX2005 at 228-229). Using error correction coding, the decoding process can identify, and in some cases correct, any bits that were corrupted during transmission due to noise. (EX2003 at 2-3, 293; EX2004 at 11; EX2005 at 228-229). By implementing error correction coding, increased system performance can be achieved. (EX2003 at 3; EX2004 at 11; EX2005 at 228).

27. Consider the following simple example to illustrate the concept of error correction coding. Assuming a transmitter receives a sequence of 3 user bits “010”. The example transmitter encodes the sequence by introducing 2 additional redundant bits for each user bit. (EX2004 at 11). This simplified example includes repeating each input user bit such as encoding “010” to “000111000”. (EX2004 at 11). This increases the length of the bit sequence that is transmitted by 3 times (from 3 bits to 9 bits). (EX2004 at 11). Such an approach would be considered to have a code rate of 1/3 (indicating for every 1 bit input, 3 bits are output). (EX2004 at 11; EX2005 at 228-229).

28. Continuing the simple example, the transmitter will modulate and transmit the longer encoded bit sequence (“000111000”) through the channel to the

receiver. (EX2004 at 11). After demodulation by the receiver, and because of noise introduced during transmission, the received bit sequence may not match the transmitted bit sequence. (EX2004 at 11). For the purposes of the example, assume the receiver demodulates the wireless signal to “010011000”. Note that the 2nd and 4th received bits are different from their corresponding bits in the transmitted bit sequence. The decoder, knowing that the transmitted bit sequence was structured such that every 3 bits were identical, can process the received bit sequence “010011000” and identify that there is an error in the first 3 bits and another error in the second 3 bits. (EX2004 at 11). Thus, the decoder can identify that errors are present in the received bit sequence. (EX2004 at 11).

29. Further, the decoder in the example could correct the errors by determining which value of the bit (“0” or “1”) occurs more frequently in each set of 3 consecutive bits and choose that bit type as the final output bit type¹. (EX2004 at 11). Thus, in the example, the decoder can identify that a “0” occurs more frequently for the first 3 bits, a “1” occurs more frequently for the second set of 3 bits, and a “0” occurs more frequently for the third set of three bits and determine

¹ In the example, for simplicity of discussion, the decoder performs “hard” bit decisions. However, a decoder can be implemented to perform “soft” bit decisions that reflect a likelihood a given bit type (“0” or “1”) is correct.

they are the most likely correct bits. In this instance, the receiver will output “010” as the final user bits. (EX2004 at 11). Such error identification and correction is possible because of the redundancy and increase in the number of transmitted bits.

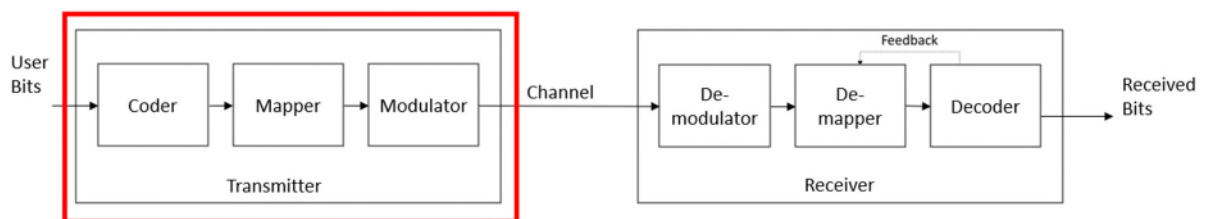
30. While the above example provides a simple error correction coding approach, there are a wide range of error correction coding approaches utilized in the field of communications that introduce redundancy into the bit sequence in different manners. (EX2003 at 2-3, 293; EX2004 at 11; EX2005 at 228-229). Examples of error correction coding approaches include convolutional codes, Walsh codes, turbo codes, low-density parity-check codes, polar codes, binary algebraic block codes (e.g., BCH codes), or non-binary algebraic block codes (e.g., Reed-Solomon codes). (EX2003 at 293, 311; EX2004 at 11; EX2005 at 230-259). Additionally, various types of decoders exist for processing error correction schemes, including Viterbi decoders, BCJR decoders, turbo decoders, belief propagation iterative decoders, polar decoders, hard decision and soft-decision algebraic decoders. (EX2003 at 293, 311; EX2004 at 11; EX2005 at 230-259).

31. Notably, any error correction coding approach will necessarily involve the encoder increasing the number of bits to-be-transmitted, and the decoder will necessarily perform the inverse operation such that the number of final received user bits is decreased from what was transmitted over the channel. (EX2003 at 293; EX2005 at 230). Processing units that do not involve the use of any error correction

coding that adds redundancy in some form into the transmitted bit sequence cannot reasonably be considered to be an encoder or decoder. (EX2003 at 2-3, 293; EX2005 at 230).

32. As described above, error correction coding is implemented using a ***coder*** at the transmitter, and a ***decoder*** at the receiver. As illustrated below, in a digital communication system, the transmitter typically includes the coder in the processing stream before the mapper and the modulator. (EX2003 at 2-3, 107; EX2004 at 3-5).

Coded System

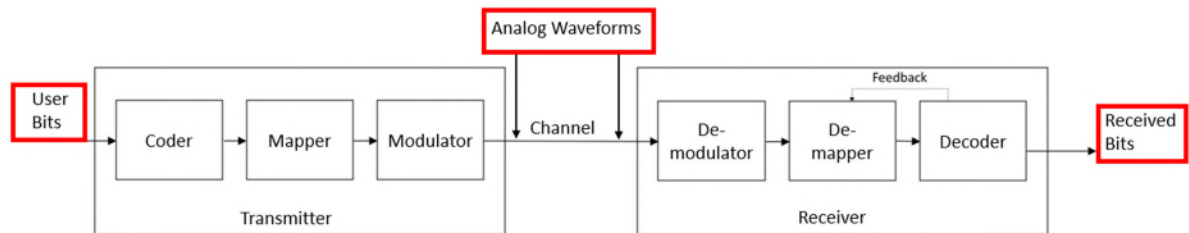


(Based on FIG. 1.1 of EX2003).

33. The ***coder*** increases the number of user bits into a longer sequence of bits that includes redundancy and error-correcting features to enable error correction at the receiver. (EX2003 at 2-4, 107; EX2004 at 6-7). This longer sequence of bits makes the transmission more robust against noise or disruptions in communication channels.

34. The resulting new bit sequence from the coder is input to the **mapper** which maps this new sequence to symbols. (EX2003 at 7; EX2004 at 181-209). Similar to the uncoded system, the mapper in the coded system provides these symbols to the transmitter's **modulator**, which creates a waveform that can be sent through the channel. (EX2004 at 3, EX2004 at 6-7).

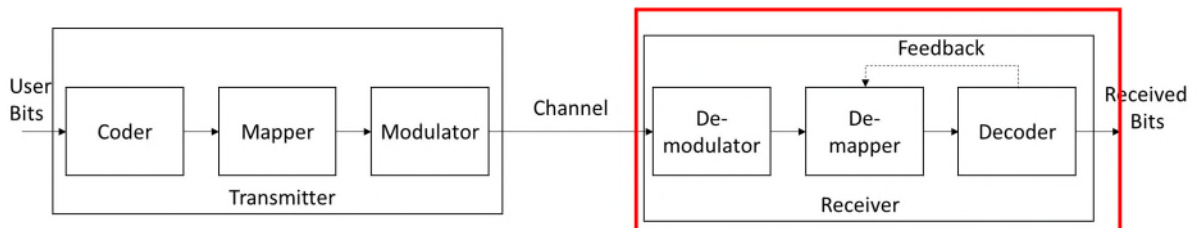
Coded System



(Based on FIG. 1.1 of EX2003).

35. Like the uncoded system, the receiver in the coded system typically mirrors the transmitter and includes: a de-modulator, a demapper, and a decoder.

Coded System



(Based on FIG. 1.1 of EX2003).

36. The **demodulator** receives the modulated waveform via the channel and attempts to extract the waveform's symbol values (in our example, amplitude). (EX2003 at 3-4; EX2004 at 4-7).

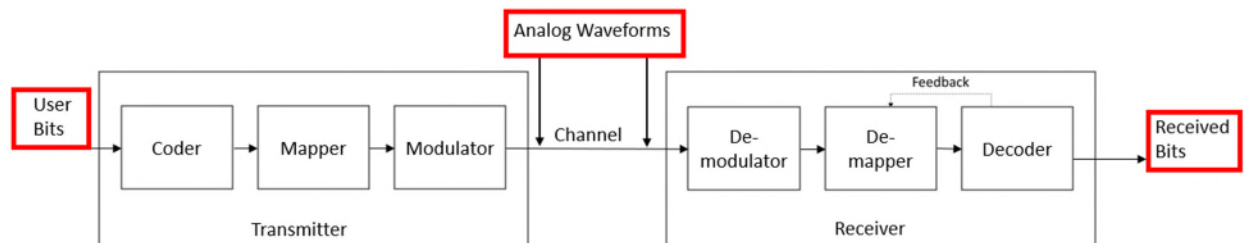
37. The extracted symbol values are then input to the **demapper**, which is used to help identify which bit sequence may correspond to the extracted symbol values. (EX2003 at 3-4, 43-46; EX2004 at 4-7). But because of noise in the transmission, the demodulated symbol values signal obtained from the demapper may not be identical to the symbol values output from the mapper at the transmitter side. (EX2003 at 43-46). The demodulated symbol values may also include likelihood information that estimates whether a particular bit is 0 or 1.

38. The **decoder** implements the error correction coding technique, as described above, to identify and eliminate errors in the symbol values. In particular, the decoder reconstructs the original signal using the output of the demapper, applies the error correction coding, and reconstructs the original signal. (EX2003 at 3-4; EX2004 at 11).

39. In light of the foregoing, an uncoded system cannot be improved by simply adding a decoder at the receiver side. The transmitter does not perform channel encoding, a decoder at the receiver side is useless. (EX2003 at 2-3; EX2005 at 228). On the other hand, only introducing an encoder at the transmitter side without the corresponding decoder at the receiver side is also useless and does not result in a performance improvement. (EX2003 at 3; EX2005 at 228). Both types of systems have different methods of recovering user data. (EX2003 at 75; EX2005 at 256-258). For example, the uncoded system applies decisions rules to obtained

symbols to recover the user bits. (EX2003 at 75). On the other hand, the coded system applies a coding scheme with an increased number of bits to eliminate errors and identify the appropriate bit sequences. (EX2003 at 75; EX2004 at 11). The coding scheme is also determined prior to the transmission over the channel and is independent of unique signal paths and their corresponding interference. (EX2003 at 2-3, 293; EX2004 at 11; EX2005 at 228-229).

40. The derivation of data bit decisions does not imply the existence of a coded system having a bank of decoders because the derivation of data bit decisions does not result in introduction of redundancy into the bit sequence to-be-transmitted. (EX2003 at 107).



(Based on FIG. 1.1 of EX2003).

B. Soft Data Bit vs Hard Data Bit Decisions in Uncoded Systems

41. As discussed, a demodulator extracts symbol values from the waveform and passes the extracted symbols to the **demapper**. (EX2003 at 3-4; EX2004 at 4-7). The task of the demapper is to associate an observed symbol value with a reference point in a space of observations to form a bit sequence. (EX2003 at 43-46

and 89, EX1012 at 85). That is, the demapper identifies a bit sequence corresponding to the extracted symbol values. (EX2003 at 3-4, 43-46; EX2004 at 4-7).

42. But extracted symbol values signal may not be identical to the symbol values generated at the transmitter side due to noise in the channel. (EX2003 at 43-46). To address variations in observed symbol values from extracted symbol values, the demapper applies **decision rules** to the extracted symbol values. (EX2003 at 75; EX2005 at 81). Decisions may be divided into two categories: hard decisions or soft decisions. (EX2003 at 75; EX2005 at 238). The demapper applies either hard decisions or soft decisions to the extracted symbol values. (EX2003 at 75; EX2005 at 238).

43. Hard decisions include requiring the demapper to assume whether a particular bit is 0 or 1. (EX2003 at 3; EX2005 at 238). For example, a demapper may observe a sequence of voltages having magnitudes of 0.66, 0.05, 0.48, and 1.05. The demapper may take each voltage from the sequence and map the voltage to a corresponding 2-bit sequence. Using the bit and symbol correlation identified below, an expected symbol value or expected sequence of voltages of 0.66, 0.0, 0.33, and 1.0 could be mapped to a bit sequence:

2-Bit Sequence	Symbol (Wave Amplitude)
----------------	----------------------------

“00”	0
“01”	.33
“10”	.66
“11”	1.0

44. But some observed voltages (i.e., 0.05V, 0.48V and 1.05V) are not exact matches to a symbol in the mapping: although there is a deviation between the observed voltage amplitude and the desired voltage magnitude, the demapper may apply hard decisions that assume that the voltages having magnitudes of 0.05, 0.48, and 1.05 are to be mapped to bit sequences 00, 01, and 11.

45. But sometimes the assumptions of hard decisions are incorrect. For example, the observation of 0.48V received more channel interference than the other observed voltages. The transmitted voltage magnitude may have been 0.66V and the channel distorted the symbol to 0.48V. Applying the mapping of bit sequence “01” instead of bit sequence “10” for the observed voltage of 0.48V is an error due to the assumption made by the hard decision.

46. In contrast to hard decisions, soft decisions estimate the likelihood that a particular bit is 0 or 1. (EX2003 at 3; EX2005 at 238).

C. Successive Interference Cancellation vs. Parallel Interference Cancellation

47. There at least two distinct approaches to interference cancellation: (1) successive interference cancellation; and (2) parallel interference cancellation. I understand the Petition highlights and relies on the material differences between the two approaches because its sole argument for combining Grounds 4-5 *Frank* and *Zha* references is its assertion that they both use the successive approach to interference cancellation. (E.g., Pet. at 49-52). Momentarily putting aside the baselessness of Samsung's conclusion (which is akin to arguing it is obvious to import any and all features from a gas engine into an electric engine because they both drive a vehicle's wheels), the entire premise for this obviousness argument is demonstrably false: while *Zha* does indeed use successive interference cancellation, every *Frank* embodiment that Samsung seeks to combine with *Zha* is explicitly and expressly parallel interference cancellation. (E.g., EX1006 at ¶¶ [0012]-[0015]). Unable to assert, much less support, how these disparate approaches would and could be combined, I understand the Petition just pretends they both use successive interference cancellation and does not address the distinct differences between the two. The following provides that missing information.

48. ***Successive Interference Cancellation:*** As the name suggests, successive interference cancellation attempts to identify and isolate the channel's

multiple signals one after the other. For example, if there were ten signals present in a channel's information stream, the receiver would first try to identify and isolate just one of those signals, ignoring the remaining nine signals as interfering noise. Once this first signal is recovered, its information is subtracted (cancelled) from the original information stream.

49. The receiver then attempts to recover a second signal from the resulting smaller residual information stream, again ignoring the remaining signals as interfering noise. Once this second signal is recovered, it, too is subtracted (cancelled) from the information stream.

50. This successive process continues, with a third signal being recovered and subtracted, a fourth signal being recovered and subtracted, *etc.*, until the information stream comprises only information for the last signal. This information is then used to recover that final signal, completing the successive interference cancellation process.

51. ***Parallel Interference Cancellation:*** In contrast, in a parallel interference cancellation process, the receiver does not attempt to recover signals one at a time, one after the other. Instead, the receiver attempts to recover all of the signals at the same time.

52. Consider again our example of ten user signals present in a single channel's information stream. In parallel interference cancellation, the receiver will

attempt to isolate and recover all ten signals at the same time. For example, the receiver may try to simultaneously subtract from each signal the interfering information for the other nine signals. For each of the ten resulting sets of information, the receiver will then attempt to reconstruct its corresponding signal.

53. Because the reliability of these initial cancellations and reconstructions is typically low, the process will continue iteratively, with the receiver repeatedly recalculating and subtracting from each signal the interfering information for the other nine signals, until reliable cancellations, symbols, and signals are achieved.

V. The '703 Patent's Bank of Decoders with Feedback to a Joint Amplitude Estimator

54. The '703 Patent and its challenged claims generally concern wireless communication systems with multiple signals. More specifically, the claims are directed to an improved apparatus that applies a bank of decoders to produce a plurality of symbol likelihood estimates for each user. Once symbol likelihood estimates are produced, the symbol likelihood estimates are fed back to the symbol estimator for error correction and a joint amplitude estimator.

55. The '703 Patent addresses extracting the correct data for a given user following transmission with interference and multipaths. (EX1001 at 2:64-66). Extracting user data can be further complicated when the number of users exceeds the number of dimensions (*e.g.*, time slots, frequency slots, polarizations, *etc.*) in a

system, resulting in an *overloaded condition*. (EX1001 at 2:66-3:2). Overloaded conditions can exist where the number of simultaneous users is doubled or tripled relative to the number of dimensions (e.g. time slots, frequency slots, polarizations, *etc.*). (EX1001 at 7:3-15).

56. The '703 Patent improves over prior systems by delivering better performance while accommodating *overloaded conditions*. (EX1001 at 5:50-52).

A. Exemplary Architecture

57. The '703 Patent describes overcoming the problems of *overloading* by providing turbo decoding based on an iterative decoding solution that exploits error correction codes. (EX1001 at Abstract). The methods and embodiments of the joint symbol estimator, the joint amplitude estimator, and the bank of decoders can provide high quality real-time processing for multiple access systems, including *overloaded situations*. (EX1001 at 11:33-37, 13:67-14:2). FIG. 2 of the '703 Patent illustrates an example system, which includes bank of decoders 130 providing feedback to both the symbol estimator 105 and joint amplitude estimator 120.

58. An exemplary receiver architecture illustrated in '703 Patent Figure 2 includes an initial amplitude estimator 110 (highlighted below in red), a symbol estimator 105 (blue), a bank of decoders 130 (yellow), and a joint amplitude estimator 120 (green):

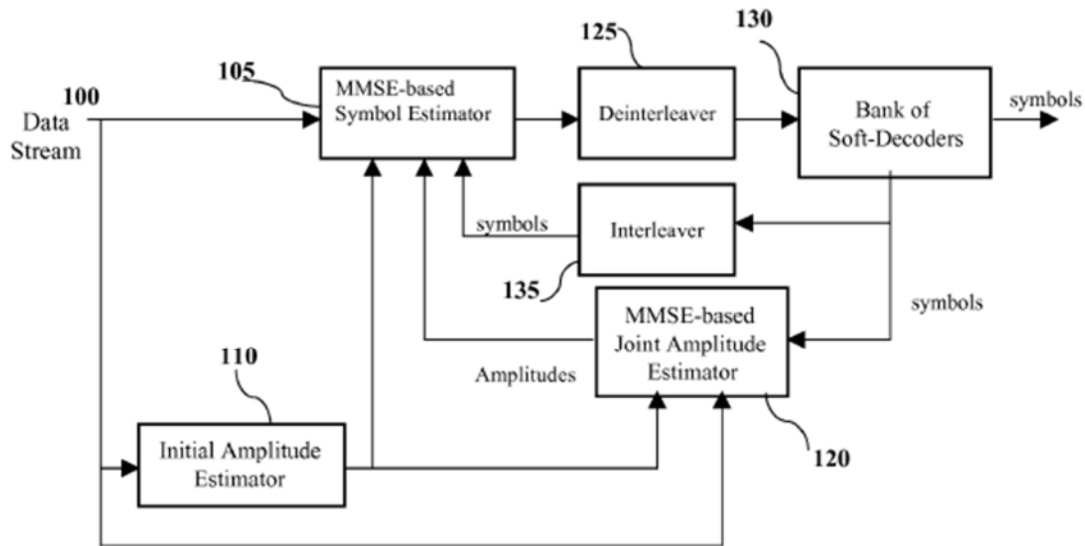


Figure 2

(EX1001 at Figure 2).

59. For a high-level overview (as illustrated above in Figure 2 and described in more detail below), this architecture works as follows:

(1) the received multi-user data stream 100 is provided to the initial amplitude estimator 110, which detects active users and calculates an initial estimate of the amplitude of each user signal in the stream (EX1001 at 15:25-44);

(2) these initial amplitude estimates are provided (along with the data stream) to the symbol estimator 105, which uses that data to estimate symbols for each user (EX1001 at 15:43-51, 16:3-7, 16:43-48);

(3) those symbol estimates are provided to the bank of error-correcting decoders 130, which calculate probabilities for the symbol estimates (in other words, how likely those symbols are correct) (EX1001 at 8:65-9:1, 16:8-14, 16:39-42);

(4) the symbol likelihoods from the decoder are passed to the joint amplitude estimator, which uses that information to calculate updated amplitude estimates, which are provided to the symbol estimator so that it can use them to calculate updated symbol estimates (EX1001 at 16:39-42, 18:65-20:52); and

(5) the symbol estimator, decoders, and joint amplitude estimator continue this cycle to iteratively calculate and provide information to one another (the joint amplitude estimator providing updates amplitude estimates to the symbol estimator, which in turn provides updated symbol estimates to the decoders, which in turn provides symbol likelihoods to the joint amplitude estimator, starting the cycle all over again) until some criteria is met, such as reaching a maximum number of iterations or a desired error rate (EX1001 at 16:39-52, 20:41-52).

60. ***Initial Amplitude Estimator:*** As illustrated below, the exemplary initial amplitude estimator 110 receives the multi-user data stream 100:

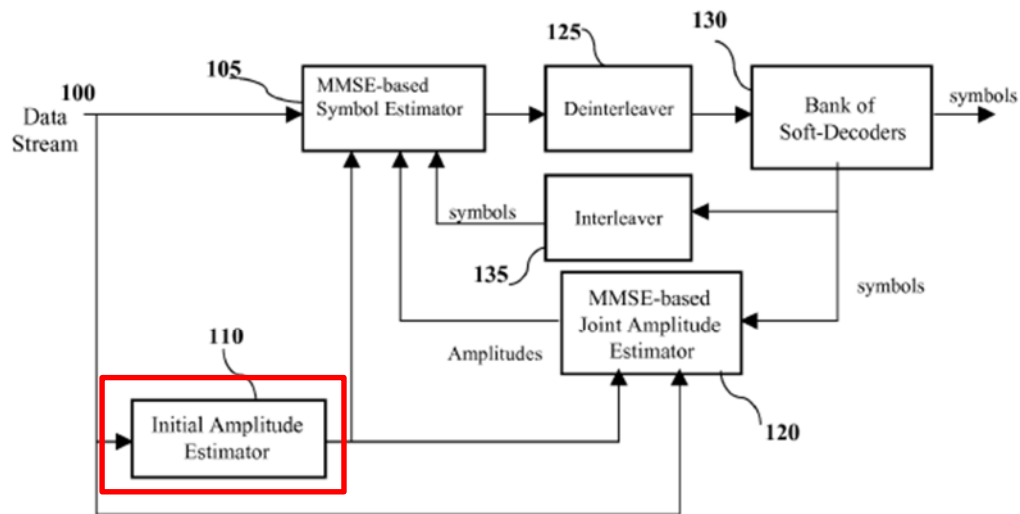


Figure 2

(EX1001 at Figure 2, 15:25-27).

61. This initial amplitude estimator uses energy detection to identify which users are active within the channel's data stream. (EX1001 at 15:35-44). It then integrates the energy out of a filter for all active users to compute an initial estimate for the amplitude of each active user's signal. (EX1001 at 15:26-34).

62. As illustrated above, the initial amplitude estimates are passed to the exemplary symbol estimator 105 and to the joint amplitude estimator 120.

63. **Symbol Estimator:** During the first iteration of the process, exemplary symbol estimator 105 receives the data stream 100 and the initial amplitude estimator 110's initial amplitude estimates:

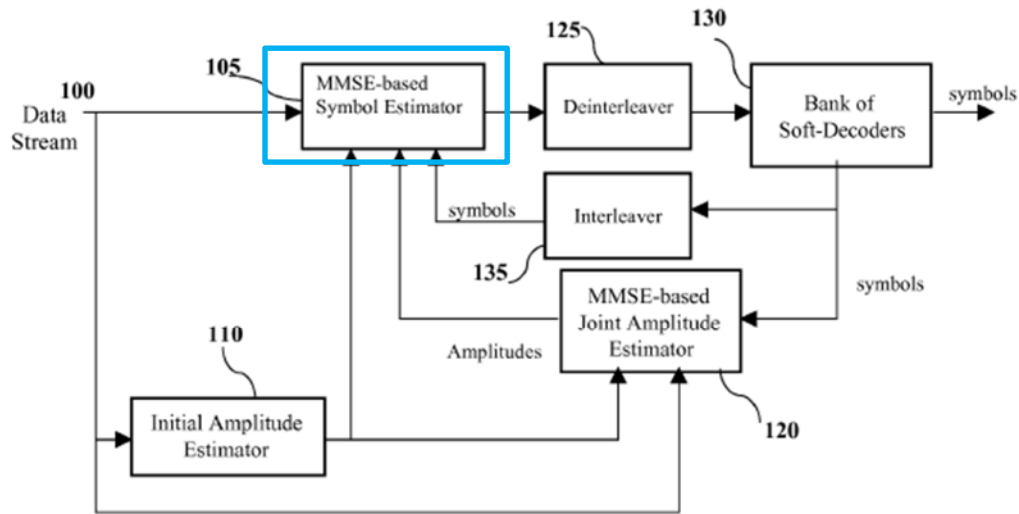


Figure 2

(EX1001 at Figure 2, 15:42-53).

64. The symbol estimator then uses that data to estimate symbols for each user. (*Id.*).

65. The symbol estimator uses the initial amplitude estimates to compute symbol estimates only during the first cycle/iteration. (EX1001 at 15:42-53). During all other iterations, the symbol estimator uses updated amplitude estimates from the joint amplitude estimator (along with other information, such as prior information on the symbols) to re-estimate the symbols. (EX1001 at 15:42-53, 16:43-52).

66. **Decoders:** The symbol estimates from the symbol estimator are routed to the exemplary decoders 130.² (EX1001 at 16:3-7). The decoders calculate the likelihood for each estimated symbol and then routes those estimated symbols and their respective likelihoods to various units, including joint amplitude estimator 120:

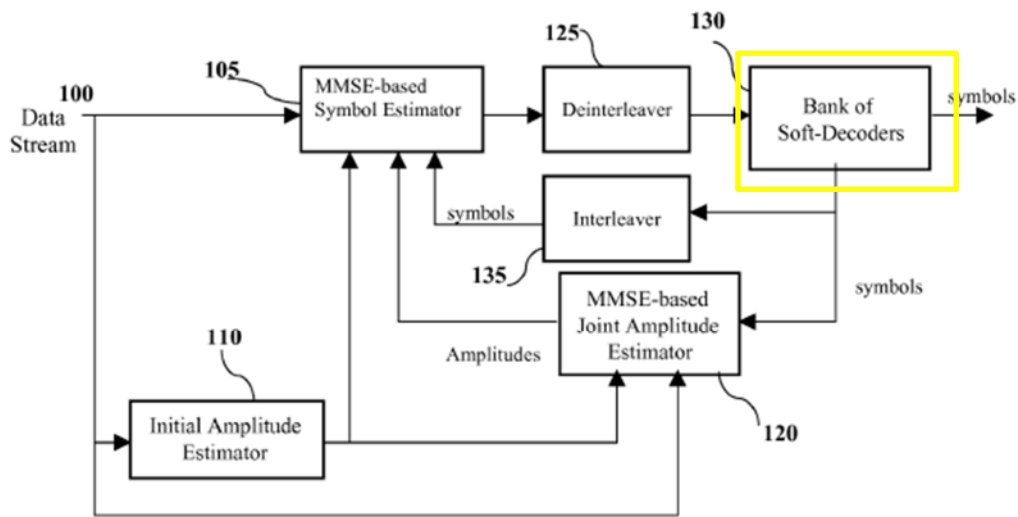


Figure 2

(EX1001 at Figure 2, 16:39-42, 18:65-20:52).

67. **Joint Amplitude Estimator:** Disclosed architecture embodiments include a joint amplitude estimator (discussed in more detail in the following

² For purposes of this general overview, details concerning other disclosed blocks, such as the deinterleaver 125 and interleaver 135 are omitted. (See, e.g., EX1001 at 16:15-28).

section) apart from the initial amplitude estimator, symbol estimator, and decoders. After the initial amplitude estimator provides the initial amplitude estimate, all updated amplitude estimates are computed and provided to the symbol estimator by and from exemplary joint amplitude estimator 120:

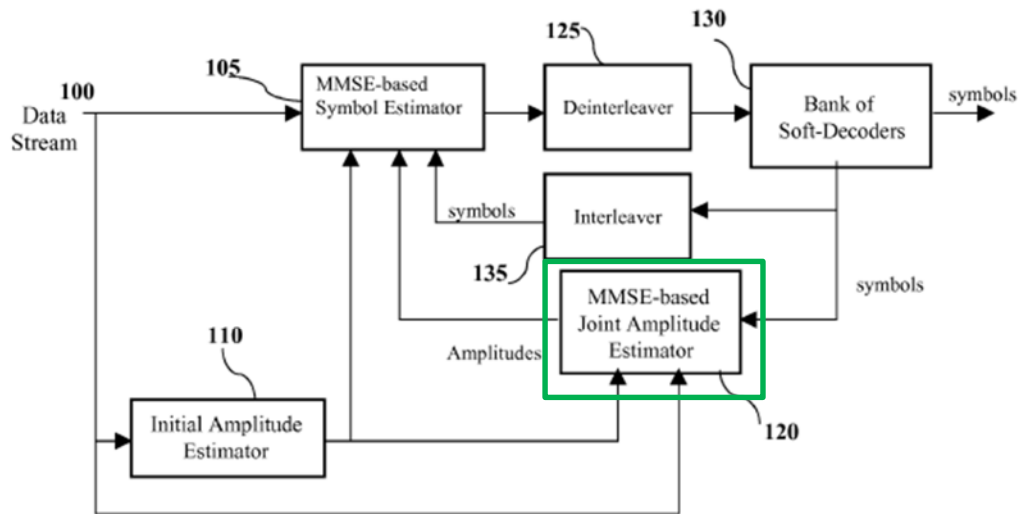


Figure 2

(EX1001 at Figure 2, 16:39-42, 18:65-20:52).

68. These updated amplitude estimates are based on the symbol likelihoods from the decoders and are provided to the symbol estimator to start a new cycle of computations, which continues and repeats until a predefined condition is met:

The new symbol likelihoods from decoders 130 are used to update previous amplitude estimates in the joint amplitude estimator 120. ... The new amplitude estimates from the join amplitude estimator 120 are passed to the MMSE-based Symbol Estimator 105 that re-estimates the symbols based on prior information on the symbols and updated parameter estimates. These updates symbol estimates from the symbol estimator 105 are then re-routed to the bank of decoders 130. This

process is repeated for either some fixed number of iterations or until estimates of the bit error rate or frame error rate achieve some desired level.

(EX1001 at 16:39-52).

69. The blocks involved in this exemplary iterative cycle are outlined in dotted blue below:

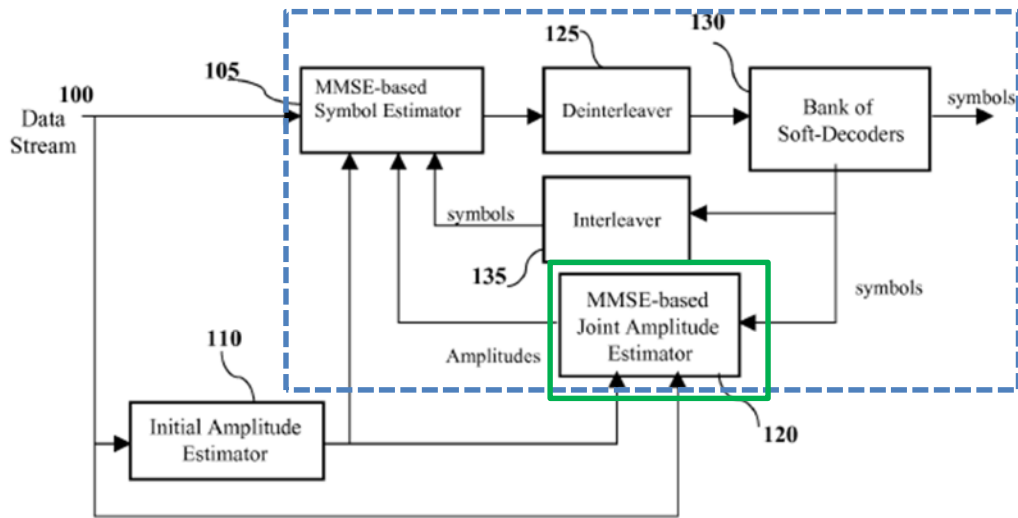


Figure 2

(EX1001 at Figure 2, 16:39-52).

VI. The Petition and Deficiencies of the Asserted References

A. The Grounds

70. I understand that Samsung's Petition asserts the following Grounds:

Ground	References	Basis	Challenged Claims
1	<i>Brommer, Lilleberg, and Hottinen</i>	§ 103	1-3
2	<i>Brommer, Lilleberg, Hottinen, and Learned</i>	§ 103	4

Ground	References	Basis	Challenged Claims
3	<i>Brommer, Lilleberg, Hottinen, and ElGamal</i>	§ 103	5
4	<i>Frank and Zha</i>	§ 103	1-3, 5
5	<i>Frank, Zha, and Learned</i>	§ 103	4

71. I understand that the Petition relies on *Brommer, Lilleberg, and Hottinen* as allegedly rendering obvious claim 1 for grounds 1-3 and *Frank and Zha* as allegedly rendering obvious claim 1 for grounds 4-5. But both of these combinations fail to disclose all the required claim limitations of independent claim 1.

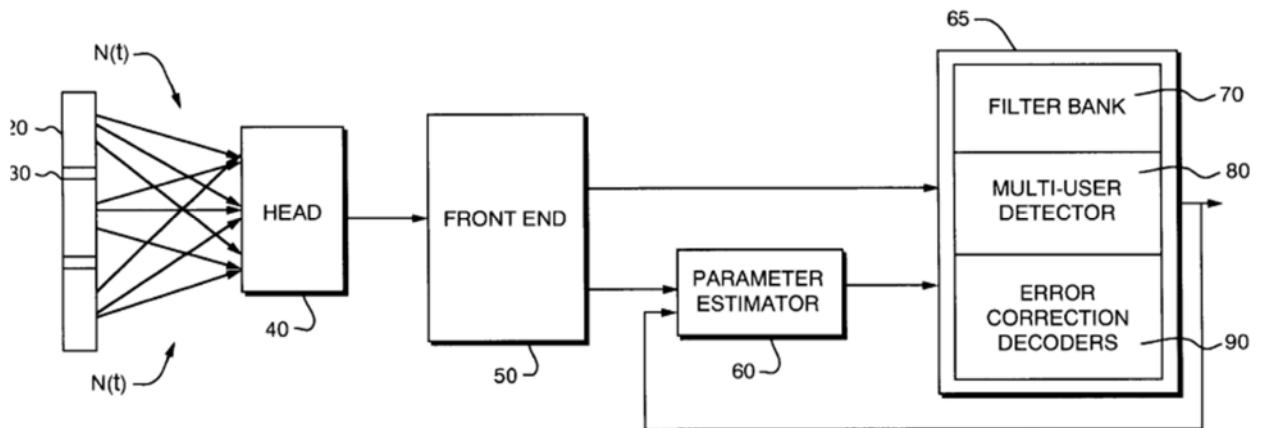
B. Grounds 1-3

72. I understand Grounds 1-3 each rely on *Brommer, Lilleberg, and Hottinen*. But *Brommer* is not prior art. And even were *Brommer* considered to be prior art, none of the references, alone or in combination, describe the claimed “bank of decoders coupled to said symbol estimator, producing a plurality of symbol likelihood estimates for each user, wherein said symbol likelihood estimates are iteratively fed back to said symbol estimator and said joint amplitude estimator.”

1. None of the Asserted References for Ground 1 Concerns or Describes a Joint Amplitude Estimator, Much less a Bank of Decoders that Provides Feed Back to the Joint Amplitude Estimator

73. *Brommer* describes multiuser detection to separate tracks of data from neighboring tracks in a digital storage medium. (EX1004 at 15: 9-35). In FIG. 1 of *Brommer*, a head 40 extracts a plurality of signals from the tracks at the digital

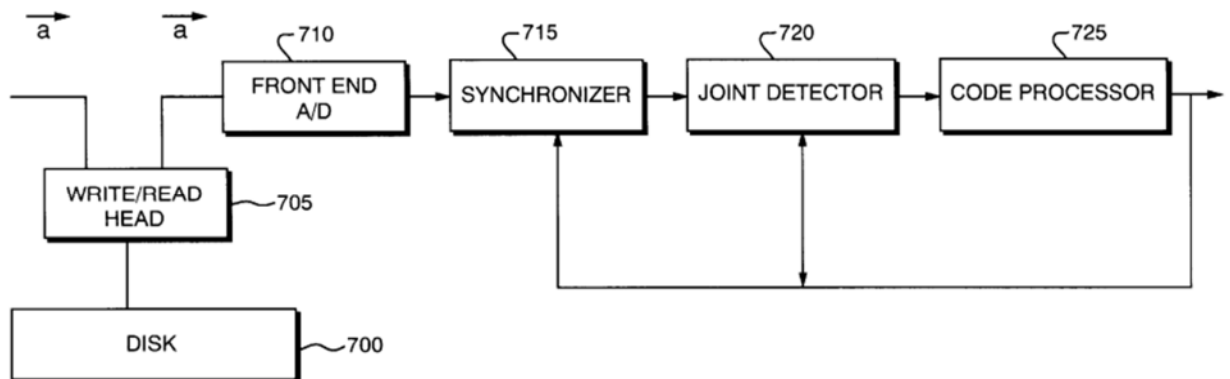
storage medium. (EX1004 at 15:9-35). The signals are processed by parameter estimator 60 and MUD processing section 65. MUD processing section 65 includes bank of matched filters 70 for preprocessing the signals. (EX1004 at 15:9-35). MUD processing section 65 also includes multi-user detector 80 that uses an algorithm to establish symbol estimates and a bank of decoders 90 to provide further processing. (EX1004 at 15:9-35). FIG. 1 of *Brommer* does not describe a joint amplitude estimator.



(EX1004 at FIG. 1).

74. *Brommer* describes another embodiment used for reading and writing to neighboring tracks in a digital storage medium. In FIG. 8 of *Brommer*, a read head 705 extracts analog voltage signals from the data on the tracks of magnetic disk platter 700. (EX1004 at 25:48-26:12). The analog voltage signals are converted to a digital stream of data by front end 710. (EX1004 at 25:48-26:12). Front end 710 feeds digital samples of the analog waveform into synchronizer 715. (EX1004

at 25:48-26:12). Synchronizer 715 generates a track transfer function for each of the appropriate functions, including estimates of the pulse envelope for each track. (EX1004 at 25:48-26:12). Using the track transfer functions and estimates of the pulse envelope, the joint detector makes preliminary estimates of the interfering digital signal values containing in the received signal. (EX1004 at 25:48-26:12). The preliminary symbol estimates produced by joint detector 720 are send to code processor 725 to update the preliminary estimates. (EX1004 at 25:48-26:12). Code processor 725 and joint detector 720 refine these estimates using iterations. (EX1004 at 25:48-26:12). But FIG. 8 of *Brommer* does not describe a bank of decoders.



(EX1004 at FIG. 8).

75. FIG. 1 and FIG. 8 of *Brommer* have different components. FIG. 8 of *Brommer* does not include at least two elements of the MUD processing section 65: bank of matched filters 70 and bank of decoders 90. Additionally, FIG. 1 and FIG. 8 also have different dataflows. For example, front end 710 in FIG. 8 feeds

all digital samples of the analog waveform into the synchronizer 715. In contrast, FIG. 1 of *Brommer* suggests the dataflow from the front end 50 may bypass parameter estimator 60 in route to MUD processing section 65.

C. Grounds 4-5

1. **Neither *Frank* nor *Zha* Concern or Describe “a bank of decoders that produce symbol likelihood estimates for each user, wherein said symbol likelihood estimates are iteratively fed back to said symbol estimator and said joint amplitude estimator until a final condition is obtained**

76. Frank describes a communication system that includes an error correction decoder such as a turbo decoder. (EX1006 at ¶¶ [0010]). I understand the Petition concedes that *Frank* does not disclose “a bank of decoders that produce symbol likelihood estimates for each user” and instead relies upon *Zha*. (Pet. at 59).

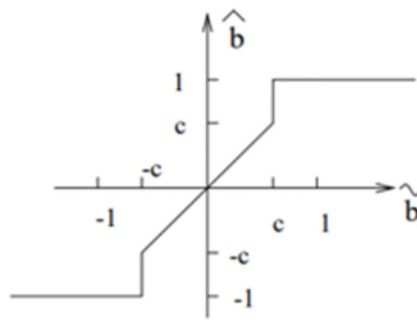
77. *Zha* describes successive interference cancellation in which individual user signals are first separated according to code division multiple access (CDMA), and then estimates of each user signal are used to successively cancel interference in the other user signals. (EX1010 at 743). By successively cancelling (or subtracting) the contribution of one user’s signal from the other user signals, the accuracy of the detection process can be improved. (EX1010 at 743-744). *Zha* notes that in certain circumstances while performing successive interference cancellation, performing “hard” decisions in the detection process can lead to reduced performance when the “hard” decision is incorrect. (EX1010 at 743). This is

because the incorrect “hard” decision error is propagated and impacts the detection of the other user’s signals. (EX1010 at 743). *Zha* notes that in some instances, when performing the cancellation, it would be better to weigh a given bit-decision by a measure of confidence in the given bit. (EX1010 at 743). Thus, if that decision is incorrect, it will have a smaller negative effect when canceling the given user’s signal from the other user signals. (EX1010 at 743). In order to implement this approach, *Zha* describes a “soft decision rule” that may output, for a given bit, a weighted value rather than an explicit “hard” “0” or “1”. (EX1010 at 744).

78. *Zha* shows that bit decisions are derived by applying the clipping function of Equation 7 to the soft data bit estimates.

$$\hat{b} = f_{dec}(\tilde{b}) = \begin{cases} 1, & \tilde{b} > c \\ \tilde{b}, & \tilde{b} \in [-c, c] \\ -1, & \tilde{b} < -c \end{cases} \quad (7)$$

79. The clipping function of Equation 7 treats soft data bit estimates with a probability above threshold c as hard data bit estimates. (EX1010 at 745). Similarly, soft data bit estimates with a probability below threshold c remain unchanged. (EX1010 at 745). This clipping function can be depicted, as shown in figure 1(d):



(d) Proposed decision rule

80. Thus, while *Zha* describes soft bit decision rules, there is no mention of any decoder, let alone a “bank of decoders”.

81. Indeed, the “soft decision rule” of *Zha* involves no error correction codes. There is no encoder at the transmitter that encodes the user bits to introduce redundancy into the transmitted signal. Similarly, there is no decoder at the receiver that uses error correction codes to assess the structure of the received signal to identify and correct errors. Moreover, *Zha* only weights a given bit and does not involve a system that performs an encoding process that increases the number of bits-to-be-transmitted and a decoder that performs the opposite operation. (EX1010 at 744). In contrast, in error correction coding, introduction of redundancy by the encoder at the transmitter increases the number of bits to be transmitted (*e.g.*, an error correction code with a code rate of 1/3 would increase the number of bits by a factor of 3), while the decoder will effect the opposite operation (*e.g.*, the decoding process).

82. *Zha*'s mere description of "data bit decisions" made by a decision rule—without any discussion of redundancy, iterations, or error correction—does not imply the existence of a bank of decoders. (Pet. at 59). Accordingly, this key claimed concept is missing from both *Frank* and *Zha*, and combining them does not and cannot result in the claimed apparatus of claim 1.

83. ***Further***, grounds 4-5 rely on combining primary reference *Frank* with *Zha*. But the supposed basis for combining these references—that they both use successive interference cancellation—is demonstrably incorrect: *Zha* uses **successive** interference cancellation, but every *Frank* embodiment relied on in the Petition explicitly uses the incompatible **parallel** interference cancellation approach. (*E.g.*, Pet. at 44-46; EX1006 at ¶¶ [0012]-[0015]). Indeed, I understand the Petition does not even identify how the references could supposedly be combined, much less establish that this undisclosed combination was somehow obvious. Nor could it. I understand the Petition does not acknowledge these material differences, nor does it try to explain how these incompatible approaches could somehow be combined.

84. *Frank* and *Zha* do not include *any* description of the bank of decoders of the inventive apparatus highlighted below in red, much less feedback between the bank of decoders and the joint amplitude estimator:

VII. The Petition Should be Denied Because Each Asserted Ground Fails to Establish the Required Likelihood of Success

85. The Petition should be denied because as established in the following sections, Grounds 1-5 all fail to establish the required reasonable likelihood of success.

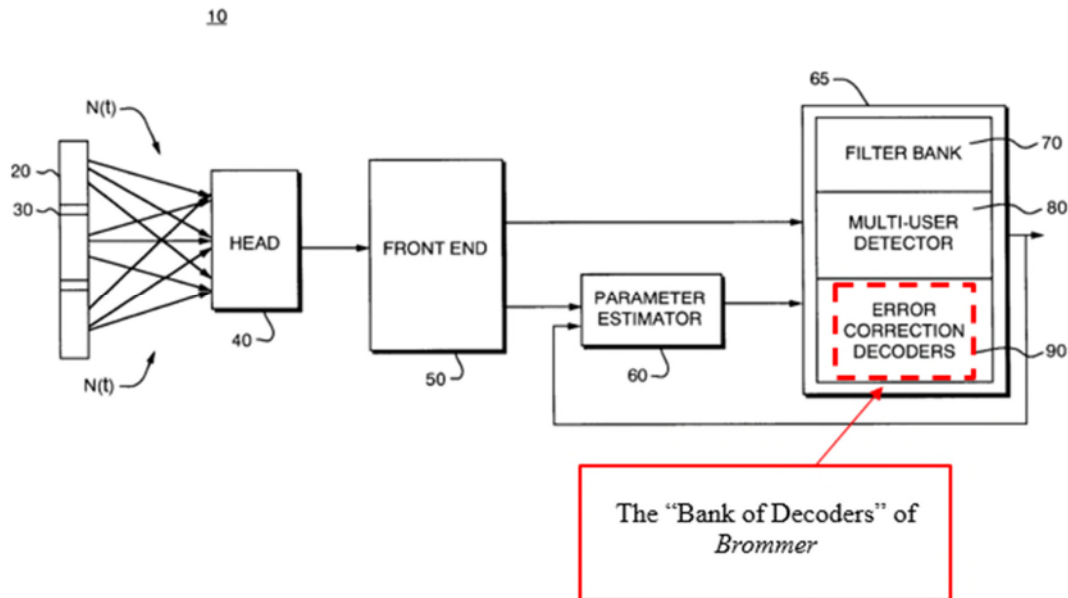
A. Grounds 1-3

86. The Petition fails to show that *Brommer* in view of *Lilleberg* in further view of *Hottinen* discloses or renders obvious independent claim 1 of the '703 patent for at least two independent reasons: (1) I understand *Brommer* is not prior art; (2) the Petition is silent regarding how the asserted references teach or suggest feedback from a bank of decoders to a joint amplitude estimator, as required by independent claim 1.

1. **The Petition fails to show that the combination of *Brommer*, *Lillieberg*, and *Hottinen* describe “a bank of decoders... producing a plurality of symbol likelihood estimates for each user, wherein said symbol likelihood estimates are iteratively fed back to said symbol estimator and said joint amplitude estimator” as required by claim 1**

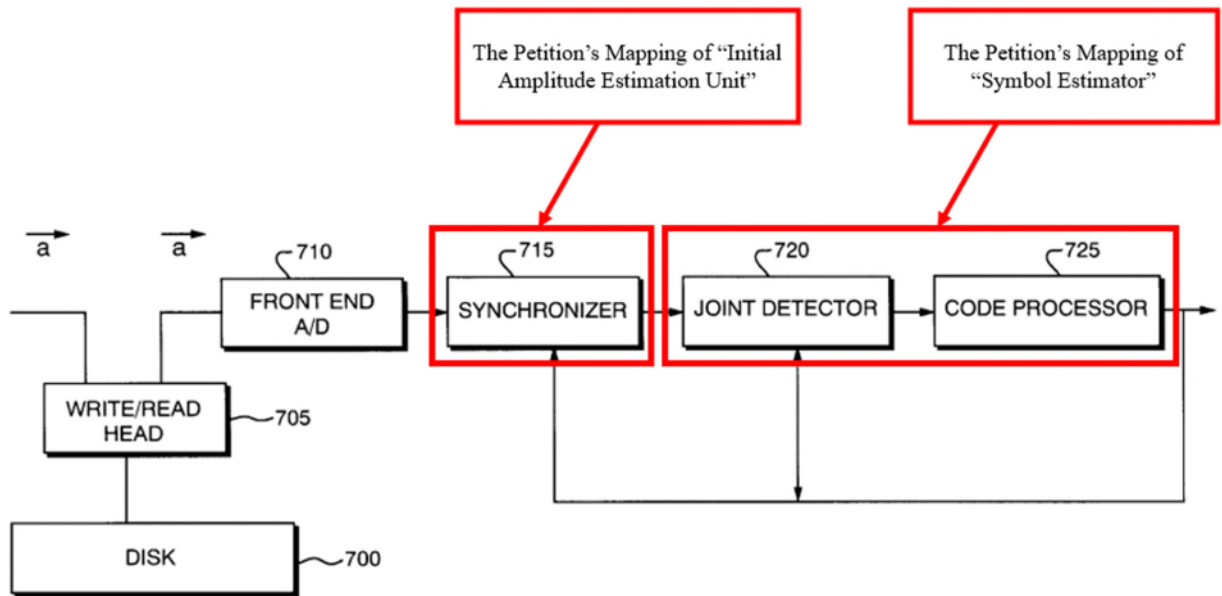
87. Even if *Brommer* were considered prior art (it is not), the Petition fails to demonstrate that *Brommer*, *Lillieberg*, and *Hottinen* describe “a bank of decoders... producing a plurality of symbol likelihood estimates for each user, wherein said symbol likelihood estimates are iteratively fed back to said symbol estimator and said joint amplitude estimator,” as required by claim 1.

88. In an attempt to show this requirement of claim 1, I understand the Petition points to *Brommer*'s "bank of decoders 90" illustrated in FIG. 1:



(Pet. at 33; EX1004 at FIG. 1).

89. I understand the Petition asserts that a POSITA would understand that, in combination with *Lilleberg*, the symbol likelihood estimates from bank of decoders 90 would be "fed back" to the symbol estimator (previously mapped to *Brommer*'s joint detector 720 and code processor 725 depicted in FIG. 8) and joint amplitude estimator. (Pet. at 33).

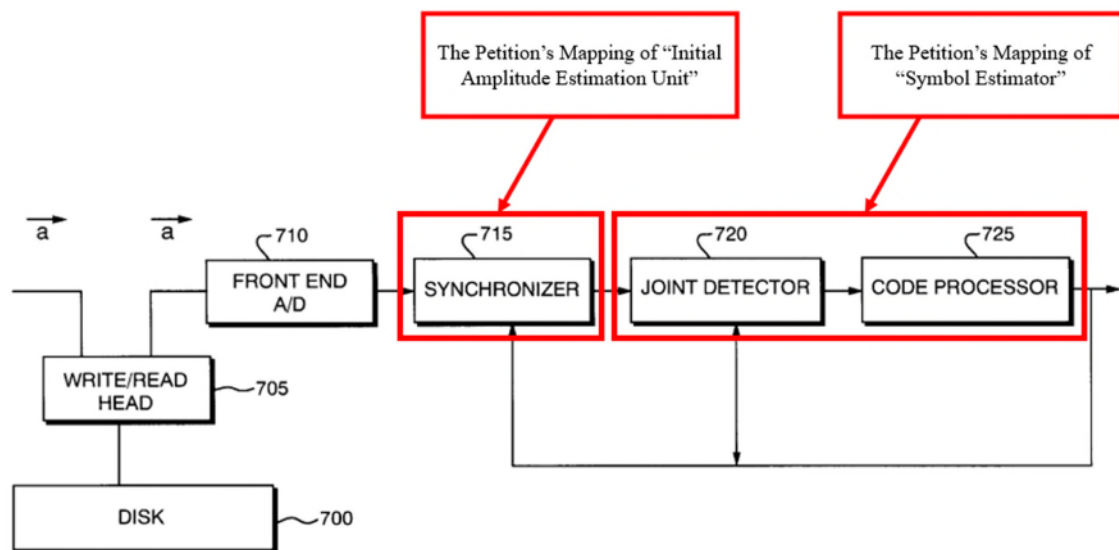


(Pet. at 33; EX1004 at FIG. 1³).

90. That is, I understand the Petition only suggests modifying FIG. 8 of *Brommer* to include a joint amplitude estimator. But the Petition ignores that FIG. 8 only discloses a code processor 725 (which I understand the Petition asserts is part of the claimed symbol estimator), and does not include the bank of decoders 90 of FIG. 1. I understand the Petition refers to FIG. 8 as “provid[ing] additional detail regarding the implementation of *Brommer*’s system” but fails to connect the structure of the FIG. 1 embodiment and the FIG. 8 embodiment in any meaningful manner. (Pet. at 26).

³ Patent Owner has added notations to FIG. 8 in line with the mapping provided in the Petition.

91. I understand the Petition provides no explanation of how *Brommer* discloses a bank of decoders in its FIG. 8 embodiment. I understand the Petitioner just assumes the bank of decoders 90 in FIG. 1 of *Brommer* also is present in FIG. 8 without explaining how or why one would believe it is present in FIG. 8. Indeed, a POSITA would **not** think there is an additional component for a bank of decoders 90 in the embodiment of FIG. 8 as FIG. 8 already has a code processor 725 (already mapped by the Petition to the symbol estimator), which is responsible for implementing error correction coding.



(Pet. at 33; EX1004 at FIG. 1, annotated).

92. A POSITA would understand that because FIG. 8 already includes the code processor 725 implementing error correcting coding, there could not be an

additional bank of decoders, which would also implement error correcting codes, within the embodiment of FIG. 8.

93. The Petition does not identify a “bank of decoders” in *Lilleberg* because it cannot as *Lilleberg* is silent regarding any bank of decoders. Further, the Petition does not connect the description of feedback in *Lilleberg* to the bank of decoders in *Brommer* in any meaningful way to show that a “bank of decoders . . . producing a plurality of symbol likelihood estimates . . . iteratively fed back to . . . said joint amplitude estimator.” Accordingly, the Petition has failed to show any “bank of decoders . . . producing a plurality of symbol likelihood estimates for each user, wherein said symbol likelihood estimates are iteratively fed back to said symbol estimator and said joint amplitude estimator” as required by claim 1, even if a POSITA were to combine *Brommer*, *Lillieberg*, and *Hottinen* as proposed.

94. And further, a POSITA would not want to modify *Brommer*’s FIG. 8 embodiment to include a “bank of decoders 90” because *Brommer* already has a code processor 725 implementing an error correcting coding (and which I understand the Petition alleges is the symbol estimator and therefore cannot be the claimed bank of decoders).

95. For this reason alone, the Petition fails to demonstrate that *Brommer* in view of *Lilleberg* in further view of *Hottinen* discloses or renders obvious claim 1 of the ’703 patent.

B. Grounds 4-5

96. The Petition fails to show that *Frank* in view of *Zha* discloses or renders obvious claims 1-5 of the '703 patent for at least the reason that none of the asserted references disclose “a bank of decoders that produce symbol likelihood estimates for each user, wherein said symbol likelihood estimates are iteratively fed back to said symbol estimator and said joint amplitude estimator until a final condition is obtained” as required by independent claim 1.

1. The Petition admits that *Frank* does not disclose a bank of decoders and there is no evidence that a bank of decoders exists in *Zha*

97. I understand the Petition fails to demonstrate that *Frank* and *Zha* disclose the required “bank of decoders that produce symbol likelihood estimates for each user, wherein said symbol likelihood estimates are iteratively fed back to said symbol estimator and said joint amplitude estimator until a final condition is obtained.” I understand the Petition admits that *Frank* does not disclose a bank of decoders and instead relies on *Zha*’s “soft decision rule” alleging that a POSITA would understand the “soft decision rule” to be a decoder. (Pet. at 59). I understand the Petition relies solely on their expert Dr. Min for this assertion and Dr. Min merely parrots the same statement as the Petition without explanation or support. (Pet at 59; EX1003 at 178).

98. But as explained above, any reasonable understanding of a decoder is one that implements an error correction coding approach. (EX2003 at 3; EX2004 at 11; EX2005 at 228). A system utilizing error correction coding requires encoding, by an encoder at the transmitter, the user bits using error correction coding such as a convolution coding, Walsh coding, Turbo Coding, low-density parity-check codes, polar codes, binary algebraic block codes (e.g., BCH codes), or non-binary algebraic block codes (e.g., Reed-Solomon codes). (EX2003 at 293, 311; EX2004 at 11; EX2005 at 230-259). This approach also requires the decoder in the receiver to decode the received signal such that the receiver can output the decoded user bits. (EX2003 at 293; EX2004 at 11; EX2005 at 228-229). Such an understanding is supported by numerous textbooks in the field, including Verdu, the text upon which I understand the Petitioner's rely. (EX2003 at 3, 293; EX2004 at 11; EX2005 at 228; EX1012 at 37-38).

99. The "soft decision rule" of *Zha* involves no error correction coding. There is no encoder at the transmitter that encodes the user bits to introduce redundancy into the transmitted signal. Similarly, there is no decoder at the receiver that uses error correction codes to assess the structure of the received signal to identify and correct errors. *Zha* only uses a soft decision rule to proportionally weigh a given bit and does not involve a system that uses an encoder to increase the number of bits-to-be-transmitted and a decoder that performs the opposite

operation. (EX1010 at 743-744). Accordingly, the “bit decision rule” in *Zha* has nothing to do with error correction coding and cannot reasonably be considered a decoder, let alone a bank of decoders. As a result, *Frank* and *Zha* fail to describe all elements of claim 1, and for this reason alone the Petition has not provided a reasonable expectation of success of showing at least one claim is unpatentable.

2. The Petition Provides No Explanation of How or Why One Would Combine *Zha* with *Frank* to Result in Claimed “Bank of Decoders”

100. I understand the Petition admits *Frank* is silent to “a bank of decoders that produce symbol likelihood estimates for each user, wherein said symbol likelihood estimates are iteratively fed back to said symbol estimator and said joint amplitude estimator until a final condition is obtained” and asserts that a POSITA would modify *Frank* with *Zha*’s bit decision rule. (Pet. at 59). But the Petition ignores that *Frank* already describes a system using error correcting codes. (see, e.g., EX1006 at Abstract and ¶¶ [0010]).

101. Because the Petition and Dr. Min ignore that *Frank* already describes a decoder utilizing error correcting codes, they are entirely silent as to how a POSITA could make the proposed combination to result in “a bank of decoders that produce symbol likelihood estimates for each user, wherein said symbol likelihood estimates are iteratively fed back to said symbol estimator and said joint amplitude estimator until a final condition is obtained.” I understand the Petition gives no explanation

of how the “bit decision rule” of *Zha* is compatible with *Frank*’s error correcting codes or whether a wholesale substitution with further unexplained functional changes would be required. Indeed, it is unclear how a POSITA even could incorporate *Zha* into *Frank* to obtain the claimed “bank of decoders” as there would be many unexplained substantial functional changes to *Frank* for which the Petition is silent.

102. Moreover, even if a POSITA could make the proposed combination (they could not), the Petition does not adequately explain why a POSITA would implement the soft bit decision rule of *Zha* within *Frank*. *Frank* already utilizes error correcting codes. *Zha* states that the bit decision rule can “achieve a performance close to that of a single user bound”. (EX1010 at 743; Pet. at 51). But *Zha* is an uncoded system and this improvement is only applicable to a similar uncoded system. There is no explanation of how or why *Zha*’s bit decision rule for an uncoded system would improve or could be combined with *Frank*’s coded system, let alone that a POSITA would understand and be motivated by the improvement.

103. This failure of the Petition to adequately explain how or why a POSITA would combine *Frank* and *Zha* to achieve the alleged advantage is another independent reason that the Petition has failed to show the challenged claims are unpatentable with respect to Grounds 4-5.

3. The Petition Provides No Explanation of How or Why One Would Combine *Zha*'s Successive Interference Cancellation with *Frank*'s Parallel Interference Cancellation

104. The Petition further fails to demonstrate that a POSITA would combine *Frank* and *Zha* because the Petition fails to explain how and why a POSITA would combine *Zha*'s improved amplitude averaging algorithm designed for a successive interference cancellation receiver with the *parallel interference cancellation receiver* disclosed in *Frank*.

105. **First**, the Petition's combination is entirely premised on combining *Zha*'s **successive** interference cancellation with *Frank*'s **successive** interference cancellation. (Pet. at 49-52). But all the *Frank* figures and embodiments relied by the Petition use **parallel** interference cancellation, not successive interference cancellation:

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. 1 is a block diagram illustrating a preferred receiver structure for MMSE equalization with parallel interference cancellation in accordance with the present invention.

[0013] FIG. 2 (divided into FIGS. 2A and 2B) is a combined block and flow diagram illustrating, in greater detail, a preferred receiver structure and method for MMSE equalization with parallel interference cancellation in accordance with the present invention.

[0014] FIG. 3 is a block diagram illustrating an apparatus embodiment of the preferred receiver structure for MMSE equalization with parallel interference cancellation in accordance with the present invention.

[0015] FIG. 4 (divided into FIGS. 4A and 4B) is a flow diagram illustrating a method embodiment for MMSE equalization with parallel interference cancellation in accordance with the present invention.

(EX1006 at ¶¶ [0012]-[0015]).

106. And I understand the Petition does not explain how a POSITA would combine the improved amplitude averaging algorithm designed for *Zha's* successive interference cancellation with *Frank's* parallel interference cancellation or how *Zha's* successive interference cancellation teachings could be applied to *Frank's* parallel interference cancellation. (See Pet. at 49-52). And for good reason—as established above but ignored by the Petition, a POSITA would understand that successive interference cancellation and parallel interference cancellation are fundamentally different cancellation techniques, and the two techniques cannot simply be mixed and matched as I understand the Petition proposes.

107. **Second**, the *Frank* and *Zha* embodiments that Samsung seeks to combine are incompatible for additional reasons. For example, *Zha*'s time-based amplitude averaging algorithm (which I understand the Petition vaguely proposes somehow using with *Frank*) requires that associated time delays are exactly known at the receiver. *Zha* states "[i]nitially, we assume that the time delays are exactly known at the receiver." (EX1010 at 743).

$$\mathbf{d}_k(i) = \delta_k \mathbf{c}_k(p_k + 1, i) + (1 - \delta_k) \mathbf{c}_k(p_k, i). \quad (5)$$

(EX1010 at 744). This known time delay— $\mathbf{d}_k(i)$ —is used in the amplitude averaging algorithm relied on by the Petition:

$$\bar{A}_k^{v+1} = \frac{1}{M} \sum_{i=1}^M \text{abs} \left(\text{Re} \left(e^{-j\theta_k} (\mathbf{d}_k(i))^H \bar{\mathbf{r}}_k^{v+1} \right) \right)$$

(Pet. at 49-52, 56; EX1010 at 744).

108. But *Zha* does not disclose how to achieve such required known time delays, nor does *Frank* disclose that time delays can be known in its disclosed wireless system as required by *Zha*'s amplitude averaging algorithm. (See EX1006). The Petition does not explain how a POSITA would use an amplitude averaging algorithm that requires the time delays to be exactly known in a system where the time delays are not known. (See Pet. at 49-52, 56).

109. For these reasons alone, *Frank* in view of *Zha* fails to disclose or render obvious claim 1 of the '703 Patent.

I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code.

Dated: January 29, 2025



Dr. Giuseppe Caire