

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

PARTEC AG *and* BF EXAQC AG,

Plaintiffs,

v.

MICROSOFT CORPORATION,

Defendant.

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CASE NO. 2:24-CV-00433-RWS-RSP

CLAIM CONSTRUCTION ORDER

ParTec AG and BF EXAQC AG (together, “ParTec”) allege infringement of three United States computing patents. Two of them—U.S. Patents 10,142,156 and 11,934,883—relate “to a computer cluster arrangement with improved resource management . . . for processing scalable computation tasks as well as complex computation tasks.” ’156 Patent at 1:19–23; *see also* ’883 Patent at 1:20–24 (same). The third, U.S. Patent 11,537,442, relates to “a heterogeneous computation environment adapted for parallel processing of a computation task.” ’442 Patent at 1:18–19. The parties dispute the scope of six terms. Having considered the parties’ briefing, along with arguments of counsel at a December 12, 2025 hearing, the Court resolves those disputes as follows.

I. BACKGROUND

A. U.S. Patents 10,142,156 and 11,934,883

These related patents¹ describe the problem in the art of “accelerators” being “tightly coupled” with computation nodes, which “results in a static assignment and leads to over- or under-subscription of accelerators.” ’156 Patent at 1:40–41. This, in turn, may lead to either a shortage

¹ The ’883 Patent is a “grandchild” of the ’156 Patent and shares the same disclosure. *See* ’883 Patent at [63].

or an excessive supply of resources. *Id.* at 1:42–43. Nor does such an arrangement “provide fault tolerance in case of accelerator failures.” *Id.* at 1:43–46.

Figure 1 (below), for example, shows a prior-art configuration in which each computation node (CN) includes a CPU and an associated accelerator (Acc). Because of the “tight coupling” of each accelerator with a CN, should one accelerator fail, the remaining operational accelerators cannot assist with computations for the CN to which the failed accelerator is coupled.

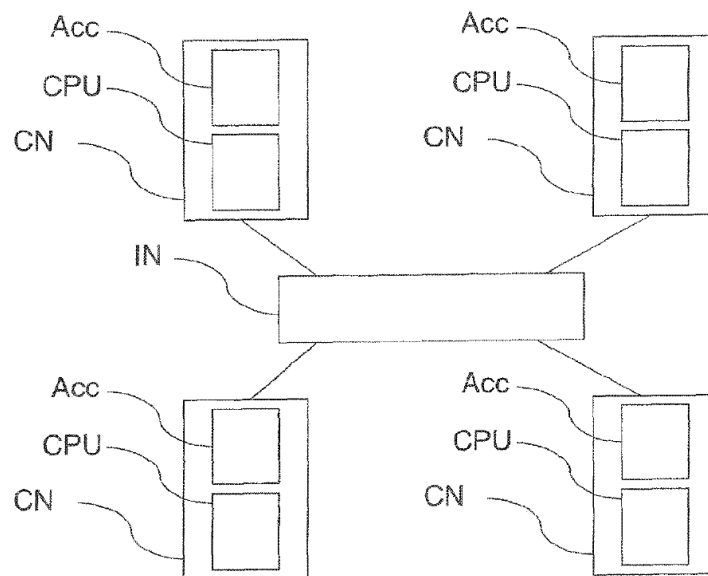


FIG. 1 of the '156 Patent

To solve this problem, the patents teach “provid[ing] a computer cluster arrangement, which allows communication flexibility [for] data exchange between accelerator and computation nodes as well as direct access of computation nodes to any and each of the accelerators.” ’156 Patent at 2:21–25. This configuration allows for “dynamic coupling of accelerators to computation nodes at runtime.” *Id.* at 2:26–28.

Figure 2 (below), for example, shows a booster group (BG) of three boosters (B) and a cluster (C) of four computation nodes (CN). The boosters are not associated with specific

computation nodes, but communicate with the nodes through infrastructure (IN). A resource manager (RM) assigns boosters to nodes as needed. *See generally* '156 Patent at 8:28–57. The main difference between boosters and computation nodes concerns their processors, which “in boosters typically comprise an extensive arithmetic logic unit and a simple control structure” relative to computation-node processors. *Id.* at 6:1–4; *see also id.* at 6:6–8 (“processors being applied in computation nodes differ in their processor design compared to processors being applied in boosters”).

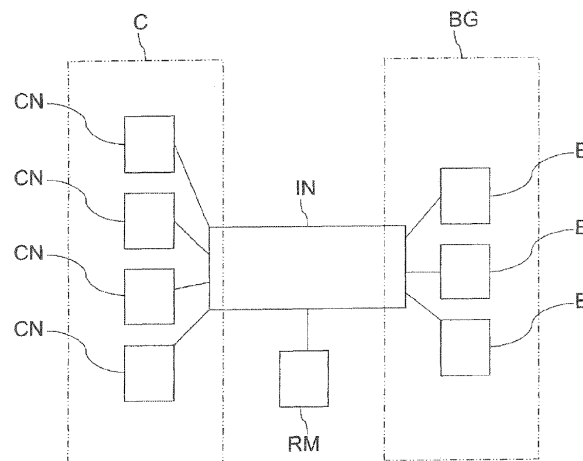


FIG. 2 of the '156 Patent

Five of the six disputes implicate Claim 1 of the '156 Patent, Claim 1 of the '883 Patent, or both. Claim 1 of the '156 Patent, which is representative, recites:

1. A **computer cluster-booster system** for processing a computation task, comprising:
 - a plurality of hardware computation nodes, each of which interfaces with a communication infrastructure, at least two of the hardware computation nodes being arranged to jointly compute at least a first part of said computation task;
 - a plurality of hardware **boosters**, each hardware **booster** having a compute capacity, at least one hardware **booster** of the plurality of hardware **boosters** being arranged to compute at least a second, specific part of said computation task after

having been assigned to at least one hardware computation node and under control of that at least one hardware computation node, the at least one hardware **booster** interfacing with the communication infrastructure; and

a resource manager being arranged to assign the at least one hardware **booster** to the at least one hardware computation node, including:

at a start of processing of said computation task, establishing an initial assignment by using a predetermined **assignment metric** specified as a function of at least one of a group of assignment parameters, and

during said processing of said computation task: (i) updating the predetermined **assignment metric**, and (ii) establishing a dynamic assignment by using the predetermined **assignment metric** that was updated, and

wherein the plurality of hardware computation nodes and the plurality of hardware **boosters** are configured such that during processing of said computation task, assignments of hardware computation nodes and hardware **boosters** can be provided such that at least (i) at least one of the plurality of hardware computation nodes is arranged to communicate with at least one of the plurality of hardware **boosters**, (ii) at least one of the plurality of hardware **boosters** is **assigned to and shared by more than one of the plurality of hardware computation nodes** such that the compute capacity of the at least one of the plurality of hardware **boosters** is shared between the more than one of the plurality of hardware computation nodes, and (iii) each of the hardware **boosters** is assignable to each of the hardware computation nodes.

'156 Patent at 13:20–63 (disputed terms in bold).

B. U.S. Patent 11,537,442

The '442 Patent, which has a common inventor with the '883 Patent and '156 Patent, also concerns computation nodes and boosters. More specifically, the patent relates to a computer

architecture in which “a resource manager is responsible for assigning one or more of the boosters and the computation nodes to each other in a dynamic manner during runtime.” ’442 Patent at 1:28–30. This “dynamic rearranging” during runtime potentially improves the efficiency of the system.

If a task is computed with a first division of sub-tasks between a computation node and a booster, it is possible that such a division is not an optimal division for the computation of the task. Certain sub-tasks which were assigned to a booster on the first iteration might in fact not be suitable for processing by the booster such that a processing of the sub-tasks by a computation node rather than a booster might optimize the computation of the task as a whole. Accordingly, for a second and possible further iterations, if needed, of the task with an altered second and/or further sub-task distribution might improve the efficiency of the computation of the task.

Accordingly, the system includes a mechanism whereby each of the computation nodes and the cluster nodes are arranged such that daemons and feed back information to the daemon relating to the processing of sub-tasks and a current state of the respective processing entity. The daemon uses the information provided by the daemons and to determine whether the distribution of sub-tasks to computation nodes and boosters could be adjusted to optimize or adapt the computation of the task for a subsequent iteration. The resource manager can also reassign computation nodes and boosters to each other, in addition to the adjusted distribution of tasks.

’442 Patent at 3:59–4:15 (reference numbers omitted).

The sole dispute from this patent concerns Claim 1, which recites:

1. A method of operating a heterogeneous computing system comprising a plurality of computation nodes and a **plurality of booster nodes**, at least one of the plurality of computation nodes and a **plurality of booster nodes** being arranged to compute a computation task, the computation task comprising a plurality of sub-tasks, the method comprising:

in a **first computing iteration**, assigning and processing the plurality of sub-tasks by at least a portion of the plurality of computation nodes and at least a portion of the **plurality of booster nodes** in a first distribution; and

generating, using information relating to the processing of the

plurality of sub-tasks by at least the portion of the plurality of computation nodes and at least the portion of the **plurality of booster nodes**, a further distribution of the plurality of sub-tasks between the plurality of computation nodes and **the plurality of booster nodes** for processing thereby in a **further computing iteration**.

'442 Patent at 5:26–46 (emphasis added). Specifically, the parties dispute whether the sub-tasks making up “the plurality of sub-tasks” introduced in the preamble can change over the course of the various computing iterations.

II. LEGAL STANDARDS

“[T]he claims of a patent define the invention to which the patentee is entitled the right to exclude.” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*). As such, if the parties dispute the scope of the claims, the court must determine their meaning. *See, e.g., Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1317 (Fed. Cir. 2007) (Gajarsa, J., concurring in part); *see also Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 390 (1996), *aff'g*, 52 F.3d 967, 976 (Fed. Cir. 1995) (*en banc*).

Claim construction, however, “is not an obligatory exercise in redundancy.” *U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997). Rather, “claim construction is a matter of [resolving] disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims” *Id.* A court need not “repeat or restate every claim term in order to comply with the ruling that claim construction is for the court.” *Id.*

When construing claims, “there is a heavy presumption that claim terms are to be given their ordinary and customary meaning.” *Aventis Pharm. Inc. v. Amino Chems. Ltd.*, 715 F.3d 1363, 1373 (Fed. Cir. 2013) (citing *Phillips*, 415 F.3d at 1312–13). Courts must therefore “look to the words of the claims themselves . . . to define the scope of the patented invention.” *Id.* (citations

omitted). The “ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, *i.e.*, as of the effective filing date of the patent application.” *Phillips*, 415 F.3d at 1313. This “person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification.” *Id.*

Intrinsic evidence is the primary resource for claim construction. *See Power-One, Inc. v. Artesyn Techs., Inc.*, 599 F.3d 1343, 1348 (Fed. Cir. 2010) (citing *Phillips*, 415 F.3d at 1312). For certain claim terms, “the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words.” *Phillips*, 415 F.3d at 1314; *see also Medrad, Inc. v. MRI Devices Corp.*, 401 F.3d 1313, 1319 (Fed. Cir. 2005) (“We cannot look at the ordinary meaning of the term . . . in a vacuum. Rather, we must look at the ordinary meaning in the context of the written description and the prosecution history.”). But for claim terms with less-apparent meanings, courts consider “those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean . . . [including] the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art.” *Phillips*, 415 F.3d at 1314.

III. THE LEVEL OF ORDINARY SKILL IN THE ART

The level of ordinary skill in the art is the skill level of a hypothetical person who is presumed to have known the relevant art at the time of the invention. *In re GPAC*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). In resolving the appropriate level of ordinary skill, courts consider the types of

and solutions to problems encountered in the art, the speed of innovation, the sophistication of the technology, and the education of workers active in the field. *Id.* Importantly, “a person of ordinary skill is also a person of ordinary creativity, not an automaton.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007). Here, neither party asserts a level of ordinary skill. Accordingly, the Court will address the appropriate level of skill only to the extent necessary to resolve the disputes.

IV. THE DISPUTED TERMS

A. “assigned to and shared by more than one of the plurality of hardware computation nodes” (’156 Patent, Claims 1, 14)

ParTec’s Construction	Microsoft’s Construction
Plain and ordinary meaning	“simultaneously assigned to and useable by more than one of the plurality of hardware computation nodes”

This dispute concerns Microsoft’s use of “simultaneously” in its proposed construction.

The claims recite a “wherein” clause with three parts. Claim 1, for example, recites:

wherein the plurality of hardware computation nodes and the plurality of hardware boosters are configured such that during processing of said computation task, assignments of hardware computation nodes and hardware boosters can be provided such that at least

- (i) at least one of the plurality of hardware computation nodes is arranged to communicate with at least one of the plurality of hardware boosters,
- (ii) at least one of the plurality of hardware boosters is **assigned to and shared by more than one of the plurality of hardware computation nodes** such that the compute capacity of the at least one of the plurality of hardware boosters is shared between the more than one of the plurality of hardware computation nodes, and
- (iii) each of the hardware boosters is assignable to each of the hardware computation nodes.

'156 Patent at 13:48–63 (emphasis added; reorganized for readability); *see also id.* at 15:20–16:6 (reciting similar language in Claim 14). The parties dispute whether the requirement that a booster be “shared” requires that the booster be performing tasks for the computation nodes to which it has been assigned at the same time. *See* Hr’g Tr., Dkt. No. 138 at 13:20–23; *id.* at 15:7–10 (asserting “simultaneous” in its construction requires the booster to be “processing for more than one node at the same time”).

Microsoft gives two reasons why the Court should adopt its construction. First, it says the applicant distinguished the invention over U.S. Publication No. 2011/0161972 (Dillenberger) by asserting that Dillenberger did not disclose “assigned to and shared by more than one (i.e., at least two) of the host such systems such that the compute capacity of the accelerator is shared between host systems.” Dkt. No. 123 at 4 (quoting '156 Patent File History, Dkt. No. 123-2 at 484). Thus, says Microsoft, the limitation “requires simultaneous—not sequential—assignment and use.” *Id.* Second, during prosecution of the parent application before the European Patent Office, the applicant explained the claim “requires allowing ‘multiple computation nodes to use a booster *simultaneously*.’” *Id.* at 4 (quoting Letter From M. Himmelsbach to EPO (Feb. 28, 2025), Dkt. No. 123-5 at 18).

Critiquing Microsoft’s construction, ParTec stresses “simultaneous” doesn’t appear in the claim language, and “useable” doesn’t appear in the patent. Dkt. No. 114 at 7. ParTec also says Microsoft’s construction would introduce ambiguity into the claim scope. *Id.* at 8; *see also* Dkt. No. 124 at 2 n.1 (questioning whether this limitation would be satisfied “if a booster was assigned to and being shared by two computation nodes . . . but for a time was busy processing part of a task for one node and accordingly could not process a task for a second computation node”). ParTec also cautions against relying on statements from foreign prosecution history. Dkt. No. 114 at

8–9. Regardless, says ParTec, the statements on which Microsoft relies do not support its construction because they concern different claim language. *Id.* at 9.

The Court agrees with ParTec. Regarding the domestic prosecution history, the distinction made by ParTec was that Dillenberger did not disclose one booster being assigned to multiple nodes, but rather one node being assigned to multiple boosters. *See* Dkt. No. 123-2 at 332 (describing FIG. 2 of Dillenberger as depicting “Accelerator W is assigned to Host System A, Accelerator X is assigned to Host System B, and Accelerator Y is assigned to Host System N” and FIG. 3 as describing “Accelerators W and X are assigned to Host System A.”). In response, ParTec argued that, in its claims, “at least one of the plurality of boosters is assigned to and shared by more than one of the plurality of hardware computation nodes such that the compute capacity of the at least one of the plurality of hardware boosters is shared between the more than one of the plurality to hardware computation nodes.” *Id.* In other words, the applicant’s claims shared one booster with multiple nodes, not one node with multiple boosters. This argument by the applicant doesn’t support interpreting the claim language to require a booster processing for two nodes at the same time.

Nor do the patentee’s arguments before the EPO. The claim language at issue in the European patent, referred to as “feature 4.2,” is identical to the language at issue here. Microsoft points to this statement from a ParTec letter to the EPO:

The key point for the correct interpretation of feature 4.2 regarding shareability is that this is claimed in the patent for a different reason. The basic shareability of the boosters, which also existed in the prior art, for example because they are many core processors, failed because the boosters were permanently assigned to their respective computation nodes, . . . so that other computation nodes could not access the boosters from a purely technical point of view, i.e., could not use their intrinsic shareability. The invention solves exactly this rigid assignment and connects all computation nodes with all boosters, so that now, a resource manager can take advantage of the already existing shareability of the boosters and allow multiple computation nodes to use a booster simultaneously.

Letter From M. Himmelsbach to EPO (Feb. 28, 2025), Dkt. No. 123-5 at 17–18. But nowhere does this letter suggest that, by arguing for “simultaneity,” ParTec meant the booster must be processing at the same time for multiple nodes. Instead, the context of the claim language, and the arguments before the EPO, suggest that “simultaneously” simply means “during the same processing task,” which is already contemplated by the claim.

At a minimum, a skilled artisan could reasonably read these domestic and foreign prosecution-history statements two ways: (1) as Microsoft suggests, and (2) that “simultaneously” refers to “during the same processing task.” That alone prevents the Court from finding the disclaimer Microsoft seeks. *See Sandisk Corp. v. Memorex Prods.*, 415 F.3d 1278, 1287 (Fed. Cir. 2005) (“There is no ‘clear and unmistakable’ disclaimer if a prosecution argument is subject to more than one reasonable interpretation . . .”).

Microsoft also argues that clause (iii) of the limitation already has the basic assignment ability where the system can assign different boosters to different nodes. Hr’g Tr., Dkt. No. 138 at 19:19–20:1. “So if that’s all this ‘shared by’ language meant,” says Microsoft, “we wouldn’t need [clause (ii)] at all.” *Id.* at 20:2–5. The Court, however, disagrees, because clause (iii) simply requires that each of the boosters can be “connected” to each of the nodes. It says nothing about one booster making computations for more than one node during the processing task.

In sum, the Court is not persuaded “shareable” requires strict “simultaneous” processing by the booster for two nodes. Rather, as already contemplated by the claims, a booster must be assigned to and shareable by multiple nodes during the same processing task. Accordingly, the Court construes this term as “assigned to and useable by more than one of the plurality of hardware computation nodes during processing of said computation task.”

B. “assignment metric” (’156 Patent, Claims 1–2, 13–15; ’883 Patent, Claims 1–2, 13–15)

ParTec’s Construction	Microsoft’s Construction
Plain and ordinary meaning (“a metric or measurement used for the act of assigning,” Dkt. No. 114 at 10)	“measurements represented as a group of several parameters”

Claim 1 of the ’156 Patent recites:

a resource manager being arranged to assign the at least one hardware booster to the at least one hardware computation node, including:

at a start of processing of said computation task, establishing an initial assignment by using a predetermined **assignment metric** specified as a function of at least one of a group of assignment parameters, and

during said processing of said computation task: (i) updating the predetermined **assignment metric**, and (ii) establishing a dynamic assignment by using the predetermined assignment metric that was updated

’156 Patent at 13:36–47 (emphasis added). Relying on dictionary definitions, the claims, and the specification, ParTec construes “assignment metric” as “a metric or measurement used for the act of assigning.” Dkt. No. 114 at 10. Microsoft asserts prosecution-history disclaimer and lexicography in support of its narrower construction. Dkt. No. 123 at 8–9.

The relevant prosecution history concerns ParTec’s response to an August 2015 Office Action that rejected the claims based on US 2012/0054770 (Krishnamurthy). At the time, the last limitation of Claim 1 recited “a resource manager (RM) being arranged to assign at least one booster (B) to at least one of said plurality of computation nodes (CN) for computation of said second part of said computation task, the assignment being accomplished as a function of a

predetermined assignment metric.” *See* ’156 Patent File History, Dkt. No. 123-2 at ParTec_165.

The examiner cited Paragraph [0042] of Krishnamurthy as teaching these elements. *Id.*

In response, the applicant amended the claim to recite, as the last limitation:

wherein said resource manager (RM) being arranged to perform the assignment by using a predetermined assignment metric at start of processing of said computation task. and (i) initialize the assignment, (ii) alter the predetermined assignment metric, and (iii) perform the assignment by using the altered predetermined assignment metric during processing of the computation task.

’156 Patent File History, Dkt. No. 123-2 at ParTec_207. In the accompanying remarks, the applicant argued that, “even under the assumption that Krishnamurthy also has some kind of assignment metric, the length of the batch window, which might be changed during runtime, would only correspond to one possible runtime parameter, but not to the metric itself.” *Id.* at ParTec_214. “Krishnamurthy only describes that a change in a runtime parameter, i.e., the length of the batch window, might result in a different resource assignment.” *Id.*

But the examiner was not persuaded. In the next action, he identified “throughput computer rate” from Para. [0040] of Krishnamurthy as an assignment metric. ’156 Patent File History, Dkt. No. 123-2 at ParTec_225; *see also id.* at ParTec_244 (noting, in an Interview Summary, “the feature ‘the assignment metric’ was discussed” and “Examiner verified that ‘operations per second’ or ‘throughput computing rate’ disclosed by Krishnamurthy . . . is mapped to ‘the assignment metric’ recited in the claims”). The examiner also specifically noted “‘an assignment metric’ is not explicitly defined by Applicant’s specification.” *Id.* at ParTec_229.

In response, the applicant added the limitation of “wherein said assignment metric is specified as a function of at least one of a group of assignment parameters to facilitate an assignment

of particular boosters to particular ones of the plurality of computation nodes.” ’156 Patent File History, Dkt. No. 123-2 at ParTec_265. The applicant then remarked:

even assuming that Krishnamurthy’s number of operations per second functions as an assignment metric, with which Applicant does not necessarily agree, Applicant’s independent claim 1 as amended clarifies that Applicant’s assignment metric is not simply a metric represented as a single numeric value, and is instead represented as a group of several parameters.

Id. at 272. This is not disclaimer. As ParTec notes in its reply, the applicant’s argument was not that Krishnamurthy did not teach an assignment metric, but that it did not teach an “assignment metric [that is] specified as a function of at least one of a group of assignment parameters to facilitate an assignment of particular boosters to particular ones of the plurality of computation nodes,” as recited in the amended claims.

But the applicant made additional statements that amount to lexicography. To start, the applicant specifically “disagrees with the Final Action’s allegation that Applicant’s assignment metric is not explicitly defined by Applicant’s specification.” ’156 Patent File History, Dkt. No. 123-2 at 272. The applicant then cited and emphasized part of Para. [0017], which states “managing the assignment metric refers to establishing and updating rules naming at least one booster, which is assigned to at least one further named computer node.” *Id.* at ParTec_273. Explaining this language, the applicant wrote: “In other words, Applicant’s specification as originally filed explains that the assignment metric may be managed via a set of rules, and therefore the assignment metric is representative of one of several groups of parameters utilized as part of these rules.” *Id.*

At least in its briefing, ParTec ignores its prosecution-history statement that the term is, in fact, defined by the specification, and instead makes a more general argument focused on disclaimer. *See* Dkt. No. 124 at 2–3. At the hearing, however, ParTec called the purported lexicography “just a different flavor from the prosecution disclaimer argument.” Hr’g Tr., Dkt. No. 138 at

33:9–11. In its view, “the patentee is not defining what the assignment metric is” *Id.* at 33:17–18. Rather, “the patentee is referring to what the patentee was adding and how that traverses the Krishnamurthy reference.” *Id.* at 33:18–20.

That contention, however, runs counter to the applicant’s express disagreement “with the Final Action’s allegation that the Applicant’s assignment metric is not explicitly defined by Applicant’s specification.” ’156 Patent File History, Dkt. No. 123-2 at ParTec_272. And notably, this part of the applicant’s arguments references the specification, not the claims, *id.* at ParTec_273, further undercutting any notion this is simply an argument that Krishnamurthy does not teach a specific claim limitation.

ParTec also makes a claim-differentiation argument based on Claims 1 and 5 of the ’883 Patent. That patent’s Claim 1 requires a “resource manager being arranged to . . . accomplish assignments [of boosters to nodes] as a function of a predetermined assignment metric” ’883 Patent at 13:12–28. Claim 5 then requires the “predetermined assignment metric” to be “specified as a function of at least one of a group of assignment parameters, said group of assignment parameters comprising: resource information, cost information, complexity information, scalability information, a computation log record, compiler information, priority information, and a time stamp.” *Id.* at 13:52–58. ParTec suggests Microsoft’s construction would violate the doctrine of claim differentiation.

The Court disagrees for two reasons. First, “claim differentiation is a guide, not a rigid rule,” *Laitram Corp. v. Rexnord, Inc.*, 939 F.2d 1533, 1538 (Fed. Cir. 1991), and ParTec provides no authority for why that guide should trump a definition provided by the applicant. Second, even applying the definition provided by the applicant, the scope of Claim 5 likely remains narrower

because of its recitation of specific constituents of the “group of assignment parameters,” so the applicant’s definition does nothing to disturb the doctrine.

Because the applicant explained the specification defines “assignment metric” and provides a definition, the Court must respect that explanation. To do otherwise would undermine the public-notice function of patents and their intrinsic record. *See Springs Window Fashions LP v. Novo Indus., L.P.*, 323 F.3d 989, 995 (Fed. Cir. 2003) (“The public notice function of a patent and its prosecution history requires that a patentee be held to what he declares during the prosecution of his patent.”). Accordingly, the Court construes “assignment metric” as “a metric used for the act of assigning that is representative of one of several groups of parameters used as part of rules by which the metric is managed.”

C. “booster” (’156 Patent, Claims 1, 4, 6–8, 12–15; ’883 Patent, Claims 1–2, 6–7, 11–13, 15)

ParTec’s Construction	Microsoft’s Construction
Plain and ordinary meaning (“a device for increasing power or effectiveness,” Dkt. No. 114 at 15)	“one or more booster nodes”

Claim 1 of the ’156 Patent recites:

a plurality of hardware boosters, each hardware booster having a compute capacity, at least one hardware booster of the plurality of hardware boosters being arranged to compute at least a second, specific part of said computation task after having been assigned to at least one hardware computation node and under control of that at least one hardware computation node, the at least one hardware booster interfacing with the communication infrastructure[.]

’156 Patent at 13:27–35. Microsoft calls “booster” a coined term. Dkt. No. 123 at 14. ParTec accuses Microsoft of ignoring the applicant’s decision to use “booster” and “booster node” as

separate terms and disputes that “booster” is coined. Dkt. No. 124 at 4–5. ParTec also says Microsoft ignores the prosecution history, which equates boosters and accelerators. *Id.* at 5 (citing ’883 Patent File History, Dkt. No. 114-6 at 902, and ’156 Patent File History, Dkt. No. 114-5 at 224).

To start, this term does not have a well-understood meaning, so the Court must look at the specification’s use of the term for guidance. Notably, the patent’s distinction between “booster” and “booster node” is only made with reference to Figure 9. The rest of the patent simply refers to “boosters” and “booster groups.” Also, the patent strongly suggests that boosters are a type of accelerator. After describing that, in the prior art, each accelerator is “tightly coupled” with a computation node, ’156 Patent at 2:3–4, the patent explains its intention “to provide a computer cluster arrangement [that] allows communication flexibility [for] data exchange between accelerator and computation nodes as well as direct access of computation nodes to any and each of the accelerators,” *id.* at 2:21–25. More specifically, the invention aims “to provide a dynamic coupling of accelerators to computation nodes at runtime.” *Id.* at 2:26–28. The patent then stops using the word “accelerator” and starts using the word “booster,” suggesting a “booster” is an “accelerator” that is not tightly coupled with a computation node. Notably, this is consistent with ParTec’s explanation during prosecution of the ’883 Patent that “boosters” are “accelerators,” which the Court adopts as its construction.

**D. “computer cluster-booster [system/arrangement]” (’156 Patent, Claims 1, 14);
“computer cluster [system/arrangement]” (’883 Patent, Claims 1, 13)**

ParTec’s Construction	Microsoft’s Construction
Preamble not limiting. If limiting, plain and ordinary meaning.	Limiting

These terms appear in the preambles of asserted claims. *See, e.g.*, ’156 Patent at 20–21 (reciting, in Claim 1’s preamble, “[a] computer cluster-booster system for processing a computation task”), 15:1–2 (reciting, in Claim 14’s preamble, “[a] method for operating a computer cluster-booster arrangement for processing a computation task”). Asserting these preambles are limiting, Microsoft points to several instances during prosecution in which the applicant supposedly relied on the preamble to distinguish its claims over Krishnamurthy. Dkt. No. 123 at 15–16 (citing ’156 Patent File History, Dkt. No. 123-2 at ParTec_309–311).

ParTec says the applicant did not rely on the preamble, but instead amended the claims to include additional distinguishing claim limitations. Dkt. No. 124 at 5–6. Moreover, the claim bodies include a structurally complete invention, so there is no basis for holding the preamble is limiting. *Id.*

The Court agrees with Microsoft. During prosecution, the applicant cited two sources “to help explain the meaning of a cluster computing arrangement as understood by [a skilled artisan].” ’156 Patent File History, Dkt. No. 123-2 at ParTec_309. First, the applicant explained:

A cluster can also refer to a group of machines that work together that perform a similar function. Unlike grid computing, a computer cluster is controlled by a single software program that manages all the computers or “nodes” within the cluster. The nodes work together to complete a single task.

Id. (quoting <https://techterms.com/definition/cluster>). Second, the applicant explained:

A computer cluster consists of a set of loosely or tightly connected computers that work together so that, in many respects, they can be viewed as a single system.

Unlike grid computers, computer clusters have each node set to perform the same task, controlled and scheduled by software. The components of a cluster are usually connected to each other through fast local area networks, with each node (computer used as a server) running its own instances of an operating system.

Id. at ParTec_310 (quoting https://en.wikipedia.org/wiki/Computer_cluster). Right after these explanations, the applicant distinguished Krishnamurthy as not “directed to a computer cluster arrangement.” *Id.* Clearly, then, the applicant relied on the preambles to distinguish the cited references during prosecution.

In addition to this prosecution history, the specification repeatedly and consistently characterizes the invention as “a computer cluster arrangement.” *See, e.g.*, ’156 Patent at [54] (“Computer Cluster Arrangement for Processing a Computation Task and Method for Operation Thereof”), [57] (“The present invention is directed to a computer cluster arrangement and a method for operation of the introduced computer cluster arrangement.”), 1:18–20 (characterizing “the present invention” as “a computer cluster arrangement”). This shows the applicant regarded its invention as that sort of arrangement, which, along with the prosecution history, warrants a holding that the preamble is limiting. *See C.R. Bard, Inc. v. United States Surgical Corp.*, 388 F.3d 858, 864 (Fed. Cir. 2004) (explaining “statements that describe the invention as a whole, rather than statements that describe only preferred embodiments, are more likely to support a limiting definition of a claim term”). Accordingly, the Court finds that the preamble is limiting.

E. “outsource the [second] part of the computation task to the assigned selected [hardware] booster under control of the first [hardware] computation node” (’883 Patent, Claims 1, 13)

ParTec’s Construction	Microsoft’s Construction
Plain and ordinary meaning	“move the [second] part of the computation task from the first [hardware] computation node to the assigned booster, without implicating the resource manager”

This is a “lexicography” dispute with two parts. First, Microsoft says ParTec defined “outsource” during prosecution to mean “move.” Second, Microsoft asserts ParTec disclaimed any embodiment in which the “outsourcing” requires a “resource manager.”

1. Whether ParTec defined “outsource” as “move”

Microsoft relies on this prosecution argument from ParTec:

In the second step, the first hardware computation node uses said assignment information to outsource a part of the computation task from the first hardware computation node to the assigned booster. The claim language clearly defines that the part of the computation task is moved **from** the first hardware computation node **to** the assigned booster

’883 Patent File History, Dkt. No. 123-3 at ParTec_903–04. Because of this argument, Microsoft asserts ParTec cannot now argue “outsource” has a broader meaning. Dkt. No. 123 at 20. ParTec, however, says there’s no reason to construe the term, contending it’s “unclear what difference Microsoft perceives, if any, between these two words.” Dkt. No. 114 at 27.

The Court agrees with ParTec. Microsoft does not establish a difference in scope between “move” and “outsource.” At the hearing, Microsoft merely suggested the patentee was “using . . . a little more friendly language of moving from the computation node to the assigned booster.” Hr’g Tr., Dkt. No. 138 at 12–14. But notwithstanding friendlier language, if there is no difference in scope, there’s no reason to substitute that language for the language chosen by the patentee.

2. Whether ParTec disavowed embodiments that can also use the resource manager after the “outsourcing”

Claim 1 requires a resource manager arranged to:

assign a selected hardware booster of the plurality of hardware boosters to a first hardware computation node of the plurality of hardware computation nodes for computation of a part of the computation task,

provide assignment information to the first hardware computation node after the assignment of the selected hardware booster so as to enable the first hardware computation node to outsource the part of the computation task to the assigned selected hardware booster under control of the first hardware computation node.

'883 Patent at 13:12–23. This is substantially the same claim language² addressed by ParTec's explanation that:

A further limitation is that the output/outourcing is performed “under control of the first hardware computation node.” Accordingly, after the assignment is performed by the resource manager, the [first] hardware computation node can make use of the assignment and outsource parts of the computation tasks to the assigned boosters (without further need to implicate the resource manager).

'883 Patent File History, Dkt. No. 123-3 at ParTec_904. According to Microsoft, this shows that, “in the claims of the '883 patent, the resource manager's role is limited to assignment and, afterward, the computation node must be capable of outsourcing tasks to the booster on its own.” Dkt. No. 123 at 21–22. ParTec's briefing does not seem to dispute that's the meaning of the claim language but asserts that it doesn't require “that the resource manager *can never* be implicated in the outsourcing.” Dkt. No. 124 at 10.

The prosecution history cited by Microsoft clearly explains the meaning of “under control of the first hardware computation node:” “the [first] hardware computation node can make use of the assignment and outsource parts of the computation tasks to the assigned boosters (without further need to implicate the resource manager).” Accordingly, the Court construes this phrase as “outsource the [second] part of the computation task to the assigned selected [hardware] booster

² See '883 Patent File History, Dkt. No. 123-3 at 899 (reciting original Claim 1).

under control of the first [hardware] computation node, without further need to implicate the resource manager.”³

F. “first computing iteration,” “further computing iteration” (’442 Patent, Claims 1, 3, 7, 9)

ParTec’s Construction	Microsoft’s Construction
Plain and ordinary meaning	“an initial execution of the plurality of sub-tasks” and “a repeated execution of the plurality of sub-tasks”

The two limitations of Claim 1 of the ’442 Patent recite:

in a **first computing iteration**, assigning and processing the plurality of sub-tasks by at least a portion of the plurality of computation nodes and at least a portion of the plurality of booster nodes in a first distribution; and

generating . . . a further distribution of the plurality of sub-tasks between the plurality of computation nodes and the plurality of booster nodes for processing thereby in a **further computing iteration**.

’442 Patent at 5:33–43 (emphasis added).

The parties dispute whether “it is the same ‘plurality of sub-tasks’ that is executed in the ‘first computing iteration’ and then repeated in the ‘further computing iteration.’” Dkt. No. 123 at 26. According to ParTec, nothing requires that the subtasks in every distribution be identical. *Id.* at 25. It accuses Microsoft of trying to “backdoor” a construction for “plurality of subtasks” rather

³ At the hearing, the Court suggested its understanding was that “the resource manager cannot be further implicated in the outsourcing of the part of the computation task from the computation node to the booster.” *See* Hr’g Tr., Dkt. No. 138 at 77:20–78:7. That’s a slight overstatement of the Court’s position. The Court does not hold that the claims exclude any instrumentality in which the resource manager is “further implicated,” but only that the claims exclude any instrumentality in which the resource manager is *needed* for the outsourcing. In other words, the computation node must be capable of outsourcing tasks to the booster on its own.

than “iteration.” Dkt. No. 124 at 7. Microsoft, however, says the sub-tasks must be the same “under black letter principles of claim construction” and grammar, and ParTec’s assertion otherwise would rewrite the claim language. Dkt. No. 123 at 26.

The Court agrees with Microsoft. “Subsequent use of the definite articles ‘the’ or ‘said’ in a claim refer back to the same claim term.” *Baldwin Graphics Sys., Inc., v. Siebert, Inc.*, 512 F.3d 1338, 1342 (Fed. Cir. 2008). The specification supports the applicability of that principle to the claims, explaining that, to improve efficiency, sub-tasks initially assigned to one booster might later be redistributed to other nodes and boosters when the system determines that redistribution is more efficient. *See* ’442 Patent at 3:59–4:15.

ParTec makes two specification-based arguments in its reply, but neither is persuasive. First, ParTec says the specification teaches “‘further sub-tasks’ may be added ‘during . . . processing’ across multiple iterations and assigned to boosters that are already processing sub-tasks that depend on those ‘further sub-tasks.’” Dkt. No. 124 at 8 (ellipsis in original). For support, ParTec cites the specification’s explanation that, “as well as adjusting the distribution of sub-tasks between computation nodes and boosters based on a scalability of the sub-task, the distribution may also be influenced by information learned about the processing of the sub-task and any need to call further sub-tasks during the processing.” ’442 Patent at 4:48–63. But that explanation is not inconsistent with Microsoft’s interpretation of the claim language, because any “further sub-tasks” would simply not be part of the “plurality” recited in the claim.

Second, ParTec says the patent teaches some or all tasks may be repeated during operation. Dkt. No. 124 at 8. For support, ParTec cites the specification’s explanation that “a job to be computed by the system may comprise a number of tasks some of which or all may be repeated a number of times during the execution of the job.” ’442 Patent at 3:44–46. ParTec reasons that “if

tasks may or may not be repeated, then the subsidiary sub-tasks likewise may or may not be repeated.” Dkt. No. 124 at 9. But the claim is directed to computing a task with sub-tasks, not a job with tasks, so this language does little to inform the scope of the claim. Even so, that the sub-tasks may be repeated is not inconsistent with how the claim language plainly reads.

In essence, ParTec’s position is that “in a first iteration, the system could process a subset of sub-tasks learning about their scalability or the nodes best suited for processing. Then in a further iteration, additional sub-tasks could be added and optimally placed based on the information learned earlier.” Dkt. No. 124 at 9. But that’s not what the claim language requires. To be sure, the claim doesn’t *preclude* executing additional sub-tasks after the first iteration, but they would not be part of the recited “plurality” when determining infringement.

The Court will give this term a “plain and ordinary meaning” construction, but clarifies “the plurality of sub-tasks” refers to “a plurality of sub-tasks” in the preamble, which are the same sub-tasks throughout performance of the method.

V. CONCLUSION

Disputed Term	The Court’s Construction
“assigned to and shared by more than one of the plurality of hardware computation nodes” (’156 Patent, Claims 1, 14)	“assigned to and useable by more than one of the plurality of hardware computation nodes during processing of said computation task”
“assignment metric” (’156 Patent, Claims 1–2, 13–15; ’883 Patent, Claims 1–2, 13–15)	“a metric used for the act of assigning that is representative of one of several groups of parameters used as part of rules by which the metric is managed”
“booster” (’156 Patent, Claims 1, 4, 6–8, 12–15; ’883 Patent, Claims 1–2, 6–7, 11–13, 15)	“accelerator”

“computer cluster-booster [system/arrangement]” (’156 Patent, Claims 1, 14) “computer cluster [system/arrangement]” (’883 Patent, Claims 1, 13)	Limiting.
“outsource the [second] part of the computation task to the assigned selected [hardware] booster under control of the first [hardware] computation node” (’883 Patent, Claims 1, 13)	“outsource the [second] part of the computation task to the assigned selected [hardware] boosters under control of the first [hardware] computation node, without further need to implicate the resource manager”
“first computing iteration” / “further computing iteration” (’442 Patent, Claims 1, 3, 7, 9)	Plain and ordinary meaning

The Court **ORDERS** each party not to refer, directly or indirectly, to its own or any other party’s claim-construction positions in the presence of the jury. Likewise, the Court **ORDERS** the parties to refrain from mentioning any part of this opinion, other than the actual positions adopted by the Court, in the presence of the jury. Neither party may take a position before the jury that contradicts the Court’s reasoning in this opinion. Any reference to claim construction proceedings is limited to informing the jury of the positions adopted by the Court.

SIGNED this 17th day of February, 2026.


ROY S. PAYNE
UNITED STATES MAGISTRATE JUDGE