AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court **Western District of Texas - Waco Division** on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:23-cv-00389	5/19/2023	Western District of Texas - Waco Division

PLAINTIFF	DEFENDANT
ParkerVision, Inc.	NXP Semiconductors N.V., NXP B.V., NXP USA, Inc. d/b/a NXP Semiconductors USA, Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,483,686	1/27/2009	ParkerVision, Inc.
2	7,865,177	1/4/2011	ParkerVision, Inc.
3	9,118,528	8/25/2015	ParkerVision, Inc.
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
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3		
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court **Western District of Texas - Waco Division** on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:23-cv-00384	5/18/2023	Western District of Texas - Waco Division

PLAINTIFF	DEFENDANT
ParkerVision, Inc.	Texas Instruments Incorporated

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,496,342	2/24/2009	ParkerVision, Inc.
2	7,865,177	1/4/2011	ParkerVision, Inc.
3	9,118,528	8/25/2015	ParkerVision, Inc.
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas - Waco Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:23-cv-00374	5/16/2023	Western District of Texas - Waco Division

PLAINTIFF	DEFENDANT
ParkerVision, Inc.	Realtek Semiconductor Corp.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,879,817	4/12/2005	ParkerVision, Inc.
2	7,865,177	1/4/2011	ParkerVision, Inc.
3	9,118,528	8/25/2015	ParkerVision, Inc.
4			
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas - Waco Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:23-cv-00375	5/17/2023	Western District of Texas - Waco Division

PLAINTIFF	DEFENDANT
ParkerVision, Inc.	MediaTek Inc. and MediaTek USA Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,483,686	1/27/2009	ParkerVision, Inc.
2	7,865,177	1/4/2011	ParkerVision, Inc.
3	9,118,528	8/25/2015	ParkerVision, Inc.
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

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Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/349,802	01/07/2009	David F. SORRELLS	1744.001000P

CONFIRMATION NO. 5719

22913
Workman Nydegger
1000 Eagle Gate Tower
60 East South Temple
Salt Lake City, UT 84111

POA ACCEPTANCE LETTER

OC000000053365076

Date Mailed: 03/27/2012

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/27/2012.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/dolipscomb/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/349,802	01/07/2009	David F. SORRELLS	1744.001000P

CONFIRMATION NO. 5719

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

POWER OF ATTORNEY NOTICE

OC000000053365075

Date Mailed: 03/27/2012

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/27/2012.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/dolipscomb/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/349,802	01/07/2009	David F. SORRELLS	1744.001000P

CONFIRMATION NO. 5719

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

MISCELLANEOUS NOTICE

OC000000053322883

Date Mailed: 03/26/2012

A communication which cannot be delivered in electronic form has been mailed to the applicant.

Doc Code: N572

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/349,802	01/07/2009	David F. SORRELLS	1744.001000P

CONFIRMATION NO. 5719

OC000000053322883

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

Cc: WORKMAN NYDEGGER
1000 EAGLE GATE TOWER
60 EAST SOUTH TEMPLE
SALT LAKE CITY, UT 84111

Date Mailed: 03/26/12

DENIAL OF REQUEST FOR POWER OF ATTORNEY

The request for Power of Attorney filed 03/19/12 is acknowledged. However, the request cannot be granted at this time for the reason stated below.

- ☐ The Power of Attorney you provided did not comply with the new Power of Attorney rules that became effective on June 25, 2004. See 37 CFR 1.32.
- ☐ The revocation is not signed by the applicant, the assignee of the entire interest, or one particular principal attorney having the authority to revoke.
- ☑ The Power of Attorney is from an assignee and the Certificate required by 37 CFR 3.73(b) has not been received.
- ☐ The person signing for the assignee has omitted their empowerment to sign on behalf of the assignee.
- ☐ The inventor(s) is without authority to appoint attorneys since the assignee has intervened as provided by 37 CFR 3.71.
- ☐ The signature(s) of _____ , a co-inventor in this application, has been omitted. The Power of Attorney will be entered upon receipt of confirmation signed by said co-inventor(s).
- ☐ The person(s) appointed in the Power of Attorney is not registered to practice before the U.S. Patent and Trademark Office.

Questions relating to this Notice should be directed to the Application Assistance Unit.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PTO/SB/80 (11-08)
Approved for use through 11/30/2011. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

☑ Practitioners associated with the Customer Number: 22913

OR

☑ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:

☑ The address associated with Customer Number: 22913

OR

☐ Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

Assignee Name and Address:

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	David F. Sorrells	Date	10-27-2011
Name	David F. Sorrells	Telephone	904-732-6100
Title	CTO		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/96 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: David F. Sorrells, et al.

Application No./Patent No.: 7,865,177 Filed/Issue Date: Jan. 4, 2011

Titled: Method and System for Down-Converting an Electromagnetic Signal, and Transforms for the Same, and Aperture Relationships

ParkerVision, Inc., a corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;

2. ☐ an assignee of less than the entire right, title, and interest in (The extent (by percentage) of its ownership interest is _____ %); or

3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 011099, Frame 0249, or for which a copy therefore is attached.

OR

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature — 3-19-12 Date

Rick D. Nydegger — Attorney of Record
Printed or Typed Name — Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/47 (03-09)
Approved for use through 03/31/2012. OMB 0651-0016
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

- OR -

Fax to:
571-273-6500

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below**: If you have a Customer Number to represent the fee address. **When to check the second box below**: If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:

☐ Customer Number: 22913

OR

☐ The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
7,865,177	

Completed by (check one):

☐ Applicant/Inventor


Signature

☐ Attorney or Agent of record 28651 (Reg. No.)

Rick D. Nydegger
Typed or printed name

☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

801-533-9800
Requester's telephone number

☐ Assignee recorded at Reel _____ Frame_____

3-19-12
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more that one signature is required, see below*.

☐ * Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1. 11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313- 1450. DO NOT SEND COMPLETED FORMS TO THIS ADDRESS.
SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt	
EFS ID:	12340853
Application Number:	12349802
International Application Number:	
Confirmation Number:	5719
Title of Invention:	METHOD AND SYSTEM FOR DOWN-CONVERTING AN ELECTROMAGNETIC SIGNAL, AND TRANSFORMS FOR SAME, AND APERTURE RELATIONSHIPS
First Named Inventor/Applicant Name:	David F. SORRELLS
Customer Number:	26111
Filer:	Rick D. Nydegger/Caitlyn Ellis
Filer Authorized By:	Rick D. Nydegger
Attorney Docket Number:	1744.001000P
Receipt Date:	19-MAR-2012
Filing Date:	07-JAN-2009
Time Stamp:	19:00:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		PV1-1-1-2-2_POAs.pdf	349148 7ea54563e8ba30dc1c43221dc8597b506b655def	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Power of Attorney	1	1
	Assignee showing of ownership per 37 CFR 3.73(b).	2	2
	Change of Address	3	3
Warnings:			
Information:			
	Total Files Size (in bytes):	349148	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/349,802	01/04/2011	7865177	1744.001000P	5719

26111 7590 12/15/2010

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 22 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

David F. SORRELLS, Jacksonville, FL;
Michael J. Bultman, Jacksonville, FL;
Robert W. Cook, Switzerland, FL;
Richard C. Looke, Jacksonville, FL;
Charley D. Moses JR., Jacksonville, FL;
Gregory S. Rawlins, Lake Mary, FL;
Michael W. Rawlins, Lake Mary, FL;

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26111 7590 06/25/2010

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/349,802	01/07/2009	David F. SORRELLS	1744.001000P	5719

TITLE OF INVENTION: METHOD AND SYSTEM FOR DOWN-CONVERTING AN ELECTROMAGNETIC SIGNAL, AND TRANSFORMS FOR SAME, AND APERTURE RELATIONSHIPS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	09/27/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
BHATTACHARYA, SAM	2617	455-413000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Sterne, Kessler, Goldstein & Fox, P.L.L.C.
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: ParkerVision, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Jacksonville, Florida

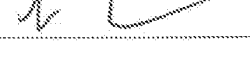
Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☒ Advance Order - # of Copies one (1)

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 19-0036 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature  Date 12/22/2010

Typed or printed name Michael Q. Lee Registration No. 35,239

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Electronic Patent Application Fee Transmittal	
Application Number:	12349802
Filing Date:	07-Jan-2009
Title of Invention:	METHOD AND SYSTEM FOR DOWN-CONVERTING AN ELECTROMAGNETIC SIGNAL, AND TRANSFORMS FOR SAME, AND APERTURE RELATIONSHIPS
First Named Inventor/Applicant Name:	David F. SORRELLS
Filer:	Viraj Dilip Tipnis/Kim Perry
Attorney Docket Number:	1744.001000P
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
Printed copy of patent - no color	8001	1	3	3
		Total in USD ($)		**1813**

Electronic Acknowledgement Receipt	
EFS ID:	8477323
Application Number:	12349802
International Application Number:	
Confirmation Number:	5719
Title of Invention:	METHOD AND SYSTEM FOR DOWN-CONVERTING AN ELECTROMAGNETIC SIGNAL, AND TRANSFORMS FOR SAME, AND APERTURE RELATIONSHIPS
First Named Inventor/Applicant Name:	David F. SORRELLS
Customer Number:	26111
Filer:	Viraj Dilip Tipnis/Kim Perry
Filer Authorized By:	Viraj Dilip Tipnis
Attorney Docket Number:	1744.001000P
Receipt Date:	22-SEP-2010
Filing Date:	07-JAN-2009
Time Stamp:	18:47:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1813
RAM confirmation Number	6795
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1		1744001000P.pdf	305186 ad2b8a5a62ccc6e06da253f35e4f7865d790f743	yes	2
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Miscellaneous Incoming Letter		1	1	
	Issue Fee Payment (PTO-85B)		2	2	
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	33729 f0afa80231e1f63dffa722802d20753e7693a44b	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	338915		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
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MICHAEL Q. LEE
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Sterne Kessler Goldstein Fox
ATTORNEYS AT LAW

September 22, 2010

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 5719
Mail Stop Issue Fee

Re: Allowed U.S. Utility Patent Application
Appl. No. 12/349,802; Filed: January 7, 2009
For: **Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same, and Aperture Relationships**
Inventors: SORRELLS *et al.*
Our Ref: 1744.001000P

Sir:

In response to the **Notice of Allowance and Fee(s) Due** dated June 25, 2010, the following documents are transmitted for appropriate action by the U.S. Patent and Trademark Office:

1. Issue Fee Transmittal (Form PTOL-85);

2. Online Credit Card Payment Authorization for $1,813.00 to cover:
$1,510.00 - Issue Fee;
$300.00 - Publication Fee; and
$3.00 - One advance copy of patent.

The above-listed documents are filed electronically through EFS-Web.

Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

MQL/VDT:bad
Enclosures

1260831_1.DOC

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/349,802	01/07/2009	David F. SORRELLS	1744.001000P	5719

26111 7590 07/06/2010

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
BHATTACHARYA, SAM	
ART UNIT	PAPER NUMBER
2617	
MAIL DATE	DELIVERY MODE
07/06/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES DEPARTMENT OF COMMERCE
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Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
12349802	1/7/2009	SORRELLS ET AL.	1744.001000P

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER
SAM BHATTACHARYA

ART UNIT	PAPER
2617	20100630

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

The IDS dated 6/28/10 is signed and attached.

/Sam Bhattacharya/
Primary Examiner, Art Unit 2617

PTO-90C (Rev.04-03)

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	14	(("7,653,145") or ("7,653,158") or ("5,222,250") or ("6,188,221") or ("7,693,230") or ("7,693,502") or ("7,697,916") or ("5,400,363") or ("6,215,830") or ("6,363,126") or ("7,724,845") or ("6,332,007") or ("5,449,939") or ("5,528,068")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/06/30 15:13
S1	12	finite adj2 time near2 integrat$3 near8 accumulat$3	US-PGPUB; USPAT; USOCR	OR	ON	2009/09/30 12:38
S2	1	("7515896").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/10/23 13:49
S3	14021	((455/413,113,118,130,131,182.1,190.1,191.1,313,323,343,350) or (327/113) or (375/130,142,143,150,152,316,343)).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/10/23 13:53
S4	1519	time near2 integrat$3 near8 accumulat$3	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/23 16:34
S5	14021	((455/413,113,118,130,131,182.1,190.1,191.1,313,323,343,350) or (327/113) or (375/130,142,143,150,152,316,343)).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/10/23 16:35
S6	66	S5 and S4	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/23 16:35
S7	12	finite adj2 time near2 integrat$3 near8 accumulat$3	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/23 16:35

S8	57	S6 not S7	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/23 16:35
S9	0	downconver$4 near7 time near2 integrat$3 near8 accumulat$3	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/23 16:40
S10	12	finite adj2 time near2 integrat$3 near8 accumulat$3	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/24 16:17
S11	3634	time near2 integrat$3 near8 (accumulat$3 sum$4 add$3)	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/24 16:47
S12	14	finite adj2 time near2 integrat$3 near8 (accumulat$3 sum$4 add$3)	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/24 16:48
S13	14	(downconvert$3 or down adj2 convert$3) near8 integrat$3 near8 (accumulat$3 sum$4 add$3)	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/24 16:49
S14	14782	((455/413,113,118,130,131,182.1,190.1,191.1,313,323,343,350) or (327/113) or (375/130,142,143,150,152,316,343)).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/05/10 10:10
S15	3	(("7515896") or ("6687493") or ("6061551")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/05/10 10:11
S16	1741	match$3 near6 (filter$3 correlat$3) near10 combin$3	US-PGPUB; USPAT; USOCR	OR	ON	2010/05/10 10:14
S17	1609	match$3 near6 filter$3 near10 combin$3	US-PGPUB; USPAT; USOCR	OR	ON	2010/05/10 10:14

S18	1395	match$3 near3 filter$3 near10 combin$3	US-PGPUB; USPAT; USOCR	OR	ON	2010/05/10 10:16
S19	324	S14 and S18	US-PGPUB; USPAT; USOCR	OR	ON	2010/05/10 10:16
S20	1	match$3 near3 filter$3 near10 combin$3 near12 (downconvert$3 or "down-converting")	US-PGPUB; USPAT; USOCR	OR	ON	2010/05/10 10:18

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S21	174	(match$3 near6 (filter$3 correlat$3) near10 combin$3).clm.	USPAT; UPAD	OR	ON	2010/05/10 10:18
S22	159	((455/413,113,118,130,131,182.1,190.1,191.1,313,323,343,350) or (327/113) or (375/130,142,143,150,152,316,343)).CCLS.	UPAD	OR	OFF	2010/05/10 10:18

6/30/2010 3:14:01 PM
C:\Documents and Settings\sbhattacharya.USPTO\My Documents\EAST\Workspaces\12349802.wsp

Equivalent of Form PTO/SB/08a (07-09)

Substitute for form 1449/PTO				Complete if Known	
FIRST SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	12/349,802
				Filing Date	January 7, 2009
				First Named Inventor	David F. SORRELLS
(Use as many sheets as necessary)				Art Unit	2617
				Examiner Name	Bhattacharya, Sam
Sheet	1	of	1	Attorney Docket Number	1744.001000P

U.S. PATENT DOCUMENTS					
Examiner initials*	Cite No.[1]	Document Number Number-Kind Code [2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	US1	7,653,145 B2	01-26-2010	Sorrells *et al.*	
	US2	7,653,158 B2	01-26-2010	Rawlins *et al.*	
	US3	5,222,250	06-22-1993	Cleveland *et al.*	
	US4	6,188,221	02-13-2001	Van de Kop *et al.*	
	US5	7,693,230 B2	04-06-2010	Sorrells *et al.*	
	US6	7,693,502 B2	04-06-2010	Sorrells *et al.*	
	US7	7,697,916 B2	04-13-2010	Sorrells *et al.*	
	US8	5,400,363	03-21-1995	Waugh *et al.*	
	US9	6,215,830 B1	04-10-2001	Temerinac *et al.*	
	US10	6,363,126 B1	03-26-2002	Furukawa *et al.*	
	US11	7,724,845 B2	05-25-2010	Sorrells *et al.*	
	US12	6,332,007 B1	12-18-2001	Sasaki	
	US13	5,449,939	09-12-1995	Horiguchi *et al.*	
	US14	5,528,068	06-18-1996	Ohmi	
	US15				
	US16				
	US17				
	US18				
	US19				

FOREIGN PATENT DOCUMENTS						
Examiner initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	FP1					
	FP2					
	FP3					
	FP4					
	FP5					
	FP6					

Examiner Signature	/Sam Bhattacharya/	Date Considered	06/30/2010

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

1131403_1.DOC

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

Substitute for form 1449/PTO

FIRST SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	12/349,802
Filing Date	January 7, 2009
First Named Inventor	David F. SORRELLS
Art Unit	2617
Examiner Name	Bhattacharya, Sam
Attorney Docket Number	1744.001000P

U.S. PATENT DOCUMENTS

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	US2	7,653,158 B2	01-26-2010	Rawlins *et al.*	
	US3	5,222,250	06-22-1993	Cleveland *et al.*	
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	US6	7,693,502 B2	04-06-2010	Sorrells *et al.*	
	US7	7,697,916 B2	04-13-2010	Sorrells *et al.*	
	US8	5,400,363	03-21-1995	Waugh *et al.*	
	US9	6,215,830 B1	04-10-2001	Temerinac *et al.*	
	US10	6,363,126 B1	03-26-2002	Furukawa *et al.*	
	US11	7,724,845 B2	05-25-2010	Sorrells *et al.*	
	US12	6,332,007 B1	12-18-2001	Sasaki	
	US13	5,449,939	09-12-1995	Horiguchi *et al.*	
	US14	5,528,068	06-18-1996	Ohmi	
	US15				
	US16				
	US17				
	US18				
	US19				

FOREIGN PATENT DOCUMENTS

Examiner initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	FP1					
	FP2					
	FP3					
	FP4					
	FP5					
	FP6					

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

1131403_1.DOC

Electronic Patent Application Fee Transmittal	
Application Number:	12349802
Filing Date:	07-Jan-2009
Title of Invention:	METHOD AND SYSTEM FOR DOWN-CONVERTING AN ELECTROMAGNETIC SIGNAL, AND TRANSFORMS FOR SAME, AND APERTURE RELATIONSHIPS
First Named Inventor/Applicant Name:	David F. SORRELLS
Filer:	Christian Andy Camarce/Valee Bartels
Attorney Docket Number:	1744.001000P
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt	
EFS ID:	7901914
Application Number:	12349802
International Application Number:	
Confirmation Number:	5719
Title of Invention:	METHOD AND SYSTEM FOR DOWN-CONVERTING AN ELECTROMAGNETIC SIGNAL, AND TRANSFORMS FOR SAME, AND APERTURE RELATIONSHIPS
First Named Inventor/Applicant Name:	David F. SORRELLS
Customer Number:	26111
Filer:	Christian Andy Camarce/Valee Bartels
Filer Authorized By:	Christian Andy Camarce
Attorney Docket Number:	1744.001000P
Receipt Date:	28-JUN-2010
Filing Date:	07-JAN-2009
Time Stamp:	12:10:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$180
RAM confirmation Number	8898
Deposit Account	190036
Authorized User	STERNE, KESSLER, GOLDSTEIN & FOX
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		1744_001000P_1st_Supplemental_IDS.pdf	520284 ad71d121307407b34cbaa8865b9f858a853e89ca	yes	9

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	2
	Transmittal Letter	3	8
	Information Disclosure Statement (IDS) Filed (SB/08)	9	9

Warnings:

Information:

2	Fee Worksheet (PTO-875)	fee-info.pdf	30717 b9f668e0fc902556401a5cda8d26da8b2aa758bd	no	2

Warnings:

Information:

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New Applications Under 35 U.S.C. 111
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National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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•Practice Limited to Federal Agencies

June 28, 2010

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Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 5719
Art Unit 2617
Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Application No. 12/349,802; Filing or 371(c) Date: January 7, 2009
For: **Method and System For Down-Converting An Electromagnetic Signal, and Transforms For Same, and Aperture Relationships**
Inventors: SORRELLS *et al.*
Our Ref: 1744.001000P

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Online Credit Card Payment Authorization in the amount of $180.00 to cover the IDS fee under 37 C.F.R. § 1.17(p);

2. First Supplemental Information Disclosure Statement; and

3. Form PTO/SB/08a (1 sheet) listing 14 documents (US1-US14).

The above-listed documents are filed electronically through EFS-Web.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Christian A. Camarce
Attorney for Applicants
Registration No. 65,021

MQL/CAC/jeg
Enclosures

1131458_1.DOC

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No. 5719
David F. SORRELLS	Art Unit: 2617
Appl. No. 12/349,802	Examiner: Bhattacharya, Sam
Filed: January 7, 2009	Atty. Docket: 1744.001000P
For: **Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same, and Aperture Relationships**	

First Supplemental Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying IDS Forms are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

Applicants provide the following comments regarding the documents:

Documents US1, US2, US5-US7, and US11 are co-owned patents which are directed to related subject matter.

Documents US3 and US4 were cited by an Examiner in U.S. Patent Application No. 12/059,333, filed March 31, 2008, entitled "Methods and Systems for Down-

Converting a Signal Using a Complementary Transistor Structure," directed to related subject matter.

Documents US8-US10 were cited by an Examiner in U.S. Patent Application No. 12/419,465, filed April 7, 2009, entitled "Down-Conversion of an Electromagnetic Signal with Feedback Control," directed to related subject matter.

Document US12 was cited by an Examiner in U.S. Patent Application No. 09/569,045, filed May 10, 2000, entitled "Universal Platform Module for a Plurality of Communication Protocols Using a Feedback Down-Conversion Embodiment," directed to related subject matter.

Documents US13 and US14 were cited by an Examiner in U.S. Patent Application No. 12/007,342, filed January 9, 2008, entitled "Method and Circuit for Down-Converting a Signal," directed to related subject matter.

This statement should not be construed as a representation that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below.

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.

☐ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.

☒ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R.

§ 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☒ c. The required fee is provided through online credit card payment authorization in the amount of $180.00 in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but on or before payment of the Issue Fee. The required fee is provided through online credit card payment authorization in the amount of $___ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. §

1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38 and MPEP 609.04(a)(III).

☐ 6. A concise explanation of the relevance of the non-English language documents appears below in accordance with 37 C.F.R. § 1.98(a)(3):

☒ 7. In accordance with 37 C.F.R. § 1.98(a)(2), no copies of U.S. patents and patent application publications cited on the attached IDS Forms are submitted.

☐ 8. Copies of the documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No._____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

☒ 9. It is expected that the examiner will review the prosecution and cited art in parent Application Nos. 09/550,644, filed April 14, 2000 (now Pat. No. 7,515,896), 09/521,879, filed March 9, 2000, 09/293,342, filed April 16, 1999, (now Pat. No. 6,687,493), and 09/176,022, filed October 21, 1998 (now Pat. No. 6,061,551), and indicate in the next communication from the office that the art cited in the earlier prosecution histories has been reviewed in connection with the present application.

☐ 10. In accordance with the Federal Circuit decision in *Dayco Prods., Inc. v. Total Containment, Inc.* 329 F.3d 1358 (Fed. Cir. 2003), Applicants submit herewith an Office Action from co-pending U.S. Patent Application No. ____. The identification of the Office Action is not to be construed as a waiver of secrecy as to the application now or upon issuance of the present application as a patent. The Examiner is respectfully requested to consider the cited application and the art cited therein during examination.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Christian A. Camarce
Attorney for Applicants
Registration No. 65,021

Date: JUNE 28, 2010

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

1131409_1.DOC

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

26111 7590 06/25/2010

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
BHATTACHARYA, SAM	
ART UNIT	PAPER NUMBER
2617	

DATE MAILED: 06/25/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/349,802	01/07/2009	David F. SORRELLS	1744.001000P	5719

TITLE OF INVENTION: METHOD AND SYSTEM FOR DOWN-CONVERTING AN ELECTROMAGNETIC SIGNAL, AND TRANSFORMS FOR SAME, AND APERTURE RELATIONSHIPS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	09/27/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26111 7590 06/25/2010

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/349,802	01/07/2009	David F. SORRELLS	1744.001000P	5719

TITLE OF INVENTION: METHOD AND SYSTEM FOR DOWN-CONVERTING AN ELECTROMAGNETIC SIGNAL, AND TRANSFORMS FOR SAME, AND APERTURE RELATIONSHIPS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	09/27/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
BHATTACHARYA, SAM	2617	455-413000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/349,802	01/07/2009	David F. SORRELLS	1744.001000P	5719

26111 7590 06/25/2010

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
BHATTACHARYA, SAM	
ART UNIT	PAPER NUMBER
2617	

DATE MAILED: 06/25/2010

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 22 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 22 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

Notice of Allowability	Application No.	Applicant(s)	
	12/349,802	SORRELLS ET AL.	
	Examiner	Art Unit	
	SAM BHATTACHARYA	2617	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the communication filed on 1/28/10*.

2. ☒ The allowed claim(s) is/are *13-27*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 13-27 are allowed.

2. The following is an examiner's statement of reasons for allowance: the prior art fails to disclose the recited combinations, including a first matched filtering/correlating module that receives an input signal, wherein said first matched filtering/correlating module down-converts said input signal according to a first control signal and outputs a first down-converted signal; a second matched filtering/correlating module that receives said input signal, wherein said second matched filtering/correlating module down-converts said input signal according to a second control signal and outputs a second down-converted signal; and a first combiner module that combines said second down-converted signal and said first down-converted signal and outputs a first channel down-converted signal, and variations thereof, as in claims 13, 26 and 27.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."Any inquiry concerning this communication or earlier communications from the examiner should be directed to SAM BHATTACHARYA whose telephone number is (571)272-7917. The examiner can normally be reached on Weekdays, 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lester Kincaid can be reached on (571) 272-7922. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Sb

/Sam Bhattacharya/
Primary Examiner, Art Unit 2617

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	14782	((455/413,113,118,130,131,182.1,190.1,191.1,313,323,343,350) or (327/113) or (375/130,142,143,150,152,316,343)).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/05/10 10:10
L2	3	(("7515896") or ("6687493") or ("6061551")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/05/10 10:11
L3	1741	match$3 near6 (filter$3 correlat$3) near10 combin$3	US-PGPUB; USPAT; USOCR	OR	ON	2010/05/10 10:14
L4	1609	match$3 near6 filter$3 near10 combin$3	US-PGPUB; USPAT; USOCR	OR	ON	2010/05/10 10:14
L5	1395	match$3 near3 filter$3 near10 combin$3	US-PGPUB; USPAT; USOCR	OR	ON	2010/05/10 10:16
L6	324	1 and 5	US-PGPUB; USPAT; USOCR	OR	ON	2010/05/10 10:16
L7	1	match$3 near3 filter$3 near10 combin$3 near12 (downconvert$3 or "down-converting")	US-PGPUB; USPAT; USOCR	OR	ON	2010/05/10 10:18
L10	305	match$3 near3 filter$3 near10 combiner	US-PGPUB; USPAT; USOCR	OR	ON	2010/05/10 10:19

L11	92	1 and 10	US-PGPUB; USPAT; USOCR	OR	ON	2010/05/10 10:19
S1	12	finite adj2 time near2 integrat$3 near8 accumulat$3	US-PGPUB; USPAT; USOCR	OR	ON	2009/09/30 12:38
S2	1	("7515896").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/10/23 13:49
S3	14021	((455/413,113,118,130,131,182.1,190.1,191.1,313,323,343,350) or (327/113) or (375/130,142,143,150,152,316,343)).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/10/23 13:53
S4	1519	time near2 integrat$3 near8 accumulat$3	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/23 16:34
S5	14021	((455/413,113,118,130,131,182.1,190.1,191.1,313,323,343,350) or (327/113) or (375/130,142,143,150,152,316,343)).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/10/23 16:35
S6	66	S5 and S4	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/23 16:35
S7	12	finite adj2 time near2 integrat$3 near8 accumulat$3	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/23 16:35
S8	57	S6 not S7	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/23 16:35
S9	0	downconver$4 near7 time near2 integrat$3 near8 accumulat$3	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/23 16:40

S10	12	finite adj2 time near2 integrat$3 near8 accumulat$3	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/24 16:17
S11	3634	time near2 integrat$3 near8 (accumulat$3 sum$4 add$3)	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/24 16:47
S12	14	finite adj2 time near2 integrat$3 near8 (accumulat$3 sum$4 add$3)	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/24 16:48
S13	14	(downconvert$3 or down adj2 convert$3) near8 integrat$3 near8 (accumulat$3 sum$4 add$3)	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/24 16:49

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L8	174	(match$3 near6 (filter$3 correlat$3) near10 combin$3).clm.	USPAT; UPAD	OR	ON	2010/05/10 10:18
L9	159	((455/413,113,118,130,131,182.1,190.1,191.1,313,323,343,350) or (327/113) or (375/130,142,143,150,152,316,343)).CCLS.	UPAD	OR	OFF	2010/05/10 10:18

5/10/2010 10:25:04 AM
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BIB DATA SHEET

CONFIRMATION NO. 5719

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/349,802	01/07/2009 RULE	455	2617	1744.001000P

APPLICANTS

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Richard C. Looke, Jacksonville, FL;
Charley D. Moses JR., Jacksonville, FL;
Gregory S. Rawlins, Lake Mary, FL;
Michael W. Rawlins, Lake Mary, FL;

**** CONTINUING DATA ***************************

This application is a DIV of 09/550,644 04/14/2000 PAT 7,515,896
which is a CIP of 09/521,879 03/09/2000 ABN
and is a CIP of 09/293,342 04/16/1999 PAT 6,687,493
which is a CIP of 09/176,022 10/21/1998 PAT 6,061,551

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

01/21/2009

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☐ No Verified and Acknowledged /SAM BHATTACHARYA/ Examiner's Signature	☐ Met after Allowance sb Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		FL	284	12	1

ADDRESS

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005
UNITED STATES

TITLE

METHOD AND SYSTEM FOR DOWN-CONVERTING AN ELECTROMAGNETIC SIGNAL, AND TRANSFORMS FOR SAME, AND APERTURE RELATIONSHIPS

FILING FEE RECEIVED		
3380	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12349802	SORRELLS ET AL.
	Examiner	Art Unit
	SAM BHATTACHARYA	2617

ORIGINAL		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
455	413	G	0	6	F	15 / 16 (2006.01.01)					

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
455	113				

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1	5	17												
	2	6	18												
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1	13														
2	14														
3	15														
4	16														

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	15	
/SAM BHATTACHARYA/ Primary Examiner.Art Unit 2617	5/7/10	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

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FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
1744.001000P	12/349,802
FIRST NAMED INVENTOR	
David F. SORRELLS	
FILING DATE	ART UNIT
January 7, 2009	2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1	2,057,613	10/1936	Gardner			
	AB1	2,241,078	05/1941	Vreeland			
	AC1	2,270,385	01/1942	Skillman			
	AD1	2,283,575	05/1942	Roberts			
	AE1	2,358,152	09/1944	Earp			
	AF1	2,410,350	10/1946	Labin *et al.*			
	AG1	2,451,430	10/1948	Barone			
	AH1	2,462,069	02/1949	Chatterjea *et al.*			
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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ1	DE 42 37 692 C1	03/1994	DE			No
	AK1	EP 0 035 166 A1	09/1981	EP			No
	AL1	EP 0 193 899 B1	06/1990	EP			N/A
	AM1	EP 0 380 351 A2	08/1990	EP			N/A

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	AN1	Aghvami, H. *et al.*, "Land Mobile Satellites Using the Highly Elliptic Orbits- The UK T-SAT Mobile Payload," *Fourth International Conference on Satellite Systems for Mobile Communications and Navigation*, IEE, pp. 147-153 (October 17-19, 1988).
	AO1	Akers, N.P. *et al.*, "RF Sampling Gates: a Brief Review," *IEE Proceedings*, IEE, Vol. 133, Part A, No. 1, pp. 45-49 (January 1986).
	AP1	Al-Ahmad, H.A.M. *et al.*, "Doppler Frequency Correction for a Non-Geostationary Communications Satellite. Techniques for CERS and T-SAT," *Electronics Division Colloquium on Low Noise Oscillators and Synthesizers,* IEE, pp. 4/1-4/5 (January 23, 1986).
	AQ1	Ali, I. *et al.*, "Doppler Characterization for LEO Satellites," *IEEE Transactions on Communications*, IEEE, Vol. 46, No. 3, pp. 309-313 (March 1998).
	AR1	Allan, D.W., "Statistics of Atomic Frequency Standards," *Proceedings Of The IEEE Special Issue on Frequency Stability*, IEEE, pp. 221-230 (February 1966).

EXAMINER	/Sam Bhattacharya/	DATE CONSIDERED	05/10/2010

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.001000P	APPLICATION NO. 12/349,802
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA2	2,472,798	06/1949	Fredendall			
	AB2	2,497,859	02/1950	Boughtwood *et al.*			
	AC2	2,499,279	02/1950	Peterson			
	AD2	2,802,208	08/1957	Hobbs			
	AE2	2,985,875	05/1961	Grisdale *et al.*			
	AF2	3,023,309	02/1962	Foulkes			
	AG2	3,069,679	12/1962	Sweeney *et al.*			
	AH2	3,104,393	09/1963	Vogelman			
	AI2	3,114,106	12/1963	McManus			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ2	EP 0 380 351 A3	02/1991	EP			N/A
	AK2	EP 0 411 840 A2	02/1991	EP			N/A
	AL2	EP 0 411 840 A3	07/1991	EP			N/A
	AM2	EP 0 411 840 B1	10/1995	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN2	Allstot, D.J. *et al.*, "MOS Switched Capacitor Ladder Filters," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-13, No. 6, pp. 806-814 (December 1978).
	AO2	Allstot, D.J. and Black Jr. W.C., "Technological Design Considerations for Monolithic MOS Switched-Capacitor Filtering Systems," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 967-986 (August 1983).
	AP2	Alouini, M. *et al.*, "Channel Characterization and Modeling for Ka-Band Very Small Aperture Terminals," *Proceedings Of the IEEE*, IEEE, Vol. 85, No. 6, pp. 981-997 (June 1997).
	AQ2	Andreyev, G.A. and Ogarev, S.A., "Phase Distortions of Keyed Millimeter-Wave Signals in the Case of Propagation in a Turbulent Atmosphere," *Telecommunications and Radio Engineering*, Scripta Technica, Vol. 43, No. 12, pp. 87-90 (December 1988).
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	FIRST NAMED INVENTOR David F. SORRELLS	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA3	3,118,117	01/1964	King *et al.*			
	AB3	3,226,643	12/1965	McNair			
	AC3	3,258,694	06/1966	Shepherd			
	AD3	3,383,598	05/1968	Sanders			
	AE3	3,384,822	05/1968	Miyagi			
	AF3	3,454,718	07/1969	Perreault			
	AG3	3,523,291	08/1970	Pierret			
	AH3	3,548,342	12/1970	Maxey			
	AI3	3,555,428	01/1971	Perreault			

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	AJ3	EP 0 423 718 A2	04/1991	EP			N/A
	AK3	EP 0 423 718 A3	08/1992	EP			N/A
	AL3	EP 0 486 095 A1	05/1992	EP			N/A
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EXAMINER INITIAL	DOC. REF.	CITATION
	AN3	Austin, J. *et al.*, "Doppler Correction of the Telecommunication Payload Oscillators in the UK T-SAT," *18th European Microwave Conference*, Microwave Exhibitions and Publishers Ltd., pp. 851-857 (September 12 - 15, 1988).
	AO3	Auston, D.H., "Picosecond optoelectronic switching and gating in silicon," *Applied Physics Letters*, American Institute of Physics, Vol. 26, No. 3, pp. 101-103 (February 1, 1975).
	AP3	Baher, H., "Transfer Functions for Switched-Capacitor and Wave Digital Filters," *IEEE Transactions on Circuits and Systems*, IEEE Circuits and Systems Society, Vol. CAS-33, No. 11, pp. 1138-1142 (November 1986).
	AQ3	Baines, R., "The DSP Bottleneck," *IEEE Communications Magazine*, IEEE Communications Society, pp. 46-54 (May 1995).
	AR3	Banjo, O.P. and Vilar, E., "Binary Error Probabilities on Earth-Space Links Subject to Scintillation Fading," *Electronics Letters*, IEE, Vol. 21, No. 7, pp. 296-297 (March 28, 1985).

EXAMINER /Sam Bhattacharya/	DATE CONSIDERED 05/10/2010

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	FILING DATE January 7, 2009	ART UNIT 2617

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA4	3,617,892	11/1971	Hawley *et al.*			
	AB4	3,621,402	11/1971	Gardner			
	AC4	3,623,160	11/1971	Giles *et al.*			
	AD4	3,626,417	12/1971	Gilbert			
	AE4	3,629,696	12/1971	Bartelink			
	AF4	3,662,268	05/1972	Gans *et al.*			
	AG4	3,689,841	09/1972	Bello *et al.*			
	AH4	3,714,577	01/1973	Hayes			
	AI4	3,717,844	02/1973	Barret *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ4	EP 0 512 748 A2	11/1992	EP			N/A
	AK4	EP 0 512 748 A3	07/1993	EP			N/A
	AL4	EP 0 512 748 B1	11/1998	EP			N/A
	AM4	EP 0 548 542 A1	06/1993	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
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	AO4	Banjo, O.P. and Vilar, E. "Measurement and Modeling of Amplitude Scintillations on Low-Elevation Earth-Space Paths and Impact on Communication Systems," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. COM-34, No. 8, pp. 774-780 (August 1986).
	AP4	Banjo, O.P. *et al.*, "Tropospheric Amplitude Spectra Due to Absorption and Scattering in Earth-Space Paths," *Fourth International Conference on Antennas and Propagation (ICAP 85)*, IEE, pp. 77-82 (April 16-19, 1985).
	AQ4	Basili,P. *et al.*, "Case Study of Intense Scintillation Events on the OTS Path," *IEEE Transactions on Antennas and Propagation*, IEEE, Vol. 38, No. 1, pp. 107-113 (January 1990).
	AR4	Basili, P. *et al.*, "Observation of High C^2 and Turbulent Path Length on OTS Space-Earth Link," *Electronics Letters*, IEE, Vol. 24, No. 17, pp. 1114-1116 (August 18, 1988).

EXAMINER /Sam Bhattacharya/	DATE CONSIDERED 05/10/2010

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	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA5	3,735,048	05/1973	Tomsa *et al.*			
	AB5	3,806,811	04/1974	Thompson			
	AC5	3,868,601	02/1975	MacAfee			
	AD5	3,949,300	04/1976	Sadler			
	AE5	3,967,202	06/1976	Batz			
	AF5	3,980,945	09/1976	Bickford			
	AG5	3,987,280	10/1976	Bauer			
	AH5	3,991,277	11/1976	Hirata			
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	AJ5	EP 0 632 288 A2	01/1995	EP			N/A
	AK5	EP 0 632 288 A3	07/1996	EP			N/A
	AL5	EP 0 696 854 A1	02/1996	EP			N/A
	AM5	EP 0 782 275 A2	07/1997	EP			N/A

NON PATENT LITERATURE DOCUMENTS

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	AN5	Blakey, J.R. *et al.*, "Measurement of Atmospheric Millimetre-Wave Phase Scintillations in an Absorption Region," *Electronics Letters*, IEE, Vol. 21, No. 11, pp. 486-487 (May 23, 1985).
	AO5	Burgueño, A. *et al.*, "Influence of rain gauge integration time on the rain rate statistics used in microwave communications," *annales des tèlècommunications*, International Union of Radio Science, pp. 522-527 (September/October 1988).
	AP5	Burgueño, A. *et al.*, "Long-Term Joint Statistical Analysis of Duration and Intensity of Rainfall Rate with Application to Microwave Communications," *Fifth International Conference on Antennas and Propagation (ICAP 87) Part 2: Propagation*, IEE, pp. 198-201 (March 30 - April 2, 1987).
	AQ5	Burgueño, A. *et al.*, "Long Term Statistics of Precipitation Rate Return Periods in the Context of Microwave Communications," *Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation*, IEE, pp. 297-301 (April 4-7, 1989).
	AR5	Burgueño, A. *et al.*, "Spectral Analysis of 49 Years of Rainfall Rate and Relation to Fade Dynamics," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 38, No. 9, pp. 1359-1366 (September 1990).

EXAMINER	/Sam Bhattacharya/	DATE CONSIDERED	05/10/2010

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

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	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA6	4,013,966	03/1977	Campbell			
	AB6	4,019,140	04/1977	Swerdlow			
	AC6	4,035,732	07/1977	Lohrmann			
	AD6	4,047,121	09/1977	Campbell			
	AE6	4,066,841	01/1978	Young			
	AF6	4,066,919	01/1978	Huntington			
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	AH6	4,130,765	12/1978	Arakelian *et al.*			
	AI6	4,130,806	12/1978	Van Gerwen *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ6	EP 0 785 635 A1	07/1997	EP			No
	AK6	EP 0 795 978 A2	09/1997	EP			N/A
	AL6	EP 0 837 565 A1	04/1998	EP			N/A
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EXAMINER INITIAL	DOC. REF.	CITATION
	AN6	Catalan, C. and Vilar, E., "Approach for satellite slant path remote sensing," *Electronics Letters,* IEE, Vol. 34, No. 12, pp. 1238-1240 (June 11, 1998).
	AO6	Chan, P. et al., "A Highly Linear 1-GHz CMOS Downconversion Mixer," *European Solid State Circuits Conference*, IEEE Communication Society, pp. 210-213 (September 22-24, 1993).
	AP6	~~Copy of Declaration of Michael L. Bultman filed in patent application Ser. No. 09/176,022, which is directed to~~ related subject matter, 2 pages.
	AQ6	~~Copy of Declaration of Robert W. Cook filed in patent application Ser. No. 09/176,022, which is directed to~~ related subject matter, 2 pages.
	AR6	~~Copy of Declaration of Alex Holtz filed in patent application Ser. No. 09/176,022, which is directed to related~~ subject matter, 3 pages.

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	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA7	4,142,155	02/1979	Adachi			
	AB7	4,170,764	10/1979	Salz *et al.*			
	AC7	4,204,171	05/1980	Sutphin, Jr.			
	AD7	4,210,872	07/1980	Gregorian			
	AE7	4,245,355	01/1981	Pascoe *et al.*			
	AF7	4,253,066	02/1981	Fisher *et al.*			
	AG7	4,253,069	02/1981	Nossek			
	AH7	4,308,614	12/1981	Fisher *et al.*			
	AI7	4,320,361	03/1982	Kikkert			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ7	EP 0 874 499 A2	10/1998	EP			N/A
	AK7	FR 2 743 231 A1	07/1997	FR			No
	AL7	GB 2 161 344 A	01/1986	GB			N/A
	AM7	GB 2 215 945 A	09/1989	GB			N/A

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN7	~~Copy of Declaration of Richard C. Looke filed in patent application Ser. No. 09/176,022, which is directed to~~ related subject matter, 2 pages.
	AO7	~~Copy of Declaration of Charley D. Moses, Jr. filed in patent application Ser. No. 09/176,022, which is directed~~ to related subject matter, 2 pages.
	AP7	~~Copy of Declaration of Jeffrey L. Parker and David F. Sorrells, with attachment Exhibit 1, filed in patent~~ application Ser. No. 09/176,022, which is directed to related subject matter, 130 pages.
	AQ7	Dewey, R.J. and Collier, C.J., "Multi-Mode Radio Receiver," *Electronics Division Colloquium on Digitally Implemented Radios,* IEE, pp. 3/1-3/5 (October 18, 1985).
	AR7	DIALOG File 347 (JAPIO) English Language Patent Abstract for JP 2-276351, 1 page (November 13, 1990 - Date of publication of application).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA8	4,320,536	03/1982	Dietrich			
	AB8	4,346,477	08/1982	Gordy			
	AC8	4,355,401	10/1982	Ikoma *et al.*			
	AD8	4,356,558	10/1982	Owen *et al.*			
	AE8	4,360,867	11/1982	Gonda			
	AF8	4,363,132	12/1982	Collin			
	AG8	4,365,217	12/1982	Berger *et al.*			
	AH8	4,370,572	01/1983	Cosand *et al.*			
	AI8	4,389,579	06/1983	Stein			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ8	JP 2-39632	02/1990	JP			No
	AK8	JP 2-131629	05/1990	JP			No
	AL8	JP 2-276351	11/1990	JP			No
	AM8	WO 80/01633 A1	08/1980	PCT			N/A

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN8	DIALOG File 347 (JAPIO) English Language Patent Abstract for JP 2-131629, 1 page (May 21, 1990 - Date of publication of application).
	AO8	DIALOG File 347 (JAPIO) English Language Patent Abstract for JP 2-39632, 1 page (February 8, 1990 - Date of publication of application).
	AP8	DIALOG File 348 (European Patents) English Language Patent Abstract for EP 0 785 635 A1, 3 pages (December 26, 1996 - Date of publication of application).
	AQ8	DIALOG File 348 (European Patents) English Language Patent Abstract for EP 35166 A1, 2 pages (February 18, 1981 - Date of publication of application).
	AR8	"DSO takes sampling rate to 1 Ghz," *Electronic Engineering*, Morgan Grampian Publishers, Vol. 59, No. 723, pp. 77 and 79 (March 1987).

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	AA9	4,392,255	07/1983	Del Giudice			
	AB9	4,430,629	02/1984	Betzl *et al.*			
	AC9	4,446,438	05/1984	Chang *et al.*			
	AD9	4,456,990	06/1984	Fisher *et al.*			
	AE9	4,472,785	09/1984	Kasuga			
	AF9	4,479,226	10/1984	Prabhu *et al.*			
	AG9	4,481,490	11/1984	Huntley			
	AH9	4,481,642	11/1984	Hanson			
	AI9	4,485,488	11/1984	Houdart			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ9	WO 94/05087 A1	03/1994	PCT			N/A
	AK9	WO 96/02977 A1	02/1996	PCT			N/A
	AL9	WO 96/08078 A1	03/1996	PCT			N/A
	AM9	WO 96/39750 A1	12/1996	PCT			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN9	Erdi, G. and Henneuse, P.R., "A Precision FET-Less Sample-and-Hold with High Charge-to-Droop Current Ratio," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-13, No. 6, pp. 864-873 (December 1978).
	AO9	Faulkner, N.D. and Vilar, E., "Subharmonic Sampling for the Measurement of Short Term Stability of Microwave Oscillators," *IEEE Transactions on Instrumentation and Measurement*, IEEE, Vol. IM-32, No. 1, pp. 208-213 (March 1983).
	AP9	Faulkner, N.D. *et al.*, "Sub-Harmonic Sampling for the Accurate Measurement of Frequency Stability of Microwave Oscillators," *CPEM 82 Digest: Conference on Precision Electromagnetic Measurements*, IEEE, pp. M-10 and M-11 (1982).
	AQ9	Faulkner, N.D. and Vilar, E., "Time Domain Analysis of Frequency Stability Using Non-Zero Dead-Time Counter Techniques," *CPEM 84 Digest Conference on Precision Electromagnetic Measurements*, IEEE, pp. 81-82 (1984).
	AR9	Filip, M. and Vilar, E., "Optimum Utilization of the Channel Capacity of a Satellite Link in the Presence of Amplitude Scintillations and Rain Attenuation," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 38, No. 11, pp. 1958-1965 (November 1990).

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	AA10	4,504,803	03/1985	Lee *et al.*			
	AB10	4,517,519	05/1985	Mukaiyama			
	AC10	4,517,520	05/1985	Ogawa			
	AD10	4,518,935	05/1985	van Roermund			
	AE10	4,521,892	06/1985	Vance *et al.*			
	AF10	4,563,773	07/1986	Dixon, Jr. *et al.*			
	AG10	4,577,157	03/1986	Reed			
	AH10	4,583,239	04/1986	Vance			
	AI10	4,591,736	05/1986	Hirao *et al.*			

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	AJ10	WO 97/38490 A1	10/1997	PCT			N/A
	AK10	WO 98/00953 A1	01/1998	PCT			N/A
	AL10	WO 98/24201 A1	06/1998	PCT			N/A
	AM10	EP 0 099 265 A1	01/1984	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN10	Fukahori, K., "A CMOS Narrow-Band Signaling Filter with Q Reduction," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-19, No. 6, pp. 926-932 (December 1984).
	AO10	Fukuchi, H. and Otsu, Y., "Available time statistics of rain attenuation on earth-space path," *IEE Proceedings-H: Microwaves, Antennas and Propagation*, IEE, Vol. 135, Pt. H, No. 6, pp. 387-390 (December 1988).
	AP10	Gibbins, C.J. and Chadha, R., "Millimetre-wave propagation through hydrocarbon flame," *IEE Proceedings*, IEE, Vol. 134, Pt. H, No.2 , pp. 169-173 (April 1987).
	AQ10	Gilchrist, B. *et al.*, "Sampling hikes performance of frequency synthesizers," *Microwaves & RF*, Hayden Publishing, Vol. 23, No. 1, pp. 93-94 and 110 (January 1984).
	AR10	Gossard, E.E., "Clear weather meteorological effects on propagation at frequencies above 1 Ghz," *Radio Science*, American Geophysical Union, Vol. 16, No. 5, pp. 589-608 (September - October 1981).

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	AA11	4,602,220	07/1986	Kurihara			
	AB11	4,603,300	07/1986	Welles, II *et al.*			
	AC11	4,612,464	09/1986	Ishikawa *et al.*			
	AD11	4,612,518	09/1986	Gans *et al.*			
	AE11	4,616,191	10/1986	Galani *et al.*			
	AF11	4,621,217	11/1986	Saxe *et al.*			
	AG11	4,628,517	12/1986	Schwarz *et al.*			
	AH11	4,634,998	01/1987	Crawford			
	AI11	4,648,021	03/1987	Alberkrack			

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	AJ11	EP 0 560 228 A1	09/1993	EP			N/A
	AK11	FR 2 245 130	04/1975	FR			Yes (See AP50)
	AL11	DE 35 41 031 A1	05/1986	DE			Yes (See AR50)
	AM11	EP 0 732 803 A1	09/1996	EP			Yes (See AN51)

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN11	Gregorian, R. *et al.*, "Switched-Capacitor Circuit Design," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 941-966 (August 1983).
	AO11	Groshong *et al.*, "Undersampling Techniques Simplify Digital Radio," *Electronic Design*, Penton Publishing, pp. 67-68, 70, 73-75 and 78 (May 23, 1991).
	AP11	Grove, W.M., "Sampling for Oscilloscopes and Other RF Systems: Dc through X-Band," *IEEE Transactions on Microwave Theory and Techniques*, IEEE, pp. 629-635 (December 1966).
	AQ11	Haddon, J. *et al.*, "Measurement of Microwave Scintillations on a Satellite Down-Link at X-Band," *Antennas and Propagation*, IEE, pp. 113-117 (1981).
	AR11	Haddon, J. and Vilar, E., "Scattering Induced Microwave Scintillations from Clear Air and Rain on Earth Space Paths and the Influence of Antenna Aperture," *IEEE Transactions on Antennas and Propagation*, IEEE, Vol. AP-34, No. 5, pp. 646-657 (May 1986).

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	AA12	4,651,034	03/1987	Sato			
	AB12	4,675,882	06/1987	Lillie *et al.*			
	AC12	4,688,253	08/1987	Gumm			
	AD12	4,716,376	12/1987	Daudelin			
	AE12	4,716,388	12/1987	Jacobs			
	AF12	4,718,113	01/1988	Rother *et al.*			
	AG12	4,726,041	02/1988	Prohaska *et al.*			
	AH12	4,733,403	03/1988	Simone			
	AI12	4,734,591	03/1988	Ichitsubo			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ12	DE 197 35 798 C1	07/1998	DE			Yes (See AP51)
	AK12	WO 98/40968 A2&A3	09/1998	PCT			N/A
	AL12	EP 0 529 836 A1	03/1993	EP			N/A
	AM12	EP 0 795 955 A2&A3	09/1997	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN12	Hafdallah, H. *et al.*, "2-4 Ghz MESFET Sampler," *Electronics Letters*, IEE, Vol. 24, No. 3, pp. 151-153 (February 4, 1988).
	AO12	Herben, M.H.A.J., "Amplitude and Phase Scintillation Measurements on 8-2 km Line-Of-Sight Path at 30 Ghz," *Electronics Letters*, IEE, Vol. 18, No. 7, pp. 287-289 (April 1, 1982).
	AP12	Hewitt, A. *et al.*, "An 18 Ghz Wideband LOS Multipath Experiment," *International Conference on Measurements for Telecommunication Transmission Systems - MTTS 85*, IEE, pp. 112-116 (November 27-28, 1985)
	AQ12	Hewitt, A. *et al.*, "An Autoregressive Approach to the Identification of Multipath Ray Parameters from Field Measurements," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 37, No. 11, pp. 1136-1143 (November 1989).
	AR12	Hewitt, A. and Vilar, E., "Selective fading on LOS Microwave Links: Classical and Spread-Spectrum Measurement Techniques," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 36, No. 7, pp. 789-796 (July 1988).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA13	4,737,969	04/1988	Steel *et al.*			
	AB13	4,743,858	05/1988	Everard			
	AC13	4,745,463	05/1988	Lu			
	AD13	4,751,468	06/1988	Agoston			
	AE13	4,757,538	07/1988	Zink			
	AF13	4,768,187	08/1988	Marshall			
	AG13	4,769,612	09/1988	Tamakoshi *et al.*			
	AH13	4,785,463	11/1988	Janc *et al.*			
	AI13	4,791,584	12/1988	Greivenkamp, Jr.			

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	AJ13	EP 0 817 369 A2&A3	01/1998	EP			N/A
	AK13	WO 91/18445 A1	11/1991	PCT			N/A
	AL13	WO 99/23755 A1	05/1999	PCT			N/A
	AM13	JP 56-114451	09/1981	JP			No

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	AN13	Hospitalier, E., "Instruments for Recording and Observing Rapidly Varying Phenomena," *Science Abstracts*, IEE, Vol. VII, pp. 22-23 (1904).
	AO13	Howard, I.M. and Swansson, N.S., "Demodulating High Frequency Resonance Signals for Bearing Fault Detection," *The Institution of Engineers Australia Vibration and Noise Conference*, Institution of Engineers, Australia, pp. 115-121 (September 18-20, 1990).
	AP13	Hu, X., *A Switched-Current Sample-and-Hold Amplifier for FM Demodulation*, Thesis for Master of Applied Science, Dept. of Electrical and Computer Engineering, University of Toronto, UMI Dissertation Services, pp. 1-64 (1995).
	AQ13	Hung, H-L. A. *et al.*, "Characterization of Microwave Integrated Circuits Using An Optical Phase-Locking and Sampling System," *IEEE MTT-S Digest*, IEEE, pp. 507-510 (1991).
	AR13	Hurst, P.J., "Shifting the Frequency Response of Switched-Capacitor Filters by Nonuniform Sampling," *IEEE Transactions on Circuits and Systems*, IEEE Circuits and Systems Society, Vol. 38, No. 1, pp. 12-19 (January 1991).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA14	4,801,823	01/1989	Yokoyama			
	AB14	4,806,790	02/1989	Sone			
	AC14	4,810,904	03/1989	Crawford			
	AD14	4,810,976	03/1989	Cowley *et al.*			
	AE14	4,811,362	03/1989	Yester, Jr. *et al.*			
	AF14	4,819,252	04/1989	Christopher			
	AG14	4,833,445	05/1989	Buchele			
	AH14	4,862,121	08/1989	Hochschild *et al.*			
	AI14	4,868,654	09/1989	Juri *et al.*			

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	AJ14	JP 8-32556	02/1996	JP			No
	AK14	JP 8-139524	05/1996	JP			No
	AL14	JP 59-144249	08/1984	JP			No
	AM14	JP 63-54002	03/1988	JP			No

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN14	Itakura, T., "Effects of the sampling pulse width on the frequency characteristics of a sample-and-hold circuit," *IEE Proceedings Circuits, Devices and Systems,* IEE, Vol. 141, No. 4, pp. 328-336 (August 1994).
	AO14	Janssen, J.M.L., "An Experimental 'Stroboscopic' Oscilloscope for Frequencies up to about 50 Mc/s: I. Fundamentals," *Philips Technical Review,* Philips Research Laboratories, Vol. 12, No. 2, pp. 52-59 (August 1950).
	AP14	Janssen, J.M.L. and Michels, A.J., "An Experimental 'Stroboscopic' Oscilloscope for Frequencies up to about 50 Mc/s: II. Electrical Build-Up," *Philips Technical Review,* Philips Research Laboratories, Vol. 12, No. 3, pp. 73-82 (September 1950).
	AQ14	Jondral, V.F. *et al.*, "Doppler Profiles for Communication Satellites," *Frequenz,* Herausberger, pp. 111-116 (May-June 1996).
	AR14	Kaleh, G.K., "A Frequency Diversity Spread Spectrum System for Communication in the Presence of In-band Interference," *1995 IEEE Globecom,* IEEE Communications Society, pp. 66-70 (1995).

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	AA15	4,870,659	09/1989	Oishi *et al.*			
	AB15	4,871,987	10/1989	Kawase			
	AC15	4,885,587	12/1989	Wiegand *et al.*			
	AD15	4,885,756	12/1989	Fontanes *et al.*			
	AE15	4,888,557	12/1989	Puckette, IV *et al.*			
	AF15	4,890,302	12/1989	Muilwijk			
	AG15	4,893,316	01/1990	Janc *et al.*			
	AH15	4,893,341	01/1990	Gehring			
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	AJ15	JP 6-237276	08/1994	JP			No
	AK15	JP 8-23359	01/1996	JP			No
	AL15	JP 47-2314	02/1972	JP			Yes (See AP53)
	AM15	JP 58-7903	01/1983	JP			Yes (See AQ53)

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	AN15	Karasawa, Y. *et al.*, "A New Prediction Method for Tropospheric Scintillation on Earth-Space Paths," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 36, No. 11, pp. 1608-1614 (November 1988).
	AO15	Kirsten, J. and Fleming, J., "Undersampling reduces data-acquisition costs for select applications," *EDN*, Cahners Publishing, Vol. 35, No. 13, pp. 217-222, 224, 226-228 (June 21, 1990).
	AP15	Lam, W.K. *et al.*, "Measurement of the Phase Noise Characteristics of an Unlocked Communications Channel Identifier," *Proceedings Of the 1993 IEEE International Frequency Control Symposium*, IEEE, pp. 283-288 (June 2-4, 1993).
	AQ15	Lam, W.K. *et al.*, "Wideband sounding of 11.6 Ghz transhorizon channel," *Electronics Letters*, IEE, Vol. 30, No. 9, pp. 738-739 (April 28, 1994).
	AR15	Larkin, K.G., "Efficient demodulator for bandpass sampled AM signals," *Electronics Letters*, IEE, Vol. 32, No. 2, pp. 101-102 (January 18, 1996).

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.001000P	APPLICATION NO. 12/349,802
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA16	4,896,152	01/1990	Tiemann			
	AB16	4,902,979	02/1990	Puckette, IV			
	AC16	4,908,579	03/1990	Tawfik *et al.*			
	AD16	4,910,752	03/1990	Yester, Jr. *et al.*			
	AE16	4,914,405	04/1990	Wells			
	AF16	4,920,510	04/1990	Senderowicz *et al.*			
	AG16	4,922,452	05/1990	Larsen *et al.*			
	AH16	4,931,921	06/1990	Anderson			
	AI16	4,944,025	07/1990	Gehring *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ16	JP 58-133004	08/1983	JP			No
	AK16	JP 60-58705	04/1985	JP			No
	AL16	JP 4-123614	04/1992	JP			No
	AM16	JP 4-127601	04/1992	JP			No

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN16	Lau, W.H. *et al.*, "Analysis of the Time Variant Structure of Microwave Line-of-sight Multipath Phenomena," *IEEE Global Telecommunications Conference & Exhibition*, IEEE, pp. 1707-1711 (November 28 - December 1, 1988).
	AO16	Lau, W.H. *et al.*, "Improved Prony Algorithm to Identify Multipath Components," *Electronics Letters*, IEE, Vol. 23, No. 20, pp. 1059-1060 (September 24, 1987).
	AP16	Lesage, P. and Audoin, C., "Effect of Dead-Time on the Estimation of the Two-Sample Variance," *IEEE Transactions on Instrumentation and Measurement*, IEEE Instrumentation and Measurement Society, Vol. IM-28, No. 1, pp. 6-10 (March 1979).
	AQ16	Liechti, C.A., "Performance of Dual-gate GaAs MESFET's as Gain-Controlled Low-Noise Amplifiers and High-Speed Modulators," *IEEE Transactions on Microwave Theory and Techniques*, IEEE Microwave Theory and Techniques Society, Vol. MTT-23, No. 6, pp. 461-469 (June 1975).
	AR16	Linnenbrink, T.E. *et al.*, "A One Gigasample Per Second Transient Recorder," *IEEE Transactions on Nuclear Science*, IEEE Nuclear and Plasma Sciences Society, Vol. NS-26, No. 4, pp. 4443-4449 (August 1979).

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	AA17	4,955,079	09/1990	Connerney *et al.*			
	AB17	4,965,467	10/1990	Bilterijst			
	AC17	4,967,160	10/1990	Quievy *et al.*			
	AD17	4,970,703	11/1990	Hariharan *et al.*			
	AE17	4,982,353	01/1991	Jacob *et al.*			
	AF17	4,984,077	01/1991	Uchida			
	AG17	4,995,055	02/1991	Weinberger *et al.*			
	AH17	5,003,621	03/1991	Gailus			
	AI17	5,005,169	04/1991	Bronder *et al.*			

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	AJ17	JP 5-175730	07/1993	JP			No
	AK17	JP 5-175734	07/1993	JP			No
	AL17	JP 7-154344	06/1995	JP			No
	AM17	JP 7-307620	11/1995	JP			No

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	AN17	Liou, M.L., "A Tutorial on Computer-Aided Analysis of Switched-Capacitor Circuits," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 987-1005 (August 1983).
	AO17	Lo, P. *et al.*, "Coherent Automatic Gain Control," *IEE Colloquium on Phase Locked Techniques*, IEE, pp. 2/1-2/6 (March 26, 1980).
	AP17	Lo, P. *et al.*, "Computation of Rain Induced Scintillations on Satellite Down-Links at Microwave Frequencies," *Third International Conference on Antennas and Propagation (ICAP 83)*, pp. 127-131 (April 12-15, 1983).
	AQ17	Lo, P.S.L.O. *et al.*, "Observations of Amplitude Scintillations on a Low-Elevation Earth-Space Path," *Electronics Letters*, IEE, Vol. 20, No. 7, pp. 307-308 (March 29, 1984).
	AR17	Madani, K. and Aithison, C.S., "A 20 Ghz Microwave Sampler," *IEEE Transactions on Microwave Theory and Techniques*, IEEE Microwave Theory and Techniques Society, Vol. 40, No. 10, pp. 1960-1963 (October 1992).

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	AA18	5,006,810	04/1991	Popescu			
	AB18	5,010,585	04/1991	Garcia			
	AC18	5,014,304	05/1991	Nicollini *et al.*			
	AD18	5,015,963	05/1991	Sutton			
	AE18	5,017,924	05/1991	Guiberteau *et al.*			
	AF18	5,020,149	05/1991	Hemmie			
	AG18	5,020,154	05/1991	Zierhut			
	AH18	5,052,050	09/1991	Collier *et al.*			
	AI18	5,065,409	11/1991	Hughes *et al.*			

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	AJ18	JP 55-66057	05/1980	JP			No
	AK18	JP 63-65587	03/1988	JP			No
	AL18	JP 63-153691	06/1988	JP			No
	AM18	EP 0 276 130 A2&A3	07/1988	EP			N/A

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	AN18	Marsland, R.A. *et al.*, "130 Ghz GaAs monolithic integrated circuit sampling head," *Appl. Phys. Lett.*, American Institute of Physics, Vol. 55, No. 6, pp. 592-594 (August 7, 1989).
	AO18	Martin, K. and Sedra, A.S., "Switched-Capacitor Building Blocks for Adaptive Systems," *IEEE Transactions on Circuits and Systems*, IEEE Circuits and Systems Society, Vol. CAS-28, No. 6, pp. 576-584 (June 1981).
	AP18	Marzano, F.S. and d'Auria, G., "Model-based Prediction of Amplitude Scintillation variance due to Clear-Air Tropospheric Turbulence on Earth-Satellite Microwave Links," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 46, No. 10, pp. 1506-1518 (October 1998).
	AQ18	Matricciani, E., "Prediction of fade durations due to rain in satellite communication systems," *Radio Science*, American Geophysical Union, Vol. 32, No. 3, pp. 935-941 (May-June 1997).
	AR18	McQueen, J.G., "The Monitoring of High-Speed Waveforms," *Electronic Engineering*, Morgan Brothers Limited, Vol. XXIV, No. 296, pp. 436-441 (October 1952).

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	AA19	5,083,050	01/1992	Vasile			
	AB19	5,091,921	02/1992	Minami			
	AC19	5,095,533	03/1992	Loper *et al.*			
	AD19	5,095,536	03/1992	Loper			
	AE19	5,111,152	05/1992	Makino			
	AF19	5,113,094	05/1992	Grace *et al.*			
	AG19	5,113,129	05/1992	Hughes			
	AH19	5,122,765	06/1992	Pataut			
	AI19	5,124,592	06/1992	Hagino			

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	AJ19	WO 95/01006 A1	01/1995	PCT			N/A
	AK19	WO 97/08839 A2&A3	03/1997	PCT			N/A
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	AN19	Merkelo, J. and Hall, R.D., "Broad-Band Thin-Film Signal Sampler," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-7, No. 1, pp. 50-54 (February 1972).
	AO19	Merlo, U. *et al.*, "Amplitude Scintillation Cycles in a Sirio Satellite-Earth Link," *Electronics Letters*, IEE, Vol. 21, No. 23, pp. 1094-1096 (November 7, 1985).
	AP19	Morris, D., "Radio-holographic reflector measurement of the 30-m millimeter radio telescope at 22 Ghz with a cosmic signal source," *Astronomy and Astrophysics*, Springer-Verlag, Vol. 203, No. 2, pp. 399-406 (September (II) 1988).
	AQ19	Moulsley, T.J. *et al.*, "The efficient acquisition and processing of propagation statistics," *Journal of the Institution of Electronic and Radio Engineers*, IERE, Vol. 55, No. 3, pp. 97-103 (March 1985).
	AR19	Ndzi, D. *et al.*, "Wide-Band Statistical Characterization of an Over-the-Sea Experimental Transhorizon Link," *IEE Colloquium on Radio Communications at Microwave and Millimetre Wave Frequencies*, IEE, pp. 1/1-1/6 (December 16, 1996).

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	AA20	5,136,267	08/1992	Cabot			
	AB20	5,140,705	08/1992	Kosuga			
	AC20	5,150,124	09/1992	Moore *et al.*			
	AD20	5,151,661	09/1992	Caldwell *et al.*			
	AE20	5,159,710	10/1992	Cusdin			
	AF20	5,170,414	12/1992	Silvian			
	AG20	5,172,070	12/1992	Hiraiwa *et al.*			
	AH20	5,191,459	03/1993	Thompson *et al.*			
	AI20	5,204,642	04/1993	Ashgar *et al.*			

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	AJ20	JP 60-130203	07/1985	JP			Yes (See AO56)
	AK20	DE 196 27 640 A1	01/1997	DE			No
	AL20	EP 0 087 336 A1	08/1983	EP			No
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	AN20	Ndzi, D. *et al.*, "Wideband Statistics of Signal Levels and Doppler Spread on an Over-The-Sea Transhorizon Link," *IEE Colloquium on Propagation Characteristics and Related System Techniques for Beyond Line-of-Sight Radio*, IEE, pp. 9/1-9/6 (November 24, 1997).
	AO20	"New zero IF chipset from Philips," *Electronic Engineering*, United News & Media, Vol. 67, No. 825, p. 10 (September 1995).
	AP20	Ohara, H. *et al.*, "First monolithic PCM filter cuts cost of telecomm systems," *Electronic Design*, Hayden Publishing Company, Vol. 27, No. 8, pp. 130-135 (April 12, 1979).
	AQ20	Oppenheim, A.V. *et al.*, *Signals and Systems*, Prentice-Hall, pp. 527-531 and 561-562 (1983).
	AR20	Ortgies, G., "Experimental Parameters Affecting Amplitude Scintillation Measurements on Satellite Links," *Electronics Letters*, IEE, Vol. 21, No. 17, pp. 771-772 (August 15, 1985).

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	AA21	5,212,827	05/1993	Meszko *et al.*			
	AB21	5,214,787	05/1993	Karkota, Jr.			
	AC21	5,220,583	06/1993	Solomon			
	AD21	5,220,680	06/1993	Lee			
	AE21	5,222,144	06/1993	Whikehart			
	AF21	5,230,097	07/1993	Currie *et al.*			
	AG21	5,239,686	08/1993	Downey			
	AH21	5,241,561	08/1993	Barnard			
	AI21	5,249,203	09/1993	Loper			

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	AJ21	EP 0 789 449 A2 & A3	08/1997	EP			N/A
	AK21	FR 2 669 787 A1	05/1992	FR			No
	AL21	GB 2 324 919 A	11/1998	GB			N/A
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EXAMINER INITIAL	DOC. REF.	CITATION
	AN21	Pärssinen et al., "A 2-GHz Subharmonic Sampler for Signal Downconversion," *IEEE Transactions on Microwave Theory and Techniques*, IEEE, Vol. 45, No. 12, 7 pages (December 1997).
	AO21	Peeters, G. *et al.*, "Evaluation of Statistical Models for Clear-Air Scintillation Prediction Using Olympus Satellite Measurements," *International Journal of Satellite Communications*, John Wiley and Sons, Vol. 15, No. 2, pp. 73-88 (March-April 1997).
	AP21	Perrey, A.G. and Schoenwetter, H.K., *NBS Technical Note 1121: A Schottky Diode Bridge Sampling Gate*, U.S. Dept. of Commerce, pp. 1-14 (May 1980).
	AQ21	Poulton, K. *et al.*, "A 1-Ghz 6-bit ADC System," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-22, No. 6, pp. 962-969 (December 1987).
	AR21	Press Release, "Parkervision, Inc. Announces Fiscal 1993 Results," Lippert/Heilshorn and Associates, 2 Pages (April 6, 1994).

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	AA22	5,251,218	10/1993	Stone *et al.*			
	AB22	5,251,232	10/1993	Nonami			
	AC22	5,260,970	11/1993	Henry *et al.*			
	AD22	5,263,194	11/1993	Ragan			
	AE22	5,263,196	11/1993	Jasper			
	AF22	5,267,023	11/1993	Kawasaki			
	AG22	5,278,826	01/1994	Murphy *et al.*			
	AH22	5,282,023	01/1994	Scarpa			
	AI22	5,287,516	02/1994	Schaub			

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	AJ22	JP 5-327356	12/1993	JP			No
	AK22	EP 0 643 477 A2 & A3	03/1995	EP			N/A
	AL22	EP 0 877 476 A1	11/1998	EP			N/A
	AM22	EP 0 977 351 A1	02/2000	EP			N/A

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN22	Press Release, "Parkervision, Inc. Announces the Appointment of Michael Baker to the New Position of National Sales Manager," Lippert/Heilshorn and Associates, 1 Page (April 7, 1994).
	AO22	Press Release, "Parkervision's Cameraman Well-Received By Distance Learning Market," Lippert/Heilshorn and Associates, 2 Pages (April 8, 1994).
	AP22	Press Release, "Parkervision, Inc. Announces First Quarter Financial Results," Lippert/Heilshorn and Associates, 2 Pages (April 26, 1994).
	AQ22	Press Release, "Parkervision, Inc. Announces The Retirement of William H. Fletcher, Chief Financial Officer," Lippert/Heilshorn and Associates, 1 Page (May 11, 1994).
	AR22	Press Release, "Parkervision, Inc. Announces New Cameraman System II™ At Infocomm Trade Show," Lippert/Heilshorn and Associates, 3 Pages (June 9, 1994).

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	AA23	5,293,398	03/1994	Hamao *et al.*			
	AB23	5,303,417	04/1994	Laws			
	AC23	5,307,517	04/1994	Rich			
	AD23	5,315,583	05/1994	Murphy *et al.*			
	AE23	5,321,852	06/1994	Seong			
	AF23	5,325,204	06/1994	Scarpa			
	AG23	5,337,014	08/1994	Najle *et al.*			
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	AJ23	WO 00/31659 A1	06/2000	PCT			N/A
	AK23	JP 9-36664	02/1997	JP			No
	AL23	DE 196 48 915 A1	06/1998	DE			Yes (See AO59)
	AM23	DE 692 21 098 T2	01/1998	DE			No

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN23	Press Release, "Parkervision, Inc. Announces Appointments to its National Sales Force," Lippert/Heilshorn and Associates, 2 Pages (June 17, 1994).
	AO23	Press Release, "Parkervision, Inc. Announces Second Quarter and Six Months Financial Results," Lippert/Heilshorn and Associates, 3 Pages (August 9, 1994).
	AP23	Press Release, "Parkervision, Inc. Announces Third Quarter and Nine Months Financial Results," Lippert/Heilshorn and Associates, 3 Pages (October 28, 1994).
	AQ23	Press Release, "Parkervision, Inc. Announces First Significant Dealer Sale of Its *Cameraman*® System II," Lippert/Heilshorn and Associates, 2 Pages (November 7, 1994).
	AR23	Press Release, "Parkervision, Inc. Announces Fourth Quarter and Year End Results," Lippert/Heilshorn and Associates, 2 Pages (March 1, 1995).

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	AC24	5,369,800	11/1994	Takagi *et al.*			
	AD24	5,375,146	12/1994	Chalmers			
	AE24	5,379,040	01/1995	Mizomoto *et al.*			
	AF24	5,379,141	01/1995	Thompson *et al.*			
	AG24	5,388,063	02/1995	Takatori *et al.*			
	AH24	5,390,364	02/1995	Webster *et al.*			
	AI24	5,400,084	03/1995	Scarpa			

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	AJ24	WO 98/53556 A2	11/1998	PCT			N/A
	AK24	DT 1936252	01/1971	DT			Yes (Doc. AO60)
	AL24	JP 62-12381	01/1987	JP			No
	AM24	JP 4-154227	05/1992	JP			No

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	AN24	Press Release, "Parkervision, Inc. Announces Joint Product Developments With VTEL," Lippert/Heilshorn and Associates, 2 Pages (March 21, 1995).
	AO24	Press Release, "Parkervision, Inc. Announces First Quarter Financial Results," Lippert/Heilshorn and Associates, 3 Pages (April 28, 1995).
	AP24	Press Release, "Parkervision Wins Top 100 Product Districts' Choice Award," Parkervision Marketing and Manufacturing Headquarters, 1 Page (June 29, 1995).
	AQ24	Press Release, "Parkervision National Sales Manager Next President of USDLA," Parkervision Marketing and Manufacturing Headquarters, 1 Page (July 6, 1995).
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	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA25	5,404,127	04/1995	Lee *et al.*			
	AB25	5,410,541	04/1995	Hotto			
	AC25	5,410,743	04/1995	Seely *et al.*			
	AD25	5,412,352	05/1995	Graham			
	AE25	5,416,803	05/1995	Janer			
	AF25	5,422,913	06/1995	Wilkinson			
	AG25	5,423,082	06/1995	Cygan *et al.*			
	AH25	5,428,638	06/1995	Cioffi *et al.*			
	AI25	5,428,640	06/1995	Townley			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ25	JP 6-284038	10/1994	JP			No
	AK25	JP 10-96778	04/1998	JP			No
	AL25	JP 11-98205	04/1999	JP			No
	AM25	JP 61-232706	10/1986	JP			No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN25	Press Release, "Parkervision, Inc. Announces Second Quarter and Six Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (July 31, 1995).
	AO25	Press Release, "Parkervision, Inc. Expands Its Cameraman System II Product Line," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (September 22, 1995).
	AP25	Press Release, "Parkervision Announces New Camera Control Technology," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 25, 1995).
	AQ25	Press Release, "Parkervision, Inc. Announces Completion of VTEL/Parkervision Joint Product Line," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 30, 1995).
	AR25	Press Release, "Parkervision, Inc. Announces Third Quarter and Nine Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 30, 1995).

EXAMINER	/Sam Bhattacharya/	DATE CONSIDERED	06/21/2010

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA26	5,434,546	07/1995	Palmer			
	AB26	5,438,692	08/1995	Mohindra			
	AC26	5,444,415	08/1995	Dent *et al.*			
	AD26	5,444,416	08/1995	Ishikawa *et al.*			
	AE26	5,444,865	08/1995	Heck *et al.*			
	AF26	5,446,421	08/1995	Kechkaylo			
	AG26	5,446,422	08/1995	Mattila *et al.*			
	AH26	5,448,602	09/1995	Ohmori *et al.*			
	AI26	5,451,899	09/1995	Lawton			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ26	JP 9-171399	06/1997	JP			No
	AK26	JP 10-41860	02/1998	JP			No
	AL26	JP 10-173563	06/1998	JP			Yes (Doc. AN62)
	AM26	JP 58-031622	02/1983	JP			No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN26	Press Release, "Parkervision's Cameraman Personal Locator Camera System Wins Telecon XV Award," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (November 1, 1995).
	AO26	Press Release, "Parkervision, Inc. Announces Purchase Commitment From VTEL Corporation," Parkervision Marketing and Manufacturing Headquarters, 1 Page (February 26, 1996).
	AP26	Press Release, "ParkerVision, Inc. Announces Fourth Quarter and Year End Results," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (February 27, 1996).
	AQ26	Press Release, "ParkerVision, Inc. Expands its Product Line," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (March 7, 1996).
	AR26	Press Release, "ParkerVision Files Patents for its Research of Wireless Technology," Parkervision Marketing and Manufacturing Headquarters, 1 Page (March 28, 1996).

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U.S. PATENT DOCUMENTS

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	AA27	5,454,007	09/1995	Dutta			
	AB27	5,454,009	09/1995	Fruit *et al.*			
	AC27	5,463,356	10/1995	Palmer			
	AD27	5,463,357	10/1995	Hobden			
	AE27	5,465,071	11/1995	Kobayashi *et al.*			
	AF27	5,465,410	11/1995	Hiben *et al.*			
	AG27	5,465,415	11/1995	Bien			
	AH27	5,471,162	11/1995	McEwan			
	AI27	5,479,120	12/1995	McEwan			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ27	JP 61-245749	11/1986	JP			No
	AK27	JP 64-048557	02/1989	JP			No
	AL27	JP 59-022438	02/1984	JP			No
	AM27	JP 59-123318	07/1984	JP			No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN27	Press Release, "Parkervision, Inc. Announces First Significant Sale of Its Cameraman® Three-Chip System," Parkervision Marketing and Manufacturing Headquarters, 2 pages (April 12, 1996).
	AO27	Press Release, "Parkervision, Inc. Introduces New Product Line For Studio Production Market," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (April 15, 1996).
	AP27	Press Release, "Parkervision, Inc. Announces Private Placement of 800,000 Shares," Parkervision Marketing and Manufacturing Headquarters, 1 Page (April 15, 1996).
	AQ27	Press Release, "Parkervision, Inc. Announces First Quarter Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (April 30, 1996).
	AR27	Press Release, "ParkerVision's New Studio Product Wins Award," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (June 5, 1996).

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	AA28	5,479,447	12/1995	Chow *et al.*			
	AB28	5,483,193	01/1996	Kennedy *et al.*			
	AC28	5,483,549	01/1996	Weinberg *et al.*			
	AD28	5,483,691	01/1996	Heck *et al.*			
	AE28	5,490,173	02/1996	Whikehart *et al.*			
	AF28	5,493,581	02/1996	Young *et al.*			
	AG28	5,493,721	02/1996	Reis			
	AH28	5,495,200	02/1996	Kwan *et al.*			
	AI28	5,495,202	02/1996	Hsu			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ28	JP 61-193521	08/1986	JP			No
	AK28	JP 62-047214	02/1987	JP			No
	AL28	JP 63-274214	11/1988	JP			No
	AM28	JP 7-169292 A	07/1995	JP			No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN28	Press Release, "Parkervision, Inc. Announces Second Quarter and Six Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (August 1, 1996).
	AO28	Press Release, "Parkervision, Inc. Announces Third Quarter and Nine Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 29, 1996).
	AP28	Press Release, "PictureTel and ParkerVision Sign Reseller Agreement," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 30, 1996).
	AQ28	Press Release, "CLI and ParkerVision Bring Enhanced Ease-of-Use to Videoconferencing," CLI/Parkervision, 2 Pages (January 20, 1997).
	AR28	Press Release, "Parkervision, Inc. Announces Fourth Quarter and Year End Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (February 27, 1997).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA29	5,495,500	02/1996	Jovanovich *et al.*			
	AB29	5,499,267	03/1996	Ohe *et al.*			
	AC29	5,500,758	03/1996	Thompson *et al.*			
	AD29	5,517,688	05/1996	Fajen *et al.*			
	AE29	5,519,890	05/1996	Pinckley			
	AF29	5,523,719	06/1996	Longo *et al.*			
	AG29	5,523,726	06/1996	Kroeger *et al.*			
	AH29	5,523,760	06/1996	McEwan			
	AI29	5,539,770	07/1996	Ishigaki			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ29	JP 10-22804 A	01/1998	JP			No
	AK29	JP 8-288882 A	11/1996	JP			No
	AL29	WO 95/19073 A2	07/1995	WO			N/A
	AM29						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN29	Press Release, "Parkervision, Inc. Announces First Quarter Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (April 29, 1997).
	AO29	Press Release, "NEC and Parkervision Make Distance Learning Closer," NEC America, 2 Pages (June 18, 1997).
	AP29	Press Release, "Parkervision Supplies JPL with Robotic Cameras, Cameraman Shot Director for Mars Mission," Parkervision Marketing and Manufacturing Headquarters, 2 pages (July 8, 1997).
	AQ29	Press Release, "ParkerVision and IBM Join Forces to Create Wireless Computer Peripherals," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (July 23, 1997).
	AR29	Press Release, "ParkerVision, Inc. Announces Second Quarter and Six Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (July 31, 1997).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA30	5,555,453	09/1996	Kajimoto *et al.*			
	AB30	5,557,641	09/1996	Weinberg			
	AC30	5,557,642	09/1996	Williams			
	AD30	5,579,341	11/1996	Smith *et al.*			
	AE30	5,579,347	11/1996	Lindquist *et al.*			
	AF30	5,584,068	12/1996	Mohindra			
	AG30	5,592,131	01/1997	Labreche *et al.*			
	AH30	5,602,847	02/1997	Pagano *et al.*			
	AI30	5,602,868	02/1997	Wilson			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ30						Yes No
	AK30						Yes No
	AL30						Yes No
	AM30						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN30	Press Release, "Parkervision, Inc. Announces Private Placement of 990,000 Shares," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (September 8, 1997).
	AO30	Press Release, "Wal-Mart Chooses Parkervision for Broadcast Production," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 24, 1997).
	AP30	Press Release, "Parkervision, Inc. Announces Third Quarter Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (October 30, 1997).
	AQ30	Press Release, "ParkerVision Announces Breakthrough in Wireless Radio Frequency Technology," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (December 10, 1997).
	AR30	Press Release, "Parkervision, Inc. Announces the Appointment of Joseph F. Skovron to the Position of Vice President, Licensing - Wireless Technologies," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (January 9, 1998).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA31	5,604,732	02/1997	Kim *et al.*			
	AB31	5,608,531	03/1997	Honda *et al.*			
	AC31	5,610,946	03/1997	Tanaka *et al.*			
	AD31	RE 35,494	04/1997	Nicollini			
	AE31	5,617,451	04/1997	Mimura *et al.*			
	AF31	5,619,538	04/1997	Sempel *et al.*			
	AG31	5,621,455	04/1997	Rogers *et al.*			
	AH31	5,630,227	05/1997	Bella *et al.*			
	AI31	5,640,415	06/1997	Pandula			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ31						Yes No
	AK31						Yes No
	AL31						Yes No
	AM31						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN31	Press Release, "Parkervision Announces Existing Agreement with IBM Terminates-- Company Continues with Strategic Focus Announced in December," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (January 27, 1998).
	AO31	Press Release, "Laboratory Tests Verify Parkervision Wireless Technology," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (March 3, 1998).
	AP31	Press Release, "Parkervision, Inc. Announces Fourth Quarter and Year End Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (March 5, 1998).
	AQ31	Press Release, "Parkervision Awarded Editors' Pick of Show for NAB 98," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (April 15, 1998).
	AR31	Press Release, "Parkervision Announces First Quarter Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (May 4, 1998).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA32	5,640,424	06/1997	Banavong *et al.*			
	AB32	5,640,428	06/1997	Abe *et al.*			
	AC32	5,640,698	06/1997	Shen *et al.*			
	AD32	5,648,985	07/1997	Bjerede *et al.*			
	AE32	5,650,785	07/1997	Rodal			
	AF32	5,661,424	08/1997	Tang			
	AG32	5,663,878	09/1997	Walker			
	AH32	5,663,986	09/1997	Striffler			
	AI32	5,668,836	09/1997	Smith *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ32						Yes No
	AK32						Yes No
	AL32						Yes No
	AM32						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN32	Press Release, "Parkervision 'DIRECT2DATA' Introduced in Response to Market Demand," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (July 9, 1998).
	AO32	Press Release, "Parkervision Expands Senior Management Team," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (July 29, 1998).
	AP32	Press Release, "Parkervision Announces Second Quarter and Six Month Financial Results," Parkervision Marketing and Manufacturing Headquarters, 4 Pages (July 30, 1998).
	AQ32	Press Release, "Parkervision Announces Third Quarter and Nine Month Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (October 30, 1998).
	AR32	Press Release, "Questar Infocomm, Inc. Invests $5 Million in Parkervision Common Stock," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (December 2, 1998).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA33	5,680,078	10/1997	Ariie			
	AB33	5,680,418	10/1997	Croft *et al.*			
	AC33	5,689,413	11/1997	Jaramillo *et al.*			
	AD33	5,699,006	12/1997	Zele *et al.*			
	AE33	5,705,955	01/1998	Freeburg *et al.*			
	AF33	5,710,998	01/1998	Opas			
	AG33	5,714,910	02/1998	Skoczen *et al.*			
	AH33	5,715,281	02/1998	Bly *et al.*			
	AI33	5,721,514	02/1998	Crockett *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ33						Yes No
	AK33						Yes No
	AL33						Yes No
	AM33						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN33	Press Release, "Parkervision Adds Two New Directors," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (March 5, 1999).
	AO33	Press Release, "Parkervision Announces Fourth Quarter and Year End Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (March 5, 1999).
	AP33	Press Release, "Joint Marketing Agreement Offers New Automated Production Solution," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (April 13, 1999).
	AQ33	"Project COST 205: Scintillations in Earth-satellite links," *Alta Frequenza: Scientific Review in Electronics*, AEI, Vol. LIV, No. 3, pp. 209-211 (May-June, 1985).
	AR33	Razavi, B., *RF Microelectronics*, Prentice-Hall, pp. 147-149 (1998).

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	AA34	5,724,002	03/1998	Hulick			
	AB34	5,724,653	03/1998	Baker *et al.*			
	AC34	5,729,577	03/1998	Chen			
	AD34	5,729,829	03/1998	Talwar *et al.*			
	AE34	5,732,333	03/1998	Cox *et al.*			
	AF34	5,736,895	04/1998	Yu *et al.*			
	AG34	5,737,035	04/1998	Rotzoll			
	AH34	5,742,189	04/1998	Yoshida *et al.*			
	AI34	5,748,683	05/1998	Smith *et al.*			

FOREIGN PATENT DOCUMENTS

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	AJ34						Yes No
	AK34						Yes No
	AL34						Yes No
	AM34						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN34	Reeves, R.J.D., "The Recording and Collocation of Waveforms (Part 1)," *Electronic Engineering*, Morgan Brothers Limited, Vol. 31, No. 373, pp. 130-137 (March 1959).
	AO34	Reeves, R.J.D., "The Recording and Collocation of Waveforms (Part 2)," *Electronic Engineering*, Morgan Brothers Limited, Vol. 31, No. 374, pp. 204-212 (April 1959).
	AP34	Rein, H.M. and Zahn, M., "Subnanosecond-Pulse Generator with Variable Pulsewidth Using Avalanche Transistors," *Electronics Letters*, IEE, Vol. 11, No. 1, pp. 21-23 (January 9, 1975).
	AQ34	Riad, S.M. and Nahman, N.S., "Modeling of the Feed-through Wideband (DC to 12.4 Ghz) Sampling-Head," *IEEE MTT-S International Microwave Symposium Digest*, IEEE, pp. 267-269 (June 27-29, 1978).
	AR34	Rizzoli, V. *et al.*, "Computer-Aided Noise Analysis of MESFET and HEMT Mixers," *IEEE Transactions on Microwave Theory and Techniques*, IEEE, Vol. 37, No. 9, pp. 1401-1410 (September 1989).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA35	RE 35,829	06/1998	Sanderford, Jr.			
	AB35	5,760,645	06/1998	Comte *et al.*			
	AC35	5,764,087	06/1998	Clark			
	AD35	5,767,726	06/1998	Wang			
	AE35	5,768,118	06/1998	Faulk *et al.*			
	AF35	5,771,442	06/1998	Wang *et al.*			
	AG35	5,777,692	07/1998	Ghosh			
	AH35	5,777,771	07/1998	Smith			
	AI35	5,786,844	07/1998	Rogers *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ35						Yes No
	AK35						Yes No
	AL35						Yes No
	AM35						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN35	Rowe, H.E., *Signals and Noise in Communication Systems*, D. Van Nostrand Company, Inc., Princeton, New Jersey, including, for example, Chapter V, Pulse Modulation Systems (1965).
	AO35	Rücker, F. and Dintelmann, F., "Effect of Antenna Size on OTS Signal Scintillations and Their Seasonal Dependence," *Electronics Letters*, IEE, Vol. 19, No. 24, pp. 1032-1034 (November 24, 1983).
	AP35	Russell, R. and Hoare, L., "Millimeter Wave Phase Locked Oscillators," *Military Microwaves '78 Conference Proceedings*, Microwave Exhibitions and Publishers, pp. 238-242 (October 25-27, 1978).
	AQ35	Sabel, L.P., "A DSP Implementation of a Robust Flexible Receiver/Demultiplexer for Broadcast Data Satellite Communications," *The Institution of Engineers Australia Communications Conference*, Institution of Engineers, Australia, pp. 218-223 (October 16-18, 1990).
	AR35	Salous, S., "IF digital generation of FMCW waveforms for wideband channel characterization," *IEE Proceedings-I*, IEE, Vol. 139, No. 3, pp. 281-288 (June 1992).

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.001000P	APPLICATION NO. 12/349,802
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA36	5,793,801	08/1998	Fertner			
	AB36	5,793,818	08/1998	Claydon *et al.*			
	AC36	5,802,463	09/1998	Zuckerman			
	AD36	5,809,060	09/1998	Cafarella *et al.*			
	AE36	5,818,582	10/1998	Fernandez *et al.*			
	AF36	5,825,254	10/1998	Lee			
	AG36	5,834,985	11/1998	Sundegård			
	AH36	5,864,754	01/1999	Hotto			
	AI36	5,881,375	03/1999	Bonds			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ36						Yes No
	AK36						Yes No
	AL36						Yes No
	AM36						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN36	"Sampling Loops Lock Sources to 23 Ghz," *Microwaves & RF*, Penton Publishing, p. 212 (September 1990).
	AO36	Sasikumar, M. *et al.*, "Active Compensation in the Switched-Capacitor Biquad," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 1008-1009 (August 1983).
	AP36	Saul, P.H., "A GaAs MESFET Sample and Hold Switch," *Fifth European Solid State Circuits Conference-ESSCIRC 79*, IEE, pp. 5-7 (1979).
	AQ36	Shen, D.H. *et al.*, "A 900-MHZ RF Front-End with Integrated Discrete-Time Filtering," *IEEE Journal of Solid-State Circuits*, IEEE Solid-State Circuits Council, Vol. 31, No. 12, pp. 1945-1954 (December 1996).
	AR36	Shen, X.D. and Vilar, E., "Anomalous transhorizon propagation and meteorological processes of a multilink path," *Radio Science*, American Geophysical Union, Vol. 30, No. 5, pp. 1467-1479 (September-October 1995).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA37	5,892,380	04/1999	Quist			
	AB37	5,894,239	04/1999	Bonaccio *et al.*			
	AC37	5,896,562	04/1999	Heinonen			
	AD37	5,900,747	05/1999	Brauns			
	AE37	5,901,054	05/1999	Leu *et al.*			
	AF37	5,901,187	05/1999	Iinuma			
	AG37	5,901,344	05/1999	Opas			
	AH37	5,901,347	05/1999	Chambers *et al.*			
	AI37	5,901,348	05/1999	Bang *et al.*			

FOREIGN PATENT DOCUMENTS

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	AJ37						Yes No
	AK37						Yes No
	AL37						Yes No
	AM37						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN37	Shen, X. and Tawfik, A.N., "Dynamic Behaviour of Radio Channels Due to Trans-Horizon Propagation Mechanisms," *Electronics Letters*, IEE, Vol. 29, No. 17, pp. 1582-1583 (August 19, 1993).
	AO37	Shen, X. *et al.*, "Modeling Enhanced Spherical Diffraction and Troposcattering on a Transhorizon Path with aid of the parabolic Equation and Ray Tracing Methods," *IEE Colloquium on Common modeling techniques for electromagnetic wave and acoustic wave propagation*, IEE, pp. 4/1-4/7 (March 8, 1996).
	AP37	Shen, X. and Vilar, E., "Path loss statistics and mechanisms of transhorizon propagation over a sea path," *Electronics Letters*, IEE, Vol. 32, No. 3, pp. 259-261 (February 1, 1996).
	AQ37	Shen, D. *et al.*, "A 900 MHZ Integrated Discrete-Time Filtering RF Front-End," *IEEE International Solid State Circuits Conference*, IEEE, Vol. 39, pp. 54-55 and 417 (February 1996).
	AR37	Spillard, C. *et al.*, "X-Band Tropospheric Transhorizon Propagation Under Differing Meteorological Conditions," *Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation*, IEE, pp. 451-455 (April 4-7, 1989).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA38	5,901,349	05/1999	Guegnaud *et al.*			
	AB38	5,903,178	05/1999	Miyatsuji *et al.*			
	AC38	5,903,187	05/1999	Claverie *et al.*			
	AD38	5,903,196	05/1999	Salvi *et al.*			
	AE38	5,903,421	05/1999	Furutani *et al.*			
	AF38	5,903,553	05/1999	Sakamoto *et al.*			
	AG38	5,903,595	05/1999	Suzuki			
	AH38	5,903,609	05/1999	Kool *et al.*			
	AI38	5,903,827	05/1999	Kennan *et al.*			

FOREIGN PATENT DOCUMENTS

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	AK38						Yes No
	AL38						Yes No
	AM38						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN38	Stafford, K.R. *et al.*, "A Complete Monolithic Sample/Hold Amplifier," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-9, No. 6, pp. 381-387 (December 1974).
	AO38	Staruk, W. Jr. *et al.*, "Pushing HF Data Rates," *Defense Electronics*, EW Communications, Vol. 17, No. 5, pp. 211, 213, 215, 217, 220 and 222 (May 1985).
	AP38	Stephenson, A.G., "Digitizing multiple RF signals requires an optimum sampling rate," *Electronics*, McGraw-Hill, pp. 106-110 (March 27, 1972).
	AQ38	Sugarman, R., "Sampling Oscilloscope for Statistically Varying Pulses," *The Review of Scientific Instruments*, American Institute of Physics, Vol. 28, No. 11, pp. 933-938 (November 1957).
	AR38	Sylvain, M., "Experimental probing of multipath microwave channels," *Radio Science*, American Geophysical Union, Vol. 24, No. 2, pp. 160-178 (March-April 1989).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA39	5,903,854	05/1999	Abe *et al.*			
	AB39	5,905,449	05/1999	Tsubouchi *et al.*			
	AC39	5,907,149	05/1999	Marckini			
	AD39	5,907,197	05/1999	Faulk			
	AE39	5,911,116	06/1999	Nosswitz			
	AF39	5,911,123	06/1999	Shaffer *et al.*			
	AG39	5,914,622	06/1999	Inoue			
	AH39	5,920,199	07/1999	Sauer			
	AI39	5,943,370	08/1999	Smith			

FOREIGN PATENT DOCUMENTS

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	AJ39						Yes No
	AK39						Yes No
	AL39						Yes No
	AM39						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN39	Takano, T., "NOVEL GaAs Pet Phase Detector Operable To Ka Band," *IEEE MT-S Digest*, IEEE, pp. 381-383 (1984).
	AO39	Tan, M.A., "Biquadratic Transconductance Switched-Capacitor Filters," *IEEE Transactions on Circuits and Systems- I: Fundamental Theory and Applications*, IEEE Circuits and Systems Society, Vol. 40, No. 4, pp. 272-275 (April 1993).
	AP39	Tanaka, K. *et al.*, "Single Chip Multisystem AM Stereo Decoder IC," *IEEE Transactions on Consumer Electronics*, IEEE Consumer Electronics Society, Vol. CE-32, No. 3, pp. 482-496 (August 1986).
	AQ39	Tawfik, A.N., "Amplitude, Duration and Predictability of Long Hop Trans-Horizon X-band Signals Over the Sea," *Electronics Letters*, IEE, Vol. 28, No. 6, pp. 571-572 (March 12, 1992).
	AR39	Tawfik, A.N. and Vilar, E., "Correlation of Transhorizon Signal Level Strength with Localized Surface Meteorological Parameters," *Eighth International Conference on Antennas and Propagation*, Electronics Division of the IEE, pp. 335-339 (March 30- April 2, 1993).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA40	4,017,798	04/1977	Gordy *et al.*			
	AB40	4,032,847	06/1977	Unkauf			
	AC40	4,253,067	02/1981	Caples *et al.*			
	AD40	4,393,395	07/1983	Hacke *et al.*			
	AE40	4,816,704	03/1989	Fiori, Jr.			
	AF40	4,841,265	06/1989	Watanabe *et al.*			
	AG40	4,943,974	07/1990	Motamedi			
	AH40	5,115,409	05/1992	Stepp			
	AI40	5,353,306	10/1994	Yamamoto			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ40						Yes No
	AK40						Yes No
	AL40						Yes No
	AM40						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN40	Tawfik, A.N. and Vilar, E., "Dynamic Structure of a Transhorizon Signal at X-band Over a Sea Path," *Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation*, IEE, pp. 446-450 (April 4-7, 1989).
	AO40	Tawfik, A.N. and Vilar, E., "Statistics of Duration and Intensity of Path Loss in a Microwave Transhorizon Sea-Path," *Electronics Letters*, IEE, Vol. 26, No. 7, pp. 474-476 (March 29, 1990).
	AP40	Tawfik, A.N. and Vilar, E., "X-Band Transhorizon Measurements of CW Transmissions Over the Sea- Part 1: Path Loss, Duration of Events, and Their Modeling," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 41, No. 11, pp. 1491-1500 (November 1993).
	AQ40	Temes, G.C. and Tsividis, T., "The Special Section on Switched-Capacitor Circuits," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 915-916 (August 1983).
	AR40	Thomas, G.B., *Calculus and Analytic Geometry*, Third Edition, Addison-Wesley Publishing, pp. 119-133 (1960).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA41	5,515,014	05/1996	Troutman			
	AB41	5,563,550	10/1996	Toth			
	AC41	5,574,755	11/1996	Persico			
	AD41	5,604,592	02/1997	Kotidis *et al.*			
	AE41	5,638,396	06/1997	Klimek			
	AF41	5,675,392	10/1997	Nayebi *et al.*			
	AG41	5,694,096	12/1997	Ushiroku *et al.*			
	AH41	5,757,870	05/1998	Miya *et al.*			
	AI41	5,768,323	06/1998	Kroeger *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ41						Yes No
	AK41						Yes No
	AL41						Yes No
	AM41						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN41	Tomassetti, Q., "An Unusual Microwave Mixer," *16th European Microwave Conference*, Microwave Exhibitions and Publishers, pp. 754-759 (September 8-12, 1986).
	AO41	Tortoli, P. *et al.*, "Bidirectional Doppler Signal Analysis Based on a Single RF Sampling Channel," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, IEEE Ultrasonics, Ferroelectrics, and Frequency Control Society, Vol. 41, No. 1, pp. 1-3 (January 1984).
	AP41	Tsividis, Y. and Antognetti, P. (Ed.), *Design of MOS VLSI Circuits for Telecommunications*, Prentice-Hall, p. 304 (1985).
	AQ41	Tsividis, Y., "Principles of Operation and Analysis of Switched-Capacitor Circuits," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 926-940 (August 1983).
	AR41	Tsurumi, H. and Maeda, T., "Design Study on a Direct Conversion Receiver Front-End for 280 MHZ, 900 MHZ, and 2.6 Ghz Band Radio Communication Systems," *41st IEEE Vehicular Technology Conference*, IEEE Vehicular Technology Society, pp. 457-462 (May 19-22, 1991).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA42	5,770,985	06/1998	Ushiroku *et al.*			
	AB42	5,778,022	07/1998	Walley			
	AC42	5,812,546	09/1998	Zhou *et al.*			
	AD42	5,818,869	10/1998	Miya *et al.*			
	AE42	5,844,449	12/1998	Abeno *et al.*			
	AF42	5,872,446	02/1999	Cranford, Jr. *et al.*			
	AG42	5,909,447	06/1999	Cox *et al.*			
	AH42	5,933,467	08/1999	Sehier *et al.*			
	AI42	5,952,895	09/1999	McCune, Jr. *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ42						Yes No
	AK42						Yes No
	AL42						Yes No
	AM42						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN42	Valdmanis, J.A. *et al.*, "Picosecond and Subpicosend Optoelectronics for Measurements of Future High Speed Electronic Devices," *IEDM Technical Digest*, IEEE, pp. 597-600 (December 5-7, 1983).
	AO42	van de Kamp, M.M.J.L., "Asymmetric signal level distribution due to tropospheric scintillation," *Electronics Letters*, IEE, Vol. 34, No. 11, pp. 1145-1146 (May 28, 1998).
	AP42	Vasseur, H. and Vanhoenacker, D., "Characterization of tropospheric turbulent layers from radiosonde data," *Electronics Letters*, IEE, Vol. 34, No. 4, pp. 318-319 (February 19, 1998).
	AQ42	Verdone, R., "Outage Probability Analysis for Short-Range Communication Systems at 60 Ghz in ATT Urban Environments," *IEEE Transactions on Vehicular Technology*, IEEE Vehicular Technology Society, Vol. 46, No. 4, pp. 1027-1039 (November 1997).
	AR42	Vierira-Ribeiro, S.A., *Single-IF DECT Receiver Architecture using a Quadrature Sub-Sampling Band-Pass Sigma-Delta Modulator*, Thesis for Degree of Master's of Engineering, Carleton University, UMI Dissertation Services, pp. 1-180 (April 1995).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA43	5,960,033	09/1999	Shibano *et al.*			
	AB43	6,041,073	03/2000	Davidovici *et al.*			
	AC43	6,054,889	04/2000	Kobayashi			
	AD43	6,084,922	07/2000	Zhou *et al.*			
	AE43	6,125,271	09/2000	Rowland *et al.*			
	AF43	6,147,340	11/2000	Levy			
	AG43	6,147,763	11/2000	Steinlechner			
	AH43	6,150,890	11/2000	Damgaard *et al.*			
	AI43	5,126,682	06/1992	Weinberg *et al.*			

FOREIGN PATENT DOCUMENTS

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	AJ43						Yes No
	AK43						Yes No
	AL43						Yes No
	AM43						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN43	Vilar, E. *et al.*, "A Comprehensive/Selective MM-Wave Satellite Downlink Experiment on Fade Dynamics," *Tenth International Conference on Antennas and Propagation*, Electronics Division of the IEE, pp. 2.98-2.101 (April 14-17, 1997).
	AO43	Vilar, E. *et al.*, "A System to Measure LOS Atmospheric Transmittance at 19 Ghz," *AGARD Conference Proceedings No. 346: Characteristics of the Lower Atmosphere Influencing Radio Wave Propagation*, AGARD, pp. 8-1 - 8-16 (October 4-7, 1983).
	AP43	Vilar, E. and Smith, H., "A Theoretical and Experimental Study of Angular Scintillations in Earth Space Paths," *IEEE Transactions on Antennas and Propagation*, IEEE, Vol. AP-34, No. 1, pp. 2-10 (January 1986).
	AQ43	Vilar, E. *et al.*, "A Wide Band Transhorizon Experiment at 11.6 Ghz," *Eighth International Conference on Antennas and Propagation*, Electronics Division of the IEE, pp. 441-445 (March 30- April 2, 1993).
	AR43	Vilar, E. and Matthews, P.A., "Amplitude Dependence of Frequency in Oscillators," *Electronics Letters*, IEE, Vol. 8, No. 20, pp. 509-511 (October 5, 1972).

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	AA44	5,841,811	11/1998	Song			
	AB44	4,051,475	09/1977	Campbell			
	AC44	5,953,642	09/1999	Feldtkeller *et al.*			
	AD44	4,653,117	03/1987	Heck			
	AE44	5,859,878	01/1999	Phillips *et al.*			
	AF44	5,894,496	04/1999	Jones			
	AG44	5,915,278	06/1999	Mallick			
	AH44	6,028,887	02/2000	Harrison *et al.*			
	AI44	6,081,691	06/2000	Renard *et al.*			

FOREIGN PATENT DOCUMENTS

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	AJ44						Yes No
	AK44						Yes No
	AL44						Yes No
	AM44						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN44	Vilar, E. *et al.*, "An experimental mm-wave receiver system for measuring phase noise due to atmospheric turbulence," *Proceedings of the 25th European Microwave Conference*, Nexus House, pp. 114-119 (1995).
	AO44	Vilar, E. and Burgueño, A., "Analysis and Modeling of Time Intervals Between Rain Rate Exceedances in the Context of Fade Dynamics," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 39, No. 9, pp. 1306-1312 (September 1991).
	AP44	Vilar, E. *et al.*, "Angle of Arrival Fluctuations in High and Low Elevation Earth Space Paths," *Fourth International Conference on Antennas and Propagation (ICAP 85)*, Electronics Division of the IEE, pp. 83-88 (April 16-19, 1985).
	AQ44	Vilar, E., "Antennas and Propagation: A Telecommunications Systems Subject," *Electronics Division Colloquium on Teaching Antennas and Propagation to Undergraduates*, IEE, pp. 7/1-7/6 (March 8, 1988).
	AR44	Vilar, E. *et al.*, "CERS*. Millimetre-Wave Beacon Package and Related Payload Doppler Correction Strategies," *Electronics Division Colloquium on CERS- Communications Engineering Research Satellite*, IEE, pp. 10/1-10/10 (April 10, 1984).

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.001000P	APPLICATION NO. 12/349,802
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA45	6,121,819	09/2000	Traylor			
	AB45	6,144,236	11/2000	Vice *et al.*			
	AC45	6,144,846	11/2000	Durec			
	AD45	6,175,728 B1	01/2001	Mitama			
	AE45	5,705,949	01/1998	Alelyunas *et al.*			
	AF45	5,883,548	03/1999	Assard *et al.*			
	AG45	4,484,143	11/1984	French *et al.*			
	AH45	5,841,324	11/1998	Williams			
	AI45	4,855,894	08/1989	Asahi *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ45						Yes No
	AK45						Yes No
	AL45						Yes No
	AM45						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN45	Vilar, E. and Moulsley, T.J., "Comment and Reply: Probability Density Function of Amplitude Scintillations," *Electronics Letters*, IEE, Vol. 21, No. 14, pp. 620-622 (July 4, 1985).
	AO45	Vilar, E. *et al.*, "Comparison of Rainfall Rate Duration Distributions for ILE-IFE and Barcelona," *Electronics Letters*, IEE, Vol. 28, No. 20, pp. 1922-1924 (September 24, 1992).
	AP45	Vilar, E., "Depolarization and Field Transmittances in Indoor Communications," *Electronics Letters*, IEE, Vol. 27, No. 9, pp. 732-733 (April 25, 1991).
	AQ45	Vilar, E. and Larsen, J.R., "Elevation Dependence of Amplitude Scintillations on Low Elevation Earth Space Paths," *Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation*, IEE, pp. 150-154 (April 4-7, 1989).
	AR45	Vilar, E. *et al.*, "Experimental System and Measurements of Transhorizon Signal Levels at 11 Ghz," *18th European Microwave Conference*, Microwave Exhibitions and Publishers Ltd., pp. 429-435 (September 12 - 15, 1988).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA46	5,319,799	06/1994	Morita			
	AB46	5,801,654	09/1998	Traylor			
	AC46	5,369,404	11/1994	Galton			
	AD46	3,716,730	02/1973	Cerny, Jr.			
	AE46	4,080,573	03/1978	Howell			
	AF46	4,334,324	06/1982	Hoover			
	AG46	4,369,522	01/1983	Cerny, Jr. *et al.*			
	AH46	5,465,418	11/1995	Zhou *et al.*			
	AI46	5,513,389	04/1996	Reeser *et al.*			

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	AJ46						Yes No
	AK46						Yes No
	AL46						Yes No
	AM46						Yes No

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN46	Vilar, E. and Matthews, P.A., "Importance of Amplitude Scintillations in Millimetric Radio Links," *Proceedings of the 4th European Microwave Conference*, Microwave Exhibitions and Publishers, pp. 202-206 (September 10-13, 1974).
	AO46	Vilar, E. and Haddon, J., "Measurement and Modeling of Scintillation Intensity to Estimate Turbulence Parameters in an Earth-Space Path," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. AP-32, No. 4, pp. 340-346 (April 1984).
	AP46	Vilar, E. and Matthews, P.A., "Measurement of Phase Fluctuations on Millimetric Radiowave Propagation," *Electronics Letters*, IEE, Vol. 7, No. 18, pp. 566-568 (September 9, 1971).
	AQ46	Vilar, E. and Wan, K.W., "Narrow and Wide Band Estimates of Field Strength for Indoor Communications in the Millimetre Band," *Electronics Division Colloquium on Radiocommunications in the Range 30-60 Ghz*, IEE, pp. 5/1-5/8 (January 17, 1991).
	AR46	Vilar, E. and Faulkner, N.D., "Phase Noise and Frequency Stability Measurements. Numerical Techniques and Limitations," *Electronics Division Colloquium on Low Noise Oscillators and Synthesizer*, IEE, 5 pages (January 23, 1986).

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	AA47	5,959,850	09/1999	Lim			
	AB47	5,157,687	10/1992	Tymes			
	AC47	5,945,660	08/1999	Nakasuji *et al.*			
	AD47	6,091,939	07/2000	Banh			
	AE47	6,091,941	07/2000	Moriyama *et al.*			
	AF47	6,098,886	08/2000	Swift *et al.*			
	AG47	6,215,475 B1	04/2001	Meyerson *et al.*			
	AH47	6,049,706	04/2000	Cook *et al.*			
	AI47	6,061,551	05/2000	Sorrells *et al.*			

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	AJ47						Yes No
	AK47						Yes No
	AL47						Yes No
	AM47						Yes No

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN47	Vilar, E. and Senin, S., "Propagation phase noise identified using 40 Ghz satellite downlink," *Electronics Letters,* IEE, Vol. 33, No. 22, pp. 1901-1902 (October 23, 1997).
	AO47	Vilar, E. *et al.*, "Scattering and Extinction: Dependence Upon Raindrop Size Distribution in Temperate (Barcelona) and Tropical (Belem) Regions," *Tenth International Conference on Antennas and Propagation,* Electronics Division of the IEE, pp. 2.230-2.233 (April 14-17, 1997).
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	AQ47	Vilar, E., "Some Limitations on Digital Transmission Through Turbulent Atmosphere," *International Conference on Satellite Communication Systems Technology,* Electronics Division of the IEE, pp. 169-187 (April 7-10, 1975).
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	AA48	6,061,555	05/2000	Bultman *et al.*			
	AB48	6,091,940	07/2000	Sorrells *et al.*			
	AC48	6,266,518 B1	07/2001	Sorrells *et al.*			
	AD48	6,353,735 B1	03/2002	Sorrells *et al.*			
	AE48	6,370,371 B1	04/2002	Sorrells *et al.*			
	AF48	5,628,055	05/1997	Stein			
	AG48	5,678,220	10/1997	Fournier			
	AH48	5,926,065	07/1999	Wakai *et al.*			
	AI48	3,622,885	11/1971	Oberdorf *et al.*			

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	AJ48						Yes No
	AK48						Yes No
	AL48						Yes No
	AM48						Yes No

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN48	Vilar, E. *et al.*, "Wideband Characterization of Scattering Channels," *Tenth International Conference on Antennas and Propagation*, Electronics Division of the IEE, pp. 2.353-2.358 (April 14-17, 1997).
	AO48	Vollmer, A., "Complete GPS Receiver Fits on Two Chips," *Electronic Design*, Penton Publishing, pp. 50, 52, 54 and 56 (July 6, 1998).
	AP48	*Voltage and Time Resolution in Digitizing Oscilloscopes: Application Note 348*, Hewlett Packard, pp. 1-11 (November 1986).
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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA49	4,483,017	11/1984	Hampel *et al.*			
	AB49	6,421,534 B1	07/2002	Cook *et al.*			
	AC49	6,330,244 B1	12/2001	Swartz *et al.*			
	AD49	4,384,357	05/1983	deBuda *et al.*			
	AE49	4,470,145	09/1984	Williams			
	AF49	5,600,680	02/1997	Mishima *et al.*			
	AG49	5,606,731	02/1997	Pace *et al.*			
	AH49	5,870,670	02/1999	Ripley *et al.*			
	AI49	6,314,279 B1	11/2001	Mohindra			

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	AJ49						Yes No
	AK49						Yes No
	AL49						Yes No
	AM49						Yes No

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN49	Wan, K.W. *et al.*, "Wideband Transhorizon Channel Sounder at 11 Ghz," *Electronics Division Colloquium on High Bit Rate UHF/SHF Channel Sounders - Technology and Measurement*, IEE, pp. 3/1-3/5 (December 3, 1993).
	AO49	Wang, H., "A 1-V Multigigahertz RF Mixer Core in 0.5 - µm CMOS," *IEEE Journal of Solid-State Circuits*, IEEE Solid-State Circuits Society, Vol. 33, No. 12, pp. 2265-2267 (December 1998).
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	AQ49	Weast, R.C. *et al.* (Ed.), *Handbook of Mathematical Tables*, Second Edition, The Chemical Rubber Co., pp. 480-485 (1964).
	AR49	Wiley, R.G., "Approximate FM Demodulation Using Zero Crossings," *IEEE Transactions on Communications*, IEEE, Vol. COM-29, No. 7, pp. 1061-1065 (July 1981).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA50	5,633,815	05/1997	Young			
	AB50	3,246,084	04/1966	Kryter			
	AC50	3,702,440	11/1972	Moore			
	AD50	3,767,984	10/1973	Shinoda *et al.*			
	AE50	3,852,530	12/1974	Shen			
	AF50	4,220,977	09/1980	Yamanaka			
	AG50	5,016,242	05/1991	Tang			
	AH50	5,937,013	08/1999	Lam *et al.*			
	AI50	6,014,551	01/2000	Pesola *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ50						Yes No
	AK50						Yes No
	AL50						Yes No
	AM50						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN50	Worthman, W., "Convergence... Again," *RF Design*, Primedia, p. 102 (March 1999).
	AO50	Young, I.A. and Hodges, D.A., "MOS Switched-Capacitor Analog Sampled-Data Direct-Form Recursive Filters," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-14, No. 6, pp. 1020-1033 (December 1979).
	AP50	Translation of Specification and Claims of FR Patent No. 2245130, 3 pages (April 18, 1975- Date of publication of application).
	AQ50	Fest, Jean-Pierre, "Le Convertisseur A/N Revolutionne Le Recepteur Radio," *Electronique*, JMJ (Publisher), No. 54, pp. 40-42 (December 1995).
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA51	6,073,001	06/2000	Sokoler			
	AB51	6,085,073	07/2000	Palermo *et al.*			
	AC51	6,400,963 B1	06/2002	Glöckler *et al.*			
	AD51	6,230,000 B1	05/2001	Tayloe			
	AE51	5,483,695	01/1996	Pardoen			
	AF51	6,542,722 B1	04/2003	Sorrells *et al.*			
	AG51	6,560,301 B1	05/2003	Cook *et al.*			
	AH51	6,098,046	08/2000	Cooper *et al.*			
	AI51	5,564,097	10/1996	Swanke			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ51						Yes No
	AK51						Yes No
	AL51						Yes No
	AM51						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN51	Translation of EP Patent No. 0 732 803 A1, 9 pages (September 18, 1996- Date of publication of application).
	AO51	Fest, Jean-Pierre, "The A/D Converter Revolutionizes the Radio Receiver," *Electronique*, JMJ (Publisher), No. 54, 3 pages (December 1995). (Translation of Doc. AQ50).
	AP51	Translation of German Patent No. DE 197 35 798 C1, 8 pages (July 16, 1998- Date of publication of application).
	AQ51	Miki, S. and Nagahama, R., *Modulation System II*, Common Edition 7, Kyoritsu Publishing Co., Ltd., pp. 146-154 (April 30, 1956).
	AR51	Miki, S. and Nagahama, R., *Modulation System II*, Common Edition 7, Kyoritsu Publishing Co., Ltd., pp. 146-149 (April 30, 1956). (Partial Translation of Doc. AQ51).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA52	5,898,912	04/1999	Heck *et al.*			
	AB52	4,660,164	04/1987	Leibowitz			
	AC52	6,580,902 B1	06/2003	Sorrells *et al.*			
	AD52	4,857,928	08/1989	Gailus *et al.*			
	AE52	5,389,839	02/1995	Heck			
	AF52	5,471,665	11/1995	Pace *et al.*			
	AG52	6,327,313 B1	12/2001	Traylor *et al.*			
	AH52	5,751,154	05/1998	Tsugai			
	AI52	5,793,817	08/1998	Wilson			

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	AJ52						Yes No
	AK52						Yes No
	AL52						Yes No
	AM52						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN52	Rabiner, L.R. and Gold, B., *Theory And Application Of Digital Signal Processing*, Prentice-Hall, Inc., pp. v-xii and 40-46 (1975).
	AO52	English-language Abstract of Japanese Patent Publication No. 08-032556, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (February 2, 1996 - Date of publication of application).
	AP52	English-language Abstract of Japanese Patent Publication No. 08-139524, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (May 31, 1996 - Date of publication of application).
	AQ52	English-language Abstract of Japanese Patent Publication No. 59-144249, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (August 18, 1984 - Date of publication of application).
	AR52	English-language Abstract of Japanese Patent Publication No. 63-054002, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (March 8, 1988 - Date of publication of application).

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	AB53	6,313,685 B1	11/2001	Rabii			
	AC53	3,614,627	10/1971	Runyan *et al.*			
	AD53	3,940,697	02/1976	Morgan			
	AE53	4,016,366	04/1977	Kurata			
	AF53	4,045,740	08/1977	Baker			
	AG53	4,115,737	09/1978	Hongu *et al.*			
	AH53	5,710,992	01/1998	Sawada *et al.*			
	AI53	5,790,587	08/1998	Smith *et al.*			

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	AJ53						Yes No
	AK53						Yes No
	AL53						Yes No
	AM53						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN53	English-language Abstract of Japanese Patent Publication No. 06-237276, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (August 23, 1994 - Date of publication of application).
	AO53	English-language Abstract of Japanese Patent Publication No. 08-023359, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (January 23, 1996 - Date of publication of application).
	AP53	Translation of Japanese Patent Publication No. 47-2314, 7 pages (February 4, 1972- Date of publication of application).
	AQ53	Partial Translation of Japanese Patent Publication No. 58-7903, 3 pages (January 17, 1983- Date of publication of application).
	AR53	English-language Abstract of Japanese Patent Publication No. 58-133004, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (August 8, 1993 - Date of publication of application).

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	AB54	5,483,600	01/1996	Werrbach			
	AC54	6,011,435	01/2000	Takeyabu *et al.*			
	AD54	6,321,073 B1	11/2001	Luz *et al.*			
	AE54	6,026,286	02/2000	Long			
	AF54	6,178,319 B1	01/2001	Kashima			
	AG54	6,634,555 B1	10/2003	Sorrells *et al.*			
	AH54	3,736,513	05/1973	Wilson			
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	AJ54						Yes No
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	AL54						Yes No
	AM54						Yes No

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	AN54	English-language Abstract of Japanese Patent Publication No. 60-058705, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (April 4, 1985 - Date of publication of application).
	AO54	English-language Abstract of Japanese Patent Publication No. 04-123614, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (April 23, 1992 - Date of publication of application).
	AP54	English-language Abstract of Japanese Patent Publication No. 04-127601, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (April 28, 1992 - Date of publication of application).
	AQ54	English-language Abstract of Japanese Patent Publication No. 05-175730, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (July 13, 1993 - Date of publication of application).
	AR54	English-language Abstract of Japanese Patent Publication No. 05-175734, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (July 13, 1993 - Date of publication of application).

EXAMINER	/Sam Bhattacharya/	DATE CONSIDERED	06/21/2010

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.001000P	APPLICATION NO. 12/349,802
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA55	4,633,510	12/1986	Suzuki *et al.*			
	AB55	5,369,789	11/1994	Kosugi *et al.*			
	AC55	5,416,449	05/1995	Joshi			
	AD55	5,438,329	08/1995	Gastouniotis *et al.*			
	AE55	6,611,569 B1	08/2003	Schier *et al.*			
	AF55	6,647,250 B1	11/2003	Bultman *et al.*			
	AG55	5,682,099	10/1997	Thompson *et al.*			
	AH55	6,094,084	07/2000	Abou-Allam *et al.*			
	AI55	6,067,329	05/2000	Kato *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ55						Yes No
	AK55						Yes No
	AL55						Yes No
	AM55						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN55	English-language Abstract of Japanese Patent Publication No. 07-154344, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (June 16, 1995 - Date of publication of application).
	AO55	English-language Abstract of Japanese Patent Publication No. 07-307620, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (November 21, 1995 - Date of publication of application).
	AP55	Oppenheim, A.V. and Schafer, R.W., *Digital Signal Processing*, Prentice-Hall, pp. vii-x, 6-35, 45-78, 87-121 and 136-165 (1975).
	AQ55	English-language Abstract of Japanese Patent Publication No. 55-066057, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (May 19, 1980 - Date of publication of application).
	AR55	English-language Abstract of Japanese Patent Publication No. 63-065587, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (March 24, 1988 - Date of publication of application).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA56	6,516,185 B1	02/2003	MacNally			
	AB56	6,608,647 B1	08/2003	King			
	AC56	6,687,493 B1	02/2004	Sorrells *et al.*			
	AD56	6,694,128 B1	02/2004	Sorrells *et al.*			
	AE56	6,031,217	02/2000	Aswell *et al.*			
	AF56	5,955,992	09/1999	Shattil			
	AG56	5,999,561	12/1999	Naden *et al.*			
	AH56	6,686,879 B2	02/2004	Shattil			
	AI56	6,704,549 B1	03/2004	Sorrells *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ56						Yes No
	AK56						Yes No
	AL56						Yes No
	AM56						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN56	English-language Abstract of Japanese Patent Publication No. 63-153691, from *http://www1.ipdl.jpo.go.jp,* 2 Pages (June 27, 1988 - Date of publication of application).
	AO56	Translation of Japanese Patent Publication No. 60-130203, 3 pages (July 11, 1985- Date of publication of application).
	AP56	Razavi, B., "A 900-MHz/1.8-Ghz CMOS Transmitter for Dual-Band Applications," *Symposium on VLSI Circuits Digest of Technical Papers*, IEEE, pp. 128-131 (1998).
	AQ56	Ritter, G.M., "SDA, A New Solution for Transceivers," *16th European Microwave Conference*, Microwave Exhibitions and Publishers, pp. 729-733 (September 8, 1986).
	AR56	DIALOG File 351 (Derwent WPI) English Language Patent Abstract for FR 2 669 787, 1 page (May 29, 1992- Date of publication of application).

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	AA57	6,704,558 B1	03/2004	Sorrells *et al.*			
	AB57	5,490,176	02/1996	Peltier			
	AC57	5,970,053	10/1999	Schick *et al.*			
	AD57	6,078,630	06/2000	Prasanna			
	AE57	6,600,911 B1	07/2003	Morishige *et al.*			
	AF57	5,179,731	01/1993	Tränkle *et al.*			
	AG57	5,589,793	12/1996	Kassapian			
	AH57	4,510,467	04/1985	Chang *et al.*			
	AI57	4,772,853	09/1988	Hart			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ57						Yes No
	AK57						Yes No
	AL57						Yes No
	AM57						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN57	Akos, D.M. *et al.*, "Direct Bandpass Sampling of Multiple Distinct RF Signals," *IEEE Transactions on Communications*, IEEE, Vol. 47, No. 7, pp. 983-988 (July 1999).
	AO57	Patel, M. *et al.*, "Bandpass Sampling for Software Radio Receivers, and the Effect of Oversampling on Aperture Jitter," *VTC 2002*, IEEE, pp. 1901-1905 (2002).
	AP57	English-language Abstract of Japanese Patent Publication No. 61-030821, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (February 13, 1986- Date of publication of application).
	AQ57	English-language Abstract of Japanese Patent Publication No. 05-327356, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (December 10, 1993 - Date of publication of application).
	AR57	Tayloe, D., "A Low-noise, High-performance Zero IF Quadrature Detector/Preamplifier," *RF Design*, Primedia Business Magazines & Media, Inc., pp. 58, 60, 62 and 69 (March 2003).

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	FILING DATE January 7, 2009	ART UNIT 2617

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA58	4,972,436	11/1990	Halim *et al.*			
	AB58	5,012,245	04/1991	Scott *et al.*			
	AC58	5,422,909	06/1995	Love *et al.*			
	AD58	5,440,311	08/1995	Gallagher *et al.*			
	AE58	5,926,513	07/1999	Suominen *et al.*			
	AF58	5,995,030	11/1999	Cabler			
	AG58	6,047,026	04/2000	Chao *et al.*			
	AH58	6,049,573	04/2000	Song			
	AI58	6,076,015	06/2000	Hartley *et al.*			

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	AJ58						Yes No
	AK58						Yes No
	AL58						Yes No
	AM58						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN58	Dines, J.A.B., "Smart Pixel Optoelectronic Receiver Based on a Charge Sensitive Amplifier Design," *IEEE Journal of Selected Topics in Quantum Electronics*, IEEE, Vol. 2, No. 1, pp. 117-120 (April 1996).
	AO58	Simoni, A. *et al.*, "A Digital Camera for Machine Vision," *20th International Conference on Industrial Electronics, Control and Instrumentation*, IEEE, pp. 879-883 (September 1994).
	AP58	Stewart, R.W. and Pfann, E., "Oversampling and sigma-delta strategies for data conversion," *Electronics & Communication Engineering Journal*, IEEE, pp. 37-47 (February 1998).
	AQ58	Rudell, J.C. *et al.*, "A 1.9-Ghz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 32, No. 12, pp. 2071-2088 (December 1997).
	AR58	English-language Abstract of Japanese Patent Publication No. 09-036664, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (February 7, 1997 - Date of publication of application).

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	AA59	6,144,331	11/2000	Jiang			
	AB59	6,018,553	01/2000	Sanielevici *et al.*			
	AC59	6,317,589 B1	11/2001	Nash			
	AD59	5,058,107	10/1991	Stone *et al.*			
	AE59	5,757,858	05/1998	Black *et al.*			
	AF59	6,531,979 B1	03/2003	Hynes			
	AG59	6,018,262	01/2000	Noro *et al.*			
	AH59	4,761,798	08/1988	Griswold, Jr. *et al.*			
	AI59	5,982,315	11/1999	Bazarjani *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ59						Yes No
	AK59						Yes No
	AL59						Yes No
	AM59						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN59	Simoni, A. *et al.*, "A Single-Chip Optical Sensor with Analog Memory for Motion Detection," *IEEE Journal of Solid-State Circtuits*, IEEE, Vol. 30, No. 7, pp. 800-806 (July 1995).
	~~AO59~~	~~English Translation of German Patent Publication No. DE 196 48 045 A1, 18 pages.~~
	AP59	Deboo, Gordon J., *Integrated Circuits and Semiconductor Devices*, 2nd Edition, McGraw-Hill, Inc., pp. 41-45 (1977).
	AQ59	Hellwarth, G.A. and Jones, G.D, "Automatic Conditioning of Speech Signals," *IEEE Transactions on Audio and Electroacoustics*, Vol. AU-16, No. 2, pp. 169-179 (June 1968).
	~~AR59~~	~~English Abstract for German Patent No. DE 602 21 088 T2, 1 page, data supplied from the espacenet.~~

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	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA60	6,459,721 B1	10/2002	Mochizuki *et al.*			
	AB60	6,151,354	11/2000	Abbey			
	AC60	6,169,733 B1	01/2001	Lee			
	AD60	6,363,262 B1	03/2002	McNicol			
	AE60	6,697,603 B1	02/2004	Lovinggood *et al.*			
	AF60	5,282,222	01/1994	Fattouche *et al.*			
	AG60	5,949,827	09/1999	DeLuca *et al.*			
	AH60	6,014,176	01/2000	Nayebi *et al.*			
	AI60	5,678,226	10/1997	Li *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ60						Yes No
	AK60						Yes No
	AL60						Yes No
	AM60						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN60	Gaudiosi, J., "Retailers will bundle Microsoft's Xbox with games and peripherals," *Video Store Magazine*, Volume 23, Issue 36, pg. 8, 2 pages (September 2-8, 2001).
	AO60	English-language Translation of German Patent Publication No. DT 1936252, translation provided by Transperfect Translations, 12 pages (January 28, 1971 - Date of publication of application).
	AP60	English-language Abstract of Japanese Patent Publication No. JP 62-12381, data supplied by the espacenet, 1 page (January 21, 1987 - Date of publication of application).
	AQ60	English-language Abstract of Japanese Patent Publication No. JP 4-154227, data supplied by the espacenet, 1 page (May 27, 1992 - Date of publication of application).
	AR60	English-language Abstract of Japanese Patent Publication No. JP 6-284038, data supplied by the espacenet, 1 page (October 7, 1994 - Date of publication of application).

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	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA61	5,760,632	06/1998	Kawakami *et al.*			
	AB61	6,160,280	12/2000	Bonn *et al.*			
	AC61	5,481,570	01/1996	Winters			
	AD61	5,745,846	04/1998	Myer *et al.*			
	AE61	5,345,239	09/1994	Madni *et al.*			
	AF61	4,132,952	01/1979	Hongu *et al.*			
	AG61	5,260,973	11/1993	Watanabe			
	AH61	6,307,894 B2	10/2001	Eidson *et al.*			
	AI61	6,091,289	07/2000	Song *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ61						Yes No
	AK61						Yes No
	AL61						Yes No
	AM61						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN61	English-language Abstract of Japanese Patent Publication No. JP 10-96778, data supplied by the espacenet, 1 page (April 14, 1998 - Date of publication of application).
	AO61	English-language Abstract of Japanese Patent Publication No. JP 11-98205, data supplied by the espacenet, 1 page (April 9, 1999 - Date of publication of application).
	AP61	English-language Abstract of Japanese Patent Publication No. JP 61-232706, data supplied by the espacenet, 1 page (October 17, 1986 - Date of publication of application).
	AQ61	English-language Abstract of Japanese Patent Publication No. JP 9-171399, data supplied by the espacenet, 1 page (June 30, 1997 - Date of publication of application).
	AR61	English-language Abstract of Japanese Patent Publication No. JP 10-41860, data supplied by the espacenet, 1 page (February 13, 1998 - Date of publication of application).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA62	6,437,639 B1	08/2002	Nguyen *et al.*			
	AB62	2002/0037706 A1	03/2002	Ichihara			
	AC62	4,441,080	04/1984	Saari			
	AD62	4,873,492	10/1989	Myer			
	AE62	5,697,074	12/1997	Makikallio *et al.*			
	AF62	5,784,689	07/1998	Kobayashi			
	AG62	6,335,656 B1	01/2002	Goldfarb *et al.*			
	AH62	6,690,232 B2	02/2004	Ueno *et al.*			
	AI62	5,636,140	06/1997	Lee *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ62						Yes No
	AK62						Yes No
	AL62						Yes No
	AM62						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN62	English-language Computer Translation of Japanese Patent Publication No. JP 10-41860, provided by the JPO (June 26, 1998 - Date of publication of application) and cited in U.S. Patent Application Ser. No. 10/305,299, directed to related subject matter.
	AO62	*What is I/Q Data?*, printed September 16, 2006, from http://zone.ni.com, 8 pages (Copyright 2003).
	AP62	English-language Abstract of Japanese Patent Publication No. JP 58-031622, data supplied by ep.espacenet.com, 1 page (Feb. 24, 1983 - Date of publication of application).
	AQ62	English-language Abstract of Japanese Patent Publication No. JP 61-245749, data supplied by ep.espacenet.com, 1 page (Nov. 1, 1986 - Date of publication of application).
	AR62	English-language Abstract of Japanese Patent Publication No. JP 64-048557, data supplied by ep.espacenet.com, 1 page (Feb. 23, 1989 - Date of publication of application).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
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	AB63	6,600,795 B1	07/2003	Ohta *et al.*			
	AC63	4,250,458	02/1981	Richmond *et al.*			
	AD63	5,760,629	06/1998	Urabe *et al.*			
	AE63	6,084,465	07/2000	Dasqupta			
	AF63	6,204,789 B1	03/2001	Nagata			
	AG63	6,064,054	05/2000	Waczynski *et al.*			
	AH63	5,218,562	06/1993	Basehore *et al.*			
	AI63	5,239,496	08/1993	Vancraeynest			

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	AJ63						Yes No
	AK63						Yes No
	AL63						Yes No
	AM63						Yes No

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	AP63	English-language Abstract of Japanese Patent Publication No. JP 61-193521, data supplied by ep.espacenet.com, 1 page (Aug. 28, 1986 - Date of publication of application).
	AQ63	English-language Abstract of Japanese Patent Publication No. JP 62-047214, data supplied by ep.espacenet.com, 1 page (Feb. 28, 1987 - Date of publication of application).
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	AA64	5,896,304	04/1999	Tiemann *et al.*			
	AB64	6,005,903	12/1999	Mendelovicz			
	AC64	5,834,979	11/1998	Yatsuka			
	AD64	6,798,351 B1	09/2004	Sorrells *et al.*			
	AE64	6,813,485 B2	11/2004	Sorrells *et al.*			
	AF64	5,410,270	04/1995	Rybicki *et al.*			
	AG64	6,509,777 B2	01/2003	Razavi *et al.*			
	AH64	5,982,329	11/1999	Pittman *et al.*			
	AI64	6,208,636 B1	03/2001	Tawil *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ64						Yes No
	AK64						Yes No
	AL64						Yes No
	AM64						Yes No

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	AN64	English-language Abstract of Japanese Patent Publication No. JP 7-169292, data supplied by ep.espacenet.com, 1 page (July 4, 1995 - Date of publication of application).
	AO64	English-language Abstract of Japanese Patent Publication No. JP 10-22804, data supplied by ep.espacenet.com, 1 page (January 23, 1998 - Date of publication of application).
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	AR64	

EXAMINER	/Sam Bhattacharya/	DATE CONSIDERED	06/21/2010

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.001000P	APPLICATION NO. 12/349,802
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA65	3,614,630	10/1971	Rorden			
	AB65	6,836,650 B2	12/2004	Sorrells *et al.*			
	AC65	5,844,868	12/1998	Takahashi *et al.*			
	AD65	6,385,439 B1	05/2002	Hellberg			
	AE65	6,741,139 B2	05/2004	Pleasant *et al.*			
	AF65	6,823,178 B2	11/2004	Pleasant *et al.*			
	AG65	6,850,742 B2	02/2005	Fayyaz			
	AH65	6,853,690 B1	02/2005	Sorrells *et al.*			
	AI65	4,789,837	12/1988	Ridgers			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ65						Yes No
	AK65						Yes No
	AL65						Yes No
	AM65						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN65	
	AO65	
	AP65	
	AQ65	
	AR65	

EXAMINER	/Sam Bhattacharya/	DATE CONSIDERED	06/21/2010

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA66	5,634,207	05/1997	Yamaji *et al.*			
	AB66	5,642,071	06/1997	Sevenhans *et al.*			
	AC66	6,211,718 B1	04/2001	Souetinov			
	AD66	6,212,369 B1	04/2001	Avasarala			
	AE66	6,308,058 B1	10/2001	Souetinov *et al.*			
	AF66	6,633,194 B2	10/2003	Arnborg *et al.*			
	AG66	2001/0036818 A1	11/2001	Dobrovolny			
	AH66	6,873,836 B1	03/2005	Sorrells *et al.*			
	AI66	6,879,817 B1	04/2005	Sorrells *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ66						Yes No
	AK66						Yes No
	AL66						Yes No
	AM66						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN66	
	AO66	
	AP66	
	AQ66	
	AR66	

EXAMINER	/Sam Bhattacharya/	DATE CONSIDERED	06/21/2010

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA67	6,057,714	05/2000	Andrys *et al.*			
	AB67	2003/0081781 A1	05/2003	Jensen *et al.*			
	AC67	5,994,689	11/1999	Charrier			
	AD67	6,512,544 B1	01/2003	Merrill *et al.*			
	AE67	6,628,328 B1	09/2003	Yokouchi *et al.*			
	AF67	6,801,253 B1	10/2004	Yonemoto *et al.*			
	AG67	3,737,778	06/1973	Van Gerwen *et al.*			
	AH67	4,286,283	08/1981	Clemens			
	AI67	4,241,451	12/1980	Maixner *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ67						Yes No
	AK67						Yes No
	AL67						Yes No
	AM67						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN67	
	AO67	
	AP67	
	AQ67	
	AR67	

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA68	5,014,130	05/1991	Heister *et al.*			
	AB68	5,390,215	02/1995	Anita *et al.*			
	AC68	5,805,460	09/1998	Greene *et al.*			
	AD68	6,882,194 B2	04/2005	Belot *et al.*			
	AE68	6,892,062 B2	05/2005	Lee *et al.*			
	AF68	6,917,796 B2	07/2005	Setty *et al.*			
	AG68	6,920,311 B2	07/2005	Rofougaran *et al.*			
	AH68	5,062,122	10/1991	Pham *et al.*			
	AI68	6,182,011 B1	01/2001	Ward			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ68						Yes No
	AK68						Yes No
	AL68						Yes No
	AM68						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN68	
	AO68	
	AP68	
	AQ68	
	AR68	

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA69	6,639,939 B1	10/2003	Naden *et al.*			
	AB69	5,787,125	07/1998	Mittel			
	AC69	5,878,088	03/1999	Knutson *et al.*			
	AD69	6,215,828	04/2001	Signell *et al.*			
	AE69	5,703,584	12/1997	Hill			
	AF69	5,887,001	03/1999	Russell			
	AG69	6,298,065 B1	10/2001	Dombkowski *et al.*			
	AH69	2002/0080728 A1	06/2002	Sugar *et al.*			
	AI69	2002/0163921 A1	11/2002	Ethridge *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ69						Yes No
	AK69						Yes No
	AL69						Yes No
	AM69						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN69	
	AO69	
	AP69	
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	AR69	

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA70	6,963,734 B2	11/2005	Sorrells *et al.*			
	AB70	6,005,506	12/1999	Bazarjani *et al.*			
	AC70	6,438,366 B1	08/2002	Lindfors *et al.*			
	AD70	5,196,806	03/1993	Ichihara			
	AE70	5,410,195	04/1995	Ichihara			
	AF70	6,404,823 B1	06/2002	Grange *et al.*			
	AG70	6,618,579 B1	09/2003	Smith *et al.*			
	AH70	2001/0015673 A1	08/2001	Yamashita *et al.*			
	AI70	2003/0045263 A1	03/2003	Wakayama *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ70						Yes No
	AK70						Yes No
	AL70						Yes No
	AM70						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN70	
	AO70	
	AP70	
	AQ70	
	AR70	

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA71	6,975,848 B2	12/2005	Rawlins *et al.*			
	AB71	6,404,758 B1	06/2002	Wang			
	AC71	6,909,739 B1	06/2005	Eerola *et al.*			
	AD71	6,910,015 B2	06/2005	Kawai			
	AE71	3,719,903	03/1973	Goodson			
	AF71	4,591,930	05/1986	Baumeister			
	AG71	7,006,805 B1	02/2006	Sorrells *et al.*			
	AH71	7,010,286 B2	03/2006	Sorrells *et al.*			
	AI71	7,010,559 B2	03/2006	Rawlins *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ71						Yes No
	AK71						Yes No
	AL71						Yes No
	AM71						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN71	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA72	5,131,014	07/1992	White			
	AB72	6,393,070 B1	05/2002	Reber			
	AC72	7,016,663 B2	03/2006	Sorrells *et al.*			
	AD72	3,694,754	09/1972	Baltzer			
	AE72	4,931,716	06/1990	Jovanovic *et al.*			
	AF72	3,617,898	11/1971	Janning, Jr.			
	AG72	3,764,921	10/1973	Huard			
	AH72	4,158,149	06/1979	Otofuji			
	AI72	4,380,828	04/1983	Moon			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ72						Yes No
	AK72						Yes No
	AL72						Yes No
	AM72						Yes No

NON PATENT LITERATURE DOCUMENTS

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	AN72	
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	AR72	

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA73	4,562,414	12/1985	Linder *et al.*			
	AB73	4,814,649	03/1989	Young			
	AC73	4,845,389	07/1989	Pyndiah *et al.*			
	AD73	5,172,019	12/1992	Naylor *et al.*			
	AE73	5,263,198	11/1993	Geddes *et al.*			
	AF73	5,551,076	08/1996	Bonn			
	AG73	5,633,610	05/1997	Maekawa *et al.*			
	AH73	7,027,786 B1	04/2006	Smith *et al.*			
	AI73	7,039,372 B1	05/2006	Sorrells *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ73						Yes No
	AK73						Yes No
	AL73						Yes No
	AM73						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN73	
	AO73	
	AP73	
	AQ73	
	AR73	

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA74	6,591,310 B1	07/2003	Johnson			
	AB74	6,963,626 B1	11/2005	Shaeffer *et al.*			
	AC74	4,811,422	03/1989	Kahn			
	AD74	5,825,257	10/1998	Klymyshyn *et al.*			
	AE74	5,986,600	11/1999	McEwan			
	AF74	6,865,399 B2	03/2005	Fujioka *et al.*			
	AG74	2006/0039449 A1	02/2006	Fontana *et al.*			
	AH74	5,847,594	12/1998	Mizuno			
	AI74	7,050,508 B2	05/2006	Sorrells *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ74						Yes No
	AK74						Yes No
	AL74						Yes No
	AM74						Yes No

NON PATENT LITERATURE DOCUMENTS

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	AN74	
	AO74	
	AP74	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA75	7,054,296 B1	05/2006	Sorrells *et al.*			
	AB75	7,065,162 B1	06/2006	Sorrells *et al.*			
	AC75	2003/0149579 A1	08/2003	Begemann *et al.*			
	AD75	5,063,387	11/1991	Mower			
	AE75	5,535,402	07/1996	Leibowitz *et al.*			
	AF75	6,512,785 B1	01/2003	Zhou *et al.*			
	AG75	6,567,483 B1	05/2003	Dent *et al.*			
	AH75	6,775,684 B1	08/2004	Toyoyama *et al.*			
	AI75	4,740,792	04/1988	Sagey *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ75						Yes No
	AK75						Yes No
	AL75						Yes No
	AM75						Yes No

NON PATENT LITERATURE DOCUMENTS

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	AN75	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA76	5,239,687	08/1993	Chen			
	AB76	5,552,789	09/1996	Schuermann			
	AC76	5,905,433	05/1999	Wortham			
	AD76	6,647,270 B1	11/2003	Himmelstein			
	AE76	6,034,566	03/2000	Ohe			
	AF76	6,313,700 B1	11/2001	Nishijima *et al.*			
	AG76	6,959,178 B2	10/2005	Macedo *et al.*			
	AH76	6,999,747 B2	02/2006	Su			
	AI76	2004/0125879 A1	07/2004	Jaussi *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ76						Yes No
	AK76						Yes No
	AL76						Yes No
	AM76						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN76	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA77	7,072,390 B1	07/2006	Sorrells *et al.*			
	AB77	7,072,427 B2	07/2006	Rawlins *et al.*			
	AC77	7,076,011 B2	07/2006	Cook *et al.*			
	AD77	7,082,171 B1	07/2006	Johnson *et al.*			
	AE77	7,085,335 B2	08/2006	Rawlins *et al.*			
	AF77	3,739,282	06/1973	Bruch *et al.*			
	AG77	4,439,787	03/1984	Mogi *et al.*			
	AH77	4,866,441	09/1989	Conway *et al.*			
	AI77	4,885,671	12/1989	Peil			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ77						Yes No
	AK77						Yes No
	AL77						Yes No
	AM77						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN77	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA78	5,164,985	11/1992	Nysen *et al.*			
	AB78	5,734,683	03/1998	Hulkko *et al.*			
	AC78	5,918,167	06/1999	Tiller *et al.*			
	AD78	6,445,726 B1	09/2002	Gharpurey			
	AE78	6,560,451 B1	05/2003	Somayajula			
	AF78	4,143,322	03/1979	Shimamura			
	AG78	2,530,824	11/1950	King			
	AH78	7,107,028 B2	09/2006	Sorrells *et al.*			
	AI78	7,110,435 B1	09/2006	Sorrells *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ78						Yes No
	AK78						Yes No
	AL78						Yes No
	AM78						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN78	
	AO78	
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	AQ78	
	AR78	

EXAMINER	/Sam Bhattacharya/	DATE CONSIDERED	06/21/2010

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.001000P	APPLICATION NO. 12/349,802
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA79	7,110,444 B1	09/2006	Sorrells *et al.*			
	AB79	6,973,476 B1	12/2005	Naden *et al.*			
	AC79	5,834,987	11/1998	Dent			
	AD79	RE37,138 E	04/2001	Dent			
	AE79	6,441,694 B1	08/2002	Turcotte *et al.*			
	AF79	6,892,057 B2	05/2005	Nilsson			
	AG79	6,741,650 B1	05/2004	Painchaud *et al.*			
	AH79	2002/0132642 A1	09/2002	Hines *et al.*			
	AI79	5,884,154	03/1999	Sano *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ79						Yes No
	AK79						Yes No
	AL79						Yes No
	AM79						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN79	
	AO79	
	AP79	
	AQ79	
	AR79	

EXAMINER /Sam Bhattacharya/	DATE CONSIDERED 06/21/2010

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA80	5,900,746	05/1999	Sheahan			
	AB80	6,246,695 B1	06/2001	Seazholtz *et al.*			
	AC80	6,597,240 B1	07/2003	Walburger *et al.*			
	AD80	7,190,941 B2	03/2007	Sorrells *et al.*			
	AE80	7,194,246 B2	03/2007	Sorrells *et al.*			
	AF80	7,209,725 B1	04/2007	Sorrells *et al.*			
	AG80	7,218,899 B2	05/2007	Sorrells *et al.*			
	AH80	7,218,907 B2	05/2007	Sorrells *et al.*			
	AI80	7,224,749 B2	05/2007	Sorrells *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ80						Yes No
	AK80						Yes No
	AL80						Yes No
	AM80						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN80	
	AO80	
	AP80	
	AQ80	
	AR80	

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA81	7,233,969 B2	06/2007	Rawlins *et al.*			
	AB81	7,236,754 B2	06/2007	Sorrells *et al.*			
	AC81	7,245,886 B2	07/2007	Sorrells *et al.*			
	AD81	7,194,044 B2	03/2007	Birkett *et al.*			
	AE81	7,212,581 B2	05/2007	Birkett *et al.*			
	AF81	4,485,347	11/1984	Hirasawa *et al.*			
	AG81	5,724,041	03/1998	Inoue *et al.*			
	AH81	2003/0193364 A1	10/2003	Liu *et al.*			
	AI81	4,771,265	09/1988	Okui *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ81						Yes No
	AK81						Yes No
	AL81						Yes No
	AM81						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN81	
	AO81	
	AP81	
	AQ81	
	AR81	

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA82	5,006,854	04/1991	White *et al.*			
	AB82	3,643,168	02/1972	Manicki			
	AC82	4,048,598	09/1977	Knight			
	AD82	4,145,659	03/1979	Wolfram			
	AE82	4,313,222	01/1982	Katthän			
	AF82	5,896,347	04/1999	Tomita *et al.*			
	AG82	6,259,293 B1	07/2001	Hayase *et al.*			
	AH82	7,272,164 B2	09/2007	Sorrells *et al.*			
	AI82	7,292,835 B2	11/2007	Sorrells *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ82						Yes No
	AK82						Yes No
	AL82						Yes No
	AM82						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN82	
	AO82	
	AP82	
	AQ82	
	AR82	

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA83	7,295,826 B1	11/2007	Cook *et al.*			
	AB83	6,112,061	08/2000	Rapeli			
	AC83	6,625,470 B1	09/2003	Fourtet *et al.*			
	AD83	6,813,320 B1	11/2004	Claxton *et al.*			
	AE83	2002/0021685 A1	02/2002	Sakusabe			
	AF83	2003/0078011 A1	04/2003	Cheng *et al.*			
	AG83	7,308,242 B2	12/2007	Sorrells *et al.*			
	AH83	7,321,640 B2	01/2008	Milne *et al.*			
	AI83	7,321,735 B1	01/2008	Smith *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ83						Yes No
	AK83						Yes No
	AL83						Yes No
	AM83						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN83	
	AO83	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA84	7,321,751 B2	01/2008	Sorrells *et al.*			
	AB84	2006/0002491 A1	01/2006	Darabi *et al.*			
	AC84	4,663,744	05/1987	Russell *et al.*			
	AD84	5,559,809	09/1996	Jeon *et al.*			
	AE84	6,038,265	03/2000	Pan *et al.*			
	AF84	6,876,846 B2	04/2005	Tamaki *et al.*			
	AG84	6,512,798 B1	01/2003	Akiyama *et al.*			
	AH84	6,072,996	06/2000	Smith			
	AI84	6,088,348	06/2000	Bell, III *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ84						Yes No
	AK84						Yes No
	AL84						Yes No
	AM84						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN84	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA85	6,198,941 B1	03/2001	Aho *et al.*			
	AB85	6,894,988 B1	05/2005	Zehavi			
	AC85	7,193,965 B1	03/2007	Nevo *et al.*			
	AD85	4,688,237	08/1987	Brault			
	AE85	5,461,646	10/1995	Anvari			
	AF85	5,483,245	01/1996	Ruinet			
	AG85	7,197,081 B2	03/2007	Saito			
	AH85	7,376,410 B2	05/2008	Sorrells *et al.*			
	AI85	7,379,515 B2	05/2008	Johnson *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ85						Yes No
	AK85						Yes No
	AL85						Yes No
	AM85						Yes No

NON PATENT LITERATURE DOCUMENTS

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	AN85	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA86	7,379,883 B2	05/2008	Sorrells			
	AB86	7,386,292 B2	06/2008	Sorrells *et al.*			
	AC86	7,389,100 B2	06/2008	Sorrells *et al.*			
	AD86	4,651,210	03/1987	Olson			
	AE86	5,659,372	08/1997	Patel *et al.*			
	AF86	6,097,762	08/2000	Suzuki *et al.*			
	AG86	5,512,946	04/1996	Murata *et al.*			
	AH86	3,809,821	05/1974	Melvin			
	AI86	6,275,542	08/2001	Katayama *et al.*			

FOREIGN PATENT DOCUMENTS

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	AJ86						Yes No
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	AL86						Yes No
	AM86						Yes No

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA87	2006/0209599 A1	09/2006	Kato *et al.*			
	AB87	5,339,395	08/1994	Pickett *et al.*			
	AC87	6,128,746	10/2000	Clark *et al.*			
	AD87	6,137,321	10/2000	Bazarjani			
	AE87	5,909,460	06/1999	Dent			
	AF87	6,546,061 B2	04/2003	Signell *et al.*			
	AG87	4,004,237	01/1977	Kratzer			
	AH87	4,363,976	12/1982	Minor			
	AI87	4,393,352	07/1983	Volpe *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ87						Yes No
	AK87						Yes No
	AL87						Yes No
	AM87						Yes No

NON PATENT LITERATURE DOCUMENTS

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	AN87	
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	AR87	

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA88	4,405,835	09/1983	Jansen *et al.*			
	AB88	4,463,320	07/1984	Dawson			
	AC88	4,596,046	06/1986	Richardson *et al.*			
	AD88	6,167,247	12/2000	Kannell *et al.*			
	AE88	6,223,061 B1	04/2001	Dacus *et al.*			
	AF88	6,366,765 B1	04/2002	Hongo *et al.*			
	AG88	6,731,146 B1	05/2004	Gallardo			
	AH88	6,738,609 B1	05/2004	Clifford			
	AI88	7,149,487 B2	12/2006	Yoshizawa			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ88						Yes No
	AK88						Yes No
	AL88						Yes No
	AM88						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN88	
	AO88	
	AP88	
	AQ88	
	AR88	

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA89	7,358,801 B2	04/2008	Perdoor *et al.*			
	AB89	5,781,600	07/1998	Reeve *et al.*			
	AC89	5,973,570	10/1999	Salvi *et al.*			
	AD89	6,690,741 B1	02/2004	Larrick, Jr. *et al.*			
	AE89	7,433,910 B2	10/2008	Rawlins *et al.*			
	AF89	7,454,453 B2	11/2008	Rawlins *et al.*			
	AG89	7,460,584 B2	12/2008	Parker *et al.*			
	AH89	4,173,164	11/1979	Adachi *et al.*			
	AI89	4,409,877	10/1983	Budelman			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ89						Yes No
	AK89						Yes No
	AL89						Yes No
	AM89						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN89	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA90	6,195,539	02/2001	Galal *et al.*			
	AB90	4,571,738	02/1986	Vance			
	AC90	5,982,810	11/1999	Nishimori			
	AD90	2002/0098823 A1	07/2002	Lindfors *et al.*			
	AE90	4,968,958	11/1990	Hoare			
	AF90	7,483,686 B2	01/2009	Sorrells *et al.*			
	AG90	7,496,342 B2	02/2009	Sorrells *et al.*			
	AH90	7,515,896 B1	04/2009	Sorrells *et al.*			
	AI90	7,529,522 B2	05/2009	Sorrells *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ90						Yes No
	AK90						Yes No
	AL90						Yes No
	AM90						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN90	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA91	7,539,474 B2	05/2009	Sorrells *et al.*			
	AB91	7,546,096 B2	06/2009	Sorrells *et al.*			
	AC91	7,554,508 B2	06/2009	Johnson *et al.*			
	AD91	6,192,225 B1	02/2001	Arpaia *et al.*			
	AE91	7,599,421 B2	10/2009	Sorrells *et al.*			
	AF91	5,757,864	05/1998	Petranovich *et al.*			
	AG91	5,559,468	09/1996	Gailus *et al.*			
	AH91	6,829,311 B1	12/2004	Riley			
	AI91	7,620,378 B2	11/2009	Sorrells *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ91						Yes No
	AK91						Yes No
	AL91						Yes No
	AM91						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN91	
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PATENT & TRADEMARK OFFICE

FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
1744.001000P	12/349,802
FIRST NAMED INVENTOR	
David F. SORRELLS	
FILING DATE	ART UNIT
January 7, 2009	2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1	2,057,613	10/1936	Gardner			
	AB1	2,241,078	05/1941	Vreeland			
	AC1	2,270,385	01/1942	Skillman			
	AD1	2,283,575	05/1942	Roberts			
	AE1	2,358,152	09/1944	Earp			
	AF1	2,410,350	10/1946	Labin *et al.*			
	AG1	2,451,430	10/1948	Barone			
	AH1	2,462,069	02/1949	Chatterjea *et al.*			
	AI1	2,462,181	02/1949	Grosselfinger			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ1	DE 42 37 692 C1	03/1994	DE			No
	AK1	EP 0 035 166 A1	09/1981	EP			No
	AL1	EP 0 193 899 B1	06/1990	EP			N/A
	AM1	EP 0 380 351 A2	08/1990	EP			N/A

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN1	Aghvami, H. *et al.*, "Land Mobile Satellites Using the Highly Elliptic Orbits- The UK T-SAT Mobile Payload," *Fourth International Conference on Satellite Systems for Mobile Communications and Navigation*, IEE, pp. 147-153 (October 17-19, 1988).
	AO1	Akers, N.P. *et al.*, "RF Sampling Gates: a Brief Review," *IEE Proceedings*, IEE, Vol. 133, Part A, No. 1, pp. 45-49 (January 1986).
	AP1	Al-Ahmad, H.A.M. *et al.*, "Doppler Frequency Correction for a Non-Geostationary Communications Satellite. Techniques for CERS and T-SAT," *Electronics Division Colloquium on Low Noise Oscillators and Synthesizers,* IEE, pp. 4/1-4/5 (January 23, 1986).
	AQ1	Ali, I. *et al.*, "Doppler Characterization for LEO Satellites," *IEEE Transactions on Communications*, IEEE, Vol. 46, No. 3, pp. 309-313 (March 1998).
	AR1	Allan, D.W., "Statistics of Atomic Frequency Standards," *Proceedings Of The IEEE Special Issue on Frequency Stability*, IEEE, pp. 221-230 (February 1966).

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.001000P	APPLICATION NO. 12/349,802
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA2	2,472,798	06/1949	Fredendall			
	AB2	2,497,859	02/1950	Boughtwood *et al.*			
	AC2	2,499,279	02/1950	Peterson			
	AD2	2,802,208	08/1957	Hobbs			
	AE2	2,985,875	05/1961	Grisdale *et al.*			
	AF2	3,023,309	02/1962	Foulkes			
	AG2	3,069,679	12/1962	Sweeney *et al.*			
	AH2	3,104,393	09/1963	Vogelman			
	AI2	3,114,106	12/1963	McManus			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ2	EP 0 380 351 A3	02/1991	EP			N/A
	AK2	EP 0 411 840 A2	02/1991	EP			N/A
	AL2	EP 0 411 840 A3	07/1991	EP			N/A
	AM2	EP 0 411 840 B1	10/1995	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN2	Allstot, D.J. *et al.*, "MOS Switched Capacitor Ladder Filters," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-13, No. 6, pp. 806-814 (December 1978).
	AO2	Allstot, D.J. and Black Jr. W.C., "Technological Design Considerations for Monolithic MOS Switched-Capacitor Filtering Systems," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 967-986 (August 1983).
	AP2	Alouini, M. *et al.*, "Channel Characterization and Modeling for Ka-Band Very Small Aperture Terminals," *Proceedings Of the IEEE*, IEEE, Vol. 85, No. 6, pp. 981-997 (June 1997).
	AQ2	Andreyev, G.A. and Ogarev, S.A., "Phase Distortions of Keyed Millimeter-Wave Signals in the Case of Propagation in a Turbulent Atmosphere," *Telecommunications and Radio Engineering*, Scripta Technica, Vol. 43, No. 12, pp. 87-90 (December 1988).
	AR2	Antonetti, A. *et al.*, "Optoelectronic Sampling in the Picosecond Range," *Optics Communications*, North-Holland Publishing Company, Vol. 21, No. 2, pp. 211-214 (May 1977).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA3	3,118,117	01/1964	King *et al.*			
	AB3	3,226,643	12/1965	McNair			
	AC3	3,258,694	06/1966	Shepherd			
	AD3	3,383,598	05/1968	Sanders			
	AE3	3,384,822	05/1968	Miyagi			
	AF3	3,454,718	07/1969	Perreault			
	AG3	3,523,291	08/1970	Pierret			
	AH3	3,548,342	12/1970	Maxey			
	AI3	3,555,428	01/1971	Perreault			

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	AJ3	EP 0 423 718 A2	04/1991	EP			N/A
	AK3	EP 0 423 718 A3	08/1992	EP			N/A
	AL3	EP 0 486 095 A1	05/1992	EP			N/A
	AM3	EP 0 486 095 B1	02/1997	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN3	Austin, J. *et al.*, "Doppler Correction of the Telecommunication Payload Oscillators in the UK T-SAT," *18th European Microwave Conference*, Microwave Exhibitions and Publishers Ltd., pp. 851-857 (September 12 - 15, 1988).
	AO3	Auston, D.H., "Picosecond optoelectronic switching and gating in silicon," *Applied Physics Letters*, American Institute of Physics, Vol. 26, No. 3, pp. 101-103 (February 1, 1975).
	AP3	Baher, H., "Transfer Functions for Switched-Capacitor and Wave Digital Filters," *IEEE Transactions on Circuits and Systems*, IEEE Circuits and Systems Society, Vol. CAS-33, No. 11, pp. 1138-1142 (November 1986).
	AQ3	Baines, R., "The DSP Bottleneck," *IEEE Communications Magazine*, IEEE Communications Society, pp. 46-54 (May 1995).
	AR3	Banjo, O.P. and Vilar, E., "Binary Error Probabilities on Earth-Space Links Subject to Scintillation Fading," *Electronics Letters*, IEE, Vol. 21, No. 7, pp. 296-297 (March 28, 1985).

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	AA4	3,617,892	11/1971	Hawley *et al.*			
	AB4	3,621,402	11/1971	Gardner			
	AC4	3,623,160	11/1971	Giles *et al.*			
	AD4	3,626,417	12/1971	Gilbert			
	AE4	3,629,696	12/1971	Bartelink			
	AF4	3,662,268	05/1972	Gans *et al.*			
	AG4	3,689,841	09/1972	Bello *et al.*			
	AH4	3,714,577	01/1973	Hayes			
	AI4	3,717,844	02/1973	Barret *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ4	EP 0 512 748 A2	11/1992	EP			N/A
	AK4	EP 0 512 748 A3	07/1993	EP			N/A
	AL4	EP 0 512 748 B1	11/1998	EP			N/A
	AM4	EP 0 548 542 A1	06/1993	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN4	Banjo, O.P. and Vilar, E., "The Dependence of Slant Path Amplitude Scintillations on Various Meteorological Parameters," *Fifth International Conference on Antennas and Propagation (ICAP 87) Part 2: Propagation*, IEE, pp. 277-280 (March 30 - April 2, 1987).
	AO4	Banjo, O.P. and Vilar, E. "Measurement and Modeling of Amplitude Scintillations on Low-Elevation Earth-Space Paths and Impact on Communication Systems," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. COM-34, No. 8, pp. 774-780 (August 1986).
	AP4	Banjo, O.P. *et al.*, "Tropospheric Amplitude Spectra Due to Absorption and Scattering in Earth-Space Paths," *Fourth International Conference on Antennas and Propagation (ICAP 85)*, IEE, pp. 77-82 (April 16-19, 1985).
	AQ4	Basili,P. *et al.*, "Case Study of Intense Scintillation Events on the OTS Path," *IEEE Transactions on Antennas and Propagation*, IEEE, Vol. 38, No. 1, pp. 107-113 (January 1990).
	AR4	Basili, P. *et al.*, "Observation of High C^2 and Turbulent Path Length on OTS Space-Earth Link," *Electronics Letters*, IEE, Vol. 24, No. 17, pp. 1114-1116 (August 18, 1988).

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	AA5	3,735,048	05/1973	Tomsa *et al.*			
	AB5	3,806,811	04/1974	Thompson			
	AC5	3,868,601	02/1975	MacAfee			
	AD5	3,949,300	04/1976	Sadler			
	AE5	3,967,202	06/1976	Batz			
	AF5	3,980,945	09/1976	Bickford			
	AG5	3,987,280	10/1976	Bauer			
	AH5	3,991,277	11/1976	Hirata			
	AI5	4,003,002	01/1977	Snijders *et al.*			

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	AJ5	EP 0 632 288 A2	01/1995	EP			N/A
	AK5	EP 0 632 288 A3	07/1996	EP			N/A
	AL5	EP 0 696 854 A1	02/1996	EP			N/A
	AM5	EP 0 782 275 A2	07/1997	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN5	Blakey, J.R. *et al.*, "Measurement of Atmospheric Millimetre-Wave Phase Scintillations in an Absorption Region," *Electronics Letters*, IEE, Vol. 21, No. 11, pp. 486-487 (May 23, 1985).
	AO5	Burgueño, A. *et al.*, "Influence of rain gauge integration time on the rain rate statistics used in microwave communications," *annales des tèlècommunications*, International Union of Radio Science, pp. 522-527 (September/October 1988).
	AP5	Burgueño, A. *et al.*, "Long-Term Joint Statistical Analysis of Duration and Intensity of Rainfall Rate with Application to Microwave Communications," *Fifth International Conference on Antennas and Propagation (ICAP 87) Part 2: Propagation*, IEE, pp. 198-201 (March 30 - April 2, 1987).
	AQ5	Burgueño, A. *et al.*, "Long Term Statistics of Precipitation Rate Return Periods in the Context of Microwave Communications," *Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation*, IEE, pp. 297-301 (April 4-7, 1989).
	AR5	Burgueño, A. *et al.*, "Spectral Analysis of 49 Years of Rainfall Rate and Relation to Fade Dynamics," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 38, No. 9, pp. 1359-1366 (September 1990).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA6	4,013,966	03/1977	Campbell			
	AB6	4,019,140	04/1977	Swerdlow			
	AC6	4,035,732	07/1977	Lohrmann			
	AD6	4,047,121	09/1977	Campbell			
	AE6	4,066,841	01/1978	Young			
	AF6	4,066,919	01/1978	Huntington			
	AG6	4,081,748	03/1978	Batz			
	AH6	4,130,765	12/1978	Arakelian *et al.*			
	AI6	4,130,806	12/1978	Van Gerwen *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ6	EP 0 785 635 A1	07/1997	EP			No
	AK6	EP 0 795 978 A2	09/1997	EP			N/A
	AL6	EP 0 837 565 A1	04/1998	EP			N/A
	AM6	EP 0 862 274 A1	09/1998	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN6	Catalan, C. and Vilar, E., "Approach for satellite slant path remote sensing," *Electronics Letters,* IEE, Vol. 34, No. 12, pp. 1238-1240 (June 11, 1998).
	AO6	Chan, P. et al., "A Highly Linear 1-GHz CMOS Downconversion Mixer," *European Solid State Circuits Conference*, IEEE Communication Society, pp. 210-213 (September 22-24, 1993).
	AP6	Copy of Declaration of Michael J. Bultman filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 2 pages.
	AQ6	Copy of Declaration of Robert W. Cook filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 2 pages.
	AR6	Copy of Declaration of Alex Holtz filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 3 pages.

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	AA7	4,142,155	02/1979	Adachi			
	AB7	4,170,764	10/1979	Salz *et al.*			
	AC7	4,204,171	05/1980	Sutphin, Jr.			
	AD7	4,210,872	07/1980	Gregorian			
	AE7	4,245,355	01/1981	Pascoe *et al.*			
	AF7	4,253,066	02/1981	Fisher *et al.*			
	AG7	4,253,069	02/1981	Nossek			
	AH7	4,308,614	12/1981	Fisher *et al.*			
	AI7	4,320,361	03/1982	Kikkert			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ7	EP 0 874 499 A2	10/1998	EP			N/A
	AK7	FR 2 743 231 A1	07/1997	FR			No
	AL7	GB 2 161 344 A	01/1986	GB			N/A
	AM7	GB 2 215 945 A	09/1989	GB			N/A

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN7	Copy of Declaration of Richard C. Looke filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 2 pages.
	AO7	Copy of Declaration of Charley D. Moses, Jr. filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 2 pages.
	AP7	Copy of Declaration of Jeffrey L. Parker and David F. Sorrells, with attachment Exhibit 1, filed in patent application Ser. No. 09/176,022, which is directed to related subject matter, 130 pages.
	AQ7	Dewey, R.J. and Collier, C.J., "Multi-Mode Radio Receiver," *Electronics Division Colloquium on Digitally Implemented Radios,* IEE, pp. 3/1-3/5 (October 18, 1985).
	AR7	DIALOG File 347 (JAPIO) English Language Patent Abstract for JP 2-276351, 1 page (November 13, 1990 - Date of publication of application).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA8	4,320,536	03/1982	Dietrich			
	AB8	4,346,477	08/1982	Gordy			
	AC8	4,355,401	10/1982	Ikoma *et al.*			
	AD8	4,356,558	10/1982	Owen *et al.*			
	AE8	4,360,867	11/1982	Gonda			
	AF8	4,363,132	12/1982	Collin			
	AG8	4,365,217	12/1982	Berger *et al.*			
	AH8	4,370,572	01/1983	Cosand *et al.*			
	AI8	4,389,579	06/1983	Stein			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ8	JP 2-39632	02/1990	JP			No
	AK8	JP 2-131629	05/1990	JP			No
	AL8	JP 2-276351	11/1990	JP			No
	AM8	WO 80/01633 A1	08/1980	PCT			N/A

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN8	DIALOG File 347 (JAPIO) English Language Patent Abstract for JP 2-131629, 1 page (May 21, 1990 - Date of publication of application).
	AO8	DIALOG File 347 (JAPIO) English Language Patent Abstract for JP 2-39632, 1 page (February 8, 1990 - Date of publication of application).
	AP8	DIALOG File 348 (European Patents) English Language Patent Abstract for EP 0 785 635 A1, 3 pages (December 26, 1996 - Date of publication of application).
	AQ8	DIALOG File 348 (European Patents) English Language Patent Abstract for EP 35166 A1, 2 pages (February 18, 1981 - Date of publication of application).
	AR8	"DSO takes sampling rate to 1 Ghz," *Electronic Engineering*, Morgan Grampian Publishers, Vol. 59, No. 723, pp. 77 and 79 (March 1987).

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	AA9	4,392,255	07/1983	Del Giudice			
	AB9	4,430,629	02/1984	Betzl *et al.*			
	AC9	4,446,438	05/1984	Chang *et al.*			
	AD9	4,456,990	06/1984	Fisher *et al.*			
	AE9	4,472,785	09/1984	Kasuga			
	AF9	4,479,226	10/1984	Prabhu *et al.*			
	AG9	4,481,490	11/1984	Huntley			
	AH9	4,481,642	11/1984	Hanson			
	AI9	4,485,488	11/1984	Houdart			

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	AJ9	WO 94/05087 A1	03/1994	PCT			N/A
	AK9	WO 96/02977 A1	02/1996	PCT			N/A
	AL9	WO 96/08078 A1	03/1996	PCT			N/A
	AM9	WO 96/39750 A1	12/1996	PCT			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN9	Erdi, G. and Henneuse, P.R., "A Precision FET-Less Sample-and-Hold with High Charge-to-Droop Current Ratio," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-13, No. 6, pp. 864-873 (December 1978).
	AO9	Faulkner, N.D. and Vilar, E., "Subharmonic Sampling for the Measurement of Short Term Stability of Microwave Oscillators," *IEEE Transactions on Instrumentation and Measurement*, IEEE, Vol. IM-32, No. 1, pp. 208-213 (March 1983).
	AP9	Faulkner, N.D. *et al.*, "Sub-Harmonic Sampling for the Accurate Measurement of Frequency Stability of Microwave Oscillators," *CPEM 82 Digest: Conference on Precision Electromagnetic Measurements*, IEEE, pp. M-10 and M-11 (1982).
	AQ9	Faulkner, N.D. and Vilar, E., "Time Domain Analysis of Frequency Stability Using Non-Zero Dead-Time Counter Techniques," *CPEM 84 Digest Conference on Precision Electromagnetic Measurements*, IEEE, pp. 81-82 (1984).
	AR9	Filip, M. and Vilar, E., "Optimum Utilization of the Channel Capacity of a Satellite Link in the Presence of Amplitude Scintillations and Rain Attenuation," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 38, No. 11, pp. 1958-1965 (November 1990).

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	AA10	4,504,803	03/1985	Lee *et al.*			
	AB10	4,517,519	05/1985	Mukaiyama			
	AC10	4,517,520	05/1985	Ogawa			
	AD10	4,518,935	05/1985	van Roermund			
	AE10	4,521,892	06/1985	Vance *et al.*			
	AF10	4,563,773	07/1986	Dixon, Jr. *et al.*			
	AG10	4,577,157	03/1986	Reed			
	AH10	4,583,239	04/1986	Vance			
	AI10	4,591,736	05/1986	Hirao *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ10	WO 97/38490 A1	10/1997	PCT			N/A
	AK10	WO 98/00953 A1	01/1998	PCT			N/A
	AL10	WO 98/24201 A1	06/1998	PCT			N/A
	AM10	EP 0 099 265 A1	01/1984	EP			N/A

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN10	Fukahori, K., "A CMOS Narrow-Band Signaling Filter with Q Reduction," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-19, No. 6, pp. 926-932 (December 1984).
	AO10	Fukuchi, H. and Otsu, Y., "Available time statistics of rain attenuation on earth-space path," *IEE Proceedings-H: Microwaves, Antennas and Propagation*, IEE, Vol. 135, Pt. H, No. 6, pp. 387-390 (December 1988).
	AP10	Gibbins, C.J. and Chadha, R., "Millimetre-wave propagation through hydrocarbon flame," *IEE Proceedings*, IEE, Vol. 134, Pt. H, No.2 , pp. 169-173 (April 1987).
	AQ10	Gilchrist, B. *et al.*, "Sampling hikes performance of frequency synthesizers," *Microwaves & RF*, Hayden Publishing, Vol. 23, No. 1, pp. 93-94 and 110 (January 1984).
	AR10	Gossard, E.E., "Clear weather meteorological effects on propagation at frequencies above 1 Ghz," *Radio Science*, American Geophysical Union, Vol. 16, No. 5, pp. 589-608 (September - October 1981).

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	AB11	4,603,300	07/1986	Welles, II *et al.*			
	AC11	4,612,464	09/1986	Ishikawa *et al.*			
	AD11	4,612,518	09/1986	Gans *et al.*			
	AE11	4,616,191	10/1986	Galani *et al.*			
	AF11	4,621,217	11/1986	Saxe *et al.*			
	AG11	4,628,517	12/1986	Schwarz *et al.*			
	AH11	4,634,998	01/1987	Crawford			
	AI11	4,648,021	03/1987	Alberkrack			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ11	EP 0 560 228 A1	09/1993	EP			N/A
	AK11	FR 2 245 130	04/1975	FR			Yes (See AP50)
	AL11	DE 35 41 031 A1	05/1986	DE			Yes (See AR50)
	AM11	EP 0 732 803 A1	09/1996	EP			Yes (See AN51)

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN11	Gregorian, R. *et al.*, "Switched-Capacitor Circuit Design," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 941-966 (August 1983).
	AO11	Groshong *et al.*, "Undersampling Techniques Simplify Digital Radio," *Electronic Design*, Penton Publishing, pp. 67-68, 70, 73-75 and 78 (May 23, 1991).
	AP11	Grove, W.M., "Sampling for Oscilloscopes and Other RF Systems: Dc through X-Band," *IEEE Transactions on Microwave Theory and Techniques*, IEEE, pp. 629-635 (December 1966).
	AQ11	Haddon, J. *et al.*, "Measurement of Microwave Scintillations on a Satellite Down-Link at X-Band," *Antennas and Propagation*, IEE, pp. 113-117 (1981).
	AR11	Haddon, J. and Vilar, E., "Scattering Induced Microwave Scintillations from Clear Air and Rain on Earth Space Paths and the Influence of Antenna Aperture," *IEEE Transactions on Antennas and Propagation*, IEEE, Vol. AP-34, No. 5, pp. 646-657 (May 1986).

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	FIRST NAMED INVENTOR David F. SORRELLS	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA12	4,651,034	03/1987	Sato			
	AB12	4,675,882	06/1987	Lillie *et al.*			
	AC12	4,688,253	08/1987	Gumm			
	AD12	4,716,376	12/1987	Daudelin			
	AE12	4,716,388	12/1987	Jacobs			
	AF12	4,718,113	01/1988	Rother *et al.*			
	AG12	4,726,041	02/1988	Prohaska *et al.*			
	AH12	4,733,403	03/1988	Simone			
	AI12	4,734,591	03/1988	Ichitsubo			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ12	DE 197 35 798 C1	07/1998	DE			Yes (See AP51)
	AK12	WO 98/40968 A2&A3	09/1998	PCT			N/A
	AL12	EP 0 529 836 A1	03/1993	EP			N/A
	AM12	EP 0 795 955 A2&A3	09/1997	EP			N/A

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN12	Hafdallah, H. *et al.*, "2-4 Ghz MESFET Sampler," *Electronics Letters*, IEE, Vol. 24, No. 3, pp. 151-153 (February 4, 1988).
	AO12	Herben, M.H.A.J., "Amplitude and Phase Scintillation Measurements on 8-2 km Line-Of-Sight Path at 30 Ghz," *Electronics Letters*, IEE, Vol. 18, No. 7, pp. 287-289 (April 1, 1982).
	AP12	Hewitt, A. *et al.*, "An 18 Ghz Wideband LOS Multipath Experiment," *International Conference on Measurements for Telecommunication Transmission Systems - MTTS 85*, IEE, pp. 112-116 (November 27-28, 1985)
	AQ12	Hewitt, A. *et al.*, "An Autoregressive Approach to the Identification of Multipath Ray Parameters from Field Measurements," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 37, No. 11, pp. 1136-1143 (November 1989).
	AR12	Hewitt, A. and Vilar, E., "Selective fading on LOS Microwave Links: Classical and Spread-Spectrum Measurement Techniques," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 36, No. 7, pp. 789-796 (July 1988).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA13	4,737,969	04/1988	Steel *et al.*			
	AB13	4,743,858	05/1988	Everard			
	AC13	4,745,463	05/1988	Lu			
	AD13	4,751,468	06/1988	Agoston			
	AE13	4,757,538	07/1988	Zink			
	AF13	4,768,187	08/1988	Marshall			
	AG13	4,769,612	09/1988	Tamakoshi *et al.*			
	AH13	4,785,463	11/1988	Janc *et al.*			
	AI13	4,791,584	12/1988	Greivenkamp, Jr.			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ13	EP 0 817 369 A2&A3	01/1998	EP			N/A
	AK13	WO 91/18445 A1	11/1991	PCT			N/A
	AL13	WO 99/23755 A1	05/1999	PCT			N/A
	AM13	JP 56-114451	09/1981	JP			No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN13	Hospitalier, E., "Instruments for Recording and Observing Rapidly Varying Phenomena," *Science Abstracts*, IEE, Vol. VII, pp. 22-23 (1904).
	AO13	Howard, I.M. and Swansson, N.S., "Demodulating High Frequency Resonance Signals for Bearing Fault Detection," *The Institution of Engineers Australia Vibration and Noise Conference*, Institution of Engineers, Australia, pp. 115-121 (September 18-20, 1990).
	AP13	Hu, X., *A Switched-Current Sample-and-Hold Amplifier for FM Demodulation*, Thesis for Master of Applied Science, Dept. of Electrical and Computer Engineering, University of Toronto, UMI Dissertation Services, pp. 1-64 (1995).
	AQ13	Hung, H-L. A. *et al.*, "Characterization of Microwave Integrated Circuits Using An Optical Phase-Locking and Sampling System," *IEEE MTT-S Digest*, IEEE, pp. 507-510 (1991).
	AR13	Hurst, P.J., "Shifting the Frequency Response of Switched-Capacitor Filters by Nonuniform Sampling," *IEEE Transactions on Circuits and Systems*, IEEE Circuits and Systems Society, Vol. 38, No. 1, pp. 12-19 (January 1991).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA14	4,801,823	01/1989	Yokoyama			
	AB14	4,806,790	02/1989	Sone			
	AC14	4,810,904	03/1989	Crawford			
	AD14	4,810,976	03/1989	Cowley *et al.*			
	AE14	4,811,362	03/1989	Yester, Jr. *et al.*			
	AF14	4,819,252	04/1989	Christopher			
	AG14	4,833,445	05/1989	Buchele			
	AH14	4,862,121	08/1989	Hochschild *et al.*			
	AI14	4,868,654	09/1989	Juri *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ14	JP 8-32556	02/1996	JP			No
	AK14	JP 8-139524	05/1996	JP			No
	AL14	JP 59-144249	08/1984	JP			No
	AM14	JP 63-54002	03/1988	JP			No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN14	Itakura, T., "Effects of the sampling pulse width on the frequency characteristics of a sample-and-hold circuit," *IEE Proceedings Circuits, Devices and Systems,* IEE, Vol. 141, No. 4, pp. 328-336 (August 1994).
	AO14	Janssen, J.M.L., "An Experimental 'Stroboscopic' Oscilloscope for Frequencies up to about 50 Mc/s: I. Fundamentals," *Philips Technical Review,* Philips Research Laboratories, Vol. 12, No. 2, pp. 52-59 (August 1950).
	AP14	Janssen, J.M.L. and Michels, A.J., "An Experimental 'Stroboscopic' Oscilloscope for Frequencies up to about 50 Mc/s: II. Electrical Build-Up," *Philips Technical Review*, Philips Research Laboratories, Vol. 12, No. 3, pp. 73-82 (September 1950).
	AQ14	Jondral, V.F. *et al.*, "Doppler Profiles for Communication Satellites," *Frequenz*, Herausberger, pp. 111-116 (May-June 1996).
	AR14	Kaleh, G.K., "A Frequency Diversity Spread Spectrum System for Communication in the Presence of In-band Interference," *1995 IEEE Globecom*, IEEE Communications Society, pp. 66-70 (1995).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA15	4,870,659	09/1989	Oishi *et al.*			
	AB15	4,871,987	10/1989	Kawase			
	AC15	4,885,587	12/1989	Wiegand *et al.*			
	AD15	4,885,756	12/1989	Fontanes *et al.*			
	AE15	4,888,557	12/1989	Puckette, IV *et al.*			
	AF15	4,890,302	12/1989	Muilwijk			
	AG15	4,893,316	01/1990	Janc *et al.*			
	AH15	4,893,341	01/1990	Gehring			
	AI15	4,894,766	01/1990	De Agro			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ15	JP 6-237276	08/1994	JP			No
	AK15	JP 8-23359	01/1996	JP			No
	AL15	JP 47-2314	02/1972	JP			Yes (See AP53)
	AM15	JP 58-7903	01/1983	JP			Yes (See AQ53)

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN15	Karasawa, Y. *et al.*, "A New Prediction Method for Tropospheric Scintillation on Earth-Space Paths," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 36, No. 11, pp. 1608-1614 (November 1988).
	AO15	Kirsten, J. and Fleming, J., "Undersampling reduces data-acquisition costs for select applications," *EDN*, Cahners Publishing, Vol. 35, No. 13, pp. 217-222, 224, 226-228 (June 21, 1990).
	AP15	Lam, W.K. *et al.*, "Measurement of the Phase Noise Characteristics of an Unlocked Communications Channel Identifier," *Proceedings Of the 1993 IEEE International Frequency Control Symposium*, IEEE, pp. 283-288 (June 2-4, 1993).
	AQ15	Lam, W.K. *et al.*, "Wideband sounding of 11.6 Ghz transhorizon channel," *Electronics Letters*, IEE, Vol. 30, No. 9, pp. 738-739 (April 28, 1994).
	AR15	Larkin, K.G., "Efficient demodulator for bandpass sampled AM signals," *Electronics Letters*, IEE, Vol. 32, No. 2, pp. 101-102 (January 18, 1996).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA16	4,896,152	01/1990	Tiemann			
	AB16	4,902,979	02/1990	Puckette, IV			
	AC16	4,908,579	03/1990	Tawfik *et al.*			
	AD16	4,910,752	03/1990	Yester, Jr. *et al.*			
	AE16	4,914,405	04/1990	Wells			
	AF16	4,920,510	04/1990	Senderowicz *et al.*			
	AG16	4,922,452	05/1990	Larsen *et al.*			
	AH16	4,931,921	06/1990	Anderson			
	AI16	4,944,025	07/1990	Gehring *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ16	JP 58-133004	08/1983	JP			No
	AK16	JP 60-58705	04/1985	JP			No
	AL16	JP 4-123614	04/1992	JP			No
	AM16	JP 4-127601	04/1992	JP			No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN16	Lau, W.H. *et al.*, "Analysis of the Time Variant Structure of Microwave Line-of-sight Multipath Phenomena," *IEEE Global Telecommunications Conference & Exhibition*, IEEE, pp. 1707-1711 (November 28 - December 1, 1988).
	AO16	Lau, W.H. *et al.*, "Improved Prony Algorithm to Identify Multipath Components," *Electronics Letters*, IEE, Vol. 23, No. 20, pp. 1059-1060 (September 24, 1987).
	AP16	Lesage, P. and Audoin, C., "Effect of Dead-Time on the Estimation of the Two-Sample Variance," *IEEE Transactions on Instrumentation and Measurement*, IEEE Instrumentation and Measurement Society, Vol. IM-28, No. 1, pp. 6-10 (March 1979).
	AQ16	Liechti, C.A., "Performance of Dual-gate GaAs MESFET's as Gain-Controlled Low-Noise Amplifiers and High-Speed Modulators," *IEEE Transactions on Microwave Theory and Techniques*, IEEE Microwave Theory and Techniques Society, Vol. MTT-23, No. 6, pp. 461-469 (June 1975).
	AR16	Linnenbrink, T.E. *et al.*, "A One Gigasample Per Second Transient Recorder," *IEEE Transactions on Nuclear Science*, IEEE Nuclear and Plasma Sciences Society, Vol. NS-26, No. 4, pp. 4443-4449 (August 1979).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA17	4,955,079	09/1990	Connerney *et al.*			
	AB17	4,965,467	10/1990	Bilterijst			
	AC17	4,967,160	10/1990	Quievy *et al.*			
	AD17	4,970,703	11/1990	Hariharan *et al.*			
	AE17	4,982,353	01/1991	Jacob *et al.*			
	AF17	4,984,077	01/1991	Uchida			
	AG17	4,995,055	02/1991	Weinberger *et al.*			
	AH17	5,003,621	03/1991	Gailus			
	AI17	5,005,169	04/1991	Bronder *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ17	JP 5-175730	07/1993	JP			No
	AK17	JP 5-175734	07/1993	JP			No
	AL17	JP 7-154344	06/1995	JP			No
	AM17	JP 7-307620	11/1995	JP			No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN17	Liou, M.L., "A Tutorial on Computer-Aided Analysis of Switched-Capacitor Circuits," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 987-1005 (August 1983).
	AO17	Lo, P. *et al.*, "Coherent Automatic Gain Control," *IEE Colloquium on Phase Locked Techniques*, IEE, pp. 2/1-2/6 (March 26, 1980).
	AP17	Lo, P. *et al.*, "Computation of Rain Induced Scintillations on Satellite Down-Links at Microwave Frequencies," *Third International Conference on Antennas and Propagation (ICAP 83)*, pp. 127-131 (April 12-15, 1983).
	AQ17	Lo, P.S.L.O. *et al.*, "Observations of Amplitude Scintillations on a Low-Elevation Earth-Space Path," *Electronics Letters*, IEE, Vol. 20, No. 7, pp. 307-308 (March 29, 1984).
	AR17	Madani, K. and Aithison, C.S., "A 20 Ghz Microwave Sampler," *IEEE Transactions on Microwave Theory and Techniques*, IEEE Microwave Theory and Techniques Society, Vol. 40, No. 10, pp. 1960-1963 (October 1992).

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	AA18	5,006,810	04/1991	Popescu			
	AB18	5,010,585	04/1991	Garcia			
	AC18	5,014,304	05/1991	Nicollini *et al.*			
	AD18	5,015,963	05/1991	Sutton			
	AE18	5,017,924	05/1991	Guiberteau *et al.*			
	AF18	5,020,149	05/1991	Hemmie			
	AG18	5,020,154	05/1991	Zierhut			
	AH18	5,052,050	09/1991	Collier *et al.*			
	AI18	5,065,409	11/1991	Hughes *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ18	JP 55-66057	05/1980	JP			No
	AK18	JP 63-65587	03/1988	JP			No
	AL18	JP 63-153691	06/1988	JP			No
	AM18	EP 0 276 130 A2&A3	07/1988	EP			N/A

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN18	Marsland, R.A. *et al.*, "130 Ghz GaAs monolithic integrated circuit sampling head," *Appl. Phys. Lett.*, American Institute of Physics, Vol. 55, No. 6, pp. 592-594 (August 7, 1989).
	AO18	Martin, K. and Sedra, A.S., "Switched-Capacitor Building Blocks for Adaptive Systems," *IEEE Transactions on Circuits and Systems*, IEEE Circuits and Systems Society, Vol. CAS-28, No. 6, pp. 576-584 (June 1981).
	AP18	Marzano, F.S. and d'Auria, G., "Model-based Prediction of Amplitude Scintillation variance due to Clear-Air Tropospheric Turbulence on Earth-Satellite Microwave Links," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 46, No. 10, pp. 1506-1518 (October 1998).
	AQ18	Matricciani, E., "Prediction of fade durations due to rain in satellite communication systems," *Radio Science*, American Geophysical Union, Vol. 32, No. 3, pp. 935-941 (May-June 1997).
	AR18	McQueen, J.G., "The Monitoring of High-Speed Waveforms," *Electronic Engineering*, Morgan Brothers Limited, Vol. XXIV, No. 296, pp. 436-441 (October 1952).

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	AA19	5,083,050	01/1992	Vasile			
	AB19	5,091,921	02/1992	Minami			
	AC19	5,095,533	03/1992	Loper *et al.*			
	AD19	5,095,536	03/1992	Loper			
	AE19	5,111,152	05/1992	Makino			
	AF19	5,113,094	05/1992	Grace *et al.*			
	AG19	5,113,129	05/1992	Hughes			
	AH19	5,122,765	06/1992	Pataut			
	AI19	5,124,592	06/1992	Hagino			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ19	WO 95/01006 A1	01/1995	PCT			N/A
	AK19	WO 97/08839 A2&A3	03/1997	PCT			N/A
	AL19	EP 0 254 844 A2	02/1988	EP			N/A
	AM19	EP 0 632 577 A1	01/1995	EP			N/A

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN19	Merkelo, J. and Hall, R.D., "Broad-Band Thin-Film Signal Sampler," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-7, No. 1, pp. 50-54 (February 1972).
	AO19	Merlo, U. *et al.*, "Amplitude Scintillation Cycles in a Sirio Satellite-Earth Link," *Electronics Letters*, IEE, Vol. 21, No. 23, pp. 1094-1096 (November 7, 1985).
	AP19	Morris, D., "Radio-holographic reflector measurement of the 30-m millimeter radio telescope at 22 Ghz with a cosmic signal source," *Astronomy and Astrophysics*, Springer-Verlag, Vol. 203, No. 2, pp. 399-406 (September (II) 1988).
	AQ19	Moulsley, T.J. *et al.*, "The efficient acquisition and processing of propagation statistics," *Journal of the Institution of Electronic and Radio Engineers*, IERE, Vol. 55, No. 3, pp. 97-103 (March 1985).
	AR19	Ndzi, D. *et al.*, "Wide-Band Statistical Characterization of an Over-the-Sea Experimental Transhorizon Link," *IEE Colloquium on Radio Communications at Microwave and Millimetre Wave Frequencies*, IEE, pp. 1/1-1/6 (December 16, 1996).

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	AA20	5,136,267	08/1992	Cabot			
	AB20	5,140,705	08/1992	Kosuga			
	AC20	5,150,124	09/1992	Moore *et al.*			
	AD20	5,151,661	09/1992	Caldwell *et al.*			
	AE20	5,159,710	10/1992	Cusdin			
	AF20	5,170,414	12/1992	Silvian			
	AG20	5,172,070	12/1992	Hiraiwa *et al.*			
	AH20	5,191,459	03/1993	Thompson *et al.*			
	AI20	5,204,642	04/1993	Ashgar *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ20	JP 60-130203	07/1985	JP			Yes (See AO56)
	AK20	DE 196 27 640 A1	01/1997	DE			No
	AL20	EP 0 087 336 A1	08/1983	EP			No
	AM20	EP 0 087 336 B1	07/1986	EP			No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN20	Ndzi, D. *et al.*, "Wideband Statistics of Signal Levels and Doppler Spread on an Over-The-Sea Transhorizon Link," *IEE Colloquium on Propagation Characteristics and Related System Techniques for Beyond Line-of-Sight Radio*, IEE, pp. 9/1-9/6 (November 24, 1997).
	AO20	"New zero IF chipset from Philips," *Electronic Engineering*, United News & Media, Vol. 67, No. 825, p. 10 (September 1995).
	AP20	Ohara, H. *et al.*, "First monolithic PCM filter cuts cost of telecomm systems," *Electronic Design*, Hayden Publishing Company, Vol. 27, No. 8, pp. 130-135 (April 12, 1979).
	AQ20	Oppenheim, A.V. *et al.*, *Signals and Systems*, Prentice-Hall, pp. 527-531 and 561-562 (1983).
	AR20	Ortgies, G., "Experimental Parameters Affecting Amplitude Scintillation Measurements on Satellite Links," *Electronics Letters*, IEE, Vol. 21, No. 17, pp. 771-772 (August 15, 1985).

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.001000P	APPLICATION NO. 12/349,802
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA21	5,212,827	05/1993	Meszko *et al.*			
	AB21	5,214,787	05/1993	Karkota, Jr.			
	AC21	5,220,583	06/1993	Solomon			
	AD21	5,220,680	06/1993	Lee			
	AE21	5,222,144	06/1993	Whikehart			
	AF21	5,230,097	07/1993	Currie *et al.*			
	AG21	5,239,686	08/1993	Downey			
	AH21	5,241,561	08/1993	Barnard			
	AI21	5,249,203	09/1993	Loper			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ21	EP 0 789 449 A2 & A3	08/1997	EP			N/A
	AK21	FR 2 669 787 A1	05/1992	FR			No
	AL21	GB 2 324 919 A	11/1998	GB			N/A
	AM21	JP 61-30821	02/1986	JP			No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN21	Pärssinen et al., "A 2-GHz Subharmonic Sampler for Signal Downconversion," *IEEE Transactions on Microwave Theory and Techniques*, IEEE, Vol. 45, No. 12, 7 pages (December 1997).
	AO21	Peeters, G. *et al.*, "Evaluation of Statistical Models for Clear-Air Scintillation Prediction Using Olympus Satellite Measurements," *International Journal of Satellite Communications*, John Wiley and Sons, Vol. 15, No. 2, pp. 73-88 (March-April 1997).
	AP21	Perrey, A.G. and Schoenwetter, H.K., *NBS Technical Note 1121: A Schottky Diode Bridge Sampling Gate*, U.S. Dept. of Commerce, pp. 1-14 (May 1980).
	AQ21	Poulton, K. *et al.*, "A 1-Ghz 6-bit ADC System," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-22, No. 6, pp. 962-969 (December 1987).
	AR21	Press Release, "Parkervision, Inc. Announces Fiscal 1993 Results," Lippert/Heilshorn and Associates, 2 Pages (April 6, 1994).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA22	5,251,218	10/1993	Stone *et al.*			
	AB22	5,251,232	10/1993	Nonami			
	AC22	5,260,970	11/1993	Henry *et al.*			
	AD22	5,263,194	11/1993	Ragan			
	AE22	5,263,196	11/1993	Jasper			
	AF22	5,267,023	11/1993	Kawasaki			
	AG22	5,278,826	01/1994	Murphy *et al.*			
	AH22	5,282,023	01/1994	Scarpa			
	AI22	5,287,516	02/1994	Schaub			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ22	JP 5-327356	12/1993	JP			No
	AK22	EP 0 643 477 A2 & A3	03/1995	EP			N/A
	AL22	EP 0 877 476 A1	11/1998	EP			N/A
	AM22	EP 0 977 351 A1	02/2000	EP			N/A

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN22	Press Release, "Parkervision, Inc. Announces the Appointment of Michael Baker to the New Position of National Sales Manager," Lippert/Heilshorn and Associates, 1 Page (April 7, 1994).
	AO22	Press Release, "Parkervision's Cameraman Well-Received By Distance Learning Market," Lippert/Heilshorn and Associates, 2 Pages (April 8, 1994).
	AP22	Press Release, "Parkervision, Inc. Announces First Quarter Financial Results," Lippert/Heilshorn and Associates, 2 Pages (April 26, 1994).
	AQ22	Press Release, "Parkervision, Inc. Announces The Retirement of William H. Fletcher, Chief Financial Officer," Lippert/Heilshorn and Associates, 1 Page (May 11, 1994).
	AR22	Press Release, "Parkervision, Inc. Announces New Cameraman System II™ At Infocomm Trade Show," Lippert/Heilshorn and Associates, 3 Pages (June 9, 1994).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA23	5,293,398	03/1994	Hamao *et al.*			
	AB23	5,303,417	04/1994	Laws			
	AC23	5,307,517	04/1994	Rich			
	AD23	5,315,583	05/1994	Murphy *et al.*			
	AE23	5,321,852	06/1994	Seong			
	AF23	5,325,204	06/1994	Scarpa			
	AG23	5,337,014	08/1994	Najle *et al.*			
	AH23	5,339,054	08/1994	Taguchi			
	AI23	5,339,459	08/1994	Schiltz *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ23	WO 00/31659 A1	06/2000	PCT			N/A
	AK23	JP 9-36664	02/1997	JP			No
	AL23	DE 196 48 915 A1	06/1998	DE			Yes (See AO59)
	AM23	DE 692 21 098 T2	01/1998	DE			No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN23	Press Release, "Parkervision, Inc. Announces Appointments to its National Sales Force," Lippert/Heilshorn and Associates, 2 Pages (June 17, 1994).
	AO23	Press Release, "Parkervision, Inc. Announces Second Quarter and Six Months Financial Results," Lippert/Heilshorn and Associates, 3 Pages (August 9, 1994).
	AP23	Press Release, "Parkervision, Inc. Announces Third Quarter and Nine Months Financial Results," Lippert/Heilshorn and Associates, 3 Pages (October 28, 1994).
	AQ23	Press Release, "Parkervision, Inc. Announces First Significant Dealer Sale of Its *Cameraman*® System II," Lippert/Heilshorn and Associates, 2 Pages (November 7, 1994).
	AR23	Press Release, "Parkervision, Inc. Announces Fourth Quarter and Year End Results," Lippert/Heilshorn and Associates, 2 Pages (March 1, 1995).

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	AA24	5,355,114	10/1994	Sutterlin *et al.*			
	AB24	5,361,408	11/1994	Watanabe *et al.*			
	AC24	5,369,800	11/1994	Takagi *et al.*			
	AD24	5,375,146	12/1994	Chalmers			
	AE24	5,379,040	01/1995	Mizomoto *et al.*			
	AF24	5,379,141	01/1995	Thompson *et al.*			
	AG24	5,388,063	02/1995	Takatori *et al.*			
	AH24	5,390,364	02/1995	Webster *et al.*			
	AI24	5,400,084	03/1995	Scarpa			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ24	WO 98/53556 A2	11/1998	PCT			N/A
	AK24	DT 1936252	01/1971	DT			Yes (Doc. AO60)
	AL24	JP 62-12381	01/1987	JP			No
	AM24	JP 4-154227	05/1992	JP			No

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EXAMINER INITIAL	DOC. REF.	CITATION
	AN24	Press Release, "Parkervision, Inc. Announces Joint Product Developments With VTEL," Lippert/Heilshorn and Associates, 2 Pages (March 21, 1995).
	AO24	Press Release, "Parkervision, Inc. Announces First Quarter Financial Results," Lippert/Heilshorn and Associates, 3 Pages (April 28, 1995).
	AP24	Press Release, "Parkervision Wins Top 100 Product Districts' Choice Award," Parkervision Marketing and Manufacturing Headquarters, 1 Page (June 29, 1995).
	AQ24	Press Release, "Parkervision National Sales Manager Next President of USDLA," Parkervision Marketing and Manufacturing Headquarters, 1 Page (July 6, 1995).
	AR24	Press Release, "Parkervision Granted New Patent," Parkervision Marketing and Manufacturing Headquarters, 1 Page (July 21, 1995).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA25	5,404,127	04/1995	Lee *et al.*			
	AB25	5,410,541	04/1995	Hotto			
	AC25	5,410,743	04/1995	Seely *et al.*			
	AD25	5,412,352	05/1995	Graham			
	AE25	5,416,803	05/1995	Janer			
	AF25	5,422,913	06/1995	Wilkinson			
	AG25	5,423,082	06/1995	Cygan *et al.*			
	AH25	5,428,638	06/1995	Cioffi *et al.*			
	AI25	5,428,640	06/1995	Townley			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ25	JP 6-284038	10/1994	JP			No
	AK25	JP 10-96778	04/1998	JP			No
	AL25	JP 11-98205	04/1999	JP			No
	AM25	JP 61-232706	10/1986	JP			No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN25	Press Release, "Parkervision, Inc. Announces Second Quarter and Six Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (July 31, 1995).
	AO25	Press Release, "Parkervision, Inc. Expands Its Cameraman System II Product Line," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (September 22, 1995).
	AP25	Press Release, "Parkervision Announces New Camera Control Technology," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 25, 1995).
	AQ25	Press Release, "Parkervision, Inc. Announces Completion of VTEL/Parkervision Joint Product Line," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 30, 1995).
	AR25	Press Release, "Parkervision, Inc. Announces Third Quarter and Nine Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 30, 1995).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	*DOC. REF.*	*DOCUMENT NUMBER*	*DATE*	*NAME*	*CLASS*	*SUB-CLASS*	*FILING DATE*
	AA26	5,434,546	07/1995	Palmer			
	AB26	5,438,692	08/1995	Mohindra			
	AC26	5,444,415	08/1995	Dent *et al.*			
	AD26	5,444,416	08/1995	Ishikawa *et al.*			
	AE26	5,444,865	08/1995	Heck *et al.*			
	AF26	5,446,421	08/1995	Kechkaylo			
	AG26	5,446,422	08/1995	Mattila *et al.*			
	AH26	5,448,602	09/1995	Ohmori *et al.*			
	AI26	5,451,899	09/1995	Lawton			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	*DOC. REF.*	*DOCUMENT NUMBER*	*DATE*	*COUNTRY*	*CLASS*	*SUB-CLASS*	*TRANSLATION*
	AJ26	JP 9-171399	06/1997	JP			No
	AK26	JP 10-41860	02/1998	JP			No
	AL26	JP 10-173563	06/1998	JP			Yes (Doc. AN62)
	AM26	JP 58-031622	02/1983	JP			No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	*DOC. REF.*	*CITATION*
	AN26	Press Release, "Parkervision's Cameraman Personal Locator Camera System Wins Telecon XV Award," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (November 1, 1995).
	AO26	Press Release, "Parkervision, Inc. Announces Purchase Commitment From VTEL Corporation," Parkervision Marketing and Manufacturing Headquarters, 1 Page (February 26, 1996).
	AP26	Press Release, "ParkerVision, Inc. Announces Fourth Quarter and Year End Results," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (February 27, 1996).
	AQ26	Press Release, "ParkerVision, Inc. Expands its Product Line," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (March 7, 1996).
	AR26	Press Release, "ParkerVision Files Patents for its Research of Wireless Technology," Parkervision Marketing and Manufacturing Headquarters, 1 Page (March 28, 1996).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA27	5,454,007	09/1995	Dutta			
	AB27	5,454,009	09/1995	Fruit *et al.*			
	AC27	5,463,356	10/1995	Palmer			
	AD27	5,463,357	10/1995	Hobden			
	AE27	5,465,071	11/1995	Kobayashi *et al.*			
	AF27	5,465,410	11/1995	Hiben *et al.*			
	AG27	5,465,415	11/1995	Bien			
	AH27	5,471,162	11/1995	McEwan			
	AI27	5,479,120	12/1995	McEwan			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ27	JP 61-245749	11/1986	JP			No
	AK27	JP 64-048557	02/1989	JP			No
	AL27	JP 59-022438	02/1984	JP			No
	AM27	JP 59-123318	07/1984	JP			No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN27	Press Release, "Parkervision, Inc. Announces First Significant Sale of Its Cameraman® Three-Chip System," Parkervision Marketing and Manufacturing Headquarters, 2 pages (April 12, 1996).
	AO27	Press Release, "Parkervision, Inc. Introduces New Product Line For Studio Production Market," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (April 15, 1996).
	AP27	Press Release, "Parkervision, Inc. Announces Private Placement of 800,000 Shares," Parkervision Marketing and Manufacturing Headquarters, 1 Page (April 15, 1996).
	AQ27	Press Release, "Parkervision, Inc. Announces First Quarter Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (April 30, 1996).
	AR27	Press Release, "ParkerVision's New Studio Product Wins Award," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (June 5, 1996).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA28	5,479,447	12/1995	Chow *et al.*			
	AB28	5,483,193	01/1996	Kennedy *et al.*			
	AC28	5,483,549	01/1996	Weinberg *et al.*			
	AD28	5,483,691	01/1996	Heck *et al.*			
	AE28	5,490,173	02/1996	Whikehart *et al.*			
	AF28	5,493,581	02/1996	Young *et al.*			
	AG28	5,493,721	02/1996	Reis			
	AH28	5,495,200	02/1996	Kwan *et al.*			
	AI28	5,495,202	02/1996	Hsu			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ28	JP 61-193521	08/1986	JP			No
	AK28	JP 62-047214	02/1987	JP			No
	AL28	JP 63-274214	11/1988	JP			No
	AM28	JP 7-169292 A	07/1995	JP			No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN28	Press Release, "Parkervision, Inc. Announces Second Quarter and Six Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (August 1, 1996).
	AO28	Press Release, "Parkervision, Inc. Announces Third Quarter and Nine Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 29, 1996).
	AP28	Press Release, "PictureTel and ParkerVision Sign Reseller Agreement," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 30, 1996).
	AQ28	Press Release, "CLI and ParkerVision Bring Enhanced Ease-of-Use to Videoconferencing," CLI/Parkervision, 2 Pages (January 20, 1997).
	AR28	Press Release, "Parkervision, Inc. Announces Fourth Quarter and Year End Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (February 27, 1997).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA29	5,495,500	02/1996	Jovanovich *et al.*			
	AB29	5,499,267	03/1996	Ohe *et al.*			
	AC29	5,500,758	03/1996	Thompson *et al.*			
	AD29	5,517,688	05/1996	Fajen *et al.*			
	AE29	5,519,890	05/1996	Pinckley			
	AF29	5,523,719	06/1996	Longo *et al.*			
	AG29	5,523,726	06/1996	Kroeger *et al.*			
	AH29	5,523,760	06/1996	McEwan			
	AI29	5,539,770	07/1996	Ishigaki			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ29	JP 10-22804 A	01/1998	JP			No
	AK29	JP 8-288882 A	11/1996	JP			No
	AL29	WO 95/19073 A2	07/1995	WO			N/A
	AM29						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN29	Press Release, "Parkervision, Inc. Announces First Quarter Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (April 29, 1997).
	AO29	Press Release, "NEC and Parkervision Make Distance Learning Closer," NEC America, 2 Pages (June 18, 1997).
	AP29	Press Release, "Parkervision Supplies JPL with Robotic Cameras, Cameraman Shot Director for Mars Mission," Parkervision Marketing and Manufacturing Headquarters, 2 pages (July 8, 1997).
	AQ29	Press Release, "ParkerVision and IBM Join Forces to Create Wireless Computer Peripherals," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (July 23, 1997).
	AR29	Press Release, "ParkerVision, Inc. Announces Second Quarter and Six Months Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (July 31, 1997).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA30	5,555,453	09/1996	Kajimoto *et al.*			
	AB30	5,557,641	09/1996	Weinberg			
	AC30	5,557,642	09/1996	Williams			
	AD30	5,579,341	11/1996	Smith *et al.*			
	AE30	5,579,347	11/1996	Lindquist *et al.*			
	AF30	5,584,068	12/1996	Mohindra			
	AG30	5,592,131	01/1997	Labreche *et al.*			
	AH30	5,602,847	02/1997	Pagano *et al.*			
	AI30	5,602,868	02/1997	Wilson			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ30						Yes No
	AK30						Yes No
	AL30						Yes No
	AM30						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN30	Press Release, "Parkervision, Inc. Announces Private Placement of 990,000 Shares," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (September 8, 1997).
	AO30	Press Release, "Wal-Mart Chooses Parkervision for Broadcast Production," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (October 24, 1997).
	AP30	Press Release, "Parkervision, Inc. Announces Third Quarter Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (October 30, 1997).
	AQ30	Press Release, "ParkerVision Announces Breakthrough in Wireless Radio Frequency Technology," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (December 10, 1997).
	AR30	Press Release, "Parkervision, Inc. Announces the Appointment of Joseph F. Skovron to the Position of Vice President, Licensing - Wireless Technologies," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (January 9, 1998).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA31	5,604,732	02/1997	Kim *et al.*			
	AB31	5,608,531	03/1997	Honda *et al.*			
	AC31	5,610,946	03/1997	Tanaka *et al.*			
	AD31	RE 35,494	04/1997	Nicollini			
	AE31	5,617,451	04/1997	Mimura *et al.*			
	AF31	5,619,538	04/1997	Sempel *et al.*			
	AG31	5,621,455	04/1997	Rogers *et al.*			
	AH31	5,630,227	05/1997	Bella *et al.*			
	AI31	5,640,415	06/1997	Pandula			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ31						Yes No
	AK31						Yes No
	AL31						Yes No
	AM31						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN31	Press Release, "Parkervision Announces Existing Agreement with IBM Terminates-- Company Continues with Strategic Focus Announced in December," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (January 27, 1998).
	AO31	Press Release, "Laboratory Tests Verify Parkervision Wireless Technology," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (March 3, 1998).
	AP31	Press Release, "Parkervision, Inc. Announces Fourth Quarter and Year End Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (March 5, 1998).
	AQ31	Press Release, "Parkervision Awarded Editors' Pick of Show for NAB 98," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (April 15, 1998).
	AR31	Press Release, "Parkervision Announces First Quarter Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (May 4, 1998).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.001000P	APPLICATION NO. 12/349,802
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA32	5,640,424	06/1997	Banavong *et al.*			
	AB32	5,640,428	06/1997	Abe *et al.*			
	AC32	5,640,698	06/1997	Shen *et al.*			
	AD32	5,648,985	07/1997	Bjerede *et al.*			
	AE32	5,650,785	07/1997	Rodal			
	AF32	5,661,424	08/1997	Tang			
	AG32	5,663,878	09/1997	Walker			
	AH32	5,663,986	09/1997	Striffler			
	AI32	5,668,836	09/1997	Smith *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ32						Yes No
	AK32						Yes No
	AL32						Yes No
	AM32						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN32	Press Release, "Parkervision 'DIRECT2DATA' Introduced in Response to Market Demand," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (July 9, 1998).
	AO32	Press Release, "Parkervision Expands Senior Management Team," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (July 29, 1998).
	AP32	Press Release, "Parkervision Announces Second Quarter and Six Month Financial Results," Parkervision Marketing and Manufacturing Headquarters, 4 Pages (July 30, 1998).
	AQ32	Press Release, "Parkervision Announces Third Quarter and Nine Month Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (October 30, 1998).
	AR32	Press Release, "Questar Infocomm, Inc. Invests $5 Million in Parkervision Common Stock," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (December 2, 1998).

EXAMINER	DATE CONSIDERED

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	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA33	5,680,078	10/1997	Ariie			
	AB33	5,680,418	10/1997	Croft *et al.*			
	AC33	5,689,413	11/1997	Jaramillo *et al.*			
	AD33	5,699,006	12/1997	Zele *et al.*			
	AE33	5,705,955	01/1998	Freeburg *et al.*			
	AF33	5,710,998	01/1998	Opas			
	AG33	5,714,910	02/1998	Skoczen *et al.*			
	AH33	5,715,281	02/1998	Bly *et al.*			
	AI33	5,721,514	02/1998	Crockett *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ33						Yes No
	AK33						Yes No
	AL33						Yes No
	AM33						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN33	Press Release, "Parkervision Adds Two New Directors," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (March 5, 1999).
	AO33	Press Release, "Parkervision Announces Fourth Quarter and Year End Financial Results," Parkervision Marketing and Manufacturing Headquarters, 3 Pages (March 5, 1999).
	AP33	Press Release, "Joint Marketing Agreement Offers New Automated Production Solution," Parkervision Marketing and Manufacturing Headquarters, 2 Pages (April 13, 1999).
	AQ33	"Project COST 205: Scintillations in Earth-satellite links," *Alta Frequenza: Scientific Review in Electronics*, AEI, Vol. LIV, No. 3, pp. 209-211 (May-June, 1985).
	AR33	Razavi, B., *RF Microelectronics*, Prentice-Hall, pp. 147-149 (1998).

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	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA34	5,724,002	03/1998	Hulick			
	AB34	5,724,653	03/1998	Baker *et al.*			
	AC34	5,729,577	03/1998	Chen			
	AD34	5,729,829	03/1998	Talwar *et al.*			
	AE34	5,732,333	03/1998	Cox *et al.*			
	AF34	5,736,895	04/1998	Yu *et al.*			
	AG34	5,737,035	04/1998	Rotzoll			
	AH34	5,742,189	04/1998	Yoshida *et al.*			
	AI34	5,748,683	05/1998	Smith *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ34						Yes No
	AK34						Yes No
	AL34						Yes No
	AM34						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN34	Reeves, R.J.D., "The Recording and Collocation of Waveforms (Part 1)," *Electronic Engineering*, Morgan Brothers Limited, Vol. 31, No. 373, pp. 130-137 (March 1959).
	AO34	Reeves, R.J.D., "The Recording and Collocation of Waveforms (Part 2)," *Electronic Engineering*, Morgan Brothers Limited, Vol. 31, No. 374, pp. 204-212 (April 1959).
	AP34	Rein, H.M. and Zahn, M., "Subnanosecond-Pulse Generator with Variable Pulsewidth Using Avalanche Transistors," *Electronics Letters*, IEE, Vol. 11, No. 1, pp. 21-23 (January 9, 1975).
	AQ34	Riad, S.M. and Nahman, N.S., "Modeling of the Feed-through Wideband (DC to 12.4 Ghz) Sampling-Head," *IEEE MTT-S International Microwave Symposium Digest*, IEEE, pp. 267-269 (June 27-29, 1978).
	AR34	Rizzoli, V. *et al.*, "Computer-Aided Noise Analysis of MESFET and HEMT Mixers," *IEEE Transactions on Microwave Theory and Techniques*, IEEE, Vol. 37, No. 9, pp. 1401-1410 (September 1989).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA35	RE 35,829	06/1998	Sanderford, Jr.			
	AB35	5,760,645	06/1998	Comte *et al.*			
	AC35	5,764,087	06/1998	Clark			
	AD35	5,767,726	06/1998	Wang			
	AE35	5,768,118	06/1998	Faulk *et al.*			
	AF35	5,771,442	06/1998	Wang *et al.*			
	AG35	5,777,692	07/1998	Ghosh			
	AH35	5,777,771	07/1998	Smith			
	AI35	5,786,844	07/1998	Rogers *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ35						Yes No
	AK35						Yes No
	AL35						Yes No
	AM35						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN35	Rowe, H.E., *Signals and Noise in Communication Systems*, D. Van Nostrand Company, Inc., Princeton, New Jersey, including, for example, Chapter V, Pulse Modulation Systems (1965).
	AO35	Rücker, F. and Dintelmann, F., "Effect of Antenna Size on OTS Signal Scintillations and Their Seasonal Dependence," *Electronics Letters*, IEE, Vol. 19, No. 24, pp. 1032-1034 (November 24, 1983).
	AP35	Russell, R. and Hoare, L., "Millimeter Wave Phase Locked Oscillators," *Military Microwaves '78 Conference Proceedings*, Microwave Exhibitions and Publishers, pp. 238-242 (October 25-27, 1978).
	AQ35	Sabel, L.P., "A DSP Implementation of a Robust Flexible Receiver/Demultiplexer for Broadcast Data Satellite Communications," *The Institution of Engineers Australia Communications Conference*, Institution of Engineers, Australia, pp. 218-223 (October 16-18, 1990).
	AR35	Salous, S., "IF digital generation of FMCW waveforms for wideband channel characterization," *IEE Proceedings-I*, IEE, Vol. 139, No. 3, pp. 281-288 (June 1992).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA36	5,793,801	08/1998	Fertner			
	AB36	5,793,818	08/1998	Claydon *et al.*			
	AC36	5,802,463	09/1998	Zuckerman			
	AD36	5,809,060	09/1998	Cafarella *et al.*			
	AE36	5,818,582	10/1998	Fernandez *et al.*			
	AF36	5,825,254	10/1998	Lee			
	AG36	5,834,985	11/1998	Sundegård			
	AH36	5,864,754	01/1999	Hotto			
	AI36	5,881,375	03/1999	Bonds			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ36						Yes No
	AK36						Yes No
	AL36						Yes No
	AM36						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN36	"Sampling Loops Lock Sources to 23 Ghz," *Microwaves & RF*, Penton Publishing, p. 212 (September 1990).
	AO36	Sasikumar, M. *et al.*, "Active Compensation in the Switched-Capacitor Biquad," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 1008-1009 (August 1983).
	AP36	Saul, P.H., "A GaAs MESFET Sample and Hold Switch," *Fifth European Solid State Circuits Conference-ESSCIRC 79*, IEE, pp. 5-7 (1979).
	AQ36	Shen, D.H. *et al.*, "A 900-MHZ RF Front-End with Integrated Discrete-Time Filtering," *IEEE Journal of Solid-State Circuits*, IEEE Solid-State Circuits Council, Vol. 31, No. 12, pp. 1945-1954 (December 1996).
	AR36	Shen, X.D. and Vilar, E., "Anomalous transhorizon propagation and meteorological processes of a multilink path," *Radio Science*, American Geophysical Union, Vol. 30, No. 5, pp. 1467-1479 (September-October 1995).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA37	5,892,380	04/1999	Quist			
	AB37	5,894,239	04/1999	Bonaccio *et al.*			
	AC37	5,896,562	04/1999	Heinonen			
	AD37	5,900,747	05/1999	Brauns			
	AE37	5,901,054	05/1999	Leu *et al.*			
	AF37	5,901,187	05/1999	Iinuma			
	AG37	5,901,344	05/1999	Opas			
	AH37	5,901,347	05/1999	Chambers *et al.*			
	AI37	5,901,348	05/1999	Bang *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ37						Yes No
	AK37						Yes No
	AL37						Yes No
	AM37						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN37	Shen, X. and Tawfik, A.N., "Dynamic Behaviour of Radio Channels Due to Trans-Horizon Propagation Mechanisms," *Electronics Letters*, IEE, Vol. 29, No. 17, pp. 1582-1583 (August 19, 1993).
	AO37	Shen, X. *et al.*, "Modeling Enhanced Spherical Diffraction and Troposcattering on a Transhorizon Path with aid of the parabolic Equation and Ray Tracing Methods," *IEE Colloquium on Common modeling techniques for electromagnetic wave and acoustic wave propagation*, IEE, pp. 4/1-4/7 (March 8, 1996).
	AP37	Shen, X. and Vilar, E., "Path loss statistics and mechanisms of transhorizon propagation over a sea path," *Electronics Letters*, IEE, Vol. 32, No. 3, pp. 259-261 (February 1, 1996).
	AQ37	Shen, D. *et al.*, "A 900 MHZ Integrated Discrete-Time Filtering RF Front-End," *IEEE International Solid State Circuits Conference*, IEEE, Vol. 39, pp. 54-55 and 417 (February 1996).
	AR37	Spillard, C. *et al.*, "X-Band Tropospheric Transhorizon Propagation Under Differing Meteorological Conditions," *Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation*, IEE, pp. 451-455 (April 4-7, 1989).

EXAMINER	DATE CONSIDERED

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA38	5,901,349	05/1999	Guegnaud *et al.*			
	AB38	5,903,178	05/1999	Miyatsuji *et al.*			
	AC38	5,903,187	05/1999	Claverie *et al.*			
	AD38	5,903,196	05/1999	Salvi *et al.*			
	AE38	5,903,421	05/1999	Furutani *et al.*			
	AF38	5,903,553	05/1999	Sakamoto *et al.*			
	AG38	5,903,595	05/1999	Suzuki			
	AH38	5,903,609	05/1999	Kool *et al.*			
	AI38	5,903,827	05/1999	Kennan *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ38						Yes No
	AK38						Yes No
	AL38						Yes No
	AM38						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN38	Stafford, K.R. *et al.*, "A Complete Monolithic Sample/Hold Amplifier," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-9, No. 6, pp. 381-387 (December 1974).
	AO38	Staruk, W. Jr. *et al.*, "Pushing HF Data Rates," *Defense Electronics*, EW Communications, Vol. 17, No. 5, pp. 211, 213, 215, 217, 220 and 222 (May 1985).
	AP38	Stephenson, A.G., "Digitizing multiple RF signals requires an optimum sampling rate," *Electronics*, McGraw-Hill, pp. 106-110 (March 27, 1972).
	AQ38	Sugarman, R., "Sampling Oscilloscope for Statistically Varying Pulses," *The Review of Scientific Instruments*, American Institute of Physics, Vol. 28, No. 11, pp. 933-938 (November 1957).
	AR38	Sylvain, M., "Experimental probing of multipath microwave channels," *Radio Science*, American Geophysical Union, Vol. 24, No. 2, pp. 160-178 (March-April 1989).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA39	5,903,854	05/1999	Abe *et al.*			
	AB39	5,905,449	05/1999	Tsubouchi *et al.*			
	AC39	5,907,149	05/1999	Marckini			
	AD39	5,907,197	05/1999	Faulk			
	AE39	5,911,116	06/1999	Nosswitz			
	AF39	5,911,123	06/1999	Shaffer *et al.*			
	AG39	5,914,622	06/1999	Inoue			
	AH39	5,920,199	07/1999	Sauer			
	AI39	5,943,370	08/1999	Smith			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ39						Yes No
	AK39						Yes No
	AL39						Yes No
	AM39						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN39	Takano, T., "NOVEL GaAs Pet Phase Detector Operable To Ka Band," *IEEE MT-S Digest*, IEEE, pp. 381-383 (1984).
	AO39	Tan, M.A., "Biquadratic Transconductance Switched-Capacitor Filters," *IEEE Transactions on Circuits and Systems- I: Fundamental Theory and Applications*, IEEE Circuits and Systems Society, Vol. 40, No. 4, pp. 272-275 (April 1993).
	AP39	Tanaka, K. *et al.*, "Single Chip Multisystem AM Stereo Decoder IC," *IEEE Transactions on Consumer Electronics*, IEEE Consumer Electronics Society, Vol. CE-32, No. 3, pp. 482-496 (August 1986).
	AQ39	Tawfik, A.N., "Amplitude, Duration and Predictability of Long Hop Trans-Horizon X-band Signals Over the Sea," *Electronics Letters*, IEE, Vol. 28, No. 6, pp. 571-572 (March 12, 1992).
	AR39	Tawfik, A.N. and Vilar, E., "Correlation of Transhorizon Signal Level Strength with Localized Surface Meteorological Parameters," *Eighth International Conference on Antennas and Propagation*, Electronics Division of the IEE, pp. 335-339 (March 30- April 2, 1993).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA40	4,017,798	04/1977	Gordy *et al.*			
	AB40	4,032,847	06/1977	Unkauf			
	AC40	4,253,067	02/1981	Caples *et al.*			
	AD40	4,393,395	07/1983	Hacke *et al.*			
	AE40	4,816,704	03/1989	Fiori, Jr.			
	AF40	4,841,265	06/1989	Watanabe *et al.*			
	AG40	4,943,974	07/1990	Motamedi			
	AH40	5,115,409	05/1992	Stepp			
	AI40	5,353,306	10/1994	Yamamoto			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ40						Yes No
	AK40						Yes No
	AL40						Yes No
	AM40						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN40	Tawfik, A.N. and Vilar, E., "Dynamic Structure of a Transhorizon Signal at X-band Over a Sea Path," *Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation*, IEE, pp. 446-450 (April 4-7, 1989).
	AO40	Tawfik, A.N. and Vilar, E., "Statistics of Duration and Intensity of Path Loss in a Microwave Transhorizon Sea-Path," *Electronics Letters*, IEE, Vol. 26, No. 7, pp. 474-476 (March 29, 1990).
	AP40	Tawfik, A.N. and Vilar, E., "X-Band Transhorizon Measurements of CW Transmissions Over the Sea- Part 1: Path Loss, Duration of Events, and Their Modeling," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. 41, No. 11, pp. 1491-1500 (November 1993).
	AQ40	Temes, G.C. and Tsividis, T., "The Special Section on Switched-Capacitor Circuits," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 915-916 (August 1983).
	AR40	Thomas, G.B., *Calculus and Analytic Geometry*, Third Edition, Addison-Wesley Publishing, pp. 119-133 (1960).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA41	5,515,014	05/1996	Troutman			
	AB41	5,563,550	10/1996	Toth			
	AC41	5,574,755	11/1996	Persico			
	AD41	5,604,592	02/1997	Kotidis *et al.*			
	AE41	5,638,396	06/1997	Klimek			
	AF41	5,675,392	10/1997	Nayebi *et al.*			
	AG41	5,694,096	12/1997	Ushiroku *et al.*			
	AH41	5,757,870	05/1998	Miya *et al.*			
	AI41	5,768,323	06/1998	Kroeger *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ41						Yes No
	AK41						Yes No
	AL41						Yes No
	AM41						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN41	Tomassetti, Q., "An Unusual Microwave Mixer," *16th European Microwave Conference*, Microwave Exhibitions and Publishers, pp. 754-759 (September 8-12, 1986).
	AO41	Tortoli, P. *et al.*, "Bidirectional Doppler Signal Analysis Based on a Single RF Sampling Channel," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, IEEE Ultrasonics, Ferroelectrics, and Frequency Control Society, Vol. 41, No. 1, pp. 1-3 (January 1984).
	AP41	Tsividis, Y. and Antognetti, P. (Ed.), *Design of MOS VLSI Circuits for Telecommunications*, Prentice-Hall, p. 304 (1985).
	AQ41	Tsividis, Y., "Principles of Operation and Analysis of Switched-Capacitor Circuits," *Proceedings of the IEEE*, IEEE, Vol. 71, No. 8, pp. 926-940 (August 1983).
	AR41	Tsurumi, H. and Maeda, T., "Design Study on a Direct Conversion Receiver Front-End for 280 MHZ, 900 MHZ, and 2.6 Ghz Band Radio Communication Systems," *41st IEEE Vehicular Technology Conference*, IEEE Vehicular Technology Society, pp. 457-462 (May 19-22, 1991).

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.001000P	APPLICATION NO. 12/349,802
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA42	5,770,985	06/1998	Ushiroku *et al.*			
	AB42	5,778,022	07/1998	Walley			
	AC42	5,812,546	09/1998	Zhou *et al.*			
	AD42	5,818,869	10/1998	Miya *et al.*			
	AE42	5,844,449	12/1998	Abeno *et al.*			
	AF42	5,872,446	02/1999	Cranford, Jr. *et al.*			
	AG42	5,909,447	06/1999	Cox *et al.*			
	AH42	5,933,467	08/1999	Sehier *et al.*			
	AI42	5,952,895	09/1999	McCune, Jr. *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ42						Yes No
	AK42						Yes No
	AL42						Yes No
	AM42						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN42	Valdmanis, J.A. *et al.*, "Picosecond and Subpicosend Optoelectronics for Measurements of Future High Speed Electronic Devices," *IEDM Technical Digest*, IEEE, pp. 597-600 (December 5-7, 1983).
	AO42	van de Kamp, M.M.J.L., "Asymmetric signal level distribution due to tropospheric scintillation," *Electronics Letters*, IEE, Vol. 34, No. 11, pp. 1145-1146 (May 28, 1998).
	AP42	Vasseur, H. and Vanhoenacker, D., "Characterization of tropospheric turbulent layers from radiosonde data," *Electronics Letters*, IEE, Vol. 34, No. 4, pp. 318-319 (February 19, 1998).
	AQ42	Verdone, R., "Outage Probability Analysis for Short-Range Communication Systems at 60 Ghz in ATT Urban Environments," *IEEE Transactions on Vehicular Technology*, IEEE Vehicular Technology Society, Vol. 46, No. 4, pp. 1027-1039 (November 1997).
	AR42	Vierira-Ribeiro, S.A., *Single-IF DECT Receiver Architecture using a Quadrature Sub-Sampling Band-Pass Sigma-Delta Modulator*, Thesis for Degree of Master's of Engineering, Carleton University, UMI Dissertation Services, pp. 1-180 (April 1995).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA43	5,960,033	09/1999	Shibano *et al.*			
	AB43	6,041,073	03/2000	Davidovici *et al.*			
	AC43	6,054,889	04/2000	Kobayashi			
	AD43	6,084,922	07/2000	Zhou *et al.*			
	AE43	6,125,271	09/2000	Rowland *et al.*			
	AF43	6,147,340	11/2000	Levy			
	AG43	6,147,763	11/2000	Steinlechner			
	AH43	6,150,890	11/2000	Damgaard *et al.*			
	AI43	5,126,682	06/1992	Weinberg *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ43						Yes No
	AK43						Yes No
	AL43						Yes No
	AM43						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN43	Vilar, E. *et al.*, "A Comprehensive/Selective MM-Wave Satellite Downlink Experiment on Fade Dynamics," *Tenth International Conference on Antennas and Propagation*, Electronics Division of the IEE, pp. 2.98-2.101 (April 14-17, 1997).
	AO43	Vilar, E. *et al.*, "A System to Measure LOS Atmospheric Transmittance at 19 Ghz," *AGARD Conference Proceedings No. 346: Characteristics of the Lower Atmosphere Influencing Radio Wave Propagation*, AGARD, pp. 8-1 - 8-16 (October 4-7, 1983).
	AP43	Vilar, E. and Smith, H., "A Theoretical and Experimental Study of Angular Scintillations in Earth Space Paths," *IEEE Transactions on Antennas and Propagation*, IEEE, Vol. AP-34, No. 1, pp. 2-10 (January 1986).
	AQ43	Vilar, E. *et al.*, "A Wide Band Transhorizon Experiment at 11.6 Ghz," *Eighth International Conference on Antennas and Propagation*, Electronics Division of the IEE, pp. 441-445 (March 30- April 2, 1993).
	AR43	Vilar, E. and Matthews, P.A., "Amplitude Dependence of Frequency in Oscillators," *Electronics Letters*, IEE, Vol. 8, No. 20, pp. 509-511 (October 5, 1972).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA44	5,841,811	11/1998	Song			
	AB44	4,051,475	09/1977	Campbell			
	AC44	5,953,642	09/1999	Feldtkeller *et al.*			
	AD44	4,653,117	03/1987	Heck			
	AE44	5,859,878	01/1999	Phillips *et al.*			
	AF44	5,894,496	04/1999	Jones			
	AG44	5,915,278	06/1999	Mallick			
	AH44	6,028,887	02/2000	Harrison *et al.*			
	AI44	6,081,691	06/2000	Renard *et al.*			

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	AJ44						Yes No
	AK44						Yes No
	AL44						Yes No
	AM44						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN44	Vilar, E. *et al.*, "An experimental mm-wave receiver system for measuring phase noise due to atmospheric turbulence," *Proceedings of the 25th European Microwave Conference*, Nexus House, pp. 114-119 (1995).
	AO44	Vilar, E. and Burgueño, A., "Analysis and Modeling of Time Intervals Between Rain Rate Exceedances in the Context of Fade Dynamics," *IEEE Transactions on Communications*, IEEE Communications Society, Vol. 39, No. 9, pp. 1306-1312 (September 1991).
	AP44	Vilar, E. *et al.*, "Angle of Arrival Fluctuations in High and Low Elevation Earth Space Paths," *Fourth International Conference on Antennas and Propagation (ICAP 85)*, Electronics Division of the IEE, pp. 83-88 (April 16-19, 1985).
	AQ44	Vilar, E., "Antennas and Propagation: A Telecommunications Systems Subject," *Electronics Division Colloquium on Teaching Antennas and Propagation to Undergraduates*, IEE, pp. 7/1-7/6 (March 8, 1988).
	AR44	Vilar, E. *et al.*, "CERS*. Millimetre-Wave Beacon Package and Related Payload Doppler Correction Strategies," *Electronics Division Colloquium on CERS- Communications Engineering Research Satellite*, IEE, pp. 10/1-10/10 (April 10, 1984).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA45	6,121,819	09/2000	Traylor			
	AB45	6,144,236	11/2000	Vice *et al.*			
	AC45	6,144,846	11/2000	Durec			
	AD45	6,175,728 B1	01/2001	Mitama			
	AE45	5,705,949	01/1998	Alelyunas *et al.*			
	AF45	5,883,548	03/1999	Assard *et al.*			
	AG45	4,484,143	11/1984	French *et al.*			
	AH45	5,841,324	11/1998	Williams			
	AI45	4,855,894	08/1989	Asahi *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ45						Yes No
	AK45						Yes No
	AL45						Yes No
	AM45						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN45	Vilar, E. and Moulsley, T.J., "Comment and Reply: Probability Density Function of Amplitude Scintillations," *Electronics Letters*, IEE, Vol. 21, No. 14, pp. 620-622 (July 4, 1985).
	AO45	Vilar, E. *et al.*, "Comparison of Rainfall Rate Duration Distributions for ILE-IFE and Barcelona," *Electronics Letters*, IEE, Vol. 28, No. 20, pp. 1922-1924 (September 24, 1992).
	AP45	Vilar, E., "Depolarization and Field Transmittances in Indoor Communications," *Electronics Letters*, IEE, Vol. 27, No. 9, pp. 732-733 (April 25, 1991).
	AQ45	Vilar, E. and Larsen, J.R., "Elevation Dependence of Amplitude Scintillations on Low Elevation Earth Space Paths," *Sixth International Conference on Antennas and Propagation (ICAP 89) Part 2: Propagation*, IEE, pp. 150-154 (April 4-7, 1989).
	AR45	Vilar, E. *et al.*, "Experimental System and Measurements of Transhorizon Signal Levels at 11 Ghz," *18th European Microwave Conference*, Microwave Exhibitions and Publishers Ltd., pp. 429-435 (September 12 - 15, 1988).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA46	5,319,799	06/1994	Morita			
	AB46	5,801,654	09/1998	Traylor			
	AC46	5,369,404	11/1994	Galton			
	AD46	3,716,730	02/1973	Cerny, Jr.			
	AE46	4,080,573	03/1978	Howell			
	AF46	4,334,324	06/1982	Hoover			
	AG46	4,369,522	01/1983	Cerny, Jr. *et al.*			
	AH46	5,465,418	11/1995	Zhou *et al.*			
	AI46	5,513,389	04/1996	Reeser *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ46						Yes No
	AK46						Yes No
	AL46						Yes No
	AM46						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN46	Vilar, E. and Matthews, P.A., "Importance of Amplitude Scintillations in Millimetric Radio Links," *Proceedings of the 4th European Microwave Conference*, Microwave Exhibitions and Publishers, pp. 202-206 (September 10-13, 1974).
	AO46	Vilar, E. and Haddon, J., "Measurement and Modeling of Scintillation Intensity to Estimate Turbulence Parameters in an Earth-Space Path," *IEEE Transactions on Antennas and Propagation*, IEEE Antennas and Propagation Society, Vol. AP-32, No. 4, pp. 340-346 (April 1984).
	AP46	Vilar, E. and Matthews, P.A., "Measurement of Phase Fluctuations on Millimetric Radiowave Propagation," *Electronics Letters*, IEE, Vol. 7, No. 18, pp. 566-568 (September 9, 1971).
	AQ46	Vilar, E. and Wan, K.W., "Narrow and Wide Band Estimates of Field Strength for Indoor Communications in the Millimetre Band," *Electronics Division Colloquium on Radiocommunications in the Range 30-60 Ghz*, IEE, pp. 5/1-5/8 (January 17, 1991).
	AR46	Vilar, E. and Faulkner, N.D., "Phase Noise and Frequency Stability Measurements. Numerical Techniques and Limitations," *Electronics Division Colloquium on Low Noise Oscillators and Synthesizer,* IEE, 5 pages (January 23, 1986).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA47	5,959,850	09/1999	Lim			
	AB47	5,157,687	10/1992	Tymes			
	AC47	5,945,660	08/1999	Nakasuji *et al.*			
	AD47	6,091,939	07/2000	Banh			
	AE47	6,091,941	07/2000	Moriyama *et al.*			
	AF47	6,098,886	08/2000	Swift *et al.*			
	AG47	6,215,475 B1	04/2001	Meyerson *et al.*			
	AH47	6,049,706	04/2000	Cook *et al.*			
	AI47	6,061,551	05/2000	Sorrells *et al.*			

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	AJ47						Yes No
	AK47						Yes No
	AL47						Yes No
	AM47						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN47	Vilar, E. and Senin, S., "Propagation phase noise identified using 40 Ghz satellite downlink," *Electronics Letters,* IEE, Vol. 33, No. 22, pp. 1901-1902 (October 23, 1997).
	AO47	Vilar, E. *et al.*, "Scattering and Extinction: Dependence Upon Raindrop Size Distribution in Temperate (Barcelona) and Tropical (Belem) Regions," *Tenth International Conference on Antennas and Propagation,* Electronics Division of the IEE, pp. 2.230-2.233 (April 14-17, 1997).
	AP47	Vilar, E. and Haddon, J., "Scintillation Modeling and Measurement - A Tool for Remote-Sensing Slant Paths," *AGARD Conference Proceedings No. 332: Propagation Aspects of Frequency Sharing, Interference And System Diversity*, AGARD, pp. 27-1 - 27-13 (October 18-22, 1982).
	AQ47	Vilar, E., "Some Limitations on Digital Transmission Through Turbulent Atmosphere," *International Conference on Satellite Communication Systems Technology,* Electronics Division of the IEE, pp. 169-187 (April 7-10, 1975).
	AR47	Vilar, E. and Matthews, P.A., "Summary of Scintillation Observations in a 36 Ghz Link Across London," *International Conference on Antennas and Propagation Part 2: Propagation,* IEE, pp. 36-40 (November 28-30, 1978).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA48	6,061,555	05/2000	Bultman *et al.*			
	AB48	6,091,940	07/2000	Sorrells *et al.*			
	AC48	6,266,518 B1	07/2001	Sorrells *et al.*			
	AD48	6,353,735 B1	03/2002	Sorrells *et al.*			
	AE48	6,370,371 B1	04/2002	Sorrells *et al.*			
	AF48	5,628,055	05/1997	Stein			
	AG48	5,678,220	10/1997	Fournier			
	AH48	5,926,065	07/1999	Wakai *et al.*			
	AI48	3,622,885	11/1971	Oberdorf *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ48						Yes No
	AK48						Yes No
	AL48						Yes No
	AM48						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN48	Vilar, E. *et al.*, "Wideband Characterization of Scattering Channels," *Tenth International Conference on Antennas and Propagation*, Electronics Division of the IEE, pp. 2.353-2.358 (April 14-17, 1997).
	AO48	Vollmer, A., "Complete GPS Receiver Fits on Two Chips," *Electronic Design*, Penton Publishing, pp. 50, 52, 54 and 56 (July 6, 1998).
	AP48	*Voltage and Time Resolution in Digitizing Oscilloscopes: Application Note 348*, Hewlett Packard, pp. 1-11 (November 1986).
	AQ48	Wan, K.W. *et al.*, "A Novel Approach to the Simultaneous Measurement of Phase and Amplitude Noises in Oscillator," *Proceedings of the 19th European Microwave Conference*, Microwave Exhibitions and Publishers Ltd., pp. 809-813 (September 4-7, 1989).
	AR48	Wan, K.W. *et al.*, "Extended Variances and Autoregressive/Moving Average Algorithm for the Measurement and Synthesis of Oscillator Phase Noise," *Proceedings Of the 43rd Annual Symposium on Frequency Control*, IEEE, pp. 331-335 (1989).

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	AA49	4,483,017	11/1984	Hampel *et al.*			
	AB49	6,421,534 B1	07/2002	Cook *et al.*			
	AC49	6,330,244 B1	12/2001	Swartz *et al.*			
	AD49	4,384,357	05/1983	deBuda *et al.*			
	AE49	4,470,145	09/1984	Williams			
	AF49	5,600,680	02/1997	Mishima *et al.*			
	AG49	5,606,731	02/1997	Pace *et al.*			
	AH49	5,870,670	02/1999	Ripley *et al.*			
	AI49	6,314,279 B1	11/2001	Mohindra			

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	AJ49						Yes No
	AK49						Yes No
	AL49						Yes No
	AM49						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN49	Wan, K.W. *et al.*, "Wideband Transhorizon Channel Sounder at 11 Ghz," *Electronics Division Colloquium on High Bit Rate UHF/SHF Channel Sounders - Technology and Measurement*, IEE, pp. 3/1-3/5 (December 3, 1993).
	AO49	Wang, H., "A 1-V Multigigahertz RF Mixer Core in 0.5 - μm CMOS," *IEEE Journal of Solid-State Circuits*, IEEE Solid-State Circuits Society, Vol. 33, No. 12, pp. 2265-2267 (December 1998).
	AP49	Watson, A.W.D. *et al.*, "Digital Conversion and Signal Processing for High Performance Communications Receivers," *Digital Processing of Signals in Communications*, Institution of Electronic and Radio Engineers, pp. 367-373 (April 22nd -26th, 1985).
	AQ49	Weast, R.C. *et al.* (Ed.), *Handbook of Mathematical Tables*, Second Edition, The Chemical Rubber Co., pp. 480-485 (1964).
	AR49	Wiley, R.G., "Approximate FM Demodulation Using Zero Crossings," *IEEE Transactions on Communications*, IEEE, Vol. COM-29, No. 7, pp. 1061-1065 (July 1981).

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	AA50	5,633,815	05/1997	Young			
	AB50	3,246,084	04/1966	Kryter			
	AC50	3,702,440	11/1972	Moore			
	AD50	3,767,984	10/1973	Shinoda *et al.*			
	AE50	3,852,530	12/1974	Shen			
	AF50	4,220,977	09/1980	Yamanaka			
	AG50	5,016,242	05/1991	Tang			
	AH50	5,937,013	08/1999	Lam *et al.*			
	AI50	6,014,551	01/2000	Pesola *et al.*			

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	AJ50						Yes No
	AK50						Yes No
	AL50						Yes No
	AM50						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN50	Worthman, W., "Convergence... Again," *RF Design*, Primedia, p. 102 (March 1999).
	AO50	Young, I.A. and Hodges, D.A., "MOS Switched-Capacitor Analog Sampled-Data Direct-Form Recursive Filters," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-14, No. 6, pp. 1020-1033 (December 1979).
	AP50	Translation of Specification and Claims of FR Patent No. 2245130, 3 pages (April 18, 1975- Date of publication of application).
	AQ50	Fest, Jean-Pierre, "Le Convertisseur A/N Revolutionne Le Recepteur Radio," *Electronique*, JMJ (Publisher), No. 54, pp. 40-42 (December 1995).
	AR50	Translation of DE Patent No. 35 41 031 A1, 22 pages (May 22, 1986- Date of publication of application).

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	AA51	6,073,001	06/2000	Sokoler			
	AB51	6,085,073	07/2000	Palermo *et al.*			
	AC51	6,400,963 B1	06/2002	Glöckler *et al.*			
	AD51	6,230,000 B1	05/2001	Tayloe			
	AE51	5,483,695	01/1996	Pardoen			
	AF51	6,542,722 B1	04/2003	Sorrells *et al.*			
	AG51	6,560,301 B1	05/2003	Cook *et al.*			
	AH51	6,098,046	08/2000	Cooper *et al.*			
	AI51	5,564,097	10/1996	Swanke			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ51						Yes No
	AK51						Yes No
	AL51						Yes No
	AM51						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN51	Translation of EP Patent No. 0 732 803 A1, 9 pages (September 18, 1996- Date of publication of application).
	AO51	Fest, Jean-Pierre, "The A/D Converter Revolutionizes the Radio Receiver," *Electronique*, JMJ (Publisher), No. 54, 3 pages (December 1995). (Translation of Doc. AQ50).
	AP51	Translation of German Patent No. DE 197 35 798 C1, 8 pages (July 16, 1998- Date of publication of application).
	AQ51	Miki, S. and Nagahama, R., *Modulation System II*, Common Edition 7, Kyoritsu Publishing Co., Ltd., pp. 146-154 (April 30, 1956).
	AR51	Miki, S. and Nagahama, R., *Modulation System II*, Common Edition 7, Kyoritsu Publishing Co., Ltd., pp. 146-149 (April 30, 1956). (Partial Translation of Doc. AQ51).

EXAMINER	DATE CONSIDERED

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.001000P	APPLICATION NO. 12/349,802
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA52	5,898,912	04/1999	Heck *et al.*			
	AB52	4,660,164	04/1987	Leibowitz			
	AC52	6,580,902 B1	06/2003	Sorrells *et al.*			
	AD52	4,857,928	08/1989	Gailus *et al.*			
	AE52	5,389,839	02/1995	Heck			
	AF52	5,471,665	11/1995	Pace *et al.*			
	AG52	6,327,313 B1	12/2001	Traylor *et al.*			
	AH52	5,751,154	05/1998	Tsugai			
	AI52	5,793,817	08/1998	Wilson			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ52						Yes No
	AK52						Yes No
	AL52						Yes No
	AM52						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN52	Rabiner, L.R. and Gold, B., *Theory And Application Of Digital Signal Processing*, Prentice-Hall, Inc., pp. v-xii and 40-46 (1975).
	AO52	English-language Abstract of Japanese Patent Publication No. 08-032556, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (February 2, 1996 - Date of publication of application).
	AP52	English-language Abstract of Japanese Patent Publication No. 08-139524, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (May 31, 1996 - Date of publication of application).
	AQ52	English-language Abstract of Japanese Patent Publication No. 59-144249, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (August 18, 1984 - Date of publication of application).
	AR52	English-language Abstract of Japanese Patent Publication No. 63-054002, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (March 8, 1988 - Date of publication of application).

EXAMINER	DATE CONSIDERED

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA53	6,225,848 B1	05/2001	Tilley *et al.*			
	AB53	6,313,685 B1	11/2001	Rabii			
	AC53	3,614,627	10/1971	Runyan *et al.*			
	AD53	3,940,697	02/1976	Morgan			
	AE53	4,016,366	04/1977	Kurata			
	AF53	4,045,740	08/1977	Baker			
	AG53	4,115,737	09/1978	Hongu *et al.*			
	AH53	5,710,992	01/1998	Sawada *et al.*			
	AI53	5,790,587	08/1998	Smith *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ53						Yes No
	AK53						Yes No
	AL53						Yes No
	AM53						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN53	English-language Abstract of Japanese Patent Publication No. 06-237276, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (August 23, 1994 - Date of publication of application).
	AO53	English-language Abstract of Japanese Patent Publication No. 08-023359, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (January 23, 1996 - Date of publication of application).
	AP53	Translation of Japanese Patent Publication No. 47-2314, 7 pages (February 4, 1972- Date of publication of application).
	AQ53	Partial Translation of Japanese Patent Publication No. 58-7903, 3 pages (January 17, 1983- Date of publication of application).
	AR53	English-language Abstract of Japanese Patent Publication No. 58-133004, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (August 8, 1993 - Date of publication of application).

EXAMINER	DATE CONSIDERED

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA54	4,740,675	04/1988	Brosnan *et al.*			
	AB54	5,483,600	01/1996	Werrbach			
	AC54	6,011,435	01/2000	Takeyabu *et al.*			
	AD54	6,321,073 B1	11/2001	Luz *et al.*			
	AE54	6,026,286	02/2000	Long			
	AF54	6,178,319 B1	01/2001	Kashima			
	AG54	6,634,555 B1	10/2003	Sorrells *et al.*			
	AH54	3,736,513	05/1973	Wilson			
	AI54	4,488,119	12/1984	Marshall			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ54						Yes No
	AK54						Yes No
	AL54						Yes No
	AM54						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN54	English-language Abstract of Japanese Patent Publication No. 60-058705, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (April 4, 1985 - Date of publication of application).
	AO54	English-language Abstract of Japanese Patent Publication No. 04-123614, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (April 23, 1992 - Date of publication of application).
	AP54	English-language Abstract of Japanese Patent Publication No. 04-127601, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (April 28, 1992 - Date of publication of application).
	AQ54	English-language Abstract of Japanese Patent Publication No. 05-175730, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (July 13, 1993 - Date of publication of application).
	AR54	English-language Abstract of Japanese Patent Publication No. 05-175734, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (July 13, 1993 - Date of publication of application).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA55	4,633,510	12/1986	Suzuki *et al.*			
	AB55	5,369,789	11/1994	Kosugi *et al.*			
	AC55	5,416,449	05/1995	Joshi			
	AD55	5,438,329	08/1995	Gastouniotis *et al.*			
	AE55	6,611,569 B1	08/2003	Schier *et al.*			
	AF55	6,647,250 B1	11/2003	Bultman *et al.*			
	AG55	5,682,099	10/1997	Thompson *et al.*			
	AH55	6,094,084	07/2000	Abou-Allam *et al.*			
	AI55	6,067,329	05/2000	Kato *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ55						Yes No
	AK55						Yes No
	AL55						Yes No
	AM55						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN55	English-language Abstract of Japanese Patent Publication No. 07-154344, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (June 16, 1995 - Date of publication of application).
	AO55	English-language Abstract of Japanese Patent Publication No. 07-307620, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (November 21, 1995 - Date of publication of application).
	AP55	Oppenheim, A.V. and Schafer, R.W., *Digital Signal Processing*, Prentice-Hall, pp. vii-x, 6-35, 45-78, 87-121 and 136-165 (1975).
	AQ55	English-language Abstract of Japanese Patent Publication No. 55-066057, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (May 19, 1980 - Date of publication of application).
	AR55	English-language Abstract of Japanese Patent Publication No. 63-065587, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (March 24, 1988 - Date of publication of application).

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA56	6,516,185 B1	02/2003	MacNally			
	AB56	6,608,647 B1	08/2003	King			
	AC56	6,687,493 B1	02/2004	Sorrells *et al.*			
	AD56	6,694,128 B1	02/2004	Sorrells *et al.*			
	AE56	6,031,217	02/2000	Aswell *et al.*			
	AF56	5,955,992	09/1999	Shattil			
	AG56	5,999,561	12/1999	Naden *et al.*			
	AH56	6,686,879 B2	02/2004	Shattil			
	AI56	6,704,549 B1	03/2004	Sorrells *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ56						Yes No
	AK56						Yes No
	AL56						Yes No
	AM56						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN56	English-language Abstract of Japanese Patent Publication No. 63-153691, from *http://www1.ipdl.jpo.go.jp,* 2 Pages (June 27, 1988 - Date of publication of application).
	AO56	Translation of Japanese Patent Publication No. 60-130203, 3 pages (July 11, 1985- Date of publication of application).
	AP56	Razavi, B., "A 900-MHz/1.8-Ghz CMOS Transmitter for Dual-Band Applications," *Symposium on VLSI Circuits Digest of Technical Papers*, IEEE, pp. 128-131 (1998).
	AQ56	Ritter, G.M., "SDA, A New Solution for Transceivers," *16th European Microwave Conference*, Microwave Exhibitions and Publishers, pp. 729-733 (September 8, 1986).
	AR56	DIALOG File 351 (Derwent WPI) English Language Patent Abstract for FR 2 669 787, 1 page (May 29, 1992- Date of publication of application).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	*DOC. REF.*	*DOCUMENT NUMBER*	*DATE*	*NAME*	*CLASS*	*SUB-CLASS*	*FILING DATE*
	AA57	6,704,558 B1	03/2004	Sorrells *et al.*			
	AB57	5,490,176	02/1996	Peltier			
	AC57	5,970,053	10/1999	Schick *et al.*			
	AD57	6,078,630	06/2000	Prasanna			
	AE57	6,600,911 B1	07/2003	Morishige *et al.*			
	AF57	5,179,731	01/1993	Tränkle *et al.*			
	AG57	5,589,793	12/1996	Kassapian			
	AH57	4,510,467	04/1985	Chang *et al.*			
	AI57	4,772,853	09/1988	Hart			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	*DOC. REF.*	*DOCUMENT NUMBER*	*DATE*	*COUNTRY*	*CLASS*	*SUB-CLASS*	*TRANSLATION*
	AJ57						Yes No
	AK57						Yes No
	AL57						Yes No
	AM57						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	*DOC. REF.*	*CITATION*
	AN57	Akos, D.M. *et al.*, "Direct Bandpass Sampling of Multiple Distinct RF Signals," *IEEE Transactions on Communications*, IEEE, Vol. 47, No. 7, pp. 983-988 (July 1999).
	AO57	Patel, M. *et al.*, "Bandpass Sampling for Software Radio Receivers, and the Effect of Oversampling on Aperture Jitter," *VTC 2002*, IEEE, pp. 1901-1905 (2002).
	AP57	English-language Abstract of Japanese Patent Publication No. 61-030821, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (February 13, 1986- Date of publication of application).
	AQ57	English-language Abstract of Japanese Patent Publication No. 05-327356, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (December 10, 1993 - Date of publication of application).
	AR57	Tayloe, D., "A Low-noise, High-performance Zero IF Quadrature Detector/Preamplifier," *RF Design*, Primedia Business Magazines & Media, Inc., pp. 58, 60, 62 and 69 (March 2003).

EXAMINER	DATE CONSIDERED

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	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA58	4,972,436	11/1990	Halim *et al.*			
	AB58	5,012,245	04/1991	Scott *et al.*			
	AC58	5,422,909	06/1995	Love *et al.*			
	AD58	5,440,311	08/1995	Gallagher *et al.*			
	AE58	5,926,513	07/1999	Suominen *et al.*			
	AF58	5,995,030	11/1999	Cabler			
	AG58	6,047,026	04/2000	Chao *et al.*			
	AH58	6,049,573	04/2000	Song			
	AI58	6,076,015	06/2000	Hartley *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ58						Yes No
	AK58						Yes No
	AL58						Yes No
	AM58						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN58	Dines, J.A.B., "Smart Pixel Optoelectronic Receiver Based on a Charge Sensitive Amplifier Design," *IEEE Journal of Selected Topics in Quantum Electronics*, IEEE, Vol. 2, No. 1, pp. 117-120 (April 1996).
	AO58	Simoni, A. *et al.*, "A Digital Camera for Machine Vision," *20th International Conference on Industrial Electronics, Control and Instrumentation*, IEEE, pp. 879-883 (September 1994).
	AP58	Stewart, R.W. and Pfann, E., "Oversampling and sigma-delta strategies for data conversion," *Electronics & Communication Engineering Journal*, IEEE, pp. 37-47 (February 1998).
	AQ58	Rudell, J.C. *et al.*, "A 1.9-Ghz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 32, No. 12, pp. 2071-2088 (December 1997).
	AR58	English-language Abstract of Japanese Patent Publication No. 09-036664, from *http://www1.ipdl.jpo.go.jp*, 2 Pages (February 7, 1997 - Date of publication of application).

EXAMINER	DATE CONSIDERED

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	*DOC. REF.*	*DOCUMENT NUMBER*	*DATE*	*NAME*	*CLASS*	*SUB-CLASS*	*FILING DATE*
	AA59	6,144,331	11/2000	Jiang			
	AB59	6,018,553	01/2000	Sanielevici *et al.*			
	AC59	6,317,589 B1	11/2001	Nash			
	AD59	5,058,107	10/1991	Stone *et al.*			
	AE59	5,757,858	05/1998	Black *et al.*			
	AF59	6,531,979 B1	03/2003	Hynes			
	AG59	6,018,262	01/2000	Noro *et al.*			
	AH59	4,761,798	08/1988	Griswold, Jr. *et al.*			
	AI59	5,982,315	11/1999	Bazarjani *et al.*			

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EXAMINER INITIAL	*DOC. REF.*	*DOCUMENT NUMBER*	*DATE*	*COUNTRY*	*CLASS*	*SUB-CLASS*	*TRANSLATION*
	AJ59						Yes No
	AK59						Yes No
	AL59						Yes No
	AM59						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	*DOC. REF.*	*CITATION*
	AN59	Simoni, A. *et al.*, "A Single-Chip Optical Sensor with Analog Memory for Motion Detection," *IEEE Journal of Solid-State Circtuits*, IEEE, Vol. 30, No. 7, pp. 800-806 (July 1995).
	AO59	English Translation of German Patent Publication No. DE 196 48 915 A1, 10 pages.
	AP59	Deboo, Gordon J., *Integrated Circuits and Semiconductor Devices*, 2nd Edition, McGraw-Hill, Inc., pp. 41-45 (1977).
	AQ59	Hellwarth, G.A. and Jones, G.D, "Automatic Conditioning of Speech Signals," *IEEE Transactions on Audio and Electroacoustics*, Vol. AU-16, No. 2, pp. 169-179 (June 1968).
	AR59	English Abstract for German Patent No. DE 692 21 098 T2, 1 page, data supplied from the espacenet.

EXAMINER	DATE CONSIDERED

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA60	6,459,721 B1	10/2002	Mochizuki *et al.*			
	AB60	6,151,354	11/2000	Abbey			
	AC60	6,169,733 B1	01/2001	Lee			
	AD60	6,363,262 B1	03/2002	McNicol			
	AE60	6,697,603 B1	02/2004	Lovinggood *et al.*			
	AF60	5,282,222	01/1994	Fattouche *et al.*			
	AG60	5,949,827	09/1999	DeLuca *et al.*			
	AH60	6,014,176	01/2000	Nayebi *et al.*			
	AI60	5,678,226	10/1997	Li *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ60						Yes No
	AK60						Yes No
	AL60						Yes No
	AM60						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN60	Gaudiosi, J., "Retailers will bundle Microsoft's Xbox with games and peripherals," *Video Store Magazine*, Volume 23, Issue 36, pg. 8, 2 pages (September 2-8, 2001).
	AO60	English-language Translation of German Patent Publication No. DT 1936252, translation provided by Transperfect Translations, 12 pages (January 28, 1971 - Date of publication of application).
	AP60	English-language Abstract of Japanese Patent Publication No. JP 62-12381, data supplied by the espacenet, 1 page (January 21, 1987 - Date of publication of application).
	AQ60	English-language Abstract of Japanese Patent Publication No. JP 4-154227, data supplied by the espacenet, 1 page (May 27, 1992 - Date of publication of application).
	AR60	English-language Abstract of Japanese Patent Publication No. JP 6-284038, data supplied by the espacenet, 1 page (October 7, 1994 - Date of publication of application).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA61	5,760,632	06/1998	Kawakami *et al.*			
	AB61	6,160,280	12/2000	Bonn *et al.*			
	AC61	5,481,570	01/1996	Winters			
	AD61	5,745,846	04/1998	Myer *et al.*			
	AE61	5,345,239	09/1994	Madni *et al.*			
	AF61	4,132,952	01/1979	Hongu *et al.*			
	AG61	5,260,973	11/1993	Watanabe			
	AH61	6,307,894 B2	10/2001	Eidson *et al.*			
	AI61	6,091,289	07/2000	Song *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ61						Yes No
	AK61						Yes No
	AL61						Yes No
	AM61						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN61	English-language Abstract of Japanese Patent Publication No. JP 10-96778, data supplied by the espacenet, 1 page (April 14, 1998 - Date of publication of application).
	AO61	English-language Abstract of Japanese Patent Publication No. JP 11-98205, data supplied by the espacenet, 1 page (April 9, 1999 - Date of publication of application).
	AP61	English-language Abstract of Japanese Patent Publication No. JP 61-232706, data supplied by the espacenet, 1 page (October 17, 1986 - Date of publication of application).
	AQ61	English-language Abstract of Japanese Patent Publication No. JP 9-171399, data supplied by the espacenet, 1 page (June 30, 1997 - Date of publication of application).
	AR61	English-language Abstract of Japanese Patent Publication No. JP 10-41860, data supplied by the espacenet, 1 page (February 13, 1998 - Date of publication of application).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA62	6,437,639 B1	08/2002	Nguyen *et al.*			
	AB62	2002/0037706 A1	03/2002	Ichihara			
	AC62	4,441,080	04/1984	Saari			
	AD62	4,873,492	10/1989	Myer			
	AE62	5,697,074	12/1997	Makikallio *et al.*			
	AF62	5,784,689	07/1998	Kobayashi			
	AG62	6,335,656 B1	01/2002	Goldfarb *et al.*			
	AH62	6,690,232 B2	02/2004	Ueno *et al.*			
	AI62	5,636,140	06/1997	Lee *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ62						Yes No
	AK62						Yes No
	AL62						Yes No
	AM62						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN62	English-language Computer Translation of Japanese Patent Publication No. JP 10-41860, provided by the JPO (June 26, 1998 - Date of publication of application) and cited in U.S. Patent Application Ser. No. 10/305,299, directed to related subject matter.
	AO62	*What is I/Q Data?*, printed September 16, 2006, from http://zone.ni.com, 8 pages (Copyright 2003).
	AP62	English-language Abstract of Japanese Patent Publication No. JP 58-031622, data supplied by ep.espacenet.com, 1 page (Feb. 24, 1983 - Date of publication of application).
	AQ62	English-language Abstract of Japanese Patent Publication No. JP 61-245749, data supplied by ep.espacenet.com, 1 page (Nov. 1, 1986 - Date of publication of application).
	AR62	English-language Abstract of Japanese Patent Publication No. JP 64-048557, data supplied by ep.espacenet.com, 1 page (Feb. 23, 1989 - Date of publication of application).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.001000P	APPLICATION NO. 12/349,802
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA63	6,366,622 B1	04/2002	Brown *et al.*			
	AB63	6,600,795 B1	07/2003	Ohta *et al.*			
	AC63	4,250,458	02/1981	Richmond *et al.*			
	AD63	5,760,629	06/1998	Urabe *et al.*			
	AE63	6,084,465	07/2000	Dasqupta			
	AF63	6,204,789 B1	03/2001	Nagata			
	AG63	6,064,054	05/2000	Waczynski *et al.*			
	AH63	5,218,562	06/1993	Basehore *et al.*			
	AI63	5,239,496	08/1993	Vancraeynest			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ63						Yes No
	AK63						Yes No
	AL63						Yes No
	AM63						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN63	English-language Abstract of Japanese Patent Publication No. JP 59-022438, data supplied by ep.espacenet.com, 1 page (Feb. 4, 1984 - Date of publication of application).
	AO63	English-language Abstract of Japanese Patent Publication No. JP 59-123318, data supplied by ep.espacenet.com, 1 page (July 17, 1984 - Date of publication of application).
	AP63	English-language Abstract of Japanese Patent Publication No. JP 61-193521, data supplied by ep.espacenet.com, 1 page (Aug. 28, 1986 - Date of publication of application).
	AQ63	English-language Abstract of Japanese Patent Publication No. JP 62-047214, data supplied by ep.espacenet.com, 1 page (Feb. 28, 1987 - Date of publication of application).
	AR63	English-language Abstract of Japanese Patent Publication No. JP 63-274214, data supplied by ep.espacenet.com, 1 page (Nov. 11, 1988 - Date of publication of application).

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	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA64	5,896,304	04/1999	Tiemann *et al.*			
	AB64	6,005,903	12/1999	Mendelovicz			
	AC64	5,834,979	11/1998	Yatsuka			
	AD64	6,798,351 B1	09/2004	Sorrells *et al.*			
	AE64	6,813,485 B2	11/2004	Sorrells *et al.*			
	AF64	5,410,270	04/1995	Rybicki *et al.*			
	AG64	6,509,777 B2	01/2003	Razavi *et al.*			
	AH64	5,982,329	11/1999	Pittman *et al.*			
	AI64	6,208,636 B1	03/2001	Tawil *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ64						Yes No
	AK64						Yes No
	AL64						Yes No
	AM64						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN64	English-language Abstract of Japanese Patent Publication No. JP 7-169292, data supplied by ep.espacenet.com, 1 page (July 4, 1995 - Date of publication of application).
	AO64	English-language Abstract of Japanese Patent Publication No. JP 10-22804, data supplied by ep.espacenet.com, 1 page (January 23, 1998 - Date of publication of application).
	AP64	English-language Abstract of Japanese Patent Publication No. JP 8-288882, data supplied by ep.espacenet.com, 1 page (November 1, 1996 - Date of publication of application).
	AQ64	
	AR64	

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA65	3,614,630	10/1971	Rorden			
	AB65	6,836,650 B2	12/2004	Sorrells *et al.*			
	AC65	5,844,868	12/1998	Takahashi *et al.*			
	AD65	6,385,439 B1	05/2002	Hellberg			
	AE65	6,741,139 B2	05/2004	Pleasant *et al.*			
	AF65	6,823,178 B2	11/2004	Pleasant *et al.*			
	AG65	6,850,742 B2	02/2005	Fayyaz			
	AH65	6,853,690 B1	02/2005	Sorrells *et al.*			
	AI65	4,789,837	12/1988	Ridgers			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ65						Yes No
	AK65						Yes No
	AL65						Yes No
	AM65						Yes No

NON PATENT LITERATURE DOCUMENTS

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA66	5,634,207	05/1997	Yamaji *et al.*			
	AB66	5,642,071	06/1997	Sevenhans *et al.*			
	AC66	6,211,718 B1	04/2001	Souetinov			
	AD66	6,212,369 B1	04/2001	Avasarala			
	AE66	6,308,058 B1	10/2001	Souetinov *et al.*			
	AF66	6,633,194 B2	10/2003	Arnborg *et al.*			
	AG66	2001/0036818 A1	11/2001	Dobrovolny			
	AH66	6,873,836 B1	03/2005	Sorrells *et al.*			
	AI66	6,879,817 B1	04/2005	Sorrells *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ66						Yes No
	AK66						Yes No
	AL66						Yes No
	AM66						Yes No

NON PATENT LITERATURE DOCUMENTS

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA67	6,057,714	05/2000	Andrys *et al.*			
	AB67	2003/0081781 A1	05/2003	Jensen *et al.*			
	AC67	5,994,689	11/1999	Charrier			
	AD67	6,512,544 B1	01/2003	Merrill *et al.*			
	AE67	6,628,328 B1	09/2003	Yokouchi *et al.*			
	AF67	6,801,253 B1	10/2004	Yonemoto *et al.*			
	AG67	3,737,778	06/1973	Van Gerwen *et al.*			
	AH67	4,286,283	08/1981	Clemens			
	AI67	4,241,451	12/1980	Maixner *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ67						Yes No
	AK67						Yes No
	AL67						Yes No
	AM67						Yes No

NON PATENT LITERATURE DOCUMENTS

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA68	5,014,130	05/1991	Heister *et al.*			
	AB68	5,390,215	02/1995	Anita *et al.*			
	AC68	5,805,460	09/1998	Greene *et al.*			
	AD68	6,882,194 B2	04/2005	Belot *et al.*			
	AE68	6,892,062 B2	05/2005	Lee *et al.*			
	AF68	6,917,796 B2	07/2005	Setty *et al.*			
	AG68	6,920,311 B2	07/2005	Rofougaran *et al.*			
	AH68	5,062,122	10/1991	Pham *et al.*			
	AI68	6,182,011 B1	01/2001	Ward			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ68						Yes No
	AK68						Yes No
	AL68						Yes No
	AM68						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN68	
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	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA69	6,639,939 B1	10/2003	Naden *et al.*			
	AB69	5,787,125	07/1998	Mittel			
	AC69	5,878,088	03/1999	Knutson *et al.*			
	AD69	6,215,828	04/2001	Signell *et al.*			
	AE69	5,703,584	12/1997	Hill			
	AF69	5,887,001	03/1999	Russell			
	AG69	6,298,065 B1	10/2001	Dombkowski *et al.*			
	AH69	2002/0080728 A1	06/2002	Sugar *et al.*			
	AI69	2002/0163921 A1	11/2002	Ethridge *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ69						Yes No
	AK69						Yes No
	AL69						Yes No
	AM69						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN69	
	AO69	
	AP69	
	AQ69	
	AR69	

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	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA70	6,963,734 B2	11/2005	Sorrells *et al.*			
	AB70	6,005,506	12/1999	Bazarjani *et al.*			
	AC70	6,438,366 B1	08/2002	Lindfors *et al.*			
	AD70	5,196,806	03/1993	Ichihara			
	AE70	5,410,195	04/1995	Ichihara			
	AF70	6,404,823 B1	06/2002	Grange *et al.*			
	AG70	6,618,579 B1	09/2003	Smith *et al.*			
	AH70	2001/0015673 A1	08/2001	Yamashita *et al.*			
	AI70	2003/0045263 A1	03/2003	Wakayama *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ70						Yes No
	AK70						Yes No
	AL70						Yes No
	AM70						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN70	
	AO70	
	AP70	
	AQ70	
	AR70	

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	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA71	6,975,848 B2	12/2005	Rawlins *et al.*			
	AB71	6,404,758 B1	06/2002	Wang			
	AC71	6,909,739 B1	06/2005	Eerola *et al.*			
	AD71	6,910,015 B2	06/2005	Kawai			
	AE71	3,719,903	03/1973	Goodson			
	AF71	4,591,930	05/1986	Baumeister			
	AG71	7,006,805 B1	02/2006	Sorrells *et al.*			
	AH71	7,010,286 B2	03/2006	Sorrells *et al.*			
	AI71	7,010,559 B2	03/2006	Rawlins *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ71						Yes No
	AK71						Yes No
	AL71						Yes No
	AM71						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN71	
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	AP71	
	AQ71	
	AR71	

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA72	5,131,014	07/1992	White			
	AB72	6,393,070 B1	05/2002	Reber			
	AC72	7,016,663 B2	03/2006	Sorrells *et al.*			
	AD72	3,694,754	09/1972	Baltzer			
	AE72	4,931,716	06/1990	Jovanovic *et al.*			
	AF72	3,617,898	11/1971	Janning, Jr.			
	AG72	3,764,921	10/1973	Huard			
	AH72	4,158,149	06/1979	Otofuji			
	AI72	4,380,828	04/1983	Moon			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ72						Yes No
	AK72						Yes No
	AL72						Yes No
	AM72						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN72	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA73	4,562,414	12/1985	Linder *et al.*			
	AB73	4,814,649	03/1989	Young			
	AC73	4,845,389	07/1989	Pyndiah *et al.*			
	AD73	5,172,019	12/1992	Naylor *et al.*			
	AE73	5,263,198	11/1993	Geddes *et al.*			
	AF73	5,551,076	08/1996	Bonn			
	AG73	5,633,610	05/1997	Maekawa *et al.*			
	AH73	7,027,786 B1	04/2006	Smith *et al.*			
	AI73	7,039,372 B1	05/2006	Sorrells *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ73						Yes No
	AK73						Yes No
	AL73						Yes No
	AM73						Yes No

NON PATENT LITERATURE DOCUMENTS

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	AN73	
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	AR73	

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA74	6,591,310 B1	07/2003	Johnson			
	AB74	6,963,626 B1	11/2005	Shaeffer *et al.*			
	AC74	4,811,422	03/1989	Kahn			
	AD74	5,825,257	10/1998	Klymyshyn *et al.*			
	AE74	5,986,600	11/1999	McEwan			
	AF74	6,865,399 B2	03/2005	Fujioka *et al.*			
	AG74	2006/0039449 A1	02/2006	Fontana *et al.*			
	AH74	5,847,594	12/1998	Mizuno			
	AI74	7,050,508 B2	05/2006	Sorrells *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ74						Yes No
	AK74						Yes No
	AL74						Yes No
	AM74						Yes No

NON PATENT LITERATURE DOCUMENTS

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA75	7,054,296 B1	05/2006	Sorrells *et al.*			
	AB75	7,065,162 B1	06/2006	Sorrells *et al.*			
	AC75	2003/0149579 A1	08/2003	Begemann *et al.*			
	AD75	5,063,387	11/1991	Mower			
	AE75	5,535,402	07/1996	Leibowitz *et al.*			
	AF75	6,512,785 B1	01/2003	Zhou *et al.*			
	AG75	6,567,483 B1	05/2003	Dent *et al.*			
	AH75	6,775,684 B1	08/2004	Toyoyama *et al.*			
	AI75	4,740,792	04/1988	Sagey *et al.*			

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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ75						Yes No
	AK75						Yes No
	AL75						Yes No
	AM75						Yes No

NON PATENT LITERATURE DOCUMENTS

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	AA76	5,239,687	08/1993	Chen			
	AB76	5,552,789	09/1996	Schuermann			
	AC76	5,905,433	05/1999	Wortham			
	AD76	6,647,270 B1	11/2003	Himmelstein			
	AE76	6,034,566	03/2000	Ohe			
	AF76	6,313,700 B1	11/2001	Nishijima *et al.*			
	AG76	6,959,178 B2	10/2005	Macedo *et al.*			
	AH76	6,999,747 B2	02/2006	Su			
	AI76	2004/0125879 A1	07/2004	Jaussi *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ76						Yes No
	AK76						Yes No
	AL76						Yes No
	AM76						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN76	
	AO76	
	AP76	
	AQ76	
	AR76	

EXAMINER	DATE CONSIDERED

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FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
1744.001000P	12/349,802
FIRST NAMED INVENTOR	
David F. SORRELLS	
FILING DATE	ART UNIT
January 7, 2009	2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA77	7,072,390 B1	07/2006	Sorrells *et al.*			
	AB77	7,072,427 B2	07/2006	Rawlins *et al.*			
	AC77	7,076,011 B2	07/2006	Cook *et al.*			
	AD77	7,082,171 B1	07/2006	Johnson *et al.*			
	AE77	7,085,335 B2	08/2006	Rawlins *et al.*			
	AF77	3,739,282	06/1973	Bruch *et al.*			
	AG77	4,439,787	03/1984	Mogi *et al.*			
	AH77	4,866,441	09/1989	Conway *et al.*			
	AI77	4,885,671	12/1989	Peil			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ77						Yes No
	AK77						Yes No
	AL77						Yes No
	AM77						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN77	
	AO77	
	AP77	
	AQ77	
	AR77	

EXAMINER	DATE CONSIDERED

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.001000P	APPLICATION NO. 12/349,802
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA78	5,164,985	11/1992	Nysen *et al.*			
	AB78	5,734,683	03/1998	Hulkko *et al.*			
	AC78	5,918,167	06/1999	Tiller *et al.*			
	AD78	6,445,726 B1	09/2002	Gharpurey			
	AE78	6,560,451 B1	05/2003	Somayajula			
	AF78	4,143,322	03/1979	Shimamura			
	AG78	2,530,824	11/1950	King			
	AH78	7,107,028 B2	09/2006	Sorrells *et al.*			
	AI78	7,110,435 B1	09/2006	Sorrells *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ78						Yes No
	AK78						Yes No
	AL78						Yes No
	AM78						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN78	
	AO78	
	AP78	
	AQ78	
	AR78	

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.001000P	APPLICATION NO. 12/349,802
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA79	7,110,444 B1	09/2006	Sorrells *et al.*			
	AB79	6,973,476 B1	12/2005	Naden *et al.*			
	AC79	5,834,987	11/1998	Dent			
	AD79	RE37,138 E	04/2001	Dent			
	AE79	6,441,694 B1	08/2002	Turcotte *et al.*			
	AF79	6,892,057 B2	05/2005	Nilsson			
	AG79	6,741,650 B1	05/2004	Painchaud *et al.*			
	AH79	2002/0132642 A1	09/2002	Hines *et al.*			
	AI79	5,884,154	03/1999	Sano *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ79						Yes No
	AK79						Yes No
	AL79						Yes No
	AM79						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN79	
	AO79	
	AP79	
	AQ79	
	AR79	

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	FIRST NAMED INVENTOR David F. SORRELLS	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA80	5,900,746	05/1999	Sheahan			
	AB80	6,246,695 B1	06/2001	Seazholtz *et al.*			
	AC80	6,597,240 B1	07/2003	Walburger *et al.*			
	AD80	7,190,941 B2	03/2007	Sorrells *et al.*			
	AE80	7,194,246 B2	03/2007	Sorrells *et al.*			
	AF80	7,209,725 B1	04/2007	Sorrells *et al.*			
	AG80	7,218,899 B2	05/2007	Sorrells *et al.*			
	AH80	7,218,907 B2	05/2007	Sorrells *et al.*			
	AI80	7,224,749 B2	05/2007	Sorrells *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ80						Yes No
	AK80						Yes No
	AL80						Yes No
	AM80						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN80	
	AO80	
	AP80	
	AQ80	
	AR80	

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	FIRST NAMED INVENTOR David F. SORRELLS	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA81	7,233,969 B2	06/2007	Rawlins *et al.*			
	AB81	7,236,754 B2	06/2007	Sorrells *et al.*			
	AC81	7,245,886 B2	07/2007	Sorrells *et al.*			
	AD81	7,194,044 B2	03/2007	Birkett *et al.*			
	AE81	7,212,581 B2	05/2007	Birkett *et al.*			
	AF81	4,485,347	11/1984	Hirasawa *et al.*			
	AG81	5,724,041	03/1998	Inoue *et al.*			
	AH81	2003/0193364 A1	10/2003	Liu *et al.*			
	AI81	4,771,265	09/1988	Okui *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ81						Yes No
	AK81						Yes No
	AL81						Yes No
	AM81						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN81	
	AO81	
	AP81	
	AQ81	
	AR81	

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	FIRST NAMED INVENTOR David F. SORRELLS	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA82	5,006,854	04/1991	White *et al.*			
	AB82	3,643,168	02/1972	Manicki			
	AC82	4,048,598	09/1977	Knight			
	AD82	4,145,659	03/1979	Wolfram			
	AE82	4,313,222	01/1982	Katthän			
	AF82	5,896,347	04/1999	Tomita *et al.*			
	AG82	6,259,293 B1	07/2001	Hayase *et al.*			
	AH82	7,272,164 B2	09/2007	Sorrells *et al.*			
	AI82	7,292,835 B2	11/2007	Sorrells *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ82						Yes No
	AK82						Yes No
	AL82						Yes No
	AM82						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN82	
	AO82	
	AP82	
	AQ82	
	AR82	

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA83	7,295,826 B1	11/2007	Cook *et al.*			
	AB83	6,112,061	08/2000	Rapeli			
	AC83	6,625,470 B1	09/2003	Fourtet *et al.*			
	AD83	6,813,320 B1	11/2004	Claxton *et al.*			
	AE83	2002/0021685 A1	02/2002	Sakusabe			
	AF83	2003/0078011 A1	04/2003	Cheng *et al.*			
	AG83	7,308,242 B2	12/2007	Sorrells *et al.*			
	AH83	7,321,640 B2	01/2008	Milne *et al.*			
	AI83	7,321,735 B1	01/2008	Smith *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ83						Yes No
	AK83						Yes No
	AL83						Yes No
	AM83						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN83	
	AO83	
	AP83	
	AQ83	
	AR83	

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	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA84	7,321,751 B2	01/2008	Sorrells *et al.*			
	AB84	2006/0002491 A1	01/2006	Darabi *et al.*			
	AC84	4,663,744	05/1987	Russell *et al.*			
	AD84	5,559,809	09/1996	Jeon *et al.*			
	AE84	6,038,265	03/2000	Pan *et al.*			
	AF84	6,876,846 B2	04/2005	Tamaki *et al.*			
	AG84	6,512,798 B1	01/2003	Akiyama *et al.*			
	AH84	6,072,996	06/2000	Smith			
	AI84	6,088,348	06/2000	Bell, III *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ84						Yes No
	AK84						Yes No
	AL84						Yes No
	AM84						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN84	
	AO84	
	AP84	
	AQ84	
	AR84	

EXAMINER	DATE CONSIDERED

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.001000P	APPLICATION NO. 12/349,802
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA85	6,198,941 B1	03/2001	Aho *et al.*			
	AB85	6,894,988 B1	05/2005	Zehavi			
	AC85	7,193,965 B1	03/2007	Nevo *et al.*			
	AD85	4,688,237	08/1987	Brault			
	AE85	5,461,646	10/1995	Anvari			
	AF85	5,483,245	01/1996	Ruinet			
	AG85	7,197,081 B2	03/2007	Saito			
	AH85	7,376,410 B2	05/2008	Sorrells *et al.*			
	AI85	7,379,515 B2	05/2008	Johnson *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ85						Yes No
	AK85						Yes No
	AL85						Yes No
	AM85						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN85	
	AO85	
	AP85	
	AQ85	
	AR85	

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1744.001000P	APPLICATION NO. 12/349,802
	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA86	7,379,883 B2	05/2008	Sorrells			
	AB86	7,386,292 B2	06/2008	Sorrells *et al.*			
	AC86	7,389,100 B2	06/2008	Sorrells *et al.*			
	AD86	4,651,210	03/1987	Olson			
	AE86	5,659,372	08/1997	Patel *et al.*			
	AF86	6,097,762	08/2000	Suzuki *et al.*			
	AG86	5,512,946	04/1996	Murata *et al.*			
	AH86	3,809,821	05/1974	Melvin			
	AI86	6,275,542	08/2001	Katayama *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ86						Yes No
	AK86						Yes No
	AL86						Yes No
	AM86						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN86	
	AO86	
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	AQ86	
	AR86	

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	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA87	2006/0209599 A1	09/2006	Kato *et al.*			
	AB87	5,339,395	08/1994	Pickett *et al.*			
	AC87	6,128,746	10/2000	Clark *et al.*			
	AD87	6,137,321	10/2000	Bazarjani			
	AE87	5,909,460	06/1999	Dent			
	AF87	6,546,061 B2	04/2003	Signell *et al.*			
	AG87	4,004,237	01/1977	Kratzer			
	AH87	4,363,976	12/1982	Minor			
	AI87	4,393,352	07/1983	Volpe *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ87						Yes No
	AK87						Yes No
	AL87						Yes No
	AM87						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN87	
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	AP87	
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	AR87	

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	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA88	4,405,835	09/1983	Jansen *et al.*			
	AB88	4,463,320	07/1984	Dawson			
	AC88	4,596,046	06/1986	Richardson *et al.*			
	AD88	6,167,247	12/2000	Kannell *et al.*			
	AE88	6,223,061 B1	04/2001	Dacus *et al.*			
	AF88	6,366,765 B1	04/2002	Hongo *et al.*			
	AG88	6,731,146 B1	05/2004	Gallardo			
	AH88	6,738,609 B1	05/2004	Clifford			
	AI88	7,149,487 B2	12/2006	Yoshizawa			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ88						Yes No
	AK88						Yes No
	AL88						Yes No
	AM88						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN88	
	AO88	
	AP88	
	AQ88	
	AR88	

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	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA89	7,358,801 B2	04/2008	Perdoor *et al.*			
	AB89	5,781,600	07/1998	Reeve *et al.*			
	AC89	5,973,570	10/1999	Salvi *et al.*			
	AD89	6,690,741 B1	02/2004	Larrick, Jr. *et al.*			
	AE89	7,433,910 B2	10/2008	Rawlins *et al.*			
	AF89	7,454,453 B2	11/2008	Rawlins *et al.*			
	AG89	7,460,584 B2	12/2008	Parker *et al.*			
	AH89	4,173,164	11/1979	Adachi *et al.*			
	AI89	4,409,877	10/1983	Budelman			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ89						Yes No
	AK89						Yes No
	AL89						Yes No
	AM89						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN89	
	AO89	
	AP89	
	AQ89	
	AR89	

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA90	6,195,539	02/2001	Galal *et al.*			
	AB90	4,571,738	02/1986	Vance			
	AC90	5,982,810	11/1999	Nishimori			
	AD90	2002/0098823 A1	07/2002	Lindfors *et al.*			
	AE90	4,968,958	11/1990	Hoare			
	AF90	7,483,686 B2	01/2009	Sorrells *et al.*			
	AG90	7,496,342 B2	02/2009	Sorrells *et al.*			
	AH90	7,515,896 B1	04/2009	Sorrells *et al.*			
	AI90	7,529,522 B2	05/2009	Sorrells *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ90						Yes No
	AK90						Yes No
	AL90						Yes No
	AM90						Yes No

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL	DOC. REF.	CITATION
	AN90	
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	AP90	
	AQ90	
	AR90	

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	FIRST NAMED INVENTOR David F. SORRELLS	
	FILING DATE January 7, 2009	ART UNIT 2617

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA91	7,539,474 B2	05/2009	Sorrells *et al.*			
	AB91	7,546,096 B2	06/2009	Sorrells *et al.*			
	AC91	7,554,508 B2	06/2009	Johnson *et al.*			
	AD91	6,192,225 B1	02/2001	Arpaia *et al.*			
	AE91	7,599,421 B2	10/2009	Sorrells *et al.*			
	AF91	5,757,864	05/1998	Petranovich *et al.*			
	AG91	5,559,468	09/1996	Gailus *et al.*			
	AH91	6,829,311 B1	12/2004	Riley			
	AI91	7,620,378 B2	11/2009	Sorrells *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ91						Yes No
	AK91						Yes No
	AL91						Yes No
	AM91						Yes No

NON PATENT LITERATURE DOCUMENTS

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	AN91	
	AO91	
	AP91	
	AQ91	
	AR91	

EXAMINER	DATE CONSIDERED

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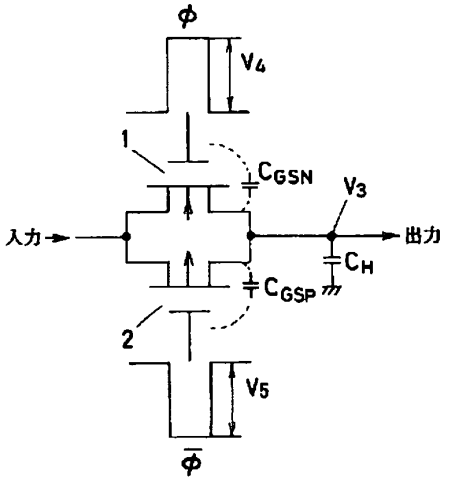
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(54)【発明の名称】　ＣＭＯＳサンプルホールド回路

(57)【要約】

【目的】　クロックリークを除去し、高Ｓ／Ｎを実現する。

【構成】　Ｎ型ＭＯＳＦＥＴ１の非飽和領域のゲート・ソース間容量C_{GSN}とホールド容量C_Hの和に対するＮ型ＭＯＳＦＥＴ１の非飽和領域のゲート・ソース間容量C_{GSN}の比C_{GSN}／（C_{GSN}＋C_H）とＮ型ＭＯＳＦＥＴ１のゲート・ソース間電圧V_{GSN}とＮ型ＭＯＳＦＥＴ１のしきい値電圧V_{TN}の差（V_{GSN}－V_{TN}）との積〔C_{GSN}／（C_{GSN}＋C_H）〕×（V_{GSN}－V_{TN}）と、Ｐ型ＭＯＳＦＥＴ２の非飽和領域のゲート・ソース間容量C_{GSP}とホールド容量C_Hの和に対するＰ型ＭＯＳＦＥＴ２の非飽和領域のゲート・ソース間容量C_{GSP}の比C_{GSP}／（C_{GSP}＋C_H）とＰ型ＭＯＳＦＥＴ２のゲート・ソース間電圧V_{GSP}とＰ型ＭＯＳＦＥＴ２のしきい値電圧V_{TP}の差（V_{GSP}－V_{TP}）との積〔C_{GSP}／（C_{GSP}＋C_H）〕×（V_{GSP}－V_{TP}）とを等しく設定する。



1　Ｎ型ＭＯＳＦＥＴ
2　Ｐ型ＭＯＳＦＥＴ
C_{GSN}　ゲート・ソース間容量
C_{GSP}　ゲート・ソース間容量
C_H　ホールド容量

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【特許請求の範囲】

【請求項1】　ドレインどうしおよびソースどうしをそれぞれ共通接続したN型MOSFETおよびP型MOSFETからなるアナログスイッチと、前記N型MOSFETおよびP型MOSFETの共通ソースに接続したホールド容量とからなるCMOSサンプルホールド回路であって、

前記N型MOSFETの非飽和領域のゲート・ソース間容量C_{GSN}と前記ホールド容量C_Hの和（$C_{GSN}+C_H$）に対する前記N型MOSFETの非飽和領域のゲート・ソース間容量C_{GSN}の比$C_{GSN}/(C_{GSN}+C_H)$と前記N型MOSFETのゲート・ソース間電圧V_{GSN}と前記N型MOSFETのしきい値電圧V_{TN}の差（$V_{GSN}-V_{TN}$）との積〔$C_{GSN}/(C_{GSN}+C_H)$〕×（$V_{GSN}-V_{TN}$）と、

前記P型MOSFETの非飽和領域のゲート・ソース間容量C_{GSP}と前記ホールド容量C_Hの和（$C_{GSP}+C_H$）に対する前記P型MOSFETの非飽和領域のゲート・ソース間容量C_{GSP}の比$C_{GSP}/(C_{GSP}+C_H)$と前記P型MOSFETのゲート・ソース間電圧V_{GSP}と前記P型MOSFETのしきい値電圧V_{TP}の差（$V_{GSP}-V_{TP}$）との積〔$C_{GSP}/(C_{GSP}+C_H)$〕×（$V_{GSP}-V_{TP}$）とを等しく設定したことを特徴とするCMOSサンプルホールド回路。

【発明の詳細な説明】

【0001】

【産業上の利用分野】この発明は、アナログ信号のサンプルホールドに用いることができるCMOSサンプルホールド回路に関するものである。

【0002】

【従来の技術】映像信号などのアナログ信号をサンプルホールドするサンプルホールド回路は、デジタル信号処理の重要性が増す中、より高精度、高速、高S／Nのものが要求されている。高S／Nを達成するには、サンプルホールドされた信号にリークするサンプリングパルスすなわちクロックパルスを最小限にする必要がある。

【0003】以下、従来のCMOSサンプルホールド回路について図2および図3を参照しながら説明する。図2は従来のCMOSサンプルホールド回路の構成を示すものであり、図3はMOSFETのゲート容量の動作点依存性を示すものである。図2において、3はN型MOSFETで、C_{GN}はN型MOSFET3のゲート容量である。4はP型MOSFETで、C_{GP}はP型MOSFET4のゲート容量であり、それぞれドレインどうし、ソースどうしが共通接続されている。C_HはN型MOSFET3およびP型MOSFET4の共通ソースに接続したホールド容量である。

【0004】φはN型MOSFET3のゲート入力パルス、／φ（／φはφの反転信号を表す）はP型MOSFET4のゲート入力パルスであり、これらは同振幅逆位

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相のパルスである。さらに、CMOSアナログスイッチを構成するN型MOSFET3とP型MOSFET4の各ゲート面積は等しく構成されている。

【0005】図3において、C_{OX}はゲート面積およびゲート酸化膜厚で決定される容量、すなわち（ゲート酸化膜の誘電率）×（ゲート面積）÷（ゲート酸化膜厚）である。C_{OL}はソースまたはドレインを形成する拡散層とゲートのオーバーラップ面積およびゲート酸化膜厚で決定される容量、すなわち（ゲート酸化膜の誘電率）×（ソースまたはドレインを形成する拡散層とゲートのオーバーラップ面積）÷ゲート酸化膜厚である。C_{GB}，C_{GS}，C_{GD}は、各々ゲート・基板間容量、ゲート・ソース間容量、ゲート・ドレイン間容量である。

【0006】以上のように構成された従来のCMOSサンプルホールド回路について、以下その動作を説明する。まず、従来のクロックパルスリークについての考え方を説明する。クロックパルスリークは、〔数1〕に示すように、ゲートに印加されるサンプリングパルス（ゲート入力パルス）φと、アナログスイッチに用いるMOSFETのゲート容量C_Gとホールド容量C_Hの容量比で決定されると考えている。さらに、MOSFETのゲート容量C_Gはゲート面積とゲート酸化膜厚で決定される、すなわち図3のC_{OX}であると考えている。

【0007】

【数1】

$$\text{クロックパルスリーク}=\frac{C_G}{C_G+C_H}\cdot\phi$$

【0008】したがって、CMOSアナログスイッチを構成するとき、N型MOSFET3での〔数1〕で表されるクロックパルスリークとP型MOSFET4での〔数1〕で表されるクロックパルスリークが同振幅逆位相、すなわち〔数2〕の関係を満たせば、クロックパルスリークが相殺されると考え、CMOSアナログスイッチを構成するN型MOSFET3とP型MOSFET4の各ゲート面積を等しくしている。

【0009】

【数2】

$$\frac{C_{OX}}{C_{OX}+C_H}\cdot\phi=\frac{C_{OX}}{C_{OX}+C_H}\cdot\phi$$

【0010】

【発明が解決しようとする課題】このような従来のCMOSサンプルホールド回路では、MOSFETのゲート容量C_Gがゲート酸化膜厚やMOSFETの寸法のみで決定されると考えており、図3に示すようなMOSFETのゲート容量C_Gの動作点依存性を考慮していなかったのでクロックパルスリークの除去が不十分であり、高S／Nを達成するには、クロック成分を除去することが必要で、このためにフィルタや、ダミーのサンプルホー

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ルド回路と差動アンプも必要であるという問題があった。

【0011】この発明は上記課題を解決するもので、クロックパルスリークを十分に除去でき高S／Nを達成できるCMOSサンプルホールド回路提供することを目的としている。

【0012】

【課題を解決するための手段】この発明のCMOSサンプルホールド回路は、ドレインどうしおよびソースどうしをそれぞれ共通接続したN型MOSFETおよびP型MOSFETからなるアナログスイッチと、N型MOSFETおよびP型MOSFETの共通ソースに接続したホールド容量とからなる。

【0013】そして、N型MOSFETの非飽和領域のゲート・ソース間容量C_{GSN}とホールド容量C_Hの和（$C_{GSN}+C_H$）に対するN型MOSFETの非飽和領域のゲート・ソース間容量C_{GSN}の比C_{GSN}／（$C_{GSN}+C_H$）とN型MOSFETのゲート・ソース間電圧V_{GSN}とN型MOSFETのしきい値電圧V_{TN}の差（$V_{GSN}-V_{TN}$）との積〔C_{GSN}／（$C_{GSN}+C_H$）〕×（$V_{GSN}-V_{TN}$）と、P型MOSFETの非飽和領域のゲート・ソース間容量C_{GSP}とホールド容量C_Hの和（$C_{GSP}+C_H$）に対するP型MOSFETの非飽和領域のゲート・ソース間容量C_{GSP}の比C_{GSP}／（$C_{GSP}+C_H$）とP型MOSFETのゲート・ソース間電圧V_{GSP}とP型MOSFETのしきい値電圧V_{TP}の差（$V_{GSP}-V_{TP}$）との積〔C_{GSP}／（$C_{GSP}+C_H$）〕×（$V_{GSP}-V_{TP}$）とを等しく設定している。

【0014】

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＊【作用】この発明の構成によれば、MOSFETのゲート・ソース間容量の動作点依存性を考慮することにより、N型MOSFETのクロック成分のリークとP型MOSFETのクロック成分のリークとをちょうどキャンセルすることができて、クロック成分の除去を十分に行うことができる。したがって、フィルタや、ダミーのサンプルホールド回路と差動アンプも必要とせずにサンプルホールドされた信号へのクロックパルスリークを除去でき、IC化に最適化である。

【0015】

【実施例】以下、この発明の一実施例について図1を参照しながら説明する。図1は、この発明の一実施例のCMOSサンプルホールド回路の構成を示すものである。図1において、1はゲート幅またはゲート長が〔数3〕を満足する、しきい値電圧V_{TN}のN型MOSFETであり、C_{GSN}はN型MOSFET1の非飽和動作領域におけるゲート・ソース間容量である。2はゲート幅またはゲート長が〔数3〕を満足する、しきい値電圧V_{TP}のP型MOSFETで、C_{GSP}はP型MOSFET2の非飽和動作領域におけるゲート・ソース間容量である。C_Hはホールド容量である。V_Sはホールド電位であり、N型MOSFET1およびP型MOSFET2のソース電位となる。ϕは振幅がV_4であるN型MOSFET1のゲート入力パルスであり、／ϕは振幅がV_5であり位相がゲート入力パルスϕと反転したP型MOSFET2のゲート入力パルスである。

【0016】

【数3】

＊

$$\frac{C_{GSN}}{C_{GSN}+C_H}\cdot(V_4-V_S-V_{TN})=\frac{C_{GSP}}{C_{GSP}+C_H}\cdot(V_S-V_S-V_{TP})$$

【0017】以上のように構成されたこの実施例のCMOSサンプルホールド回路について、以下その動作を説明する。まず、この発明の原理となるクロックパルスリークについての考え方を説明する。CMOSサンプルホールド回路のアナログスイッチに用いるMOSFETは、ゲートにパルスが印加されてオン状態にあるときは、非飽和動作領域で作用している。

【0018】したがって、MOSFETの非飽和動作領域におけるゲート・ソース間容量をC_{GS}、ゲート・ソース間電圧をV_{GS}、しきい値電圧をV_T、またホールド容量をC_Hとすると、クロックパルスリークは〔数4〕となる。

【0019】

※【数4】

$$\text{クロックパルスリーク}=\frac{C_{GS}}{C_{GS}+C_H}\cdot(V_{GS}-V_T)$$

【0020】したがって、CMOSアナログスイッチを構成するとき、N型MOSFET1での〔数4〕で表されるクロックパルスリークとP型MOSFET2での〔数4〕で表されるクロックパルスリークが同振幅逆位相、すなわち〔数5〕の関係を満たせば、クロックパルスリークが相殺される。

【0021】

【数5】

※

$$\frac{C_{GSN}}{C_{GSN}+C_H}\cdot(V_{GSN}-V_{TN})=\frac{C_{GSP}}{C_{GSP}+C_H}\cdot(V_{GSP}-V_{TP})$$

【0022】なお、〔数5〕において、V_{GSN}はN型MOSFET1のゲート・ソース間電圧で（V_4-V_S）に等しい。V_{GSP}はP型MOSFET2のゲート・ソース間電圧で、（V_5-V_S）に等しい。この実施例のC

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MOSサンプルホールド回路においては、CMOSアナログスイッチを構成するN型MOSFET1およびP型MOSFET2の各々ゲート幅またはゲート長が〔数3〕すなわち〔数5〕を満たすので、クロックパルスリークはちょうど相殺される。

【0023】

【発明の効果】この発明のCMOSサンプルホールド回路によれば、N型MOSFETの非飽和領域のゲート・ソース間容量C_{GSN}とホールド容量C_Hの和（$C_{GSN}+C_H$）に対するN型MOSFETの非飽和領域のゲート・ソース間容量C_{GSN}の比$C_{GSN}/(C_{GSN}+C_H)$とN型MOSFETのゲート・ソース間電圧V_{GSN}とN型MOSFETのしきい値電圧V_{TN}の差（$V_{GSN}-V_{TN}$）との積$[C_{GSN}/(C_{GSN}+C_H)]\times(V_{GSN}-V_{TN})$と、P型MOSFETの非飽和領域のゲート・ソース間容量C_{GSP}とホールド容量C_Hの和（$C_{GSP}+C_H$）に対するP型MOSFETの非飽和領域のゲート・ソース間容量C_{GSP}の比$C_{GSP}/(C_{GSP}+C_H)$とP型MOSFETのゲート・ソース間電圧V_{GSP}とP型MOSFETのしきい値電圧V_{TP}の差（$V_{GSP}-V_{TP}$）と

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の積$[C_{GSP}/(C_{GSP}+C_H)]\times(V_{GSP}-V_{TP})$とを等しく設定しているので、クロック成分を除去するために、フィルタや、ダミーのサンプルホールド回路と差動アンプも必要とせずにサンプルホールドされた信号へのクロックパルスリークを十分に除去でき、高S／Nを実現でき、IC化に最適化である。

【図面の簡単な説明】

【図1】この発明の一実施例のCMOSサンプルホールド回路の回路図である。

【図2】従来のCMOSサンプルホールド回路の回路図である。

【図3】MOSFETのゲート容量の動作点依存性を示す特性図である。

【符号の説明】

1　N型MOSFET

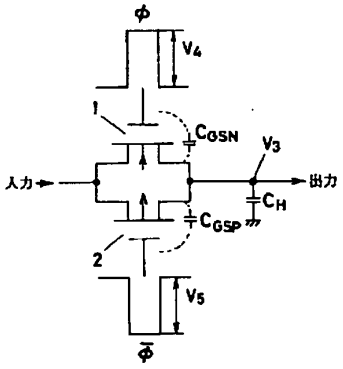
2　P型MOSFET

C_{GSN}　ゲート・ソース間容量

C_{GSP}　ゲート・ソース間容量

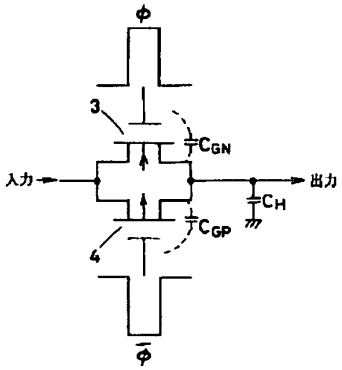
C_H　ホールド容量

【図1】

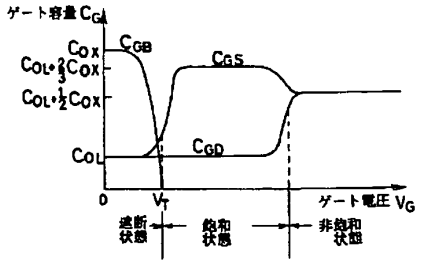


1　N型MOSFET
2　P型MOSFET
C_{GSN}　ゲート・ソース間容量
C_{GSP}　ゲート・ソース間容量
C_H　ホールド容量

【図2】



【図3】



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Ｇ０１Ｒ　15/00			Ｇ０１Ｒ　15/00		

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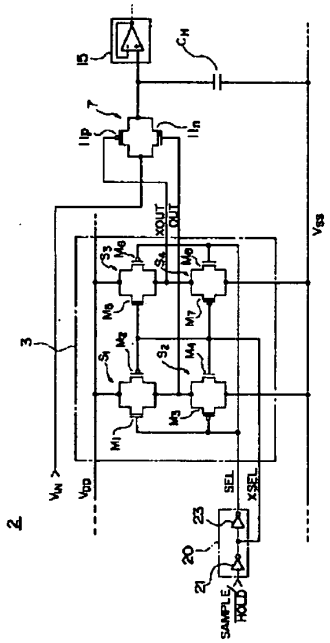
(74)代理人　弁理士　石島　茂男　（外１名）

(54)【発明の名称】　波形整形回路、及びその波形整形回路を有するサンプルホールド回路

(57)【要約】

【課題】　ホールド容量に誤差を生じさせない波形整形回路を提供する。

【解決手段】　ロー又はハイの状態の一方を示す第1の状態と、第1の状態とは反対の論理状態を示す第2の論理状態のうち、定常状態ではいずれか一方の論理状態で安定したXSEL信号と、該XSEL信号とは反対の論理状態で安定したSEL信号とが入力され、SEL信号の示す論理状態をOUT信号として出力し、XSEL信号の示す論理状態をXOUT信号として出力するように構成された波形整形回路3に対し、XSEL信号が論理反転を開始し、次いでSEL信号が論理反転を開始する過渡状態の際、XSEL信号の論理反転開始を検出してOUT信号の論理状態とXOUT信号の論理状態とを変化させ始め、次いでSEL信号の論理反転開始を検出してOUT信号の論理状態とXOUT信号の論理状態とを更に変化させる。OUT信号の論理反転とXOUT信号の論理反転とが同時に開始し、同時に完了するので、ホールド容量C_Hの電圧に誤差が生じない。



【特許請求の範囲】
【請求項１】　ロー又はハイの論理状態のいずれか一方を示す第１の論理状態と、その第１の論理状態とは反対の論理状態を示す第２の論理状態のうち、定常状態では前記第１の論理状態又は前記第２の論理状態のいずれか一方の論理状態で安定したＸＳＥＬ信号と、該ＸＳＥＬ信号とは反対の論理状態で安定したＳＥＬ信号とが入力され、
前記ＳＥＬ信号の示す論理状態をＯＵＴ信号として出力し、前記ＸＳＥＬ信号の示す論理状態をＸＯＵＴ信号として出力するように構成された波形整形回路であって、
前記ＸＳＥＬ信号が第１の論理状態から第２の論理状態への論理反転を開始し、次いで前記ＳＥＬ信号が第２の論理状態から第１の論理状態への論理反転を開始する過渡状態の際、
前記ＸＳＥＬ信号の論理反転開始を検出して前記ＯＵＴ信号の論理状態と前記ＸＯＵＴ信号の論理状態とを変化させ始め、次いで前記ＳＥＬ信号の論理反転開始を検出して前記ＯＵＴ信号の論理状態と前記ＸＯＵＴ信号の論理状態とを更に変化させ、前記ＯＵＴ信号の論理反転と前記ＸＯＵＴ信号の論理反転とを完了させるように構成されたことを特徴とする波形整形回路。
【請求項２】　前記ＸＳＥＬ信号が第２の論理状態から第１の論理状態への論理反転を開始し、次いで前記ＳＥＬ信号が第１の論理状態から第２の論理状態への論理反転を開始する過渡状態の際、
前記ＸＳＥＬ信号の論理反転開始を検出して前記ＯＵＴ信号の論理状態と前記ＸＯＵＴ信号の論理状態とを変化させ始め、次いで前記ＳＥＬ信号の論理反転開始を検出して前記ＯＵＴ信号の論理状態と前記ＸＯＵＴ信号の論理状態とを更に変化させ、前記ＯＵＴ信号の論理反転と前記ＸＯＵＴ信号の論理反転とを完了させるように構成されたことを特徴とする請求項１記載の波形整形回路。
【請求項３】　ホールド容量と、
ｎチャネルＭＯＳＦＥＴとｐチャネルＭＯＳＦＥＴとが並列接続されたアナログスイッチと、
請求項１又は請求項２のいずれか１項記載の波形整形回路とを有するサンプルホールド回路において、
前記ＳＥＬ信号は前記ＸＳＥＬ信号がインバーターで反転されて作られ、
前記アナログスイッチは、定常状態では前記ＸＯＵＴ信号の論理状態と前記ＯＵＴ信号の論理状態に応じて導通状態と遮断(非導通)状態とに置かれるように構成され、
前記ホールド容量は、前記アナログスイッチが導通状態に置かれたときにサンプリングすべき電圧で充放電され、前記アナログスイッチが遮断状態に置かれたときに電圧が維持されるように構成されたことを特徴とするサンプルホールド回路。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明はサンプルホールド回路の技術分野にかかり、特に、サンプル・ホールド信号から作られた互いに相補の論理状態を示す信号を整形する波形整形回路と、その波形整形回路が用いられるサンプルホールド回路に関する。
【０００２】
【従来の技術】一般に、サンプルホールド回路はＡ・Ｄコンバーター等の変換装置の入力段に設けられており、所定のタイミングで入力電圧をサンプリングし、変換装置が変換し終わるまでサンプリングした電圧を保持する回路である。そのようなサンプルホールド回路の従来技術のものを図４(ａ)の符号１０２に示す。
【０００３】このサンプルホールド回路１０２は、ホールド容量１０６と、アナログスイッチ１０７と、スイッチ制御回路１２０と、出力回路１１５とを有しており、アナログスイッチ１０７が導通状態になったときに、サンプリング電圧V_{IN}でホールド容量１０６を充放電し、次いで、アナログスイッチ１０７が遮断状態になったときに、ホールド容量１０６に蓄積された電荷を保持し、出力回路１１５によってホールド容量１０６のホールド電圧を、次段の回路へ出力するように構成されている。
【０００４】このような動作はサンプル・ホールド信号の指示によって行われており、そのサンプル・ホールド信号は、スイッチ制御回路１２０が有するインバーター１２１に入力されている。
【０００５】インバーター１２１は、入力されたサンプル・ホールド信号を反転し、ＸＯＵＴ信号として出力しており、そのＸＯＵＴ信号は、アナログスイッチ１０７とインバーター１２３とに出力され、該インバーター１２３で再度反転され、ＯＵＴ信号としてアナログスイッチ１０７に出力されている。
【０００６】アナログスイッチ１０７は、ｐチャネルＭＯＳＦＥＴ111_pとｎチャネルＭＯＳＦＥＴ111_nとが並列接続されて構成されており、ＸＯＵＴ信号はｐチャネルＭＯＳＦＥＴ111_pのゲート端子に入力され、ＯＵＴ信号はｎチャネルＭＯＳＦＥＴ111_nのゲート端子に入力されている。
【０００７】ＯＵＴ信号はインバーター１２３によってＸＯＵＴ信号が反転されて作られているため、定常状態ではＸＯＵＴ信号の論理状態とＯＵＴ信号の論理状態とは、互いに反対(相補)の論理状態を示している。また、ＸＯＵＴ信号はインバーター１２１によってサンプル・ホールド信号を反転して作られているため、サンプル・ホールド信号がハイ状態のときは、ＸＯＵＴ信号はロー状態、ＯＵＴ信号はハイ状態となる。従って、サンプル・ホールド信号がハイ状態では、ｐチャネルＭＯＳＦＥＴ111_p及びｎチャネルＭＯＳＦＥＴ111_nはＯＮし、アナログスイッチ１０７は導通状態となる。他方、サンプル・ホールド信号がロー状態のときは、ＸＯＵＴ信号はハイ状態、ＯＵＴ信号はロー状態となり、ｐチャ

ネルMOSFET111_p及びnチャネルMOSFET111_nは共にOFFとなり、アナログスイッチ107は非導通状態となる。

【0008】このように、サンプル・ホールド信号の状態をハイ状態(サンプル)とロー状態(ホールド)とに制御すると、pチャネルMOSFET111_p及びnチャネルMOSFET111_nがON／OFFし、アナログスイッチ107の導通状態と遮断(非導通)状態とを切換えることができるので、ホールド容量106の充放電と電圧の維持を行うことができる。

【0009】前述のXOUT信号及びOUT信号のハイ状態は電源の高電位側の電圧V_{DD}のレベルであり、他方、ロー状態は電源の低電位側の電圧V_{SS}のレベルである($V_{DD}>V_{SS}$)。一般に、MOSFETがONするためには、ソース・ゲート間にスレッショルド電圧(しきい値)以上の電圧が印加する必要がある。このアナログスイッチ107のpチャネルMOSFET111_pとnチャネルMOSFET111_nでは、入力電圧V_{IN}に応じてソース電位が変動するため、ソース・ゲート間の電圧がスレッショルド電圧Vth(p)、Vth(n)より小さい場合にはONすることができない。pチャネルMOSFET111_pの出力電圧は、図4(b)に示す符号V_pの範囲となり、nチャネルMOSFET111_nの出力電圧は、符号V_nの範囲となる。

【0010】従って、サンプル電圧V_{IN}がV_{DD}に近い場合は、pチャネルMOSFET111_qのみによってサンプリングされ、V_{SS}に近い場合はnチャネルMOSFET111_nのみによってサンプリングされることになる。このように、pチャネルMOSFET111_pとnチャネルMOSFET111_nとを並列接続することによって互いの出力電圧V_n、V_pの範囲を補完し合い、電圧V_{SS}～V_{DD}の範囲をサンプリングできるように構成されている。

【0011】このようなアナログスイッチ107を導通状態から遮断状態に移行させるため、サンプル・ホールド信号がハイ状態からロー状態に反転すると、先ず、XOUT信号がロー状態(電圧V_{SS})からハイ状態(電圧V_{DD})に論理反転するため、nチャネルMOSFET111_nよりも先にpチャネルMOSFET111_pがOFFする。このとき、pチャネルMOSFET111_pのゲート端子とドレイン端子との間に形成されている寄生容量112_pが放電(充電)される。

【0012】この寄生容量112_pが放電(充電)されるときは、まだnチャネルMOSFET111_nがONしているため、寄生容量の放電(充電)に伴う電流はnチャネルMOSFET111_nを通って流れ、ホールド電圧に変化はない。

【0013】次いで、インバーター123の動作時間だけ遅れてOUT信号がハイ状態からロー状態に論理反転し、nチャネルMOSFET111_nがOFFする。このとき、nチャネルMOSFET111_nのゲート端子とソース端子との間に形成された寄生容量112_nが放電(充電)される。nチャネルMOSFET111_nがOFFするときは、pチャネルMOSFET111_pは既にOFFしているため、寄生容量112_nが放電(充電)される際の電流iはホールド容量106に流れることとなり、ホールド容量106の電圧を変化させてしまう。上述のように、pチャネルMOSFETが先にOFFする場合には、ホールド電圧の値はサンプリング電圧V_{IN}よりも低くなってしまい、ホールド電圧に誤差を生じてしまう原因になっていた。

【0014】このような誤差電圧は、電源電圧V_{DD}、V_{SS}の大きさが変わるとその値も変わるため、補正することができない。そのため、従来は、寄生容量と比較して大きなキャパシタンスのホールド容量を用いて電圧誤差を小さくしていたが、ホールド容量をチップ上に設ける場合にはチップ面積の増大を招いており、その解決が望まれていた。

【0015】

【発明が解決しようとする課題】本発明は上記従来技術の不都合を解決するために創作されたもので、その目的は、サンプリングしたホールド電圧に誤差を生じない波形整形回路、及びその波形整形回路を用いたサンプルホールド回路を提供することにある。

【0016】

【課題を解決するための手段】上記課題を解決するために、請求項1記載の発明は、ロー又はハイの論理状態のいずれか一方を示す第1の論理状態と、その第1の論理状態とは反対の論理状態を示す第2の論理状態のうち、定常状態では前記第1の論理状態又は前記第2の論理状態のいずれか一方の論理状態で安定したXSEL信号と、該XSEL信号とは反対の論理状態で安定したSEL信号とが入力され、前記SEL信号の示す論理状態をOUT信号として出力し、前記XSEL信号の示す論理状態をXOUT信号として出力するように構成された波形整形回路であって、前記XSEL信号が第1の論理状態から第2の論理状態への論理反転を開始し、次いで前記SEL信号が第2の論理状態から第1の論理状態への論理反転を開始する過渡状態の際、前記XSEL信号の論理反転開始を検出して前記OUT信号の論理状態と前記XOUT信号の論理状態とを変化させ始め、次いで前記SEL信号の論理反転開始を検出して前記OUT信号の論理状態と前記XOUT信号の論理状態とを更に変化させ、前記OUT信号の論理反転と前記XOUT信号の論理反転とを完了させるように構成されたことを特徴とする。

【0017】また、請求項2記載の発明は、請求項1記載の波形整形回路であって、前記XSEL信号が第2の論理状態から第1の論理状態への論理反転を開始し、次いで前記SEL信号が第1の論理状態から第2の論理状

態への論理反転を開始する過渡状態の際、前記ＸＳＥＬ信号の論理反転開始を検出して前記ＯＵＴ信号の論理状態と前記ＸＯＵＴ信号の論理状態とを変化させ始め、次いで前記ＳＥＬ信号の論理反転開始を検出して前記ＯＵＴ信号の論理状態と前記ＸＯＵＴ信号の論理状態とを更に変化させ、前記ＯＵＴ信号の論理反転と前記ＸＯＵＴ信号の論理反転とを完了させるように構成されたことを特徴とする。

【００１８】他方、請求項３記載の発明は、ホールド容量と、ｎチャネルＭＯＳＦＥＴとｐチャネルＭＯＳＦＥＴとが並列接続されたアナログスイッチと、請求項１又は請求項２のいずれか１項記載の波形整形回路とを有するサンプルホールド回路であて、前記ＳＥＬ信号は前記ＸＳＥＬ信号がインバーターで反転されて作られ、前記アナログスイッチは、定常状態では前記ＸＯＵＴ信号の論理状態と前記ＯＵＴ信号の論理状態に応じて導通状態と遮断(非導通)状態とに置かれるように構成され、前記ホールド容量は、前記アナログスイッチが導通状態に置かれたときにサンプリングすべき電圧で充放電され、前記アナログスイッチが遮断状態に置かれたときに電圧が維持されるように構成されたことを特徴とする。

【００１９】上述した本発明の波形整形回路には、ロー又はハイの論理状態のいずれか一方を示す第１の論理状態と、その第１の論理状態とは反対の論理状態を示す第２の論理状態のうち、定常状態では第１の論理状態又は第２の論理状態のいずれか一方の論理状態で安定したＸＳＥＬ信号と、該ＸＳＥＬ信号とは反対の論理状態で安定したＳＥＬ信号とが入力され、ＳＥＬ信号の示す論理状態をＯＵＴ信号として出力し、ＸＳＥＬ信号の示す論理状態をＸＯＵＴ信号として出力するように構成されているが、ＸＳＥＬ信号が第１の論理状態から第２の論理状態への論理反転を開始し、次いでＳＥＬ信号が第２の論理状態から第１の論理状態への論理反転を開始する過渡状態の際、先ず、ＸＳＥＬ信号の論理反転開始を検出してＯＵＴ信号の論理状態とＸＯＵＴ信号の論理状態とを変化させ始め、次いで、ＳＥＬ信号の論理反転開始を検出してＯＵＴ信号の論理状態とＸＯＵＴ信号の論理状態とを更に変化させるので、ＯＵＴ信号の論理反転とＸＯＵＴ信号の論理反転が同時に開始され、同時に完了する。

【００２０】このように同時に変化するＯＵＴ信号とＸＯＵＴ信号とをアナログスイッチのｎチャネルＭＯＳＦＥＴとｐチャネルＭＯＳＦＥＴとに入力させ、そのｎチャネルＭＯＳＦＥＴとｐチャネルＭＯＳＦＥＴを同時にＯＦＦさせれば、互いの寄生容量に流れる電流が打ち消し合い、アナログスイッチに接続されたホールド容量のホールド電圧に誤差を生じさせずに済む。

【００２１】この場合、ＸＳＥＬ信号が第２の論理状態から第１の論理状態への論理反転を開始し、次いでＳＥＬ信号が第１の論理状態から第２の論理状態への論理反転を開始する過渡状態の際、先ず、ＸＳＥＬ信号の論理反転開始を検出してＯＵＴ信号の論理状態とＸＯＵＴ信号の論理状態とを変化させ始め、次いで、ＳＥＬ信号の論理反転開始を検出してＯＵＴ信号の論理状態とＸＯＵＴ信号の論理状態とを更に変化させるようにすれば、ＯＵＴ信号の第１の論理状態から第２の論理状態への論理反転と、ＸＯＵＴ信号の第２の論理状態から第１の論理状態への論理反転とが同時に開始され、同時に完了するので、前述のアナログスイッチのｎチャネルＭＯＳＦＥＴとｐチャネルＭＯＳＦＥＴとを同時にＯＮさせることができる。

【００２２】

【発明の実施の形態】本発明の実施の形態を図面を用いて説明する。図１を参照し、符号２は本発明の一例のサンプルホールド回路であり、このサンプルホールド回路２は、スイッチ制御回路２０と、アナログスイッチ７と、出力回路１５と、ホールド容量C_Hと、本発明の一例の波形整形回路３とを有している。

【００２３】このサンプルホールド回路２にはサンプル動作とホールド動作とのいずれか一方を指示するサンプル・ホールド信号が入力されており、そのサンプル・ホールド信号がハイ状態(電圧がV_{DD})のときにサンプル電圧V_{IN}でホールド容量C_Hを充放電し(サンプル動作)、ロー状態(電圧がV_{SS})のときにホールド容量C_Hに現れるホールド電圧を維持する(ホールド動作)ように構成されており、その動作内容をサンプルホールド回路２の構成と共に説明する。

【００２４】スイッチ制御回路２０は、インバーター２１、２３がこの順で直列接続されて構成されており、前段のインバーター２１には前述のサンプル・ホールド信号が入力され、該インバーター２１によって反転された信号がＸＳＥＬ信号として出力されている。そのＸＳＥＬ信号は、波形整形回路３に入力されると共に後段のインバーター２３にも入力されており、該インバーター２３によって反転された信号がＳＥＬ信号として出力され、波形整形回路３に入力されている。

【００２５】波形整形回路３は、スイッチS_1～スイッチS_4を有しており、スイッチS_1とスイッチS_2とが、電源の高電位側の電圧V_{DD}が印加される配線と低電位側の電圧V_{SS}が印加される配線との間でこの順に直列接続されており、また、同様に、スイッチS_3とスイッチS_4とが電圧V_{DD}が印加される配線と電圧V_{SS}が印加される配線との間で、この順に直列接続されて構成されている。

【００２６】スイッチS_1～S_4は、ｎチャネルＭＯＳＦＥＴ(M_1)、(M_4)、(M_5)、(M_8)とｐチャネルＭＯＳＦＥＴ(M_2)、(M_3)、(M_6)、(M_7)とをそれぞれ１個ずつ有しており、各ｎチャネルＭＯＳＦＥＴ(M_1)、(M_4)、(M_5)、(M_8)のドレイン端子とソース端子とが、ｐチャネルＭＯＳＦＥＴ(M_2)、(M_3)、(M_6)、(M_7)のソース

端子とドレイン端子とにそれぞれ接続され、各スイッチS_1～S_4は、2個のMOSFETが並列接続されて構成されている。

【0027】スイッチS_1、S_4のnチャネルMOSFET(M_1)、(M_8)のゲート端子と、スイッチS_2、S_3のpチャネルMOSFET(M_3)、(M_6)のゲート端子には、SEL信号が入力されており、他方、スイッチS_1、S_4のpチャネルMOSFET(M_2)、(M_7)のゲート端子と、スイッチS_2、S_3のnチャネルMOSFET(M_4)、(M_5)のゲート端子にはXSEL信号が入力されており、SEL信号がハイ状態、XSEL信号がロー状態のときに、スイッチS_1、S_4がON、スイッチS_2、S_3がOFFとなり、SEL信号とXSEL信号との論理状態がそれとは反対のときに、スイッチS_2、S_3がON、スイッチS_1、S_4がOFFとなるように構成されている。

【0028】従って、SEL信号の論理状態とXSEL信号の論理状態とが互いに反対になる定常状態では、同時にONするのはスイッチS_1とスイッチS_4の組か、スイッチS_2とスイッチS_3の組のいずれか一方である。

【0029】そして、スイッチS_1とスイッチS_2との接続中点からはOUT信号が取り出され、スイッチS_3とスイッチS_4とが接続されたところからはXOUT信号が取り出されているので、スイッチS_1とスイッチS_4の組がONのときはOUT信号がハイ状態、XOUT信号がロー状態となり、スイッチS_2とスイッチS_3の組がONのときはOUT信号がロー状態、XOUT信号がハイ状態となり、定常状態ではOUT信号とXOUT信号とは互いに反対の論理状態になるように構成されている。

【0030】アナログスイッチ7は、pチャネルMOSFET11_pとnチャネルMOSFET11_nとが互いのソース端子とドレイン端子とが接続されて並列接続に構成されており、nチャネルMOSFET11_nのゲート端子にはOUT信号が入力され、pチャネルMOSFET11_pのゲート端子にはXOUT信号が入力されている。

【0031】従って、このアナログスイッチ7では、XOUT信号がロー状態、OUT信号がハイ状態のときにpチャネルMOSFET11_pとnチャネルMOSFET11_nとが共にONしてアナログスイッチ全体として導通状態となり、サンプル電圧V_{IN}でホールド容量C_Hを充放電する。他方、XOUT信号がハイ状態、OUT信号がロー状態のときはpチャネルMOSFET11_pとnチャネルMOSFET11_nは共にOFFして遮断状態となり、ホールド容量C_Hに現れるホールド電圧の値を維持し、高入力インピーダンスの出力回路15を介してそのホールドした電圧を外部回路に出力できるように構成されている。

【0032】いま、サンプル・ホールド信号が、ハイ状態(サンプル動作)で安定しているものとする。サンプル信号がハイ状態で安定している場合、XSEL信号は第1の論理状態であるロー状態、SEL信号は第2の論理状態であるハイ状態で安定しており、この場合には、スイッチS_1、S_4がON、スイッチS_2、S_3がOFFとなり、OUT信号がSEL信号の示すハイ状態を出力し、XOUT信号がXSEL信号の示すロー状態を出力している。

【0033】従って、nチャネルMOSFET11_nとpチャネルMOSFET11_pとは共にONし、アナログスイッチ7は導通状態にあるので、サンプル容量C_Hの電圧はサンプル電圧V_{IN}と同電位になっており、ホールド電圧はサンプル電圧V_{IN}と等しくなっている。

【0034】その状態からサンプル・ホールド信号がロー状態(ホールド動作)に切り替わると、先ず、インバーター21によってXSEL信号のロー状態からハイ状態への論理反転が開始され、次いでインバーター23の遅延時間だけ遅れてSEL信号のハイ状態からロー状態への論理反転が開始される。

【0035】そのときのSEL信号とXSEL信号の波形の一例を図2に示す。この図2はシミュレーション結果であり、XSEL信号は時間軸(横軸)の21n(ナノ)秒付近、SEL信号は24n(ナノ)秒付近で変化し始めており、SEL信号の論理反転の開始はXSEL信号の論理反転の開始よりも3n(ナノ)秒遅れている。

【0036】このようなSEL信号とXSEL信号とが入力される波形整形回路3の各MOSFET(M_1)～(M_8)は、一つのシリコン基板に形成されており、各pチャネルMOSFET(M_2)、(M_3)、(M_6)、(M_7)のバックゲートには最も高い電圧V_{DD}が印加され、また、各nチャネルMOSFET(M_1)、(M_4)、(M_5)、(M_8)のバックゲートには最も低い電圧V_{SS}が印加されている。

【0037】また、各MOSFET(M_1)～(M_8)は駆動能力が等しくなるように形成されており、具体的には、ソース・ドレイン間に同じ電圧が印加され、且つ、ソース・ゲート間に同じ電圧が印加されて動作条件が等しい場合には、同じ大きさのドレイン電流が流れるように設計されている。

【0038】定常状態に於いて、スイッチS_1、S_4がON、スイッチS_2、S_3がOFFの状態で安定している場合には、nチャネルMOSFET(M_4)、(M_5)のドレイン端子には電圧V_{DD}が印加され、ソース端子には電圧V_{SS}が印加されているので、nチャネルMOSFET(M_4)、(M_5)の動作条件は同じであり、XSEL信号の変化によってnチャネルMOSFET(M_4)、(M_5)のソース・ゲート間の電圧がスレッショルド電圧以上になったときに、そのnチャネルMOSFET(M_4)、(M_5)は同時にONし始める。

【0039】nチャネルMOSFET(M_4)、(M_5)が同時にONするとOUT信号の論理状態とXOUT信号の論理状態とが同時に変化し始め、その後、SEL信号の

電圧が変化し始める。

【0040】OUT信号とXOUT信号とが変化し始めた頃は、pチャネルMOSFET(M_3)のソース・ドレイン間の電圧と、pチャネルMOSFET(M_6)のソース・ドレイン間の電圧はほぼ等しく、この2つのpチャネルMOSFET(M_3)、(M_6)の動作条件はほぼ同じである。SEL信号の変化により、pチャネルMOSFET(M_3)、(M_6)のソース・ゲート間の電圧がスレッショルド電圧以上になると、そのpチャネルMOSFET(M_3)、(M_6)がほぼ同時にONし始める。

【0041】pチャネルMOSFET(M_3)、(M_6)がONすると、nチャネルMOSFET(M_4)によって電圧が下げられ始めていたOUT信号の電圧が更に下げられる。また、それと同時に、nチャネルMOSFET(M_5)によって電圧が上げられ始めていたXOUT信号の電圧が更に上げられる。

【0042】その状態からXSEL信号の電圧が更に上昇すると、先ず、スイッチS_1とスイッチS_4のpチャネルMOSFET(M_2)、(M_7)がOFFし、OUT信号の電圧を下げ、それと同時にXOUT信号の電圧を上げる。

【0043】次いで、SEL信号の電圧が下がり、スイッチS_1とスイッチS_4のnチャネルMOSFET(M_1)、(M_8)がOFFし、OUT信号の電圧を更に下げ、それと同時にXOUT信号の電圧を更に上げる。かくてOUT信号とXOUT信号の反転は完了する。

【0044】このようなOUT信号とXOUT信号の変化のシミュレーション結果を、図2のタイミングチャートに重ねて示す。OUT信号とXOUT信号の反転は同時に行われていることが分かる。

【0045】このように、OUT信号とXOUT信号の反転は同時に開始され、同時に完了するので、アナログスイッチ7のpチャネルMOSFET11_pとnチャネルMOSFET11_nとは同時にOFFし、互いの寄生容量に蓄積された電荷が充放電し合うので、ホールド容量C_Hにサンプリングされているホールド電圧は変化せず、誤差が生じることはない。

【0046】以上は、サンプルホールド回路2がサンプル動作からホールド動作に移行した場合について、ロー状態を第1の論理状態とし、ハイ状態を第2の論理状態とし、XSEL信号が第1の論理状態から第2の論理状態へ論理反転し、次いで、SEL信号が第2の論理状態から第1の論理状態へ論理反転する場合について説明した。

【0047】そのように、ロー状態を第1の論理状態とし、ハイ状態を第2の論理状態とすると、サンプルホールド回路がホールド動作からサンプル動作に移行する場合には、XSEL信号が第2の論理状態から第1の論理状態へ論理反転し、次いで、SEL信号が第1の論理状態から第2の論理状態へ論理反転する。その場合でもXSEL信号の論理反転の開始により、OUT信号の論理状態とXOUT信号の論理状態との変化を開始させ、SEL信号の論理反転の開始によりOUT信号の論理状態とXOUT信号の論理状態とを更に変化させれば、OUT信号とXOUT信号の論理状態の反転を同時に開始し、同時に完了させることができるので、アナログスイッチ7のpチャネルMOSFET11_pとnチャネルMOSFET11_nとを同時にONさせることができる。

【0048】他方、上述の波形整形回路3のpチャネルMOSFET(M_7)とnチャネルMOSFET(M_1)とは、サンプルホールド回路2がホールド状態からサンプル状態に切り替わるとき、SEL信号とXSEL信号の波形整形に大きく関与するが、サンプル状態からホールド状態に切り替わる際にはほとんど関与しない。このサンプルホールド回路2では、アナログスイッチ7が導通状態から遮断状態に切り替わるときだけ、ホールド容量C_Hが寄生容量の充放電による影響を受けるので、ホールド電圧の誤差だけを防止するためには、pチャネルMOSFET(M_7)とnチャネルMOSFET(M_1)とは不要となる。

【0049】そこで、波形整形回路3からnチャネルMOSFET(M_1)とpチャネルMOSFET(M_7)とを削除して図3の符号3'に示す波形整形回路を構成し、サンプルホールド回路に用いてもよい。

【0050】なお、以上の波形整形回路3、3'はpチャネルMOSFETとnチャネルMOSFETとで構成したが、それ以外の素子、例えばバイポーラートランジスタで構成する場合も本発明に含まれる。また、本発明の波形整形回路3、3'はアナログスイッチ7に入力される信号の波形を整形する場合に限定されるものではなく、互いに反対の論理状態になるSEL信号とXSEL信号との伝達遅延を修正する必要のある回路に広く用いることが可能である。

【0051】

【発明の効果】簡単な回路で、互いに反対の論理状態になるXSEL信号とSEL信号との反転の際の伝達遅延を修正することができる。

【0052】それにより、ホールド容量がアナログスイッチの寄生容量の影響を受けずに済み、ホールド電圧に誤差が生じなくなる。

【0053】半導体集積回路上に形成するホールド容量を大きくする必要がなくなるので、チップサイズを小さくでき、コストを低減させることができる。

【図面の簡単な説明】

【図1】　本発明の波形整形回路とサンプルホールド回路との一例を示す回路ブロック図

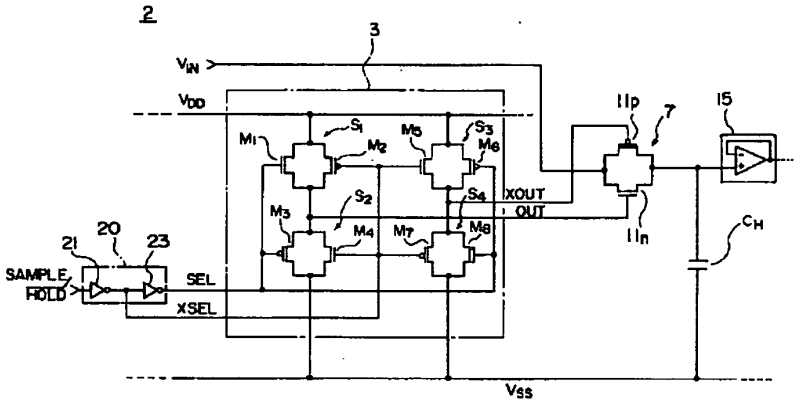
【図2】　その動作を説明するためのタイミングチャート

【図3】　本発明の波形整形回路の他の例を示す回路図

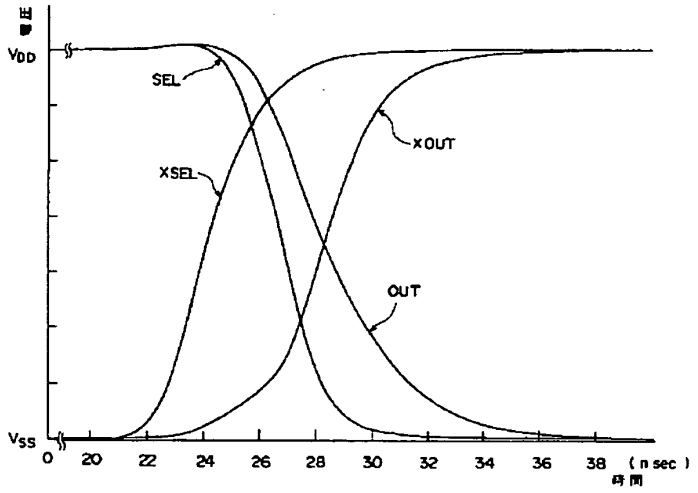
【図4】　(a)：従来技術を説明するための回路ブロッ

ク図
（b）：アナログスイッチの振幅を説明するための図
【符号の説明】
2……サンプルホールド回路　　3、3'……波形整形回路
7……アナログスイッチ
11_n……nチャネルMOSFET　　11_p……pチャネルMOSFET
23……インバーター
C_H……ホールド容量

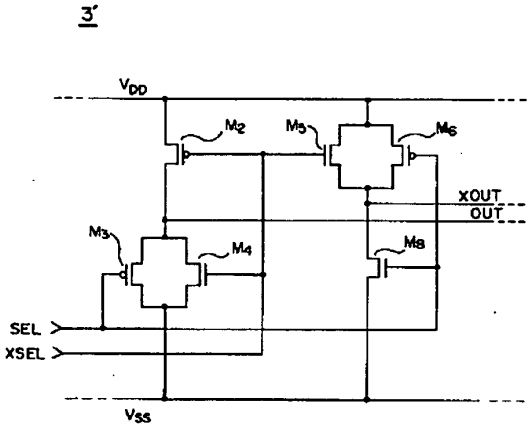
【図1】



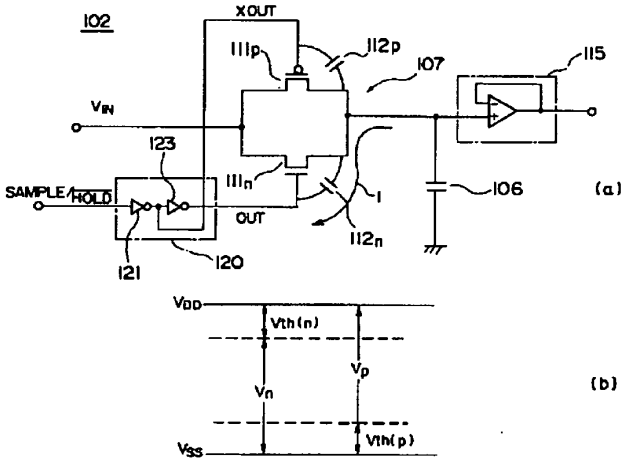
【図2】



【図3】


3'
VDD
M2
M5
M6
XOUT
OUT
M3
M4
M8
SEL
XSEL
VSS

【図4】


102
XOUT
111p
112p
107
115
VIN
123
SAMPLE/HOLD
111n
OUT
I
106
(a)
112n
121
120
VDD
Vth(n)
Vp
Vn
(b)
VSS
Vth(p)

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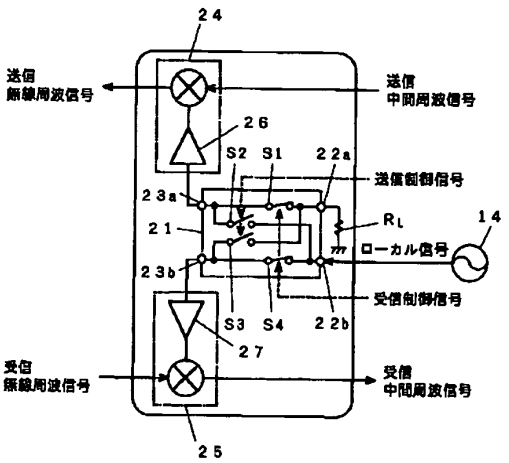
(54)【発明の名称】　ディジタル移動通信機器用高周波回路

(57)【要約】

【目的】高周波回路（特に送信用ミキサ及び受信用ミキサ）に対する通電の断続によるローカル信号発生回路の擾乱を有効に防止し得る新規なディジタル移動通信機器用高周波回路を提供すること。

【構成】ローカル信号発生回路の出力端子を切り替えて送信用ミキサ及び受信用ミキサの各々に交互に接続するためのスイッチ回路を用いて構成する。スイッチ回路は、ローカル信号発生回路の出力端子を両ミキサのいずれか一方の入力端子に接続した場合に、他方のミキサの入力端子をインピーダンス整合用終端抵抗に接続するダブルポール・ダブルスロー型スイッチである。その他に、ローカル信号発生回路の出力端子に接続した緩衝増幅器（ローカル信号発生回路に整合する入力インピーダンスを有する）と、同増幅器の出力のローカル信号を送信用ミキサ及び受信用ミキサのそれぞれに分配するための一対の出力増幅器（常時通電又は切り替え通電）からなる信号分配回路を用いて構成する。

図１



１４…ローカル信号発生回路
２１…スイッチ回路
２２…入力端子
２３…出力端子
２４…送信用ミキサ
２５…受信用ミキサ
２６，２７…ローカル信号増幅器
R_L…終端抵抗
Ｓ…スイッチ素子

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【特許請求の範囲】

【請求項1】アップコンバータとして機能する送信用ミキサを有する送信回路と、ダウンコンバータとして機能する受信用ミキサを有する受信回路と、送受信のための信号変換に必要なローカル信号を発生するためのローカル信号発生回路と、当該回路の出力端子を切り替えて送信用ミキサ及び受信用ミキサのそれぞれに交互に接続するためのスイッチ回路とを少なくとも備え、かつ、当該スイッチ回路は、ローカル信号発生回路の出力端子を両ミキサのいずれか一方の入力端子に接続した場合に、他方のミキサの入力端子をインピーダンス整合用終端抵抗に接続するための手段を具備するものであることを特徴とするディジタル移動通信機器用高周波回路。

【請求項2】前記スイッチ回路は、ローカル信号発生回路の出力端子に接続された第1の入力端子と、インピーダンス整合用終端抵抗に接続された第2の入力端子と、送信用ミキサの入力端子に接続された第1の出力端子と、受信用ミキサの入力端子に接続された第2の出力端子と、各入力端子と各出力端子との間に交差的にそれぞれ接続されたスイッチ素子からなるダブルポール・ダブルスロー型スイッチをもって構成されていることを特徴とする請求項1に記載の高周波回路。

【請求項3】前記スイッチ回路は、送信用ミキサ及び受信用ミキサと共にワンチップ半導体集積回路として構成されていることを特徴とする請求項2に記載の高周波回路。

【請求項4】アップコンバータとして機能する送信用ミキサを有する送信回路と、ダウンコンバータとして機能する受信用ミキサを有する受信回路と、送受信のための信号変換に必要なローカル信号を発生するためのローカル信号発生回路と、当該回路の出力端子に接続された緩衝増幅器と、当該増幅器の出力信号（ローカル信号）を送信用ミキサ及び受信用ミキサのそれぞれに分配するための一対の出力増幅器からなる信号分配回路を少なくとも備え、かつ、前記緩衝増幅器は、その入力インピーダンスがローカル信号発生回路の出力インピーダンスと整合する値に設定されていることを特徴とするディジタル移動通信機器用高周波回路。

【請求項5】前記出力増幅器は、スイッチ素子として機能し、緩衝増幅器の出力信号（ローカル信号）を切り替えて送信用ミキサ及び受信用ミキサのそれぞれに交互に供給するものであることを特徴とする請求項4に記載の高周波回路。

【請求項6】前記緩衝増幅器及び信号分配回路は、送信用ミキサ及び受信用ミキサと共にワンチップ半導体集積回路として構成されていることを特徴とする請求項4又は請求項5に記載の高周波回路。

【請求項7】前記送信用ミキサは、平衡型の回路をもって構成されていることを特徴とする請求項1～請求項6のいずれか一に記載の高周波回路。

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【請求項8】平衡型の回路をもって構成されている前記送信用ミキサは、不平衡信号を平衡信号に変換するインダクタンスと静電容量からなる180度位相器と、同180度位相器の出力端子が入力端子に接続された差動増幅器と、同差動増幅器の出力端子が入力端子に接続された平衡型のミキサ本体をもって構成されていることを特徴とする請求項7に記載の高周波回路。

【請求項9】前記差動増幅器は、デュアルゲート型の電界効果トランジスタの差動対をもって構成され、同差動対の一方の電界効果トランジスタの下段のゲートが差動増幅器の一方の入力端子であり、同差動対の他方の電界効果トランジスタの下段のゲートが差動増幅器の他方の入力端子であることを特徴とする請求項8に記載の高周波回路。

【請求項10】前記差動増幅器の一方の出力端子が前記差動対の一方の電界効果トランジスタのドレイン端子であり、他方の出力端子が前記差動対の他方の電界効果トランジスタのドレイン端子であり、両出力端子にそれぞれインピーダンス素子が接続され、同インピーダンス素子の他端が互いに接続されて第1の接続点をなし、同第1の接続点に電気抵抗を介して電源が接続されていることを特徴とする請求項9に記載の高周波回路。

【請求項11】前記差動増幅器の前記差動対の一方の電界効果トランジスタの上段のゲートと他方の電界効果トランジスタの上段のゲートが互い接続されて第2の接続点をなし、同第2の接続点に差動増幅器の電流量を制御するための電圧が供給されていることを特徴とする請求項9又は請求項10に記載の高周波回路。

【請求項12】デュアルゲート型の電界効果トランジスタの前記差動対のソースに単一の電界効果トランジスタのドレインが接続され、同単一の電界効果トランジスタのゲートに前記差動対の電流量を制御するための電圧が供給されていることを特徴とする請求項9又は請求項10のいずれか一に記載の高周波回路。

【請求項13】前記ミキサ本体は、入力端子に前記作動増幅器の出力端子が接続された二組の差動対と、同二組の差動対に直列に接続された別の差動対をもって構成され、いずれの差動対も電界効果トランジスタにより構成され、当該別の差動対の一方の電界効果トランジスタのゲートは周波数が変換される信号の入力端子であり、他方の電界効果トランジスタのゲートはミキサ本体の電流量を制御するための電圧が供給されていることを特徴とする請求項8～請求項12に記載の高周波回路。

【請求項14】電界効果型トランジスタのゲートが制御端子をなし、ソースが接地され、ドレインが出力端子をなし、極性をそろえて直列に接続したダイードのアノードが出力端子に接続され、同ダイオードのカソードが制御端子に接続されてなる半導体回路が電流量を制御して回路動作を制御するための回路として接続されていることを特徴とする請求項5又は請求項11～請求項13の

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いずれか一に記載の高周波回路。

【請求項15】前記半導体回路の制御端子と出力端子の間に静電容量が接続されていることを特徴とする請求項14に記載のディジタル移動通信端末用ミキサ回路。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は、ディジタル移動通信機器用高周波回路、特に電池駆動式の移動端末に適用して好適な高周波回路に関するものである。

【0002】

【従来の技術】TDMA(Time Domain Multiple Access)ディジタル移動通信システムにおいて使用されている電池駆動式移動端末の高周波回路の一例を図14に示す。アンテナ1と送信回路8又は受信回路9との間は、スイッチ3による送受切替が可能なように接続されており、送信時には、送信回路8の出力である無線周波信号が帯域通過フィルタ2を介してアンテナ1に伝達され、受信時には、アンテナ1によって受信された無線周波信号が帯域通過フィルタ2を介して受信回路9に伝達される。

【0003】送信回路8は、電力増幅器4、帯域通過フィルタ5、送信用ミキサ10（アップコンバータ）などにより構成されており、一方、受信回路9は、低雑音増幅器6、帯域通過フィルタ7、受信用ミキサ11（ダウンコンバータ）などにより構成されている。ローカル信号発生回路14は、ローカル信号増幅器12又は13を介して送信用ミキサ10及び受信用ミキサ11に共通に接続されている。

【0004】図14の高周波回路の動作タイミングを図15に示す。この場合、移動通信の通話路は、送信用に4スロット、受信用に4スロットが使用されており、送信回路8及び受信回路9は、それぞれに割り当てられたスロット「送1」又はスロット「受1」の期間中に動作状態（ON）となり、他のタイミングでは非動作状態（OFF）となる。電池駆動式移動端末の場合は、通話可能な時間をできるだけ長くするため、詳細図示せざるも、送信回路8又は受信回路9が非動作状態にある期間中は、これらの回路を含む関連回路に対する通電を停止して電池の消耗を抑制する対策が採られている。

【0005】しかしながら、送信用ミキサ10及び受信用ミキサ11に対する通電が断続した場合、ローカル信号発生回路14から両ミキサを見た入力インピーダンスが瞬間的に微妙に変動する。ローカル信号発生回路14は、ループ利得が大きく時定数も長い帰還回路を含むPLL(Phase Locked Loop)回路を用いて構成するのが普通であるから、この種のインピーダンス変動は、ローカル信号発生回路14の安定性に悪い影響を与える。即ち、PLL回路は、ミキサ10，11の入力インピーダンスの瞬間的な変動に追従することができないため、大きな誤差信号を一時的に発生してローカル信号発生回路

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14の発振周波数を不安定にする結果、タイムスロットの欠落等の重大な障害が発生する。

【0006】

【発明が解決しようとする課題】本発明の主たる目的は、高周波回路（特に送信用ミキサ及び受信用ミキサ）に対する通電の断続によるローカル信号発生回路の擾乱を有効に防止し得る新規なディジタル移動通信機器用高周波回路を提供することにあり、かつ、その付帯的な目的は、ローカル信号発生回路の擾乱防止機能を備えたディジタル移動通信機器用高周波回路の送信用ミキサ及び受信用ミキサと両ミキサにローカル信号を供給する回路をワンチップ半導体集積回路を用いて実現することにある。

【0007】

【課題を解決するための手段】本発明の前記課題は、ローカル信号発生回路の出力端子を切り替えて送信用ミキサ及び受信用ミキサのそれぞれに交互に接続するためのスイッチ回路を用いることによって解決することができる。もっとも、このようなスイッチ回路をただ単に用いただけでは、切替接続による過渡現象に伴うインピーダンス変動が不可避的に発生する結果、ローカル信号発生回路の動作が一時的に乱れる現象を完全に防止することができない。

【0008】このため、前記スイッチ回路は、ローカル信号発生回路の出力端子を両ミキサのいずれか一方の入力端子に接続した場合に、他方のミキサの入力端子をインピーダンス整合用終端抵抗に接続するための手段を具備するものであることが必要である。この種のスイッチ回路は、それぞれ一対の入力端子及び出力端子の相互間にスイッチ素子を交差的に配設してなるダブルポール・ダブルスロー型スイッチを用いて構成することが可能である。この場合、一方の入力端子はローカル信号発生回路の出力端子に接続し、他方の入力端子は前記終端抵抗にそれぞれ接続すると共に、一対の出力端子は送信用ミキサ及び受信用ミキサの入力端子にそれぞれ接続する。

【0009】本発明の前記課題は、ローカル信号発生回路の出力端子に接続した緩衝増幅器と、当該増幅器の出力信号（ローカル信号）を送信用ミキサ及び受信用ミキサのそれぞれに分配するための一対の出力増幅器からなる信号分配回路を用いることによっても解決することが可能である。但し、この場合は、緩衝増幅器の入力インピーダンスがローカル信号発生回路の出力インピーダンスと整合する値に設定されていることを必要とする。一対の出力増幅器は、単なる増幅素子として機能し、緩衝増幅器の出力信号を常時送信用ミキサ及び受信用ミキサに供給するものであるか、或は、スイッチ素子として機能し、緩衝増幅器の出力信号を切り替えて送信用ミキサ及び受信用ミキサのそれぞれに交互に供給するものであることが望ましい。

【0010】

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【作用】本発明の前記スイッチ回路は、送信用ミキサ及び受信用ミキサのそれぞれの入力端子をローカル信号発生回路又はインピーダンス整合用終端抵抗のいずれか一方に必ず接続しておくものであるから、ミキサ回路の入力インピーダンスを切替接続の前後を通して常に一定に保持することが可能となり、同回路の入力インピーダンスの変動に伴うローカル信号発生回路の擾乱を防止することができる。

【００１１】また、本発明の前記緩衝増幅器においては、トランジスタ（電界効果トランジスタ）のゲート又はソースを入力側として用い、出力側（ドレイン）のインピーダンス変動が入力側からみて遮断される効果を利用する。更に、緩衝増幅器に接続する一対の出力増幅器も、入力側を電界効果トランジスタのソース又はゲートにして出力増幅器の出力側のインピーダンス変動が遮断されるようにする。このようにして、出力増幅器の出力側に接続する送信用ミキサ、受信用ミキサのインピーダンス変動が、緩衝増幅器の入力側からみて、二重に抑圧される。従って、ローカル信号発生回路に与えるインピーダンス変動を極めて僅かものにすることができる。

【００１２】また、出力増幅器の入力側をゲートにし、一対の出力増幅器の動作、非動作を交互に切り替えてスイッチ素子として機能させることが可能である。ゲートのインピーダンスは動作、非動作のいずれの場合も非常に高いので、緩衝増幅器に与える影響を僅少なものとすることができる。

【００１３】以上の緩衝増幅器及び一対の出力増幅器の構成を用いることによって、ローカル信号発生回路の擾乱を効果的に防止することができる。なお、緩衝段増幅器の入力側のインピーダンスが整合インピーダンスとなるように、ゲートを入力側とする場合は、整合用の付加抵抗を入力側に接続し、ソースを入力側とする場合には、トランジスタの動作電流を所定の値に設定する。

【００１４】緩衝増幅器及び一対の出力増幅器は、言うまでもなく電力消費があるが（回路を簡単な構成にして消費電力を低く抑えることは可能である）、これを許容してもローカル信号発生回路の擾乱を高度に抑える必要がある用途（例えば基地局）に用いられる場合が多い。これに対して前記スイッチ回路は、電力消費がほとんどないので、特に消費電力低減を目的とする用途（例えば移動端末）に用いられる場合が多い。

【００１５】なお、前記スイッチ回路、或いは緩衝増幅器及び一対の出力増幅器は、送信用ミキサ及び受信用ミキサと共にワンチップ半導体集積回路として構成することが望ましい。

【００１６】

【実施例】以下、本発明に係るディジタル移動通信端末用ミキサ回路を図面に示した実施例を参照して更に詳細に説明する。

【００１７】（実施例１）図１に示したスイッチ回路２

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１は、一対の入力端子２２ａ，２２ｂと一対の出力端子２３ａ，２３ｂを備え、かつ、各入力端子と各出力端子との間に４個のスイッチ素子Ｓ１～Ｓ４を交差的に配設した公知のダブルポール・ダブルスロー型スイッチである。一方の入力端子２２ａには、インピーダンス整合用の終端抵抗R_Lが接続されており、他方の入力端子２２ｂには、ローカル信号発生回路１４の出力端子が接続されている。また、一方の出力端子２３ａは、送信用ミキサ２４の一部であるローカル信号増幅器２６の入力端子に接続されており、他方の出力端子２３ｂは、受信用ミキサ２５の一部であるローカル信号増幅器２７の入力端子に接続されている。なお、入力端子２２ａと出力端子２３ａとの間及び入力端子２２ｂと出力端子２３ｂの間に配設されたスイッチ素子Ｓ１及びＳ４は、受信制御信号によって連動して動作するものであり、かつ、入力端子２２ｂと出力端子２３ａとの間及び入力端子２２ａと出力端子２３ｂの間に配設されたスイッチ素子Ｓ２及びＳ３は、送信制御信号によって連動して動作するものである。

【００１８】図１のスイッチ回路２１は終端抵抗R_Lを含めて、図２に示したように、送信用ミキサ２４及び受信用ミキサ２５と共に、ワンチップ半導体集積回路２８として構成することが可能である。なお、図１におけるスイッチ素子Ｓ１～Ｓ４は、電界効果トランジスタＴ１～Ｔ４を用いて構成されている。送信用ミキサ２４（ローカル信号増幅器２６を含む）及び受信ミキサ２５（ローカル信号増幅器２７を含む）は、ピンチオフ電圧Ｖｐが浅く（－１Ｖ）、相互コンダクタンスｇｍが高い電界効果トランジスタを使用し、スイッチ回路２１は、オン抵抗低減の観点から、ピンチオフ電圧Ｖｐが深く（－２Ｖ）、相互コンダクタンスｇｍが低い電界効果トランジスタを使用することが望ましい。なお、送信用ミキサ２４及び受信用ミキサ２５は、公知の回路構成を採用した。

【００１９】図３に示すように、送信のために送信制御信号をハイレベル（０Ｖ）にしてトランジスタＴ２，Ｔ３を導通状態（ＯＮ）にし、受信のために受信制御信号をハイレベル（０Ｖ）にしてトランジスタＴ１，Ｔ４を導通状態（ＯＮ）にする。送信制御信号及び受信制御信号のローレベルは－３Ｖとし、ローレベルのときのトランジスタは、非導通状態（ＯＦＦ）になる。終端抵抗R_Lは、ローカル信号発生回路１４との整合が可能な５０Ωとした。なお、トランジスタＴ１～Ｔ４のそれぞれのゲートに接続した抵抗は、トランジスタＴ１～Ｔ４が導通状態の時に、送信制御信号又は受信制御信号の供給線がソース又はドレインに短絡してローカル信号に損失を与えるのを防止するためのものである。

【００２０】本実施例のスイッチ回路２１を採用することにより、良好なインピーダンスの整合を図りつつ、ローカル信号発生回路１４の出力端子を送信ミキサ２４又

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は受信ミキサ２５のいずれか一方に切え替えて接続することが可能となった。また、送信ミキサ２４及び受信ミキサ２５は、ローカル信号発生回路１４に接続されていない場合であっても、その入力端子が５０Ωのインピーダンス整合用抵抗R_tで終端されることになり、接続切替の際に発生する過渡的なインピーダンスの変動を小さくすることができた。

【００２１】送信用ミキサ２４及び受信用ミキサ２５のインピーダンス変動を反射波の測定によって評価した結果、図４ａに示すように、反射波の振幅が０．０５Ｖ以下、変動の持続時間が５ｎｓ以内の極めて良好な結果を得ることができた。終端抵抗R_tを接続しないで、入力端子２２ａを直接接地した場合の反射波は、図４ｂに示すように大きく変動した。

【００２２】なお、スイッチ回路２１による接続切替を行なう前に、非動作状態にある送信用ミキサ２４（又は受信用ミキサ２５）を動作状態にし、接続切替が完了してから動作状態にある受信用ミキサ２５（又は送信用ミキサ２４）を非動作状態にした場合は、インピーダンス変動抑圧の効果を更に高めることができた。交信中、両ミキサ２４，２５のローカル信号増幅器２６，２７を常時動作状態にすることによっても、同様の効果を期待することが可能である。両ミキサ２４，２５は、同じ回路形式であることが望ましいが、ローカル信号発生回路１４のＰＬＬ回路の特性によっては、回路形式の異なるミキサを組み合わせて使用することも可能である。

【００２３】本実施例では以上のように、ローカル信号を送信用ミキサ２４又は受信用ミキサ２５のいずれか一方にのみ供給するので、同時に両ミキサに供給する従来の高周波回路に比べてローカル信号の供給電力を低減することができる利点がある。

【００２４】〈実施例２〉図５において、２９は緩衝増幅器、３０は、一対の出力増幅器３１ａ，３１ｂからなる信号分配回路を示す。出力増幅器３１ａは、送信用ミキサの入力端子にローカル信号を供給する増幅器、出力増幅器３１ｂは、受信用ミキサの入力端子にローカル信号を供給する増幅器である。

【００２５】図６に示したように、緩衝増幅器２９は、ディプリージョン形の電界効果トランジスタＴ５を用いたソース接地型とし、ローカル信号を整合回路を介してトランジスタＴ５のゲートに入力する構成とした。同ゲートにはインピーダン整合用の抵抗を接続した。出力増幅器３１ａ，３１ｂは、同じくディプリージョン形の電界効果トランジスタＴ９，１０を用いたゲート接地型である。トランジスタＴ６，７のソースを共通に接続し、そこにトランジスタ５のドレインを接続した。増幅器３１ａ，３１ｂのドレインの出力端子は、それぞれ出力整合回路（図６ではＬＣ回路）を介して送信用ミキサ２４、受信用ミキサ２５の入力端子に接続される。なお、出力整合回路の他方の端子に電源電圧V_{dd}が供給される。

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【００２６】以上の回路構成によって、送信用ミキサ２４、受信用ミキサ２５の入力インピーダンスの変動は、緩衝増幅器２９と信号分配回路３０によって二重に抑圧される。

【００２７】なお、緩衝増幅器２９及び信号分配回路３０は、送信用ミキサ２４、受信用ミキサ２５とともにワンチップ半導体集積回路２８（図５）として構成することが可能である。また、本実施例は、全体としてカスコード回路となり、高利得を得易い。但し、利得の増加と共に発振の可能性が増すために接地端子の位置に注意する必要がある。本実施例を集積化した場合に、安定に動作させるため図６に示したように、入力整合回路の接地端子とカスコード回路の接地端子を独立させることが望ましい。また、ローカル信号増幅器２６、２７（図５）の接地端子とも独立させることが望ましい。本実施例により、インピーダンス変動を抑え且つ簡易な回路構成で消費電力を少なくした緩衝増幅器２９及び信号分配回路３０を実現することができた。

【００２８】〈実施例３〉本実施例は、図７に示したように、出力増幅器３１ａに送信制御信号、出力増幅器３１ｂに受信制御信号を供給して増幅器３１ａ，３１ｂを交互に動作状態にし、両増幅器をスイッチ素子として機能させたものである。ローカル信号は、送信ミキサ２４と受信用ミキサ２５に切り替えて供給される。

【００２９】図８に示すように、緩衝増幅器２９はディプリージョン型の電界効果トランジスタＴ８、一対の出力増幅器３１ａ，３１ｂからなる信号分配回路３０は同じくディプリージョン型の電界効果トランジスタＴ９，Ｔ１０を用いて構成した。緩衝増幅器２９及び信号分配回路３０は、送信用ミキサ２４及び受信用ミキサ２５と共に、ワンチップ半導体集積回路２８（図７）として構成することが可能である。送信制御信号及び受信制御信号の波形及び電圧値を図９に示した。

【００３０】図８において、緩衝増幅器２９はトランジスタＴ８のゲート接地型とした。ゲート接地形においては、出力側（ドレイン）の負荷インピーダンスはドレイン・ソース間の高いインピーダンスに遮蔽されてソース側では殆どみえず、ソースをみた入力インピーダンスは、ほぼ１／ｇｍで一定にみえる。即ち、出力側のインピーダンス変動は遮断される。ｇｍ(相互コンダクタンス)は、トランジスタの動作電流を調節して２０ｍＳ近辺に設定することができる。従って、入力インピータンスを容易に信号源インピーダンスである５０Ωと整合を取ることができた。出力側のドレインには、集積化した場合のチップ面積削減の観点から抵抗負荷を採用した。

【００３１】出力増幅器３１ａ，３１ｂは、各々トランジスタＴ９，Ｔ１０によるソースフォロア回路で構成した。トランジスタＴ９，Ｔ１０のゲートを相互に接続してトランジスタＴ８のドレインに接続した。トランジス

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タT9，T10のゲートをみたインピーダンス（制御信号を供給するための抵抗を除く）は、トランジスタが電界効果型であるためにほぼ開放状態に近く、トランジスタ8の負荷抵抗に比べて格段に高くすることができる。更に、ソースに接続した送信用ミキサ24、受信用ミキサ25の入力インピーダンスが変動しても、ゲート側は高いインピーダンスのままとなってトランジスタ8の負荷抵抗に与える影響が小さく、更に、トランジスタが非動作状態になっても開放状態に近いことでは同様であり、やはり負荷抵抗に与える影響が小さい。以上から、緩衝増幅器29の入力側からみたインピーダンスの変動を効果的に抑えることができる。本実施例により容易に整合を取り、かつ、インピーダンス変動を抑えた緩衝増幅器29及び信号分配回路30を実現することができた。

【0032】〈実施例4〉本実施例は、実施例1～実施例3において送信用ミキサのミキサ本体とローカル信号増幅器を平衡型で構成したもので、特にローカル信号が送信の無線周波信号に漏洩するのを防止することを目的としたものである。図10に回路の基本構成を示す。まず、インダクタンスと静電容量を用いた周知の180度位相器51を用いて、入力端子(L_{oin}）の不平衡のローカル信号を平衡信号に変換する。平衡信号（差動信号）を平衡型の差動増幅器52に供給し、その出力信号を平衡型の送信用ミキサ本体53に供給した。ローカル信号増幅器26は、位相器51と差動増幅器52により構成される。ミキサ本体53の入力端子（IF_{in}）の中間周波信号は、無線周波信号に変換されて出力端子（RF_{out}）に出力される。

【0033】図11に詳細な回路図を示す。図11において、トランジスタにディプリージョン形の電界効果トランジスタを用いたが、エンハンスメント形電界効果トランジスタ、バイポーラトランジスタを用いてもバイアスレベルが異なる以外は同じ特徴、効果を得ることができる。

【0034】位相器51の差動信号をデュアルゲート型の電界効果トランジスタT12，T13（差動対）を用いた差動増幅器52に供給し、電力を増幅する。位相器51の出力で残っている同相成分は、差動増幅器52の同相除去特性で更に抑圧される。差動増幅器52には、整合を取るための抵抗R12と静電容量C3の直列接続回路があるが、これも同相除去特性を劣化させることのないようにトランジスタT12，T13に等しく接続した。加えて差動増幅器52の出力端子にインダクタンスL2を経てから接続した抵抗R2により同相成分が更に除去される。これらの三重の同相成分の抑圧機構により、素子バラツキに強い差動ローカル信号を得ることができた。なお、抵抗R2を介して差動増幅器52に電源電圧BV_{dd}が供給される。

【0035】差動増幅器52の電流制御（回路動作のON，OFF）は、トランジスタT12，T13の上段のゲートのバイアスを制御することで行なう。電流制御の信号は、端子V_{in}から供給される。電界効果トランジスタのピンチオフ電圧が－1Vである場合は、ゲートバイアスを－1V以下にすれば電界効果トランジスタを流れる電流をほとんど0にすることが可能となる。ローカル信号が印加される下段のゲートのバイアスを制御しないのは入力端子からPLL回路へ伝わるインピーダンス変動を小さくするためである。下段のゲートは、抵抗R3を介して接地電位にバイアスした。このことについて少し詳細に述べる。使用しているディプリージョン形の電界効果トランジスタは、GaAs MESFET (Metal Semiconductor Field Effect Transistor) であるので、ゲートに加わる逆バイアスを変化させると、ゲートのショットキー接合容量の値が大きく変わるため、バイアス制御を行うゲートの入力インピーダンスは大きく変動する。下段の、ローカル信号が印加されるゲートのバイアスを変化させると入力インピーダンスの変化が大きくなる。このためローカル信号が印加されるゲートを制御端子として用いるのは望ましくない。以上のことから上段のゲートを電流制御に使用した。

【0036】送信用ミキサ本体53は、ギルバート型の乗算器を平衡型ミキサとして使用した。差動対の電界効果トランジスタT14，T15の端子IF_{in}に送信の中間周波信号を入力した。トランジスタT14，T15の差動対は、低電圧で動作させるために、電流源を抵抗R6で構成した。また、同差動対の歪特性改善の為に抵抗R7をトランジスタT14，T15のソース間に付加した。差動増幅器52からの180度位相の異なる差動ローカル信号を電界効果トランジスタT16，T17及びT18，T19の二組の差動対に供給する。同二組の差動対がトランジスタT14，T15で増幅した送信の中間周波信号をローカル信号でスイッチングする。これによって、出力端子RF_{out}においてアップコンバートされた送信の無線周波信号を得る。ミキサ本体53の電流制御は、トランジスタT14，T15の差動対のゲートバイアスを制御することで行なった。電流制御の信号を端子V_{in}から供給した。これも差動増幅器52と同様、ローカル信号の入力されるゲートは、電流制御には使用しない。以上のように、ローカル信号の入力されるゲートと電流制御の為のゲートを独立にさせることで、ローカル入力端子L_{oin}から見たインピーダンス変動の小さいミキサ回路を実現することができた。なお、電源電圧MV_bを供給してトランジスタT16，T17及びT18，T19のゲートにバイアス電圧を与え、ドレインに電源電圧MV_{dd}を供給した。

【0037】〈実施例5〉本実施例は、図11の差動増幅器52の電流制御をトランジスタT11を用いて行なったもので、回路図を図12に示す。図11の場合には、差動増幅器52を非動作状態にしても、図11の抵

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抗R4，R5に電流が流れる為、非動作時にも電流を消費してしまう。本実施例ではこの点を改善している。実施例4との相違点は、図12に示すように、電流制御を定電流源として動作させているT11のゲートで制御すること、デュアルゲートトランジスタT12，T13の上段のゲートを抵抗R4を介してT12，T13のソース電位にバイアスしていることの2点である。トランジスタT11のゲートに電流制御の信号を入力する端子をV_{cb}とした。差動増幅器52を流れる全ての直流電流は、T11を通るためT11の電流を切るとすべての電流が切れる。本実施例により、非動作時に消費する電流を低減した移動通信機器に好適なローカル増幅器を実現出することができた。

【0038】〈実施例6〉差動増幅器52に用いたディプリージョン形の電界効果型トランジスタ（GaAs MESFET)は、ゲートに逆バイアスを深くかけた後、通電すると電流量が元の量に達するまでに遅延が生じる現象が知られている。このため電流制御のバイアスが深くなると、図15で示したTDMA動作に対し、回路が追随して動作出来ない場合が生ずる。しかしながら逆バイアスの深さは、本回路のみでは決まらず、他の回路との関係で決定される。本実施例は、深い逆バイアスを制御電位として与えられても、ゲートに加わる逆バイアスを浅く保つ回路を提供するものである。図13に本実施例の回路図を示す。制御信号がトランジスタT20、ダイオードD1，D2を介して、例えば図12の制御するトランジスタT11のゲート(端子V_{cb}に接続されている）に供給される。ダイオードD1，D2は、制御信号の電圧を制限するために制御端子とトランジスタT20のドレインの間に接続したものであり、ダイオードD1，D2に並列に接続した静電容量C_b1は、高周波雑音を除去するためのもの、トランジスタT20のゲートに接続した抵抗は、トランジスタT20がON（導通状態）となったときに制御端子がドレイン、ソースに短絡するのを防止するために挿入したものである。

【0039】図13において、制御端子には0(V)と－Vcon(V)がかかるものとする。0(V)がかかった場合は、トランジスタT20がONとなり、トランジスタT11（図12）のゲートには0(V)が印加される。制御端子に、トランジスタT20のピンチオフ電圧以下の、－Vcon(V)がかかった場合に、トランジスタT11のゲートには$-Vcon+2V_D$(V)印加される。V_Dは、ダイオードD1，D2のON電圧である。ダイオードD1，D2は、トランジスタT11のゲートのリーク電流で駆動する。このように複数のダイオードD1，D2のON電圧分だけゲートに加わる逆バイアスは浅くなる。例えば－Vcon(V)＝－3(V)、V_D(V)＝0．7(V)の場合、トランジスタT11のゲートには0(V)から－1．6(V)のバイアスが印加される。このように、制御バイアスを浅くすることでON、OFFに対する応答特

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性を改善し、低消費電流動作特性の優れた回路を実現することができた。直列ダイオードの個数を変えることで受ける制御信号の電圧値を最適化することができる。

【0040】なお、同様にディプリージョン形の電界効果型トランジスタ（GaAs MESFET）を使用している図8の回路に対しても送信制御信号及び受信制御信号の入力端子に本実施例が適用され、更に図11の回路に対しても端子V_{cb}，V_{cl}に本実施例が適用される。

【0041】

【発明の効果】本発明によれば、ローカル信号発生回路の動作不安定を招く高周波回路のインピーダンス変動を抑えることができ、送信用ミキサ、受信用ミキサ及びローカル信号を供給する回路をワンチップ化したディジタル移動通信機器に好適な半導体集積回路を実現することができる。また、ローカル信号の供給電力が低減されるので装置の低消費電力化が可能である。

【図面の簡単な説明】

【図1】本発明に係るディジタル移動通信機器用高周波回路の第1の実施例を説明するための回路構成図。

【図2】第1の実施例で使用するスイッチ回路及びワンチップ半導体集積回路を説明するための回路構成図。

【図3】スイッチ回路の動作を説明するための時間系統図。

【図4】第1の実施例の入力端子のインピーダンス変動を示す曲線図。

【図5】本発明の第2の実施例を説明するための回路構成図。

【図6】第2の実施例で用いる緩衝増幅器および出力増幅器を説明するための回路図。

【図7】本発明の第3の実施例を説明するための回路構成図。

【図8】第3の実施例で用いる緩衝増幅器および出力増幅器を説明するための回路図。

【図9】第3の実施例で用いる出力増幅器の動作を説明するための時間系統図。

【図10】本発明の第4の実施例を説明するための回路構成図。

【図11】第4の実施例で用いる平衡型の送信用ミキサを説明するための回路図。

【図12】本発明の第5の実施例を説明するための回路図。

【図13】本発明の第6の実施例を説明するための回路図。

【図14】TDMA方式を採用した移動通信機器の従来の高周波回路を説明するための回路構成図。

【図15】図14で示した高周波回路の動作タイミングを説明するための時間系統図。

【符号の説明】

10，24…送信用ミキサ

11，25…受信用ミキサ

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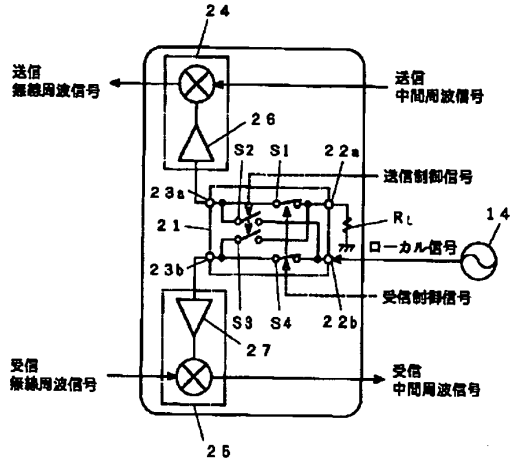
12，13，26，27…ローカル信号増幅器
14…ローカル信号発生回路
21…スイッチ回路
22…スイッチ回路の入力端子
23…スイッチ回路の出力端子
28…ワンチップ半導体集積回路
29…緩衝増幅器
30…信号分配回路
31…出力増幅器

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51…180度位相器
52…差動増幅器
53…送信用ミキサ本体
C…静電容量
D…ダイオード
S…スイッチ素子
R_L…終端抵抗
T…電界効果トランジスタ

【図1】

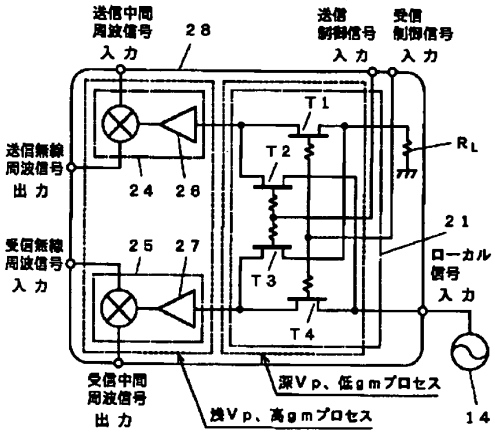
図1



14…ローカル信号発生回路
21…スイッチ回路
22…入力端子
23…出力端子
24…送信用ミキサ
25…受信用ミキサ
26，27…ローカル信号増幅器
R_L…終端抵抗
S…スイッチ素子

【図2】

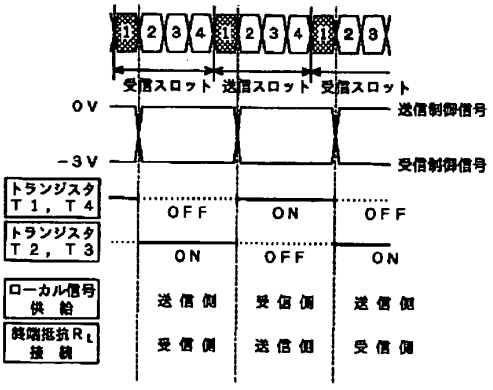
図2



14…ローカル信号発生回路
21…スイッチ回路
24…送信用ミキサ
25…受信用ミキサ
26，27…ローカル信号増幅器
28…ワンチップ半導体集積回路
R_L…終端抵抗
T…電界効果トランジスタ

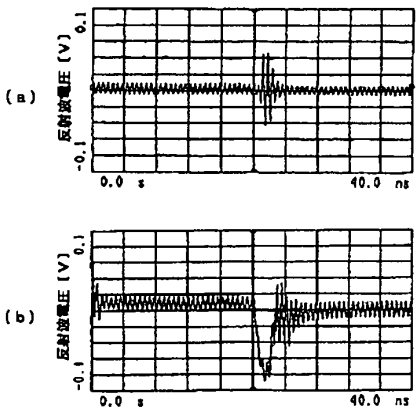
【図3】

図3



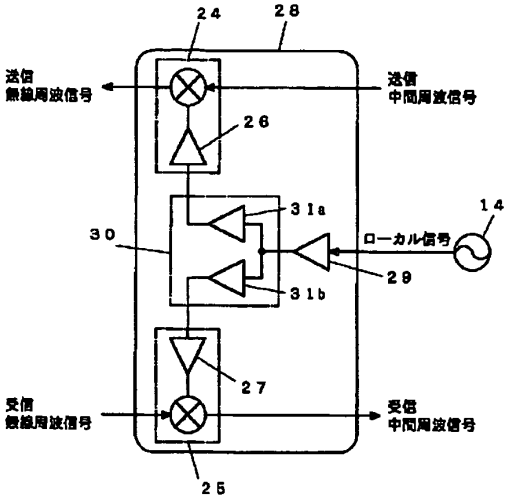
【図4】

図4



【図5】

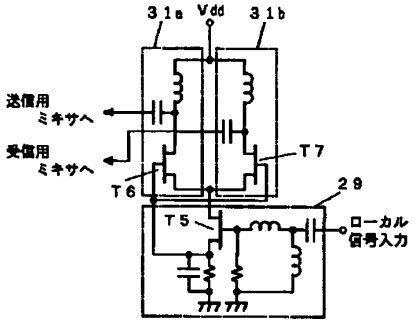
図5



14…ローカル信号発生回路
24…送信用ミキサ
25…受信用ミキサ
26，27…ローカル信号増幅器
28…ワンチップ半導体集積回路
29…緩衝増幅器
30…信号分配回路
31…出力増幅器

【図6】

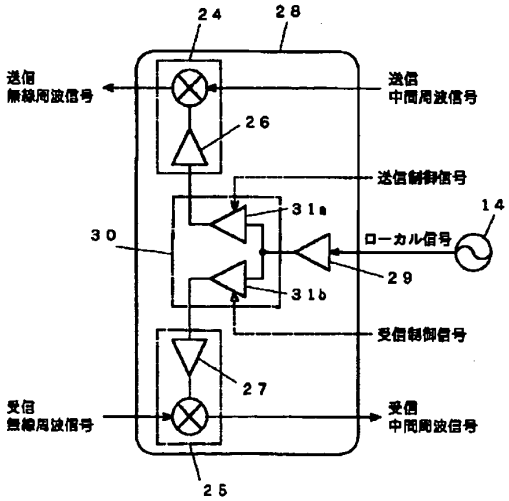
図6



29…緩衝増幅器
31a，31b…出力増幅器
T…電界効果トランジスタ

【図7】

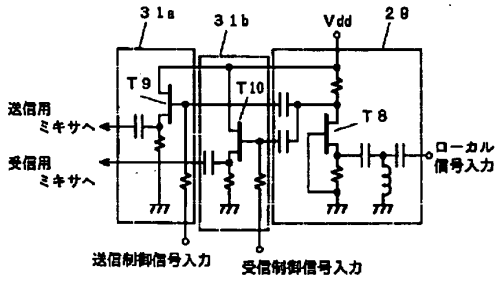
図7



14…ローカル信号発生回路
24…送信用ミキサ
25…受信用ミキサ
26，27…ローカル信号増幅器
28…ワンチップ半導体集積回路
29…緩衝増幅器
30…信号分配回路
31…出力増幅器

【図8】

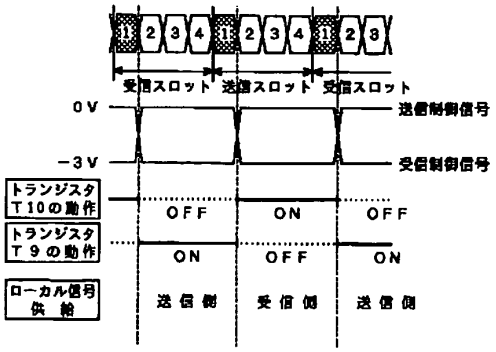
図8



29…緩衝増幅器
31a，31b…出力増幅器
T…電界効果トランジスタ

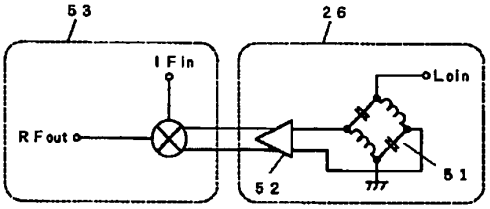
【図9】

図9



【図10】

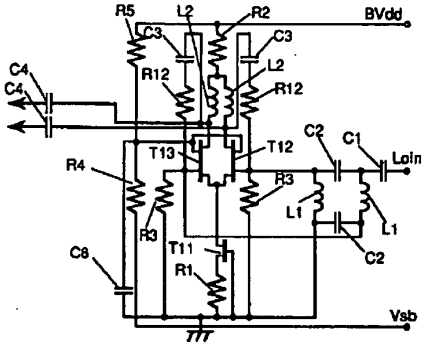
図10



53…送信用ミキサ本体
26…ローカル信号増幅器
51…180度位相器
52…差動増幅器

【図12】

図12



【図11】

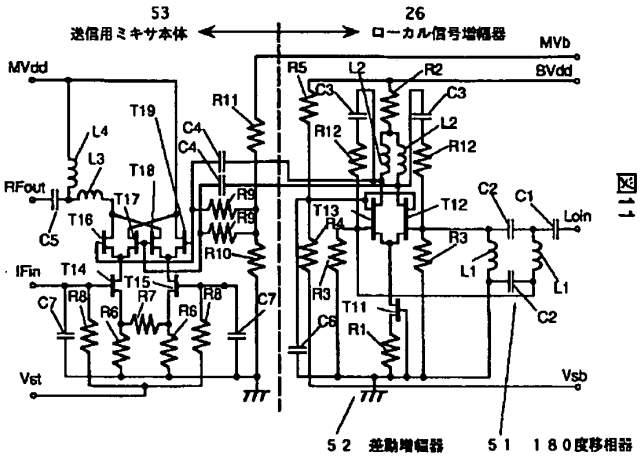
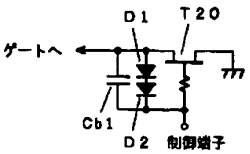


図11

【図13】

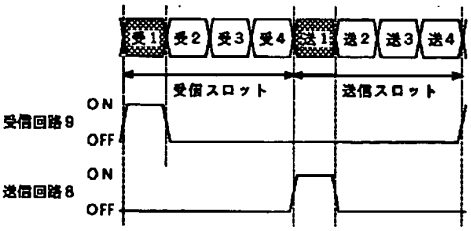
図13



C…静電容量
D…ダイオード
T…電界効果トランジスタ

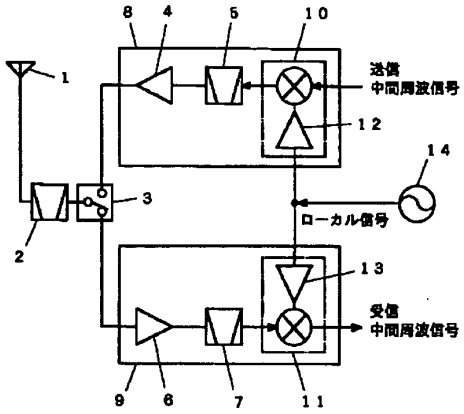
【図15】

図15



【図１４】

図１４



1…アンテナ
2，5，7…帯域通過フィルタ
3…スイッチ
4…電力増幅器
6…低雑音増幅器
8…送信回路
9…受信回路
10…送信用ミキサ
11…受信用ミキサ
12，13…ローカル信号増幅器
14…ローカル信号発生回路

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(54) Title: RECEIVER HAVING AN ADJUSTABLE BANDWIDTH FILTER

(57) Abstract

A radio receiver has a frequency down conversion stage (28) including a first passive filter (50, 51, 52) tuned to a lower frequency. An amplifier (56, 58) functioning as a voltage to current converter (54) comprises a resistor (60) which can be shunted by a second passive filter (70, 71, 74) in response to actuation of symmetrically arranged switching devices (72, 73). When the second passive filter shunts the resistor the overall pass band is raised to a higher frequency. Additionally the amplifier has a lower noise figure when the second passive filter shunts the transconductor.

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DESCRIPTION

RECEIVER HAVING AN ADJUSTABLE BANDWIDTH FILTER

TECHNICAL FIELD

The present invention relates to a radio frequency receiver and particularly but not exclusively to an adjustable bandwidth filter for use in a radio frequency receiver for receiving particularly, but not exclusively, digital signals.

BACKGROUND ART

Communication receivers for receiving digital signals, for example digitised speech, are well known and frequently have an architecture in which a received signal is applied to an adjustable gain r.f. amplifier prior to a first frequency down conversion stage which produces an i.f. frequency. The i.f. frequency is filtered in say a SAW filter and the filtered signal is applied to another frequency down conversion stage in which the i.f. signal is applied to nominally quadrature related mixers, the outputs of which are low pass filtered and then applied to a digital signal processor (DSP). Figure 1 illustrates a typical low pass filter input-output characteristic in which the ordinate is amplitude in db and the abscissa is frequency f. The wanted signal band is indicated as f_w and the unwanted higher band of frequencies is indicated as f_{uw}. The receiver noise level is indicated by a horizontal broken line RNL. As is known in the art in order to be able to determine the correct value of a digital signal the amplitude of the input signal need only be several dbs above a level termed the Minimum Distinguishable Signal MDS. Accordingly there is little point in designing filters to handle much bigger signals if the result is the consumption of a lot more current.

If the input signal applied to the low pass filters should

significantly exceed this MDS level, the filter will then be overdriven. Eliminating this problem could lead to an unwanted increase in current consumption due the filter having to be designed to cope with a dynamic range of input signals which is much larger than is strictly necessary. Generally this problem is countered by the DSP applying automatic gain control signals to the adjustable gain r.f. amplifier.

In the interests of current saving the low pass filters are thus generally designed to handle a limited dynamic range of wanted signals and to consume a low power. However a problem arises when strong unwanted signals need to be blocked by the filters as there is no AGC applied by the DSP. The filters must be able to cope with such unwanted signals in a linear way. If the filters are designed to be capable of handling large unwanted signals this could lead to a significant increase in power consumption, for example 141 times more power could be required for handling an unwanted signal which is greater than the MDS level by 23 db than for a signal just above that level.

Such low pass filters are not infrequently voltage driven transconductor filters. However if such filters comprise current driven transconductor filters then a much larger signal, for example 14.5 db larger in the case of a Gaussian to 6 db filter, can occur in the stop-band than in the wanted band without the filter going non-linear. Even with this improvement there is still a desire to cope with an even larger signal, for example up to say 23 db larger, in the stop-band without the filter going non-linear and also to make the filter have an adjustable bandwidth to be able to selectively pass a narrow band signal which for example occurs in the Pan-European or GSM cellular telephone system and a wider band signal which for example occurs in the Digital European Cordless Telephone (DECT) system.

DISCLOSURE OF INVENTION

According to the present invention there is provided a radio frequency receiver comprising a frequency down conversion stage which includes first passive filtering means having a first cut-off frequency, first and second outputs from the frequency down conversion stage, an amplifier having first and second active devices coupled respectively to the first and second outputs and having respective current outputs, first resistive means interconnecting corresponding electrodes of the first and second active devices, filtering means having inputs for receiving current outputs from said first and second active devices, said filtering means including transconducting means connected to said inputs, and second passive filtering means which are connectable in parallel with said first resistive means, whereby when said second passive filtering means is not connected in parallel with the first resistive means a narrow band signal is applied to the filtering means and when said second passive filtering means is connected in parallel with the first resistive means a wideband signal is applied to the filtering means.

By providing the first passive filtering means in the frequency down conversion stage and a current driven transconductor filtering means, the level of signal in the stop band which can be handled without the filter going non-linear is increased from 14.5 db to 23 db without increasing the current consumption. The provision of the second passive filtering means enables the filter bandwidth to be selectively adjustable.

The second passive filtering means may comprise second and third resistance means of substantially equal resistance value, each second and third resistive means having first and second ends, the first ends being coupled to respective ends of the first resistive means, capacitive

means, and first and second switching means being coupled respectively between the second ends of the second and third resistive means and the capacitance means, whereby when said first and second switching means are conductive the second passive filtering means shunts the first resistive means and when said first and second switching means are non-conductive the second passive filtering means is disconnected electrically from the first resistive means. The first and second switching means may comprise field effect transistors and by locating them between the second and third resistive means and the capacitive means it is possible to operate the switching means using relatively small d.c. voltages and minimise non-linearities due to differences in potential between the first switching means and the substrate and the second switching means and the substrate. Also using two switching means rather than one maintains the symmetry of the circuit and in so doing avoids the risk of introducing other non-linearities. An advantage of arranging the second passive filtering means to be connected in parallel with the first resistive means when selecting the wider band signals is that the narrow band signal is not compromised because the second and third switching means are then open (non-conductive) and the non-linearities are not present.

BRIEF DESCRIPTION OF DRAWINGS

The present invention will now be described, by way of example, with reference to the accompanying drawings, wherein:

Figure 1 is a graph of a low pass filter characteristic,

Figure 2 is a block schematic diagram of a radio frequency receiver,

Figure 3 is a schematic diagram of a mixer and low pass filter arrangement,

Figure 4 is a schematic circuit diagram of the voltage to current

converter 54 shown in Figure 3 in which the switch devices 72,73 comprise field effect transistors,

Figure 5 is a schematic diagram of a variant of the voltage to current converter 54 shown in Figure 3,

Figure 6 is an equivalent circuit of a 5th order current driven transconductance filter,

Figure 7 is a graph of the various individual and composite filter characteristics, and

Figure 8 is a graph of the noise figure of the voltage to current converter as a function of the logarithm of the source resistance (Log R_s) versus frequency (f).

In the drawings the same reference numerals have been used to indicate corresponding features.

MODES FOR CARRYING OUT THE INVENTION

Referring to Figure 2, the receiver comprises an antenna 10 which is connected to an r.f. input stage 12 comprising adjustable gain r.f. amplifiers 14,15 and a mixer 16 connected in cascade and a first local oscillator 18 connected to the mixer 16. The products of mixing are supplied to a band pass filter 20 which selects the desired band of intermediate frequencies (i.f.). A second frequency down conversion stage 22 is coupled to an output of the filter 20. The stage 22 comprises an i.f. amplifier 24 and two nominally quadrature related signal paths I and Q which are connected to inputs of a DSP 26. Each of the I and Q signal paths comprises a mixer 28,29 having an input coupled to an output of the amplifier 24 and an adjustable bandwidth low pass filter 30,31 coupled between its mixer 28,29, respectively, and the DSP 26. The nominally quadrature related signal paths I and Q are obtained in the illustrated receiver by supplying a local oscillator signal nominally in quadrature to the mixers 28,29. This is done by

connecting an output of a local oscillator 32 directly to the mixer 28 and to a nominally $\pi/2$ phase shifter 34 having an output connected to the mixer 29. The DSP 26 not only is used to recover the signal but also is used to control the gain of one or both r.f. amplifiers 14,15 so that the amplitude of the wanted signal f_w (Figure 1) is only slightly greater than the MDS level. The operation of this type of receiver is generally well known and has been summarised in the preamble of this specification.

Figure 3 illustrates an embodiment of a mixer 28 and a low pass filter 30 having a switchable bandwidth. The mixer 28 comprises a first long tail pair circuit formed by NPN transistors 36,37 whose base electrodes receive an input signal from the amplifier 24 (Figure 2) and whose emitter electrodes are jointly connected to a current source 38. The collector electrodes of the transistors 36,37 are respectively connected to second and third long tail pair circuits formed by pairs of NPN transistors 40,41 and 42,43. The emitter electrodes of the pairs of transistors 40,41 and 42,43 are respectively connected to the collector electrodes of the transistors 36,37. The base electrodes of the transistors 40,43 are interconnected as are the base electrodes of the transistors 41,42. A local oscillator (LO) source is connected to the respective interconnections. The collector electrodes of the transistors 40,42 and of the transistors 41,43 are interconnected at junctions 44,46, respectively. The junctions 44,46 are coupled to a supply rail V+ by way of a first passive filtering means 48 formed by resistive devices 50,51 of substantially equal value connected respectively between the junctions 44,46 and the supply line V+ and a shunt capacitor 52.

The partially filtered output voltages appearing at the junctions 44,46 are supplied to a post mixer amplifier consisting of a voltage to

current converter 54 comprising NPN transistors 56,58 whose base electrodes are connected respectively to the junctions 44,46, whose emitter electrodes are interconnected by an emitter degeneration resistive device 60 and are connected to respective current sources 62,64, and whose collector electrodes are connected to respective inputs 65,67 of a current driven transconductor filter 66 to be described with reference to Figure 6.

A second, switchable passive filtering means 68 is connectable in parallel with the resistive device 60. The filtering means comprises two substantially equal value resistive devices 70,71 having one end connected respectively to the emitter electrodes of the transistors 56,58, a capacitive element 74 and switch devices 72,73 connected between the second ends of the resistive devices 70,71, respectively and respective plates of the capacitive element 74.

Figure 4 illustrates an embodiment in which the switch devices 72,73 comprise field effect transistors, the gate electrodes of which are connected to a bandwidth control input 75. The switch devices 72,73 are non-conductive when the second passive filtering means 68 is non-operative and the overall circuit is behaving as a narrow band filter and conductive, in response to a signal on the input 75, when the second passive filtering means 68 is shunting the resistive device 60 to provide a broader bandwidth filter. An advantage of such an arrangement is that narrow band systems tend to have relatively stringent linearity requirements and by the field effect transistors being non-conductive for narrow band operation the risk of the on-resistance of these transistors degrading the performance of the first passive filtering means is avoided.

Figure 5 is a variant of the voltage to current converter 54 in which the current sources 62,64 are combined into one current source

63 which is connected to a centre tap of the resistor 60. An advantage of using a single current source is that any noise which is generated is rejected due to it being a common mode signal. However such an arrangement is not suited to low voltage circuits because of the dc drops across the respective parts of the resistor 60.

The current driven transconductor low pass filter 66 (Figure 6) comprises a transconductor 76 configured as a resistor connected between the inputs 65,67, a simulation of an LC filter comprising two series connected inductances 78,79 and three shunt capacitive elements 80,81,82 and a transconductor 84 configured as a resistor connected to outputs 85,86.

Figure 7 illustrates how the second, switchable passive filtering means can be used to widen the filter response. With the switches 72,73 open, the filter response 88 is that shown by the continuous line and is produced by the first passive filtering means. The response is a narrow band response having a cut-off above a wanted frequency f_a but below the frequency f_b of the alternative wanted broadband signal. The second, switchable passive filtering means modifies the normally frequency independent response of the voltage to current converter 54 so that it has the response 90 shown in broken lines. By closing the switch devices 72,73, an overall broadband filter response 92 shown in chain-dot lines is thus obtained. By making the resistive and capacitive elements 70,71,74 of the same materials as those used for making the components of the first passive filter, the two filter responses track each other. This can be illustrated mathematically by giving the following components the value indicated:

Resistors 50,51 = $R_s/2$

Capacitor 52 = C_s

Resistor 60 = R_d

Resistors 70,71 = $R_n/2$

Capacitor 74 = C_n

Frequency f_a is defined by the product $C_s \times 2(R_s/2) = C_s R_S$

$$R_n = 2 \times (R_n/2) = \frac{R_d}{(\frac{f_b}{f_a} - 1)} \quad (1)$$

$$C_n = (1 - \frac{f_a}{f_b}) \frac{R_s}{R_d} . C_s \quad (2)$$

The presence of the resistor, capacitor and frequency ratios confirms that tracking will occur.

As mentioned, two switch devices 72,73 are provided in order to maintain symmetry and thereby avoid introducing non-linearities. By arranging these devices 72,73 to be on either side of the capacitive element 74 then the effect of voltage variations with respect to the substrate are very small or substantially zero. However if the switch devices 72,73 were located on the other sides of the resistive elements 70,71 then the effect of voltage variations with respect to the substrate will be much larger which is undesirable. As the frequency increases the voltage across the capacitive element 74 goes down thereby causing the switch devices 72,73 to get closer together, differences in the influence of the substrate on the on-resistance diminishing.

Referring now to Figure 8, the curve 94 shown by a full line is the typical noise characteristic of an amplifier. This characteristic has a minima which indicates the value of the source resistance Rs which gives the best noise figure. In the circuit shown in Figure 3 the voltage to current converter 54 sees the output resistance (Rs_{28}) of the mixer

28 which is less than the optimum value. This is normally the case and is a consequence of the resistive device 60 being relatively large so that the linearity of the voltage to current converter 54 is adequate. The optimum value of Rs would typically be hundreds of kilohms. Working at one end of the characteristic has the benefit that when the second passive filtering means 68 is switched into the circuit and at frequencies greater than f_a the noise characteristic is shifted towards the ordinate and becomes the curve 96 shown in broken lines and for a source resistance Rs_{28} the noise figure has reduced. The noise performance of the voltage to current converter is dependent on the net effective resistance of the totality of the network comprising the resistive devices 60,70,71 and the capacitance 74. By closing the switch devices 72,73 the effective on-resistance of the switch devices 72,73 is made negligible to the totality of resistive devices 60,70,71 and the capacitance 74. The shift in the characteristic is explained by the fact that at a frequency f_b, say 576 kHz, which is greater than the frequency f_a, say 80 kHz, the value of R_n (resistive devices 70,71) is less than the value R_d (resistive device 60), see equation (1) above for a ratio of

$$\left(\frac{f_b}{f_a}\right)=\frac{576}{80}=7.2$$

Thus the curve is moved in a direction of reducing the source resistance and as a consequence for the same value of Rs_{28} the noise figure is lower. Additionally as the amplitude of the signal at the mixer output decreases at higher frequencies and the noise figure is improving then the signal to noise ratio at the input to the voltage to current converter 54 remains substantially unchanged, in other words the amplitude of the mixer output and the noise figure effectively track each other. In a specific example of the second passive filter for f_a = 80 kHz and f_b =

576 kHz, R_d = 20 kΩ, R_n = 3.23 kΩ, R_s = 6.6 kΩ, C_s = 217 pF and C_n = 61.7 pF. The cut-off frequency of the current driven transconductor filter 66 can also be tuned from f_a to f_b in known manner.

From reading the present disclosure, other modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the design, manufacture and use of radio frequency receivers and filters thereof and which may be used instead of or in addition to features already described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of the disclosure of the present application also includes any novel feature or any novel combination of features disclosed herein either explicitly or implicitly or any generalisation thereof, whether or not it relates to the same invention as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as does the present invention. The applicants hereby give notice that new claims may be formulated to such features and/or combinations of such features during the prosecution of the present application or of any further application derived therefrom.

INDUSTRIAL APPLICABILITY

Radio receiver suitable for digital cellular and/or digital cordless telephones.

CLAIMS

1. A radio frequency receiver comprising a frequency down conversion stage which includes first passive filtering means having a first cut-off frequency, first and second outputs from the frequency down conversion stage, an amplifier having first and second active devices coupled respectively to the first and second outputs and having respective current outputs, first resistive means interconnecting corresponding electrodes of the first and second active devices, filtering means having inputs for receiving current outputs from said first and second active devices, said filtering means including transconducting means connected to said inputs, and second passive filtering means which are connectable in parallel with said first resistive means, whereby when said second passive filtering means is not connected in parallel with the first resistive means a narrow band signal is applied to the filtering means and when said second passive filtering means is connected in parallel with the first resistive means a wideband signal is applied to the filtering means.

2. A receiver as claimed in claim 1, characterised in that the second passive filtering means comprises second and third resistive means of substantially equal resistance value, each second and third resistive means having first and second ends, the first ends being coupled to respective ends of the first resistive means, capacitive means, and first and second switching means coupled respectively between the second ends of the second and third resistive means and the capacitance means, whereby when said first and second switching means are conductive the second passive filtering means shunts the first resistive means and when said first and second switching means are non-conductive the second passive filtering means is disconnected electrically from the first resistive means.

3. A receiver as claimed in claim 2, characterised in that the first and second switching means comprise field effect transistors.

4. A receiver as claimed in claim 2 or 3, characterised in that the total resistance value of the second and third resistive means is less than the resistance value of said first resistive means.

5. A receiver as claimed in any one of claims 1 to 4, characterised in that components of the first and second passive filtering means are fabricated from the same materials.

6. A receiver as claimed in any one of claims 1 to 5, characterised in that current sources are connected to each of the junctions formed by the first ends of the second and third resistive means with the ends of the first resistive means.

7. A receiver as claimed in any one of claims 1 to 5, characterised in that the first resistive means has a tap and in that a current source is connected to the tap.

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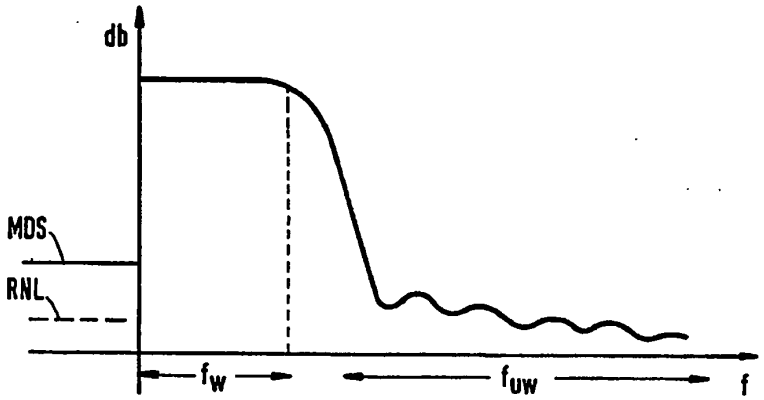

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FIG.1

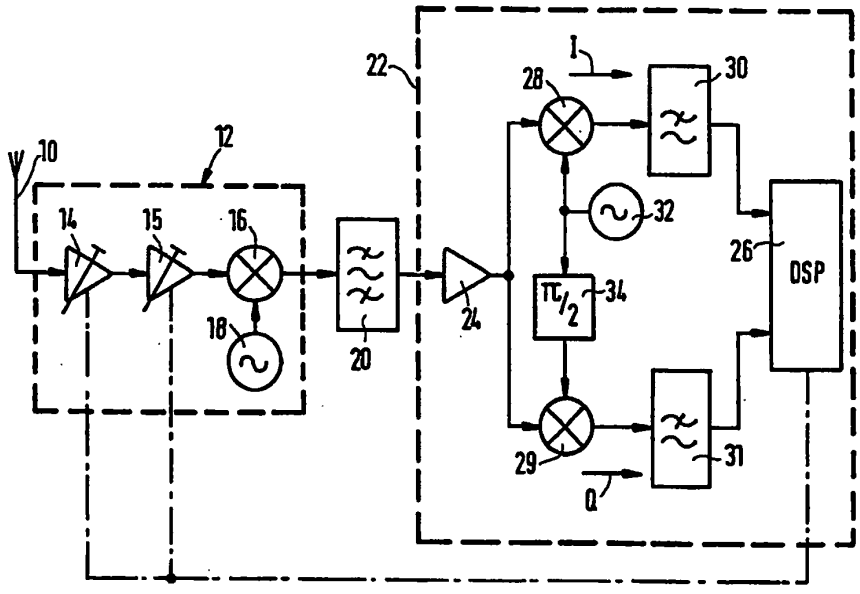

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FIG.2

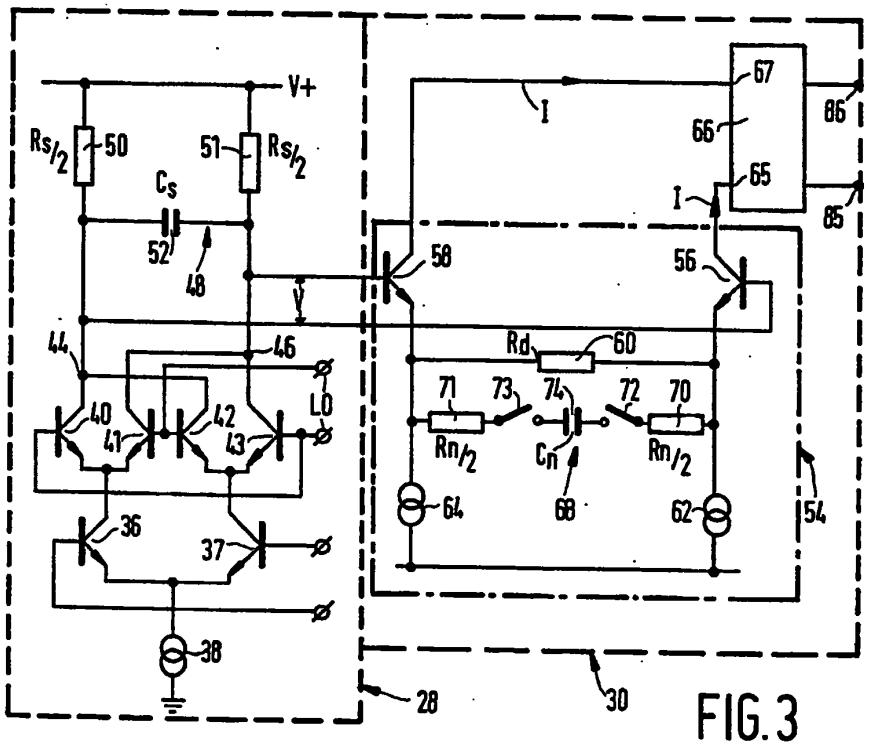


FIG.3

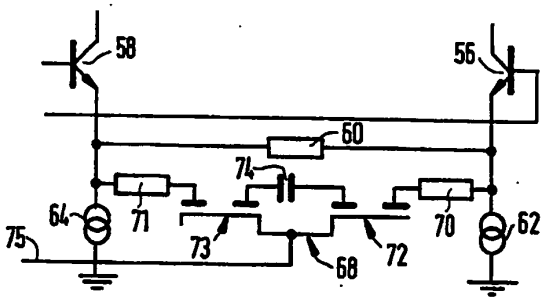


FIG.4

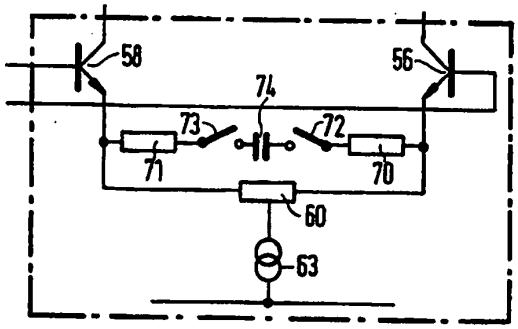


FIG.5

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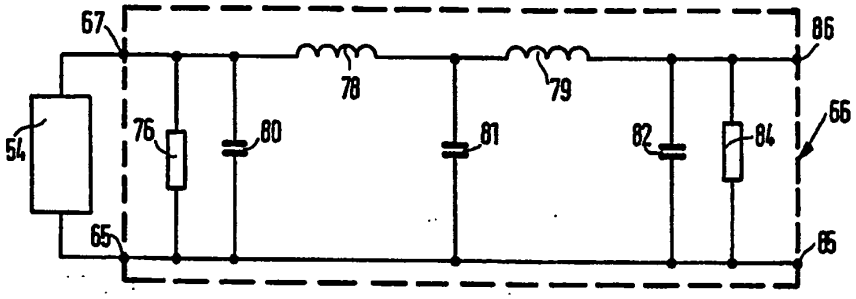


FIG.6

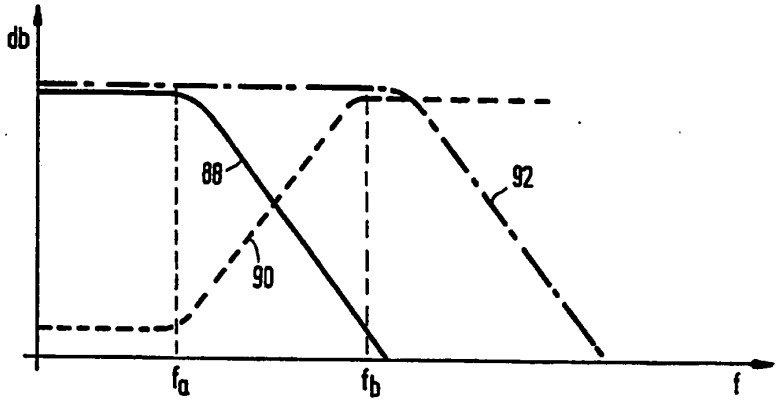


FIG.7

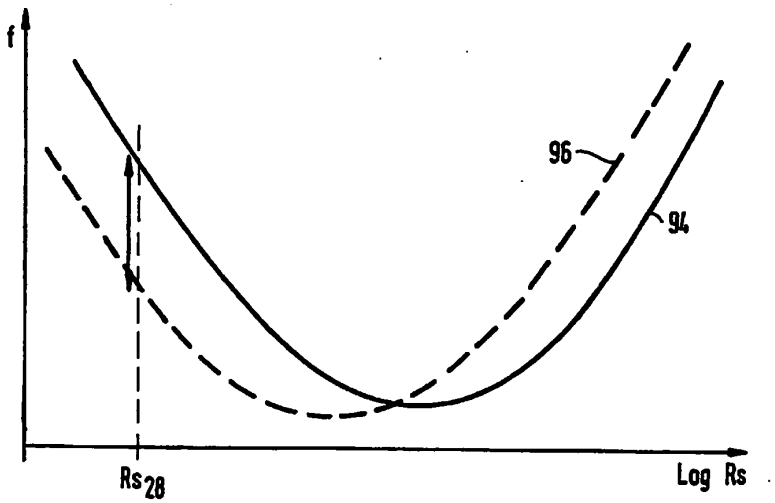


FIG.8

ARTIFACT SHEET

Enter artifact number below. Artifact number is application number + artifact type code (see list below) + sequential letter (A, B, C …). The first artifact folder for an artifact type receives the letter A, the second B, etc.. Examples: 59123456PA, 59123456PB, 59123456ZA, 59123456ZB

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[ ] Other, description: _____
Doc Code: Artifact Artifact Type Code: Z

March 8, 2004

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Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Art Unit 2617

Re: U.S. Utility Patent Application
Appl. No. 12/349,802; Filed: January 7, 2009
For: **Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same, and Aperture Relationships**
Inventor: David F. SORRELLS
Our Ref: 1744.001000P

Sir:

Transmitted herewith for appropriate action are the following documents:

1. PTO-2038 Credit Card Payment Form for $180.00 to cover the IDS Late Filing Surcharge (under 37 C.F.R. § 1.17(p));

2. Information Disclosure Statement;

3. Ninety-one (91) pages of Form PTO-1449 listing one thousand two hundred and fifty-two (1252) documents;

4. One (1) Compact Disc labeled *IDS References Copy 1 of 2*, containing PDF copies of each of the Foreign Patent documents and Non Patent Literature documents listed on the Form PTO-1449;

5. One (1) Compact Disc labeled *IDS References Copy 2 of 2*, which is a courtesy duplicate copy of item no. 4 above;

6. Copies of Foreign Patent documents AM28 and AJ29-AL29;

7. Copies of Non Patent Literature documents AN64-AP64; and

8. One (1) return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

MQL/VDT:jeg
Enclosures

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In re application of:	Confirmation No. 5719
David F. SORRELLS	Art Unit: 2617
Appl. No. 12/349,802	Examiner: Bhattacharya, Sam
Filed: January 7, 2009	Atty. Docket: 1744.001000P
For: **Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same, and Aperture Relationships**	

Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98.

Solely for the convenience of the Examiner, and in addition to providing hard copies of the documents as required by applicable rules (see box 8 on page 35 below), Applicants herewith provide two (2) copies of a Compact Disc labeled "IDS References" having stored thereon searchable electronic copies (in PDF format) of the documents (except for the U.S. Patent documents) listed on the PTO-1449. More specifically, the CDs contains electronic copies of documents AJ1-AR1, AJ2-AR2, AJ3-AR3, AJ4-AR4, AJ5-AR5, AJ6-AR6, AJ7-AR7, AJ8-AR8, AJ9-AR9, AJ10-AR10, AJ11-AR11, AJ12-AR12, AJ13-AR13, AJ14-AR14, AJ15-AR15, AJ16-AR16, AJ17-AR17, AJ18-AR18, AJ19-AR19, AJ20-AR20, AJ21-AR21, AJ22-AR22, AJ23-AR23, AJ24-AR24, AJ25-AR25, AJ26-AR26, AJ27-AR27, AJ28-

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AR28, AJ29-AL29, AN29-AR29, AN30-AR30, AN31-AR31, AN32-AR32, AN33-AR33, AN34-AR34, AN35-AR35, AN36-AR36, AN37-AR37, AN38-AR38, AN39-AR39, AN40-AR40, AN41-AR41, AN42-AR42, AN43-AR43, AN44-AR44, AN45-AR45, AN46-AR46, AN47-AR47, AN48-AR48, AN49-AR49, AN50-AR50, AN51-AR51, AN52-AR52, AN53-AR53, AN54-AR54, AN55-AR55, AN56-AR56, AN57-AR57, AN58-AR58, AN59-AR59, AN60-AR60, AN61-AR61, AN62-AR62, AN63-AR63, and AN64-AP64. The file names on the CDs correspond to the identifiers on the PTO-1449 form. Applicant is also providing hard copies of the documents to the extent required by applicable rules (see box 8 on page 35 below). The enclosed CDs are being provided solely for the convenience of the Examiner.

Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

Applicants provide the following comments regarding the documents:

Documents AD1, AL1, AO1, AC2, AF2, AG2, AI2, AC5, AG5, AB6, AF7, AI7, AB8, AF8, AG9, AK9, AO9, AO11, AA12, AE14, AN14, AB15, AE15, AH15, AO15, AF16, AD18, AG18, AB20, AC20, AQ20, AA22, AH22, AI23, AC24, AF26,

AC30, AH31, AC32, AA33, AR33, AH34, AP35 and AO48 were included with Petitions to Make Special pleadings in co-owned related U.S. Patent Nos. 6,061,551, 6,061,555, 6,049,706 and 6,091,940.

Documents AJ1, AL9, AJ10, AA19, AC25, AB30 and AF32 were cited in search reports in the corresponding foreign applications of the above-referenced co-owned related patents.

Documents AM4, AH6, AL7, AJ9, AM9, AC17, AA20, AG20, AG21, AA24, AD24, AG24, AI31, AA32, AG34, AD36 and AQ37 were cited in searches performed at Applicant's request by the European Patent Office's Searching Authority in the above-referenced co-owned related patents.

Documents AH5, AH17, AD21, AB34, AE34, AB36, AI36 and AI38 were cited by the Examiners in the above-referenced co-owned related patents.

Documents AP6-AR6 and AN7-AP7 are copies of Declarations (including Exhibits) made by Messrs. Bultman, Cook, Holtz, Looke, Moses, Parker, and Sorrells, filed in the above-referenced co-owned related patents.

Documents AA6, AD6, AO6, AE7, AE8, AA11, AE11, AH11, AI12, AB13, AD13, AH13, AC14, AG14, AE16, AB17, AF19, AD20, AN21, AG23, AH27, AI27, AI28, AH29, AG30, AD37, AR40, AO49 and AQ49 were suggested or identified by potential licensees.

Documents AR21, AN22-AR22, AN23-AR23, AN24-AR24, AN25-AR25, AN26-AR26, AN27-AR27, AN28-AR28, AN29-AR29, AN30-AR30, AN31-AR31, AN32-AR32 and AN33-AP33 are press releases issued by assignee ParkerVision, Inc.

Documents AA1, AB1, AD1-AG1, AA2, AH21, AD44, and AD59-AF59 were cited by an Examiner in U.S. Patent Application No. 09/569,044, filed May 10, 2000, entitled "Universal Platform Module and Methods and Apparatuses Relating Thereto Enabled by Universal Frequency Translation Technology," directed to related subject matter.

Document AA1-AD1, AB48, and AH64 were cited by an Examiner in U.S. Patent Application No. 10/197,441, filed July 18, 2002, entitled "Method and System for Frequency Up-Conversation with a Variety of Transmitter Configurations," directed to related subject matter.

Documents AJ1, AK9-AM9, AG28, AB30, AA32, AN52 and AP55 were cited by an Examiner in European Patent Application No. 99954905.8, filed October 18, 1999, entitled "Integrated Frequency Translation and Selectivity with a Variety of Filter Embodiments," directed to related subject matter.

Documents AM4, AL24, AM24, AJ25-AL25, and AF71 were cited by an Examiner in Israel Patent Application No. 142,699, filed October 18, 1999, entitled "Method and System for Frequency Up-Conversion," directed to related subject matter.

Documents AI7, AJ9, AK9, AG20, AG21, AB30 and AI43 were cited in a written opinion in PCT Application No. PCT/US00/23923, filed October 18, 1999, entitled "Applications of Frequency Translation," directed to related subject matter.

Documents AI7, AE34, AA46, and AB48 were cited by an Examiner in U.S. Patent Application No. 09/293,580, filed April 16, 1999, entitled "Method and System

for Frequency Up-Conversion with a Variety of Transmitted Configurations," directed to related subject matter.

Documents AJ9, AL11, AJ12, AK12, AJ24, AA27, AE45, AF45, and AQ50 were cited by an Examiner in European Patent Application No. 04020115.4, filed October 6, 2000, entitled "Down Converter Using Subsampling," directed to related subject matter.

Documents AK9, AM9, AE15, AL19, AM19, AB46 and AA50 were cited in a search report in PCT Application No. PCT/US01/08969, filed March 22, 2001, entitled, "Integrated Frequency Translation and Selectivity with a Gain Control Functionality, and Applications Thereof," directed to related subject matter.

Documents AK9, AE15, AK22-AM22, AA27, AC32, AE45, AI51, AA52, and AQ58 were cited in a search report in PCT Application No. PCT/US01/15555, filed May 16, 2001, entitled, "Apparatus, System, and Method for Down-Converting and Up-Converting Electromagnetic Signals," directed to related subject matter.

Documents AK9, AC17, AD36 and AD40 were cited in a search report in PCT Application No. PCT/US00/21359, filed August 4, 2000, entitled "Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology," directed to related subject matter.

Documents AK9, AK24, AC32, AI51, AQ58, and AE71 were cited by an Examiner in European Patent Application No. 01977965.1, filed May 16, 2001, entitled "Apparatus, System, And Method For Down-Converting And Up-Converting Electromagnetic Signals," directed to related subject matter.

Documents AJ10, AH17, AG28, AH34, AD44-AI44, and AA45-AD45 were cited by an Examiner in U.S. Patent Application No. 09/261,129, filed March 3, 1999, entitled "Applications of Universal Frequency Translation," directed to related subject matter.

Documents AM10, AJ11, AK11 and AE40 were cited in a communication issued by the International Preliminary Examination Authority in PCT Application No. PCT/US00/01108, filed January 19, 2000, entitled "Frequency Translation and Embodiments Thereof Such as the Family Radio Service," directed to related subject matter.

Documents AL11, AM11, AA44, and AQ50 were cited in a communication issued by the International Searching Authority in PCT Application No. PCT/US00/09911, filed April 14, 2000, entitled "Method And System For Down-converting an Electromagnetic Signal, And Transforms For Same," directed to related subject matter.

Documents AJ12, AK12, AE45, and AF45 were cited in a search report in PCT Application No. PCT/US00/27555, filed October 6, 2000, entitled "DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," directed to related subject matter.

Documents AL12, AM12, AG45, and AH45 were cited in a search report in PCT Application No. PCT/US00/34771, filed January 21, 2000, entitled "Phase Comparator Using Undersampling," directed to related subject matter.

Documents AJ13-AL13, AI45, and AB46 were cited in a search report issued in PCT Application No. PCT/US00/27281, filed October 4, 2000, entitled "Frequency Converter and Method," directed to related subject matter.

Documents AL13, AM18, AJ19, and AI45 were cited in a search report in PCT Application No. PCT/US00/31659, filed November 20, 2000, entitled "Phase Shifting Applications of Universal Frequency Translation," directed to related subject matter.

Documents AM13, AJ14, AK14, AM21, AJ22 and AQ51 were cited by an Examiner in Japanese Patent Application No. 2000-577,765, filed June 21, 2000, entitled "Method and System for Ensuring Reception of a Communications Signal," directed to related subject matter.

Documents AL14, AM14, AJ15 and AK15 were cited by an Examiner in Japanese Patent Application No. 2000-577,761, filed June 20, 2000, entitled "Method and System for Frequency Up-conversion," directed to related subject matter.

Documents AL15, AM15, AJ16-AM16, AJ17-AM17, AJ20, and AK23 were cited by an Examiner in Japanese Patent Application No. 2000-577,764, filed June 21, 2000, entitled "Applications of Frequency Translation," directed to related subject matter.

Documents AJ18-AL18, AB47, AC47, AE47-AG47, AB48, and AC49 were cited by an Examiner in U.S. Patent Application No. 09/489,675, filed January 24, 2000, entitled "Bar Code Scanner Using Universal Frequency Translation Technology for Up-Conversion and Down-Conversion," directed to related subject matter.

Documents AK19 and AF48 were cited in a search report in PCT Application No. PCT/US01/15111, filed October 5, 2001, entitled "Method and Apparatuses Relating to a Universal Platform Module and Enabled by Universal Frequency Translation Technology," directed to related subject matter.

Documents AJ20, AM25, AJ26, and AK26 were cited by an Examiner in Japanese Patent Application No. 2002-048676, filed October 18, 1999, entitled "Integrated Frequency Translation and Selectivity with a Variety of Filter Embodiments," directed to related subject matter.

Documents AK20, AL20, AJ21, AK21, AL21, AE42, AP56 and AQ56 were cited in a search report in PCT Application No. PCT/US01/12086, filed April 13, 2001, entitled, "Frequency Converter," directed to related subject matter.

Documents AI23, AL26, AD29, AF72-AI72, AA73-AG73, and AB82-AE82 were cited by an Examiner in U.S. Patent Application No. 10/305,299, filed November 27, 2002, entitled "Method and Apparatus for Improving Dynamic Range In a Communication System," directed to related subject matter.

Documents AI23, AB30, AB60-AE60, AC65, AB70, AC70, AG79, AD90, and AF91 were cited by an Examiner in U.S. Patent Application No. 09/569,045, filed May 10, 2000, entitled "Methods and Apparatuses Relating to a Universal Platform Module and Enabled by Universal Frequency Translation Technology," directed to related subject matter.

Document AI23 and AD46 were cited by an Examiner in U.S. Patent Application No. 09/293,095, filed April 16, 1999, entitled "Method and System for

Down-Converting an Electromagnetic Signal Having Optimized Switch Structures," directed to related subject matter.

Documents AI23, AH50, AB55, AI59, and AA60 were cited by an Examiner in U.S. Patent Application No. 09/525,185, filed March 14, 2000, entitled "Spread Spectrum Applications of Universal Frequency Translation Technology," directed to related subject matter.

Documents AI23, AI59, AF60-AH60, and AA65 were cited by an Examiner in U.S. Patent Application No. 09/590,955, filed June 9, 2000, entitled "Phase-Shifting Applications of Universal Frequency Translation," directed to related subject matter.

Documents AJ23 and AB52 were cited in an Invitation to Pay Additional Fees in PCT Application No. PCT/US01/43077, filed November 14, 2001, entitled "Method and Apparatus for a Parallel Correlator and Applications Thereof," directed to related subject matter.

Documents AL23, AH47, AB49, AG51, AF56-AH56, AO59, and AE61 were cited by an Examiner in U.S. Patent Application No. 09/669,634, filed September 26, 2000, entitled "High Frequency Translator and Method of High Frequency Translation," directed to related subject matter.

Documents AM23 and AB30 were cited by an Examiner in German Patent Application No. 19983659.0, filed October 18, 1999, entitled "Method and System for Frequency Up-Conversion," directed to related subject matter.

Documents AC24, AD47, AA48, and AB50 were cited by an Examiner in U.S. Patent Application No. 09/376,509, filed August 18, 1999, entitled "Method and

System for Ensuring Reception of a Communications Signal," directed to related subject matter.

Documents AM26, AJ27, and AK27 were cited by the Japanese Patent Office in Japanese Patent Appl. No. 2000-577764, filed October 18, 1999, entitled "Applications of Universal Translation," directed to related subject matter.

Documents AG27, AH47, AI47, AC52, AC56, AE64, AI65, AA66-AG66, and AD68-AG68 were cited by an Examiner in U.S. Patent Application No. 09/855,851, filed May 16, 2001, entitled "Apparatus, System, and Method for Down-Converting and Up-Converting Electromagnetic Signals," directed to related subject matter.

Documents AL27, AM27, AJ28-AL28, AI81, and AA82 were cited by the Israeli Patent Office in Israeli Patent Appl. No. 145,908, filed April 14, 2000, entitled "Device for Frequency Down-Converting Using Undersampling, and Method," directed to related subject matter.

Documents AD28, AD83, AD86, and AE86 were cited by an Examiner in U.S. Patent Appl. No. 11/356,419, filed February 17, 2006, entitled "Gain Control in a Communication Channel," directed to related subject matter.

Documents AM28 and AJ29 were cited by an Examiner in Japanese Patent Application No. 2002-054734, filed October 20, 1999, entitled "Method and System for Down-Converting an Electromagnetic Signal," directed to related subject matter.

Document AK29 was cited by an Examiner in Japanese Patent Application No. 2003-015382, filed October 18, 1999, entitled "Applications of Universal Frequency Translation," directed to related subject matter.

Document AL29 was cited by an Examiner in Japanese Patent Application No. 2000-613067, filed April 14, 2000, entitled "Device for Frequency Down-Converting Using Undersampling, and Method," directed to related subject matter.

Documents AH34 and AI67 were cited by an Examiner in U.S. Patent Application No. 09/796,824, filed March 2, 2001, entitled "Phased Array Antenna Applications of Universal Frequency Translation," directed to related subject matter.

Documents AH34, AG56, AI78, and AD87 were cited by an Examiner in U.S. Patent Application No. 11/404,957, filed April 17, 2006, entitled "Spread Spectrum Applications of Universal Frequency Translation," directed to related subject matter.

Documents AD35, AB44, AC44, AE46-AI46, and AA47 were cited by an Examiner in U.S. Patent Application No. 09/293,342, filed April 16, 1999, entitled "Method and System for Down-Converting Electromagnetic Signals Including Resonant Structures for Enhanced Energy Transfer," directed to related subject matter.

Documents AR35, AH79, AF82, and AG82 were cited by an Examiner in U.S. Patent Application No. 10/453,622, filed June 4, 2003, entitled "Active Polyphase Inverter Filter for Quadrature Signal Generation," directed to related subject matter.

Documents AA38 and AG48 were cited by an Examiner in U.S. Patent Application No. 09/476,091, filed January 3, 2000, entitled "Image-Reject Down-Converter and Embodiments Thereof, Such as the Family Radio Service," directed to related subject matter.

Documents AA39, AG39, and AC74-AG74 were cited by an Examiner in U.S. Patent Application No. 11/068,370, filed March 1, 2005, entitled "Method and System for Frequency Up-Conversion with a Variety of Transmitter Configurations," directed to related subject matter.

Documents AI43, AH47 and AH48 were cited by an Examiner in U.S. Patent Application No. 09/293,283, filed April 16, 1999, entitled "Integrated Frequency Translation and Selectivity with a Variety of Filter Embodiments," directed to related subject matter.

Documents AI43, AH47, AH48, AB49, AG51, and AB69-AD69 were cited by an Examiner in U.S. Patent Application No. 10/359,636, filed February 7, 2003, entitled "Integrated Frequency Translation and Selectivity," directed to related subject matter.

Documents AC45, AC51, AE55, AH59, AB65, AH65, AH66, AE80, AD81, and AE81 were cited by an Examiner in U.S. Patent Application No. 10/914,337, filed August 10, 2004, entitled "Method And System For Down-Converting And Up-Converting An Electromagnetic Signal, And Transforms For Same," directed to related subject matter.

Documents AC46 and AA48 were cited by an Examiner in U.S. Patent Application No. 09/670,831, filed September 28, 2000, entitled "Universal Frequency Translation, Embodiments Thereof, and a Web Site and Web Pages Directed to Same," directed to related subject matter.

Documents AH47, AI47, AA48-AE48, AB49, AF51, AG51, AC52, AG54, AF55, AC56, AD56, AI56, AA57, AD64, AE64, AB65, AH65, AH66, AI66, AA70, AA71, AG71-AI71, AC72, AH73, AI73, AI74, AA75, AB75, AA77-AE77, AH78, AI78, AA79, AD80-AI80, AA81-AC81, AH82, AI82, AA83, AG83-AI83, AA84, AH85, AI85, AA86-AC86, AE89-AG89, AF90-AI990, AA91-AC91, AE91, and AI91 are co-owned patents and patent application publications which are directed to related subject matter.

Documents AI47, AH50, AF55, AC56, AD56, AI56, AA57, and AH59 were cited by an Examiner in U.S. Patent Application No. 09/838,387, filed April 20, 2001, entitled "Method and System for Down-Converting and Up-Converting an Electromagnetic Signal, and Transforms for Same," directed to related subject matter.

Documents AB48, AD48, AH54, AI54, and AA55-AC55 were cited by an Examiner in U.S. Patent Application No. 09/548,923, filed April 13, 2000, entitled "Method and System for Frequency Conversion with Modulation Embodiments," directed to related subject matter.

Documents AB48, AE48, AD56, AI56, AG651, and AH61 were cited by an Examiner in U.S. Patent Application No. 09/525,615, filed March 14, 2000, entitled "Method, System, and Apparatus for Balanced Frequency Up-conversion of a Baseband Signal," directed to related subject matter.

Documents AB48, AI79, AB80, and AC80 were cited by an Examiner in U.S. Patent Application No. 10/086,367, filed March 4, 2002, entitled "Method and System for Frequency Up-Conversion," directed to related subject matter.

Documents AI48, AA49, and AF50 were cited by an Examiner in U.S. Patent Application No. 09/567,963, filed May 10, 2000, entitled "Frequency Synthesizer Using Universal Frequency Translation Technology," directed to related subject matter.

Documents AD49-AI49, AE51, AB67, and AF78 were cited by an Examiner in U.S. Patent Application No. 09/476,092, filed January 3, 2000, entitled "Analog Zero IF FM Decoder and Embodiments Thereof, Such as the Family Radio Service," directed to related subject matter.

Documents AI49, AH50, AI50, AA51, AB51, AI62, AA63, and AB63 were cited by an Examiner in U.S. Patent Application No. 09/632,857, filed August 4, 2000, entitled "Wireless Local Area Network (WLAN) Technology and Applications Including Techniques of Universal Frequency Translation," directed to related subject matter.

Documents AC50-AE50, AG50, AI50 and AC51 were cited by an Examiner in U.S. Patent Application No. 09/476,330, filed January 3, 2000, entitled, "Multi-Mode, Multi-Band Communication System," directed to related subject matter.

Documents AH50, AA51 and AB51 were cited in by an Examiner in U.S. Patent Application No. 09/526,041, filed March 14, 2000, entitled, "DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," directed to related subject matter.

Documents AH50, AC53-AI53, and AF61 were cited by an Examiner in U.S. Patent Application No. 09/476,093, filed January 3, 2000, entitled "Family Radio

System with Multi-Mode and Multi-Band Functionality," directed to related subject matter.

Documents AH50 and AB57-AE57 were cited by an Examiner in U.S. Patent Application No. 09/567,978, filed May 10, 2000, entitled "Carrier and Clock Recovery Using Universal Frequency Translation," directed to related subject matter.

Documents AH51, AB56, AE56, AN58-AP58, AN59, AP59, AG63, AC67-AF67, and AH74 were cited by an Examiner in U.S. Patent Application No. 09/567,977, filed May 10, 2000, entitled "Optical Down-converter Using Universal Frequency Translation Technology," directed to related subject matter.

Documents AA52, AF52, AI52, and AG59 were cited by an Examiner in U.S. Patent Application No. 10/289,377, filed November 7, 2002, entitled "Method and Apparatus for Reducing DC Offsets in a Communication System," directed to related subject matter.

Documents AD52-AG52 and AC63-AF63 were cited by an Examiner in U.S. Patent Application No. 09/986,764, filed November 9, 2001, entitled "Method and Apparatus for Reducing DC Offsets in a Communication System," directed to related subject matter.

Documents AA52, AE52, AH52, AI52, AA53, and AB53 were cited in a search report in PCT Application No. PCT/US02/35861, filed November 8, 2002, entitled "Method and Apparatus for Reducing DC Offsets in a Communication System," directed to related subject matter.

Documents AA54-AD54 were cited in a search report in a related PCT Application No. PCT/US03/16403, filed May 27, 2003, entitled "Method and Apparatus for DC Offset Removal in a Radio Frequency Communication Channel," directed to related subject matter.

Documents AB54, AI61, AA62, and AB62 were cited in a written opinion in PCT Application No. PCT/US03/16403, filed May 27, 2003, entitled "Method and Apparatus for DC Offset Removal in a Radio Frequency Communication Channel," directed to related subject matter.

Documents AB54, AQ59, AI61, and AA62-AH62 were cited by an Examiner in U.S. Patent Application No. 10/290,323, filed November 8, 2002, entitled "Method and Apparatus for DC Offset Removal in a Radio Frequency Communication Channel," directed to related subject matter.

Documents AE54, AF54, AH55, AI60, AA61, AB61, and AA67 were cited by an Examiner in U.S. Patent Application No. 09/550,642, filed April 14, 2000, entitled "Method and System for Down-converting an Electromagnetic Signal, and Transforms for Same," directed to related subject matter.

Documents AD55 and AE55 were cited by an Examiner in U.S. Patent Application No. 09/543,867, filed April 5, 2000, entitled "Automated Meter Reader Applications of Universal Frequency Translation," directed to related subject matter.

Documents AG55 and AH55 were cited by an Examiner in U.S. Patent Application No. 10/317,181, filed December 12, 2002, entitled "Differential

Frequency Down-Conversion Using Techniques of Universal Frequency Translation Technology," directed to related subject matter.

Documents AI55, AA56, AC61, and AD61 were cited by an Examiner in U.S. Patent Application No. 10/317,165, filed December 12, 2002, entitled "Method and Apparatus for Reducing DC Offsets in Communication Systems Using Universal Frequency Translation Technology," directed to related subject matter.

Document AC56, AH65, AD77, AG84, and AB90 were cited by an Examiner in U.S. Patent Application No. 11/015,653, filed December 20, 2004, entitled "Method, System, And Apparatus For Balanced Frequency Up-Conversion, Including Circuitry To Directly Couple The Outputs Of Multiple Transistors," directed to related subject matter.

Documents AG56, AH56, AH68, AI68, and AA69 were cited by an Examiner in U.S. Patent Application No. 10/315,174, filed December 10, 2002, entitled "Reducing DC Offsets Using Spectral Spreading," directed to related subject matter.

Documents AF57 and AG57 were cited by an Examiner in U.S. Patent Application No. 10/330,219, filed December 30, 2002, entitled "Methods and Systems for Down-Converting Electromagnetic Signals, and Applications Thereof," directed to related subject matter.

Documents AH57, AI57, AA58-AI58, and AA59 were cited by an Examiner in U.S. Patent Application No. 09/566,188, filed May 5, 2000, entitled "Integrated Frequency Translation and Selectivity with Gain Control Functionality, and Applications Thereof," directed to related subject matter.

Documents AB59 and AC59 were cited by an Examiner in U.S. Patent Application No. 09/632,856, filed August 4, 2000, entitled "Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments and Circuit Implementation," directed to related subject matter.

Documents AB59, AH86, AI86, AA90, and AD91 were cited by an Examiner in U.S. Patent Application No. 11/390,153, filed March 28, 2006, entitled "Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same," directed to related subject matter.

Documents AN60, AD71, and AC75 were cited by an Examiner in U.S. Patent Application No. 10/197,253, filed July 18, 2002, entitled "Networking Methods and Systems," directed to related subject matter.

Documents AO62, AC79-AF79 were identified in a search relating to related U.S. Patent Application No. 11/582,367, filed October 18, 2006, entitled "Apparatus and Method for Communicating an Input Signal in Polar Representation," directed to related subject matter.

Documents AH63, AI63, AA64, and AB64 were cited by an Examiner in U.S. Patent Application No. 09/987,193, filed November 13, 2001, entitled "Method and Apparatus for a Parallel Correlator and Applications Thereof," directed to related subject matter.

Document AC64 was cited by an Examiner in U.S. Patent Application No. 09/632,857, filed August 4, 2000, entitled "Wireless Local Area Network (WLAN)

Technology and Applications Including Techniques of Universal Frequency Translation," directed to related subject matter.

Documents AF64 and AG64 were cited by an Examiner in U.S. Patent Application No. 10/289,377, filed November 7, 2002, entitled "Method and Apparatus for Reducing DC Offsets in A Communication System," directed to related subject matter.

Document AI64 was cited by an Examiner in U.S. Patent Application No. 10/086,250, filed March 4, 2002, entitled "Applications of Universal Frequency Translation," directed to related subject matter.

Documents AI64, AC72, AI75, and AA76-AD76 were cited by an Examiner in U.S. Patent Application No. 11/230,732, filed September 21, 2005, entitled "Applications of Universal Frequency Translation," directed to related subject matter.

Documents AB65, AA72 and AB72 were cited by an Examiner in U.S. Patent Application No. 10/394,069, filed March 24, 2003, entitled "Method and Circuit for Down-Converting a Signal," directed to related subject matter.

Documents AD65-AG65 were cited by an Examiner in U.S. Patent Application No. 09/770,675, filed January 29, 2001, entitled "Wireless and Wired Cable Modem Applications of Universal Frequency Translation Technology," directed to related subject matter.

Documents AG65, AE69-AI69, AA74, AB74, AE83, AF83, and AA87-AC87 were cited by an Examiner in U.S. Patent Application No. 10/197,255, filed July 18, 2002, entitled "Networking Methods and Systems," directed to related subject matter.

Documents AH65 and AD70-AI70 were cited by an Examiner in U.S. Patent Application No. 10/961,272, filed October 12, 2004, entitled "Apparatus, System, And Method For Down-Converting And Up-Converting Electromagnetic Signals," directed to related subject matter.

Documents AG67 and AH67 were cited by an Examiner in U.S. Patent Application No. 09/632,855, filed August 4, 2000, entitled "Wireless Local Area Network (WLAN) Using Universal Frequency Translation Technology Including Multi-Phase Embodiments," directed to related subject matter.

Documents AA68-AC68, AF77-AI77, and AA78-AE78 were cited by an Examiner in U.S. Patent Application No. 10/318,207, filed December 13, 2002, entitled "Method and Apparatus for Reducing Re-Radiation Using Techniques of Universal Frequency Translation Technology," directed to related subject matter.

Documents AF70 and AE76-AI76 were cited by an Examiner in U.S. Patent Application No. 10/961,253, filed October 12, 2004, entitled "Apparatus, System, and Method for Down Converting and Up Converting Electromagnetic Signals," directed to related subject matter.

Documents AB71, AC71, AD75, and AF86 were cited by an Examiner in U.S. Patent Application No. 09/550,644, filed April 14, 2000, entitled "Method And System For Down-Converting An Electromagnetic Signal, Transforms For Same, And Aperture Relationships," directed to related subject matter.

Documents AB72, AD72, AE72, and AG78 were cited by an Examiner in U.S. Patent Application No. 11/173,021, filed July 5, 2005, entitled "Method and Circuit for Down-Converting a Signal," directed to related subject matter.

Documents AE75-AH75 were cited by an Examiner in U.S. Patent Application No. 11/107,861, filed April 18, 2005, entitled "Method and Apparatus for a Parallel Correlator and Applications Thereof," directed to related subject matter.

Documents AB78, AB84-AF84, AE85, AF85, AH89, and AI89 were cited by an Examiner in U.S. Patent Application No. 11/826,416, filed July 16, 2007, entitled "Method and System for Frequency Up-Conversion with Modulation Embodiments," directed to related subject matter.

Document AB79 was cited in an International Search Report and Written Opinion in PCT Application No. PCT/US2004/013813, filed April 30, 2004, entitled "Real-Time Wireless Exchange of Objects," directed to related subject matter.

Document AA80 was cited by an Examiner in U.S. Patent Application No. 11/020,547, filed December 27, 2004, entitled "Methods and Systems for Down-Converting a Signal Using a Complementary Transistor Structure," directed to related subject matter.

Documents AF81-AH81 were cited by an Examiner in U.S. Patent Application No. 11/355,167, filed February 16, 2006, entitled "Methods and Systems for Down-Converting a Signal Using a Complementary Transistor Structure," directed to related subject matter.

Documents AB83, AC83, AD85, and AG86 were cited by an Examiner in U.S. Patent Application No. 11/802,389, filed May 22, 2007, entitled "Method And System For Frequency Up-Conversion," directed to related subject matter.

Documents AG84 and AG85 were cited by an Examiner in U.S. Patent Application No. 11/292,118, filed December 2, 2005, entitled "Methods and Systems for Utilizing Universal Frequency Translators for Phase and/or Frequency Detection," directed to related subject matter.

Documents AH84, AI84 and AA85-AC85 were cited by an Examiner in U.S. Patent Application No. 10/973,917, filed October 27, 2004, entitled "Universal Platform Module And Methods And Apparatuses Relating Thereto Enabled By Universal Frequency Translation Technology," directed to related subject matter.

Documents AE87, AF87, and AE90 were cited by an Examiner in U.S. Patent Application No. 11/358,395, filed February 22, 2006, entitled "Apparatus and Method of Differential IQ Frequency Up-Conversion," directed to related subject matter.

Documents AG87-AI87, AA88-AI88, AA89, AG91, and AH91 were cited by an Examiner in U.S. Patent Application No. 10/961,342, filed October 12, 2004, entitled "Apparatus, System, and Method for Down Converting and Up Converting Electromagnetic Signals," directed to related subject matter.

Documents AB89-AD89 were cited by an Examiner in U.S. Patent Application No. 11/582,367, filed October 18, 2006, entitled "Apparatus and Method for Communicating an Input Signal in Polar Representation," directed to related subject matter.

Document AC90 was cited by an Examiner in U.S. Patent Application No. 11/404,957, filed April 17, 2006, entitled "Spread Spectrum Applications of Universal Frequency Translation," directed to related subject matter.

The other documents in the PTO-1449 do not fall within the above categories.

It is noted that some of these documents could be classified in more than one of the above categories.

This statement should not be construed as a representation that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below.

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.

☐ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

☒ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing

date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☒ c. Attached is our PTO-2038 Credit Card Payment Form in the amount of $180.00 in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Enclosed find our PTO-2038 Credit Card Payment Form in

the amount of $_____ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

☒ 6. Concise explanations of the relevance of the non-English language documents AJ1, AK1, AJ6, AK7, AJ8-AL8, AK11-AM11, AJ12, AM13, AJ14-AM14,

AJ15-AM15, AJ16-AM16, AJ17-AM17, AJ18-AL18, AJ20-AL20, AK21, AM21, AJ22, AK23, AL23, AM23, AK24-AM24, AJ25-AL25, AJ26-AM26, AJ27-AM27, AJ28-AM28, AJ29-AL29, AQ50, and AQ51 appear below:

Document AJ1 (DE 42 37 692 C1) appears to be a receiver for a digital radio signal. Document AJ1 is a counterpart German application of document AG28, which is in the English language.

Document AK1 (EP 0 035 166 A1) appears to describe a digitized receiver. An English language abstract of document AK1 is enclosed as document AQ8.

Document AJ6 (EP 0 785 635 A1) appears to describe a method and apparatus for frequency diversity transmission using a plurality of uncorrelated carriers. An English language abstract of document AJ6 is enclosed as document AP8.

Document AK7 (FR 2 743 231 A1) is the corresponding French application of document AJ6 (EP 0 785 635 A1), which is described above.

Document AJ8 (JP 2-39632) appears to describe a transmitter for frequency diversity. An English language abstract of document AJ8 is enclosed as document AO8.

Document AK8 (JP 2-131629) appears to describe a transmitter-receiver for frequency diversity. An English language abstract of document AK8 is enclosed as document AN8.

Document AL8 (JP 2-276351) appears to describe an FSK demodulating circuit. An English language abstract of document AL8 is enclosed as document AR7.

Document AK11 (FR 2245130) appears to describe a converter. A partial English language translation of document AK11 is enclosed as document AP50.

Document AL11 (DE 3541031) appears to describe a method and device for demodulating high-frequency modulated signals. An English language translation of document AL11 is enclosed as document AR50.

Document AM11 (EP 0 732 803) appears to describe a procedure and device for demodulation by sampling. An English translation of document AM11 is enclosed as document AN51.

Document AJ12 (DE 19735798) appears to describe a transceiver. An English translation of document AJ12 is enclosed as document AP51.

Document AM13 (JP 56-114451) appears to describe a system for diversity radio transmission. Document AM13 is a counterpart Japanese application of document AF8, which is in the English language.

Document AJ14 (JP 8-32556) appears to describe a data transmitter-receiver. An English language abstract of document AJ14 is enclosed as document AO52.

Document AK14 (JP 8-139524) appears to describe a frequency converting circuit and radio communication device. An English language abstract of document AK14 is enclosed as document AP52.

Document AL14 (JP 59-144249) appears to describe a pulse signal transmission system. An English language abstract of document AL14 is enclosed as document AQ52.

Document AM14 (JP 63-54002) appears to describe a microwave burst signal generator which incorporates a FET frequency multiplier. An English language abstract of document AM14 is enclosed as document AR52.

Document AJ15 (JP 6-237276) appears to describe a quadrature modulator. An English language abstract of document AJ15 is enclosed as document AN53.

Document AK15 (JP 8-23359) appears to describe a digital quadrature modulation device. An English language abstract of document AK15 is enclosed as document AO53.

Document AL15 (JP 47-2314) appears to describe a demodulator. An English language translation of document AL15 is enclosed as document AP53.

Document AM15 (JP 58-7903) appears to describe a switched capacitor modulator. A partial English language translation of document AM15 is enclosed as document AQ53.

Document AJ16 (JP 58-133004) appears to describe an amplitude detector. An English language abstract of document AJ16 is enclosed as document AR53.

Document AK16 (JP 60-58705) appears to describe a frequency converting circuit. An English language abstract of document AK16 is enclosed as document AN54.

Document AL16 (JP 4-123614) appears to describe a level converting circuit. An English language abstract of document AL16 is enclosed as document AO54.

Document AM16 (JP 4-127601) appears to describe a frequency conversion circuit. An English language abstract of document AM16 is enclosed as document AP54.

Document AJ17 (JP 5-175730) appears to describe a time division direct receiver. An English language abstract of document AJ17 is enclosed as document AQ54.

Document AK17 (JP 5-175734) appears to describe an FM demodulator. An English language abstract of document AK17 is enclosed as document AR54.

Document AL17 (JP 7-154344) appears to describe a receiver for receiving modulated carrier signals and an IQ mixer/demodulator using it's receiving constitution. An English language abstract of document AL17 is enclosed as document AN55.

Document AM17 (JP 7-307620) appears to describe a bottom detection circuit. An English language abstract of document AM17 is enclosed as document AO55.

Document AJ18 (JP 55-66057) appears to describe a bar-code detection circuit. An English language abstract of document AJ18 is enclosed as document AQ55.

Document AK18 (JP 63-65587) appears to describe a wireless light pen device. An English language abstract of document AK18 is enclosed as document AR55.

Document AL18 (JP 63-153691) appears to describe a data transfer for a semiconductor data carrier system. An English language abstract of document AL18 is enclosed as document AN56.

Document AJ20 (JP 60-130203) appears to describe a frequency converter. An English language abstract of document AJ20 is enclosed as document AO56.

Document AK20 (DE 196 27 640 A1) appears to describe a mixer. Document AK20 is a counterpart German application of document AA33, which is in the English language.

Document AL20 (EP 0 087 336 A1) appears to describe a transistorized mixer for microwave transmitters. The granted version of document AL20 is cited as document AM20 (EP 0 087 336 B1) and contains an English language version of the claims.

Document AK21 (FR 2 669 787 A1) appears to describe a symmetrical super high frequency mixer. An English language abstract of document AK21 is enclosed as document AR56.

Document AM21 (JP 61-30821) appears to describe a squelch device. An English language abstract of document AL21 is enclosed as document AP57.

Document AJ22 (JP 5-327356) appears to describe a frequency converter. An English language abstract of document AJ22 is enclosed as document AQ57.

Document AK23 (JP 9-36664) appears to describe a frequency conversion circuit. An English language abstract of document AK23 is enclosed as document AR58.

Document AL23 (DE 196 48 915 A1) appears to describe a process of frequency conversion. An English language translation of document AL23 is enclosed as document AO59.

Document AM23 (DE 692 21 098 T2) appears to describe a radiofrequency frequency multiplier comprising an automatic level control circuit. An English-language abstract of document AM23 is enclosed as document AR59. It is also noted that document AM23 is a counterpart of European Patent Publication EP 0 548 542 A1, which is in the English language and is listed as document AM4.

Document AK24 (DT 1936252) appears to describe a modulator or demodulator in integrated technology. An English language translation of document AK24 is enclosed as document AO60.

Document AL24 (JP 62-12381) appears to describe a pulse-width modulation control system of an inverter. An English language abstract of document AL24 is enclosed as document AP60.

Document AM24 (JP 4-154227) appears to describe a relay monitoring device for broadcasting radio waves. An English language abstract of document AM24 is enclosed as document AQ60.

Document AJ25 (JP 6-284038) appears to describe a transceiver. An English language abstract of document AJ25 is enclosed as document AR60.

Document AK25 (JP 10-96778) appears to describe a distance measuring device. An English language abstract of document AK25 is enclosed as document AN61.

Document AL25 (JP 11-98205) appears to describe a demodulator for digital radio communication. An English language abstract of document AL25 is enclosed as document AO61.

Document AM25 (JP 61-232706) appears to describe a frequency converter for signals. An English language abstract of document AM25 is enclosed as document AP61.

Document AJ26 (JP 9-171399) appears to describe a sound synthesizing method and circuit. An English language abstract of document AJ26 is enclosed as document AQ61.

Document AK26 (JP 10-41860) appears to describe an echo canceller. An English language abstract of document AK26 is enclosed as document AR61.

Document AL26 (JP 10-173563) appears to describe an up-down tuner. An English language translation of document AL26 is enclosed as document AN62.

Document AM26 (JP 58-031622) appears to describe a frequency converting circuit. An English language abstract of document AM26 is enclosed as document AP62.

Document AJ27 (JP 61-245749) appears to describe a PCM signal transmission system for CATV. An English language abstract of document AJ27 is enclosed as document AQ62.

Document AK27 (JP 64-048557) appears to describe a circuit for reforming and modulating at least two data signals. An English language abstract of document AK27 is enclosed as document AR62.

Document AL27 (JP 59-022438) appears to describe a bipolar analog-frequency converting circuit. An English language abstract of document AL27 is enclosed as document AN63.

Document AM27 (JP 59-123318) appears to describe an analog-digital converting circuit. An English language abstract of document AM27 is enclosed as document AO63.

Document AJ28 (JP 61-193521) appears to describe an analog-digital converting circuit. An English language abstract of document AJ28 is enclosed as document AP63.

Document AK28 (JP 62-047214) appears to describe a digital-analog converting circuit. An English language abstract of document AK28 is enclosed as document AQ63.

Document AL28 (JP 63-274214) appears to describe a digital/analog converting circuit. An English language abstract of document AL28 is enclosed as document AR63.

Document AM28 (JP 7-169292 A) appears to describe a CMOS sample-and-hold circuit. An English language abstract of document AM28 is enclosed as document AN64.

Document AJ29 (JP 10-22804 A) appears to describe a waveform-shaping circuit and sample-and-hold circuit having the same. An English language abstract of document AJ29 is enclosed as document AO64.

Document AK29 (JP 8-288882 A) appears to describe a high frequency circuit for digital mobile communication equipment. An English language abstract of document AK29 is enclosed as document AP64.

Document AQ50 (Fest et al.) appears to discuss analog-digital converters. An English language translation of document AQ50 is enclosed as document AO51.

Document AQ51 (Miki et al.) appears to describe modulation systems. A partial English language translation of document AQ51 is enclosed as document AR51.

☒ 7. In accordance with 37 C.F.R. § 1.98(a)(2), copies of the U.S. patents and patent application publications cited on the attached Form PTO-1449 are not enclosed.

☒ 8. Copies of Foreign Patent documents AM28 and AJ29-AL29, and Non Patent Literature documents AN64-AP64 are enclosed. However, copies of the remaining listed Foreign Patent documents and Non Patent Literature Documents were cited by or submitted to the Patent Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application Nos. 09/550,644, filed April 14, 2000 (now Pat. No. 7,515,896), 09/521,879, filed March 9, 2000, 09/293,342, filed April 16, 1999, (now Pat. No. 6,687,493), or 09/176,022, filed October 21, 1998 (now Pat. No. 6,061,551), which are relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of the 'Foreign Patent Documents' and 'Other Documents' cited in the parent applications are not enclosed. 37 C.F.R. § 1.98(d).

☒ 9. It is expected that the examiner will review the prosecution and cited art in parent Application Nos. 09/550,644, filed April 14, 2000 (now Pat. No. 7,515,896), 09/521,879, filed March 9, 2000, 09/293,342, filed April 16, 1999, (now Pat. No. 6,687,493), and 09/176,022, filed October 21, 1998 (now Pat. No. 6,061,551), and indicate in the next communication from the office that the art cited in the earlier prosecution histories has been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

Atty. Docket: 1744.001000P

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
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Date: 2/3/2010

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1075370_1.DOC

Atty. Docket: 1744.001000P

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/349,802	01/07/2009	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 02/03/2010	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/TYWANA P. LOVELACE/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 5719
SORRELLS *et al.*	Art Unit: 2617
Appl. No.: 12/349,802	Examiner: Bhattacharya, Sam
Filed: January 7, 2009	Atty. Docket: 1744.001000P
For: **Method and System For Down-Converting An Electromagnetic Signal, Transforms For Same, and Aperture Relationships**	

Amendment and Reply Under 37 C.F.R. § 1.111

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the Office Action dated October 29, 2009, (PTO Prosecution File Wrapper Paper No. 20091022), Applicants submit the following Amendment and Remarks.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks and Arguments begin on page 7 of this paper.

It is not believed that extensions of time or fees for net addition of claims are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net

addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1-12. (Canceled)

13. (New) A system for down-converting an electromagnetic signal, comprising:

a first matched filtering/correlating module that receives an input signal, wherein said first matched filtering/correlating module down-converts said input signal according to a first control signal and outputs a first down-converted signal;

a second matched filtering/correlating module that receives said input signal, wherein said second matched filtering/correlating module down-converts said input signal according to a second control signal and outputs a second down-converted signal; and

a first combiner module that combines said second down-converted signal and said first down-converted signal and outputs a first channel down-converted signal.

14. (New) The system of claim 13, wherein said input signal is a RF carrier signal that is AM, FM, or PM modulated with an information signal.

15. (New) The system of claim 14, wherein said first channel down-converted signal is a baseband signal.

16. (New) The system of claim 14, wherein said first channel down-converted signal is an intermediate frequency signal.

17. (New) The system of claim 13, further comprising:

a third matched filtering/correlating module that receives an input signal, wherein said third matched filtering/correlating module down-converts said input signal according to a third control signal and outputs a third down-converted signal;

a fourth matched filtering/correlating module that receives said input signal, wherein said fourth matched filtering/correlating module down-converts said input signal according to a fourth control signal and outputs a fourth down-converted signal; and

a second combiner module that combines said fourth down-converted signal and said third down-converted signal and outputs a second channel down-converted signal.

18. (New) The system of claim 17, wherein said first combiner module and said second combiner module each comprise a differential amplifier.

19. (New) The system of claim 17, further comprising:

a first filter that filters said first down-converted signal;

a second filter that filters said second down-converted signal;

a third filter that filters said third down-converted signal; and

a fourth filter that filters said fourth down-converted signal.

20. (New) The system of claim 19, wherein said first, second, third, and fourth filters each comprise a low-pass filter.

21. (New) The system of claim 20, wherein each said low-pass filter comprises a resistor and a capacitor.

22. (New) The system of claim 17, further comprising a low-noise amplifier that amplifies said input signal.

23. (New) The system of claim 17, wherein said input signal comprises an RF I/Q modulated signal.

24. (New) The system of claim 23, wherein said first channel down-converted signal comprises an I-phase information signal portion of said RF I/Q modulated signal, and wherein said second channel down-converted signal comprises a Q-phase information signal portion of said RF I/Q modulate signal.

25. (New) The system of claim 24, wherein a second control signal pulse of said second control signal occurs 1.5 cycles of a frequency of said input signal after the occurrence of a first control signal pulse of said first control signal;

wherein a fourth control signal pulse of said fourth control signal occurs 1.5 cycles of said frequency of said input signal after the occurrence of a third control signal pulse of said fourth control signal; and

wherein said third control signal pulse occurs .75 cycles of said frequency of said input signal after the occurrence of said first control signal pulse.

26. (New) A method for down-converting an electromagnetic signal, comprising:

receiving an input signal at a first matched filtering/correlating module;

down converting said input signal at said first matched filtering/correlating module according to a first control signal and outputting a first down-converted signal;

receiving said input signal at a second matched filtering/correlating module;

down-converting said input signal at said second matched filtering/correlating module according to a second control signal and outputting a second down-converted signal; and

combining said second down-converted signal and said first down-converted signal to output a first channel down-converted signal.

27. (New) An article of manufacture including a computer-readable medium having instructions stored thereon that, if executed by a computing device, cause said computing device to perform operations comprising:

receiving an input signal at a first matched filtering/correlating module;

down converting said input signal at said first matched filtering/correlating module according to a first control signal and outputting a first down-converted signal;

receiving said input signal at a second matched filtering/correlating module;

down-converting said input signal at said second matched filtering/correlating module according to a second control signal and outputting a second down-converted signal; and

combining said second down-converted signal and said first down-converted signal to output a first channel down-converted signal.

Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 13-27 are pending in the application, with claims 13, 26 and 27 being the independent claims. Claims 1-12 are sought to be canceled without prejudice to or disclaimer of the subject matter therein. New claims 13-27 are sought to be added. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Objections to the Claims

On page 2 of the Office Action, claims 4 and 7 were objected to for alleged informalities. Claims 4 and 7 have been canceled thereby rendering the objections moot. Reconsideration and withdrawal of these objections is respectfully requested.

Rejections under 35 U.S.C. § 101

On page 2 of the Office Action, claims 1, 7 and 10-12 were rejected under 35 U.S.C. § 101 for allegedly being directed to non-statutory subject matter. Claims 1, 7 and 10-12 have been canceled thereby rendering the rejections moot. Reconsideration and withdrawal of these rejections is respectfully requested.

Provisional Double Patenting Rejections

On page 3 of the Office Action claims 1-3, 5, 6, and 8-12 were provisionally rejected under 35 U.S.C. § 101 as allegedly claiming the same invention as that of claims

13-18 and 20-24 of co-pending U.S. Patent Application No. 11/390,153. On page 4 of the Office Action claims 1-3, 5, 6, and 8-12 were provisionally rejected on the ground of non-statutory obviousness type double patenting as allegedly being unpatentable over claims 13-18 and 20-24 of co-pending U.S. Patent Application No. 11/390,153.

Claims 1-3, 5, 6, and 8-12 have been canceled thereby rendering the provisional double patenting rejections moot. Reconsideration and withdrawal of these rejections is respectfully requested.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

Date: 1/28/2010

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1047776_1.DOC

Electronic Acknowledgement Receipt

EFS ID:	6899262
Application Number:	12349802
International Application Number:	
Confirmation Number:	5719
Title of Invention:	Method and System For Down-Converting An Electromagnetic Signal, And Transforms For Same, And Aperture Relationships
First Named Inventor/Applicant Name:	David F. SORRELLS
Customer Number:	26111
Filer:	Viraj Dilip Tipnis/joanne king
Filer Authorized By:	Viraj Dilip Tipnis
Attorney Docket Number:	1744.001000P
Receipt Date:	28-JAN-2010
Filing Date:	07-JAN-2009
Time Stamp:	13:30:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		1744001000PAMNDFILING.pdf	320838 f1497fb6e5539227d7373d4a54519980109bf354	yes	10

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	1
	Amendment/Req. Reconsideration-After Non-Final Reject	2	3
	Claims	4	7
	Applicant Arguments/Remarks Made in an Amendment	8	10
Warnings:			
Information:			
	Total Files Size (in bytes):	320838	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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+Admitted only in Virginia
•Practice Limited to Federal Agencies

January 28, 2010

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MLEE@SKGF.COM

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Art Unit 2617

Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Application No. 12/349,802; Filing or 371(c) Date: January 7, 2009
For: **Method and System For Down-Converting An Electromagnetic Signal, Transforms For Same, and Aperture Relationships**
Inventors: SORRELLS *et al.*
Our Ref: 1744.001000P

Sir:

Transmitted herewith for appropriate action is an Amendment and Reply Under 37 C.F.R. § 1.111. This document is being filed electronically through EFS-Web.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

MQL/VDT/jk
Enclosure

1074992_1

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/349,802	Filing Date 01/07/2009	☐ To be Mailed

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	01/28/2010	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 15	Minus	** 20	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	**0**

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/JACQUELINE E. COUPLIN/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/349,802	01/07/2009	David F. SORRELLS	1744.001000P	5719

26111 7590 10/29/2009

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
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EXAMINER	
BHATTACHARYA, SAM	
ART UNIT	PAPER NUMBER
2617	
MAIL DATE	DELIVERY MODE
10/29/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/349,802	SORRELLS ET AL.	
	Examiner	Art Unit	
	SAM BHATTACHARYA	2617	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 4 and 7 are objected to because of the following informalities: in claim 4, the terms A, □t, □ and "in accordance with" are not defined; in claim 7, u(t), T_A, ω and φ are not defined. Appropriate correction is required.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1, 7 and 10-12 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 1, 7 and 10-12 are rejected under 35 U.S.C. 101 as not falling within one of the four statutory categories of invention. Supreme Court precedent~ and recent Federal Circuit decisions indicate that a statutory "process" under 35 U.S.C. 101 must (1) be tied to another statutory category (such as a particular apparatus), or (2) transform underlying subject matter (such as an article or material) to a different state or thing. *Diamond v. Diehr,* 450 U.S. 175, 184 (1981); *Parker v. Flook,* 437 U.S. 584, 588 n.9 (1978); *Gottschalk v. Benson,* 409 U.S. 63, 70 (1972); *Cochrane v. Deener,* 94 U.S. 780, 787-88 (1876). *In reBilski,* 88 USPQ2d 1385 (Fed. Cir. 2008).

1. While the instant claim(s) recite a series of steps or acts to be performed, the claim(s) neither transform underlying subject matter nor positively tie to another statutory category that accomplishes the claimed method steps, and therefore do not qualify as a statutory process. For example, the claims simply perform an integration and accumulation operation on a signal

(which alone is considered non-statutory subject matter). There is no transformation (with regards to the signal) and the steps of the claims are not tied to another statutory category.

Double Patenting

2. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

3. Claims 1-3, 5, 6 and 8-12 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 13-18 and 20-24 of copending Application No. 11/390,153. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned

with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-3, 5, 6 and 8-12 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 13-18 and 20-24 of copending Application No. 11/390,153. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 13 of the copending application recites a finite time integrating operation, accumulating the results and repeating, with minor variations, as in claim 1; claim 14 of the copending application recites operating on an approximate half cycle of the carrier signal, as in claim 2; claim 15 of the copending application recites controlling a switch to pass an approximate half cycle, as in claim 3; claim 17 of the copending application recites transferring a portion of the energy to an energy storage device, as in claim 5; claim 18 of the copending application recites transferring a portion of the energy to a capacitive storage device, as in claim 6; claim 16 of the copending application recites an aperture impulse response duration, and accumulating energy from an approximate half cycle, as in claim 7; claim 20 of the copending application recites passing on the accumulation result to a reconstruction filter, as in claim 8; claim 21 of the copending application recites passing on the accumulation result to an interpolation filter, as in claim 9; claim 22 of the copending application recites sub-harmonic rate of the carrier signal, as in claim 10; claim 23 of the copending application recites an off-set of a sub-harmonic rate of a carrier signal, as in claim 11; and claim 24 of the copending application recites positive approximate half cycles of the carrier signal and inverted negative approximate half cycles of the carrier signal, as in claim 12.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Allowable Subject Matter

6. Claims 1-12 would be allowable if rewritten to overcome the objection and rejections in this Office action.

7. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose the recited combination of elements in down-converting an electromagnetic signal, including performing a finite time integrating operation on a portion of a carrier signal, accumulating the result and repeating for additional portions of the carrier signal, whereby the results form a down-converted signal.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Stetson, Jr. (US 5,020,745) and Hogrefe et al (US 3,740,636).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SAM BHATTACHARYA whose telephone number is (571)272-7917. The examiner can normally be reached on Weekdays, 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lester Kincaid can be reached on (571) 272-7922. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

sb
/Sam Bhattacharya/
Primary Examiner, Art Unit 2617

Notice of References Cited	Application/Control No. 12/349,802	Applicant(s)/Patent Under Reexamination SORRELLS ET AL.	
	Examiner SAM BHATTACHARYA	Art Unit 2617	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,020,745	06-1991	Stetson, Jr., John B.	244/165
*	B	US-3,740,636	06-1973	Hogrefe et al.	320/101
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12349802	SORRELLS ET AL.
	Examiner	Art Unit
	SAM BHATTACHARYA	2617

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	10/22/2009								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								
	11	✓								
	12	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12349802	SORRELLS ET AL.
	Examiner	Art Unit
	SAM BHATTACHARYA	2617

SEARCHED			
Class	Subclass	Date	Examiner
455	413,113,118,130,131,182.1,190.1,191.1,313,323,343,350	10/22/2009	sb
327	113	10/22/2009	sb
375	130,142,143,150,152,316,343	10/22/2009	sb

SEARCH NOTES		
Search Notes	Date	Examiner
East	10/22/2009	sb

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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BIB DATA SHEET

CONFIRMATION NO. 5719

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/349,802	01/07/2009 RULE	455	2617	1744.001000P

APPLICANTS

David F. SORRELLS, Jacksonville, FL;
Michael J. Bultman, Jacksonville, FL;
Robert W. Cook, Switzerland, FL;
Richard C. Looke, Jacksonville, FL;
Charley D. Moses JR., Jacksonville, FL;
Michael W. Rawlins, Lake Mary, FL;
Gregory S. Rawlins, Lake Mary, FL;

**** CONTINUING DATA ***************************

This application is a DIV of 09/550,644 04/14/2000 PAT 7,515,896
which is a CIP of 09/521,879 03/09/2000 ABN
and is a CIP of 09/293,342 04/16/1999 PAT 6,687,493
which is a CIP of 09/176,022 10/21/1998 PAT 6,061,551

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

01/21/2009

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☐ No Verified and Acknowledged /SAM BHATTACHARYA/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		FL	284	12	1

ADDRESS

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005
UNITED STATES

TITLE

Method and System For Down-Converting An Electromagnetic Signal, And Transforms For Same, And Aperture Relationships

FILING FEE RECEIVED	FEES: Authority has been given in Paper	☐ All Fees
3380	No._____ to charge/credit DEPOSIT ACCOUNT	☐ 1.16 Fees (Filing)
	No._____ for following:	☐ 1.17 Fees (Processing Ext. of time)
		☐ 1.18 Fees (Issue)
		☐ Other _____
		☐ Credit

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	12	finite adj2 time near2 integrat$3 near8 accumulat$3	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/24 16:17
L2	3634	time near2 integrat$3 near8 (accumulat$3 sum$4 add$3)	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/24 16:47
L3	14	finite adj2 time near2 integrat$3 near8 (accumulat$3 sum$4 add$3)	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/24 16:48
L4	14	(downconvert$3 or down adj2 convert$3) near8 integrat$3 near8 (accumulat$3 sum$4 add$3)	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/24 16:49
S1	12	finite adj2 time near2 integrat$3 near8 accumulat$3	US-PGPUB; USPAT; USOCR	OR	ON	2009/09/30 12:38
S2	1	("7515896").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/10/23 13:49
S3	14021	((455/413,113,118,130,131,182.1,190.1,191.1,313,323,343,350) or (327/113) or (375/130,142,143,150,152,316,343)).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/10/23 13:53
S4	1519	time near2 integrat$3 near8 accumulat$3	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/23 16:34

S5	14021	((455/413,113,118,130,131,182.1,190.1,191.1,313,323,343,350) or (327/113) or (375/130,142,143,150,152,316,343)).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/10/23 16:35
S6	66	S5 and S4	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/23 16:35
S7	12	finite adj2 time near2 integrat$3 near8 accumulat$3	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/23 16:35
S8	57	S6 not S7	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/23 16:35
S9	0	downconver$4 near7 time near2 integrat$3 near8 accumulat$3	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/23 16:40

EAST Search History (Interference)

<This search history is empty>

10/24/2009 4:50:07 PM
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/349,802	01/07/2009	David F. SORRELLS	1744.001000P

CONFIRMATION NO. 5719

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

PUBLICATION NOTICE

OC000000037650100

Title: Method and System For Down-Converting An Electromagnetic Signal, And Transforms For Same, And Aperture Relationships

Publication No.US-2009-0221257-A1
Publication Date:09/03/2009

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/349,802	01/07/2009	2618	3380	1744.001000P	12	1

CONFIRMATION NO. 5719

UPDATED FILING RECEIPT

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005



Date Mailed: 05/28/2009

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

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Michael J. Bultman, Jacksonville, FL;
Robert W. Cook, Switzerland, FL;
Richard C. Looke, Jacksonville, FL;
Charley D. Moses JR., Jacksonville, FL;
Michael W. Rawlins, Lake Mary, FL;
Gregory S. Rawlins, Lake Mary, FL;

Assignment For Published Patent Application

ParkerVision, Inc., Jacksonville, FL

Power of Attorney: The patent practitioners associated with Customer Number 26111

Domestic Priority data as claimed by applicant

This application is a DIV of 09/550,644 04/14/2000 PAT 7,515,896
which is a CIP of 09/521,879 03/09/2000 ABN
and is a CIP of 09/293,342 04/16/1999 PAT 6,687,493
which is a CIP of 09/176,022 10/21/1998 PAT 6,061,551

Foreign Applications

If Required, Foreign Filing License Granted: 01/21/2009

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/349,802**

Projected Publication Date: 09/03/2009

Non-Publication Request: No

Early Publication Request: No
Title

Method and System For Down-Converting An Electromagnetic Signal, And Transforms For Same, And Aperture Relationships

Preliminary Class

455

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/349,802	01/07/2009	David F. SORRELLS	1744.001000P

CONFIRMATION NO. 5719

26111
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1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

POA ACCEPTANCE LETTER

OC000000036135853

Date Mailed: 05/28/2009

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 05/15/2009.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/hnguyen/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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*Admitted only in Maryland
+Admitted only in Virginia
•Practice Limited to Federal Agencies

May 15, 2009

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INTERNET ADDRESS:
MLEE@SKGF.COM

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Mail Stop Missing Parts

Re: U.S. Utility Patent Application
Appl. No. 12/349,802; Filed: January 7, 2009
For: **Method and System For Down-Converting An Electromagnetic Signal, Transforms For Same, and Aperture Relationships**
Inventors: SORRELLS *et al.*
Our Ref: 1744.001000P

Sir:

In reply to the "Notice to File Missing Parts of Non-Provisional Application," dated January 23, 2009, Applicants transmit the following documents for appropriate action by the U.S. Patent and Trademark Office:

1. Petition for Extension of Time under 37 C.F.R. § 1.136;

2. Power of Attorney from Assignee;

3. Statement Under 37 C.F.R. § 3.73(b);

4. Online Credit Card Payment Authorization for $3,870.00 to cover:
$ 1,090.00 Patent Application fee (including basic filing, search and examination fees)
$ 2,160.00 Application size fee
$ 130.00 Surcharge for late filing fee or Declaration; and
$ 490.00 Two (2) Months Extension of time fees.

The above-listed documents are filed electronically through EFS-Web.

Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036. If extensions of time under 37 C.F.R. § 1.136 other than those otherwise provided for herewith are required to prevent abandonment of the present patent application, then such extensions of time are hereby petitioned, and any fees therefor are hereby authorized to be charged to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

MQL/VDT/jk
Enclosures

979180_1

PTO/SB/22 (02-09)
Approved for use through 03/31/2009. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARMENT OF COMMERCE
Under the paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a) **FY 2009** ***(Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).)***	Docket Number (Optional) 1744.001000P
Application Number 12/349,802	Filed January 7, 2009
For Method and System For Down-Converting An Electromagnetic Signal, Transforms For Same, and Aperture Relationships	
Art Unit 2618	Examiner To Be Assigned

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

		Fee	Small Entity Fee	
☐	One month (37 CFR 1.17(a)(1))	$130	$65	$
☒	Two months (37 CFR 1.17(a)(2))	$490	$245	$ 490.00
☐	Three months (37 CFR 1.17(a)(3))	$1110	$555	$
☐	Four months (37 CFR 1.17(a)(4))	$1730	$865	$
☐	Five months (37 CFR 1.17(a)(5))	$2350	$1175	$

☐ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check in the amount of the fee is enclosed.

☒ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 19-0036.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

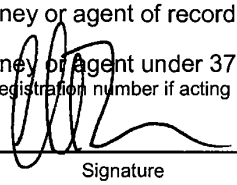
I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed (Form PTO/SB/96).

☐ attorney or agent of record. Registration Number _____

☒ attorney or agent under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 35,239

	5/15/09
Signature	Date
Michael Q. Lee	(202) 371-2600
Typed or printed name	Telephone Number

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☒ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

979202_1

PTO/SB/80 (11-08)
Approved for use through 11/30/2011. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

[X] Practitioners associated with the Customer Number: **26111**

OR

[ ] Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:

[X] The address associated with Customer Number: **26111**

OR

[ ] Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

Assignee Name and Address:

ParkerVision, Inc.
D2DTM Technologies
7915 Baymeadows Way, Suite 400
Jacksonville, Florida 32256

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	David Sorrells	Date	4/28/09
Name	David F. Sorrells	Telephone	(904) 737-1367
Title	Co-Founder and CTO		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/96 (02-09)
Approved for use through 03/31/2009. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(b)

Atty. Docket No. 1744.001000P

Applicant/Patent Owner: SORRELLS et al.

Application No./Patent No.: 12/349,802 Filed/Issue Date: January 7, 2009

Titled: Method and System For Down-Converting An Electromagnetic Signal, Transforms For Same, and Aperture Relationships

ParkerVision, Inc. , a Corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.

states that it is:

1. [X] the assignee of the entire right, title, and interest in;

2. [ ] an assignee of less than the entire right, title, and interest in
(The extent (by percentage) of its ownership interest is _____ %); or

3. [ ] the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

A. [X] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 011099, Frame 0249, or for which a copy therefore is attached.

OR

B. [ ] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

[ ] Additional documents in the chain of title are listed on a supplemental sheet(s).

[X] As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature

5/15/09
Date

Michael Q. Lee
Printed or Typed Name

Attorney of Record
Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

979745_1

Electronic Patent Application Fee Transmittal

Application Number:	12349802
Filing Date:	07-Jan-2009
Title of Invention:	Method and System For Down-Converting An Electromagnetic Signal, And Transforms For Same, And Aperture Relationships
First Named Inventor/Applicant Name:	David F. SORRELLS
Filer:	Michael Q. Lee/joanne king
Attorney Docket Number:	1744.001000P

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Utility Appl Size fee per 50 sheets >100	1081	8	270	2160
Claims:				
Miscellaneous-Filing:				
Late filing fee for oath or declaration	1051	1	130	130

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 2 months with $0 paid	1252	1	490	490
Miscellaneous:				
		Total in USD ($)		**3870**

Electronic Acknowledgement Receipt

EFS ID:	5344701
Application Number:	12349802
International Application Number:	
Confirmation Number:	5719
Title of Invention:	Method and System For Down-Converting An Electromagnetic Signal, And Transforms For Same, And Aperture Relationships
First Named Inventor/Applicant Name:	David F. SORRELLS
Customer Number:	26111
Filer:	Michael Q. Lee/joanne king
Filer Authorized By:	Michael Q. Lee
Attorney Docket Number:	1744.001000P
Receipt Date:	15-MAY-2009
Filing Date:	07-JAN-2009
Time Stamp:	17:40:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$3870
RAM confirmation Number	3731
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1		1744001000PEOTPOAFILING.pdf	240941 f704f18fe0e8f28b86b67e200913cebdd5908d16	yes	5

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	2
	Extension of Time	3	3
	Power of Attorney	4	4
	Assignee showing of ownership per 37 CFR 3.73(b).	5	5

Warnings:

Information:

2	Fee Worksheet (PTO-875)	fee-info.pdf	40331 4dc2898595081e9ab03b9d714be81f384ae7448b	no	2

Warnings:

Information:

Total Files Size (in bytes):	281272

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/349,802	01/07/2009	2618	0.00	1744.001000P	12	1

CONFIRMATION NO. 5719

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

FILING RECEIPT



Date Mailed: 01/23/2009

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

David F. SORRELLS, Jacksonville, FL;
Michael J. Bultman, Jacksonville, FL;
Robert W. Cook, Switzerland, FL;
Richard C. Looke, Jacksonville, FL;
Charley D. Moses JR., Jacksonville, FL;
Michael W. Rawlins, Lake Mary, FL;
Gregory S. Rawlins, Lake Mary, FL;

Assignment For Published Patent Application

ParkerVision, Inc., Jacksonville, FL

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a DIV of 09/550,644 04/14/2000
which is a CIP of 09/521,879 03/09/2000 ABN
and is a CIP of 09/293,342 04/16/1999 PAT 6,687,493
which is a CIP of 09/176,022 10/21/1998 PAT 6,061,551

Foreign Applications

If Required, Foreign Filing License Granted: 01/21/2009

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/349,802**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No
Title

Method and System For Down-Converting An Electromagnetic Signal, And Transforms For Same, And Aperture Relationships

Preliminary Class

455

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/349,802	01/07/2009	David F. SORRELLS	1744.001000P

CONFIRMATION NO. 5719

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

FORMALITIES LETTER

OC000000034149158

Date Mailed: 01/23/2009

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
  *Applicant must submit $**330** to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).*

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of $**130** for a non-small entity, must be submitted with the missing items identified in this notice.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is $**3380** for a non-small entity
- $**330** Statutory basic filing fee.
- $**130** Surcharge.
- The application search fee has not been paid. Applicant must submit $**540** to complete the search fee.
- The application examination fee has not been paid. Applicant must submit $**220** to complete the examination fee for a non-small entity.
- The specification and drawings submitted electronically contain the equivalent of more than 100 pages. Applicant owes $**2160** for **392** pages in excess of **100** pages for a non-small entity.

Replies should be mailed to:

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/349,802	01/07/2009	David F. SORRELLS	1744.001000P

CONFIRMATION NO. 5719

26111
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IMPROPER CPOA LETTER

OC000000034132830

Date Mailed: 01/23/2009

NOTICE REGARDING POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/07/2009. The Power of Attorney in this application is not accepted for the reason(s) listed below:

- The Power of Attorney you provided did not comply with the new Power of Attorney rules that became effective on June 25, 2004. See 37 CFR 1.32.

/akassa/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PTO/SB/05 (08-08)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	**1744.001000P**
First Inventor	**David F. SORRELLS**
Title	**See 1 in Addendum**
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☐ **Fee Transmittal Form** (e.g., PTO/SB/17)
2. ☐ **Applicant claims small entity status.** See 37 CFR 1.27.
3. ☒ **Specification** [*Total Pages* 372] Both the claims and abstract must start on a new page *(For information on the preferred arrangement, see MPEP 608.01(a))*
4. ☒ **Drawing(s)** (*35 U.S.C. 113*) [*Total Sheets* 284]
5. **Oath or Declaration** [*Total Sheets* 4]
   a. ☐ Newly executed (original or copy)
   b. ☒ A copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 18 completed)*
      i. ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. ☒ **Application Data Sheet.** See 37 CFR 1.76
7. ☐ **CD-ROM or CD-R** in duplicate, large table or Computer Program *(Appendix)* ☐ Landscape Table on CD
8. **Nucleotide and/or Amino Acid Sequence Submission** *(if applicable, items a. – c. are required)*
   a. ☐ Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper
   c. ☐ Statements verifying identity of above copies

ADDRESS TO: **Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450**

ACCOMPANYING APPLICATION PARTS

9. ☐ **Assignment Papers** (cover sheet (PTO-1595) & document(s)) Name of Assignee _____
10. ☐ **37 CFR 3.73(b) Statement** *(when there is an assignee)* ☐ **Power of Attorney**
11. ☐ **English Translation Document** *(if applicable)*
12. ☐ **Information Disclosure Statement** (PTO/SB/08 or PTO-1449) ☐ Copies of foreign patent documents, publications, & other information
13. ☐ **Preliminary Amendment**
14. ☐ **Return Receipt Postcard** (MPEP 503) *(Should be specifically itemized)*
15. ☐ **Certified Copy of Priority Document(s)** *(if foreign priority is claimed)*
16. ☐ **Nonpublication Request** under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
17. ☒ Other: **Authorization under 37 CFR 1.136(a)(3)**

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:*

☐ Continuation ☒ Divisional ☐ Continuation-in-part (CIP) of prior application No.: 09/550,644

Prior application information: *Examiner* _____ *Art Unit:* _____

19. CORRESPONDENCE ADDRESS

☒ The address associated with Customer Number: **26111** *OR* ☐ Correspondence address below

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City		State		Zip Code	
Country		Telephone		Email	

Signature		Date	1/7/09
Name (Print/Type)	**Michael Q. Lee**	Registration No. (Attorney/Agent)	**35,239**

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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921283

Addendum

1. Method And System For Down-Converting An Electromagnetic Signal, And Transforms For Same, And Aperture Relationships

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: To Be Assigned
SORRELLS *et al.*	Art Unit: To Be Assigned
Appl. No.: To Be Assigned	Examiner: To Be Assigned
Filed: Herewith (January 7, 2009)	Atty. Docket: 1744.001000P
For: **Method and System For Down-Converting An Electromagnetic Signal, And Transforms For Same, And Aperture Relationships**	

Authorization to Treat a Reply as Incorporating an Extension of Time Under 37 C.F.R. § 1.136(a)(3)

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

The U.S. Patent and Trademark Office is hereby authorized to treat any concurrent or future reply that requires a petition for an extension of time under this paragraph for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. The U.S. Patent and Trademark Office is hereby authorized to charge all required extension of time fees to our Deposit Account No. 19-0036, if such fees are not otherwise provided for in such reply.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

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921232_1.DOC

APPLICATION DATA SHEET

Electronic Version v14
Stylesheet Version v14.1

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Customer Number:	26111	*26111*

Application Information:

Title of Invention:	Method and System For Down-Converting An Electromagnetic Signal, And Transforms For Same, And Aperture Relationships

Application Type: regular, utility
Attorney Docket Number: 1744.00100P

Botanic Information:

Publication Information:
Suggested Figure for Publication -
Suggested Classification -
Suggested Technology Center -
Total Number of Drawing Sheets - 284

Representative Information:

practitioner(s) at Customer Number:

26111 *26111*

as our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.

Domestic Priority Information:

This is a Division of US application number 09/550,644, filed 2000-04-14, now pending.

US application number 09/550,644, filed 2000-04-14 is a continuation-in-part of U.S. application number 09/521,879, filed March 9, 2000 (now abandoned) .

US application number 09/550,644, filed 2000-04-14 is a Continuation-in-part of US application number 09/293,342, filed 1999-04-16, now US patent number 6,687,493, issued 2004-02-03.

US application number 09/293,342, filed 1999-04-16 is a Continuation-in-part of US application number 09/176,022, filed 1998-10-21, now US patent number 6,061,551, issued 2000-05-09.

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921325_1.DOC

Combined Declaration and Power of Attorney for Patent Application

Docket Number: 1744.0010009

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter that is claimed and for which a patent is sought on the invention entitled **Method and System for Down-Converting an Electromagnetic Signal, Transforms for Same, and Aperture Relationships**, the specification of which is attached hereto unless the following box is checked:

■ was filed on April 14, 2000 ;
as United States Application Number or PCT International Application Number 09/550,644 ; and
was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application, which designated at least one country other than the United States listed below, and have also identified below any foreign application for patent or inventor's certificate, or PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Claimed
_____	_____	_____	□ Yes □ No
(Application No.)	(Country)	(Day/Month/Year Filed)	
_____	_____	_____	□ Yes □ No
(Application No.)	(Country)	(Day/Month/Year Filed)	

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

_____	_____
(Application No.)	(Filing Date)
_____	_____
(Application No.)	(Filing Date)

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or under § 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. § 1.56 that became available between the filing date of the prior application and the national or PCT international filing date of this application.

09/176,022	October 21, 1998	patented
(Application No.)	(Filing Date)	(Status - patented, pending, abandoned)
09/293,342	April 16, 1999	pending
(Application No.)	(Filing Date)	(Status - patented, pending, abandoned)
09/521,879	March 9, 2000	pending
(Application No.)	(Filing Date)	(Status - patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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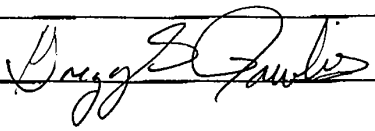
(202) 371-2600

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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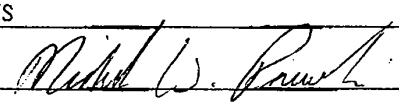
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Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same, and Aperture Relationships

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Cross-Reference to Other Applications

The present application is a divisional application of pending U.S. application "Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same, and Aperture Relationships," Ser. No. 09/550,644, filed April 14, 2000, which is a continuation-in-part of U.S. application "Matched Filter Characterization and Implementation of Universal Frequency Translation Method and Apparatus," Ser. No. 09/521,879, filed March 9, 2000 (now abandoned). Pending U.S. application "Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same, and Aperture Relationships," Ser. No. 09/550,644, filed April 14, 2000, is also a continuation-in-part application of U.S. application "Method and System for Down-Converting an Electromagnetic Signal Including Resonant Structures for Enhanced Energy Transfer," Ser. No. 09/293,342, filed April 16, 1999 (now U.S. Patent No. 6,687,493), which is a continuation-in-part application of U.S. application "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998 (now U.S. Patent No. 6,061,551), each of which is herein incorporated by reference in their entireties.

The following applications of common assignee are related to the present application, and are herein incorporated by reference in their entireties:

"Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed October 21, 1998 (now U.S. Patent No. 6,091,940);

"Method and System for Ensuring Reception of a Communications Signal," Ser. No. 09/176,415, filed October 21, 1998 (now U.S. Patent No. 6,061,555);

"Integrated Frequency Translation and Selectivity," Ser. No. 09/175,966, filed October 21, 1998 (now U.S. Patent No. 6,049,706);

"Universal Frequency Translation, and Applications of Same," Ser. No. 09/176,027, filed October 21, 1998 (now abandoned);

"Method and System for Down-Converting Electromagnetic Signals Having Optimized Switch Structures," Ser. No. 09/293,095, filed April 16, 1999 (now U.S. Patent No. 6,580,902);

"Method and System for Frequency Up-Conversion with a Variety of Transmitter Configurations," Ser. No. 09/293,580, filed April 16, 1999 (U.S. Patent No. 6,542,722); and

"Integrated Frequency Translation and Selectivity with a Variety of Filter Embodiments," Ser. No. 09/293,283, filed April 16, 1999 (now U.S. Patent No. 6,560,301).

Background of the Invention

Field of the Invention

The present invention relates to down-conversion of electromagnetic (EM) signals. More particularly, the present invention relates to down-conversion of EM signals to intermediate frequency signals, to direct down-conversion of EM modulated carrier signals to demodulated baseband signals, and to conversion of FM signals to non-FM signals. The present invention also relates to under-sampling and to transferring energy at aliasing rates.

Related Art

Electromagnetic (EM) information signals (baseband signals) include, but are not limited to, video baseband signals, voice baseband signals, computer baseband signals, etc. Baseband signals include analog baseband signals and digital baseband signals.

It is often beneficial to propagate EM signals at higher frequencies. This is generally true regardless of whether the propagation medium is wire, optic fiber, space, air, liquid, etc.. To enhance efficiency and practicality, such as improved ability to radiate and added ability for multiple channels of baseband signals, up-conversion to a higher frequency is utilized. Conventional up-conversion processes modulate higher frequency carrier signals with baseband signals. Modulation refers to a variety of techniques for impressing information from the baseband signals onto the higher frequency carrier signals. The resultant signals are referred to herein as modulated carrier signals. For example, the amplitude of an AM carrier signal varies in relation to changes in the baseband signal, the frequency of an FM carrier signal varies in relation to changes in the baseband signal, and the phase of a PM carrier signal varies in relation to changes in the baseband signal.

In order to process the information that was in the baseband signal, the information must be extracted, or demodulated, from the modulated carrier signal. However, because conventional signal processing technology is limited in operational speed, conventional signal processing technology cannot easily demodulate a baseband signal from higher frequency modulated carrier signal directly. Instead, higher frequency modulated carrier signals must be down-converted to an intermediate frequency (IF), from where a conventional demodulator can demodulate the baseband signal.

Conventional down-converters include electrical components whose properties are frequency dependent. As a result, conventional down-

converters are designed around specific frequencies or frequency ranges and do not work well outside their designed frequency range.

Conventional down-converters generate unwanted image signals and thus must include filters for filtering the unwanted image signals. However, such filters reduce the power level of the modulated carrier signals. As a result, conventional down-converters include power amplifiers, which require external energy sources.

When a received modulated carrier signal is relatively weak, as in, for example, a radio receiver, conventional down-converters include additional power amplifiers, which require additional external energy.

What is needed includes, without limitation:

an improved method and system for down-converting EM signals;

a method and system for directly down-converting modulated carrier signals to demodulated baseband signals;

a method and system for transferring energy and for augmenting such energy transfer when down-converting EM signals;

a controlled impedance method and system for down-converting an EM signal;

a controlled aperture under-sampling method and system for down-converting an EM signal;

a method and system for down-converting EM signals using a universal down-converter design that can be easily configured for different frequencies;

a method and system for down-converting EM signals using a local oscillator frequency that is substantially lower than the carrier frequency;

a method and system for down-converting EM signals using only one local oscillator;

a method and system for down-converting EM signals that uses fewer filters than conventional down-converters;

a method and system for down-converting EM signals using less power than conventional down-converters;

a method and system for down-converting EM signals that uses less space than conventional down-converters;

a method and system for down-converting EM signals that uses fewer components than conventional down-converters;

a method and system for down-converting EM signals that can be implemented on an integrated circuit (IC); and

a method and system for down-converting EM signals that can also be used as a method and system for up-converting a baseband signal.

Summary of the Invention

Briefly stated, the present invention is directed to methods, systems, and apparatuses for down-converting an electromagnetic (EM), and applications thereof.

Generally, in an embodiment, the invention operates by receiving an EM signal and recursively operating on approximate half cycles of a carrier signal. The recursive operations are typically performed at a sub-harmonic rate of the carrier signal. The invention accumulates the results of the recursive operations and uses the accumulated results to form a down-converted signal.

In an embodiment, the invention down-converts the EM signal to an intermediate frequency (IF) signal.

In another embodiment, the invention down-converts the EM signal to a demodulated baseband information signal.

In another embodiment, the EM signal is a frequency modulated (FM) signal, which is down-converted to a non-FM signal, such as a phase modulated (PM) signal or an amplitude modulated (AM) signal.

The invention is applicable to any type of EM signal, including but not limited to, modulated carrier signals (the invention is applicable to any modulation scheme or combination thereof) and unmodulated carrier signals.

Further features and advantages of the invention, as well as the structure and operation of various embodiments of the invention, are described in detail below with reference to the accompanying drawings. It is noted that the invention is not limited to the specific embodiments described herein. Such embodiments are presented herein for illustrative purposes only. Additional embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

Brief Description of the Drawings

The drawing in which an element first appears is typically indicated by the leftmost digit(s) in the corresponding reference number.

The present invention will be described with reference to the accompanying drawings wherein:

FIGS.1 illustrates a structural block diagram of an example modulator;

FIG. 2 illustrates an example analog modulating baseband signal;

FIG. 3 illustrates an example digital modulating baseband signal;

FIG. 4 illustrates an example carrier signal;

FIGS. 5A-5C illustrate example signal diagrams related to amplitude modulation;

FIGS. 6A-6C illustrate example signal diagrams related to amplitude shift keying modulation;

FIGS. 7A-7C illustrate example signal diagrams related to frequency modulation;

FIGS. 8A-8C illustrate example signal diagrams related to frequency shift keying modulation;

FIGS. 9A-9C illustrate example signal diagrams related to phase modulation;

FIGS. 10A-10C illustrate example signal diagrams related to phase shift keying modulation;

FIG. 11 illustrates a structural block diagram of a conventional receiver;

FIG.12A-D illustrate various flowcharts for down-converting an EM-signal according to embodiments of the invention;

FIG. 13 illustrates a structural block diagram of an aliasing system according to an embodiment of the invention;

FIGS. 14A-D illustrate various flowcharts for down-converting an EM signal by under-sampling the EM signal according to embodiments of the invention;

FIGS. 15A-E illustrate example signal diagrams associated with flowcharts in FIGS. 14A-D according to embodiments of the invention;

FIG. 16 illustrates a structural block diagram of an under-sampling system according to an embodiment of the invention;

FIG. 17 illustrates a flowchart of an example process for determining an aliasing rate according to an embodiment of the invention;

FIGS. 18A-E illustrate example signal diagrams associated with down-converting a digital AM signal to an intermediate frequency signal by under-sampling according to embodiments of the invention;

FIGS. 19A-E illustrate example signal diagrams associated with down-converting an analog AM signal to an intermediate frequency signal by under-sampling according to embodiments of the invention;

FIGS. 20A-E illustrate example signal diagrams associated with down-converting an analog FM signal to an intermediate frequency signal by under-sampling according to embodiments of the invention;

FIGS. 21A-E illustrate example signal diagrams associated with down-converting a digital FM signal to an intermediate frequency signal by under-sampling according to embodiments of the invention;

FIGS. 22A-E illustrate example signal diagrams associated with down-converting a digital PM signal to an intermediate frequency signal by under-sampling according to embodiments of the invention;

FIGS. 23A-E illustrate example signal diagrams associated with down-converting an analog PM signal to an intermediate frequency signal by under-sampling according to embodiments of the invention;

FIG. 24A illustrates a structural block diagram of a make before break under-sampling system according to an embodiment of the invention;

FIG. 24B illustrates an example timing diagram of an under sampling signal according to an embodiment of the invention;

FIG. 24C illustrates an example timing diagram of an isolation signal according to an embodiment of the invention;

FIGS. 25A-H illustrate example aliasing signals at various aliasing rates according to embodiments of the invention;

FIG. 26A illustrates a structural block diagram of an exemplary sample and hold system according to an embodiment of the invention;

FIG. 26B illustrates a structural block diagram of an exemplary inverted sample and hold system according to an embodiment of the invention;

FIG. 27 illustrates a structural block diagram of sample and hold module according to an embodiment of the invention;

FIGS. 28A-D illustrate example implementations of a switch module according to embodiments of the invention;

FIGS. 29A-F illustrate example implementations of a holding module according to embodiments of the present invention;

FIG. 29G illustrates an integrated under-sampling system according to embodiments of the invention;

FIGS. 29H-K illustrate example implementations of pulse generators according to embodiments of the invention;

FIG. 29L illustrates an example oscillator;

FIG. 30 illustrates a structural block diagram of an under-sampling system with an under-sampling signal optimizer according to embodiments of the invention;

FIG. 31A illustrates a structural block diagram of an under-sampling signal optimizer according to embodiments of the present invention;

FIGS. 31B and 31C illustrate example waveforms present in the circuit of FIG. 31A;

FIG. 32A illustrates an example of an under-sampling signal module according to an embodiment of the invention;

FIG. 32B illustrates a flowchart of a state machine operation associated with an under-sampling module according to embodiments of the invention;

FIG. 32C illustrates an example under-sampling module that includes an analog circuit with automatic gain control according to embodiments of the invention;

FIGS. 33A-D illustrate example signal diagrams associated with direct down-conversion of an EM signal to a baseband signal by under-sampling according to embodiments of the present invention;

FIGS. 34A-F illustrate example signal diagrams associated with an inverted sample and hold module according to embodiments of the invention;

FIGS. 35A-E illustrate example signal diagrams associated with directly down-converting an analog AM signal to a demodulated baseband signal by under-sampling according to embodiments of the invention;

FIGS. 36A-E illustrate example signal diagrams associated with down-converting a digital AM signal to a demodulated baseband signal by under-sampling according to embodiments of the invention;

FIGS. 37A-E illustrate example signal diagrams associated with directly down-converting an analog PM signal to a demodulated baseband signal by under-sampling according to embodiments of the invention;

FIGS. 38A-E illustrate example signal diagrams associated with down-converting a digital PM signal to a demodulated baseband signal by under-sampling according to embodiments of the invention;

FIGS. 39A-D illustrate down-converting a FM signal to a non-FM signal by under-sampling according to embodiments of the invention;

FIGS. 40A-E illustrate down-converting a FSK signal to a PSK signal by under-sampling according to embodiments of the invention;

FIGS. 41A-E illustrate down-converting a FSK signal to an ASK signal by under-sampling according to embodiments of the invention;

FIG. 42 illustrates a structural block diagram of an inverted sample and hold according to an embodiment of the present invention;

FIG. 43 illustrates an equation that represents the change in charge in an storage device of embodiments of a UFT module.

FIG. 44A illustrates a structural block diagram of a differential system according to embodiments of the invention;

FIG. 44B illustrates a structural block diagram of a differential system with a differential input and a differential output according to embodiments of the invention;

FIG. 44C illustrates a structural block diagram of a differential system with a single input and a differential output according to embodiments of the invention;

FIG. 44D illustrates a differential input with a single output according to embodiments of the invention;

FIG. 44E illustrates an example differential input to single output system according to embodiments of the invention;

FIGS 45A-B illustrate a conceptual illustration of aliasing including under-sampling and energy transfer according to embodiments of the invention;

FIGS. 46A-D illustrate various flowchart for down-converting an EM signal by transferring energy from the EM signal at an aliasing rate according to embodiments of the invention;

FIGS. 47A-E illustrate example signal diagrams associated with the flowcharts in FIGS. 46A-D according to embodiments of the invention;

FIG. 48 is a flowchart that illustrates an example process for determining an aliasing rate associated with an aliasing signal according to an embodiment of the invention;

FIG. 49A-H illustrate example energy transfer signals according to embodiments of the invention;

FIGS. 50A-G illustrate example signal diagrams associated with down-converting an analog AM signal to an intermediate frequency by transferring energy at an aliasing rate according to embodiments of the invention;

FIGS. 51A-G illustrate example signal diagrams associated with down-converting an digital AM signal to an intermediate frequency by transferring energy at an aliasing rate according to embodiments of the invention;

FIGS. 52A-G illustrate example signal diagrams associated with down-converting an analog FM signal to an intermediate frequency by transferring energy at an aliasing rate according to embodiments of the invention;

FIGS. 53A-G illustrate example signal diagrams associated with down-converting an digital FM signal to an intermediate frequency by transferring energy at an aliasing rate according to embodiments of the invention;

FIGS. 54A-G illustrate example signal diagrams associated with down-converting an analog PM signal to an intermediate frequency by transferring energy at an aliasing rate according to embodiments of the invention;

FIGS. 55A-G illustrate example signal diagrams associated with down-converting an digital PM signal to an intermediate frequency by transferring energy at an aliasing rate according to embodiments of the invention;

FIGS. 56A-D illustrate an example signal diagram associated with direct down-conversion according to embodiments of the invention;

FIGS. 57A-F illustrate directly down-converting an analog AM signal to a demodulated baseband signal according to embodiments of the invention;

FIGS. 58A-F illustrate directly down-converting an digital AM signal to a demodulated baseband signal according to embodiments of the invention;

FIGS. 59A-F illustrate directly down-converting an analog PM signal to a demodulated baseband signal according to embodiments of the invention;

FIGS. 60A-F illustrate directly down-converting an digital PM signal to a demodulated baseband signal according to embodiments of the invention;

FIGS. 61A-F illustrate down-converting an FM signal to a PM signal according to embodiments of the invention;

FIGS. 62A-F illustrate down-converting an FM signal to a AM signal according to embodiments of the invention;

FIG. 63 illustrates a block diagram of an energy transfer system according to an embodiment of the invention;

FIG. 64A illustrates an exemplary gated transfer system according to an embodiment of the invention;

FIG. 64B illustrates an exemplary inverted gated transfer system according to an embodiment of the invention;

FIG. 65 illustrates an example embodiment of the gated transfer module according to an embodiment of the invention;

FIGS. 66A-D illustrate example implementations of a switch module according to embodiments of the invention;

FIG. 67A illustrates an example embodiment of the gated transfer module as including a break-before-make module according to an embodiment of the invention;

FIG. 67B illustrates an example timing diagram for an energy transfer signal according to an embodiment of the invention;

FIG. 67C illustrates an example timing diagram for an isolation signal according to an embodiment of the invention;

FIGS. 68A-F illustrate example storage modules according to embodiments of the invention;

FIG. 68G illustrates an integrated gated transfer system according to an embodiment of the invention;

FIGS. 68H-K illustrate example aperture generators;

FIG. 68L illustrates an oscillator according to an embodiment of the present invention;

FIG. 69 illustrates an energy transfer system with an optional energy transfer signal module according to an embodiment of the invention;

FIG. 70 illustrates an aliasing module with input and output impedance match according to an embodiment of the invention;

FIG. 71A illustrates an example pulse generator;

FIGS. 71B and C illustrate example waveforms related to the pulse generator of FIG. 71A;

FIG. 72 illustrates an example embodiment where preprocessing is used to select a portion of the carrier signal to be operated upon;

FIG. 73 illustrates an example energy transfer module with a switch module and a reactive storage module according to an embodiment of the invention;

FIG. 74 illustrates an example inverted gated transfer module as including a switch module and a storage module according to an embodiment of the invention;

FIGS. 75A-F illustrate an example signal diagrams associated with an inverted gated energy transfer module according to embodiments of the invention;

FIGS. 76A-E illustrate energy transfer modules in configured in various differential configurations according to embodiments of the invention;

FIGS. 77A-C illustrate example impedance matching circuits according to embodiments of the invention;

FIGS. 78A-B illustrate example under-sampling systems according to embodiments of the invention;

FIGS. 79A-F illustrate example timing diagrams for under-sampling systems according to embodiments of the invention;

FIGS. 80A-F illustrate example timing diagrams for an under-sampling system when the load is a relatively low impedance load according to embodiments of the invention;

FIGS. 81A-F illustrate example timing diagrams for an under-sampling system when the holding capacitance has a larger value according to embodiments of the invention;

FIGS. 82A-B illustrate example energy transfer systems according to embodiments of the invention;

FIGS. 83A-F illustrate example timing diagrams for energy transfer systems according to embodiments of the present invention;

FIGS. 84A-D illustrate down-converting an FSK signal to a PSK signal according to embodiments of the present invention;

FIG. 85A illustrates an example energy transfer signal module according to an embodiment of the present invention;

FIG. 85B illustrates a flowchart of state machine operation according to an embodiment of the present invention;

FIG. 85C is an example energy transfer signal module;

FIG. 86 is a schematic diagram of a circuit to down-convert a 915 MHZ signal to a 5 MHZ signal using a 101.1 MHZ clock according to an embodiment of the present invention;

FIG. 87 shows simulation waveforms for the circuit of FIG. 86 according to embodiments of the present invention;

FIG. 88 is a schematic diagram of a circuit to down-convert a 915 MHZ signal to a 5 MHz signal using a 101 MHZ clock according to an embodiment of the present invention;

FIG. 89 shows simulation waveforms for the circuit of FIG. 88 according to embodiments of the present invention;

FIG. 90 is a schematic diagram of a circuit to down-convert a 915 MHZ signal to a 5 MHZ signal using a 101.1 MHZ clock according to an embodiment of the present invention;

FIG. 91 shows simulation waveforms for the circuit of FIG. 90 according to an embodiment of the present invention;

FIG. 92 shows a schematic of the circuit in FIG. 86 connected to an FSK source that alternates between 913 and 917 MHZ at a baud rate of 500 Kbaud according to an embodiment of the present invention;

FIG. 93 shows the original FSK waveform 9202 and the down-converted waveform 9204 at the output of the load impedance match circuit according to an embodiment of the present invention;

FIG. 94A illustrates an example energy transfer system according to an embodiment of the invention;

FIGS. 94B-C illustrate example timing diagrams for the example system of FIG. 94A;

FIG. 95 illustrates an example bypass network according to an embodiment of the invention;

FIG. 96 illustrates an example bypass network according to an embodiment of the invention;

FIG. 97 illustrates an example embodiment of the invention;

FIG. 98A illustrates an example real time aperture control circuit according to an embodiment of the invention;

FIG. 98B illustrates a timing diagram of an example clock signal for real time aperture control, according to an embodiment of the invention;

FIG. 98C illustrates a timing diagram of an example optional enable signal for real time aperture control, according to an embodiment of the invention;

FIG. 98D illustrates a timing diagram of an inverted clock signal for real time aperture control, according to an embodiment of the invention;

FIG. 98E illustrates a timing diagram of an example delayed clock signal for real time aperture control, according to an embodiment of the invention;

FIG. 98F illustrates a timing diagram of an example energy transfer including pulses having apertures that are controlled in real time, according to an embodiment of the invention;

FIG. 99 is a block diagram of a differential system that utilizes non-inverted gated transfer units, according to an embodiment of the invention;

FIG.100 illustrates an example embodiment of the invention;

FIG.101 illustrates an example embodiment of the invention;

FIG.102 illustrates an example embodiment of the invention;

FIG.103 illustrates an example embodiment of the invention;

FIG.104 illustrates an example embodiment of the invention;

FIG.105 illustrates an example embodiment of the invention;

FIG.106 illustrates an example embodiment of the invention;

FIG.107A is a timing diagram for the example embodiment of FIG. 103;

FIG.107B is a timing diagram for the example embodiment of FIG. 104;

FIG.108A is a timing diagram for the example embodiment of FIG. 105;

FIG.108B is a timing diagram for the example embodiment of FIG. 106;

FIG.109A illustrates and example embodiment of the invention;

FIG.109B illustrates equations for determining charge transfer, in accordance with the present invention;

FIG.109C illustrates relationships between capacitor charging and aperture, in accordance with the present invention;

FIG.109D illustrates relationships between capacitor charging and aperture, in accordance with the present invention;

FIG.109E illustrates power-charge relationship equations, in accordance with the present invention;

FIG.109F illustrates insertion loss equations, in accordance with the present invention;

FIG. 110A illustrates aliasing module 11000 a single FET configuration;

FIG.110B illustrates FET conductivity vs. $V_{GS;}$

FIGS.111A-C illustrate signal waveforms associated with aliasing module 11000;

FIG. 112 illustrates aliasing module 11200 with a complementary FET configuration;

FIGS. 113A-E illustrate signal waveforms associated with aliasing module11200;

FIG. 114 illustrates aliasing module 11400;

FIG. 115 illustrates aliasing module 11500;

FIG. 116 illustrates aliasing module 11602;

FIG. 117 illustrates aliasing module 11702;

FIGS. 118-120 illustrate signal waveforms associated with aliasing module 11602;

FIGS. 121-123 illustrate signal waveforms associated with aliasing module 11702.

FIG. 124A is a block diagram of a splitter according to an embodiment of the invention;

FIG. 124B is a more detailed diagram of a splitter according to an embodiment of the invention;

FIGS. 124C and 124D are example waveforms related to the splitter of FIGS. 124A and 124B;

FIG. 124E is a block diagram of an I/Q circuit with a splitter according to an embodiment of the invention;

FIGS. 124F-124J are example waveforms related to the diagram of FIG. 124A;

FIG. 125 is a block diagram of a switch module according to an embodiment of the invention;

FIG. 126A is an implementation example of the block diagram of FIG. 125;

FIGS. 126B-126Q are example waveforms related to FIG. 126A;

FIG. 127A is another implementation example of the block diagram of FIG. 125;

FIGS. 127B-127Q are example waveforms related to FIG. 127A;

FIG. 128A is an example MOSFET embodiment of the invention;

FIG. 128B is an example MOSFET embodiment of the invention;

FIG. 128C is an example MOSFET embodiment of the invention;

FIG. 129A is another implementation example of the block diagram of FIG. 125;

FIGS. 129B-129Q are example waveforms related to FIG. 127A;

FIGS. 130 and 131 illustrate the amplitude and pulse width modulated transmitter according to embodiments of the present invention;

FIGS. 132-134 illustrate example signal diagrams associated with the amplitude and pulse width modulated transmitter according to embodiments of the present invention;

FIG. 135 shows an embodiment of a receiver block diagram to recover the amplitude or pulse width modulated information;

FIG. 136 illustrates example signal diagrams associated with a waveform generator according to embodiments of the present invention;

FIGS. 137-139 are example schematic diagrams illustrating various circuits employed in the receiver of FIG. 135;

FIGS. 140-143 illustrate time and frequency domain diagrams of alternative transmitter output waveforms;

FIGS. 144 and 145 illustrate differential receivers in accord with embodiments of the present invention;

FIGS. 146 and 147 illustrate time and frequency domains for a narrow bandwidth/constant carrier signal in accord with an embodiment of the present invention;

FIG. 148 illustrates a method for down-converting an electromagnetic signal according to an embodiment of the present invention using a matched filtering/correlating operation;

FIG. 149 illustrates a matched filtering/correlating processor according to an embodiment of the present invention;

FIG. 150 illustrates a method for down-converting an electromagnetic signal according to an embodiment of the present invention using a finite time integrating operation;

FIG. 151 illustrates a finite time integrating processor according to an embodiment of the present invention;

FIG. 152 illustrates a method for down-converting an electromagnetic signal according to an embodiment of the present invention using an RC processing operation.

FIG. 153 illustrates an RC processor according to an embodiment of the present invention;

FIG. 154 illustrates an example pulse train;

FIG. 155 illustrates combining a pulse train of energy signals to produce a power signal according to an embobiment of the invention;

FIG. 156 illustrates an example piecewise linear reconstruction of a sine wave.

FIG. 157 illustrates how certain portions of a carrier signal or sine waveform are selected for processing according to an embodiment of the present invention;

FIG. 158 illustrates an example double sideband large carrier AM waveform;

FIG. 159 illustrates a block diagram of an example optimum processor system;

FIG. 160 illustrates the frequency response of an optimum processor according to an embodiment of the present invention;

FIG. 161 illustrates example frequency responses for a processor at various apertures;

FIGS. 162-163 illustrates an example processor embodiment according to the present invention;

FIGS. 164A-C illustrate example impulse responses of a matched filter processor and a finite time integrator;

FIG. 165 illustrates a basic circuit for an RC processor according to an embodiment of the present invention;

FIGS. 166-167 illustrate example plots of voltage signals;

FIGS. 168-170 illustrate the various characteristics of a processor according to an embodiment of the present invention;

FIGS. 171-173 illustrate example processor embodiments according to the present invention;

FIG. 174 illustrates the relationship between beta and the output charge of a processor according to an embodiment of the present invention;

FIG. 175A illustrates an RC processor according to an embodiment of the present invention coupled to a load resistance;

FIG. 175B illustrates an example implementation of the present invention;

FIG. 175C illustrates an example charge/discharge timing diagram according to an embodiment of the present invention;

FIG. 175D illustrates example energy transfer pulses according to an embodiment of the present invention;

FIG. 176 illustrates example performance characteristics of an embodiment of the present invention;

FIG. 177A illustrates example performance characteristics of an embodiment of the present invention;

FIG. 177B illustrates example waveforms for elementary matched filters.

FIG. 177C illustrates a waveform for an embodiment of a UFT subharmonic matched filter of the present invention.

FIG. 177D illustrates example embodiments of complex matched filter/correlator processor;

FIG. 177E illustrates an embodiment of a complex matched filter/ correlator processor of the present invention;

FIG. 177F illustrates an embodiment of the decomposition of a non-ideal correlator alignment into an ideally aligned UFT coorrelator component of the present invention;

FIGS. 178A-178B illustrate example processor waveforms according to an embodiment of the present invention;

FIG. 179 illustrates the Fourier transforms of example waveforms waveforms according to an embodiment of the present invention;

FIGS. 180-181 illustrates actual waveforms from an embodiment of the present invention;

FIG. 182 illustrates a relationship between an example UFT waveform and an example carrier waveform;

FIG. 183 illustrates example impulse samplers having various apertures;

FIG. 184 illustrates the allingment of sample apertures according to an embodiment of the present invention;

FIG. 185 illustrates an ideal aperture according to an embodiment of the present invention;

FIG. 186 illustrates the relationship of a step function and delta functions;

FIG. 187 illustrates an embodiment of a receiver with bandpass filter for complex down-converting of the present invention;

FIG. 188 illustrates Fourier transforms used to analyze a clock embodiment in accordance with the present invention;

FIG. 189 illustrates an acquistion and hold processor according to an embodiment of the present invention;

FIGS. 190-191 illustrate frequency representations of transforms according to an embodiment of the present invention;

FIG. 192 illustrates an example clock generator;

FIG. 193 illustrates the down-conversion of an electromagnetic signal according to an embodiment of the present invention;

FIG. 194 illustrates a receiver according to an embodiment of the present invention;

FIG. 195 illustrates a vector modulator according to an embodiment of the present invention;

FIG. 196 illustrates example waveforms for the vector modulator of FIG. 195;

FIG. 197 illustrates an exemplary I/Q modulation receiver, according to an embodiment of the present invention;

FIG. 198 illustrates a I/Q modulation control signal generator, according to an embodiment of the present invention;

FIG. 199 illustrates example waveforms related to the I/Q modulation control signal generator of FIG. 198;

FIG. 200 illustrates example control signal waveforms overlaid upon an example input RF signal;

FIG. 201 illustrates a I/Q modulation receiver circuit diagram, according to an embodiment of the present invention;

FIGS. 202-212 illustrate example waveforms related to a receiver implemented in accordance with the present invention;

FIG. 213 illustrates a single channel receiver, according to an embodiment of the present invention;

FIG. 214 illustrates exemplary waveforms associated with quad aperture implementations of the receiver of FIG. 281, according to embodiments of the present invention;

FIG. 215 illustrates a high-level example UFT module radio architecture, according to an embodiment of the present invention;

FIG. 216 illustrates wireless design considerations;

FIG. 217 illustrates noise figure calculations based on RMS voltage and current noise specifications;

FIG. 218A illustrates an example differential input, differential output receiver configuration, according to an embodiment of the present invention;

FIG. 218B illustrates a example receiver implementation, configured as an I-phase channel, according to an embodiment of the present invention;

FIG. 218C illustrates example waveforms related to the receiver of FIG. 218B;

FIG. 218D illustrates an example re-radiation frequency spectrum related to the receiver of FIG. 218B, according to an embodiment of the present invention;

FIG. 218E illustrates an example re-radiation frequency spectral plot related to the receiver of FIG. 218B, according to an embodiment of the present invention;

FIG. 218F illustrates example impulse sampling of an input signal;

FIG. 218G illustrates example impulse sampling of an input signal in a environment with more noise relative to that of FIG. 218F;

FIG. 219 illustrates an example integrated circuit conceptual schematic, according to an embodiment of the present invention;

FIG. 220 illustrates an example receiver circuit architecture, according to an embodiment of the present invention;

FIG. 221 illustrates example waveforms related to the receiver of FIG. 220, according to an embodiment of the present invention;

FIG. 222 illustrates DC equations, according to an embodiment of the present invention;

FIG. 223 illustrates an example receiver circuit, according to an embodiment of the present invention;

FIG. 224 illustrates example waveforms related to the receiver of FIG. 223;

FIG. 225 illustrates an example receiver circuit, according to an embodiment of the present invention;

FIGS. 226 and 227 illustrate example waveforms related to the receiver of FIG. 225;

FIGS. 228-230 illustrate equations and information related to charge transfer;

FIG. 231 illustrates a graph related to the equations of FIG. 230;

FIG. 232 illustrates example control signal waveforms and an example input signal waveform, according to embodiments of the present invention;

FIG. 233 illustrates an example differential output receiver, according to an embodiment of the present invention;

FIG. 234 illustrates example waveforms related to the receiver of FIG. 233;

FIG. 235 illustrates an example transmitter circuit, according to an embodiment of the present invention;

FIG. 236 illustrates example waveforms related to the transmitter of FIG. 235;

FIG. 237 illustrates an example frequency spectrum related to the transmitter of FIG. 235;

FIG. 238 illustrates an intersection of frequency selectivity and frequency translation, according to an embodiment of the present invention;

FIG. 239 illustrates a multiple criteria, one solution aspect of the present invention;

FIG. 240 illustrates an example complementary FET switch structure, according to an embodiment of the present invention;

FIG. 241 illustrates example waveforms related to the complementary FET switch structure of FIG. 240;

FIG. 242 illustrates an example differential configuration, according to an embodiment of the present invention;

FIG. 243 illustrates an example receiver implementing clock spreading, according to an embodiment of the present invention;

FIG. 244 illustrates example waveforms related to the receiver of FIG. 243;

FIG. 245 illustrates waveforms related to the receiver of FIG. 243 implemented without clock spreading, according to an embodiment of the present invention;

FIG. 246 illustrates an example recovered I/Q waveforms, according to an embodiment of the present invention;

FIG. 247 illustrates an example CMOS implementation, according to an embodiment of the present invention;

FIG. 248 illustrates an example LO gain stage of FIG. 247 at a gate level, according to an embodiment of the present invention;

FIG. 249 illustrates an example LO gain stage of FIG. 247 at a transistor level, according to an embodiment of the present invention;

FIG. 250 illustrates an example pulse generator of FIG. 247 at a gate level, according to an embodiment of the present invention;

FIG. 251 illustrates an example pulse generator of FIG. 247 at a transistor level, according to an embodiment of the present invention;

FIG. 252 illustrates an example power gain block of FIG. 247 at a gate level, according to an embodiment of the present invention;

FIG. 253 illustrates an example power gain block of FIG. 247 at a transistor level, according to an embodiment of the present invention;

FIG. 254 illustrates an example switch of FIG. 247 at a transistor level, according to an embodiment of the present invention;

FIG. 255 illustrates an example CMOS "hot clock" block diagram, according to an embodiment of the present invention;

FIG. 256 illustrates an example positive pulse generator of FIG. 255 at a gate level, according to an embodiment of the present invention;

FIG. 257 illustrates an example positive pulse generator of FIG. 255 at a transistor level, according to an embodiment of the present invention;

FIG. 258 illustrates pulse width error effect for ½ cycle;

FIG. 259 illustrates an example single-ended receiver circuit implementation, according to an embodiment of the present invention;

FIG. 260 illustrates an example single-ended receiver circuit implementation, according to an embodiment of the present invention;

FIG. 261 illustrates an example full differential receiver circuit implementation, according to an embodiment of the present invention;

FIG. 262 illustrates an example full differential receiver implementation, according to an embodiment of the present invention;

FIG. 263 illustrates an example single-ended receiver implementation, according to an embodiment of the present invention;

FIG. 264 illustrates a plot of loss in sensitivity vs. clock phase deviation, according to an example embodiment of the present invention;

FIGS. 265 and 266 illustrate example 802.11 WLAN receiver/transmitter implementations, according to embodiments of the present invention;

FIG. 267 illustrates 802.11 requirements in relation to embodiments of the present invention;

FIG. 268 illustrates an example doubler implementation for phase noise cancellation, according to an embodiment of the present invention;

FIG. 269 illustrates an example doubler implementation for phase noise cancellation, according to an embodiment of the present invention;

FIG. 270 illustrates a example bipolar sampling aperture, according to an embodiment of the present invention;

FIG. 271 illustrates an example diversity receiver, according to an embodiment of the present invention;

FIG. 272 illustrates an example equalizer implementation, according to an embodiment of the present invention;

FIG. 273 illustrates an example multiple aperture receiver using two apertures, according to an embodiment of the present invention;

FIG. 274 illustrates exemplary waveforms related to the multiple aperture receiver of FIG. 273, according to an embodiment of the present invention;

FIG. 275 illustrates an example multiple aperture receiver using three apertures, according to an embodiment of the present invention;

FIG. 276 illustrates exemplary waveforms related to the multiple aperture receiver of FIG. 275, according to an embodiment of the present invention;

FIG. 277 illustrates an example multiple aperture transmitter, according to an embodiment of the present invention;

FIG. 278 illustrates example frequency spectrums related to the transmitter of FIG. 277;

FIG. 279 illustrates an example output waveform in a double aperture implementation of the transmitter of FIG. 277;

FIG. 280 illustrates an example output waveform in a single aperture implementation of the transmitter of FIG. 277;

FIG. 281 illustrates an example multiple aperture receiver implementation, according to an embodiment of the present invention;

FIG. 282 illustrates exemplary waveforms in a single aperture implementation of the receiver of FIG. 281, according to an embodiment of the present invention;

FIG. 283 illustrates exemplary waveforms in a dual aperture implementation of the receiver of FIG. 281, according to an embodiment of the present invention;

FIG. 284 illustrates exemplary waveforms in a triple aperture implementation of the receiver of FIG. 281, according to an embodiment of the present invention; and

FIG. 285 illustrates exemplary waveforms in quad aperture implementations of the receiver of FIG. 281, according to embodiments of the present invention.

Detailed Description of the Invention

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3. Benefits of the Invention Using an Example Conventional Receiver for Comparison

II. Under-Sampling

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I. Introduction

1. General Terminology

For illustrative purposes, the operation of the invention is often represented by flowcharts, such as flowchart 1201 in FIG. 12A. It should be understood, however, that the use of flowcharts is for illustrative purposes only, and is not limiting. For example, the invention is not limited to the operational embodiment(s) represented by the flowcharts. Instead, alternative operational embodiments will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein. Also, the use of flowcharts should not be interpreted as limiting the invention to discrete or digital operation. In practice, as will be appreciated by persons skilled in the relevant art(s) based on the herein discussion, the invention can be achieved via discrete or continuous operation, or a combination thereof. Further, the flow of control represented by the flowcharts is provided for illustrative purposes only. As will be appreciated by persons skilled in the relevant art(s), other operational control flows are within the scope and spirit of the present invention. Also, the ordering of steps may differ in various embodiments.

Various terms used in this application are generally described in this section. The description in this section is provided for illustrative and convenience purposes only, and is not limiting. The meaning of these terms will be apparent to persons skilled in the relevant art(s) based on the entirety of the teachings provided herein. These terms may be discussed throughout the specification with additional detail.

The term modulated carrier signal, when used herein, refers to a carrier signal that is modulated by a baseband signal.

The term unmodulated carrier signal, when used herein, refers to a signal having an amplitude that oscillates at a substantially uniform frequency and phase.

The term baseband signal, when used herein, refers to an information signal including, but not limited to, analog information signals, digital information signals and direct current (DC) information signals.

The term carrier signal, when used herein, and unless otherwise specified when used herein, refers to modulated carrier signals and unmodulated carrier signals, information signals, digital information signals, and direct current (DC) information signals.

The term electromagnetic (EM) signal, when used herein, refers to a signal in the EM spectrum. EM spectrum includes all frequencies greater than zero hertz. EM signals generally include waves characterized by variations in electric and magnetic fields. Such waves may be propagated in any medium, both natural and manmade, including but not limited to air, space, wire, cable, liquid, waveguide, micro-strip, strip-line, optical fiber, etc. Unless stated otherwise, all signals discussed herein are EM signals, even when not explicitly designated as such.

The term intermediate frequency (IF) signal, when used herein, refers to an EM signal that is substantially similar to another EM signal except that the IF signal has a lower frequency than the other signal. An IF signal frequency can be any frequency above zero HZ. Unless otherwise stated, the terms lower frequency, intermediate frequency, intermediate and IF are used interchangeably herein.

The term analog signal, when used herein, refers to a signal that is constant or continuously variable, as contrasted to a signal that changes between discrete states.

The term baseband, when used herein, refers to a frequency band occupied by any generic information signal desired for transmission and/or reception.

The term baseband signal, when used herein, refers to any generic information signal desired for transmission and/or reception.

The term carrier frequency, when used herein, refers to the frequency of a carrier signal. Typically, it is the center frequency of a transmission signal that is generally modulated.

The term carrier signal, when used herein, refers to an EM wave having at least one characteristic that may be varied by modulation, that is capable of carrying information via modulation.

The term demodulated baseband signal, when used herein, refers to a signal that results from processing a modulated signal. In some cases, for example, the demodulated baseband signal results from demodulating an intermediate frequency (IF) modulated signal, which results from down converting a modulated carrier signal. In another case, a signal that results from a combined downconversion and demodulation step.

The term digital signal, when used herein, refers to a signal that changes between discrete states, as contrasted to a signal that is continuous. For example, the voltage of a digital signal may shift between discrete levels.

The term electromagnetic (EM) spectrum, when used herein, refers to a spectrum comprising waves characterized by variations in electric and magnetic fields. Such waves may be propagated in any communication medium, both natural and manmade, including but not limited to air, space, wire, cable, liquid, waveguide, microstrip, stripline, optical fiber, etc. The EM spectrum includes all frequencies greater than zero hertz.

The term electromagnetic (EM) signal, when used herein, refers to a signal in the EM spectrum. Also generally called an EM wave. Unless stated

otherwise, all signals discussed herein are EM signals, even when not explicitly designated as such.

The term modulating baseband signal, when used herein, refers to any generic information signal that is used to modulate an oscillating signal, or carrier signal.

1.1 Modulation

It is often beneficial to propagate electromagnetic (EM) signals at higher frequencies. This includes baseband signals, such as digital data information signals and analog information signals. A baseband signal can be up-converted to a higher frequency EM signal by using the baseband signal to modulate a higher frequency carrier signal, F_C. When used in this manner, such a baseband signal is herein called a modulating baseband signal F_{MB}.

Modulation imparts changes to the carrier signal F_C that represent information in the modulating baseband signal F_{MB}. The changes can be in the form of amplitude changes, frequency changes, phase changes, etc., or any combination thereof. The resultant signal is referred to herein as a modulated carrier signal F_{MC}. The modulated carrier signal F_{MC} includes the carrier signal F_C modulated by the modulating baseband signal, F_{MB}, as in:

$$F_{MB} \text{ combined with } F_C \rightarrow F_{MC}$$

The modulated carrier signal F_{MC} oscillates at, or near the frequency of the carrier signal F_C and can thus be efficiently propagated.

FIG. 1 illustrates an example modulator 110, wherein the carrier signal F_C is modulated by the modulating baseband signal F_{MB}, thereby generating the modulated carrier signal F_{MC}.

Modulating baseband signal F_{MB} can be an analog baseband signal, a digital baseband signal, or a combination thereof.

FIG. 2 illustrates the modulating baseband signal F_{MB} as an exemplary analog modulating baseband signal 210. The exemplary analog modulating baseband signal 210 can represent any type of analog information including, but not limited to, voice/speech data, music data, video data, etc. The amplitude of analog modulating baseband signal 210 varies in time.

Digital information includes a plurality of discrete states. For ease of explanation, digital information signals are discussed below as having two discrete states. But the invention is not limited to this embodiment.

FIG. 3 illustrates the modulating baseband signal F_{MB} as an exemplary digital modulating baseband signal 310. The digital modulating baseband signal 310 can represent any type of digital data including, but not limited to, digital computer information and digitized analog information. The digital modulating baseband signal 310 includes a first state 312 and a second state 314. In an embodiment, first state 312 represents binary state 0 and second state 314 represents binary state 1. Alternatively, first state 312 represents binary state 1 and second state 314 represents binary state 0. Throughout the remainder of this disclosure, the former convention is followed, whereby first state 312 represents binary state zero and second state 314 represents binary state one. But the invention is not limited to this embodiment. First state 312 is thus referred to herein as a low state and second state 314 is referred to herein as a high state.

Digital modulating baseband signal 310 can change between first state 312 and second state 314 at a data rate, or baud rate, measured as bits per second.

Carrier signal F_C is modulated by the modulating baseband signal $F_{MB,}$ by any modulation technique, including, but not limited to, amplitude modulation (AM), frequency modulation (FM), phase modulation (PM), etc., or any combination thereof. Examples are provided below for amplitude modulating, frequency modulating, and phase modulating the analog

modulating baseband signal 210 and the digital modulating baseband signal 310, on the carrier signal F_C. The examples are used to assist in the description of the invention. The invention is not limited to, or by, the examples.

FIG. 4 illustrates the carrier signal F_C as a carrier signal 410. In the example of FIG. 4, the carrier signal 410 is illustrated as a 900 MHZ carrier signal. Alternatively, the carrier signal 410 can be any other frequency. Example modulation schemes are provided below, using the examples signals from FIGS. 2, 3 and 4.

1.1.1 Amplitude Modulation

In amplitude modulation (AM), the amplitude of the modulated carrier signal F_{MC} is a function of the amplitude of the modulating baseband signal F_{MB}. FIGS. 5A-5C illustrate example timing diagrams for amplitude modulating the carrier signal 410 with the analog modulating baseband signal 210. FIGS. 6A-6C illustrate example timing diagrams for amplitude modulating the carrier signal 410 with the digital modulating baseband signal 310.

FIG. 5A illustrates the analog modulating baseband signal 210. FIG. 5B illustrates the carrier signal 410. FIG. 5C illustrates an analog AM carrier signal 516, which is generated when the carrier signal 410 is amplitude modulated using the analog modulating baseband signal 210. As used herein, the term "analog AM carrier signal" is used to indicate that the modulating baseband signal is an analog signal.

The analog AM carrier signal 516 oscillates at the frequency of carrier signal 410. The amplitude of the analog AM carrier signal 516 tracks the amplitude of analog modulating baseband signal 210, illustrating that the information contained in the analog modulating baseband signal 210 is retained in the analog AM carrier signal 516.

FIG. 6A illustrates the digital modulating baseband signal 310. FIG. 6B illustrates the carrier signal 410. FIG. 6C illustrates a digital AM carrier signal 616, which is generated when the carrier signal 410 is amplitude modulated using the digital modulating baseband signal 310. As used herein, the term "digital AM carrier signal" is used to indicate that the modulating baseband signal is a digital signal.

The digital AM carrier signal 616 oscillates at the frequency of carrier signal 410. The amplitude of the digital AM carrier signal 616 tracks the amplitude of digital modulating baseband signal 310, illustrating that the information contained in the digital modulating baseband signal 310 is retained in the digital AM signal 616. As the digital modulating baseband signal 310 changes states, the digital AM signal 616 shifts amplitudes. Digital amplitude modulation is often referred to as amplitude shift keying (ASK) , and the two terms are used interchangeably throughout the specification.

1.1.2 Frequency Modulation

In frequency modulation (FM), the frequency of the modulated carrier signal F_{MC} varies as a function of the amplitude of the modulating baseband signal F_{MB}. FIGS. 7A-7C illustrate example timing diagrams for frequency modulating the carrier signal 410 with the analog modulating baseband signal 210. FIGS. 8A-8C illustrate example timing diagrams for frequency modulating the carrier signal 410 with the digital modulating baseband signal 310.

FIG. 7A illustrates the analog modulating baseband signal 210. FIG. 7B illustrates the carrier signal 410. FIG. 7C illustrates an analog FM carrier signal 716, which is generated when the carrier signal 410 is frequency modulated using the analog modulating baseband signal 210. As used herein, the term "analog FM carrier signal" is used to indicate that the modulating baseband signal is an analog signal.

The frequency of the analog FM carrier signal 716 varies as a function of amplitude changes on the analog baseband signal 210. In the illustrated example, the frequency of the analog FM carrier signal 716 varies in proportion to the amplitude of the analog modulating baseband signal 210. Thus, at time t1, the amplitude of the analog baseband signal 210 and the frequency of the analog FM carrier signal 716 are at maximums. At time t3, the amplitude of the analog baseband signal 210 and the frequency of the analog AM carrier signal 716 are at minimums.

The frequency of the analog FM carrier signal 716 is typically centered around the frequency of the carrier signal 410. Thus, at time t2, for example, when the amplitude of the analog baseband signal 210 is at a mid-point, illustrated here as zero volts, the frequency of the analog FM carrier signal 716 is substantially the same as the frequency of the carrier signal 410.

FIG. 8A illustrates the digital modulating baseband signal 310. FIG. 8B illustrates the carrier signal 410. FIG. 8C illustrates a digital FM carrier signal 816, which is generated when the carrier signal 410 is frequency modulated using the digital baseband signal 310. As used herein, the term "digital FM carrier signal" is used to indicate that the modulating baseband signal is a digital signal.

The frequency of the digital FM carrier signal 816 varies as a function of amplitude changes on the digital modulating baseband signal 310. In the illustrated example, the frequency of the digital FM carrier signal 816 varies in proportion to the amplitude of the digital modulating baseband signal 310. Thus, between times t0 and t1, and between times t2 and t4, when the amplitude of the digital baseband signal 310 is at the higher amplitude second state, the frequency of the digital FM carrier signal 816 is at a maximum. Between times t1 and t2, when the amplitude of the digital baseband signal 310 is at the lower amplitude first state, the frequency of the digital FM carrier signal 816 is at a minimum. Digital frequency modulation is often referred to

as frequency shift keying (FSK), and the terms are used interchangeably throughout the specification.

Typically, the frequency of the digital FM carrier signal 816 is centered about the frequency of the carrier signal 410, and the maximum and minimum frequencies are equally offset from the center frequency. Other variations can be employed but, for ease of illustration, this convention will be followed herein.

1.1.3 Phase Modulation

In phase modulation (PM), the phase of the modulated carrier signal F_{MC} varies as a function of the amplitude of the modulating baseband signal F_{MB}. FIGS. 9A-9C illustrate example timing diagrams for phase modulating the carrier signal 410 with the analog modulating baseband signal 210. FIGS. 10A-10C illustrate example timing diagrams for phase modulating the carrier signal 410 with the digital modulating baseband signal 310.

FIG. 9A illustrates the analog modulating baseband signal 210. FIG. 9B illustrates the carrier signal 410. FIG. 9C illustrates an analog PM carrier signal 916, which is generated by phase modulating the carrier signal 410 with the analog baseband signal 210. As used herein, the term "analog PM carrier signal" is used to indicate that the modulating baseband signal is an analog signal.

Generally, the frequency of the analog PM carrier signal 916 is substantially the same as the frequency of carrier signal 410. But the phase of the analog PM carrier signal 916 varies with amplitude changes on the analog modulating baseband signal 210. For relative comparison, the carrier signal 410 is illustrated in FIG. 9C by a dashed line.

The phase of the analog PM carrier signal 916 varies as a function of amplitude changes of the analog baseband signal 210. In the illustrated example, the phase of the analog PM signal 916 lags by a varying amount as

determined by the amplitude of the baseband signal 210. For example, at time t1, when the amplitude of the analog baseband signal 210 is at a maximum, the analog PM carrier signal 916 is in phase with the carrier signal 410. Between times t1 and t3, when the amplitude of the analog baseband signal 210 decreases to a minimum amplitude, the phase of the analog PM carrier signal 916 lags the phase of the carrier signal 410, until it reaches a maximum out of phase value at time t3. In the illustrated example, the phase change is illustrated as approximately 180 degrees. Any suitable amount of phase change, varied in any manner that is a function of the baseband signal, can be utilized.

FIG. 10A illustrates the digital modulating baseband signal 310. FIG. 10B illustrates the carrier signal 410. FIG. 10C illustrates a digital PM carrier signal 1016, which is generated by phase modulating the carrier signal 410 with the digital baseband signal 310. As used herein, the term "digital PM carrier signal" is used to indicate that the modulating baseband signal is a digital signal.

The frequency of the digital PM carrier signal 1016 is substantially the same as the frequency of carrier signal 410. The phase of the digital PM carrier signal 1016 varies as a function of amplitude changes on the digital baseband signal 310. In the illustrated example, when the digital baseband signal 310 is at the first state 312, the digital PM carrier signal 1016 is out of phase with the carrier signal 410. When the digital baseband signal 310 is at the second state 314, the digital PM carrier signal 1016 is in-phase with the carrier signal 410. Thus, between times t1 and t2, when the amplitude of the digital baseband signal 310 is at the first state 312, the digital PM carrier signal 1016 is out of phase with the carrier signal 410. Between times t0 and t1, and between times t2 and t4, when the amplitude of the digital baseband signal 310 is at the second state 314, the digital PM carrier signal 1016 is in phase with the carrier signal 410.

In the illustrated example, the out of phase value between times t1 and t3 is illustrated as approximately 180 degrees out of phase. Any suitable amount of phase change, varied in any manner that is a function of the baseband signal, can be utilized. Digital phase modulation is often referred to as phase shift keying (PSK) , and the terms are used interchangeably throughout the specification.

1.2 Demodulation

When the modulated carrier signal F_{MC} is received, it can be demodulated to extract the modulating baseband signal F_{MB}. Because of the typically high frequency of modulated carrier signal F_{MC}, however, it is generally impractical to demodulate the baseband signal F_{MB} directly from the modulated carrier signal F_{MC}. Instead, the modulated carrier signal F_{MC} must be down-converted to a lower frequency signal that contains the original modulating baseband signal.

When a modulated carrier signal is down-converted to a lower frequency signal, the lower frequency signal is referred to herein as an intermediate frequency (IF) signal F_{IF}. The IF signal F_{IF} oscillates at any frequency, or frequency band, below the frequency of the modulated carrier frequency F_{MC}. Down-conversion of F_{MC} to F_{IF} is illustrated as:

$$F_{MC} \rightarrow F_{IF}$$

After F_{MC} is down-converted to the IF modulated carrier signal F_{IF}, F_{IF} can be demodulated to a baseband signal F_{DMB}, as illustrated by:

$$F_{IF} \rightarrow F_{DMB}$$

F_{DMB} is intended to be substantially similar to the modulating baseband signal F_{MB}, illustrating that the modulating baseband signal F_{MB} can be substantially recovered.

It will be emphasized throughout the disclosure that the present invention can be implemented with any type of EM signal, including, but not limited to, modulated carrier signals and unmodulated carrier signals. The above examples of modulated carrier signals are provided for illustrative purposes only. Many variations to the examples are possible. For example, a carrier signal can be modulated with a plurality of the modulation types described above. A carrier signal can also be modulated with a plurality of baseband signals, including analog baseband signals, digital baseband signals, and combinations of both analog and digital baseband signals.

2. Overview of the Invention

Conventional signal processing techniques follow the Nyquist sampling theorem, which states that, in order to faithfully reproduce a sampled signal, the signal must be sampled at a rate that is greater than twice the frequency of the signal being sampled. When a signal is sampled at less than or equal to twice the frequency of the signal, the signal is said to be under-sampled, or aliased. Conventional signal processing thus teaches away from under-sampling and aliasing, in order to faithfully reproduce a sampled signal.

2.1 Aspects of the Invention

Contrary to conventional wisdom, the present invention is a method and system for down-converting an electromagnetic (EM) signal by aliasing the EM signal. Aliasing is represented generally in FIG. 45A as 4502.

By taking a carrier and aliasing it at an aliasing rate, the invention can down-convert that carrier to lower frequencies. One aspect that can be

exploited by this invention is realizing that the carrier is not the item of interest, the lower baseband signal is of interest to reproduce sufficiently. This baseband signal's frequency content, even though its carrier may be aliased, does satisfy the Nyquist criteria and as a result, the baseband information can be sufficiently reproduced.

FIG. 12A depicts a flowchart 1201 that illustrates a method for aliasing an EM signal to generate a down-converted signal. The process begins at step 1202, which includes receiving the EM signal. Step 1204 includes receiving an aliasing signal having an aliasing rate. Step 1206 includes aliasing the EM signal to down-convert the EM signal. The term aliasing, as used herein, refers to both down-converting an EM signal by under-sampling the EM signal at an aliasing rate and to down-converting an EM signal by transferring energy from the EM signal at the aliasing rate. These concepts are described below.

FIG. 13 illustrates a block diagram of a generic aliasing system 1302, which includes an aliasing module 1306. In an embodiment, the aliasing system 1302 operates in accordance with the flowchart 1201. For example, in step 1202, the aliasing module 1306 receives an EM signal 1304. In step 1204, the aliasing module 1306 receives an aliasing signal 1310. In step 1206, the aliasing module 1306 down-converts the EM signal 1304 to a down-converted signal 1308. The generic aliasing system 1302 can also be used to implement any of the flowcharts 1207, 1213 and 1219.

In an embodiment, the invention down-converts the EM signal to an intermediate frequency (IF) signal. FIG. 12B depicts a flowchart 1207 that illustrates a method for under-sampling the EM signal at an aliasing rate to down-convert the EM signal to an IF signal. The process begins at step 1208, which includes receiving an EM signal. Step 1210 includes receiving an aliasing signal having an aliasing rate F_{AR}. Step 1212 includes under-sampling the EM signal at the aliasing rate to down- convert the EM signal to an IF signal.

In another embodiment, the invention down-converts the EM signal to a demodulated baseband information signal. FIG. 12C depicts a flowchart 1213 that illustrates a method for down- converting the EM signal to a demodulated baseband signal. The process begins at step 1214, which includes receiving an EM signal. Step 1216 includes receiving an aliasing signal having an aliasing rate F_{AR}. Step 1218 includes down-converting the EM signal to a demodulated baseband signal. The demodulated baseband signal can be processed without further down-conversion or demodulation.

In another embodiment, the EM signal is a frequency modulated (FM) signal, which is down-converted to a non-FM signal, such as a phase modulated (PM) signal or an amplitude modulated (AM) signal. FIG. 12D depicts a flowchart 1219 that illustrates a method for down-converting the FM signal to a non-FM signal. The process begins at step 1220, which includes receiving an EM signal. Step 1222 includes receiving an aliasing signal having an aliasing rate. Step 1224 includes down-converting the FM signal to a non-FM signal.

The invention down-converts any type of EM signal, including, but not limited to, modulated carrier signals and unmodulated carrier signals. For ease of discussion, the invention is further described herein using modulated carrier signals for examples. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention can be implemented to down-convert signals other than carrier signals as well. The invention is not limited to the example embodiments described above.

In an embodiment, down-conversion is accomplished by under-sampling an EM signal. This is described generally in Section I.2.2. below and in detail in Section II and its sub-sections. In another embodiment, down-conversion is achieved by transferring non-negligible amounts of energy from an EM signal. This is described generally in Section I.2.3. below and in detail in Section III.

2.2 Down-Converting by Under-Sampling

The term aliasing, as used herein, refers both to down-converting an EM signal by under-sampling the EM signal at an aliasing rate and to down-converting an EM signal by transferring energy from the EM signal at the aliasing rate. Methods for under-sampling an EM signal to down-convert the EM signal are now described at an overview level. FIG. 14A depicts a flowchart 1401 that illustrates a method for under-sampling the EM signal at an aliasing rate to down-convert the EM signal. The process begins at step 1402, which includes receiving an EM signal. Step 1404 includes receiving an under-sampling signal having an aliasing rate. Step 1406 includes under-sampling the EM signal at the aliasing rate to down-convert the EM signal.

Down-converting by under-sampling is illustrated by 4504 in FIG. 45A and is described in greater detail in Section II.

2.2.1 Down-Converting to an Intermediate Frequency (IF) Signal

In an embodiment, an EM signal is under-sampled at an aliasing rate to down-convert the EM signal to a lower, or intermediate frequency (IF) signal. The EM signal can be a modulated carrier signal or an unmodulated carrier signal. In an exemplary example, a modulated carrier signal F_{MC} is down-converted to an IF signal F_{IF}.

$$F_{MC} \rightarrow F_{IF}$$

FIG. 14B depicts a flowchart 1407 that illustrates a method for under-sampling the EM signal at an aliasing rate to down-convert the EM signal to an IF signal. The process begins at step 1408, which includes receiving an EM signal. Step 1410 includes receiving an under-sampling signal having an

aliasing rate. Step 1412 includes under-sampling the EM signal at the aliasing rate to down-convert the EM signal to an IF signal.

This embodiment is illustrated generally by 4508 in FIG. 45B and is described in Section II.1.

2.2.2 Direct-to-Data Down-Converting

In another embodiment, an EM signal is directly down-converted to a demodulated baseband signal (direct-to-data down-conversion), by under-sampling the EM signal at an aliasing rate. The EM signal can be a modulated EM signal or an unmodulated EM signal. In an exemplary embodiment, the EM signal is the modulated carrier signal F_{MC}, and is directly down-converted to a demodulated baseband signal F_{DMB}.

$$F_{MC} \rightarrow F_{DMB}$$

FIG. 14C depicts a flowchart 1413 that illustrates a method for under-sampling the EM signal at an aliasing rate to directly down-convert the EM signal to a demodulated baseband signal. The process begins at step 1414, which includes receiving an EM signal. Step 1416 includes receiving an under-sampling signal having an aliasing rate. Step 1418 includes under-sampling the EM signal at the aliasing rate to directly down-convert the EM signal to a baseband information signal.

This embodiment is illustrated generally by 4510 in FIG. 45B and is described in Section II.2

2.2.3 Modulation Conversion

In another embodiment, a frequency modulated (FM) carrier signal F_{FMC} is converted to a non-FM signal $F_{(NON\text{-}FM)}$, by under-sampling the FM carrier signal F_{FMC}.

$$F_{FMC} \rightarrow F_{(NON\text{-}FM)}$$

FIG. 14D depicts a flowchart 1419 that illustrates a method for under-sampling an FM signal to convert it to a non-FM signal. The process begins at step 1420, which includes receiving the FM signal. Step 1422 includes receiving an under-sampling signal having an aliasing rate. Step 1424 includes under-sampling the FM signal at the aliasing rate to convert the FM signal to a non-FM signal. For example, the FM signal can be under-sampled to convert it to a PM signal or an AM signal.

This embodiment is illustrated generally by 4512 in FIG. 45B, and described in Section II.3

2.3 Down-Converting by Transferring Energy

The term aliasing, as used herein, refers both to down-converting an EM signal by under-sampling the EM signal at an aliasing rate and to down-converting an EM signal by transferring non-negligible amounts energy from the EM signal at the aliasing rate. Methods for transferring energy from an EM signal to down-convert the EM signal are now described at an overview level. More detailed descriptions are provided in Section III.

FIG. 46A depicts a flowchart 4601 that illustrates a method for transferring energy from the EM signal at an aliasing rate to down-convert the EM signal. The process begins at step 4602, which includes receiving an EM signal. Step 4604 includes receiving an energy transfer signal having an

aliasing rate. Step 4606 includes transferring energy from the EM signal at the aliasing rate to down-convert the EM signal.

Down-converting by transferring energy is illustrated by 4506 in FIG. 45A and is described in greater detail in Section III.

2.3.1 Down-Converting to an Intermediate Frequency (IF) Signal

In an embodiment, EM signal is down-converted to a lower, or intermediate frequency (IF) signal, by transferring energy from the EM signal at an aliasing rate. The EM signal can be a modulated carrier signal or an unmodulated carrier signal. In an exemplary example, a modulated carrier signal F_{MC} is down-converted to an IF signal F_{IF}.

$$F_{MC} \rightarrow F_{IF}$$

FIG. 46B depicts a flowchart 4607 that illustrates a method for transferring energy from the EM signal at an aliasing rate to down-convert the EM signal to an IF signal. The process begins at step 4608, which includes receiving an EM signal. Step 4610 includes receiving an energy transfer signal having an aliasing rate. Step 4612 includes transferring energy from the EM signal at the aliasing rate to down-convert the EM signal to an IF signal.

This embodiment is illustrated generally by 4514 in FIG. 45B and is described in Section III.1.

2.3.2 Direct-to-Data Down-Converting

In another embodiment, an EM signal is down-converted to a demodulated baseband signal by transferring energy from the EM signal at an aliasing rate. This embodiment is referred to herein as direct-to-data down-conversion. The EM signal can be a modulated EM signal or an unmodulated

EM signal. In an exemplary embodiment, the EM signal is the modulated carrier signal F_{MC}, and is directly down-converted to a demodulated baseband signal F_{DMB}.

$$F_{MC} \rightarrow F_{DMB}$$

FIG. 46C depicts a flowchart 4613 that illustrates a method for transferring energy from the EM signal at an aliasing rate to directly down-convert the EM signal to a demodulated baseband signal. The process begins at step 4614, which includes receiving an EM signal. Step 4616 includes receiving an energy transfer signal having an aliasing rate. Step 4618 includes transferring energy from the EM signal at the aliasing rate to directly down-convert the EM signal to a baseband signal.

This embodiment is illustrated generally by 4516 in FIG. 45B and is described in Section III.2

2.3.3 Modulation Conversion

In another embodiment, a frequency modulated (FM) carrier signal F_{FMC} is converted to a non-FM signal $F_{(NON\text{-}FM)}$, by transferring energy from the FM carrier signal F_{FMC} at an aliasing rate.

$$F_{FMC} \rightarrow F_{(NON\text{-}FM)}$$

The FM carrier signal F_{FMC} can be converted to, for example, a phase modulated (PM) signal or an amplitude modulated (AM) signal. FIG. 46D depicts a flowchart 4619 that illustrates a method for transferring energy from an FM signal to convert it to a non-FM signal. Step 4620 includes receiving the FM signal. Step 4622 includes receiving an energy transfer signal having an aliasing rate. In FIG. 46D, step 4612 includes transferring energy from the

FM signal to convert it to a non-FM signal. For example, energy can be transferred from an FSK signal to convert it to a PSK signal or an ASK signal.

This embodiment is illustrated generally by 4518 in FIG. 45B, and described in Section III.3

2.3 Determining the Aliasing Rate

In accordance with the definition of aliasing, the aliasing rate is equal to, or less than, twice the frequency of the EM carrier signal. Preferably, the aliasing rate is much less than the frequency of the carrier signal. The aliasing rate is preferably more than twice the highest frequency component of the modulating baseband signal F_{MB} that is to be reproduced. The above requirements are illustrated in EQ. (1).

$$2 \bullet F_{MC} \geq F_{AR} > 2 \bullet \text{(Highest Freq. Component of } F_{MB}) \qquad \text{EQ. (1)}$$

In other words, by taking a carrier and aliasing it at an aliasing rate, the invention can down-convert that carrier to lower frequencies. One aspect that can be exploited by this invention is that the carrier is not the item of interest; instead the lower baseband signal is of interest to be reproduced sufficiently. The baseband signal's frequency content, even though its carrier may be aliased, satisfies the Nyquist criteria and as a result, the baseband information can be sufficiently reproduced, either as the intermediate modulating carrier signal F_{IF} or as the demodulated direct-to-data baseband signal F_{DMB}.

In accordance with the invention, relationships between the frequency of an EM carrier signal, the aliasing rate, and the intermediate frequency of the down-converted signal, are illustrated in EQ. (2).

$$F_C = n \bullet F_{AR} \pm F_{IF} \qquad \text{EQ. (2)}$$

Where:

F_C is the frequency of the EM carrier signal that is to be aliased;

F_{AR} is the aliasing rate;

n identifies a harmonic or sub-harmonic of the aliasing rate (generally, n=0.5, 1, 2, 3, 4, . . .); and

F_{IF} is the intermediate frequency of the down-converted signal.

Note that as $(n \bullet F_{AR})$ approaches F_C, F_{IF} approaches zero. This is a special case where an EM signal is directly down-converted to a demodulated baseband signal. This special case is referred to herein as Direct-to-Data down-conversion. Direct-to-Data down-conversion is described in later sections.

High level descriptions, exemplary embodiments and exemplary implementations of the above and other embodiments of the invention are provided in sections below.

3. Benefits of the Invention Using an Example Conventional Receiver for Comparison

FIG. 11 illustrates an example conventional receiver system 1102. The conventional system 1102 is provided both to help the reader to understand the functional differences between conventional systems and the present invention, and to help the reader to understand the benefits of the present invention.

The example conventional receiver system 1102 receives an electromagnetic (EM) signal 1104 via an antenna 1106. The EM signal 1104 can include a plurality of EM signals such as modulated carrier signals. For example, the EM signal 1104 includes one or more radio frequency (RF) EM signals, such as a 900 MHZ modulated carrier signal. Higher frequency RF signals, such as 900 MHZ signals, generally cannot be directly processed by

conventional signal processors. Instead, higher frequency RF signals are typically down-converted to lower intermediate frequencies (IF) for processing. The receiver system 1102 down-converts the EM signal 1104 to an intermediate frequency (IF) signal 1108n, which can be provided to a signal processor 1110. When the EM signal 1104 includes a modulated carrier signal, the signal processor 1110 usually includes a demodulator that demodulates the IF signal 1108n to a baseband information signal (demodulated baseband signal).

Receiver system 1102 includes an RF stage 1112 and one or more IF stages 1114. The RF stage 1112 receives the EM signal 1104. The RF stage 1112 includes the antenna 1106 that receives the EM signal 1104.

The one or more IF stages 1114a-1114n down-convert the EM signal 1104 to consecutively lower intermediate frequencies. Each of the one or more IF sections 1114a-1114n includes a mixer 1118a-1118n that down-converts an input EM signal 1116 to a lower frequency IF signal 1108. By cascading the one or more mixers 1118a-1118n, the EM signal 1104 is incrementally down-converted to a desired IF signal 1108n.

In operation, each of the one or more mixers 1118 mixes an input EM signal 1116 with a local oscillator (LO) signal 1119, which is generated by a local oscillator (LO) 1120. Mixing generates sum and difference signals from the input EM signal 1116 and the LO signal 1119. For example, mixing an input EM signal 1116a, having a frequency of 900 MHZ, with a LO signal 1119a, having a frequency of 830 MHZ, results in a sum signal, having a frequency of 900 MHZ + 830 MHZ = 1.73 GHZ, and a difference signal, having a frequency of 900 MHZ - 830 MHZ = 70 MHZ.

Specifically, in the example of FIG. 11, the one or more mixers 1118 generate a sum and difference signals for all signal components in the input EM signal 1116. For example, when the EM signal 1116a includes a second EM signal, having a frequency of 760 MHZ, the mixer 1118a generates a

second sum signal, having a frequency of 760 MHZ + 830 MHZ = 1.59 GHZ, and a second difference signal, having a frequency of 830 MHZ - 760 MHZ = 70 MHZ. In this example, therefore, mixing two input EM signals, having frequencies of 900 MHZ and 760 MHZ, respectively, with an LO signal having a frequency of 830 MHZ, results in two IF signals at 70 MHZ.

Generally, it is very difficult, if not impossible, to separate the two 70 MHZ signals. Instead, one or more filters 1122 and 1123 are provided upstream from each mixer 1118 to filter the unwanted frequencies, also known as image frequencies. The filters 1122 and 1123 can include various filter topologies and arrangements such as bandpass filters, one or more high pass filters, one or more low pass filters, combinations thereof, etc.

Typically, the one or more mixers 1118 and the one or more filters 1122 and 1123 attenuate or reduce the strength of the EM signal 1104. For example, a typical mixer reduces the EM signal strength by 8 to 12 dB. A typical filter reduces the EM signal strength by 3 to 6 dB.

As a result, one or more low noise amplifiers (LNAs) 1121 and 1124a-1124n are provided upstream of the one or more filters 1123 and 1122a-1122n. The LNAs and filters can be in reversed order. The LNAs compensate for losses in the mixers 1118, the filters 1122 and 1123, and other components by increasing the EM signal strength prior to filtering and mixing. Typically, for example, each LNA contributes 15 to 20 dB of amplification.

However, LNAs require substantial power to operate. Higher frequency LNAs require more power than lower frequency LNAs. When the receiver system 1102 is intended to be portable, such as a cellular telephone receiver, for example, the LNAs require a substantial portion of the total power.

At higher frequencies, impedance mismatches between the various stages further reduce the strength of the EM signal 1104. In order to optimize power transferred through the receiver system 1102, each component should

be impedance matched with adjacent components. Since no two components have the exact same impedance characteristics, even for components that were manufactured with high tolerances, impedance matching must often be individually fine tuned for each receiver system 1102. As a result, impedance matching in conventional receivers tends to be labor intensive and more art than science. Impedance matching requires a significant amount of added time and expense to both the design and manufacture of conventional receivers. Since many of the components, such as LNA, filters, and impedance matching circuits, are highly frequency dependent, a receiver designed for one application is generally not suitable for other applications. Instead, a new receiver must be designed, which requires new impedance matching circuits between many of the components.

Conventional receiver components are typically positioned over multiple IC substrates instead of on a single IC substrate. This is partly because there is no single substrate that is optimal for both RF, IF, and baseband frequencies. Other factors may include the sheer number of components, their various sizes and different inherent impedance characteristics, etc. Additional signal amplification is often required when going from chip to chip. Implementation over multiple substrates thus involves many costs in addition to the cost of the ICs themselves.

Conventional receivers thus require many components, are difficult and time consuming to design and manufacture, and require substantial external power to maintain sufficient signal levels. Conventional receivers are thus expensive to design, build, and use.

In an embodiment, the present invention is implemented to replace many, if not all, of the components between the antenna 1106 and the signal processor 1110, with an aliasing module that includes a universal frequency translator (UFT) module. (More generally, the phrase "universal frequency translator," "universal frequency translation," "UFT," "UFT transform," and

"UFT technology" (or similar phrases) are used herein to refer to the frequency translation technology/concepts described herein.) The UFT is able to down-convert a wide range of EM signal frequencies using very few components. The UFT is easy to design and build, and requires very little external power. The UFT design can be easily tailored for different frequencies or frequency ranges. For example, UFT design can be easily impedance matched with relatively little tuning. In a direct-to-data embodiment of the invention, where an EM signal is directly down-converted to a demodulated baseband signal, the invention also eliminates the need for a demodulator in the signal processor 1110.

When the invention is implemented in a receiver system, such as the receiver system 1102, power consumption is significantly reduced and signal to noise ratio is significantly increased.

In an embodiment, the invention can be implemented and tailored for specific applications with easy to calculate and easy to implement impedance matching circuits. As a result, when the invention is implemented as a receiver, such as the receiver 1102, specialized impedance matching experience is not required.

In conventional receivers, components in the IF sections comprise roughly eighty to ninety percent of the total components of the receivers. The UFT design eliminates the IF section(s) and thus eliminates the roughly eighty to ninety percent of the total components of conventional receivers.

Other advantages of the invention include, but are not limited to:

The invention can be implemented as a receiver with only a single local oscillator;

The invention can be implemented as a receiver with only a single, lower frequency, local oscillator;

The invention can be implemented as a receiver using few filters;

The invention can be implemented as a receiver using unit delay filters;

The invention can be implemented as a receiver that can change frequencies and receive different modulation formats with no hardware changes;

The invention can be also be implemented as frequency up-converter in an EM signal transmitter;

The invention can be also be implemented as a combination up-converter (transmitter) and down-converter (receiver), referred to herein as a transceiver;

The invention can be implemented as a method and system for ensuring reception of a communications signal, as disclosed in co-pending patent application titled, "Method and System for Ensuring Reception of a Communications Signal," Attorney Docket No. ~~1744.0030000~~ Ser. No. 09/176,415 (now U.S. Patent No. 6,091,940), incorporated herein by reference in its entirety;

The invention can be implemented in a differential configuration, whereby signal to noise ratios are increased;

A receiver designed in accordance with the invention can be implemented on a single IC substrate, such as a silicon-based IC substrate;

A receiver designed in accordance with the invention and implemented on a single IC substrate, such as a silicon-based IC substrate, can down-convert EM signals from frequencies in the giga Hertz range;

A receiver built in accordance with the invention has a relatively flat response over a wide range of frequencies. For example, in an embodiment, a receiver built in accordance with the invention to operate around 800 MHZ has a substantially flat response (i.e., plus or minus a few dB of power) from 100 MHZ to 1 GHZ. This is referred to herein as a wide-band receiver; and

A receiver built in accordance with the invention can include multiple, user-selectable, Impedance match modules, each designed for a different wide-

band of frequencies, which can be used to scan an ultra-wide-band of frequencies.

II. Down-Converting by Under-Sampling

1. Down-Converting an EM Carrier Signal to an EM Intermediate Signal by Under- Sampling the EM Carrier Signal at the Aliasing Rate

In an embodiment, the invention down-converts an EM signal to an IF signal by under-sampling the EM signal. This embodiment is illustrated by 4508 in FIG. 45B.

This embodiment can be implemented with modulated and unmodulated EM signals. This embodiment is described herein using the modulated carrier signal F_{MC} in FIG. 1, as an example. In the example, the modulated carrier signal F_{MC} is down-converted to an IF signal F_{IF}. The IF signal F_{IF} can then be demodulated, with any conventional demodulation technique to obtain a demodulated baseband signal F_{DMB}. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention can be implemented to down-convert any EM signal, including but not limited to, modulated carrier signals and unmodulated carrier signals.

The following sections describe example methods for down-converting the modulated carrier signal F_{MC} to the IF signal F_{IF}, according to embodiments of the invention. Exemplary structural embodiments for implementing the methods are also described. It should be understood that the invention is not limited to the particular embodiments described below. Equivalents, extensions, variations, deviations, etc., of the following will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such equivalents, extensions, variations, deviations, etc., are within the scope and spirit of the present invention.

The following sections include a high level discussion, example embodiments, and implementation examples.

1.1 High Level Description

This section (including its subsections) provides a high-level description of down-converting an EM signal to an IF signal $F_{IF,}$ according to an embodiment of the invention. In particular, an operational process of under-sampling a modulated carrier signal F_{MC} to down-convert it to the IF signal F_{IF}, is described at a high-level. Also, a structural implementation for implementing this process is described at a high-level. This structural implementation is described herein for illustrative purposes, and is not limiting. In particular, the process described in this section can be achieved using any number of structural implementations, one of which is described in this section. The details of such structural implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

1.1.1 Operational Description

FIG. 14B depicts a flowchart 1407 that illustrates an exemplary method for under-sampling an EM signal to down-convert the EM signal to an intermediate signal F_{IF}. The exemplary method illustrated in the flowchart 1407 is an embodiment of the flowchart 1401 in FIG. 14A.

Any and all combinations of modulation techniques are valid for this invention. For ease of discussion, the digital AM carrier signal 616 is used to illustrate a high level operational description of the invention. Subsequent sections provide detailed flowcharts and descriptions for AM, FM and PM example embodiments. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention can be

implemented to down-convert any type of EM signal, including any form of modulated carrier signal and unmodulated carrier signals.

The method illustrated in the flowchart 1407 is now described at a high level using the digital AM carrier signal 616 of FIG. 6C. The digital AM carrier signal 616 is re-illustrated in FIG. 15A for convenience. FIG. 15E illustrates a portion 1510 of the AM carrier signal 616, between time t1 and t2, on an expanded time scale.

The process begins at step 1408, which includes receiving an EM signal. Step 1408 is represented by the digital AM carrier signal 616.

Step 1410 includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. 15B illustrates an example under-sampling signal 1502, which includes a train of pulses 1504 having negligible apertures that tend toward zero time in duration. The pulses 1504 repeat at the aliasing rate, or pulse repetition rate. Aliasing rates are discussed below.

Step 1412 includes under-sampling the EM signal at the aliasing rate to down-convert the EM signal to the intermediate signal F_{IF}. When down-converting an EM signal to an IF signal, the frequency or aliasing rate of the pulses 1504 sets the IF.

FIG. 15C illustrates a stair step AM intermediate signal 1506, which is generated by the down-conversion process. The AM intermediate signal 1506 is similar to the AM carrier signal 616 except that the AM intermediate signal 1506 has a lower frequency than the AM carrier signal 616. The AM carrier signal 616 has thus been down-converted to the AM intermediate signal 1506. The AM intermediate signal 1506 can be generated at any frequency below the frequency of the AM carrier signal 616 by adjusting the aliasing rate.

FIG. 15D depicts the AM intermediate signal 1506 as a filtered output signal 1508. In an alternative embodiment, the invention outputs a stair step, non-filtered or partially filtered output signal. The choice between filtered,

partially filtered and non-filtered output signals is generally a design choice that depends upon the application of the invention.

The intermediate frequency of the down-converted signal F_{IF} , which in this example is the AM intermediate signal 1506, can be determined from EQ. (2), which is reproduced below for convenience.

$$F_C = n \bullet F_{AR} \pm F_{IF} \qquad \text{EQ. (2)}$$

A suitable aliasing rate F_{AR} can be determined in a variety of ways. An example method for determining the aliasing rate F_{AR}, is provided below. After reading the description herein, one skilled in the relevant art(s) will understand how to determine appropriate aliasing rates for EM signals , including ones in addition to the modulated carrier signals specifically illustrated herein.

In FIG. 17, a flowchart 1701 illustrates an example process for determining an aliasing rate F_{AR}. But a designer may choose, or an application may dictate, that the values be determined in an order that is different than the illustrated order. The process begins at step 1702, which includes determining, or selecting, the frequency of the EM signal. The frequency of the FM carrier signal 616 can be, for example, 901 MHZ.

Step 1704 includes determining, or selecting, the intermediate frequency. This is the frequency to which the EM signal will be down-converted. The intermediate frequency can be determined, or selected, to match a frequency requirement of a down-stream demodulator. The intermediate frequency can be, for example, 1 MHZ.

Step 1706 includes determining the aliasing rate or rates that will down-convert the EM signal to the IF specified in step 1704.

EQ. (2) can be rewritten as EQ. (3):

$$n \bullet F_{AR} = F_C \pm F_{IF} \qquad \text{EQ. (3)}$$

Which can be rewritten as EQ. (4):

$$n = \frac{F_C \pm F_{IF}}{F_{AR}} \qquad \text{EQ. (4)}$$

or as EQ. (5):

$$F_{AR} = \frac{F_C \pm F_{IF}}{n} \qquad \text{EQ. (5)}$$

($F_C \pm F_{IF}$) can be defined as a difference value F_{DIFF}, as illustrated in EQ. (6):

$$(F_C \pm F_{IF}) = F_{DIFF} \qquad \text{EQ. (6)}$$

EQ. (4) can be rewritten as EQ. (7):

$$n = \frac{F_{DIFF}}{F_{AR}} \qquad \text{EQ. (7)}$$

From EQ. (7), it can be seen that, for a given n and a constant F_{AR}, F_{DIFF} is constant. For the case of $F_{DIFF} = F_C - F_{IF}$, and for a constant F_{DIFF}, as F_C increases, F_{IF} necessarily increases. For the case of $F_{DIFF} = F_C + F_{IF}$, and for a constant F_{DIFF}, as F_C increases, F_{IF} necessarily decreases. In the latter case of $F_{DIFF} = F_C + F_{IF}$, any phase or frequency changes on F_C correspond to reversed or inverted phase or frequency changes on F_{IF}. This is mentioned to teach the reader that if $F_{DIFF} = F_C + F_{IF}$ is used, the above effect will affect the phase and frequency response of the modulated intermediate signal F_{IF}.

EQs. (2) through (7) can be solved for any valid n. A suitable n can be determined for any given difference frequency F_{DIFF} and for any desired aliasing rate $F_{AR(Desired)}$. EQs. (2) through (7) can be utilized to identify a specific harmonic closest to a desired aliasing rate $F_{AR(Desired)}$ that will generate the desired intermediate signal F_{IF}.

An example is now provided for determining a suitable n for a given difference frequency F_{DIFF} and for a desired aliasing rate $F_{AR(Desired)}$. For ease of illustration, only the case of $(F_C - F_{IF})$ is illustrated in the example below.

$$n = \frac{F_C - F_{IF}}{F_{AR(Desired)}} = \frac{F_{DIFF}}{F_{AR(Desired)}}$$

The desired aliasing rate $F_{AR(Desired)}$ can be, for example, 140 MHZ. Using the previous examples, where the carrier frequency is 901 MHZ and the IF is 1 MHZ, an initial value of n is determined as:

$$n = \frac{901\ \text{MHZ} - 1\ \text{MHZ}}{140\ \text{MHZ}} = \frac{900}{140} = 6.4$$

The initial value 6.4 can be rounded up or down to the valid nearest n, which was defined above as including (0.5, 1, 2, 3, . . .). In this example, 6.4 is rounded down to 6.0, which is inserted into EQ. (5) for the case of $(F_C - F_{IF}) = F_{DIFF}$.:

$$F_{AR} = \frac{F_C - F_{IF}}{n}$$

$$F_{AR} = \frac{901\ \text{MHZ} - 1\ \text{MHZ}}{n} = \frac{900\ \text{MHZ}}{n} = 150\ \text{MHZ}$$

In other words, under-sampling a 901 MHZ EM carrier signal at 150 MHZ generates an intermediate signal at 1 MHZ. When the under-sampled EM carrier signal is a modulated carrier signal, the intermediate signal will also substantially include the modulation. The modulated intermediate signal can be demodulated through any conventional demodulation technique.

Alternatively, instead of starting from a desired aliasing rate, a list of suitable aliasing rates can be determined from the modified form of EQ. (5), by solving for various values of n. Example solutions are listed below.

$$F_{AR} = \frac{\left(F_C - F_{IF}\right)}{n} = \frac{F_{DIFF}}{n} = \frac{901\ \text{MHZ} - 1\ \text{MHZ}}{n} = \frac{900\ \text{MHZ}}{n}$$

Solving for n = 0.5, 1, 2, 3, 4, 5 and 6:

900 MHZ/0.5 = 1.8 GHZ (i.e., second harmonic, illustrated in FIG. 25A as 2502);

900 MHZ/1 = 900 MHZ (i.e., fundamental frequency, illustrated in FIG. 25B as 2504);

900 MHZ/2 = 450 MHZ (i.e., second sub-harmonic, illustrated in FIG. 25C as 2506);

900 MHZ/3 = 300 MHZ (i.e., third sub-harmonic, illustrated in FIG. 25D as 2508);

900 MHZ/4 = 225 MHZ (i.e., fourth sub-harmonic, illustrated in FIG. 25E as 2510);

900 MHZ/5 = 180 MHZ(i.e., fifth sub-harmonic, illustrated in FIG. 25F as 2512); and

900 MHZ/6 = 150 MHZ(i.e., sixth sub-harmonic, illustrated in FIG. 25G as 2514).

The steps described above can be performed for the case of (F_C+F_{IF}) in a similar fashion. The results can be compared to the results obtained from the case of (F_C-F_{IF}) to determine which provides better result for an application.

In an embodiment, the invention down-converts an EM signal to a relatively standard IF in the range of, for example, 100KHZ to 200 MHZ. In another embodiment, referred to herein as a small off-set implementation, the invention down-converts an EM signal to a relatively low frequency of, for example, less than 100 KHZ. In another embodiment, referred to herein as a large off-set implementation, the invention down-converts an EM signal to a relatively higher IF signal, such as, for example, above 200 MHZ.

The various off-set implementations provide selectivity for different applications. Generally, lower data rate applications can operate at lower intermediate frequencies. But higher intermediate frequencies can allow more information to be supported for a given modulation technique.

In accordance with the invention, a designer picks an optimum information bandwidth for an application and an optimum intermediate frequency to support the baseband signal. The intermediate frequency should be high enough to support the bandwidth of the modulating baseband signal F_{MB}.

Generally, as the aliasing rate approaches a harmonic or sub-harmonic frequency of the EM signal, the frequency of the down-converted IF signal decreases. Similarly, as the aliasing rate moves away from a harmonic or sub-harmonic frequency of the EM signal, the IF increases.

Aliased frequencies occur above and below every harmonic of the aliasing frequency. In order to avoid mapping other aliasing frequencies in the band of the aliasing frequency (IF) of interest, the IF of interest is preferably not near one half the aliasing rate.

As described in example implementations below, an aliasing module, including a universal frequency translator (UFT) module built in accordance

with the invention, provides a wide range of flexibility in frequency selection and can thus be implemented in a wide range of applications. Conventional systems cannot easily offer, or do not allow, this level of flexibility in frequency selection.

1.1.2 Structural Description

FIG. 16 illustrates a block diagram of an under-sampling system 1602 according to an embodiment of the invention. The under-sampling system 1602 is an example embodiment of the generic aliasing system 1302 in FIG. 13. The under-sampling system 1602 includes an under-sampling module 1606. The under-sampling module 1606 receives the EM signal 1304 and an under-sampling signal 1604, which includes under-sampling pulses having negligible apertures that tend towards zero time, occurring at a frequency equal to the aliasing rate F_{AR}. The under-sampling signal 1604 is an example embodiment of the aliasing signal 1310. The under-sampling module 1606 under-samples the EM signal 1304 at the aliasing rate F_{AR} of the under-sampling signal 1604. The under-sampling system 1602 outputs a down-converted signal 1308A.

Preferably, the under-sampling module 1606 under-samples the EM signal 1304 to down-convert it to the intermediate signal F_{IF} in the manner shown in the operational flowchart 1407 of FIG. 14B. But it should be understood that the scope and spirit of the invention includes other structural embodiments for performing the steps of the flowchart 1407. The specifics of the other structural embodiments will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein. In an embodiment, the aliasing rate F_{AR} of the under-sampling signal 1604 is chosen in the manner discussed in Section II.1.1.1 so that the under-sampling module 1606 under-samples the EM carrier signal 1304 generating the intermediate frequency F_{IF}.

The operation of the under-sampling system 1602 is now described with reference to the flowchart 1407 and to the timing diagrams in FIGS. 15A-D. In step 1408, the under-sampling module 1606 receives the AM signal 616 (FIG. 15A). In step 1410, the under-sampling module 1606 receives the under-sampling signal 1502 (FIG. 15B). In step 1412, the under-sampling module 1606 under-samples the AM carrier signal 616 at the aliasing rate of the under-sampling signal 1502, or a multiple thereof, to down-convert the AM carrier signal 616 to the intermediate signal 1506 (FIG. 15D).

Example implementations of the under-sampling module 1606 are provided in Sections 4 and 5 below.

1.2 Example Embodiments

Various embodiments related to the method(s) and structure(s) described above are presented in this section (and its subsections). These embodiments are described herein for purposes of illustration, and not limitation. The invention is not limited to these embodiments. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

The method for down-converting the EM signal 1304 to the intermediate signal F_{IF}, illustrated in the flowchart 1407 of FIG. 14B, can be implemented with any type of EM signal, including unmodulated EM carrier signals and modulated carrier signals including, but not limited to, AM, FM, PM, etc., or any combination thereof. Operation of the flowchart 1407 of FIG. 14B is described below for AM, FM and PM carrier signals. The exemplary descriptions below are intended to facilitate an understanding of the present invention. The present invention is not limited to or by the exemplary embodiments below.

1.2.1 First Example Embodiment: Amplitude Modulation

1.2.1.1 Operational Description

Operation of the exemplary process of the flowchart 1407 in FIG. 14B is described below for the analog AM carrier signal 516, illustrated in FIG. 5C, and for the digital AM carrier signal 616, illustrated in FIG. 6C.

1.2.1.1.1 Analog AM Carrier Signal

A process for down-converting the analog AM carrier signal 516 in FIG. 5C to an analog AM intermediate signal is now described with reference to the flowchart 1407 in FIG. 14B. The analog AM carrier signal 516 is re-illustrated in FIG. 19A for convenience. For this example, the analog AM carrier signal 516 oscillates at approximately 901 MHZ. In FIG. 19B, an analog AM carrier signal 1904 illustrates a portion of the analog AM carrier signal 516 on an expanded time scale.

The process begins at step 1408, which includes receiving the EM signal. This is represented by the analog AM carrier signal 516 in FIG. 19A.

Step 1410 includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. 19C illustrates an example under-sampling signal 1906 on approximately the same time scale as FIG. 19B. The under-sampling signal 1906 includes a train of pulses 1907 having negligible apertures that tend towards zero time in duration. The pulses 1907 repeat at the aliasing rate, or pulse repetition rate, which is determined or selected as previously described. Generally, when down-converting to an intermediate signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency F_{DIFF}. For this example, the aliasing rate is approximately 450 MHZ.

Step 1412 includes under-sampling the EM signal at the aliasing rate to down-convert the EM signal to the intermediate signal F_{IF}. Step 1412 is illustrated in FIG. 19B by under-sample points 1905.

Because a harmonic of the aliasing rate is off-set from the AM carrier signal 516, the under-sample points 1905 "walk through" the analog AM carrier signal 516. In this example, the under-sample points 1905 "walk through" the analog AM carrier signal 516 at approximately a one megahertz rate. In other words, the under-sample points 1905 occur at different locations on subsequent cycles of the AM carrier signal 516. As a result, the under-sample points 1905 capture varying amplitudes of the analog AM signal 516. For example, under-sample point1905A has a larger amplitude than under-sample point 1905B.

In FIG. 19D, the under-sample points 1905 correlate to voltage points 1908. In an embodiment, the voltage points 1908 form an analog AM intermediate signal 1910. This can be accomplished in many ways. For example, each voltage point 1908 can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as discussed below.

In FIG. 19E, an AM intermediate signal 1912 represents the AM intermediate signal 1910, after filtering, on a compressed time scale. Although FIG. 19E illustrates the AM intermediate signal 1912 as a filtered output signal, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications.

The AM intermediate signal 1912 is substantially similar to the AM carrier signal 516, except that the AM intermediate signal 1912 is at the 1 MHZ intermediate frequency. The AM intermediate signal 1912 can be demodulated through any conventional AM demodulation technique.

The drawings referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the AM intermediate signal 1910 in FIG. 19D and the AM intermediate signal 1912 in FIG. 19E illustrate that the AM carrier signal 516 was successfully down-converted to an intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.1.1.2 Digital AM Carrier Signal

A process for down-converting the digital AM carrier signal 616 in FIG. 6C to a digital AM intermediate signal is now described with reference to the flowchart 1407 in FIG. 14B. The digital AM carrier signal 616 is re-illustrated in FIG. 18A for convenience. For this example, the digital AM carrier signal 616 oscillates at approximately 901 MHZ. In FIG. 18B, an AM carrier signal 1804 illustrates a portion of the AM signal 616, from time t0 to t1, on an expanded time scale.

The process begins at step 1408, which includes receiving an EM signal. This is represented by the AM signal 616 in FIG. 18A.

Step 1410 includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. 18C illustrates an example under-sampling signal 1806 on approximately the same time scale as FIG. 18B. The under-sampling signal 1806 includes a train of pulses 1807 having negligible apertures that tend towards zero time in duration. The pulses 1807 repeat at the aliasing rate, or pulse repetition rate, which is determined or selected as previously described. Generally, when down- converting to an intermediate signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency F_{DIFF}. For this example, the aliasing rate is approximately 450 MHZ.

Step 1412 includes under-sampling the EM signal at the aliasing rate to down-convert the EM signal to the intermediate signal F_{IF}. Step 1412 is illustrated in FIG. 18B by under-sample points 1805.

Because a harmonic of the aliasing rate is off-set from the AM carrier signal 616, the under-sample points 1805 walk through the AM carrier signal 616. In other words, the under-sample points 1805 occur at different locations of subsequent cycles of the AM signal 616. As a result, the under-sample points 1805 capture various amplitudes of the AM signal 616. In this example, the under-sample points 1805 walk through the AM carrier signal 616 at approximately a 1 MHZ rate. For example, under-sample point 1805A has a larger amplitude than under-sample point 1805B.

In FIG. 18D, the under-sample points 1805 correlate to voltage points 1808. In an embodiment, the voltage points 1805 form an AM intermediate signal 1810. This can be accomplished in many ways. For example, each voltage point 1808 can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as discussed below.

In FIG. 18E, an AM intermediate signal 1812 represents the AM intermediate signal 1810, after filtering, on a compressed time scale. Although FIG. 18E illustrates the AM intermediate signal 1812 as a filtered output signal, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications.

The AM intermediate signal 1812 is substantially similar to the AM carrier signal 616, except that the AM intermediate signal 1812 is at the 1 MHZ intermediate frequency. The AM intermediate signal 1812 can be demodulated through any conventional AM demodulation technique.

The drawings referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the AM intermediate signal

1810 in FIG. 18D and the AM intermediate signal 1812 in FIG. 18E illustrate that the AM carrier signal 616 was successfully down-converted to an intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.1.2 Structural Description

The operation of the under-sampling system 1602 is now described for the analog AM carrier signal 516, with reference to the flowchart 1407 and to the timing diagrams of FIGS. 19A-E. In step 1408, the under-sampling module 1606 receives the AM carrier signal 516 (FIG. 19A). In step 1410, the under-sampling module 1606 receives the under-sampling signal 1906 (FIG. 19C). In step 1412, the under-sampling module 1606 under-samples the AM carrier signal 516 at the aliasing rate of the under-sampling signal 1906 to down-convert it to the AM intermediate signal 1912 (FIG. 19E).

The operation of the under-sampling system 1602 is now described for the digital AM carrier signal 616, with reference to the flowchart 1407 and to the timing diagrams of FIGS. 18A-E. In step 1408, the under-sampling module 1606 receives the AM carrier signal 616 (FIG. 18A). In step 1410, the under-sampling module 1606 receives the under-sampling signal 1806 (FIG. 18C). In step 1412, the under-sampling module 1606 under-samples the AM carrier signal 616 at the aliasing rate of the under-sampling signal 1806 to down-convert it to the AM intermediate signal 1812 (FIG. 18E).

Example implementations of the under-sampling module 1606 are provided in Sections 4 and 5 below.

1.2.2 Second Example Embodiment: Frequency Modulation

1.2.2.1 Operational Description

Operation of the exemplary process of the flowchart 1407 in FIG. 14B is described below for the analog FM carrier signal 716, illustrated in FIG. 7C, and for the digital FM carrier signal 816, illustrated in FIG. 8C.

1.2.2.1.1 Analog FM Carrier Signal

A process for down-converting the analog FM carrier signal 716 to an analog FM intermediate signal is now described with reference to the flowchart 1407 in FIG. 14B. The analog FM carrier signal 716 is re-illustrated in FIG. 20A for convenience. For this example, the analog FM carrier signal 716 oscillates at approximately 901 MHZ. In FIG. 20B, an FM carrier signal 2004 illustrates a portion of the analog FM carrier signal 716, from time t1 to t3, on an expanded time scale.

The process begins at step 1408, which includes receiving an EM signal. This is represented in FIG. 20A by the FM carrier signal 716.

Step 1410 includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. 20C illustrates an example under-sampling signal 2006 on approximately the same time scale as FIG. 20B. The under-sampling signal 2006 includes a train of pulses 2007 having negligible apertures that tend towards zero time in duration. The pulses 2007 repeat at the aliasing rate or pulse repetition rate, which is determined or selected as previously described. Generally, when down-converting to an intermediate signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency F_{DIFF}. For this example, where the FM carrier signal 716 is centered around 901 MHZ, the aliasing rate is approximately 450 MHZ.

Step 1412 includes under-sampling the EM signal at the aliasing rate to down-convert the EM signal to the intermediate signal F_{IF}. Step 1412 is illustrated in FIG. 20B by under-sample points 2005.

Because a harmonic of the aliasing rate is off-set from the FM carrier signal 716, the under-sample points 2005 occur at different locations of subsequent cycles of the under-sampled signal 716. In other words, the under-sample points 2005 walk through the signal 716. As a result, the under-sample points 2005 capture various amplitudes of the FM carrier signal 716.

In FIG. 20D, the under-sample points 2005 correlate to voltage points 2008. In an embodiment, the voltage points 2005 form an analog FM intermediate signal 2010. This can be accomplished in many ways. For example, each voltage point 2008 can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as discussed below.

In FIG. 20E, an FM intermediate signal 2012 illustrates the FM intermediate signal 2010, after filtering, on a compressed time scale. Although FIG. 20E illustrates the FM intermediate signal 2012 as a filtered output signal, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications.

The FM intermediate signal 2012 is substantially similar to the FM carrier signal 716, except that the FM intermediate signal 2012 is at the 1 MHZ intermediate frequency. The FM intermediate signal 2012 can be demodulated through any conventional FM demodulation technique.

The drawings referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the FM intermediate signal 2010 in FIG. 20D and the FM intermediate signal 2012 in FIG. 20E illustrate that the FM carrier signal 716 was successfully down-converted to an

intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.2.1.2 Digital FM Carrier Signal

A process for down-converting the digital FM carrier signal 816 to a digital FM intermediate signal is now described with reference to the flowchart 1407 in FIG. 14B. The digital FM carrier signal 816 is re-illustrated in FIG. 21A for convenience. For this example, the digital FM carrier signal 816 oscillates at approximately 901 MHZ. In FIG. 21B, an FM carrier signal 2104 illustrates a portion of the FM carrier signal 816, from time t1 to t3, on an expanded time scale.

The process begins at step 1408, which includes receiving an EM signal. This is represented in FIG. 21A, by the FM carrier signal 816.

Step 1410 includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. 21C illustrates an example under-sampling signal 2106 on approximately the same time scale as FIG. 21B. The under-sampling signal 2106 includes a train of pulses 2107 having negligible apertures that tend toward zero time in duration. The pulses 2107 repeat at the aliasing rate, or pulse repetition rate, which is determined or selected as previously described. Generally, when down-converting to an intermediate signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency F_{DIFF}. In this example, where the FM carrier signal 816 is centered around 901 MHZ, the aliasing rate is selected as approximately 450 MHZ, which is a sub-harmonic of 900 MHZ, which is off-set by 1 MHZ from the center frequency of the FM carrier signal 816.

Step 1412 includes under-sampling the EM signal at the aliasing rate to down-convert the EM signal to an intermediate signal F_{IF}. Step 1412 is illustrated in FIG. 21B by under-sample points 2105.

Because a harmonic of the aliasing rate is off-set from the FM carrier signal 816, the under-sample points 2105 occur at different locations of subsequent cycles of the FM carrier signal 816. In other words, the under-sample points 2105 walk through the signal 816. As a result, the under-sample points 2105 capture various amplitudes of the signal 816.

In FIG. 21D, the under-sample points 2105 correlate to voltage points 2108. In an embodiment, the voltage points 2108 form a digital FM intermediate signal 2110. This can be accomplished in many ways. For example, each voltage point 2108 can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as described below.

In FIG. 21E, an FM intermediate signal 2112 represents the FM intermediate signal 2110, after filtering, on a compressed time scale. Although FIG. 21E illustrates the FM intermediate signal 2112 as a filtered output signal, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications.

The FM intermediate signal 2112 is substantially similar to the FM carrier signal 816, except that the FM intermediate signal 2112 is at the 1 MHZ intermediate frequency. The FM intermediate signal 2112 can be demodulated through any conventional FM demodulation technique.

The drawings referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the FM intermediate signal 2110 in FIG. 21D and the FM intermediate signal 2112 in FIG. 21E illustrate that the FM carrier signal 816 was successfully down-converted to an intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.2.2 Structural Description

The operation of the under-sampling system 1602 is now described for the analog FM carrier signal 716, with reference to the flowchart 1407 and the timing diagrams of FIGS. 20A-E. In step 1408, the under-sampling module 1606 receives the FM carrier signal 716 (FIG. 20A). In step 1410, the under-sampling module 1606 receives the under-sampling signal 2006 (FIG. 20C). In step 1412, the under-sampling module 1606 under-samples the FM carrier signal 716 at the aliasing rate of the under-sampling signal 2006 to down-convert the FM carrier signal 716 to the FM intermediate signal 2012 (FIG. 20E).

The operation of the under-sampling system 1602 is now described for the digital FM carrier signal 816, with reference to the flowchart 1407 and the timing diagrams of FIGS. 21A-E. In step 1408, the under-sampling module 1606 receives the FM carrier signal 816 (FIG. 21A). In step 1410, the under-sampling module 1606 receives the under-sampling signal 2106 (FIG. 21C). In step 1412, the under-sampling module 1606 under-samples the FM carrier signal 816 at the aliasing rate of the under-sampling signal 2106 to down-convert the FM carrier signal 816 to the FM intermediate signal 2112 (FIG. 21E).

Example implementations of the under-sampling module 1606 are provided in Sections 4 and 5 below.

1.2.3 Third Example Embodiment: Phase Modulation

1.2.3.1 Operational Description

Operation of the exemplary process of the flowchart 1407 in FIG. 14B is described below for the analog PM carrier signal 916, illustrated in FIG. 9C, and for the digital PM carrier signal 1016, illustrated in FIG. 10C.

1.2.3.1.1 Analog PM Carrier Signal

A process for down-converting the analog PM carrier signal 916 to an analog PM intermediate signal is now described with reference to the flowchart 1407 in FIG. 14B. The analog PM carrier signal 916 is re-illustrated in FIG. 23A for convenience. For this example, the analog PM carrier signal 916 oscillates at approximately 901 MHZ. In FIG. 23B, a PM carrier signal 2304 illustrates a portion of the analog PM carrier signal 916, from time t1 to t3, on an expanded time scale.

The process of down-converting the PM carrier signal 916 to a PM intermediate signal begins at step 1408, which includes receiving an EM signal. This is represented in FIG. 23A, by the analog PM carrier signal 916.

Step 1410 includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. 23C illustrates an example under-sampling signal 2306 on approximately the same time scale as FIG. 23B. The under-sampling signal 2306 includes a train of pulses 2307 having negligible apertures that tend towards zero time in duration. The pulses 2307 repeat at the aliasing rate, or pulse repetition rate, which is determined or selected as previously described. Generally, when down-converting to an intermediate signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency F_{DIFF}. In this example, the aliasing rate is approximately 450 MHZ.

Step 1412 includes under-sampling the EM signal at the aliasing rate to down-convert the EM signal to the intermediate signal F_{IF}. Step 1412 is illustrated in FIG. 23B by under-sample points 2305.

Because a harmonic of the aliasing rate is off-set from the PM carrier signal 916, the under-sample points 2305 occur at different locations of subsequent cycles of the PM carrier signal 916. As a result, the under-sample points capture various amplitudes of the PM carrier signal 916.

In FIG. 23D, voltage points 2308 correlate to the under-sample points 2305. In an embodiment, the voltage points 2308 form an analog PM intermediate signal 2310. This can be accomplished in many ways. For example, each voltage point 2308 can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as described below.

In FIG. 23E, an analog PM intermediate signal 2312 illustrates the analog PM intermediate signal 2310, after filtering, on a compressed time scale. Although FIG. 23E illustrates the PM intermediate signal 2312 as a filtered output signal, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications.

The analog PM intermediate signal 2312 is substantially similar to the analog PM carrier signal 916, except that the analog PM intermediate signal 2312 is at the 1 MHZ intermediate frequency. The analog PM intermediate signal 2312 can be demodulated through any conventional PM demodulation technique.

The drawings referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the analog PM intermediate signal 2310 in FIG. 23D and the analog PM intermediate signal 2312 in FIG. 23E illustrate that the analog PM carrier signal 2316 was successfully down-converted to an intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.3.1.2 Digital PM Carrier Signal

A process for down-converting the digital PM carrier signal 1016 to a digital PM intermediate signal is now described with reference to the flowchart 1407 in FIG. 14B. The digital PM carrier signal 1016 is re-illustrated in FIG. 22A for convenience. For this example, the digital PM

carrier signal 1016 oscillates at approximately 901 MHZ. In FIG. 22B, a PM carrier signal 2204 illustrates a portion of the digital PM carrier signal 1016, from time t1 to t3, on an expanded time scale.

The process begins at step 1408, which includes receiving an EM signal. This is represented in FIG. 22A by the digital PM carrier signal 1016.

Step 1408 includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. 22C illustrates example under-sampling signal 2206 on approximately the same time scale as FIG. 22B. The under-sampling signal 2206 includes a train of pulses 2207 having negligible apertures that tend towards zero time in duration. The pulses 2207 repeat at the aliasing rate, or a pulse repetition rate, which is determined or selected as previously described. Generally, when down-converting to an intermediate signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency F_{DIFF}. In this example, the aliasing rate is approximately 450 MHZ.

Step 1412 includes under-sampling the EM signal at the aliasing rate to down-convert the EM signal to an intermediate signal F_{IF}. Step 1412 is illustrated in FIG. 22B by under-sample points 2205.

Because a harmonic of the aliasing rate is off-set from the PM carrier signal 1016, the under-sample points 2205 occur at different locations of subsequent cycles of the PM carrier signal 1016.

In FIG. 22D, voltage points 2208 correlate to the under-sample points 2205. In an embodiment, the voltage points 2208 form a digital analog PM intermediate signal 2210. This can be accomplished in many ways. For example, each voltage point 2208 can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as described below.

In FIG. 22E, a digital PM intermediate signal 2212 represents the digital PM intermediate signal 2210 on a compressed time scale. Although

FIG. 22E illustrates the PM intermediate signal 2212 as a filtered output signal, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications.

The digital PM intermediate signal 2212 is substantially similar to the digital PM carrier signal 1016, except that the digital PM intermediate signal 2212 is at the 1 MHZ intermediate frequency. The digital PM carrier signal 2212 can be demodulated through any conventional PM demodulation technique.

The drawings referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the digital PM intermediate signal 2210 in FIG. 22D and the digital PM intermediate signal 2212 in FIG. 22E illustrate that the digital PM carrier signal 1016 was successfully down-converted to an intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.3.2 Structural Description

The operation of the under-sampling system 1602 is now described for the analog PM carrier signal 916, with reference to the flowchart 1407 and the timing diagrams of FIGS. 23A-E. In step 1408, the under-sampling module 1606 receives the PM carrier signal 916 (FIG. 23A). In step 1410, the under-sampling module 1606 receives the under-sampling signal 2306 (FIG. 23C). In step 1412, the under-sampling module 1606 under-samples the PM carrier signal 916 at the aliasing rate of the under-sampling signal 2306 to down-convert the PM carrier signal 916 to the PM intermediate signal 2312 (FIG. 23E).

The operation of the under-sampling system 1602 is now described for the digital PM carrier signal 1016, with reference to the flowchart 1407 and the timing diagrams of FIGS. 22A-E. In step 1408, the under-sampling

module 1606 receives the PM carrier signal 1016 (FIG. 22A). In step 1410, the under-sampling module 1606 receives the under-sampling signal 2206 (FIG. 22C). In step 1412, the under-sampling module 1606 under-samples the PM carrier signal 1016 at the aliasing rate of the under-sampling signal 2206 to down-convert the PM carrier signal 1016 to the PM intermediate signal 2212 (FIG. 22E).

Example implementations of the under-sampling module 1606 are provided in Sections 4 and 5 below.

1.2.4 Other Embodiments

The embodiments described above are provided for purposes of illustration. These embodiments are not intended to limit the invention. Alternate embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate embodiments fall within the scope and spirit of the present invention. Example implementations of the under-sampling module 1606 are provided in Sections 4 and 5 below.

1.3 Implementation Examples

Exemplary operational and/or structural implementations related to the method(s), structure(s), and/or embodiments described above are presented in Sections 4 and 5 below. The implementations are presented for purposes of illustration, and not limitation. The invention is not limited to the particular implementation examples described therein. Alternate implementations (including equivalents, extensions, variations, deviations, etc., of those described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

2. *Directly Down-Converting an EM Signal to a Baseband Signal (Direct-to-Data)*

In an embodiment, the invention directly down-converts an EM signal to a baseband signal, by under-sampling the EM signal. This embodiment is referred to herein as direct-to-data down-conversion and is illustrated in FIG. 45B as 4510.

This embodiment can be implemented with modulated and unmodulated EM signals. This embodiment is described herein using the modulated carrier signal F_{MC} in FIG. 1, as an example. In the example, the modulated carrier signal F_{MC} is directly down-converted to the demodulated baseband signal F_{DMB}. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention is applicable to down-convert any EM signal, including but not limited to, modulated carrier signals and unmodulated carrier signals.

The following sections describe example methods for directly down-converting the modulated carrier signal F_{MC} to the demodulated baseband signal F_{DMB}. Exemplary structural embodiments for implementing the methods are also described. It should be understood that the invention is not limited to the particular embodiments described below. Equivalents, extensions, variations, deviations, etc., of the following will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such equivalents, extensions, variations, deviations, etc., are within the scope and spirit of the present invention.

The following sections include a high level discussion, example embodiments, and implementation examples.

2.1 High Level Description

This section (including its subsections) provides a high-level description of directly down-converting the modulated carrier signal F_{MC} to the demodulated baseband signal F_{DMB}, according to the invention. In particular, an operational process of directly down-converting the modulated carrier signal F_{MC} to the demodulated baseband signal F_{DMB} is described at a high-level. Also, a structural implementation for implementing this process is described at a high-level. The structural implementation is described herein for illustrative purposes, and is not limiting. In particular, the process described in this section can be achieved using any number of structural implementations, one of which is described in this section. The details of such structural implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

2.1.1 Operational Description

FIG. 14C depicts a flowchart 1413 that illustrates an exemplary method for directly down-converting an EM signal to a demodulated baseband signal F_{DMB}. The exemplary method illustrated in the flowchart 1413 is an embodiment of the flowchart 1401 in FIG. 14A.

Any and all combinations of modulation techniques are valid for this invention. For ease of discussion, the digital AM carrier signal 616 is used to illustrate a high level operational description of the invention. Subsequent sections provide detailed descriptions for AM and PM example embodiments. FM presents special considerations that are dealt with separately in Section II.3, below. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention can be implemented to down-convert any type of EM signal, including any form of modulated carrier signal and unmodulated carrier signals.

The method illustrated in the flowchart 1413 is now described at a high level using the digital AM carrier signal 616, from FIG. 6C. The digital AM carrier signal 616 is re-illustrated in FIG. 33A for convenience.

The process of the flowchart 1413 begins at step 1414, which includes receiving an EM signal. Step 1414 is represented by the digital AM carrier signal 616 in FIG. 33A.

Step 1416 includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. 33B illustrates an example under-sampling signal 3302 which includes a train of pulses 3303 having negligible apertures that tend towards zero time in duration. The pulses 3303 repeat at the aliasing rate or pulse repetition rate. The aliasing rate is determined in accordance with EQ. (2), reproduced below for convenience.

$$F_C = n \bullet F_{AR} \pm F_{IF} \qquad \text{EQ. (2)}$$

When directly down-converting an EM signal to baseband (i.e., zero IF), EQ. (2) becomes:

$$F_C = n \bullet F_{AR} \qquad \text{EQ. (8)}$$

Thus, to directly down-convert the AM signal 616 to a demodulated baseband signal, the aliasing rate is substantially equal to the frequency of the AM signal 616 or to a harmonic or sub-harmonic thereof. Although the aliasing rate is too low to permit reconstruction of higher frequency components of the AM signal 616 (i.e., the carrier frequency), it is high enough to permit substantial reconstruction of the lower frequency modulating baseband signal 310.

Step 1418 includes under-sampling the EM signal at the aliasing rate to directly down-convert it to the demodulated baseband signal F_{DMB}. FIG. 33C illustrates a stair step demodulated baseband signal 3304, which is generated

by the direct down-conversion process. The demodulated baseband signal 3304 is similar to the digital modulating baseband signal 310 in FIG. 3.

FIG. 33D depicts a filtered demodulated baseband signal 3306, which can be generated from the stair step demodulated baseband signal 3304. The invention can thus generate a filtered output signal, a partially filtered output signal, or a relatively unfiltered stair step output signal. The choice between filtered, partially filtered and non-filtered output signals is generally a design choice that depends upon the application of the invention.

2.1.2 Structural Description

FIG. 16 illustrates the block diagram of the under-sampling system 1602 according to an embodiment of the invention. The under-sampling system 1602 is an example embodiment of the generic aliasing system 1302 in FIG. 13.

In a direct to data embodiment, the frequency of the under-sampling signal 1604 is substantially equal to a harmonic of the EM signal 1304 or, more typically, a sub-harmonic thereof Preferably, the under-sampling module 1606 under-samples the EM signal 1304 to directly down-convert it to the demodulated baseband signal F_{DMB}, in the manner shown in the operational flowchart 1413. But it should be understood that the scope and spirit of the invention includes other structural embodiments for performing the steps of the flowchart 1413. The specifics of the other structural embodiments will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

The operation of the aliasing system 1602 is now described for the digital AM carrier signal 616, with reference to the flowchart 1413 and to the timing diagrams in FIGS. 33A-D. In step 1414, the under-sampling module 1606 receives the AM carrier signal 616 (FIG. 33A). In step 1416, the under-sampling module 1606 receives the under-sampling signal 3302 (FIG. 33B).

In step 1418, the under-sampling module 1606 under-samples the AM carrier signal 616 at the aliasing rate of the under-sampling signal 3302 to directly down-convert the AM carrier signal 616 to the demodulated baseband signal 3304 in FIG. 33C or the filtered demodulated baseband signal 3306 in FIG. 33D.

Example implementations of the under-sampling module 1606 are provided in Sections 4 and 5 below.

2.2 Example Embodiments

Various embodiments related to the method(s) and structure(s) described above are presented in this section (and its subsections). These embodiments are described herein for purposes of illustration, and not limitation. The invention is not limited to these embodiments. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

The method for down-converting the EM signal 1304 to the demodulated baseband signal F_{DMB}, illustrated in the flowchart 1413 of FIG. 14C, can be implemented with any type EM signal, including modulated carrier signals, including but not limited to, AM, PM, etc., or any combination thereof. Operation of the flowchart 1413 of FIG. 14C is described below for AM and PM carrier signals. The exemplary descriptions below are intended to facilitate an understanding of the present invention. The present invention is not limited to or by the exemplary embodiments below.

2.2.1 First Example Embodiment: Amplitude Modulation

2.2.1.1 Operational Description

Operation of the exemplary process of the flowchart 1413 in FIG. 14C is described below for the analog AM carrier signal 516, illustrated in FIG. 5C and for the digital AM carrier signal 616, illustrated in FIG. 6C.

2.2.1.1.1 Analog AM Carrier Signal

A process for directly down-converting the analog AM carrier signal 516 to a demodulated baseband signal is now described with reference to the flowchart 1413 in FIG. 14C. The analog AM carrier signal 516 is re-illustrated in 35A for convenience. For this example, the analog AM carrier signal 516 oscillates at approximately 900 MHZ. In FIG. 35B, an analog AM carrier signal 3504 illustrates a portion of the analog AM carrier signal 516 on an expanded time scale.

The process begins at step 1414, which includes receiving an EM signal. This is represented by the analog AM carrier signal 516.

Step 1416 includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. 35C illustrates an example under-sampling signal 3506 on approximately the same time scale as FIG. 35B. The under-sampling signal 3506 includes a train of pulses 3507 having negligible apertures that tend towards zero time in duration. The pulses 3507 repeat at the aliasing rate or pulse repetition rate, which is determined or selected as previously described. Generally, when directly down-converting to a demodulated baseband signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the under-sampled signal. In this example, the aliasing rate is approximately 450 MHZ.

Step 1418 includes under-sampling the EM signal at the aliasing rate to directly down-convert it to the demodulated baseband signal F_{DMB}. Step 1418 is illustrated in FIG. 35B by under- sample points 3505. Because a harmonic of the aliasing rate is substantially equal to the frequency of the signal 516, essentially no IF is produced. The only substantial aliased component is the baseband signal.

In FIG. 35D, voltage points 3508 correlate to the under-sample points 3505. In an embodiment, the voltage points 3508 form a demodulated baseband signal 3510. This can be accomplished in many ways. For example, each voltage point 3508 can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as described below.

In FIG. 35E, a demodulated baseband signal 3512 represents the demodulated baseband signal 3510, after filtering, on a compressed time scale. Although FIG. 35E illustrates the demodulated baseband signal 3512 as a filtered output signal, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications.

The demodulated baseband signal 3512 is substantially similar to the modulating baseband signal 210. The demodulated baseband signal 3512 can be processed using any signal processing technique(s) without further down-conversion or demodulation.

The aliasing rate of the under-sampling signal is preferably controlled to optimize the demodulated baseband signal for amplitude output and polarity, as desired.

In the example above, the under-sample points 3505 occur at positive locations of the AM carrier signal 516. Alternatively, the under-sample points 3505 can occur at other locations including negative points of the analog AM carrier signal 516. When the under-sample points 3505 occur at negative

locations of the AM carrier signal 516, the resultant demodulated baseband signal is inverted relative to the modulating baseband signal 210.

The drawings referred to herein illustrate direct to data down-conversion in accordance with the invention. For example, the demodulated baseband signal 3510 in FIG. 35D and the demodulated baseband signal 3512 in FIG. 35E illustrate that the AM carrier signal 516 was successfully down-converted to the demodulated baseband signal 3510 by retaining enough baseband information for sufficient reconstruction.

2.2.1.1.2 Digital AM Carrier Signal

A process for directly down-converting the digital AM carrier signal 616 to a demodulated baseband signal is now described with reference to the flowchart 1413 in FIG. 14C. The digital AM carrier signal 616 is re-illustrated in FIG. 36A for convenience. For this example, the digital AM carrier signal 616 oscillates at approximately 901 MHZ. In FIG. 36B, a digital AM carrier signal 3604 illustrates a portion of the digital AM carrier signal 616 on an expanded time scale.

The process begins at step 1414, which includes receiving an EM signal. This is represented by the digital AM carrier signal 616.

Step 1416 includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. 36C illustrates an example under-sampling signal 3606 on approximately the same time scale as FIG. 36B. The under-sampling signal 3606 includes a train of pulses 3607 having negligible apertures that tend towards zero time in duration. The pulses 3607 repeat at the aliasing rate or pulse repetition rate, which is determined or selected as previously described. Generally, when directly down-converting to a demodulated baseband signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the under-sampled signal. In this example, the aliasing rate is approximately 450 MHZ. .

Step 1418 includes under-sampling the EM signal at the aliasing rate to directly down-convert it to the demodulated baseband signal F_{DMB}. Step 1418 is illustrated in FIG. 36B by under- sample points 3605. Because the aliasing rate is substantially equal to the AM carrier signal 616, or to a harmonic or sub-harmonic thereof, essentially no IF is produced. The only substantial aliased component is the baseband signal.

In FIG. 36D, voltage points 3608 correlate to the under-sample points 3605. In an embodiment, the voltage points 3608 form a demodulated baseband signal 3610. This can be accomplished in many ways. For example, each voltage point 3608 can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as described below.

In FIG. 36E, a demodulated baseband signal 3612 represents the demodulated baseband signal 3610, after filtering, on a compressed time scale. Although FIG. 36E illustrates the demodulated baseband signal 3612 as a filtered output signal, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications.

The demodulated baseband signal 3612 is substantially similar to the digital modulating baseband signal 310. The demodulated analog baseband signal 3612 can be processed using any signal processing technique(s) without further down-conversion or demodulation.

The aliasing rate of the under-sampling signal is preferably controlled to optimize the demodulated baseband signal for amplitude output and polarity, as desired.

In the example above, the under-sample points 3605 occur at positive locations of signal portion 3604. Alternatively, the under-sample points 3605 can occur at other locations including negative locations of the signal portion 3604. When the under-sample points 3605 occur at negative points, the

resultant demodulated baseband signal is inverted with respect to the modulating baseband signal 310.

The drawings referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the demodulated baseband signal 3610 in FIG. 36D and the demodulated baseband signal 3612 in FIG. 36E illustrate that the digital AM carrier signal 616 was successfully down-converted to the demodulated baseband signal 3610 by retaining enough baseband information for sufficient reconstruction.

2.2.1.2 Structural Description

The operation of the under-sampling module 1606 is now described for the analog AM carrier signal 516, with reference to the flowchart 1413 and the timing diagrams of FIGS. 35A-E. In step 1414, the under-sampling module 1606 receives the analog AM carrier signal 516 (FIG. 35A). In step 1416, the under-sampling module 1606 receives the under-sampling signal 3506 (FIG. 35C). In step 1418, the under-sampling module 1606 under-samples the analog AM carrier signal 516 at the aliasing rate of the under-sampling signal 3506 to directly to down-convert the AM carrier signal 516 to the demodulated analog baseband signal 3510 in FIG. 35D or to the filtered demodulated analog baseband signal 3512 in FIG. 35E.

The operation of the under-sampling system 1602 is now described for the digital AM carrier signal 616, with reference to the flowchart 1413 and the timing diagrams of FIGS. 36A-E. In step 1414, the under-sampling module 1606 receives the digital AM carrier signal 616 (FIG. 36A). In step 1416, the under-sampling module 1606 receives the under-sampling signal 3606 (FIG. 36C). In step 1418, the under-sampling module 1606 under-samples the digital AM carrier signal 616 at the aliasing rate of the under-sampling signal 3606 to down-convert the digital AM carrier signal 616 to the demodulated

digital baseband signal 3610 in FIG. 36D or to the filtered demodulated digital baseband signal 3612 in FIG. 36E.

Example implementations of the under-sampling module 1606 are provided in Sections 4 and 5 below.

2.2.2 Second Example Embodiment: Phase Modulation

2.2.2.1 Operational Description

Operation of the exemplary process of the flowchart 1413 in FIG. 14C is described below for the analog PM carrier signal 916, illustrated in FIG. 9C, and for the digital PM carrier signal 1016, illustrated in FIG. 10C.

2.2.2.1.1 Analog PM Carrier Signal

A process for directly down-converting the analog PM carrier signal 916 to a demodulated baseband signal is now described with reference to the flowchart 1413 in FIG. 14C. The analog PM carrier signal 916 is re-illustrated in 37A for convenience. For this example, the analog PM carrier signal 916 oscillates at approximately 900 MHZ. In FIG. 37B, an analog PM carrier signal 3704 illustrates a portion of the analog PM carrier signal 916 on an expanded time scale.

The process begins at step 1414, which includes receiving an EM signal. This is represented by the analog PM signal 916.

Step 1416 includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. 37C illustrates an example under-sampling signal 3706 on approximately the same time scale as FIG. 37B. The under-sampling signal 3706 includes a train of pulses 3707 having negligible apertures that tend towards zero time in duration. The pulses 3707 repeat at the aliasing rate or pulse repetition rate, which is determined or selected as previously described.

Generally, when directly down-converting to a demodulated baseband signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the under-sampled signal. In this example, the aliasing rate is approximately 450 MHZ.

Step 1418 includes under-sampling the analog PM carrier signal 916 at the aliasing rate to directly down-convert it to a demodulated baseband signal. Step 1418 is illustrated in FIG. 37B by under-sample points 3705.

Because a harmonic of the aliasing rate is substantially equal to the frequency of the signal 916, or substantially equal to a harmonic or sub-harmonic thereof, essentially no IF is produced. The only substantial aliased component is the baseband signal.

In FIG. 37D, voltage points 3708 correlate to the under-sample points 3705. In an embodiment, the voltage points 3708 form a demodulated baseband signal 3710. This can be accomplished in many ways. For example, each voltage point 3708 can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as described below.

In FIG. 37E, a demodulated baseband signal 3712 represents the demodulated baseband signal 3710, after filtering, on a compressed time scale. Although FIG. 37E illustrates the demodulated baseband signal 3712 as a filtered output signal, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications.

The demodulated baseband signal 3712 is substantially similar to the analog modulating baseband signal 210. The demodulated baseband signal 3712 can be processed without further down-conversion or demodulation.

The aliasing rate of the under-sampling signal is preferably controlled to optimize the demodulated baseband signal for amplitude output and polarity, as desired.

In the example above, the under-sample points 3705 occur at positive locations of the analog PM carrier signal 916. Alternatively, the under-sample points 3705 can occur at other locations include negative points of the analog PM carrier signal 916. When the under-sample points 3705 occur at negative locations of the analog PM carrier signal 916, the resultant demodulated baseband signal is inverted relative to the modulating baseband signal 210.

The drawings referred to herein illustrate direct to data down-conversion in accordance with the invention. For example, the demodulated baseband signal 3710 in FIG. 37D and the demodulated baseband signal 3712 in FIG. 37E illustrate that the analog PM carrier signal 916 was successfully down-converted to the demodulated baseband signal 3710 by retaining enough baseband information for sufficient reconstruction.

2.2.2.1.2 Digital PM Carrier Signal

A process for directly down-converting the digital PM carrier signal 1016 to a demodulated baseband signal is now described with reference to the flowchart 1413 in FIG. 14C. The digital PM carrier signal 1016 is re-illustrated in 38A for convenience. For this example, the digital PM carrier signal 1016 oscillates at approximately 900 MHZ. In FIG. 38B, a digital PM carrier signal 3804 illustrates a portion of the digital PM carrier signal 1016 on an expanded time scale.

The process begins at step 1414, which includes receiving an EM signal. This is represented by the digital PM signal 1016.

Step 1416 includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. 38C illustrates an example under-sampling signal 3806 on approximately the same time scale as FIG. 38B. The under-sampling signal 3806 includes a train of pulses 3807 having negligible apertures that tend towards zero time in duration. The pulses 3807 repeat at the aliasing rate or pulse repetition rate, which is determined or selected as described above.

Generally, when directly down-converting to a demodulated baseband signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the under-sampled signal. In this example, the aliasing rate is approximately 450 MHZ.

Step 1418 includes under-sampling the digital PM carrier signal 1016 at the aliasing rate to directly down-convert it to a demodulated baseband signal. This is illustrated in FIG. 38B by under-sample points 3705.

Because a harmonic of the aliasing rate is substantially equal to the frequency of the signal 1016, essentially no IF is produced. The only substantial aliased component is the baseband signal.

In FIG. 38D, voltage points 3808 correlate to the under-sample points 3805. In an embodiment, the voltage points 3808 form a demodulated baseband signal 3810. This can be accomplished in many ways. For example, each voltage point 3808 can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as described below.

In FIG. 38E, a demodulated baseband signal 3812 represents the demodulated baseband signal 3810, after filtering, on a compressed time scale. Although FIG. 38E illustrates the demodulated baseband signal 3812 as a filtered output signal, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications.

The demodulated baseband signal 3812 is substantially similar to the digital modulating baseband signal 310. The demodulated baseband signal 3812 can be processed without further down-conversion or demodulation.

The aliasing rate of the under-sampling signal is preferably controlled to optimize the demodulated baseband signal for amplitude output and polarity, as desired.

In the example above, the under-sample points 3805 occur at positive locations of the digital PM carrier signal 1016. Alternatively, the under-sample points 3805 can occur at other locations include negative points of the digital PM carrier signal 1016. When the under-sample points 3805 occur at negative locations of the digital PM carrier signal 1016, the resultant demodulated baseband signal is inverted relative to the modulating baseband signal 310.

The drawings referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the demodulated baseband signal 3810 in FIG. 38D and the demodulated baseband signal 3812 in FIG. 38E illustrate that the digital PM carrier signal 1016 was successfully down-converted to the demodulated baseband signal 3810 by retaining enough baseband information for sufficient reconstruction.

2.2.2.2 Structural Description

The operation of the under-sampling system 1602 is now described for the analog PM carrier signal 916, with reference to the flowchart 1413 and the timing diagrams of FIGS. 37A-E. In step 1414, the under-sampling module 1606 receives the analog PM carrier signal 916 (FIG. 37A). In step 1416, the under-sampling module 1606 receives the under-sampling signal 3706 (FIG. 37C). In step 1418, the under-sampling module 1606 under-samples the analog PM carrier signal 916 at the aliasing rate of the under-sampling signal 3706 to down-convert the PM carrier signal 916 to the demodulated analog baseband signal 3710 in FIG. 37D or to the filtered demodulated analog baseband signal 3712 in FIG. 37E.

The operation of the under-sampling system 1602 is now described for the digital PM carrier signal 1016, with reference to the flowchart 1413 and the timing diagrams of FIGS. 38A-E. In step 1414, the under-sampling module 1606 receives the digital PM carrier signal 1016 (FIG. 38A). In step

1416, the under-sampling module 1606 receives the under-sampling signal 3806 (FIG. 38C). In step 1418, the under-sampling module 1606 under-samples the digital PM carrier signal 1016 at the aliasing rate of the under-sampling signal 3806 to down-convert the digital PM carrier signal 1016 to the demodulated digital baseband signal 3810 in FIG. 38D or to the filtered demodulated digital baseband signal 3812 in FIG. 38E.

2.2.3 Other Embodiments

The embodiments described above are provided for purposes of illustration. These embodiments are not intended to limit the invention. Alternate embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate embodiments fall within the scope and spirit of the present invention.

2.3 Implementation Examples

Exemplary operational and/or structural implementations related to the method(s), structure(s), and/or embodiments described above are presented in Sections 4 and 5 below. These implementations are presented for purposes of illustration, and not limitation. The invention is not limited to the particular implementation examples described therein. Alternate implementations (including equivalents, extensions, variations, deviations, etc., of those described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

3. Modulation Conversion

In an embodiment, the invention down-converts an FM carrier signal F_{FMC} to a non-FM signal $F_{(NON\text{-}FM)}$, by under-sampling the FM carrier signal F_{FMC}. This embodiment is illustrated in FIG. 45B as 4512.

In an example embodiment, the FM carrier signal F_{FMC} is down-converted to a phase modulated (PM) signal F_{PM}. In another example embodiment, the FM carrier signal F_{FMC} is down- converted to an amplitude modulated (AM) signal F_{AM}. The invention is not limited to these embodiments. The down-converted signal can be demodulated with any conventional demodulation technique to obtain a demodulated baseband signal F_{DMB}.

The invention can be implemented with any type of FM signal. Exemplary embodiments are provided below for down-converting a frequency shift keying (FSK) signal to a non-FSK signal. FSK is a sub-set of FM, wherein an FM signal shifts or switches between two or more frequencies. FSK is typically used for digital modulating baseband signals, such as the digital modulating baseband signal 310 in FIG. 3. For example, in FIG. 8, the digital FM signal 816 is an FSK signal that shifts between an upper frequency and a lower frequency, corresponding to amplitude shifts in the digital modulating baseband signal 310. The FSK signal 816 is used in example embodiments below.

In a first example embodiment, the FSK signal 816 is under-sampled at an aliasing rate that is based on a mid-point between the upper and lower frequencies of the FSK signal 816. When the aliasing rate is based on the mid-point, the FSK signal 816 is down-converted to a phase shift keying (PSK) signal. PSK is a sub-set of phase modulation, wherein a PM signal shifts or switches between two or more phases. PSK is typically used for digital modulating baseband signals. For example, in FIG. 10, the digital PM signal

1016 is a PSK signal that shifts between two phases. The PSK signal 1016 can be demodulated by any conventional PSK demodulation technique(s).

In a second example embodiment, the FSK signal 816 is under-sampled at an aliasing rate that is based upon either the upper frequency or the lower frequency of the FSK signal 816. When the aliasing rate is based upon the upper frequency or the lower frequency of the FSK signal 816, the FSK signal 816 is down-converted to an amplitude shift keying (ASK) signal. ASK is a sub-set of amplitude modulation, wherein an AM signal shifts or switches between two or more amplitudes. ASK is typically used for digital modulating baseband signals. For example, in FIG. 6, the digital AM signal 616 is an ASK signal that shifts between the first amplitude and the second amplitude. The ASK signal 616 can be demodulated by any conventional ASK demodulation technique(s).

The following sections describe methods for under-sampling an FM carrier signal F_{FMC} to down-convert it to the non-FM signal $F_{(NON-FM)}$. Exemplary structural embodiments for implementing the methods are also described. It should be understood that the invention is not limited to the particular embodiments described below. Equivalents, extensions, variations, deviations, etc., of the following will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such equivalents, extensions, variations, deviations, etc., are within the scope and spirit of the present invention.

The following sections include a high level discussion, example embodiments, and implementation examples.

3.1 High Level Description

This section (including its subsections) provides a high-level description of under-sampling the FM carrier signal F_{FM} to down-convert it to the non-FM signal $F_{(NON-FM)}$, according to the invention. In particular, an

operational process for down-converting the FM carrier signal F_{FM} to the non-FM signal $F_{(NON-FM)}$ is described at a high-level. Also, a structural implementation for implementing this process is described at a high-level. The structural implementation is described herein for illustrative purposes, and is not limiting. In particular, the process described in this section can be achieved using any number of structural implementations, one of which is described in this section. The details of such structural implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

3.1.1 Operational Description

FIG. 14D depicts a flowchart 1419 that illustrates an exemplary method for down-converting the FM carrier signal F_{FMC} to the non-FM signal $F_{(NON-FM)}$. The exemplary method illustrated in the flowchart 1419 is an embodiment of the flowchart 1401 in FIG. 14A.

Any and all forms of frequency modulation techniques are valid for this invention. For ease of discussion, the digital FM carrier (FSK) signal 816 is used to illustrate a high level operational description of the invention. Subsequent sections provide detailed flowcharts and descriptions for the FSK signal 816. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention can be implemented to down-convert any type of FM signal.

The method illustrated in the flowchart 1419 is described below at a high level for down-converting the FSK signal 816 in FIG. 8C to a PSK signal. The FSK signal 816 is re-illustrated in FIG. 39A for convenience.

The process of the flowchart 1419 begins at step 1420, which includes receiving an FM signal. This is represented by the FSK signal 816. The FSK signal 816 shifts between an upper frequency 3910 and a lower frequency 3912. In an exemplary embodiment, the upper frequency 3910 is

approximately 901 MHZ and the lower frequency 3912 is approximately 899 MHZ.

Step 1422 includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. 39B illustrates an example under-sampling signal 3902 which includes a train of pulses 3903 having negligible apertures that tend towards zero time in duration. The pulses 3903 repeat at the aliasing rate or pulse repetition rate.

When down-converting an FM carrier signal F_{FMC} to a non-FM signal $F_{(NON\text{-}FM)}$, the aliasing rate is substantially equal to a frequency contained within the FM signal, or substantially equal to a harmonic or sub-harmonic thereof. In this example overview embodiment, where the FSK signal 816 is to be down-converted to a PSK signal, the aliasing rate is based on a mid-point between the upper frequency 3910 and the lower frequency 3912. For this example, the mid-point is approximately 900 MHZ. In another embodiment described below, where the FSK signal 816 is to be down-converted to an ASK signal, the aliasing rate is based on either the upper frequency 3910 or the lower frequency 3912, not the mid-point.

Step 1424 includes under-sampling the FM signal F_{FMC} at the aliasing rate to down-convert the FM carrier signal F_{FMC} to the non-FM signal $F_{(NON\text{-}FM)}$. Step 1424 is illustrated in FIG. 39C, which illustrates a stair step PSK signal 3904, which is generated by the modulation conversion process.

When the upper frequency 3910 is under-sampled, the PSK signal 3904 has a frequency of approximately 1 MHZ and is used as a phase reference. When the lower frequency 3912 is under-sampled, the PSK signal 3904 has a frequency of 1 MHZ and is phase shifted 180 degrees from the phase reference.

FIG. 39D depicts a PSK signal 3906, which is a filtered version of the PSK signal 3904. The invention can thus generate a filtered output signal, a partially filtered output signal, or a relatively unfiltered stair step output signal.

The choice between filtered, partially filtered and non-filtered output signals is generally a design choice that depends upon the application of the invention.

The aliasing rate of the under-sampling signal is preferably controlled to optimize the down-converted signal for amplitude output and polarity, as desired.

Detailed exemplary embodiments for down-converting an FSK signal to a PSK signal and for down-converting an FSK signal to an ASK signal are provided below.

3.1.2 Structural Description

FIG. 16 illustrates the block diagram of the under-sampling system 1602 according to an embodiment of the invention. The under-sampling system 1602 includes the under-sampling module 1606. The under-sampling system 1602 is an example embodiment of the generic aliasing system 1302 in FIG. 13.

In a modulation conversion embodiment, the EM signal 1304 is an FM carrier signal and the under-sampling module 1606 under-samples the FM carrier signal at a frequency that is substantially equal to a harmonic of a frequency within the FM signal or, more typically, substantially equal to a sub-harmonic of a frequency within the FM signal. Preferably, the under-sampling module 1606 under-samples the FM carrier signal F_{FMC} to down-convert it to a non-FM signal $F_{(NON\text{-}FM)}$ in the manner shown in the operational flowchart 1419. But it should be understood that the scope and spirit of the invention includes other structural embodiments for performing the steps of the flowchart 1419. The specifics of the other structural embodiments will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

The operation of the under-sampling system 1602 shall now be described with reference to the flowchart 1419 and the timing diagrams of

FIGS. 39A-39D. In step 1420, the under-sampling module 1606 receives the FSK signal 816. In step 1422, the under-sampling module 1606 receives the under-sampling signal 3902. In step 1424, the under-sampling module 1606 under-samples the FSK signal 816 at the aliasing rate of the under-sampling signal 3902 to down-convert the FSK signal 816 to the PSK signal 3904 or 3906.

Example implementations of the under-sampling module 1606 are provided in Section 4 below.

3.2 Example Embodiments

Various embodiments related to the method(s) and structure(s) described above are presented in this section (and its subsections). These embodiments are described herein for purposes of illustration, and not limitation. The invention is not limited to these embodiments. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

The method for down-converting an FM carrier signal F_{FMC} to a non-FM signal, $F_{(NON\text{-}FM)}$, illustrated in the flowchart 1419 of FIG.14D, can be implemented with any type of FM carrier signal including, but not limited to, FSK signals. The flowchart 1419 is described in detail below for down-converting an FSK signal to a PSK signal and for down-converting a PSK signal to an ASK signal. The exemplary descriptions below are intended to facilitate an understanding of the present invention. The present invention is not limited to or by the exemplary embodiments below.

3.2.1 First Example Embodiment: Down-Converting an FM Signal to a PM Signal

3.2.1.1 Operational Description

Operation of the exemplary process of the flowchart 1419 in FIG. 14D is now described for down-converting the FSK signal 816 illustrated in FIG. 8C to a PSK signal. The FSK signal 816 is re-illustrated in FIG. 40A for convenience.

The FSK signal 816 shifts between a first frequency 4006 and a second frequency 4008. In the exemplary embodiment, the first frequency 4006 is lower than the second frequency 4008. In an alternative embodiment, the first frequency 4006 is higher than the second frequency 4008. For this example, the first frequency 4006 is approximately 899 MHZ and the second frequency 4008 is approximately 901 MHZ.

FIG. 40B illustrates an FSK signal portion 4004 that represents a portion of the FSK signal 816 on an expanded time scale.

The process of down-converting the FSK signal 816 to a PSK signal begins at step 1420, which includes receiving an FM signal. This is represented by the FSK signal 816.

Step 1422 includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. 40C illustrates an example under-sampling signal 4007 on approximately the same time scale as FIG. 40B. The under-sampling signal 4007 includes a train of pulses 4009 having negligible apertures that tend towards zero time in duration. The pulses 4009 repeat at the aliasing rate, which is determined or selected as described above. Generally, when down-converting an FM signal to a non-FM signal, the aliasing rate is substantially equal to a harmonic or, more typically, a sub-harmonic of a frequency contained within the FM signal.

In this example, where an FSK signal is being down-converted to a PSK signal, the aliasing rate is substantially equal to a harmonic of the mid-

point between the frequencies 4006 and 4008 or, more typically, substantially equal to a sub-harmonic of the mid-point between the frequencies 4006 and 4008. In this example, where the first frequency 4006 is 899 MHZ and second frequency 4008 is 901 MHZ, the mid-point is approximately 900 MHZ. Suitable aliasing rates include 1.8 GHZ, 900 MHZ, 450 MHZ, etc. In this example, the aliasing rate of the under-sampling signal 4008 is approximately 450 MHZ.

Step 1424 includes under-sampling the FM signal at the aliasing rate to down-convert it to the non-FM signal $F_{(NON-FM)}$. Step 1424 is illustrated in FIG. 40B by under-sample points 4005. The under-sample points 4005 occur at the aliasing rate of the pulses 4009.

In FIG. 40D, voltage points 4010 correlate to the under-sample points 4005. In an embodiment, the voltage points 4010 form a PSK signal 4012. This can be accomplished in many ways. For example, each voltage point 4010 can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as described below.

When the first frequency 4006 is under-sampled, the PSK signal 4012 has a frequency of approximately 1 MHZ and is used as a phase reference. When the second frequency 4008 is under-sampled, the PSK signal 4012 has a frequency of 1 MHZ and is phase shifted 180 degrees from the phase reference.

In FIG. 40E, a PSK signal 4014 illustrates the PSK signal 4012, after filtering, on a compressed time scale. Although FIG. 40E illustrates the PSK signal 4012 as a filtered output signal 4014, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications. The PSK signal 4014 can be demodulated through any conventional phase demodulation technique.

The aliasing rate of the under-sampling signal is preferably controlled to optimize the down-converted signal for amplitude output and polarity, as desired.

In the example above, the under-sample points 4005 occur at positive locations of the FSK signal 816. Alternatively, the under-sample points 4005 can occur at other locations including negative points of the FSK signal 816. When the under-sample points 4005 occur at negative locations of the FSK signal 816, the resultant PSK signal is inverted relative to the PSK signal 4014.

The drawings referred to herein illustrate modulation conversion in accordance with the invention. For example, the PSK signal 4014 in FIG. 40E illustrates that the FSK signal 816 was successfully down-converted to the PSK signal 4012 and 4014 by retaining enough baseband information for sufficient reconstruction.

3.2.1.2 Structural Description

The operation of the under-sampling system 1602 is now described for down-converting the FSK signal 816 to a PSK signal, with reference to the flowchart 1419 and to the timing diagrams of FIGS. 40A-E. In step 1420, the under-sampling module 1606 receives the FSK signal 816 (FIG. 40A). In step 1422, the under-sampling module 1606 receives the under-sampling signal 4007 (FIG. 40C). In step 1424, the under-sampling module 1606 under-samples the FSK signal 816 at the aliasing rate of the under-sampling signal 4007 to down-convert the FSK signal 816 to the PSK signal 4012 in FIG. 40D or the PSK signal 4014 in FIG. 40E.

3.2.2 Second Example Embodiment: Down-Converting an FM Signal to an AM Signal

3.2.2.1 Operational Description

Operation of the exemplary process of FIG. 14D is now described for down-converting the FSK signal 816, illustrated in FIG. 8C, to an ASK signal. The FSK signal 816 is re-illustrated in FIG. 41A for convenience.

The FSK signal 816 shifts between a first frequency 4106 and a second frequency 4108. In the exemplary embodiment, the first frequency 4106 is lower than the second frequency 4108. In an alternative embodiment, the first frequency 4106 is higher than the second frequency 4108. For this example, the first frequency 4106 is approximately 899 MHZ and the second frequency 4108 is approximately 901 MHZ.

FIG. 41B illustrates an FSK signal portion 4104 that represents a portion of the FSK signal 816 on an expanded time scale.

The process of down-converting the FSK signal 816 to an ASK signal begins at step 1420, which includes receiving an FM signal. This is represented by the FSK signal 816.

Step 1422 includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. 41C illustrates an example under-sampling signal 4107 illustrated on approximately the same time scale as FIG. 42B. The under-sampling signal 4107 includes a train of pulses 4109 having negligible apertures that tend towards zero time in duration. The pulses 4109 repeat at the aliasing rate, or pulse repetition rate. The aliasing rate is determined or selected as described above.

Generally, when down-converting an FM signal to a non-FM signal, the aliasing rate is substantially equal to a harmonic of a frequency within the FM signal or, more typically, to a sub-harmonic of a frequency within the FM signal. When an FSK signal 816 is being down-converted to an ASK signal, the aliasing rate is substantially equal to a harmonic of the first frequency 4106

or the second frequency 4108 or, more typically, substantially equal to a sub-harmonic of the first frequency 4106 or the second frequency 4108 . In this example, where the first frequency 4106 is 899 MHZ and the second frequency 4108 is 901 MHZ, the aliasing rate can be substantially equal to a harmonic or sub-harmonic of 899 MHZ or 901 MHZ. In this example the aliasing rate is approximately 449.5 MHZ, which is a sub-harmonic of the first frequency 4106.

Step 1424 includes under-sampling the FM signal at the aliasing rate to down-convert it to a non-FM signal $F_{(NON\text{-}FM)}$. Step 1424 is illustrated in FIG. 41B by under-sample points 4105. The under-sample points 4105 occur at the aliasing rate of the pulses 4109. When the first frequency 4106 is under-sampled, the aliasing pulses 4109 and the under-sample points 4105 occur at the same location of subsequent cycles of the FSK signal 816. This generates a relatively constant output level. But when the second frequency 4108 is under-sampled, the aliasing pulses 4109 and the under-sample points 4005 occur at different locations of subsequent cycles of the FSK signal 816. This generates an oscillating pattern at approximately (901 MHZ - 899 MHZ) = 2 MHZ.

In FIG. 41D, voltage points 4110 correlate to the under-sample points 4105. In an embodiment, the voltage points 4110 form an ASK signal 4112. This can be accomplished in many ways. For example, each voltage point 4110 can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as described below.

In FIG. 41E, an ASK signal 4114 illustrates the ASK signal 4112, after filtering, on a compressed time scale. Although FIG. 41E illustrates the ASK signal 4114 as a filtered output signal, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications. The ASK signal 4114

can be demodulated through any conventional amplitude demodulation technique

When down-converting from FM to AM, the aliasing rate of the under-sampling signal is preferably controlled to optimize the demodulated baseband signal for amplitude output and/or polarity, as desired.

In an alternative embodiment, the aliasing rate is based on the second frequency and the resultant ASK signal is reversed relative to the ASK signal 4114.

The drawings referred to herein illustrate modulation conversion in accordance with the invention. For example, the ASK signal 4114 in FIG. 41E illustrates that the FSK carrier signal 816 was successfully down-converted to the ASK signal 4114 by retaining enough baseband information for sufficient reconstruction.

3.2.2.2 Structural Description

The operation of the under-sampling system 1602 is now described for down-converting the FSK signal 816 to an ASK signal, with reference to the flowchart 1419 and to the timing diagrams of FIGS. 41A-E. In step 1420, the under-sampling module 1606 receives the FSK signal 816 (FIG. 41A). In step 1422, the under-sampling module 1606 receives the under-sampling signal 4107 (FIG. 41C). In step 1424, the under-sampling module 1606 under-samples the FSK signal 816 at the aliasing of the under-sampling signal 4107 to down-convert the FSK signal 816 to the ASK signal 4112 of FIG. 41D or the ASK signal 4114 in FIG. 41E.

3.2.3 Other Example Embodiments

The embodiments described above are provided for purposes of illustration. These embodiments are not intended to limit the invention.

Alternate embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate embodiments fall within the scope and spirit of the present invention.

3.3 Implementation Examples

Exemplary operational and/or structural implementations related to the method(s), structure(s), and/or embodiments described above are presented in Sections 4 and 5 below. These implementations are presented for purposes of illustration, and not limitation. The invention is not limited to the particular implementation examples described therein. Alternate implementations (including equivalents, extensions, variations, deviations, etc., of those described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

4. Implementation Examples

Exemplary operational and/or structural implementations related to the method(s), structure(s), and/or embodiments described in the Sub-Sections above are presented in this section (and its subsections). These implementations are presented herein for purposes of illustration, and not limitation. The invention is not limited to the particular implementation examples described herein. Alternate implementations (including equivalents, extensions, variations, deviations, etc., of those described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

FIG. 13 illustrates a generic aliasing system 1302, including an aliasing module 1306. FIG. 16 illustrates an under-sampling system 1602, which includes an under-sampling module 1606. The under-sampling module 1606 receives an under-sampling signal 1604 having an aliasing rate F_{AR}. The under-sampling signal 1604 includes a train of pulses having negligible apertures that tend towards zero time in duration. The pulses repeat at the aliasing rate F_{AR}. The under-sampling system 1602 is an example implementation of the generic aliasing system 1303. The under-sampling system 1602 outputs a down-converted signal 1308A.

FIG. 26A illustrates an exemplary sample and hold system 2602, which is an exemplary implementation of the under-sampling system 1602. The sample and hold system 2602 is described below.

FIG. 26B illustrates an exemplary inverted sample and hold system 2606, which is an alternative example implementation of the under-sampling system 1602. The inverted sample and hold system 2606 is described below.

4.1 The Under-Sampling System as a Sample and Hold System

FIG. 26A is a block diagram of a the sample and hold system 2602, which is an example embodiment of the under-sampling module 1606 in FIG. 16, which is an example embodiment of the generic aliasing module 1306 in FIG. 13.

The sample and hold system 2602 includes a sample and hold module 2604, which receives the EM signal 1304 and the under-sampling signal 1604. The sample and hold module 2604 under-samples the EM signal at the aliasing rate of the under-sampling signal 1604, as described in the sections above with respect to the flowcharts 1401 in FIG. 14A, 1407 in FIG. 14B, 1413 in FIG. 14C and 1419 in FIG. 14D. The under-sampling system 1602 outputs a down-converted signal 1308A.

FIG. 27 illustrates an under-sampling system 2701 as a sample and hold system, which is an example implementation of the under-sampling system 2602. The under-sampling system 2701 includes a switch module 2702 and a holding module 2706. The under-sampling system 2701 is described below.

FIG. 24A illustrates an under-sampling system 2401 as a break before make under-sampling system, which is an alternative implementation of the under-sampling system 2602. The break before make under-sampling system 2401 is described below.

4.4.1 The Sample and Hold System as a Switch Module and a Holding Module

FIG. 27 illustrates an exemplary embodiment of the sample and hold module 2604 from FIG. 26A. In the exemplary embodiment, the sample and hold module 2604 includes a switch module 2702, and a holding module 2706.

Preferably, the switch module 2702 and the holding module 2706 under-sample the EM signal 1304 to down-convert it in any of the manners shown in the operation flowcharts 1401, 1407, 1413 and 1419. For example, the sample and hold module 2604 can receive and under-sample any of the modulated carrier signal signals described above, including, but not limited to, the analog AM signal 516, the digital AM signal 616, the analog FM signal 716, the digital FM signal 816, the analog PM signal 916, the digital PM signal 1016, etc., and any combinations thereof.

The switch module 2702 and the holding module 2706 down-convert the EM signal 1304 to an intermediate signal, to a demodulated baseband or to a different modulation scheme, depending upon the aliasing rate.

For example, operation of the switch module 2702 and the holding module 2706 are now described for down-converting the EM signal 1304 to an

intermediate signal, with reference to the flowchart 1407 and the example timing diagrams in FIG. 79A-F.

In step 1408, the switch module 2702 receives the EM signal 1304 (FIG. 79A). In step 1410, the switch module 2702 receives the under-sampling signal 1604 (FIG. 79C). In step 1412, the switch module 2702 and the holding module 2706 cooperate to under-sample the EM signal 1304 and down-convert it to an intermediate signal. More specifically, during step 1412, the switch module 2702 closes during each under-sampling pulse to couple the EM signal 1304 to the holding module 2706. In an embodiment, the switch module 2702 closes on rising edges of the pulses. In an alternative embodiment, the switch module 2702 closes on falling edges of the pulses. When the EM signal 1304 is coupled to the holding module 2706, the amplitude of the EM signal 1304 is captured by the holding module 2706. The holding module 2706 is designed to capture and hold the amplitude of the EM signal 1304 within the short time frame of each negligible aperture pulse. FIG. 79B illustrates the EM signal 1304 after under-sampling.

The holding module 2706 substantially holds or maintains each under-sampled amplitude until a subsequent under-sample. (FIG. 79D). The holding module 2706 outputs the under-sampled amplitudes as the down-converted signal 1308A. The holding module 2706 can output the down-converted signal 1308A as an unfiltered signal, such as a stair step signal (FIG. 79E), as a filtered down-converted signal (FIG. 79F) or as a partially filtered down-converted signal.

4.1.2 The Sample and Hold System as Break-Before-Make Module

FIG. 24A illustrates a break-before-make under-sampling system 2401, which is an alternative implementation of the under-sampling system 2602.

Preferably, the break-before-make under-sampling system 2401 under-samples the EM signal 1304 to down-convert it in any of the manners shown in the operation flowcharts 1401, 1407, 1413 and 1419. For example, the sample and hold module 2604 can receive and under-sample any of the unmodulated or modulated carrier signal signals described above, including, but not limited to, the analog AM signal 516, the digital AM signal 616, the analog FM signal 716, the digital FM signal 816, the analog PM signal 916, the digital PM signal 1016, etc., and combinations thereof.

The break-before-make under-sampling system 2401 down-converts the EM signal 1304 to an intermediate signal, to a demodulated baseband or to a different modulation scheme, depending upon the aliasing rate.

FIG. 24A includes a break-before-make switch 2402. The break-before-make switch 2402 includes a normally open switch 2404 and a normally closed switch 2406. The normally open switch 2404 is controlled by the under-sampling signal 1604, as previously described. The normally closed switch 2406 is controlled by an isolation signal 2412. In an embodiment, the isolation signal 2412 is generated from the under-sampling signal 1604. Alternatively, the under-sampling signal 1604 is generated from the isolation signal 2412. Alternatively, the isolation signal 2412 is generated independently from the under-sampling signal 1604. The break-before-make module 2402 substantially isolates a sample and hold input 2408 from a sample and hold output 2410.

FIG. 24B illustrates an example timing diagram of the under-sampling signal 1604 that controls the normally open switch 2404. FIG. 24C illustrates an example timing diagram of the isolation signal 2412 that controls the normally closed switch 2406. Operation of the break-before-make module 2402 is described with reference to the example timing diagrams in FIGS. 24B and 24C.

Prior to time t0, the normally open switch 2404 and the normally closed switch 2406 are at their normal states.

At time t0, the isolation signal 2412 in FIG. 24C opens the normally closed switch 2406. Then, just after time t0, the normally open switch 2404 and the normally closed switch 2406 are open and the input 2408 is isolated from the output 2410.

At time t1, the under-sampling signal 1604 in FIG. 24B briefly closes the normally open switch 2404. This couples the EM signal 1304 to the holding module 2416.

Prior to t2, the under-sampling signal 1604 in FIG. 24B opens the normally open switch 2404. This de-couples the EM signal 1304 from the holding module 2416.

At time t2, the isolation signal 2412 in FIG. 24C closes the normally closed switch 2406. This couples the holding module 2416 to the output 2410.

The break-before-make under-sampling system 2401 includes a holding module 2416, which can be similar to the holding module 2706 in FIG. 27. The break-before-make under-sampling system 2401 down-converts the EM signal 1304 in a manner similar to that described with reference to the under-sampling system 2702 in FIG. 27.

4.1.3 Example Implementations of the Switch Module

The switch module 2702 in FIG. 27 and the switch modules 2404 and 2406 in FIG. 24A can be any type of switch device that preferably has a relatively low impedance when closed and a relatively high impedance when open. The switch modules 2702, 2404 and 2406 can be implemented with normally open or normally closed switches. The switch device need not be an ideal switch device. FIG. 28B illustrates the switch modules 2702, 2404 and 2406 as, for example, a switch module 2810.

The switch device 2810 (e.g., switch modules 2702, 2404 and 2406) can be implemented with any type of suitable switch device, including, but not limited to mechanical switch devices and electrical switch devices, optical switch devices, etc., and combinations thereof. Such devices include, but are not limited to transistor switch devices, diode switch devices, relay switch devices, optical switch devices, micro-machine switch devices, etc..

In an embodiment, the switch module 2810 can be implemented as a transistor, such as, for example, a field effect transistor (FET), a bi-polar transistor, or any other suitable circuit switching device.

In FIG. 28A, the switch module 2810 is illustrated as a FET 2802. The FET 2802 can be any type of FET, including, but not limited to, a MOSFET, a JFET, a GaAsFET, etc.. The FET 2802 includes a gate 2804, a source 2806 and a drain 2808. The gate 2804 receives the under-sampling signal 1604 to control the switching action between the source 2806 and the drain 2808. Generally, the source 2806 and the drain 2808 are interchangeable.

It should be understood that the illustration of the switch module 2810 as a FET 2802 in FIG. 28A is for example purposes only. Any device having switching capabilities could be used to implement the switch module 2810 (e.g., switch modules 2702, 2404 and 2406), as will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

In FIG. 28C, the switch module 2810 is illustrated as a diode switch 2812, which operates as a two lead device when the under-sampling signal 1604 is coupled to the output 2813.

In FIG. 28D, the switch module 2810 is illustrated as a diode switch 2814, which operates as a two lead device when the under-sampling signal 1604 is coupled to the output 2815.

4.1.4 Example Implementations of the Holding Module

The holding modules 2706 and 2416 preferably captures and holds the amplitude of the original, unaffected, EM signal 1304 within the short time frame of each negligible aperture under-sampling signal pulse.

In an exemplary embodiment, holding modules 2706 and 2416 are implemented as a reactive holding module 2901 in FIG. 29A, although the invention is not limited to this embodiment. A reactive holding module is a holding module that employs one or more reactive electrical components to preferably quickly charge to the amplitude of the EM signal 1304. Reactive electrical components include, but are not limited to, capacitors and inductors.

In an embodiment, the holding modules 2706 and 2416 include one or more capacitive holding elements, illustrated in FIG. 29B as a capacitive holding module 2902. In FIG. 29C, the capacitive holding module 2902 is illustrated as one or more capacitors illustrated generally as capacitor(s) 2904. Recall that the preferred goal of the holding modules 2706 and 2416 is to quickly charge to the amplitude of the EM signal 1304. In accordance with principles of capacitors, as the negligible aperture of the under-sampling pulses tends to zero time in duration, the capacitive value of the capacitor 2904 can tend towards zero Farads. Example values for the capacitor 2904 can range from tens of pico Farads to fractions of pico Farads. A terminal 2906 serves as an output of the sample and hold module 2604. The capacitive holding module 2902 provides the under-samples at the terminal 2906, where they can be measured as a voltage. FIG. 29F illustrates the capacitive holding module 2902 as including a series capacitor 2912, which can be utilized in an inverted sample and hold system as described below.

In an alternative embodiment, the holding modules 2706 and 2416 include one or more inductive holding elements, illustrated in FIG. 29D as an inductive holding module 2908.

In an alternative embodiment, the holding modules 2706 and 2416 include a combination of one or more capacitive holding elements and one or more inductive holding elements, illustrated in FIG. 29E as a capacitive/inductive holding module 2910.

FIG. 29G illustrates an integrated under-sampling system that can be implemented to down-convert the EM signal 1304 as illustrated in, and described with reference to, FIGS. 79A-F.

4.1.5 Optional Under-Sampling Signal Module

FIG. 30 illustrates an under-sampling system 3001, which is an example embodiment of the under-sampling system 1602. The under-sampling system 3001 includes an optional under-sampling signal module 3002 that can perform any of a variety of functions or combinations of functions, including, but not limited to, generating the under-sampling signal 1604.

In an embodiment, the optional under-sampling signal module 3002 includes an aperture generator, an example of which is illustrated in FIG. 29J as an aperture generator 2920. The aperture generator 2920 generates negligible aperture pulses 2926 from an input signal 2924. The input signal 2924 can be any type of periodic signal, including, but not limited to, a sinusoid, a square wave, a saw-tooth wave, etc. Systems for generating the input signal 2924 are described below.

The width or aperture of the pulses 2926 is determined by delay through the branch 2922 of the aperture generator 2920. Generally, as the desired pulse width decreases, the tolerance requirements of the aperture generator 2920 increase. In other words, to generate negligible aperture pulses for a given input EM frequency, the components utilized in the example aperture generator 2920 require greater reaction times, which are typically obtained with more expensive elements, such as gallium arsenide (GaAs), etc.

The example logic and implementation shown in the aperture generator 2920 are provided for illustrative purposes only, and are not limiting. The actual logic employed can take many forms. The example aperture generator 2920 includes an optional inverter 2928, which is shown for polarity consistency with other examples provided herein. An example implementation of the aperture generator 2920 is illustrated in FIG. 29K.

Additional examples of aperture generation logic is provided in FIGS. 29H and 29I. FIG. 29H illustrates a rising edge pulse generator 2940, which generates pulses 2926 on rising edges of the input signal 2924. FIG. 29I illustrates a falling edge pulse generator 2950, which generates pulses 2926 on falling edges of the input signal 2924.

In an embodiment, the input signal 2924 is generated externally of the under-sampling signal module 3002, as illustrated in FIG. 30. Alternatively, the input signal 2924 is generated internally by the under-sampling signal module 3002. The input signal 2924 can be generated by an oscillator, as illustrated in FIG. 29L by an oscillator 2930. The oscillator 2930 can be internal to the under-sampling signal module 3002 or external to the under-sampling signal module 3002. The oscillator 2930 can be external to the under-sampling system 3001.

The type of down-conversion performed by the under-sampling system 3001 depends upon the aliasing rate of the under-sampling signal 1604, which is determined by the frequency of the pulses 2926. The frequency of the pulses 2926 is determined by the frequency of the input signal 2924. For example, when the frequency of the input signal 2924 is substantially equal to a harmonic or a sub-harmonic of the EM signal 1304, the EM signal 1304 is directly down-converted to baseband (e.g. when the EM signal is an AM signal or a PM signal), or converted from FM to a non-FM signal. When the frequency of the input signal 2924 is substantially equal to a harmonic or a

sub-harmonic of a difference frequency, the EM signal 1304 is down-converted to an intermediate signal.

The optional under-sampling signal module 3002 can be implemented in hardware, software, firmware, or any combination thereof.

4.2 The Under-Sampling System as an Inverted Sample and Hold

FIG. 26B illustrates an exemplary inverted sample and hold system 2606, which is an alternative example implementation of the under-sampling system 1602.

FIG. 42 illustrates a inverted sample and hold system 4201, which is an example implementation of the inverted sample and hold system 2606 in FIG. 26B. The sample and hold system 4201 includes a sample and hold module 4202, which includes a switch module 4204 and a holding module 4206. The switch module 4204 can be implemented as described above with reference to FIGS. 28A-D.

The holding module 4206 can be implemented as described above with reference to FIGS. 29A-F, for the holding modules 2706 and 2416. In the illustrated embodiment, the holding module 4206 includes one or more capacitors 4208. The capacitor(s) 4208 are selected to pass higher frequency components of the EM signal 1304 through to a terminal 4210, regardless of the state of the switch module 4204. The capacitor 4202 stores charge from the EM signal 1304 during aliasing pulses of the under-sampling signal 1604 and the signal at the terminal 4210 is thereafter off-set by an amount related to the charge stored in the capacitor 4206.

Operation of the inverted sample and hold system 4201 is illustrated in FIGS. 34A-F. FIG. 34A illustrates an example EM signal 1304. FIG. 34B illustrates the EM signal 1304 after under-sampling. FIG. 34C illustrates the under-sampling signal 1606, which includes a train of aliasing pulses having negligible apertures.

FIG. 34D illustrates an example down-converted signal 1308A. FIG. 34E illustrates the down-converted signal 1308A on a compressed time scale. Since the holding module 4206 is series element, the higher frequencies (e.g., RF) of the EM signal 1304 can be seen on the down-converted signal. This can be filtered as illustrated in FIG. 34F.

The inverted sample and hold system 4201 can be used to down-convert any type of EM signal, including modulated carrier signals and unmodulated carrier signals, to IF signals and to demodulated baseband signals.

4.3 Other Implementations

The implementations described above are provided for purposes of illustration. These implementations are not intended to limit the invention. Alternate implementations, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

5. Optional Optimizations of Under-Sampling at an Aliasing Rate

The methods and systems described in sections above can be optionally optimized with one or more of the optimization methods or systems described below.

5.1 Doubling the Aliasing Rate (FAR) of the Under-Sampling Signal

In an embodiment, the optional under-sampling signal module 3002 in FIG. 30 includes a pulse generator module that generates aliasing pulses at a multiple of the frequency of the oscillating source, such as twice the frequency

of the oscillating source. The input signal 2926 may be any suitable oscillating source.

FIG. 31A illustrates an example circuit 3102 that generates a doubler output signal 3104 (FIG. 31A and C) that may be used as an under-sampling signal 1604. The example circuit 3102 generates pulses on rising and falling edges of the input oscillating signal 3106 of FIG. 31B. Input oscillating signal 3106 is one embodiment of optional input signal 2926. The circuit 3102 can be implemented as a pulse generator and aliasing rate (F_{AR}) doubler, providing the under-sampling signal 1604 to under-sampling module 1606 in FIG. 30.

The aliasing rate is twice the frequency of the input oscillating signal F_{osc} 3106, as shown by EQ. (9) below.

$$F_{AR} = 2 \cdot F_{osc} \qquad \text{EQ. (9)}$$

The aperture width of the aliasing pulses is determined by the delay through a first inverter 3108 of FIG. 31A. As the delay is increased, the aperture is increased. A second inverter 3112 is shown to maintain polarity consistency with examples described elsewhere. In an alternate embodiment inverter 3112 is omitted. Preferably, the pulses have negligible aperture widths that tend toward zero time. The doubler output signal 3104 may be further conditioned as appropriate to drive a switch module with negligible aperture pulses. The circuit 3102 may be implemented with integrated circuitry, discretely, with equivalent logic circuitry, or with any valid fabrication technology.

5.2 Differential Implementations

The invention can be implemented in a variety of differential configurations. Differential configurations are useful for reducing common mode noise. This can be very useful in receiver systems where common mode interference can be caused by intentional or unintentional radiators such as cellular phones, CB radios, electrical appliances etc. Differential

configurations are also useful in reducing any common mode noise due to charge injection of the switch in the switch module or due to the design and layout of the system in which the invention is used. Any spurious signal that is induced in equal magnitude and equal phase in both input leads of the invention will be substantially reduced or eliminated. Some differential configurations, including some of the configurations below, are also useful for increasing the voltage and/or for increasing the power of the down-converted signal 1308A. While an example of a differential under-sampling module is shown below, the example is shown for the purpose of illustration, not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc.) of the embodiment described herein will be apparent to those skilled in the relevant art based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

FIG. 44A illustrates an example differential system 4402 that can be included in the under-sampling module 1606. The differential system 4202 includes an inverted under-sampling design similar to that described with reference to FIG. 42. The differential system 4402 includes inputs 4404 and 4406 and outputs 4408 and 4410. The differential system 4402 includes a first inverted sample and hold module 4412, which includes a holding module 4414 and a switch module 4416. The differential system 4402 also includes a second inverted sample and hold module 4418, which includes a holding module 4420 and the switch module 4416, which it shares in common with sample and hold module 4412.

One or both of the inputs 4404 and 4406 are coupled to an EM signal source. For example, the inputs can be coupled to an EM signal source, wherein the input voltages at the inputs 4404 and 4406 are substantially equal in amplitude but 180 degrees out of phase with one another. Alternatively,

where dual inputs are unavailable, one of the inputs 4404 and 4406 can be coupled to ground.

In operation, when the switch module 4416 is closed, the holding modules 4414 and 4420 are in series and, provided they have similar capacitive values, they charge to equal amplitudes but opposite polarities. When the switch module 4416 is open, the voltage at the output 4408 is relative to the input 4404, and the voltage at the output 4410 is relative to the voltage at the input 4406.

Portions of the voltages at the outputs 4408 and 4410 include voltage resulting from charge stored in the holding modules 4414 and 4420, respectively, when the switch module 4416 was closed. The portions of the voltages at the outputs 4408 and 4410 resulting from the stored charge are generally equal in amplitude to one another but 180 degrees out of phase.

Portions of the voltages at the outputs 4408 and 4410 also include ripple voltage or noise resulting from the switching action of the switch module 4416. But because the switch module is positioned between the two outputs, the noise introduced by the switch module appears at the outputs 4408 and 4410 as substantially equal and in-phase with one another. As a result, the ripple voltage can be substantially filtered out by inverting the voltage at one of the outputs 4408 or 4410 and adding it to the other remaining output. Additionally, any noise that is impressed with substantially equal amplitude and equal phase onto the input terminals 4404 and 4406 by any other noise sources will tend to be canceled in the same way.

The differential system 4402 is effective when used with a differential front end (inputs) and a differential back end (outputs). It can also be utilized in the following configurations, for example:

a) A single-input front end and a differential back end; and

b) A differential front end and single-output back end.

Examples of these system are provided below.

5.2.1 Differential Input-to-Differential Output

FIG. 44B illustrates the differential system 4402 wherein the inputs 4404 and 4406 are coupled to equal and opposite EM signal sources, illustrated here as dipole antennas 4424 and 4426. In this embodiment, when one of the outputs 4408 or 4410 is inverted and added to the other output, the common mode noise due to the switching module 4416 and other common mode noise present at the input terminals 4404 and 4406 tend to substantially cancel out.

5.2.2 Single Input-to-Differential Output

FIG. 44C illustrates the differential system 4402 wherein the input 4404 is coupled to an EM signal source such as a monopole antenna 4428 and the input 4406 is coupled to ground.

FIG. 44E illustrates an example single input to differential output receiver/down-converter system 4436. The system 4436 includes the differential system 4402 wherein the input 4406 is coupled to ground. The input 4404 is coupled to an EM signal source 4438.

The outputs 4408 and 4410 are coupled to a differential circuit 4444 such as a filter, which preferably inverts one of the outputs 4408 or 4410 and adds it to the other output 4408 or 4410. This substantially cancels common mode noise generated by the switch module 4416. The differential circuit 4444 preferably filters the higher frequency components of the EM signal 1304 that pass through the holding modules 4414 and 4420. The resultant filtered signal is output as the down-converted signal 1308A.

5.2.3 Differential Input-to-Single Output

FIG. 44D illustrates the differential system 4402 wherein the inputs 4404 and 4406 are coupled to equal and opposite EM signal sources illustrated here as dipole antennas 4430 and 4432. The output is taken from terminal 4408.

5.3 Smoothing the Down-Converted Signal

The down-converted signal 1308A may be smoothed by filtering as desired. The differential circuit 4444 implemented as a filter in FIG 44E illustrates but one example. Filtering may be accomplished in any of the described embodiments by hardware, firmware and software implementation as is well known by those skilled in the arts.

5.4 Load Impedance and Input/Output Buffering

Some of the characteristics of the down-converted signal 1308A depend upon characteristics of a load placed on the down-converted signal 1308A. For example, in an embodiment, when the down-converted signal 1308A is coupled to a high impedance load, the charge that is applied to a holding module such as holding module 2706 in FIG 27 or 2416 in FIG. 24A during a pulse generally remains held by the holding module until the next pulse. This results in a substantially stair-step-like representation of the down-converted signal 1308A as illustrated in FIG. 15C, for example. A high impedance load enables the under-sampling system 1606 to accurately represent the voltage of the original unaffected input signal.

The down-converted signal 1308A can be buffered with a high impedance amplifier, if desired.

Alternatively, or in addition to buffering the down-converted signal 1308A, the input EM signal may be buffered or amplified by a low noise amplifier.

5.5 Modifying the Under-Sampling Signal Utilizing Feedback

FIG. 30 shows an embodiment of a system 3001 which uses down-converted signal 1308A as feedback 3006 to control various characteristics of the under-sampling module 1606 to modify the down-converted signal 1308A.

Generally, the amplitude of the down-converted signal 1308A varies as a function of the frequency and phase differences between the EM signal 1304 and the under-sampling signal 1604. In an embodiment, the down-converted signal 1308A is used as the feedback 3006 to control the frequency and phase relationship between the EM signal 1304 and the under-sampling signal 1604. This can be accomplished using the example block diagram shown in FIG 32A. The example circuit illustrated in FIG. 32A can be included in the under-sampling signal module 3002. Alternate implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Alternate implementations fall within the scope and spirit of the present invention. In this embodiment a state-machine is used for clarity, and is not limiting.

In the example of FIG. 32A, a state machine 3204 reads an analog to digital converter, A/D 3202, and controls a digital to analog converter (DAC) 3206. In an embodiment, the state machine 3204 includes 2 memory locations, *Previous* and *Current,* to store and recall the results of reading A/D 3202. In an embodiment, the state machine 3204 utilizes at least one memory flag.

DAC 3206 controls an input to a voltage controlled oscillator, VCO 3208. VCO 3208 controls a frequency input of a pulse generator 3210, which,

in an embodiment, is substantially similar to the pulse generator shown in FIG. 29J. The pulse generator 3210 generates the under-sampling signal 1604.

In an embodiment, the state machine 3204 operates in accordance with the state machine flowchart 3220 in FIG. 32B. The result of this operation is to modify the frequency and phase relationship between the under-sampling signal 1604 and the EM signal 1304, to substantially maintain the amplitude of the down-converted signal 1308A at an optimum level.

The amplitude of the down-converted signal 1308A can be made to vary with the amplitude of the under-sampling signal 1604. In an embodiment where Switch Module 2702 is a FET as shown in FIG 28A, wherein the gate 2804 receives the under-sampling signal 1604, the amplitude of the under-sampling signal 1604 can determine the "on" resistance of the FET, which affects the amplitude of down-converted signal 1308A. Under-sampling signal module 3002, as shown in FIG. 32C, can be an analog circuit that enables an automatic gain control function. Alternate implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Alternate implementations fall within the scope and spirit of the present invention.

III. Down-Converting by Transferring Energy

The energy transfer embodiments of the invention provide enhanced signal to noise ratios and sensitivity to very small signals, as well as permitting the down-converted signal to drive lower impedance loads unassisted. The energy transfer aspects of the invention are represented generally by 4506 in FIGS. 45A and 45B. Fundamental descriptions of how this is accomplished is presented step by step beginning with a comparison with an under-sampling system.

0.1 Energy Transfer Compared to Under-Sampling

Section II above disclosed methods and systems for down-converting an EM signal by under-sampling. The under-sampling systems utilize a sample and hold system controlled by an under-sampling signal. The under-sampling signal includes a train of pulses having negligible apertures that tend towards zero time in duration. The negligible aperture pulses minimize the amount of energy transferred from the EM signal. This protects the under-sampled EM signal from distortion or destruction. The negligible aperture pulses also make the sample and hold system a high impedance system. An advantage of under-sampling is that the high impedance input allows accurate voltage reproduction of the under-sampled EM signal. The methods and systems disclosed in Section II are thus useful for many situations including, but not limited to, monitoring EM signals without distorting or destroying them.

Because the under-sampling systems disclosed in Section II transfer only negligible amounts of energy, they are not suitable for all situations. For example, in radio communications, received radio frequency (RF) signals are typically very weak and must be amplified in order to distinguish them over noise. The negligible amounts of energy transferred by the under-sampling systems disclosed in Section II may not be sufficient to distinguish received RF signals over noise.

In accordance with an aspect of the invention, methods and systems are disclosed below for down-converting EM signals by transferring non-negligible amounts of energy from the EM signals. The resultant down-converted signals have sufficient energy to allow the down-converted signals to be distinguishable from noise. The resultant down-converted signals also have sufficient energy to drive lower impedance circuits without buffering.

Down-converting by transferring energy is introduced below in an incremental fashion to distinguish it from under-sampling. The introduction begins with further descriptions of under-sampling.

0.1.1 Review of Under-Sampling

FIG. 78A illustrates an exemplary under-sampling system 7802 for down-converting an input EM signal 7804. The under-sampling system 7802 includes a switching module 7806 and a holding module shown as a holding capacitance 7808. An under-sampling signal 7810 controls the switch module 7806. The under-sampling signal 7810 includes a train of pulses having negligible pulse widths that tend toward zero time. An example of a negligible pulse width or duration can be in the range of 1-10 psec for under-sampling a 900 MHZ signal. Any other suitable negligible pulse duration can be used as well, where accurate reproduction of the original unaffected input signal voltage is desired without substantially affecting the original input signal voltage.

In an under-sampling environment, the holding capacitance 7808 preferably has a small capacitance value. This allows the holding capacitance 7808 to substantially charge to the voltage of the input EM signal 7804 during the negligible apertures of the under-sampling signal pulses. For example, in an embodiment, the holding capacitance 7808 has a value in the range of 1pF. Other suitable capacitance values can be used to achieve substantially the voltage of the original unaffected input signal. Various capacitances can be employed for certain effects, which are described below. The under-sampling system is coupled to a load 7812. In FIG. 78B, the load 7812 of FIG. 78A is illustrated as a high impedance load 7818. A high impedance load is one that is relatively insignificant to an output drive impedance of the system for a given output frequency. The high impedance load 7818 allows the

holding capacitance 7808 to substantially maintain the charge accumulated during the under-sampling pulses.

FIGS. 79A-F illustrate example timing diagrams for the under-sampling system 7802. FIG. 79A illustrates an example input EM signal 7804.

FIG. 79C illustrates an example under-sampling signal 7810, including pulses 7904 having negligible apertures that tend towards zero time in duration.

FIG. 79B illustrates the negligible effects to the input EM signal 7804 when under-sampled, as measured at a terminal 7814 of the under-sampling system 7802. In FIG. 79B, negligible distortions 7902 correlate with the pulses of the under-sampling signal 7810. In this embodiment, the negligible distortions 7902 occur at different locations of subsequent cycles of the input EM signal 7804. As a result, the input EM signal will be down-converted. The negligible distortions 7902 represent negligible amounts of energy, in the form of charge that is transferred to the holding capacitance 7808.

When the load 7812 is a high impedance load, the holding capacitance 7808 does not significantly discharge between pulses 7904. As a result, charge that is transferred to the holding capacitance 7808 during a pulse 7904 tends to "hold" the voltage value sampled constant at the terminal 7816 until the next pulse 7904. When voltage of the input EM signal 7804 changes between pulses 7904, the holding capacitance 7808 substantially attains the new voltage and the resultant voltage at the terminal 7816 forms a stair step pattern, as illustrated in FIG. 79D.

FIG. 79E illustrates the stair step voltage of FIG. 79D on a compressed time scale. The stair step voltage illustrated in FIG. 79E can be filtered to produce the signal illustrated in FIG. 79F. The signals illustrated in FIGS. 79D, E, and F have substantially all of the baseband characteristics of the input EM signal 7804 in FIG. 79A, except that the signals illustrated in FIGS. 79D, E, and F have been successfully down-converted.

Note that the voltage level of the down-converted signals illustrated in FIGS. 79E and 79F are substantially close to the voltage level of the input EM signal 7804. The under-sampling system 7802 thus down-converts the input EM signal 7804 with reasonable voltage reproduction, without substantially affecting the input EM signal 7804. But also note that the power available at the output is relatively negligible (e.g. :V^2/R; ~ 5mV and 1 MOhm), given the input EM signal 7804 would typically have a driving impedance, in an RF environment, of 50 Ohms (e.g.: V^2/R; ~ 5mV and 50 Ohms).

0.1.1.1 Effects of Lowering the Impedance of the Load

Effects of lowering the impedance of the load 7812 are now described. FIGS. 80A-E illustrate example timing diagrams for the under-sampling system 7802 when the load 7812 is a relatively low impedance load, one that is significant relative to the output drive impedance of the system for a given output frequency.

FIG. 80A illustrates an example input EM signal 7804, which is substantially similar to that illustrated in FIG. 79A.

FIG. 80C illustrates an example under-sampling signal 7810, including pulses 8004 having negligible apertures that tend towards zero time in duration. The example under-sampling signal 7810 illustrated in FIG. 80C is substantially similar to that illustrated in FIGS. 79C.

FIG.80B illustrates the negligible effects to the input EM signal 7804 when under-sampled, as measured at a terminal 7814 of the under-sampling system 7802. In FIG. 80B, negligible distortions 8002 correlate with the pulses 8004 of the under-sampling signal 7810 in FIG. 80C. In this example, the negligible distortions 8002 occur at different locations of subsequent cycles of the input EM signal 7804. As a result, the input EM signal 7804 will be down-converted. The negligible distortions 8002 represent negligible

amounts of energy, in the form of charge that is transferred to the holding capacitance 7808.

When the load 7812 is a low impedance load, the holding capacitance 7808 is significantly discharged by the load between pulses 8004 (FIG. 80C). As a result, the holding capacitance 7808 cannot reasonably attain or "hold" the voltage of the original EM input signal 7804, as was seen in the case of FIG. 79D. Instead, the charge appears as the output illustrated in FIG. 80D.

FIG. 80E illustrates the output from FIG. 80D on a compressed time scale. The output in FIG. 80E can be filtered to produce the signal illustrated in FIG. 80F. The down-converted signal illustrated in FIG. 80F is substantially similar to the down-converted signal illustrated in FIG. 79F, except that the signal illustrated in FIG. 80F is substantially smaller in magnitude than the amplitude of the down-converted signal illustrated in FIG. 79F. This is because the low impedance of the load 7812 prevents the holding capacitance 7808 from reasonably attaining or "holding" the voltage of the original EM input signal 7804. As a result, the down-converted signal illustrated in FIG. 80F cannot provide optimal voltage reproduction, and has relatively negligible power available at the output (e.g.: V^2/R; ~ 200□V and 2KOhms), given the input EM signal 7804 would typically have a driving impedance, in an RF environment, of 50 Ohms (e.g.: V^2/R; ~ 5mV and 50 Ohms).

0.1.1.2 Effects of Increasing the Value of the Holding Capacitance

Effects of increasing the value of the holding capacitance 7808, while having to drive a low impedance load 7812, is now described. FIGS. 81A-F illustrate example timing diagrams for the under-sampling system 7802 when the holding capacitance 7808 has a larger value, in the range of 18pF for example.

FIG. 81 A illustrates an example input EM signal 7804, which is substantially similar to that illustrated in FIGS. 79A and 80A.

FIG. 81C illustrates an example under-sampling signal 7810, including pulses 8104 having negligible apertures that tend towards zero time in duration. The example under-sampling signal 7810 illustrated in FIG. 81C is substantially similar to that illustrated in FIGS. 79C and 80C.

FIG.81B illustrates the negligible effects to the input EM signal 7804 when under-sampled, as measured at a terminal 7814 of the under-sampling system 7802. In FIG. 81B, negligible distortions 8102 correlate with the pulses 8104 of the under-sampling signal 7810 in FIG. 81C. Upon close inspection, the negligible distortions 8102 occur at different locations of subsequent cycles of the input EM signal 7804. As a result, the input EM signal 7804 will be down-converted. The negligible distortions 8102 represent negligible amounts of energy, in the form of charge that is transferred to the holding capacitance 7808.

FIG. 81D illustrates the voltage measured at the terminal 7816, which is a result of the holding capacitance 7808 attempting to attain and "hold" the original input EM signal voltage, but failing to do so, during the negligible apertures of the pulses 8104 illustrated in FIG. 81C.

Recall that when the load 7812 is a low impedance load, the holding capacitance 7808 is significantly discharged by the load between pulses 8104 (FIG. 81C), this again is seen in FIGS. 81D and E. As a result, the holding capacitance 7808 cannot reasonably attain or "hold" the voltage of the original EM input signal 7804, as was seen in the case of FIG. 79D. Instead, the charge appears as the output illustrated in FIG. 81D.

FIG. 81E illustrates the down-converted signal 8106 on a compressed time scale. Note that the amplitude of the down-converted signal 8106 is significantly less than the amplitude of the down-converted signal illustrated in FIGS. 80D and 80E. This is due to the higher capacitive value of the holding

capacitance 7808. Generally, as the capacitive value increases, it requires more charge to increase the voltage for a given aperture. Because of the negligible aperture of the pulses 8104 in FIG. 81C, there is insufficient time to transfer significant amounts of energy or charge from the input EM signal 7804 to the holding capacitance 7808. As a result, the amplitudes attained by the holding capacitance 7808 are significantly less than the amplitudes of the down-converted signal illustrated in FIGS. 80D and 80E.

In FIGS. 80E and 80F, the output signal, non-filtered or filtered, cannot provide optimal voltage reproduction, and has relatively negligible power available at the output (e.g.: V^2/R; ~ 150□V and 2KOhms), given the input EM signal 7804 would typically have a driving impedance, in an RF environment, of 50 Ohms (e.g.: V^2/R; ~ 5mV and 50 Ohms).

In summary, under-sampling systems, such as the under-sampling system 7802 illustrated in FIG. 78, are well suited for down-converting EM signals with relatively accurate voltage reproduction. Also, they have a negligible affect on the original input EM signal. As illustrated above, however, the under-sampling systems, such as the under-sampling system 7802 illustrated in FIG. 78, are not well suited for transferring energy or for driving lower impedance loads.

0.1.2 Introduction to Energy Transfer

In an embodiment, the present invention transfers energy from an EM signal by utilizing an energy transfer signal instead of an under-sampling signal. Unlike under-sampling signals that have negligible aperture pulses, the energy transfer signal includes a train of pulses having non-negligible apertures that tend away from zero. This provides more time to transfer energy from an EM input signal. One direct benefit is that the input impedance of the system is reduced so that practical impedance matching circuits can be implemented to further improve energy transfer and thus

overall efficiency. The non-negligible transferred energy significantly improves the signal to noise ratio and sensitivity to very small signals, as well as permitting the down-converted signal to drive lower impedance loads unassisted. Signals that especially benefit include low power ones typified by RF signals. One benefit of a non-negligible aperture is that phase noise within the energy transfer signal does not have as drastic of an effect on the down-converted output signal as under-sampling signal phase noise or conventional sampling signal phase noise does on their respective outputs.

FIG. 82A illustrates an exemplary energy transfer system 8202 for down-converting an input EM signal 8204. The energy transfer system 8202 includes a switching module 8206 and a storage module illustrated as a storage capacitance 8208. The terms storage module and storage capacitance, as used herein, are distinguishable from the terms holding module and holding capacitance, respectively. Holding modules and holding capacitances, as used above, identify systems that store negligible amounts of energy from an under-sampled input EM signal with the intent of "holding" a voltage value. Storage modules and storage capacitances, on the other hand, refer to systems that store non-negligible amounts of energy from an input EM signal.

The energy transfer system 8202 receives an energy transfer signal 8210, which controls the switch module 8206. The energy transfer signal 8210 includes a train of energy transfer pulses having non-negligible pulse widths that tend away from zero time in duration. The non-negligible pulse widths can be any non-negligible amount. For example, the non-negligible pulse widths can be ½ of a period of the input EM signal. Alternatively, the non-negligible pulse widths can be any other fraction of a period of the input EM signal, or a multiple of a period plus a fraction. In an example embodiment, the input EM signal is approximately 900 MHZ and the non-negligible pulse width is approximately 550 pico seconds. Any other suitable non-negligible pulse duration can be used.

In an energy transfer environment, the storage module, illustrated in FIG. 82 as a storage capacitance 8208, preferably has the capacity to handle the power being transferred, and to allow it to accept a non-negligible amount of power during a non-negligible aperture period. This allows the storage capacitance 8208 to store energy transferred from the input EM signal 8204, without substantial concern for accurately reproducing the original, unaffected voltage level of the input EM signal 8204. For example, in an embodiment, the storage capacitance 8208 has a value in the range of 18pF. Other suitable capacitance values and storage modules can be used.

One benefit of the energy transfer system 8202 is that, even when the input EM signal 8204 is a very small signal, the energy transfer system 8202 transfers enough energy from the input EM signal 8204 that the input EM signal can be efficiently down-converted.

The energy transfer system 8202 is coupled to a load 8212. Recall from the overview of under-sampling that loads can be classified as high impedance loads or low impedance loads. A high impedance load is one that is relatively insignificant to an output drive impedance of the system for a given output frequency. A low impedance load is one that is relatively significant. Another benefit of the energy transfer system 8202 is that the non-negligible amounts of transferred energy permit the energy transfer system 8202 to effectively drive loads that would otherwise be classified as low impedance loads in under-sampling systems and conventional sampling systems. In other words, the non-negligible amounts of transferred energy ensure that, even for lower impedance loads, the storage capacitance 8208 accepts and maintains sufficient energy or charge to drive the load 8202. This is illustrated below in the timing diagrams of FIGS. 83A-F.

FIGS. 83A-F illustrate example timing diagrams for the energy transfer system 8202 in FIG. 82. FIG. 83A illustrates an example input EM signal 8302.

FIG. 83C illustrates an example under-sampling signal 8304, including energy transfer pulses 8306 having non-negligible apertures that tend away from zero time in duration.

FIG.83B illustrates the effects to the input EM signal 8302, as measured at a terminal 8214 in FIG. 82A, when non-negligible amounts of energy are transfer from it. In FIG. 83B, non-negligible distortions 8308 correlate with the energy transfer pulses 8306 in FIG. 83C. In this example, the non-negligible distortions 8308 occur at different locations of subsequent cycles of the input EM signal 8302. The non-negligible distortions 8308 represent non-negligible amounts of transferred energy, in the form of charge that is transferred to the storage capacitance 8208 in FIG. 82.

FIG. 83D illustrates a down-converted signal 8310 that is formed by energy transferred from the input EM signal 8302.

FIG. 83E illustrates the down-converted signal 8310 on a compressed time scale. The down-converted signal 8310 can be filtered to produce the down-converted signal 8312 illustrated in FIG. 83F. The down-converted signal 8312 is similar to the down-converted signal illustrated in FIG. 79F, except that the down-converted signal 8312 has substantially more power (e.g.: V^2/R; approximately (~) 2mV and 2K Ohms) than the down-converted signal illustrated in FIG. 79F (e.g.: V^2/R; ~ 5mV and 1M Ohms) . As a result, the down-converted signals 8310 and 8312 can efficiently drive lower impedance loads, given the input EM signal 8204 would typically have a driving impedance, in an RF environment, of 50 Ohms (V^2/R; ~ 5mV and 50 Ohms).

The energy transfer aspects of the invention are represented generally by 4506 in FIGS. 45A and 45B.

1. Down-Converting an EM Signal to an IF EM Signal by Transferring Energy from the EM Signal at an Aliasing Rate

In an embodiment, the invention down-converts an EM signal to an IF signal by transferring energy from the EM signal at an aliasing rate. This embodiment is illustrated by 4514 in FIG. 45B.

This embodiment can be implemented with any type of EM signal, including, but not limited to, modulated carrier signals and unmodulated carrier signals. This embodiment is described herein using the modulated carrier signal F_{MC} in FIG. 1 as an example. In the example, the modulated carrier signal F_{MC} is down-converted to an intermediate frequency (IF) signal F_{IF}. The intermediate frequency signal F_{IF} can be demodulated to a baseband signal F_{DMB} using conventional demodulation techniques. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention can be implemented to down-convert any EM signal, including, but not limited to, modulated carrier signals and unmodulated carrier signals.

The following sections describe methods for down-converting an EM signal to an IF signal F_{IF} by transferring energy from the EM signal at an aliasing rate. Exemplary structural embodiments for implementing the methods are also described. It should be understood that the invention is not limited to the particular embodiments described below. Equivalents, extensions, variations, deviations, etc., of the following will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such equivalents, extensions, variations, deviations, etc., are within the scope and spirit of the present invention.

The following sections include a high level discussion, example embodiments, and implementation examples.

1.1 High Level Description

This section (including its subsections) provides a high-level description of down-converting an EM signal to an IF signal F_{IF} by transferring energy, according to the invention. In particular, an operational process of down-converting the modulated carrier signal F_{MC} to the IF modulated carrier signal F_{IF}, by transferring energy, is described at a high-level. Also, a structural implementation for implementing this process is described at a high-level. This structural implementation is described herein for illustrative purposes, and is not limiting. In particular, the process described in this section can be achieved using any number of structural implementations, one of which is described in this section. The details of such structural implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

1.1.1 Operational Description

FIG. 46B depicts a flowchart 4607 that illustrates an exemplary method for down-converting an EM signal to an intermediate signal F_{IF}, by transferring energy from the EM signal at an aliasing rate. The exemplary method illustrated in the flowchart 4607 is an embodiment of the flowchart 4601 in FIG. 46A.

Any and all combinations of modulation techniques are valid for this invention. For ease of discussion, the digital AM carrier signal 616 is used to illustrate a high level operational description of the invention. Subsequent sections provide detailed flowcharts and descriptions for AM, FM and PM example embodiments. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention can be implemented to down-convert any type of EM signal, including any form of modulated carrier signal and unmodulated carrier signals.

The method illustrated in the flowchart 4607 is now described at a high level using the digital AM carrier signal 616 of FIG. 6C. Subsequent sections provide detailed flowcharts and descriptions for AM, FM and PM example embodiments. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention can be implemented to down-convert any type of EM signal, including any form of modulated carrier signal and unmodulated carrier signals.

The process begins at step 4608, which includes receiving an EM signal. Step 4608 is illustrated by the digital AM carrier signal 616. The digital AM carrier signal 616 of FIG. 6C is re-illustrated in FIG. 47A for convenience. FIG. 47E illustrates a portion of the digital AM carrier signal 616 on an expanded time scale.

Step 4610 includes receiving an energy transfer signal having an aliasing rate F_{AR}. FIG. 47B illustrates an example energy transfer signal 4702. The energy transfer signal 4702 includes a train of energy transfer pulses 4704 having non-negligible apertures 4701 that tend away from zero time duration. Generally, the apertures 4701 can be any time duration other than the period of the EM signal. For example, the apertures 4701 can be greater or less than a period of the EM signal. Thus, the apertures 4701 can be approximately 1/10, ¼, ½, 3/4, etc., or any other fraction of the period of the EM signal. Alternatively, the apertures 4701 can be approximately equal to one or more periods of the EM signal plus 1/10, ¼, ½, 3/4, etc., or any other fraction of a period of the EM signal. The apertures 4701 can be optimized based on one or more of a variety of criteria, as described in sections below.

The energy transfer pulses 4704 repeat at the aliasing rate. A suitable aliasing rate can be determined or selected as described below. Generally, when down-converting an EM signal to an intermediate signal, the aliasing rate is substantially equal to a difference frequency, which is described below,

or substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency.

Step 4612 includes transferring energy from the EM signal at the aliasing rate to down-convert the EM signal to the intermediate signal F_{IF}. FIG. 47C illustrates transferred energy 4706, which is transferred from the EM signal during the energy transfer pulses 4704. Because a harmonic of the aliasing rate occurs at an off-set of the frequency of the AM signal 616, the pulses 4704 "walk through" the AM signal 616 at the off-set frequency. By "walking through" the AM signal 616, the transferred energy 4706 forms an AM intermediate signal 4706 that is similar to the AM carrier signal 616, except that the AM intermediate signal has a lower frequency than the AM carrier signal 616. The AM carrier signal 616 can be down-converted to any frequency below the AM carrier signal 616 by adjusting the aliasing rate F_{AR}, as described below.

FIG. 47D depicts the AM intermediate signal 4706 as a filtered output signal 4708. In an alternative embodiment, the invention outputs a stair step, or non-filtered output signal. The choice between filtered, partially filtered and non-filtered output signals is generally a design choice that depends upon the application of the invention.

The intermediate frequency of the down-converted signal F_{IF}, which, in this example, is the intermediate signal 4706 and 4708, can be determined from EQ. (2), which is reproduced below for convenience.

$$F_C = n \bullet F_{AR} \pm F_{IF} \qquad \text{EQ. (2)}$$

A suitable aliasing rate F_{AR} can be determined in a variety of ways. An example method for determining the aliasing rate F_{AR}, is provided below. After reading the description herein, one skilled in the relevant art(s) will understand how to determine appropriate aliasing rates for EM signals,

including ones in addition to the modulated carrier signals specifically illustrated herein.

In FIG. 48, a flowchart 4801 illustrates an example process for determining an aliasing rate F_{AR}. But a designer may choose, or an application may dictate, that the values be determined in an order that is different than the illustrated order. The process begins at step 4802, which includes determining, or selecting, the frequency of the EM signal. The frequency of the AM carrier signal 616 can be, for example, 901 MHZ.

Step 4804 includes determining, or selecting, the intermediate frequency. This is the frequency to which the EM signal will be down-converted The intermediate frequency can be determined, or selected, to match a frequency requirement of a down-stream demodulator. The intermediate frequency can be, for example, 1 MHZ.

Step 4806 includes determining the aliasing rate or rates that will down-convert the EM signal to the IF specified in step 4804.

EQ. (2) can be rewritten as EQ. (3):

$$n \bullet F_{AR} = F_C \pm F_{IF} \qquad \text{EQ. (3)}$$

Which can be rewritten as EQ. (4):

$$n = \frac{F_C \pm F_{IF}}{F_{AR}} \qquad \text{EQ. (4)}$$

or as EQ. (5):

$$F_{AR} = \frac{F_C \pm F_{IF}}{n} \qquad \text{EQ. (5)}$$

($F_C \pm F_{IF}$) can be defined as a difference value F_{DIFF}, as illustrated in EQ. (6):

$$(F_C \pm F_{IF}) = F_{DIFF} \qquad \text{EQ. (6)}$$

EQ. (4) can be rewritten as EQ. (7):

$$n = \frac{F_{DIFF}}{F_{AR}} \qquad \text{EQ. (7)}$$

From EQ. (7), it can be seen that, for a given n and a constant F_{AR}, F_{DIFF} is constant. For the case of $F_{DIFF} = F_C - F_{IF}$, and for a constant F_{DIFF}, as F_C increases, F_{IF} necessarily increases. For the case of $F_{DIFF} = F_C + F_{IF}$, and for a constant F_{DIFF}, as F_C increases, F_{IF} necessarily decreases. In the latter case of $F_{DIFF} = F_C + F_{IF}$, any phase or frequency changes on F_C correspond to reversed or inverted phase or frequency changes on F_{IF}. This is mentioned to teach the reader that if $F_{DIFF} = F_C + F_{IF}$ is used, the above effect will occur to the phase and frequency response of the modulated intermediate signal F_{IF}.

EQs. (2) through (7) can be solved for any valid n. A suitable n can be determined for any given difference frequency F_{DIFF} and for any desired aliasing rate $F_{AR(Desired)}$. EQs. (2) through (7) can be utilized to identify a specific harmonic closest to a desired aliasing rate $F_{AR(Desired)}$ that will generate the desired intermediate signal F_{IF}.

An example is now provided for determining a suitable n for a given difference frequency F_{DIFF} and for a desired aliasing rate $F_{AR(Desired)}$. For ease of illustration, only the case of ($F_C - F_{IF}$) is illustrated in the example below.

$$n = \frac{F_C - F_{IF}}{F_{AR(Desired)}} = \frac{F_{DIFF}}{F_{AR(Desired)}}$$

The desired aliasing rate $F_{AR(Desired)}$ can be, for example, 140 MHZ. Using the previous examples, where the carrier frequency is 901 MHZ and the IF is 1 MHZ, an initial value of n is determined as:

$$n = \frac{901\ \text{MHZ} - 1\ \text{MHZ}}{140\ \text{MHZ}} = \frac{900}{140} = 6.4$$

The initial value 6.4 can be rounded up or down to the valid nearest n, which was defined above as including (0.5, 1, 2, 3, . . .). In this example, 6.4 is rounded down to 6.0, which is inserted into EQ. (5) for the case of $(F_C - F_{IF}) = F_{DIFF}$.:

$$F_{AR} = \frac{F_c - F_{IF}}{n}$$

$$F_{AR} = \frac{901\ \text{MHZ} - 1\ \text{MHZ}}{6} = \frac{900\ \text{MHZ}}{6} = 150\ \text{MHZ}$$

In other words, transferring energy from a 901 MHZ EM carrier signal at 150 MHZ generates an intermediate signal at 1 MHZ. When the EM carrier signal is a modulated carrier signal, the intermediate signal will also substantially include the modulation. The modulated intermediate signal can be demodulated through any conventional demodulation technique.

Alternatively, instead of starting from a desired aliasing rate, a list of suitable aliasing rates can be determined from the modified form of EQ. (5), by solving for various values of n. Example solutions are listed below.

$$F_{AR} = \frac{(F_C - F_{IF})}{n} = \frac{F_{DIFF}}{n} = \frac{901\ \text{MHZ} - 1\ \text{MHZ}}{n} = \frac{900\ \text{MHZ}}{n}$$

Solving for n = 0.5, 1, 2, 3, 4, 5 and 6:

900MHZ/0.5 = 1.8 GHZ (i.e., second harmonic);

900MHZ/1 = 900 MHZ (i.e., fundamental frequency);

900MHZ/2 = 450 MHZ (i.e., second sub-harmonic);
900MHZ/3 = 300 MHZ (i.e., third sub-harmonic);
900MHZ/4 = 225 MHZ (i.e., fourth sub-harmonic);
900 MHZ/5 = 180 MHZ(i.e., fifth sub-harmonic); and
900 MHZ/6 = 150 MHZ(i.e., sixth sub-harmonic).

The steps described above can be performed for the case of (F_C+F_{IF}) in a similar fashion. The results can be compared to the results obtained from the case of (F_C-F_{IF}) to determine which provides better result for an application.

In an embodiment, the invention down-converts an EM signal to a relatively standard IF in the range of, for example, 100KHZ to 200 MHZ. In another embodiment, referred to herein as a small off-set implementation, the invention down-converts an EM signal to a relatively low frequency of, for example, less than 100 KHZ. In another embodiment, referred to herein as a large off-set implementation, the invention down-converts an EM signal to a relatively higher IF signal, such as, for example, above 200 MHZ.

The various off-set implementations provide selectivity for different applications. Generally, lower data rate applications can operate at lower intermediate frequencies. But higher intermediate frequencies can allow more information to be supported for a given modulation technique.

In accordance with the invention, a designer picks an optimum information bandwidth for an application and an optimum intermediate frequency to support the baseband signal. The intermediate frequency should be high enough to support the bandwidth of the modulating baseband signal F_{MB}.

Generally, as the aliasing rate approaches a harmonic or sub-harmonic frequency of the EM signal, the frequency of the down-converted IF signal decreases. Similarly, as the aliasing rate moves away from a harmonic or sub-harmonic frequency of the EM signal, the IF increases.

Aliased frequencies occur above and below every harmonic of the aliasing frequency. In order to avoid mapping other aliasing frequencies in the band of the aliasing frequency (IF) of interest, the IF of interest should not be near one half the aliasing rate.

As described in example implementations below, an aliasing module, including a universal frequency translator (UFT) module built in accordance with the invention provides a wide range of flexibility in frequency selection and can thus be implemented in a wide range of applications. Conventional systems cannot easily offer, or do not allow, this level of flexibility in frequency selection.

1.1.2 Structural Description

FIG. 63 illustrates a block diagram of an energy transfer system 6302 according to an embodiment of the invention. The energy transfer system 6302 is an example embodiment of the generic aliasing system 1302 in FIG. 13. The energy transfer system 6302 includes an energy transfer module 6304. The energy transfer module 6304 receives the EM signal 1304 and an energy transfer signal 6306, which includes a train of energy transfer pulses having non-negligible apertures that tend away from zero time in duration, occurring at a frequency equal to the aliasing rate F_{AR}. The energy transfer signal 6306 is an example embodiment of the aliasing signal 1310 in FIG. 13. The energy transfer module 6304 transfers energy from the EM signal 1304 at the aliasing rate F_{AR} of the energy transfer signal 6306.

Preferably, the energy transfer module 6304 transfers energy from the EM signal 1304 to down-convert it to the intermediate signal F_{IF} in the manner shown in the operational flowchart 4607 of FIG. 46B. But it should be understood that the scope and spirit of the invention includes other structural embodiments for performing the steps of the flowchart 4607. The specifics of

the other structural embodiments will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

The operation of the energy transfer system 6302 is now described in detail with reference to the flowchart 4607 and to the timing diagrams illustrated in FIGS. 47A-E. In step 4608, the energy transfer module 6304 receives the AM carrier signal 616. In step 4610, the energy transfer module 6304 receives the energy transfer signal 4702. In step 4612, the energy transfer module 6304 transfers energy from the AM carrier signal 616 at the aliasing rate to down-convert the AM carrier signal 616 to the intermediate signal 4706 or 4708.

Example implementations of the energy transfer system 6302 are provided in Sections 4 and 5 below.

1.2 Example Embodiments

Various embodiments related to the method(s) and structure(s) described above are presented in this section (and its subsections). These embodiments are described herein for purposes of illustration, and not limitation. The invention is not limited to these embodiments. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

The method for down-converting the EM signal 1304 by transferring energy can be implemented with any type of EM signal, including modulated carrier signals and unmodulated carrier signals. For example, the method of the flowchart 4601 can be implemented to down-convert AM signals, FM signals, PM signals, etc., or any combination thereof. Operation of the flowchart 4601 of FIG. 46A is described below for down-converting AM, FM and PM. The down-conversion descriptions include down-converting to

intermediate signals, directly down-converting to demodulated baseband signals, and down-converting FM signals to non-FM signals. The exemplary descriptions below are intended to facilitate an understanding of the present invention. The present invention is not limited to or by the exemplary embodiments below.

1.2.1 First Example Embodiment: Amplitude Modulation

1.2.1.1 Operational Description

Operation of the exemplary process of the flowchart 4607 in FIG. 46B is described below for the analog AM carrier signal 516, illustrated in FIG. 5C, and for the digital AM carrier signal 616, illustrated in FIG. 6C.

1.2.1.1.1 Analog AM Carrier Signal

A process for down-converting the analog AM carrier signal 516 in FIG. 5C to an analog AM intermediate signal is now described for the flowchart 4607 in FIG. 46B. The analog AM carrier signal 516 is re-illustrated in FIG. 50A for convenience. For this example, the analog AM carrier signal 516 oscillates at approximately 901 MHZ. In FIG. 50B, an analog AM carrier signal 5004 illustrates a portion of the analog AM carrier signal 516 on an expanded time scale.

The process begins at step 4608, which includes receiving the EM signal. This is represented by the analog AM carrier signal 516.

Step 4610 includes receiving an energy transfer signal having an aliasing rate F_{AR}. FIG. 50C illustrates an example energy transfer signal 5006 on approximately the same time scale as FIG. 50B. The energy transfer signal 5006 includes a train of energy transfer pulses 5007 having non-negligible apertures 5009 that tend away from zero time in duration. The energy transfer

pulses 5007 repeat at the aliasing rate F_{AR}, which is determined or selected as previously described. Generally, when down-converting to an intermediate signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency F_{DIFF}.

Step 4612 includes transferring energy from the EM signal at the aliasing rate to down-convert the EM signal to an intermediate signal F_{IF}. In FIG. 50D, an affected analog AM carrier signal 5008 illustrates effects of transferring energy from the analog AM carrier signal 516 at the aliasing rate F_{AR}. The affected analog AM carrier signal 5008 is illustrated on substantially the same time scale as FIGS. 50B and 50C.

FIG 50E illustrates a down-converted AM intermediate signal 5012, which is generated by the down-conversion process. The AM intermediate signal 5012 is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

The down-converted signal 5012 includes portions 5010A, which correlate with the energy transfer pulses 5007 in FIG. 50C, and portions 5010B, which are between the energy transfer pulses 5007. Portions 5010A represent energy transferred from the AM analog signal 516 to a storage device, while simultaneously driving an output load. The portions 5010A occur when a switching module is closed by the energy transfer pulses 5007. Portions 5010B represent energy stored in a storage device continuing to drive the load. Portions 5010B occur when the switching module is opened after energy transfer pulses 5007.

Because a harmonic of the aliasing rate is off-set from the analog AM carrier signal 516, the energy transfer pulses 5007 "walk through" the analog AM carrier signal 516 at the difference frequency F_{DIFF}. In other words, the energy transfer pulses 5007 occur at different locations of subsequent cycles of the AM carrier signal 516. As a result, the energy transfer pulses 5007 capture varying amounts of energy from the analog AM carrier signal 516, as

illustrated by portions 5010A, which provides the AM intermediate signal 5012 with an oscillating frequency F_{IF}.

In FIG. 50F, an AM intermediate signal 5014 illustrates the AM intermediate signal 5012 on a compressed time scale. In FIG. 50G, an AM intermediate signal 5016 represents a filtered version of the AM intermediate signal 5014. The AM intermediate signal 5016 is substantially similar to the AM carrier signal 516, except that the AM intermediate signal 5016 is at the intermediate frequency. The AM intermediate signal 5016 can be demodulated through any conventional demodulation technique.

The present invention can output the unfiltered AM intermediate signal 5014, the filtered AM intermediate signal 5016, a partially filtered AM intermediate signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention.

The signals referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the AM intermediate signals 5014 in FIG. 50F and 5016 in FIG. 50G illustrate that the AM carrier signal 516 was successfully down-converted to an intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.1.1.2 Digital AM Carrier Signal

A process for down-converting the digital AM carrier signal 616 to a digital AM intermediate signal is now described for the flowchart 4607 in FIG. 46B. The digital AM carrier signal 616 is re-illustrated in FIG. 51A for convenience. For this example, the digital AM carrier signal 616 oscillates at approximately 901 MHZ. In FIG. 51B, a digital AM carrier signal 5104 illustrates a portion of the digital AM carrier signal 616 on an expanded time scale.

The process begins at step 4608, which includes receiving an EM signal. This is represented by the digital AM carrier signal 616.

Step 4610 includes receiving an energy transfer signal having an aliasing rate F_{AR}. FIG. 51C illustrates an example energy transfer signal 5106 on substantially the same time scale as FIG. 51B. The energy transfer signal 5106 includes a train of energy transfer pulses 5107 having non-negligible apertures 5109 that tend away from zero time in duration. The energy transfer pulses 5107 repeat at the aliasing rate, which is determined or selected as previously described. Generally, when down-converting to an intermediate signal, the aliasing rate is substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency F_{DIFF}.

Step 4612 includes transferring energy from the EM signal at the aliasing rate to down-convert the EM signal to the intermediate signal F_{IF}. In FIG. 51D, an affected digital AM carrier signal 5108 illustrates effects of transferring energy from the digital AM carrier signal 616 at the aliasing rate F_{AR}. The affected digital AM carrier signal 5108 is illustrated on substantially the same time scale as FIGS. 51B and 51C.

FIG 51E illustrates a down-converted AM intermediate signal 5112, which is generated by the down-conversion process. The AM intermediate signal 5112 is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

The down-converted signal 5112 includes portions 5110A, which correlate with the energy transfer pulses 5107 in FIG. 51C, and portions 5110B, which are between the energy transfer pulses 5107. Portions 5110A represent energy transferred from the digital AM carrier signal 616 to a storage device, while simultaneously driving an output load. The portions 5110A occur when a switching module is closed by the energy transfer pulses 5107. Portions 5110B represent energy stored in a storage device continuing to drive

the load. Portions 5110B occur when the switching module is opened after energy transfer pulses 5107.

Because a harmonic of the aliasing rate is off-set from the frequency of the digital AM carrier signal 616, the energy transfer pulses 5107 "walk through" the digital AM signal 616 at the difference frequency F_{DIFF}. In other words, the energy transfer pulse 5107 occur at different locations of subsequent cycles of the digital AM carrier signal 616. As a result, the energy transfer pulses 5107 capture varying amounts of energy from the digital AM carrier signal 616, as illustrated by portions 5110, which provides the AM intermediate signal 5112 with an oscillating frequency F_{IF}.

In FIG. 51F, a digital AM intermediate signal 5114 illustrates the AM intermediate signal 5112 on a compressed time scale. In FIG. 51G, an AM intermediate signal 5116 represents a filtered version of the AM intermediate signal 5114. The AM intermediate signal 5116 is substantially similar to the AM carrier signal 616, except that the AM intermediate signal 5116 is at the intermediate frequency. The AM intermediate signal 5116 can be demodulated through any conventional demodulation technique.

The present invention can output the unfiltered AM intermediate signal 5114, the filtered AM intermediate signal 5116, a partially filtered AM intermediate signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention.

The signals referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the AM intermediate signals 5114 in FIG. 51F and 5116 in FIG. 51G illustrate that the AM carrier signal 616 was successfully down-converted to an intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.1.2 Structural Description

The operation of the energy transfer system 6302 is now described for the analog AM carrier signal 516, with reference to the flowchart 4607 and to the timing diagrams in FIGS. 50A-G. In step 4608, the energy transfer module 6304 receives the analog AM carrier signal 516. In step 4610, the energy transfer module 6304 receives the energy transfer signal 5006. In step 4612, the energy transfer module 6304 transfers energy from the analog AM carrier signal 516 at the aliasing rate of the energy transfer signal 5006, to down-convert the analog AM carrier signal 516 to the AM intermediate signal 5012.

The operation of the energy transfer system 6302 is now described for the digital AM carrier signal 616, with reference to the flowchart 1401 and the timing diagrams in FIGS. 51A-G. In step 4608, the energy transfer module 6304 receives the digital AM carrier signal 616. In step 4610, the energy transfer module 6304 receives the energy transfer signal 5106. In step 4612, the energy transfer module 6304 transfers energy from the digital AM carrier signal 616 at the aliasing rate of the energy transfer signal 5106, to down-convert the digital AM carrier signal 616 to the AM intermediate signal 5112.

Example embodiments of the energy transfer module 6304 are disclosed in Sections 4 and 5 below.

1.2.2 Second Example Embodiment: Frequency Modulation

1.2.2.1 Operational Description

Operation of the exemplary process of the flowchart 4607 in FIG. 46B is described below for the analog FM carrier signal 716, illustrated in FIG. 7C, and for the digital FM carrier signal 816, illustrated in FIG. 8C.

1.2.2.1.1 Analog FM Carrier Signal

A process for down-converting the analog FM carrier signal 716 in FIG. 7C to an FM intermediate signal is now described for the flowchart 4607 in FIG. 46B. The analog FM carrier signal 716 is re-illustrated in FIG. 52A for convenience. For this example, the analog FM carrier signal 716 oscillates around approximately 901 MHZ. In FIG. 52B, an analog FM carrier signal 5204 illustrates a portion of the analog FM carrier signal 716 on an expanded time scale.

The process begins at step 4608, which includes receiving an EM signal. This is represented by the analog FM carrier signal 716.

Step 4610 includes receiving an energy transfer signal having an aliasing rate F_{AR}. FIG. 52C illustrates an example energy transfer signal 5206 on approximately the same time scale as FIG. 52B. The energy transfer signal 5206 includes a train of energy transfer pulses 5207 having non-negligible apertures that tend away from zero time in duration. The energy transfer pulses 5207 repeat at the aliasing rate F_{AR}, which is determined or selected as previously described. Generally, when down- converting to an intermediate signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency F_{DIFF}.

Step 4612 includes transferring energy from the EM signal at the aliasing rate to down-convert the EM signal to an intermediate signal F_{IF}. In FIG. 52D, an affected analog FM carrier signal 5208 illustrates effects of transferring energy from the analog FM carrier signal 716 at the aliasing rate F_{AR}. The affected analog FM carrier signal 5208 is illustrated on substantially the same time scale as FIGS. 52B and 52C.

FIG 52E illustrates a down-converted FM intermediate signal 5212, which is generated by the down-conversion process. The FM intermediate signal 5212 is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

The down-converted signal 5212 includes portions 5210A, which correlate with the energy transfer pulses 5207 in FIG. 52C, and portions 5210B, which are between the energy transfer pulses 5207. Portions 5210A represent energy transferred from the analog FM carrier signal 716 to a storage device, while simultaneously driving an output load. The portions 5210A occur when a switching module is closed by the energy transfer pulses 5207. Portions 5210B represent energy stored in a storage device continuing to drive the load. Portions 5210B occur when the switching module is opened after energy transfer pulses 5207.

Because a harmonic of the aliasing rate is off-set from the frequency of the analog FM carrier signal 716, the energy transfer pulses 5207 "walk through" the analog FM carrier signal 716 at the difference frequency F_{DIFF}. In other words, the energy transfer pulse 5207 occur at different locations of subsequent cycles of the analog FM carrier signal 716. As a result, the energy transfer pulses 5207 capture varying amounts of energy from the analog FM carrier signal 716, as illustrated by portions 5210, which provides the FM intermediate signal 5212 with an oscillating frequency F_{IF}.

In FIG. 52F, an analog FM intermediate signal 5214 illustrates the FM intermediate signal 5212 on a compressed time scale. In FIG. 52G, an FM intermediate signal 5216 represents a filtered version of the FM intermediate signal 5214. The FM intermediate signal 5216 is substantially similar to the analog FM carrier signal 716, except that the FM intermediate signal 5216 is at the intermediate frequency. The FM intermediate signal 5216 can be demodulated through any conventional demodulation technique.

The present invention can output the unfiltered FM intermediate signal 5214, the filtered FM intermediate signal 5216, a partially filtered FM intermediate signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention.

The signals referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the FM intermediate signals 5214 in FIG. 52F and 5216 in FIG. 52G illustrate that the FM carrier signal 716 was successfully down-converted to an intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.2.1.2 Digital FM Carrier Signal

A process for down-converting the digital FM carrier signal 816 in FIG. 8C is now described for the flowchart 4607 in FIG. 46B. The digital FM carrier signal 816 is re-illustrated in FIG. 53A for convenience. For this example, the digital FM carrier signal 816 oscillates at approximately 901 MHZ. In FIG. 53B, a digital FM carrier signal 5304 illustrates a portion of the digital FM carrier signal 816 on an expanded time scale.

The process begins at step 4608, which includes receiving an EM signal. This is represented by the digital FM carrier signal 816.

Step 4610 includes receiving an energy transfer signal having an aliasing rate F_{AR}. FIG. 53C illustrates an example energy transfer signal 5306 on substantially the same time scale as FIG. 53B. The energy transfer signal 5306 includes a train of energy transfer pulses 5307 having non-negligible apertures 5309 that tend away from zero time in duration. The energy transfer pulses 5307 repeat at the aliasing rate, which is determined or selected as previously described. Generally, when down-converting to an intermediate signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency F_{DIFF}.

Step 4612 includes transferring energy from the EM signal at the aliasing rate to down-convert the EM signal to the an intermediate signal F_{IF}. In FIG. 53D, an affected digital FM carrier signal 5308 illustrates effects of transferring energy from the digital FM carrier signal 816 at the aliasing rate

F_{AR}. The affected digital FM carrier signal 5308 is illustrated on substantially the same time scale as FIGS. 53B and 53C.

FIG 53E illustrates a down-converted FM intermediate signal 5312, which is generated by the down-conversion process. The down-converted signal 5312 includes portions 5310A, which correlate with the energy transfer pulses 5307 in FIG. 53C, and portions 5310B, which are between the energy transfer pulses 5307. Down-converted signal 5312 is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

Portions 5310A represent energy transferred from the digital FM carrier signal 816 to a storage device, while simultaneously driving an output load. The portions 5310A occur when a switching module is closed by the energy transfer pulses 5307.

Portions 5310B represent energy stored in a storage device continuing to drive the load. Portions 5310B occur when the switching module is opened after energy transfer pulses 5307.

Because a harmonic of the aliasing rate is off-set from the frequency of the digital FM carrier signal 816, the energy transfer pulses 5307 "walk through" the digital FM carrier signal 816 at the difference frequency F_{DIFF}. In other words, the energy transfer pulse 5307 occur at different locations of subsequent cycles of the digital FM carrier signal 816. As a result, the energy transfer pulses 5307 capture varying amounts of energy from the digital FM carrier signal 816, as illustrated by portions 5310, which provides the FM intermediate signal 5312 with an oscillating frequency F_{IF}.

In FIG. 53F, a digital FM intermediate signal 5314 illustrates the FM intermediate signal 5312 on a compressed time scale. In FIG. 53G, an FM intermediate signal 5316 represents a filtered version of the FM intermediate signal 5314. The FM intermediate signal 5316 is substantially similar to the digital FM carrier signal 816, except that the FM intermediate signal 5316 is at

the intermediate frequency. The FM intermediate signal 5316 can be demodulated through any conventional demodulation technique.

The present invention can output the unfiltered FM intermediate signal 5314, the filtered FM intermediate signal 5316, a partially filtered FM intermediate signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention.

The signals referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the FM intermediate signals 5314 in FIG. 53F and 5316 in FIG. 53G illustrate that the FM carrier signal 816 was successfully down-converted to an intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.2.2 Structural Description

The operation of the energy transfer system 6302 is now described for the analog FM carrier signal 716, with reference to the flowchart 4607 and the timing diagrams in FIGS. 52A-G. In step 4608, the energy transfer module 6304 receives the analog FM carrier signal 716. In step 4610, the energy transfer module 6304 receives the energy transfer signal 5206. In step 4612, the energy transfer module 6304 transfers energy from the analog FM carrier signal 716 at the aliasing rate of the energy transfer signal 5206, to down-convert the analog FM carrier signal 716 to the FM intermediate signal 5212.

The operation of the energy transfer system 6302 is now described for the digital FM carrier signal 816, with reference to the flowchart 4607 and the timing diagrams in FIGS. 53A-G. In step 4608, the energy transfer module 6304 receives the digital FM carrier signal 816. In step 4610, the energy transfer module 6304 receives the energy transfer signal 5306. In step 4612, the energy transfer module 6304 transfers energy from the digital FM carrier

signal 816 at the aliasing rate of the energy transfer signal 5306, to down-convert the digital FM carrier signal 816 to the FM intermediate signal 5212.

Example embodiments of the energy transfer module 6304 are disclosed in Sections 4 and 5 below.

1.2.3 Third Example Embodiment: Phase Modulation

1.2.3.1 Operational Description

Operation of the exemplary process of the flowchart 4607 in FIG. 46B is described below for the analog PM carrier signal 916, illustrated in FIG. 9C, and for the digital PM carrier signal 1016, illustrated in FIG. 10C.

1.2.3.1.1 Analog PM Carrier Signal

A process for down-converting the analog PM carrier signal 916 in FIG. 9C to an analog PM intermediate signal is now described for the flowchart 4607 in FIG. 46B. The analog PM carrier signal 916 is re-illustrated in FIG. 54A for convenience. For this example, the analog PM carrier signal 916 oscillates at approximately 901 MHZ. In FIG. 54B, an analog PM carrier signal 5404 illustrates a portion of the analog PM carrier signal 916 on an expanded time scale.

The process begins at step 4608, which includes receiving an EM signal. This is represented by the analog PM carrier signal 916.

Step 4610 includes receiving an energy transfer signal having an aliasing rate F_{AR}. FIG. 54C illustrates an example energy transfer signal 5406 on approximately the same time scale as FIG. 54B. The energy transfer signal 5406 includes a train of energy transfer pulses 5407 having non-negligible apertures that tend away from zero time in duration. The energy transfer pulses 5407 repeat at the aliasing rate, which is determined or selected as

previously described. Generally, when down-converting to an intermediate signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency F_{DIFF}.

Step 4612 includes transferring energy from the EM signal at the aliasing rate to down-convert the EM signal to the IF signal F_{IF}. In FIG. 54D, an affected analog PM carrier signal 5408 illustrates effects of transferring energy from the analog PM carrier signal 916 at the aliasing rate F_{AR}. The affected analog PM carrier signal 5408 is illustrated on substantially the same time scale as FIGS. 54B and 54C.

FIG 54E illustrates a down-converted PM intermediate signal 5412, which is generated by the down-conversion process. The down-converted PM intermediate signal 5412 includes portions 5410A, which correlate with the energy transfer pulses 5407 in FIG. 54C, and portions 5410B, which are between the energy transfer pulses 5407. Down-converted signal 5412 is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

Portions 5410A represent energy transferred from the analog PM carrier signal 916 to a storage device, while simultaneously driving an output load. The portions 5410A occur when a switching module is closed by the energy transfer pulses 5407.

Portions 5410B represent energy stored in a storage device continuing to drive the load. Portions 5410B occur when the switching module is opened after energy transfer pulses 5407.

Because a harmonic of the aliasing rate is off-set from the frequency of the analog PM carrier signal 716, the energy transfer pulses 5407 "walk through" the analog PM carrier signal 916 at the difference frequency F_{DIFF}. In other words, the energy transfer pulse 5407 occur at different locations of subsequent cycles of the analog PM carrier signal 916. As a result, the energy transfer pulses 5407 capture varying amounts of energy from the analog PM

carrier signal 916, as illustrated by portions 5410, which provides the PM intermediate signal 5412 with an oscillating frequency F_{IF}.

In FIG. 54F, an analog PM intermediate signal 5414 illustrates the PM intermediate signal 5412 on a compressed time scale. In FIG. 54G, an PM intermediate signal 5416 represents a filtered version of the PM intermediate signal 5414. The PM intermediate signal 5416 is substantially similar to the analog PM carrier signal 916, except that the PM intermediate signal 5416 is at the intermediate frequency. The PM intermediate signal 5416 can be demodulated through any conventional demodulation technique.

The present invention can output the unfiltered PM intermediate signal 5414, the filtered PM intermediate signal 5416, a partially filtered PM intermediate signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention.

The signals referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the PM intermediate signals 5414 in FIG. 54F and 5416 in FIG. 54G illustrate that the PM carrier signal 916 was successfully down-converted to an intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.3.1.2 Digital PM Carrier Signal

A process for down-converting the digital PM carrier signal 1016 in FIG. 10C to a digital PM signal is now described for the flowchart 3607 in FIG. 46B. The digital PM carrier signal 1016 is re-illustrated in FIG. 55A for convenience. For this example, the digital PM carrier signal 1016 oscillates at approximately 901 MHZ. In FIG. 55B, a digital PM carrier signal 5504 illustrates a portion of the digital PM carrier signal 1016 on an expanded time scale.

The process begins at step 4608, which includes receiving an EM signal. This is represented by the digital PM carrier signal 1016.

Step 4610 includes receiving an energy transfer signal having an aliasing rate F_{AR}. FIG. 55C illustrates an example energy transfer signal 5506 on substantially the same time scale as FIG. 55B. The energy transfer signal 5506 includes a train of energy transfer pulses 5507 having non-negligible apertures 5509 that tend away from zero time in duration. The energy transfer pulses 5507 repeat at an aliasing rate, which is determined or selected as previously described. Generally, when down-converting to an intermediate signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency F_{DIFF}.

Step 4612 includes transferring energy from the EM signal at the aliasing rate to down-convert the EM signal to an intermediate signal F_{IF}. In FIG. 55D, an affected digital PM carrier signal 5508 illustrates effects of transferring energy from the digital PM carrier signal 1016 at the aliasing rate F_{AR}. The affected digital PM carrier signal 5508 is illustrated on substantially the same time scale as FIGS. 55B and 55C.

FIG 55E illustrates a down-converted PM intermediate signal 5512, which is generated by the down-conversion process. The down-converted PM intermediate signal 5512 includes portions 5510A, which correlate with the energy transfer pulses 5507 in FIG. 55C, and portions 5510B, which are between the energy transfer pulses 5507. Down-converted signal 5512 is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

Portions 5510A represent energy transferred from the digital PM carrier signal 1016 to a storage device, while simultaneously driving an output load. The portions 5510A occur when a switching module is closed by the energy transfer pulses 5507.

Portions 5510B represent energy stored in a storage device continuing to drive the load. Portions 5510B occur when the switching module is opened after energy transfer pulses 5507.

Because a harmonic of the aliasing rate is off-set from the frequency of the digital PM carrier signal 716, the energy transfer pulses 5507 "walk through" the digital PM carrier signal 1016 at the difference frequency F_{DIFF}. In other words, the energy transfer pulse 5507 occur at different locations of subsequent cycles of the digital PM carrier signal 1016. As a result, the energy transfer pulses 5507 capture varying amounts of energy from the digital PM carrier signal 1016, as illustrated by portions 5510, which provides the PM intermediate signal 5512 with an oscillating frequency F_{IF}.

In FIG. 55F, a digital PM intermediate signal 5514 illustrates the PM intermediate signal 5512 on a compressed time scale. In FIG. 55G, an PM intermediate signal 5516 represents a filtered version of the PM intermediate signal 5514. The PM intermediate signal 5516 is substantially similar to the digital PM carrier signal 1016, except that the PM intermediate signal 5516 is at the intermediate frequency. The PM intermediate signal 5516 can be demodulated through any conventional demodulation technique.

The present invention can output the unfiltered PM intermediate signal 5514, the filtered PM intermediate signal 5516, a partially filtered PM intermediate signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention.

The signals referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the PM intermediate signals 5514 in FIG. 55F and 5516 in FIG. 55G illustrate that the PM carrier signal 1016 was successfully down-converted to an intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.3.2 Structural Description

Operation of the energy transfer system 6302 is now described for the analog PM carrier signal 916, with reference to the flowchart 4607 and the timing diagrams in FIGS. 54A-G. In step 4608, the energy transfer module 6304 receives the analog PM carrier signal 916. In step 4610, the energy transfer module 6304 receives the energy transfer signal 5406. In step 4612, the energy transfer module 6304 transfers energy from the analog PM carrier signal 916 at the aliasing rate of the energy transfer signal 5406, to down-convert the analog PM carrier signal 916 to the PM intermediate signal 5412.

Operation of the energy transfer system 6302 is now described for the digital PM carrier signal 1016, with reference to the flowchart 1401 and the timing diagrams in FIGS. 55A-G. In step 4608, the energy transfer module 6304 receives the digital PM carrier signal 1016. In step 4610, the energy transfer module 6304 receives the energy transfer signal 5506. In step 4612, the energy transfer module 6304 transfers energy from the digital PM carrier signal 1016 at the aliasing rate of the energy transfer signal 5506, to down-convert the digital PM carrier signal 1016 to the PM intermediate signal 5512.

Example embodiments of the energy transfer module 6304 are disclosed in Sections 4 and 5 below.

1.2.4 Other Embodiments

The embodiments described above are provided for purposes of illustration. These embodiments are not intended to limit the invention. Alternate embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate embodiments fall within the scope and spirit of the present invention. Example implementations of the energy transfer module 6304 are disclosed in Sections 4 and 5 below.

1.3 Implementation Examples

Exemplary operational and/or structural implementations related to the method(s), structure(s), and/or embodiments described above are presented in Sections 4 and 5 below. These implementations are presented for purposes of illustration, and not limitation. The invention is not limited to the particular implementation examples described therein. Alternate implementations (including equivalents, extensions, variations, deviations, etc., of those described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

2. Directly Down-Converting an EM Signal to an Demodulated Baseband Signal by Transferring Energy from the EM Signal

In an embodiment, the invention directly down-converts an EM signal to a baseband signal, by transferring energy from the EM signal. This embodiment is referred to herein as direct-to-data down-conversion and is illustrated by 4516 in FIG. 45B.

This embodiment can be implemented with modulated and unmodulated EM signals. This embodiment is described herein using the modulated carrier signal F_{MC} in FIG. 1, as an example. In the example, the modulated carrier signal F_{MC} is directly down-converted to the demodulated baseband signal F_{DMB}. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention can be implemented to down-convert any EM signal, including but not limited to, modulated carrier signals and unmodulated carrier signals.

The following sections describe methods for directly down-converting the modulated carrier signal F_{MC} to the demodulated baseband signal F_{DMB}. Exemplary structural embodiments for implementing the methods are also

described. It should be understood that the invention is not limited to the particular embodiments described below. Equivalents, extensions, variations, deviations, etc., of the following will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such equivalents, extensions, variations, deviations, etc., are within the scope and spirit of the present invention.

The following sections include a high level discussion, example embodiments, and implementation examples.

2.1 High Level Description

This section (including its subsections) provides a high-level description of transferring energy from the modulated carrier signal F_{MC} to directly down-convert the modulated carrier signal F_{MC} to the demodulated baseband signal F_{DMB}, according to the invention. In particular, an operational process of directly down-converting the modulated carrier signal F_{MC} to the demodulated baseband signal F_{DMB} is described at a high-level. Also, a structural implementation for implementing this process is described at a high-level. The structural implementation is described herein for illustrative purposes, and is not limiting. In particular, the process described in this section can be achieved using any number of structural implementations, one of which is described in this section. The details of such structural implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

2.1.1 Operational Description

FIG. 46C depicts a flowchart 4613 that illustrates an exemplary method for transferring energy from the modulated carrier signal F_{MC} to directly down-convert the modulated carrier signal F_{MC} to the demodulated baseband signal

F_{DMB}. The exemplary method illustrated in the flowchart 4613 is an embodiment of the flowchart 4601 in FIG. 46A.

Any and all combinations of modulation techniques are valid for this invention. For ease of discussion, the digital AM carrier signal 616 is used to illustrate a high level operational description of the invention. Subsequent sections provide detailed flowcharts and descriptions for AM and PM example embodiments. FM presents special considerations that are dealt with separately in Section III.3. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention can be implemented to down-convert any type of EM signal, including any form of modulated carrier signal and unmodulated carrier signals.

The high-level process illustrated in the flowchart 4613 is now described at a high level using the digital AM carrier signal 616, from FIG. 6C. The digital AM carrier signal 616 is re-illustrated in FIG. 56A for convenience.

The process of the flowchart 4613 begins at step 4614, which includes receiving an EM signal. Step 4613 is represented by the digital AM carrier signal 616.

Step 4616 includes receiving an energy transfer signal having an aliasing rate F_{AR}. FIG. 56B illustrates an example energy transfer signal 5602, which includes a train of energy transfer pulses 5604 having apertures 5606 that are optimized for energy transfer. The optimized apertures 5606 are non-negligible and tend away from zero.

The non-negligible apertures 5606 can be any width other than the period of the EM signal, or a multiple thereof. For example, the non-negligible apertures 5606 can be less than the period of the signal 616 such as, 1/8, ¼, ½, 3/4, etc., of the period of the signal 616. Alternatively, the non-negligible apertures 5606 can be greater than the period of the signal 616. The

width and amplitude of the apertures 5606 can be optimized based on one or more of a variety of criteria, as described in sections below.

The energy transfer pulses 5604 repeat at the aliasing rate or pulse repetition rate. The aliasing rate is determined in accordance with EQ. (2), reproduced below for convenience.

$$F_C = n \bullet F_{AR} \pm F_{IF} \qquad \text{EQ. (2)}$$

When directly down-converting an EM signal to baseband (i.e., zero IF), EQ. (2) becomes:

$$F_C = n \bullet F_{AR} \qquad \text{EQ. (8)}$$

Thus, to directly down-convert the AM signal 616 to a demodulated baseband signal, the aliasing rate is substantially equal to the frequency of the AM signal 616 or to a harmonic or sub-harmonic thereof. Although the aliasing rate is too low to permit reconstruction of higher frequency components of the AM signal 616 (i.e., the carrier frequency), it is high enough to permit substantial reconstruction of the lower frequency modulating baseband signal 310.

Step 4618 includes transferring energy from the EM signal at the aliasing rate to directly down-convert the EM signal to a demodulated baseband signal $F_{DMB.}$ FIG. 56C illustrates a demodulated baseband signal 5610 that is generated by the direct down-conversion process. The demodulated baseband signal 5610 is similar to the digital modulating baseband signal 310 in FIG. 3.

FIG. 56D depicts a filtered demodulated baseband signal 5612, which can be generated from the demodulated baseband signal 5610. The invention can thus generate a filtered output signal, a partially filtered output signal, or a relatively unfiltered output signal. The choice between filtered, partially

filtered and non-filtered output signals is generally a design choice that depends upon the application of the invention.

2.1.2 Structural Description

In an embodiment, the energy transfer system 6302 transfers energy from any type of EM signal, including modulated carrier signals and unmodulated carrier signal, to directly down-convert the EM signal to a demodulated baseband signal. Preferably, the energy transfer system 6302 transfers energy from the EM signal 1304 to down-convert it to demodulated baseband signal in the manner shown in the operational flowchart 4613. However, it should be understood that the scope and spirit of the invention includes other structural embodiments for performing the steps of the flowchart 4613. The specifics of the other structural embodiments will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

Operation of the energy transfer system 6302 is now described in at a high level for the digital AM carrier signal 616, with reference to the flowchart 4613 and the timing diagrams illustrated in FIGS. 56A-D. In step 4614, the energy transfer module 6304 receives the digital AM carrier signal 616. In step 4616, the energy transfer module 6304 receives the energy transfer signal 5602. In step 4618, the energy transfer module 6304 transfers energy from the digital AM carrier signal 616 at the aliasing rate to directly down-convert it to the demodulated baseband signal 5610.

Example implementations of the energy transfer module 6302 are disclosed in Sections 4 and 5 below.

2.2 Example Embodiments

Various embodiments related to the method(s) and structure(s) described above are presented in this section (and its subsections). These embodiments are described herein for purposes of illustration, and not limitation. The invention is not limited to these embodiments. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

The method for down-converting the EM signal to the demodulated baseband signal F_{DMB}, illustrated in the flowchart 4613 of FIG. 46C, can be implemented with various types of modulated carrier signals including, but not limited to, AM, PM, etc., or any combination thereof. The flowchart 4613 of FIG. 46C is described below for AM and PM. The exemplary descriptions below are intended to facilitate an understanding of the present invention. The present invention is not limited to or by the exemplary embodiments below.

2.2.1 First Example Embodiment: Amplitude Modulation

2.2.1.1 Operational Description

Operation of the exemplary process of the flowchart 4613 in FIG. 46C is described below for the analog AM carrier signal 516, illustrated in FIG. 5C, and for the digital AM carrier signal 616, illustrated in FIG. 6C.

2.2.1.1.1 Analog AM Carrier Signal

A process for directly down-converting the analog AM carrier signal 516 in FIG. 5C to a demodulated baseband signal is now described with reference to the flowchart 4613 in FIG. 46C. The analog AM carrier signal

516 is re-illustrated in 57A for convenience. For this example, the analog AM carrier signal 516 oscillates at approximately 900 MHZ. In FIG. 57B, an analog AM carrier signal portion 5704 illustrates a portion of the analog AM carrier signal 516 on an expanded time scale.

The process begins at step 4614, which includes receiving an EM signal. This is represented by the analog AM carrier signal 516.

Step 4616 includes receiving an energy transfer signal having an aliasing rate F_{AR}. In FIG. 57C, an example energy transfer signal 5706 is illustrated on approximately the same time scale as FIG. 57B. The energy transfer signal 5706 includes a train of energy transfer pulses 5707 having non-negligible apertures that tend away from zero time in duration. The energy transfer pulses 5707 repeat at the aliasing rate, which is determined or selected as previously described. Generally, when down-converting an EM signal to a demodulated baseband signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the EM signal.

Step 4618 includes transferring energy from the EM signal at the aliasing rate to directly down-convert the EM signal to the demodulated baseband signal F_{DMB}. In FIG. 57D, an affected analog AM carrier signal 5708 illustrates effects of transferring energy from the analog AM carrier signal 516 at the aliasing rate F_{AR}. The affected analog AM carrier signal 5708 is illustrated on substantially the same time scale as FIGS. 57B and 57C.

FIG. 57E illustrates a demodulated baseband signal 5712, which is generated by the down-conversion process. Because a harmonic of the aliasing rate is substantially equal to the frequency of the signal 516, essentially no IF is produced. The only substantial aliased component is the baseband signal. The demodulated baseband signal 5712 is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

The demodulated baseband signal 5712 includes portions 5710A, which correlate with the energy transfer pulses 5707 in FIG. 57C, and portions 5710B, which are between the energy transfer pulses 5707. Portions 5710A represent energy transferred from the analog AM carrier signal 516 to a storage device, while simultaneously driving an output load. The portions 5710A occur when a switching module is closed by the energy transfer pulses 5707. Portions 5710B represent energy stored in a storage device continuing to drive the load. Portions 5710B occur when the switching module is opened after energy transfer pulses 5707.

In FIG. 57F, a demodulated baseband signal 5716 represents a filtered version of the demodulated baseband signal 5712, on a compressed time scale. The demodulated baseband signal 5716 is substantially similar to the modulating baseband signal 210 and can be further processed using any signal processing technique(s) without further down-conversion or demodulation.

The present invention can output the unfiltered demodulated baseband signal 5712, the filtered demodulated baseband signal 5716, a partially filtered demodulated baseband signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention.

The aliasing rate of the energy transfer signal is preferably controlled to optimize the demodulated baseband signal for amplitude output and polarity, as desired.

The drawings referred to herein illustrate direct down-conversion in accordance with the invention. For example, the demodulated baseband signals 5712 in FIG. 57E and 5716 in FIG. 57F illustrate that the analog AM carrier signal 516 was directly down-converted to a demodulated baseband signal by retaining enough baseband information for sufficient reconstruction.

2.2.1.1.2 Digital AM Carrier Signal

A process for directly down-converting the digital AM carrier signal 616 in FIG. 6C to a demodulated baseband signal is now described for the flowchart 4613 in FIG. 46C. The digital AM carrier signal 616 is re-illustrated in 58A for convenience. For this example, the digital AM carrier signal 616 oscillates at approximately 900 MHZ. In FIG. 58B, a digital AM carrier signal portion 5804 illustrates a portion of the digital AM carrier signal 616 on an expanded time scale.

The process begins at step 4614, which includes receiving an EM signal. This is represented by the digital AM carrier signal 616.

Step 4616 includes receiving an energy transfer signal having an aliasing rate F_{AR}. In FIG. 58C, an example energy transfer signal 5806 is illustrated on approximately the same time scale as FIG. 58B. The energy transfer signal 5806 includes a train of energy transfer pulses 5807 having non-negligible apertures that tend away from zero time in duration. The energy transfer pulses 5807 repeat at the aliasing rate, which is determined or selected as previously described. Generally, when directly down-converting an EM signal to a demodulated baseband signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the EM signal.

Step 4618 includes transferring energy from the EM signal at the aliasing rate to directly down-convert the EM signal to the demodulated baseband signal F_{DMB}. In FIG. 58D, an affected digital AM carrier signal 5808 illustrates effects of transferring energy from the digital AM carrier signal 616 at the aliasing rate F_{AR}. The affected digital AM carrier signal 5808 is illustrated on substantially the same time scale as FIGS. 58B and 58C.

FIG. 58E illustrates a demodulated baseband signal 5812, which is generated by the down-conversion process. Because a harmonic of the aliasing rate is substantially equal to the frequency of the signal 616, essentially no IF is produced. The only substantial aliased component is the

baseband signal. The demodulated baseband signal 5812 is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

The demodulated baseband signal 5812 includes portions 5810A, which correlate with the energy transfer pulses 5807 in FIG. 58C, and portions 5810B, which are between the energy transfer pulses 5807. Portions 5810A represent energy transferred from the digital AM carrier signal 616 to a storage device, while simultaneously driving an output load. The portions 5810A occur when a switching module is closed by the energy transfer pulses 5807. Portions 5810B represent energy stored in a storage device continuing to drive the load. Portions 5810B occur when the switching module is opened after energy transfer pulses 5807.

In FIG. 58F, a demodulated baseband signal 5816 represents a filtered version of the demodulated baseband signal 5812, on a compressed time scale. The demodulated baseband signal 5816 is substantially similar to the modulating baseband signal 310 and can be further processed using any signal processing technique(s) without further down-conversion or demodulation.

The present invention can output the unfiltered demodulated baseband signal 5812, the filtered demodulated baseband signal 5816, a partially filtered demodulated baseband signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention.

The aliasing rate of the energy transfer signal is preferably controlled to optimize the down-converted signal for amplitude output and polarity, as desired.

The drawings referred to herein illustrate direct down-conversion in accordance with the invention. For example, the demodulated baseband signals 5812 in FIG. 58E and 5816 in FIG. 58F illustrate that the digital AM

carrier signal 616 was directly down-converted to a demodulated baseband signal by retaining enough baseband information for sufficient reconstruction.

2.2.1.2 Structural Description

In an embodiment, the energy transfer module 6304 preferably transfers energy from the EM signal to directly down-convert it to a demodulated baseband signal in the manner shown in the operational flowchart 4613. But it should be understood that the scope and spirit of the invention includes other structural embodiments for performing the steps of the flowchart 1413. The specifics of the other structural embodiments will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

Operation of the energy transfer system 6302 is now described for the digital AM carrier signal 516, with reference to the flowchart 4613 and the timing diagrams in FIGS. 57A-F. In step 4612, the energy transfer module 6404 receives the analog AM carrier signal 516. In step 4614, the energy transfer module 6404 receives the energy transfer signal 5706. In step 4618, the energy transfer module 6404 transfers energy from the analog AM carrier signal 516 at the aliasing rate of the energy transfer signal 5706, to directly down-convert the digital AM carrier signal 516 to the demodulated baseband signals 5712 or 5716.

The operation of the energy transfer system 6402 is now described for the digital AM carrier signal 616, with reference to the flowchart 4613 and the timing diagrams in FIGS. 58A-F. In step 4614, the energy transfer module 6404 receives the digital AM carrier signal 616. In step 4616, the energy transfer module 6404 receives the energy transfer signal 5806. In step 4618, the energy transfer module 6404 transfers energy from the digital AM carrier signal 616 at the aliasing rate of the energy transfer signal 5806, to directly

down-convert the digital AM carrier signal 616 to the demodulated baseband signals 5812 or 5816.

Example implementations of the energy transfer module 6302 are disclosed in Sections 4 and 5 below.

2.2.2 Second Example Embodiment: Phase Modulation

2.2.2.1 Operational Description

Operation of the exemplary process of flowchart 4613 in FIG. 46C is described below for the analog PM carrier signal 916, illustrated in FIG. 9C and for the digital PM carrier signal 1016, illustrated in FIG. 10C.

2.2.2.1.1 Analog PM Carrier Signal

A process for directly down-converting the analog PM carrier signal 916 to a demodulated baseband signal is now described for the flowchart 4613 in FIG. 46C. The analog PM carrier signal 916 is re-illustrated in 59A for convenience. For this example, the analog PM carrier signal 916 oscillates at approximately 900 MHZ. In FIG. 59B, an analog PM carrier signal portion 5904 illustrates a portion of the analog PM carrier signal 916 on an expanded time scale.

The process begins at step 4614, which includes receiving an EM signal. This is represented by the analog PM carrier signal 916.

Step 4616 includes receiving an energy transfer signal having an aliasing rate F_{AR}. In FIG. 59C, an example energy transfer signal 5906 is illustrated on approximately the same time scale as FIG. 59B. The energy transfer signal 5906 includes a train of energy transfer pulses 5907 having non-negligible apertures that tend away from zero time in duration. The energy transfer pulses 5907 repeat at the aliasing rate, which is determined or selected

as previously described. Generally, when directly down-converting an EM signal to a demodulated baseband signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the EM signal.

Step 4618 includes transferring energy from the EM signal at the aliasing rate to directly down-convert the EM signal to the demodulated baseband signal F_{DMB}. In FIG. 59D, an affected analog PM carrier signal 5908 illustrates effects of transferring energy from the analog PM carrier signal 916 at the aliasing rate F_{AR}. The affected analog PM carrier signal 5908 is illustrated on substantially the same time scale as FIGS. 59B and 59C.

FIG. 59E illustrates a demodulated baseband signal 5912, which is generated by the down-conversion process. Because a harmonic of the aliasing rate is substantially equal to the frequency of the signal 516, essentially no IF is produced. The only substantial aliased component is the baseband signal. The demodulated baseband signal 5912 is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

The demodulated baseband signal 5912 includes portions 5910A, which correlate with the energy transfer pulses 5907 in FIG. 59C, and portions 5910B, which are between the energy transfer pulses 5907. Portions 5910A represent energy transferred from the analog PM carrier signal 916 to a storage device, while simultaneously driving an output load. The portions 5910A occur when a switching module is closed by the energy transfer pulses 5907. Portions 5910B represent energy stored in a storage device continuing to drive the load. Portions 5910B occur when the switching module is opened after energy transfer pulses 5907.

In FIG. 59F, a demodulated baseband signal 5916 represents a filtered version of the demodulated baseband signal 5912, on a compressed time scale. The demodulated baseband signal 5916 is substantially similar to the

modulating baseband signal 210 and can be further processed using any signal processing technique(s) without further down-conversion or demodulation.

The present invention can output the unfiltered demodulated baseband 5912, the filtered demodulated baseband signal 5916, a partially filtered demodulated baseband signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention.

The aliasing rate of the energy transfer signal is preferably controlled to optimize the down-converted signal for amplitude output and polarity, as desired.

The drawings referred to herein illustrate direct down-conversion in accordance with the invention. For example, the demodulated baseband signals 5912 in FIG. 59E and 5916 in FIG. 59F illustrate that the analog PM carrier signal 916 was successfully down-converted to a demodulated baseband signal by retaining enough baseband information for sufficient reconstruction.

2.2.2.1.2 Digital PM Carrier Signal

A process for directly down-converting the digital PM carrier signal 1016 in FIG. 6C to a demodulated baseband signal is now described for the flowchart 4613 in FIG. 46C. The digital PM carrier signal 1016 is re-illustrated in 60A for convenience. For this example, the digital PM carrier signal 1016 oscillates at approximately 900 MHZ. In FIG. 60B, a digital PM carrier signal portion 6004 illustrates a portion of the digital PM carrier signal 1016 on an expanded time scale. The process begins at step 4614, which includes receiving an EM signal. This is represented by the digital PM carrier signal 1016.

Step 4616 includes receiving an energy transfer signal F_{AR}. In FIG. 60C, an example energy transfer signal 6006 is illustrated on approximately

the same time scale as FIG. 60B. The energy transfer signal 6006 includes a train of energy transfer pulses 6007 having non-negligible apertures that tend away from zero time in duration. The energy transfer pulses 6007 repeat at the aliasing rate, which is determined or selected as previously described. Generally, when directly down-converting an EM signal to a demodulated baseband signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the EM signal.

Step 4618 includes transferring energy from the EM signal at the aliasing rate to directly down-convert the EM signal to the demodulated baseband signal F_{DMB}. In FIG. 60D, an affected digital PM carrier signal 6008 illustrates effects of transferring energy from the digital PM carrier signal 1016 at the aliasing rate F_{AR}. The affected digital PM carrier signal 6008 is illustrated on substantially the same time scale as FIGS. 60B and 60C.

FIG. 60E illustrates a demodulated baseband signal 6012, which is generated by the down-conversion process. Because a harmonic of the aliasing rate is substantially equal to the frequency of the signal 1016, essentially no IF is produced. The only substantial aliased component is the baseband signal. The demodulated baseband signal 6012 is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

The demodulated baseband signal 6012 includes portions 6010A, which correlate with the energy transfer pulses 6007 in FIG. 60C, and portions 6010B, which are between the energy transfer pulses 6007. Portions 6010A represent energy transferred from the digital PM carrier signal 1016 to a storage device, while simultaneously driving an output load. The portions 6010A occur when a switching module is closed by the energy transfer pulses 6007. Portions 6010B represent energy stored in a storage device continuing to drive the load. Portions 6010B occur when the switching module is opened after energy transfer pulses 6007.

In FIG. 60F, a demodulated baseband signal 6016 represents a filtered version of the demodulated baseband signal 6012, on a compressed time scale. The demodulated baseband signal 6016 is substantially similar to the modulating baseband signal 310 and can be further processed using any signal processing technique(s) without further down-conversion or demodulation.

The present invention can output the unfiltered demodulated baseband signal 6012, the filtered demodulated baseband signal 6016, a partially filtered demodulated baseband signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention.

The aliasing rate of the energy transfer signal is preferably controlled to optimize the down-converted signal for amplitude output and polarity, as desired.

The drawings referred to herein illustrate direct down-conversion in accordance with the invention. For example, the demodulated baseband signals 6012 in FIG. 60E and 6016 in FIG. 60F illustrate that the digital PM carrier signal 1016 was successfully down-converted to a demodulated baseband signal by retaining enough baseband information for sufficient reconstruction.

2.2.2.2 Structural Description

In an embodiment, the energy transfer system 6302 preferably transfers energy from an EM signal to directly down-convert it to a demodulated baseband signal in the manner shown in the operational flowchart 4613. But it should be understood that the scope and spirit of the invention includes other structural embodiments for performing the steps of the flowchart 1413. The specifics of the other structural embodiments will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

Operation of the energy transfer system 6302 is now described for the analog PM carrier signal 916, with reference to the flowchart 4613 and the timing diagrams in FIGS. 59A-F. In step 4614, the energy transfer module 6304 receives the analog PM carrier signal 916. In step 4616, the energy transfer module 6304 receives the energy transfer signal 5906. In step 4618, the energy transfer module 6304 transfers energy from the analog PM carrier signal 916 at the aliasing rate of the energy transfer signal 5906, to directly down-convert the analog PM carrier signal 916 to the demodulated baseband signals 5912 or 5916.

Operation of the energy transfer system 6302 is now described for the digital PM carrier signal 1016, with reference to the flowchart 4613 and to the timing diagrams in FIGS. 60A-F. In step 4614, the energy transfer module 6404 receives the digital PM carrier signal 1016. In step 4616, the energy transfer module 6404 receives the energy transfer signal 6006. In step 4618, the energy transfer module 6404 transfers energy from the digital PM carrier signal 1016 at the aliasing rate of the energy transfer signal 6006, to directly down-convert the digital PM carrier signal 1016 to the demodulated baseband signal 6012 or 6016.

Example implementations of the energy transfer module 6302 are disclosed in Sections 4 and 5 below.

2.2.3 Other Embodiments

The embodiments described above are provided for purposes of illustration. These embodiments are not intended to limit the invention. Alternate embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate embodiments fall within the scope and spirit of the present invention. Example implementations of the energy transfer module 6302 are disclosed in Sections 4 and 5 below.

2.3 Implementation Examples

Exemplary operational and/or structural implementations related to the method(s), structure(s), and/or embodiments described above are presented in Sections 4 and 5 below. These implementations are presented for purposes of illustration, and not limitation. The invention is not limited to the particular implementation examples described therein. Alternate implementations (including equivalents, extensions, variations, deviations, etc., of those described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

3. Modulation Conversion

In an embodiment, the invention down-converts an FM carrier signal F_{FMC} to a non-FM signal $F_{(NON\text{-}FM)}$, by transferring energy from the FM carrier signal F_{FMC} at an aliasing rate. This embodiment is illustrated in FIG. 45B as 4518.

In an example embodiment, the FM carrier signal F_{FMC} is down-converted to a phase modulated (PM) signal F_{PM}. In another example embodiment, the FM carrier signal F_{FMC} is down- converted to an amplitude modulated (AM) signal F_{AM}. The down-converted signal can be demodulated with any conventional demodulation technique to obtain a demodulated baseband signal F_{DMB}.

The invention can be implemented with any type of FM signal. Exemplary embodiments are provided below for down-converting a frequency shift keying (FSK) signal to a non-FSK signal. FSK is a sub-set of FM, wherein an FM signal shifts or switches between two or more frequencies. FSK is typically used for digital modulating baseband signals, such as the

digital modulating baseband signal 310 in FIG. 3. For example, in FIG. 8, the digital FM signal 816 is an FSK signal that shifts between an upper frequency and a lower frequency, corresponding to amplitude shifts in the digital modulating baseband signal 310. The FSK signal 816 is used in example embodiments below.

In a first example embodiment, energy is transferred from the FSK signal 816 at an aliasing rate that is based on a mid-point between the upper and lower frequencies of the FSK signal 816. When the aliasing rate is based on the mid-point, the FSK signal 816 is down-converted to a phase shift keying (PSK) signal. PSK is a sub-set of phase modulation, wherein a PM signal shifts or switches between two or more phases. PSK is typically used for digital modulating baseband signals. For example, in FIG. 10, the digital PM signal 1016 is a PSK signal that shifts between two phases. The PSK signal 1016 can be demodulated by any conventional PSK demodulation technique(s).

In a second example embodiment, energy is transferred from the FSK signal 816 at an aliasing rate that is based upon either the upper frequency or the lower frequency of the FSK signal 816. When the aliasing rate is based upon the upper frequency or the lower frequency of the FSK signal 816, the FSK signal 816 is down-converted to an amplitude shift keying (ASK) signal. ASK is a sub-set of amplitude modulation, wherein an AM signal shifts or switches between two or more amplitudes. ASK is typically used for digital modulating baseband signals. For example, in FIG. 6, the digital AM signal 616 is an ASK signal that shifts between the first amplitude and the second amplitude. The ASK signal 616 can be demodulated by any conventional ASK demodulation technique(s).

The following sections describe methods for transferring energy from an FM carrier signal F_{FMC} to down-convert it to the non-FM signal $F_{(NON\text{-}FM)}$. Exemplary structural embodiments for implementing the methods are also

described. It should be understood that the invention is not limited to the particular embodiments described below. Equivalents, extensions, variations, deviations, etc., of the following will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such equivalents, extensions, variations, deviations, etc., are within the scope and spirit of the present invention.

The following sections include a high level discussion, example embodiments, and implementation examples.

3.1 High Level Description

This section (including its subsections) provides a high-level description of transferring energy from the FM carrier signal F_{FM} to down-convert it to the non-FM signal $F_{(NON\text{-}FM)}$, according to the invention. In particular, an operational process for down-converting the FM carrier signal F_{FM} to the non-FM signal $F_{(NON\text{-}FM)}$ is described at a high-level. Also, a structural implementation for implementing this process is described at a high-level. The structural implementation is described herein for illustrative purposes, and is not limiting. In particular, the process described in this section can be achieved using any number of structural implementations, one of which is described in this section. The details of such structural implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

3.1.1 Operational Description

FIG. 46D depicts a flowchart 4619 that illustrates an exemplary method for down-converting the FM carrier signal F_{FMC} to the non-FM signal $F_{(NON\text{-}FM)}$. The exemplary method illustrated in the flowchart 4619 is an embodiment of the flowchart 4601 in FIG. 46A.

Any and all forms of frequency modulation techniques are valid for this invention. For ease of discussion, the digital FM carrier (FSK) signal 816 is used to illustrate a high level operational description of the invention. Subsequent sections provide detailed flowcharts and descriptions for the FSK signal 816. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention can be implemented to down-convert any type of FM signal.

The method illustrated in the flowchart 4619 is described below at a high level for down-converting the FSK signal 816 in FIG. 8C to a PSK signal. The FSK signal 816 is re-illustrated in FIG. 84A for convenience.

The process of the flowchart 4619 begins at step 4620, which includes receiving an FM signal. This is represented by the FSK signal 816. The FSK signal 816 shifts between a first frequency 8410 and a second frequency 8412. The first frequency 8410 can be higher or lower than the second frequency 8412. In an exemplary embodiment, the first frequency 8410 is approximately 899 MHZ and the second frequency 8412 is approximately 901 MHZ.

Step 4622 includes receiving an energy transfer signal having an aliasing rate F_{AR}. FIG. 84B illustrates an example energy transfer signal 8402 which includes a train of energy transfer pulses 8403 having non-negligible apertures 8405 that tend away from zero time in duration.

The energy transfer pulses 8403 repeat at the aliasing rate F_{AR}, which is determined or selected as previously described. Generally, when down-converting an FM carrier signal F_{FMC} to a non-FM signal $F_{(NON-FM)}$, the aliasing rate is substantially equal to a harmonic or, more typically, a sub-harmonic of a frequency within the FM signal. In this example overview embodiment, where the FSK signal 816 is to be down-converted to a PSK signal, the aliasing rate is substantially equal to a harmonic or, more typically, a sub-harmonic of the mid-point between the first frequency 8410 and the second frequency 8412. For the present example, the mid-point is approximately 900 MHZ.

Step 4624 includes transferring energy from the FM carrier signal F_{FMC} at the aliasing rate to down-convert the FM carrier signal F_{FMC} to the non-FM signal $F_{(NON-FM)}$. FIG. 84C illustrates a PSK signal 8404, which is generated by the modulation conversion process.

When the second frequency 8412 is under-sampled, the PSK signal 8404 has a frequency of approximately 1 MHZ and is used as a phase reference. When the first frequency 8410 is under-sampled, the PSK signal 8404 has a frequency of 1 MHZ and is phase shifted 180 degrees from the phase reference.

FIG. 84D depicts a PSK signal 8406, which is a filtered version of the PSK signal 8404. The invention can thus generate a filtered output signal, a partially filtered output signal, or a relatively unfiltered stair step output signal. The choice between filtered, partially filtered and non-filtered output signals is generally a design choice that depends upon the application of the invention.

The aliasing rate of the energy transfer signal is preferably controlled to optimize the down-converted signal for amplitude output and polarity, as desired.

Detailed exemplary embodiments for down-converting an FSK signal to a PSK signal and for down-converting an FSK signal to an ASK signal are provided below.

3.1.2 Structural Description

FIG. 63 illustrates the energy transfer system 6302 according to an embodiment of the invention. The energy transfer system 6302 includes the energy transfer module 6304. The energy transfer system 6302 is an example embodiment of the generic aliasing system 1302 in FIG. 13.

In a modulation conversion embodiment, the EM signal 1304 is an FM carrier signal F_{FMC} and the energy transfer module 6304 transfers energy from FM carrier signal at a harmonic or, more typically, a sub-harmonic of a

frequency within the FM frequency band. Preferably, the energy transfer module 6304 transfers energy from the FM carrier signal F_{FMC} to down-convert it to a non- FM signal $F_{(NON-FM)}$ in the manner shown in the operational flowchart 4619. But it should be understood that the scope and spirit of the invention includes other structural embodiments for performing the steps of the flowchart 4619. The specifics of the other structural embodiments will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

The operation of the energy transfer system 6302 shall now be described with reference to the flowchart 4619 and the timing diagrams of FIGS. 84A-84D. In step 4620, the energy transfer module 6304 receives the FSK signal 816. In step 4622, the energy transfer module 6304 receives the energy transfer signal 8402. In step 4624, the energy transfer module 6304 transfers energy from the FSK signal 816 at the aliasing rate of the energy transfer signal 8402 to down-convert the FSK signal 816 to the PSK signal 8404 or 8406.

Example implementations of the energy transfer module 6302 are provided in Section 4 below.

3.2 Example Embodiments

Various embodiments related to the method(s) and structure(s) described above are presented in this section (and its subsections). These embodiments are described herein for purposes of illustration, and not limitation. The invention is not limited to these embodiments. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

The method for down-converting an FM carrier signal F_{FMC} to a non-FM signal, $F_{(NON-FM)}$, illustrated in the flowchart 4619 of FIG.46D, can be implemented with any type of FM carrier signal including, but not limited to, FSK signals. The flowchart 4619 is described in detail below for down-converting an FSK signal to a PSK signal and for down-converting a PSK signal to an ASK signal. The exemplary descriptions below are intended to facilitate an understanding of the present invention. The present invention is not limited to or by the exemplary embodiments below.

3.2.1 First Example Embodiment: Down-Converting an FM Signal to a PM Signal

3.2.1.1 Operational Description

A process for down-converting the FSK signal 816 in FIG. 8C to a PSK signal is now described for the flowchart 4619 in FIG. 46D.

The FSK signal 816 is re-illustrated in FIG. 61A for convenience. The FSK signal 816 shifts between a first frequency 6106 and a second frequency 6108. In the exemplary embodiment, the first frequency 6106 is lower than the second frequency 6108. In an alternative embodiment, the first frequency 6106 is higher than the second frequency 6108. For this example, the first frequency 6106 is approximately 899 MHZ and the second frequency 6108 is approximately 901 MHZ.

FIG. 61B illustrates an FSK signal portion 6104 that represents a portion of the FSK signal 816 on an expanded time scale.

The process begins at step 4620, which includes receiving an FM signal. This is represented by the FSK signal 816.

Step 4622 includes receiving an energy transfer signal having an aliasing rate F_{AR}. FIG. 61C illustrates an example energy transfer signal 6107 on approximately the same time scale as FIG. 61B. The energy transfer signal 6107 includes a train of energy transfer pulses 6109 having non-negligible

apertures that tend away from zero time in duration. The energy transfer pulses 6109 repeat at the aliasing rate F_{AR}, which is determined or selected as described above. Generally, when down- converting an FM signal to a non-FM signal, the aliasing rate is substantially equal to a harmonic or, more typically, a sub-harmonic of a frequency within the FM signal.

In this example, where an FSK signal is being down-converted to a PSK signal, the aliasing rate is substantially equal to a harmonic or, more typically, a sub-harmonic, of the mid-point between the frequencies 6106 and 6108. In this example, where the first frequency 6106 is 899 MHZ and second frequency 6108 is 901 MHZ, the mid-point is approximately 900 MHZ. Suitable aliasing rates thus include 1.8 GHZ, 900 MHZ, 450 MHZ, etc.

Step 4624 includes transferring energy from the FM signal at the aliasing rate to down-convert it to the non-FM signal $F_{(NON-FM)}$. In FIG. 61D, an affected FSK signal 6118 illustrates effects of transferring energy from the FSK signal 816 at the aliasing rate F_{AR}. The affected FSK signal 6118 is illustrated on substantially the same time scale as FIGS. 61B and 61C.

FIG. 61E illustrates a PSK signal 6112, which is generated by the modulation conversion process. PSK signal 6112 is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

The PSK signal 6112 includes portions 6110A, which correlate with the energy transfer pulses 6107 in FIG. 61C. The PSK signal 6112 also includes portions 6110B, which are between the energy transfer pulses 6109. Portions 6110A represent energy transferred from the FSK 816 to a storage device, while simultaneously driving an output load. The portions 6110A occur when a switching module is closed by the energy transfer pulses 6109. Portions 6110B represent energy stored in a storage device continuing to drive the load. Portions 6110B occur when the switching module is opened after energy transfer pulses 6107.

In FIG. 61F, a PSK signal 6114 represents a filtered version of the PSK signal 6112, on a compressed time scale. The present invention can output the unfiltered demodulated baseband signal 6112, the filtered demodulated baseband signal 6114, a partially filtered demodulated baseband signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention. The PSK signals 6112 and 6114 can be demodulated with a conventional demodulation technique(s).

The aliasing rate of the energy transfer signal is preferably controlled to optimize the down-converted signal for amplitude output and polarity, as desired.

The drawings referred to herein illustrate modulation conversion in accordance with the invention. For example, the PSK signals 6112 in FIG. 61E and 6114 in FIG. 61F illustrate that the FSK signal 816 was successfully down-converted to a PSK signal by retaining enough baseband information for sufficient reconstruction.

3.2.1.2 Structural Description

The operation of the energy transfer system 1602 is now described for down-converting the FSK signal 816 to a PSK signal, with reference to the flowchart 4619 and to the timing diagrams of FIGS. 61A-E. In step 4620, the energy transfer module 1606 receives the FSK signal 816 (FIG. 61A). In step 4622, the energy transfer module 1606 receives the energy transfer signal 6107 (FIG. 61C). In step 4624, the energy transfer module 1606 transfers energy from the FSK signal 816 at the aliasing rate of the energy transfer signal 6107 to down-convert the FSK signal 816 to the PSK signal 6112 in FIG. 61E or the PSK signal 6114 in FIG. 61F.

3.2.2. Second Example Embodiment: Down-Converting an FM Signal to an AM Signal

3.2.2.1 Operational Description

A process for down-converting the FSK signal 816 in FIG. 8C to an ASK signal is now described for the flowchart 4619 in FIG. 46D.

The FSK signal 816 is re-illustrated in FIG. 62A for convenience. The FSK signal 816 shifts between a first frequency 6206 and a second frequency 6208. In the exemplary embodiment, the first frequency 6206 is lower than the second frequency 6208. In an alternative embodiment, the first frequency 6206 is higher than the second frequency 6208. For this example, the first frequency 6206 is approximately 899 MHZ and the second frequency 6208 is approximately 901 MHZ.

FIG. 62B illustrates an FSK signal portion 6204 that represents a portion of the FSK signal 816 on an expanded time scale.

The process begins at step 4620, which includes receiving an FM signal. This is represented by the FSK signal 816.

Step 4622 includes receiving an energy transfer signal having an aliasing rate F_{AR}. FIG. 62C illustrates an example energy transfer signal 6207 on approximately the same time scale as FIG. 62B. The energy transfer signal 6207 includes a train of energy transfer pulses 6209 having non-negligible apertures that tend away from zero time in duration. The energy transfer pulses 6209 repeat at the aliasing rate F_{AR}, which is determined or selected as described above. Generally, when down- converting an FM signal to a non-FM signal, the aliasing rate is substantially equal to a harmonic or, more typically, a sub-harmonic of a frequency within the FM signal.

In this example, where an FSK signal is being down-converted to an ASK signal, the aliasing rate is substantially equal to a harmonic or, more typically, a sub-harmonic, of either the first frequency 6206 or the second frequency 6208. In this example, where the first frequency 6206 is 899 MHZ

and the second frequency 6208 is 901 MHZ, the aliasing rate can be substantially equal to a harmonic or sub-harmonic of 899 MHZ or 901 MHZ.

Step 4624 includes transferring energy from the FM signal at the aliasing rate to down-convert it to the non-FM signal $F_{(NON-FM)}$. In FIG. 62D, an affected FSK signal 6218 illustrates effects of transferring energy from the FSK signal 816 at the aliasing rate F_{AR}. The affected FSK signal 6218 is illustrated on substantially the same time scale as FIGS. 62B and 62C.

FIG. 62E illustrates an ASK signal 6212, which is generated by the modulation conversion process. ASK signal 6212 is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

The ASK signal 6212 includes portions 6210A, which correlate with the energy transfer pulses 6209 in FIG. 62C. The ASK signal 6212 also includes portions 6210B, which are between the energy transfer pulses 6209. Portions 6210A represent energy transferred from the FSK 816 to a storage device, while simultaneously driving an output load. Portions 6210A occur when a switching module is closed by the energy transfer pulses 6207. Portions 6210B represent energy stored in a storage device continuing to drive the load. Portions 6210B occur when the switching module is opened after energy transfer pulses 6207.

In FIG. 62F, an ASK signal 6214 represents a filtered version of the ASK signal 6212, on a compressed time scale. The present invention can output the unfiltered demodulated baseband signal 6212, the filtered demodulated baseband signal 6214, a partially filtered demodulated baseband signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention. The ASK signals 6212 and 6214 can be demodulated with a conventional demodulation technique(s).

The aliasing rate of the energy transfer signal is preferably controlled to optimize the down-converted signal for amplitude output and/or polarity, as desired.

The drawings referred to herein illustrate modulation conversion in accordance with the invention. For example, the ASK signals 6212 in FIG. 62E and 6214 in FIG. 62F illustrate that the FSK signal 816 was successfully down-converted to an ASK signal by retaining enough baseband information for sufficient reconstruction.

3.2.2.2 Structural Description

The operation of the energy transfer system 1602 is now described for down-converting the FSK signal 816 to an ASK signal, with reference to the flowchart 4619 and to the timing diagrams of FIGS. 62A-F. In step 4620, the energy transfer module 6304 receives the FSK signal 816 (FIG. 62A). In step 4622, the energy transfer module 6304 receives the energy transfer signal 6207 (FIG. 62C). In step 4624, the energy transfer module 6304 transfers energy from the FSK signal 818 at the aliasing rate of the energy transfer signal 6207 to down-convert the FSK signal 816 to the ASK signal 6212 in FIG. 62E or the ASK signal 6214 in FIG. 62F.

3.2.3 Other Example Embodiments

The embodiments described above are provided for purposes of illustration. These embodiments are not intended to limit the invention. Alternate embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate embodiments fall within the scope and spirit of the present invention.

Example implementations of the energy transfer module 6302 are disclosed in Sections 4 and 5 below.

3.3 Implementation Examples

Exemplary operational and/or structural implementations related to the method(s), structure(s), and/or embodiments described above are presented in Sections 4 and 5 below. These implementations are presented for purposes of illustration, and not limitation. The invention is not limited to the particular implementation examples described therein. Alternate implementations (including equivalents, extensions, variations, deviations, etc., of those described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

4. Implementation Examples

Exemplary operational and/or structural implementations related to the method(s), structure(s), and/or embodiments described above are presented in this section (and its subsections). These implementations are presented herein for purposes of illustration, and not limitation. The invention is not limited to the particular implementation examples described herein. Alternate implementations (including equivalents, extensions, variations, deviations, etc., of those described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

FIG. 63 illustrates an energy transfer system 6302, which is an exemplary embodiment of the generic aliasing system 1302 in FIG. 13. The energy transfer system 6302 includes an energy transfer module 6304, which receives the EM signal 1304 and an energy transfer signal 6306. The energy

transfer signal 6306 includes a train of energy transfer pulses having non-negligible apertures that tend away from zero time in duration. The energy transfer pulses repeat at an aliasing rate F_{AR}.

The energy transfer module 6304 transfers energy from the EM signal 1304 at the aliasing rate of the energy transfer signal 6306, as described in the sections above with respect to the flowcharts 4601 in FIG. 46A, 4607 in FIG. 46B, 4613 in FIG. 46C and 4619 in FIG. 46D. The energy transfer module 6304 outputs a down-converted signal 1308B, which includes non-negligible amounts of energy transferred from the EM signal 1304.

FIG. 64A illustrates an exemplary gated transfer system 6402, which is an example of the energy transfer system 6302. The gated transfer system 6402 includes a gated transfer module 6404, which is described below.

FIG. 64B illustrates an exemplary inverted gated transfer system 6406, which is an alternative example of the energy transfer system 6302. The inverted gated transfer system 6406 includes an inverted gated transfer module 6408, which is described below.

4.1 The Energy Transfer System as a Gated Transfer System

FIG. 64A illustrates the exemplary gated transfer system 6402, which is an exemplary implementation of the energy transfer system 6302. The gated transfer system 6402 includes the gated transfer module 6404, which receives the EM signal 1304 and the energy transfer signal 6306. The energy transfer signal 6306 includes a train of energy transfer pulses having non-negligible apertures that tend away from zero time in duration. The energy transfer pulses repeat at an aliasing rate F_{AR}.

The gated transfer module 6404 transfers energy from the EM signal 1304 at the aliasing rate of the energy transfer signal 6306, as described in the sections above with respect to the flowcharts 4601 in FIG. 46A, 4607 in FIG. 46B, 4613 in FIG. 46C and 4619 in FIG. 46D. The gated transfer module

6404 outputs the down-converted signal 1308B, which includes non-negligible amounts of energy transferred from the EM signal 1304.

4.1.1 The Gated Transfer System as a Switch Module and a Storage Module

FIG. 65 illustrates an example embodiment of the gated transfer module 6404 as including a switch module 6502 and a storage module 6506. Preferably, the switch module 6502 and the storage module 6506 transfer energy from the EM signal 1304 to down-convert it in any of the manners shown in the operational flowcharts 4601 in FIG. 46A, 4607 in FIG. 46B, 4613 in FIG. 46C and 4619 in FIG. 46D.

For example, operation of the switch module 6502 and the storage module 6506 is now described for down-converting the EM signal 1304 to an intermediate signal, with reference to the flowchart 4607 and the example timing diagrams in FIG. 83A-F.

In step 4608, the switch module 6502 receives the EM signal 1304 (FIG. 83A). In step 4610, the switch module 6502 receives the energy transfer signal 6306 (FIG. 83C). In step 4612, the switch module 6502 and the storage module 6506 cooperate to transfer energy from the EM signal 1304 and down-convert it to an intermediate signal. More specifically, during step 4612, the switch module 6502 closes during each energy transfer pulse to couple the EM signal 1304 to the storage module 6506. In an embodiment, the switch module 6502 closes on rising edges of the energy transfer pulses. In an alternative embodiment, the switch module 6502 closes on falling edges of the energy transfer pulses. While the EM signal 1304 is coupled to the storage module 6506, non-negligible amounts of energy are transferred from the EM signal 1304 to the storage module 6506. FIG. 83B illustrates the EM signal 1304 after the energy is transferred from it. FIG. 83D illustrates the transferred energy stored in the storage module 6506. The storage module 6506 outputs

the transferred energy as the down-converted signal 1308B. The storage module 6506 can output the down-converted signal 1308B as an unfiltered signal such as signal shown in FIG. 83E, or as a filtered down-converted signal (FIG. 83F).

4.1.2 The Gated Transfer System as Break-Before-Make Module

FIG. 67A illustrates an example embodiment of the gated transfer module 6404 as including a break-before-make module 6702 and a storage module 6716. Preferably, the break before make module 6702 and the storage module 6716 transfer energy from the EM signal 1304 to down-convert it in any of the manners shown in the operational flowcharts 4601 in FIG. 46A, 4607 in FIG. 46B, 4613 in FIG. 46C and 4619 in FIG. 46D.

In FIG. 67A, the break-before-make module 6702 includes a includes a normally open switch 6704 and a normally closed switch 6706. The normally open switch 6704 is controlled by the energy transfer signal 6306. The normally closed switch 6706 is controlled by an isolation signal 6712. In an embodiment, the isolation signal 6712 is generated from the energy transfer signal 6306. Alternatively, the energy transfer signal 6306 is generated from the isolation signal 6712. Alternatively, the isolation signal 6712 is generated independently from the energy transfer signal 6306. The break-before-make module 6702 substantially isolates an input 6708 from an output 6710.

FIG. 67B illustrates an example timing diagram of the energy transfer signal 6306, which controls the normally open switch 6704. FIG. 67C illustrates an example timing diagram of the isolation signal 6712, which controls the normally closed switch 6706. Operation of the break-before-make module 6702 is now described with reference to the example timing diagrams in FIGS. 67B and 67C.

Prior to time t0, the normally open switch 6704 and the normally closed switch 6706 are at their normal states.

At time t0, the isolation signal 6712 in FIG. 67C opens the normally closed switch 6706. Thus, just after time t0, the normally open switch 6704 and the normally closed switch 6706 are open and the input 6708 is isolated from the output 6710.

At time t1, the energy transfer signal 6306 in FIG. 67B closes the normally open switch 6704 for the non-negligible duration of a pulse. This couples the EM signal 1304 to the storage module 6716.

Prior to t2, the energy transfer signal 6306 in FIG. 67B opens the normally open switch 6704. This de-couples the EM signal 1304 from the storage module 6716.

At time t2, the isolation signal 6712 in FIG. 67C closes the normally closed switch 6706. This couples the storage module 6716 to the output 6710.

The storage module 6716, is similar to the storage module 6506 FIG. 65. The break-before-make gated transfer system 6701 down-converts the EM signal 1304 in a manner similar to that described with reference to the gated transfer system 6501 in FIG. 65.

4.1.3 Example Implementations of the Switch Module

The switch module 6502 in FIG. 65 and the switch modules 6704 and 6706 in FIG. 67A can be any type of switch device that preferably has a relatively low impedance when closed and a relatively high impedance when open. The switch modules 6502, 6704 and 6706 can be implemented with normally open or normally closed switches. The switch modules need not be ideal switch modules.

FIG. 66B illustrates the switch modules 6502, 6704 and 6706 as a switch module 6610. Switch module 6610 can be implemented in either

normally open or normally closed architecture. The switch module 6610 (e.g., switch modules 6502, 6704 and 6706) can be implemented with any type of suitable switch device, including, but not limited, to mechanical switch devices and electrical switch devices, optical switch devices, etc., and combinations thereof. Such devices include, but are not limited to transistor switch devices, diode switch devices, relay switch devices, optical switch devices, micro-machine switch devices, etc., or combinations thereof.

In an embodiment, the switch module 6610 can be implemented as a transistor, such as, for example, a field effect transistor (FET), a bi-polar transistor, or any other suitable circuit switching device.

In FIG. 66A, the switch module 6610 is illustrated as a FET 6602. The FET 6602 can be any type of FET, including, but not limited to, a MOSFET, a JFET, a GaAsFET, etc.. The FET 6602 includes a gate 6604, a source 6606 and a drain 6608. The gate 6604 receives the energy transfer signal 6306 to control the switching action between the source 6606 and the drain 6608. In an embodiment, the source 6606 and the drain 6608 are interchangeable.

It should be understood that the illustration of the switch module 6610 as a FET 6602 in FIG. 66A is for example purposes only. Any device having switching capabilities could be used to implement the switch module 6610 (i.e., switch modules 6502, 6704 and 6706), as will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

In FIG. 66C, the switch module 6610 is illustrated as a diode switch 6612, which operates as a two lead device when the energy transfer signal 6306 is coupled to the output 6613.

In FIG. 66D, the switch module 6610 is illustrated as a diode switch 6614, which operates as a two lead device when the energy transfer signal 6306 is coupled to the output 6615.

4.1.4 Example Implementations of the Storage Module

The storage modules 6506 and 6716 store non-negligible amounts of energy from the EM signal 1304. In an exemplary embodiment, the storage modules 6506 and 6716 are implemented as a reactive storage module 6801 in FIG. 68A, although the invention is not limited to this embodiment. A reactive storage module is a storage module that employs one or more reactive electrical components to store energy transferred from the EM signal 1304. Reactive electrical components include, but are not limited to, capacitors and inductors.

In an embodiment, the storage modules 6506 and 6716 include one or more capacitive storage elements, illustrated in FIG. 68B as a capacitive storage module 6802. In FIG. 68C, the capacitive storage module 6802 is illustrated as one or more capacitors illustrated generally as capacitor(s) 6804.

The goal of the storage modules 6506 and 6716 is to store non-negligible amounts of energy transferred from the EM signal 1304. Amplitude reproduction of the original, unaffected EM input signal is not necessarily important. In an energy transfer environment, the storage module preferably has the capacity to handle the power being transferred, and to allow it to accept a non-negligible amount of power during a non-negligible aperture period.

A terminal 6806 serves as an output of the capacitive storage module 6802. The capacitive storage module 6802 provides the stored energy at the terminal 6806. FIG. 68F illustrates the capacitive storage module 6802 as including a series capacitor 6812, which can be utilized in an inverted gated transfer system described below.

In an alternative embodiment, the storage modules 6506 and 6716 include one or more inductive storage elements, illustrated in FIG. 68D as an inductive storage module 6808.

In an alternative embodiment, the storage modules 6506 and 6716 include a combination of one or more capacitive storage elements and one or more inductive storage elements, illustrated in FIG. 68E as a capacitive/inductive storage module 6810.

FIG. 68G illustrates an integrated gated transfer system 6818 that can be implemented to down-convert the EM signal 1304 as illustrated in, and described with reference to, FIGS. 83A-F.

4.1.5 Optional Energy Transfer Signal Module

FIG. 69 illustrates an energy transfer system 6901, which is an example embodiment of the energy transfer system 6302. The energy transfer system 6901 includes an optional energy transfer signal module 6902, which can perform any of a variety of functions or combinations of functions including, but not limited to, generating the energy transfer signal 6306.

In an embodiment, the optional energy transfer signal module 6902 includes an aperture generator, an example of which is illustrated in FIG. 68J as an aperture generator 6820. The aperture generator 6820 generates non-negligible aperture pulses 6826 from an input signal 6824. The input signal 6824 can be any type of periodic signal, including, but not limited to, a sinusoid, a square wave, a saw-tooth wave, etc. Systems for generating the input signal 6824 are described below.

The width or aperture of the pulses 6826 is determined by delay through the branch 6822 of the aperture generator 6820. Generally, as the desired pulse width increases, the difficulty in meeting the requirements of the aperture generator 6820 decrease. In other words, to generate non-negligible aperture pulses for a given EM input frequency, the components utilized in the example aperture generator 6820 do not require as fast reaction times as those that are required in an under-sampling system operating with the same EM input frequency.

The example logic and implementation shown in the aperture generator 6820 are provided for illustrative purposes only, and are not limiting. The actual logic employed can take many forms. The example aperture generator 6820 includes an optional inverter 6828, which is shown for polarity consistency with other examples provided herein.

An example implementation of the aperture generator 6820 is illustrated in FIG. 68K. Additional examples of aperture generation logic are provided in FIGS. 68H and 68I. FIG. 68H illustrates a rising edge pulse generator 6840, which generates pulses 6826 on rising edges of the input signal 6824. FIG. 68I illustrates a falling edge pulse generator 6850, which generates pulses 6826 on falling edges of the input signal 6824.

In an embodiment, the input signal 6824 is generated externally of the energy transfer signal module 6902, as illustrated in FIG. 69. Alternatively, the input signal 6924 is generated internally by the energy transfer signal module 6902. The input signal 6824 can be generated by an oscillator, as illustrated in FIG. 68L by an oscillator 6830. The oscillator 6830 can be internal to the energy transfer signal module 6902 or external to the energy transfer signal module 6902. The oscillator 6830 can be external to the energy transfer system 6901. The output of the oscillator 6830 may be any periodic waveform.

The type of down-conversion performed by the energy transfer system 6901 depends upon the aliasing rate of the energy transfer signal 6306, which is determined by the frequency of the pulses 6826. The frequency of the pulses 6826 is determined by the frequency of the input signal 6824. For example, when the frequency of the input signal 6824 is substantially equal to a harmonic or a sub-harmonic of the EM signal 1304, the EM signal 1304 is directly down-converted to baseband (e.g. when the EM signal is an AM signal or a PM signal), or converted from FM to a non-FM signal. When the frequency of the input signal 6824 is substantially equal to a harmonic or a

sub-harmonic of a difference frequency, the EM signal 1304 is down-converted to an intermediate signal.

The optional energy transfer signal module 6902 can be implemented in hardware, software, firmware, or any combination thereof.

4.2 The Energy Transfer System as an Inverted Gated Transfer System

FIG. 64B illustrates an exemplary inverted gated transfer system 6406, which is an exemplary implementation of the energy transfer system 6302. The inverted gated transfer system 6406 includes an inverted gated transfer module 6408, which receives the EM signal 1304 and the energy transfer signal 6306. The energy transfer signal 6306 includes a train of energy transfer pulses having non-negligible apertures that tend away from zero time in duration. The energy transfer pulses repeat at an aliasing rate F_{AR}. The inverted gated transfer module 6408 transfers energy from the EM signal 1304 at the aliasing rate of the energy transfer signal 6306, as described in the sections above with respect to the flowcharts 4601 in FIG. 46A, 4607 in FIG. 46B, 4613 in FIG. 46C and 4619 in FIG. 46D. The inverted gated transfer module 6408 outputs the down-converted signal 1308B, which includes non-negligible amounts of energy transferred from the EM signal 1304.

4.2.1 The Inverted Gated Transfer System as a Switch Module and a Storage Module

FIG. 74 illustrates an example embodiment of the inverted gated transfer module 6408 as including a switch module 7404 and a storage module 7406. Preferably, the switch module 7404 and the storage module 7406 transfer energy from the EM signal 1304 to down-convert it in any of the manners shown in the operational flowcharts 4601 in FIG. 46A, 4607 in FIG. 46B, 4613 in FIG. 46C and 4619 in FIG. 46D.

The switch module 7404 can be implemented as described above with reference to FIGS. 66A-D. The storage module 7406 can be implemented as described above with reference to FIGS. 68A-F.

In the illustrated embodiment, the storage module 7206 includes one or more capacitors 7408. The capacitor(s) 7408 are selected to pass higher frequency components of the EM signal 1304 through to a terminal 7410, regardless of the state of the switch module 7404. The capacitor 7408 stores non-negligible amounts of energy from the EM signal 1304. Thereafter, the signal at the terminal 7410 is off-set by an amount related to the energy stored in the capacitor 7408.

Operation of the inverted gated transfer system 7401 is illustrated in FIGS. 75A-F. FIG. 75A illustrates the EM signal 1304. FIG. 75B illustrates the EM signal 1304 after transferring energy from it. FIG. 75C illustrates the energy transfer signal 6306, which includes a train of energy transfer pulses having non-negligible apertures.

FIG. 75D illustrates an example down-converted signal 1308B. FIG. 75E illustrates the down-converted signal 1308B on a compressed time scale. Since the storage module 7406 is a series element, the higher frequencies (e.g., RF) of the EM signal 1304 can be seen on the down-converted signal. This can be filtered as illustrated in FIG. 75F.

The inverted gated transfer system 7401 can be used to down-convert any type of EM signal, including modulated carrier signals and unmodulated carrier signals.

4.3 Rail to Rail Operation for Improved Dynamic Range

4.3.1 Introduction

FIG. 110A illustrates aliasing module 11000 that down-converts EM signal 11002 to down-converted signal 11012 using aliasing signal 11014

(sometimes called an energy transfer signal). Aliasing module 11000 is an example of energy transfer module 6304 in FIG. 63. Aliasing module 11000 includes UFT module 11004 and storage module 11008. As shown in FIG. 110A, UFT module 11004 is implemented as a n-channel FET 11006, and storage module 11008 is implemented as a capacitor 11010, although the invention is not limited to this embodiment.

FET 11006 receives the EM signal 11002 and aliasing signal 11014. In one embodiment, aliasing signal 11014 includes a train of pulses having non-negligible apertures that repeat at an aliasing rate. The aliasing rate may be harmonic or sub-harmonic of the EM signal 11002. FET 11006 samples EM signal 11002 at the aliasing rate of aliasing signal 11014 to generate down-converted signal 11012. In one embodiment, aliasing signal 11014 controls the gate of FET 11006 so that FET 11006 conducts (or turns on) when the FET gate-to-source voltage (V_{GS}) exceeds a threshold voltage (V_T) . When the FET 11006 conducts, a channel is created from source to drain of FET 11006 so that charge is transferred from the EM signal 11002 to the capacitor 11010. More specifically, the FET 11006 conductance (1/R) vs V_{GS} is a continuous function that reaches an acceptable level at V_T, as illustrated in FIG. 110B. The charge stored by capacitor 11010 during successive samples forms down-converted signal 11012.

As stated above, n-channel FET 11006 conducts whenV_{GS} exceeds the threshold voltage V_T. As shown in FIG.110A, the gate voltage of FET 11006 is determined by aliasing signal 11014, and the source voltage is determined by the input EM signal 11002. Aliasing signal 11014 is preferably a plurality of pulses whose amplitude is predictable and set by a system designer. However, the EM signal 11002 is typically received over a communications medium by a coupling device (such as antenna). Therefore, the amplitude of EM signal 11102 may be variable and dependent on a number of factors including the strength of the transmitted signal, and the attenuation of the

communications medium. Thus, the source voltage on FET 11006 is not entirely predictable and will affect V_{GS} and the conductance of FET 11006, accordingly.

For example, FIG. 111A illustrates EM signal 11102, which is an example of EM signal 11002 that appears on the source of FET 11006. EM signal 11102 has a section 11104 with a relatively high amplitude as shown. FIG. 111B illustrates the aliasing signal 11106 as an example of aliasing signal 11014 that controls the gate of FET 11006. FIG. 111C illustrates V_{GS} 11108, which is the difference between the gate and source voltages shown in FIGS. 111B and 111A, respectively. FET 11006 has an inherent threshold voltage V_T 11112 shown in FIG. 111C, above which FET 11006 conducts. It is preferred that $V_{GS} > V_T$ during each pulse of aliasing signal 11106, so that FET 11006 conducts and charge is transferred from the EM signal 11102 to the capacitor 11010 during each pulse of aliasing signal 11106. As shown in FIG. 111C, the high amplitude section 11104 of EM signal 11102 causes a V_{GS} pulse 11110 that does exceed the V_T 11112, and therefore FET 11006 will not fully conduct as is desired. Therefore, the resulting sample of EM signal 11102 may be degraded, which potentially negatively affects the down-converted signal 11012.

As stated earlier, the conductance of FET 11006 vs V_{GS} is mathematically continuous and is not a hard cutoff. In other words, FET 11006 will marginally conduct when controlled by pulse 11110, even though pulse 11110 is below V_T 11112. However, the insertion loss of FET 11006 will be increased when compared with a V_{GS} pulse 11111, which is greater than V_T 11112. The performance reduction caused by a large amplitude input signal is often referred to as clipping or compression. Clipping causes distortion in the down-converted signal 11012, which adversely affects the faithful down-conversion of input EM signal 11102. Dynamic range is a figure of merit associated with the range of input signals that can be faithfully down-

converted without introducing distortion in the down-converted signal. The higher the dynamic range of a down-conversion circuit, the larger the input signals that can down-converted without introducing distortion in the down-converted signal.

4.3.2 Complementary UFT Structure for Improved Dynamic Range

FIG. 112 illustrates aliasing module 11200, according to an embodiment of the invention, that down-converts EM signal 11208 to generate down-converted signal 11214 using aliasing signal 11220. Aliasing module 11200 is able to down-convert input signals over a larger amplitude range as compared to aliasing module 11000, and therefore aliasing module 11200 has an improved dynamic range when compared with aliasing module 11000. The dynamic range improvement occurs because aliasing module 11200 includes two UFT modules that are implemented with complementary FET devices. In other words, one FET is n-channel, and the other FET is p-channel, so that at least one FET is always conducting during an aliasing signal pulse, assuming the input signal does not exceed the power supply constraints. Aliasing module 11200 includes: delay 11202; UFT modules 11206, 11216; nodes 11210, 11212; and inverter 11222. Inverter 11222 is tied to voltage supplies V_+ 11232 and V_- 11234. UFT module 11206 comprises n–channel FET 11204, and UFT module 11216 comprises p-channel FET 11218.

As stated, aliasing module 11200 operates two complementary FETs to extend the dynamic range and reduce any distortion effects. This requires that two complementary aliasing signals 11224, 11226 be generated from aliasing signal 11220 to control the sampling by FETs 11218, 11204, respectively. To do so, inverter 11222 receives and inverts aliasing signal 11220 to generate aliasing signal 11224 that controls p-channel FET 11218. Delay 11202 delays aliasing signal 11220 to generate aliasing signal 11226, where the amount of

time delay is approximately equivalent to that associated with inverter 11222. As such, aliasing signals 11224 and 11226 are approximately complementary in amplitude.

Node 11210 receives EM signal 11208, and couples EM signals 11227, 11228 to the sources of n-channel FET 11204 and p-channel FET 11218, respectively, where EM signals 11227, 11228 are substantially replicas of EM signal 11208. N–channel FET 11204 samples EM signal 11227 as controlled by aliasing signal 11226, and produces samples 11236 at the drain of FET 11204. Likewise, p-channel FET 11218 samples EM signal 11228 as controlled by aliasing signal 11224, and produces samples 11238 at the drain of FET 11218. Node 11212 combines the resulting charge samples into charge samples 11240, which are stored by capacitor 11230. The charge stored by capacitor 11230 during successive samples forms down-converted signal 11214. Aliasing module 11200 offers improved dynamic range over aliasing module 11000 because n-channel FET 11204 and p-channel FET 11214 are complementary devices. Therefore, if one device is cutoff because of a large input EM signal 11208, the other device will conduct and sample the input signal, as long as the input signal is between the power supply voltages V_+ 11232 and V_- 11234. This is often referred to as rail-to-rail operation as will be understood by those skilled in the arts.

For example, FIG. 113A illustrates EM signal 11302 which is an example of EM signals 11227, 11228 that are coupled to the sources of n-channel FET 11204 and p-channel FET 11218, respectively. As shown, EM signal 11302 has a section 11304 with a relatively high amplitude including pulses 11303, 11305. FIG. 113B illustrates the aliasing signal 11306 as an example of aliasing signal 11226 that controls the gate of n-channel FET 11204. Likewise for the p-channel FET, FIG. 113D illustrates the aliasing signal 11314 as an example of aliasing signal 11224 that controls the gate of p-

channel FET 11218. Aliasing signal 11314 is the amplitude complement of aliasing signal 11306.

FIG. 113C illustrates V_{GS} 11308, which is the difference between the gate and source voltages on n–channel FET 11204 that are depicted in FIGS. 113B and 113A, respectively. FIG. 113C also illustrates the inherent threshold voltage V_T 11309 for FET 11204, above which FET 11204 conducts. Likewise for the p-channel FET, FIG. 113E illustrates V_{GS} 11316, which is the difference between the gate and source voltages for p-channel FET 11218 that are depicted in FIGS. 113D and 113A, respectively. FIG. 113E also illustrates the inherent threshold voltage V_T 11317 for FET 11218, below which FET 11218 conducts.

As stated, n-channel FET 11204 conducts when V_{GS} 11308 exceeds V_T 11309, and p-channel FET 11218 conducts when V_{GS} 11316 drops below V_T 11317. As illustrated by FIG. 113C, n–channel FET 11204 conducts over the range of EM signal 11302 depicted in FIG. 113A, except for the EM signal pulse 11305 that results in a corresponding V_{GS} pulse 11310 (FIG. 113C) that does not exceed V_T 11309. However, p-channel FET 11218 does conduct because the same EM signal pulse 11305 causes a V_{GS} pulse 11320 (FIG. 113E) that drops well below that of V_T 11317 for the p-channel FET. Therefore, the sample of the EM signal 11302 is properly taken by p-channel FET 11218, and no distortion is introduced in down-converted signal 11214. Similarly, EM signal pulse 11303 results inV_{GS} pulse 11322 (FIG. 113E) that is inadequate for the p-channel FET 11218 to fully conduct. However, n-channel FET 11204 does fully conduct because the same EM signal pulse 11303 results in a V_{GS} 11311 (FIG. 113C) that greatly exceeds V_T 11309.

As illustrated above, aliasing module 11200 offers an improvement in dynamic range over aliasing module 11000 because of the complimentary FET structure. Any input signal that is within the power supply voltages V_+ 11232 and V_- 11234 will cause either FET 11204 or FET 11218 to conduct, or cause

both FETs to conduct, as is demonstrated by FIGS. 113A-113E. This occurs because any input signal that produces a V_{GS} that cuts-off the n-channel FET 11204 will push the p- channel FET 11218 into conduction. Likewise, any input signal that cuts-off the p-channel FET 11218 will push the n-channel FET 11204 into conduction, and therefore prevent any distortion of the down-converted output signal.

4.3.3 Biased Configurations

FIG. 114 illustrates aliasing module 11400, which is an alternate embodiment of aliasing module 11200. Aliasing module 11400 includes positive voltage supply (V_+) 11402, resistors 11404, 11406, and the elements in aliasing module 11200. V_+ 11402 and resistors 11404,11406 produce a positive DC voltage at node 11405. This allows node 11405 to drive a coupled circuit that requires a positive voltage supply, and enables unipolar supply operation of aliasing module 11400. The positive supply voltage also has the effect of raising the DC level of the input EM signal 11208. As such, any input signal that is within the power supply voltages V_+ 11402 and ground will cause either FET 11204 or FET 11218 to conduct, or cause both FETs to conduct, as will be understood by those skilled in the arts based on the discussion herein.

FIG. 115 illustrates aliasing module 11500, which is an alternate biased configuration of aliasing module 11200. Aliasing module 11500 includes positive voltage supply 11502, negative voltage supply 11508, resistors 11504, 11506, and the elements in aliasing module 11200. The use of both a positive and negative voltage supply allows for node 11505 to be biased anywhere between V_+ 11502 and V-11508 . This allows node 11505 to drive a coupled circuit that requires either a positive or negative supply voltage. Furthermore, any input signal that is within the power supply voltages V_+ 11502 and V-11508 will cause either FET 11204 or FET 11218 to conduct, or cause both

FETs to conduct, as will be understood by those skilled in the arts based on the discussion herein.

4.3.4 Simulation Examples

As stated, an aliasing module with a complementary FET structure offers improved dynamic range when compared with a single (or unipolar) FET configuration. This is further illustrated by comparing the signal waveforms associated aliasing module 11602 (of FIG. 116) which has a complementary FET structure, with that of aliasing module 11702 (of FIG.117) which has a single (or unipolar) FET structure.

Aliasing module 11602 (FIG. 116) down-converts EM signal 11608 using aliasing signal 11612 to generate down-converted signal 11610. Aliasing module 11602 has a complementary FET structure and includes n-channel FET 11604, p-channel FET 11606, inverter 11614, and aliasing signal generator 11608. Aliasing module 11602 is biased by supply circuit 11616 as is shown. Aliasing module 11702 (FIG. 117) down-converts EM signal 11704 using aliasing signal 11708 to generate down-converted signal 11706. Aliasing module 11702 is a single FET structure comprising n-channel FET 11712 and aliasing signal generator 11714, and is biased using voltage supply circuit 11710.

FIGS. 118-120 are signal waveforms that correspond to aliasing module 11602, and FIGS. 121-123 are signal waveforms that correspond to aliasing module 11702. FIGS. 118, 121 are down-converted signals 11610, 11706, respectively. FIGS. 119, 122 are the sampled EM signal 11608, 11704, respectively. FIGS. 120, 123 are the aliasing signals 11612, 11708, respectively. Aliasing signal 11612 is identical to aliasing signal 11708 in order that a proper comparison between modules 11602 and 11702 can be made.

EM signals 11608, 11704 are relatively large input signals that approach the power supply voltages of ± 1.65 volts, as is shown in FIGS. 119, 122, respectively. In FIG. 119, sections 11902 and 11904 of signal 11608 depict energy transfer from EM signal 11608 to down-converted signal 11610 during by aliasing module 11602. More specifically, section 11902 depicts energy transfer near the -1.65v supply, and section 11904 depicts energy transfer near the +1.65v supply. The symmetrical quality of the energy transfer near the voltage supply rails indicates that at least one of complementary FETs 11604, 11606 are appropriately sampling the EM signal during each of the aliasing pulses 11612. This results in a down-converted signal 11610 that has minimal high frequency noise, and is centered between -1.0v and 1.0v (i.e. has negligible DC voltage component).

Similarly in FIG. 122, sections 12202 and 12204 illustrate the energy transfer from EM signal 11704 to down-converted signal 11706 by aliasing module 11702 (single FET configuration). More specifically, section 12202 depicts energy transfer near the -1.65v supply, and section 12204 depicts energy transfer near the +1.65v supply. By comparing sections 12202, 12204 with sections 11902, 11904 of FIG. 119, it is clear that the energy transfer in sections 12202, 12204 is not as symmetrical near the power supply rails as that of sections 11902, 11904. This is evidence that the EM signal 11704 is partially pinching off single FET 11712 over part of the signal 11704 trace. This results in a down-converted signal 11706 that has more high frequency noise when compared to down-converted signal 11610, and has a substantial negative DC voltage component.

In summary, down-converted signal 11706 reflects distortion introduced by a relatively large EM signal that is pinching-off the single FET 11712 in aliasing module 11702. Down-converted signal 11610 that is produced by aliasing module 11602 is relatively distortion free. This occurs because the complementary FET configuration in aliasing module 11602 is

able to handle input signals with large amplitudes without introducing distortion in the down-converted signal 11610. Therefore, the complementary FET configuration in the aliasing module 11602 offers improved dynamic range when compared with the single FET configuration of the aliasing module 11702.

4.4 Optimized Switch Structures

4.4.1 Splitter in CMOS

FIG. 124A illustrates an embodiment of a splitter circuit 12400 implemented in CMOS. This embodiment is provided for illustrative purposes, and is not limiting. In an embodiment, splitter circuit 12400 is used to split a local oscillator (LO) signal into two oscillating signals that are approximately 90° out of phase. The first oscillating signal is called the I-channel oscillating signal. The second oscillating signal is called the Q-channel oscillating signal. The Q-channel oscillating signal lags the phase of the I-channel oscillating signal by approximately 90°. Splitter circuit 12400 includes a first I-channel inverter 12402, a second I-channel inverter 12404, a third I-channel inverter 12406, a first Q-channel inverter 12408, a second Q-channel inverter 12410, an I-channel flip-flop 12412, and a Q-channel flip-flop 12414.

FIGS. 124F-J are example waveforms used to illustrate signal relationships of splitter circuit 12400. The waveforms shown in FIGS. 124F-J reflect ideal delay times through splitter circuit 12400 components. LO signal 12416 is shown in FIG. 124F. First, second, and third I-channel inverters 12402, 12404, and 12406 invert LO signal 12416 three times, outputting inverted LO signal 12418, as shown in FIG. 124G. First and second Q-channel inverters 12408 and 12410 invert LO signal 12416 twice, outputting non-inverted LO signal 12420, as shown in FIG. 124H. The delay through

first, second, and third I-channel inverters 12402, 12404, and 12406 is substantially equal to that through first and second Q-channel inverters 12408 and 12410, so that inverted LO signal 12418 and non-inverted LO signal 12420 are approximately 180° out of phase. The operating characteristics of the inverters may be tailored to achieve the proper delay amounts, as would be understood by persons skilled in the relevant art(s).

I-channel flip-flop 12412 inputs inverted LO signal 12418. Q-channel flip-flop 12414 inputs non-inverted LO signal 12420. In the current embodiment, I-channel flip-flop 12412 and Q-channel flip-flop 12414 are edge-triggered flip-flops. When either flip-flop receives a rising edge on its input, the flip-flop output changes state. Hence, I-channel flip-flop 12412 and Q-channel flip-flop 12414 each output signals that are approximately half of the input signal frequency. Additionally, as would be recognized by persons skilled in the relevant art(s), because the inputs to I-channel flip-flop 12412 and Q-channel flip-flop 12414 are approximately 180° out of phase, their resulting outputs are signals that are approximately 90° out of phase. I-channel flip-flop 12412 outputs I- channel oscillating signal 12422, as shown in FIG. 124I. Q-channel flip-flop 12414 outputs Q-channel oscillating signal 12424, as shown in FIG. 124J. Q-channel oscillating signal 12424 lags the phase of I-channel oscillating signal 12422 by 90°, also as shown in a comparison of FIGS. 124I and 124J.

FIG. 124B illustrates a more detailed circuit embodiment of the splitter circuit 12400 of FIG. 124. The circuit blocks of FIG. 124B that are similar to those of FIG. 124A are indicated by corresponding reference numbers. FIGS. 124C-D show example output waveforms relating to the splitter circuit 12400 of FIG. 124B. FIG. 124C shows I-channel oscillating signal 12422. FIG. 124D shows Q-channel oscillating signal 12424. As is indicated by a comparison of FIGS. 124C and 124D, the waveform of Q-channel oscillating

signal 12424 of FIG. 124D lags the waveform of I-channel oscillating signal 12422 of FIG. 124C by approximately 90°.

It should be understood that the illustration of the splitter circuit 12400 in FIGS. 124A and 124B is for example purposes only. Splitter circuit 12400 may be comprised of an assortment of logic and semiconductor devices of a variety of types, as will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

4.4.2 I/Q Circuit

FIG. 124E illustrates an example embodiment of a complete I/Q circuit 12426 in CMOS. I/Q circuit 12426 includes a splitter circuit 12400 as described in detail above. Further description regarding I/Q circuit implementations are provided herein, including the applications referenced above.

4.5 Example I and Q Implementations

4.5.1 Switches of Different Sizes

In an embodiment, the switch modules discussed herein can be implemented as a series of switches operating in parallel as a single switch. The series of switches can be transistors, such as, for example, field effect transistors (FET), bi-polar transistors, or any other suitable circuit switching devices. The series of switches can be comprised of one type of switching device, or a combination of different switching devices.

For example, FIG. 125 illustrates a switch module 12500. In FIG. 125, the switch module is illustrated as a series of FETs 12502a-n. The FETs 12502a-n can be any type of FET, including, but not limited to, a MOSFET, a JFET, a GaAsFET, etc. Each of FETs 12502a-n includes a gate 12504a-n, a source 12506a-n, and a drain 12508a-n, similarly to that of FET 2802 of FIG.

28A. The series of FETs 12502a-n operate in parallel. Gates 12504a-n are coupled together, sources 12506a-n are coupled together, and drains 12508a-n are coupled together. Each of gates 12504a-n receives the control signal 1604, 8210 to control the switching action between corresponding sources 12506a-n and drains 12508a-n. Generally, the corresponding sources 12506a-n and drains 12508a-n of each of FETs 12502a-n are interchangeable. There is no numerical limit to the number of FETs. Any limitation would depend on the particular application, and the "a-n" designation is not meant to suggest a limit in any way.

In an embodiment, FETs 12502a-n have similar characteristics. In another embodiment, one or more of FETs 12502a-n have different characteristics than the other FETs. For example, FETs 12502a-n may be of different sizes. In CMOS, generally, the larger size a switch is (meaning the larger the area under the gate between the source and drain regions), the longer it takes for the switch to turn on. The longer turn on time is due in part to a higher gate to channel capacitance that exists in larger switches. Smaller CMOS switches turn on in less time, but have a higher channel resistance. Larger CMOS switches have lower channel resistance relative to smaller CMOS switches. Different turn on characteristics for different size switches provides flexibility in designing an overall switch module structure. By combining smaller switches with larger switches, the channel conductance of the overall switch structure can be tailored to satisfy given requirements.

In an embodiment, FETs 12502a-n are CMOS switches of different relative sizes. For example, FET 12502a may be a switch with a smaller size relative to FETs 12502b-n. FET 12502b may be a switch with a larger size relative to FET 12502a, but smaller size relative to FETs 12502c-n. The sizes of FETs 12502c-n also may be varied relative to each other. For instance, progressively larger switch sizes may be used. By varying the sizes of FETs 12502a-n relative to each other, the turn on characteristic curve of the switch

module can be correspondingly varied. For instance, the turn on characteristic of the switch module can be tailored such that it more closely approaches that of an ideal switch. Alternately, the switch module could be tailored to produce a shaped conductive curve.

By configuring FETs 12502a-n such that one or more of them are of a relatively smaller size, their faster turn on characteristic can improve the overall switch module turn on characteristic curve. Because smaller switches have a lower gate to channel capacitance, they can turn on more rapidly than larger switches.

By configuring FETs 12502a-n such that one or more of them are of a relatively larger size, their lower channel resistance also can improve the overall switch module turn on characteristics. Because larger switches have a lower channel resistance, they can provide the overall switch structure with a lower channel resistance, even when combined with smaller switches. This improves the overall switch structure's ability to drive a wider range of loads. Accordingly, the ability to tailor switch sizes relative to each other in the overall switch structure allows for overall switch structure operation to more nearly approach ideal, or to achieve application specific requirements, or to balance trade-offs to achieve specific goals, as will be understood by persons skilled in the relevant arts(s) from the teachings herein.

It should be understood that the illustration of the switch module as a series of FETs 12502a-n in FIG. 125 is for example purposes only. Any device having switching capabilities could be used to implement the switch module (e.g., switch modules 2802, 2702, 2404 and 2406), as will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

4.5.2 Reducing Overall Switch Area

Circuit performance also can be improved by reducing overall switch area. As discussed above, smaller switches (i.e., smaller area under the gate between the source and drain regions) have a lower gate to channel capacitance relative to larger switches. The lower gate to channel capacitance allows for lower circuit sensitivity to noise spikes. FIG. 126A illustrates an embodiment of a switch module, with a large overall switch area. The switch module of FIG. 126A includes twenty FETs 12602-12640. As shown, FETs 12602-12640 are the same size ("Wd" and "lng" parameters are equal). Input source 12646 produces the input EM signal. Pulse generator 12648 produces the energy transfer signal for FETs 12602-12640. Capacitor C1 is the storage element for the input signal being sampled by FETs 12602-12640. FIGS. 126B-126Q illustrate example waveforms related to the switch module of FIG. 126A. FIG. 126B shows a received 1.01 GHz EM signal to be sampled and downconverted to a 10 MHZ intermediate frequency signal. FIG. 126C shows an energy transfer signal having an aliasing rate of 200 MHZ, which is applied to the gate of each of the twenty FETs 12602-12640. The energy transfer signal includes a train of energy transfer pulses having non-negligible apertures that tend away from zero time in duration. The energy transfer pulses repeat at the aliasing rate. FIG. 126D illustrates the affected received EM signal, showing effects of transferring energy at the aliasing rate, at point 12642 of FIG. 126A. FIG. 126E illustrates a down-converted signal at point 12644 of FIG. 126A, which is generated by the down-conversion process.

FIG. 126F illustrates the frequency spectrum of the received 1.01 GHz EM signal. FIG. 126G illustrates the frequency spectrum of the received energy transfer signal. FIG. 126H illustrates the frequency spectrum of the affected received EM signal at point 12642 of FIG. 126A. FIG. 126I illustrates the frequency spectrum of the down-converted signal at point 12644 of FIG. 126A.

FIGS. 126J-126M respectively further illustrate the frequency spectrums of the received 1.01 GHz EM signal, the received energy transfer signal, the affected received EM signal at point 12642 of FIG. 126A, and the down-converted signal at point 12644 of FIG. 126A, focusing on a narrower frequency range centered on 1.00 GHz. As shown in FIG. 126L, a noise spike exists at approximately 1.0 GHz on the affected received EM signal at point 12642 of FIG. 126A. This noise spike may be radiated by the circuit, causing interference at 1.0 GHz to nearby receivers.

FIGS. 126N-126Q respectively illustrate the frequency spectrums of the received 1.01 GHz EM signal, the received energy transfer signal, the affected received EM signal at point 12642 of FIG. 126A, and the down-converted signal at point 12644 of FIG. 126A, focusing on a narrow frequency range centered near 10.0 MHZ. In particular, FIG. 126Q shows that an approximately 5 mV signal was downconverted at approximately 10 MHZ.

FIG 127A illustrates an alternative embodiment of the switch module, this time with fourteen FETs 12702-12728 shown, rather than twenty FETs 12602-12640 as shown in FIG. 126A. Additionally, the FETs are of various sizes (some "Wd" and "lng" parameters are different between FETs).

FIGS. 127B-127Q, which are example waveforms related to the switch module of FIG. 127A, correspond to the similarly designated figures of FIGS. 126B-126Q. As FIG. 127L shows, a lower level noise spike exists at 1.0 GHz than at the same frequency of FIG. 126L. This correlates to lower levels of circuit radiation. Additionally, as FIG. 127Q shows, the lower level noise spike at 1.0 GHz was achieved with no loss in conversion efficiency. This is represented in FIG. 127Q by the approximately 5 mV signal downconverted at approximately 10 MHZ. This voltage is substantially equal to the level downconverted by the circuit of FIG. 126A. In effect, by decreasing the number of switches, which decreases overall switch area, and by reducing switch area on a switch-by-switch basis, circuit parasitic

capacitance can be reduced, as would be understood by persons skilled in the relevant art(s) from the teachings herein. In particular this may reduce overall gate to channel capacitance, leading to lower amplitude noise spikes and reduced unwanted circuit radiation.

It should be understood that the illustration of the switches above as FETs in FIGSs. 126A-126Q and 127A-127Q is for example purposes only. Any device having switching capabilities could be used to implement the switch module, as will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

4.5.3 Charge Injection Cancellation

In embodiments wherein the switch modules discussed herein are comprised of a series of switches in parallel, in some instances it may be desirable to minimize the effects of charge injection. Minimizing charge injection is generally desirable in order to reduce the unwanted circuit radiation resulting therefrom. In an embodiment, unwanted charge injection effects can be reduced through the use of complementary n-channel MOSFETs and p-channel MOSFETs. N-channel MOSFETs and p-channel MOSFETs both suffer from charge injection. However, because signals of opposite polarity are applied to their respective gates to turn the switches on and off, the resulting charge injection is of opposite polarity. Resultingly, n-channel MOSFETs and p-channel MOSFETs may be paired to cancel their corresponding charge injection. Hence, in an embodiment, the switch module may be comprised of n-channel MOSFETs and p-channel MOSFETS, wherein the members of each are sized to minimize the undesired effects of charge injection.

FIG 129A illustrates an alternative embodiment of the switch module, this time with fourteen n-channel FETs 12902-12928 and twelve p-channel FETs 12930-12952 shown, rather than twenty FETs 12602-12640 as shown in

FIG. 126A. The n-channel and p-channel FETs are arranged in a complementary configuration. Additionally, the FETs are of various sizes (some "Wd" and "lng" parameters are different between FETs).

FIGS. 129B-129Q, which are example waveforms related to the switch module of FIG. 129A, correspond to the similarly designated figures of FIGS. 126B-126Q. As FIG. 129L shows, a lower level noise spike exists at 1.0 GHz than at the same frequency of FIG. 126L. This correlates to lower levels of circuit radiation. Additionally, as FIG. 129Q shows, the lower level noise spike at 1.0 GHz was achieved with no loss in conversion efficiency. This is represented in FIG. 129Q by the approximately 5 mV signal downconverted at approximately 10 MHZ. This voltage is substantially equal to the level downconverted by the circuit of FIG. 126A. In effect, by arranging the switches in a complementary configuration, which assists in reducing charge injection, and by tailoring switch area on a switch-by-switch basis, the effects of charge injection can be reduced, as would be understood by persons skilled in the relevant art(s) from the teachings herein. In particular this leads to lower amplitude noise spikes and reduced unwanted circuit radiation.

It should be understood that the use of FETs in FIGSs. 129A-129Q in the above description is for example purposes only. From the teachings herein, it would be apparent to persons of skill in the relevant art(s) to manage charge injection in various transistor technologies using transistor pairs.

4.5.4 Overlapped Capacitance

The processes involved in fabricating semiconductor circuits, such as MOSFETs, have limitations. In some instances, these process limitations may lead to circuits that do not function as ideally as desired. For instance, a non-ideally fabricated MOSFET may suffer from parasitic capacitances, which in some cases may cause the surrounding circuit to radiate noise. By fabricating

circuits with structure layouts as close to ideal as possible, problems of non-ideal circuit operation can be minimized.

FIG. 128A illustrates a cross-section of an example n-channel enhancement-mode MOSFET 12800, with ideally shaped n+ regions. MOSFET 12800 includes a gate 12802, a channel region 12804, a source contact 12806, a source region 12808, a drain contact 12810, a drain region 12812, and an insulator 12814. Source region 12808 and drain region 12812 are separated by p-type material of channel region 12804. Source region 12808 and drain region 12812 are shown to be n+ material. The n+ material is typically implanted in the p-type material of channel region 12804 by an ion implantation/diffusion process. Ion implantation/diffusion processes are well known by persons skilled in the relevant art(s). Insulator 12814 insulates gate 12802 which bridges over the p-type material. Insulator 12814 generally comprises a metal-oxide insulator. The channel current between source region 12808 and drain region 12812 for MOSFET 12800 is controlled by a voltage at gate 12802.

Operation of MOSFET 12800 shall now be described. When a positive voltage is applied to gate 12802, electrons in the p-type material of channel region 12804 are attracted to the surface below insulator 12814, forming a connecting near-surface region of n-type material between the source and the drain, called a channel. The larger or more positive the voltage between the gate contact 12806 and source region 12808, the lower the resistance across the region between.

In FIG. 128A, source region 12808 and drain region 12812 are illustrated as having n+ regions that were formed into idealized rectangular regions by the ion implantation process. FIG. 128B illustrates a cross-section of an example n-channel enhancement-mode MOSFET 12816 with non-ideally shaped n+ regions. Source region 12820 and drain region 12822 are illustrated as being formed into irregularly shaped regions by the ion

implantation process. Due to uncertainties in the ion implantation/diffusion process, in practical applications, source region 12820 and drain region 12822 do not form rectangular regions as shown in FIG. 128A. FIG. 128B shows source region 12820 and drain region 12822 forming exemplary irregular regions. Due to these process uncertainties, the n+ regions of source region 12820 and drain region 12822 also may diffuse further than desired into the p-type region of channel region 12818, extending underneath gate 12802 The extension of the source region 12820 and drain region 12822 underneath gate 12802 is shown as source overlap 12824 and drain overlap 12826. Source overlap 12824 and drain overlap 12826 are further illustrated in FIG. 128C. FIG. 128C illustrates a top-level view of an example layout configuration for MOSFET 12816. Source overlap 12824 and drain overlap 12826 may lead to unwanted parasitic capacitances between source region 12820 and gate 12802, and between drain region 12822 and gate 12802. These unwanted parasitic capacitances may interfere with circuit function. For instance, the resulting parasitic capacitances may produce noise spikes that are radiated by the circuit, causing unwanted electromagnetic interference.

As shown in FIG. 128C, an example MOSFET 12816 may include a gate pad 12828. Gate 12802 may include a gate extension 12830, and a gate pad extension 12832. Gate extension 12830 is an unused portion of gate 12802 required due to metal implantation process tolerance limitations. Gate pad extension 12832 is a portion of gate 12802 used to couple gate 12802 to gate pad 12828. The contact required for gate pad 12828 requires gate pad extension 12832 to be of non-zero length to separate the resulting contact from the area between source region 12820 and drain region 12822. This prevents gate 12802 from shorting to the channel between source region 12820 and drain region 12822 (insulator 12814 of FIG. 128B is very thin in this region). Unwanted parasitic capacitances may form between gate extension 12830 and the substrate (FET 12816 is fabricated on a substrate), and between gate pad

extension 12832 and the substrate. By reducing the respective areas of gate extension 12830 and gate pad extension 12832, the parasitic capacitances resulting therefrom can be reduced. Accordingly, embodiments address the issues of uncertainty in the ion implantation/diffusion process. it will be obvious to persons skilled in the relevant art(s) how to decrease the areas of gate extension 12830 and gate pad extension 12832 in order to reduce the resulting parasitic capacitances.

It should be understood that the illustration of the n-channel enhancement-mode MOSFET is for example purposes only. The present invention is applicable to depletion mode MOSFETs, and other transistor types, as will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

4.6 Other Implementations

The implementations described above are provided for purposes of illustration. These implementations are not intended to limit the invention. Alternate implementations, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

5. Optional Optimizations of Energy Transfer at an Aliasing Rate

The methods and systems described in sections above can be optimized with one or more of the optimization methods or systems described below.

5.1 Doubling the Aliasing Rate (FAR) of the Energy Transfer Signal

In an embodiment, the optional energy transfer signal module 6902 in FIG. 69 includes a pulse generator module that generates aliasing pulses at twice the frequency of the oscillating source. The input signal 6828 may be any suitable oscillating source.

FIG. 71A illustrates a circuit 7102 that generates a doubler output signal 7104 (FIG. 71C) that may be used as an energy transfer signal 6306. The circuit 7102 generates pulses on both rising and falling edges of the input oscillating signal 7106 of FIG. 71B. The circuit 7102 can be implemented as a pulse generator and aliasing rate (F_{AR}) doubler. The doubler output signal 7104 can be used as the energy transfer signal 6306.

In the example of FIG. 71A, the aliasing rate is twice the frequency of the input oscillating signal F_{osc} 7106, as shown by EQ. (9) below.

$$F_{AR} = 2 \bullet F_{osc} \qquad \text{EQ. (9)}$$

The aperture width of the aliasing pulses is determined by the delay through a first inverter 7108 of FIG. 71A. As the delay is increased, the aperture is increased. A second inverter 7112 is shown to maintain polarity consistency with examples described elsewhere. In an alternate embodiment inverter 7112 is omitted. Preferably, the pulses have non-negligible aperture widths that tend away from zero time. The doubler output signal 7104 may be further conditioned as appropriate to drive the switch module with non-negligible aperture pulses. The circuit 7102 may be implemented with integrated circuitry, discretely, with equivalent logic circuitry, or with any valid fabrication technology.

5.2 Differential Implementations

The invention can be implemented in a variety of differential configurations. Differential configurations are useful for reducing common mode noise. This can be very useful in receiver systems where common mode interference can be caused by intentional or unintentional radiators such as cellular phones, CB radios, electrical appliances etc.. Differential configurations are also useful in reducing any common mode noise due to charge injection of the switch in the switch module or due to the design and layout of the system in which the invention is used. Any spurious signal that is induced in equal magnitude and equal phase in both input leads of the invention will be substantially reduced or eliminated. Some differential configurations, including some of the configurations below, are also useful for increasing the voltage and/or for increasing the power of the down-converted signal 1308B.

Differential systems are most effective when used with a differential front end (inputs) and a differential back end (outputs). They can also be utilized in the following configurations, for example:

a) A single-input front end and a differential back end; and

b) A differential front end and a single-output back end.

Examples of these system are provided below, with a first example illustrating a specific method by which energy is transferred from the input to the output differentially..

While an example of a differential energy transfer module is shown below, the example is shown for the purpose of illustration, not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations etc.) of the embodiment described herein will be apparent to those skilled in the relevant art based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

5.2.1 An Example Illustrating Energy Transfer Differentially

FIG.76A illustrates a differential system 7602 that can be included in the energy transfer module 6304. The differential system 7602 includes an inverted gated transfer design similar to that described with reference to FIG. 74. The differential system 7602 includes inputs 7604 and 7606 and outputs 7608 and 7610. The differential system 7602 includes a first inverted gated transfer module 7612, which includes a storage module 7614 and a switch module 7616. The differential system 7602 also includes a second inverted gated transfer module 7618, which includes a storage module 7620 and a switch module 7616, which it shares in common with inverted gated transfer module 7612.

One or both of the inputs 7604 and 7606 are coupled to an EM signal source. For example, the inputs can be coupled to an EM signal source, wherein the input voltages at the inputs 7604 and 7606 are substantially equal in amplitude but 180 degrees out of phase with one another. Alternatively, where dual inputs are unavailable, one of the inputs 7604 and 7606 can be coupled to ground.

In operation, when the switch module 7616 is closed, the storage modules 7614 and 7620 are in series and, provided they have similar capacitive values, accumulate charge of equal magnitude but opposite polarities. When the switch module 7616 is open, the voltage at the output 7608 is relative to the input 7604, and the voltage at the output 7610 is relative to the voltage at the input 7606.

Portions of the signals at the outputs 7608 and 7610 include signals resulting from energy stored in the storage modules 7614 and 7620, respectively, when the switch module 7616 was closed. The portions of the signals at the outputs 7608 and 7610 resulting from the stored charge are generally equal in amplitude to one another but 180 degrees out of phase.

Portions of the signals at the outputs 7608 and 7610 also include ripple voltage or noise resulting from the switching action of the switch module 7616. But because the switch module is positioned between the two outputs 7608 and 7610, the noise introduced by the switch module appears at the outputs as substantially equal and in-phase with one another. As a result, the ripple voltage can be substantially canceled out by inverting the signal at one of the outputs 7608 or 7610 and adding it to the other remaining output. Additionally, any noise that is impressed with equal amplitude and equal phase onto the input terminals 7604 and 7606 by any other noise sources will tend to be canceled in the same way.

5.2.1.1 Differential Input-to-Differential Output

FIG. 76B illustrates the differential system 7602 wherein the inputs 7604 and 7606 are coupled to equal and opposite EM signal sources, illustrated here as dipole antennas 7624 and 7626. In this embodiment, when one of the outputs 7608 or 7610 is inverted and added to the other output, the common mode noise due to the switching module 7616 and other common mode noise present at the input terminals 7604 and 7606 tend to substantially cancel out.

5.2.1.2 Single Input-to-Differential Output

FIG. 76C illustrates the differential system 7602 wherein the input 7604 is coupled to an EM signal source such as a monopole antenna 7628 and the input 7606 is coupled to ground. In this configuration, the voltages at the outputs 7608 and 7610 are approximately one half the value of the voltages at the outputs in the implementation illustrated in FIG. 76B, given all other parameters are equal.

FIG. 76E illustrates an example single input to differential output receiver/down-converter system 7636. The system 7636 includes the differential system 7602 wherein the input 7606 is coupled to ground as in FIG. 76C. The input 7604 is coupled to an EM signal source 7638 through an optional input impedance match 7642. The EM signal source impedance can be matched with an impedance match system 7642 as described in section 5 below.

The outputs 7608 and 7610 are coupled to a differential circuit 7644 such as a filter, which preferably inverts one of the outputs 7608 or 7610 and adds it to the other output 7608 or 7610. This substantially cancels common mode noise generated by the switch module 7616. The differential circuit 7644 preferably filters the higher frequency components of the EM signal 1304 that pass through the storage modules 7614 and 7620. The resultant filtered signal is output as the down-converted signal 1308B.

5.2.1.3 Differential Input-to-Single Output

FIG. 76D illustrates the differential input to single output system 7629 wherein the inputs 7604 and 7606 of the differential system 7602 are coupled to equal and opposite EM signal dipole antennas 7630 and 7632. In system 7629, the common mode noise voltages are not canceled as in systems shown above. The output is coupled from terminal 7608 to a load 7648.

5.2.2 Specific Alternative Embodiments

In specific alternative embodiments, the present invention is implemented using a plurality of gated transfer modules controlled by a common energy transfer signal with a storage module coupled between the outputs of the plurality of gated transfer modules. For example, FIG. 99 illustrates a differential system 9902 that includes first and second gated

transfer modules 9904 and 9906, and a storage module 9908 coupled between. Operation of the differential system 9902 will be apparent to one skilled in the relevant art(s), based on the description herein.

As with the first implementation described above in section 5.5.1 and its sub-sections, the gated transfer differential system 9902 can be implemented with a single input, differential inputs, a single output, differential outputs, and combinations thereof. For example, FIG. 100 illustrates an example single input-to-differential output system 10002.

Where common-mode rejection is desired to protect the input from various common-mode effects, and where common mode rejection to protect the output is not necessary, a differential input-to-single output implementation can be utilized. FIG. 102 illustrates an example differential-to-single ended system 10202, where a balance/unbalance (balun) circuit 10204 is utilized to generate the differential input. Other input configurations are contemplated. A first output 10206 is coupled to a load 10208. A second output 10210 is coupled to ground point 10212.

Typically, in a balanced-to-unbalanced system, where a single output is taken from a differential system without the use of a balun, (i.e., where one of the output signals is grounded), a loss of about 6 db is observed. In the configuration of FIG. 102, however, the ground point 10212 simply serves as a DC voltage reference for the circuit. The system 10202 transfers charge from the input in the same manner as if it were full differential, with its conversion efficiency generally affected only by the parasitics of the circuit components used, such as the Rds(on) on FET switches if used in the switch module. In other words, the charge transfer still continues in the same manner of a single ended implementation, providing the necessary single-ended ground to the input circuitry when the aperture is active, yet configured to allow the input to be differential for specific common-mode rejection capability and/or interface between a differential input and a single ended output system.

5.2.3 Specific Examples of Optimizations and Configurations for Inverted and Non-Inverted Differential Designs

Gated transfer systems and inverted gated transfer systems can be implemented with any of the various optimizations and configurations disclosed through the specification, such as, for example, impedance matching, tanks and resonant structures, bypass networks, etc. For example, the differential system 10002 in FIG. 100 , which utilizes gated transfer modules with an input impedance matching system 10004 and a tank circuit 10006, which share a common capacitor. Similarly, differential system 10102 in FIG. 101 , utilizes an inverted gated transfer module with an input impedance matching system 10104 and a tank circuit 10106, which share a common capacitor.

5.3 Smoothing the Down-Converted Signal

The down-converted signal 1308B may be smoothed by filtering as desired. The differential circuit 7644 implemented as a filter in FIG 76E illustrates but one example. This may be accomplished in any of the described embodiments by hardware, firmware and software implementation as is well known by those skilled in the arts.

5.4 Impedance Matching

The energy transfer module has input and output impedances generally defined by (1) the duty cycle of the switch module, and (2) the impedance of the storage module, at the frequencies of interest (e.g. at the EM input, and intermediate/baseband frequencies).

Starting with an aperture width of approximately ½ the period of the EM signal being down-converted as a preferred embodiment, this aperture

width (e.g. the "closed time") can be decreased. As the aperture width is decreased, the characteristic impedance at the input and the output of the energy transfer module increases. Alternatively, as the aperture width increases from ½ the period of the EM signal being down-converted, the impedance of the energy transfer module decreases.

One of the steps in determining the characteristic input impedance of the energy transfer module could be to measure its value. In an embodiment, the energy transfer module's characteristic input impedance is 300 ohms. An impedance matching circuit can be utilized to efficiently couple an input EM signal that has a source impedance of, for example, 50 ohms, with the energy transfer module's impedance of, for example, 300 ohms. Matching these impedances can be accomplished in various manners, including providing the necessary impedance directly or the use of an impedance match circuit as described below.

Referring to FIG. 70, a specific embodiment using an RF signal as an input, assuming that the impedance 7012 is a relatively low impedance of approximately 50 Ohms, for example, and the input impedance 7016 is approximately 300 Ohms, an initial configuration for the input impedance match module 7006 can include an inductor 7306 and a capacitor 7308, configured as shown in FIG. 73. The configuration of the inductor 7306 and the capacitor 7308 is a possible configuration when going from a low impedance to a high impedance. Inductor 7306 and the capacitor 7308 constitute an L match, the calculation of the values which is well known to those skilled in the relevant arts.

The output characteristic impedance can be impedance matched to take into consideration the desired output frequencies. One of the steps in determining the characteristic output impedance of the energy transfer module could be to measure its value. Balancing the very low impedance of the storage module at the input EM frequency, the storage module should have an

impedance at the desired output frequencies that is preferably greater than or equal to the load that is intended to be driven (for example, in an embodiment, storage module impedance at a desired 1MHz output frequency is 2K ohm and the desired load to be driven is 50 ohms). An additional benefit of impedance matching is that filtering of unwanted signals can also be accomplished with the same components.

In an embodiment, the energy transfer module's characteristic output impedance is 2K ohms. An impedance matching circuit can be utilized to efficiently couple the down-converted signal with an output impedance of, for example, 2K ohms, to a load of, for example, 50 ohms. Matching these impedances can be accomplished in various manners, including providing the necessary load impedance directly or the use of an impedance match circuit as described below.

When matching from a high impedance to a low impedance, a capacitor 7314 and an inductor 7316 can be configured as shown in FIG. 73. The capacitor 7314 and the inductor 7316 constitute an L match, the calculation of the component values being well known to those skilled in the relevant arts.

The configuration of the input impedance match module 7006 and the output impedance match module 7008 are considered to be initial starting points for impedance matching, in accordance with the present invention. In some situations, the initial designs may be suitable without further optimization. In other situations, the initial designs can be optimized in accordance with other various design criteria and considerations.

As other optional optimizing structures and/or components are utilized, their affect on the characteristic impedance of the energy transfer module should be taken into account in the match along with their own original criteria.

5.5 Tanks and Resonant Structures

Resonant tank and other resonant structures can be used to further optimize the energy transfer characteristics of the invention. For example, resonant structures, resonant about the input frequency, can be used to store energy from the input signal when the switch is open, a period during which one may conclude that the architecture would otherwise be limited in its maximum possible efficiency. Resonant tank and other resonant structures can include, but are not limited to, surface acoustic wave (SAW) filters, dielectric resonators, diplexers, capacitors, inductors, etc.

An example embodiment is shown in FIG. 94A. Two additional embodiments are shown in FIG. 88 and FIG. 97. Alternate implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Alternate implementations fall within the scope and spirit of the present invention. These implementations take advantage of properties of series and parallel (tank) resonant circuits.

FIG. 94A illustrates parallel tank circuits in a differential implementation. A first parallel resonant or tank circuit consists of a capacitor 9438 and an inductor 9420 (tank1). A second tank circuit consists of a capacitor 9434 and an inductor 9436 (tank2).

As is apparent to one skilled in the relevant art(s), parallel tank circuits provide:

low impedance to frequencies below resonance;
low impedance to frequencies above resonance; and
high impedance to frequencies at and near resonance.

In the illustrated example of FIG. 94A, the first and second tank circuits resonate at approximately 920Mhz. At and near resonance, the impedance of these circuits is relatively high. Therefore, in the circuit configuration shown in FIG 94A, both tank circuits appear as relatively high

impedance to the input frequency of 950Mhz, while simultaneously appearing as relatively low impedance to frequencies in the desired output range of 50Mhz.

An energy transfer signal 9442 controls a switch 9414. When the energy transfer signal 9442 controls the switch 9414 to open and close, high frequency signal components are not allowed to pass through tank1 or tank2. However, the lower signal components (50Mhz in this embodiment) generated by the system are allowed to pass through tank1 and tank2 with little attenuation. The effect of tank1 and tank2 is to further separate the input and output signals from the same node thereby producing a more stable input and output impedance. Capacitors 9418 and 9440 act to store the 50Mhz output signal energy between energy transfer pulses.

Further energy transfer optimization is provided by placing an inductor 9410 in series with a storage capacitor 9412 as shown. In the illustrated example, the series resonant frequency of this circuit arrangement is approximately 1 GHz. This circuit increases the energy transfer characteristic of the system. The ratio of the impedance of inductor 9410 and the impedance of the storage capacitor 9412 is preferably kept relatively small so that the majority of the energy available will be transferred to storage capacitor 9412 during operation. Exemplary output signals A and B are illustrated in FIGS. 94B and 94C, respectively.

In FIG. 94A, circuit components 9404 and 9406 form an input impedance match. Circuit components 9432 and 9430 form an output impedance match into a 50 ohm resistor 9428. Circuit components 9422 and 9424 form a second output impedance match into a 50 ohm resistor 9426. Capacitors 9408 and 9412 act as storage capacitors for the embodiment. Voltage source 9446 and resistor 9402 generate a 950Mhz signal with a 50ohm output impedance, which are used as the input to the circuit. Circuit

element 9416 includes a 150Mhz oscillator and a pulse generator, which are used to generate the energy transfer signal 9442.

FIG. 88 illustrates a shunt tank circuit 8810 in a single-ended to-single-ended system 8812. Similarly, FIG. 97 illustrates a shunt tank circuit 9710 in a system 9712. The tank circuits 8810 and 9710 lower driving source impedance, which improves transient response. The tank circuits 8810 and 9710 are able store the energy from the input signal and provide a low driving source impedance to transfer that energy throughout the aperture of the closed switch. The transient nature of the switch aperture can be viewed as having a response that, in addition to including the input frequency, has large component frequencies above the input frequency, (i.e. higher frequencies than the input frequency are also able to effectively pass through the aperture). Resonant circuits or structures, for example resonant tanks 8810 or 9710, can take advantage of this by being able to transfer energy throughout the switch's transient frequency response (i.e. the capacitor in the resonant tank appears as a low driving source impedance during the transient period of the aperture).

The example tank and resonant structures described above are for illustrative purposes and are not limiting. Alternate configurations can be utilized. The various resonant tanks and structures discussed can be combined or utilized independently as is now apparent.

5.6 Charge and Power Transfer Concepts

Concepts of charge transfer are now described with reference to FIGS. 109A-F. FIG. 109A illustrates a circuit 10902, including a switch S and a capacitor 10906 having a capacitance C. The switch S is controlled by a control signal 10908, which includes pulses 19010 having apertures T.

In FIG. 109B, Equation 10 illustrates that the charge q on a capacitor having a capacitance C, such as the capacitor 10906, is proportional to the voltage V across the capacitor, where:

q = Charge in Coulombs

C = Capacitance in Farads

V = Voltage in Volts

A = Input Signal Amplitude

Where the voltage V is represented by Equation 11, Equation 10 can be rewritten as Equation 12. The change in charge Δq over time t is illustrated as in Equation 13 as $\Delta q(t)$, which can be rewritten as Equation 14. Using the sum-to-product trigonometric identity of Equation 15, Equation 14 can be rewritten as Equation 16, which can be rewritten as equation 17.

Note that the sin term in Equation 11 is a function of the aperture T only. Thus, $\Delta q(t)$ is at a maximum when T is equal to an odd multiple of π (i.e., π, 3π, 5π, . . .). Therefore, the capacitor 10906 experiences the greatest change in charge when the aperture T has a value of π or a time interval representative of 180 degrees of the input sinusoid. Conversely, when T is equal to 2π, 4π, 6π, . . ., minimal charge is transferred.

Equations 18, 19, and 20 solve for q(t) by integrating Equation 10, allowing the charge on the capacitor 10906 with respect to time to be graphed on the same axis as the input sinusoid sin(t), as illustrated in the graph of FIG. 109C. As the aperture T decreases in value or tends toward an impulse, the phase between the charge on the capacitor C or q(t) and sin(t) tend toward zero. This is illustrated in the graph of FIG. 109D, which indicates that the maximum impulse charge transfer occurs near the input voltage maxima. As this graph indicates, considerably less charge is transferred as the value of T decreases.

Power/charge relationships are illustrated in Equations 21-26 of FIG. 109E, where it is shown that power is proportional to charge, and transferred charge is inversely proportional to insertion loss.

Concepts of insertion loss are illustrated in FIG. 109F. Generally, the noise figure of a lossy passive device is numerically equal to the device insertion loss. Alternatively, the noise figure for any device cannot be less that its insertion loss. Insertion loss can be expressed by Equation 27 or 28.

From the above discussion, it is observed that as the aperture T increases, more charge is transferred from the input to the capacitor 10906, which increases power transfer from the input to the output. It has been observed that it is not necessary to accurately reproduce the input voltage at the output because relative modulated amplitude and phase information is retained in the transferred power.

5.7 Optimizing and Adjusting the Non-Negligible Aperture Width/Duration

5.7.1 Varying Input and Output Impedances

In an embodiment of the invention, the energy transfer signal 6306 of FIG.63 is used to vary the input impedance seen by the EM Signal 1304 and to vary the output impedance driving a load. An example of this embodiment is described below using the gated transfer module 6404 shown in FIG. 68G, and in FIG. 82A. The method described below is not limited to the gated transfer module 6404, as it can be applied to all of the embodiments of energy transfer module 6304.

In FIG. 82A, when switch 8206 is closed, the impedance looking into circuit 8202 is substantially the impedance of storage module illustrated as the storage capacitance 8208, in parallel with the impedance of the load 8212. When the switch 8206 is open, the impedance at point 8214 approaches infinity. It follows that the average impedance at point 8214 can be varied from the impedance of the storage module illustrated as the storage capacitance 8208, in parallel with the load 8212, to the highest obtainable impedance when switch 8206 is open, by varying the ratio of the time that

switch 8206 is open to the time switch 8206 is closed. Since the switch 8206 is controlled by the energy transfer signal 8210, the impedance at point 8214 can be varied by controlling the aperture width of the energy transfer signal, in conjunction with the aliasing rate.

An example method of altering the energy transfer signal 6306 of FIG. 63 is now described with reference to FIG. 71A, where the circuit 7102 receives the input oscillating signal 7106 and outputs a pulse train shown as doubler output signal 7104. The circuit 7102 can be used to generate the energy transfer signal 6306. Example waveforms of 7104 are shown on FIG. 71C.

It can be shown that by varying the delay of the signal propagated by the inverter 7108, the width of the pulses in the doubler output signal 7104 can be varied. Increasing the delay of the signal propagated by inverter 7108, increases the width of the pulses. The signal propagated by inverter 7108 can be delayed by introducing a R/C low pass network in the output of inverter 7108. Other means of altering the delay of the signal propagated by inverter 7108 will be well known to those skilled in the art.

5.7.2 Real Time Aperture Control

In an embodiment, the aperture width/duration is adjusted in real time. For example, referring to the timing diagrams in FIGS. 98B-F, a clock signal 9814 (FIG. 98B) is utilized to generate an energy transfer signal9816 (FIG. 98F), which includes energy transfer pluses 9818, having variable apertures 9820. In an embodiment, the clock signal 9814 is inverted as illustrated by inverted clock signal 9822 (FIG. 98D). The clock signal 9814 is also delayed, as illustrated by delayed clock signal 9824 (FIG. 98E). The inverted clock signal 9814 and the delayed clock signal 9824 are then ANDed together, generating an energy transfer signal 9816, which is active - energy transfer pulses 9818 - when the delayed clock signal 9824 and the inverted clock signal

9822 are both active. The amount of delay imparted to the delayed clock signal 9824 substantially determines the width or duration of the apertures 9820. By varying the delay in real time, the apertures are adjusted in real time.

In an alternative implementation, the inverted clock signal 9822 is delayed relative to the original clock signal 9814, and then ANDed with the original clock signal 9814. Alternatively, the original clock signal 9814 is delayed then inverted, and the result ANDed with the original clock signal 9814.

FIG. 98A illustrates an exemplary real time aperture control system 9802 that can be utilized to adjust apertures in real time. The example real time aperture control system 9802 includes an RC circuit 9804, which includes a voltage variable capacitor 9812 and a resistor 9826. The real time aperture control system 9802 also includes an inverter 9806 and an AND gate 9808. The AND gate 9808 optionally includes an enable input 9810 for enabling/disabling the AND gate 9808. The RC circuit 9804. The real time aperture control system 9802 optionally includes an amplifier 9828.

Operation of the real time aperture control circuit is described with reference to the timing diagrams of FIGS. 98B-F. The real time control system 9802 receives the input clock signal 9814, which is provided to both the inverter 9806 and to the RC circuit 9804. The inverter 9806 outputs the inverted clock signal 9822 and presents it to the AND gate 9808. The RC circuit 9804 delays the clock signal 9814 and outputs the delayed clock signal 9824. The delay is determined primarily by the capacitance of the voltage variable capacitor 9812. Generally, as the capacitance decreases, the delay decreases.

The delayed clock signal 9824 is optionally amplified by the optional amplifier 9828, before being presented to the AND gate 9808. Amplification is desired, for example, where the RC constant of the RC circuit 9804 attenuates the signal below the threshold of the AND gate 9808.

The AND gate 9808 ANDs the delayed clock signal 9824, the inverted clock signal 9822, and the optional Enable signal 9810, to generate the energy transfer signal 9816. The apertures 9820 are adjusted in real time by varying the voltage to the voltage variable capacitor 9812.

In an embodiment, the apertures 9820 are controlled to optimize power transfer. For example, in an embodiment, the apertures 9820 are controlled to maximize power transfer. Alternatively, the apertures 9820 are controlled for variable gain control (e.g. automatic gain control - AGC). In this embodiment, power transfer is reduced by reducing the apertures 9820.

As can now be readily seen from this disclosure, many of the aperture circuits presented, and others, can be modified in the manner described above (e.g. circuits in FIGS. 68 H-K). Modification or selection of the aperture can be done at the design level to remain a fixed value in the circuit, or in an alternative embodiment, may be dynamically adjusted to compensate for, or address, various design goals such as receiving RF signals with enhanced efficiency that are in distinctively different bands of operation, e.g. RF signals at 900MHz and 1.8GHz.

5.8 Adding a Bypass Network

In an embodiment of the invention, a bypass network is added to improve the efficiency of the energy transfer module. Such a bypass network can be viewed as a means of synthetic aperture widening. Components for a bypass network are selected so that the bypass network appears substantially lower impedance to transients of the switch module (i.e., frequencies greater than the received EM signal) and appears as a moderate to high impedance to the input EM signal (e.g., greater that 100 Ohms at the RF frequency).

The time that the input signal is now connected to the opposite side of the switch module is lengthened due to the shaping caused by this network, which in simple realizations may be a capacitor or series resonant inductor-

capacitor. A network that is series resonant above the input frequency would be a typical implementation. This shaping improves the conversion efficiency of an input signal that would otherwise, if one considered the aperture of the energy transfer signal only, be relatively low in frequency to be optimal.

For example, referring to FIG. 95 a bypass network 9502 (shown in this instance as capacitor 9512), is shown bypassing switch module 9504. In this embodiment the bypass network increases the efficiency of the energy transfer module when, for example, less than optimal aperture widths were chosen for a given input frequency on the energy transfer signal 9506. The bypass network 9502 could be of different configurations than shown in FIG 95. Such an alternate is illustrated in FIG.90. Similarly, FIG. 96 illustrates another example bypass network 9602, including a capacitor 9604.

The following discussion will demonstrate the effects of a minimized aperture and the benefit provided by a bypassing network. Beginning with an initial circuit having a 550ps aperture in FIG. 103, its output is seen to be 2.8mVpp applied to a 50 ohm load in FIG. 107A. Changing the aperture to 270ps as shown in FIG. 104 results in a diminished output of 2.5Vpp applied to a 50 ohm load as shown in FIG. 107B. To compensate for this loss, a bypass network may be added, a specific implementation is provided in FIG. 105. The result of this addition is that 3.2Vpp can now be applied to the 50 ohm load as shown in FIG. 108A. The circuit with the bypass network in FIG. 105 also had three values adjusted in the surrounding circuit to compensate for the impedance changes introduced by the bypass network and narrowed aperture. FIG. 106 verifies that those changes added to the circuit, but without the bypass network, did not themselves bring about the increased efficiency demonstrated by the embodiment in FIG. 105 with the bypass network. FIG. 108B shows the result of using the circuit in FIG. 106 in which only 1.88Vpp was able to be applied to a 50 ohm load.

5.9 Modifying the Energy Transfer Signal Utilizing Feedback

FIG. 69 shows an embodiment of a system 6901 which uses down-converted Signal 1308B as feedback 6906 to control various characteristics of the energy transfer module 6304 to modify the down-converted signal 1308B.

Generally, the amplitude of the down-converted signal 1308B varies as a function of the frequency and phase differences between the EM signal 1304 and the energy transfer signal 6306. In an embodiment, the down-converted signal 1308B is used as the feedback 6906 to control the frequency and phase relationship between the EM signal 1304 and the energy transfer signal 6306. This can be accomplished using the example logic in FIG 85A. The example circuit in FIG. 85A can be included in the energy transfer signal module 6902. Alternate implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Alternate implementations fall within the scope and spirit of the present invention. In this embodiment a state-machine is used as an example.

In the example of FIG. 85A, a state machine 8504 reads an analog to digital converter, A/D 8502, and controls a digital to analog converter, DAC 8506. In an embodiment, the state machine 8504 includes 2 memory locations, *Previous* and *Current,* to store and recall the results of reading A/D 8502. In an embodiment, the state machine 8504 utilizes at least one memory flag.

The DAC 8506 controls an input to a voltage controlled oscillator, VCO 8508. VCO 8508 controls a frequency input of a pulse generator 8510, which, in an embodiment, is substantially similar to the pulse generator shown in FIG. 68J. The pulse generator 8510 generates energy transfer signal 6306.

In an embodiment, the state machine 8504 operates in accordance with a state machine flowchart 8519 in FIG. 85B. The result of this operation is to modify the frequency and phase relationship between the energy transfer signal

6306 and the EM signal 1304, to substantially maintain the amplitude of the down-converted signal 1308B at an optimum level.

The amplitude of the down-converted signal 1308B can be made to vary with the amplitude of the energy transfer signal 6306. In an embodiment where the switch module 6502 is a FET as shown in FIG 66A, wherein the gate 6604 receives the energy transfer signal 6306, the amplitude of the energy transfer signal 6306 can determine the "on" resistance of the FET, which affects the amplitude of the down-converted signal 1308B. The energy transfer signal module 6902, as shown in FIG. 85C, can be an analog circuit that enables an automatic gain control function. Alternate implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Alternate implementations fall within the scope and spirit of the present invention.

5.10 Other Implementations

The implementations described above are provided for purposes of illustration. These implementations are not intended to limit the invention. Alternate implementations, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

6. Example Energy Transfer Downconverters

Example implementations are described below for illustrative purposes. The invention is not limited to these examples.

FIG. 86 is a schematic diagram of an exemplary circuit to down convert a 915 MHz signal to a 5 MHz signal using a 101.1 MHz clock.

FIG. 87 shows example simulation waveforms for the circuit of figure 86. Waveform 8602 is the input to the circuit showing the distortions caused by the switch closure. Waveform 8604 is the unfiltered output at the storage unit. Waveform 8606 is the impedance matched output of the downconverter on a different time scale.

FIG. 88 is a schematic diagram of an exemplary circuit to downconvert a 915 MHz signal to a 5 MHz signal using a 101.1 MHz clock. The circuit has additional tank circuitry to improve conversion efficiency.

FIG. 89 shows example simulation waveforms for the circuit of figure 88. Waveform 8802 is the input to the circuit showing the distortions caused by the switch closure. Waveform 8804 is the unfiltered output at the storage unit. Waveform 8806 is the output of the downconverter after the impedance match circuit.

FIG. 90 is a schematic diagram of an exemplary circuit to downconvert a 915 MHz signal to a 5 MHz signal using a 101.1 MHz clock. The circuit has switch bypass circuitry to improve conversion efficiency.

FIG. 91 shows example simulation waveforms for the circuit of figure 90. Waveform 9002 is the input to the circuit showing the distortions caused by the switch closure. Waveform 9004 is the unfiltered output at the storage unit. Waveform 9006 is the output of the downconverter after the impedance match circuit.

FIG. 92 shows a schematic of the example circuit in FIG. 86 connected to an FSK source that alternates between 913 and 917 MHz, at a baud rate of 500 Kbaud. FIG. 93 shows the original FSK waveform 9202 and the downconverted waveform9204 at the output of the load impedance match circuit.

IV. Mathematical Description of the Present Invention

As described and illustrated in the preceding sections and sub-sections, embodiments of the present invention down-convert an electromagnetic signal by repeatedly transferring energy from portions of the electromagnetic signal. This section describes the operation of the present invention mathematically using matched filter theory, sampling theory, and frequency domain techniques. The concepts and principles of these theories are used to describe the present invention's waveform processing and would be known to persons skilled in the relevant arts.

As will be apparent to persons skilled in the relevant arts based on the teachings contained herein, the description of the present invention contained herein is a unique and specific application of matched filter theory, sampling theory, and frequency domain techniques. It is not taught or suggested in the present literature. Therefore, a new transform has been developed, based on matched filter theory, sampling theory, and frequency domain techniques, to describe the present invention. This new transform is referred to as the UFT transform, and it is described in Section 8, below.

It is noted that the following describes embodiments of the invention, and it is provided for illustrative purposes. The invention is not limited to the descriptions and embodiments described below. It is also noted that characterizations such as "optimal," "sub-optimal," "maximum," "minimum," "ideal," "non-ideal," and the like, contained herein, denote relative relationships.

1. Overview of the Invention

Embodiments of the present invention down-convert an electromagnetic signal by repeatedly performing a matched filtering or

correlating operation on a received carrier signal. Embodiments of the invention operate on or near approximate half cycles (e.g., ½, 1½, 2½, etc.) of the received signal. The results of each matched filtering/correlating process are accumulated, for example using a capacitive storage device, and used to form a down-converted version of the electromagnetic signal. In accordance with embodiments of the invention, the matched filtering/correlating process can be performed at a sub-harmonic or fundamental rate.

Operating on an electromagnetic signal with a matched filtering/correlating process or processor produces enhanced (and in some cases the best possible) signal-to-noise ration (SNR) for the processed waveform. A matched filtering/correlating process also preserves the energy of the electromagnetic signal and transfers it through the processor.

Since it is not always practical to design a matched filtering/correlating processor with passive networks, the sub-sections that follow also describe how to implement the present invention using a finite time integrating operation and an RC processing operation. These embodiments of the present invention are very practical and can be implemented using existing technologies, for example but not limited to CMOS technology.

1.1 High Level Description of a Matched Filtering/Correlating Characterization/Embodiment of the Invention

In order to understand how embodiments of the present invention operate, it is useful to keep in mind the fact that such embodiments do not operate by trying to emulate an ideal impulse sampler. Rather, the present invention operates by accumulating the energy of a carrier signal and using the accumulated energy to produce the same or substantially the same result that would be obtained by an ideal impulse sampler, if such a device could be built. Stated more simply, embodiments of the present invention recursively determine a voltage or current value for approximate half cycles (e.g., ½, 1½,

2½, etc.) of a carrier signal, typically at a sub-harmonic rate, and use the determined voltage or current values to form a down-converted version of an electromagnetic signal. The quality of the down-converted electromagnetic signal is a function of how efficiently the various embodiments of the present invention are able to accumulate the energy of the approximate half cycles of the carrier signal.

Ideally, some embodiments of the present invention accumulate all of the available energy contained in each approximate half cycle of the carrier signal operated upon. This embodiment is generally referred to herein as a matched filtering/correlating process or processor. As described in detail below, a matched filtering/correlating processor is able to transfer substantially all of the energy contained in a half cycle of the carrier signal through the processor for use in determining, for example, a peak or an average voltage value of the carrier signal. This embodiment of the present invention produces enhanced (and in some cases the best possible) signal-to-noise ration (SNR), as described in the sub-sections below.

FIG. 148 illustrates an example method 14800 for down-converting an electromagnetic signal using a matched filtering/correlating operation. Method 14800 starts at step 14810.

In step 14810, a matched filtering/correlating operation is performed on a portion of a carrier signal. For example, a match filtering/correlating operation can be performed on a 900 MHz RF signal, which typically comprises a 900 MHz sinusoid having noise signals and information signals superimposed on it. Many different types of signals can be operated upon in step 14810, however, and the invention is not limited to operating on a 900 MHz RF signal. In embodiments, Method 14800 operates on approximate half cycles of the carrier signal.

In an embodiment of the invention, step 14810 comprises the step of convolving an approximate half cycle of the carrier signal with a

representation of itself in order to efficiently acquire the energy of the approximate half cycle of the carrier signal. As described elsewhere herein, other embodiments use other means for efficiently acquiring the energy of the approximate half cycle of the carrier signal. The matched filtering/correlating operation can be performed on any approximate half cycle of the carrier signal (although the invention is not limited to this), as described in detail in the sub-sections below.

In step 14820, the result of the matched filtering/correlating operation in step 14810 is accumulated, preferably in an energy storage device. In an embodiment of the present invention, a capacitive storage devise is used to store a portion of the energy of an approximate half cycle of the carrier signal.

Steps 14810 and 14820 are repeated for additional half cycles of the carrier signal. In an embodiment of the present invention, steps 14810 and 14820 are normally performed at a sub-harmonic rate of the carrier signal, for example at a third sub-harmonic rate. In another embodiment, steps 14810 and 14820 are repeated at an off-set of a sub-harmonic rate of the carrier signal.

In step 14830, a down-converted signal is output. In embodiments, the results of steps 14810 and 14820 are passed on to a reconstruction filter or an interpolation fiter.

FIG. 149 illustrates an example gated matched filtering/correlating system 14900, which can be used to implement method 14800. Ideally, in an embodiment, an impulse response of matched filtering/correlating system 14900 is identical to the modulated carrier signal, $S_i(t)$, to be processed. As can be seen in FIG. 149, system 14900 comprises a multiplying module 14902, a switching module 14904, and an integrating module 14906.

System 14900 can be thought of as a convolution processor. System 14900 multiplies the modulated carrier signal, $S_i(t)$, by a representation of itself, $S_i(t-\tau)$, using multiplication model 14902. The output of multiplication

module 14902 is then gated by switching module 14904 to integrating module 14906. As can be seen in FIG. 149, switching module 14904 is controlled by a windowing function, $u(t) - u(t-T_A)$. The length of the windowing function aperture is T_A, which is in an embodiment equal to an approximate half cycle of the carrier signal. Switching module 14904 in an embodiment ensures that approximate half cycles of the carrier signal are normally operated upon at a sub-harmonic rate. In an embodiment shown in FIG. 72, preprocessing is used to select a portion of the carrier signal to be operated upon in accordance with the present invention. In an embodiment of system 14900, the received carrier signal is operated on at an off-set of a sub-harmonic rate of the carrier signal. Integration module 14906 integrates the gated output of multiplication module 14902 and passes on its result, $S_0(t)$. This embodiment of the present invention is described in more detail in subsequent sub-sections.

As will be apparent to persons skilled in the relevant arts given the discussion herein, the present invention is not a traditional realization of a matched filter/correlator.

1.2 High Level Description of a Finite Time Integrating Characterization/Embodiment of the Invention

As described herein, in some embodiments, a matched filter/correlator embodiment according to the present invention provides maximum energy transfer and maximum SNR. A matched filter/correlator embodiment, however, might not always provide an optimum solution for all applications. For example, a matched filter/correlator embodiment might be too expensive or too complicated to implement for some applications. In such instances, other embodiments according to the present invention may provide acceptable results at a substantially lower cost, using less complex circuitry. The invention is directed to those embodiments as well.

As described herein in subsequent sub-sections, a gated matched filter/correlator processor can be approximated by a processor whose impulse response is a step function having a duration substantially equal to the time interval defined for the waveform, typically a half cycle of the electromagnetic signal, and an integrator. Such an approximation of a gated matched filter/correlator is generally referred to as a finite time integrator. A finite time integrator in accordance with an embodiment of the present invention can be implemented with, for example, a switching device controlled by a train of pulses having apertures substantially equal to the time interval defined for the waveform. The energy transfer and SNR of a finite time integrator implemented in accordance with an embodiment of the present invention is nearly that of a gated matched filter/correlator, but without having to tailor the matched filter/correlator for a particular type of electromagnetic signal. As described in sub-section 6, a finite time integrator embodiment according to the present invention can provide a SNR result that differs from the result of matched filter/correlator embodiment by only 0.91dB.

FIG. 150 illustrates an example method 15000 for down-converting an electromagnetic signal using a matched filtering/correlating operation. Method 15000 starts at step 15010.

In step 15010, a matched filtering/correlating operation is performed on a portion of a carrier signal. For example, a match filtering/correlating operation can be performed on a 900 MHz RF signal, which typically comprises a 900 MHz sinusoid having noise signals and information signals superimposed on it. Many different types of signals can be operated upon in step 15010, however, and the invention is not limited to operating on a 900 MHz RF signal. In embodiments, Method 15000 operates on approximate half cycles of the carrier signal.

In an embodiment of the invention, step 15010 comprises the step of convolving an approximate half cycle of the carrier signal with a representation of itself in order to efficiently acquire the energy of the approximate half cycle of the carrier signal. As described elsewhere herein, other embodiments use other means for efficiently acquiring the energy of the approximate half cycle of the carrier signal. The matched filtering/correlating operation can be performed on any approximate half cycle of the carrier signal (although the invention is not limited to this), as described in detail in the sub-sections below.

In step 15020, the result of the matched filtering/correlating operation in step 15010 is accumulated, preferably in an energy storage device. In an embodiment of the present invention, a capacitive storage devise is used to store a portion of the energy of an approximate half cycle of the carrier signal.

Steps 15010 and 15020 are repeated for additional half cycles of the carrier signal. In one embodiment of the present invention, steps 15010 and 15020 are performed at a sub-harmonic rate of the carrier signal. In another embodiment, steps 15010 and 15020 are repeated at an off-set of a sub-harmonic rate of the carrier signal.

In step 15030, a down-converted signal is output. In embodiments, the results of steps 15010 and 15020 are passed on to a reconstruction filter or an interpolation fiter.

FIG. 151 illustrates an example finite time integrating system 15100, which can be used to implement method 15000. Finite time integrating system 15100 has an impulse response that is approximately rectangular, as further described in sub-section 4. As can be seen in FIG. 151, system 15100 comprises a switching module 15102 and an integrating module 15104.

Switching module 15102 is controlled by a windowing function, $u(t) - u(t-T_A)$. The length of the windowing function aperture is T_A, which is equal to an approximate half cycle of the received carrier signal, $S_i(t)$. Switching module 15102 ensures that approximate half cycles of the carrier signal can be operated upon at a sub-harmonic rate. In an embodiment of system 15100, the received carrier signal is operated on at an off-set of a sub-harmonic rate of the carrier signal.

Integration module 15104 integrates the output of switching module 15102 and passes on its result, $S_0(t)$. This embodiment of the present invention is described in more detail in sub-section 4 below.

1.3 High Level Description of an RC Processing Characterization/Embodiment of the Invention

The prior sub-section describes how a gated matched filter/correlator can be approximated with a finite time integrator. This sub-section describes how the integrator portion of the finite time integrator can be approximated with a resistor/capacitor (RC) processor. This embodiment of the present invention is generally referred to herein as an RC processor, and it can be very inexpensive to implement. Additionally, the RC processor embodiment according to the present invention can be implemented using only passive circuit devices, and it can be implemented, for example, using existing CMOS

technology. This RC processor embodiment, shown in FIG. 153, utilizes a very low cost integrator or capacitor as a memory across the aperture or switching module. If the capacitor is suitably chosen for this embodiment, the performance of the RC processor approaches that of the matched filter/correlator embodiments described herein.

FIG. 152 illustrates an example method 15200 for down-converting an electromagnetic signal using a matched filtering/correlating operation. Method 15200 starts at step 15210.

In step 15210, a matched filtering/correlating operation is performed on a portion of a carrier signal. For example, a match filtering/correlating operation can be performed on a 900 MHz RF signal, which typically comprises a 900 MHz sinusoid having noise signals and information signals superimposed on it. Many different types of signals can be operated upon in step 15210, however, and the invention is not limited to operating on a 900 MHz RF signal. In embodiments, Method 15200 operates on approximate half cycles of the carrier signal.

In an embodiment of the invention, step 15210 comprises the step of convolving an approximate half cycle of the carrier signal with a representation of itself in order to efficiently acquire the energy of the approximate half cycle of the carrier signal. As described elsewhere herein, other embodiments use other means for efficiently acquiring the energy of the approximate half cycle of the carrier signal. The matched filtering/correlating operation can be performed on any approximate half cycle of the carrier signal (although the invention is not limited to this), as described in detail in the sub-sections below.

In step 15220, the result of the matched filtering/correlating operation in step 15210 is accumulated, preferably in an energy storage device. In an embodiment of the present invention, a capacitive storage devise is used to store a portion of the energy of an approximate half cycle of the carrier signal.

Steps 15210 and 15220 are repeated for additional half cycles of the carrier signal. In an embodiment of the present invention, steps 15210 and 15220 are normally performed at a sub-harmonic rate of the carrier signal, for example at a third sub-harmonic rate. In another embodiment, steps 15210 and 15220 are repeated at an off-set of a sub-harmonic rate of the carrier signal.

In step 15230, a down-converted signal is output. In embodiments, the results of steps 15210 and 15220 are passed on to a reconstruction filter or an interpolation fiter.

FIG. 153 illustrates an example RC processing system 15300, which can be used to implement method 15200. As can be seen in FIG. 153, system 15300 comprises a source resistance 15302, a switching module 15304, and a capacitance 15306. Source resistance 15302 is a lumped sum resistance.

Switching module 15304 is controlled by a windowing function, $u(t) - u(t-T_A)$. The length of the windowing function aperture is T_A, which is equal to an approximate half cycle of the received carrier signal, $S_i(t)$. Switching module 15304 ensures that approximate half cycles of the carrier signal are normally processed at a sub-harmonic rate. In an embodiment of system 15300, the received carrier signal is processed on at an off-set of a sub-harmonic rate of the carrier signal.

Capacitor 15306 integrates the output of switching module 15304 and accumulates the energy of the processed portions of the received carrier signal. RC processor 15300 also passes on its result, $S_0(t)$, to subsequent circuitry for further processing. This embodiment of the present invention is described in more detail in subsequent sub-sections.

It is noted that the implementations of the invention presented above are provided for illustrative purposes. Other implementations will be apparent to persons skilled in the art based on the herein teachings, and the invention is directed to such implementations.

2. *Representation of a Power Signal as a Sum of Energy Signals*

This sub-section describes how a power signal can be represented as a sum of energy signals. The detailed mathematical descriptions in the sub-sections below use both Fourier transform analysis and Fourier series analysis to describe embodiments of the present invention. Fourier transform analysis typically is used to describe energy signals while Fourier series analysis is used to describe power signals. In a strict mathematical sense, Fourier transforms do not exist for power signals. It is occasionally mathematically convenient, however, to analyze certain repeating or periodic power signals using Fourier transform analysis.

Both Fourier series analysis and Fourier transform analysis can be used to describe periodic waveforms with pulse like structure. For example, consider the ideal impulse sampling train in EQ. (10).

$$x(t) = \sum_{m=-\infty}^{\infty} \delta(t - mT_s) \qquad \text{EQ. (10)}$$

Suppose that this sampling train is convolved (in the time domain) with a particular waveform $s(t)$, which is of finite duration T_A. Hence $s(t)$ is an energy waveform. Then:

$$s(t) * x(t) = \sum_{m=-\infty}^{\infty} \delta(t - mT_s) * s(t) \qquad \text{EQ.(11)}$$

$$= \sum_{m=-\infty}^{\infty} s(t - mT_s) \qquad \text{EQ. (12)}$$

The above equation is a well known form of the sampler equation for arbitrary pulse shapes which may be of finite time duration rather than impulse-like. The sampler equation possesses a Fourier transform on a term-by-term basis because each separate is an energy waveform.

Applying the convolution theorem and a term-by-term Fourier transform yields:

$$\tilde{\Im}\{s(t) * x(t)\} \triangleq \tilde{\Im}\left\{\sum_{m=-\infty}^{\infty}\right\}\delta(t - mT_s)s(f)$$

$$= \sum_{m=-\infty}^{\infty} T_s^{-1}\delta\left(f - m/T_s\right)S\left(n/T_s\right) \qquad \text{EQ. (13)}$$

where $f_s = T_s^{-1}$. In this manner the Fourier transform may be derived for a train of pulses of arbitrary time domain definition provided that each pulse is of finite time duration and each pulse in the train is identical to the next. If the pulses are not deterministic then techniques viable for stochastic signal analysis may be required. It is therefore possible to represent the periodic signal, which is a power signal, by an infinite linear sum of finite duration energy signals. If the power signal is of infinite time duration, an infinite number of energy waveforms are required to create the desired representation.

FIG. 154 illustrates a pulse train 15402. Each pulse of pulse deterministic train 15402, for example pulse 15404, is an energy signal.

FIG. 155 illustrates one heuristic method based on superposition for combining pulses to form pulse deterministic train 15402.

The method of FIG. 155 shows how a power signal can be obtained from a linear piece-wise continuous sum of energy signals.

2.1 De-Composition of a Sine Wave into an Energy Signal Representation

The heuristic discussion presented in the previous section can be applied to the piecewise linear reconstruction of a sine wave function or carrier. FIG. 156 illustrates a simple way to view such a construction.

Using the previously developed equations, the waveform $y(t)$ can be represented by:

$$\sin(\omega_c t+\phi)\Big|_{t=0}^{mT} = \sum_{\ell=0}^{m=even}\sin(\omega_c t+\phi)\left[u(t)-u\left(t-\frac{T_c}{2}\right)\right]*\delta\left(t-\ell\cdot\frac{T_s}{2}\right)$$
$$+\sum_{k=1}^{m=odd}\sin(\omega_c t+\phi)\left[u\left(t-\frac{T_c}{2}\right)-u\left(t-\frac{3T_c}{2}\right)\right]*\delta\left(t-k\frac{T_s}{2}\right)$$

EQ. (14)

and $y(t)$ can be rewritten as:

$$y(t)=\sum_{\ell=0}^{m,even}\left[u\left(t-\frac{\ell T_s}{2}\right)-u\left(t-\frac{\ell T_s}{2}-\frac{T_c}{2}\right)\right]\cdot\sin\left(\omega_c\left(t-\frac{\ell T_s}{2}\right)+\phi\right)$$
$$+\sum_{k=1}^{m,odd}\left[u(t-kT_s)-u(t-kT_s)\right]\cdot\sin\left(\omega_c\left(t-kT_s-\frac{T_c}{2}\right)\right)\sin(\omega_c(t-kT_s)+\phi)$$

EQ. (15)

In general, T_s is usually integrally related to T_c. That is, the sampling interval T_s divided by T_c usually results in an integer, which further reduces the above equation. The unit step functions are employed to carve out the portion of a sine function applicable for positive pulses and negative pulse, respectively. The point is a power signal may be viewed as an infinite linear sum of energy signals.

2.2 Decomposition of Sine Waveforms

FIG. 157 illustrates how portions of a carrier signal or sine waveform are selected for processing according to embodiments of the present invention. Embodiments of the present invention operate recursively, at a sub-harmonic rate, on a carrier signal (i.e., sine wave waveform). FIG. 157 shows the case where there is synchronism in phase and frequency between the clock of the present invention and the carrier signal. This sub-section, as well as the previous sub-sections, illustrates the fact that each half-sine segment of a carrier signal can be viewed as an energy signal, and may be partitioned from the carrier or power signal by a gating process.

3. Matched Filtering/Correlating Characterization/Embodiment

3.1 Time Domain Description

Embodiments of the present invention are interpreted as a specific implementation of a matched filter and a restricted Fourier sine or cosine transform. The matched filter of such embodiments is not a traditional realization of a matched filter designed to extract information at the data bandwidth. Rather, the correlation properties of the filter of the embodiments exploit specific attributes of bandpass waveforms to efficiently down convert signals from RF. A controlled aperture specifically designed to the bandpass waveform is used. In addition, the matched filter operation of embodiments of the present invention is applied recursively to the bandpass signal at a rate sub-harmonically related to the carrier frequency. Each matched filtered result or correlation of embodiments of the present invention is retained and accumulated to provide an initial condition for subsequent recursions of the correlator. This accumulation is approximated as a zero order data hold filter.

An attribute of bandpass waveforms is that they inherently possess time domain structure, which can be compared to sampling processes. For example, FIG. 158 illustrates a double sideband large carrier AM waveform 15802, with a dashed reference 15804 and black sample dots 15806. Each half sine above or below the dashed reference 15804 can represent a finite duration pulse that possesses information impressed on the carrier by the modulation process.

Sampled systems attempt to extract information in the envelope, at the black sample dots 15806, if possible. The sample times illustrated by the black sample dots 15806 are shown here at optimum sampling times.

Difficulties arise when the bandpass waveform is at RF. Then sampling is difficult because of sample rate, sample aperture, and aperture

uncertainty. When the traditional sampler acquires, the aperture and aperture uncertainty must be minimized such that the number associated with the acquired waveform value possesses great accuracy at a particular instant in time with minimum variance. Sample rate can be reduced by sampling sub-harmonically. However, precisely controlling a minimized aperture makes the process very difficult, if not impossible, at RF.

In FIG. 158, the area under a half-sine cycle 15808 is illustrated with hatched marks. In accordance with embodiments of the present invention, instead of obtaining a sample of a single waveform voltage value, energy in the hatched area is acquired. By acquiring energy in the hatched area, the effects of aperture uncertainty can be minimized. Moreover, the waveform itself possesses the sampling information between the half sine zero crossings. This is true because the total energy of the hatched area is proportional to the peak of the modulated half sine peak. This is illustrated by EQ. (16), below. All that remains is to extract that latent information. IN embodiments, the underlying theory for optimal extractions of the energy is in fact matched filter theory.

$$E_A = \int_{-\infty}^{\infty} S_i(t)^2\,dt = 2A^2 \int_0^{T_A/2} \left(\sin(2\pi ft)\right)^2 dt = \frac{A^2 T_A}{2} \qquad \text{EQ. (16)}$$

Historically, an optimization figure of merit is signal-to-noise ration (SNR) at the system output. FIG. 159 illustrates a block diagram of an example optimum processor system 15902, which considers additive white Gaussian noise (AWGN). The general theory described herein can be extended to systems operating in the presence of colored noise as well.

Although an RF carrier with modulated information is typically a power signal, the analysis which follows considers the power signal to be a piece-wise construct of sequential energy signals where each energy waveform is a half sine pulse (single aperture) or multiple sine pulses (see sub-section 2

above). Hence, theorems related to finite time observations, Fourier transforms, etc., may be applied throughout.

Analysis begins with the assumption that a filtering process can improve SNR. No other assumptions are necessary except that the system is casual and linear. The analysis determines the optimum processor for SNR enhancement and maximum energy transfer.

The output of the system is given by the convolution integral illustrated in EQ. (17):

$$S_0(t) = \int_0^\infty h(\tau) S_i(t-\tau) d\tau \qquad \text{EQ. (17)}$$

where $h(\tau)$ is the unknown impulse response of the optimum processor.

The output noise variance is found from EQ. (18):

$$\sigma_0^2 = N_0 \int_0^\infty h^2(\tau) d\tau \qquad \text{EQ. (18)}$$

The signal to noise ratio at time t_0 is given by EQ. (19):

$$\frac{S_0^2(t_0)}{\sigma_0^2} = \frac{\left[\int_0^\infty h(\tau) S_i(t_0-\tau) d\tau\right]^2}{N_0 \int_0^\infty h^2(\tau) d\tau} \qquad \text{EQ. (19)}$$

The Schwarz inequality theorem may be used to maximize the above ratio by recognizing, in EQ. (20), that:

$$\frac{S_0^2(t_0)}{\sigma_0^2} \le \frac{\int_0^\infty h^2(\tau) \int_0^\infty S_i^2(t_0-\tau) d\tau}{N_0 \int_0^\infty h^2(\tau) d\tau} \qquad \text{EQ. (20)}$$

The maximum SNR occurs for the case of equality in EQ. 20, which yields EQ. (21):

$$\left|\frac{S_0^2(t_0)}{\sigma_0^2}\right| \max = \frac{1}{N_0} \int_0^\infty S_i^2(t_0-\tau) d\tau \qquad \text{EQ. (21)}$$

In general therefore:

$$h(\tau) = k S_i(t_0-\tau) u(\tau) \qquad \text{EQ. (22)}$$

where $u(\tau)$ is added as a statement of causality and k is an arbitrary gain

constant. Since, in general, the original waveform $S_i(t)$ can be considered as an energy signal (single half sine for the present case), it is important to add the consideration of t_0, a specific observation time. That is, an impulse response for an optimum processor may not be optimal for all time. This is due to the fact that an impulse response for realizable systems operating on energy signals will typically die out over time. Hence, the signal at t_0 is said to possess the maximum SNR.

This can be verified by maximizing EQ. (21) in general.

$$\left(\frac{d}{dt}\right)\frac{S_0^2(t)}{\sigma_0^2} = 0 \qquad \text{EQ. (23)}$$

It is of some interest to rewrite EQ. (21) by a change of variable, substituting $t = t_0 - \tau$. This yields:

$$k\int_0^\infty S_i^2(t_0 - \tau)d\tau = k\int_{-\infty}^{t_0} S_i^2(t)dt \qquad \text{EQ. (24)}$$

This is the energy of the waveform up to time t_0. After t_0, the energy falls off again due to the finite impulse response nature of the processor. EQ. (24) is of great importance because it reveals an often useful form of a matched filter known as a correlator. That is, the matched filter may be implemented by multiplying the subject waveform by itself over the time interval defined for the waveform, and then integrated. In this realization the maximum output occurs when the waveform and its optimal processor aperture are exactly overlapped for $t_0 = T_a$. It should also be evident from the matched filter equivalency stated in EQ. (24) that the maximum SNR solution also preserves the maximum energy transfer of the desired waveform through the processor. This may be proven using the Parseval and/or Rayliegh energy theorems. EQ. (24) relates directly to Parseval's theorem.

3.2 Frequency Domain Description

The previous sub-section derived an optimal processor from the time domain point-of-view according to embodiments of the invention. Alternately, Fourier transforms may be applied to obtain a frequency domain representation for h(t). This result is shown below.

$$H(f) = kS_i^*(f)e^{-j2\pi ft_0} \qquad \text{EQ. (25)}$$

Letting $j\omega = j2Bf$ and $t_0 = T_A$, we can write the following EQ. (26) for FIGS.

$$H(j\omega) = \frac{2}{T_A}e^{-j\omega T_A/2}\frac{\sin(\omega T_A/2)}{\omega T_A/2} \qquad \text{EQ. (20)}$$

160 and 161.

The frequency domain representation in FIG. 160 represents the response of an optimum processor according to embodiments. FIG. 161 illustrates responses of processors that use parameters different than T_A. For $t_0 << T_A$, the frequency domain response possesses too wide a bandwidth which captures too little of the main lobe of desired energy with respect to out of band noise power. Conversely, when $t_0 >> T_A$, the energy transfer from the signal's main lobe is very inefficient. Therefore, proper selection of T_A is key for implementation efficiency.

Another simple but useful observation is gleaned from EQ. (24) and Rayleigh's Energy Theorem for Fourier transforms:

$$E = \int_{-\infty}^{\infty}|S_i(t)|^2\,dt = \int_{-\infty}^{\infty}|H(f)|^2\,df \qquad \text{EQ. (27)}$$

EQ. (27) verifies that the transform of the optimal filter of various embodiments should substantially match the transform of the specific pulse, which is being processed, for efficient energy transfer.

4. Finite Time Integrating Characterization/Embodiment

It is not always practical to design the matched filter with passive networks. Sometimes the waveform correlation of $S_i(t)$ is also cumbersome to generate exactly. However, a single aperture realization of embodiments of the present invention is practical, even in CMOS, with certain concessions.

Consider FIGS. 162 and 163, which illustrate an optimum single aperture realization of embodiments of the present invention using sub harmonic sampling (3rd harmonic) and a processor 16310 according to such embodiments. Ideally over the aperture of interest, T_A, a half sine impulse response or waveform is used to operate on the original gated $S_i(t)$. Suppose for ease of implementation, however, that a rectangular impulse response is used, as illustrated in FIGS. 164A and 164B. The Fourier transform of this processor still overlaps the Fourier transform for the original pulse $S_i(t)$ with exactly the same nulls, as shown in FIG. 164C. Although the Fourier correlation is not perfect, it is still quite good. Furthermore, it can be implemented using a simple switch that lets the half sine through in order to charge a capacitor, which acquires the total energy of the half sine at $t_0 \cong T_A$.

Applying EQ. (26) for both the matched filter and non-matched filter embodiments yields:

$$E_{A0} = \int_0^{T_A} S_i^2(t)\, dt = \frac{A^2 T_A}{2} \qquad \textit{Optimal Matched Filter Embodiment}$$

Result; and

$$E_{AS0} = \left(\int_0^{T_A} A \cdot S(t) \right)^2 dt = \left(\frac{2T_A A}{\pi} \right)^2 \quad \textit{Finite Time Integrator Embodiment}$$

Result

It turns out in practice that realizable apertures are not perfectly rectangular and do possess a finite rise and fall time. In particular, they become triangular or nearly sinusoidal for very high frequency

implementations. Thus, the finite time integrating processor result tends toward the matched filtering/correlating processor result when the aperture becomes sine-like, if the processor possesses constant impedance across the aperture duration. Even though the matched filter/correlator response produces a lower output value at T_A, it yields a higher SNR by a factor of 0.9dB, as further illustrated below in sub-section 6.

5. RC Processing Characterization/Embodiment

Sometimes a precise matched filter is difficult to construct, particularly if the pulse shape is complex. Often, such complexities are avoided in favor of suitable approximations, which preserve the essential features. The single aperture realization of embodiments of the present invention is usually implemented conceptually as a first order approximation to a matched filter where the pulse shape being matched is a half-sine pulse. As shown in above, in embodiments, the matched filter is applied recursively to a carrier waveform. The time varying matched filter output correlation contains information modulated onto the carrier. If many such matched filter correlation samples are extracted, the original information modulated onto the carrier is recovered.

A baseband filter, matched or otherwise, may be applied to the recovered information to optimally process the signal at baseband. The present invention should not be confused with this optimal baseband processing. Rather embodiments of the present invention are applied on a time microscopic basis on the order of the time scale of a carrier cycle.

FIG. 165 illustrates a basic circuit 16502 that can be used to describe an example RC processor according to embodiments of the present invention. Circuit 16502 comprises a switch 16504. The switch 16504 is closed on a T_A

basis in order to sample $V_i(t)$. In the analysis that follows, the transfer function and impulse response are derived for circuit 16502.

The switch 16504 functions as a sampler, which possesses multiplier attributes. Heviside's operator is used to model the switch function. The operator is multiplied in the impulse response, thus rendering it essential to the matched filtering/correlating process.

In the analysis that follows, only one aperture event is considered. That is, the impulse response of the circuit is considered to be isolated aperture-to-aperture, except for the initial value inherited from the previous aperture.

For circuit 16502, shown in Figure 165:

$$V_0(t) = \frac{1}{C}\int i(t)\ dt \qquad \text{EQ. (28)}$$

$$i(t) = \frac{V_i(t)[u(t) - u(t - T_A)] - V_0(t)}{R} \qquad \text{EQ. (29)}$$

$$V_0(t) = \int \frac{V_i(t)[u(t) - (t - T_A)] - V_0(t)}{RC}\ dt \qquad \text{EQ. (30)}$$

$$V_0(t) + \int \frac{V_0(t)}{RC}\ dt = \int \frac{V_i(t)[u(t) - u(t - T_A)]}{RC}\ dt \qquad \text{EQ. (31)}$$

EQ. (31) represents the integro-differential equation for circuit 16502. The right hand side of EQ. (31) represents the correlation between the input waveform $V_i(t)$ and a rectangular window over the period T_A.

The Laplace transform of EQ. (31) is:

initial condition initial condition

$$V_0(s)\left(1 + \frac{1}{sRC}\right) + \frac{V_0(0)}{sRC} = V_i(s)\left(\frac{1 - e^{-sT_A}}{s^2RC}\right) + \frac{V_i(0)}{sRC} \qquad \text{EQ. (32)}$$

Consider that the initial condition equal to zero, then:

$$H(s)=\frac{V_0(s)}{V_i(s)}=RC^{-1}\cdot\left(\frac{1-e^{-sT_A}}{s}\right)\cdot\left(\frac{1}{s+(RC)^{-1}}\right) \qquad \text{EQ. (33)}$$

$$\therefore h(t)=\left(\frac{e^{\frac{t}{-RC}}}{RC}\right)[u(t)-u(t-T_A)] \qquad \text{EQ. (34)}$$

Suppose that $V_i(t)=A\sin\left(2\pi\frac{f_A}{2}t+\phi\right)$, as illustrated in FIG. 166,

where $f_A = T_A^{-1}$ and ϕ is an arbitrary phase shift. (FIG. 166 also shows h(t).) Note in FIG. 166 that h(t) is not ideally a sine pulse. However, the cross correlation of h(t) and $V_i(t)$ can still be quite good if RC is properly selected. This is the optimization, which is required in order to approximate a matched filter result (namely SNR optimization given h(t) and $V_i(t)$).

$$V_0(t)=V_i(t)*h(t)=A\sin(\pi f_A t)*h(t)\ ;0\le t\le T_A \qquad \text{EQ. (35)}$$

$$V_0(t)=\int_0^{\infty}\sin(\pi f_A(t-\tau))\frac{e^{\frac{-\tau}{RC}}}{RC}\,d\tau \qquad \text{EQ. (36)}$$

By a change of variables;

$$V_0(t)=\int_{-\infty}^{t}A\sin(\pi f_A\tau+\phi)\cdot\frac{e^{\frac{-(t-\tau)}{RC}}}{RC}\,[u(t-\tau)-u(t-\tau-T_A)]d\tau$$

where $f_A \triangleq 2f = T_A^{-1}$ EQ. (37)

$$\therefore V_0(t)=\frac{A}{1+(\pi f_A RC)^2}(-\pi f_A t+\phi)+\sin(\pi f_A t+\phi)-Ae^{-t/RC}\left(\sin\phi-\frac{(\pi f_A RC)^2}{1+(\pi f_A RC)^2}\cdot\sin\phi-\frac{\pi f_A RC}{1+(\pi f_A RC)^2}\cdot\cos\phi\right)$$

$0\le t\le T_A$

$$V_0(t)=\left[\frac{1}{1+(RC\pi f_A)^2}\right]\left(\sin(\pi f_A t)-\pi f_A RC\cdot\cos(\pi f_A t)+\pi f_A RC\cdot e^{-t/RC}\right)0\le t\le T_A$$

, $\phi = 0$

Notice that the differential equation solution provides for carrier phase skew, ϕ. It is not necessary to calculate the convolution beyond T_A since the gating function restricts the impulse response length.

FIG. 167 illustrates the response $V_0(t)$. The output peaks just before T_A because the example RC processor is not a perfect matched filtering/correlating processor, but rather an approximation. FIG. 168 illustrates that the maximum of the function occurs at $t \cong .75T_A$, for a $\beta = 2.6$, which can be verified by evaluating:

$$\frac{\partial}{\partial t} V_0(t) = 0 \qquad \text{EQ. (38)}$$

Solving the differential equation for $V_0(t)$ permits an optimization of $\beta = (RC)^{-1}$ for maximization of V_0.

FIG. 169 illustrates a spread of values for beta. In embodiments, the peak β occurs at approximately $\beta \cong 2.6$. FIG. 169 illustrates a family of output responses for processors according to embodiments of the present invention having different beta values. In embodiments, the definition used for optimality to obtain $\beta = 2.6$ is the highest value of signal obtained at the cutoff instant, T_A. Other criteria can be applied, particularly for multiple pulse accumulation and SNR consideration.

In embodiments, one might be tempted to increase β and cutoff earlier (i.e., arbitrarily reduce T_A). However, this does not necessarily always lead to enhanced SNR, and it reduces charge transfer in the process. It can also create impedance matching concerns, and possibly make it necessary to have a high-speed buffer. That is, reducing T_A and C is shown below to decrease SNR. Nevertheless, some gain might be achieved by reducing T_A to .75 for $\beta = 2.6$, if maximum voltage is the goal.

In embodiments, in order to maximize SNR, consider the following. The power in white noise can be found from:

$$\sigma^2 = N_0 \int_0^{\infty} h^2(\lambda) d\lambda \qquad \text{EQ. (39)}$$

$$\sigma^2 = N_0 \int_0^{\infty} \left(\frac{e^{-2\lambda / RC^2}}{RC} \right) \left(u(t) - u(\lambda - T_A) \right) \, d\lambda \qquad \text{EQ. (40)}$$

$$\sigma^2 = \frac{\beta \, N_0 \left(1 - e^{-2\beta \, N_0 T_A} \right)}{2} \; @ T_A \qquad \text{EQ. (41)}$$

$$\beta = (RC)^{-1}$$

Notice that σ^2 is a function of RC.

The signal power is calculated from:

$$(V_0(t))^2 = \left(\frac{1}{1 + \left(\beta^{-1} \pi f_A \right)^2} \right)^2 \left(\sin(\pi f_A t) - \beta^{-1} \pi f_A \cdot \cos(\pi f_A t) + \beta^{-1} \pi f_A e^{-\beta t} \right)^2$$

EQ. (42)

Hence, the SNR at T_A is given by:

Error! Objects cannot be created from editing field codes.

EQ. (43)

Maximizing the SNR requires solving:

$$\frac{\partial}{\partial \beta} \left(\frac{V_0(t)^2}{\sigma^2} \right) = 0 \qquad \text{EQ. (44)}$$

Solving the SNR_{max} numerically yields β values that are ever decreasing but with a diminishing rate of return.

As can be seen in FIG. 170, in embodiments, $\beta = 2.6$ for the maximum voltage response, which corresponds to a normalized SNR relative to an ideal matched filter of 0.431. However, in embodiments, selecting a β of $1/10$ the β, which optimizes voltage, produces a superior normalized SNR of 0.805 (about 80.5% efficiency) This is a gain in SNR performance of about 2.7dB.

In certain embodiments, it turns out that for an ideal matched filter the optimum sampling point corresponding to correlator peak is precisely T_A.

However, in embodiments, for the RC processor, the peak output of occurs at approximately 0.75 T_A for large β (i.e., $\beta = 2.6$). That is because the impulse response is not perfectly matched to the carrier signal. However, as β is reduced significantly, the RC processor response approaches the efficiency of the finite time integrating processor response in terms of SNR performance. As β is lowered, the optimal SNR point occurs closer to T_A, which simplifies design greatly. Embodiments of the present invention provides excellent energy accumulation over T_A for low β, particularly when simplicity is valued.

5.1 Charge Transfer and Correlation

The basic equation for charge transfer is:

$$\frac{dq}{dt} = C\frac{dv}{dt}, \text{ (assuming C constant over time)} \qquad \text{EQ. (45)}$$

$$q = CV$$

Similarly the energy *u* stored by a capacitor can be found from:

$$u = \int_0^q \frac{q_x}{C}\, dq_x = \frac{q^2}{2C} \qquad \text{EQ. (46)}$$

From EQs. (45) and (46):

$$u = \frac{Cv^2}{2} \qquad \text{EQ. (47)}$$

Thus, the charge stored by a capacitor is proportional to the voltage across the capacitor, and the energy stored by the capacitor is proportional to the square of the charge or the voltage. Hence, by transferring charge, voltage and energy are also transferred. If little charge is transferred, little energy is transferred, and a proportionally small voltage results unless C is lowered.

The law of conversation of charge is an extension of the law of the conservation of energy. EQ. (45) illustrates that if a finite amount of charge

must be transferred in an infinitesimally short amount of time then the voltage, and hence voltage squared, tends toward infinity. The situation becomes even more troubling when resistance is added to the equation. Furthermore,

$$V_c = \frac{1}{C}\int_0^{T_A} idt \qquad \text{EQ. (48)}$$

This implies an infinite amount of current must be supplied to create the infinite voltage if T_A is infinitesimally small. Clearly, such a situation is impractical, especially for a device without gain.

In most radio systems, the antenna produces a small amount of power available for the first conversion, even with amplification from an LNA. Hence, if a finite voltage and current restriction do apply to the front end of a radio then a conversion device, which is an impulse sampler, must by definition possess infinite gain. This would not be practical for a switch. What is usually approximated in practice is a fast sample time, charging a small capacitor, then holding the value acquired by a hold amplifier, which preserves the voltage from sample to sample.

The analysis that follows shows that given a finite amount of time for energy transfer through a conversion device, the impulse response of the ideal processor, which transfers energy to a capacitor when the input voltage source is a sinusoidal carrier and possesses a finite source impedance, is represented by embodiments of the present invention. If a significant amount of energy can be transferred in the sampling process then the tolerance on the charging capacitor can be reduced, and the requirement for a hold amplifier is significantly reduced or even eliminated.

In embodiments, the maximum amount of energy available over a half sine pulse can be found from:

$$u = \int_0^{T_A} S_i^2(t)dt = \frac{A^2 T_A}{2} \qquad \text{EQ. (49)}$$

This points to a correlation processor or matched filter processor. If energy is of interest then a useful processor, which transfers all of the half sine energy, is revealed in EQ. (48), where T_A is an aperture equivalent to the half sine pulse. In embodiments, EQ. (49) provides the clue to an optimal processor.

Consider the following equation sequence.

$$\int_0^{\infty} h(\tau)S_i(t-\tau)d\tau \Rightarrow \int_0^{T_A} kS_i^2(T_A-\tau)d\tau \Rightarrow \int_{-0}^{T_A} S_i^2(t)dt$$

EQ. (50)

where $h(\vartheta) = S_i(T_A - \vartheta)$ and $t = T_A - \vartheta$.

This is the matched filter equation with the far most right hand side revealing a correlator implementation, which is obtained by a change of variables as indicated. The matched filter proof for $h(\tau) = S_i(T_A - \tau)$ is provided in sub-section 8.4 below. Note that the correlator form of the matched filter is exactly a statement of the desired signal energy. Therefore a matched filter/correlator accomplishes acquisition of all the energy available across a finite duration aperture. Such a matched filter/correlator can be implemented as shown in FIG. 171.

In embodiments, when optimally configured, the example matched filter/correlator of FIG. 171 operates in synchronism with the half sine pulse $S_i(t)$ over the aperture T_A. Phase skewing and phase roll will occur for clock frequencies, which are imprecise. Such imprecision can be compensated for by a carrier recovery loop, such as a Costas Loop. A Costas Loop can develop the control for the acquisition clock, which also serves as a sub-harmonic carrier. However, phase skew and non-conherency does not invalidate the optimal form of the processor provided that the frequency or phase errors are small, relative to T^{-1}_A. Non-coherent and differentially coherent processors may extract energy from both I and Q with a complex correlation operation followed by a rectifier or phase calculator. It has been shown that phase skew does not alter the optimum SNR processor formulation. The energy which is

not transferred to I is transferred to Q and vice versa when phase skew exists. This is an example processor for a finite duration sample window with finite gain sampling function, where energy or charge is the desired output.

A matched filter/correlator embodiment according to the present invention might be too expensive and complicated to build for some applications. In such cases, however, other processes and processors according to embodiments of the invention can be used. The approximation to the matched filter/correlator embodiment shown in FIG. 172 is just one embodiment that can be used in such instances. The finite time integrator embodiment of FIG. 172 requires only a switch and an integrator. Sub-section 6 below shows that this embodiment of the present invention has only a 0.91dB difference in SNR compared to the matched filter/correlator embodiment.

Another very low cost and easy to build embodiment of the present invention is the RC processor. This embodiment, shown in FIG. 173, utilizes a very low cost integrator or capacitor as a memory across the aperture. If C is suitable chosen for this embodiment, its performance approaches that of the matched filter/correlator embodiment, shown in FIG. 171. Notice the inclusion of the source impedance, R, along with the switch and capacitor. This simple embodiment nevertheless can approximate the optimum energy transfer of the matched filter/correlator embodiment if properly designed.

When maximum charge is transferred, the voltage across the capacitor 17304 in FIG. 173 is maximized over the aperture period for a specific RC combination.

Using EQs. (45) and (48) yields:

$$q = C \cdot \frac{1}{C} \int_0^{T_A} i_c dt \qquad \text{EQ. (51)}$$

If it is accepted that an infinite amplitude impulse with zero time duration is not available or practical, due to physical parameters of capacitors like ESR,

inductance and breakdown voltages, as well as currents, then EQ. (51) reveals the following important considerations for embodiments of the invention:

- The transferred charge, q, is influenced by the amount of time available for transferring the charge;
- The transferred charge, q, is proportional to the current available for charging the energy storage device; and
- Maximization of charge, q, is a function of i_c, C, and T_A.

Therefore, it can be shown that for embodiments:

$$q_{max} = Cv_{max} = C\left[\frac{1}{C}\int_0^{T_A} i_c dt\right]_{max} \qquad \text{(EQ. 52)}$$

The impulse response for the RC processing network was found in sub-section 5.2 below to be;

$$h(t) = \frac{e^{\frac{-\tau}{RC}}}{RC}\left[u(\tau) - u(\tau - T_A)\right] \qquad \text{EQ. (53)}$$

Suppose that T_A is constrained to be less than or equal to $^1/_2$ cycle of the carrier period. Then, for a synchronous forcing function, the voltage across a capacitor is given by EQ. (54).

$$V_0(t) = \int_{-\infty}^{t} \sin(\pi f_A \tau) \cdot \frac{e^{\frac{-(t-\tau)}{RC}}}{RC}\, d\tau \qquad \text{EQ. (54)}$$

Maximizing the charge, q, requires maximizing EQ. (37) with respect to t and β.

$$\frac{\partial^2 V_0(t)}{\partial t\, \partial \beta} = 0 \qquad \text{EQ. (55)}$$

It is easier, however, to set R = 1, T_A = 1, A =1, $f_A = T_A^{-1}$ and then calculate $q = cV_0$ from the previous equations by recognizing that $q = \frac{\beta^{-1}}{R}\ V_0 = cV_0$, which produces a normalized response.

FIG. 174 illustrates that increasing C is preferred in embodiments of the invention. It can be seen in FIG. 174 that as C increases (i.e., as $\exists$ decreases) the charge transfer also increases. This is what is to be expected based on the optimum SNR solution. Hence, for embodiments of the present invention, an optimal SNR design results in optimal charge transfer. As C is increased, bandwidth considerations should be taken into account.

In embodiments, EQ. (49) establishes T_A as the entire half sine for an optimal processor. However, in embodiments, optimizing jointly for t and β reveals that the RC processor response creates an output across the energy storage capacitor that peaks for $t_{max} \cong .75T_A$, and $\beta_{max} \cong 2.6$, when the forcing function to the network is a half sine pulse.

In embodiments, if the capacitor of the RC processor embodiment is replaced by an ideal integrator then $t_{max} \rightarrow T_A$.

$$\beta T_A \simeq 1.95 \qquad \text{EQ. (56)}$$

where $\exists = (RC)^{-1}$

For example, for a 2.45 GHz signal and a source impedance of 50Ω, EQ. (56) above suggests the use of a capacitor of ≅ 2pf. This is the value of capacitor for the aperture selected, which permits the optimum voltage peak for a single pulse accumulation. For practical realization of the present invention, the capacitance calculated by EQ. (56) is a minimum capacitance. SNR is not considered optimized at $\beta T_A \simeq 1.95$. As shown earlier, a smaller β yields better SNR and better charge transfer. In embodiments, as discussed below, it turns out that charge can also be optimized if multiple apertures are used for collecting the charge.

In embodiments, for the ideal matched filter/correlator approximation, βT_A is constant and equivalent for both consideration of optimum SNR and optimum charge transfer, and charge is accumulated over many apertures for

most practical designs. Consider the following example, $\beta = .25$, and $T_A = 1$. Thus $\beta T_A = .25$. At 2.45 GHz, with R =50Ω, C can be calculated from:

$$C \geq \frac{T_A}{R(.25)} \geq 16.3pf \qquad \text{EQ. (57)}$$

The charge accumulates over several apertures, and SNR is simultaneously optimized melding the best of two features of the present invention. Checking CV for $\beta T_A \simeq 1.95$ vs. $\beta T_A = .25$ confirms that charge is optimized for the latter.

5.2 Load Resistor Consideration

The general forms of the differential equation and transfer function, described above, for embodiments of the present invention are the same as for a case involving a load resistor, R_L, applied across capacitor, C. FIG. 175A illustrates an example RC processor embodiment 17502 of the present invention having a load resistance 17504 across a capacitance 17506.

Consider RC processing embodiment 17502 (without initial conditions).

EQ. (33) becomes:

$$H(s) = \frac{1 - e^{-sT_A}}{s}\left(\frac{1}{sCR + k}\right) \qquad \text{EQ. (58)}$$

$$k = \left(R/R_L + 1\right) \qquad \text{EQ. (59)}$$

$$h(t) = \left(\frac{e^{-\frac{t \cdot k}{RC}}}{RC}\right)\left[u(t) - (t - T_A)\right] \qquad \text{EQ. (60)}$$

It should be clear that R_L 17504,and therefore k, accelerate the exponential decay cycle.

$$V_0(t) = \int_{-\infty}^{t} \sin(\pi f_a \tau) \cdot \frac{e^{-\frac{k(t-\tau)}{RC}}}{RC} \, d\tau \qquad \text{EQ. (61)}$$

$$V_0(t) = \left(\frac{1}{k^2 + (\pi f_A)^2} \right) \left[k \cdot \sin(\pi f_A t) - \pi f_A RC \cdot \cos(\pi f_A t) + RCe^{-\frac{kt}{RC}} \right] \quad 0 \le t \le T_A$$

EQ.(62)

This result is valid only over the acquisition aperture. After the switch is opened, the final voltage that occurred at the sampling instance $t \cong T_A$ becomes an initial condition for a discharge cycle across R_L 17504. The discharge cycle possesses the following response:

$$V_D = \frac{V_A \cdot e^{-\frac{t}{R_L C}}}{R_L C} u(t - T_A) \quad \textit{(single event discharge)}$$

EQ. (63)

V_A is defined as $V_0(t \cong T_A)$. Of course, if the capacitor 17506 does not completely discharge, there is an initial condition present for the next acquisition cycle.

FIG. 175B illustrates an example implementation of the invention, modeled as a switch S, a capacitor C_S, and a load resistance R. FIG. 175D illustrates example energy transfer pulses, having apertures A, for controlling the switch S. FIG. 175C illustrates an example charge/discharge timing diagram for the capacitor C_S, where the capacitor C_S charges during the apertures A, and discharge between the apertures A.

Equations 63.1 through 63.15 derive a relationship between the capacitance of the capacitor C_S ($C_S(R)$), the resistance of the resistor R, the duration of the aperture A (aperture width), and the frequency of the energy transfer pulses (freq LO). Equation 63.11 illustrates that optimum energy transfer occurs when x = 0.841. Based on the disclosure herein, one skilled in the relevant art(s) will realize that values other that 0.841 can be utilized.

$$\phi = \frac{1}{C}\int i(t)\partial t + Ri(t) \qquad \text{EQ. (63.1)}$$

$$\frac{\partial}{\partial t}\phi = \frac{\partial}{\partial t}\left[\frac{1}{C}\int i(t)\partial t + Ri(t)\right] \qquad \text{EQ. (63.2)}$$

$$\phi = \frac{i(t)}{C_s} + \frac{R\partial i(t)}{\partial t} \qquad \text{EQ. (63.3)}$$

$$\phi = \frac{1}{C_s} + R \cdot s \qquad \text{EQ. (63.4)}$$

$$s = \frac{-1}{C_s \cdot R}, \text{ by definition: } \; i_{init}(t) = \frac{V_{C_s} init}{R} \qquad \text{EQ. (63.5)}$$

$$i(t) = \left(\frac{V_{C_s} init}{R}\right) \cdot e^{\left(\frac{-t}{C_s \cdot R}\right)} \qquad \text{EQ. (63.6)}$$

$$V_{out}(t) = R \cdot i(t) = V_{C_s} init \cdot e\left(\frac{-t}{C_s \cdot R}\right) \qquad \text{EQ. (63.7)}$$

Maximum power transfer occurs when:

$$Power\_Final = \frac{1}{\sqrt{2}} \cdot Peak\_Power \qquad \text{EQ. (63.8)}$$

$$Power\_Peak = \frac{\left(V_{C_s} peak\right)^2}{R} \qquad \text{EQ. (63.9)}$$

$$Power\_Final = \frac{\left(x \cdot V_{C_s} peak\right)^2}{R} \qquad \text{EQ. (63.10)}$$

$$\frac{\left(x \cdot V_{C_s} peak\right)^2}{R} = \frac{\left(V_{C_s} peak\right)^2}{R} \cdot \frac{1}{\sqrt{2}} \text{ yields x = 0.841} \qquad \text{EQ. (63.11)}$$

Let $V_{Cs}init = 1$, then $V_{out}(t) = 0.841$ when

$$t = \frac{1}{freqLO} - Aperture\_Width\,. \qquad \text{EQ. (63.12)}$$

$$0.841 = 1 \cdot e^{\left(\frac{\frac{1}{freqLO} - Aperture\_Width}{C_s \cdot R}\right)} \qquad \text{EQ. (63.13)}$$

$$\ln(0.841) = \left(\frac{\frac{1}{freqLO} - Aperture\_Width}{C_s \cdot R}\right) \qquad \text{EQ. (63.14)}$$

$$C_s(R) = \left(\frac{\frac{1}{freqLO} - Aperture\_Width}{-\ln(0.841) \cdot R}\right) \qquad \text{EQ. (63.15)}$$

6. Signal-To-Noise Ratio Comparison of the Various Embodiments

The prior sub-sections described the basic SNR definition and the SNR of an optimal matched filter/correlator processor according to embodiments of the present invention. This sub-section section describes the SNR of additional processor embodiments of the present invention and compares their

SNR with the SNR of a optimal matched filter/correlator embodiment. The description in this sub-section is based on calculations relating to single apertures and not accumulations of multiple aperture averages. Since SNR is a relative metric, this method is useful for comparing different embodiments of the present invention.

EQ. (65), which can be obtained from EQ. (64), represents the output SNR for a single aperture embodiment assuming a constant envelope sine wave input. The results could modify according to the auto-correlation function of the input process, however, over a single carrier half cycle, this relationship is exact.

$$SNR_{opt} \triangleq \frac{1}{N_0} \int_0^{\infty} S_i^2(t_0 - \tau)\ d\tau \qquad \text{EQ. (64)}$$

$$SNR_{opt} \triangleq \frac{T_A A^2}{2N_0} \quad \text{(single aperture case)} \qquad \text{EQ. (65)}$$

The description that follows illustrates the SNR for three processor embodiments of the present invention for a given input waveform. These embodiments are:

- An Example Optimal Matched Filter/Correlator Processor Embodiment;
- An Example Finite Time Integrator processor Embodiment; and
- An Example RC Processor Embodiment

The relative value of the SNR of these three embodiments is accurate for purposes of comparing the embodiments. The absolute SNR may be adjusted according to the statistic and modulation of the input process and its complex envelope.

Consider an example finite time integrator processor, such as the one illustrated in FIG. 164B. The impulse response of the finite time integrator processor is given by EQ. (66):

$$h(t) = k, \ 0 \le t \le T_A \qquad \text{EQ. (66)}$$

where *k* is defined as an arbitrary constant.

The output of the finite time integrator processor, $y(t)$, is found from the input, $x(t)$, using:

$$y(t) = \int_{t-T_A}^{t} x(u)\ du \qquad \text{EQ. (67)}$$

A change of variables yields EQ. (68):

$$y(t-\tau) = \int_{t-\tau-T_A}^{t-\tau} x(v)\ dv \qquad \text{EQ. (68)}$$

The output auto correlation then becomes that shown in EQ. (69):

$$R_v(\tau) = \int_{t-T_A}^{t} du \int_{t-\tau-T_A}^{t-\tau} R_x(u-v)\ dv \qquad \text{EQ. (69)}$$

which leads to:

$$R_x(u-v) = \frac{1}{2\pi}\int_{-\infty}^{\infty} S_x(\omega)\ e^{j\omega(u-v)} d\omega \qquad \text{EQ. (70)}$$

This Fourier transform may be substituted into the expression for $R_y(\tau)$, in EQ. (71), which becomes:

$$R_y(\tau) = \frac{1}{2\pi}\int_{-\infty}^{\infty} S_x(\omega) d\omega \int_{t-T_A}^{t} e^{S\omega u} du \int_{t-\tau-T_A}^{t-\tau} e^{-j\omega v} dv \qquad \text{EQ. (71)}$$

$$R_y(\tau) = \frac{1}{2\pi}\int_{-\infty}^{\infty} S_x(\omega)\left[\frac{e^{j\omega t}\left(1-e^{-j\omega T_A}\right)}{j\omega}\right]\left[\frac{e^{-j\omega(t-\tau)}\left(1-e^{-j\omega T_A}\right)}{j\omega}\right] d\omega$$

EQ. (72)

$$\therefore S_y(\omega) = S_x(\omega)\frac{\sin^2 \omega T_A/2}{(\omega/2)^2} \qquad \text{EQ. (73)}$$

$S_y(\omega)$ is the power spectral density at the output of the example finite time integrator, whose integration aperture is T_A and whose input power spectrum is defined by $S_x(\omega)$. For the case of wide band noise:

$$S_{yn}(\omega) = \frac{N_0}{2\pi}\frac{\sin^2 \omega T_A/2}{(\omega/2)^2} \qquad \text{EQ. (74)}$$

The total noise power across the band can be found from EQ. (75):

$$\int_{-\infty}^{\infty} S_{yn}(\omega)d\omega = \frac{N_0}{2\pi}\int_{-\infty}^{\infty} \frac{\sin^2(\omega T_A/2)}{(\omega/2)^2}\, d\omega = T_A N_0 \qquad \text{EQ. (75)}$$

This result can be verified by EQ. (76):

$$\overline{Y^2} = N_0 \int_0^{\infty} h^2(\tau)\, d\tau \qquad \text{EQ. (76)}$$

The signal power over a single aperture is obtained by EQ. (77):

$$y(t)^2 = \left(2A\int_0^{T_A/2} \sin(\omega t)dt\right)^2 \qquad \text{EQ. (77)}$$

Choosing A = 1, the finite time integrator output SNR becomes:

$$SNR_{\text{int}} = \frac{4T_A}{\pi^2 N_0} \qquad \text{EQ. (78)}$$

An example RC filter can also be used to model an embodiment of the present invention. The mean squared output of a linear system may be found from EQ. (79):

$$\overline{Y^2} = \int_0^{\infty} d\tau_1 \int_0^{\infty} R_x(\tau_A - \tau_1)h(\tau_1)h(\tau_2)\, d\tau_2 \qquad \text{EQ. (79)}$$

For the case of input AWGN:

$$R_{xn}(\tau) = N_0\delta(\tau) \qquad \text{EQ. (80)}$$

$$\overline{Y^2} = N_0 \int_0^{\infty} d\tau_1 \int_0^{\infty} \delta(\tau_2 - \tau_1)h(\tau_1)h(\tau_2)\, d\tau_2 \qquad \text{EQ. (81)}$$

$$\overline{Y_n^2} = N_0 \int_0^{\infty} h^2(\tau)\, d\tau \qquad \text{EQ. (82)}$$

This leads to the result in EQ. (83):

$$H(s) = \frac{1/RC}{s + 1/RC} * \left(\frac{1 - e^{-sT_A}}{s}\right) \qquad \text{EQ. (83)}$$

R is the resistor associated with processor source, and *C* is the energy storage capacitor.

Therefore;

$$h(t) = \frac{1}{RC} e^{-t/RC}\ (u(t) - u(t - T_A)) \qquad \text{EQ. (84)}$$

And finally:

$$\overline{Y_n^2} = \frac{N_0}{2RC}\left(1 - e^{-\left(2N_0 T_A / RC\right)}\right) \qquad \text{EQ. (85)}$$

The detailed derivation for the signal voltage at the output to the RC filter is provided in sub-section 5 above. The use of the β parameter is also described in sub-section 5. Hence, the SNR_{RC} is given by:

$$SNR_{RC} = \frac{2\left(V_0(t_s)\right)^2}{\beta N_0} \quad T_A = 1, \quad A = 1 \qquad \text{EQ. (86)}$$

Illustrative SNR performance values of the three example processor embodiments of the present invention are summarized in the table below:

Example Matched Filter	Performance Relative to the Performance of an Optimal Matched Filter Embodiment
$SNR_{MF} = \frac{T_A}{2N_0}$	0dB
Example Integrator Approximate	
$SNR_{INT} = \frac{4T_A}{\pi^2 N_0}$	-.91dB
Example RC Approximate (3 example cases for reference)	
$SNR_{RC} = \frac{V_0(t)^2 \cdot 2}{\beta N_0} \cong \frac{.2142}{N_0}$	-3.7dB, at $T_A = 1$, $\beta = 2.6$
$SNR_{RC} \cong \frac{.377}{N_0}$	-1.2dB, at $T_A = .75$, $\beta = 2.6$
$SNR_{RC} \cong \frac{.405}{N_0}$	-.91dB at $T_A = 1$, $\beta \leq .25$

Notice that as the capacitor becomes larger, the RC processor behaves

like a finite time integrator and approximates its performance. As described above in sub-section 5, with a β of 0.25, a carrier signal of 2450 MHz, and R = 50Ω, the value for C becomes $C \geq 16.3pf$.

FIG. 176 illustrates the output voltage waveforms for all three processor embodiments. (Note that two curves are shown for the RC correlator processor, $\exists = 2.6$ and $\exists = 0.25$). FIG. 177A illustrates the relative SNR's over the aperture.

6.2 Carrier Offset and Phase Skew Characteristics of Embodiments of the Present Invention

FIG. 177B illustrates some basic matched filter waveforms that are common to some communications applications. The first waveform 17750 is a baseband rect function. Since this waveform is symmetric it is easy to visualize the time reversed waveform corresponding to the ideal matched filter impulse response, $h(t)$, which is also a rect function:

$$h(t) * S_i(t-\tau)\int_{t_1}^{t_2} S_i(t-\tau)h(t)dt \qquad \text{EQ. (86.1)}$$

The second waveform 17760 illustrates the same rect function envelope at passband (RF) and it's matched filter impulse response. Notice the sine function phase reversal corresponding to the required time axis flip. FIG. 177C shows a waveform 17770. Waveform 17770 is a single half sine pulse whose time reversed representation is identical. This last impulse response would be optimal but as pointed out earlier may be difficult to implement exactly. Fortunately, an exact replica is not required.

FIG. 177D illustrates some exemplary approaches for a complex matched filter/correlator processor applied to a variety of waveforms. As shown in FIG. 177D, approaches 17780 and 17785 are classical ways to producing a complex matched filter/correlator processor. FIG. 177E shows approach 17790. Approach 17790 shows one embodiment of a complex matched filter/correlator processor implemented with the UFT as the processor. The only difference in the UFT approach 17790 is the duration of the pulse envelope. The fact that the gating pulse is small compared to other applications for a correlator is of little consequence to the complex baseband processor. When there is no phase skew then all of the correlated energy is transferred to the I output. When there is a phase skew then a portion of the aliased down converted energy is transferred to the I output and the remainder to the Q. All of the correlated energy is still available, in its optimally filtered form, for final processing in the BB processor.

The fact that a non-coherent processor is used or a differentially coherent BB processor used in lieu of a coherent Costas Loop in no way diminishes the contribution of the UFT correlator effect obtained by selecting the optimal aperture T_A based on matched filter theory.

Consider FIG. 177E which illustrates an aperture with a phase shifted sine function. In addition, a derivation is provided which indicates that the aperture with phase skew, as referenced to the half sine function, can be represented by the fundamental correlator kernel multiplied by a constant. This provides insight into the interesting SNR properties of the UFT which are based on matched filter principles over the aperture regardless of phase skew ϕ.

Moreover, Section IV, part 5.1 above illustrates that a complex UFT downconverter which utilizes a bandpass filter actually resembles the optimal matched filter/correlator kernel in complex form with the in phase result scaled by $\cos\phi$ and the quadrature phase component scaled by $\sin\phi$. This process preserves all the energy of the downconverter signal envelope (minus system loses) with a part of the energy in I and the remainder in Q.

7. Multiple Aperture Embodiments of the Present Invention

The above sub-sections describe single aperture embodiments of the present invention. That is, the above sub-sections describe the acquisition of single half sine waves according to embodiments of the invention. Other embodiments of the present invention are also possible, however, and the present invention can be extended to other waveform partitions that capture multiple half sine waves. For example, capturing two half sine waves provides twice the energy compared to capturing only a single half sine. Capturing n half sines provides n times the energy, et cetera, until sub harmonic sampling is no longer applicable. The invention is directed to other embodiments as well. Of course, the matched filter waveform requires a different correlating aperture for each new n. This aspect of the present invention is illustrated in FIGS. 178A and 178B.

In the example of FIG. 178B, the sample aperture window is twice as long as the examples in the previous sub-sections. The matched filter impulse response in FIG. 178B is bipolar to accommodate a full sine cycle. The embodiment of this example can be implemented, for example, with a rectangular bipolar function (Haar's Wavelet) gating device.

Fourier transforming the components for the example processor yields the results shown in FIG. 179 and EQ. (87).

$$S(f) \cong \sum_{n=-\infty}^{\infty} \frac{Af_s T_A}{2}\left[\frac{\sin(\pi(nf_s - Nf_s)T_A)}{(\pi(nf_s - Nf_s)T_A)} + \frac{\sin(\pi nf_s + Nf_s)T_A}{(\pi(nf_s + Nf_s)T_A)}\right]\delta(f - nf_s)$$

EQ. (87)

The transform of the periodic, sampled, signal is first given a Fourier series representation (since the Fourier transform of a power signal does not exist in strict mathematical sense) and each term in the series is transformed sequentially to produce the result illustrated. Notice that outside of the desired main lobe aperture response that certain harmonics are nulled by the (sinx)/x response. Even those harmonics, which are not completely nulled, are reduced by the side lobe attenuation. Some sub-harmonics and super-harmonics are eliminated or attenuated by the frequency domain nulls and side lobes of the bipolar matched filter/correlator processor, which is a remarkable result.

Theoretically, arbitrary impulse responses may be constructed in the manner above, particularly if weighting is applied across the aperture or if multiple apertures are utilized to create a specific Fourier response. FIR filters and convolvers may be constructed by extending the aperture and utilizing the appropriate weighting factors. Likewise, disjoint or staggered apertures may be constructed to provide a particular desired impulse response. These apertures can be rearranged and tuned 'on the fly'.

FIG. 180 (I/Q Bipolar Aperture for 2.4 – 2.5 GHz 3rd Harmonic Down Converter Application) and FIG. 181 (Down Converted I/Q Waveforms - Slight Carrier Offset) illustrate the results from an actual circuit design and simulation targeting the 2.4 – 2.5 GHz ISM band and implementing a bipolar weighted aperture. FIG. 180 illustrates actual gating pulses, which form the apertures for I-, I+, Q-, and Q+. FIG. 181 illustrates the baseband I and Q outputs corresponding to the down converter. In embodiments, the sequence I-, I+, Q- and Q+ apertures are repeated every three carrier cycles, nominally. Hence, out of six sine carrier segments, four are captured. Conversion losses well below 10dB are possible with this embodiment of the present invention.

8. Mathematical Transform Describing Embodiments of the Present Invention

8.1 Overview

The operation of the present invention represents a new signal-processing paradigm. Embodiments of the invention can be shown to be related to particular Fourier sine and cosine transforms. Hence, the new term UFT transform is utilized to refer to the process. As already stated, in embodiments of the present invention can be viewed as a matched filter or correlator operation, which in embodiments is normally applied recursively to the carrier signal at a sub-harmonic rate. A system equation may be written to describe this operation, assuming a rectangular sample aperture and integrators as operators, as shown in FIG. 182 and EQ. (88). The process integrates across an acquisition aperture then stores that value, or a significant portion thereof, to be accumulated with the next aperture. Hence, energy from the input is acquired during T_A and held for T_s - T_A until the next acquisition.

$$D_n \triangleq \sum_{n=1}^{k} \int_{nT_S}^{nT_S+T_A} \left(u\left(t - nT_s\right) - u\left(t - \left(nT_S + T_A\right)\right)\right) \cdot A_n \sin\left(\omega t + \phi_{(n-\ell)}\right) dt$$

$$-\alpha \sum_{n=1}^{k} \int_{(n+\ell)T_S}^{(n+\ell)T_S+T_A} \left(u\left(t - (n-\ell)T_S\right) - u\left(t - \left(n - (1-\ell)\right)T_S + T_A\right)\right) \cdot A_{(n-\ell)} S_i\left(\omega t + \phi_{(n-\ell)}\right) dt$$

EQ. (88)

where:

T_A is the aperture duration;

T_S is the sub-harmonic sample period;

k is the total number of collected apertures;

ℓ is the sample memory depth;

$\forall$ is the UFT leakage coefficient;

A_n is the amplitude weighting on the nth aperture due to modulation, noise, etc.; and

ν_n is the phase domain shift of nth aperture due to modulation, noise, carrier offset, etc.

D_n represents the UFT transform applicable to embodiments of the invention. The first term defines integration over a rectangular segment of the carrier signal of T_A time duration. k pulses are summed to form a memory of the recursively applied kernel. The second term in the equation provides for the fact that practical implementations possess finite memory. Hence, embodiments of the present invention are permitted to leak after a fashion by selecting α and ℓ. This phenomena is reflected in the time variant differential equation, EQ. (31), derived in sub-section 5. In embodiments, for a perfect zero order data hold function, $\alpha = 0$.

8.2 The Kernel for Embodiments of the Invention

The UFT kernel applicable to embodiments of the invention is given by EQ. (89):

$$D_1 = \int_0^{T_A} (u(t) - u(t - T_A)) \cdot A \sin(\omega t + \phi) dt \qquad \text{EQ. (89)}$$

EQ. 89 accounts for the integration over a single aperture of the carrier signal with arbitrary phase, ϕ, and amplitude, A. Although A and ϕ are shown as constants in this equation, they actually may vary over many (often hundreds or thousands) of carrier cycles. Actually, $\phi(t)$ and $A(t)$ may contain the modulated information of interest at baseband. Nevertheless, over the duration of a pulse, they may be considered as constant.

8.3 Waveform Information Extraction

Ever since Nyquist developed general theories concerning waveform sampling and information extraction, researchers and developers have pursued optimum sampling techniques and technologies. In recent years, many radio architectures have embraced these technologies as a means to an end for ever more 'digital like' radios. Sub sampling, IF sampling, syncopated sampling, etc., are all techniques employed for operating on the carrier to extract the information of interest. All of these techniques share a common theory and common technology theme, i.e., Nyquist's theory and ideal impulse samplers. Clearly, Nyquist's theory is truly ideal, from a theoretical perspective, while ideal impulse samplers are pursued but never achieved.

Consider the method of developing an impulse sample using functions with shrinking apertures, as illustrated in FIG. 183. The method illustrated in FIG. 183 utilizes a pulse shape, for example a normalized Gaussian, a modified sinc, or some other suitable type, and permits the pulse width to shrink as the peak amplitude grows. As the pulse width shrinks, the area of the pulse becomes unity. These pulse generation methods are formulated

using distribution mathematics techniques. Typically, such formulations require the assumption that causality is violated as is illustrated by the precursors in FIG. 183. Hence, such pulses are not practical because they are non-causal. In addition, since impulse samplers are implemented to store the sample value at an instantaneous waveform point, they typically utilize a sample and hold approach, which typically implies the charging of a capacitor. As would be known to persons skilled in the relevant arts given the discussion herein, parasitics can present significant charging concerns for such pulses because of the relationships represented by EQ. (90) and EQ. (91).

$$\frac{dq}{dt} = C\frac{dv}{dt} \text{ (Charge Differential)} \qquad \text{EQ. (90)}$$

$$u = \int_0^q \frac{q_x}{c} - dq_x = \frac{q^2}{2c} = \frac{Cv^2}{2} \text{ (Energy)} \qquad \text{EQ. (91)}$$

As would be apparent to persons skilled in the relevant arts given the discussion herein, an arbitrary capacitance, *c*, cannot be charged in an infinitesimally short time period without an infinite amount of energy. Even approximations to an ideal impulse therefore can place unrealistic demands on analog sample acquisition interface circuits in terms of parasitic capacitance vs. pulse width, amplitude, power source, etc. Therefore, a trade-off is typically made concerning some portion of the mix.

The job of a sample and hold circuit is to approximate an ideal impulse sampler followed by a memory. There are limitations in practice, however. A hold capacitor of significant value must be selected in order to store the sample without droop between samples. This requires a healthy charging current and a buffer, which isolates the capacitor in between samples, not to mention a capacitor, which is not 'leaky,' and a buffer without input leakage currents. In general, ideal impulse samplers are very difficult to approximate when they must operate on RF waveforms, particularly if IC implementations and low power consumption are required.

The ideal sample extraction process is mathematically represented in

EQ. (92) by the sifting function.

$$\int_{-\infty}^{\infty} x(t)\delta\left(t - T_A/2\right)\,dt = x\left(\frac{T_A}{2}\right) \qquad \text{EQ. (92)}$$

where: $\frac{T_A}{2}$ $\triangleq$ Sample Time; $x(t)$ $\triangleq$ Sampled Function; and $\delta(t)$ $\triangleq$ Impulse Sample Function.

Suppose now that:

$$x(t) = A\sin(t+\phi) \qquad \text{EQ. (93)}$$

then:

$$\int_{-\infty}^{\infty} A\sin(t+\phi)\delta\left(t - T_A/2\right)dt = A\sin\left(T_A/2 + \phi\right)$$

$$= A\cos(\phi)\int_{-\infty}^{\infty}\sin(t)\delta\left(t - T_A/2\right)dt + A\sin(\phi)\int_{-\infty}^{\infty}\cos(t)\delta\left(t - T_A/2\right)\,dt$$

EQ. (94)

$$= A\cos(\phi)\sin\left(T_A/2\right) = A\cos(\phi); T_A = \pi \qquad \text{EQ. (95)}$$

This represents the sample value acquired by an impulse sampler operating on a carrier signal with arbitrary phase shift ϕ. EQ. (95) illustrates that the equivalence of representing the output of the sampler operating on a signal, $\tilde{X}(t)$, without phase shift, ϕ, weighted by $\cos\phi$, and the original sampled $X(t)$, which does have a phase shift. The additional requirement is that a time aperture of T_A corresponds to π radians.

Next, consider the UFT kernel:

$$D_1 \triangleq \int_{-\infty}^{\infty}(u(t)-u(t-T_A))\sin(t+\phi)dt \qquad \text{EQ. (96)}$$

Using trigonometric identities yields:

$$D_1 \triangleq A\cos(\phi)\int_{-\infty}^{\infty}(u(t)-u(t-T_A))\sin(t)dt \qquad \text{EQ. (97)}$$

Now the kernel does not possess a phase term, and it is clear that the aperture straddles the sine half cycle depicted in FIG. 184. In EQ. (97), $\cos\phi$ is a weighting factor on the result, which originally illustrated the non-ideal alignment of the present invention clock and carrier signal. Trigonometric identities provide a means of realigning the present invention clock and carrier signal while accounting for the output result due to phase skew.

Consider the ideal aperture of embodiments of the invention shown in FIG. 185. Notice that the ideal aperture is illustrated as possessing two equal ½ aperture components. Hence the UFT kernel for embodiments of the invention can be rewritten as:

$$D_1 \triangleq A\cos(\phi)\left[\int_{-\infty}^{\infty}\left(u(t)-u\left(T_A/2\right)\right)\sin(t)dt+\int_{-\infty}^{\infty}\left(u\left(t-T_A/2\right)-u(t-T_A)\right)\sin(t)dt\right]$$

EQ. (98)

It should also be apparent to those skilled in the relevant arts given the discussion herein that the first integral is equivalent to the second, so that;

$$D_1 = 2A\cos(\phi)\int_{-\infty}^{\infty}\left(u(t)-u\left(t-T_A/2\right)\right)\sin(t)dt$$

EQ. (99)

As illustrated in FIG. 186, a property relating unit step functions and delta functions is useful. In FIG. 186, a step function is created by integrating a delta function. Therefore;

$$D_1 = 2A\cos(\phi)\int_{-\infty}^{\infty}\left[\int_{-\infty}^{t}\delta\left(t'\right)dt'-\int_{-\infty}^{t}\delta\left(t'-T_A/2\right)dt'\right]\sin(t)\,dt$$

EQ. (100)

Using the principle of integration by parts yields EQ. (101).

$$D_1 = 2A\cos(\phi)\int_{-\infty}^{t}\cos(t')\,\delta\left(t'\right)dt'+2A\cos(\phi)\int_{-\infty}^{t}\cos(t')\,\delta\left(t'-T_A/2\right)dt$$

$$= 2A\cos\phi\int_{-\infty}^{t}\sin(t')\delta\left(t-T_A/2\right)dt'$$

$$= 2A\cos(\phi), \text{ for } T_A=\pi$$

EQ. (101)

This is a remarkable result because it reveals the equivalence of the output of embodiments of the present invention with the result presented earlier for the arbitrarily phased ideal impulse sampler, derived by time sifting. That is, in embodiments, the UFT transform calculates the numerical result obtained by an ideal sampler. It accomplishes this by averaging over a specially constructed aperture. Hence, the impulse sampler value expected at $T_A/2$ is implicitly derived by the UFT transform operating over an interval, T_A. This leads to the following very important implications for embodiments of the invention:

- The UFT transform is very easy to construct with existing circuitry hardware, and it produces the results of an ideal impulse sampler, indirectly, without requiring an impulse sampler.
- Various processor embodiments of the present invention reduce the variance of the expected ideal sample, over that obtained by impulse sampling, due to the averaging process over the aperture.

8.4 Proof Statement for UFT Complex Downconverter Embodiment of the Present Invention

The following analysis utilizes concepts of the convolution property for the sampling waveform and properties of the Fourier transform to analyze the complex clock waveform for the UFT as well as the down conversion correlation process. FIG. 187 illustrates this process.

In addition *r(t)* is considered filtered, by a bandpass filter. In one exemplary embodiment, sub-optimal correlators approximate the UFT. This analysis illustrates that some performance is regained when the front-end bandpass filter is used, such that the derived correlator kernel resembles the optimal form obtained from matched filter theory. Furthermore, the analysis illustrates that the arbitrary phase shift of a carrier on which the UFT operates, does not alter the optimality of the correlator structure which can always be modeled as a constant times the optimal kernel. This is due to the fact that UFT is by definition matched to a pulse shape resembling the carrier half cycle which permits phase skew to be viewed as carrier offset rather than pulse shape distortion.

Using the pulse techniques described above, describing pulse trains, the clock signal for UFT may be written as equation 18802 of FIG. 188.

$p_c(t) \triangleq$ A basic pulse shape of the clock (gating waveform), in our case defined to have specific correlation properties matched to the half sine of the carrier waveform.

$T_s \triangleq$ Time between recursively applied gating waveforms.

$T_A \triangleq$ Width of gating waveform

In FIG. 188, $C_I(t)$ in equation 18804 and $C_Q(t)$ in equation 18806 are considered to be complex clocks shifted in phase by $T_A/2$. The received carrier is related to T_A by $f_c \approx (2T_A)^{-1}$

Although the approximation is used, ideal carrier tracking for coherent demodulation will yield an equal sign after lock. However, this is not required to attain the excellent benefit from UFT processing. Other sections herein provide embodiments that develop expressions for C_I and C_Q from Fourier series analysis to illustrate the components of the gating waveforms at the Carrier frequency which are harmonically related to T_s.

By the methods described above, the Fourier transform of the clock is found from:

$$C_I(f) = \Im\left\{ \sum_{m=-\infty}^{\infty} \delta(t - mT_s) \right\} P_c(f) \qquad \text{EQ. (102)}$$

$$C_I(f) = \sum_{n=-\infty}^{\infty} \frac{T_A}{T_s} \frac{\sin(n\pi f_s T_A)}{n\pi f_s T_A} \cdot \delta(f - nf_s) \qquad \text{EQ. (103)}$$

C_Q possesses the same magnitude response of course but is delayed or shifted in phase and therefore may be written as:

$$C_Q(f) = C_I(f) e^{-jn\pi f T_A} \qquad \text{EQ. (104)}$$

When T_A corresponds to a half sine width then the above phase shift related to a $\frac{\pi}{2}$ radians phase skew for C_Q relative to C_I.

In one exemplary embodiment, consider then the complex UFT processor operating on a shifted carrier for a single recursion only,

$$S_0(t) = \int_0^{T_A} r(t) C_I(t) dt + \int_{T_A/2}^{3T_A/2} r(t) C_Q(t) dt \qquad \text{EQ. (105.1)}$$

$$S_0(t) = \int_0^{T_A} (A\sin(\omega t + \phi) + n(t))C_I(t)dt + \int_{T_A/2}^{3T_A/2} (A\sin(\omega t + \phi) + n(t))C_Q(t)dt \quad \text{EQ. (105.2)}$$

This analysis assumes that *r(t),* the input carrier plus noise, is band limited by a filter. In this case therefore the delta function comb evident in the transform of C_I and C_Q are ignored except for the components at the carrier. Embodiments in other sections break C_I and C_Q into a Fourier series. In this series, only the harmonic of interest would be retained when the input waveform *r(t)* is bandpass limited because all other cross correlations tend to zero. Hence,

$$S_0(t) \sim K\int_0^{T_A} (A\sin(\omega t + \phi) + n(t))\sin(\omega t)dt + K\int_{T_A/2}^{3T_A/2} (A\sin(\omega t + \phi) + n(t))\cos(\omega t)dt \quad \text{EQ. (105.3)}$$

$$S_0(t) \sim K\int_0^{T_A} (A\sin(\omega t)\cos\phi + \cos(\omega t)\sin\phi + n(t))\sin(\omega t)dt + K\int_{T_A/2}^{3T_A/2} (A\sin(\omega t)\cos\phi + \cos(\omega t)\sin\phi + n(t))\cos(\omega t)dt \quad \text{EQ. (105.4)}$$

The clock waveforms have been replaced by the single sine and cosine components from the Fourier transform and Fourier series, which produce the desired result due to the fact that a front-end filter filters all other spectral components. This produces a myriad of cross correlations for the complex UFT processor. K is included as a scaling factor evident in the transform.

$$S_0(t) = KA\cos\phi \overbrace{\int_0^{T_A} (\sin(\omega t))^2}^{optimal\ correlator} dt +$$

$$K\int_0^{T_A} n(t)\sin\omega t dt + KA\sin\phi \overbrace{\int_{T_A/2}^{3T_A/2} (\cos(\omega t))^2}^{optimal\ correlator} dt + K\int_{T_A/2}^{3T_A/2} n(t)\cos\omega t dt$$

EQ. (106.1)

$$\therefore S_0(t) = \left(\frac{KA\pi}{2}\cos\phi + \tilde{n}_I\right) I \text{ component} \qquad \text{EQ. (106.2)}$$

$$+\left(\frac{KA\pi}{2}\sin\phi + \tilde{n}_Q\right) Q \text{ component} \qquad \text{EQ. (106.2.1)}$$

$$\text{where } K = \left(\frac{T_A}{T_s}\frac{\sin\left(n\pi\frac{T_A}{T_s}\right)}{\left(n\pi\frac{T_A}{T_s}\right)}\right) \qquad \text{EQ. (106.3)}$$

A and ϕ are the original components of the complex modulation envelope (amplitude and phase) for the carrier and are assumed to vary imperceptibly over the duration for T_A. What is very interesting to note is that the above equations are exactly the optimum form for the complex correlator whose pulse shape is a half sine with components weighted by cosine for I, and sine for Q. Furthermore, when an input bandpass filter is considered as a part of the system then the approximate kernels used throughout various analyses based on the gating function become replaced by the ideal matched filter analogy. Hence, the approximation in CMOS using rectangular gating functions, which are known to cause only a 0.91 dB hit in performance if C is selected correctly, probably can be considered pessimistic if the receiver front end is filtered.

8.5 Acquisition and Hold Processor Embodiment

As illustrated in FIG. 189, embodiments of the present invention can be approximately modeled as a particular case of a sampling system. In the example model in FIG. 189, both an acquisition phase and a hold phase for each T_s cycle is shown, where:

$r(t)\underline{\Delta}$ Input Waveform RF Modulated Carrier Plus Noise

$C_A(t)\underline{\Delta}$ Present Invention Aperture Waveform Pulse Train

$\delta_H(t)\underline{\Delta}$ Holding Phase Impulse Train

$h_A(t)\underline{\Delta}$ Integrator Impulse Response of the present Invention

$h_H(t)\underline{\Delta}$ ⧧0DH Portion of Present Invention Impulse Response

The embodiment in FIG. 189 consists of a gating device followed by a finite time integrator, then an ideal sampler, and finally a holding filter, which accumulates and stores the energy from the acquisition phase. This is called an acquisition and hold processor. The acquisition phase of the operation is described by:

$$X(t) = C_T(t)r(t) * h_A(t) \qquad \text{EQ. (107)}$$

$$X(t) = \sum_{k=-\infty}^{\infty}\left(u(t-kT_s) - u(t-(kT_s+T_A))\right)A_k\left(\sin(\omega_c t+\phi_k)\right) * h_A(t)) \qquad \text{EQ. (108)}$$

The ultimate output includes the hold phase of the operation and is written as:

$$S_0(t) = (X(t)\delta_H(t)) * h_H(t) \qquad \text{EQ. (109)}$$

$$S_0(t) = \sum_{k=-\infty}^{\infty}(X(t)\delta_H(t-k(T_s))) * u(t-(kT_s+T_A)) - u(t-(k+1)T_s) \qquad \text{EQ. (110)}$$

$$T = T_s - T_A \qquad \text{EQ. (111)}$$

This embodiment considers the aperture operation as implemented with an ideal integrator and the hold operation as implemented with the ideal

integrator. As shown elsewhere herein, this can be approximated by energy storage in a capacitor under certain circumstances.

The acquisition portion of the operation possesses a Fourier transform given by:

$$X_0(\omega) = \Im_0\{X_0(t)\} = \sum_{k=-\infty}^{\infty} \frac{1}{2\pi T_s} \overbrace{\delta(\omega - k\omega_s)}^{Harmonic\ Sifter} \overbrace{\left(\frac{T_A}{2} e^{j\omega T_A/2} \frac{\sin(\omega T_A/2)}{\omega T_A/2}\right)}^{Finite\ Time\ Integrator} \underbrace{S_i(\omega)_C}_{Original\ Information\ Specturm\ Chopped\ by\ C(t)}$$

$S_i(\omega) = \Im\{r(t)\}$ (Modulated Information Spectrum)

$S_0(\omega)$ can be found in a similar manner.

$$\Im\{S_0(t)\} = \sum_{k=-\infty}^{\infty} \frac{1}{2\pi T_s} \overbrace{\delta(\omega - k\omega_s)}^{Harmonic\ Sifter} \overbrace{\left(\frac{T}{2} e^{j\omega T_A/2} \frac{\sin(\omega T/2)}{\omega T/2}\right)}^{Z0DH\ Response} X(\omega)$$

$T = T_s - T_A$

The example of FIG. 190 illustrates the various components of the above transform superimposed on the same graph, for a down conversion case, where T_A is chosen as a single aperture realization and the 3rd sub harmonic is used for down conversion. The analysis does not consider the affect of noise, although, it is straightforward to accomplish, particularly in the case of AWGN. The lowpass spectrum possesses nulls at nf_{SA}, $n = 0, \pm 1, \pm 2, \ldots$, where $f_s = (T_s - T_A)^{-1}$. This Z0DH spectral response is also present at each harmonic of f_s, although it is not indicated by the graphic.

The acquisition portion of the Fourier transform yields the following an important insight:

$$X_0(\omega) = \frac{KT_A}{T_s} \sum_{k=-\infty}^{\infty} \delta(\omega - k\omega_s) \left(e^{j\omega T_A/2} \frac{\sin\left(\omega \frac{T_A}{2}\right)}{\omega \frac{T_A}{2}}\right) \cdot S_i(\omega)_c$$

EQ. (112)

$$S_i(\omega)_c = A_k T_A e^{j\omega T_A/2} \frac{\sin\left(\omega\left(T_A/2\right)\right)}{\omega\left(T_A/2\right)} \left(\delta(\omega-\omega_c)+\delta(\omega+\omega_c)\right)$$

EQ. (113)

As should be apparent to persons skilled in the relevant arts given the discussion herein, down conversion occurs whenever $k\omega_s = \omega_c$. It is useful to find $T_{A,}$ which maximizes the component of the spectrum at ω_c, which is subject to down conversion and is the desired signal. This is accomplished simply by examining the kernel.

$$\tilde{X} \underline{\Delta} \left| \frac{T_A}{T_s} \frac{\sin\left(\omega\left(T_A/2\right)\right)}{\omega\left(T_A/2\right)} \right| \qquad \text{EQ. (114)}$$

For $\omega = \omega_c$,

$$\tilde{X} = \left| \frac{T_A}{n \cdot T_c} \frac{\sin\left(\pi \frac{T_A}{T_c}\right)}{\left(\pi \frac{T_A}{T_c}\right)} \right|, \quad nT_c = T_s \text{ for Harmonic Conversion}$$

$$\therefore \tilde{X} = \frac{1}{n\pi} \sin\left(\pi \frac{T_A}{T_c}\right) \qquad \text{EQ. (115)}$$

The kernel is maximized for values of $\frac{T_A}{T_c} = 1/2,\ 3/2,\ 5/2, \cdots$

Advocates of impulse samplers might be quick to point out that letting $T_A \to 0$ maximizes the sinc function. This is true, but the sinc function is multiplied by T_A in the acquisition phase. Hence, a delta function that does not have infinite amplitude will not acquire any energy during the acquisition phase of the sampler process. It must possess infinite amplitude to cancel the effect of $T_A \to 0$ so that the multiplier of the sinc function possesses unity weighting. Clearly, this is not possible for practical circuits.

On the other hand, embodiments of the present invention with $\frac{T_A}{T_c} = 1/2,\ 3/2,\ 5/2, \cdots$ etc., does pass significant calculable energy during the acquisition phase. This energy is directly used to drive the energy storage element of Z0DH filter or other interpolation filter, resulting in practical RF impedance circuits. The cases for T_A/T_c other than $1/2$ can be represented by multiple correlators, for example, operating on multiple half sine basis.

Moreover, it has been shown that the specific gating aperture, $C(t)$, does not destroy the information. Quite the contrary, the aperture design for embodiments of the present invention produces the result of the impulse sampler, scaled by a gain constant, and possessing less variance. Hence, the delta sifting criteria, above trigonometric optimization, and correlator principles all point to an aperture of $\frac{T_A}{T_c} = \frac{1}{2}$ nominal.

If other impulse responses are added around the present invention (i.e., energy storage networks, matching networks, etc.) or if the present invention is implemented by simple circuits (such as the RC processor) then in embodiments the optimal aperture can be adjusted slightly to reflect the peaking of these other embodiments. It is also of interest to note that the Fourier analysis above predicts greater DC offsets for increasing ratios of $\frac{T_A}{T_c}$. Therefore, for various embodiments, $\frac{T_A}{T_c} = \frac{1}{2}$ is probably the best design parameter for a low DC offset system.

9. Comparison of the UFT Transform to the Fourier Sine and Cosine Transforms

The sine and cosine transforms are defined as follows:

$$F_c(\omega) \triangleq \int_0^\infty f(t)\sin\ \omega t\ dt\ \omega \geq 0 \text{ (sine transform)} \qquad \text{EQ. (116)}$$

$$F_s(\omega) \triangleq \int_0^\infty f(t)\cos\ \omega t\ dt\ \omega \geq 0 \text{ (cosine transform)} \qquad \text{EQ. (117)}$$

Notice that when $f(t)$ is defined by EQ. (118):

$$f(t) = u(t) - u(u - T_A) \qquad \text{EQ. (118)}$$

the UFT transform kernel appears as a sine or cosine transform depending on ϕ. Hence, many of the Fourier sine and cosine transform properties may be used in conjunction with embodiments of the present invention to solve signal processing problems.

The following sine and cosine transform properties predict the following results of embodiments of the invention:

Sine and Cosine Transform Property	Prediction of Embodiments of the Invention
Frequency Shift Property	Modulation and Demodulation while Preserving Information
Time Shift Property	Aperture Values Equivalent to Constant Time Delta Time Sift.
Frequency Scale Property	Frequency Division and Multiplication

Of course many other properties are applicable as well. The subtle point presented here is that for embodiments the UFT transform does in fact implement the transform, and therefore inherently possesses these properties.

Consider the following specific example: let $f(t) = u(t) - u(t - T_A)$ and let $\omega = 2\pi f = \pi f_A = 1$.

$$\Im_c[f(t)] = \int_0^{T_A} \cos(\omega t)\ dt = \frac{1}{\omega}\ \sin \omega T_A = 0 \qquad \text{EQ. (119)}$$

$$\Im_s[f(t)] = \frac{1}{\omega} - \frac{1}{\omega}\ \cos \omega T_A = 2 \qquad \text{EQ. (120)}$$

This is precisely the result for D_{1c} and D_{1s}. Time shifting yields:

$$\Im_s[f_0(t + T_s) + f_0(t - T_s)] = 2F_s(\omega)\cos(T_s\omega) \text{(Time Shift Property)}$$

Let the time shift to be denoted by T_s.

$$f(t) = u(t) - u(t - T_A) \qquad \text{EQ. (121)}$$

$$f_0(t)\ \Delta\ \frac{1}{2}(u(t + T_s) - u(t)) + \frac{1}{2}(u(t) - u(t - T_s)) \qquad \text{EQ. (122)}$$

Notice that $f_0(t)$ has been formed due to the single sided nature of the sine and cosine transforms. Nevertheless, the amplitude is adjusted by $1/2$ to

accommodate the fact that the energy must be normalized to reflect the odd function extension. Then finally:

$$\Im_s\left[f_0(t+T_s)+f_0(t-T_s)\right]=\frac{2}{2}F_s(\omega)\cos(T_s\omega)=2\cos\left(\pi T_s/T_A\right)$$

EQ. (123)

which is the same solution for phase offset obtained earlier by other means.

The implications of this transform may be far reaching when it is considered that the discrete Fourier sine and cosine transforms are originally based on the continuous transforms as follows:

$$\Im_c\{f(t)\}=\int_0^\infty f(t)\cos\omega t\ dt \qquad \text{EQ. (124)}$$

$$\Im_{DC}\{f(t)\}\ \triangleq\ \Im\{f(n)\}=\sqrt{\frac{2}{N}}\sum_{m=0}^{N}\alpha_m\alpha_n\cos\left(\frac{mn\pi}{N}\right)\ f(n) \qquad \text{EQ. (125)}$$

That is, the original kernel $\cos(\omega t)$ and function $f(t)$ are sampled such that:

$f(n)\ \triangleq$ Sampled Version of $f(t)$

$\omega_m=2\pi_m\Delta f$

$t_n=n\Delta t$

$\Delta f \triangleq$ Frequency Sample Interval

$\Delta t \triangleq$ Time Sample Interval

Hence the new discrete cosine transform kernel is:

$$k_c(m,n)=\cos(2\pi mn\ \Delta f\Delta t)=\cos(\pi mn/n)\ \Delta f\Delta t=1/2N$$

EQ. (126)

N is the total number of accumulated samples for m, n, or the total record length.

In recent years, the discrete cosine transform (DCT) and discrete sine transform (DST) have gained much recognition due to their efficiency for waveform coding compression, spectrum analysis, etc. In fact, it can be shown that these transforms can approach the efficiency of Karhunen-Loeve

transforms (KLT), with minimal computational complexity. The implication is that the sifted values from D_1 could be used as DCT sample values $f(n)$. Then the DCT and DST properties will apply along with their processing architectures. In this manner, communications signals, like OFDM, could be demodulated in a computationally efficient manner. Many other signal processing applications are possible using the present invention, and the possibilities are rich and varied.

10. Conversion, Fourier Transform, and Sampling Clock Considerations

The previous sub-sections described how embodiments of the present invention involve gating functions of controlled duration over which integration can occur. This section now addresses some consideration for the controlling waveform of the gating functions.

For sub harmonic sampling:

$$f_s = f_c / M$$

$f_s \triangleq$ Sample Rate

$f_c \triangleq$ Carrier Frequency

$M \triangleq$ As an integer such that $0 < M < \infty$

The case M=1 represents a classic down conversion scenario since $f_s = f_c$. In general though, M will vary from 3 to 10 for most practical applications. Thus the matched filtering operation of embodiments of the present invention is applied successively at a rate, f_s, using the approach of embodiments of the present invention. Each matched filter/correlator operation represents a new sample of the bandpass waveform.

The subsequent equations illustrate the sampling concept, with an analysis base on approximations that ignore some circuit phenomena. A more rigorous analysis requires explicit transformation of the circuit impulse response. This problem can be solved by convolving in the time domain as

well, as will be apparent to persons skilled in the relevant arts given the discussion herein. The results will be the same. The analysis presented herein is an abbreviated version of one provided above. As in the subsection 8, the acquisition portion of the present invention response is analyzed separately from the hold portion of the response to provide some insight into each. The following sub-section uses a shorthand notation for convenience.

$$X_0(t) = S_i(t)\sum_{k=-\infty}^{\infty}\tilde{C}(t-kT_s) \text{ (approximate output of acquisition)}$$

EQ. (127)

$X_0(t)\triangleq$ Output of Sample

$S_i[t]\triangleq$ Waveform being Sampled

$k\triangleq$ Sampling Index

$T_s\triangleq$ Sampling Interval $= f_s^{-1}$

$\tilde{C}(t-kT_s)\ \triangleq$ Quasi-Matched Filter/Correlator Sampling Aperture, which includes averaging over the Aperture.

EQ. (127) can be rewritten a:

$$X_0(t) \cong \sum_{k=-\infty}^{\infty} S_i(kT_s)\ * \tilde{C}(t-kT_s) \qquad \text{EQ. (128)}$$

If $\tilde{C}(t)$ possesses a very small aperture with respect to the inverse information bandwidth, $T_A << BW_i^{-1}$, then the sampling aperture will weight the frequency domain harmonics of f_s. The Fourier transform and the modulation property may be applied to EQ. (128) to obtain EQ. (129) (note this problem was solved above by convolving in the time domain).

$$X_0(\omega) = \left(S_i(\omega)_c\ \tilde{C}(\omega) \right) \qquad \text{EQ. (129)}$$

$$\therefore X_0(\omega) \cong \frac{K}{T_s}\sum_{k=-\infty}^{\infty}\delta_i(\omega - k\omega_s)\left[\frac{T_A \cdot e^{j\omega T_A/2}}{2}\frac{\sin(\omega T_A/2)}{\omega T_A/2}\right]\cdot S_i(\omega)_c$$

EQ. (130)

$K \triangleq$ Arbitrary Gain Constant, which includes a $1/2\pi$ factor

$\omega \triangleq 2\pi f$

Essentially, on the macroscopic frequency scale, there is a harmonic sample comb generated, which possesses components at every Nf_s for N = 1,2,3...∞, with nulls at every $Z \cdot f_A$, where f_A is defined as T_A^{-1}. FIG. 191 illustrates this result.

The thickness of each spike in FIG. 191 illustrates the surrounding band produced from $S_i(\omega)$. $S_i(\omega)$ is a complex transform including magnitude and phase, which can be assigned a vector representation in the time domain (i.e., I and Q components). The natural action of embodiments of the present invention, in the hold portion of the response, acts as a lowpass filter in the down conversion case, thereby reducing the levels of all the harmonic sidebands. Likewise, the up converter utilizes a bandpass matched filter to extract the desired carrier and reject unwanted images.

Notice that each harmonic including baseband possesses a replica of $S_i(\omega)$ which is in fact the original desired signal. { $S_i(\omega)$ is the original information spectrum and is shown to survive the acquisition response of the present invention (i.e., independent integration over each aperture)}. Lathi and many others pointed out that $\tilde{C}(\omega)$ could be virtually any harmonic function and that conversion to baseband or passband will result from such operations on $S_i(t)$.

Each discrete harmonic spectrum provides a potential down conversion source to baseband (at DC). Of course, theoretically, there cannot be a conversion of $Z \cdot f_a$ because of the spectral nulls. FIG. 191 illustrates the important relationships between f_s, f_a, and the relative harmonic conversion efficiency related to the sinc^2 function harmonic comb weighting, resulting from a simple rectangular sampling aperture.

It should also be noted that in all practical cases, $f_s >> 2 \cdot BW_i$, so that Nyquist criteria are more than satisfied. The lowpass response of embodiments of the present invention can be ideally modeled as a zero order data hold filter, with a finite time integrator impulse response duration of $T = T_s - T_A$. The ultimate output Fourier transform is given by EQ. (131).

$$S_0(\omega) = \sum_{k=-\infty}^{\infty} \underbrace{\frac{K}{T_s}\delta(\omega - k\omega_s)}_{Harmonic\ Sifter} \underbrace{\left(\frac{T}{2} e^{j\omega T/2} \frac{\sin \omega T/2}{\omega T/2}\right)}_{Z0DH\ Response} \cdot \underbrace{X(\omega)}_{Acquisition\ Response}$$

EQ. (131)

The $Z0DH$ is a type of lowpass filter or sample interpolator which provides a memory in between acquisitions. Each acquisition is accomplished by a correlation over T_A, and the result becomes an accumulated initial condition for the next acquisition.

10.1 Phase Noise Multiplication

Typically, processor embodiments of the present invention sample at a sub-harmonic rate. Hence the carrier frequency and associated bandpass signal are down converted by a $M \cdot f_s$ harmonic. The harmonic generation operation can be represented with a complex phasor.

$$S_{amp}(t) \triangleq \left(e^{-j\omega_s t + \phi(t)}\right)^m \qquad \text{EQ. (132)}$$

$S_{amp}(t)$ can be rewritten as:

$$S_{amp}(t) = e^{-jM\omega_s t} \cdot e^{M\phi(t)} \qquad \text{EQ. (133)}$$

$\phi(t) \triangleq$ Phase Noise on the Conversion Clock

As EQ. (133) indicates, not only is the frequency content of the phasor multiplied by M but the phase noise is also multiplied by M. This results in an M-tuple convolution of the phase noise spectrum around the harmonic. The total phase noise power increase is approximated by EQ. (134).

$$\phi = \underline{\Delta} 20 \log_{10} \mathrm{M} \text{ (Phase Noise)} \qquad \text{EQ. (134)}$$

That is, whatever the phase jitter component, $\phi(t)$, existing on the original sample clock at Mf_s, it possesses a phase noise floor degraded according to EQ. (134).

10.2 AM–PM Conversion and Phase Noise

This section describes what the conversion constant and the output noise is for AM to PM conversion according to embodiments of the present invention, considering the noise frequency of the threshold operation. As illustrated in FIG. 192, suppose that the output of a sine signal source must be filtered and compared, in order to obtain a suitable clock signal. For cases where the equivalent input noise power of the threshold device can be considered to be much less than the input power source sine wave, a single zero crossing per cycle of sine wave can be assumed to occur. For such low noise cases, the threshold operation may be viewed as an AM to PM conversion device.

The slope at the zero crossings of a pure sine wave, $s(t) = A \sin \omega t$, can be calculated. Differentiating s(t) with respect to *t* yields $s(t)' = \omega A \cos \omega t$. For ω A≠0, the zero crossings occur at $\omega t = \pi/2, 3\pi/2, 5\pi/2 \ldots$.

$$\therefore t = \frac{1}{4f}, \frac{3}{4f}, \frac{5}{4f} \ldots \{\text{for } s(t)\} \qquad \text{EQ. (135)}$$

These zero crossings represent the points of minimum slope or crests of the original *s(t)*. The maximum slope is found at the zero crossings of. s(t) at ωt = 0, π, 2π, . . . etc. Plugging those arguments into $s(t)'$ give slopes of: Slope = ωA, -ωA, ωA, -ωA . . . etc. The time at which these zero crossings occur is given by: ωt = π, 2π, 3π . . . $t = \frac{1}{2f}, \frac{1}{f}, \frac{3}{2f}, \ldots \{for\ s(t)\}$.

It stands to reason that for the low noise power assumption, which implies one zero crossing per carrier cycle, the slope at the zero crossing will be modified randomly if a Gaussian process *(n(t))* is summed to the signal. Of course, if the change in slope of the signal is detectable, the delta time of the zero crossing is detectable, and hence phase noise is produced. The addition of noise to the signal has the effect of moving the signal up and down on the amplitude axis while maintaining a zero mean. This can be written more formally as:

$$\left|\frac{\partial\, s(t)}{\partial\, t}\right| = \omega A = \text{ for } \omega\, t = n\pi/2 \qquad \text{EQ. (136)}$$

If A is replaced by A-Δa, where Δa represents the noise deviation, then one will not always observe a zero crossing at the point of maximum slope ωA. Sometimes the zero crossing will occur at ω(A-Δa). This leads to the low noise approximation:

$$\omega(\mathrm{A} - \Delta\mathrm{a}) = \omega \mathrm{A}\cos[\omega(\mathrm{t} \pm \varepsilon)] \qquad \text{EQ. (137)}$$

$$\arccos\left(\frac{\frac{A - \Delta a}{A}}{\omega}\right) = t \pm \varepsilon \qquad \text{EQ. (138)}$$

The low noise assumption implies that the low noise power prohibits the arcos function from transforming the Gaussian pdf of the noise. That is, $\pm\Delta$a occurs over minute ranges for the argument of the arcos and hence the relationship is essentially linear. Secondly, since A is a peak deviation in the sine wave Δa will be considered as a peak deviation of the additive noise process. This is traditionally accepted as being 4σ where σ is the standard deviation of the process and σ^2 is the variance. Therefore we write K $\arccos(1 - 4\sigma / \mathrm{A}) = \mathrm{t} \pm \varepsilon$, where ε represents a peak time deviation in the zero crossing excursion, $K = 1/\omega$, and t is the mean zero crossing time given

previously as: $t = {}^{1}\!/\!_{sf}, {}^{1}\!/\!_{f}, {}^{3}\!/\!_{2f}, \ldots$ If only the deviation contribution to the above equation is retained, the equation reduces to:

$$K\cos^{-1}\left(\frac{4\sigma}{A}\right) = \varepsilon = \Delta t \qquad \text{EQ. (139)}$$

Since for $4\sigma / A << .01$, the above function is quasi-linear, one can write the final approximation as:

$$K\frac{4\sigma}{A} = \Delta t = \frac{4\sigma}{\omega A} \text{ seconds (peak)} \qquad \text{EQ. (140)}$$

An appropriate conversion to degrees becomes,

$$360^{\circ} f_c = \frac{4\sigma_x}{\frac{4\sigma}{\omega_c A}} \qquad \text{EQ. (141)}$$

f_c = frequency of carrier

σ_x = phase noise in degrees rms

σ = standard deviation of equivalent input comparator noise

$$\therefore \sigma_x = \frac{(360)\sigma}{2\pi A} \text{ degrees rms} \qquad \text{EQ. (142)}$$

$\frac{\sigma_x}{57.3}$ = radians rms = σ_ϕ

$\sigma_{\phi_x}{}^2$ = variance or power in dBc

Now a typical threshold operator may have a noise figure, NF, of approximately 15 dB. Hence, one can calculate σ_x (assume $\sigma_\phi{}^2 = 2.4x10^{-8} rad^2$ source phase noise):

$$-174 dBm/Hz + 15 + 10\log_{10} 100x10^6 = -79 dBm \qquad \text{EQ. (143)}$$

where 100 MHz of input bandwidth is assumed.

$$anti\log -7.9 = 1.26x10^{-8} milliwatts = 1.26x10^{-11} watts \qquad \text{EQ. (144)}$$

$$\therefore \sigma = \sqrt{1.26\text{x}10^{-11}} \cong 3.55\text{x}10^{-6} \qquad \text{EQ. (145)}$$

$$\sigma_x = \frac{(360)3.55x10^{-6}}{2\pi(.6)} \simeq 3.39x10^{-4} \text{ degrees rms}$$

$$\sigma_{\phi_x} \cong 5.92x10^{-6} \text{ rad rms}$$

$$\sigma_{\phi_t}{}^2 = \sigma_\theta{}^2 + \sigma_{\phi_x}{}^2 \simeq 2.4x10^{-8} + 3.5x10^{-11} \cong 2.4x10^{-8} rad^2$$

$\sigma_\theta{}^2 =$ phase noise of source before threshold device

Therefore, the threshold device has little to no impact on the total phase noise modulation on this particular source because the original source phase noise dominates. A more general result can be obtained for arbitrarily shaped waveforms (other than simple sine waves) by using a Fourier series expansion and weighting each component of the series according to the previously described approximation. For simple waveforms like a triangle pulse, the slope is simply the amplitude divided by the time period so that in the approximation:

$$\Delta t \simeq \frac{k4\sigma T_r}{A_T} \qquad \text{EQ. (146)}$$

k; an arbitrary scaling constant

T_r; time period for the ramping edge of the triangle

Hence, the ratio of $\left(\sigma T_r / A_r\right)$ is important and should be minimized.

As an example, suppose that the triangle pulse rise time is 500 nsec. Furthermore, suppose that the amplitude, A_T, is 35 milli volts. Then, with a 15 dB NF, the Δt becomes:

$$\Delta t = \frac{k \cdot 4 \cdot (3.55 \times 10^{-6}) V 500 nsec}{.035} \simeq 203 \text{ ps}$$

$\sigma \simeq 203/4 \cong 50.7$ ps (1Ω)

This is all normalized to a 1Ω system. If a 50Ω system were assumed then:

$\sigma \simeq 358.5$ ps (50Ω)

In addition, it is straight forward to extend these results to the case of DC offset added to the input of the threshold device along with the sine wave.

Essentially the zero crossing slope is modified due to the virtual phase shift of the input sine function at the threshold. DC offset will increase the phase noise component on the present invention clock, and it could cause significant degradation for certain link budgets and modulation types.

11. Pulse Accumulation and System Time Constant

11.1 Pulse Accumulation

Examples and derivations presented in previous sub-sections illustrate that in embodiments single aperture acquisitions recover energies proportional to:

$$E_\ell = \int_0^{T_A} S_i^2(t)dt = \frac{A_n^2 T_A}{2} \text{ (optimum aperture)} \qquad \text{EQ. (147)}$$

$A_n \triangleq$ as the carrier envelope weighting of the *nth* sample.

In addition, sub-section 8 above, describes a complete UFT transform over many pulses applicable to embodiments of the invention. The following description therefore is an abbreviated description used to illustrate a long-term time constant consideration for the system.

As described elsewhere herein, the sample rate is much greater than the information bandwidth of interest for most if not all practical applications.

$$f_s >> BW_i \qquad \text{EQ. (148)}$$

Hence, many samples may be accumulated as indicated in previous sub-sections, provided that the following general rule applies:

$$\frac{f_s}{\ell} > BW_i \qquad \text{EQ. (149)}$$

where ℓ represents the total number of accumulated samples. EQ. (149) requires careful consideration of the desired information at baseband, which must be extracted. For instance, if the baseband waveform consists of sharp

features such as square waves then several harmonics would necessarily be required to reconstruct the square wave which could require BW_i of up to seven times the square wave rate. In many applications however the base band waveform has been optimally prefiltered or bandwidth limited apriori (in a transmitter), thus permitting significant accumulation. In such circumstances, f_s / ℓ will approach BW_i.

This operation is well known in signal processing and historically has been used to mimic an average. In fact it is a means of averaging scaled by a gain constant. The following equation relates to EQ. (127).

$$\sum_{n=1}^{\ell} E_\ell = \sum_{\ell=1}^{x} \frac{A_n^2 T_A}{2} \cong \frac{\ell A^2 T_A}{2} \qquad \text{EQ. (150)}$$

Notice that the *nth* index has been removed from the sample weighting. In fact, the bandwidth criteria defined in EQ. (149) permits the approximation because the information is contained by the pulse amplitude**.** A more accurate description is given by the complete UFT transform, which does permit variation in *A*. *A* cannot significantly vary from pulse to pulse over an ℓ pulse interval of accumulation, however. If *A* does vary significantly, ℓ is not properly selected. *A* must be permitted to vary naturally, however, according to the information envelope at a rate proportional to BW_i. This means that ℓ cannot be permitted to be too great because information would be lost due to filtering. This shorthand approximation illustrates that there is a long term system time constant that should be considered in addition to the short- term aperture integration interval.

In embodiments, usually the long term time constant is controlled by the integration capacitor value, the present invention source impedance, the present invention output impedance, and the load. The detailed models presented elsewhere herein consider all these affects. The analysis in this section does not include a leakage term that was presented in previous sub-sections.

EQs. (149) and (150) can be considered a specification for slew rate. For instance, suppose that the bandwidth requirement can be specified in terms of a slew rate as follows:

$$SR = \times \frac{volts}{\mu \sec} \qquad \text{EQ. (151)}$$

The number of samples per μsec is given by:

$\ell_s = f_s \times 1 \times 10^{-6}$ (f_s is derived from the present invention clock rate)

If each sample produces a voltage proportional to $A^2 T_A / 2$ then the total voltage accumulated per microsecond is:

$$V_{\mu \sec} \cong \ell_s \frac{A^2 T_A}{2} \qquad \text{EQ. (152)}$$

The previous sub-sections illustrates how the present invention output can accumulate voltage (proportional to energy) to acquire the information modulated onto a carrier. For down conversion, this whole process is akin to lowpass filtering, which is consistent with embodiments of the present invention that utilize a capacitor as a storage device or means for integration.

11.2 Pulse Accumulation by Correlation

The previous sub-sections introduced the idea that in embodiments information bandwidth is much less than the bandwidth associated with the present invention's impulse response for practical applications. The concept of single aperture energy accumulation was used above to describe the central ideas of the present invention. As shown in FIG. 193, multiple aperture accumulation permits baseband waveform reconstruction. FIG. 193 illustrates the results from simulation of actual circuits according to embodiments of the present invention implemented with CMOS and passive components.

The staircase output of the example in FIG. 193 follows the complex modulation envelope for the input signal. Sub-section **5** predicts this result via

the time variant linear differential equation. FIG. 193 illustrates the staircase accumulation of half sine energy for three apertures based on 3x sampling. As can be seen in FIG. 193, the leakage between accumulations is very small.

12. Energy Budget Considerations

Consider the following equation for a window correlator aperture:

$$E_{ASO} = \int_0^{TA} A \cdot S_i(t)dt \qquad \text{EQ. (153)}$$

In EQ. (153), the rectangular aperture correlation function is weighted by A. For convenience, it is now assumed to be weighted such that:

$$E_{ASO} = \int_0^{TA} kA \cdot S_i(t)dt = 2A \text{ (normalized)} \qquad \text{EQ. (154)}$$

Since embodiments of the present invention typically operate at a sub-harmonic rate, not all of the energy is directly available due to the sub-harmonic sampling process. For the case of single aperture acquisition, the energy transferred versus the energy available is given by:

$$\frac{E_0}{E_i} = \frac{E_{ASO}}{2N} = \frac{A}{N} \qquad \text{EQ. (155)}$$

$N \triangleq$ harmonic of operation

The power loss due to harmonic operation is:

$$E_{LN} = 10 \log_{10}(2N) \qquad \text{EQ. (156)}$$

There is an additional loss due to the finite aperture, T_A, which induces (sin x/x) like weighting onto the harmonic of interest. This energy loss is proportional to:

$$E_{LSINC} \simeq \left(\frac{\sin(\pi N f_s T_A)}{\pi N f_s T_A} \right) \text{(up conversion only)} \qquad \text{EQ. (157)}$$

$N \cdot f_s \triangleq$ operating carrier frequency

$f_s \triangleq$ sampling rate (directly related to the clock rate)

EQ. (157) indicates that the harmonic spectrum attenuates rapidly as $N \cdot f_s$ approaches T_A^{-1}. Of course there is some attenuation even if that scenario is avoided. EQ. (157) also reveals, however, that in embodiments for single aperture operation the conversion loss due to E_{LSINC} will always be near 3.92dB. This is because:

$$\left(2 \cdot Nf_s\right)^{-1} = T_A \text{ (~3.92dB condition)} \qquad \text{EQ. (158)}$$

Another way of stating the condition is that T_A is always $^1/_2$ the carrier period.

Consider an ideal implementation of an embodiment of the present invention, without any circuit losses, operating on a 5th harmonic basis. Without any other considerations, the energy loss through the device is at minimum:

$$E_L = E_{LN} + E_{LSINC} = 10\text{dB} + 3.92 \simeq 14\text{dB (for up conversion)} \qquad \text{EQ. (159)}$$

Down conversion does not possess the 3.92dB loss so that the baseline loss for down conversion is that represented by EQ. (156). Parasitics will also affect the losses for practical systems. These parasitics must be examined in detail for the particular technology of interest.

Next suppose that a number of pulses may be accumulated using the multi-aperture strategy and diversity means of an embodiment of the present invention, as described above. In this case, some of the energy loss calculated by EQ. (159) can be regained. For example, if four apertures are used then the pulse energy accumulation gain is 6dB. For the previous example, this results in an overall gain of 6dB – 14dB, or -8dB (instead of –14dB). This energy gain is significant and will translate to system level specification improvements in the areas of noise frequency, intercept point, power consumption, size, etc. It should be recognized, however, that a diversity system with active split or separate amplifier chains would use more power and become more costly. In addition, in embodiments, energy storage networks coupled to the circuitry of the present invention may be used to

accumulate energy between apertures so that each aperture delivers some significant portion of the stored energy from the network. In this manner, some inefficiencies of the sub harmonic sampling process can be removed by trading impedance matching vs. complexity, etc., as further described below.

12.1 Energy Storage Networks

Embodiments of the present invention have been shown to be a type of correlator, which is applied to the carrier on a sub harmonic basis. It is also been shown herein that certain architectures according to embodiments of the invention benefit significantly from the addition of passive networks, particular when coupled to the front end of a processor according to the present invention used as a receiver. This result can be explained using linear systems theory.

To understand this, it is useful to consider the following. Embodiments of the present invention can be modeled as a linear, time-variant (LTV) device. Therefore, the following concepts apply:

- The LTV circuits can be modeled to have an average impedance; and
- The LTV circuits can be modeled to have an average power transfer or gain.

These are powerful concepts because they permit the application of the maximum bilateral power transfer theorem to embodiments of the present invention. As a result, in embodiments, energy storage devices/circuits which fly wheel between apertures to pump up the inter sample power can be viewed on the many sample basis (long time average) as providing optimum power transfer through matching properties. The between sample model on the time microscopic scale is best viewed on a differential equation basis while the time macroscopic view can utilize simpler analysis techniques such as the

maximum power transfer equations for networks, correlator theory, etc. The fact that the differential equations can be written for all time unifies the theory between the short time (between sample) view and long time (many sample accumulation) view. Fortunately, the concepts for information extraction from the output of the present invention are easily formulated without differential equation analysis.

Network theory can be used to explain why certain networks according to the present invention provide optimum power gain. For example, network theory explains embodiments of the present invention when energy storage networks or matching networks are utilized to 'fly wheel' between apertures, thereby, on the average, providing a good impedance match. Network theory does not explain, however, why T_A is optimal. For instance, in some embodiments, one may deliberately utilize an aperture that is much less than a carrier half cycle. For such an aperture, there is an optimal matching network nonetheless. That is, a processor according to an embodiment of the present invention utilizing an improper aperture can be optimized, although it will not perform as well as a processor according to an embodiment of the present invention that utilizes an optimal aperture accompanied by an optimal matching network.

The idea behind selecting an optimal aperture is matched filter theory, which provides a general guideline for obtaining the best correlation properties between the incoming waveform and the selected aperture. Any practical correlator or matched filter is constrained by the same physical laws, however, which spawned the maximum power transfer theorems for networks. It does not do any good to design the optimum correlator aperture if the device possesses extraordinary impedance mismatches with its source and load. The circuit theorems do predict the optimal impedance match while matched filter theory does not. The two work hand in hand to permit a practical explanation for:

- Why T_A is optimal; and
- How processors according to embodiments of the present invention are optimized for performance in practical circuits.

The following sub-section analyzes the present invention on a macroscopic scale using the notions of average impedance and power transfer.

12.2 Impedance Matching

When a processor embodiment according to the present invention is 'off,' there is one impedance, and when a processor embodiment according to the present invention is 'on,' there is another impedance due to the architecture of the present invention and its load. In practice, the aperture will affect the 'on' impedance. Hence, on the average, the input impedance looking into the circuitry of an embodiment of the present invention (i.e., its ports) is modified according to the present invention clock and T_A. Impedance matching networks must take this into account.

$$\not{Z}_{av} = \frac{V}{I_{av}} \qquad \text{EQ. (160)}$$

EQ. (160) illustrates that the average impedance, $\not{Z}_{av}$, is related to the voltage, V, divided by the average current flow, I_{av}, into a device, for example a processor according to an embodiment of the present invention. EQ. (160) indicates that for a processor according to an embodiment of the present invention the narrower T_A and the less frequent a sample is acquired, the greater $\not{Z}_{av}$ becomes.

To understand this, consider the fact that a 10th harmonic system according to an embodiment of the present invention operates with half as many samples as a 5th harmonic sample according to the present invention. Thus, according to EQ. (160), a 5th harmonic sample according to an embodiment of the present invention would typically possess a higher

input/output impedance than that a 10th harmonic system according to the present invention. Of course, practical board and circuit parasitics will place limits on how much the impedance scaling properties of the present invention processor clock signals control the processor's overall input/output impedance.

As will be apparent to persons skilled in the relevant arts given the discussion herein, in embodiments, matching networks should be included at the ports of a processor according to the present invention to accommodate $\not{Z}_{av}$, as measured by a typical network analyzer.

13. Time Domain Analysis

All signals can be represented by vectors in the complex signal plane. Previous sub-sections derived the result for down converting (or up converting) $S_i(t)$ in the transform domain via $S_i(\omega)$. An I/Q modem embodiment of the present invention, however, was developed using a time domain analysis. This time domain analysis is repeated here and provides a complementary view to the previous sub-sections.

FIG. 194 illustrates an embodiment of the present invention implementing a complex down converter architecture. Operation of this embodiment is described given by:

$$S_0(t_k) \cong \sum_{k=0}^{\infty} \left(S_i(t_k) + n(t_k)\right) \left(C_{Ik} + C_{Qk}\right) \qquad \text{EQ. (161.1)}$$

where $S_i(t_k)$ is defined as the kth sample from the UFT transform such that $S_i(t_k)$ is filtered over the kth interval, $n(t_k)$ is defined as the noise sample at the output of the kth present invention kernel interval such that it has been averaged by the present invention process over the interval, C_{Ik} is defined as the kth in phase gating waveform (the present invention clock), and C_{Qk} is defined as the kth quadrature phase gating waveform (the present invention clock).

The 'goodness' of $S_i(t_k)$ and $n_i(t_k)$ has been shown previously herein as related to the type of present invention processor used (e.g.., matched filtering/correlating processor, finite time integrating processor, or RC processor). Each t_k instant is the time tick corresponding to the averaging of input waveform energy over a T_A (aperture) duration. It has been assumed that C_{Ik} and C_{Qk} are constant envelope and phase for the current analysis, although in general this is not required. Many different, interesting processors according to embodiments of the present invention can be constructed by manipulating the amplitudes and phases of the present invention clock.

C_{Ik} and C_{Qk} can be expanded as follows:

$$C_{Ik} = K\frac{T_A}{T_s}\left[1+2\left(\frac{\sin\pi\frac{T_A}{T_s}}{\pi\frac{T_A}{T_s}}\cdot\cos 2\pi f_s t_k + \frac{\sin 2\pi\frac{T_A}{T_s}}{\pi\frac{T_A}{T_s}}\cdot\cos 4\pi f_s t_k + \frac{\sin 3\pi\frac{T_A}{T_s}}{3\pi\frac{T_A}{T_s}}\cdot\cos 6\pi f_s t_k \right.\right.$$
$$\left.\left. + \ldots\frac{\sin n\pi\frac{T_A}{T_s}}{n\pi\frac{T_A}{T_s}}\cdot\cos n\cdot 2\pi f_s t_k\right)\right]$$

EQ. (161.2)

$$C_{Qk} = K\frac{T_A}{T_s}\left[1+2\left(\frac{\sin\pi\frac{T_A}{T_s}}{\pi\frac{T_A}{T_s}}\cdot\sin 2\pi f_s t_k - \frac{\sin 2\pi\frac{T_A}{T_s}}{\pi\frac{T_A}{T_s}}\cdot\cos 4\pi f_s t_k - \right.\right.$$
$$\left.\left. \frac{\sin 3\pi\frac{T_A}{T_s}}{3\pi\frac{T_A}{T_s}}\cdot\sin 6\pi f_s t_k \ldots\frac{\sin n\pi\frac{T_A}{T_s}}{n\pi\frac{T_A}{T_s}}\cdot\cos\left(n\cdot 2\pi f_s t_k + n\phi\right)\right)\right]$$

EQ. (161.3)

The above treatment is a Fourier series expansion of the present invention clocks where:

$K \triangleq$ Arbitrary Gain Constant

$T_A \triangleq$ Aperture Time $= f_s^{-1}$

T_s $\triangleq$ The Present Invention Clock Interval or Sample Time

n $\triangleq$ Harmonic Spectrum Harmonic Order

ϕ $\triangleq$ As phase shift angle usually selected as 90° $\left(\pi/2\right)$ for orthogonal signaling

Each term from $C_{Ik,}\ C_{Qk}$ will down convert (or up convert). However, only the odd terms in the above formulation (for $\phi = \pi/2$) will convert in quadrature. ϕ could be selected otherwise to utilize the even harmonics, but this is typically not done in practice.

For the case of down conversion, $r(t)$ can be written as:

$$r(t_k) = \sqrt{2}A\left(\tilde{S}_{iI}(t_k)\cos(m \cdot 2\pi f t_k + \Theta) - \tilde{S}_{iQ}(t_k)\sin(m \cdot 2\pi f t_k + \Theta) + n(t)\right) \quad \text{EQ. (162)}$$

After applying ($C_{Ik,}\ C_{Qk}$) and lowpass filtering, which in embodiments is inherent to the present invention process, the down converted components become:

$$S_0(t_k)_I = A\ S_{iI}(t_k) + \tilde{n}_{Ik} \quad \text{EQ. (163)}$$

$$S_0(t_k)_Q = A\ S_{iQ}(t_k) + \tilde{n}_{Qk} \quad \text{EQ. (164)}$$

where:

$S_{iI}(t_k)$ $\triangleq$ The In phase component of the desired baseband signal.

$S_{iQ}(t_k)$ $\triangleq$ The quadrature phase component of the desired baseband signal.

$\tilde{n}_I, \tilde{n}_Q$ $\triangleq$ In phase and quadrature phase noise samples

m $\triangleq$ Is the harmonic of interest equal to one of the 'n' numbers, for perfect carrier synchronization.

Now m and n can be selected such that the down conversion ideally strips the carrier (mf_s), after lowpass filtering.

If the carrier is not perfectly coherent, a phase shift occurs as described in previous sub-section. The result presented above would modify to:

$$S_0(t) = \left(S_0(t)_I + jS_0(t)_Q\right) e^{j\phi} \qquad \text{EQ. (165)}$$

where ϕ is the phase shift. This is the same phase shift affect derived earlier as $\cos\phi$ in the present invention transform. When there is a slight carrier offset then ϕ can be written as $\phi(t)$ and the I and Q outputs represent orthogonal, harmonically oscillating vectors super imposed on the desired signal output with a beat frequency proportional to:

$$f_{error} \triangleq nf_s \pm m(f_s \pm f_\Delta) = f_s(n-m) + mf_\Delta \qquad \text{EQ. (166)}$$

$f_\Delta \triangleq$ as a slight frequency offset between the carrier and the present invention clock

This entire analysis could have been accomplished in the frequency domain as described herein, or it could have been formulated from the present invention kernel as:

$$S_0(t) = \mathrm{D}_{IQ}(S_i(t) + n(t)) \qquad \text{EQ. (167)}$$

The recursive kernel D_{IQ} is defined in sub-section 8 and the I/Q version is completed by superposition and phase shifting the quadrature kernel.

The previous equation for $r(t)$ could be replaced with:

$$BB(t) = \tilde{S}_{iI} \pm \tilde{S}_{iQ} \text{ where } f = 0 \text{ and } \Theta = \pi/4 \text{ and } n(t) = 0 \qquad \text{EQ. (168)}$$

BB(t) could be up converted by applying C_I, C_Q. The desired carrier then is the appropriate harmonic of C_I, C_Q whose energy is optimally extracted by a network matched to the desired carrier.

14. Complex Passband Waveform Generation Using the Present Invention Cores

This sub-section introduces the concept of using a present invention core to modulate signals at RF according to embodiments of the invention.

Although many specific modulator architectures are possible, which target individual signaling schemes such as AM, FM, PM, etc., the example architecture presented here is a vector signal modulator. Such a modulator can be used to create virtually every known useful waveform to encompass the whole of analog and digital communications applications, for "wired" or "wireless," at radio frequency or intermediate frequency. In essence, a receiver process, which utilizes the present invention, may be reversed to create signals of interest at passband. Using I/Q waveforms at baseband, all points within the two dimensional complex signaling constellation may be synthesized when cores according to the present invention are excited by orthogonal sub-harmonic clocks and connected at their outputs with particular combining networks. A basic architecture that can be used is shown in FIG. 195.

FIG. 195 depicts one embodiment of a based vector modulator according to the present invention. FIG. 195 shows I and Q inputs that can accept analog or balanced digital waveforms. By selecting I and Q appropriately, AM, FM, BPSK, QPSK, MSK, QAM, OFDM, multi-tone, and a host of other signals can be synthesized. In this embodiment of the present invention, the present invention cores are driven differentially on I and Q. $C_I, C_{\bar{I}}, C_Q, C_{\bar{Q}}$ are the in phase and quadrature sub-harmonic clocks, respectively, with their inverted phases as well. C_I and C_Q can be created in quadrature for I Q operation if the output power combiner is a 0° combiner. On the other hand, C_I and C_Q can be in phase when a 90° output power combiner is utilized at RF. This latter architecture can be used whenever the signaling bandwidth is very small with respect to the RF center frequency of the output and small with respect to the 1dB passband response of the combiner. If one assumes constant values on I and $\bar{I}$, the waveform diagrams in FIG 196 can be constructed. As indicated in FIG. 195, the power combiner and bandpass reconstruction filter are optional components.

In FIG. 196, C_I and $\overline{C_I}$ are out of phase by 180° if referenced back to the clock. In this case, clock refers to the sub-harmonic waveform used to generate C_I and $\overline{C_I}$. C_I is coincident with the rising edges of clock with a pulse width of T_A while $\overline{C_I}$ is coincident with the falling edges of clock with a pulse width of T_A. C_I and $\overline{C_I}$ activate two of the processors according to the present invention, as shown in FIG. 195, which are driven by differential signals. I_c is illustrated as if the system is ideal without losses, parasitics, or distortions. The time axis for I_c may be arranged in a manner to represent the waveform as an odd function. For such an arrangement, the Fourier series is calculated to obtain EQ. (169).

$$I_c(t) = \sum_{n=1}^{\infty} \left(\frac{4 \sin\left(\frac{n\pi T_A}{T_s}\right) \cdot \sin\left(\frac{n\pi}{2}\right)}{n\pi} \right) \cdot \sin\left(\frac{2n\pi t}{T_s}\right) \qquad \text{EQ. (169)}$$

To illustrate this, if a passband waveform must be created at five times the frequency of the sub-harmonic clock then a baseline power for that harmonic extraction can be calculated for $n = 5$. For the case of $n = 5$, it is found that the 5th harmonic yields:

$$I_c(t)\big|_{n=5} = \frac{4}{5\pi}\left(\sin(5\omega_s t)\right) \qquad \text{EQ. (170)}$$

This component can be extracted from the Fourier series via a bandpass filter centered around f_s. This component is a carrier at 5 times the sampling frequency.

This illustration can be extended to show the following:

$$m(t) \cdot I_c(t)\big|_{\substack{n=5 \\ \emptyset=(t)}} = \frac{4 \cdot m(t)}{5\pi}\left(\sin\left(5\omega_s t + 5\phi(t)\right)\right) \qquad \text{EQ. (171)}$$

This equation illustrates that a message signal may have been superposed on I and $\bar{I}$ such that both amplitude and phase are modulated, i.e., $m(t)$ for

amplitude and $\phi(t)$ for phase. In such cases, it should be noted that $\phi(t)$ is augmented modulo n while the amplitude modulation $m(t)$ is scaled. The point of this illustration is that complex waveforms may be reconstructed from their Fourier series with multi-aperture processor combinations, according to the present invention.

In a practical system according to an embodiment of the present invention, parasitics, filtering, etc., may modify $I_c(t)$. In many applications according to the present invention, charge injection properties of processors play a significant role. However, if the processors and the clock drive circuits according to embodiments of the present invention are matched then even the parasitics can be managed, particularly since unwanted distortions are removed by the final bandpass filter, which tends to completely reconstruct the waveform at passband.

Like the receiver embodiments of the present invention, which possess a lowpass information extraction and energy extraction impulse response, various transmitter embodiments of the present invention use a network to create a bandpass impulse response suitable for energy transfer and waveform reconstruction. In embodiments, the simplest reconstruction network is an L-C tank, which resonates at the desired carrier frequency $N \cdot f_s = f_c$.

V. Additional Embodiments

1. Example I/Q Modulation Receiver Embodiment

FIG. 197 illustrates an example I/Q modulation receiver 19700, according to an embodiment of the present invention. I/Q modulation receiver 19700 comprises a first Processing module 19702, a first optional filter 19704, a second Processing module 19706, a second optional filter 19708, a third Processing module 19710, a third optional filter 19712, a fourth Processing

module 19714, a fourth filter 19716, an optional LNA 19718, a first differential amplifier 19720, a second differential amplifier 19722, and an antenna 19772.

I/Q modulation receiver 19700 receives, down-converts, and demodulates a I/Q modulated RF input signal 19782 to an I baseband output signal 19784, and a Q baseband output signal 19786. I/Q modulated RF input signal comprises a first information signal and a second information signal that are I/Q modulated onto an RF carrier signal. I baseband output signal 19784 comprises the first baseband information signal. Q baseband output signal 19786 comprises the second baseband information signal.

Antenna 19772 receives I/Q modulated RF input signal 19782. I/Q modulated RF input signal 19782 is output by antenna 19772 and received by optional LNA 19718. When present, LNA 19718 amplifies I/Q modulated RF input signal 19782, and outputs amplified I/Q signal 19788.

First Processing module 19702 receives amplified I/Q signal 19788. First Processing module 19702 down-converts the I-phase signal portion of amplified input I/Q signal 19788 according to an I control signal 19790. First Processing module 19702 outputs an I output signal 19798.

In an embodiment, first Processing module 19702 comprises a first storage module 19724, a first UFT module 19726, and a first voltage reference 19728. In an embodiment, a switch contained within first UFT module 19726 opens and closes as a function of I control signal 19790. As a result of the opening and closing of this switch, which respectively couples and de-couples first storage module 19724 to and from first voltage reference 19728, a down-converted signal, referred to as I output signal 19798, results. First voltage reference 19728 may be any reference voltage, and is ground in some embodiments. I output signal 19798 is stored by first storage module 19724.

In an embodiment, first storage module 19724 comprises a first capacitor 19774. In addition to storing I output signal 19798, first capacitor

19774 reduces or prevents a DC offset voltage resulting from charge injection from appearing on I output signal 19798

I output signal 19798 is received by optional first filter 19704. When present, first filter 19704 is a high pass filter to at least filter I output signal 19798 to remove any carrier signal "bleed through". In an embodiment, when present, first filter 19704 comprises a first resistor 19730, a first filter capacitor 19732, and a first filter voltage reference 19734. Preferably, first resistor 19730 is coupled between I output signal 19798 and a filtered I output signal 19707, and first filter capacitor 19732 is coupled between filtered I output signal 19707 and first filter voltage reference 19734. Alternately, first filter 19704 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant arts. First filter 19704 outputs filtered I output signal 19707.

Second Processing module 19706 receives amplified I/Q signal 19788. Second Processing module 19706 down-converts the inverted I-phase signal portion of amplified input I/Q signal 19788 according to an inverted I control signal 19792. Second Processing module 19706 outputs an inverted I output signal 19701.

In an embodiment, second Processing module 19706 comprises a second storage module 19736, a second UFT module 19738, and a second voltage reference 19740. In an embodiment, a switch contained within second UFT module 19738 opens and closes as a function of inverted I control signal 19792. As a result of the opening and closing of this switch, which respectively couples and de-couples second storage module 19736 to and from second voltage reference 19740, a down-converted signal, referred to as inverted I output signal 19701, results. Second voltage reference 19740 may be any reference voltage, and is preferably ground. Inverted I output signal 19701 is stored by second storage module 19736.

In an embodiment, second storage module 19736 comprises a second capacitor 19776. In addition to storing inverted I output signal 19701, second capacitor 19776 reduces or prevents a DC offset voltage resulting from above described charge injection from appearing on inverted I output signal 19701.

Inverted I output signal 19701 is received by optional second filter 19708. When present, second filter 19708 is a high pass filter to at least filter inverted I output signal 19701 to remove any carrier signal "bleed through". In an embodiment, when present, second filter 19708 comprises a second resistor 19742, a second filter capacitor 19744, and a second filter voltage reference 19746. In an embodiment, second resistor 19742 is coupled between inverted I output signal 19701 and a filtered inverted I output signal 19709, and second filter capacitor 19744 is coupled between filtered inverted I output signal 19709 and second filter voltage reference 19746. Alternately, second filter 19708 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant arts. Second filter 19708 outputs filtered inverted I output signal 19709.

First differential amplifier 19720 receives filtered I output signal 19707 at its non-inverting input and receives filtered inverted I output signal 19709 at its inverting input. First differential amplifier 19720 subtracts filtered inverted I output signal 19709 from filtered I output signal 19707, amplifies the result, and outputs I baseband output signal 19784. Other suitable subtractor modules may be substituted for first differential amplifier 19720, and second differential amplifier 19722, as would be understood by persons skilled in the relevant arts from the teachings herein. Because filtered inverted I output signal 19709 is substantially equal to an inverted version of filtered I output signal 19707, I baseband output signal 19784 is substantially equal to filtered I output signal 19709, with its amplitude doubled. Furthermore, filtered I output signal 19707 and filtered inverted I output signal 19709 may comprise substantially equal noise and DC offset contributions of the same polarity from

prior down-conversion circuitry, including first Processing module 19702 and second Processing module 19706, respectively. When first differential amplifier 19720 subtracts filtered inverted I output signal 19709 from filtered I output signal 19707, these noise and DC offset contributions substantially cancel each other.

Third Processing module 19710 receives amplified I/Q signal 19788. Third Processing module 19710 down-converts the Q-phase signal portion of amplified input I/Q signal 19788 according to an Q control signal 19794. Third Processing module 19710 outputs an Q output signal 19703.

In an embodiment, third Processing module 19710 comprises a third storage module 19748, a third UFT module 19750, and a third voltage reference 19752. In an embodiment, a switch contained within third UFT module 19750 opens and closes as a function of Q control signal 19794. As a result of the opening and closing of this switch, which respectively couples and de-couples third storage module 19748 to and from third voltage reference 19752, a down-converted signal, referred to as Q output signal 19703, results. Third voltage reference 19752 may be any reference voltage, and is preferably ground. Q output signal 19703 is stored by third storage module 19748.

In an embodiment, third storage module 19748 comprises a third capacitor 19778. In addition to storing Q output signal 19703, third capacitor 19778 reduces or prevents a DC offset voltage resulting from above described charge injection from appearing on Q output signal 19703.

Q output signal 19703 is received by optional third filter 19716. When present, third filter 19716 is a high pass filter to at least filter Q output signal 19703 to remove any carrier signal "bleed through". In an embodiment, when present, third filter 19712 comprises a third resistor 19754, a third filter capacitor 19758, and a third filter voltage reference 19758. In an embodiment, third resistor 19754 is coupled between Q output signal 19703 and a filtered Q output signal 19711, and third filter capacitor 19756 is coupled between

filtered Q output signal 19711 and third filter voltage reference 19758. Alternately, third filter 19712 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant arts. Third filter 19712 outputs filtered Q output signal 19711.

Fourth Processing module 19714 receives amplified I/Q signal 19788. Fourth Processing module 19714 down-converts the inverted Q-phase signal portion of amplified input I/Q signal 19788 according to an inverted Q control signal 19796. Fourth Processing module 19714 outputs an inverted Q output signal 19705.

In an embodiment, fourth Processing module 19714 comprises a fourth storage module 19760, a fourth UFT module 19762, and a fourth voltage reference 19764. In an embodiment, a switch contained within fourth UFT module 19762 opens and closes as a function of inverted Q control signal 19796. As a result of the opening and closing of this switch, which respectively couples and de-couples fourth storage module 19760 to and from fourth voltage reference 19764, a down-converted signal, referred to as inverted Q output signal 19705, results. Fourth voltage reference 19764 may be any reference voltage, and is preferably ground. Inverted Q output signal 19705 is stored by fourth storage module 19760.

In an embodiment, fourth storage module 19760 comprises a fourth capacitor 19780. In addition to storing inverted Q output signal 19705, fourth capacitor 19780 reduces or prevents a DC offset voltage resulting from above described charge injection from appearing on inverted Q output signal 19705.

Inverted Q output signal 19705 is received by optional fourth filter 19716. When present, fourth filter 19716 is a high pass filter to at least filter inverted Q output signal 19705 to remove any carrier signal "bleed through". In an embodiment, when present, fourth filter 19716 comprises a fourth resistor 19766, a fourth filter capacitor 19768, and a fourth filter voltage reference 19770. In an embodimnet, fourth resistor 19766 is coupled between

inverted Q output signal 19705 and a filtered inverted Q output signal 19713, and fourth filter capacitor 19768 is coupled between filtered inverted Q output signal 19713 and fourth filter voltage reference 19770. Alternately, fourth filter 19716 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant arts. Fourth filter 19716 outputs filtered inverted Q output signal 19713.

Second differential amplifier 19722 receives filtered Q output signal 19711 at its non-inverting input and receives filtered inverted Q output signal 19713 at its inverting input. Second differential amplifier 19722 subtracts filtered inverted Q output signal 19713 from filtered Q output signal 19711, amplifies the result, and outputs Q baseband output signal 19786. Because filtered inverted Q output signal 19713 is substantially equal to an inverted version of filtered Q output signal 19711, Q baseband output signal 19786 is substantially equal to filtered Q output signal 19713, with its amplitude doubled. Furthermore, filtered Q output signal 19711 and filtered inverted Q output signal 19713 may comprise substantially equal noise and DC offset contributions of the same polarity from prior down-conversion circuitry, including third Processing module 19710 and fourth Processing module 19714, respectively. When second differential amplifier 19722 subtracts filtered inverted Q output signal 19713 from filtered Q output signal 19711, these noise and DC offset contributions substantially cancel each other.

2. *Example I/Q Modulation Control Signal Generator Embodiments*

FIG. 198 illustrates an exemplary block diagram for an example I/Q modulation control signal generator 19800, according to an embodiment of the present invention. I/Q modulation control signal generator 19800 generates I control signal 19790, inverted I control signal 19792, Q control signal 19794, and inverted Q control signal 19796 used by I/Q modulation receiver 19700 of

FIG. 197. I control signal 19790 and inverted I control signal 19792 operate to down-convert the I-phase portion of an input I/Q modulated RF signal. Q control signal 19794 and inverted Q control signal 19796 act to down-convert the Q-phase portion of the input I/Q modulated RF signal. Furthermore, I/Q modulation control signal generator 19800 has the advantage of generating control signals in a manner such that resulting collective circuit re-radiation is radiated at one or more frequencies outside of the frequency range of interest. For instance, potential circuit re-radiation is radiated at a frequency substantially greater than that of the input RF carrier signal frequency.

I/Q modulation control signal generator 19800 comprises a local oscillator 19802, a first divide-by-two module 19804, a 180 degree phase shifter 19806, a second divide-by-two module 19808, a first pulse generator 19810, a second pulse generator 19812, a third pulse generator 19814, and a fourth pulse generator 19816.

Local oscillator 19802 outputs an oscillating signal 19818. FIG. 199 shows an exemplary oscillating signal 19818.

First divide-by-two module 19804 receives oscillating signal 19818, divides oscillating signal 19818 by two, and outputs a half frequency LO signal 19820 and a half frequency inverted LO signal 19826. FIG. 199 shows an exemplary half frequency LO signal 19820. Half frequency inverted LO signal 19826 is an inverted version of half frequency LO signal 19820. First divide-by-two module 19804 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant arts.

180 degree phase shifter 19806 receives oscillating signal 19818, shifts the phase of oscillating signal 19818 by 180 degrees, and outputs phase shifted LO signal 19822. 180 degree phase shifter 19806 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be

known by persons skilled in the relevant arts. In alternative embodiments, other amounts of phase shift may be used.

Second divide-by two module 19808 receives phase shifted LO signal 19822, divides phase shifted LO signal 19822 by two, and outputs a half frequency phase shifted LO signal 19824 and a half frequency inverted phase shifted LO signal 19828. FIG. 199 shows an exemplary half frequency phase shifted LO signal 19824. Half frequency inverted phase shifted LO signal 19828 is an inverted version of half frequency phase shifted LO signal 19824. Second divide-by-two module 19808 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant arts.

First pulse generator 19810 receives half frequency LO signal 19820, generates an output pulse whenever a rising edge is received on half frequency LO signal 19820, and outputs I control signal 19790. FIG. 199 shows an exemplary I control signal 19790.

Second pulse generator 19812 receives half frequency inverted LO signal 19826, generates an output pulse whenever a rising edge is received on half frequency inverted LO signal 19826, and outputs inverted I control signal 19792. FIG. 199 shows an exemplary inverted I control signal 19792.

Third pulse generator 19814 receives half frequency phase shifted LO signal 19824, generates an output pulse whenever a rising edge is received on half frequency phase shifted LO signal 19824, and outputs Q control signal 19794. FIG. 199 shows an exemplary Q control signal 19794.

Fourth pulse generator 19816 receives half frequency inverted phase shifted LO signal 19828, generates an output pulse whenever a rising edge is received on half frequency inverted phase shifted LO signal 19828, and outputs inverted Q control signal 19796. FIG. 199 shows an exemplary inverted Q control signal 19796.

In an embodiment, control signals 19790, 19792, 19794 and 19796 output pulses having a width equal to one-half of a period of I/Q modulated RF input signal 19782. The invention, however, is not limited to these pulse widths, and control signals 19790, 19792, 19794, and 19796 may comprise pulse widths of any fraction of, or multiple and fraction of, a period of I/Q modulated RF input signal 19782. Also, other circuits for generating control signals 19790, 19792, 19794, and 19796 will be apparent to persons skilled in the relevant arts based on the herein teachings.

First, second, third, and fourth pulse generators 19810, 19812, 19814, and 19816 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant arts.

As shown in FIG. 199, in embodiments control signals 19790, 19792, 19794, and 19796 comprise pulses that are non-overlapping. Furthermore, in this example, pulses appear on these signals in the following order: I control signal 19790, Q control signal 19794, inverted I control signal 19792, and inverted Q control signal 19796. Potential circuit re-radiation from I/Q modulation receiver 19700 may comprise frequency components from a combination of these control signals.

For example, FIG. 200 shows an overlay of pulses from I control signal 19790, Q control signal 19794, inverted I control signal 19792, and inverted Q control signal 19796. When pulses from these control signals leak through first, second, third, and fourth Processing modules 19702, 19706, 19710, and 19714 to antenna 19782 (shown in FIG. 197), they may be radiated from I/Q modulation receiver 19700, with a combined waveform that appears to have a primary frequency equal to four times the frequency of any single one of control signals 19790, 19792, 19794, and 19796. FIG. 199 shows an example combined control signal 19902.

FIG. 200 also shows an example I/Q modulation RF input signal 19782 overlaid upon control signals 19790, 19792, 19794, and 19796. As shown in FIG. 200, pulses on I control signal 19790 overlay and act to down-convert a positive I-phase portion of I/Q modulation RF input signal 19782. Pulses on inverted I control signal 19792 overlay and act to down-convert a negative I-phase portion of I/Q modulation RF input signal 19782. Pulses on Q control signal 19794 overlay and act to down-convert a rising Q-phase portion of I/Q modulation RF input signal 19782. Pulses on inverted Q control signal 19796 overlay and act to down-convert a falling Q-phase portion of I/Q modulation RF input signal 19782.

As FIG. 200 further shows in this example, the frequency ratio between the combination of control signals 19790, 19792, 19794, and 19796 and I/Q modulation RF input signal 19782 is 4:3. Because the frequency of the potentially re-radiated signal, combined control signal 19902, is substantially different from that of the signal being down-converted, I/Q modulation RF input signal 19782, it does not interfere with signal down-conversion as it is out of the frequency band of interest, and hence may be filtered out. In this manner, I/Q modulation receiver 19700 reduces problems due to circuit re-radiation. As will be understood by persons skilled in the relevant arts from the teachings herein, frequency ratios other than 4:3 may be implemented to achieve similar reduction of problems of circuit re-radiation.

It should be understood that the above control signal generator circuit example is provided for illustrative purposes only. The invention is not limited to these embodiments. Alternative embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) for I/Q modulation control signal generator 19800 will be apparent to persons skilled in the relevant arts from the teachings herein, and are within the scope of the present invention.

3. Detailed Example I/Q Modulation Receiver Embodiment with Exemplary Waveforms

FIG. 201 illustrates a more detailed example circuit implementation of I/Q modulation receiver 19700, according to an embodiment of the present invention. FIGS. 202-40 show waveforms related to an example implementation of I/Q modulation receiver 19700 of FIG. 201.

FIGS. 202 and 203 show first and second input data signals 20102 and 20104 to be I/Q modulated with a RF carrier signal frequency as the I-phase and Q-phase information signals, respectively.

FIGS. 205 and 206 show the signals of FIG. 202 and 203 after modulation with a RF carrier signal frequency, respectively, as I-modulated signal 20106 and Q-modulated signal 20108.

FIG. 204 shows an I/Q modulation RF input signal 19782 formed from I-modulated signal 20106 and Q-modulated signal 20108 of FIGS. 205 and 206, respectively.

FIG. 211 shows an overlaid view of filtered I output signal 21102 and filtered inverted I output signal 21104.

FIG. 212 shows an overlaid view of filtered Q output signal 21202 and filtered inverted Q output signal 21204.

FIGS. 207 and 208 show I baseband output signal 19784 and Q baseband output signal 19786, respectfully. A data transition 20402 is indicated in both I baseband output signal 19784 and Q baseband output signal 19786. The corresponding data transition 20402 is indicated in I-modulated signal 20106 of FIG. 205, Q-modulated signal 20108 of FIG. 206, and I/Q modulation RF input signal 19782 of FIG. 204.

FIGS. 209 and 210 show I baseband output signal 19784 and Q baseband output signal 19786 over a wider time interval.

4. Example Single Channel Receiver Embodiment

FIG. 213 illustrates an example single channel receiver 21300, corresponding to either the I or Q channel of I/Q modulation receiver 19700, according to an embodiment of the present invention. Single channel receiver 21300 can down-convert an input RF signal 21306 modulated according to AM, PM, FM, and other modulation schemes. Refer to the section above for further description on the operation of single channel receiver 21300.

5. *Example Automatic Gain Control (AGC) Embodiment*

According to embodiments of the invention, the amplitude level of the down-converted signal can be controlled by modifying the aperture of the control signal that controls the switch module. Consider FIG. 43, that illustrates an equation that represents the change in charge in the storage device of embodiments of the UFT module, such as a capacitor. This equation is a function of T, which is the aperture of the control signal. Thus, by modifying the aperture T of the control signal, it is possible to modify the amplitude level of the down-converted signal.

Some embodiments may include a control mechanism to enable manual control of aperture T, and thus manual control of the amplitude level of the down-converted signal. Other embodiments may include automatic or semi-automatic control modules to enable automatic or semi-automatic control of aperture T, and thus automatic or semi-automatic control of the amplitude level of the down-converted signal. Such embodiments are herein referred to (without limitation) as automatic gain control (AGC) embodiments. Other embodiments include a combination of manual and automatic control of aperture T.

6. Other Example Embodiments

Additional aspects/embodiments of the invention are considered in this section.

In one embodiment of the present invention there is provided a method of transmitting information between a transmitter and a receiver comprising the steps of transmitting a first series of signals each having a known period from the transmitter at a known first repetition rate; sampling by the receiver each signal in the first series of signals a single time and for a known time interval the sampling of the first series of signals being at a second repetition rate that is a rate different from the first repetition rate by a known amount; and generating by the receiver an output signal indicative of the signal levels sampled in step B and having a period longer than the known period of a transmitted signal.

In another embodiment of the invention there is provided a communication system comprising a transmitter means for transmitting a first series of signals of known period at a known first repetition rate, a receiver means for receiving the first series of signals, the receiver means including sampling means for sampling the signal level of each signal first series of signals for a known time interval at a known second repetition rate, the second repetition rate being different from the first repetition rate by a known amount as established by the receiver means. The receiver means includes first circuit means for generating a first receiver output signal indicative of the signal levels sampled and having a period longer than one signal of the first series of signals. The transmitter means includes an oscillator for generating an oscillator output signal at the first repetition rate, switch means for receiving the oscillator output signal and for selectively passing the oscillator output signal, waveform generating means for receiving the oscillator output signal

for generating a waveform generator output signal having a time domain and frequency domain established by the waveform generating means.

The embodiment of the invention described herein involves a single or multi-user communications system that utilizes coherent signals to enhance the system performance over conventional radio frequency schemes while reducing cost and complexity. The design allows direct conversion of radio frequencies into baseband components for processing and provides a high level of rejection for signals that are not related to a known or controlled slew rate between the transmitter and receiver timing oscillators. The system can be designed to take advantage of broadband techniques that further increase its reliability and permit a high user density within a given area. The technique employed allows the system to be configured as a separate transmitter-receiver pair or a transceiver.

An objective of the present system is to provide a new communication technique that can be applied to both narrow and wide band systems. In its most robust form, all of the advantages of wide band communications are an inherent part of the system and the invention does not require complicated and costly circuitry as found in conventional wide band designs. The communications system utilizes coherent signals to send and receive information and consists of a transmitter and a receiver in its simplest form. The receiver contains circuitry to turn its radio frequency input on and off in a known relationship in time to the transmitted signal. This is accomplished by allowing the transmitter timing oscillator and the receiver timing oscillator to operate at different but known frequencies to create a known slew rate between the oscillators. If the slew rate is small compared to the timing oscillator frequencies, the transmitted waveform will appear stable in time, i.e., coherent (moving at the known slew rate) to the receiver's switched input. The transmitted waveform is the only waveform that will appear stable in time to the receiver and thus the receiver's input can be averaged to achieve the

desired level filtering of unwanted signals. This methodology makes the system extremely selective without complicated filters and complex encoding and decoding schemes and allows the direct conversion of radio frequency energy from an antenna or cable to baseband frequencies with a minimum number of standard components further reducing cost and complexity. The transmitted waveform can be a constant carrier (narrowband), a controlled pulse (wideband and ultra-wideband) or a combination of both such as a dampened sinusoidal wave and or any arbitrary periodic waveform thus the system can be designed to meet virtually any bandwidth requirement. Simple standard modulation and demodulation techniques such as AM and Pulse Width Modulation can be easily applied to the system.

Depending on the system requirements such as the rate of information transfer, the process gain, and the intended use, there are multiple preferred embodiments of the invention. The embodiment discussed herein will be the amplitude and pulse width modulated system. It is one of the simplest implementations of the technology and has many common components with the subsequent systems. A amplitude modulated transmitter consists of a Transmitter Timing Oscillator, a Multiplier, a Waveform Generator, and an Optional Amplifier. The Transmitter Timing Oscillator frequency can be determined by a number of resonate circuits including an inductor and capacitor, a ceramic resonator, a SAW resonator, or a crystal. The output waveform is sinusoidal, although a squarewave oscillator would produce identical system performance.

The Multiplier component multiplies the Transmitter Timing Oscillator output signal by 0 or 1 or other constants, K1 and K2, to switch the oscillator output on and off to the Waveform Generator. In this embodiment, the information input can be digital data or analog data in the form of pulse width modulation. The Multiplier allows the Transmitter Timing Oscillator output to be present at the Waveform Generator input when the information input is

above a predetermined value. In this state the transmitter will produce an output waveform. When the information input is below a predetermined value, there is no input to the Waveform Generator and thus there will be no transmitter output waveform. The output of the Waveform Generator determines the system's bandwidth in the frequency domain and consequently the number of users, process gain immunity to interference and overall reliability), the level of emissions on any given frequency, and the antenna or cable requirements. The Waveform Generator in this example creates a one cycle pulse output which produces an ultra-wideband signal in the frequency domain. An optional power Amplifier stage boosts the output of the Waveform Generator to a desired power level.

With reference now to the drawings, the amplitude and pulse width modulated transmitter in accord with the present invention is depicted at numeral 13000 in FIGS. 130 and 131. The Transmitter Timing Oscillator 13002 is a crystal-controlled oscillator operating at a frequency of 25 MHZ. Multiplier 13004 includes a two-input NAND gate 13102 controlling the gating of oscillator 13002 output to Waveform Generator 13006. Waveform Generator 13006 produces a pulse output as depicted at 13208 in FIGS. 132 and 133, which produces a frequency spectrum 13402 in FIG. 134. Amplifier 13008 is optional. The transmitter 13000 output is applied to antenna or cable 13010, which as understood in the art, may be of various designs as appropriate in the circumstances.

FIGS. 132-134 illustrate the various signals present in transmitter 13000. The output of transmitter 13000 at "A" may be either a sinusoidal or squarewave signal 13202 that is provided as one input into NAND gate 13102. Gate 13102 also receives an information signal 13204 at "B" which, in the embodiment shown, is digital in form. The output 13206 of Multiplier 13004 can be either sinusoidal or squarewave depending upon the original signal 13202. Waveform Generator 13006 provides an output of a single cycle

impulse signal 13208. The single cycle impulse 13210 varies in voltage around a static level 13212 and is created at 40 nanoseconds intervals. In the illustrated embodiment, the frequency of transmitter 13002 is 25 MHZ and accordingly, one cycle pulses of 1.0 GHZ are transmitted every 40 nanoseconds during the total time interval that gate 13102 is "on" and passes the output of transmitter oscillator 13002.

FIG. 135 shows the preferred embodiment receiver block diagram to recover the amplitude or pulse width modulated information and consists of a Receiver Timing Oscillator 13510, Waveform Generator 13508, RF Switch Fixed or Variable Integrator 13506, Decode Circuit 13514, two optional Amplifier/Filter stages 13504 and 13512, antenna or cable input 13502, and Information Output 13516. The Receiver Timing Oscillator 13510 frequency can be determined by a number of resonate circuits including an inductor and capacitor, a ceramic resonator, a SAW resonator, or a crystal. As in the case of the transmitter, the oscillator 13510 shown here is a crystal oscillator. The output waveform is a squarewave, although a sinewave oscillator would produce identical system performance. The squarewave timing oscillator output 13602 is shown as A in FIG. 136. The Receiver Timing Oscillator 13510 is designed to operate within a range of frequencies that creates a known range of slew rates relative to the Transmitter Timing Oscillator 13002. In this embodiment, the Transmitter Timing Oscillator 13002 frequency is 25 MHZ and the Receiver Timing Oscillator 13510 outputs between 25.0003 MHZ and 25.0012 MHZ which creates a +300 to +1200 Hz slew rate.

The Receiver Timing Oscillator 13510 is connected to the Waveform Generator 13508 which shapes the oscillator signal into the appropriate output to control the amount of the time that the RF switch 13506 is on and off. The on-time of the RF switch 13506 should be less than ½ of a cycle (1/10 of a cycle is preferred) or in the case of a single pulse, no wider than the pulse width of the transmitted waveform or the signal gain of the system will be

reduced. Examples are illustrated in Table A1. Therefore the output of the Waveform Generator 13508 is a pulse of the appropriate width that occurs once per cycle of the receiver timing oscillator 13510. The output 13604 of the Waveform Generator is shown as B in FIG. 136.

Transmitted Waveform	Gain Limit on-time	Preferred on-time
Single 1 nanosecond pulse	1 nanosecond	100 picoseconds
1 Gigahertz 1,2,3..etc. cycle output	500 picoseconds	50 picoseconds
10 Gigahertz 1,2,3..etc. cycle output	50 picoseconds	5 picoseconds

Table A1

The RF Switch/Integrator 13506 samples the RF signal 13606 shown as "C" in FIG. 136 when the Waveform Generator output 13604 is below a predetermined value. When the Waveform Generator output 13604 is above a predetermined value, the RF Switch 13506 becomes a high impedance node and allows the Integrator to hold the last RF signal sample 13606 until the next cycle of the Waveform Generator 13508 output. The Integrator section of 13506 is designed to charge the Integrator quickly (fast attack) and discharge the Integrator at a controlled rate (slow decay). This embodiment provides unwanted signal rejection and is a factor in determining the baseband frequency response of the system. The sense of the switch control is arbitrary depending on the actual hardware implementation.

In an embodiment of the present invention, the gating or sampling rate of the receiver 13500 is 300 Hz higher than the 25 MHZ transmission rate from the transmitter 13000. Alternatively, the sampling rate could be less than the transmission rate. The difference in repetition rates between the transmitter 13000 and receiver 13500, the "slew rate," is 300 Hz and results in a controlled drift of the sampling pulses over the transmitted pulse which thus appears "stable" in time to the receiver 13500. With reference now to FIGS.

132 and 136, an example is illustrated for a simple case of an output signal 13608 (FIG. 136, "D") that is constructed of four samples from four RF input pulses 13606 for ease of explanation. As can be clearly seen, by sampling the RF pulses 13606 passed when the transmitter information signal 13204 (FIG. 132) is above a predetermine threshold the signal 13608 is a replica of a signal 13606 but mapped into a different time base. In the case of this example, the new time base has a period four times longer than real time signal. The use of an optional amplifier/filter 13512 results in a further refinement of the signal 13608 which is present at "E" as signal 13610.

Decode Circuitry 13514 extracts the information contained in the transmitted signal and includes a Rectifier that rectifies signal 13608 or 13610 to provide signal 13612 at "G" in FIG. 136. The Variable Threshold Generator circuitry in circuit 13514 provides a DC threshold signal level 13614 for signal 13610 that is used to determine a high (transmitter output on) or low (transmitter output off) and is shown at "H." The final output signal 13616 at "F" is created by an output voltage comparator in circuit 13514 that combines signals 13612 and 13614 such that when the signal 13612 is a higher voltage than signal 13614, the information output signal goes high. Accordingly, signal 13616 represents, for example, a digital "1" that is now time-based to a 1:4 expansion of the period of an original signal 13606. While this illustration provides a 4:1 reduction in frequency, it is sometimes desired to provide a reduction of more than 50,000:1; in the preferred embodiment, 100,000:1 or greater is achieved. This results in a shift directly from RF input frequency to low frequency baseband without the requirement of expensive intermediate circuitry that would have to be used if only a 4:1 conversion was used as a first stage. Table A2 provides information as to the time base conversion and includes examples.

Units

s = 1 ps = 1_10^{12} ns = 1_10^{-9} us = 1_10^{-6} MHz = 1_10^{6} KHz = 1_10^{3}

Receiver Timing Oscillator Frequency = 25.0003 MHz

Transmitter Timing Oscillator Frequency = 25 MHz

$$\text{period} = \frac{1}{\text{Transmitter Timing Oscillator Frequency}}$$

period = 40 ns

$$\text{slew rate} = \frac{1}{\text{Receiver Timing Oscillator Frequency} - \text{Transmitter Timing Oscillator Frequency}}$$

slew rate =0.003 s

$$\text{time base multiplier} = \frac{\text{slew rate}}{\text{period}} \text{ seconds per nanosecond}$$

time base multiplier = 8.333_10^4

Example 1:

1 nanosecond translates into 83.33 microseconds

time base = (1 ns)_ time base multiplier

time base = 83.333 us

Example 2:

2 Gigahertz translates into 24 Kilohertz 2 Gigahertz = 500 picosecond period

time base = (500 ps)_ time base multiplier

time base = 41.667 us

$$\text{frequency} = \frac{1}{\text{time base}}$$

frequency = 24 KHz

Table A2

In the illustrated embodiment, the signal 13616 at "F" has a period of 83.33 usec, a frequency of 12 KHz and it is produced once every 3.3 msec for a 300 Hz slew rate. Stated another way, the system is converting a 1 gigahertz transmitted signal into an 83.33 microsecond signal.

Accordingly, the series of RF pulses 13210 that are transmitted during the presence of an "on" signal at the information input gate 13102 are used to reconstruct the information input signal 13204 by sampling the series of pulses at the receiver 13500. The system is designed to provide an adequate number of RF inputs 13606 to allow for signal reconstruction.

An optional Amplifier/Filter stage or stages 13504 and 13512 may be included to provide additional receiver sensitivity, bandwidth control or signal conditioning for the Decode Circuitry 13514. Choosing an appropriate time base multiplier will result in a signal at the output of the Integrator 13506 that can be amplified and filtered with operational amplifiers rather than RF amplifiers with a resultant simplification of the design process. The signal 13610 at "E" illustrates the use of Amplifier/Filter 13512 (FIG. 137). The optional RF amplifier 13504 shown as the first stage of the receiver should be included in the design when increased sensitivity and/or additional filtering is required. Example receiver schematics are shown in FIGS. 137-139.

FIGS. 140-143 illustrate different pulse output signals 14002 and 14202 and their respective frequency domain at 14102 and 14302. As can be seen from FIGS. 140 and 141, the half-cycle signal 14002 generates a spectrum less subject to interference than the single cycle of FIG. 133 and the 10-cycle pulse of FIG. 142. The various outputs determine the system's immunity to interference, the number of users in a given area, and the cable

and antenna requirements. FIGS. 133 and 134 illustrate example pulse outputs.

FIGS. 144 and 145 show example differential receiver designs. The theory of operation is similar to the non-differential receiver of FIG. 135 except that the differential technique provides an increased signal to noise ratio by means of common mode rejection. Any signal impressed in phase at both inputs on the differential receiver will attenuated by the differential amplifier shown in FIGS. 144 and 145 and conversely any signal that produces a phase difference between the receiver inputs will be amplified.

FIGS. 146 and 147 illustrate the time and frequency domains of a narrow band/constant carrier signal in contrast to the ultra-wide band signals used in the illustrated embodiment.

VI. Additional Features of the Invention

1. Architectural Features of the Invention

The present invention provides, among other things, the following architectural features:

optimal baseband signal to noise ratio regardless of modulation (programmable RF matched filter);

exceptional linearity per milliwatt consumed;

easily integrated into bulk C-MOS (small size/low cost, high level of integration);

fundamental or sub-harmonic operation (does not change conversion efficiency);

transmit function provides frequency multiplication and signal gain; and

optimal power transfer into a scalable output impedance (independent of device voltage or current);

The present invention provides simultaneous solutions for two domains: power sampling and matched filtering. A conventional sampler is a voltage sampling device, and does not substantially affect the input signal. A power sampler according to the present invention attempts to take as much power from the input to construct the output, and does not necessarily preserve the input signal.

2. Additional Benefits of the Invention

2.1 Compared to an Impulse Sampler

The present invention out-performs a theoretically perfect impulse sampler. The performance of a practical implementation of the present invention exceeds the performance of a practical implementation of an impulse sampler. The present invention is easily implemented (does not require impulse circuitry).

2.2 Linearity

The present invention provides exceptional linearity per milliwatt. For example, rail to rail dynamic range is possible with minimal increase in power.

In an example integrated circuit embodiment, the present invention provides +55dmb IP2, +15 dbm IP3, @ 3.3V, 4.4ma, -15dmb LO. GSM system requirements are +22dbm IP2, -10.5dmb IP3. CDMA system requirements are +50dmb IP2, +10dbm IP3.

2.3 Optimal Power Transfer into a Scalable Output Impedance

In an embodiment of the present invention, output impedance is scalable to facilitate a low system noise figure. In an embodiment, changes in output impedance do not affect power consumption.

2.4 System Integration

In an embodiment, the present invention enables a high level of integration in bulk C-MOS. Other features include:

small footprint;

no multiplier circuits (no device matching or balancing transistors);

transmit and receive filters at baseband;

low frequency synthesizers;

DC offset solutions;

Referring to FIG. 218A, a single-switch, differential input, differential output receiver 21800, according to an embodiment of the present invention, is shown. If an I/Q signal is being received, receiver 21800 could be implemented for each of the I- and Q-phase signals. No balanced transistor is required in receiver 21800. Any charge injection that creates a DC offset voltage on a first switch input 21802 creates a substantially equal DC offset voltage on a second switch input 21804, so that any resulting DC offset due to charge injection is substantially canceled.

In an embodiment, LO signal 21806 runs at a sub-harmonic. Gilbert cells lose efficiency when run at a sub-harmonic, as compared to the receiver of the present invention.

FIG. 218A shows a substantially maximal linearity configuration. The drain and source voltages are virtually fixed in relation to V_{gs}. The DC voltage across first switch input 21802 and second switch input 21804 remains substantially constant.

Single-switch, differential input, differential output receiver embodiments according to the present invention, are discussed in further detail elsewhere herein.

architecturally reduces re-radiation;

Referring to FIG. 218A, re-radiation is substantially all common mode. With a perfect splitter, the re-radiation will be substantially eliminated.

Referring to FIG. 218B, a first switch 21810 and a second switch 21812 are implemented in a receiver 21814, according to an embodiment of the present invention. Receiver 21814 moves re-radiation off frequency to the next even harmonic frequency higher. Referring to FIG. 218D, re-radiation was substantially shifted from 2.49 GHz (see re-radiation spike 21818) to 3.29 GHz (see larger re-radiation spike 21820).

Receiver embodiments, according to the present invention, for reducing or eliminating circuit re-radiation, such as receiver 21814, are discussed in further detail elsewhere herein.

inherent noise rejection; and
lower cost.

2.5 Fundamental or Sub-Harmonic Operation

Sub-harmonic operation is preferred for many direct down-conversion implementations because it tends to avoid oscillators and/or signals near the desired operating frequency.

Conversion efficiency is generally constant regardless of the sub-harmonic. Sub-harmonic operation enables micro power receiver designs.

2.6 Frequency Multiplication and Signal Gain

A transmit function in accordance with the present invention provides frequency multiplication and signal gain. For example, a 900 MHz design example (0.35 μ CMOS) embodiment features -15 dbm 180 MHz LO, 0 dbm 900 MHz I/O output, 5 VDC, 5 ma. A 2400 MHz design example (0.35 μ CMOS) embodiment features -15 dbm 800 MHz LO, -6 dbm 2.4 GHz I/O output, 5 VDC, 16 ma.

A transmit function in accordance with the present invention also provides direct up-conversion (true zero IF).

3. Controlled Aperture Sub-Harmonic Matched Filter Features

3.1 Non-Negligible Aperture

A non-negligible aperture, as taught herein, substantially preserves amplitude and phase information, but not necessarily the carrier signal. A general concept is to under-sample the carrier while over sampling the information.

The present invention transfers optimum energy. Example embodiments have been presented herein, including DC examples and carrier half cycle examples.

3.2 Bandwidth

With regard to input bandwidth, optimum energy transfer generally occurs every n + ½ cycle. Output bandwidth is generally a function of the LO.

3.3 Architectural Advantages of a Universal Frequency Down-Converter

A universal frequency down-converter (UDF), in accordance with the invention, can be designed to provides, among other things, the following features:

filter Q's of 100,000+;
filters with gain;
filter integration in CMOS;
electrically modified center frequency and bandwidth;
stable filter parameters in the presence of high level signals; and
UDF's can be mass produced without tuning.

3.4 Complimentary FET Switch Advantages

Complimentary FET switch implementations of the invention provide, among other things, increased dynamic range (lower Rds_{on} - increased conversion efficiency, higher IIP2, IIP3, minimal current increase (+ CMOS inverter), and lower re-radiation (charge cancellation). For example, refer to FIGS. 240 and 241.

3.5 Differential Configuration Characteristics

Differential configuration implementations of the invention provide, among other things, DC off-set advantages, lower re-radiation, input and output common mode rejection, and minimal current increase. For example, refer to FIG. 242.

3.6 Clock Spreading Characteristics

Clock spreading aspects of the invention provide, among other things, lower re-radiation, DC off-set advantages, and flicker noise advantages. For example, refer to FIGS. 243-245.

3.7 Controlled Aperture Sub Harmonic Matched Filter Principles

The invention provides, among other things, optimization of signal to noise ratio subject to maximum energy transfer given a controlled aperture, and maximum energy transfer while preserving information. The invention also provides bandpass wave form auto sampling and pulse energy accumulation

3.8 Effects of Pulse Width Variation

Pulse width can be optimized for a frequency of interest. Generally, pulse width is n plus ½ cycles of a desired input frequency. Generally, in CMOS implementations of the invention, pulse width variation across process variations and temperature of interest is less than +/- 16 percent.

4. Conventional Systems

4.1 Heterodyne Systems

Conventional heterodyne systems, in contrast to the present invention, are relatively complex, require multiple RF synthesizers, require management of various electromagnetic modes (shield, etc.), require significant inter-modulation management, and require a myriad of technologies that do not easily integrate onto integrated circuits.

4.2 Mobile Wireless Devices

High quality mobile wireless devices have not been implemented via zero IF because of the high power requirements for the first conversion in order to obtain necessary dynamic range, the high level of LO required (LO re-radiation), adjacent channel interference rejection filtering, transmitter modulation filtering, transmitter LO leakage, and limitations on RF synthesizer performance and technology.

5. Phase Noise Cancellation

The complex phasor notation of a harmonic signal is known from Euler's equation, shown here as equation 172.

$$S(t) = e^{-j(\omega_c t + \varphi)} \qquad \text{EQ. (172)}$$

Suppose that φ is also some function of time φ(t). φ(t) represents phase noise or some other phase perturbation of the waveform. Furthermore, suppose that φ(t) and -φ(t) can be derived and manipulated. Then if follows that the multiplication of $S_1(t)$ and $S_2(t)$ will yield equation 173.

$$S(t) = S_1(t) \bullet S_2(t) = e^{-j(\omega_c t + \varphi(t))} \bullet e^{-j(\omega_c t - \varphi(t))} = e^{-j2\omega_c t} \qquad \text{EQ. (173)}$$

Thus, the phase noise φ(t) can be canceled. Trigonometric identities verify the same result except for an additional term at DC. This can be implemented with, for example, a four-quadrant version of the invention. FIG. 268 illustrates an implementation for a doubler (2X clock frequency and harmonics thereof). FIG. 269 illustrates another implementation (harmonics with odd order phase noise canceling).

In an embodiment two clocks are utilized for phase noise cancellation of odd and even order harmonics by cascading stages. A four quadrant implementation of the invention can be utilized to eliminate the multiplier illustrated in FIG. 269.

6. Multiplexed UFD

In an embodiment, parallel receivers and transmitters are implemented using single pole, double throw, triple throw, etc., implementations of the invention.

A multiple throw implementation of the invention can also be utilized. In this embodiment, many frequency conversion options at multiple rates can be performed in parallel or serial. This can be implemented for multiple receive functions, multi-band radios, multi-rate filters, etc.

7. Sampling Apertures

Multiple apertures can be utilized to accomplish a variety of effects. For example, FIG. 270 illustrates a bipolar sample aperture and a corresponding sine wave being sampled. The bipolar sample aperture is operated at a sub harmonic of the sine wave being sampled. By calculating the Fourier transform of each component within the Fourier series, it can be shown that the sampling power spectrum goes to zero at the sub harmonics and super harmonics. As a result, the comb spectrum is substantially eliminated except at the conversion frequency.

Similarly, the number of apertures can be extended with associated bipolar weighting to form a variety of impulse responses and to perform filtering at RF.

8. Diversity Reception and Equalizers

The present invention can be utilized to implement maximal ratio post detection combiners, equal gain post detection combiners, and selectors.

FIG. 271 illustrates an example diversity receiver implemented in accordance with the present invention.

FIG. 272 illustrates an example equalizer implemented in accordance with the present invention.

The present invention can serve as a quadrature down converter and as a unit delay function. In an example of such an implementation, the unit delay function is implemented with a decimated clock at baseband.

VII. Conclusions

Example embodiments of the methods, systems, and components of the present invention have been described herein. As noted elsewhere, these example embodiments have been described for illustrative purposes only, and are not limiting. Other embodiments are possible and are covered by the invention. Such other embodiments include but are not limited to hardware, software, and software/hardware implementations of the methods, systems, and components of the invention. Such other embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

VIII. Glossary of Terms

A.M.	Amplitude Modulation
A/D	Analog/Digital
AWGN	Additive White Gaussian
C	Capacitor

CMOS	Complementary Metal Oxide Semiconductor
dB	Decibel
dBm	Decibels with Respect to One Milliwatt
DC	Direct Current
DCT	Discrete Cosine Transform
DST	Discrete Sine Transform
FIR	Finite Impulse Response
GHz	Giga Hertz
I/Q	In Phase/Quadrature Phase
IC	Integrated Circuits, Initial Conditions
IF	Intermediate Frequency
ISM	Industrial, Scientific, Medical Band
L-C	Inductor-Capacitor
LO	Local Oscillator
NF	Noise Frequency
OFDM	Orthogonal Frequency Division Multiplex
R	Resistor
RF	Radio Frequency
rms	Root Mean Square
SNR	Signal to Noise Ratio
WLAN	Wireless Local Area Network
UFT	Universal Frequency Translation

5

What Is Claimed Is:

1. A method for down-converting an electromagnetic signal, comprising the steps of:

(1) performing a finite time integrating operation on a portion of a carrier signal;

(2) accumulating the result of the finite time integrating operation of step (1); and

(3) repeating steps (1) and (2) for additional portions of the carrier signal, whereby the accumulation results form a down-converted signal.

2. The method according to claim 1, wherein step (1) comprises the step of operating on an approximate half cycle of the carrier signal with a filter having an approximately rectangular impulse response and integrating the output of the filter.

3. The method according to claim 1, wherein step (1) comprises the step of controlling a switch to pass an approximate half cycle of the carrier signal through the switch and integrating the output of the switch.

4. The method according to claim 1, where is a transform, u(t)-u(t-TA) is a windowing operator or aperture of duration TA, and Asin (□t + □) is an approximate half cycle of the carrier signal, and wherein step (1) comprises the step of processing the approximate half cycle of the carrier signal in accordance with:

.

5. The method according to claim 1, wherein step (2) comprises the step of transferring a portion of the energy contained in an approximate half cycle of the carrier signal to an energy storage device.

6. The method according to claim 1, wherein step (2) comprises the step of transferring a portion of the energy contained in an approximate half cycle of the carrier signal to a capacitive storage device.

7. The method according to claim 1, where E is energy, A is a constant, A•Si(t) is an aperture impulse response of duration TA, and wherein step (2) comprises the step of accumulating energy from an approximate half cycle of the carrier signal in accordance with:

$$D_1 = \int_0^{T_A} \left(u(t) - u(t - T_A)\right) \cdot A \sin(\omega t + \phi) dt$$

8. The method according to claim 1, further comprising the step of:

(4) passing on the accumulation result of step (2) to a reconstruction filter.

9. The method according to claim 1, further comprising the step of:

(4) passing on the accumulation result of step (2) to an interpolation filter.

10. The method according to claim 1, wherein step (3) comprises the step of repeating steps (1) and (2) at a sub-harmonic rate of the carrier signal.

11. The method according to claim 1, wherein step (3) comprises the step of repeating steps (1) and (2) at an off-set of a sub-harmonic rate of the carrier signal.

12. The method according to claim 1, further comprising the step of:

(4) performing steps (1), (2), and (3) for positive approximate half cycles of the carrier signal and for inverted negative approximate half cycles of the carrier signal.

Abstract

Methods, systems, and apparatuses, and combinations and sub-combinations thereof, for down-converting an electromagnetic (EM) signal are described herein. Briefly stated, in embodiments the invention operates by receiving an EM signal and recursively operating on approximate half cycles (½, 1½, 2½, etc.) of the carrier signal. The recursive operations can be performed at a sub-harmonic rate of the carrier signal. The invention accumulates the results of the recursive operations and uses the accumulated results to form a down-converted signal. In an embodiment, the EM signal is down-converted to an intermediate frequency (IF) signal. In another embodiment, the EM signal is down-converted to a baseband information signal. In another embodiment, the EM signal is a frequency modulated (FM) signal, which is down-converted to a non-FM signal, such as a phase modulated (PM) signal or an amplitude modulated (AM) signal.

FIG. 1

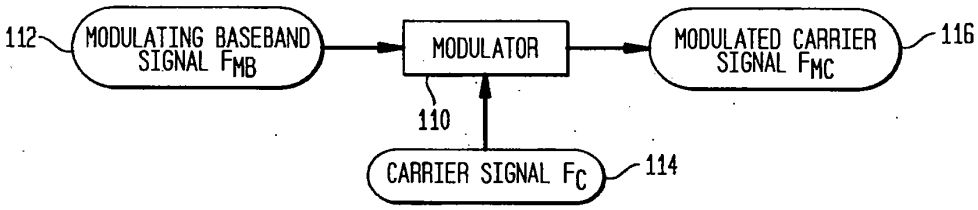


FIG. 2

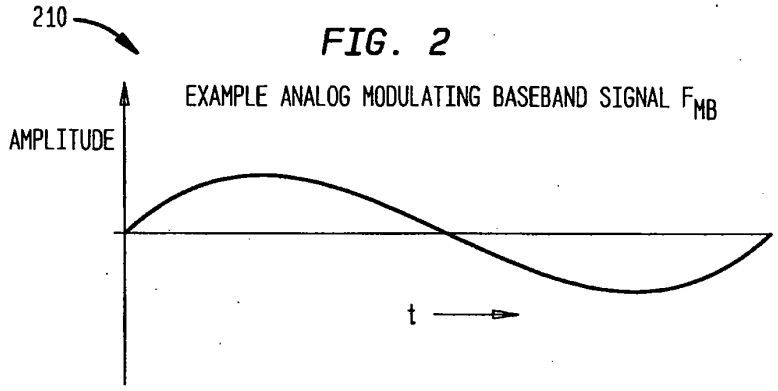


FIG. 3

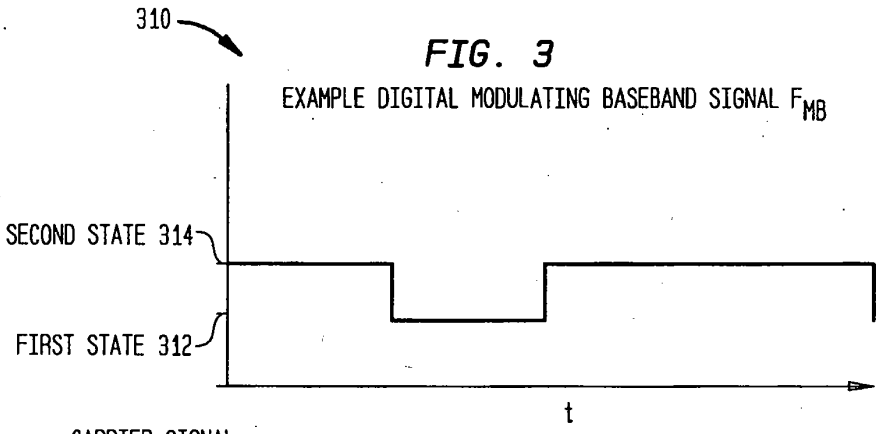
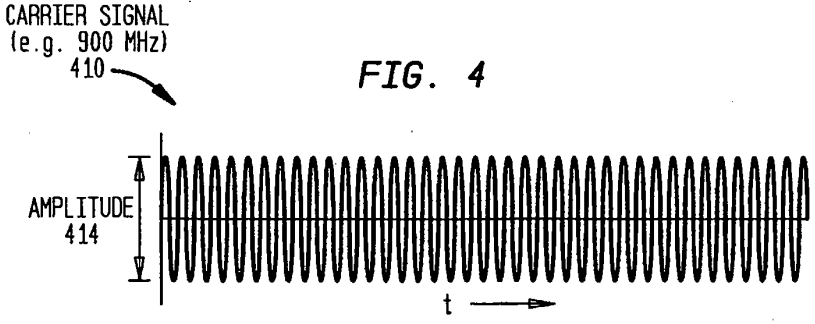


FIG. 4



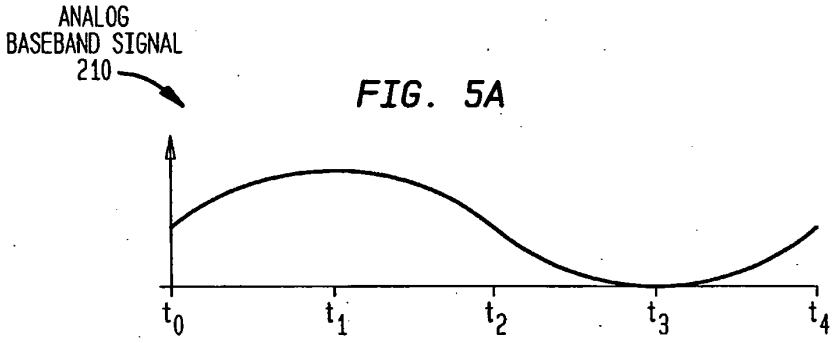


FIG. 5A

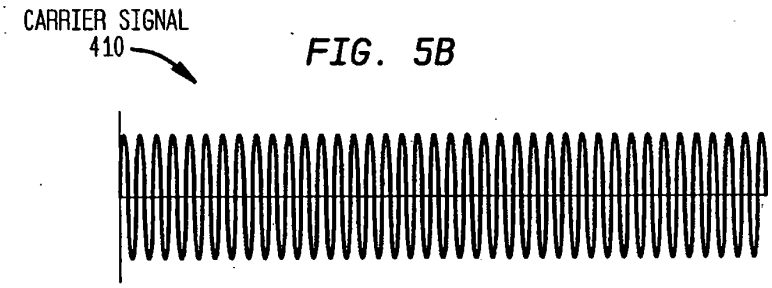


FIG. 5B

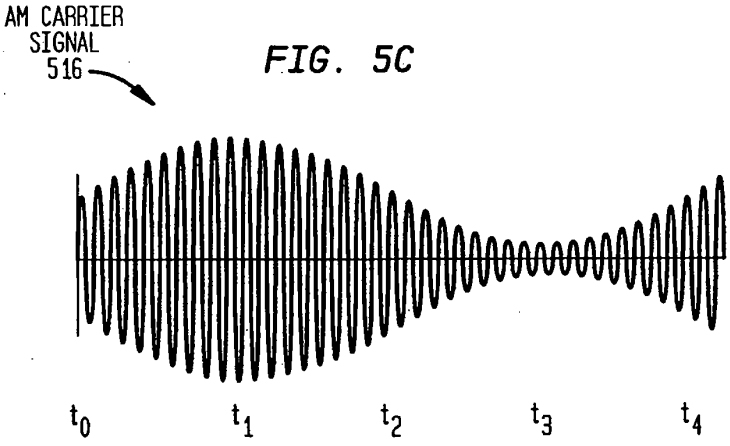


FIG. 5C

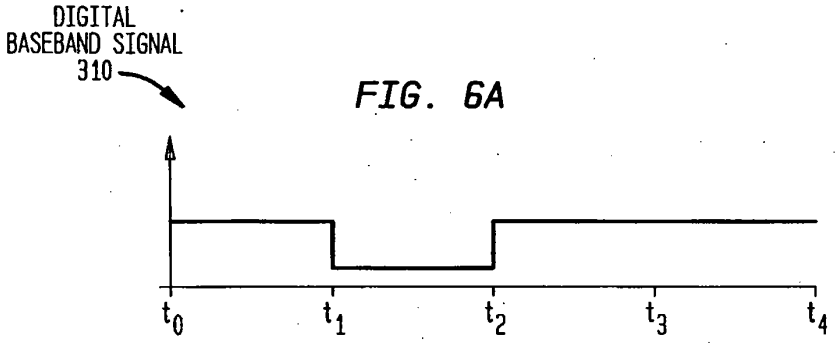


FIG. 6A

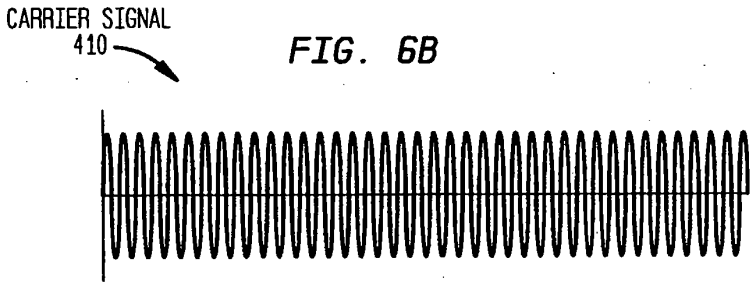


FIG. 6B

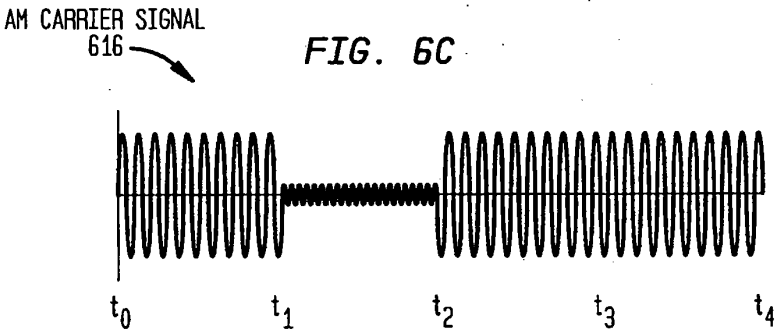


FIG. 6C

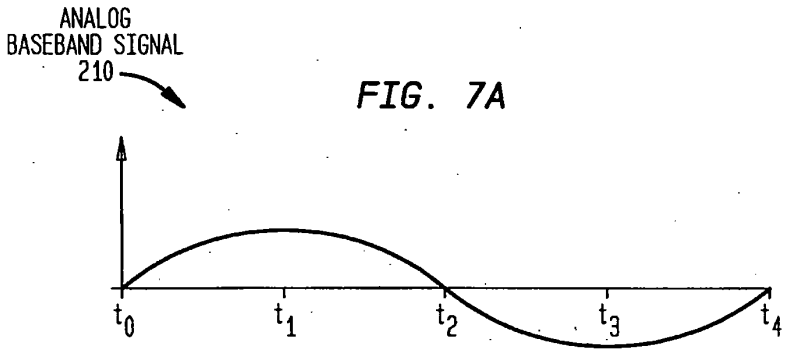


FIG. 7A

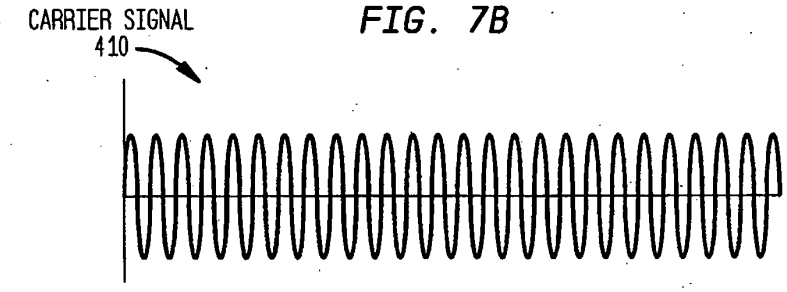


FIG. 7B

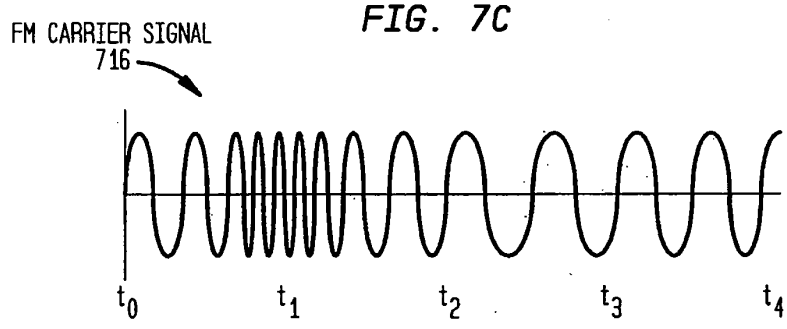


FIG. 7C

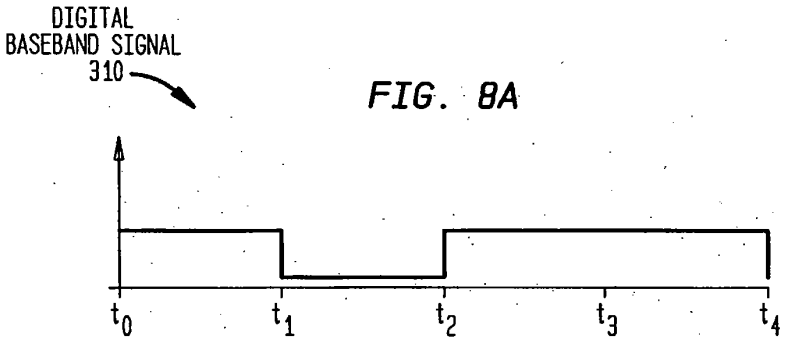


FIG. 8A

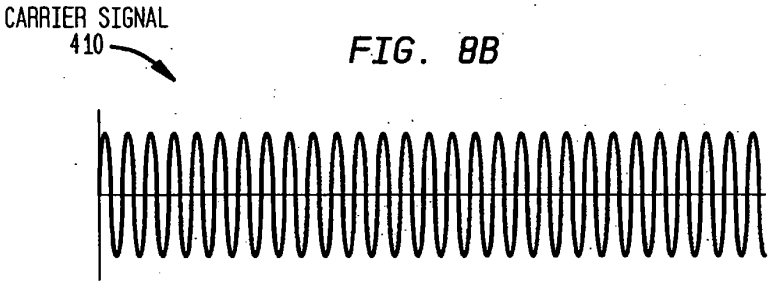


FIG. 8B

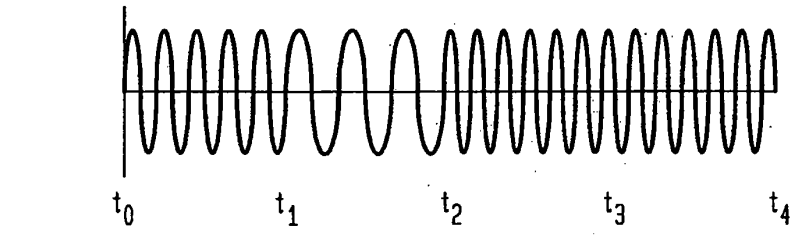


FIG. 8C

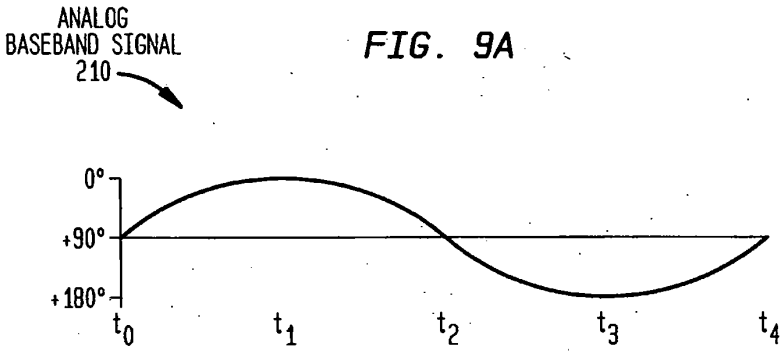


FIG. 9A

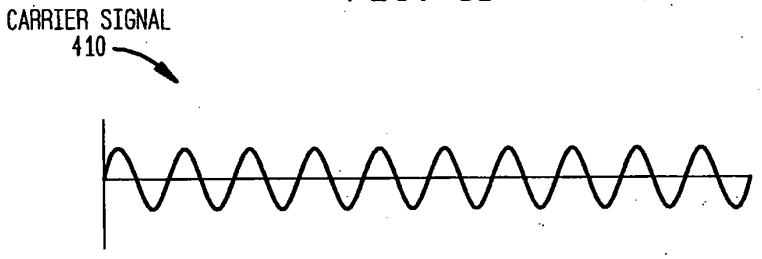


FIG. 9B

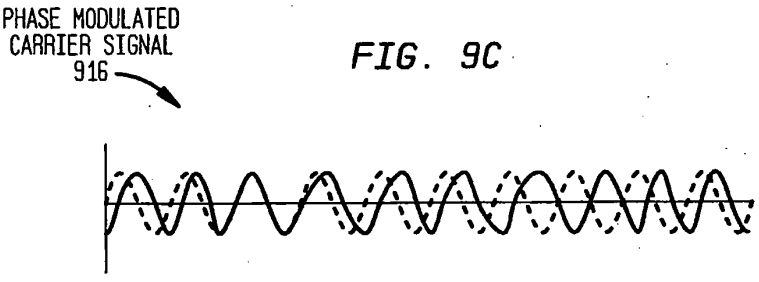


FIG. 9C

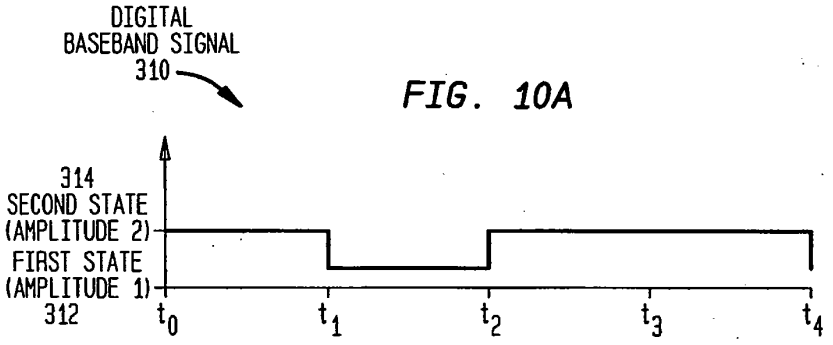


FIG. 10A

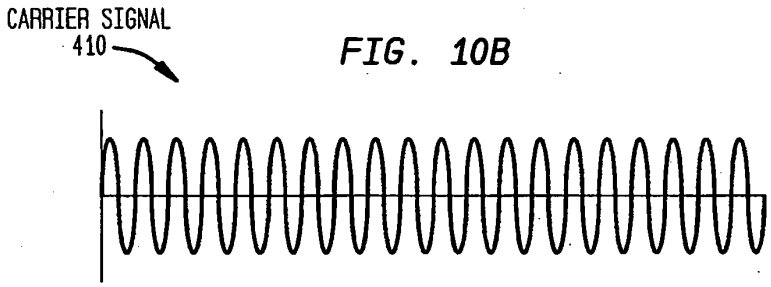


FIG. 10B

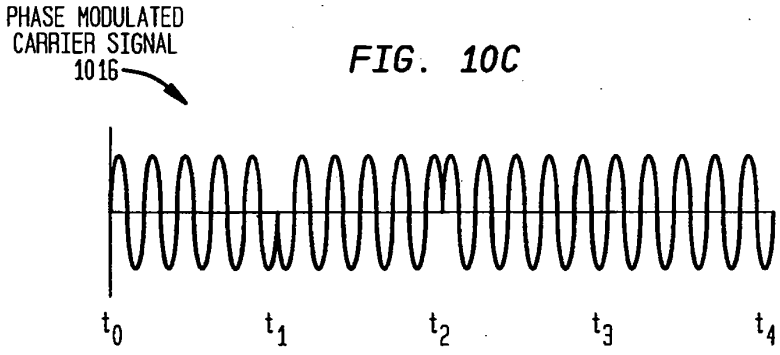


FIG. 10C

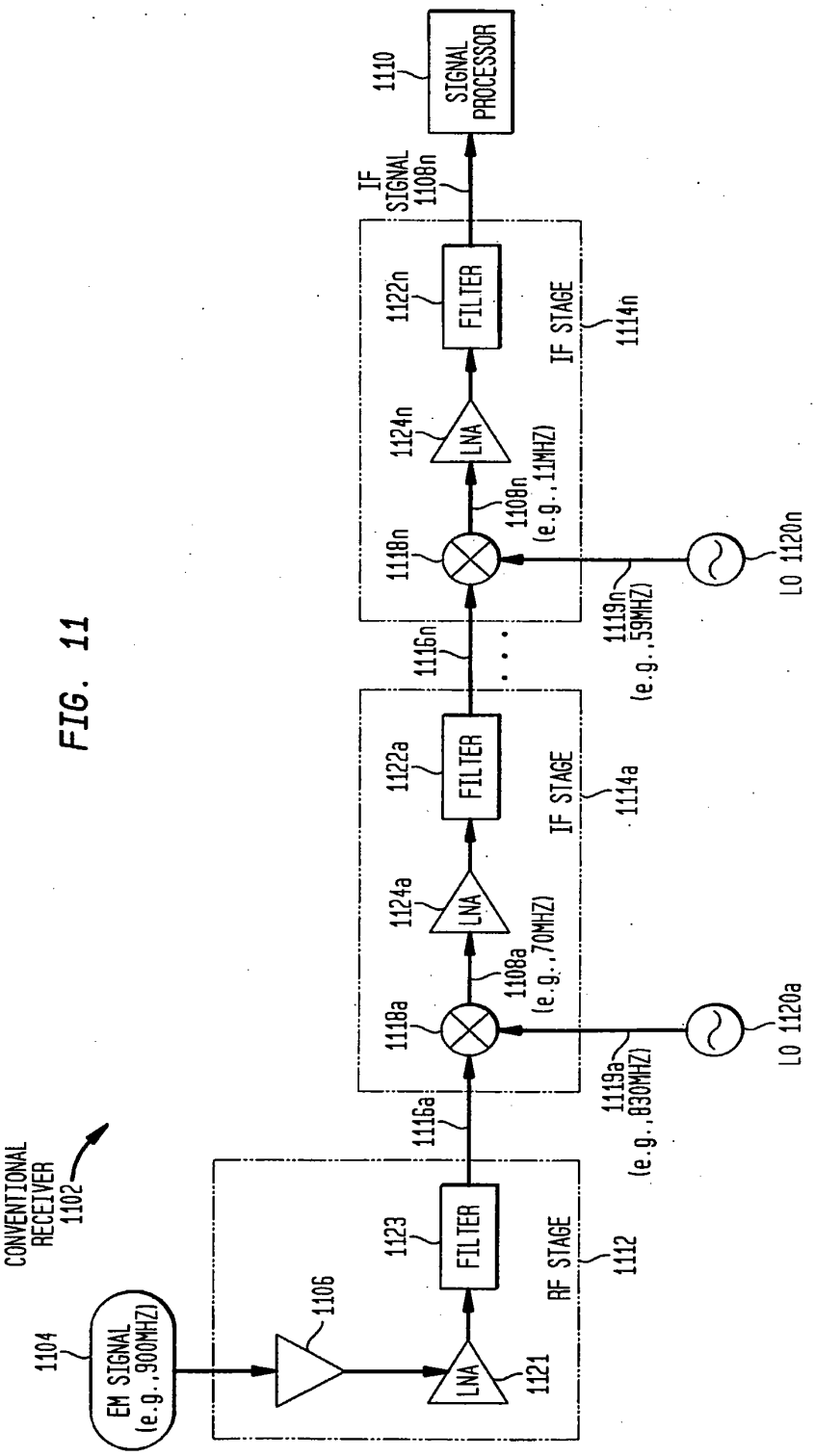
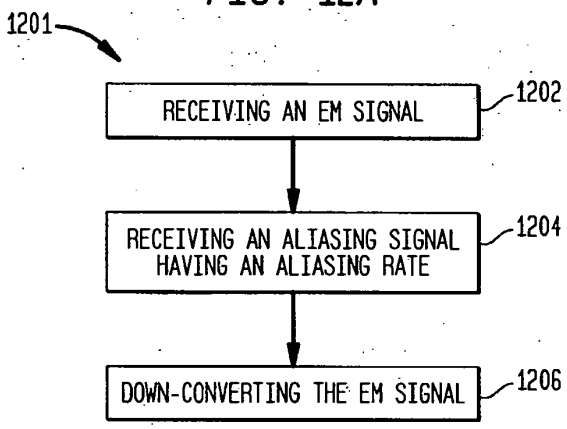

CONVENTIONAL RECEIVER 1102
1104
EM SIGNAL (e.g., 900MHZ)
1106
1121
LNA
1123
FILTER
RF STAGE
1112
1116a
1118a
1108a (e.g., 70MHZ)
1124a
LNA
1122a
FILTER
IF STAGE
1114a
1119a (e.g., 830MHZ)
LO 1120a
1116n
1118n
1108n (e.g., 11MHZ)
1124n
LNA
1122n
FILTER
IF STAGE
1114n
1119n (e.g., 59MHZ)
LO 1120n
IF SIGNAL 1108n
1110
SIGNAL PROCESSOR

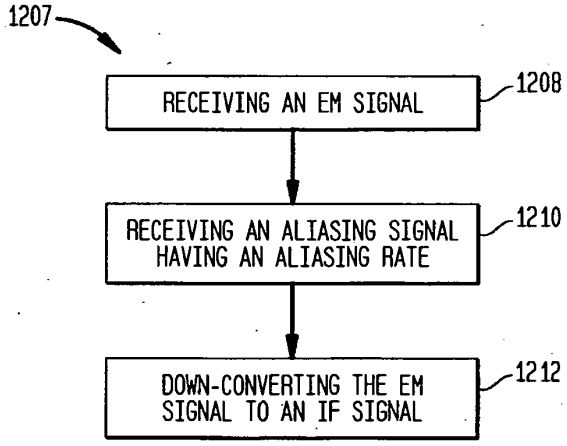
FIG. 11

FIG. 12A



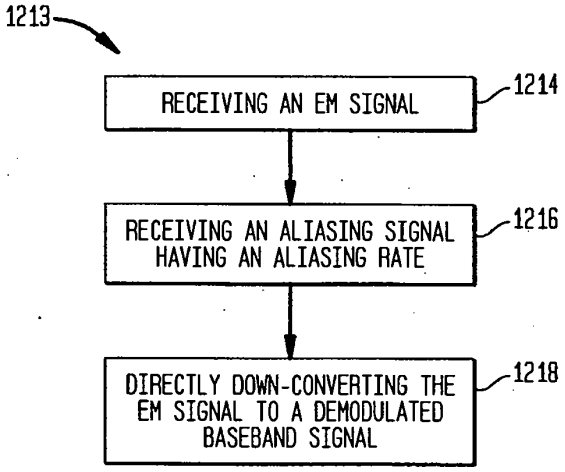
GENERIC DOWN-CONVERTING FLOWCHART

FIG. 12B



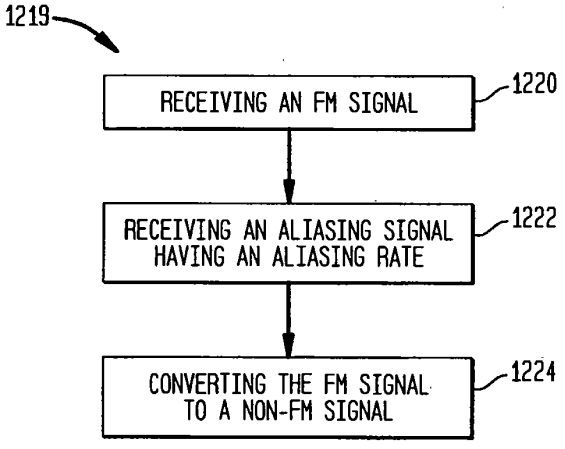
DOWN-CONVERTING AN EM SIGNAL TO AN IF SIGNAL

FIG. 12C



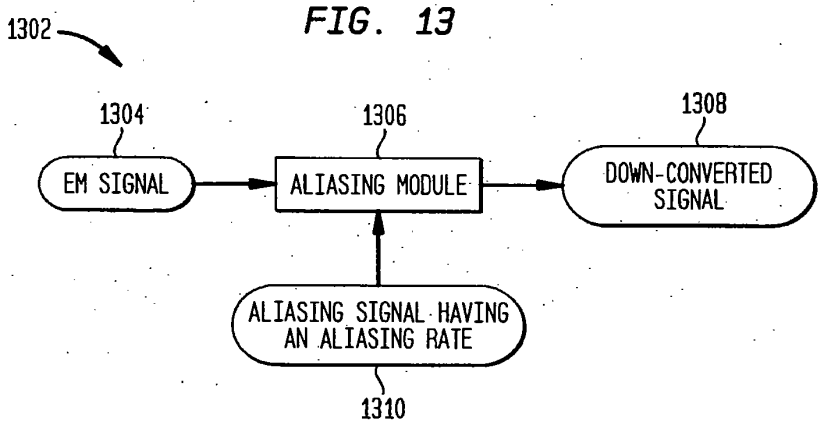
DIRECTLY DOWN-CONVERTING AN EM SIGNAL TO A DEMODULATED BASEBAND SIGNAL

FIG. 12D



MODULATION CONVERSION

FIG. 13



GENERIC DOWN-CONVERTING SYSTEM

FIG. 14A

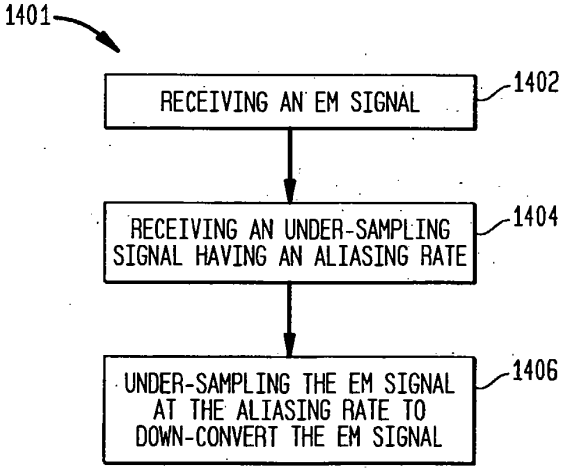


FIG. 14B

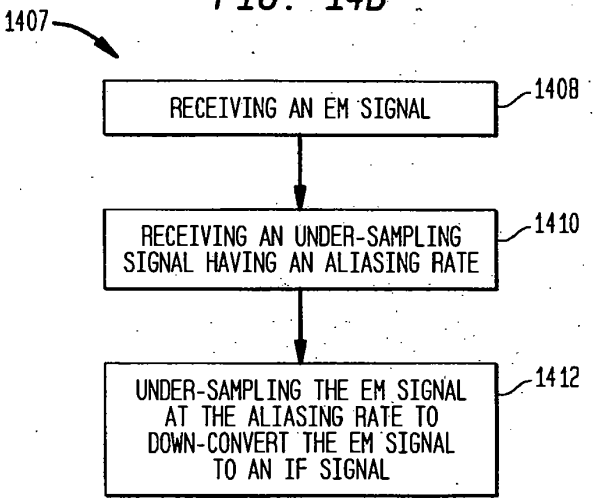


FIG. 14C

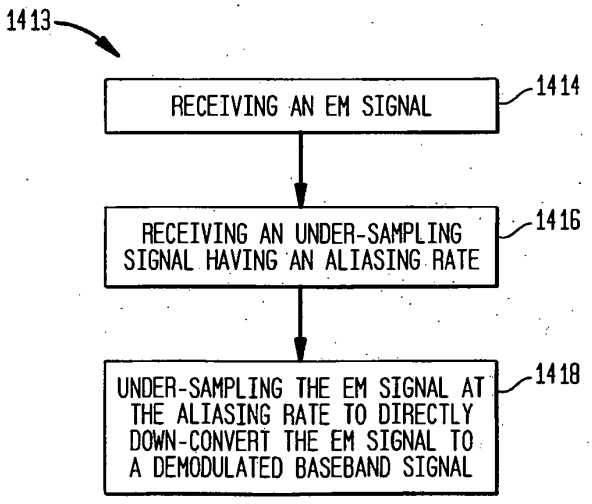


FIG. 14D

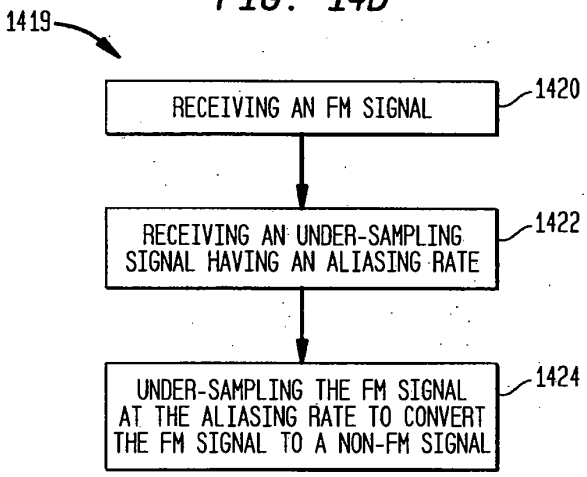

1419
RECEIVING AN FM SIGNAL
1420
RECEIVING AN UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE
1422
UNDER-SAMPLING THE FM SIGNAL AT THE ALIASING RATE TO CONVERT THE FM SIGNAL TO A NON-FM SIGNAL
1424

FIG. 15E

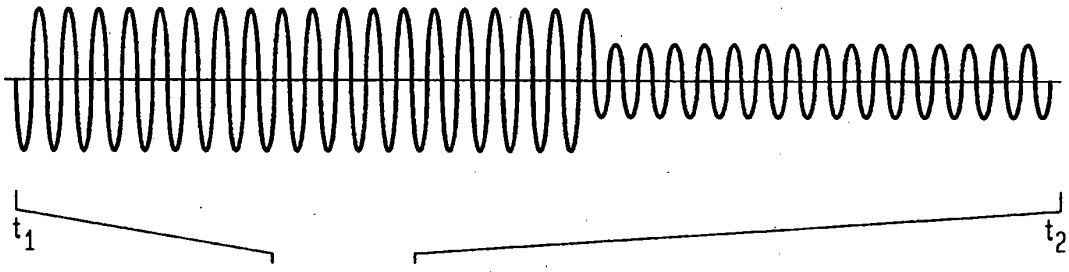


FIG. 15A

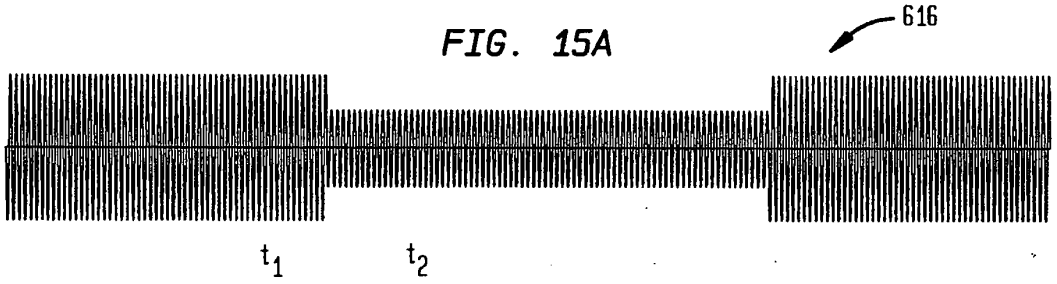


FIG. 15B

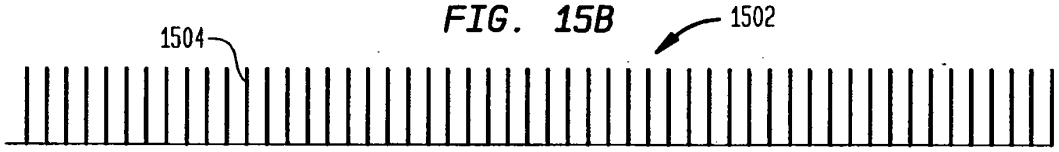


FIG. 15C

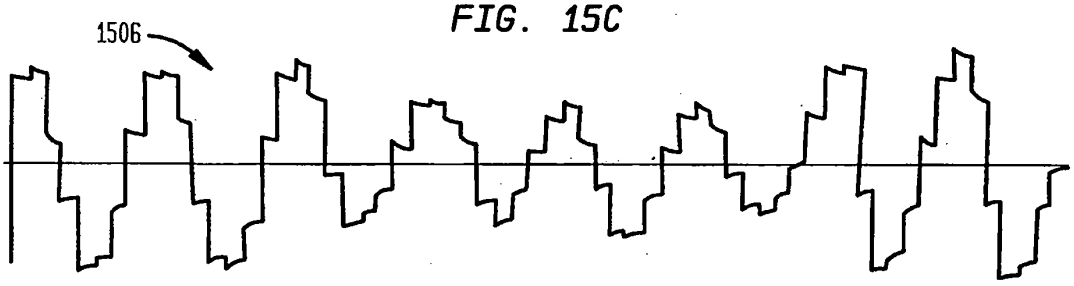


FIG. 15D

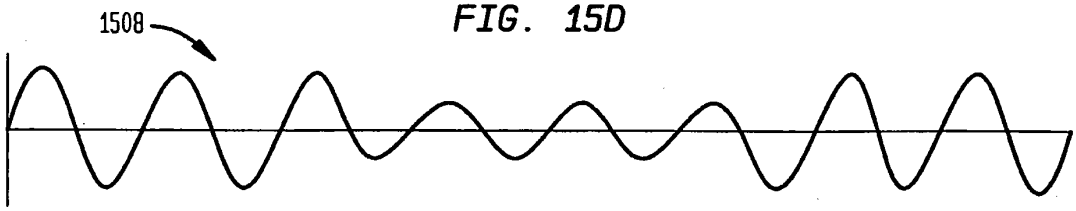


FIG. 16

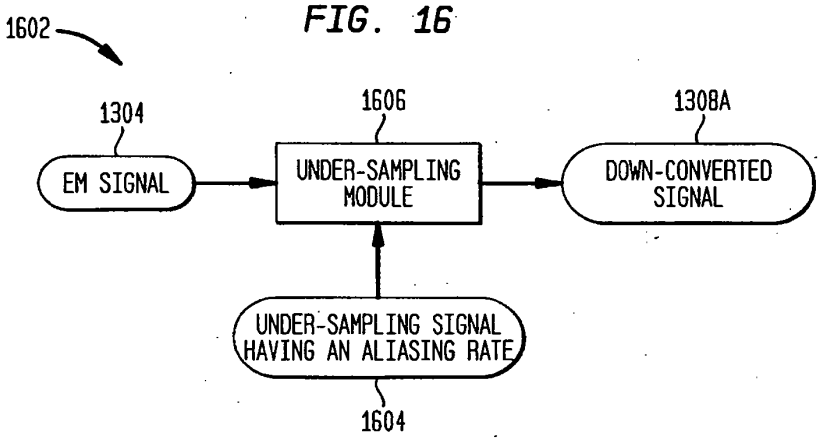

1602
1304
EM SIGNAL
1606
UNDER-SAMPLING MODULE
1308A
DOWN-CONVERTED SIGNAL
UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE
1604

FIG. 17

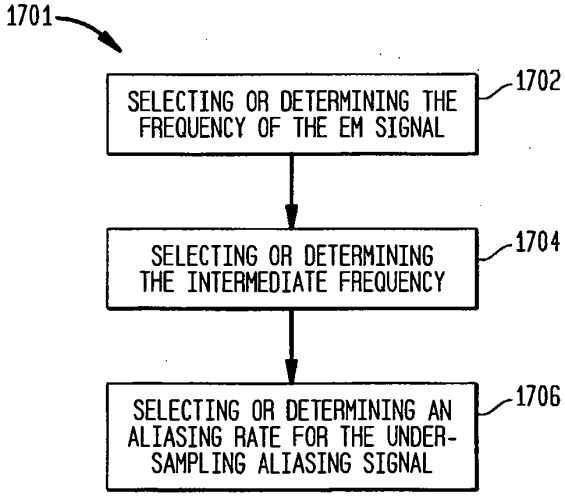

1701
SELECTING OR DETERMINING THE FREQUENCY OF THE EM SIGNAL
1702
SELECTING OR DETERMINING THE INTERMEDIATE FREQUENCY
1704
SELECTING OR DETERMINING AN ALIASING RATE FOR THE UNDER-SAMPLING ALIASING SIGNAL
1706

FIG. 18A

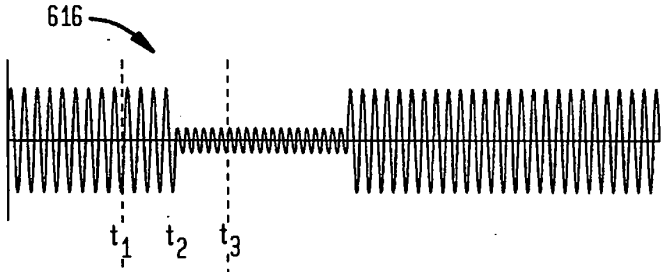


FIG. 18B

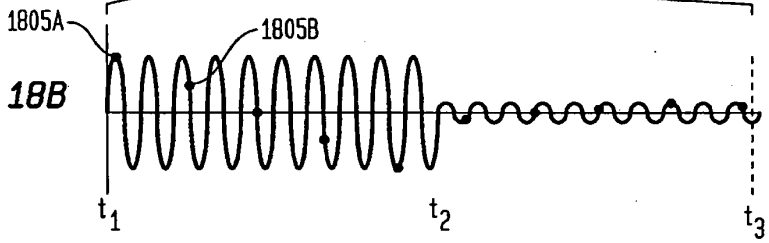


FIG. 18C

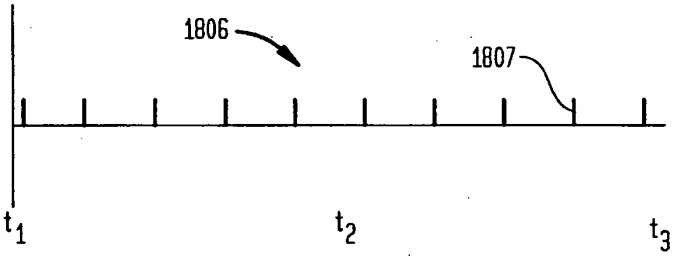


FIG. 18D

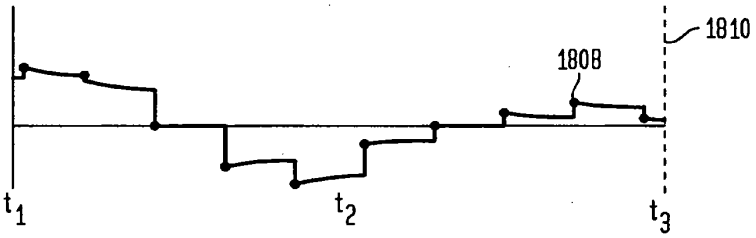


FIG. 18E

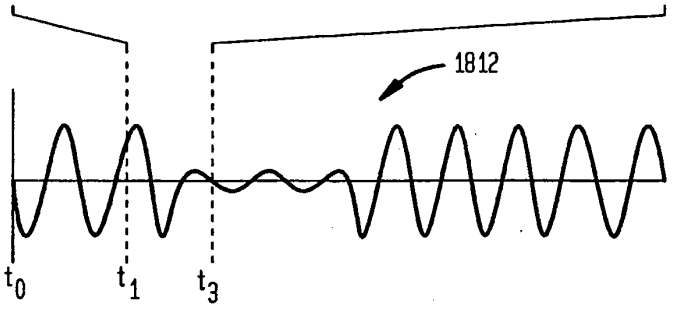


FIG. 19A

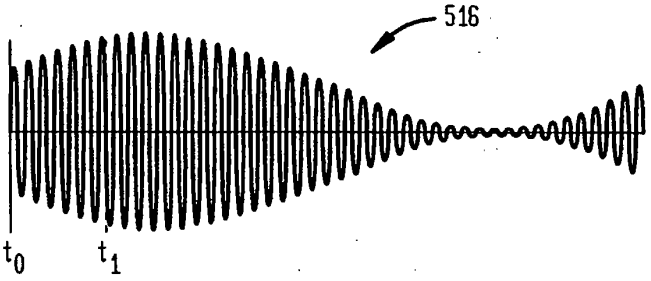


FIG. 19B

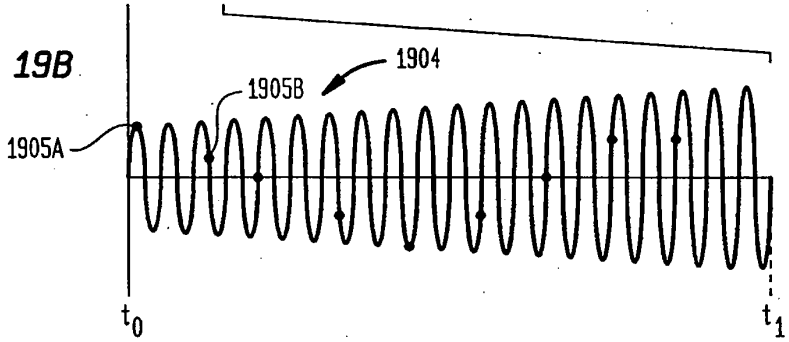


FIG. 19C

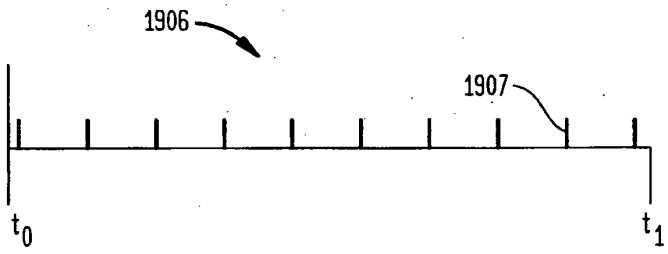


FIG. 19D

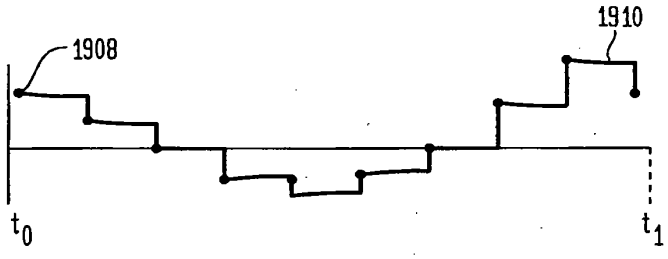


FIG. 19E

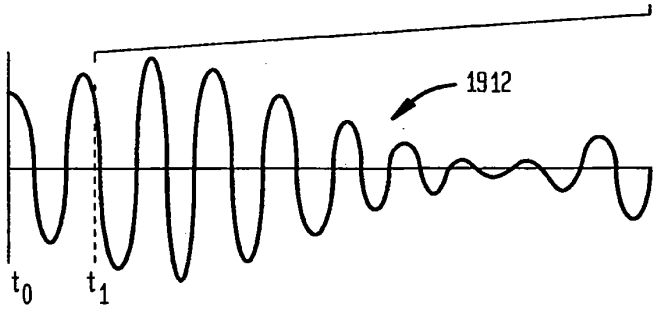


FIG. 20A

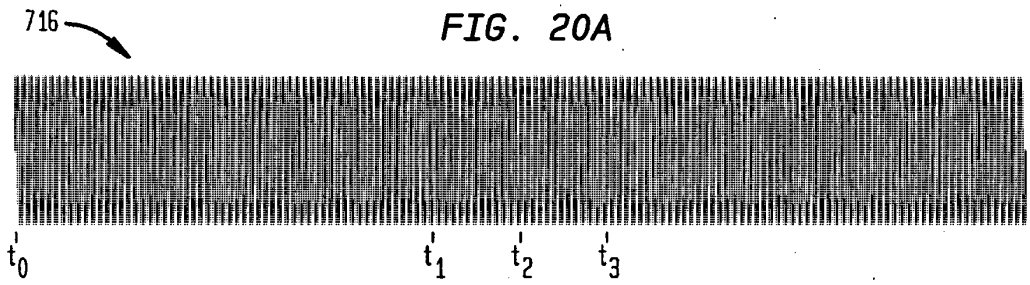


FIG. 20B

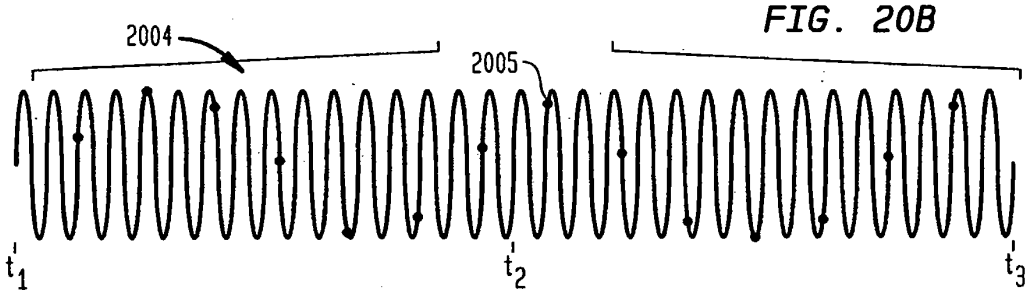


FIG. 20C

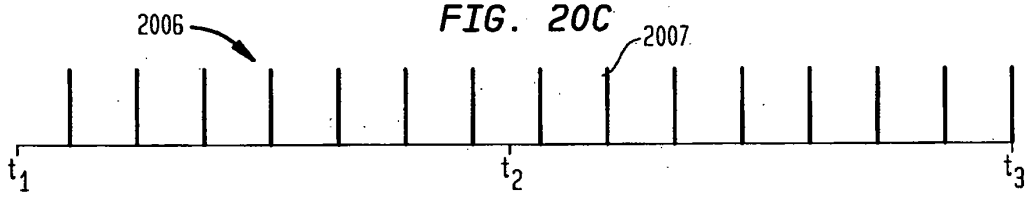


FIG. 20D

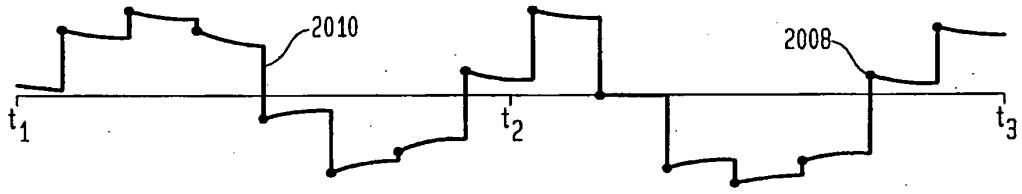


FIG. 20E

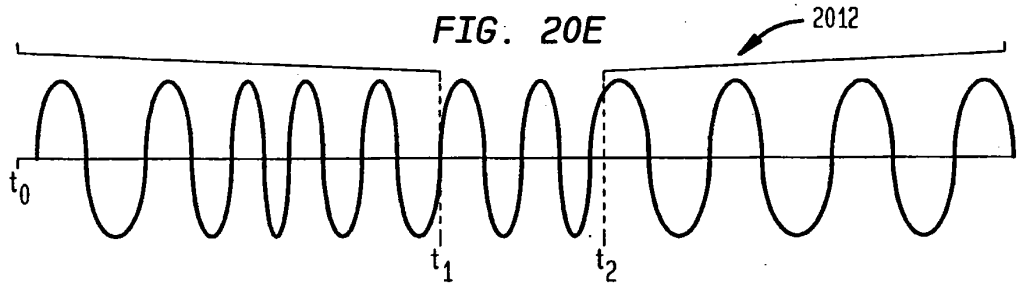


FIG. 21A

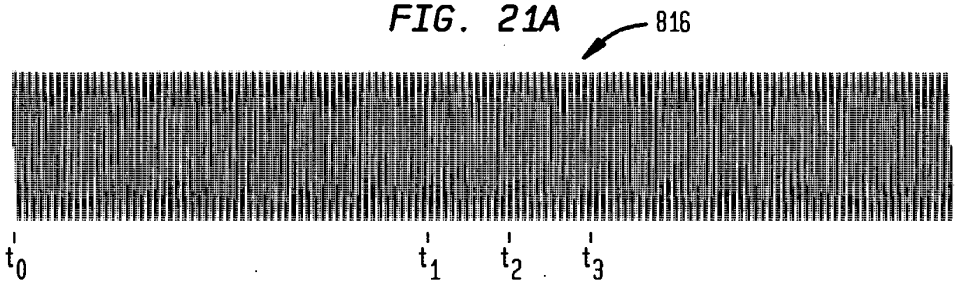


FIG. 21B

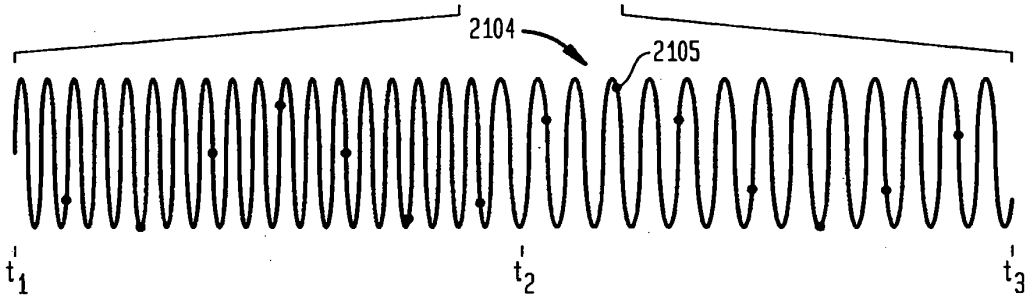


FIG. 21C

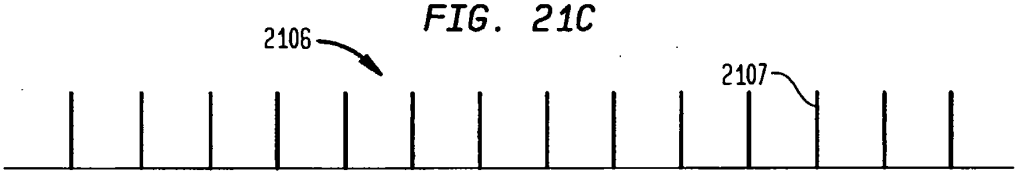


FIG. 21D

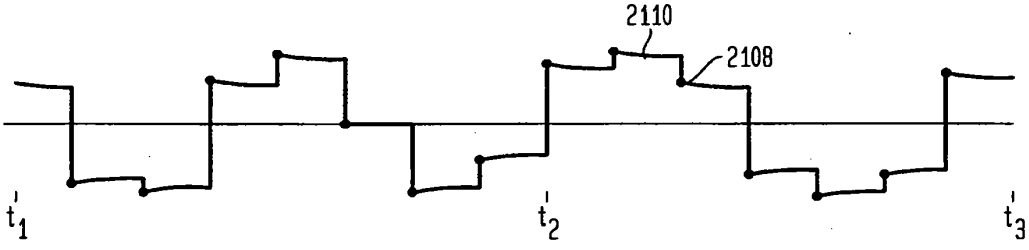


FIG. 21E

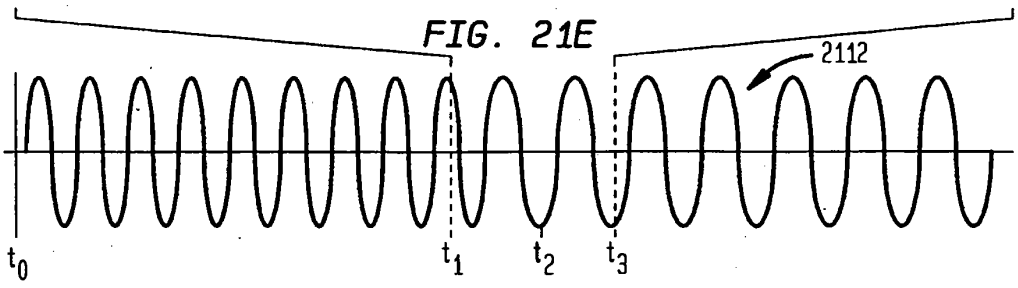


FIG. 22A

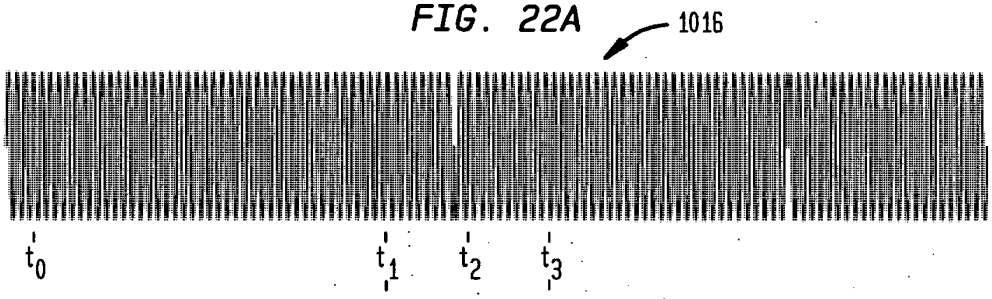


FIG. 22B

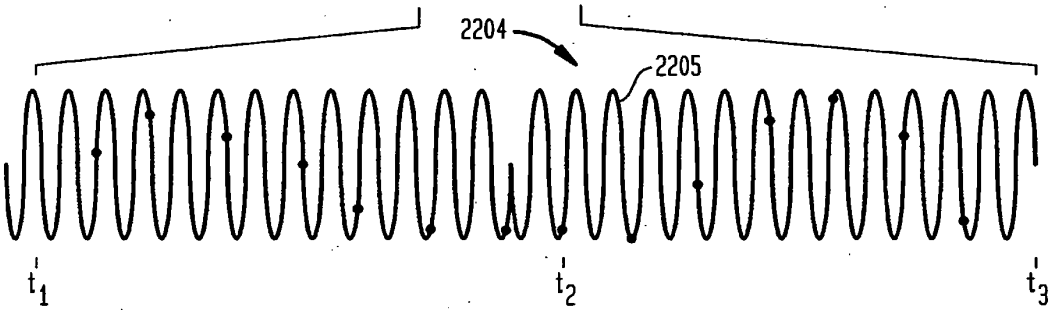


FIG. 22C

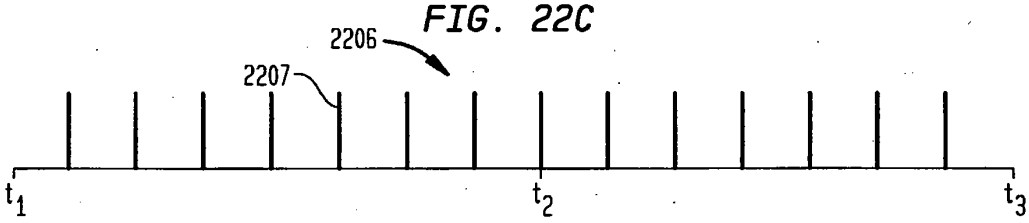


FIG. 22D

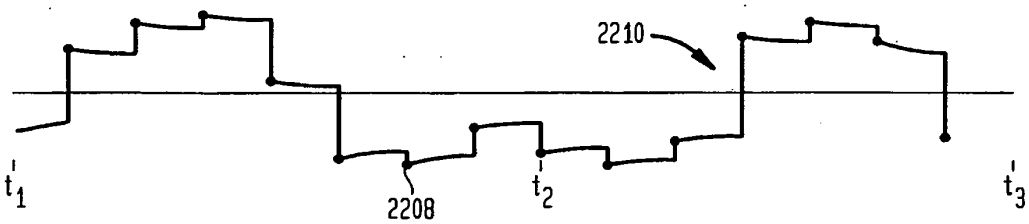


FIG. 22E

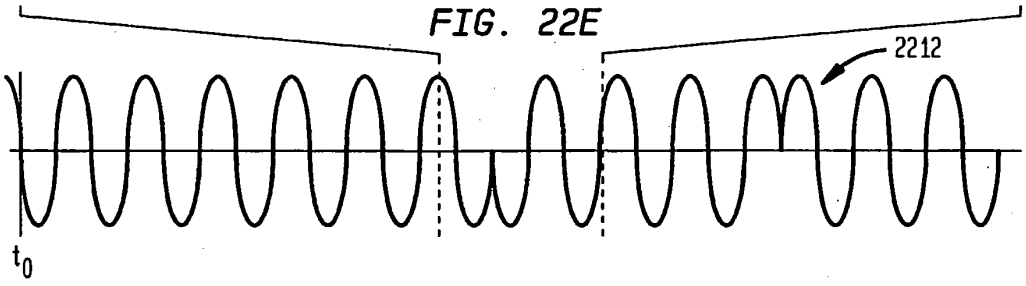


FIG. 23A

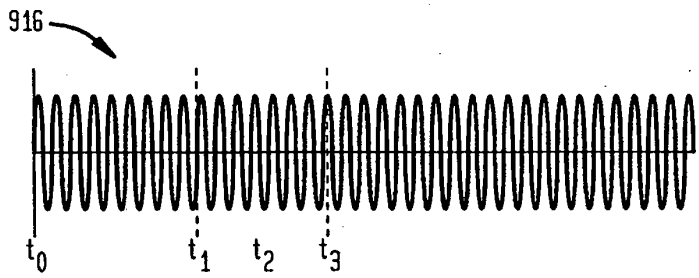


FIG. 23B

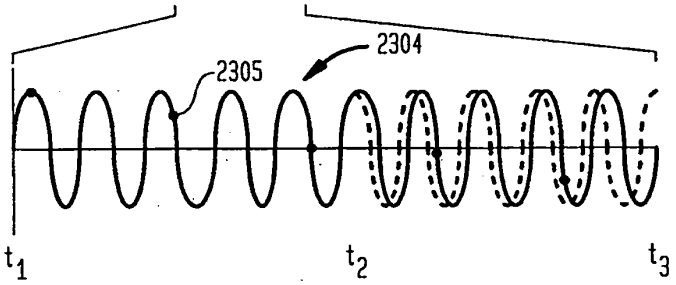


FIG. 23C

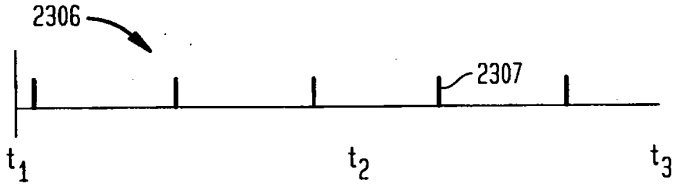


FIG. 23D

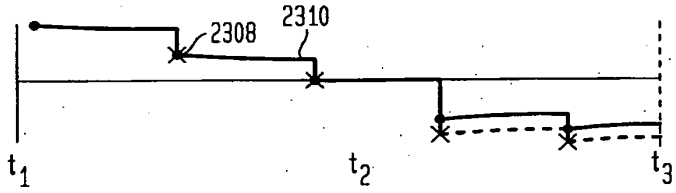
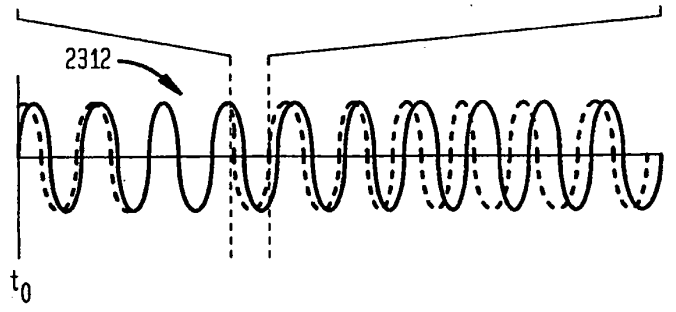


FIG. 23E



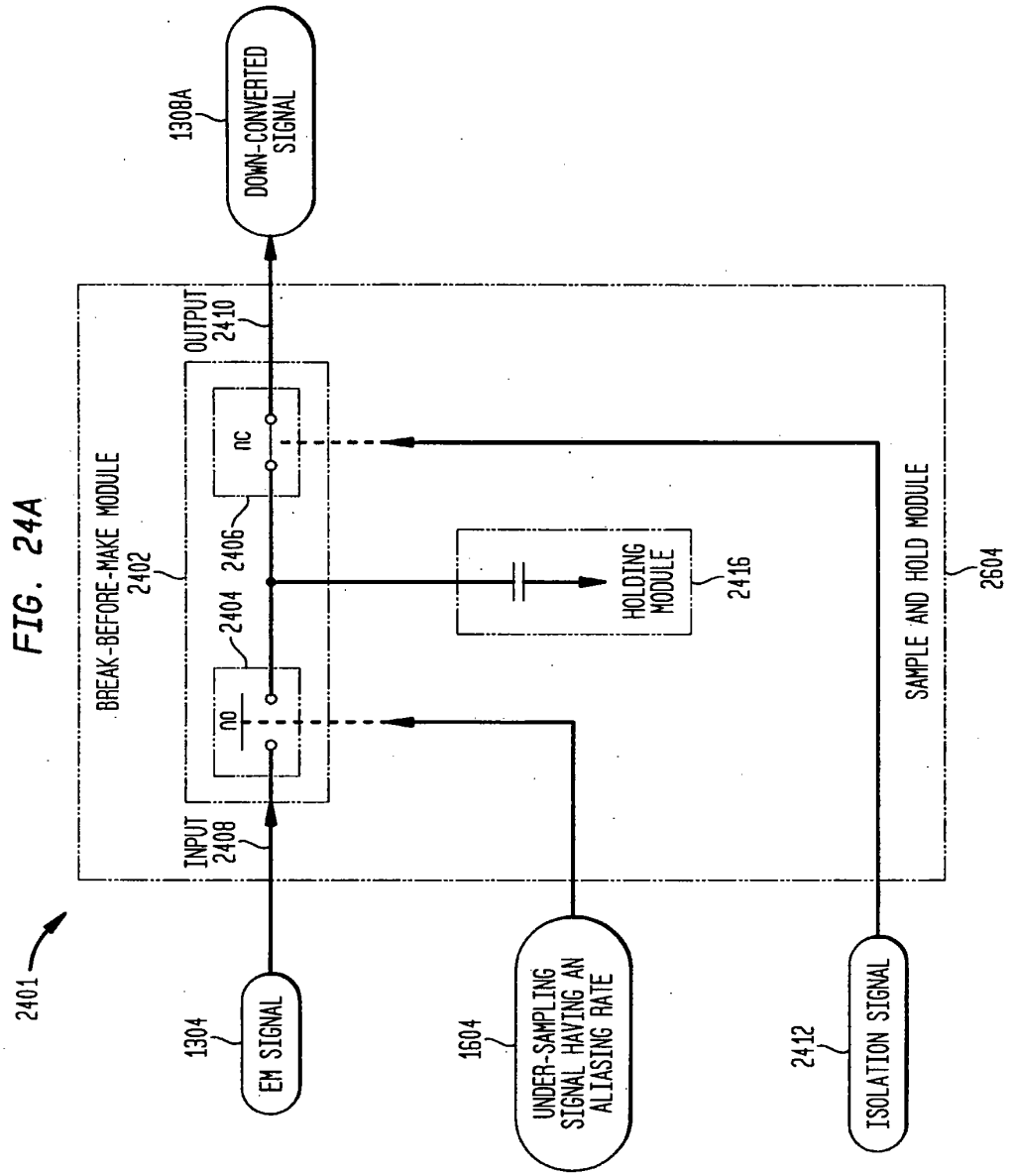

2401
1304
EM SIGNAL
1604
UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE
2412
ISOLATION SIGNAL
BREAK-BEFORE-MAKE MODULE
2402
INPUT
2408
OUTPUT
2410
2404
2406
no
nc
HOLDING MODULE
2416
SAMPLE AND HOLD MODULE
2604
1308A
DOWN-CONVERTED SIGNAL

FIG. 24A

FIG. 24B

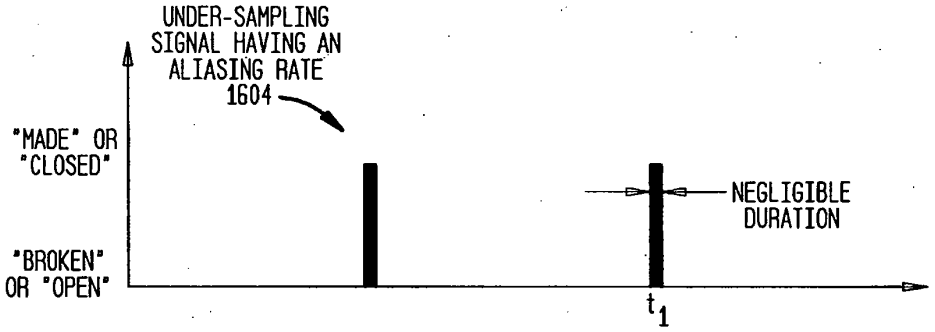
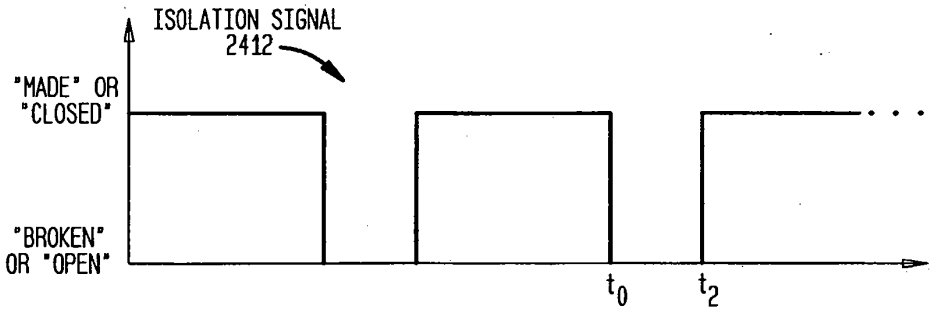


FIG. 24C



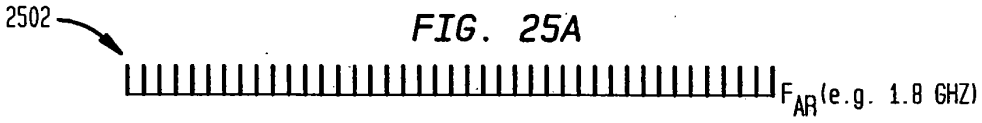


FIG. 25A

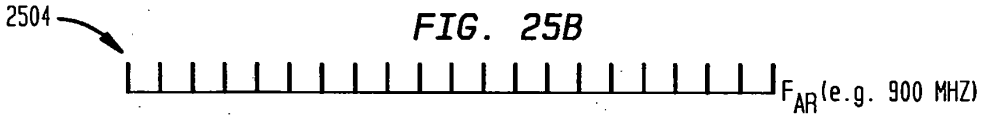


FIG. 25B

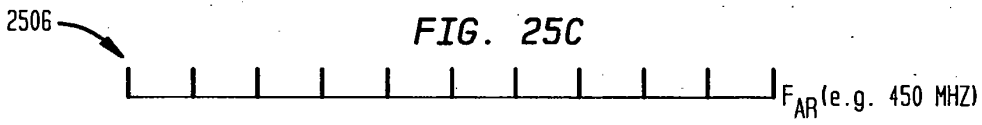


FIG. 25C

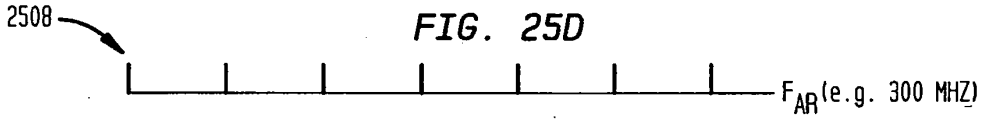


FIG. 25D

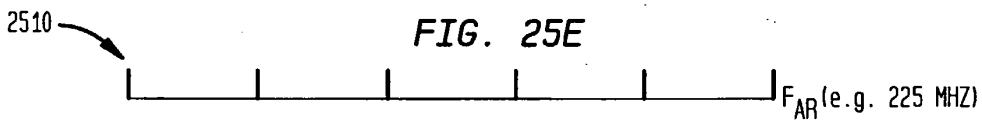


FIG. 25E

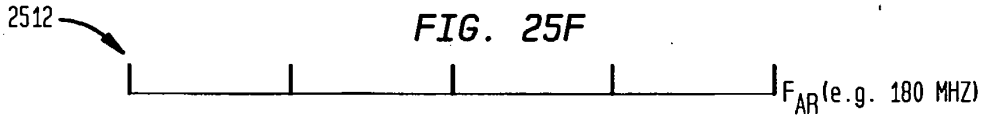


FIG. 25F

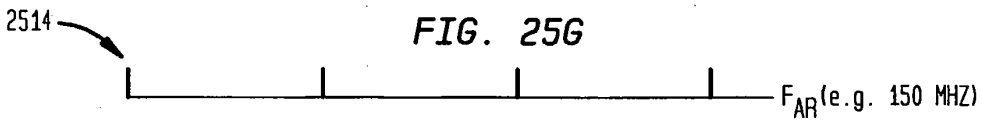


FIG. 25G

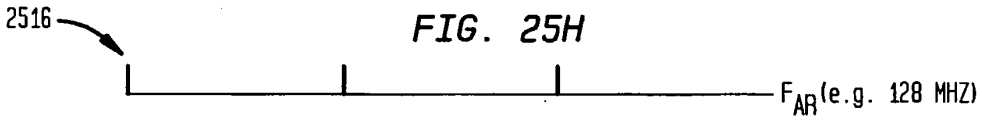


FIG. 25H

FIG. 26A

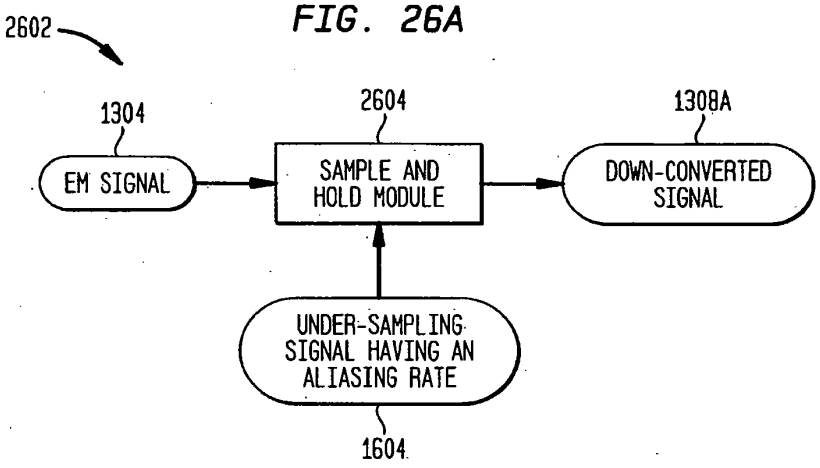
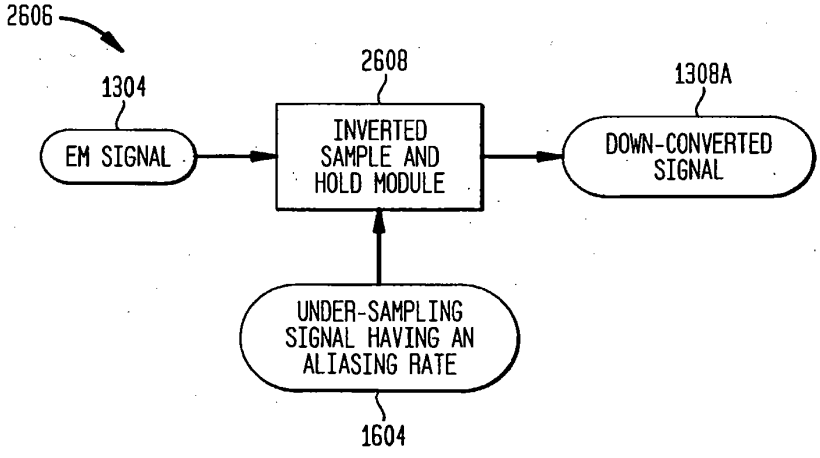


FIG. 26B



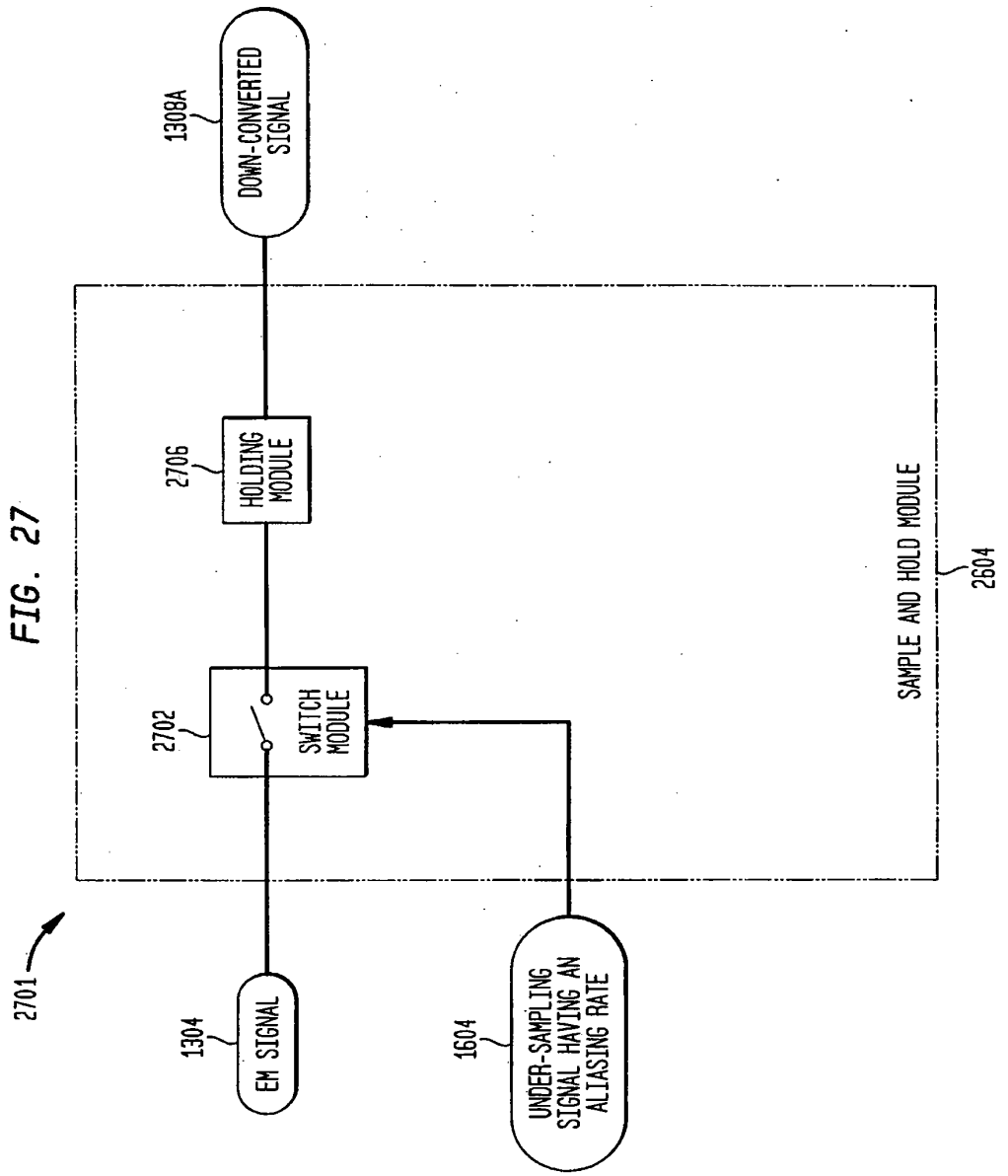

FIG. 27
2701
1304
EM SIGNAL
1604
UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE
2702
SWITCH MODULE
2706
HOLDING MODULE
1308A
DOWN-CONVERTED SIGNAL
SAMPLE AND HOLD MODULE
2604

FIG. 28A

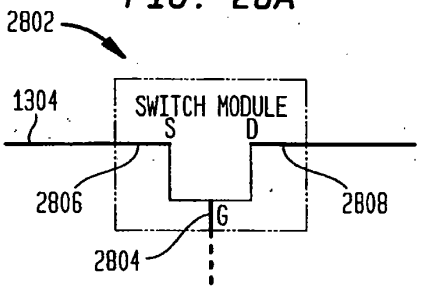


FIG. 28B

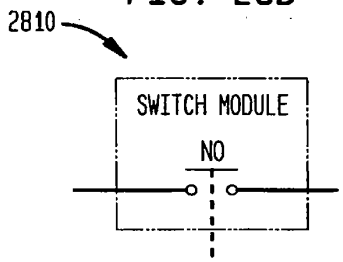


FIG. 28C

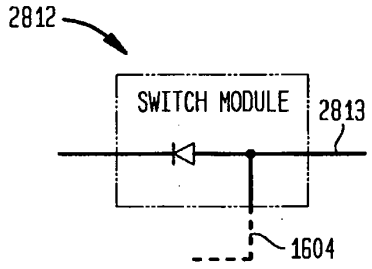


FIG. 28D

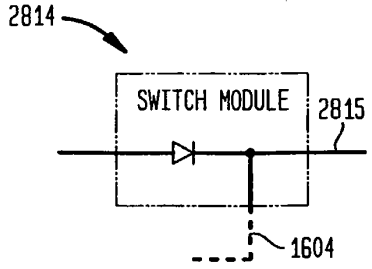


FIG. 29A

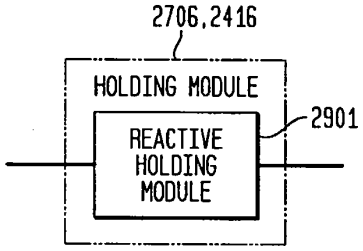


FIG. 29B

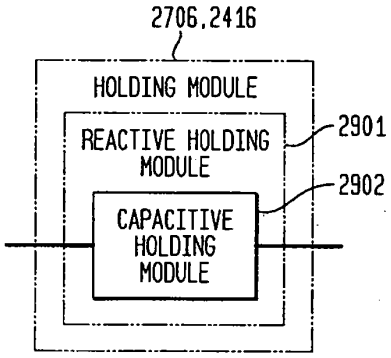


FIG. 29C

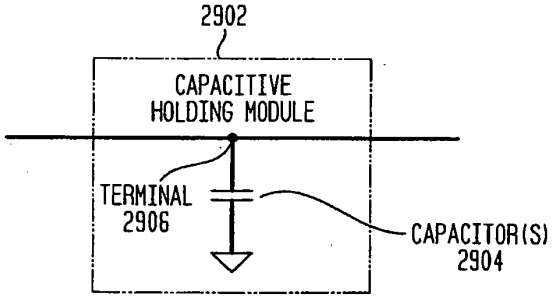


FIG. 29D

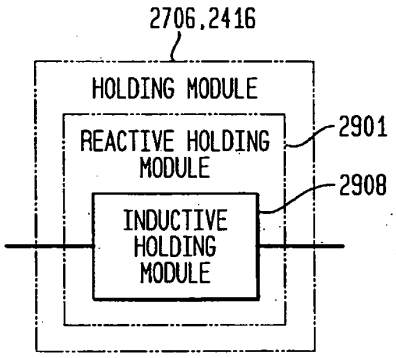


FIG. 29E

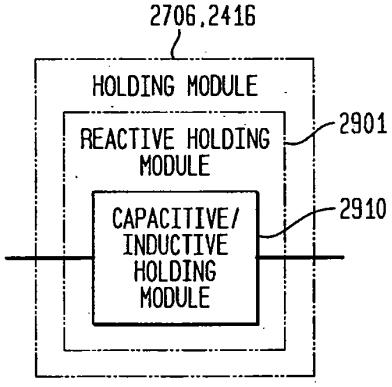


FIG. 29F

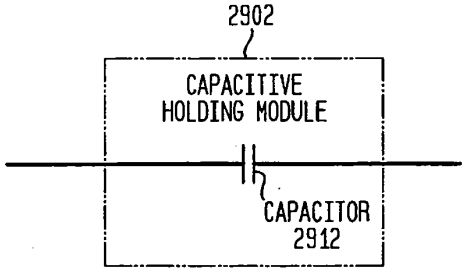


FIG. 29G

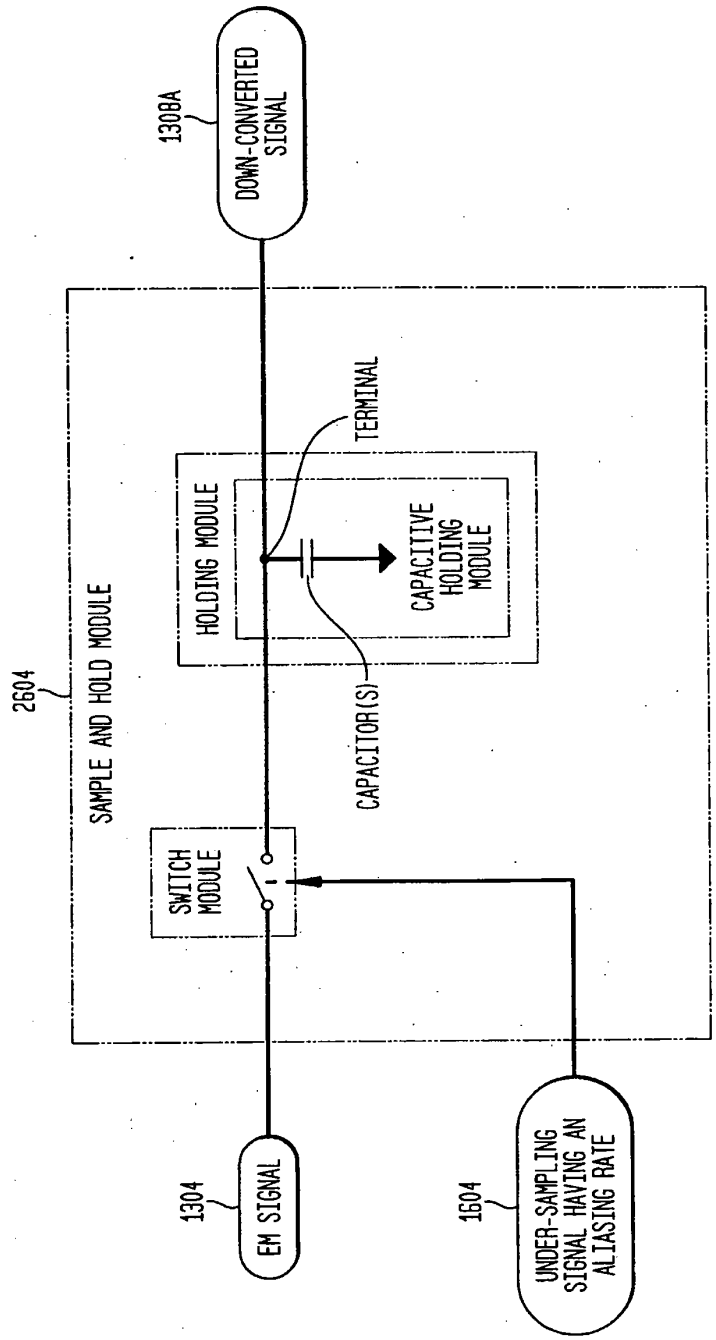
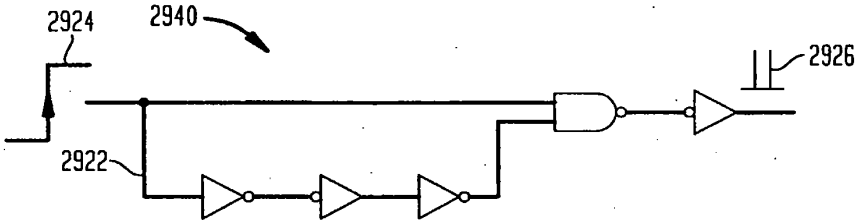
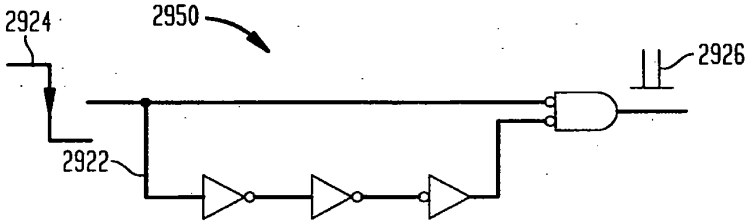

1308A
DOWN-CONVERTED SIGNAL
2604
SAMPLE AND HOLD MODULE
HOLDING MODULE
TERMINAL
CAPACITIVE HOLDING MODULE
CAPACITOR(S)
SWITCH MODULE
1304
EM SIGNAL
1604
UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE

FIG. 29H



A. RISING EDGE PULSE GENERATOR

FIG. 29I



B. FALLING-EDGE PULSE GENERATOR

FIG. 29J

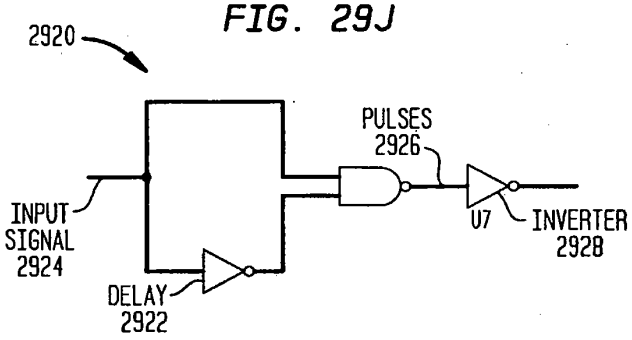


FIG. 29K

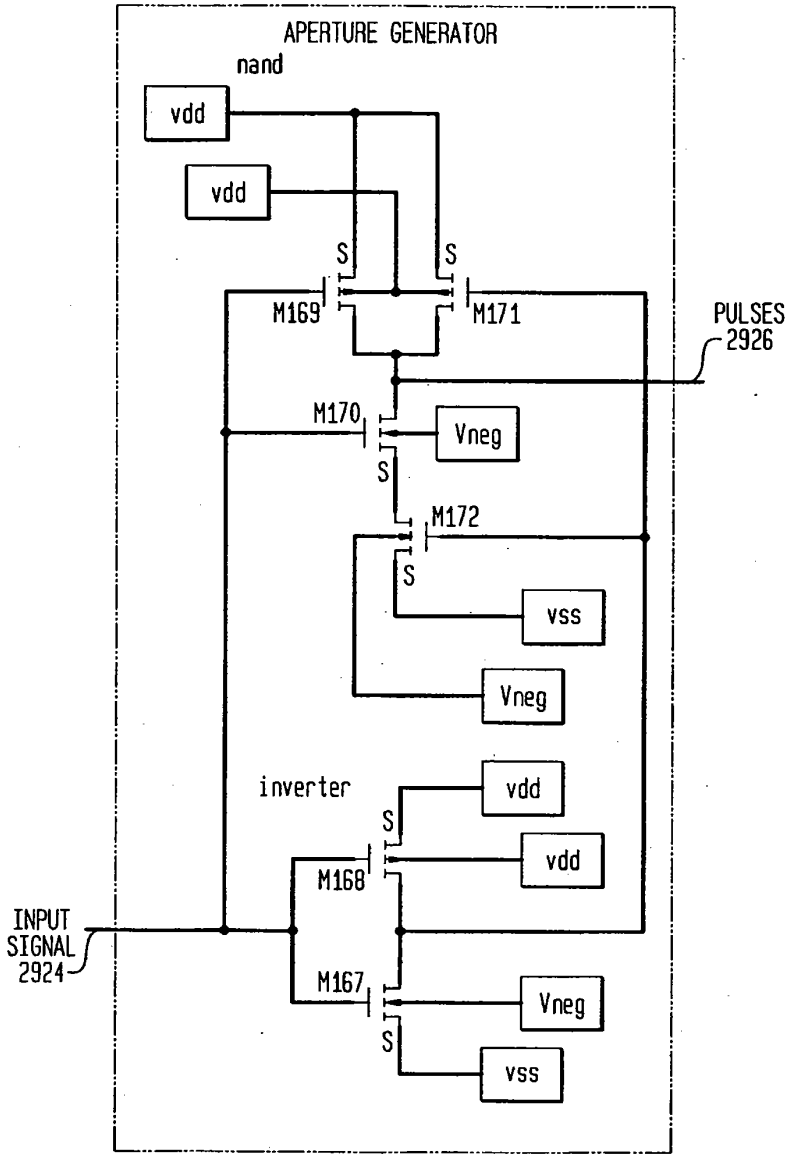


FIG. 29L

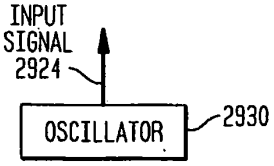


FIG. 30

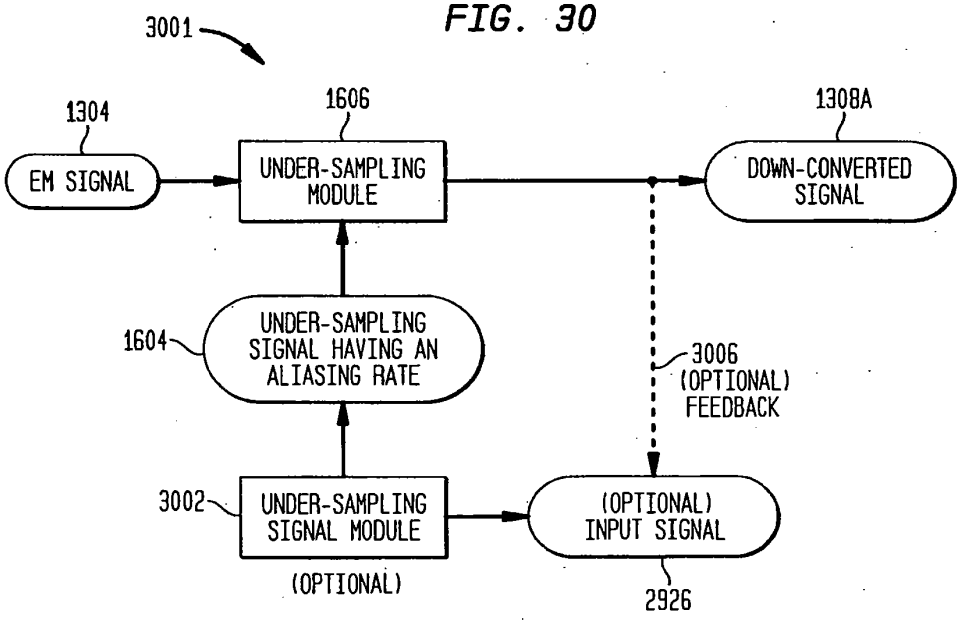

3001
1304
EM SIGNAL
1606
UNDER-SAMPLING MODULE
1308A
DOWN-CONVERTED SIGNAL
1604
UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE
3006 (OPTIONAL) FEEDBACK
3002
UNDER-SAMPLING SIGNAL MODULE
(OPTIONAL)
(OPTIONAL) INPUT SIGNAL
2926

FIG. 31A

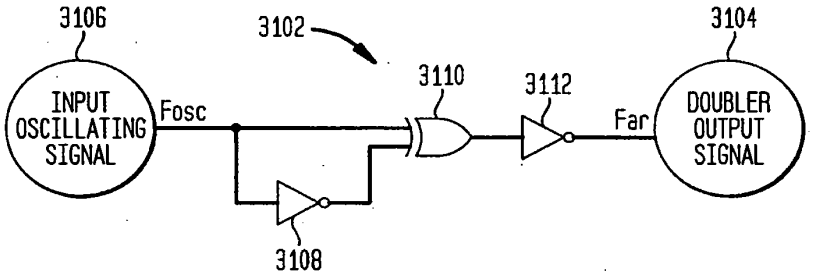

3106
3102
3104
3110
3112
INPUT OSCILLATING SIGNAL
Fosc
Far
DOUBLER OUTPUT SIGNAL
3108

FIG. 31B

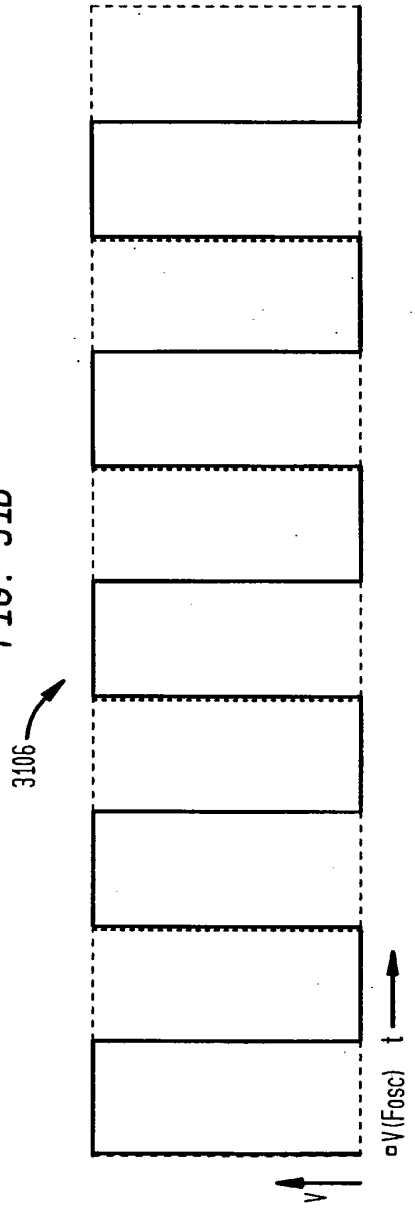


FIG. 31C

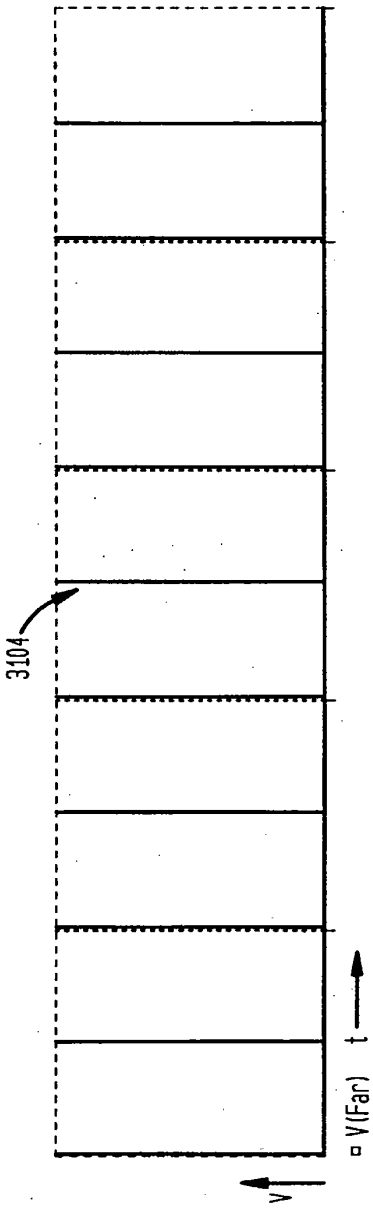


FIG. 32A

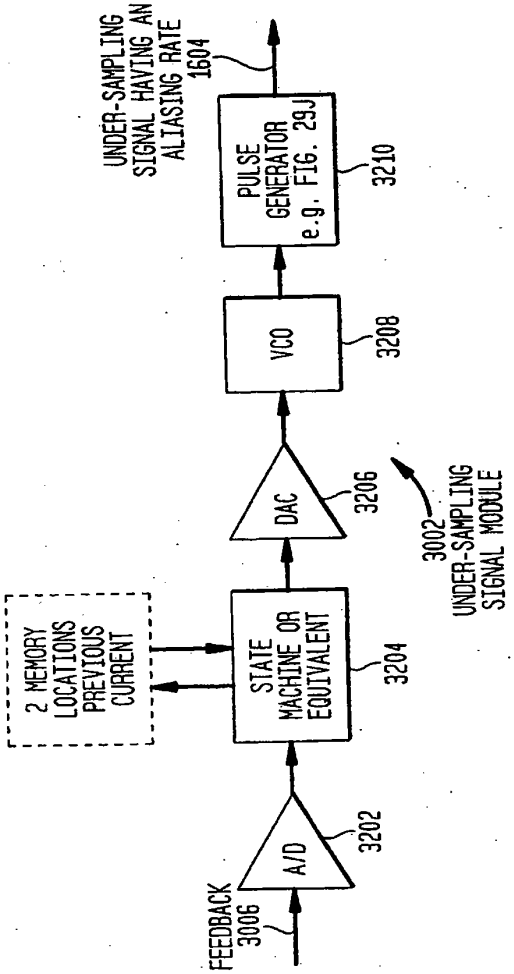
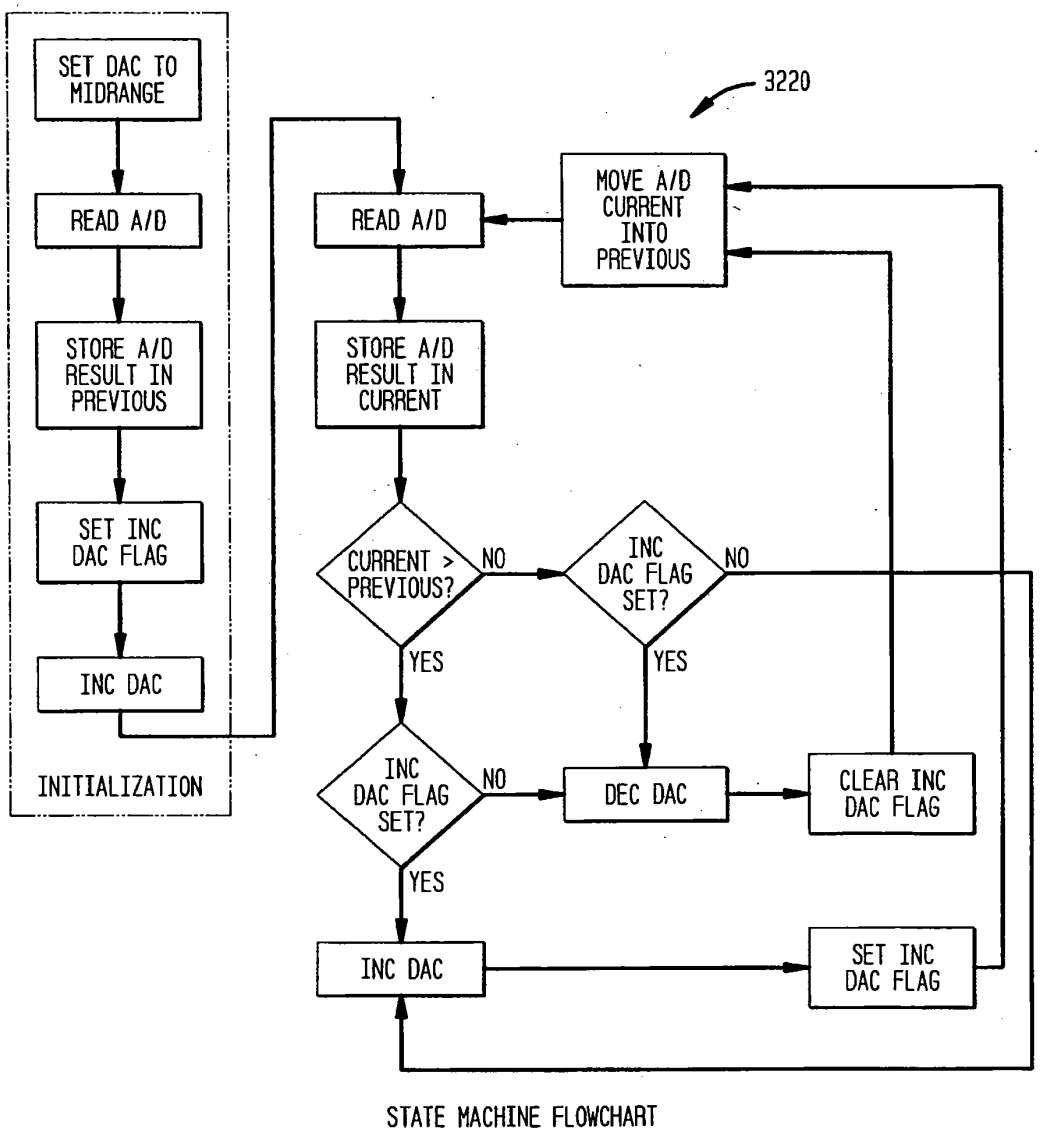
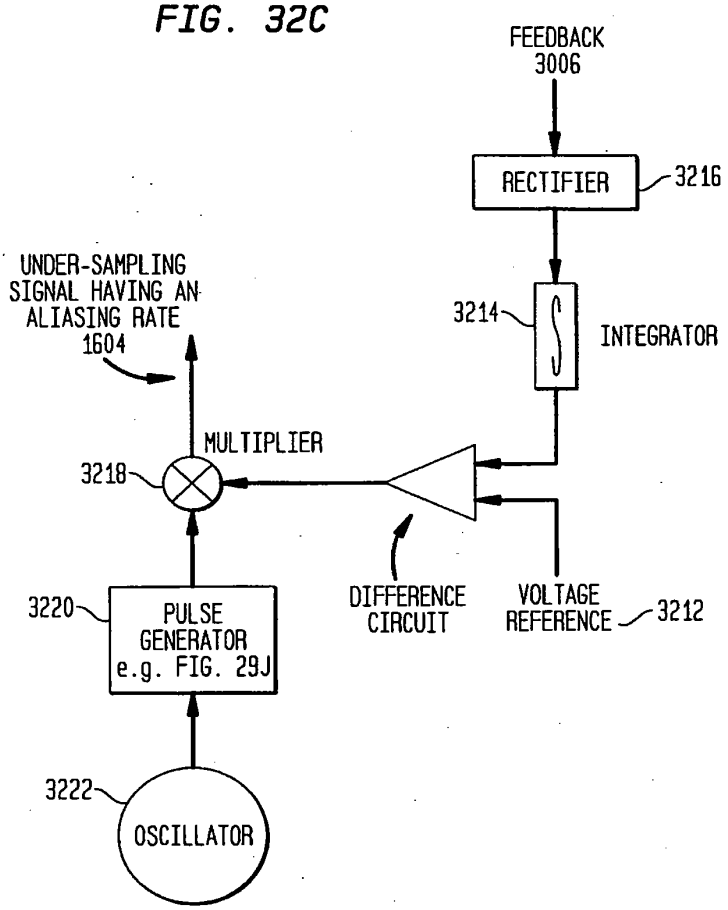

FEEDBACK
3006
A/D
3202
STATE MACHINE OR EQUIVALENT
3204
2 MEMORY LOCATIONS PREVIOUS CURRENT
DAC
3206
VCO
3208
PULSE GENERATOR e.g. FIG. 29J
3210
UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE
1604
3002
UNDER-SAMPLING SIGNAL MODULE

FIG. 32B



STATE MACHINE FLOWCHART

FIG. 32C



ENERGY TRANSFER SIGNAL MODULE 3002

FIG. 33A

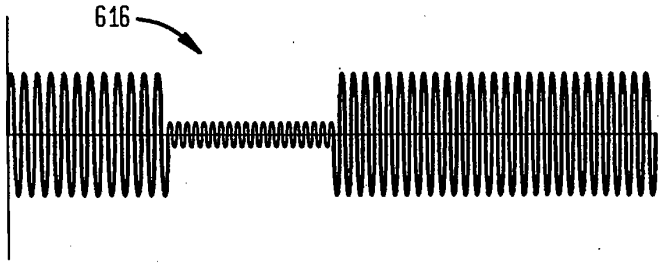


FIG. 33B

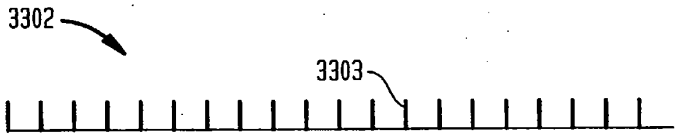


FIG. 33C

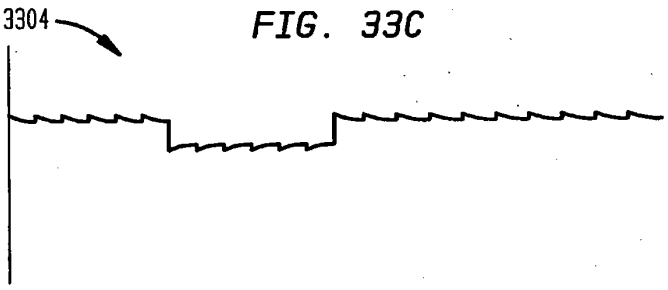


FIG. 33D

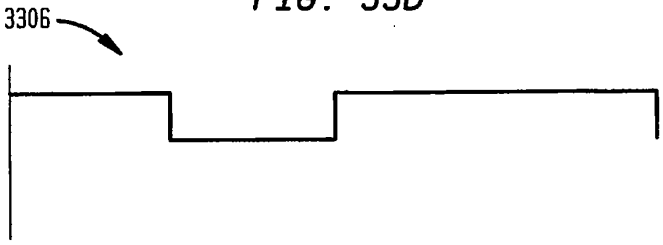


FIG. 34A

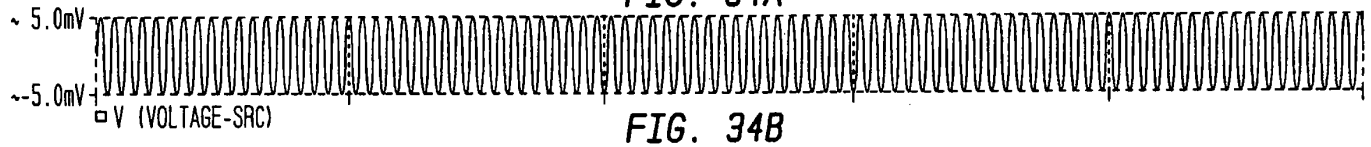


FIG. 34B

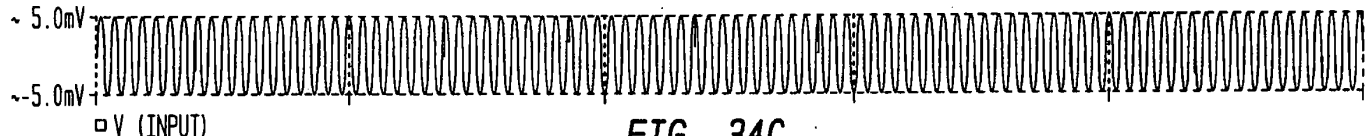


FIG. 34C

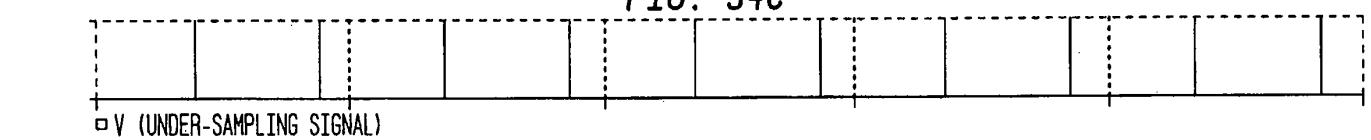


FIG. 34D

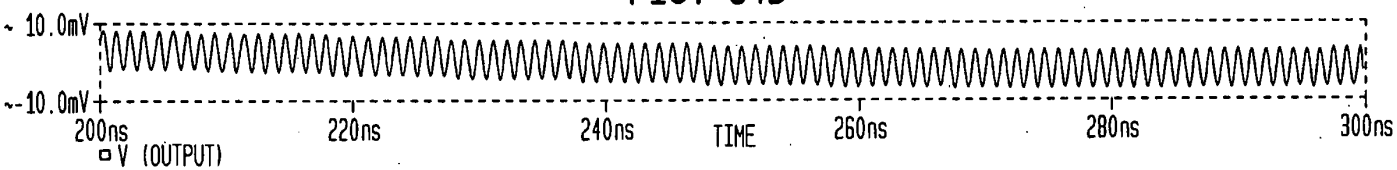


FIG. 34E

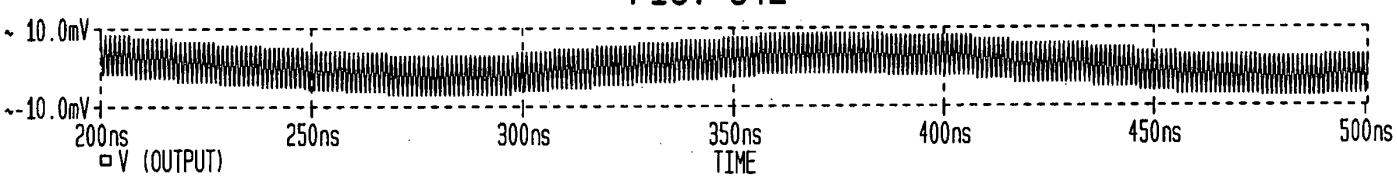


FIG. 34F

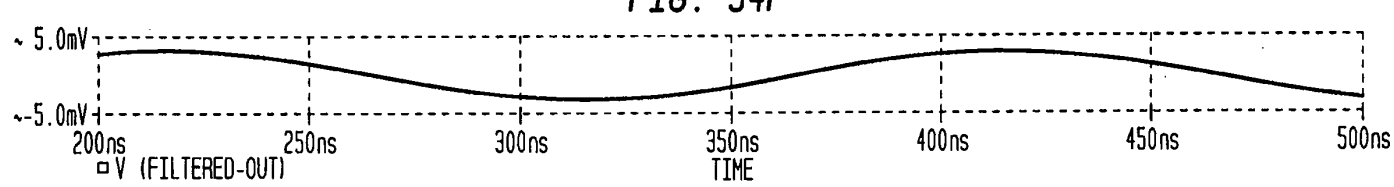


FIG. 35A

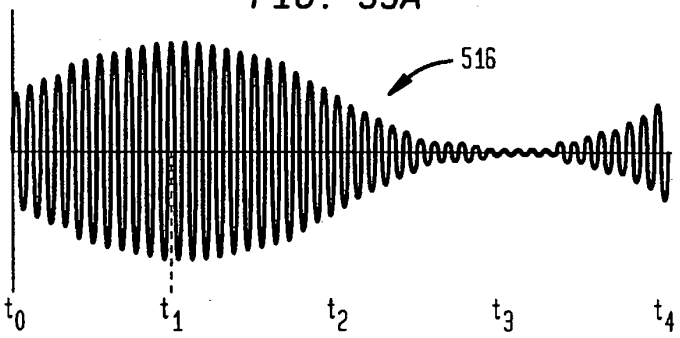


FIG. 35B

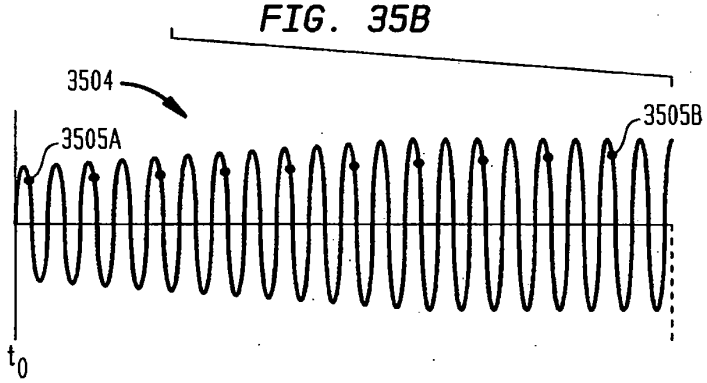


FIG. 35C

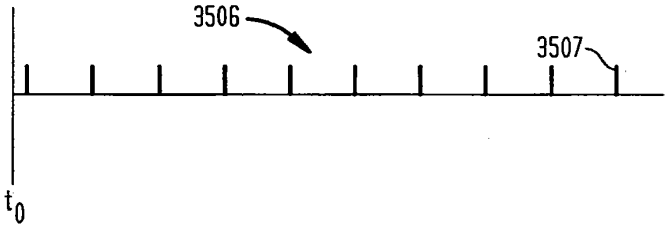


FIG. 35D

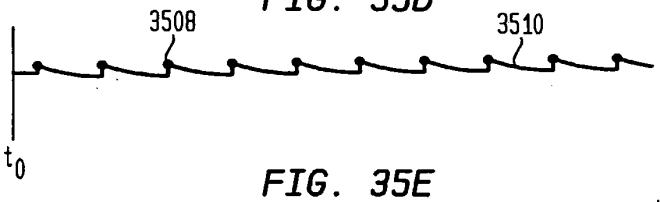


FIG. 35E

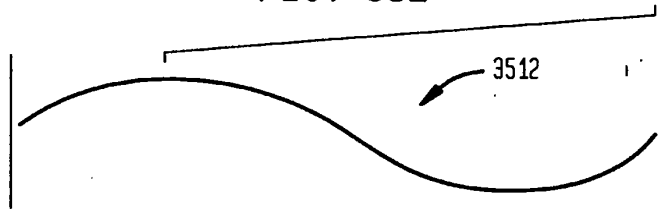


FIG. 36A

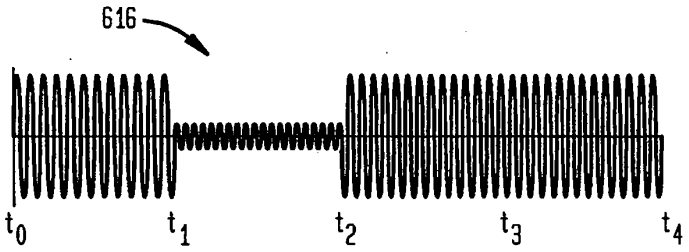


FIG. 36B

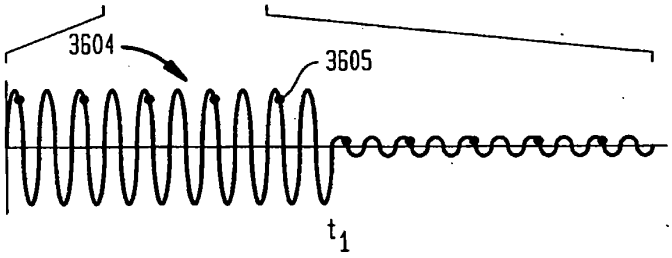


FIG. 36C

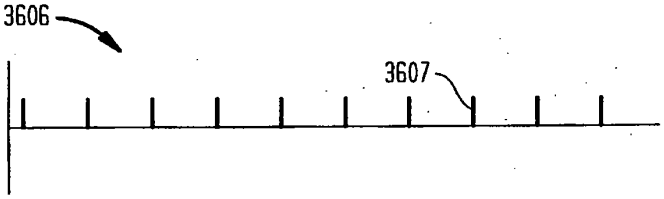


FIG. 36D

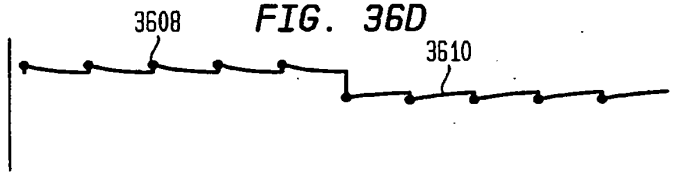


FIG. 36E

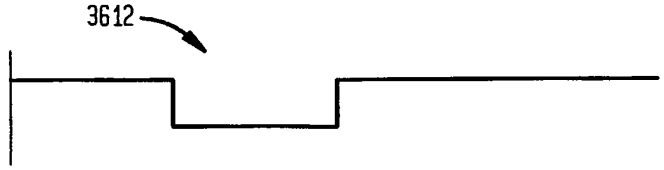


FIG. 37A

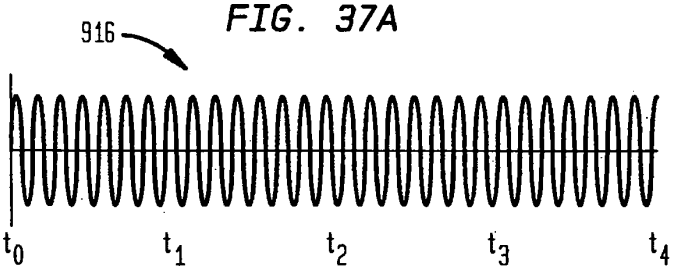


FIG. 37B

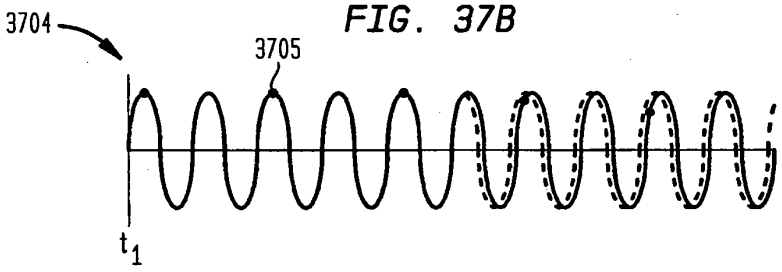


FIG. 37C

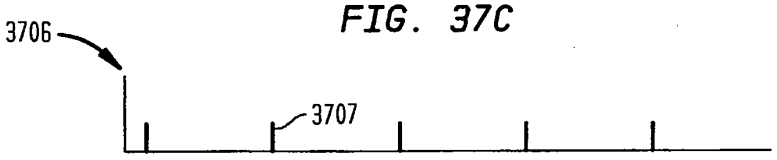


FIG. 37D

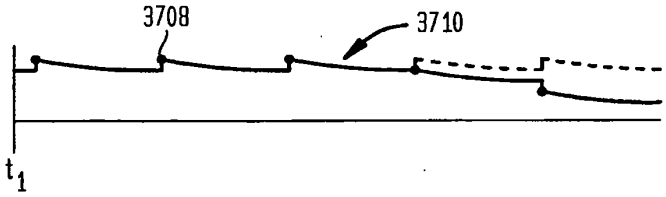


FIG. 37E

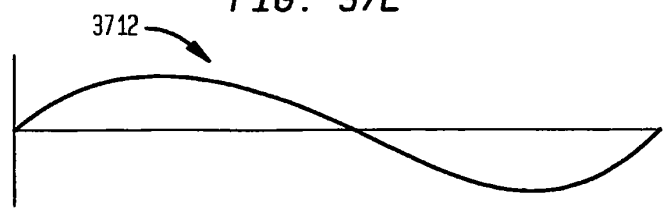


FIG. 38A

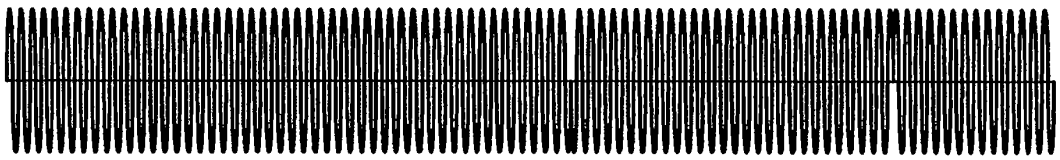


FIG. 38B

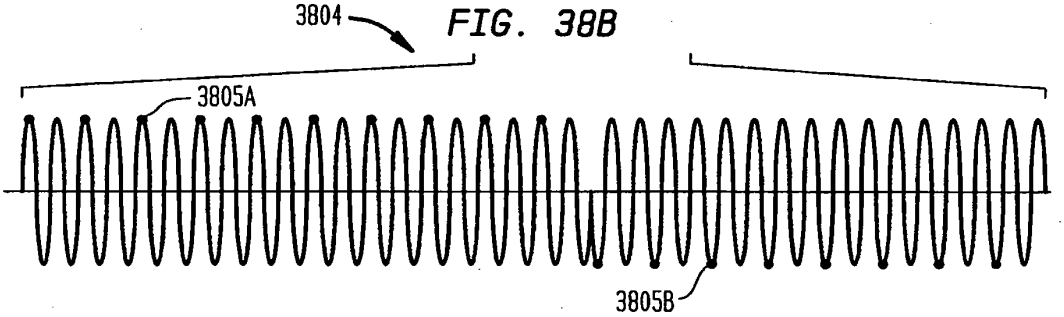


FIG. 38C

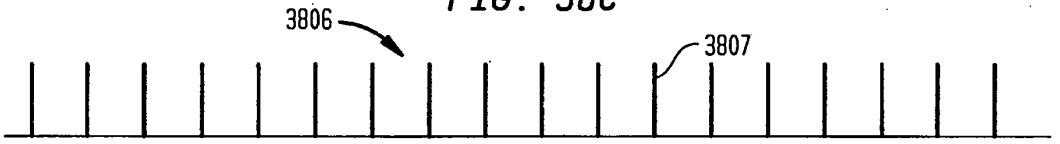


FIG. 38D

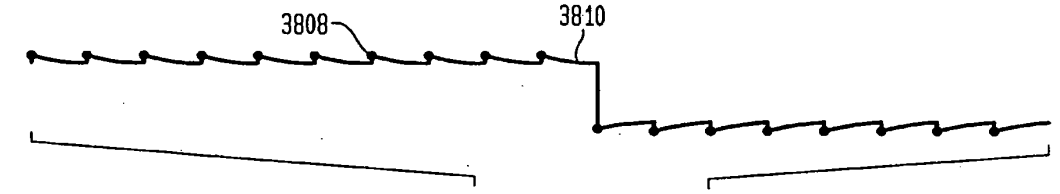


FIG. 38E

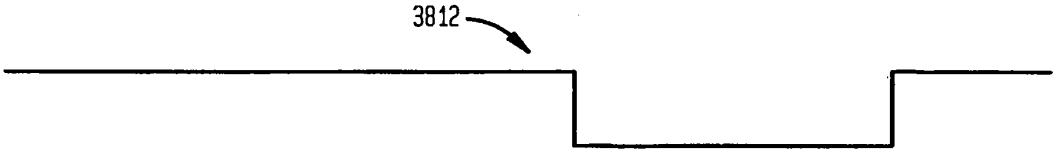


FIG. 39A

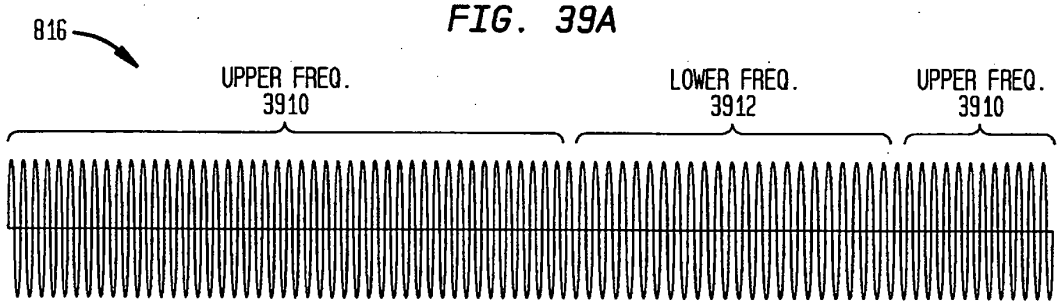


FIG. 39B

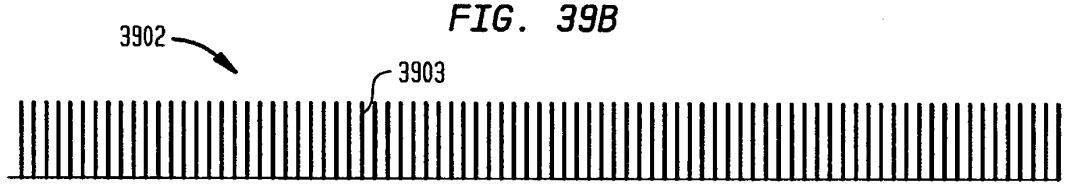


FIG. 39C



FIG. 39D

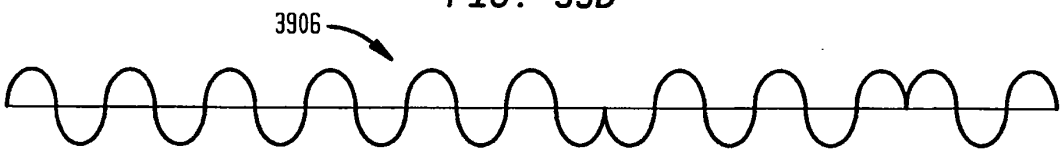


FIG. 40A

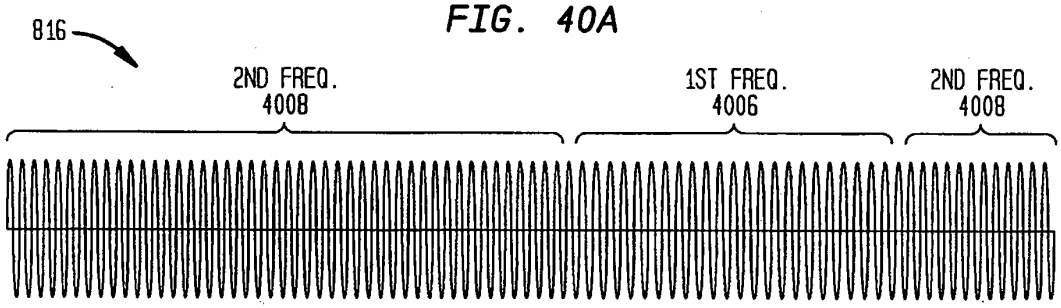


FIG. 40B

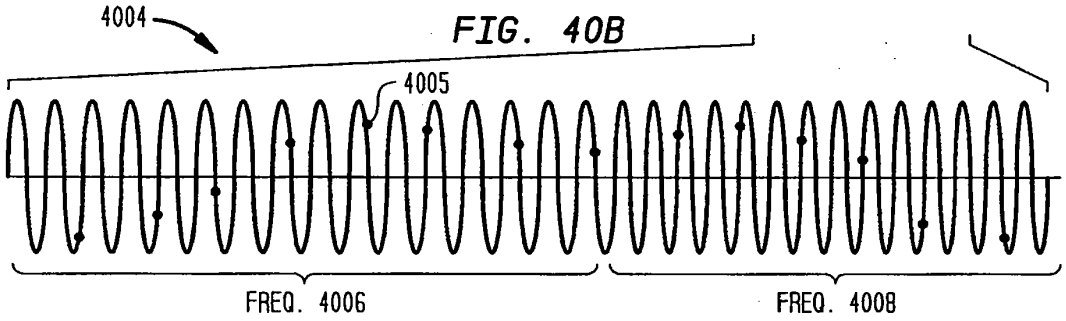


FIG. 40C

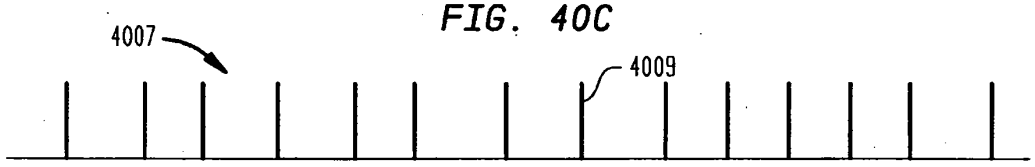


FIG. 40D

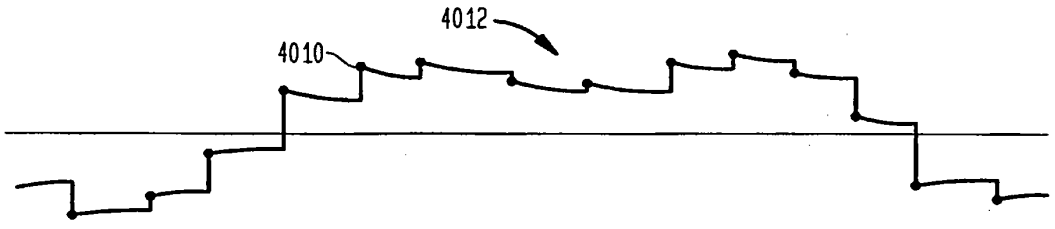
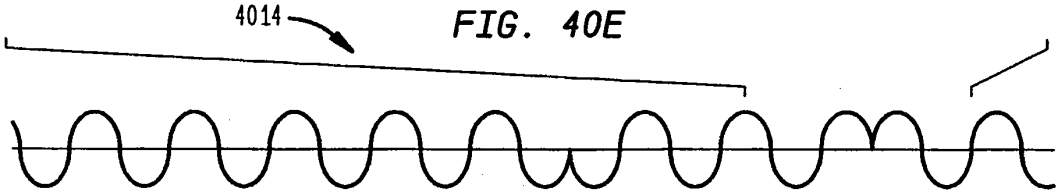


FIG. 40E



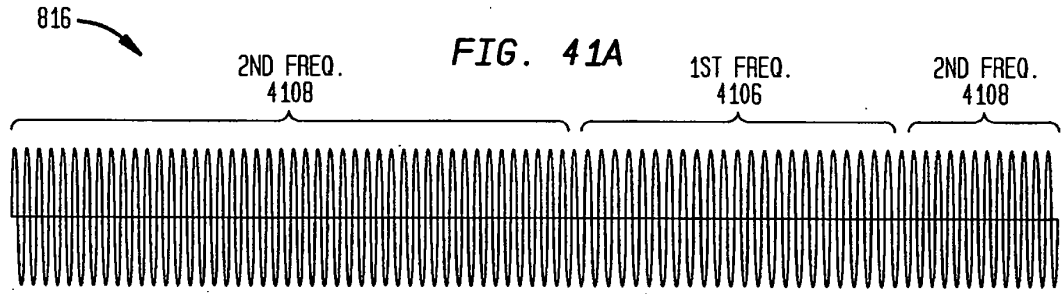


FIG. 41A

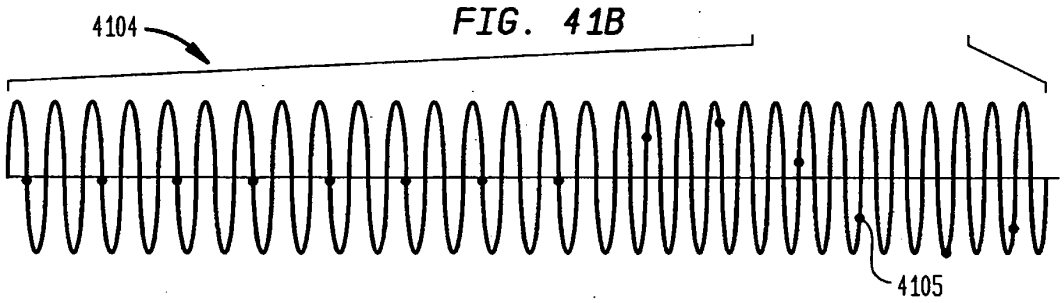


FIG. 41B

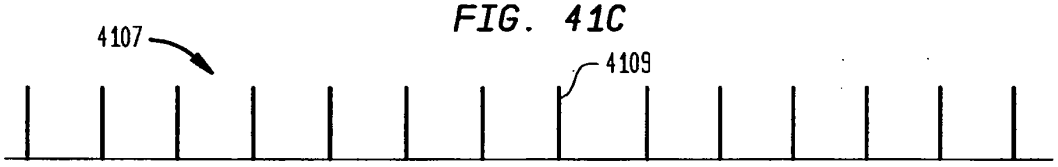


FIG. 41C

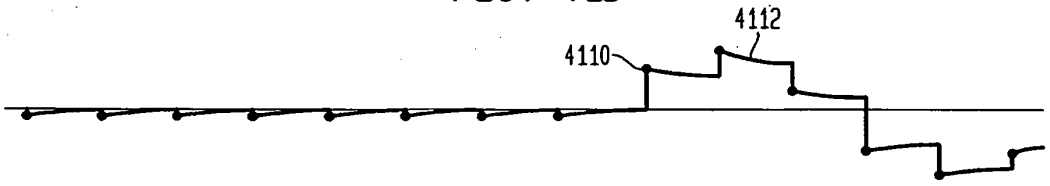


FIG. 41D

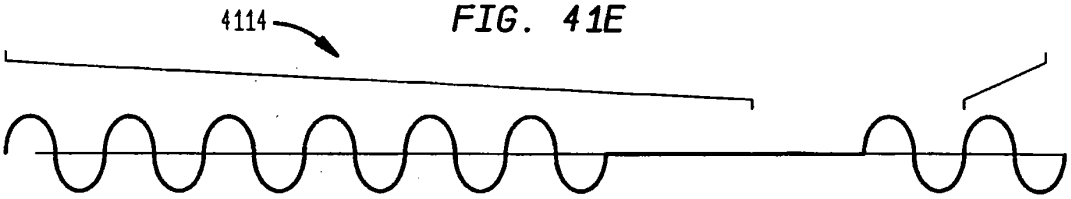


FIG. 41E

FIG. 42

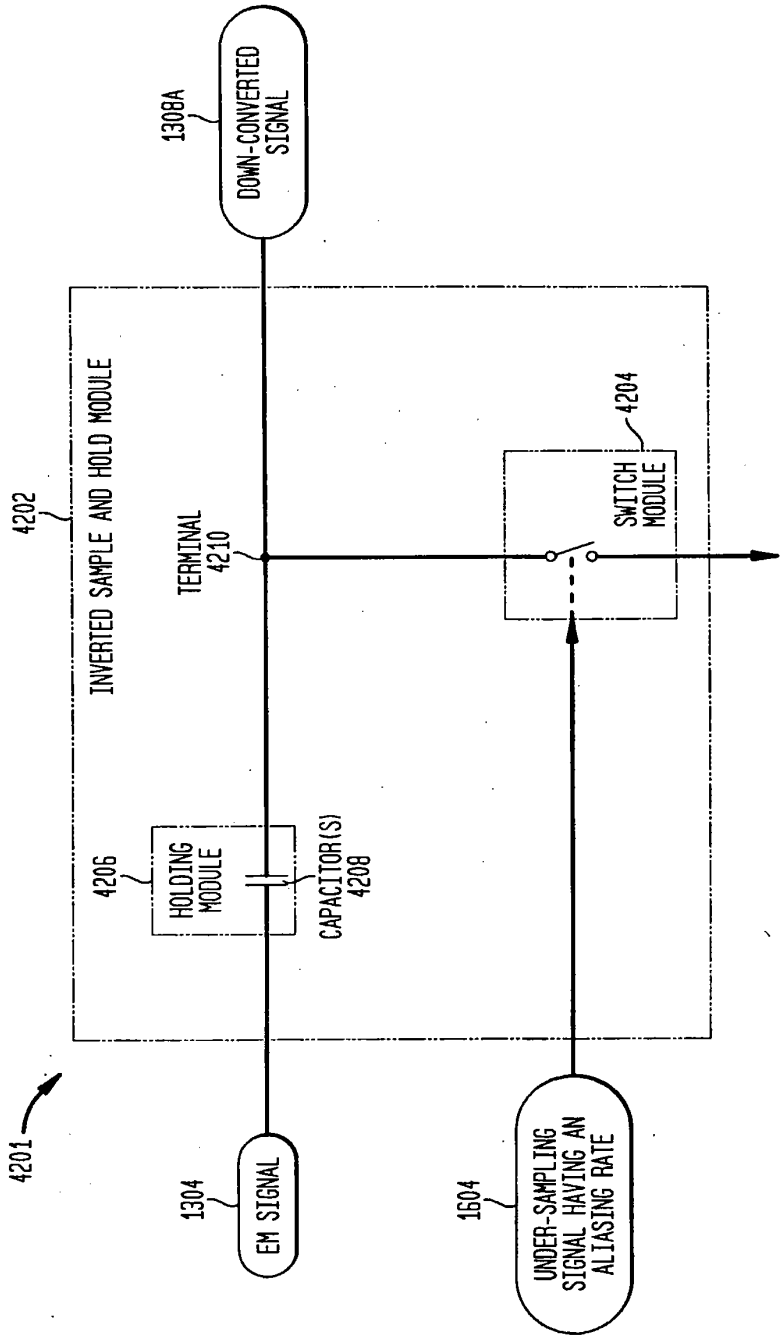

4201
1304
EM SIGNAL
1604
UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE
4202
INVERTED SAMPLE AND HOLD MODULE
1308A
DOWN-CONVERTED SIGNAL
TERMINAL 4210
4204
SWITCH MODULE
4206
HOLDING MODULE
CAPACITOR(S) 4208

FIG. 43

$$\Delta q(t) = 2 \cdot C \cdot A \cdot \sin\left(\frac{1}{2} \cdot T\right) \cdot \cos\left(t - \frac{1}{2} \cdot T\right)$$

793

FIG. 44A
DIFFERENTIAL CONFIGURATION

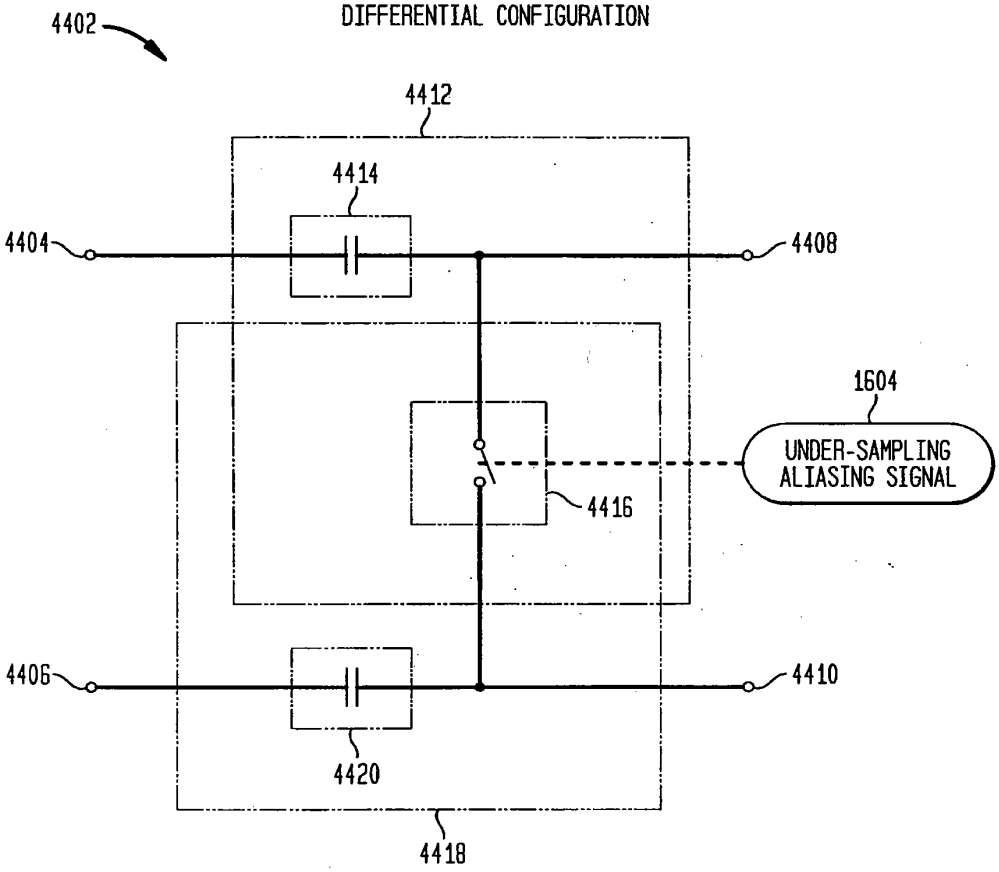


FIG. 44B

DIFFERENTIAL INPUT TO DIFFERENTIAL OUTPUT

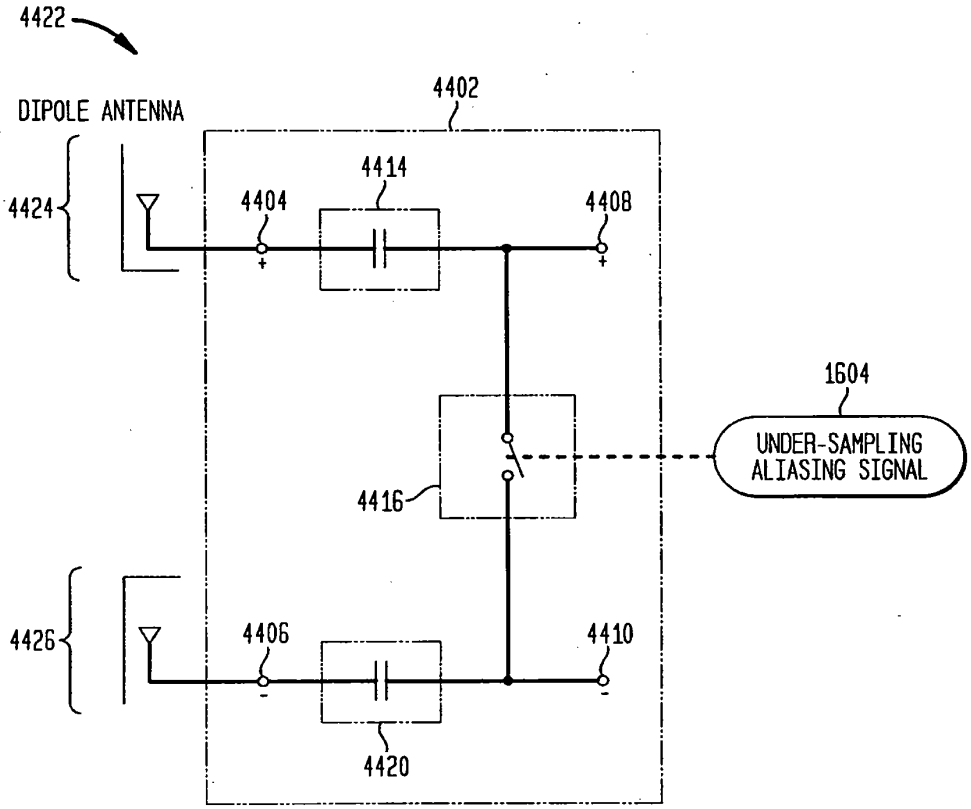


FIG. 44C

SINGLE INPUT TO DIFFERENTIAL OUTPUT

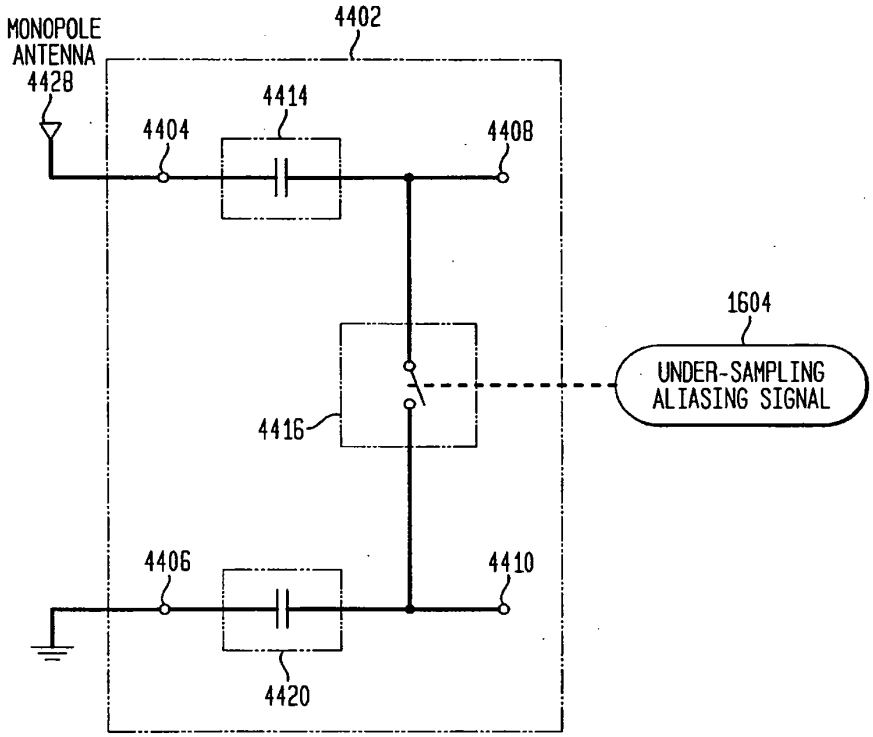


FIG. 44D

DIFFERENTIAL INPUT TO SINGLE OUTPUT

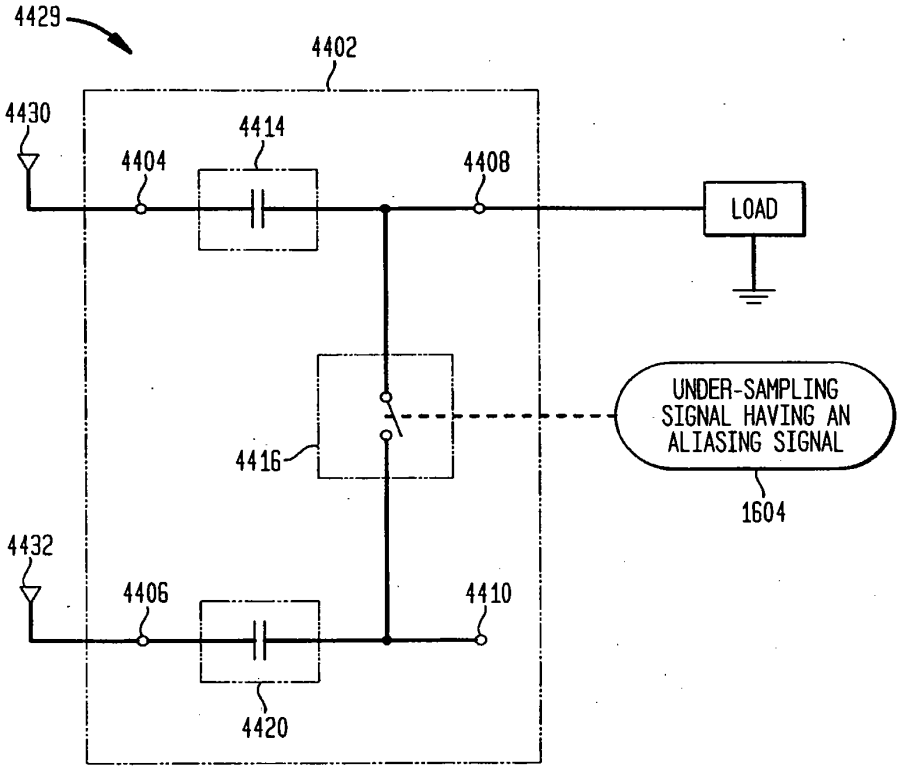


FIG. 44E

EXAMPLE INPUT/OUTPUT CIRCUITRY

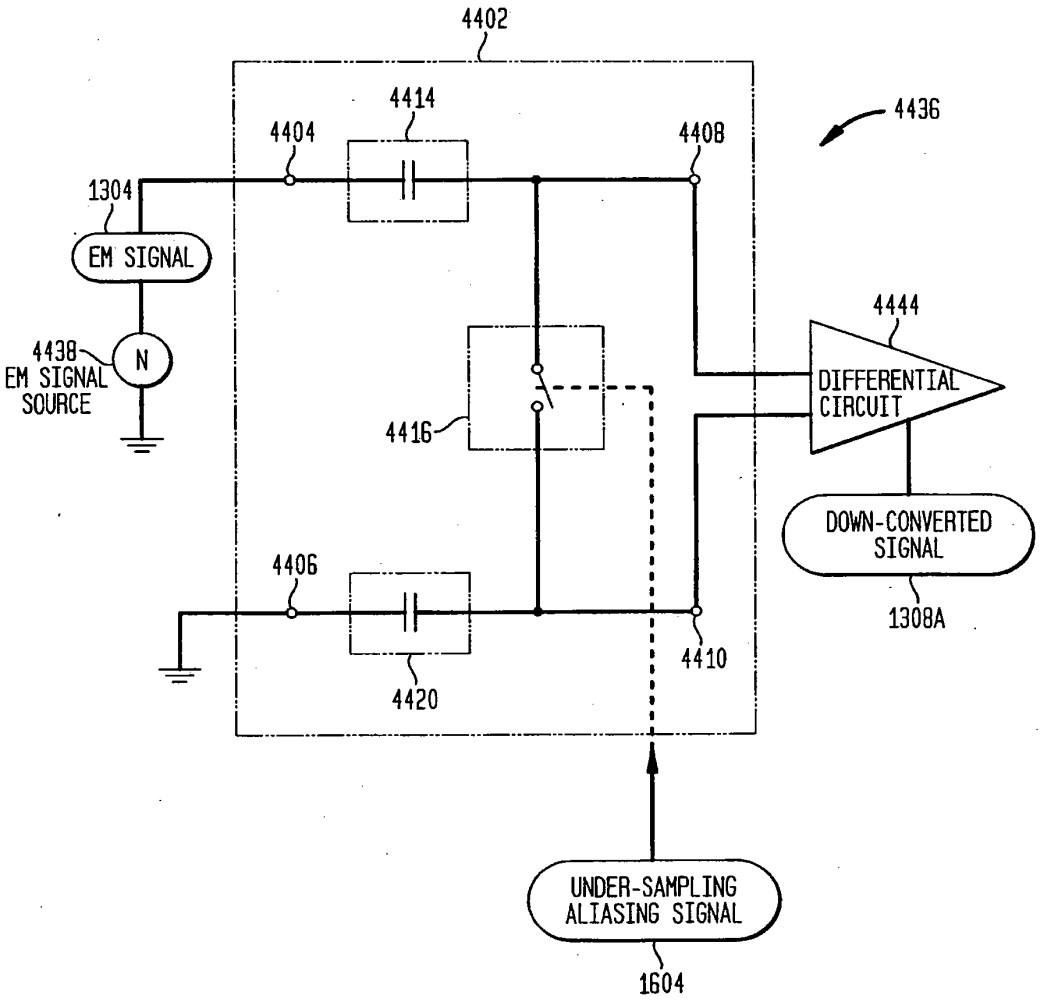


FIG. 45A

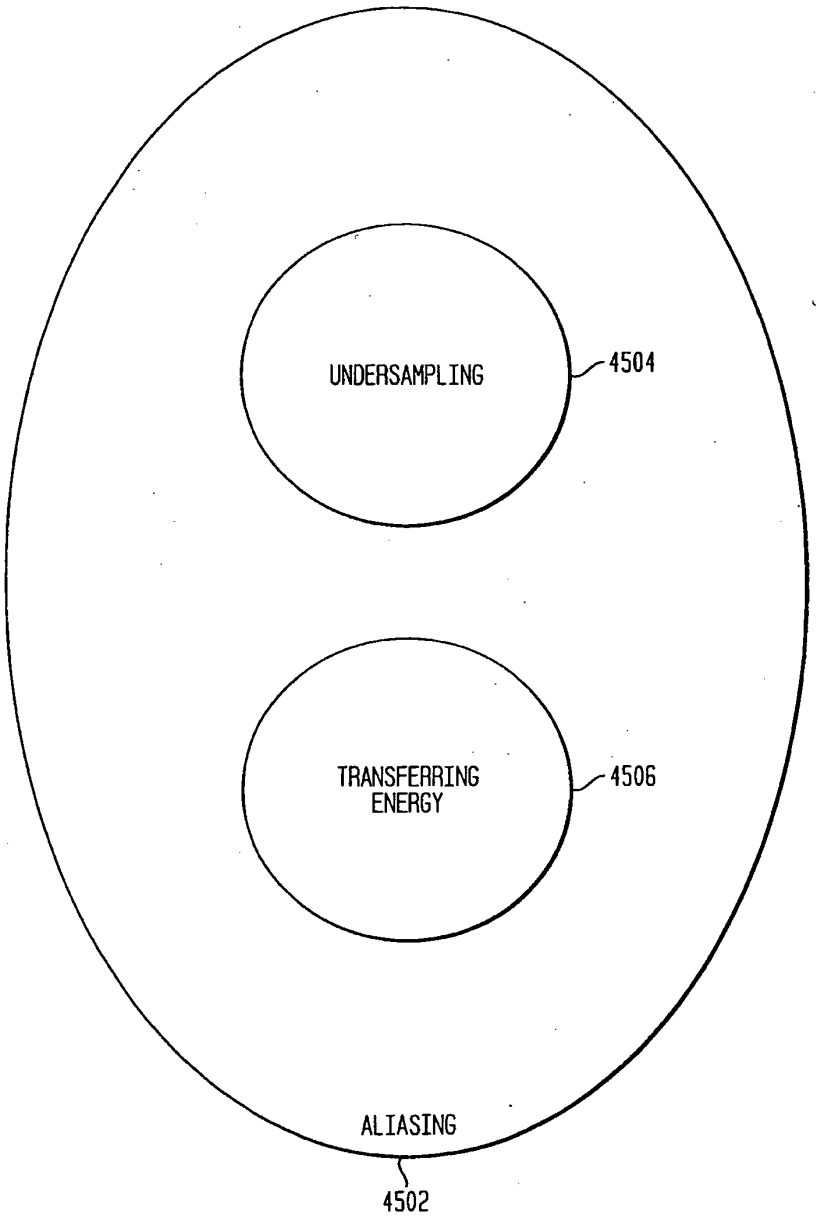

UNDERSAMPLING
4504
TRANSFERRING ENERGY
4506
ALIASING
4502

FIG. 45B

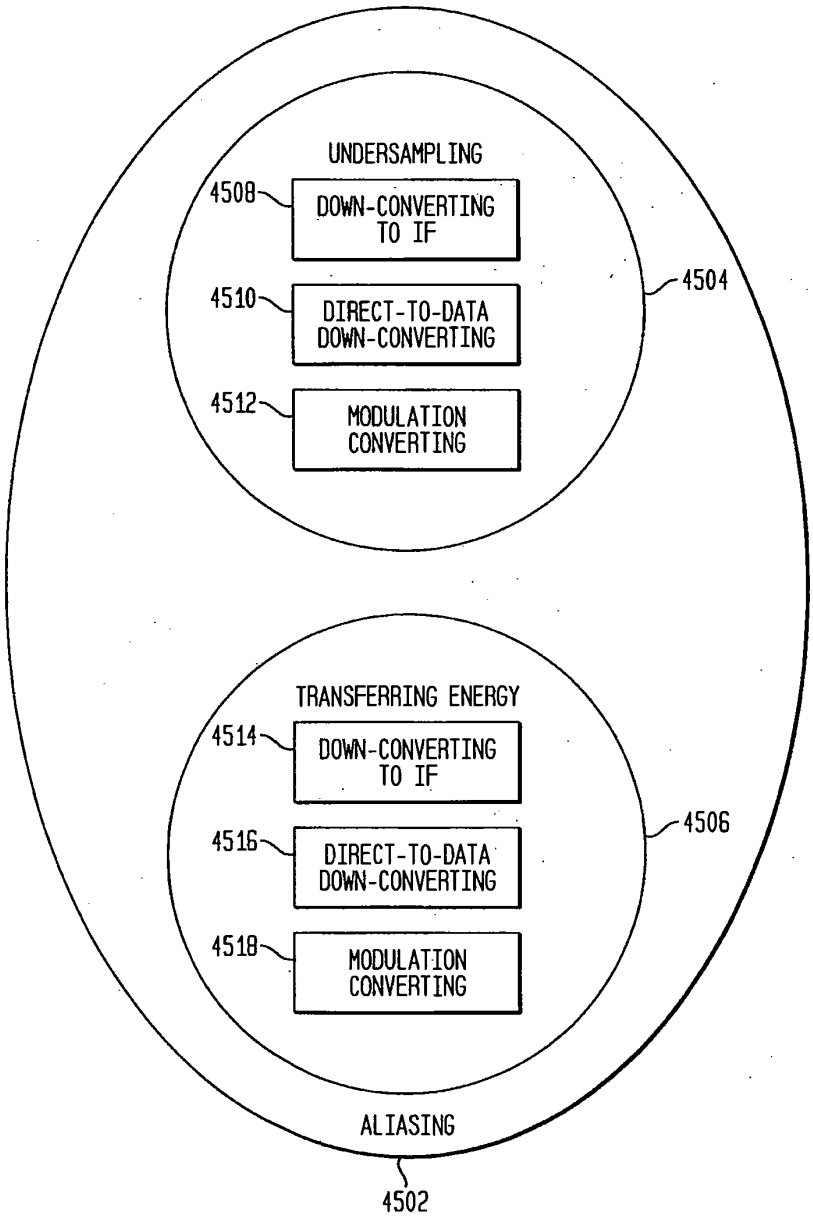

UNDERSAMPLING
4508
DOWN-CONVERTING TO IF
4510
DIRECT-TO-DATA DOWN-CONVERTING
4512
MODULATION CONVERTING
4504
TRANSFERRING ENERGY
4514
DOWN-CONVERTING TO IF
4516
DIRECT-TO-DATA DOWN-CONVERTING
4518
MODULATION CONVERTING
4506
ALIASING
4502

FIG. 46A

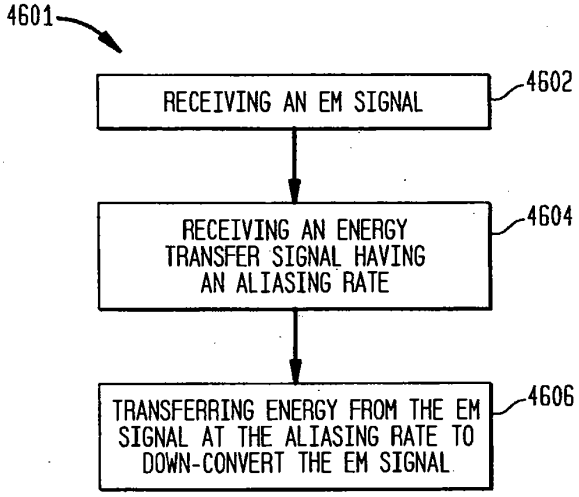


FIG. 46B

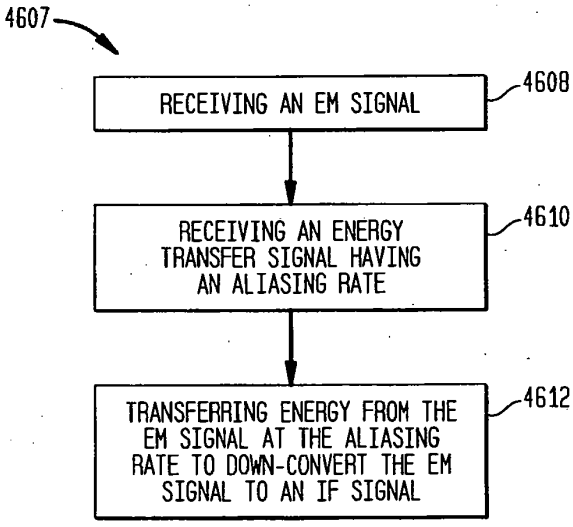


FIG. 46C

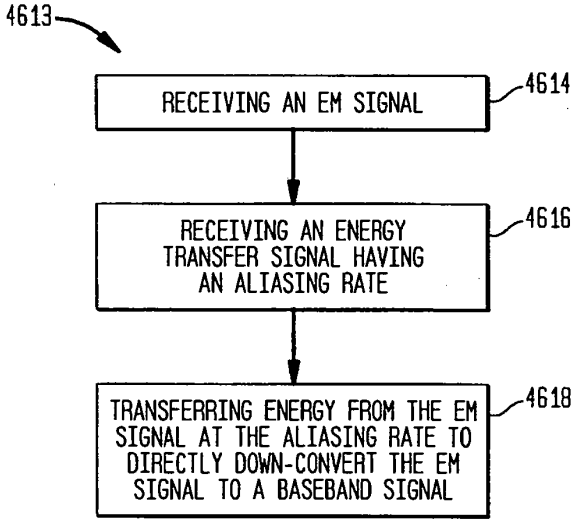


FIG. 46D

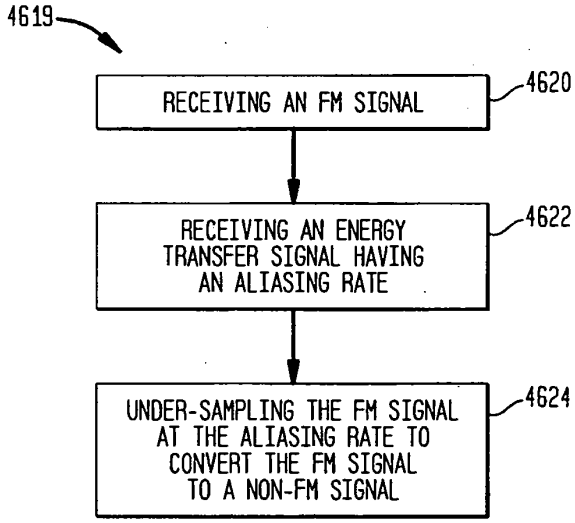


FIG. 47E

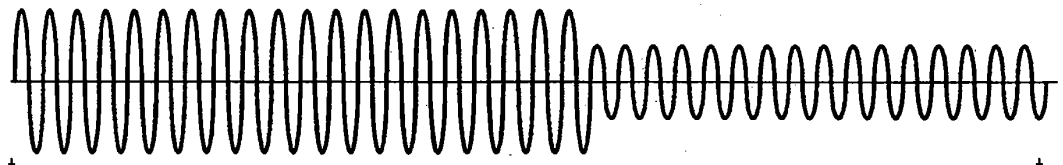


FIG. 47A

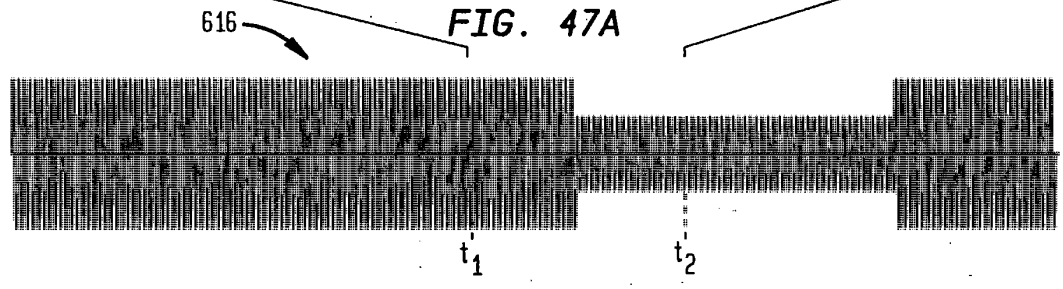


FIG. 47B

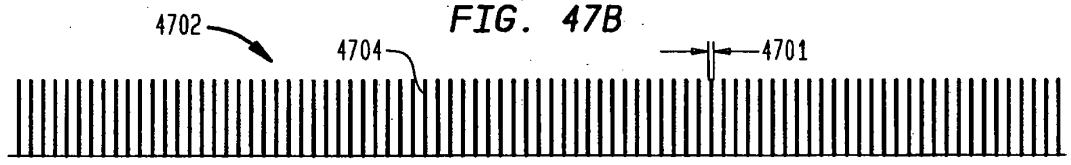


FIG. 47C

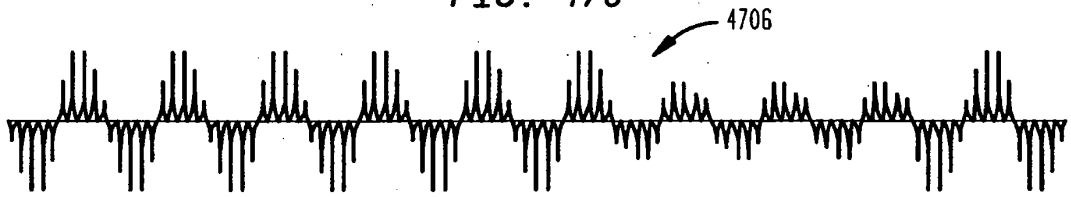


FIG. 47D

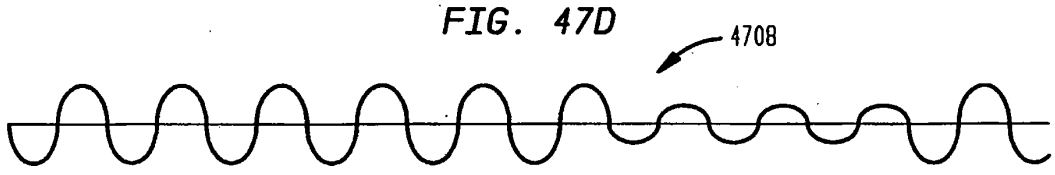


FIG. 48

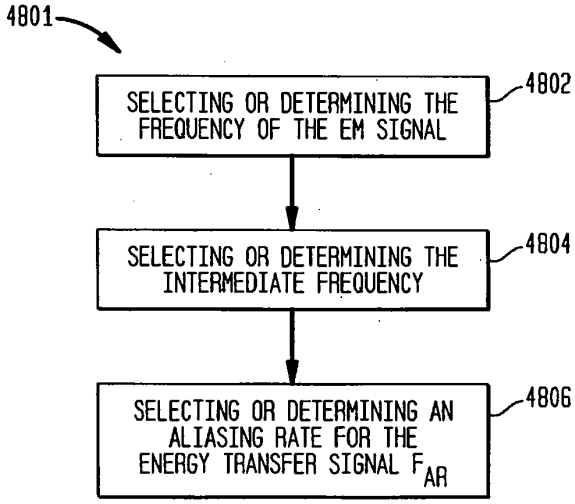

4801
SELECTING OR DETERMINING THE FREQUENCY OF THE EM SIGNAL
4802
SELECTING OR DETERMINING THE INTERMEDIATE FREQUENCY
4804
SELECTING OR DETERMINING AN ALIASING RATE FOR THE ENERGY TRANSFER SIGNAL F_{AR}
4806

FIG. 49A

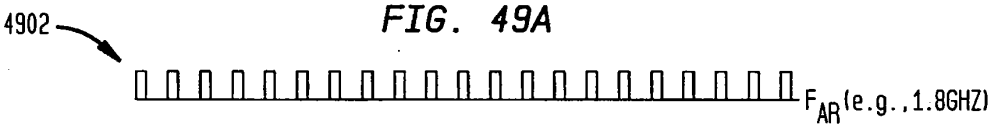


FIG. 49B

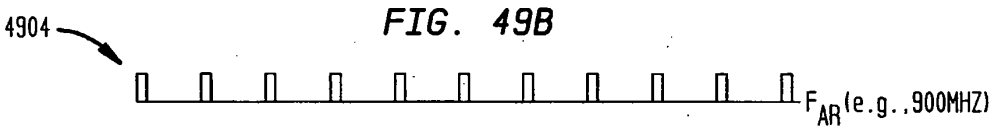


FIG. 49C

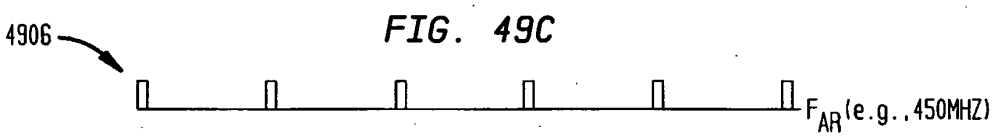


FIG. 49D

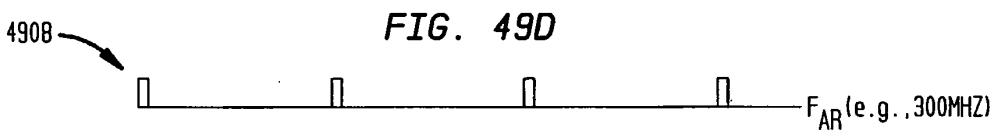


FIG. 49E

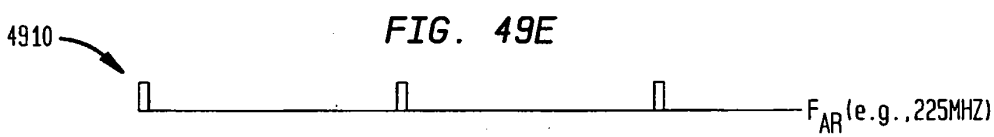


FIG. 49F

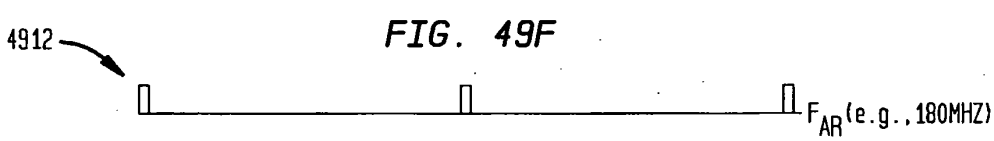


FIG. 49G

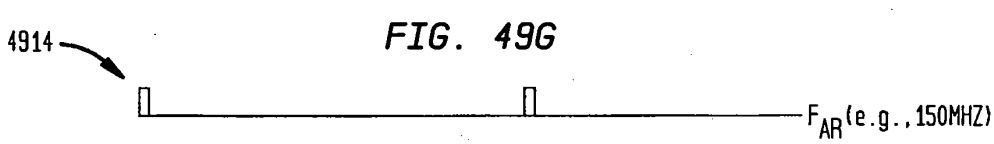
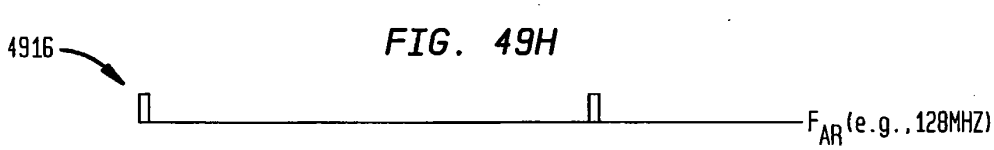


FIG. 49H



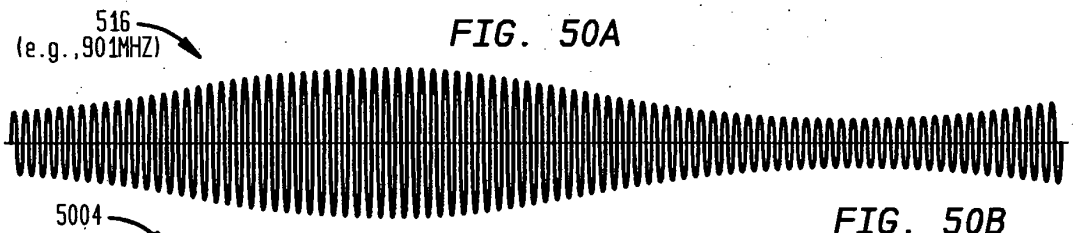


FIG. 50A

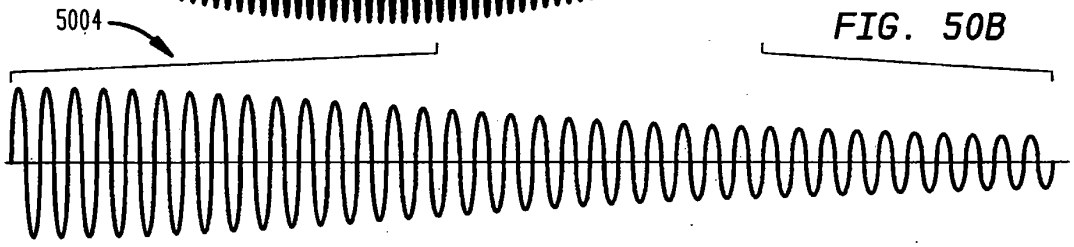


FIG. 50B

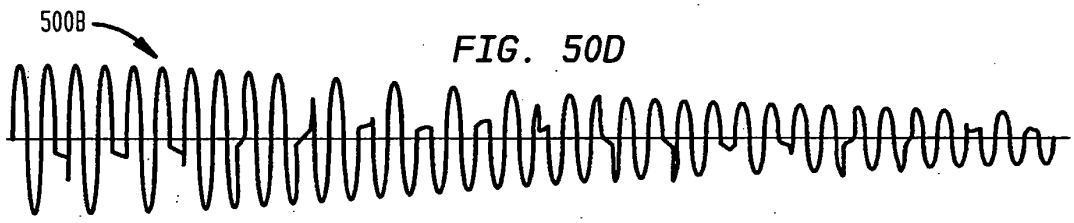


FIG. 50D

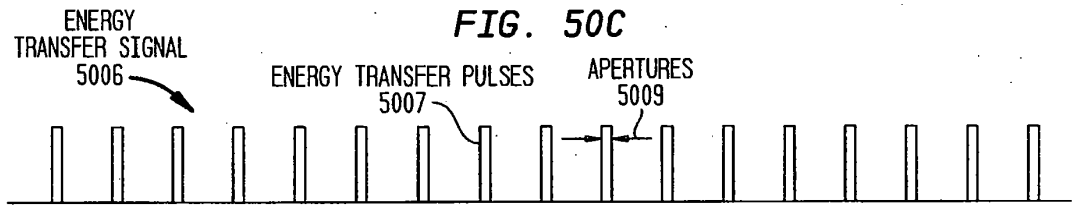


FIG. 50C

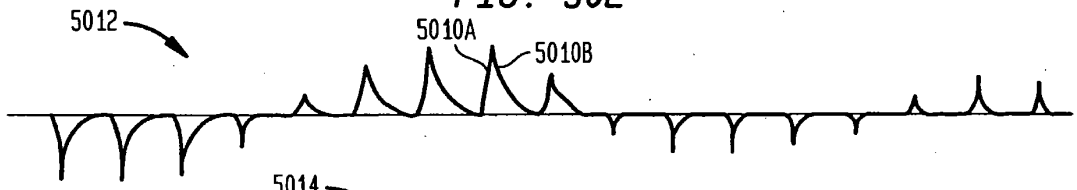


FIG. 50E

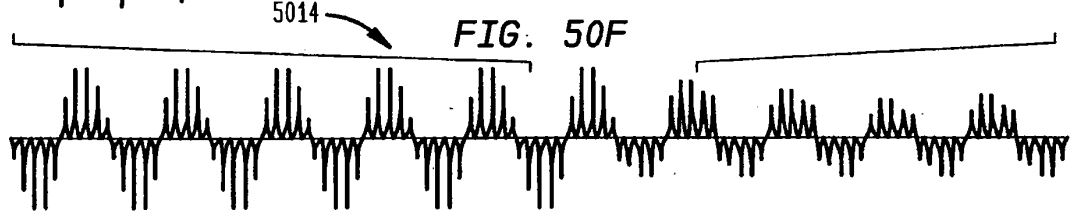


FIG. 50F

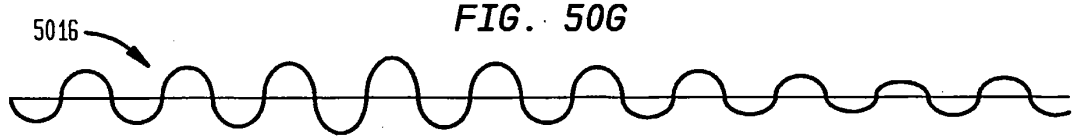


FIG. 50G

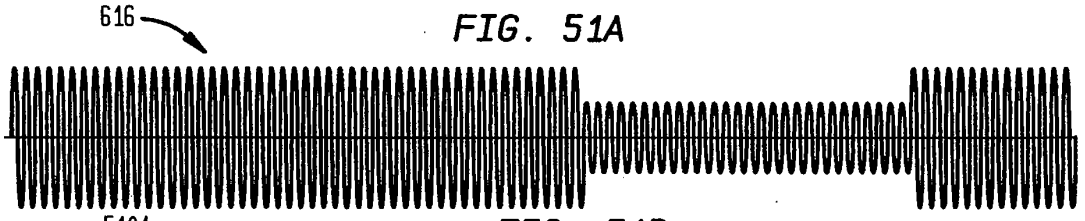


FIG. 51A

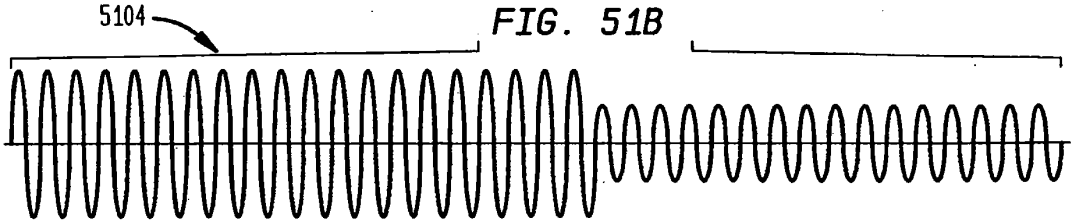


FIG. 51B

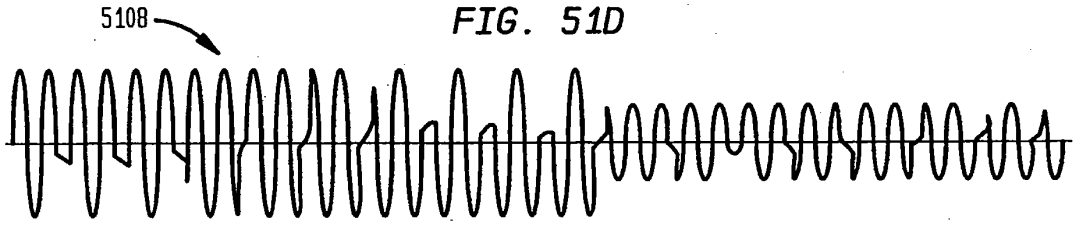


FIG. 51D

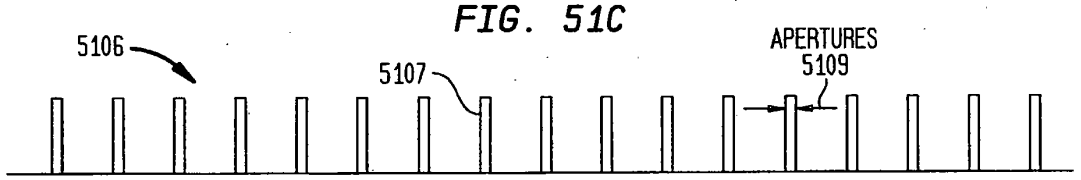


FIG. 51C

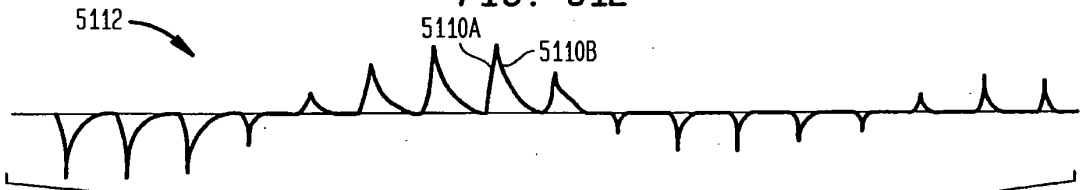


FIG. 51E

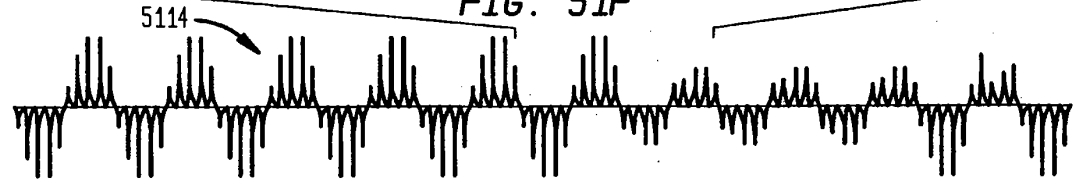


FIG. 51F

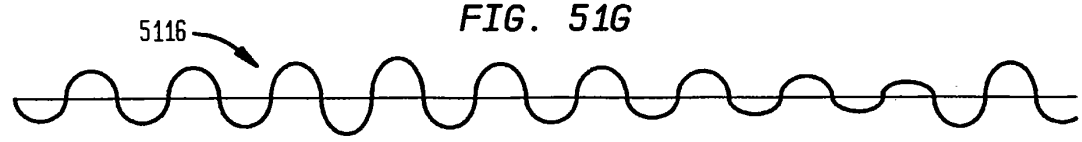


FIG. 51G

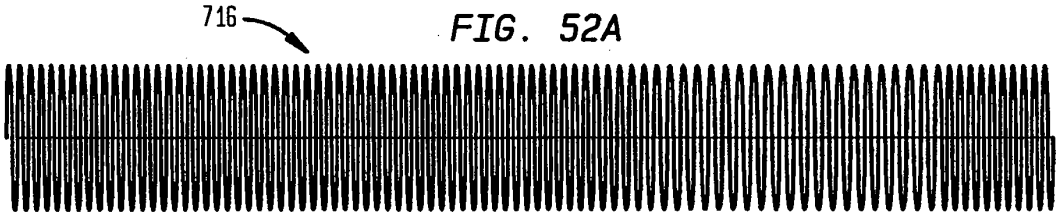


FIG. 52A

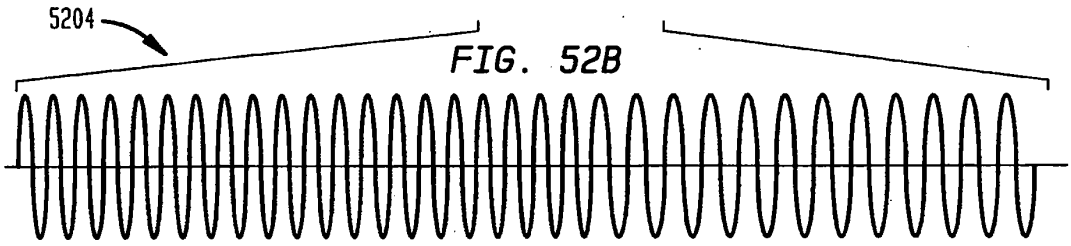


FIG. 52B

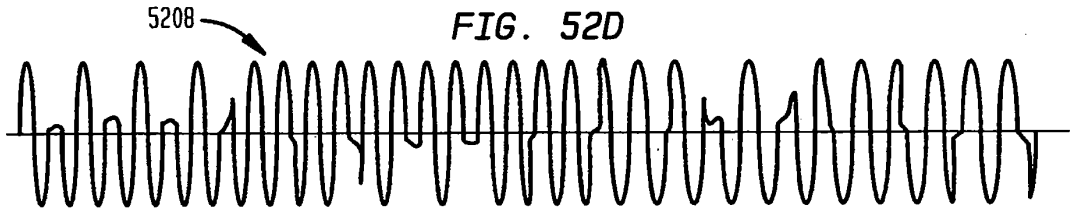


FIG. 52D

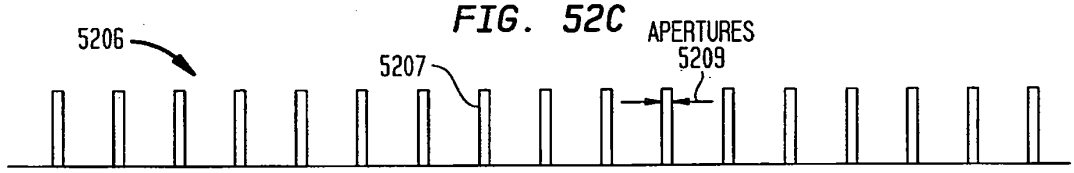


FIG. 52C

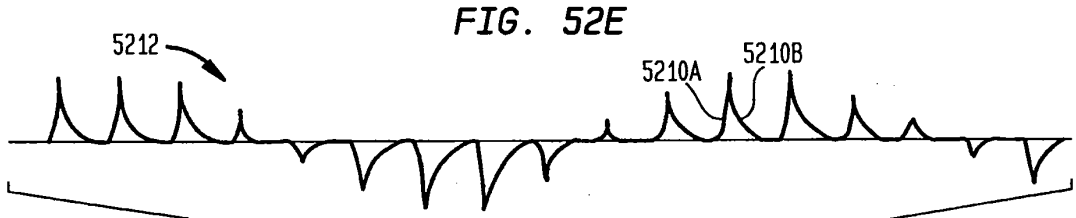


FIG. 52E

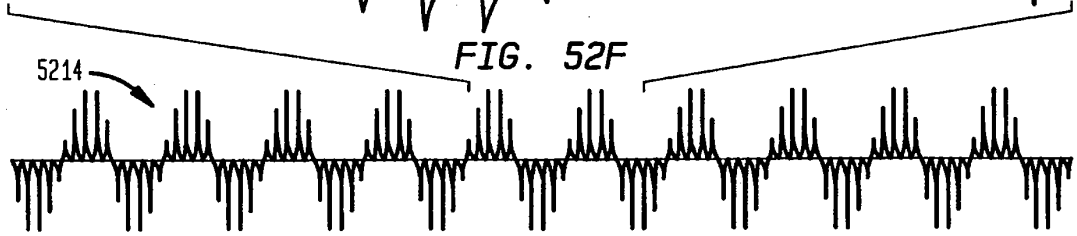


FIG. 52F

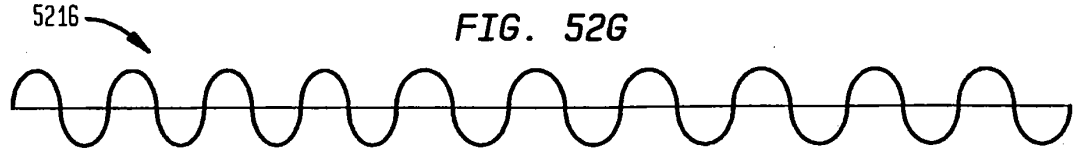
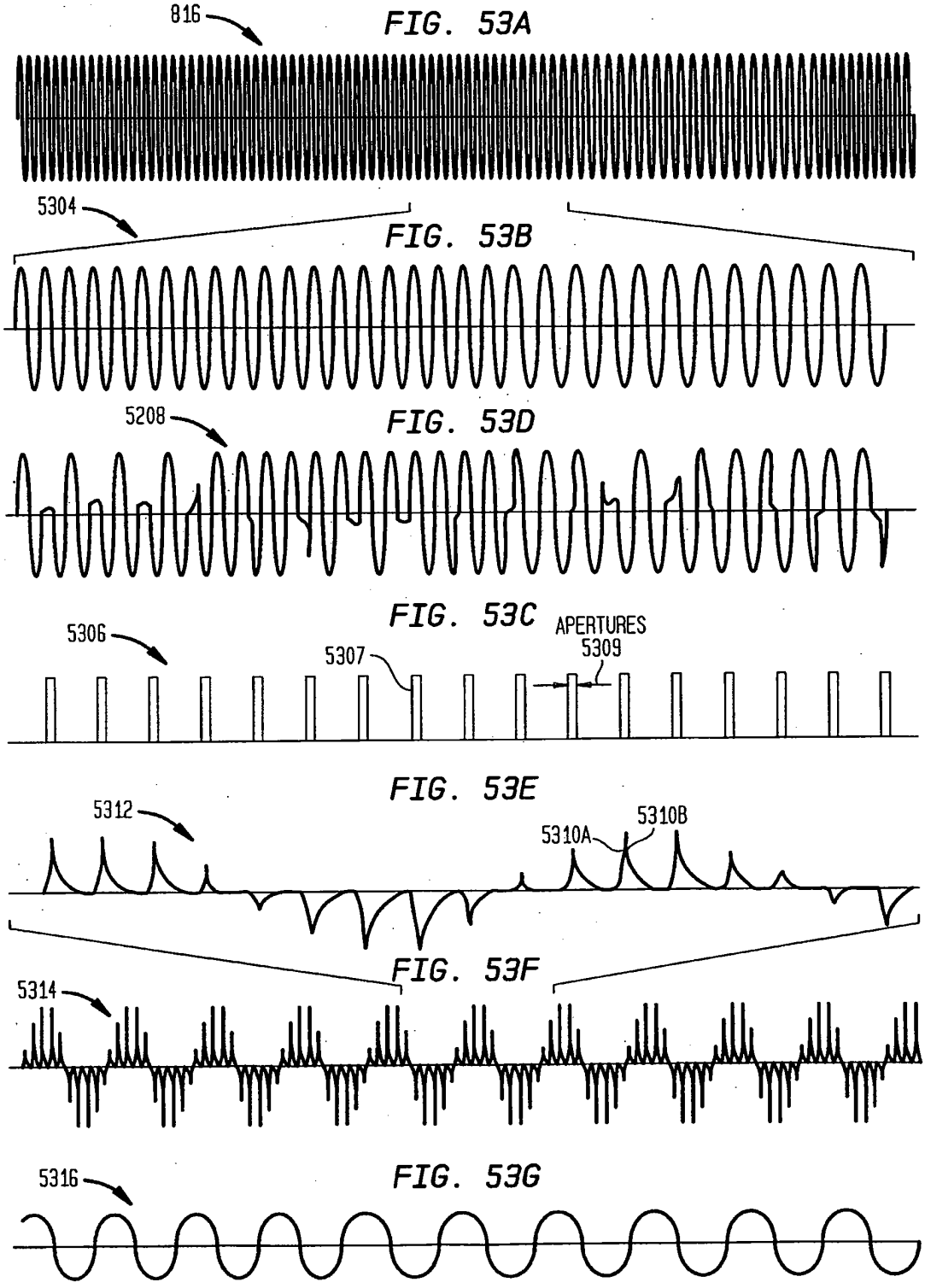


FIG. 52G


816
FIG. 53A
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FIG. 53B
5208
FIG. 53D
FIG. 53C
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FIG. 53E
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5310A
5310B
FIG. 53F
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FIG. 53G

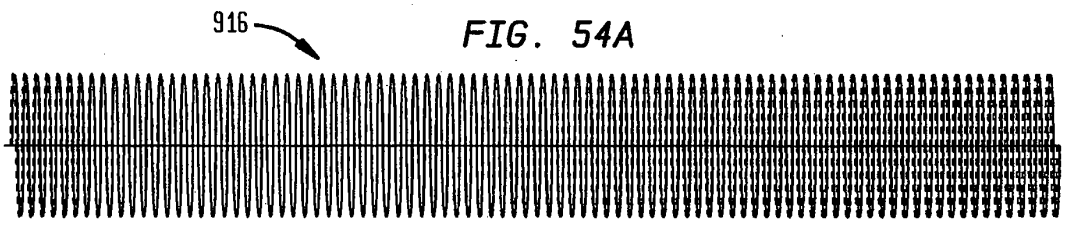


FIG. 54A

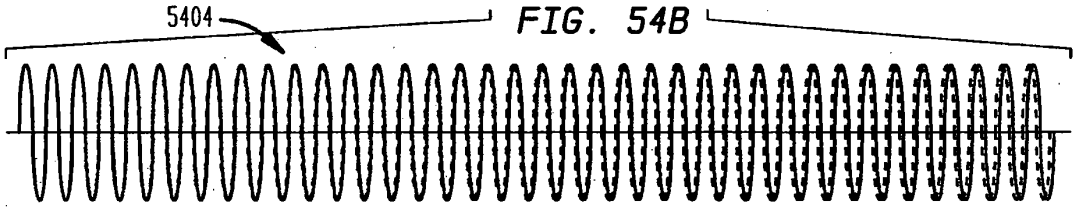


FIG. 54B

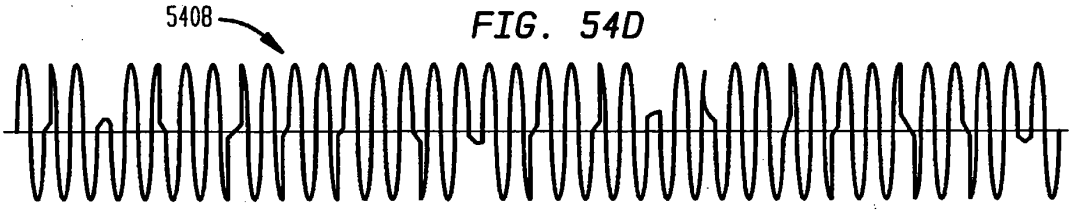


FIG. 54D

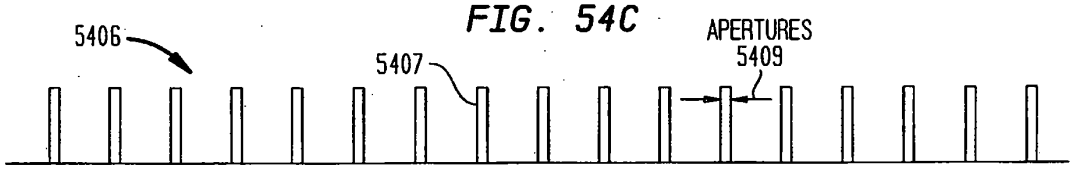


FIG. 54C

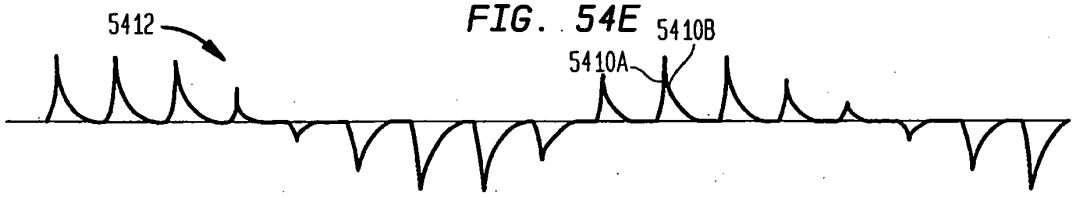


FIG. 54E

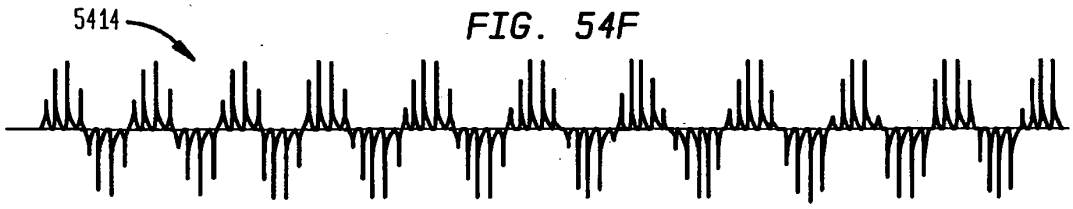


FIG. 54F

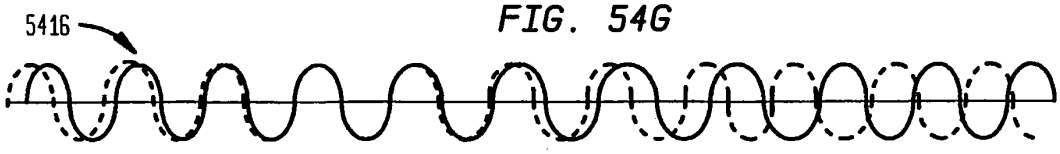


FIG. 54G

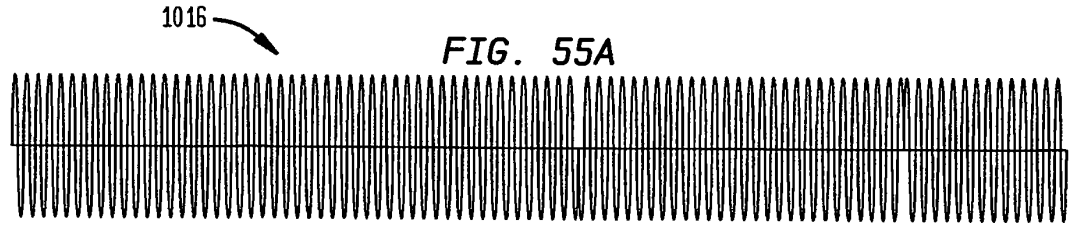


FIG. 55A

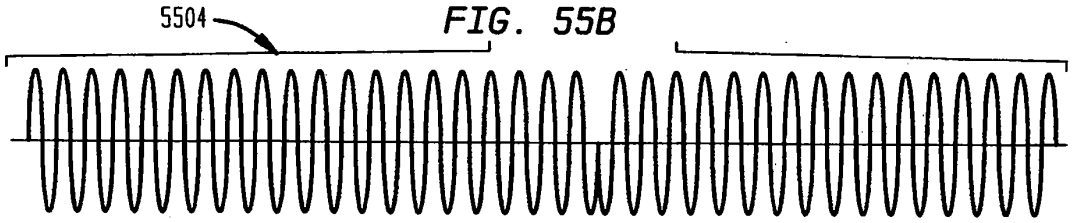


FIG. 55B

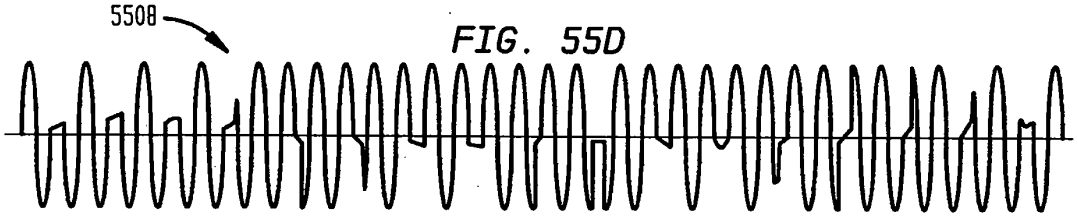


FIG. 55D

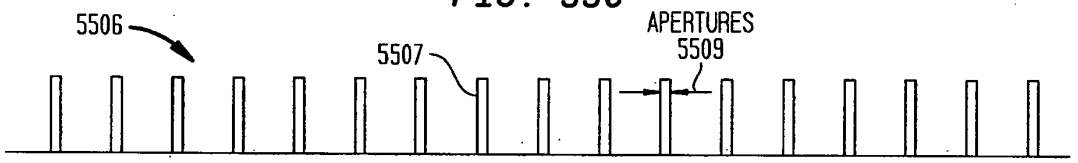


FIG. 55C

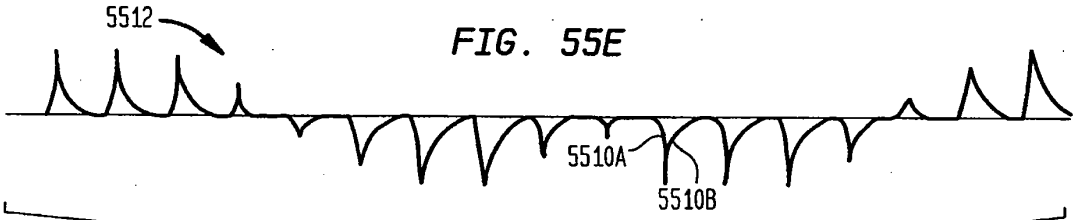


FIG. 55E

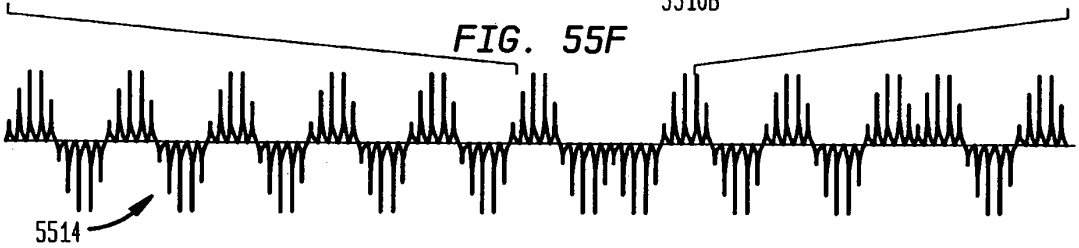


FIG. 55F

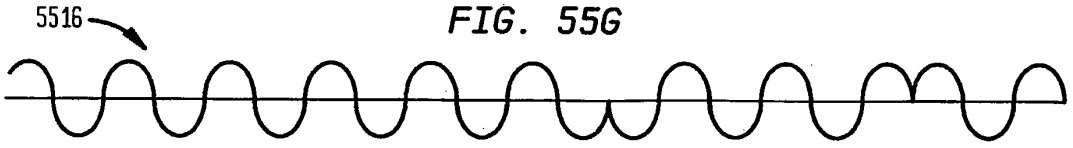


FIG. 55G

FIG. 56A

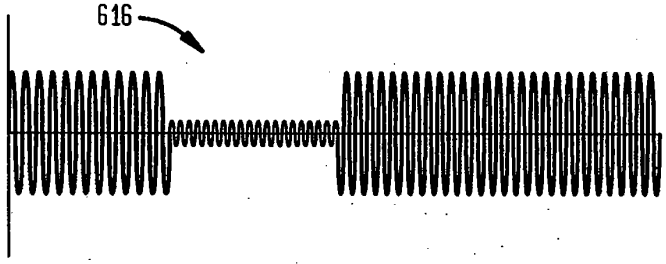


FIG. 56B

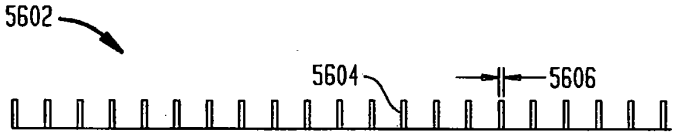


FIG. 56C

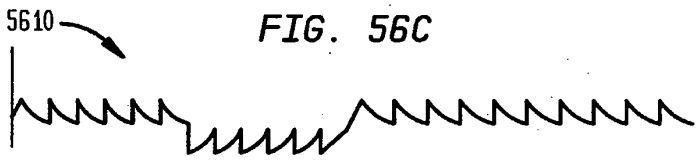


FIG. 56D

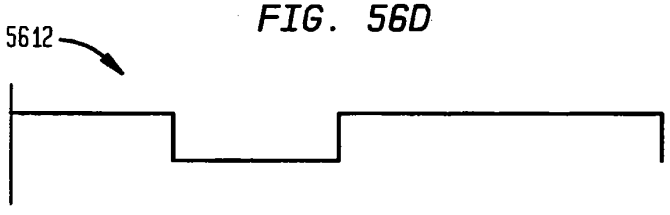
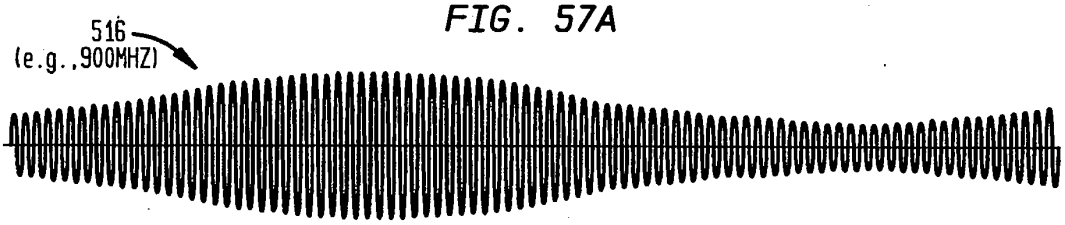


FIG. 57A



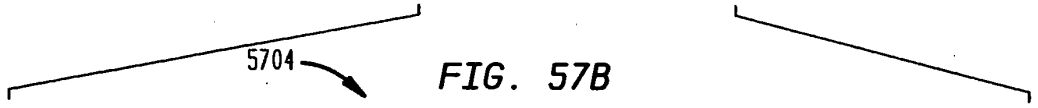


FIG. 57B

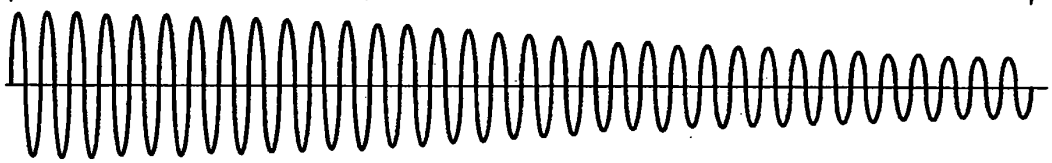


FIG. 57D

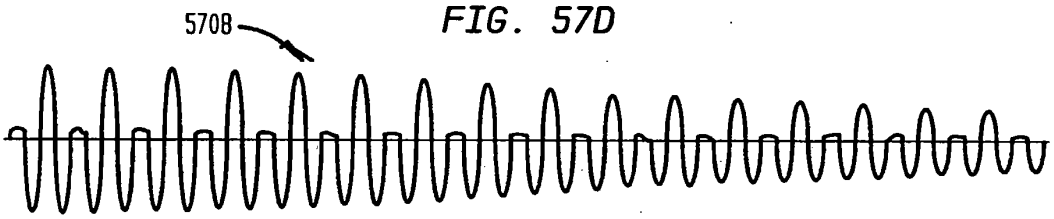


FIG. 57C

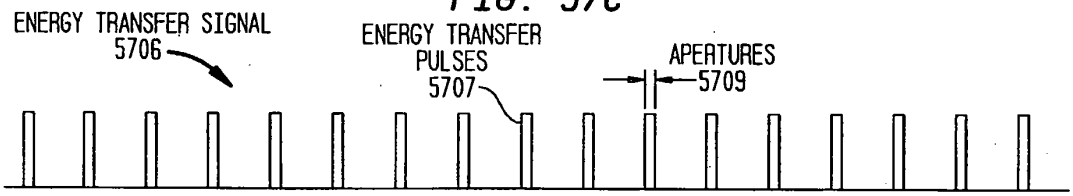
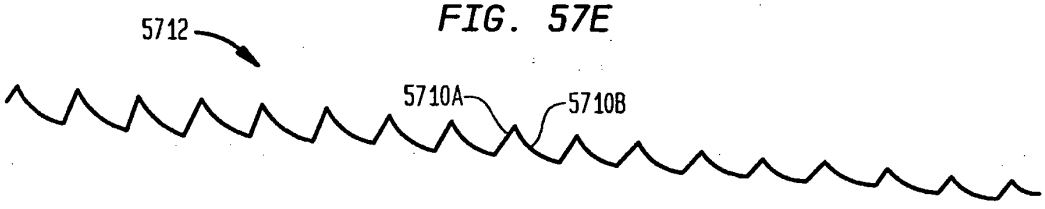


FIG. 57E



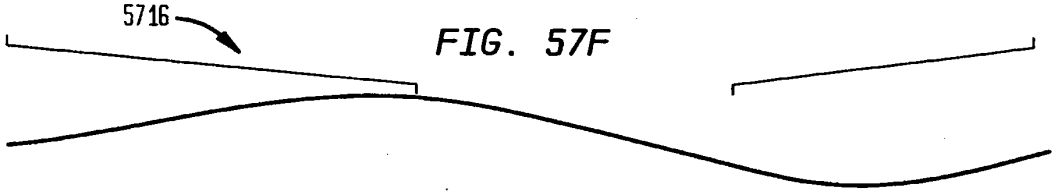


FIG. 57F

FIG. 58A

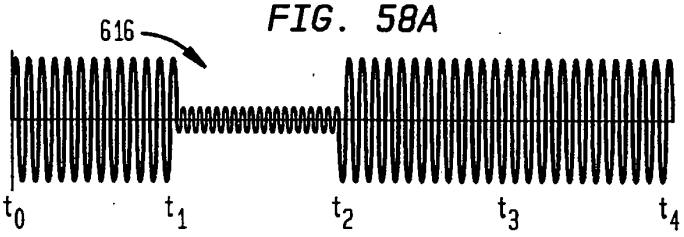


FIG. 58B

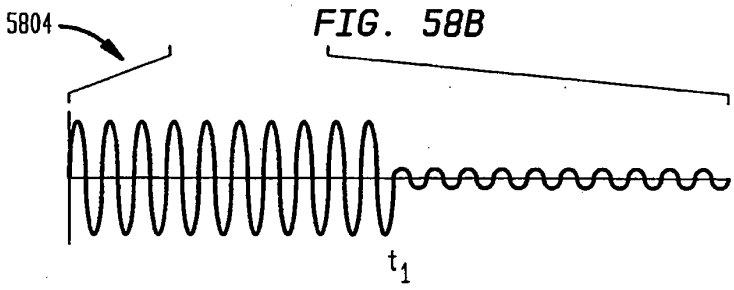


FIG. 58D

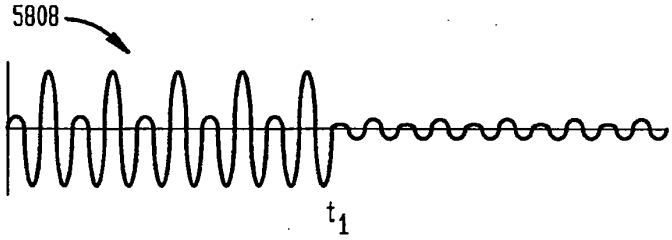


FIG. 58C

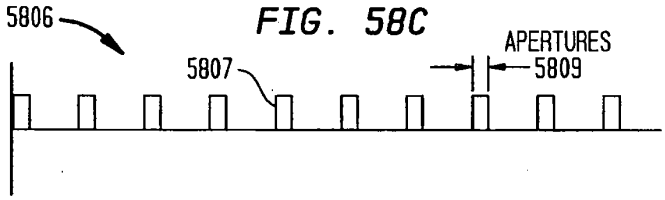


FIG. 58E

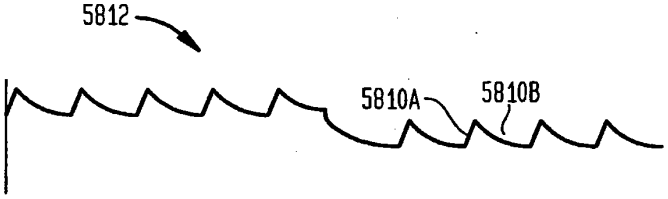


FIG. 58F

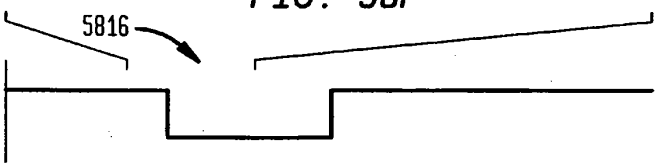
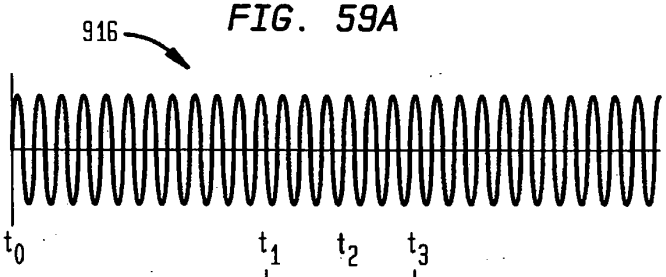


FIG. 59A



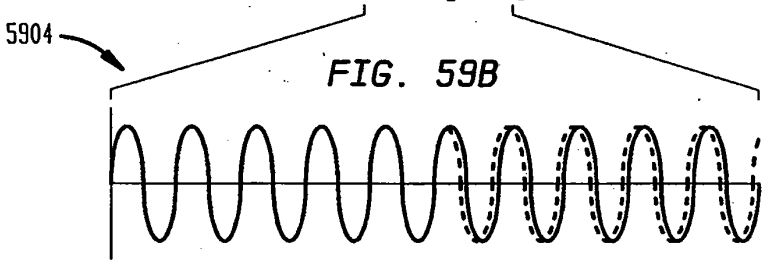


FIG. 59B

FIG. 59D

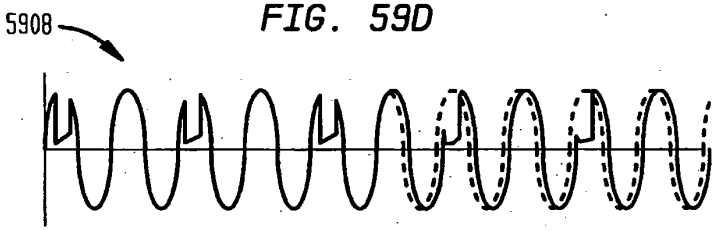


FIG. 59C

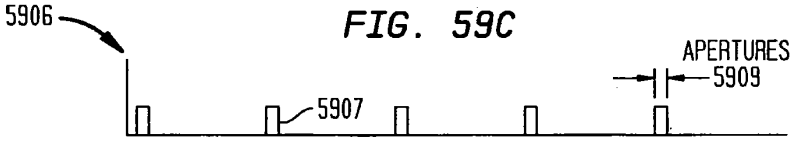
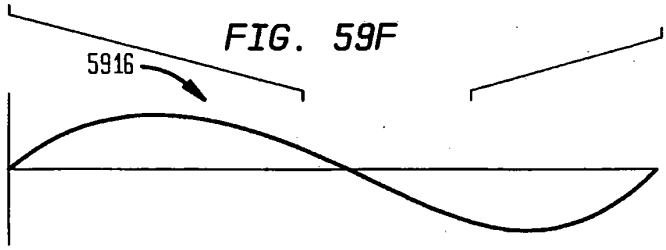


FIG. 59E



FIG. 59F



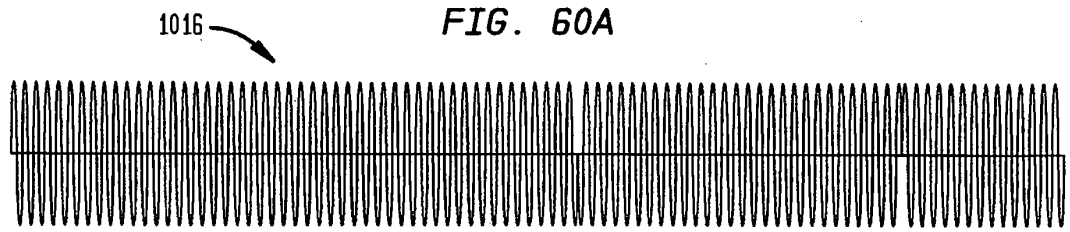


FIG. 60A

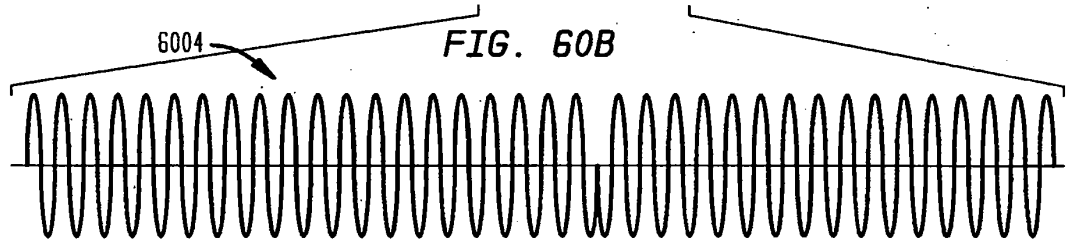


FIG. 60B

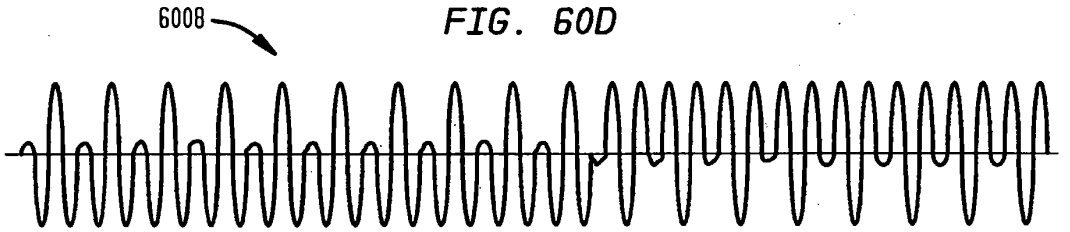


FIG. 60D

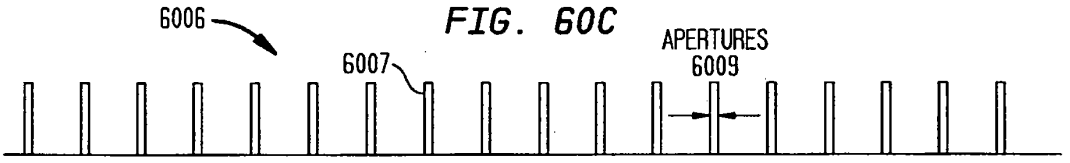


FIG. 60C



FIG. 60E

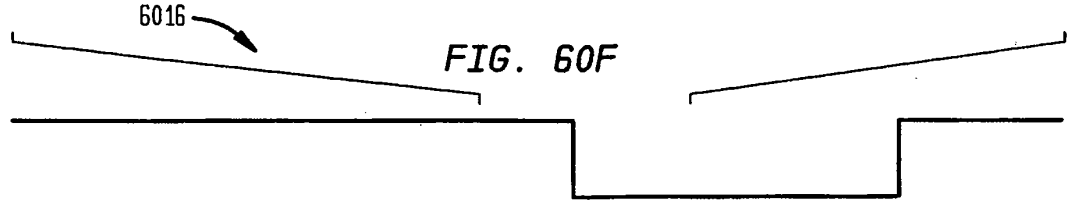


FIG. 60F

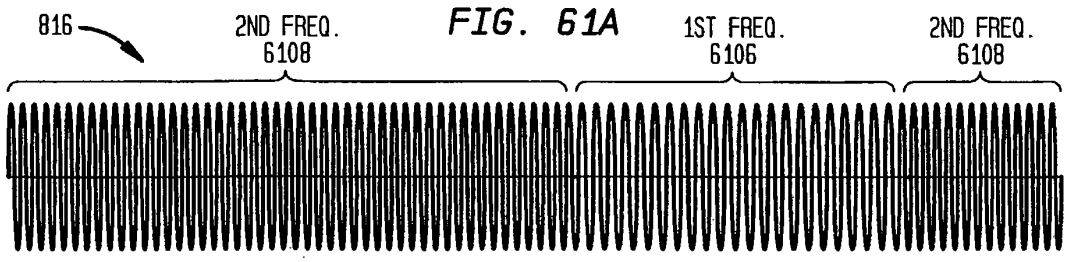


FIG. 61A

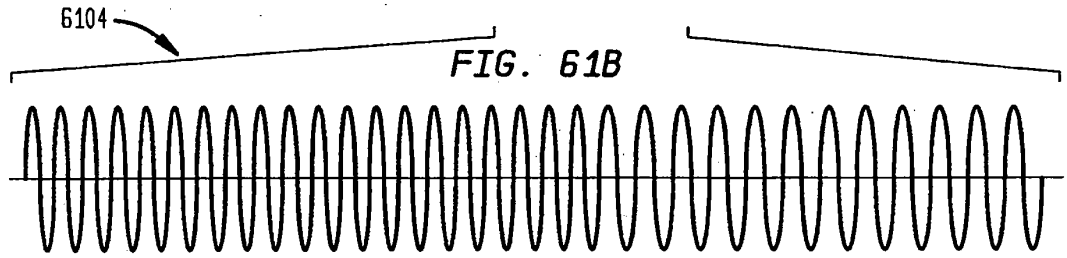


FIG. 61B

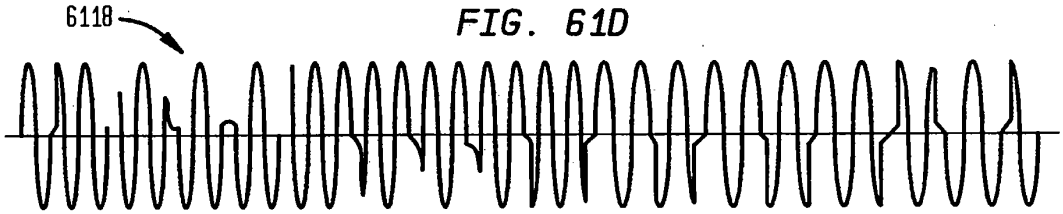


FIG. 61D

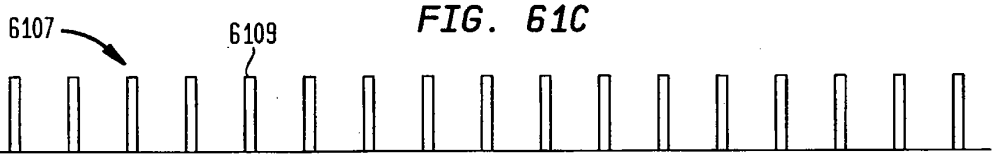


FIG. 61C

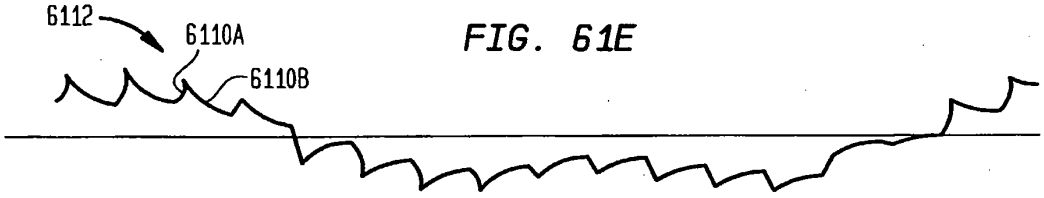


FIG. 61E

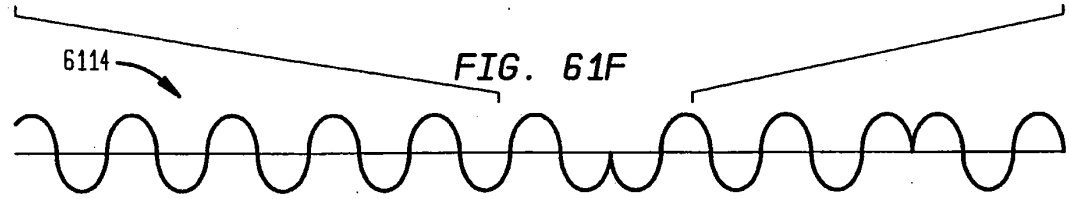


FIG. 61F

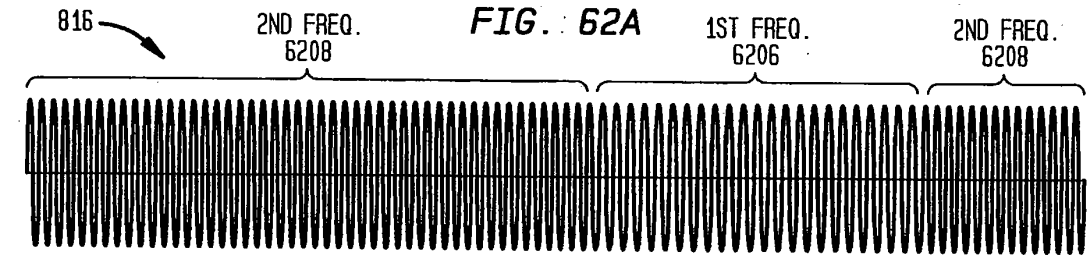


FIG. 62A

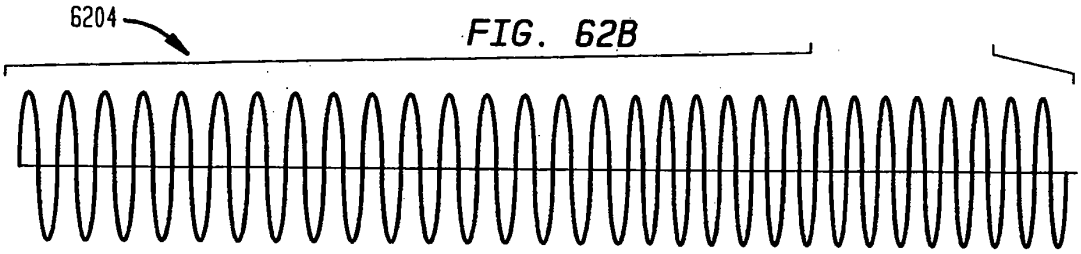


FIG. 62B

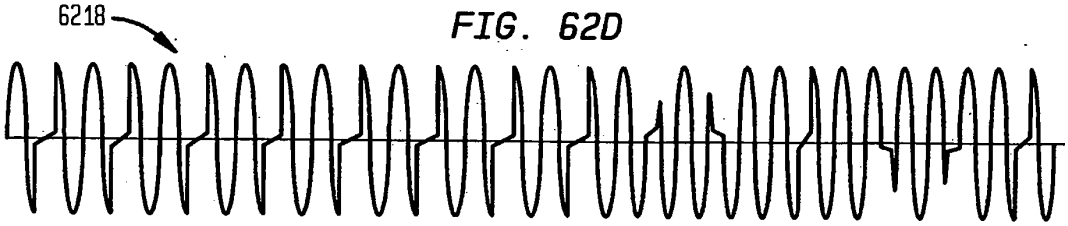


FIG. 62D

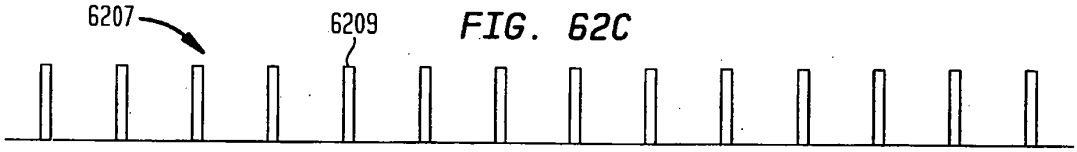


FIG. 62C

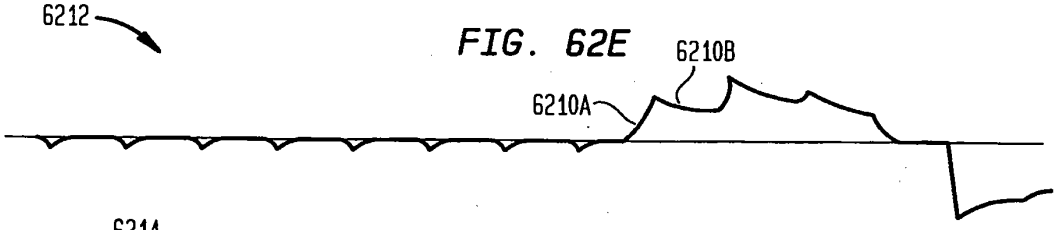


FIG. 62E

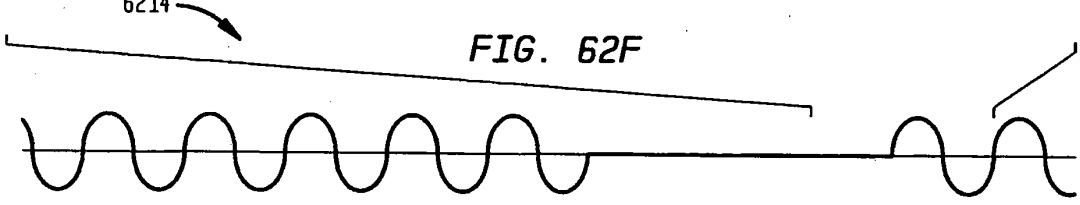


FIG. 62F

FIG. 63

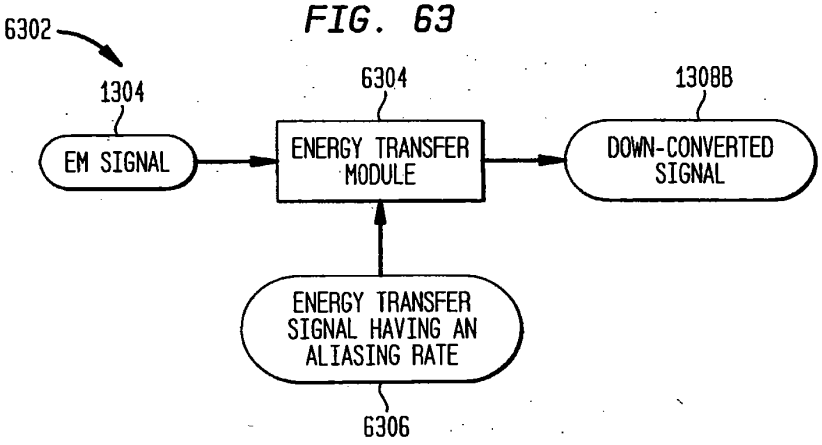


FIG. 64A

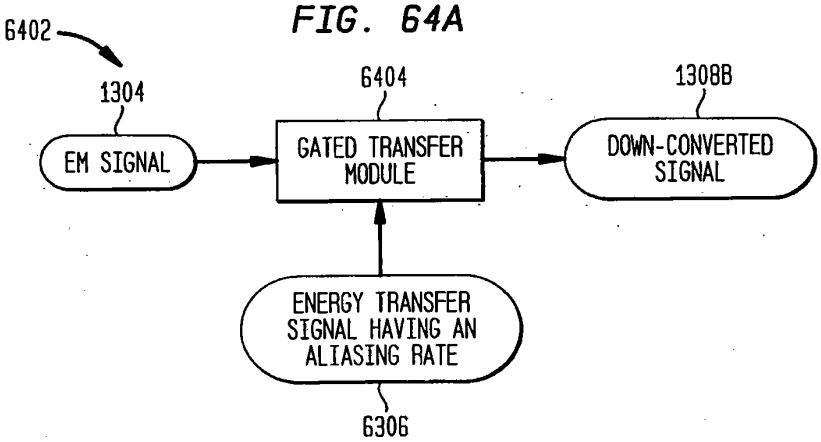


FIG. 64B

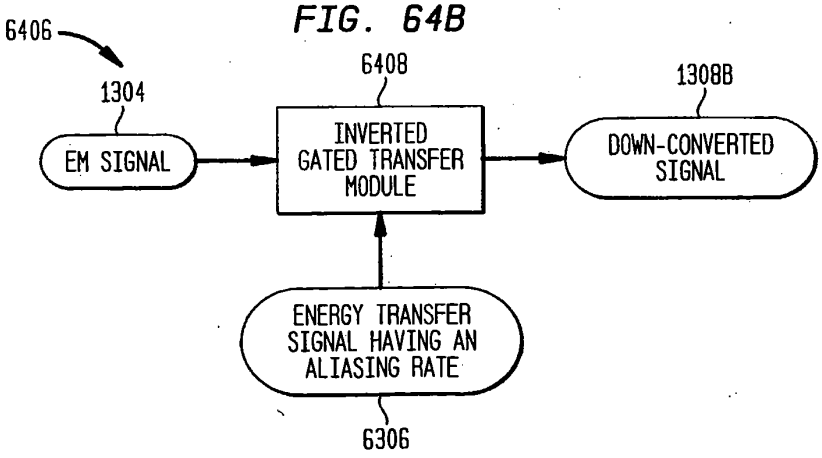


FIG. 65

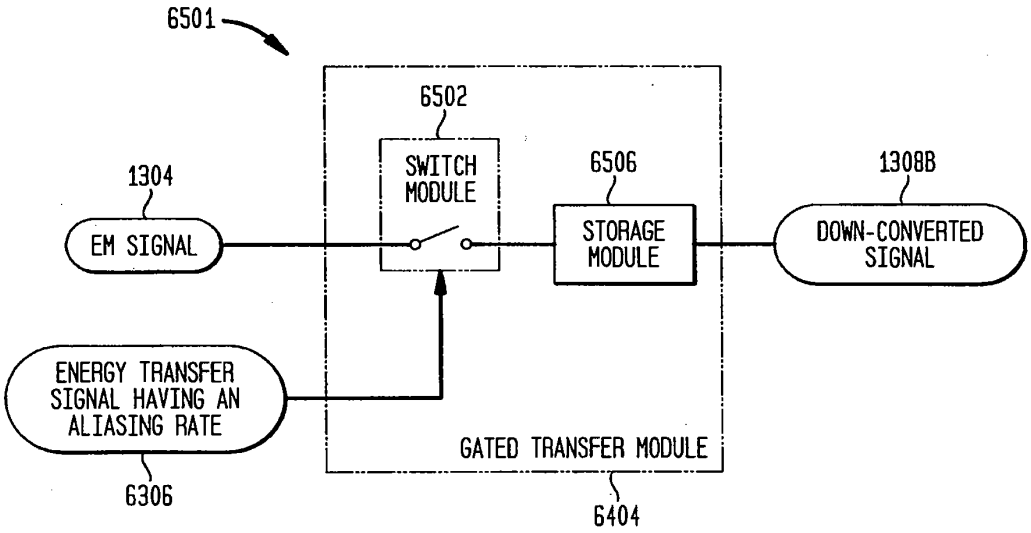


FIG. 66A

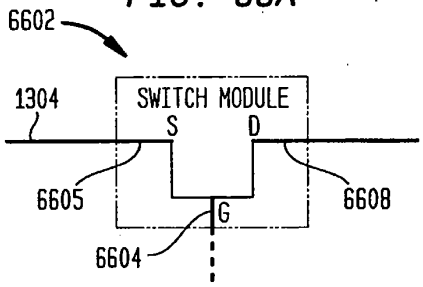


FIG. 66B

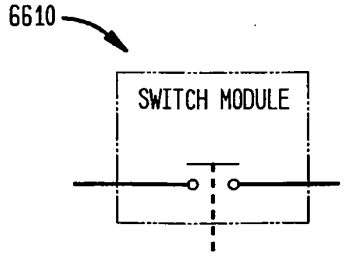


FIG. 66C

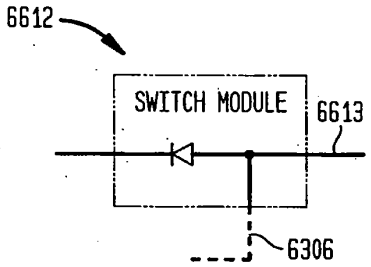
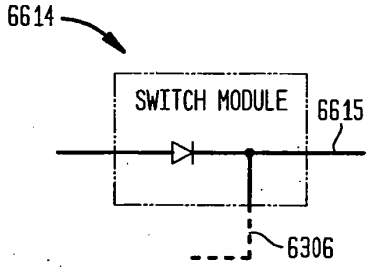


FIG. 66D



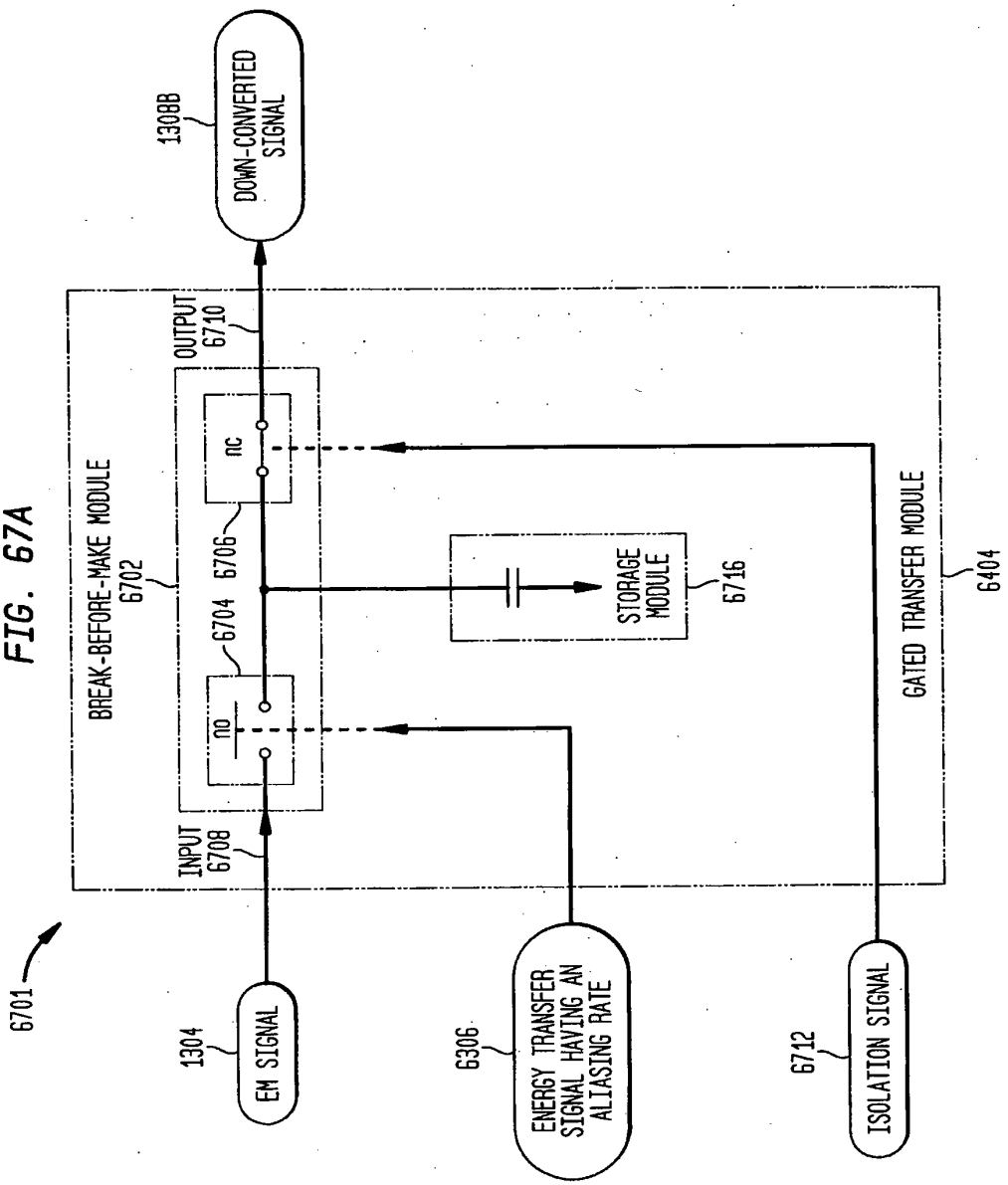

6701
1304
EM SIGNAL
6306
ENERGY TRANSFER SIGNAL HAVING AN ALIASING RATE
6712
ISOLATION SIGNAL
INPUT 6708
BREAK-BEFORE-MAKE MODULE 6702
nc
nc
6704
6706
OUTPUT 6710
1308B
DOWN-CONVERTED SIGNAL
STORAGE MODULE 6716
GATED TRANSFER MODULE 6404

FIG. 67A

FIG. 67B

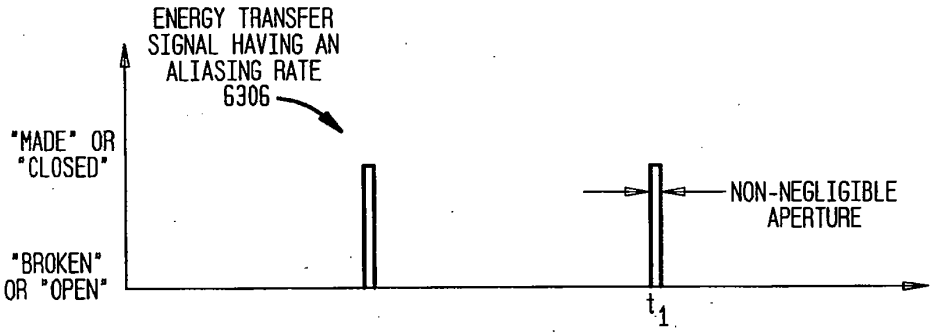


FIG. 67C

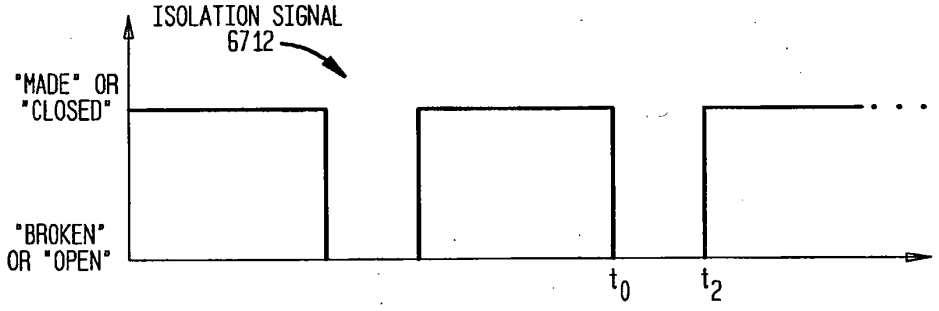


FIG. 68A

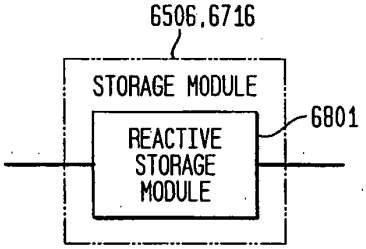


FIG. 68B

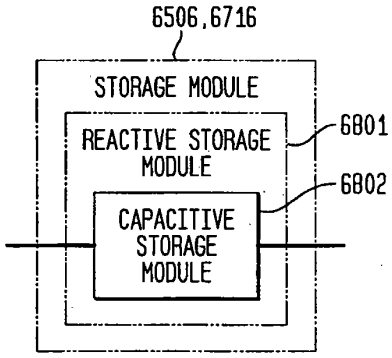


FIG. 68C

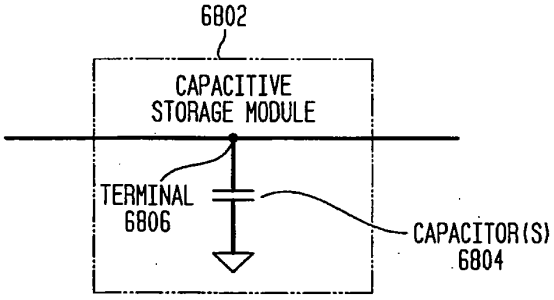


FIG. 68D

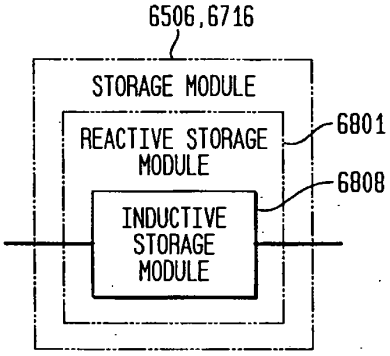


FIG. 68E

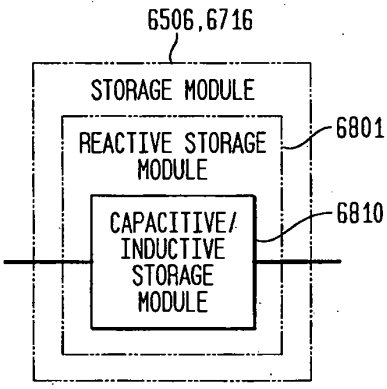


FIG. 68F

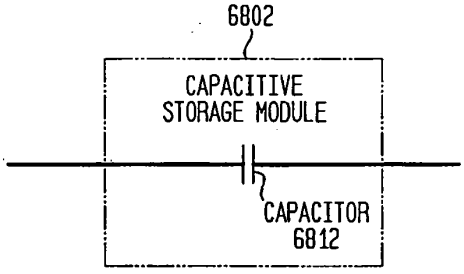


FIG. 68G

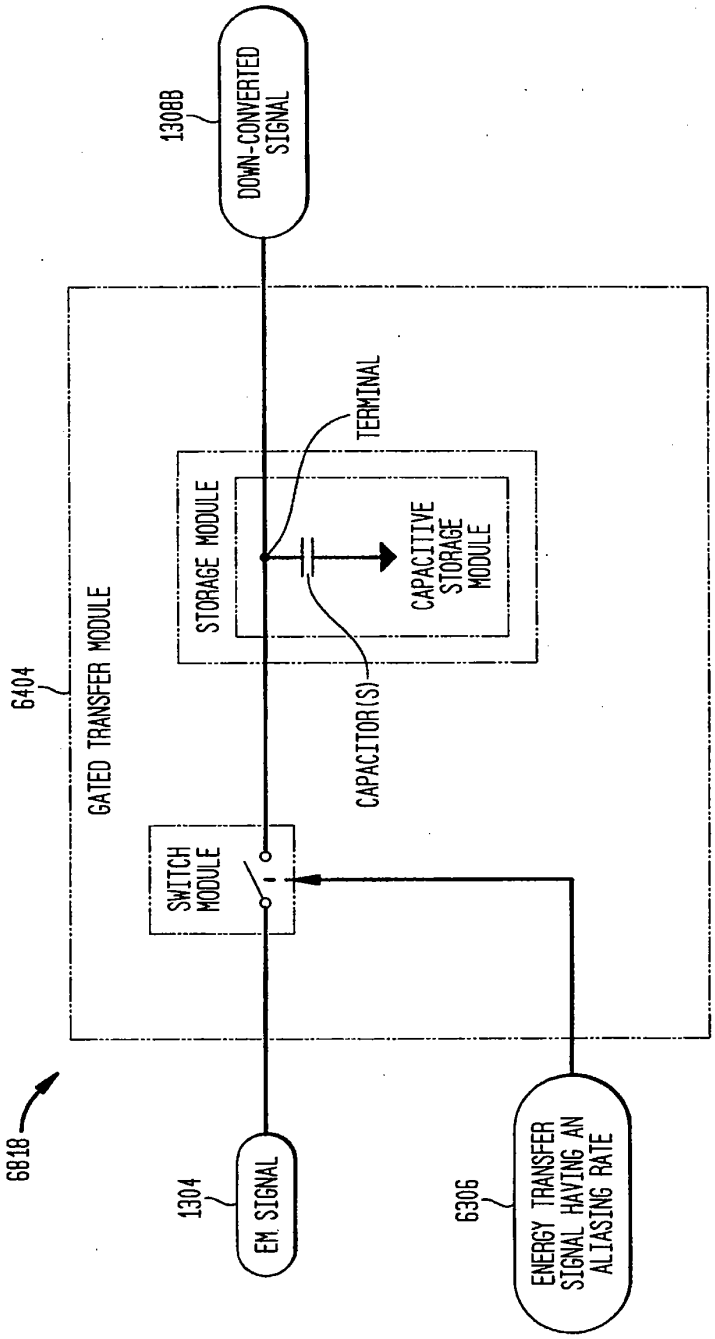
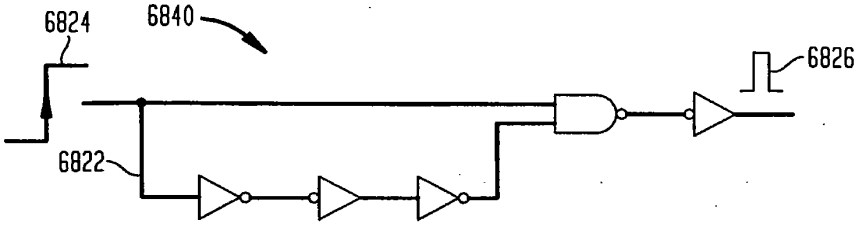
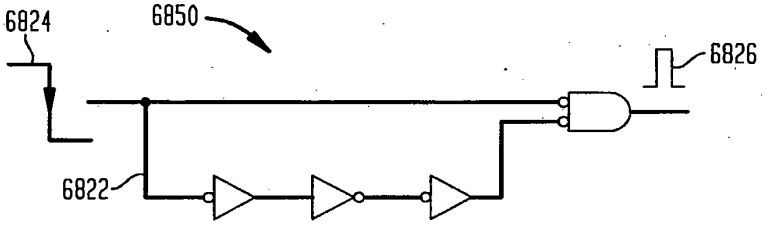

6818
6404
GATED TRANSFER MODULE
SWITCH MODULE
STORAGE MODULE
CAPACITIVE STORAGE MODULE
TERMINAL
CAPACITOR(S)
1308B
DOWN-CONVERTED SIGNAL
1304
EM SIGNAL
6306
ENERGY TRANSFER SIGNAL HAVING AN ALIASING RATE

FIG. 68H



A. RISING EDGE PULSE GENERATOR

FIG. 68I



B. FALLING-EDGE PULSE GENERATOR

FIG. 68J

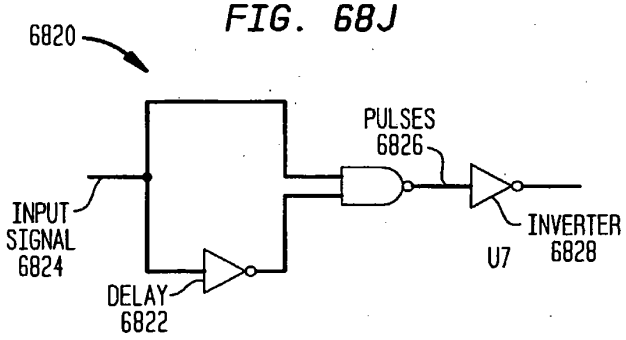


FIG. 68K

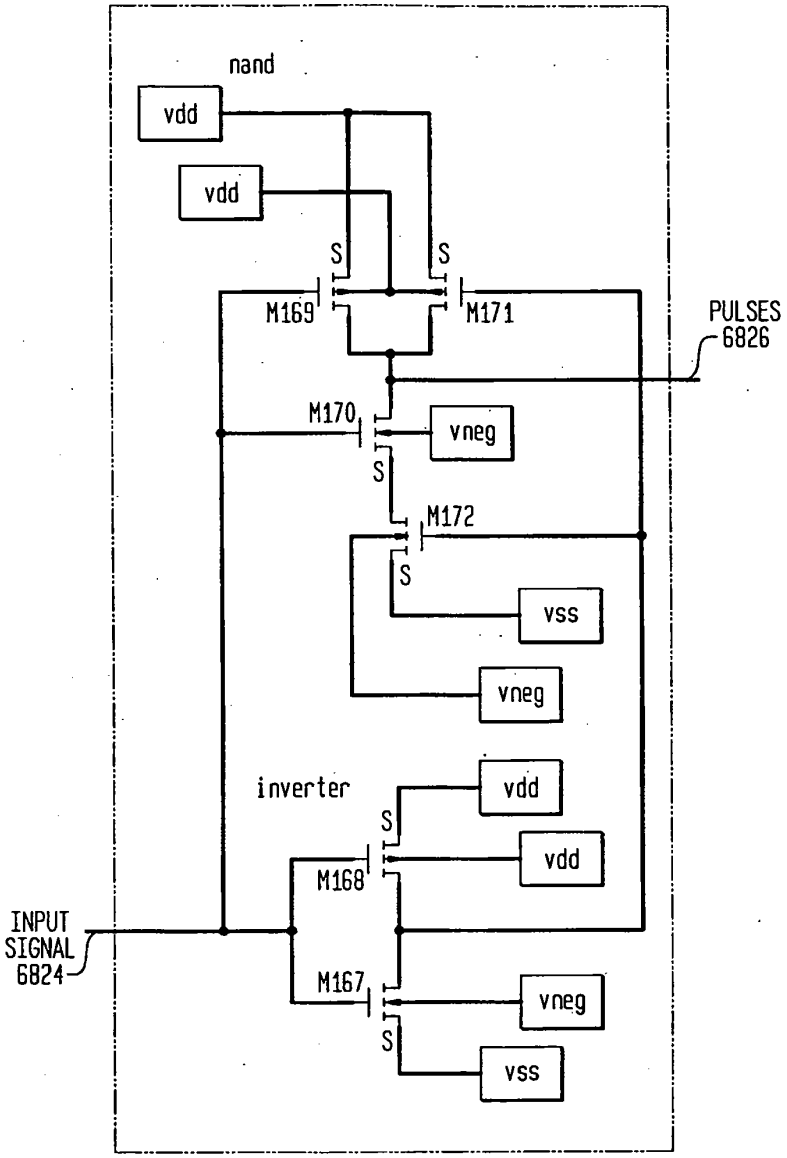


FIG. 68L

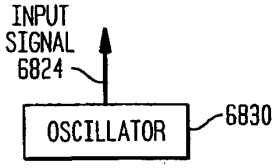


FIG. 69

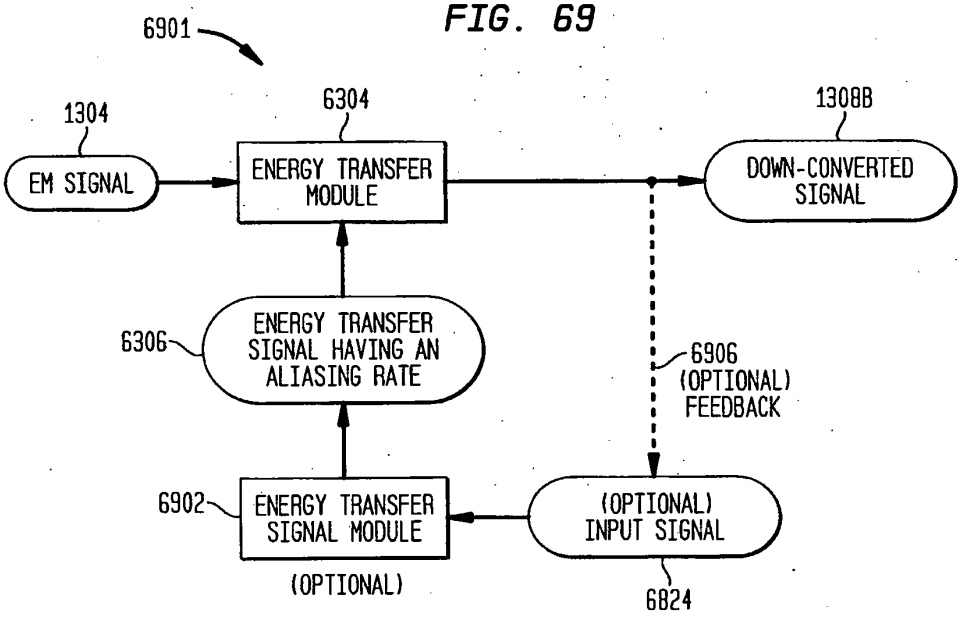

6901
1304
EM SIGNAL
6304
ENERGY TRANSFER MODULE
1308B
DOWN-CONVERTED SIGNAL
6306
ENERGY TRANSFER SIGNAL HAVING AN ALIASING RATE
6906
(OPTIONAL) FEEDBACK
6902
ENERGY TRANSFER SIGNAL MODULE
(OPTIONAL)
(OPTIONAL) INPUT SIGNAL
6824

FIG. 70

IMPEDANCE MATCHED ALIASING MODULE

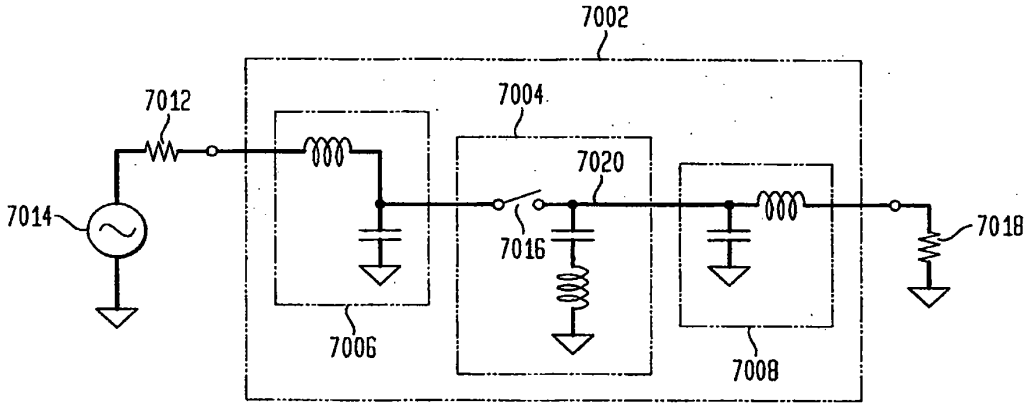


FIG. 71A

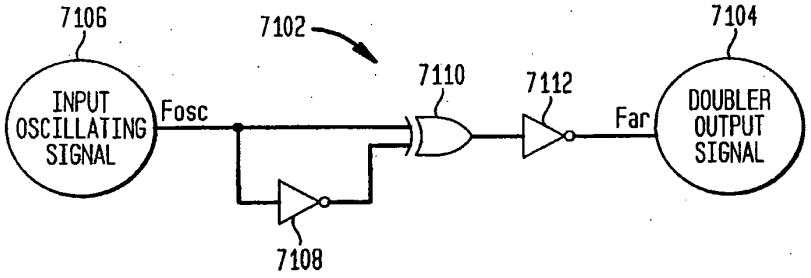


FIG. 71B

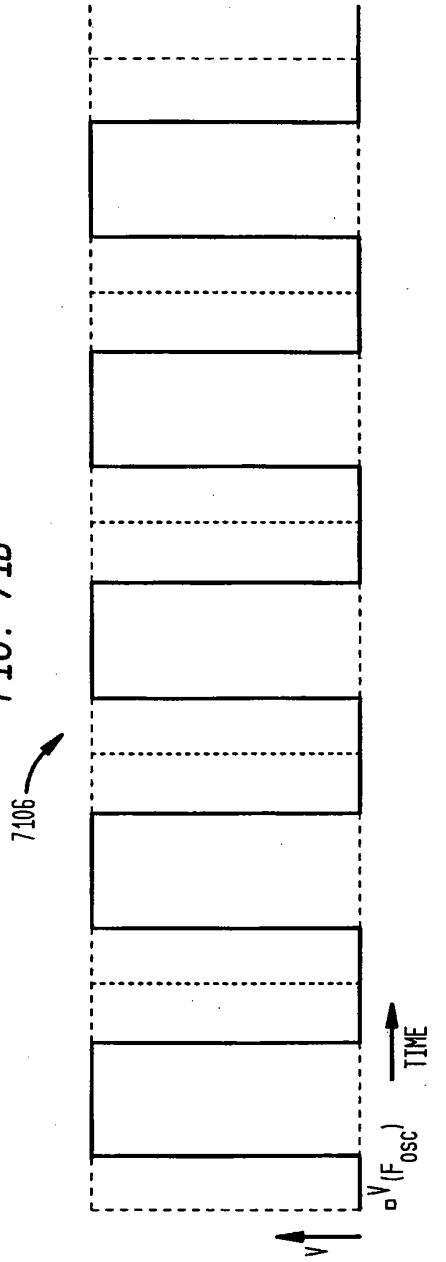


FIG. 71C

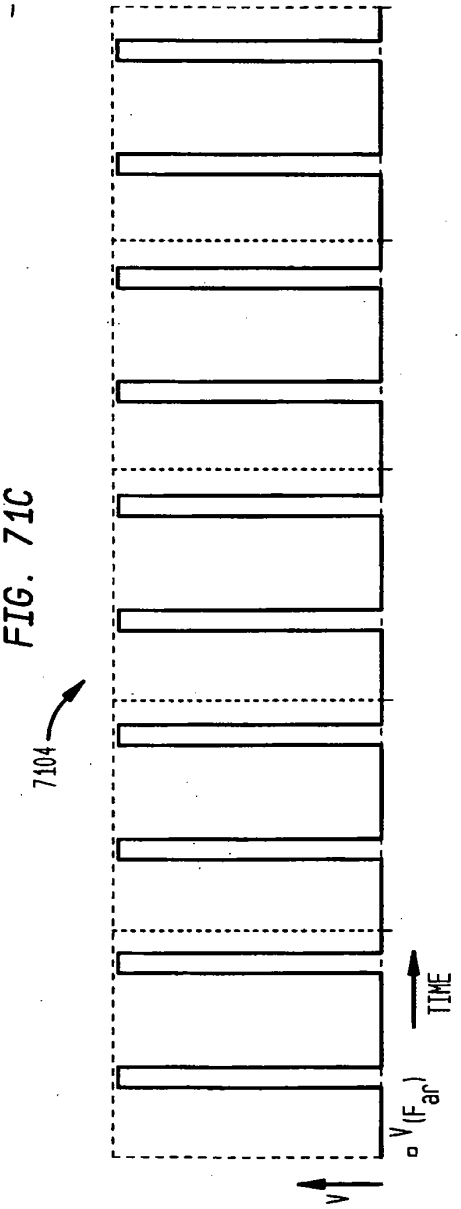


FIG. 72

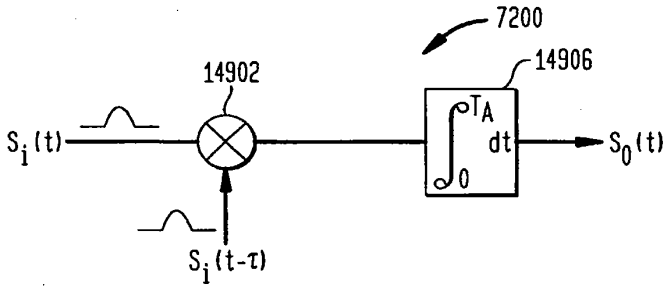


FIG. 73

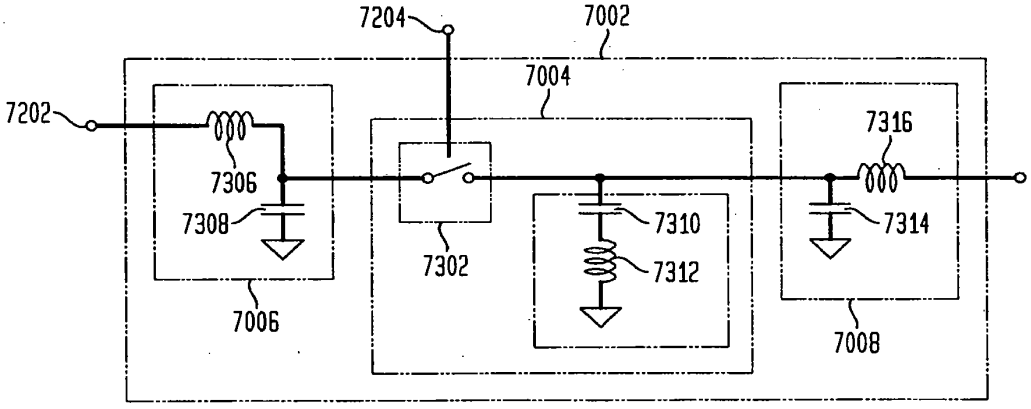

ALIASING MODULE
7204
7002
7004
7202
7306
7308
7006
7302
7310
7312
7316
7314
7008

FIG. 74

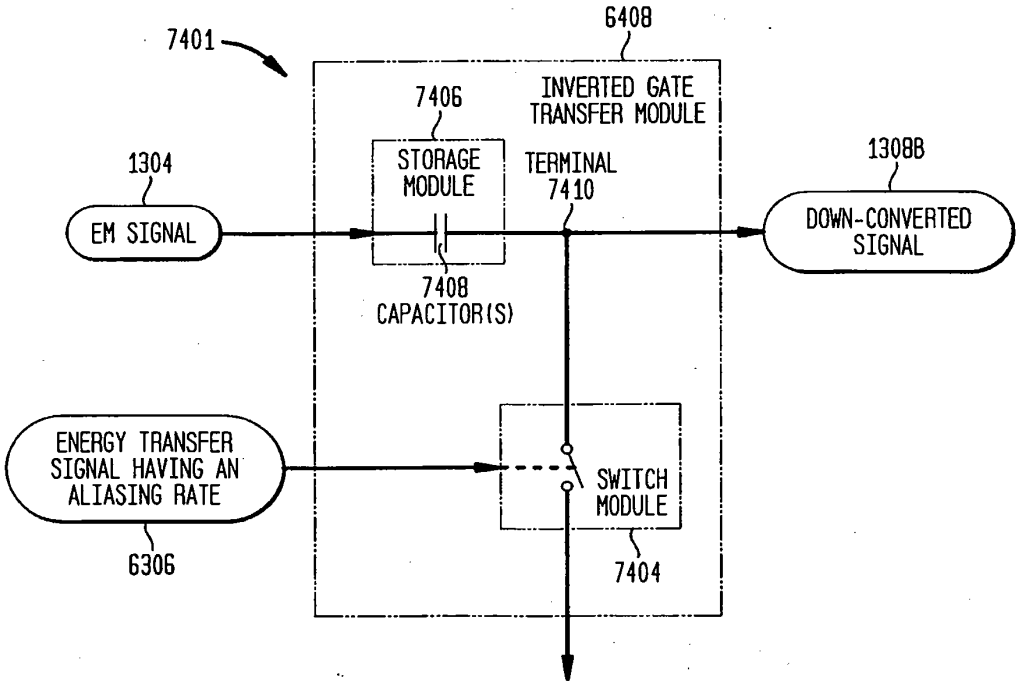

7401
6408
INVERTED GATE TRANSFER MODULE
7406
STORAGE MODULE
TERMINAL 7410
1304
EM SIGNAL
1308B
DOWN-CONVERTED SIGNAL
7408 CAPACITOR(S)
ENERGY TRANSFER SIGNAL HAVING AN ALIASING RATE
6306
SWITCH MODULE
7404

FIG. 75A



FIG. 75B



FIG. 75C



FIG. 75D

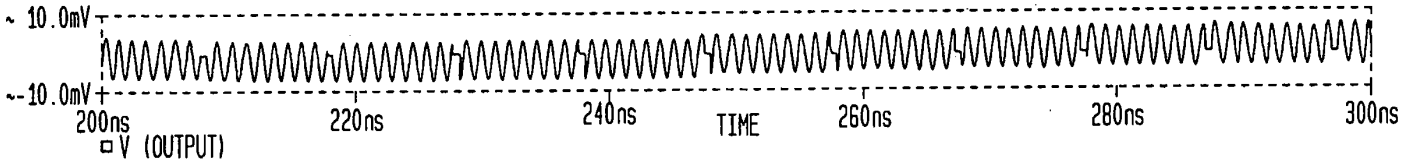


FIG. 75E

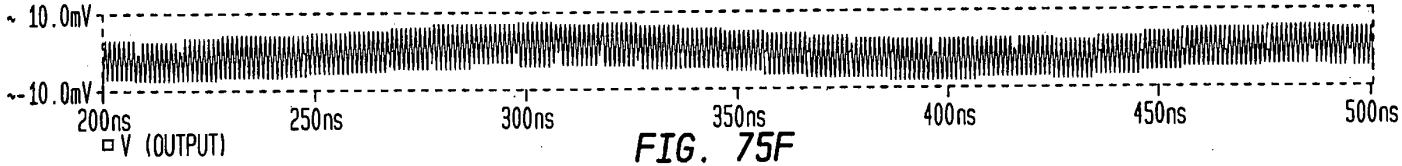


FIG. 75F

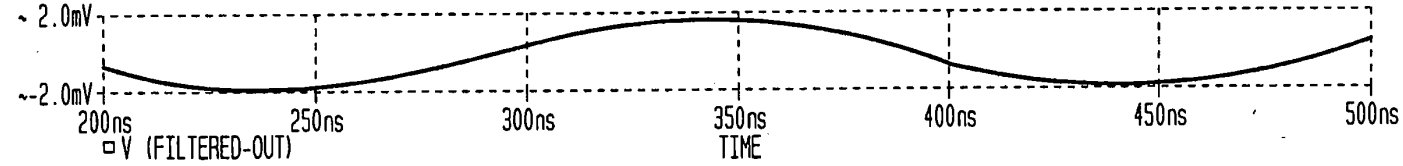


FIG. 76A

DIFFERENTIAL ENERGY TRANSFER CONFIGURATION

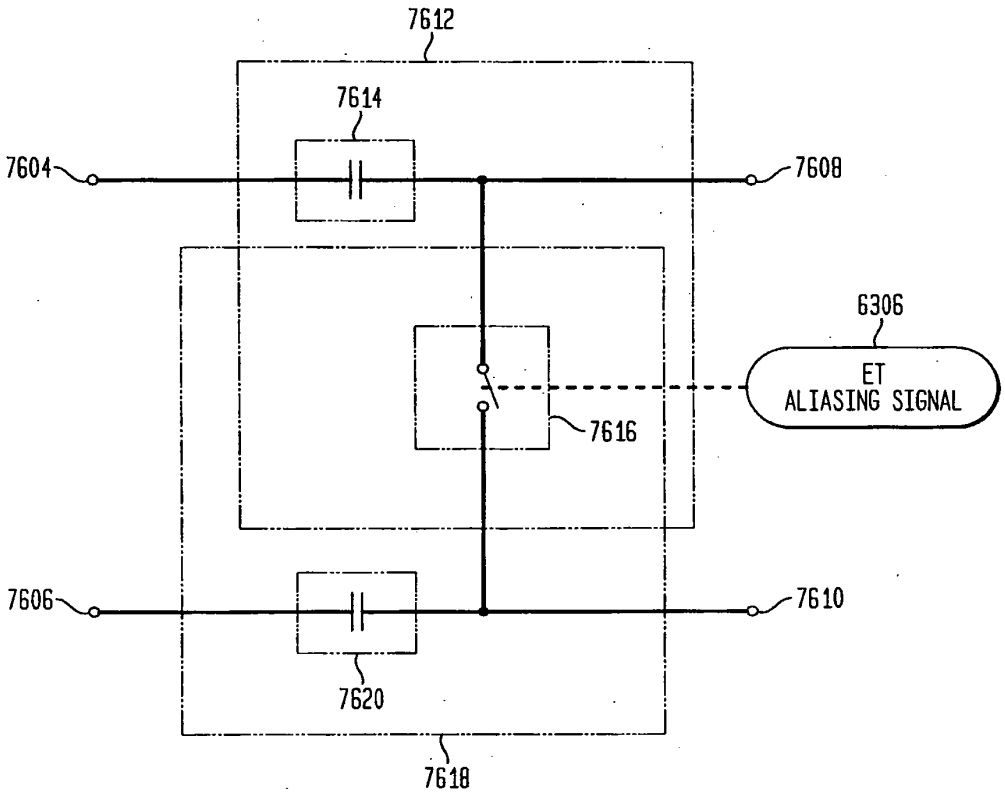


FIG. 76B

DIFFERENTIAL INPUT TO DIFFERENTIAL OUTPUT

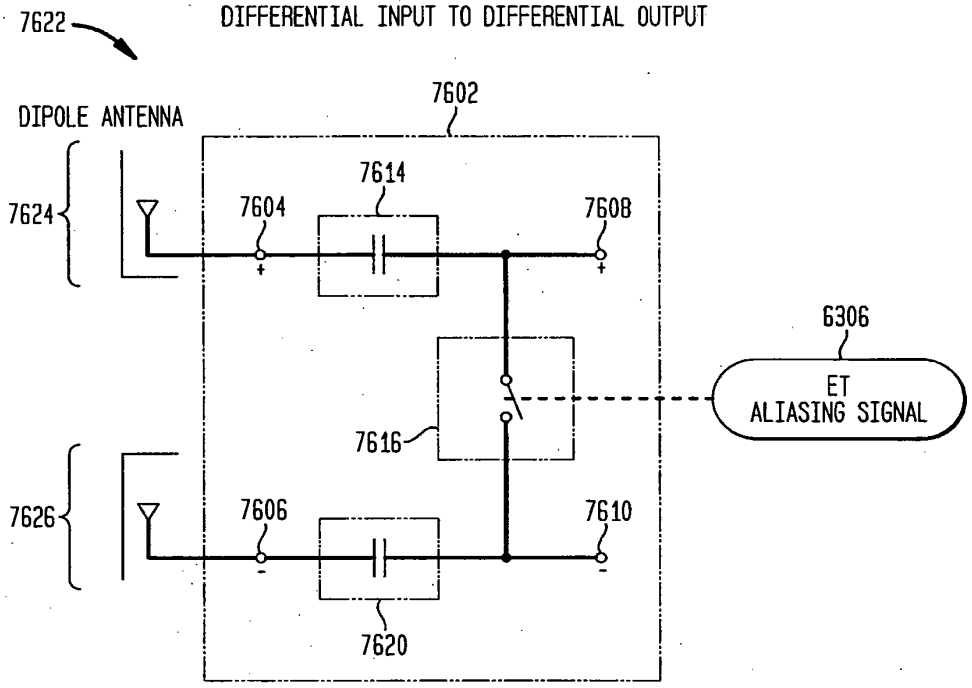


FIG. 76C

SINGLE INPUT TO DIFFERENTIAL OUTPUT

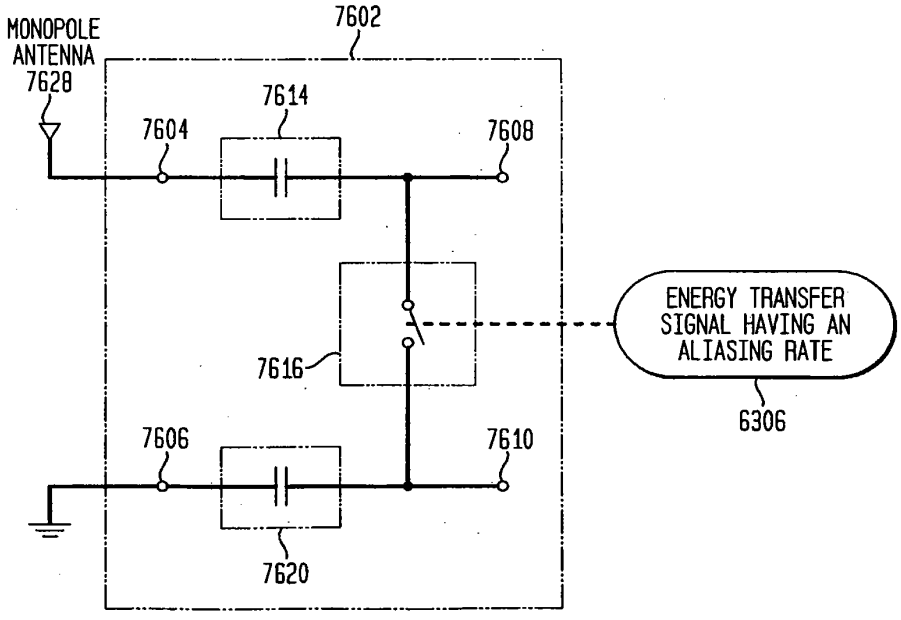


FIG. 76D

DIFFERENTIAL INPUT TO SINGLE OUTPUT

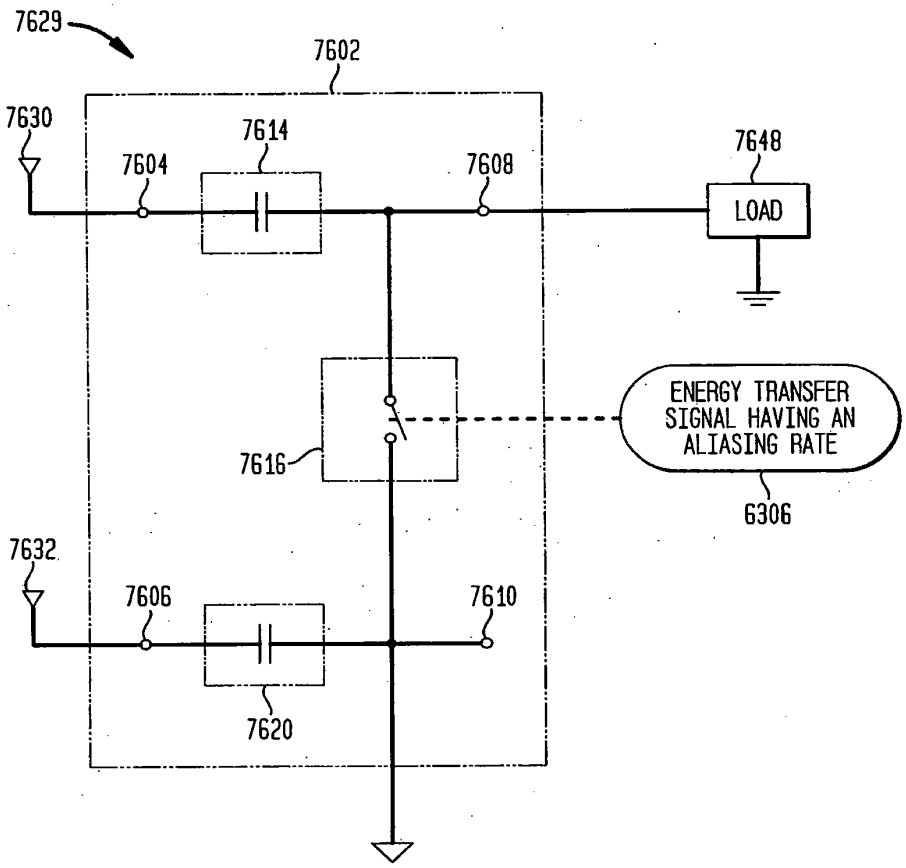


FIG. 76E

EXAMPLE INPUT/OUTPUT CIRCUITRY

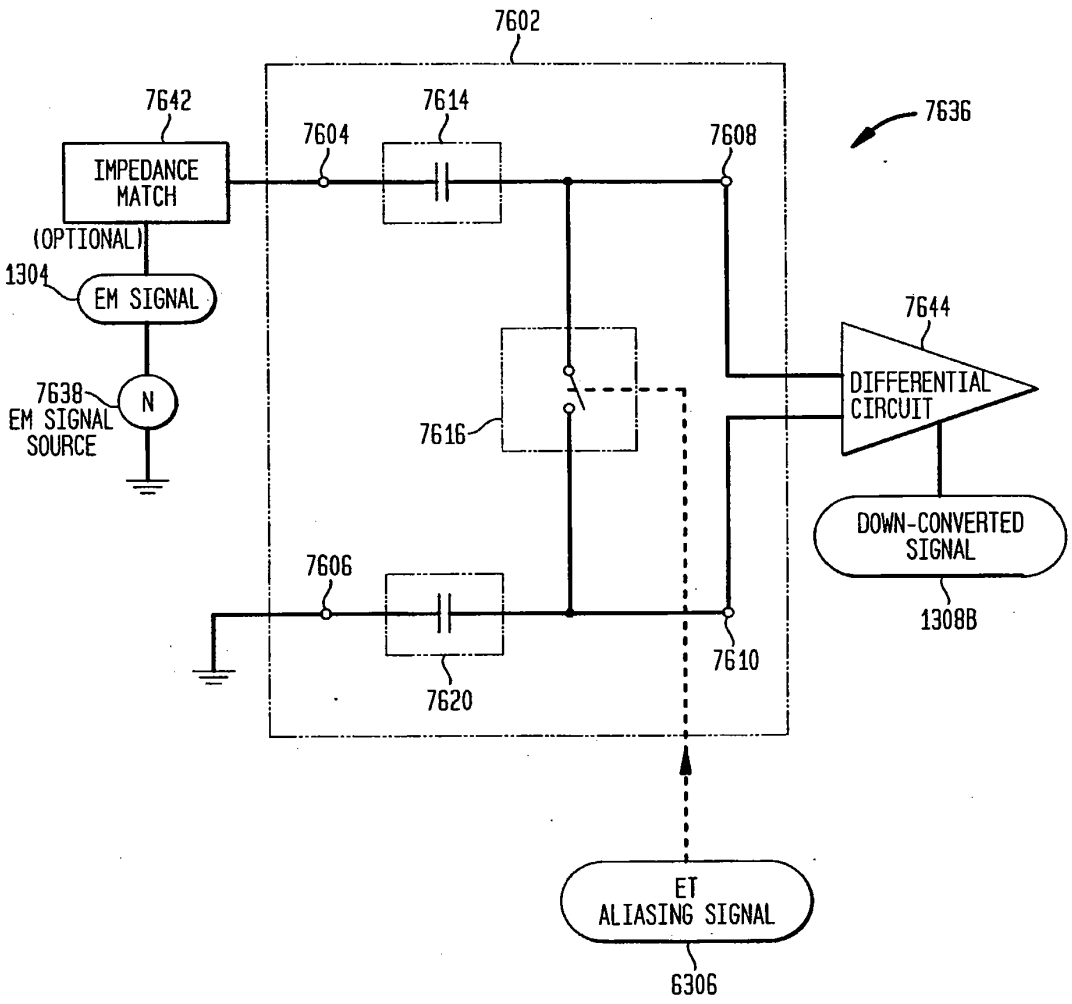


FIG. 77A

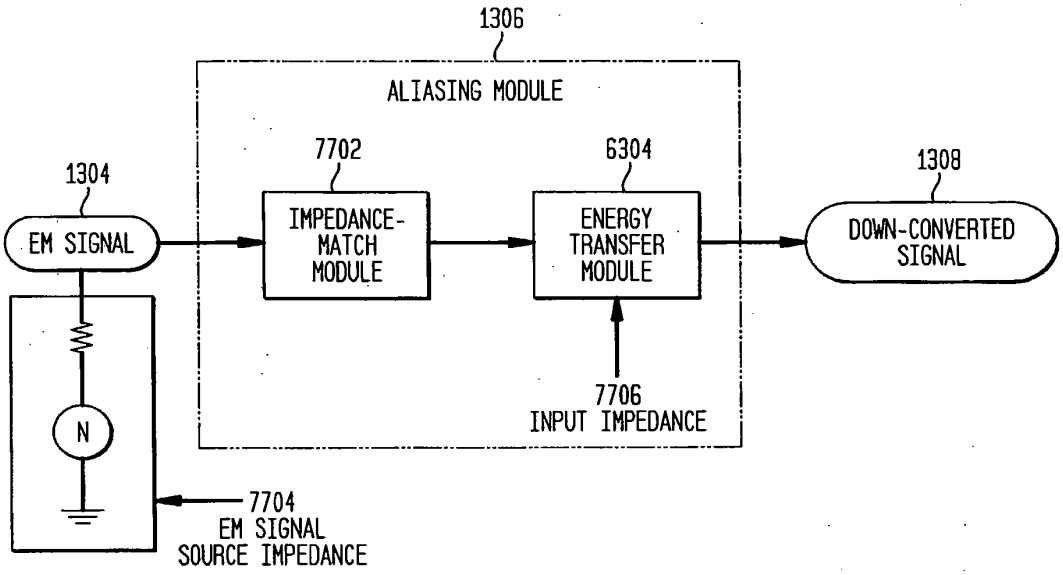


FIG. 77B

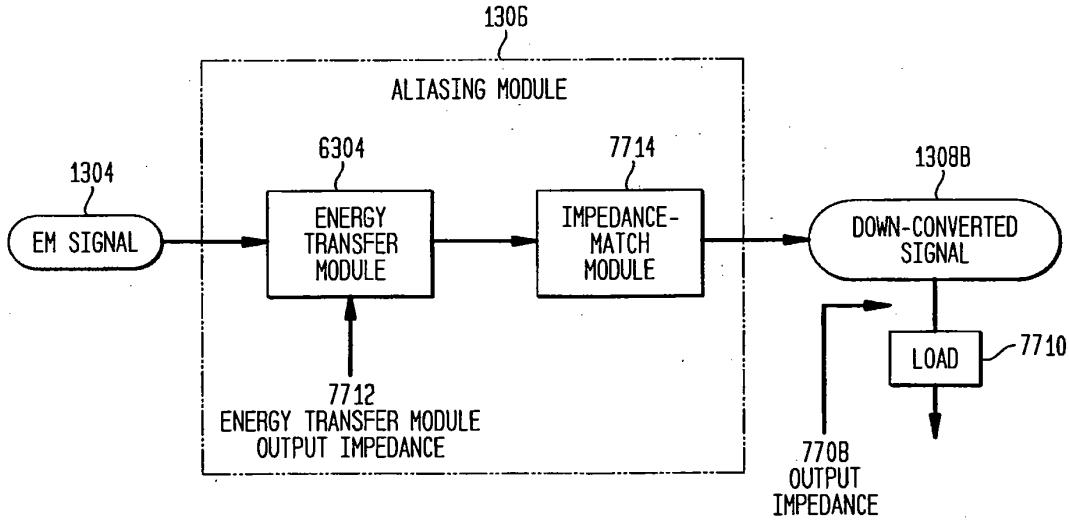


FIG. 77C

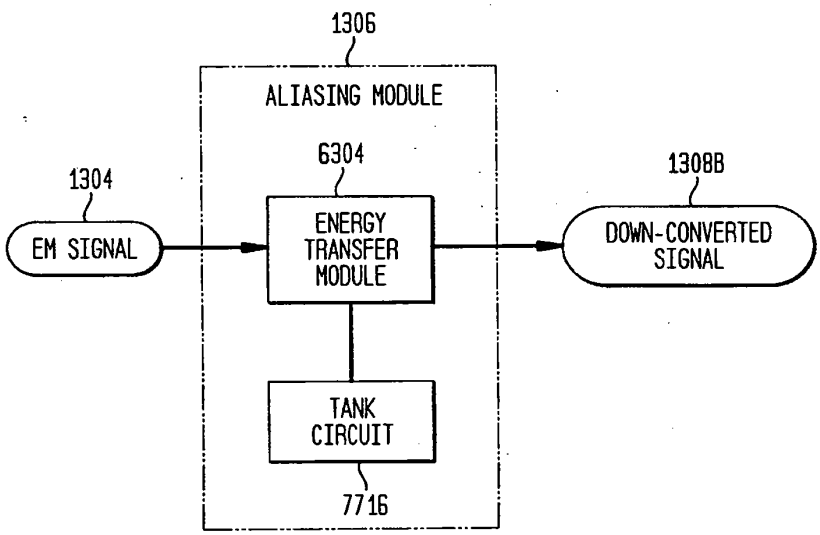

1306
ALIASING MODULE
6304
1304
EM SIGNAL
ENERGY TRANSFER MODULE
1308B
DOWN-CONVERTED SIGNAL
TANK CIRCUIT
7716

FIG. 78A

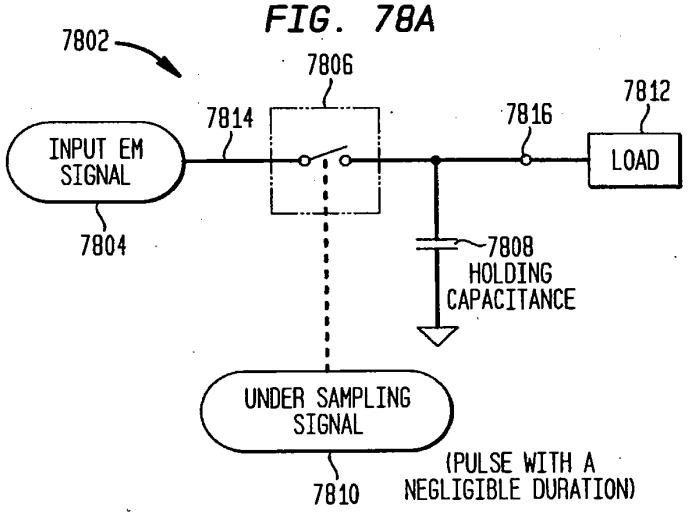


FIG. 78B

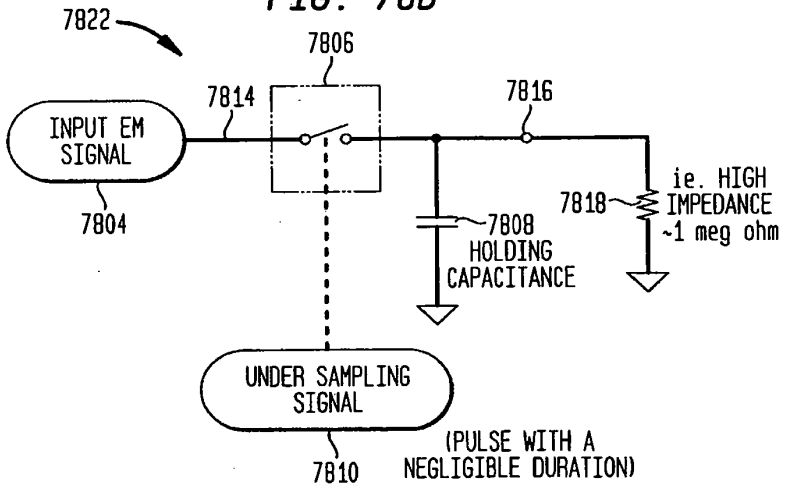


FIG. 79A

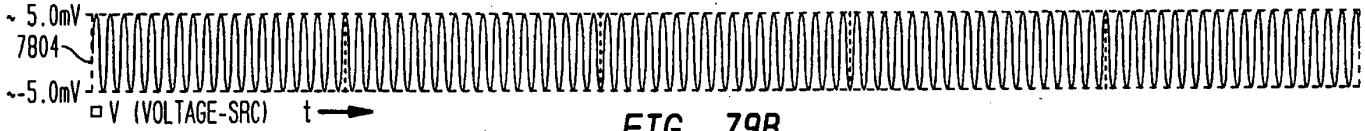


FIG. 79B

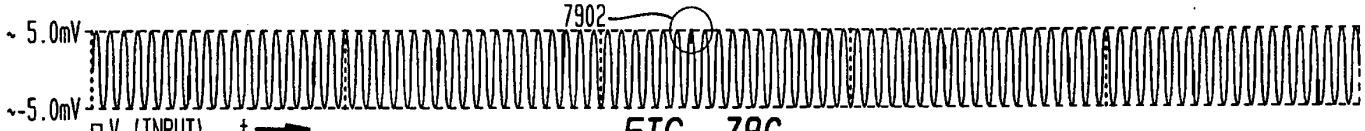


FIG. 79C

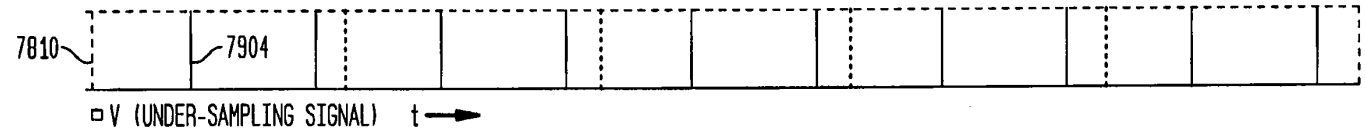


FIG. 79D

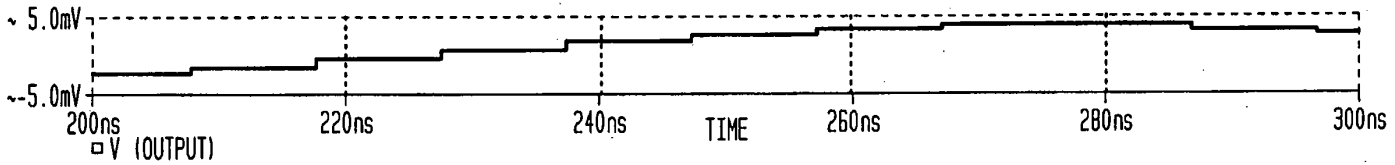


FIG. 79E

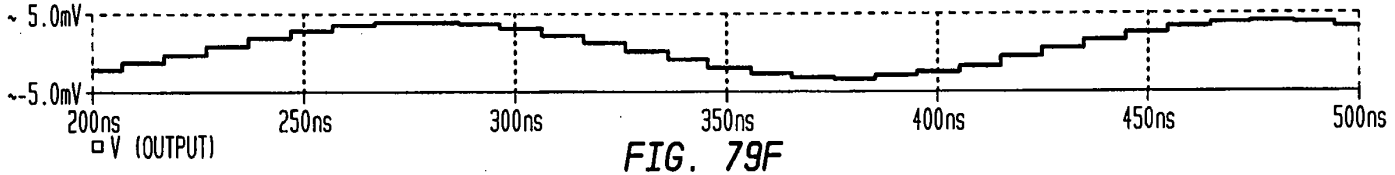


FIG. 79F

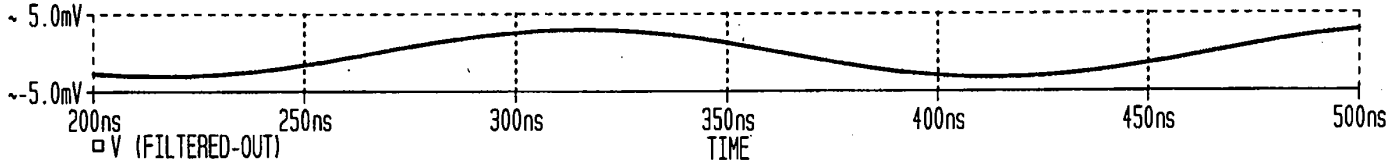


FIG. 80A



FIG. 80B

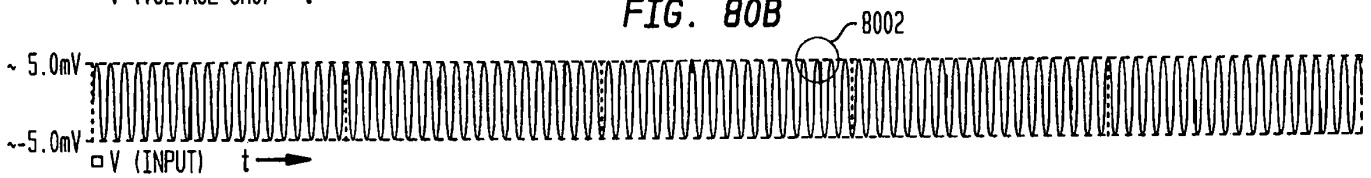


FIG. 80C

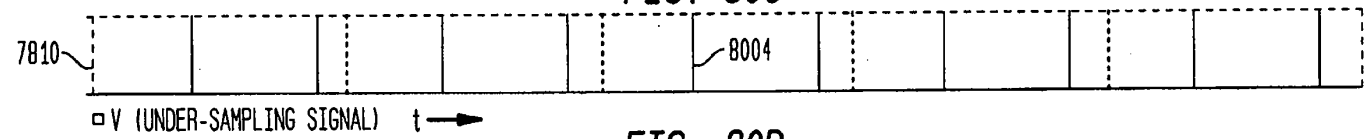


FIG. 80D

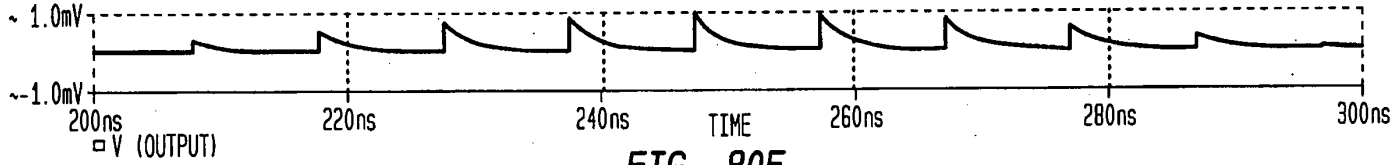


FIG. 80E

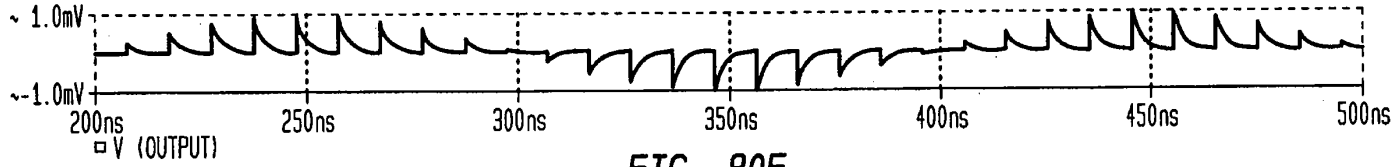


FIG. 80F

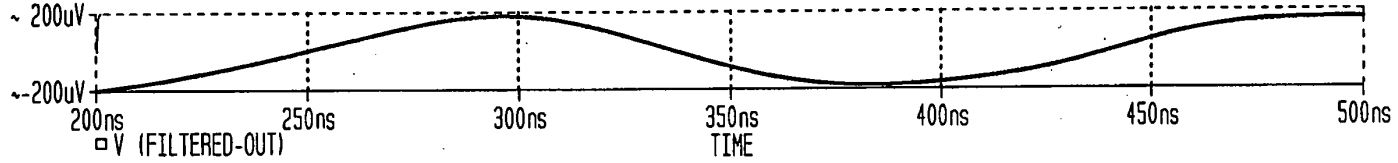


FIG. 81A

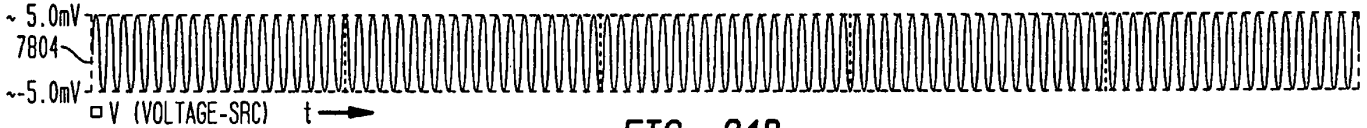


FIG. 81B

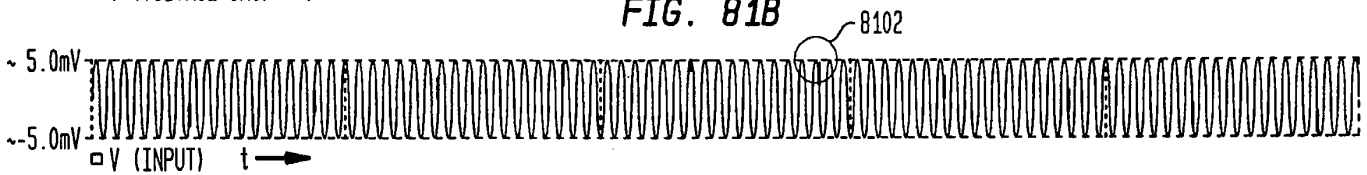


FIG. 81C

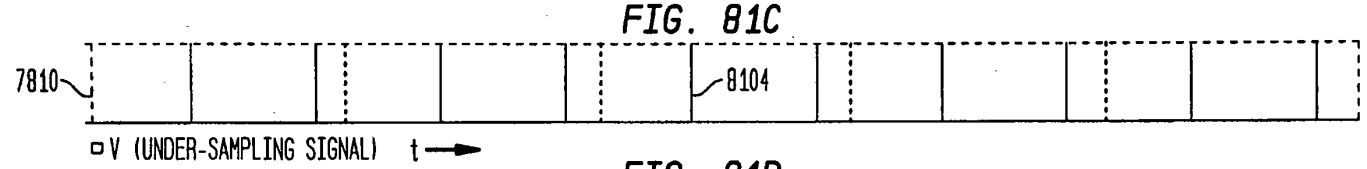


FIG. 81D

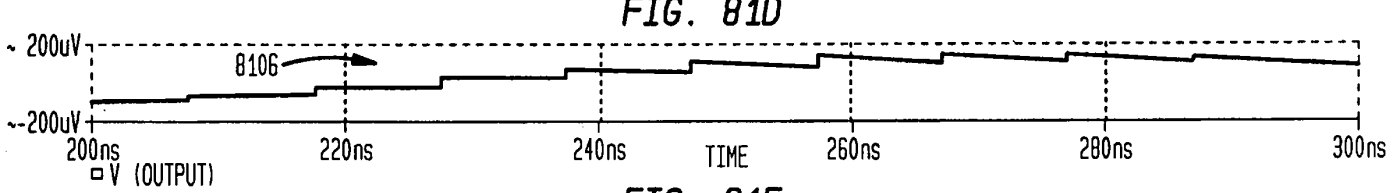


FIG. 81E

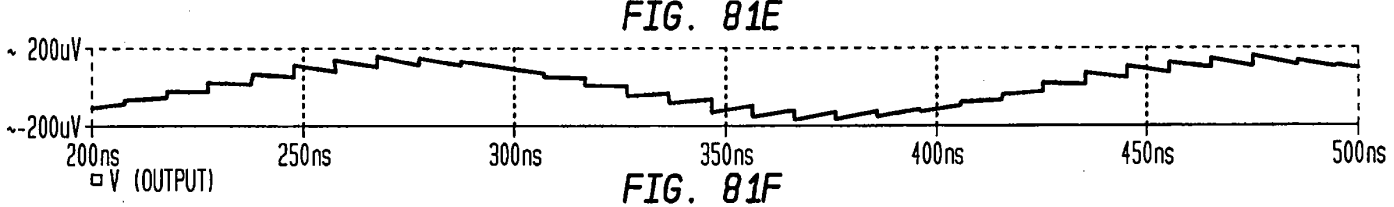
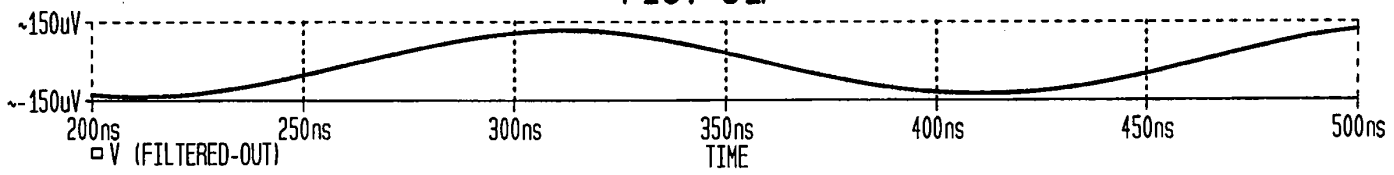


FIG. 81F



844

FIG. 82A

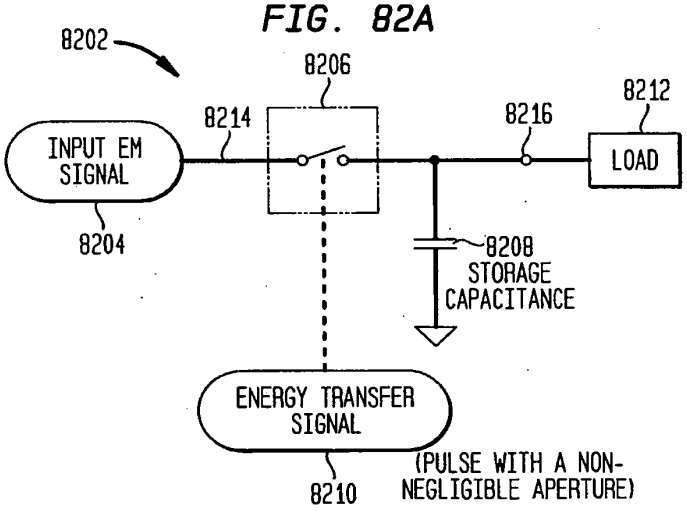


FIG. 82B

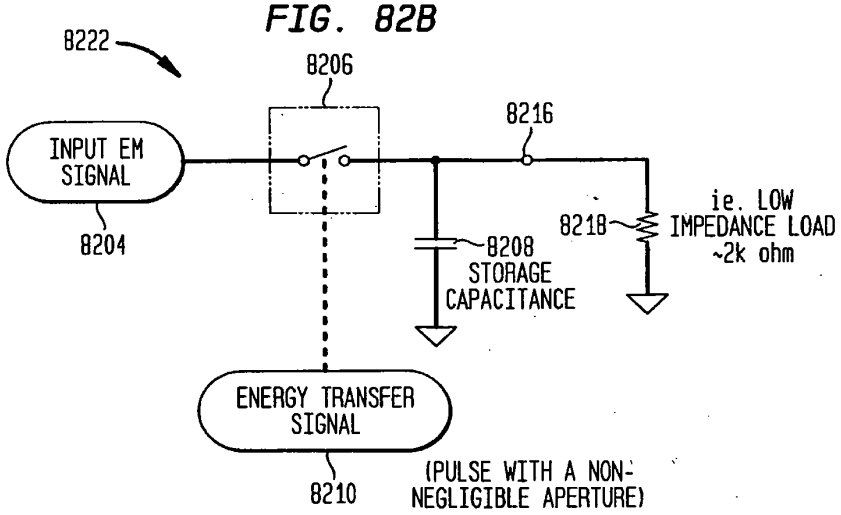


FIG. 83A

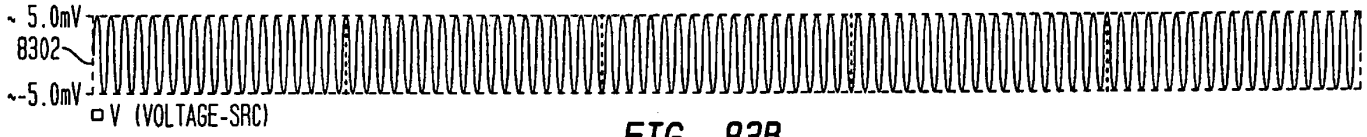


FIG. 83B

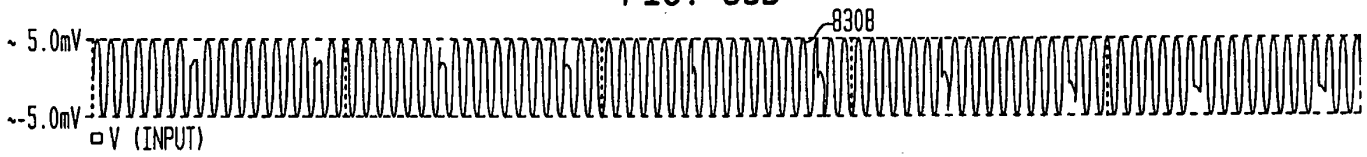


FIG. 83C

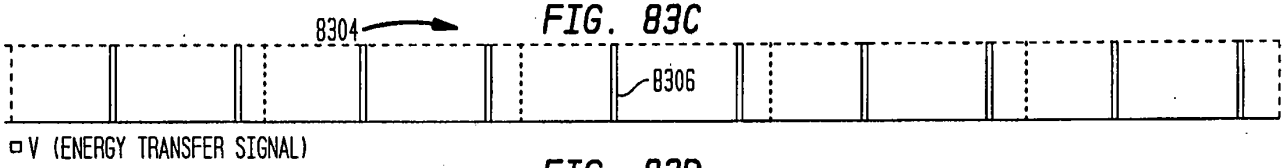


FIG. 83D

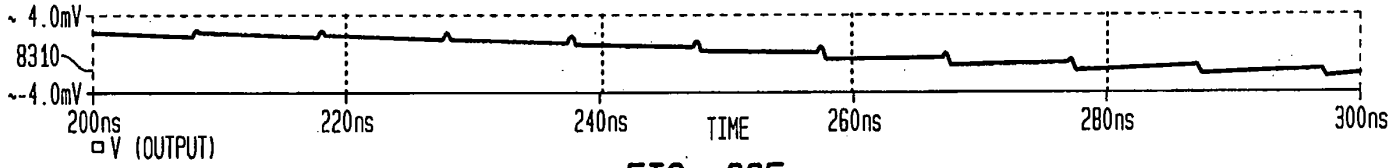


FIG. 83E

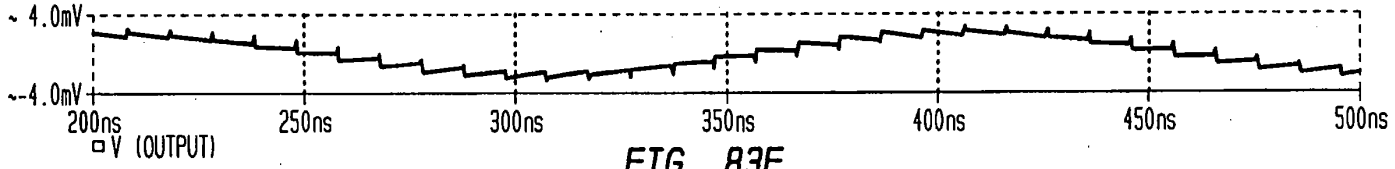


FIG. 83F

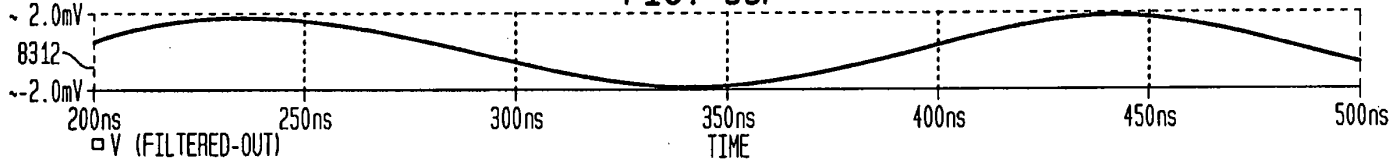


FIG. 84A

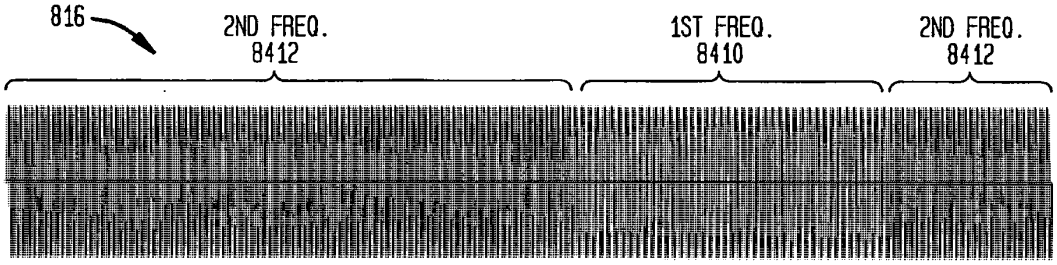


FIG. 84B

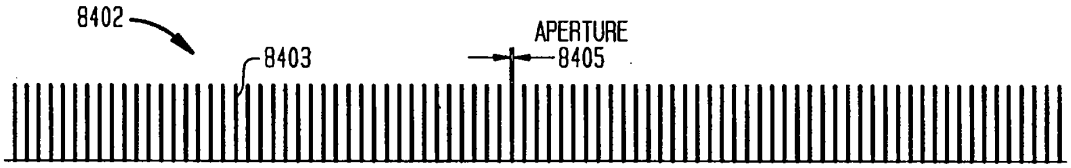


FIG. 84C

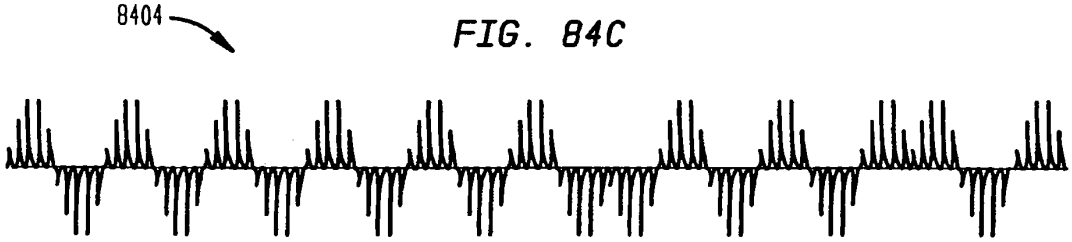


FIG. 84D

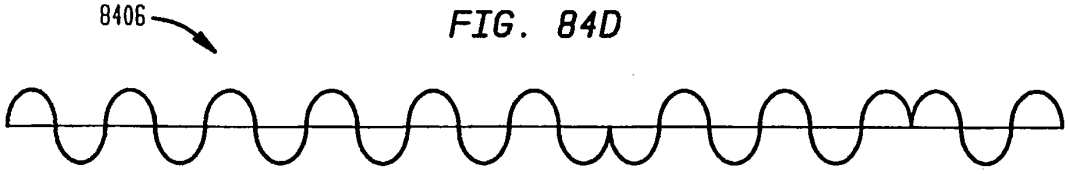


FIG. 85A

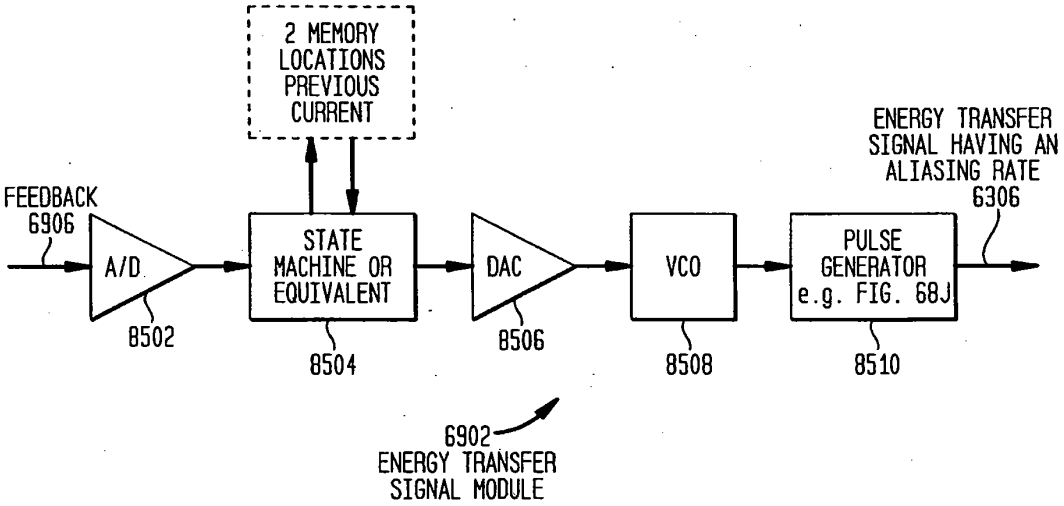

2 MEMORY LOCATIONS PREVIOUS CURRENT
FEEDBACK 6906
A/D
8502
STATE MACHINE OR EQUIVALENT
8504
DAC
8506
VCO
8508
PULSE GENERATOR e.g. FIG. 68J
8510
ENERGY TRANSFER SIGNAL HAVING AN ALIASING RATE 6306
6902 ENERGY TRANSFER SIGNAL MODULE

FIG. 85B

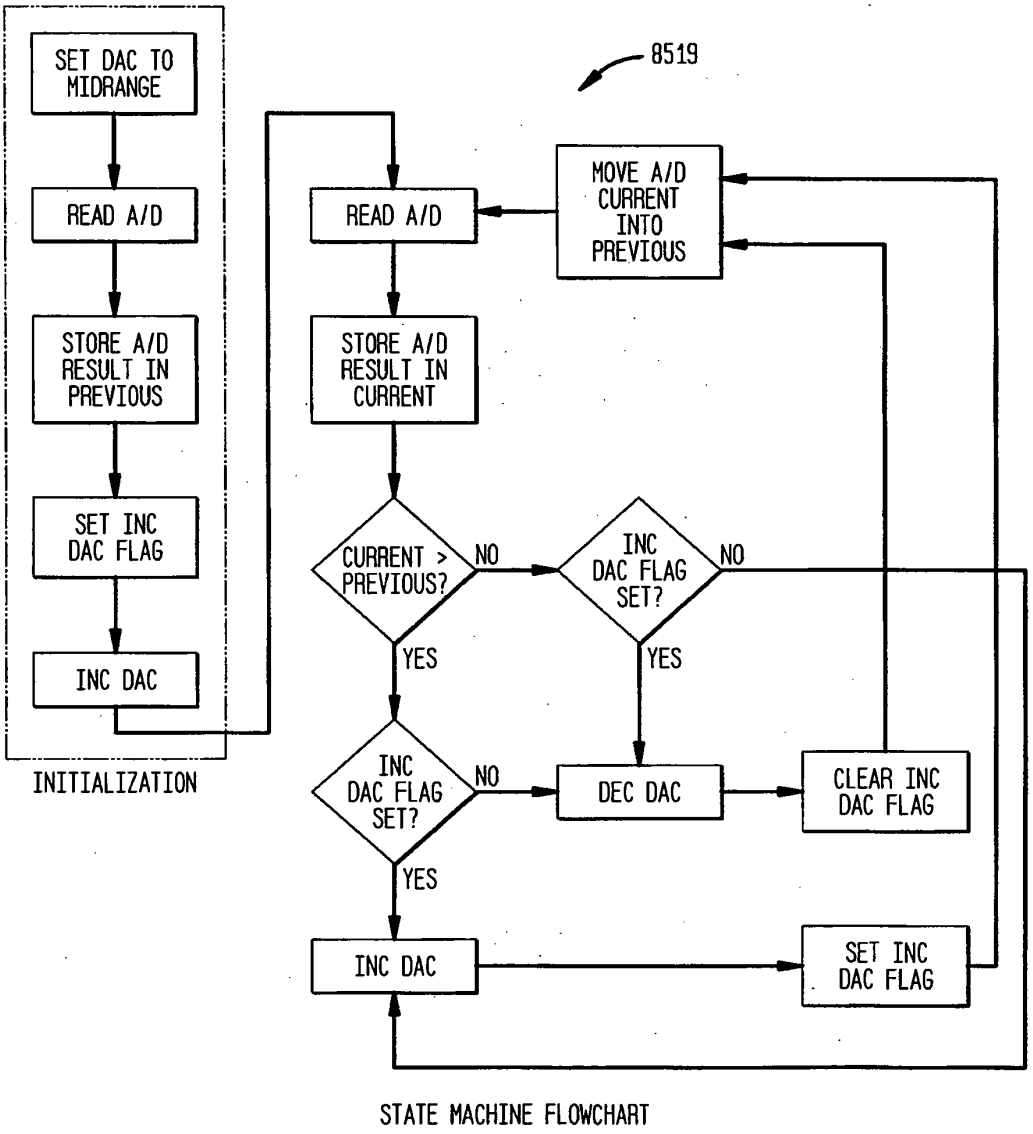
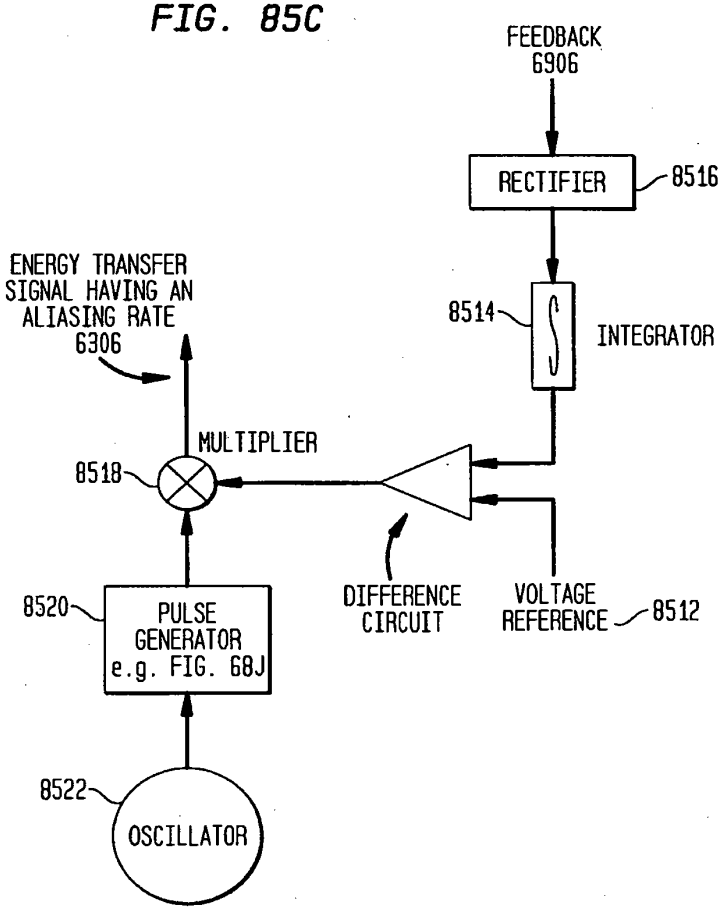

SET DAC TO MIDRANGE
READ A/D
STORE A/D RESULT IN PREVIOUS
SET INC DAC FLAG
INC DAC
INITIALIZATION
8519
READ A/D
MOVE A/D CURRENT INTO PREVIOUS
STORE A/D RESULT IN CURRENT
CURRENT > PREVIOUS?
NO
INC DAC FLAG SET?
NO
YES
YES
INC DAC FLAG SET?
NO
DEC DAC
CLEAR INC DAC FLAG
YES
INC DAC
SET INC DAC FLAG
STATE MACHINE FLOWCHART

FIG. 85C



ENERGY TRANSFER SIGNAL MODULE 6902

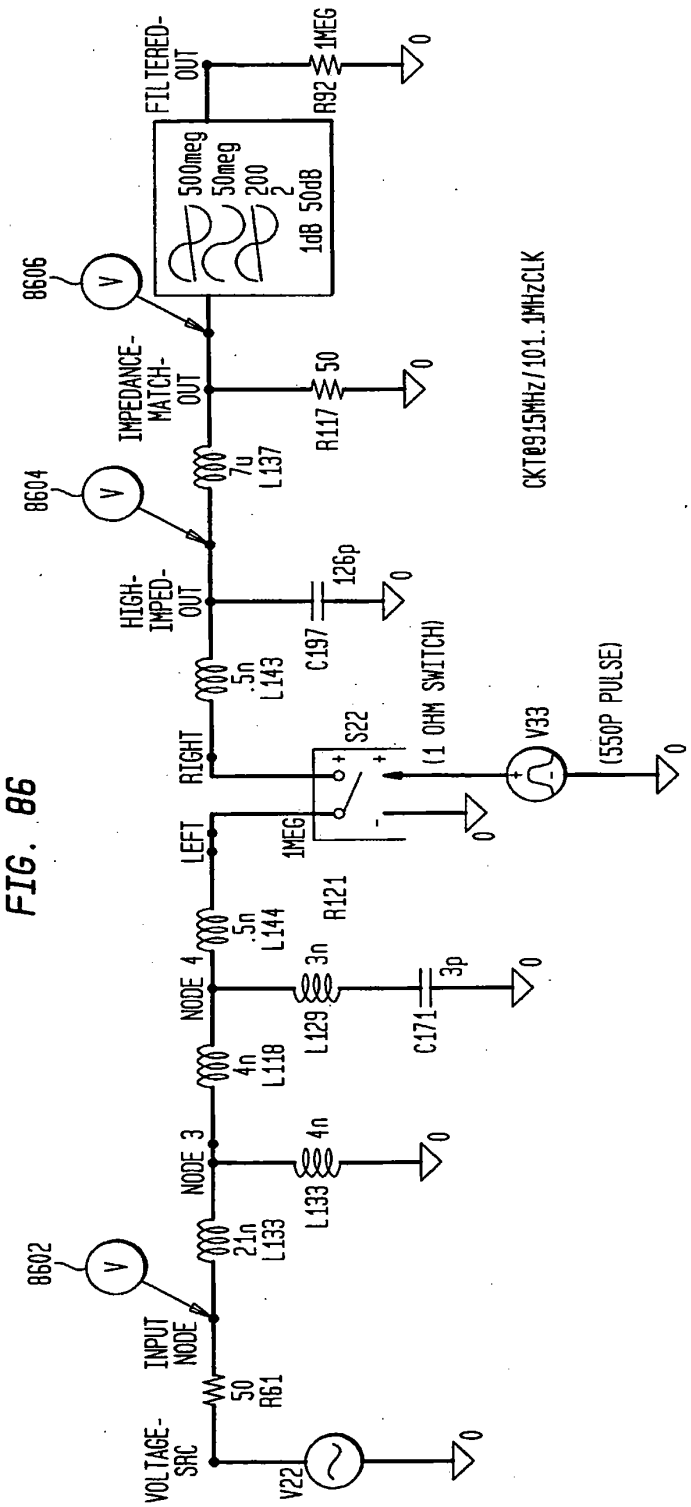
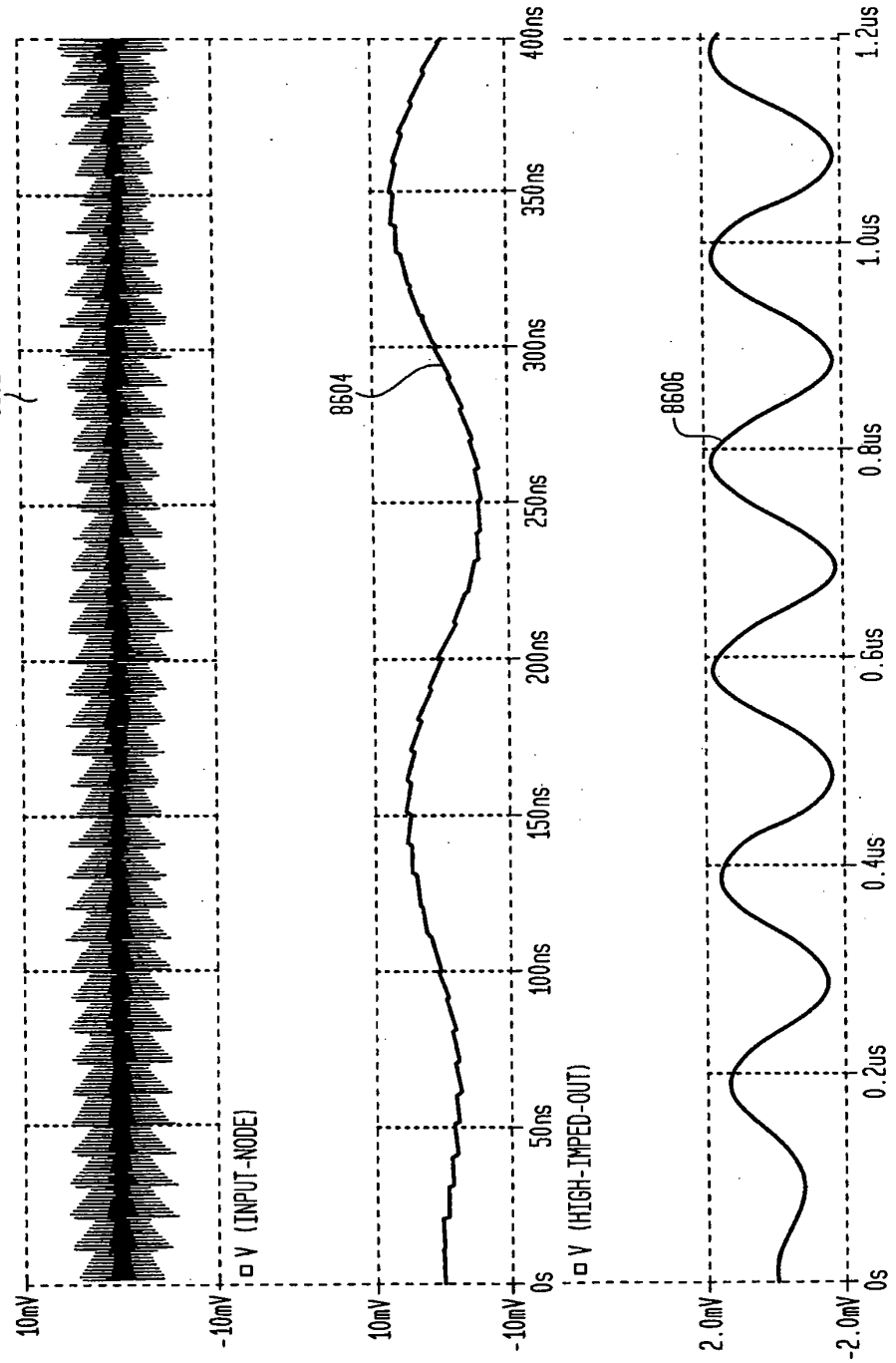

VOLTAGE-SRC
V22
0
50
R61
INPUT NODE
8602
21n
L133
NODE 3
4n
L133
0
4n
L118
NODE 4
3n
L129
3p
C171
0
.5n
L144
LEFT
1MEG
R121
0
RIGHT
S22
1 OHM SWITCH)
V33
(550P PULSE)
0
.5n
L143
HIGH-IMPED-OUT
126p
C197
0
8604
7u
L137
IMPEDANCE-MATCH-OUT
50
R117
0
8606
500meg
50meg
200
2
1dB 50dB
FILTERED-OUT
1MEG
R92
0
CKT@915MHz/101.1MHzCLK

FIG. 86

FIG. 87


8602
8604
8606
10mV
-10mV
V (INPUT-NODE)
10mV
-10mV
0s
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
V (HIGH-IMPED-OUT)
2.0mV
-2.0mV
0s
0.2us
0.4us
0.6us
0.8us
1.0us
1.2us
V (IMPEDANCE-MATCH-OUT)

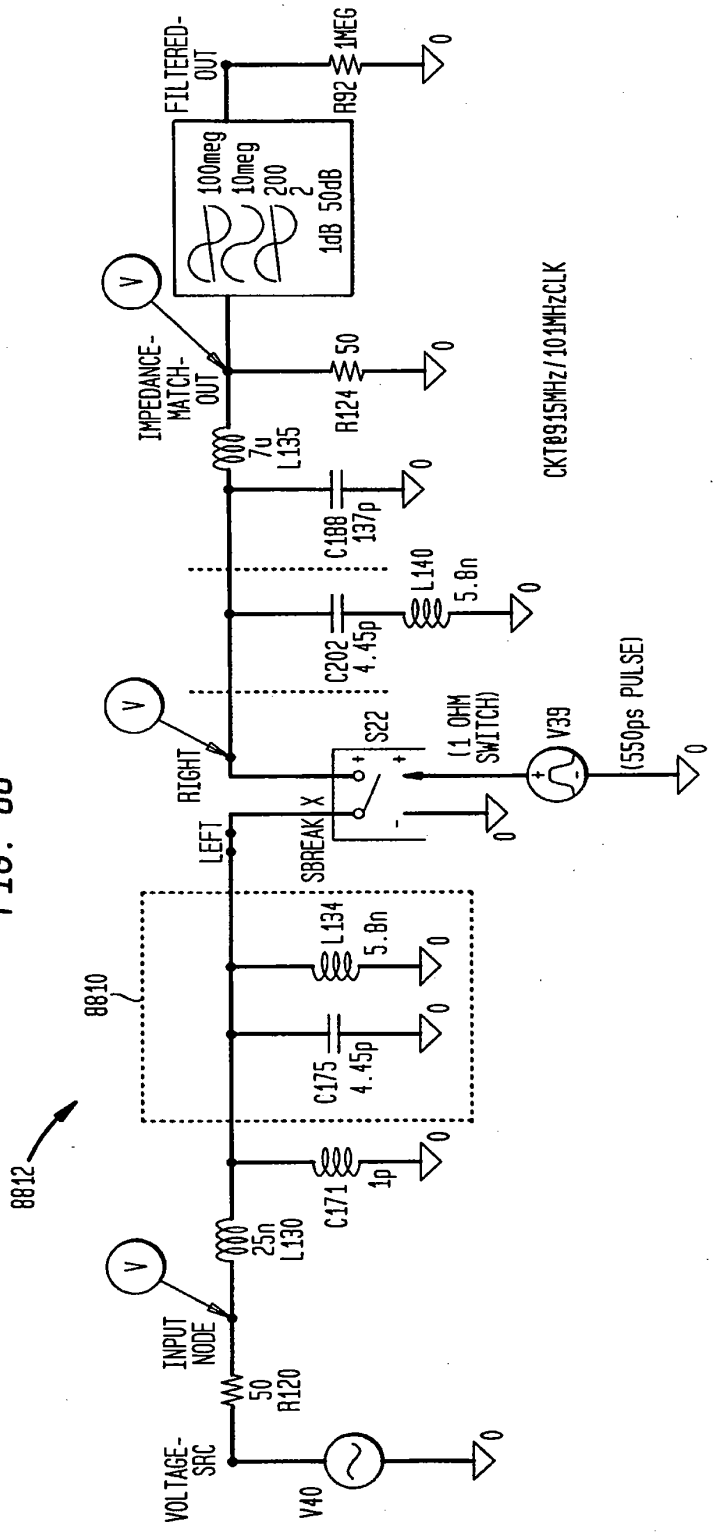

8812
8810
VOLTAGE-SRC
V40
INPUT NODE
50
R120
25n
L130
C171
1p
C175
4.45p
L134
5.8n
LEFT
SBREAK
X
S22
(1 OHM SWITCH)
V39
(550ps PULSE)
RIGHT
C202
4.45p
L140
5.8n
C188
137p
7u
L135
IMPEDANCE-MATCH-OUT
R124
50
100meg
10meg
200
2
1dB 50dB
FILTERED-OUT
R92
1MEG
CKT@915MHz/1011MHzCLK
0

FIG. 88

FIG. 89

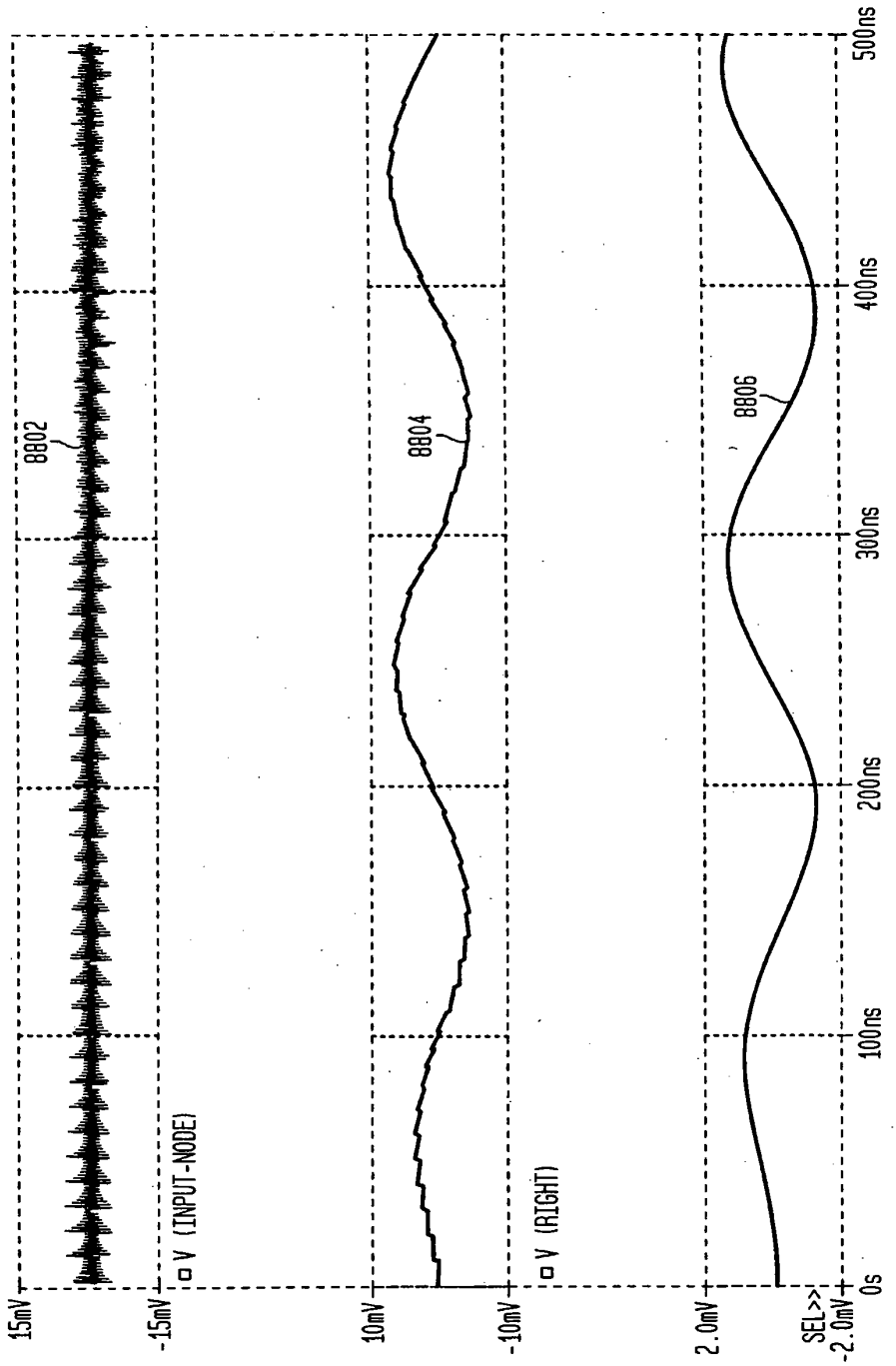

15mV
-15mV
V (INPUT-NODE)
8802
10mV
-10mV
V (RIGHT)
8804
2.0mV
SEL>>
-2.0mV
V (IMPEDANCE-MATCH-OUT)
8806
0s
100ns
200ns
300ns
400ns
500ns

FIG. 90

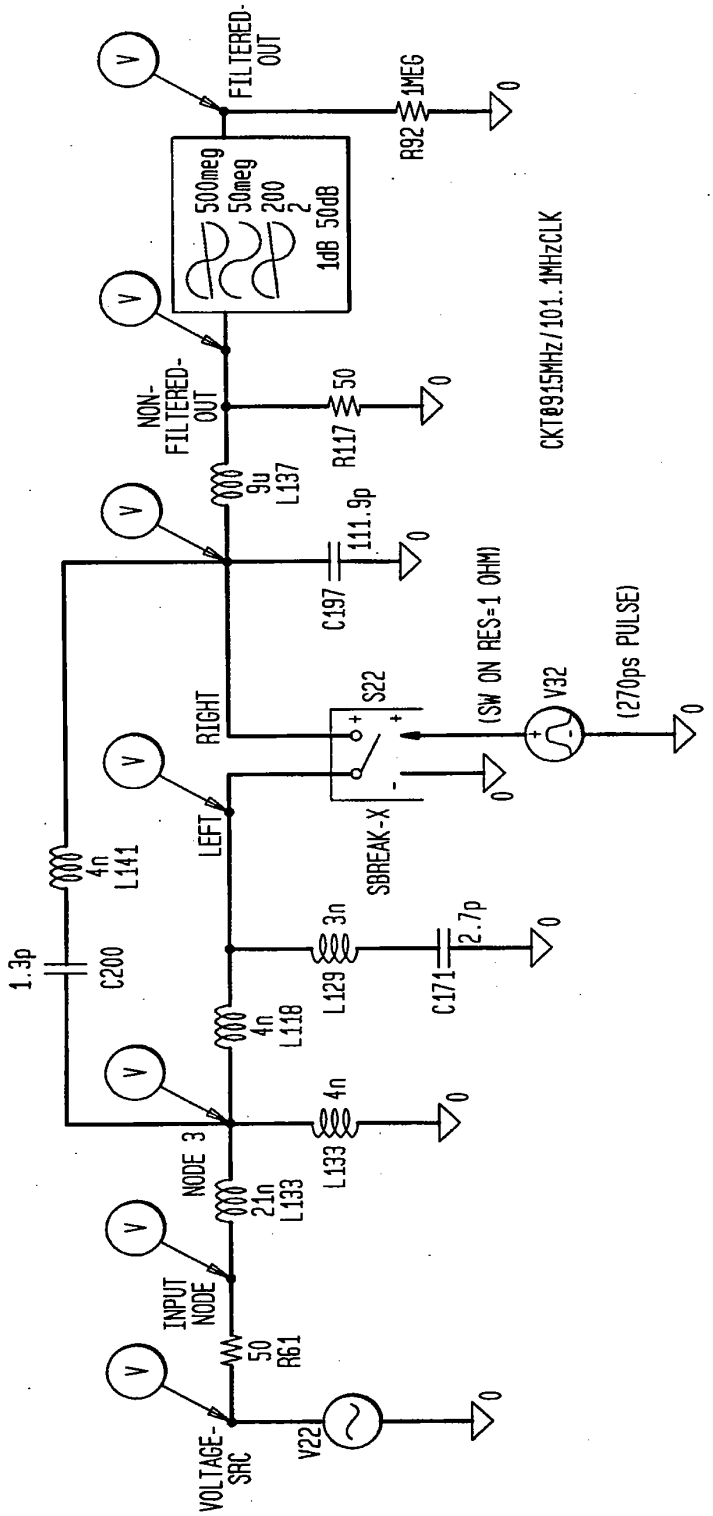
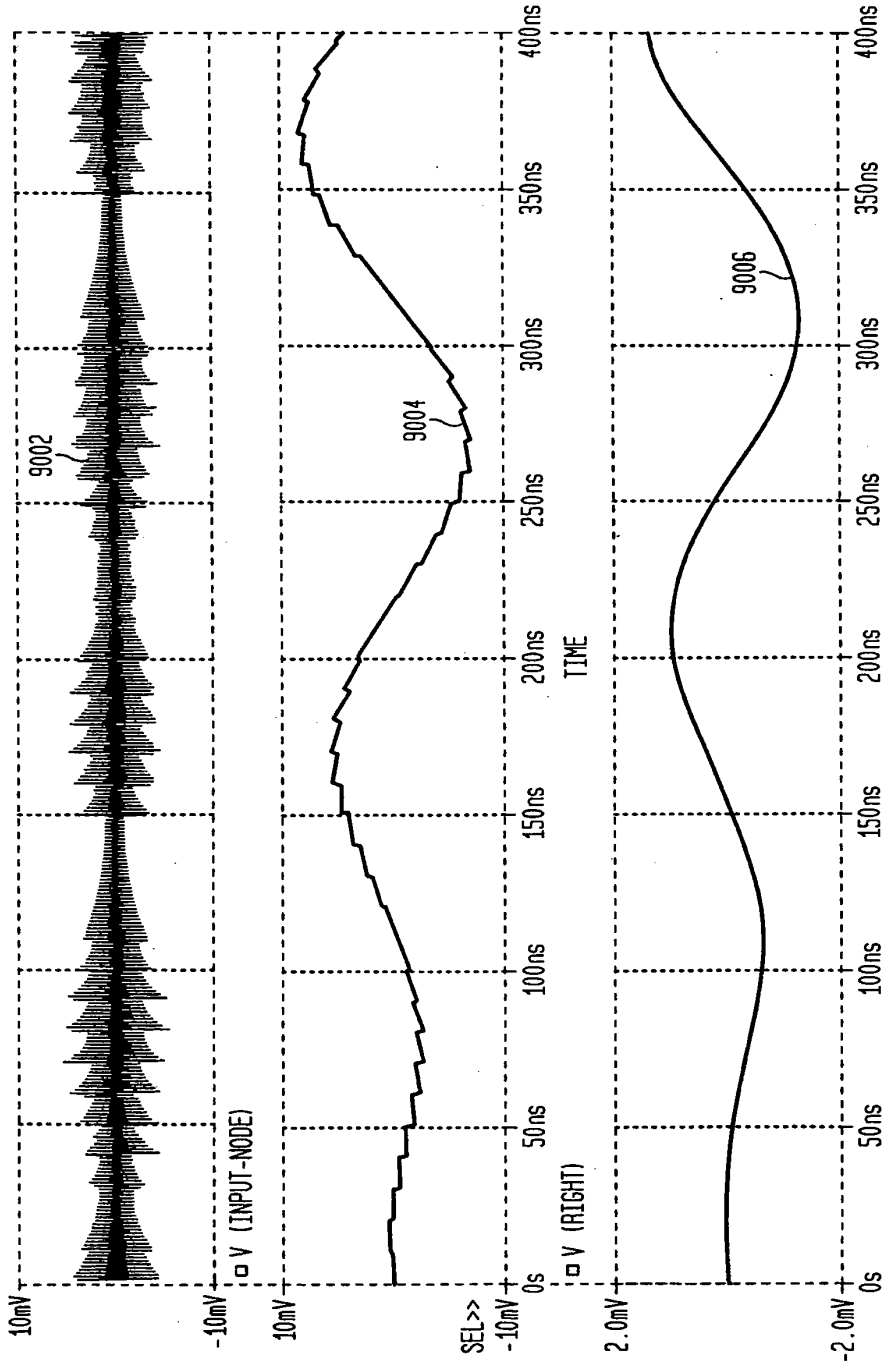

VOLTAGE-SRC
V22
50
R61
INPUT NODE
21n
L133
NODE 3
4n
L133
4n
L118
3n
L129
2.7p
C171
1.3p
C200
4n
L141
LEFT
SBREAK-X
S22
RIGHT
111.9p
C197
9u
L137
NON-FILTERED-OUT
50
R117
500meg
50meg
200
2
1dB 50dB
FILTERED-OUT
1MEG
R92
(SW ON RES=1 OHM)
V32
(270ps PULSE)
CKT@915MHz/101.1MHzCLK
0

FIG. 91


9002
9004
9006
10mV
-10mV
10mV
SEL>>
-10mV
2.0mV
-2.0mV
0s
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
TIME
V (INPUT-NODE)
V (RIGHT)
V (NON-FILTERED-OUT)

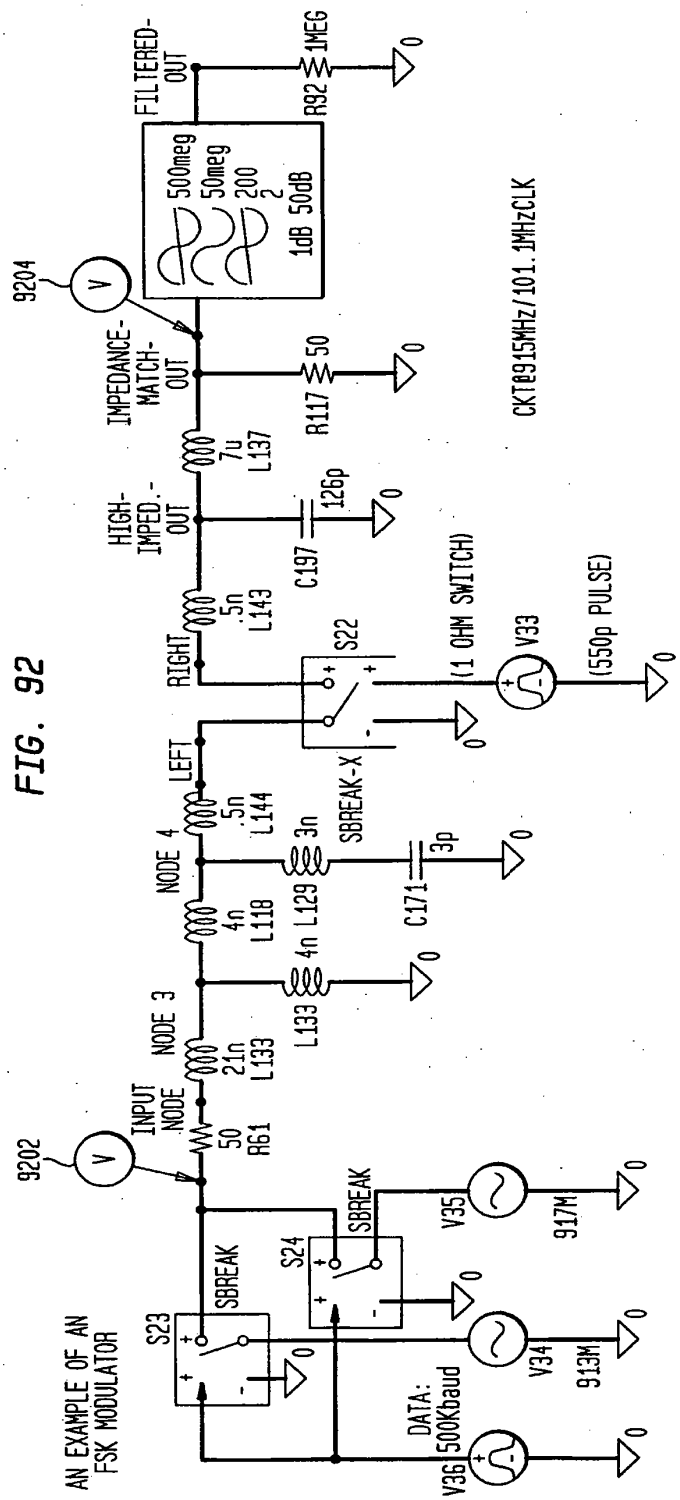

AN EXAMPLE OF AN FSK MODULATOR
9202
INPUT NODE
50 R61
21n L133
NODE 3
4n L133
4n L118
NODE 4
3n L129
.5n L144
LEFT
3p C171
SBREAK-X
.5n L143
RIGHT
126p C197
HIGH-IMPED.-OUT
7u L137
IMPEDANCE-MATCH-OUT
50 R117
9204
500meg 50meg 200 2 1dB 50dB
FILTERED-OUT
1MEG R92
S22
(1 OHM SWITCH)
V33
(550p PULSE)
S23
SBREAK
S24
SBREAK
V35
917M
V34
913M
DATA: 500Kbaud
V36
CKT@915MHz/101.1MHzCLK
0

FIG. 92

FIG. 93

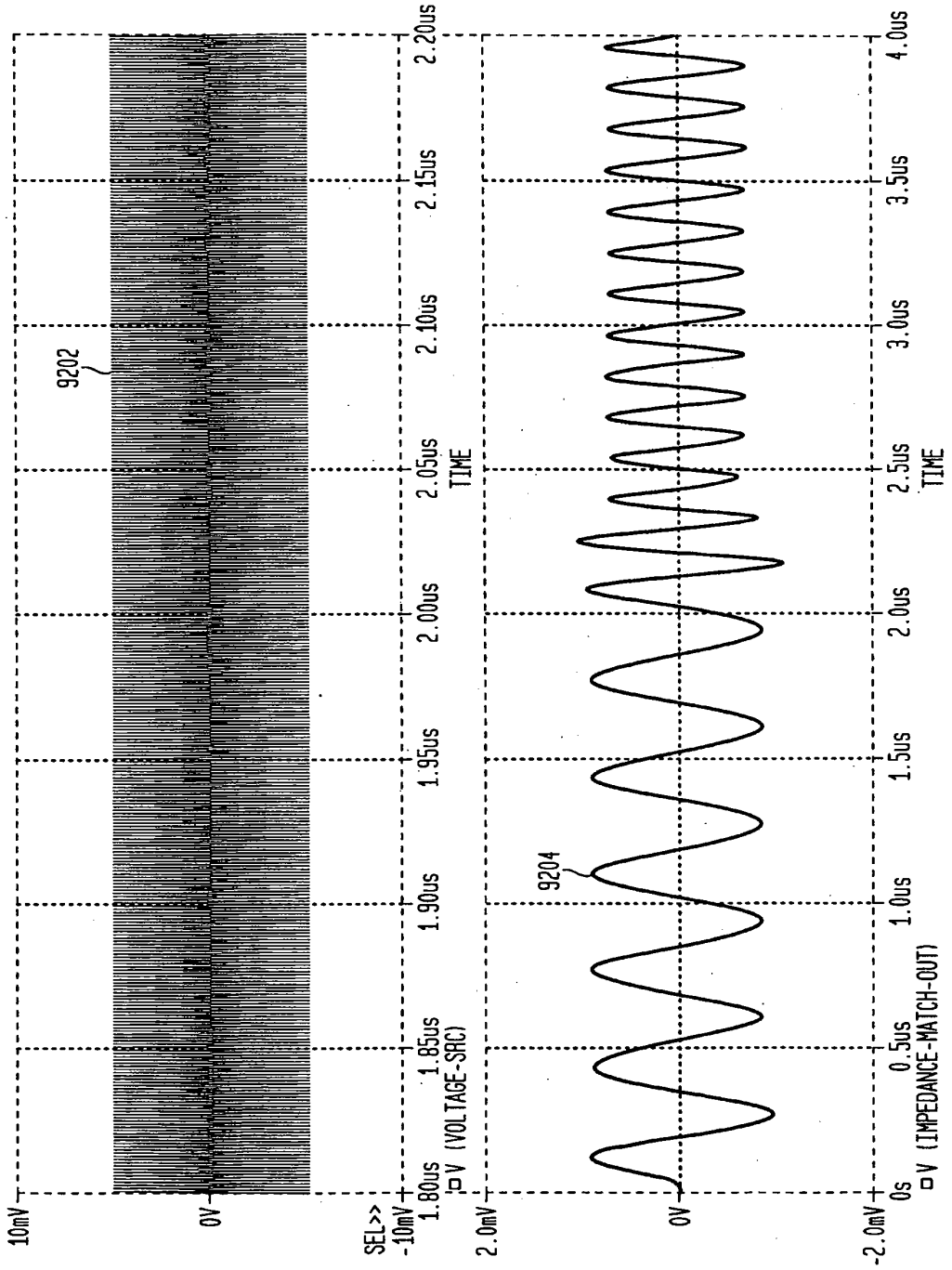
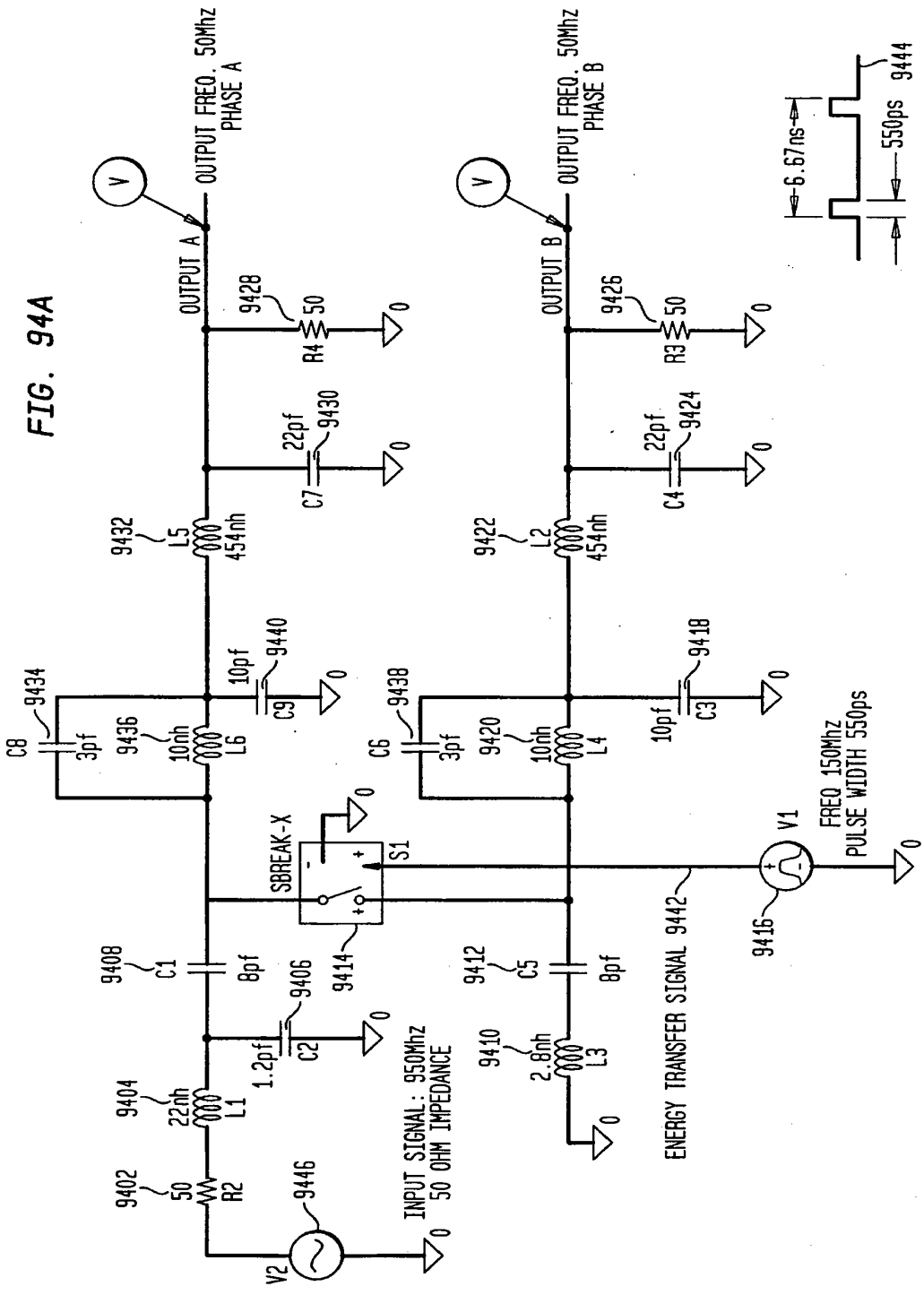

9202
9204
10mV
0V
SEL>>
-10mV
1.80us
1.85us
1.90us
1.95us
2.00us
2.05us
2.10us
2.15us
2.20us
TIME
V (VOLTAGE-SRC)
2.0mV
0V
-2.0mV
0s
0.5us
1.0us
1.5us
2.0us
2.5us
3.0us
3.5us
4.0us
TIME
V (IMPEDANCE-MATCH-OUT)

FIG. 94A


OUTPUT FREQ. 50Mhz
PHASE A
OUTPUT A
9428
R4
50
22pf
9430
C7
9432
L5
454nh
10pf
9440
C9
9434
C8
3pf
9436
10nh
L6
SBREAK-X
S1
9414
9408
C1
8pf
9406
1.2pf
C2
9404
22nh
L1
9402
50
R2
9446
V2
INPUT SIGNAL: 950Mhz
50 OHM IMPEDANCE
OUTPUT FREQ. 50Mhz
PHASE B
OUTPUT B
9426
R3
50
22pf
9424
C4
9422
L2
454nh
10pf
9418
C3
9438
C6
3pf
9420
10nh
L4
9412
C5
8pf
9410
2.8nh
L3
ENERGY TRANSFER SIGNAL 9442
9416
V1
FREQ 150Mhz
PULSE WIDTH 550ps
6.67ns
550ps
9444

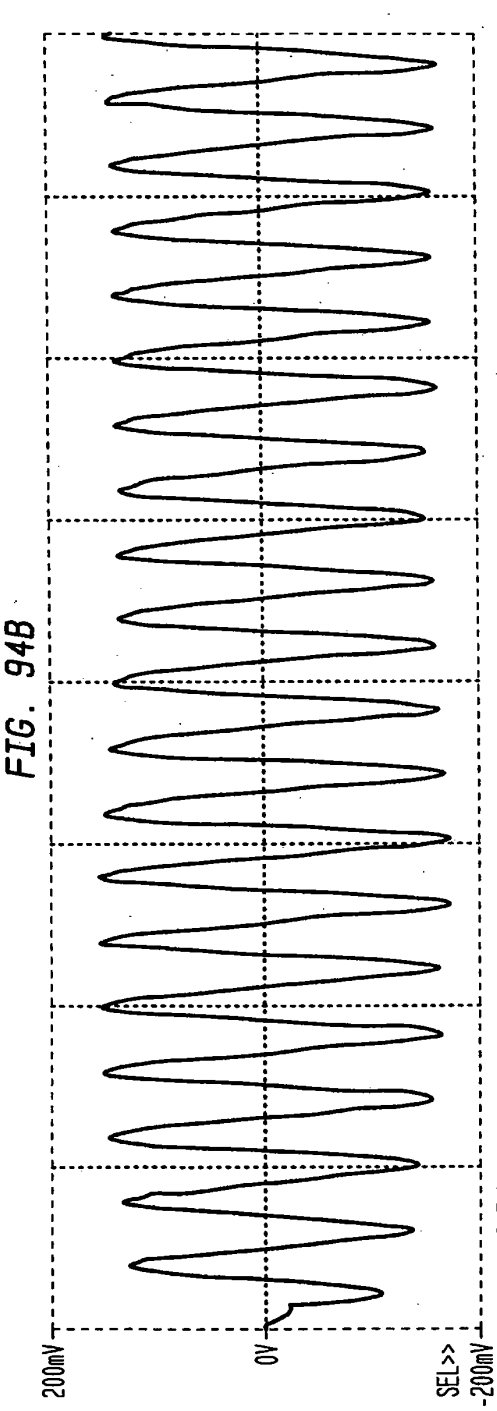


FIG. 94B

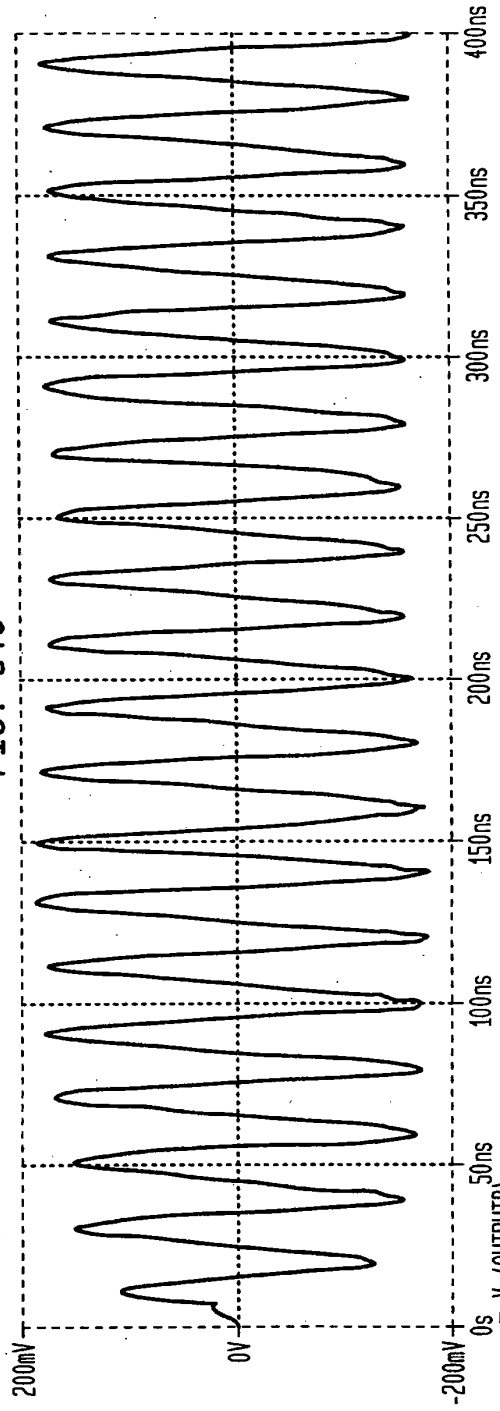


FIG. 94C

FIG. 95

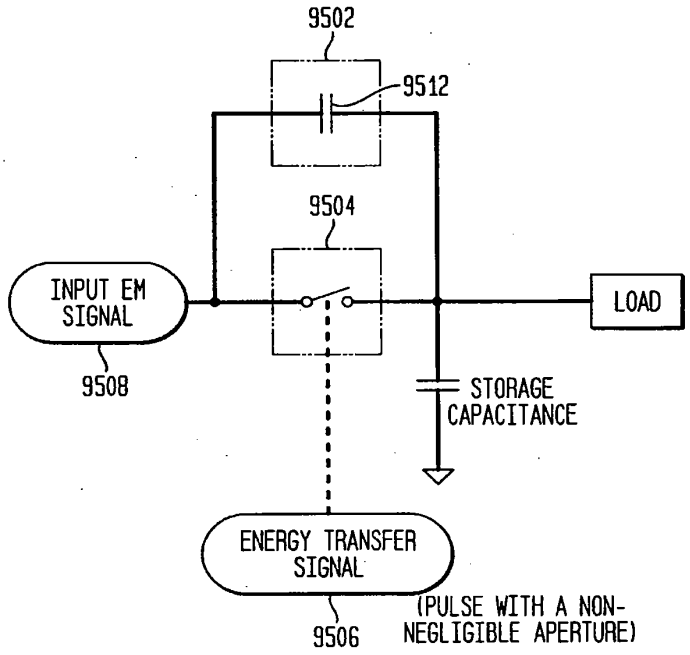
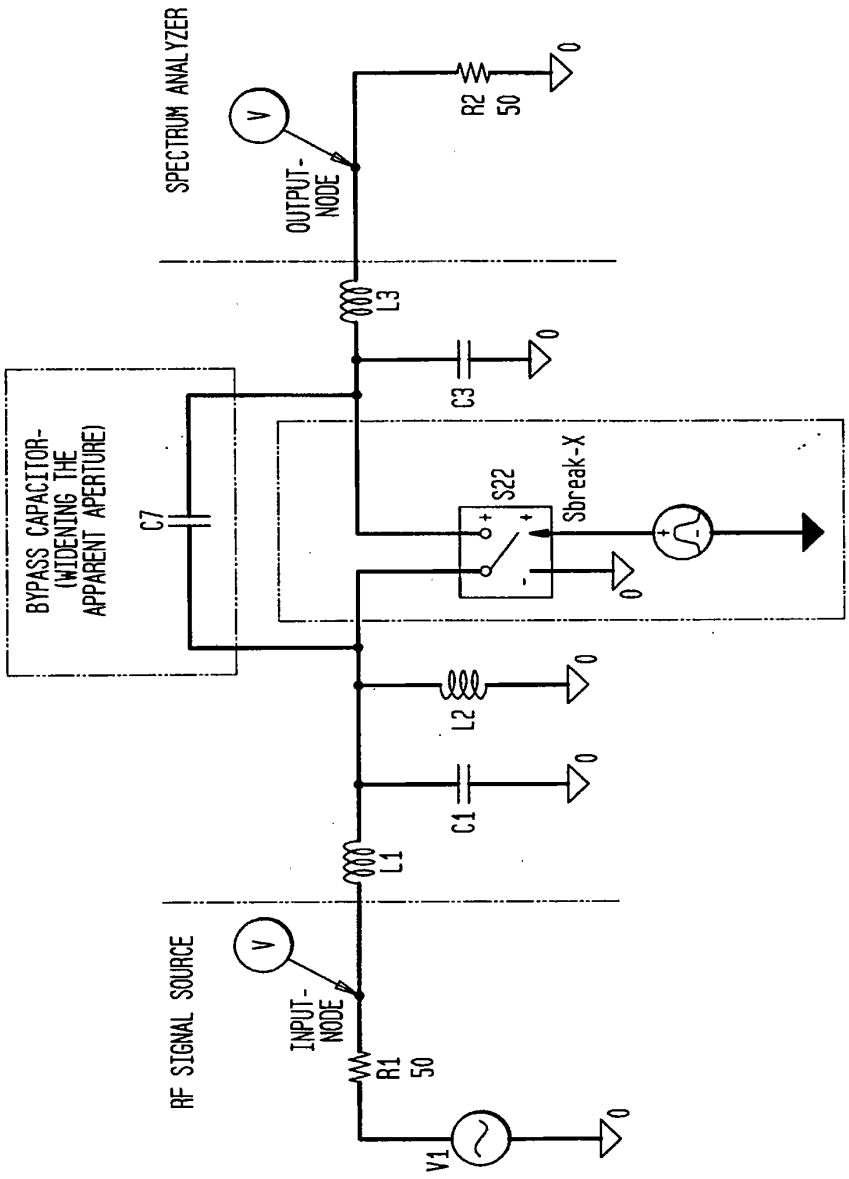

9502
9512
9504
INPUT EM SIGNAL
9508
LOAD
STORAGE CAPACITANCE
ENERGY TRANSFER SIGNAL
9506
(PULSE WITH A NON-NEGLIGIBLE APERTURE)

FIG. 96


SPECTRUM ANALYZER
OUTPUT-NODE
R2
50
0
L3
C3
BYPASS CAPACITOR-(WIDENING THE APPARENT APERTURE)
C7
S22
Sbreak-X
L2
C1
L1
RF SIGNAL SOURCE
INPUT-NODE
R1
50
V1

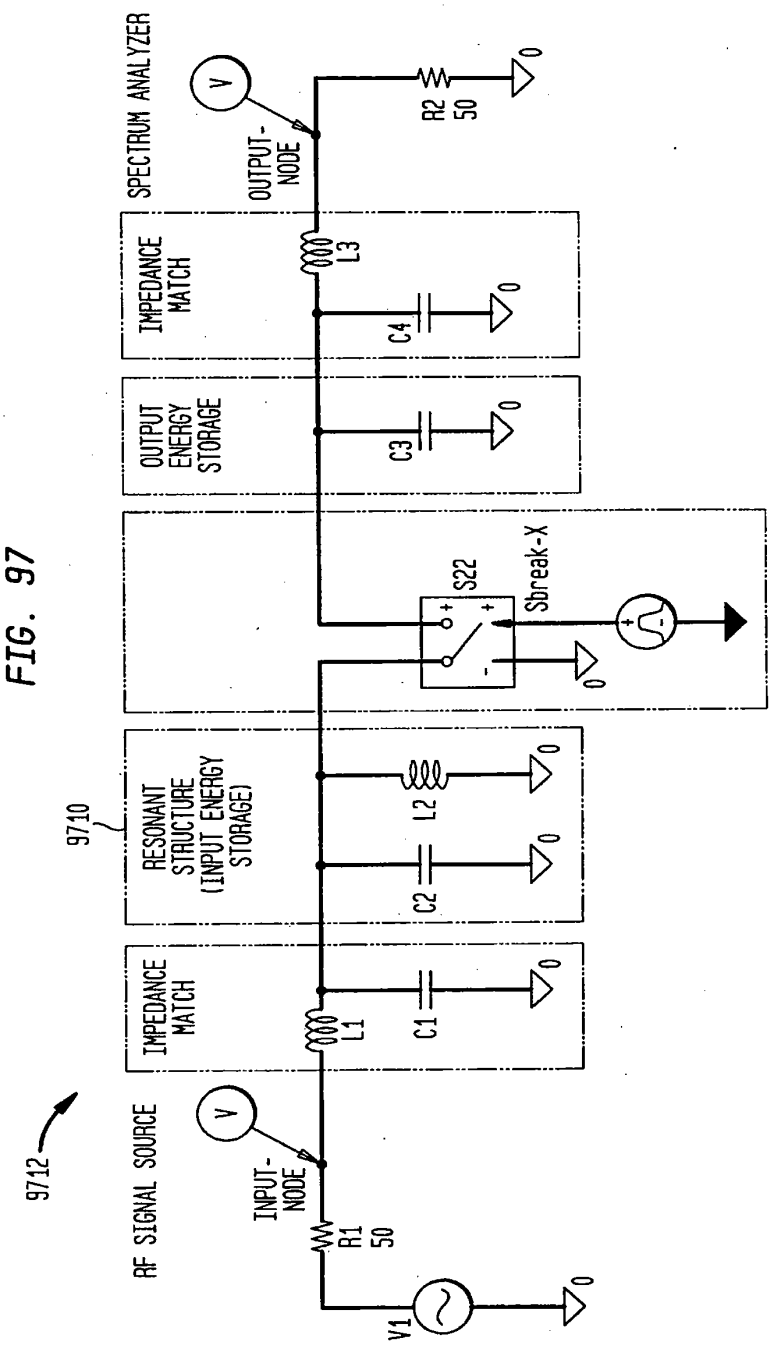
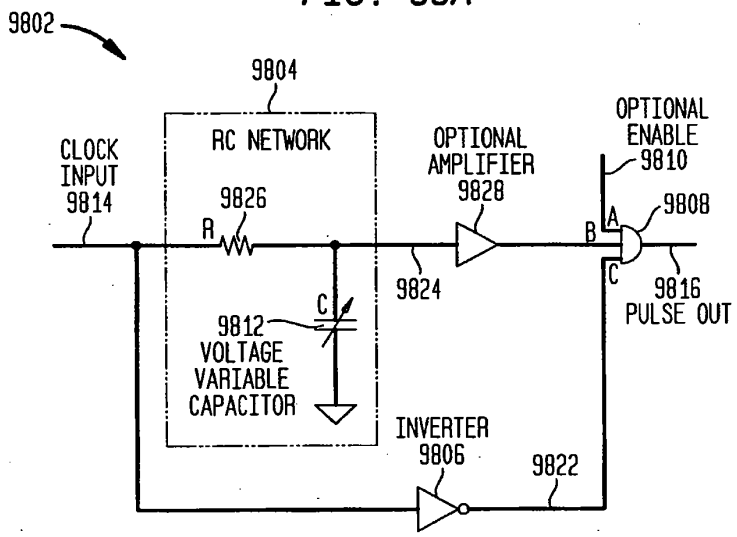

RF SIGNAL SOURCE
9712
INPUT-
NODE
R1
50
V1
IMPEDANCE
MATCH
L1
C1
9710
RESONANT
STRUCTURE
(INPUT ENERGY
STORAGE)
L2
C2
S22
Sbreak-X
OUTPUT
ENERGY
STORAGE
C3
IMPEDANCE
MATCH
L3
C4
OUTPUT-
NODE
SPECTRUM ANALYZER
R2
50
0

FIG. 97

FIG. 98A


9802
9804
RC NETWORK
CLOCK INPUT 9814
9826
R
C
9812 VOLTAGE VARIABLE CAPACITOR
OPTIONAL AMPLIFIER 9828
9824
OPTIONAL ENABLE 9810
9808
A
B
C
9816 PULSE OUT
INVERTER 9806
9822

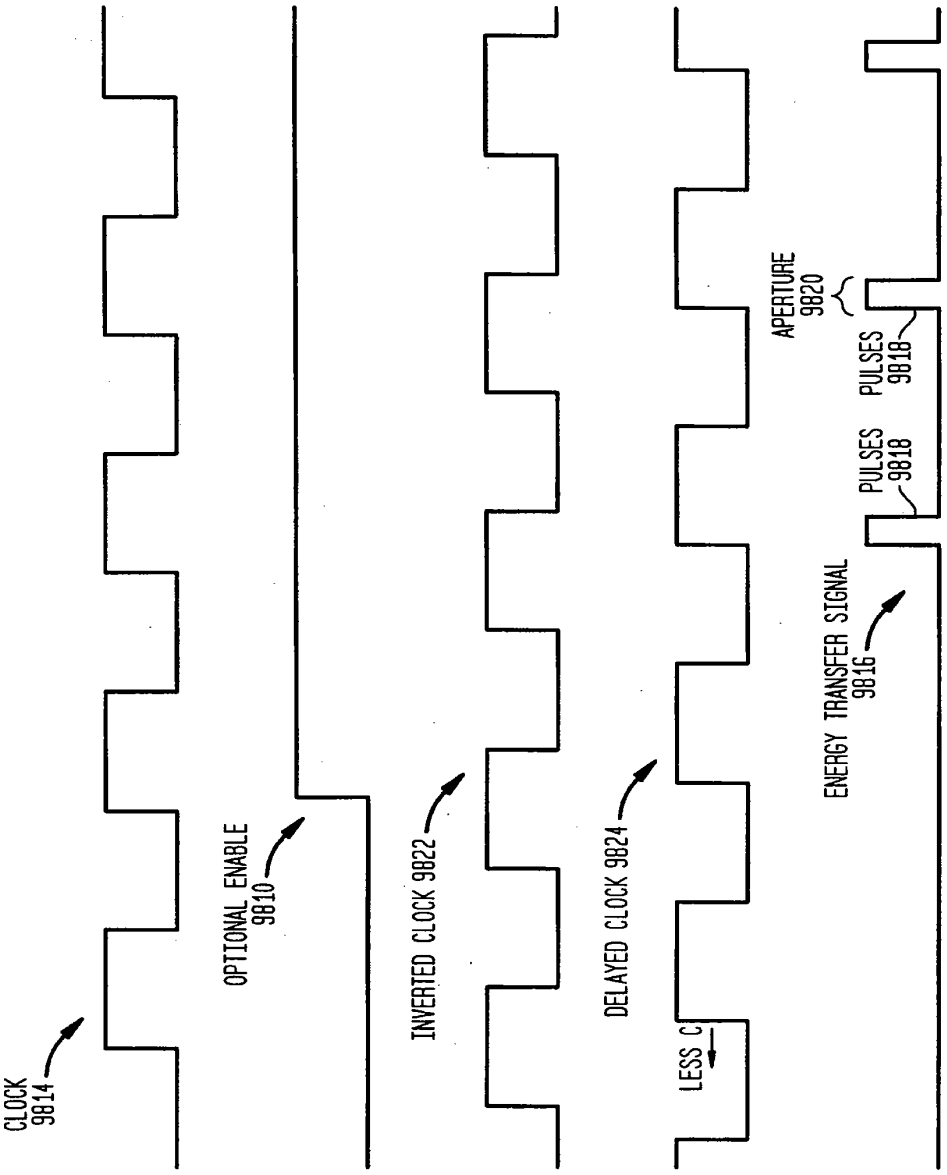


FIG. 98B FIG. 98C FIG. 98D FIG. 98E FIG. 98F

FIG. 99

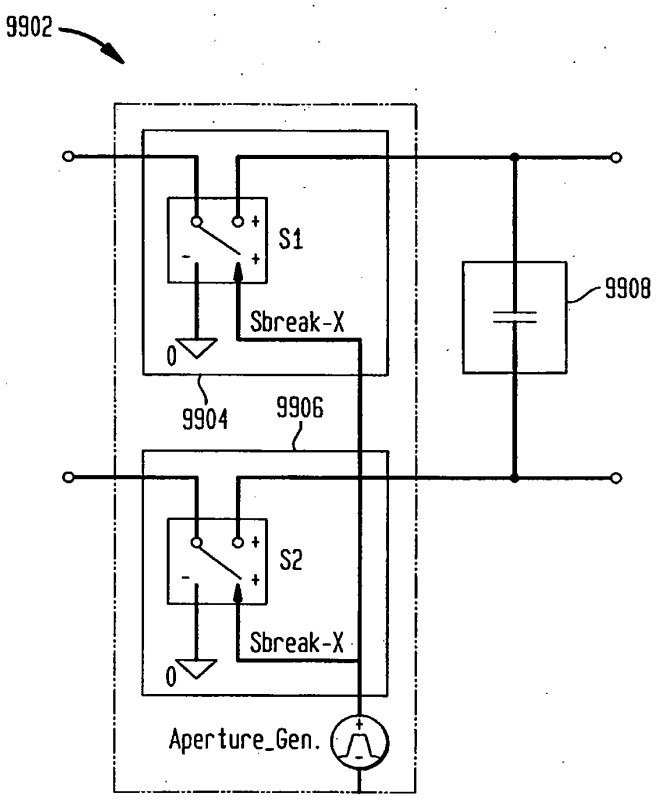


FIG. 100

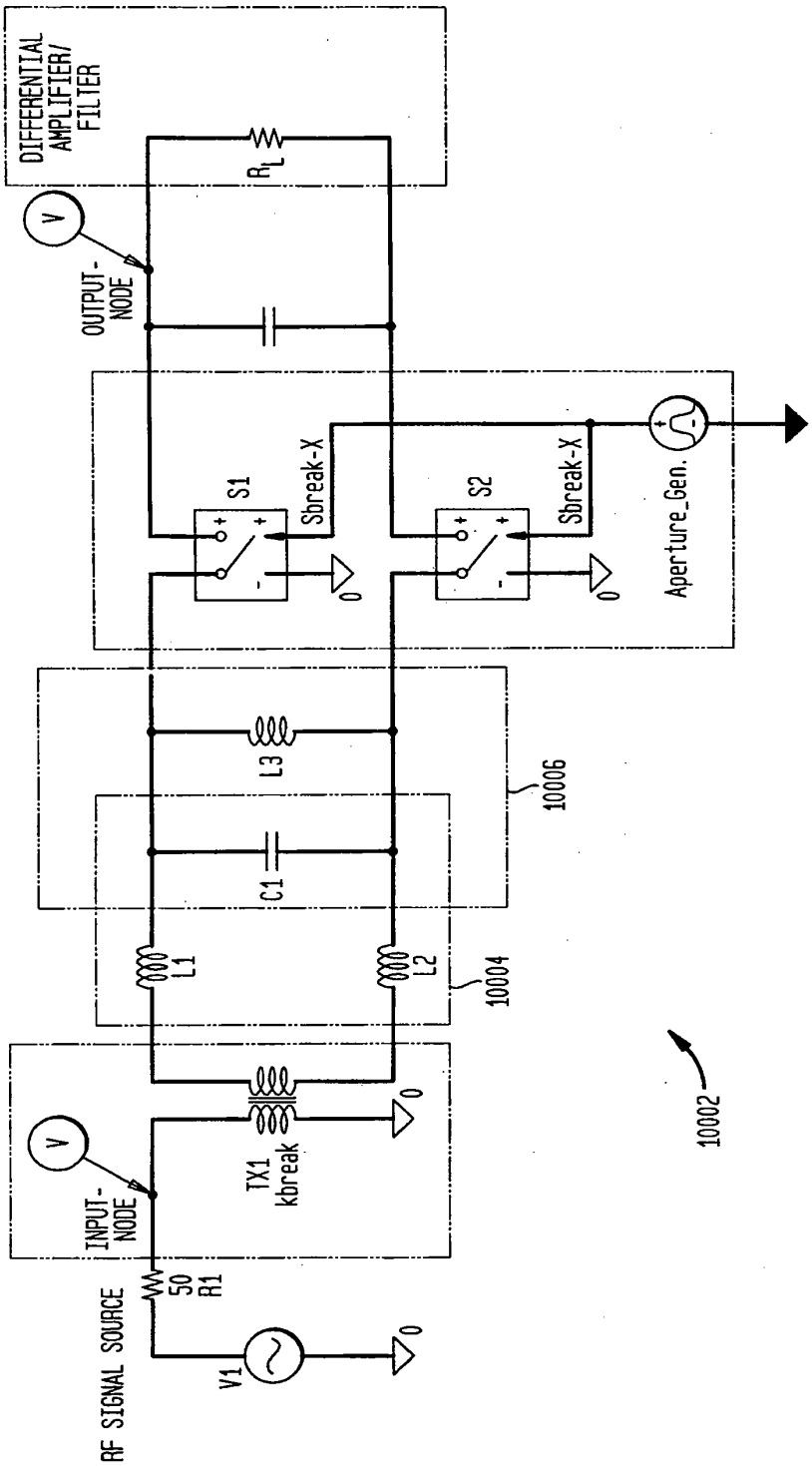

DIFFERENTIAL AMPLIFIER/ FILTER
R_L
V
OUTPUT-NODE
S1
Sbreak-X
S2
Sbreak-X
Aperture_Gen.
0
L3
C1
10006
L1
L2
10004
TX1
kbreak
INPUT-NODE
RF SIGNAL SOURCE
50
R1
V1
10002

FIG. 101

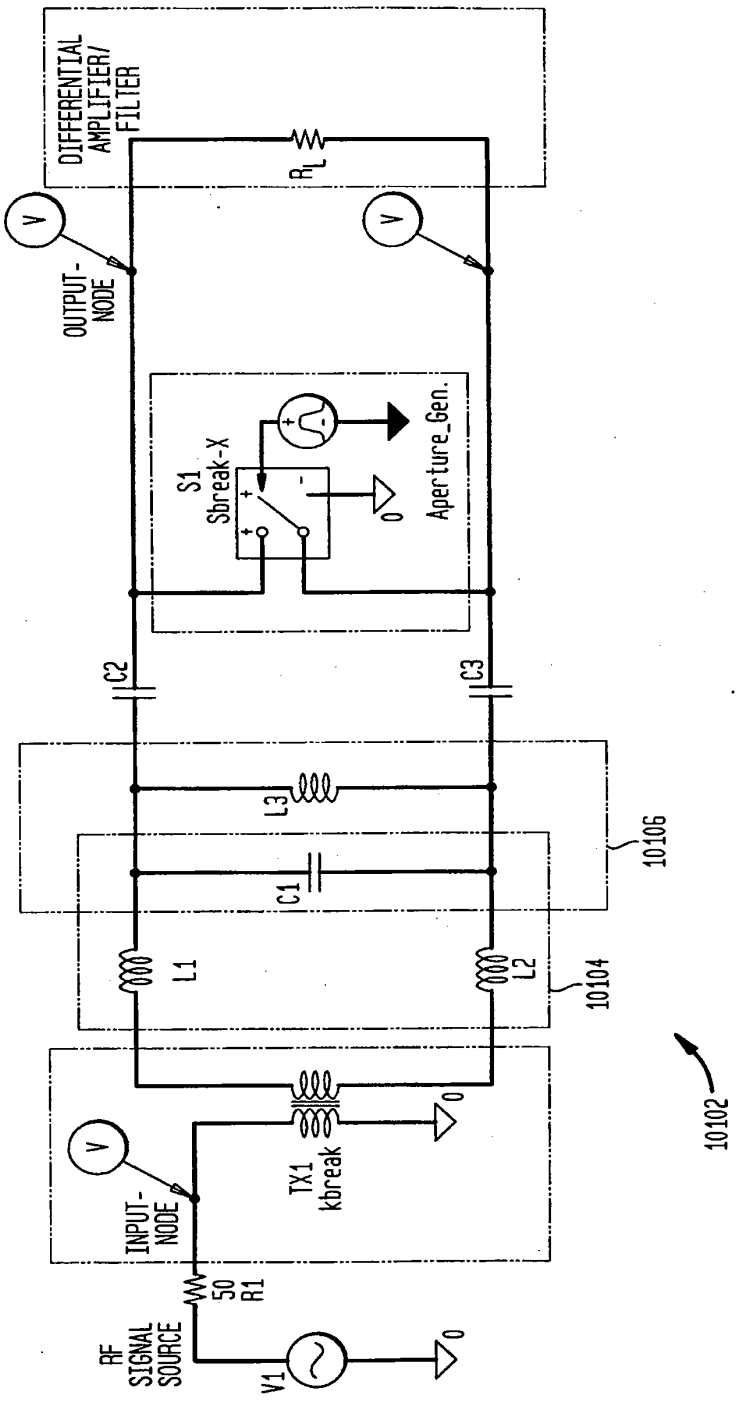

DIFFERENTIAL AMPLIFIER/ FILTER
R_L
V
OUTPUT-NODE
S1
Sbreak-X
Aperture_Gen.
0
C2
C3
L3
C1
L1
L2
10106
10104
10102
TX1
kbreak
INPUT-NODE
50
R1
RF SIGNAL SOURCE
V1

FIG. 102

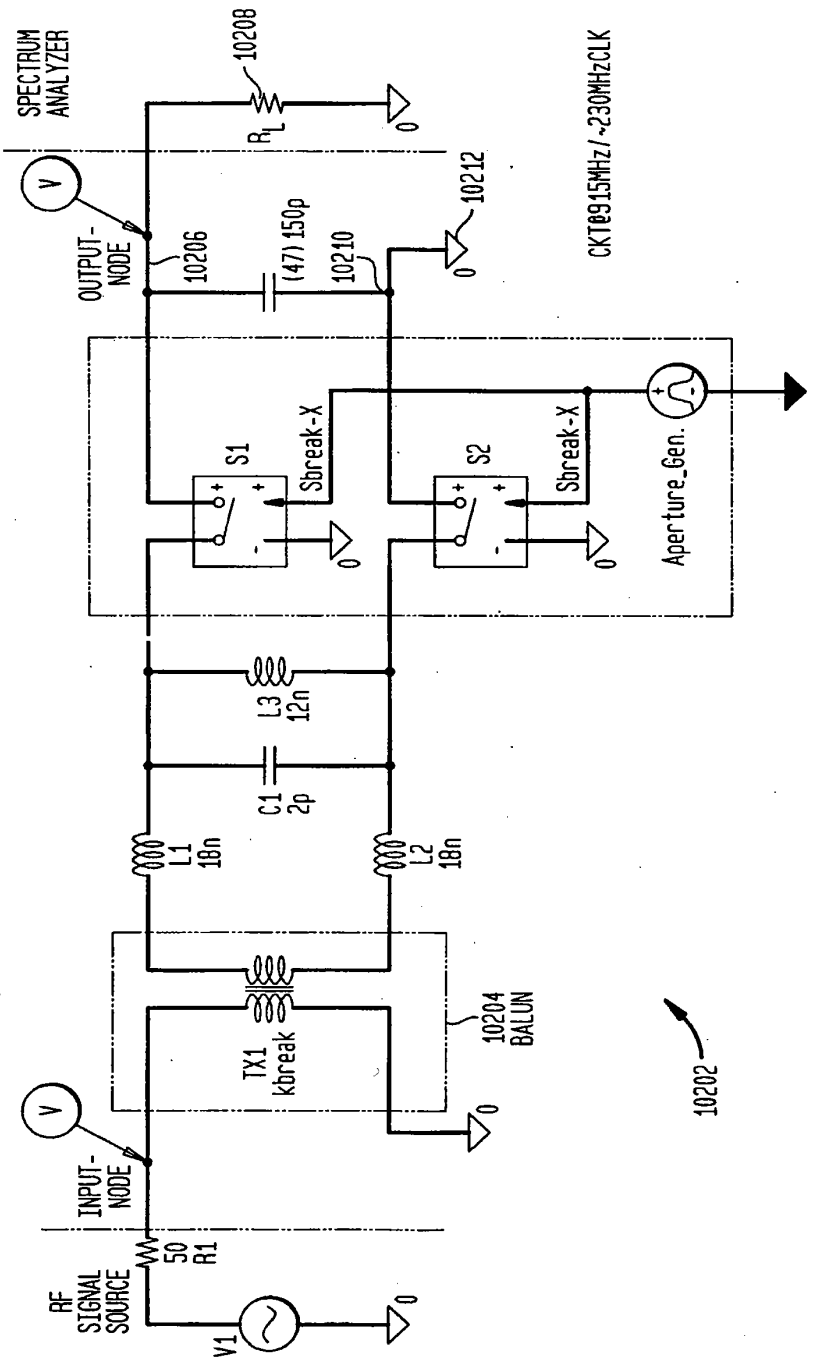

SPECTRUM ANALYZER
10208
R_L
OUTPUT-NODE
10206
(47) 150p
10210
10212
CKT@915MHz/~230MHzCLK
S1
Sbreak-X
S2
Sbreak-X
Aperture_Gen.
L3 12n
C1 2p
L1 18n
L2 18n
TX1 kbreak
10204 BALUN
10202
INPUT-NODE
50 R1
RF SIGNAL SOURCE
V1
0

FIG. 103

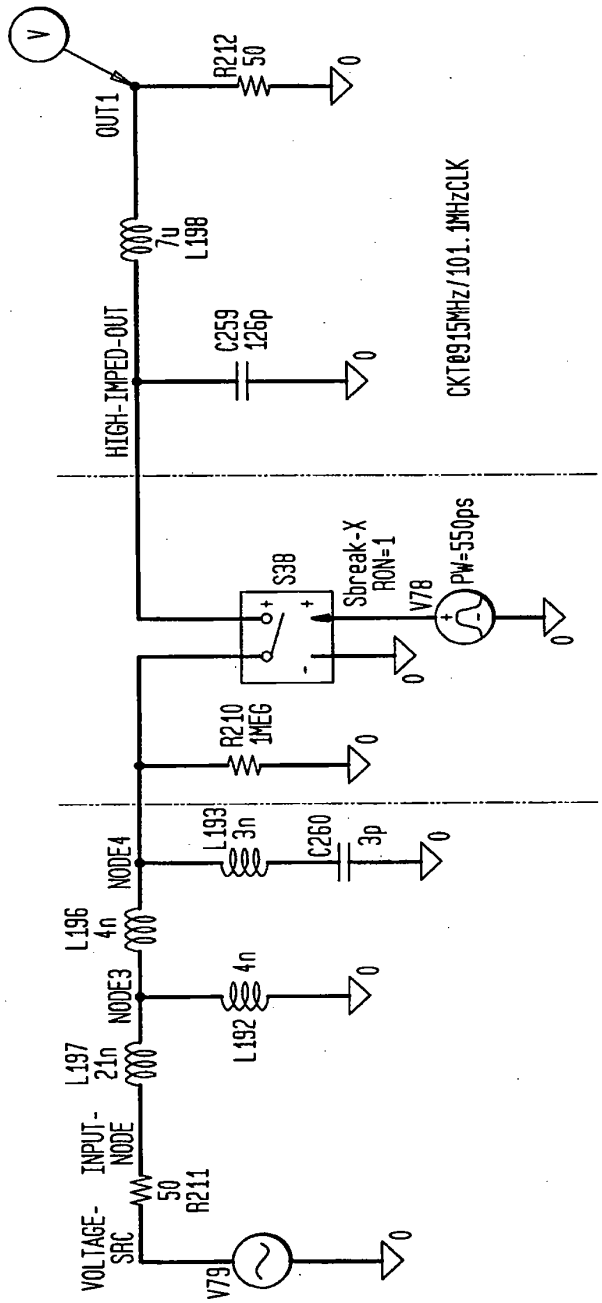

V
OUT1
R212
50
0
7u
L198
HIGH-IMPED-OUT
C259
126p
CKT8915MHz/101.1MHzCLK
S3B
Sbreak-X
RON=1
V78
PW=550ps
R210
1MEG
L193
3n
C260
3p
NODE4
L196
4n
NODE3
4n
L192
L197
21n
INPUT-
NODE
50
R211
VOLTAGE-
SRC
V79

FIG. 104

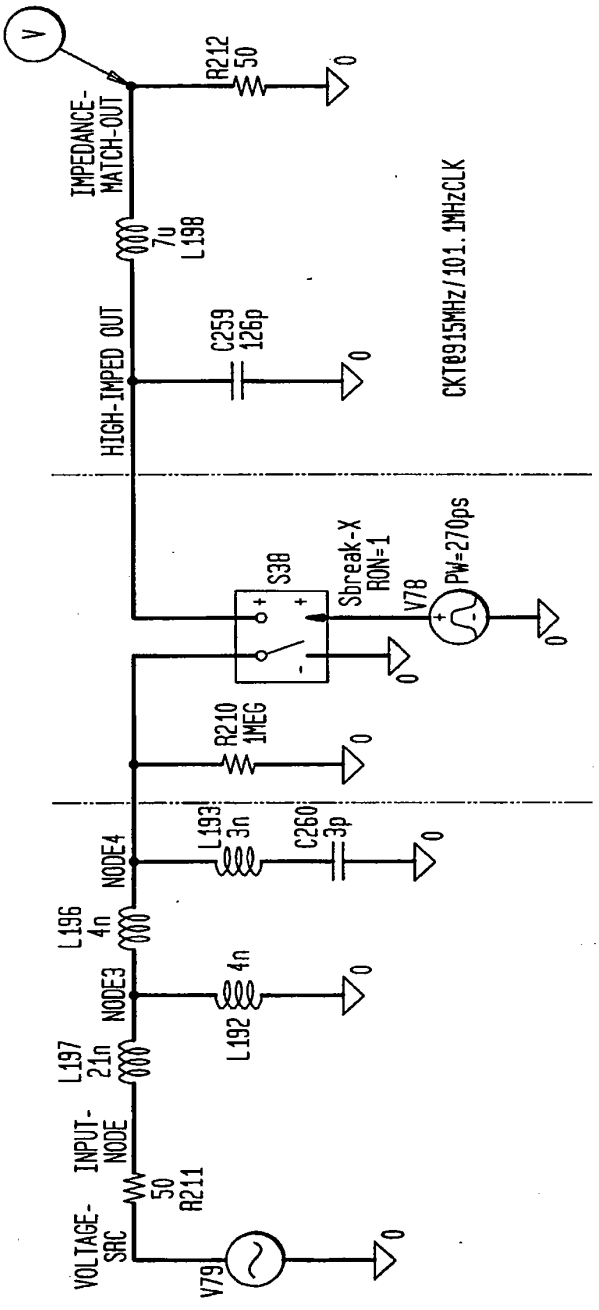

V
IMPEDANCE-MATCH-OUT
R212 50
0
7u L198
HIGH-IMPED OUT
C259 126p
CKT@915MHz/101.1MHzCLK
S38
Sbreak-X RON=1
V78 PW=270ps
R210 1MEG
L193 3n
C260 3p
NODE4
L196 4n
NODE3
4n L192
L197 21n
INPUT-NODE
50 R211
VOLTAGE-SRC
V79

FIG. 105

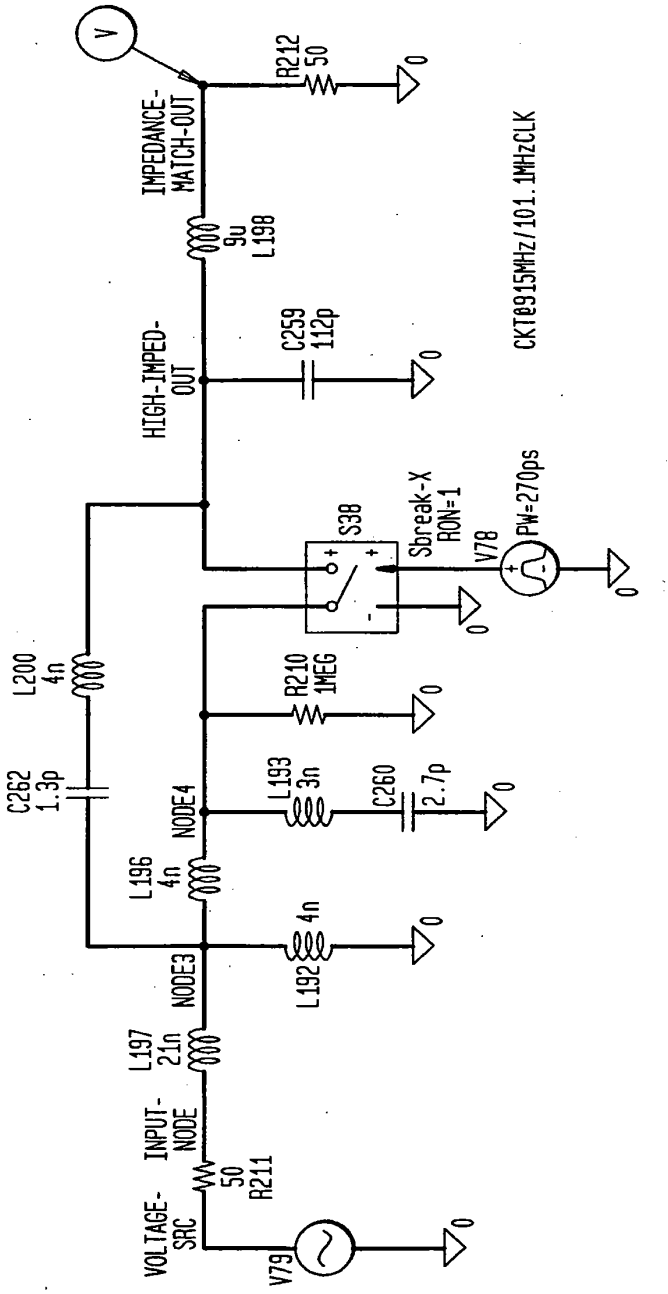

V
R212
50
0
IMPEDANCE-
MATCH-OUT
9u
L198
C259
112p
HIGH-IMPED-
OUT
S38
Sbreak-X
RON=1
V78
PW=270ps
CKT@915MHz/101.1MHzCLK
L200
4n
R210
1MEG
C262
1.3p
L193
3n
C260
2.7p
NODE4
L196
4n
4n
L192
NODE3
L197
21n
INPUT-
NODE
50
R211
VOLTAGE-
SRC
V79

FIG. 106

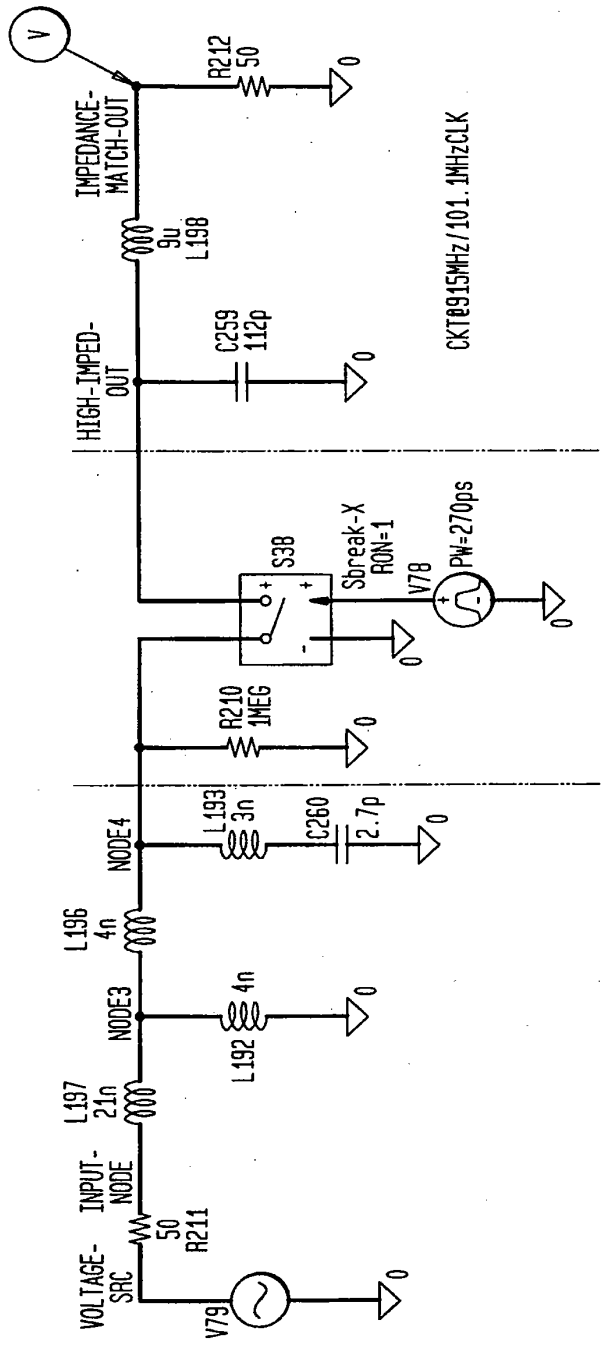
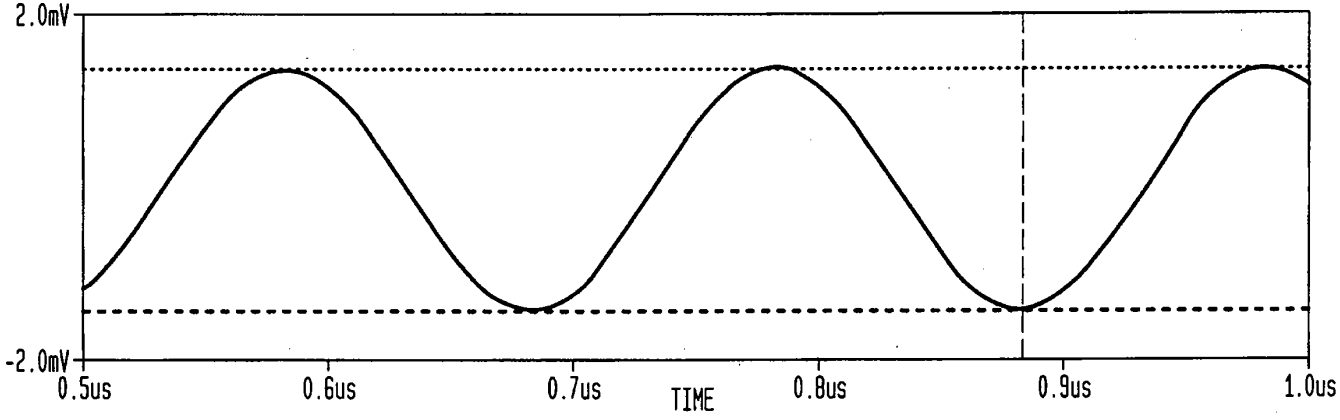
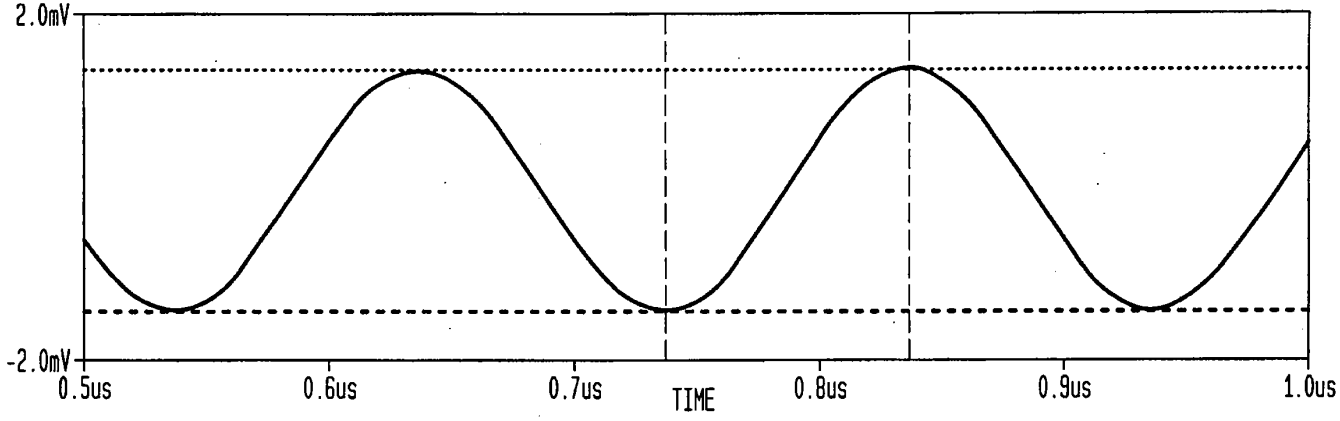

V
R212
50
0
IMPEDANCE-
MATCH-OUT
9u
L198
C259
112p
0
HIGH-IMPED-
OUT
CKT@915MHz/101.1MHzCLK
S3B
Sbreak-X
RON=1
V78
PW=270ps
0
0
R210
1MEG
0
L193
3n
C260
2.7p
0
NODE4
L196
4n
NODE3
4n
L192
0
L197
21n
INPUT-
NODE
50
R211
VOLTAGE-
SRC
V79
0

FIG. 107A



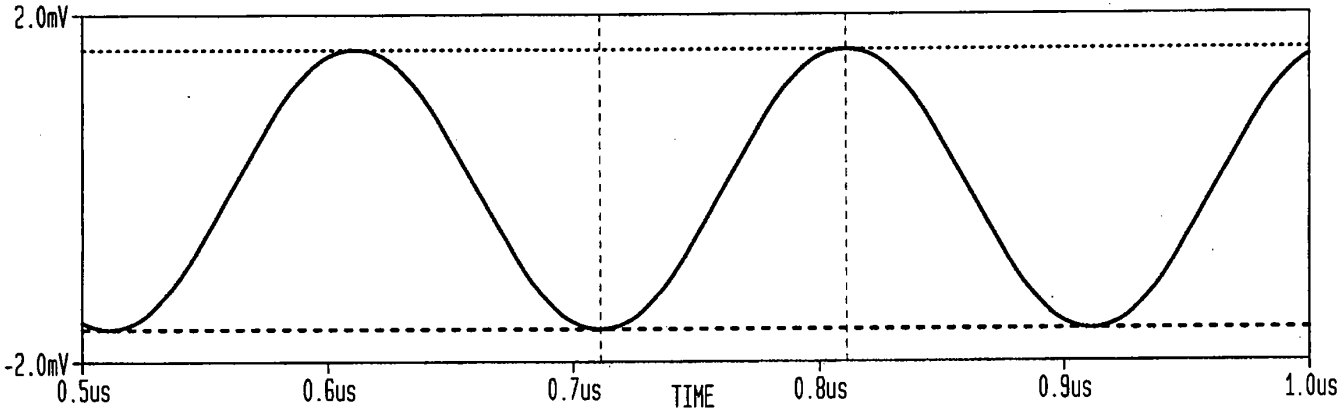
V(out1)
E1: (981.86n, 1.404m) E2: (883.04n, -1.402m) DIFF(E): (98.82n, 2.806m)
F1: (837.43n, 1.253m) F2: (738.01n, -1.252m) DIFF(F): (99.42n, 2.505m)

FIG. 107B



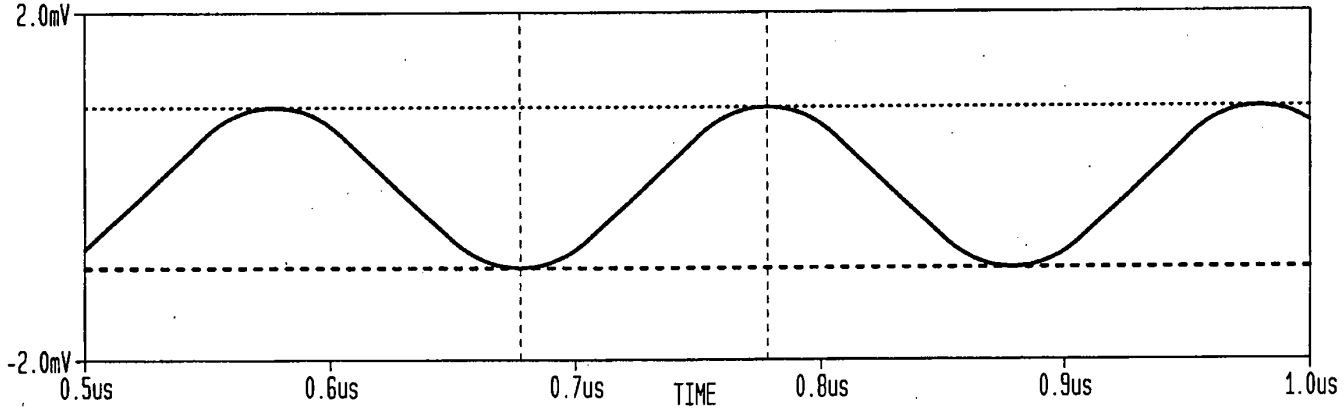
V(impedance-match-out)
E1: (981.86n, 1.404m) E2: (883.04n, -1.402m) DIFF(E): (98.82n, 2.806m)
F1: (837.43n, 1.253m) F2: (738.01n, -1.252m) DIFF(F): (99.42n, 2.505m)

FIG. 108A



V(impedance-match-out)
A1: (810.53n, 1.642m) A2: (710.52n, -1.621m) DIFF(A): (100.01n, 3.263m)
B1: (777.78n, 942.32u) B2: (677.18n, -942.51u) DIFF(B): (100.60n, 1.885m)

FIG. 108B



V(impedance-match-out)
A1: (810.53n, 1.642m) A2: (710.52n, -1.621m) DIFF(A): (100.01n, 3.263m)
B1: (777.78n, 942.32u) B2: (677.18n, -942.51u) DIFF(B): (100.60n, 1.885m)

FIG. 109A

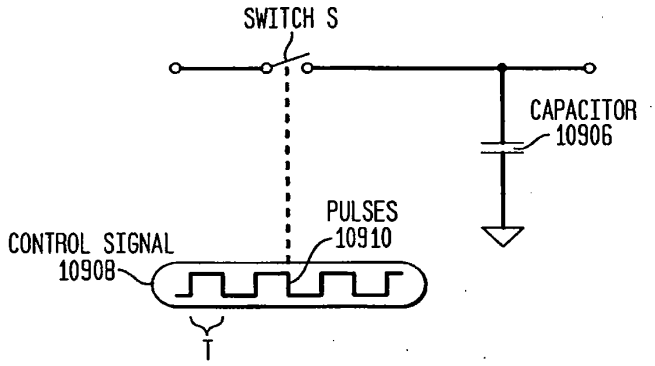


FIG. 109B

$$q=C\cdot V \qquad \text{EQ. 10}$$

$$V=A\cdot\sin(t) \qquad \text{EQ. 11}$$

$$q(t)=C\cdot A\cdot\sin(t) \qquad \text{EQ. 12}$$

$$\Delta q(t)=C\cdot A\cdot\sin(t)-C\cdot A\cdot\sin(t-T) \qquad \text{EQ. 13}$$

$$\Delta q(t)=C\cdot A\cdot(\sin(t)-\sin(t-T)) \qquad \text{EQ. 14}$$

$$\sin(\alpha)-\sin(\beta)=2\cdot\sin\left(\frac{\alpha-\beta}{2}\right)\cdot\cos\left(\frac{\alpha+\beta}{2}\right) \qquad \text{EQ. 15}$$

$$\Delta q(t)=2\cdot C\cdot A\cdot\sin\left[\frac{t-(t-T)}{2}\right]\cdot\cos\left[\frac{t+(t-T)}{2}\right] \qquad \text{EQ. 16}$$

$$\Delta q(t)=2\cdot C\cdot A\cdot\sin\left(\frac{1}{2}\cdot T\right)\cdot\cos\left(t-\frac{1}{2}\cdot T\right) \qquad \text{EQ. 17}$$

$$q(t)=\int C\cdot A\cdot(\sin(t)-\sin(t-T))\,dt \qquad \text{EQ. 18}$$

$$q(t)=-\cos(t)\cdot C\cdot A+\cos(t-T)\cdot C\cdot A \qquad \text{EQ. 19}$$

$$q(t)=C\cdot A\cdot(\cos(t-T)-\cos(t)) \qquad \text{EQ. 20}$$

FIG. 109C

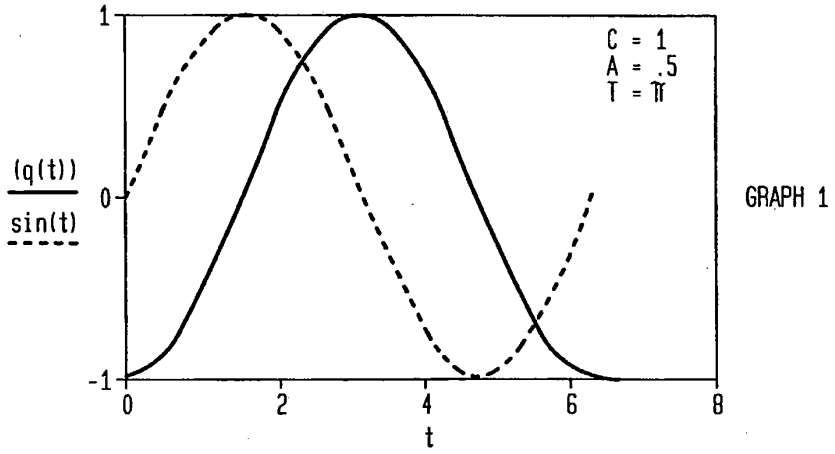


FIG. 109D

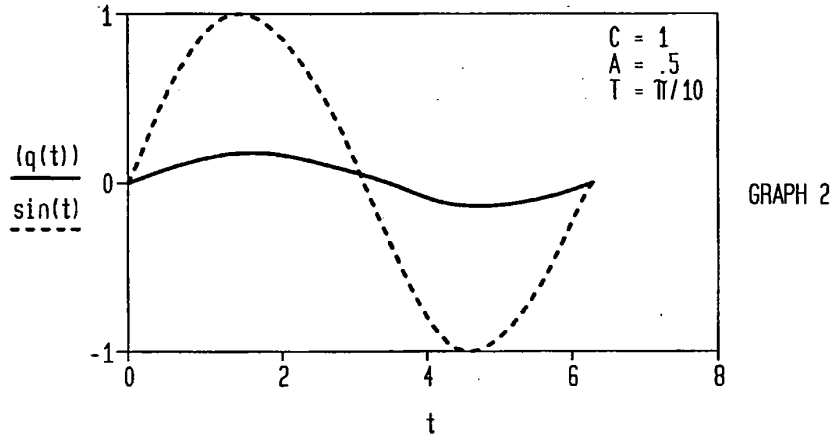


FIG. 109E

POWER-CHARGE RELATIONSHIP

$q=C \cdot V$	EQ. 21
$V=q/C$	EQ. 22
$V=J/C$	EQ. 23
$J=q^2/C$	EQ. 24
$P=J/S$	EQ. 25
$P=\frac{q^2}{C \cdot S}$	EQ. 26

FIG. 109F

INSERTION LOSS

INSERTION LOSS IN dB IS EXPRESSED BY:

$$ILdB=10 \cdot \log\left(\frac{Pin}{Pout}\right) \text{ or}$$

$$ILdB=10 \cdot \log\left[\frac{\left(\frac{Vin^2}{Rin}\right)}{\left(\frac{Vout^2}{Rout}\right)}\right]$$

FIG. 110A

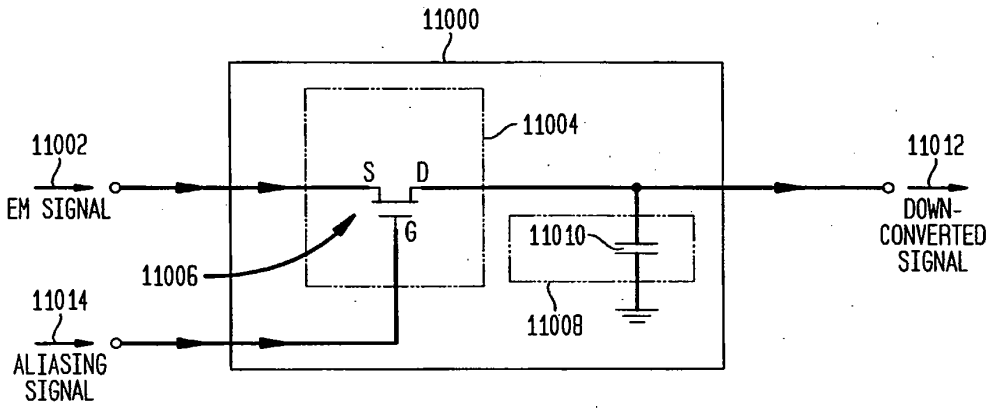
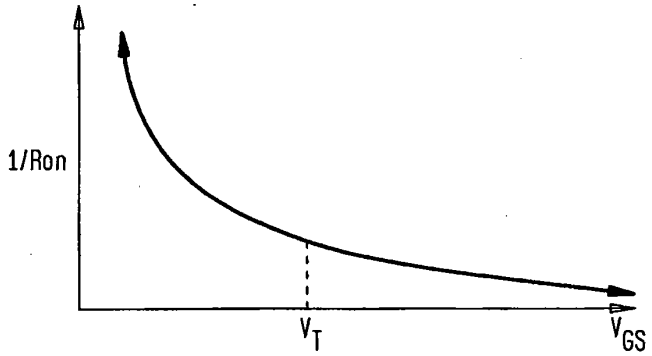


FIG. 110B



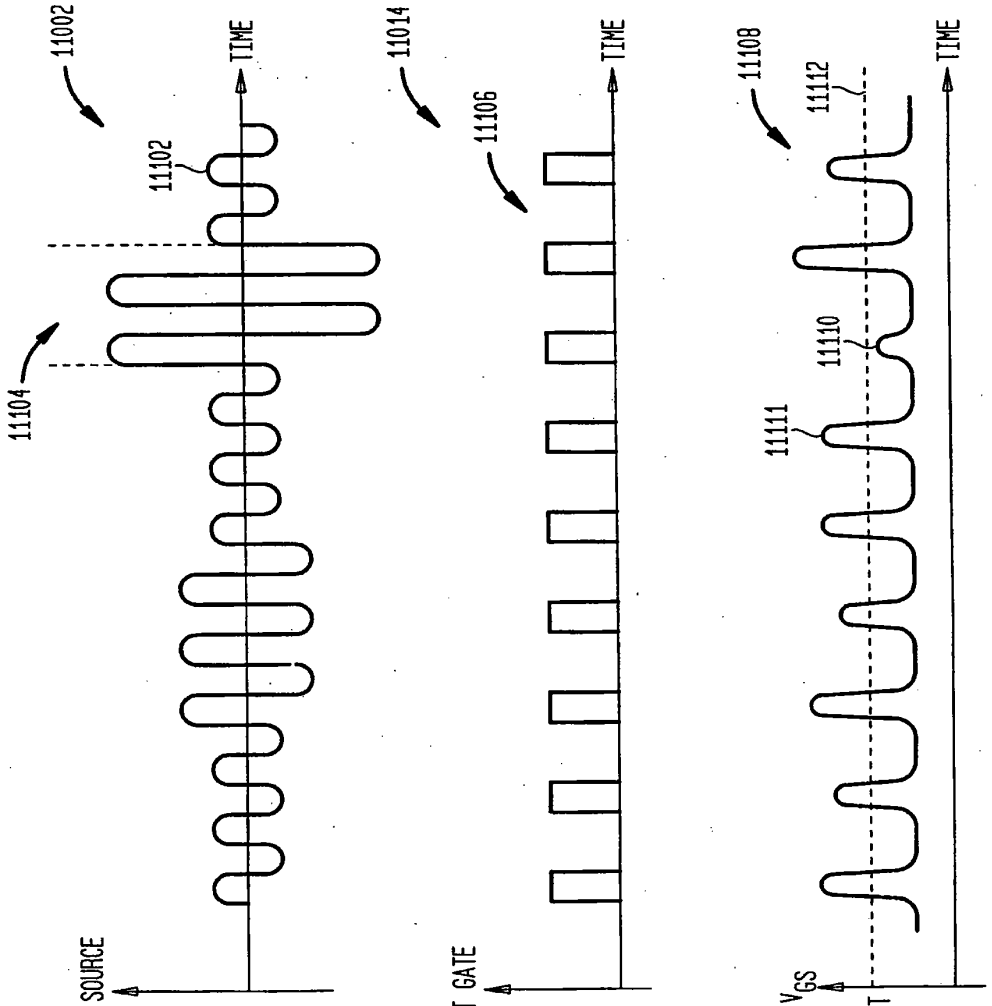


FIG. 111A

FIG. 111B

FIG. 111C

FIG. 112

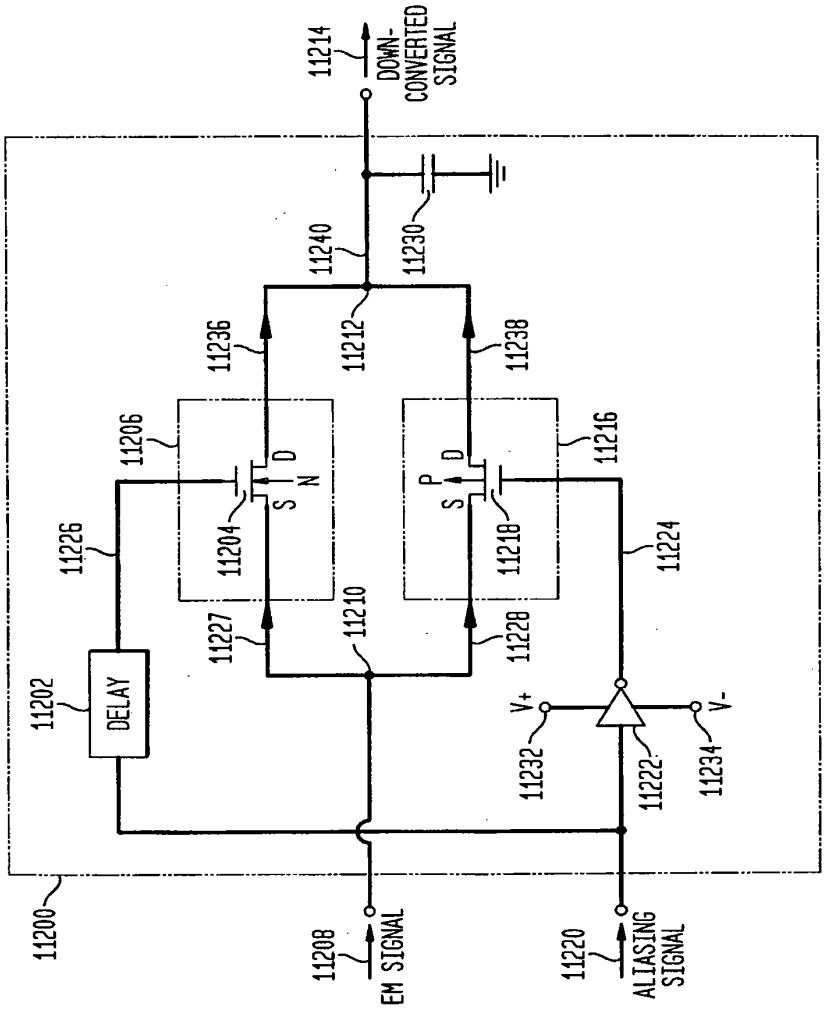

11214
DOWN-CONVERTED SIGNAL
11230
11240
11212
11236
11238
11206
11216
11226
11204
11218
11224
11227
11210
11228
11202
DELAY
V+
V-
11232
11222
11234
11200
11208
EM SIGNAL
11220
ALIASING SIGNAL
N
P
S
D

FIG. 113A

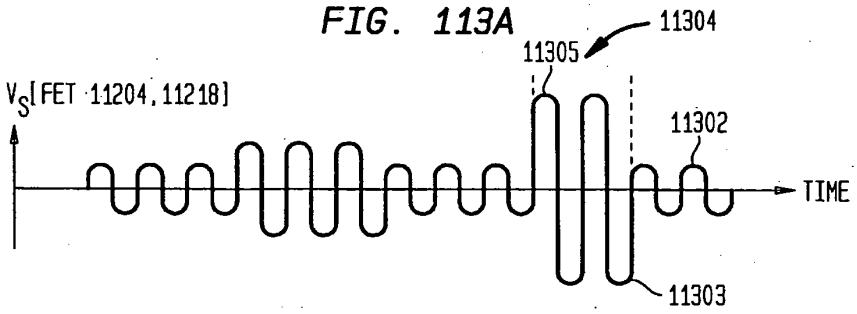


FIG. 113B

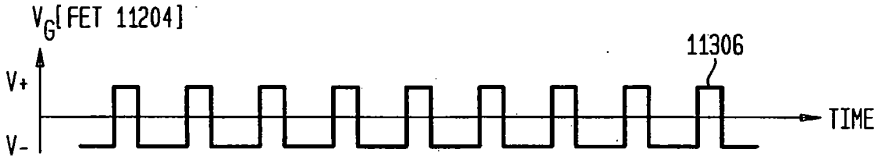


FIG. 113C

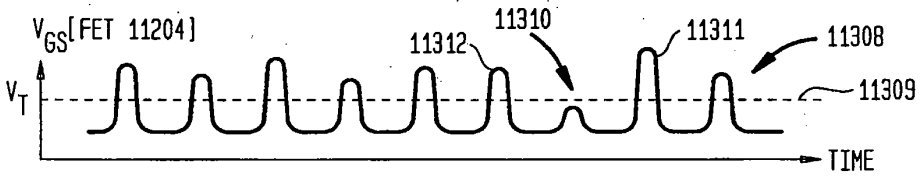


FIG. 113D

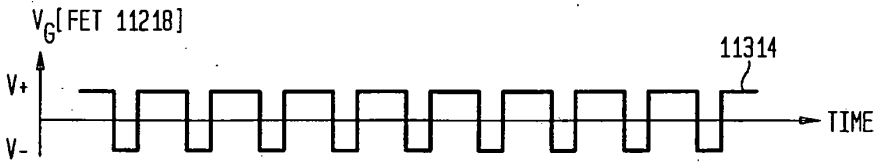


FIG. 113E

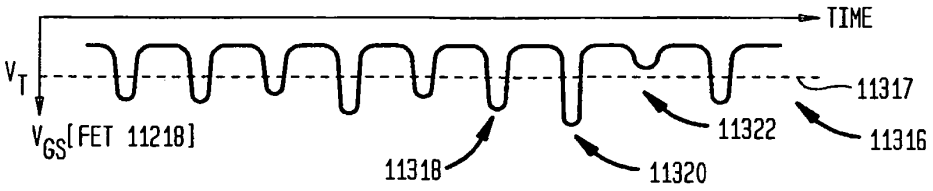


FIG. 114

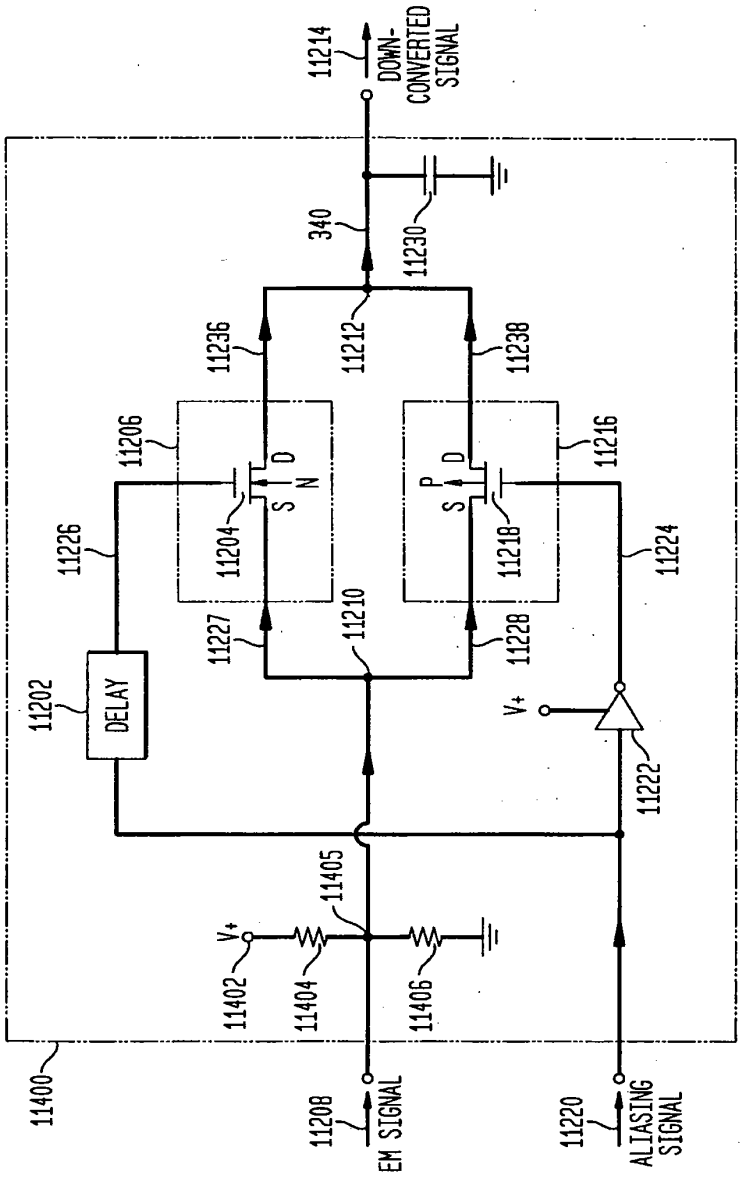

11400
11202
DELAY
11226
11206
11204
S
D
N
11227
11210
11228
11218
S
D
P
11216
11224
11236
11212
11238
340
11230
11214
DOWN-CONVERTED SIGNAL
V+
11222
11405
V+
11402
11404
11406
11208
EM SIGNAL
11220
ALIASING SIGNAL

FIG. 115

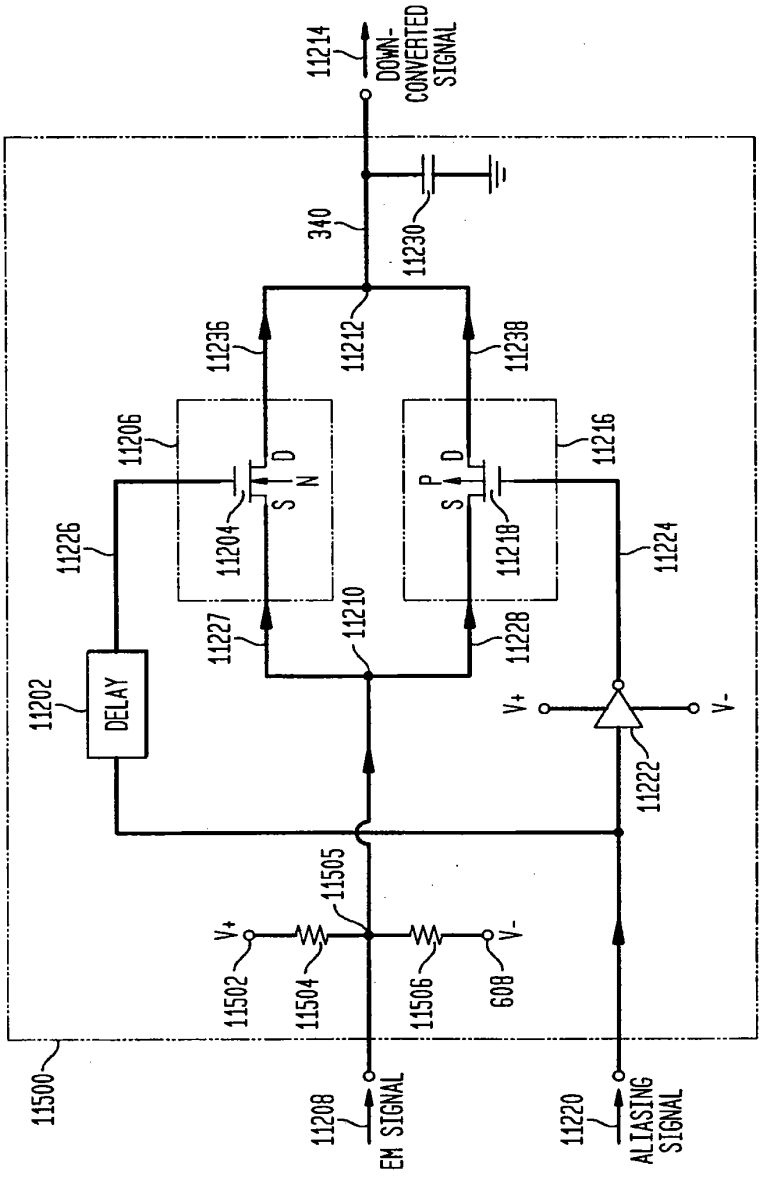

11214
DOWN-CONVERTED SIGNAL
340
11230
11212
11236
11238
11206
11216
11226
11204
11218
11224
11227
11210
11228
11202
DELAY
V+
V-
11222
11505
11502
11504
11506
608
11500
11208
EM SIGNAL
11220
ALIASING SIGNAL
N
P
S
D

FIG. 116

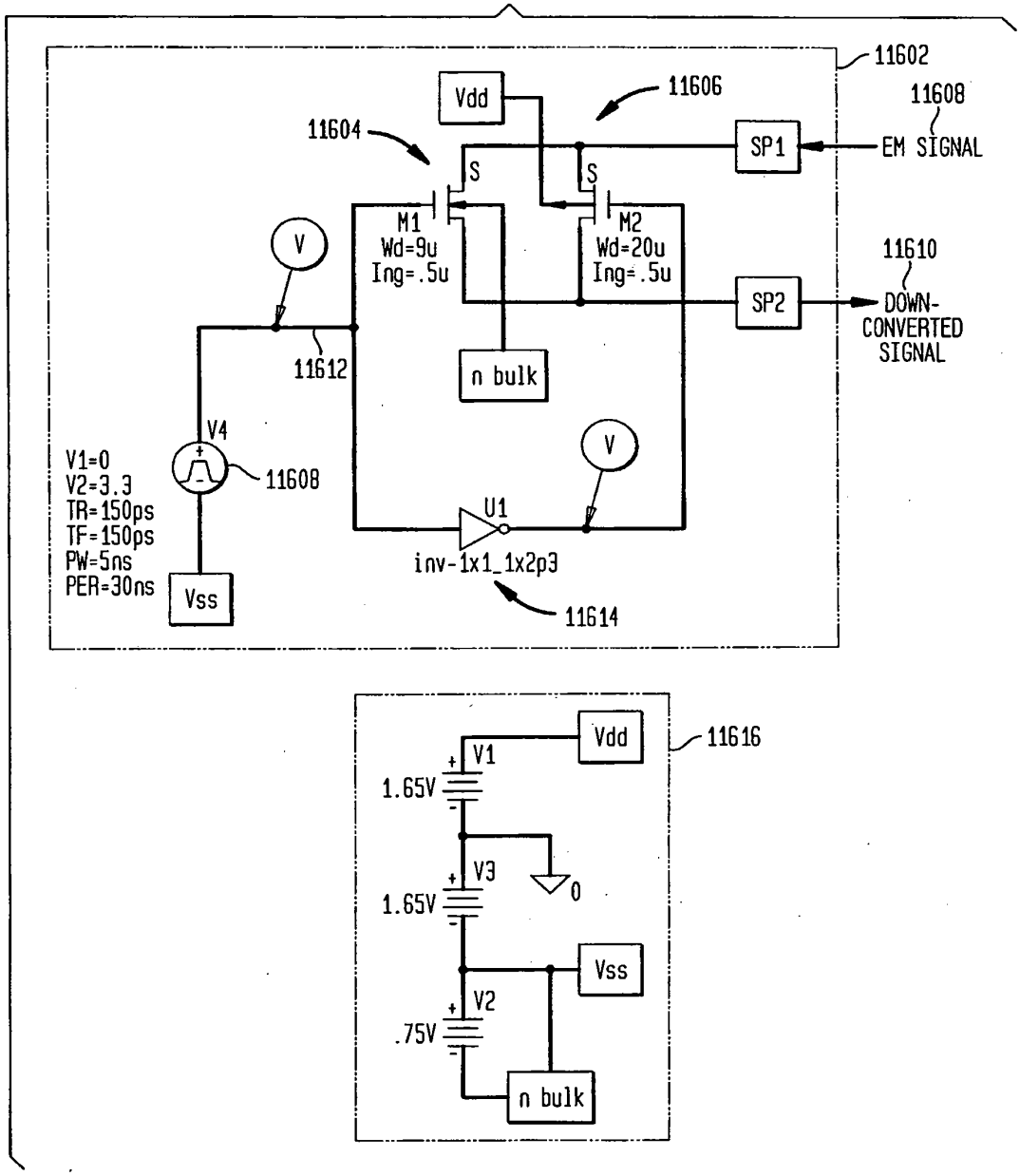

11602
Vdd
11606
11608
11604
SP1
EM SIGNAL
S
S
M1
Wd=9u
Lng=.5u
M2
Wd=20u
Lng=.5u
V
11610
SP2
DOWN-
CONVERTED
SIGNAL
11612
n bulk
V4
V
V1=0
V2=3.3
TR=150ps
TF=150ps
PW=5ns
PER=30ns
11608
U1
Vss
inv-1x1_1x2p3
11614
Vdd
11616
V1
1.65V
V3
1.65V
0
Vss
V2
.75V
n bulk

FIG. 117

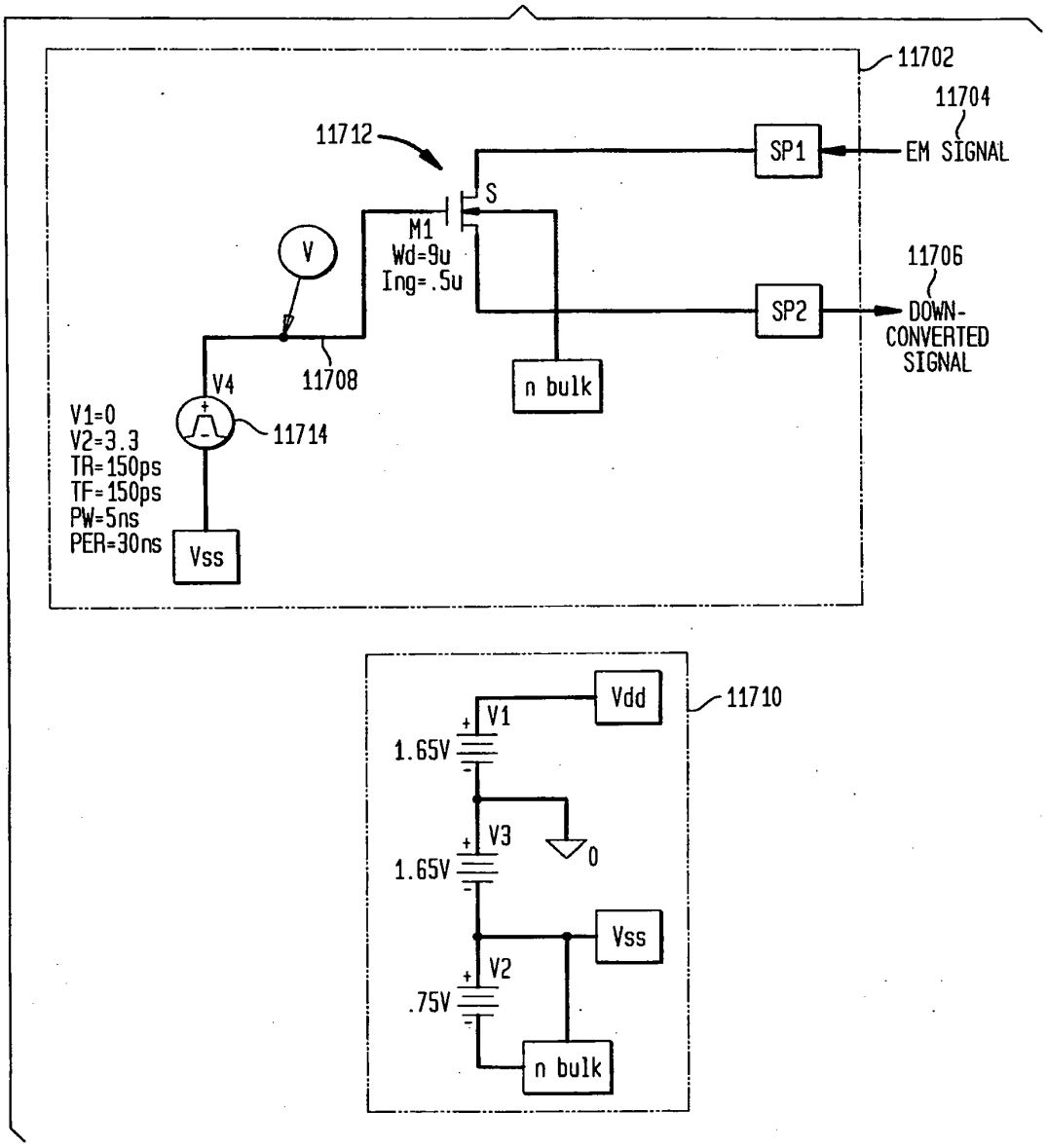

11702
11704
11712
SP1
EM SIGNAL
S
M1
Wd=9u
Lng=.5u
V
11706
SP2
DOWN-
CONVERTED
SIGNAL
V4
11708
n bulk
V1=0
V2=3.3
TR=150ps
TF=150ps
PW=5ns
PER=30ns
11714
Vss
Vdd
11710
V1
1.65V
V3
1.65V
0
Vss
V2
.75V
n bulk

FIG. 118

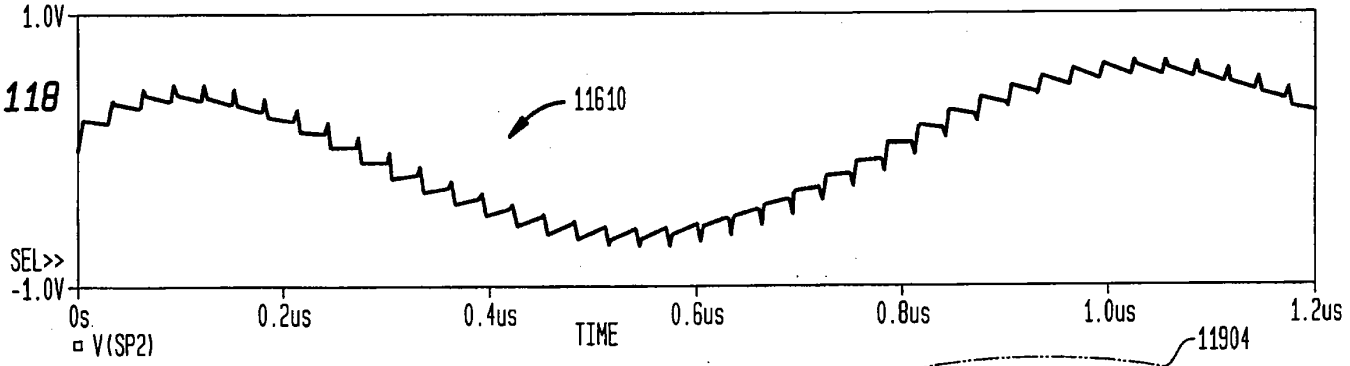


FIG. 119

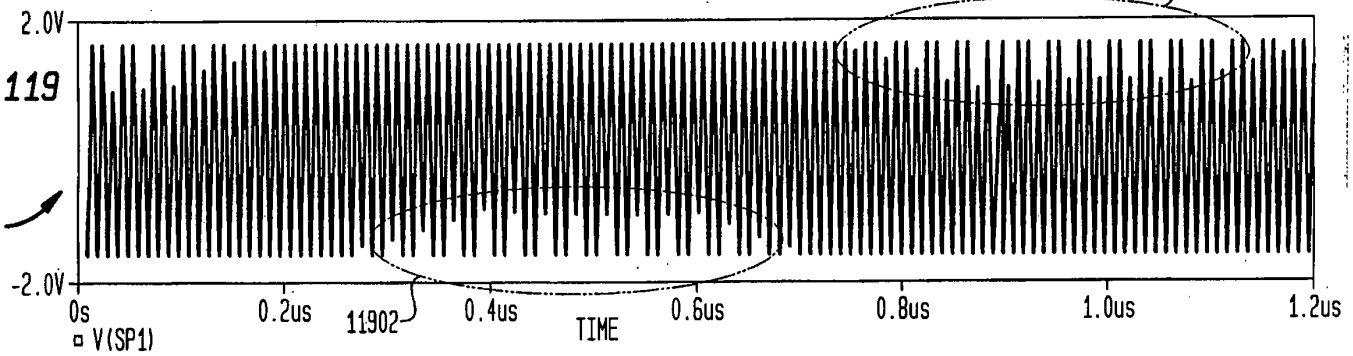


FIG. 120

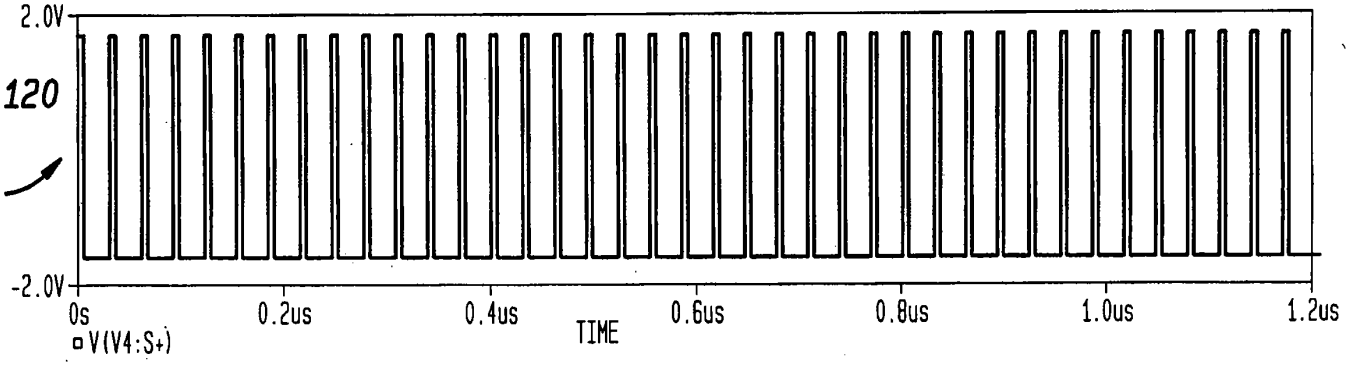


FIG. 121

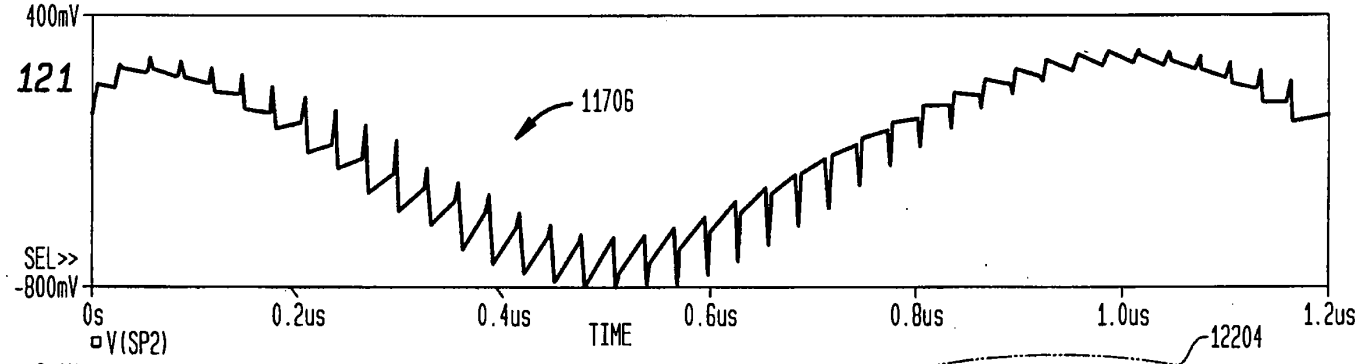


FIG. 122

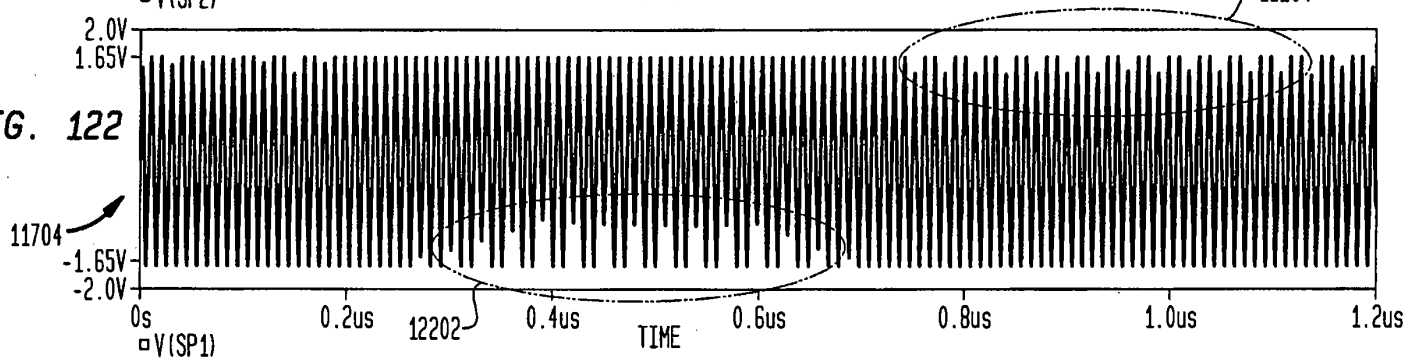


FIG. 123

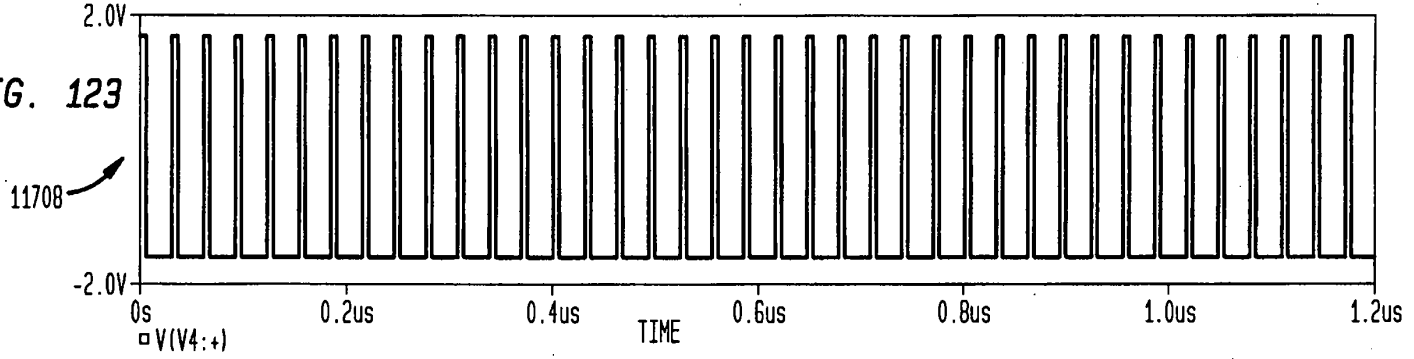


FIG. 124A

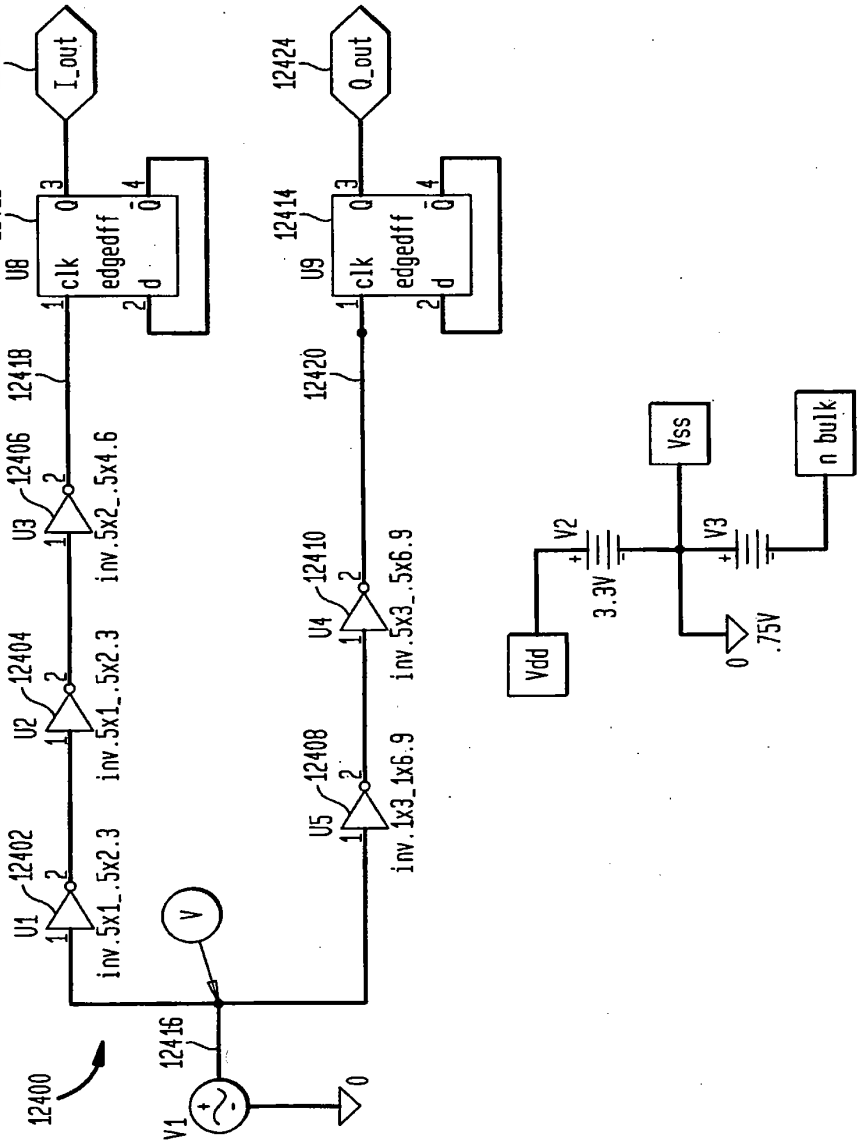

12400
12402
U1
inv.5x1_.5x2.3
12404
U2
inv.5x1_.5x2.3
12406
U3
inv.5x2_.5x4.6
12408
U5
inv.1x3_1x6.9
12410
U4
inv.5x3_.5x6.9
12412
U8
clk
edgedff
d
12414
U9
clk
edgedff
d
12416
V1
V
0
12418
12420
12422
I_out
12424
Q_out
Vdd
3.3V
V2
Vss
V3
.75V
0
n bulk

FIG. 124B

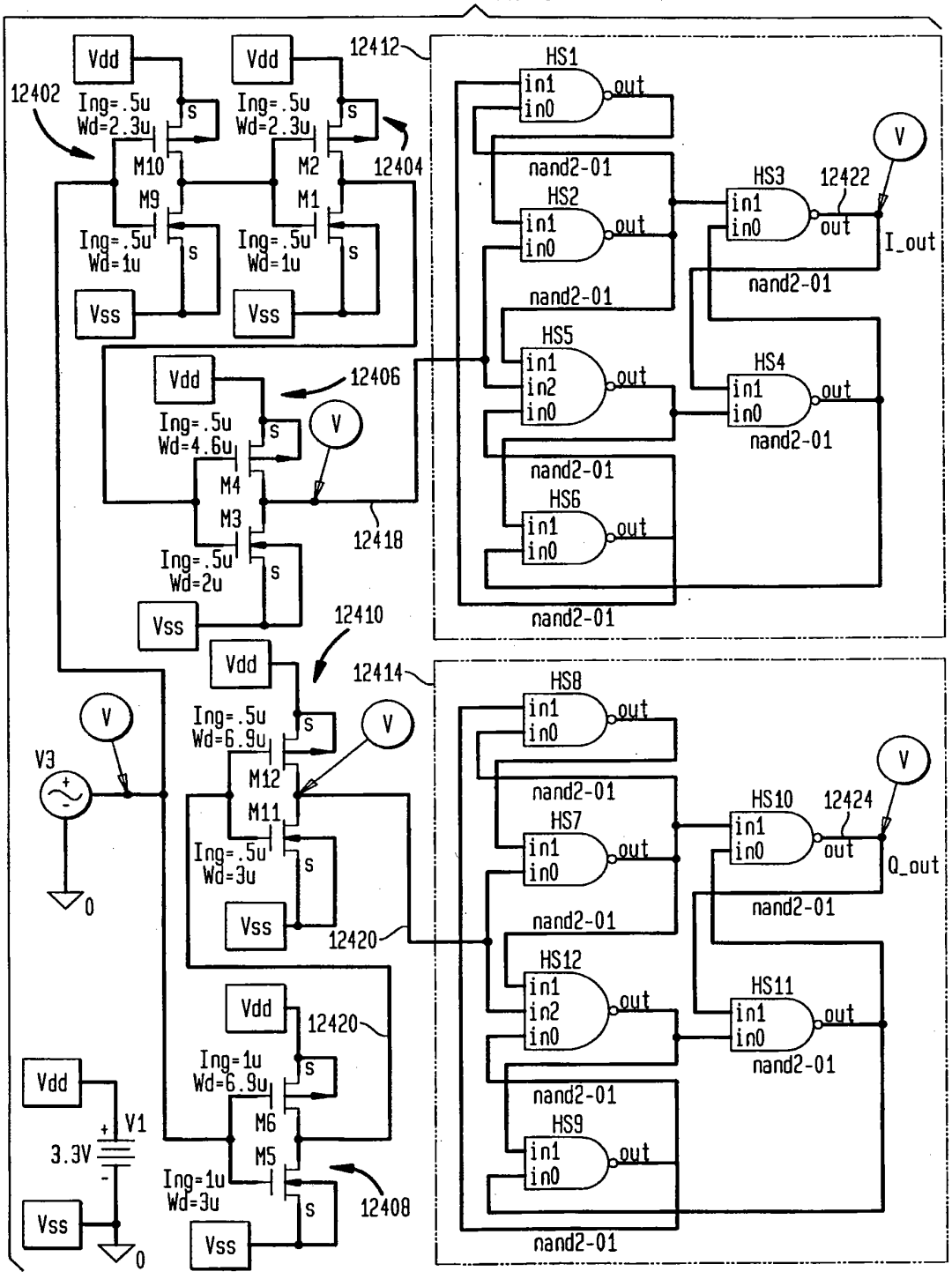

12402
12404
12406
12408
12410
12412
12414
12418
12420
12422
12424
Vdd
Vss
M10
M9
M2
M1
M4
M3
M12
M11
M6
M5
Ing=.5u
Wd=2.3u
Wd=1u
Wd=4.6u
Wd=2u
Wd=6.9u
Wd=3u
Ing=1u
Wd=6.9u
Wd=3u
V
V3
V1
3.3V
0
HS1
HS2
HS3
HS4
HS5
HS6
HS7
HS8
HS9
HS10
HS11
HS12
in1
in2
in0
out
nand2-01
I_out
Q_out

FIG. 124C

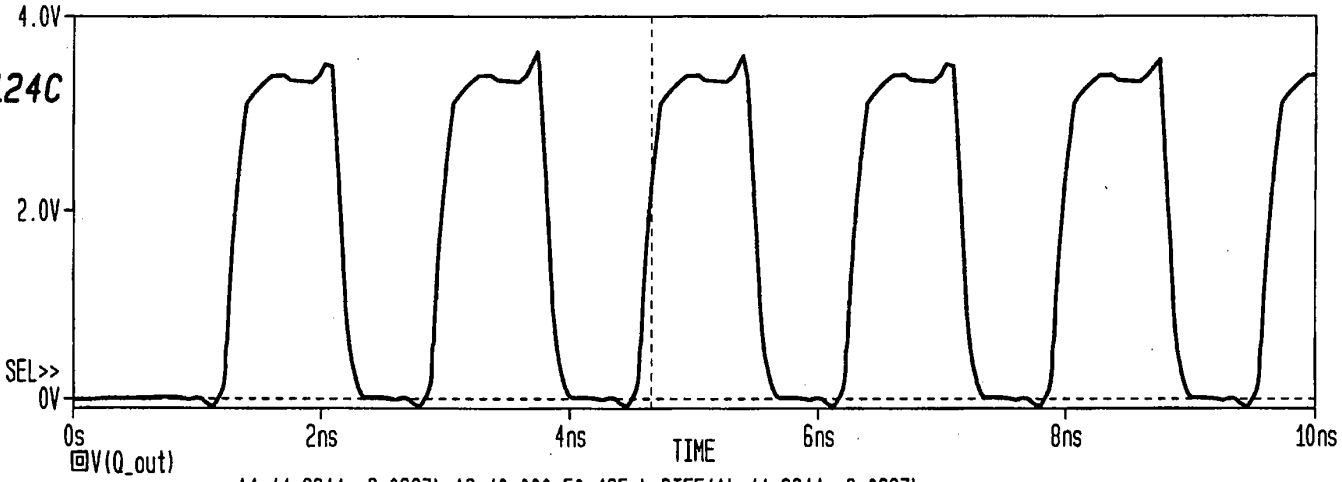


FIG. 124D

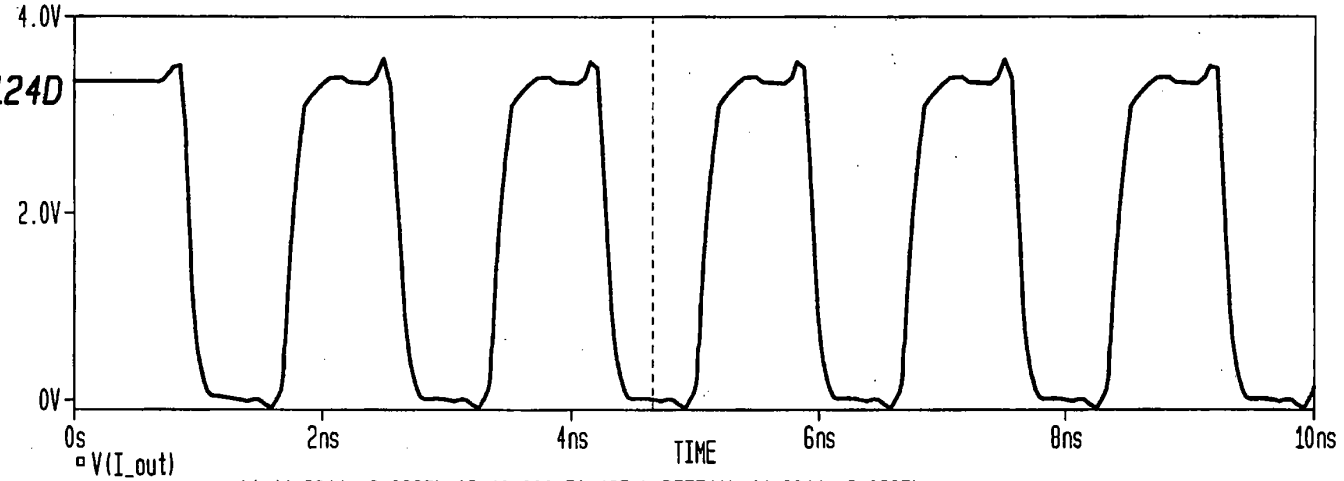


FIG. 124E

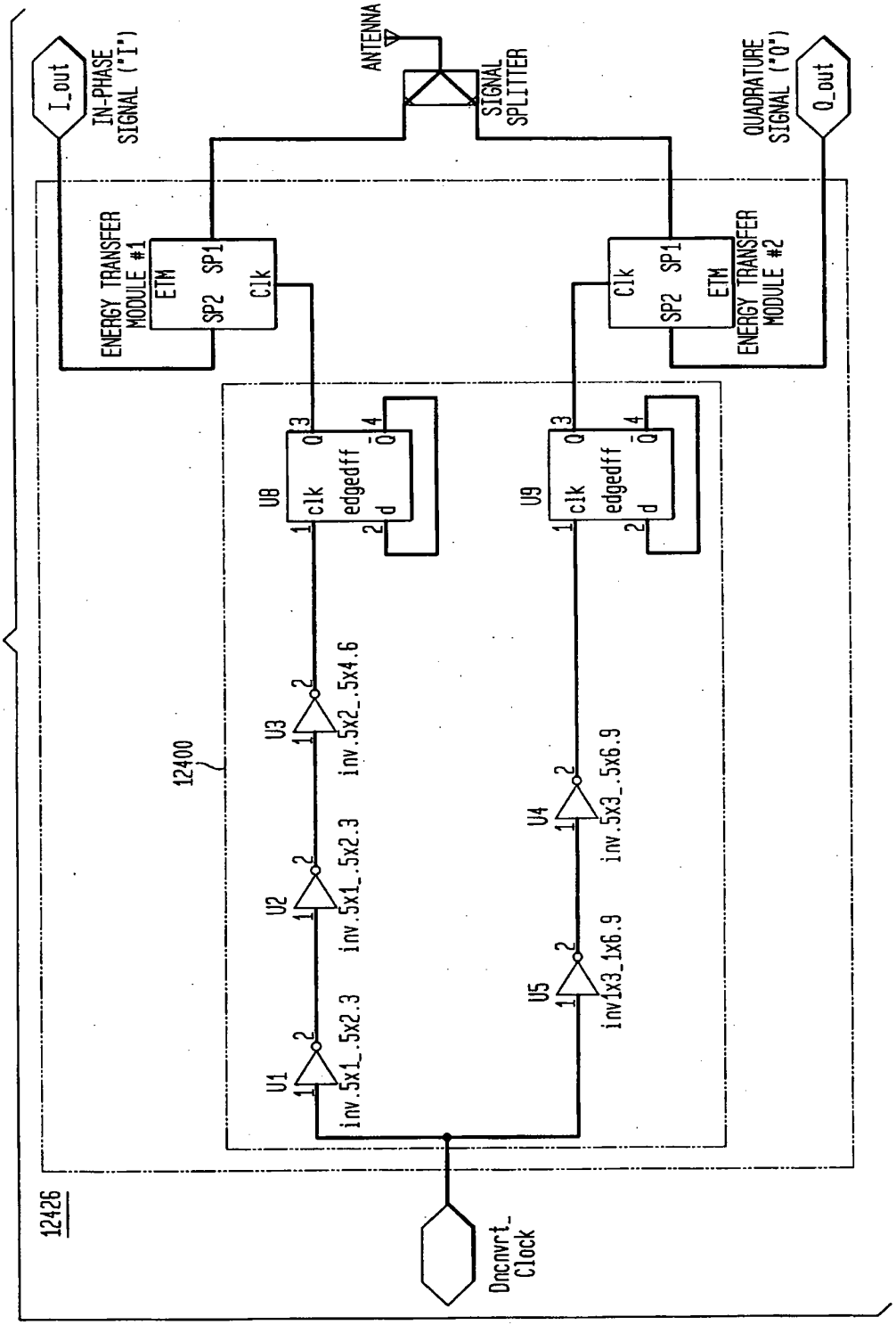

I_out
IN-PHASE SIGNAL ("I")
ANTENNA
SIGNAL SPLITTER
Q_out
QUADRATURE SIGNAL ("Q")
ENERGY TRANSFER MODULE #1
ETM
SP2 SP1
Clk
ENERGY TRANSFER MODULE #2
12426
12400
U8
U9
clk
edgedff
d
U1
U2
U3
U4
U5
inv.5x1_.5x2.3
inv.5x1_.5x2.3
inv.5x2_.5x4.6
inv.5x3_.5x6.9
inv1x3_1x6.9
Dncnvrt_ Clock

FIG. 124F

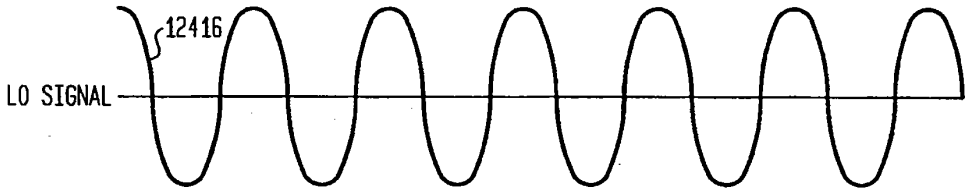


FIG. 124G

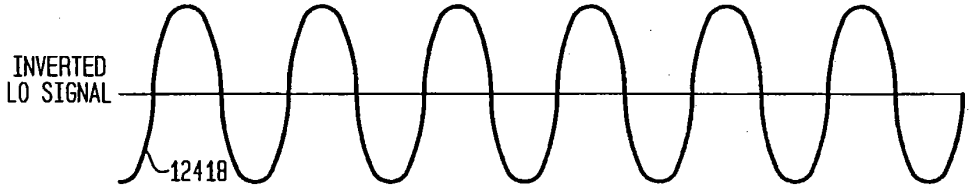


FIG. 124H

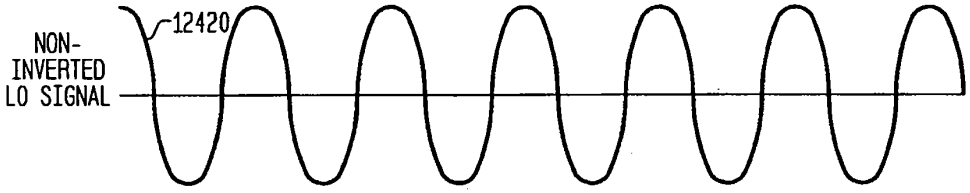


FIG. 124I

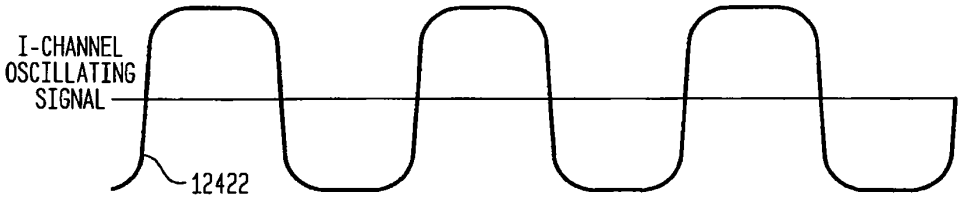


FIG. 124J

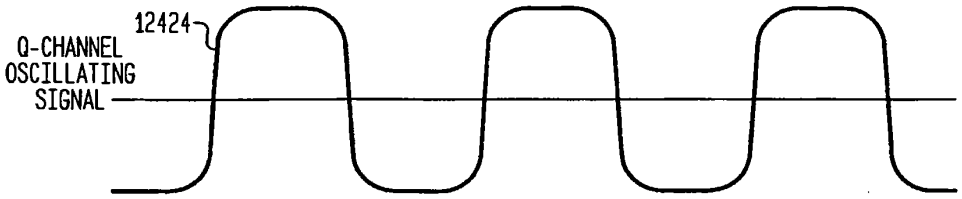


FIG. 125

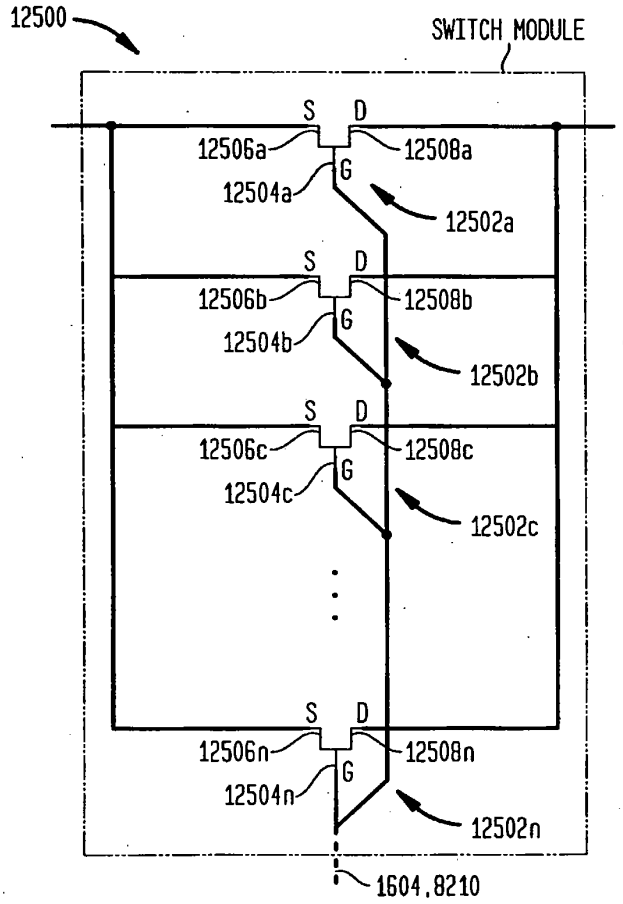

12500
SWITCH MODULE
S
D
12506a
12508a
G
12504a
12502a
12506b
12508b
12504b
12502b
12506c
12508c
12504c
12502c
12506n
12508n
12504n
12502n
1604,8210

FIG. 126A

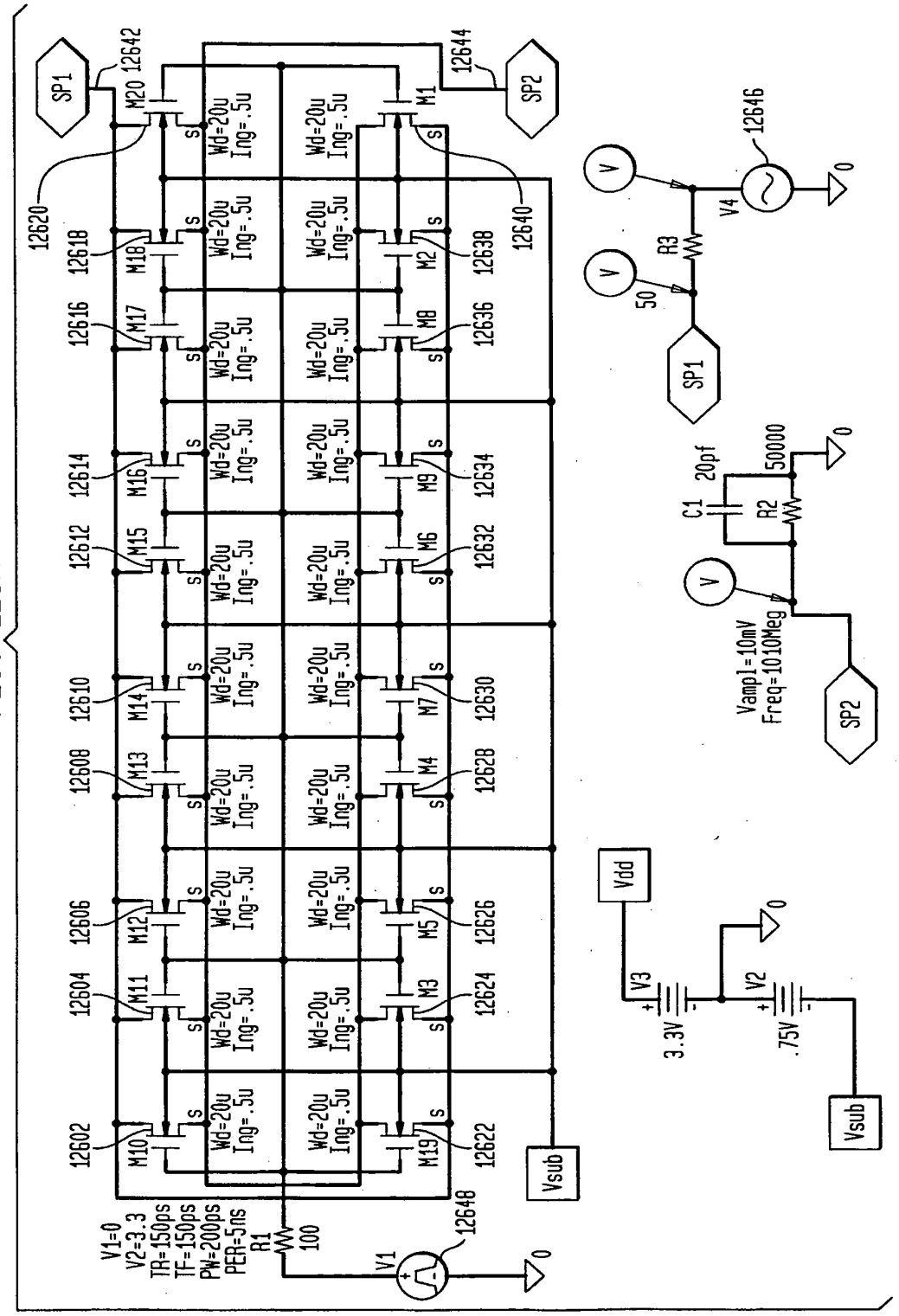

SP1
SP2
12620
12640
12642
12644
12646
12648
M20
M1
M18
M2
M17
M8
M16
M9
M15
M6
M14
M7
M13
M4
M12
M5
M11
M3
M10
M19
12602
12604
12606
12608
12610
12612
12614
12616
12618
12622
12624
12626
12628
12630
12632
12634
12636
12638
Wd=20u
Lng=.5u
s
V1=0
V2=3.3
TR=150ps
TF=150ps
PW=200ps
PER=5ns
R1
100
V1
0
Vsub
Vdd
V3
3.3V
V2
.75V
V
R3
50
V4
C1
20pf
R2
50000
Vampl=10mV
Freq=1010Meg

FIG. 126B

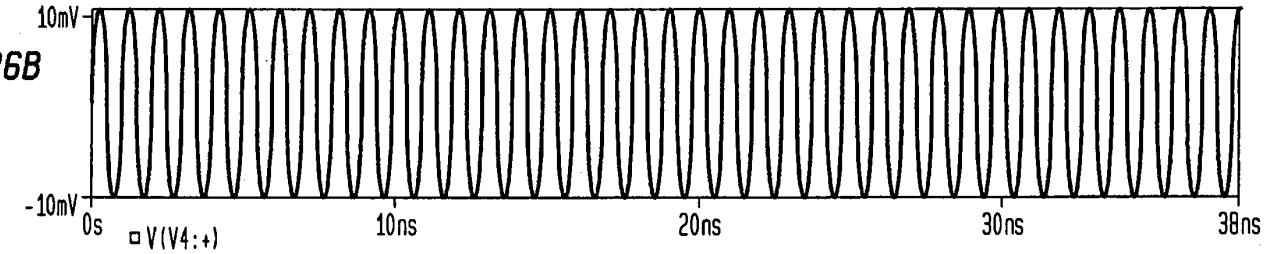


FIG. 126C

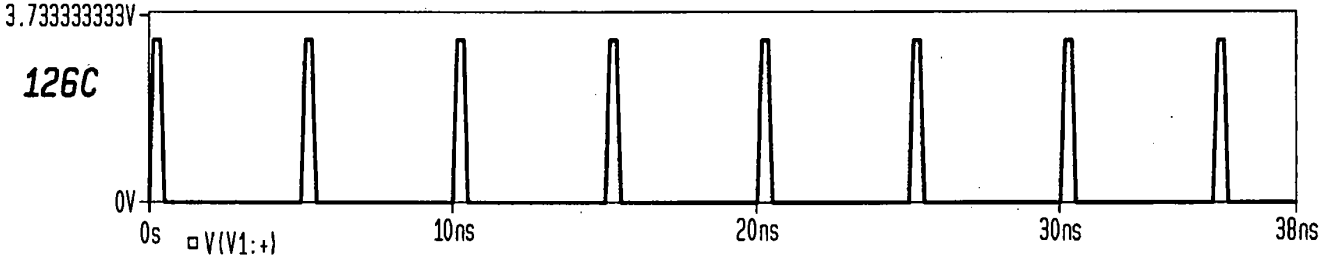


FIG. 126D

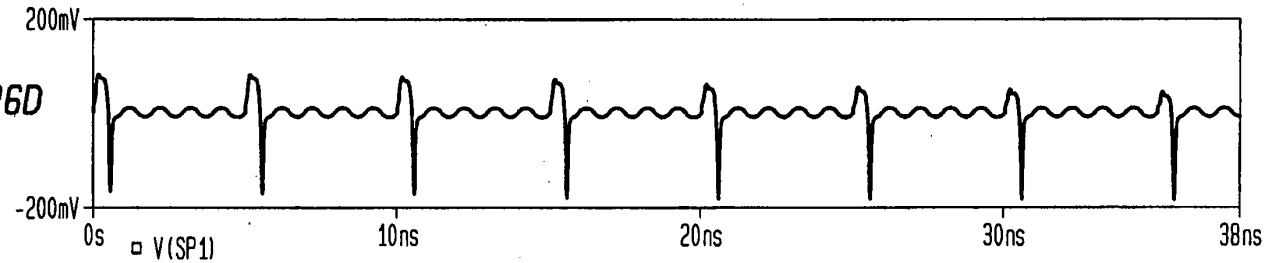


FIG. 126E

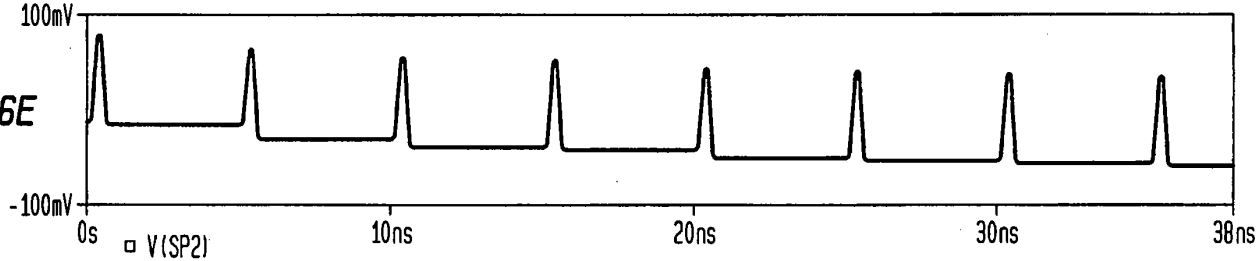


FIG. 126F

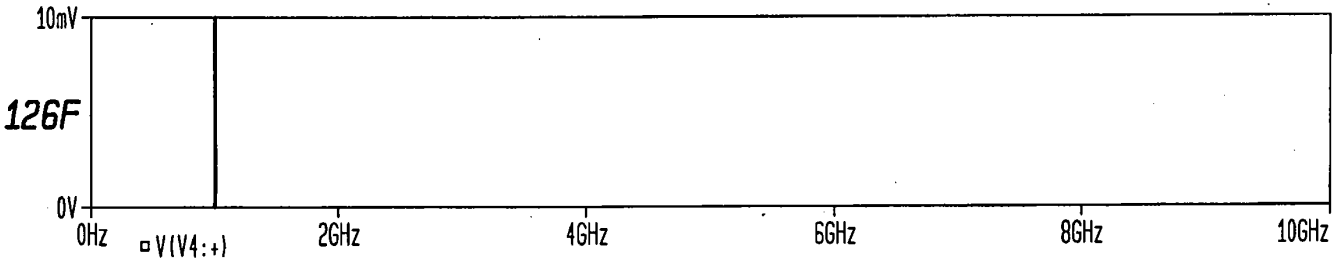


FIG. 126G

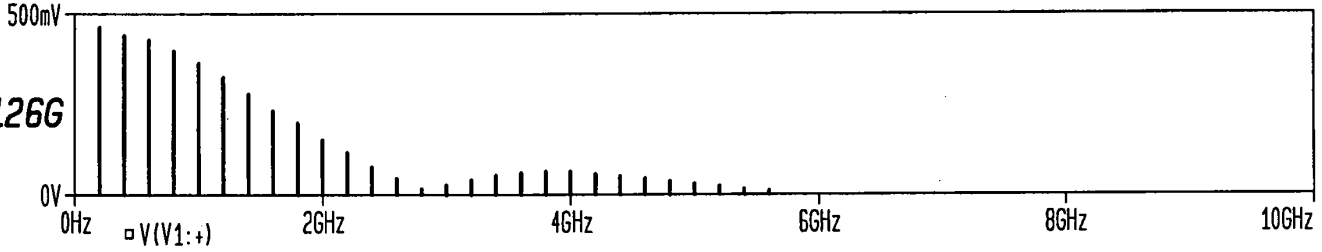


FIG. 126H

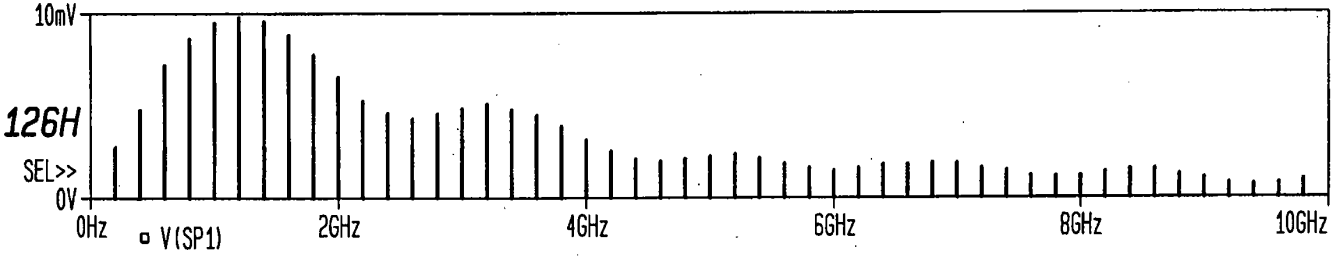


FIG. 126I

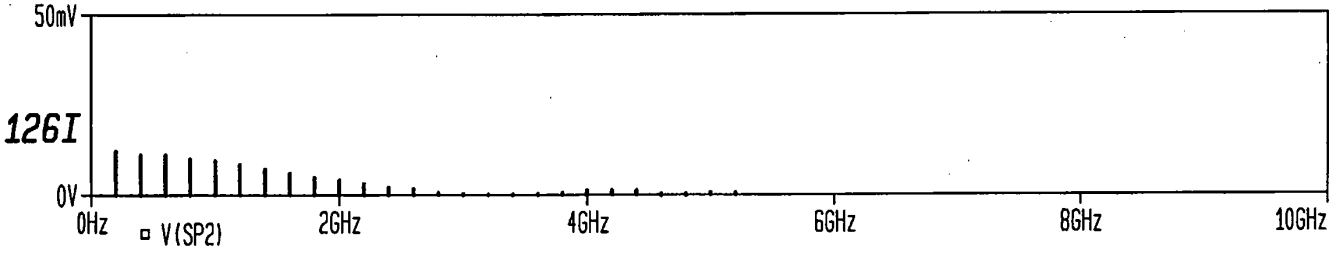


FIG. 126J

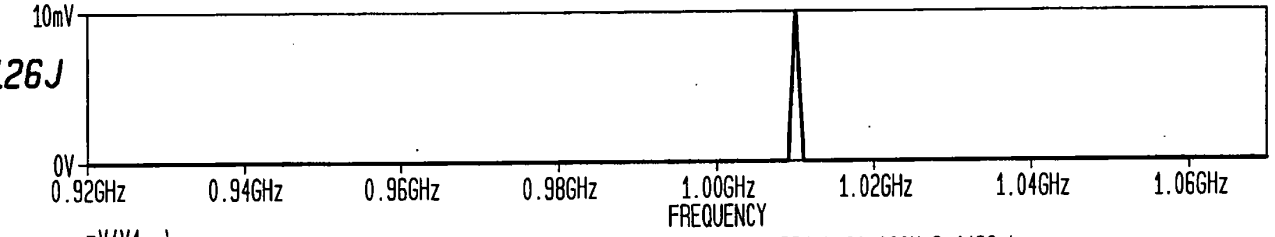


FIG. 126K

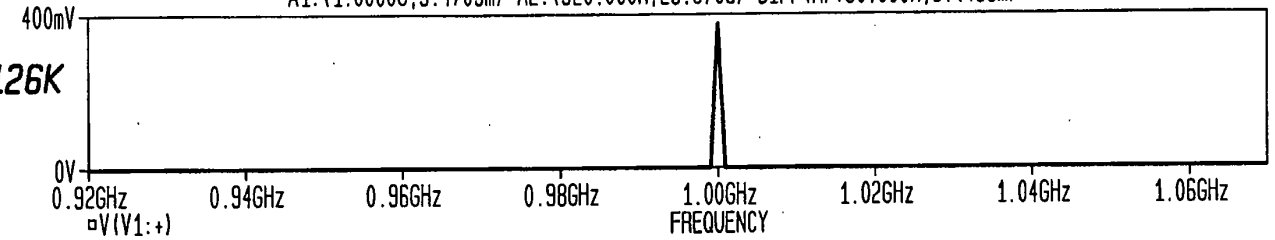


FIG. 126L

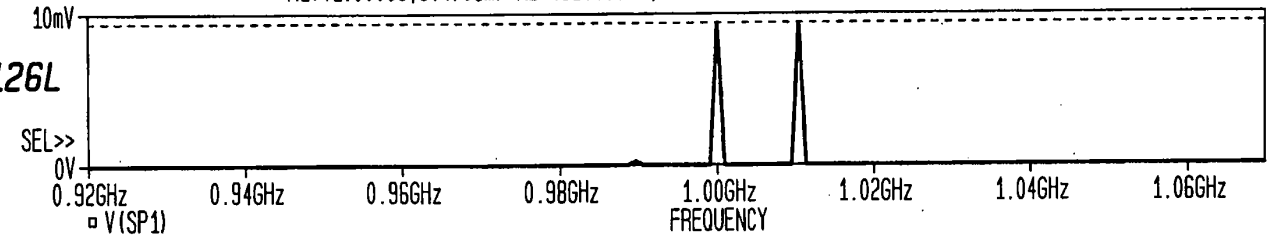


FIG. 126M

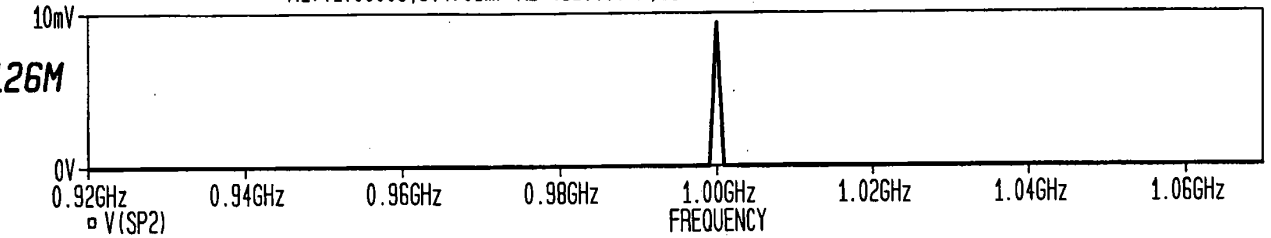


FIG. 126N

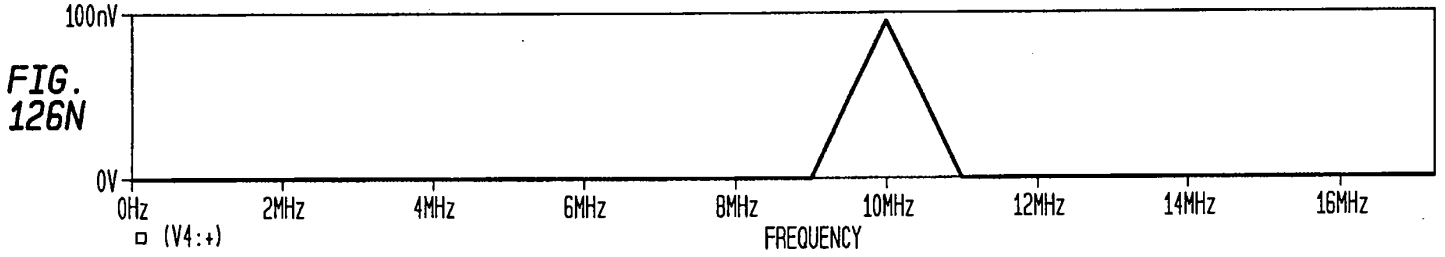


FIG. 1260

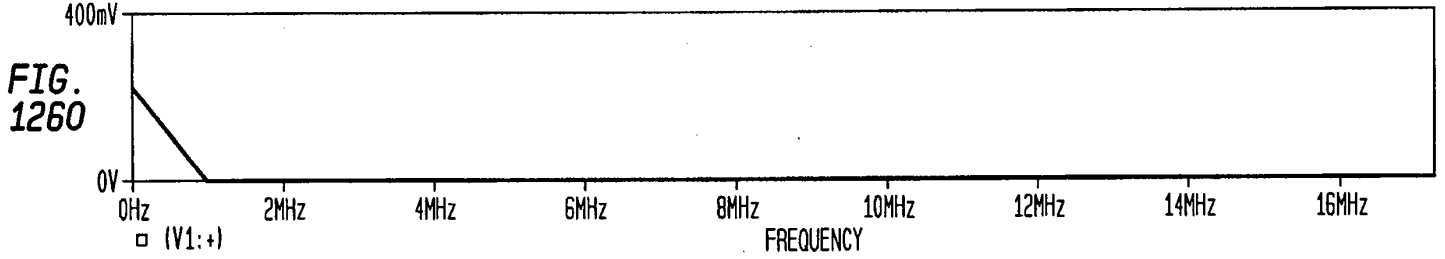


FIG. 126P

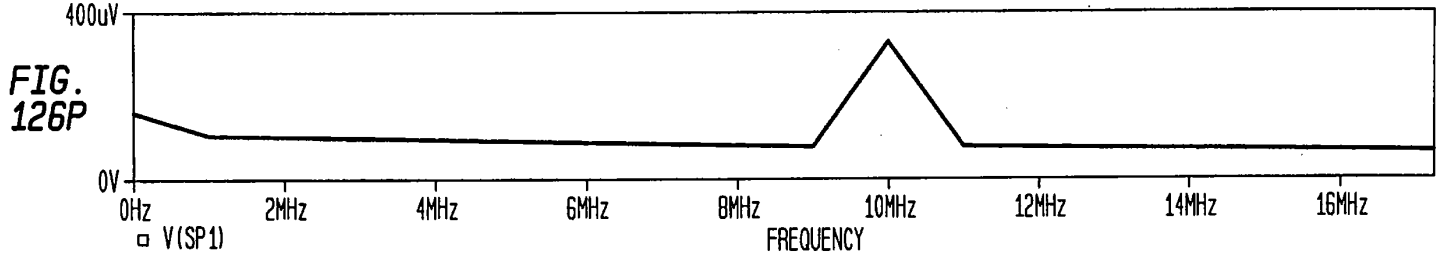


FIG. 126Q

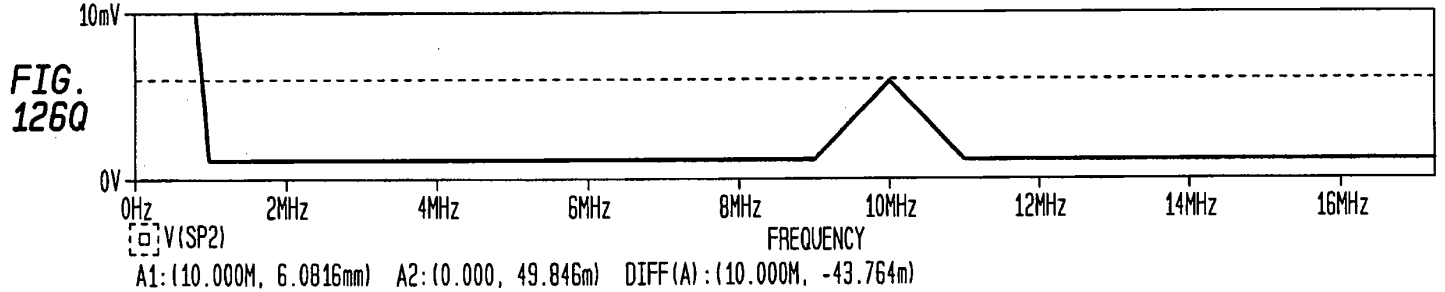
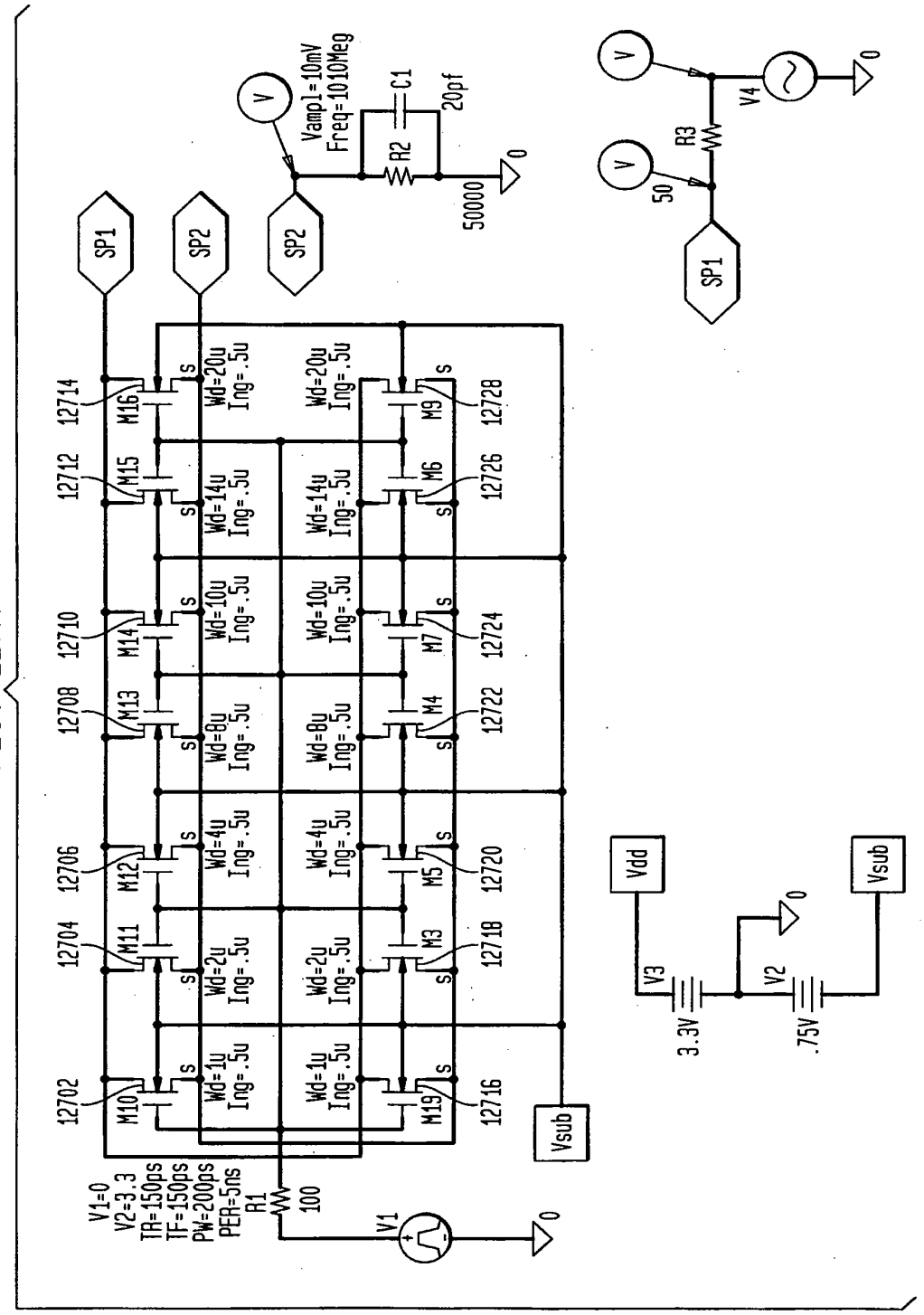


FIG. 127A


SP1
SP2
SP2
V
Vampl=10mV
Freq=1010Meg
C1
20pf
R2
50000
0
V
V
50
R3
V4
0
SP1
12714
M16
12712
M15
12710
M14
12708
M13
12706
M12
12704
M11
12702
M10
12728
M9
12726
M6
12724
M7
12722
M4
12720
M5
12718
M3
12716
M19
Wd=20u
Lng=.5u
Wd=14u
Lng=.5u
Wd=10u
Lng=.5u
Wd=8u
Lng=.5u
Wd=4u
Lng=.5u
Wd=2u
Lng=.5u
Wd=1u
Lng=.5u
s
Vsub
V1=0
V2=3.3
TR=150ps
TF=150ps
PW=200ps
PER=5ns
R1
100
V1
0
Vdd
V3
3.3V
0
V2
.75V
Vsub

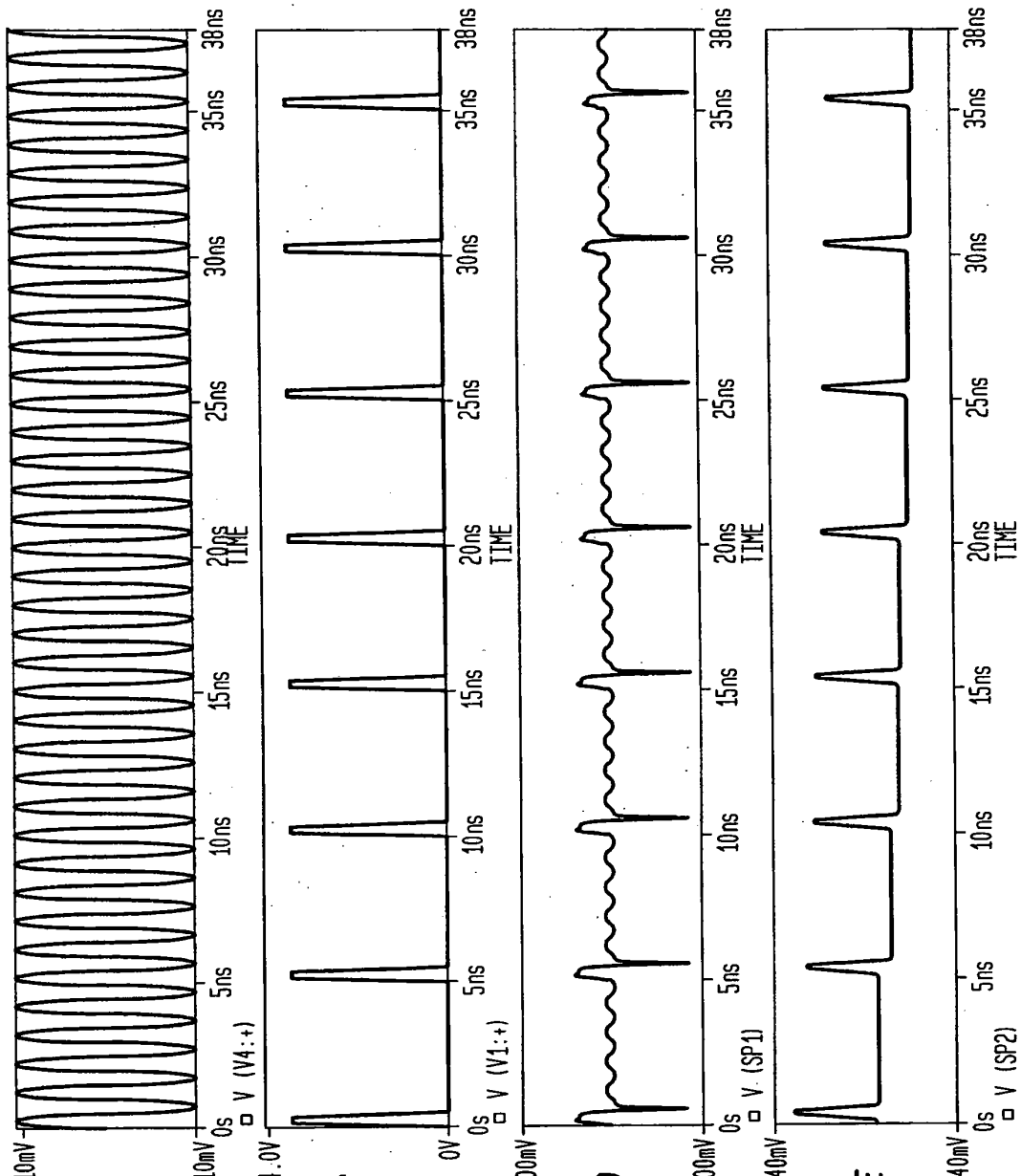


FIG. 127B

FIG. 127C

FIG. 127D

FIG. 127E

FIG. 127F

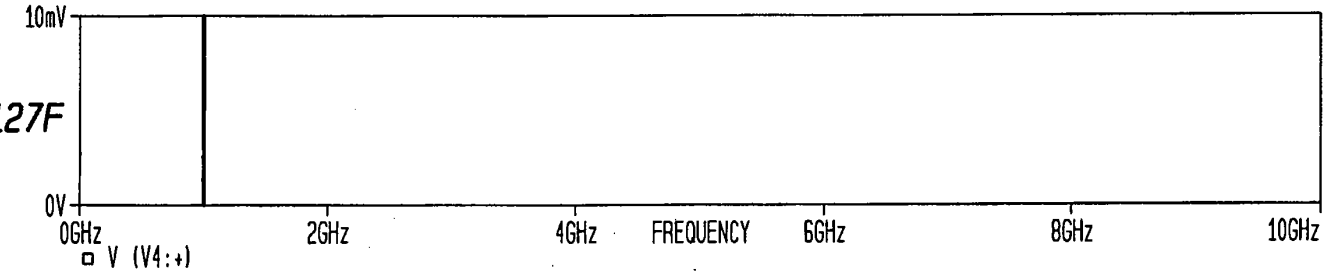


FIG. 127G

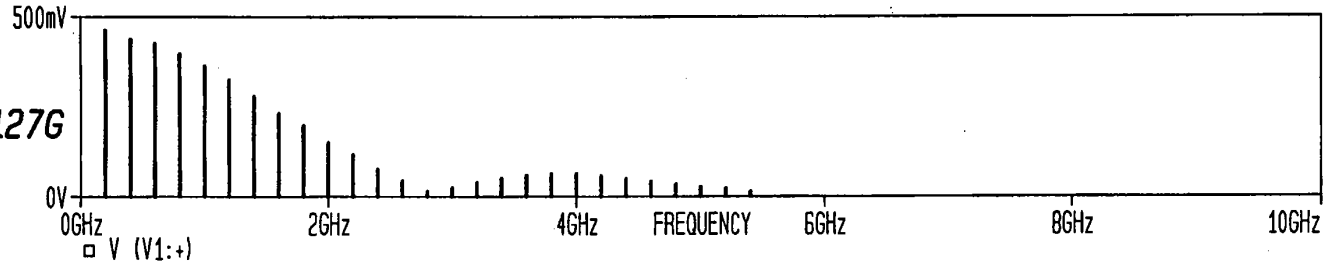


FIG. 127H

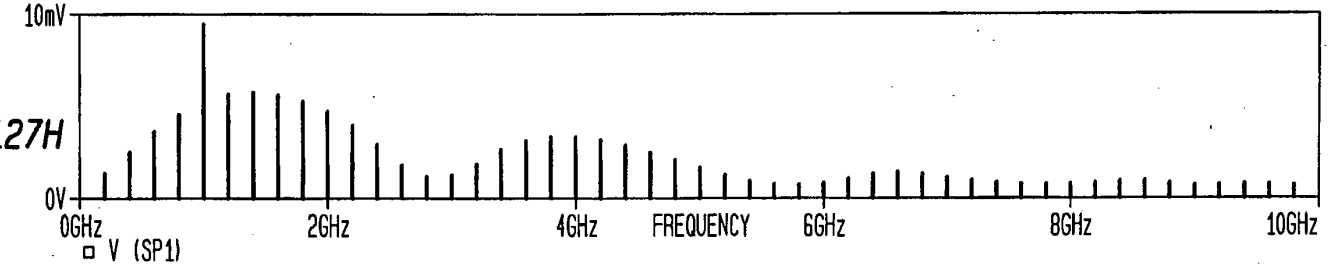


FIG. 127I

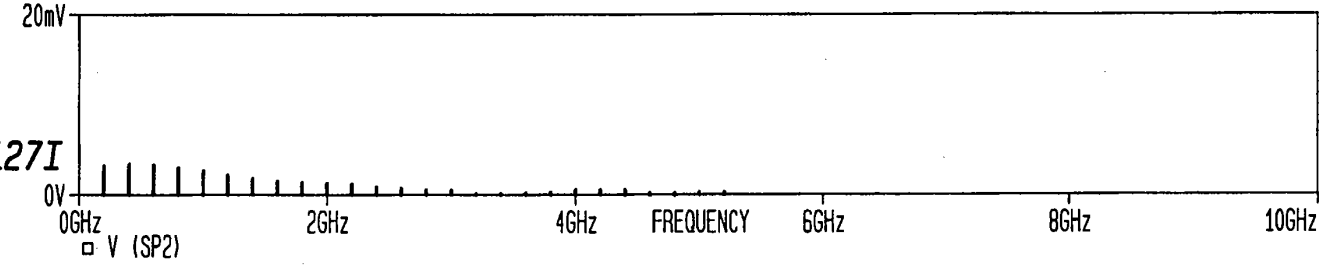


FIG. 127J

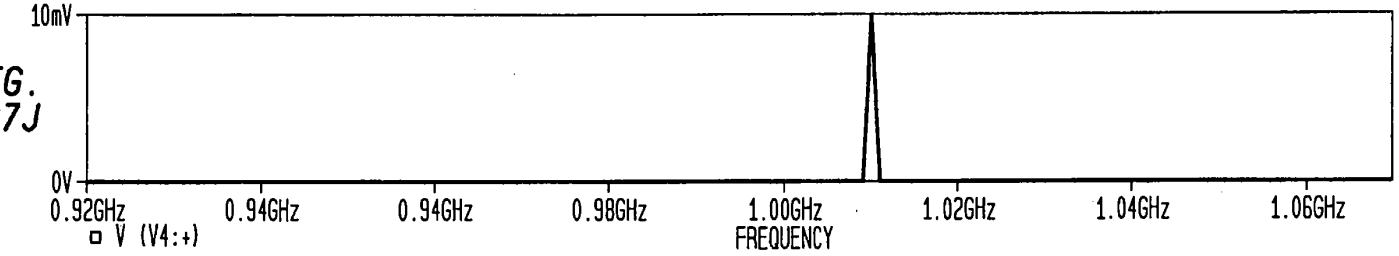


FIG. 127K

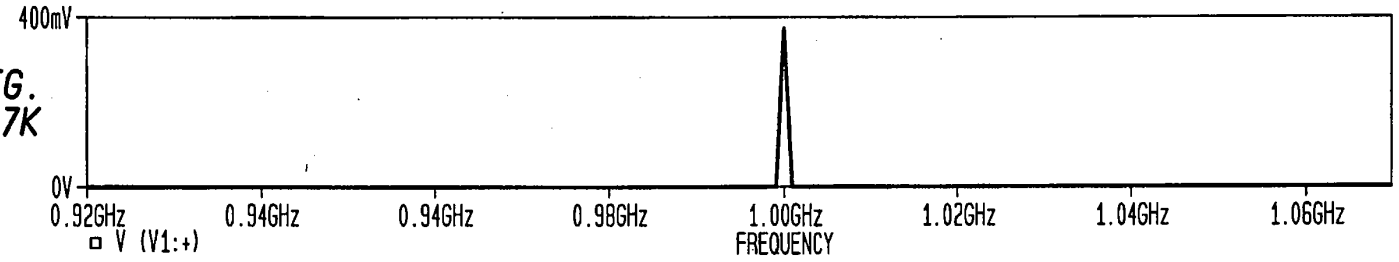


FIG. 127L

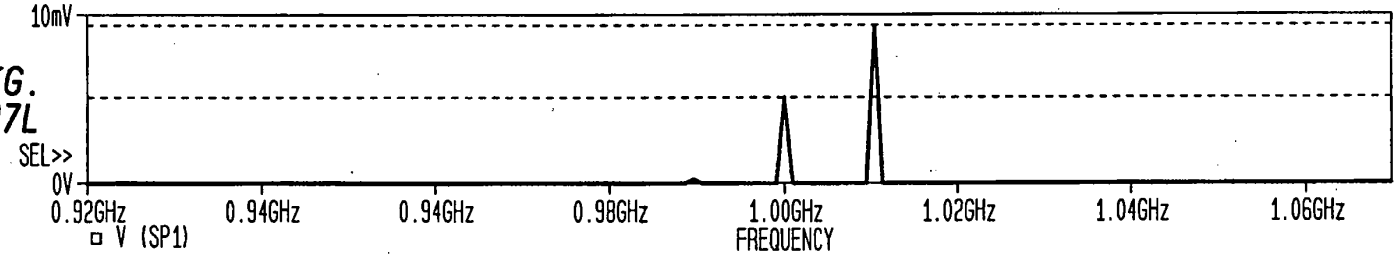
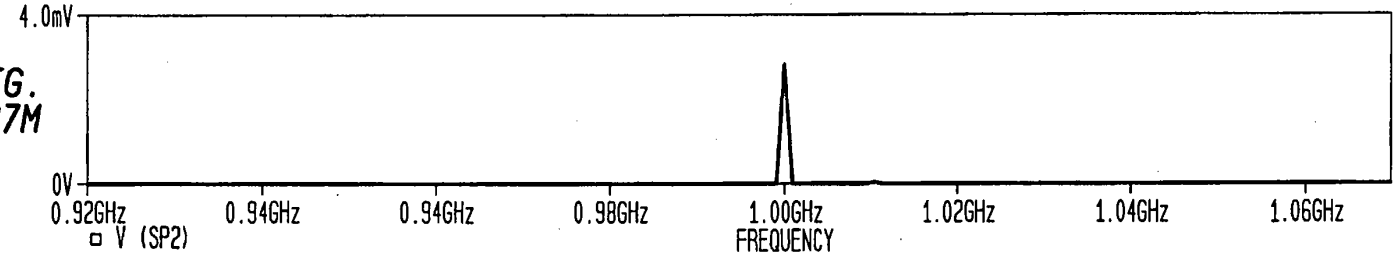


FIG. 127M



A1:(1.0000G, 5.3091m) A2:(818.000M, 11.646u) DIFF(A):(182.000M, 5.2974m)

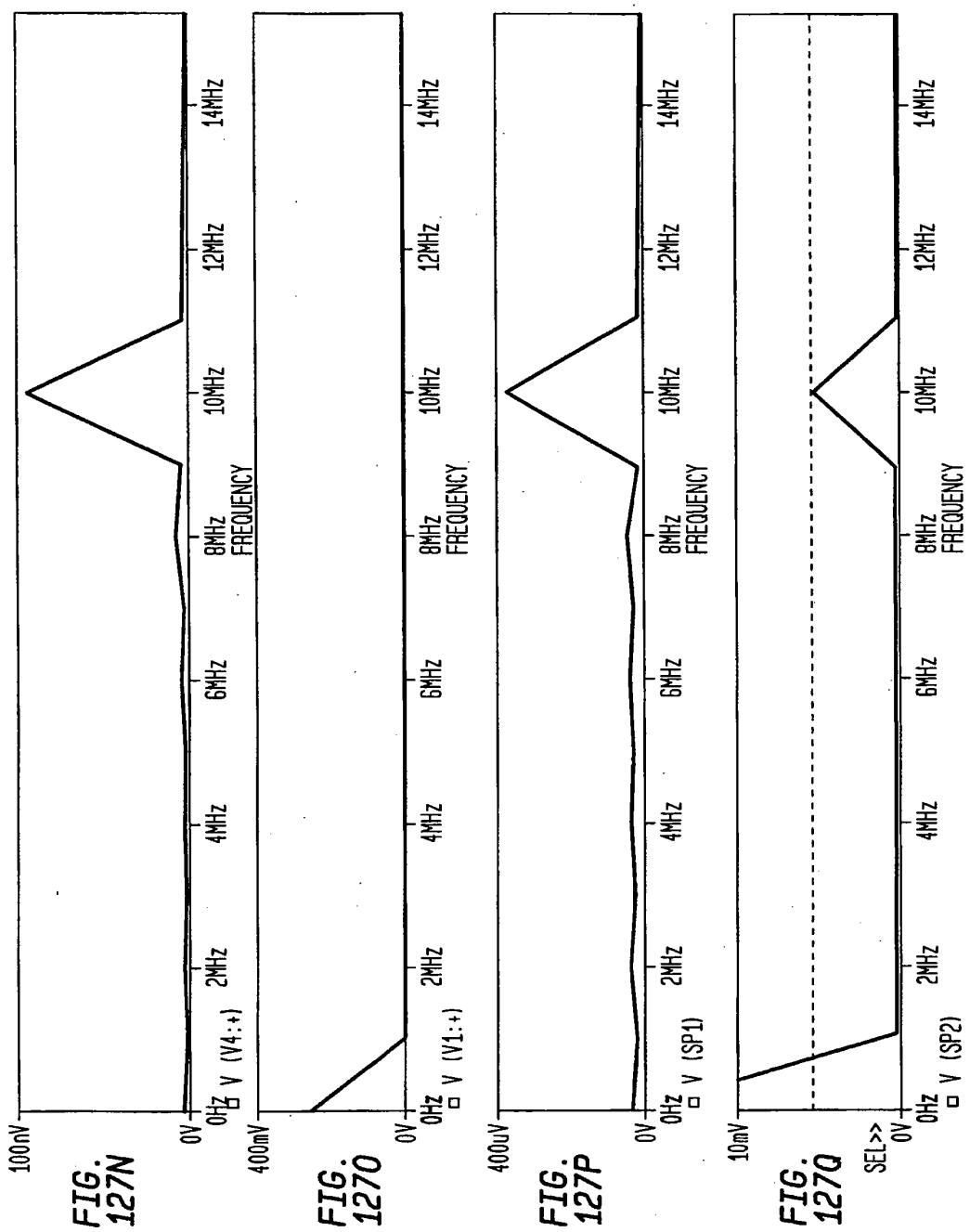


FIG. 127N

FIG. 127O

FIG. 127P

FIG. 127Q

FIG. 128A

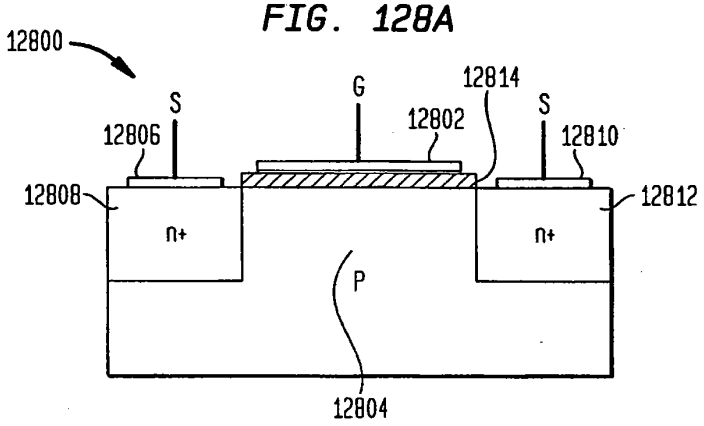


FIG. 128B

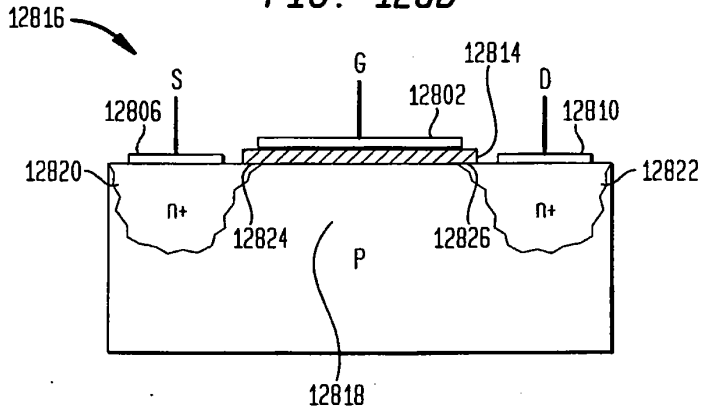


FIG. 128C

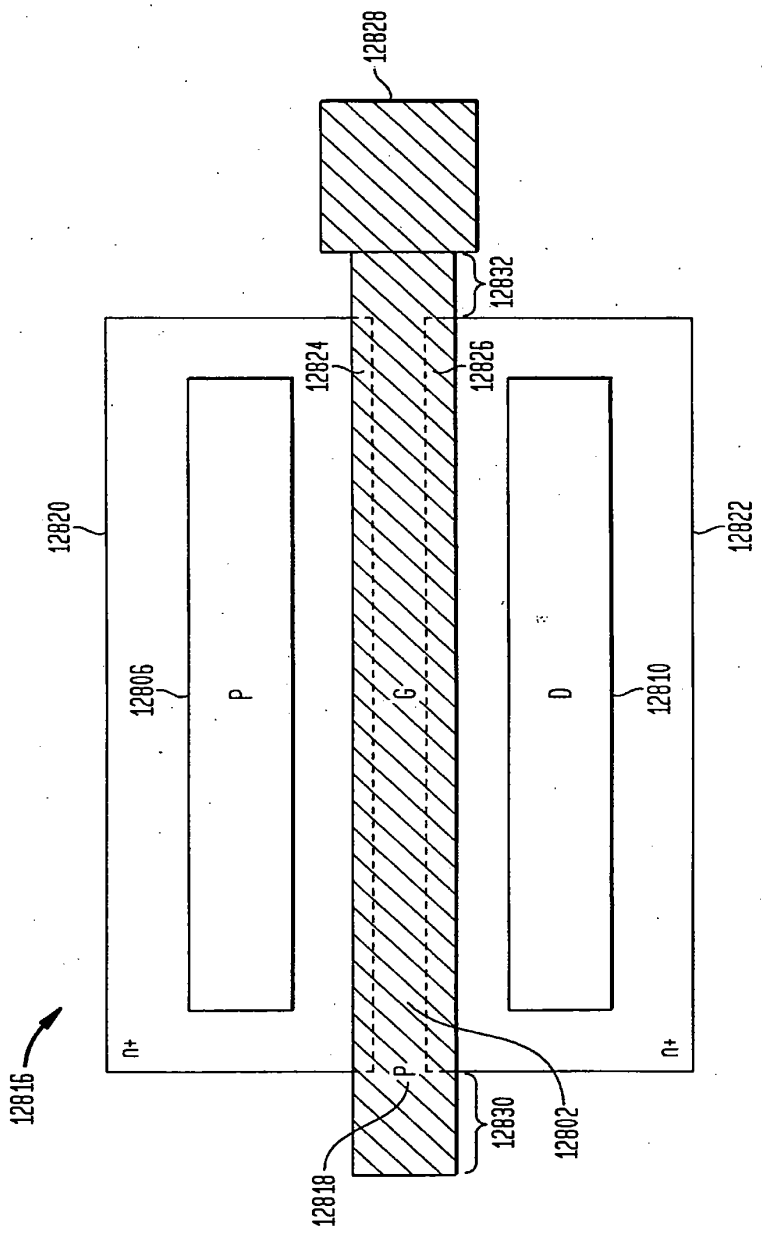
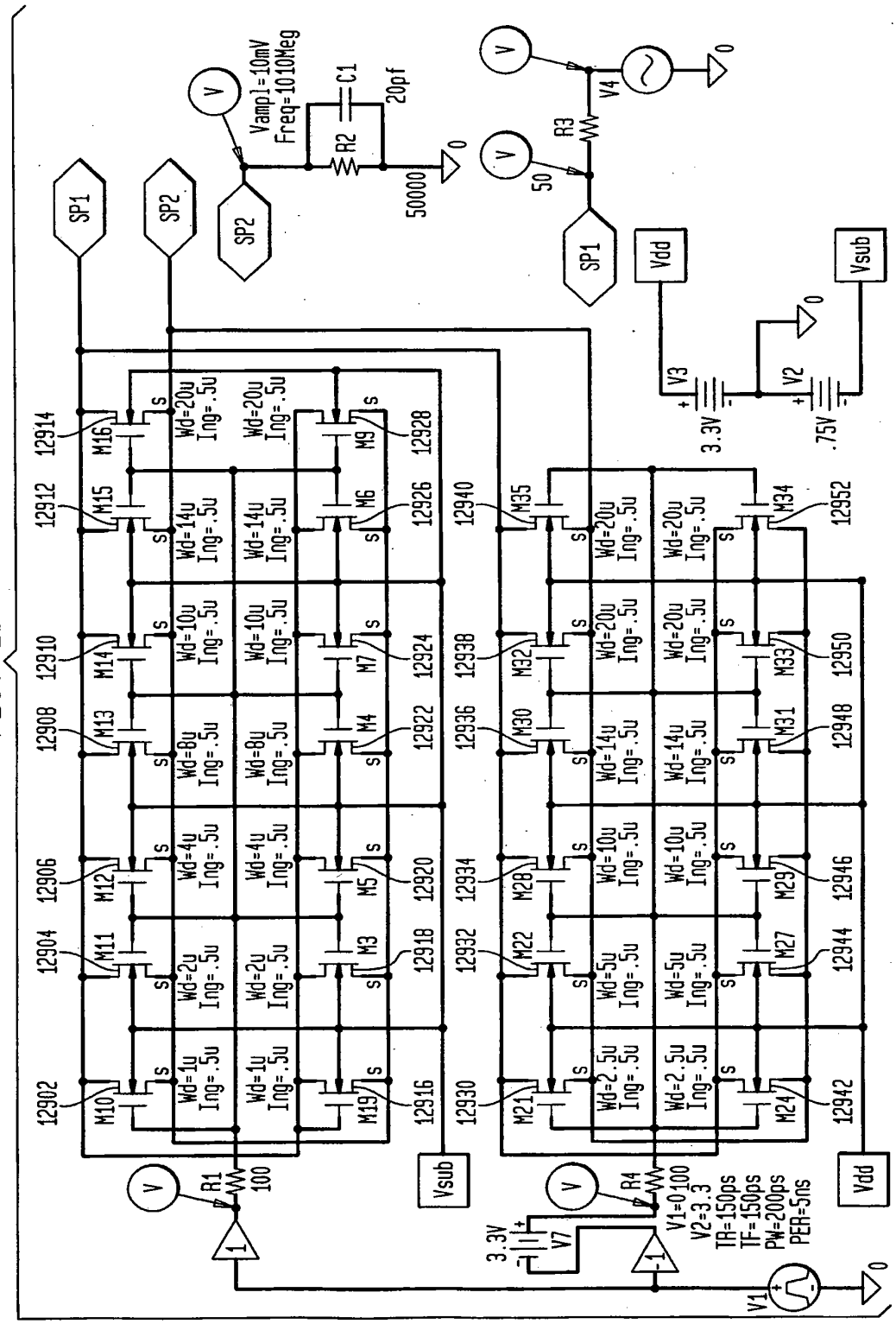

12828
12832
12824
12826
12820
12822
12806
P
G
D
12810
n+
n+
12816
P
12830
12802
12818

FIG. 129A


SP1
SP2
Vampl=10mV
Freq=1010Meg
C1
20pf
R2
50000
R3
50
V4
Vdd
Vsub
V3
3.3V
V2
.75V
R1
100
R4
V7
3.3V
V1=0100
V2=3.3
TR=150ps
TF=150ps
PW=200ps
PER=5ns
V1
M10
M11
M12
M13
M14
M15
M16
M19
M3
M5
M4
M7
M6
M9
M21
M22
M28
M30
M32
M35
M27
M29
M31
M33
M34
M24
12902
12904
12906
12908
12910
12912
12914
12916
12918
12920
12922
12924
12926
12928
12930
12932
12934
12936
12938
12940
12942
12944
12946
12948
12950
12952
Wd=1u
Wd=2u
Wd=4u
Wd=8u
Wd=10u
Wd=14u
Wd=20u
Wd=2.5u
Wd=5u
Lng=.5u

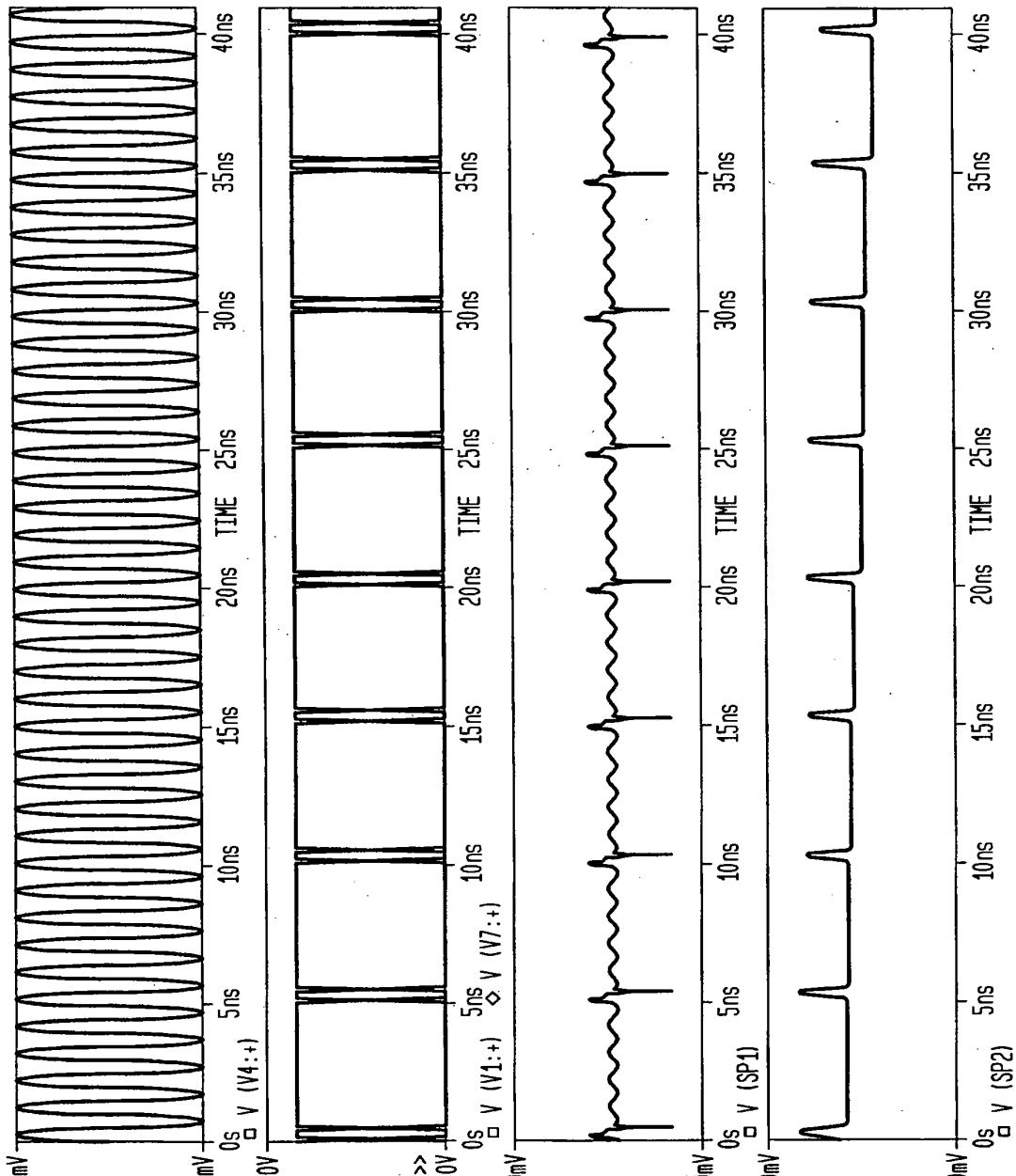


FIG. 129B

FIG. 129C

FIG. 129D

FIG. 129E

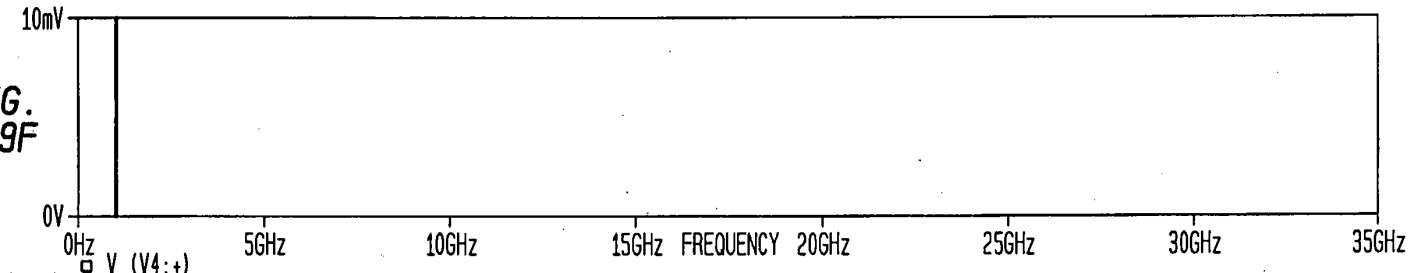


FIG. 129F

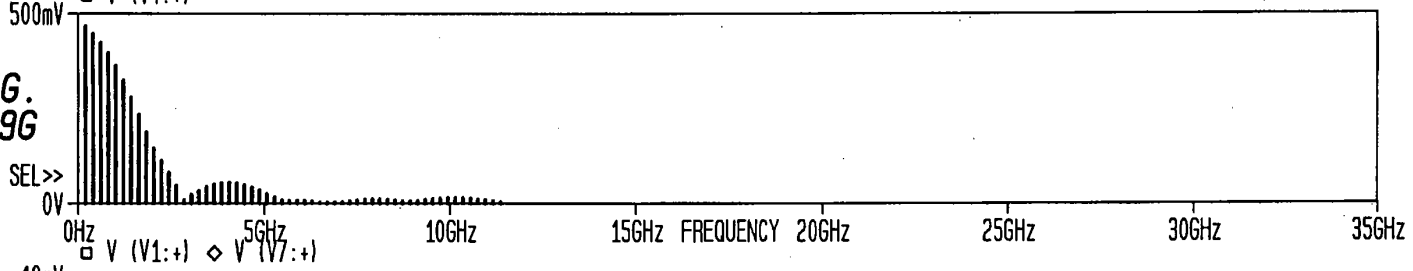


FIG. 129G

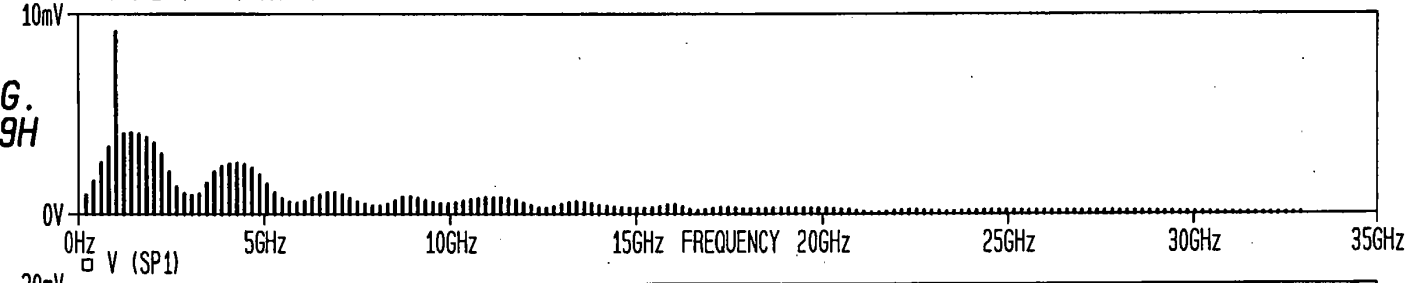


FIG. 129H

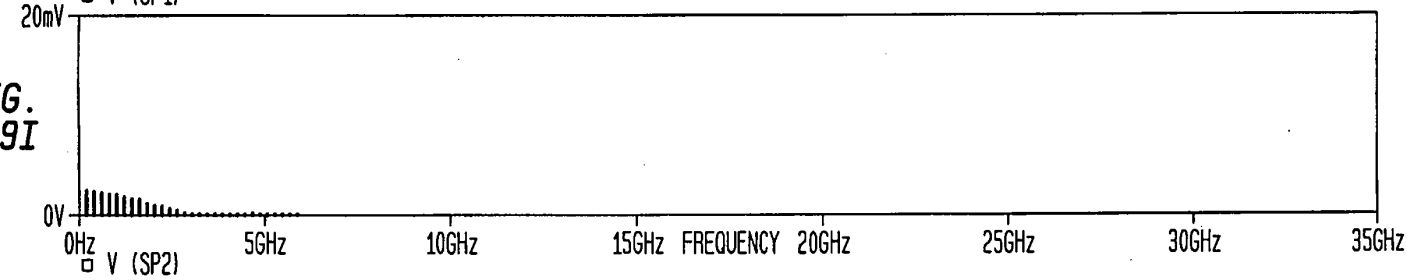


FIG. 129I

FIG. 129J

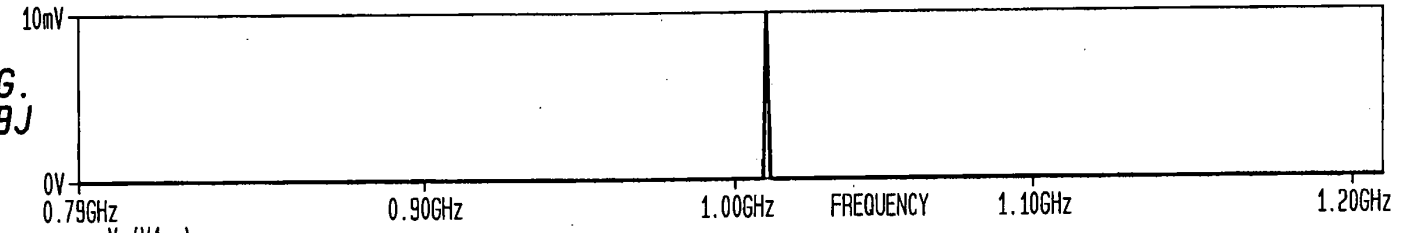


FIG. 129K

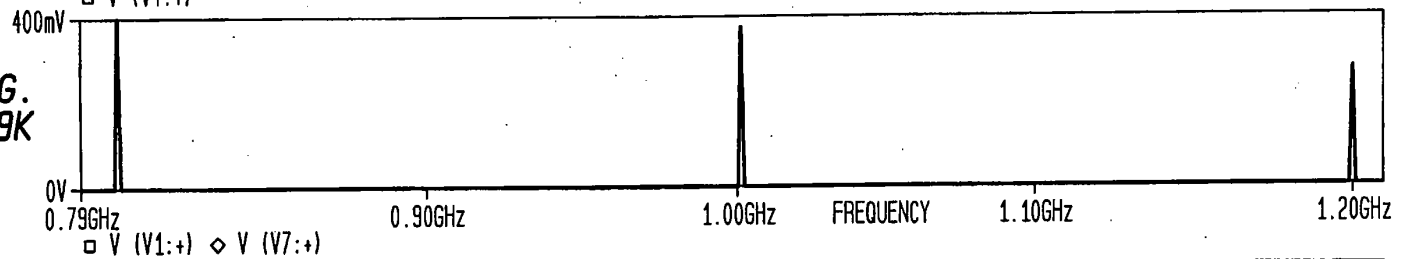


FIG. 129L

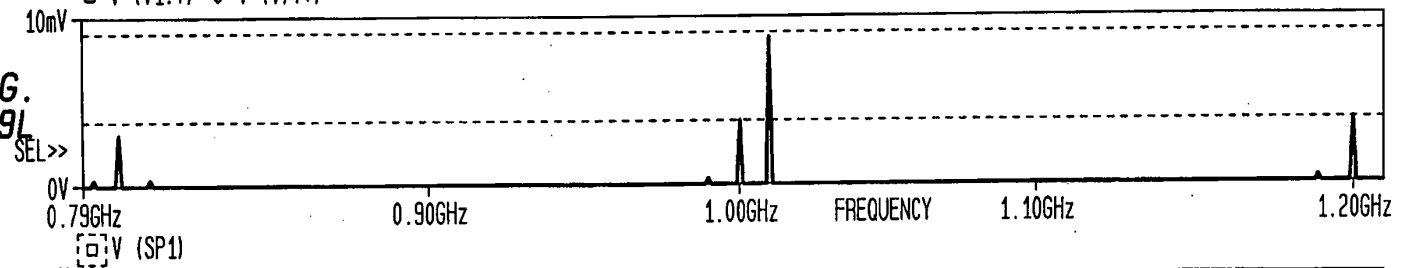
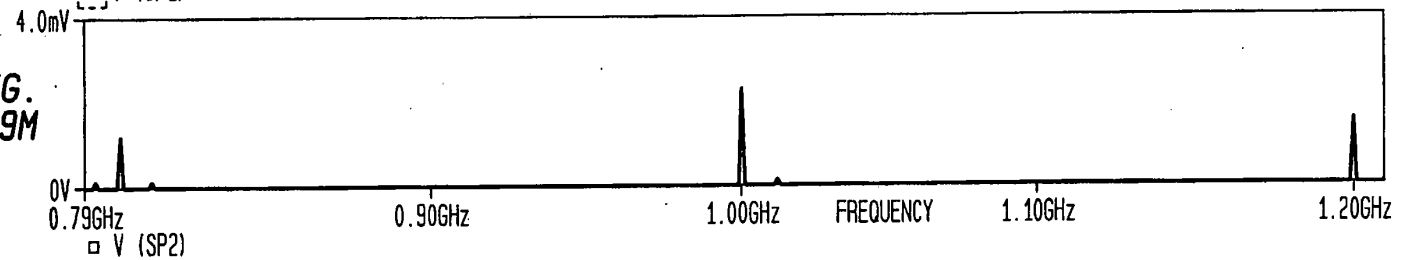


FIG. 129M



A1:(1.0000G, 3.9326m) A2:(788.000M, 9.0941u) DIFF(A):(212.000M, -3.9235m)

606

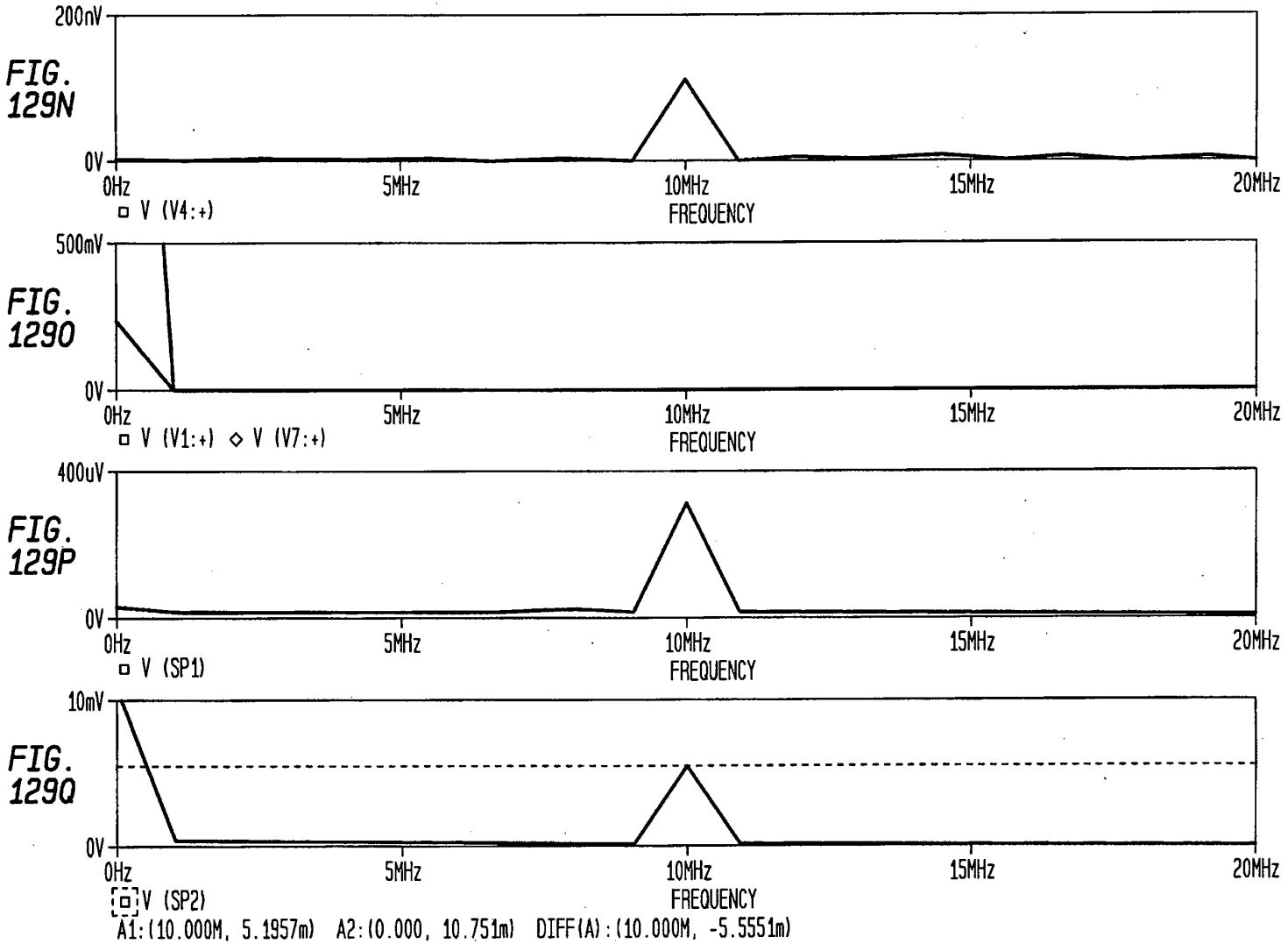


FIG. 129N

FIG. 129O

FIG. 129P

FIG. 129Q

910

FIG. 130

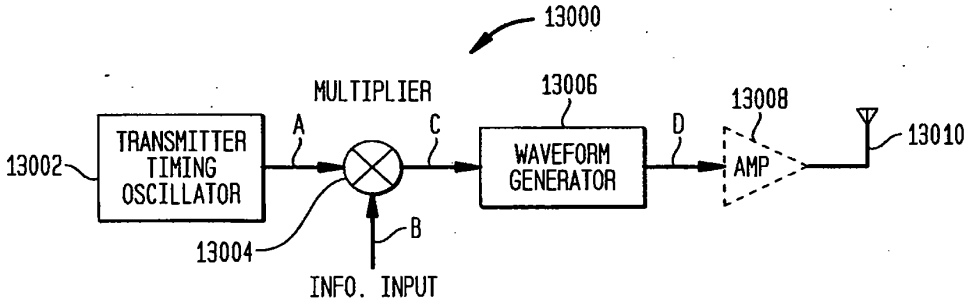

13000
MULTIPLIER
13006
13008
13010
13002
TRANSMITTER TIMING OSCILLATOR
A
C
WAVEFORM GENERATOR
D
AMP
13004
B
INFO. INPUT

FIG. 131

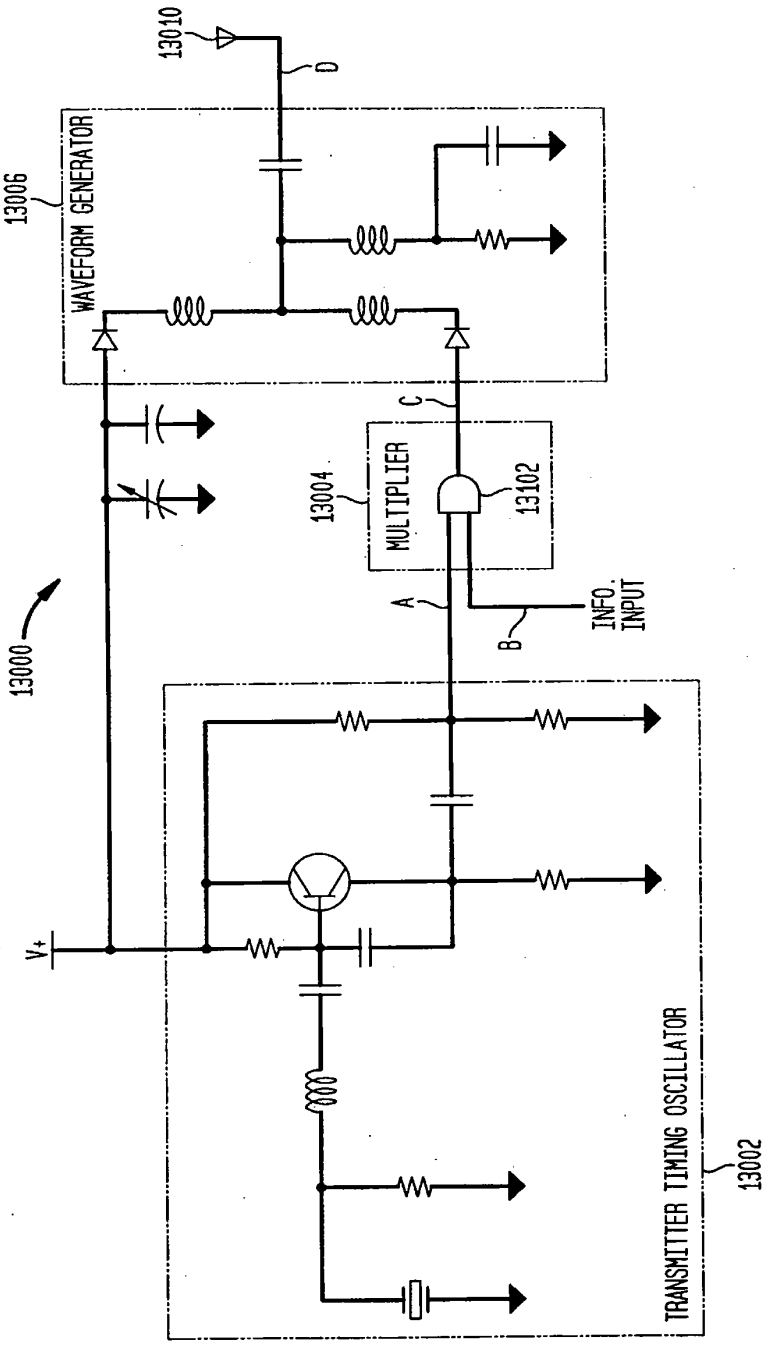

13010
D
13006
WAVEFORM GENERATOR
C
13004
MULTIPLIER
13102
A
B
INFO. INPUT
13000
V+
TRANSMITTER TIMING OSCILLATOR
13002

FIG. 132A

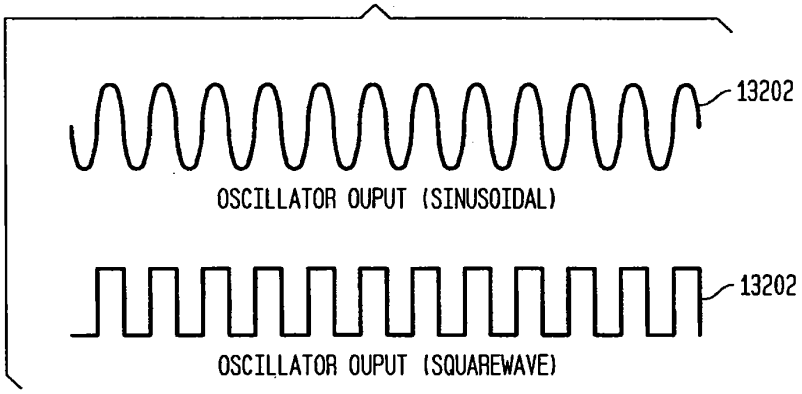


FIG. 132B

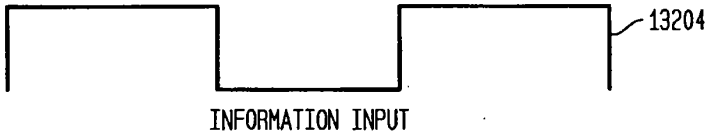


FIG. 132C

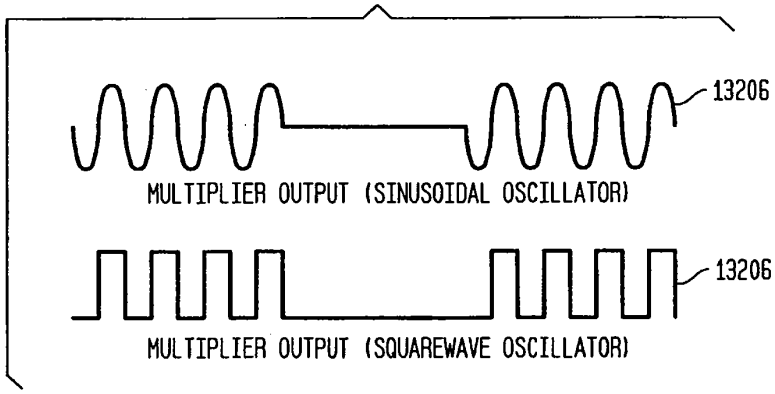


FIG. 132D

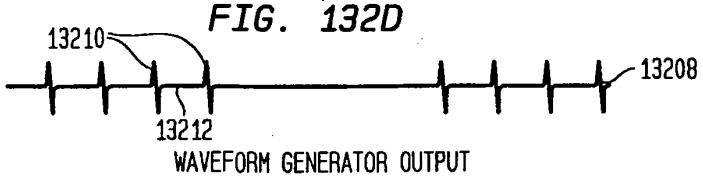


FIG. 133

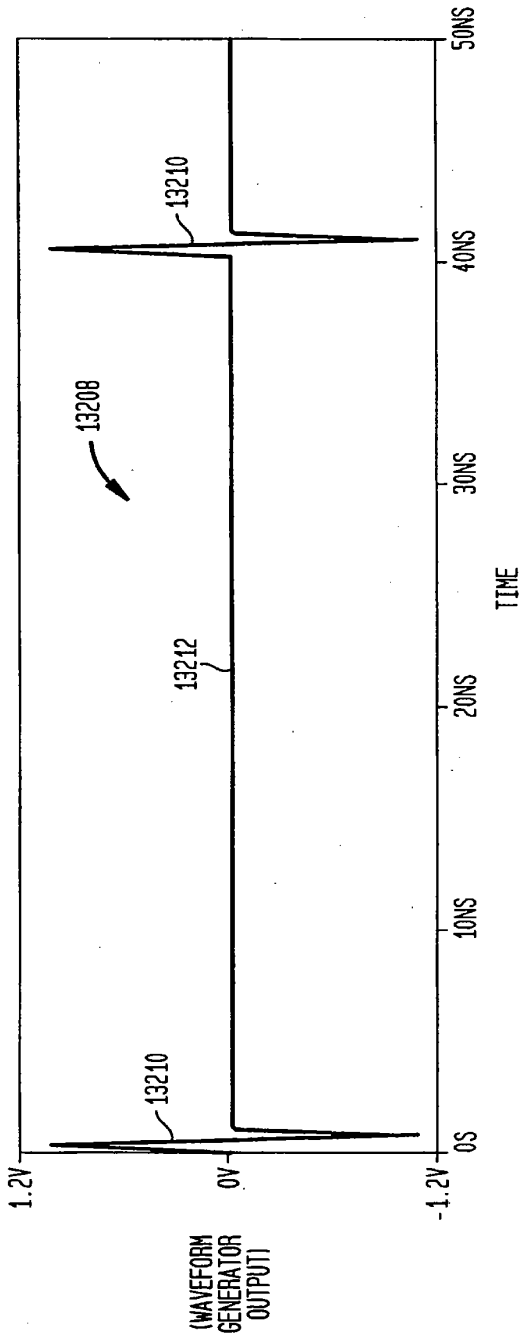

1.2V
0V
-1.2V
(WAVEFORM GENERATOR OUTPUT)
0S
10NS
20NS
30NS
40NS
50NS
TIME
13210
13212
13208
13210

FIG. 134

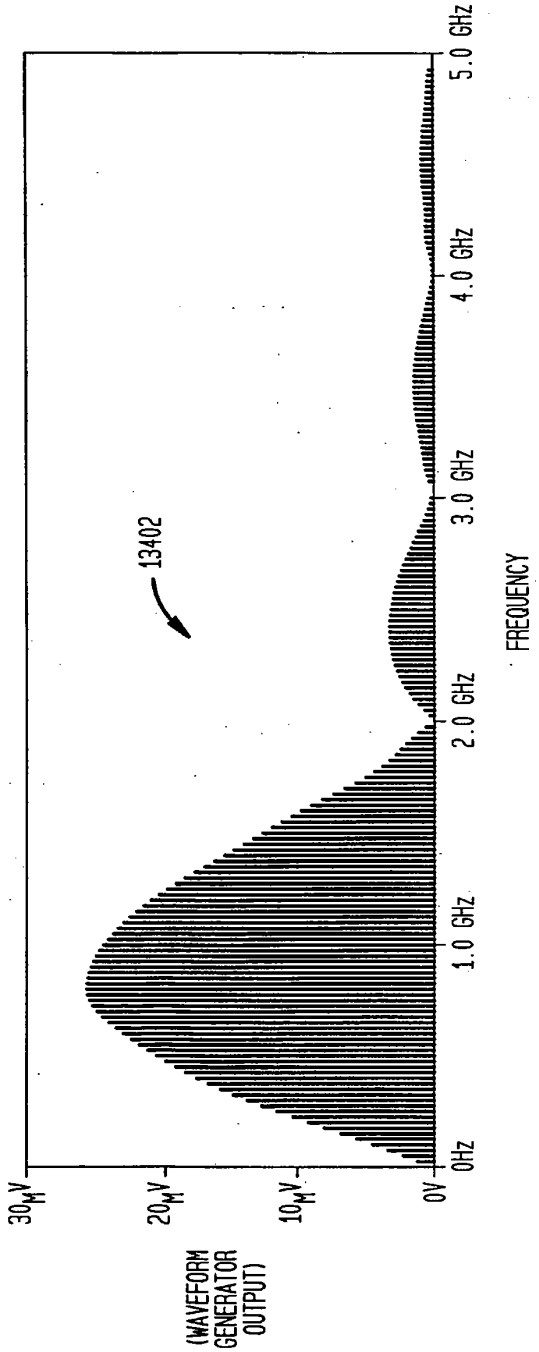

13402
30μV
20μV
10μV
0V
(WAVEFORM GENERATOR OUTPUT)
0Hz
1.0 GHz
2.0 GHz
3.0 GHz
4.0 GHz
5.0 GHz
FREQUENCY

FIG. 135

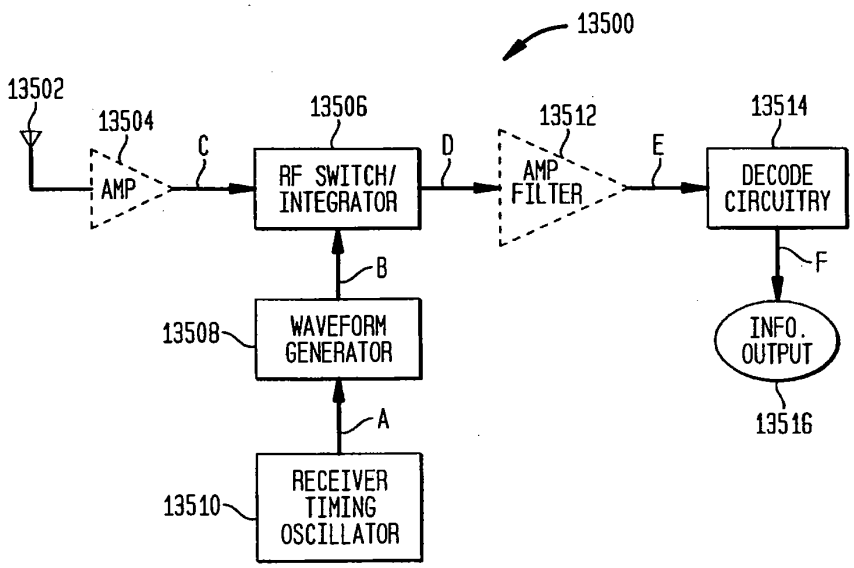
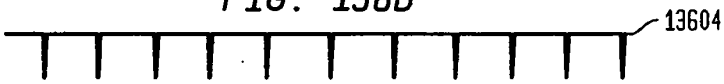

13500
13502
13504
AMP
C
13506
RF SWITCH/
INTEGRATOR
D
13512
AMP
FILTER
E
13514
DECODE
CIRCUITRY
F
INFO.
OUTPUT
13516
B
13508
WAVEFORM
GENERATOR
A
13510
RECEIVER
TIMING
OSCILLATOR

FIG. 136A



RECEIVER TIMING OSCILLATOR OUTPUT

FIG. 136B



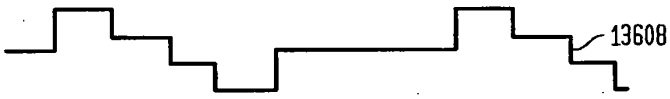
WAVEFORM GENERATOR OUTPUT

FIG. 136C



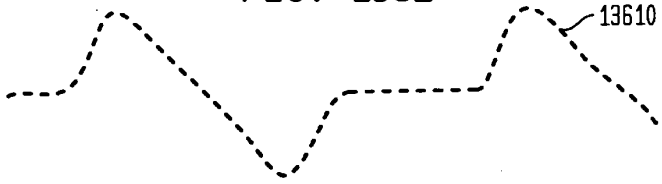
RF INPUT

FIG. 136D



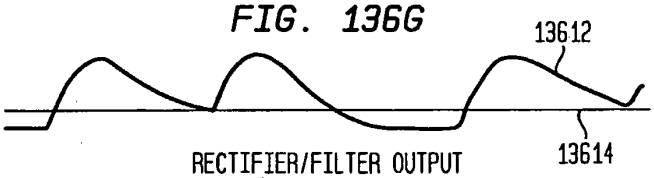
RF SWITCH/INTEGRATOR OUTPUT

FIG. 136E



OPTIONAL AMPLIFIER/FILTER OUTPUT

FIG. 136G



RECTIFIER/FILTER OUTPUT
VARIABLE THRESHOLD GENERATOR OUTPUT

FIG. 136F

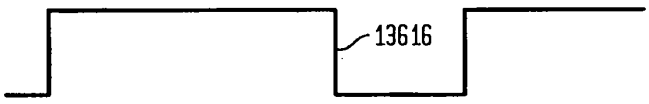
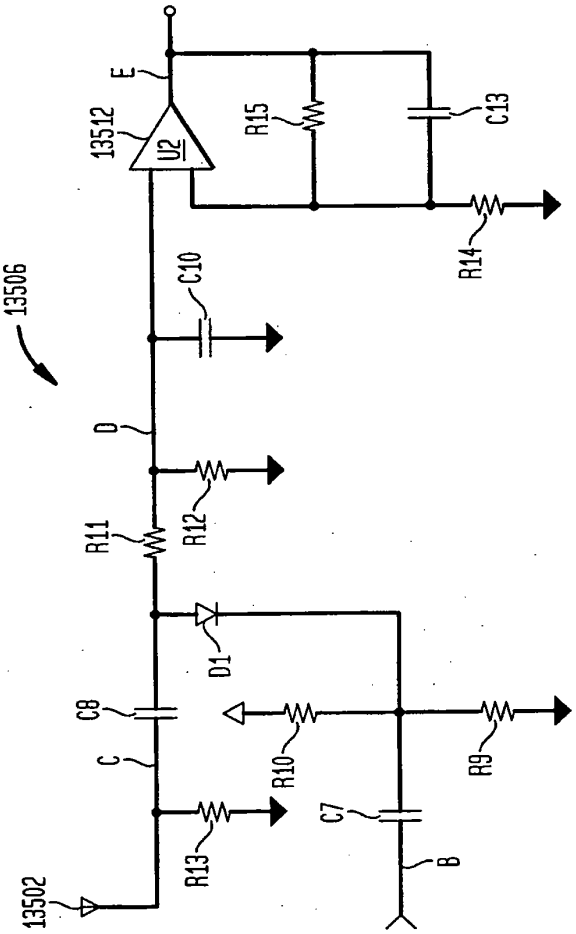


FIG. 137


13506
13502
13512
U2
E
D
C
B
C13
R15
R14
C10
R12
R11
D1
C8
R10
R9
C7
R13

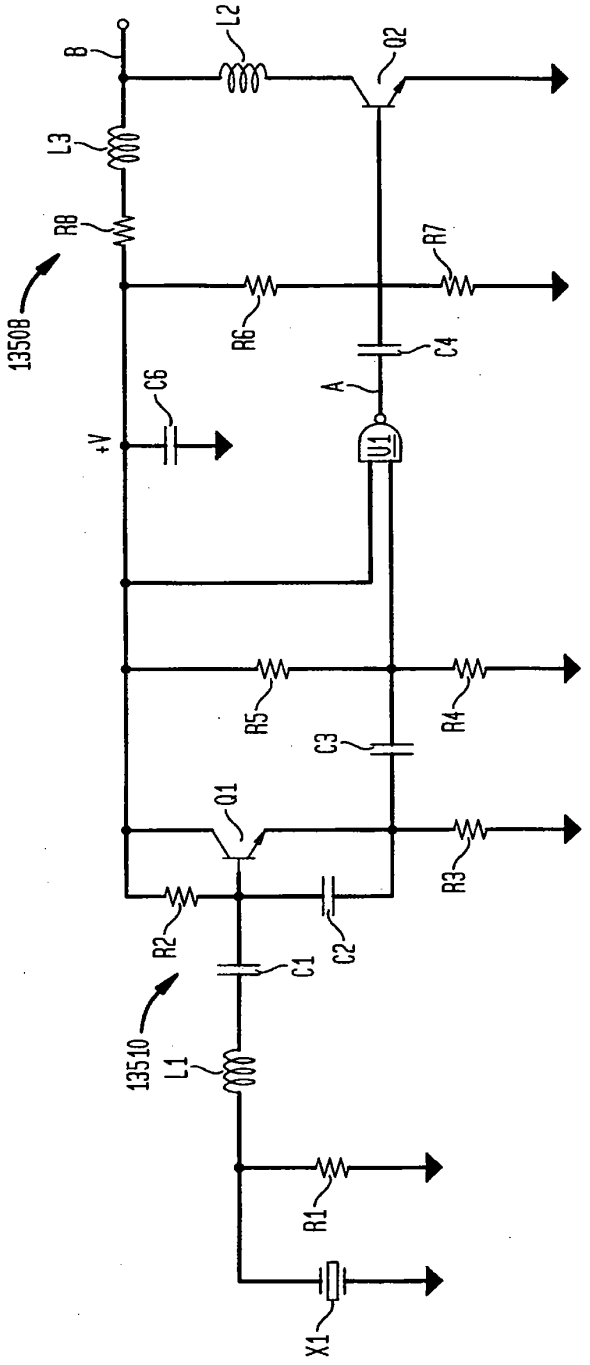

B
L2
Q2
L3
R8
13508
R7
R6
C4
A
C6
+V
U1
R5
R4
C3
Q1
R3
R2
C2
C1
13510
L1
R1
X1

FIG. 138

FIG. 139

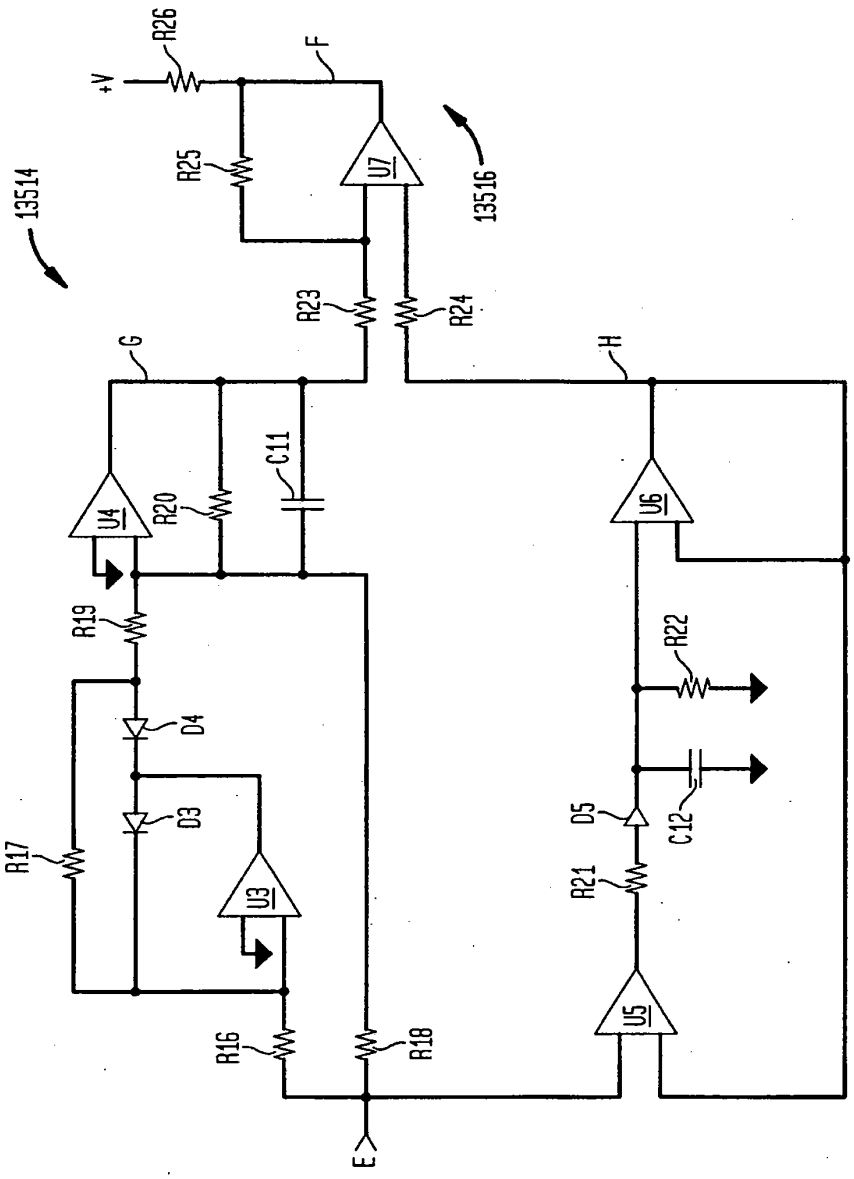

13514
13516
+V
R26
F
R25
U7
R23
R24
G
H
C11
U4
R20
U6
R19
R22
D4
D3
D5
C12
R17
U3
R21
U5
R16
R18
E

FIG. 140

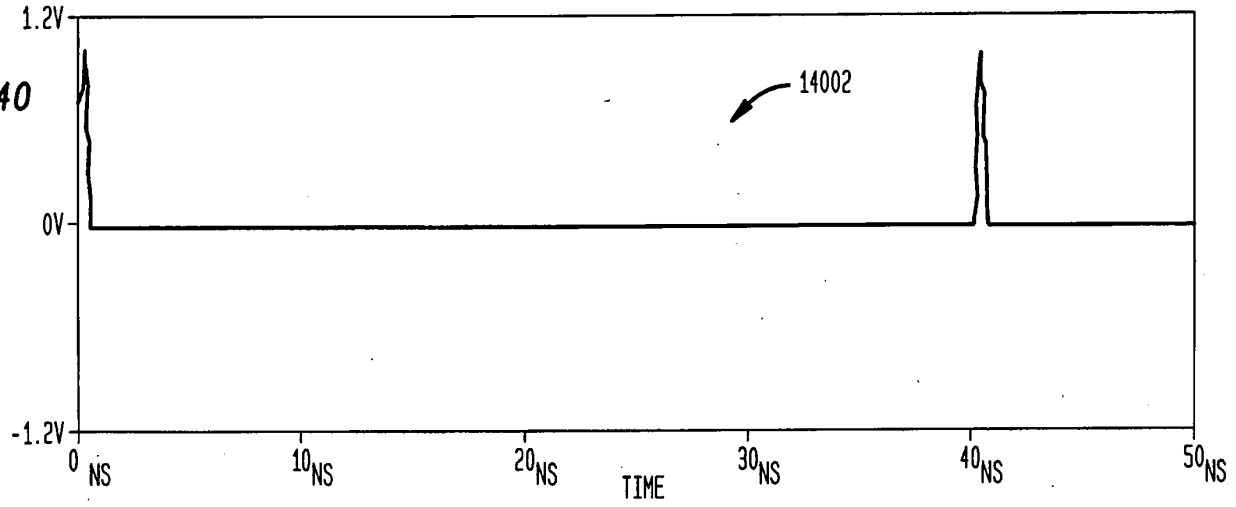


FIG. 141

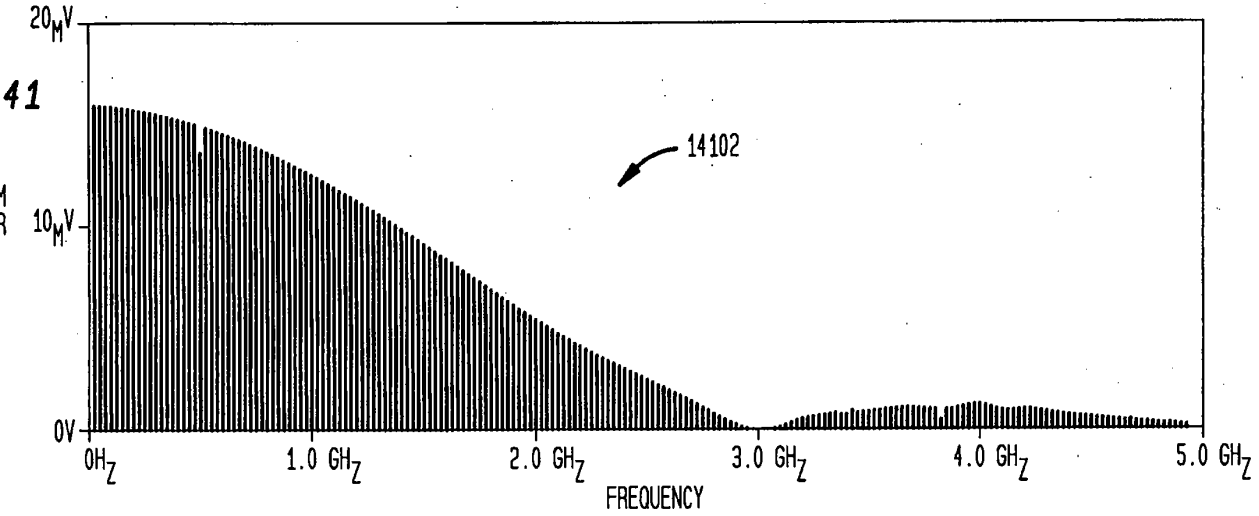


FIG. 142

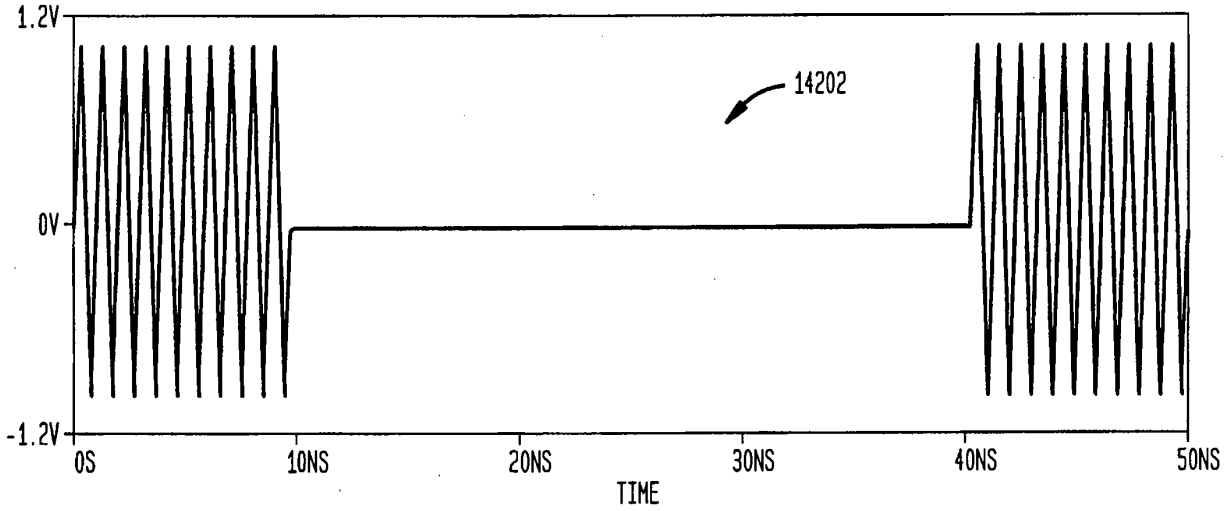


FIG. 143

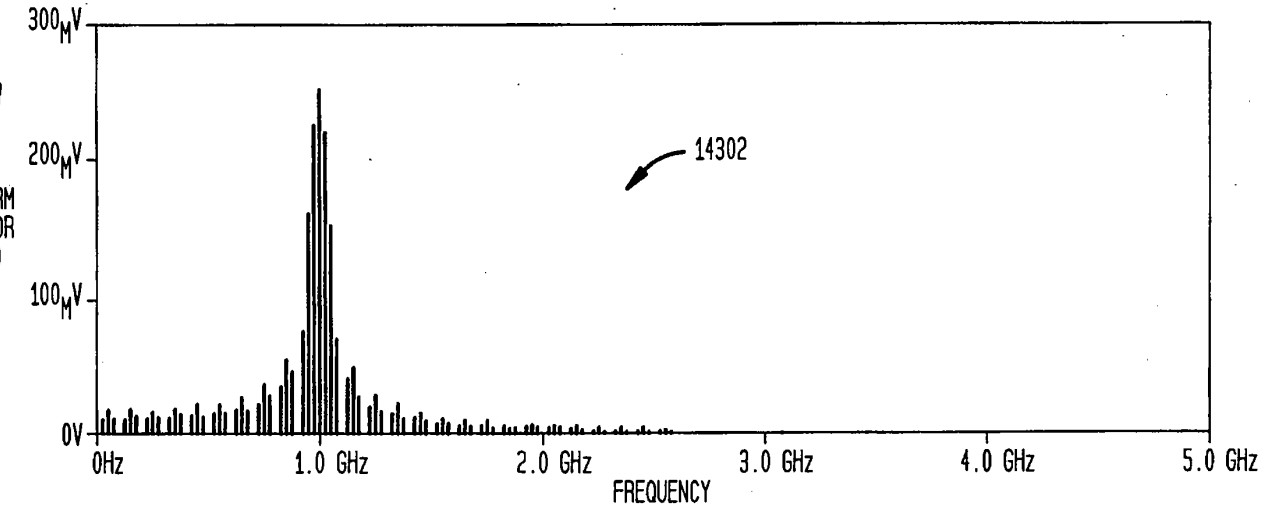


FIG. 144

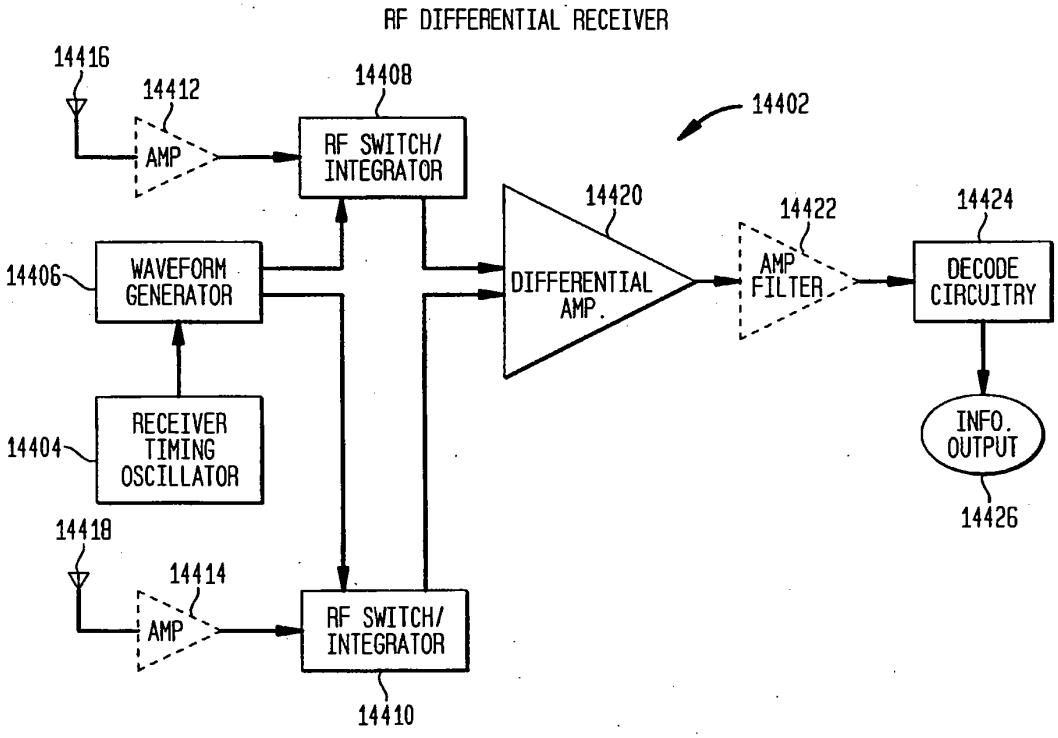

RF DIFFERENTIAL RECEIVER
14416
14412
AMP
14408
RF SWITCH/ INTEGRATOR
14402
14420
DIFFERENTIAL AMP.
14422
AMP FILTER
14424
DECODE CIRCUITRY
14406
WAVEFORM GENERATOR
14404
RECEIVER TIMING OSCILLATOR
INFO. OUTPUT
14426
14418
14414
AMP
RF SWITCH/ INTEGRATOR
14410

FIG. 145

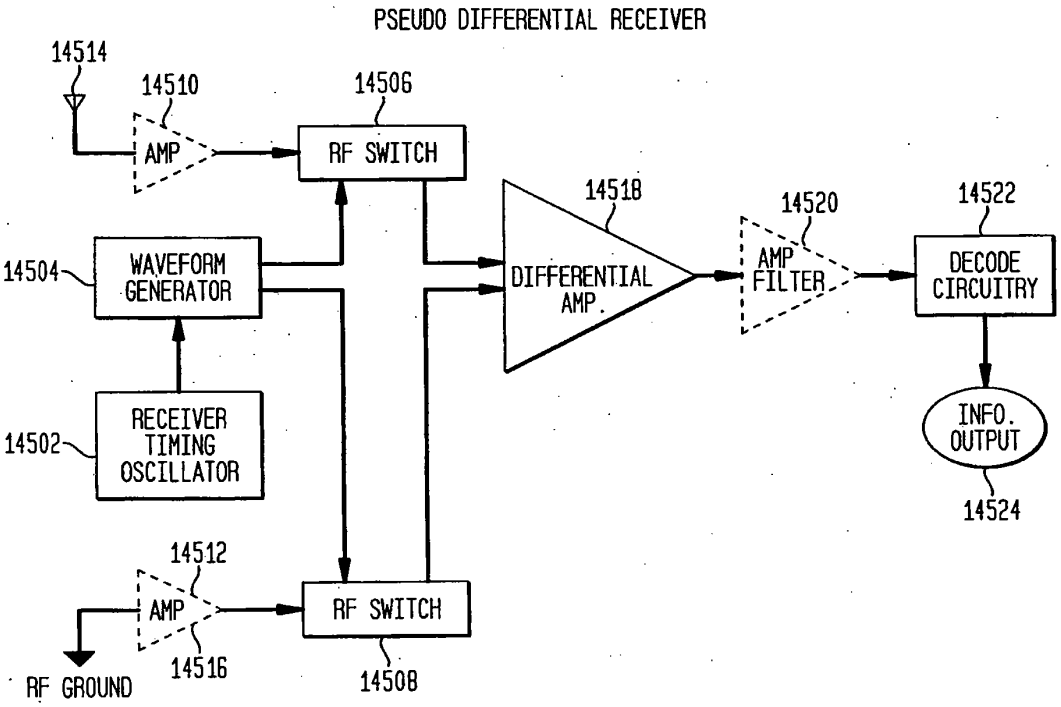

PSEUDO DIFFERENTIAL RECEIVER
14514
14510
AMP
14506
RF SWITCH
14518
DIFFERENTIAL AMP.
14520
AMP FILTER
14522
DECODE CIRCUITRY
INFO. OUTPUT
14524
14504
WAVEFORM GENERATOR
14502
RECEIVER TIMING OSCILLATOR
14512
AMP
14516
RF GROUND
RF SWITCH
14508

FIG. 146

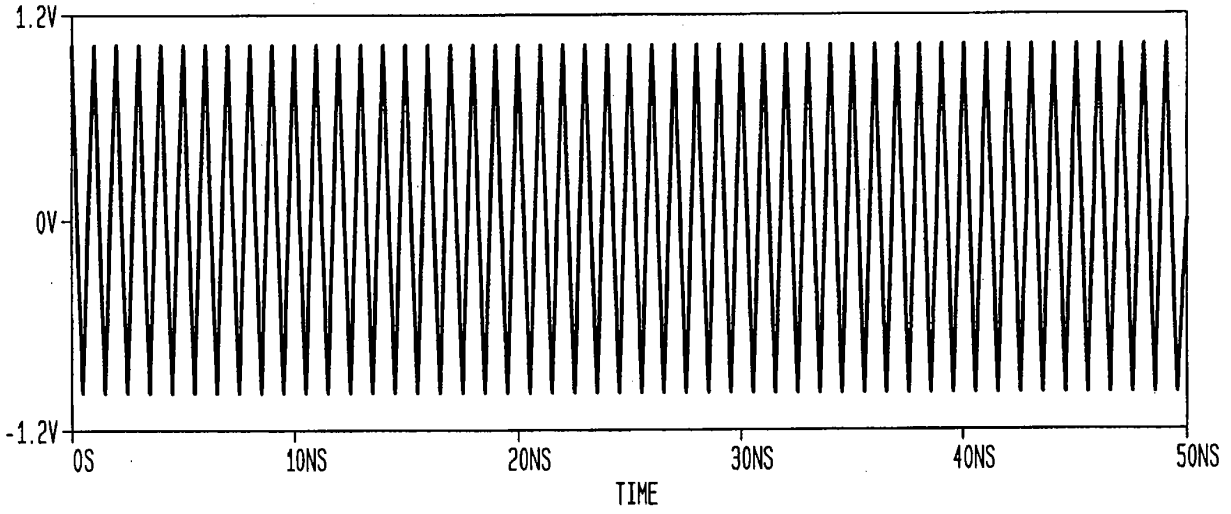


FIG. 147

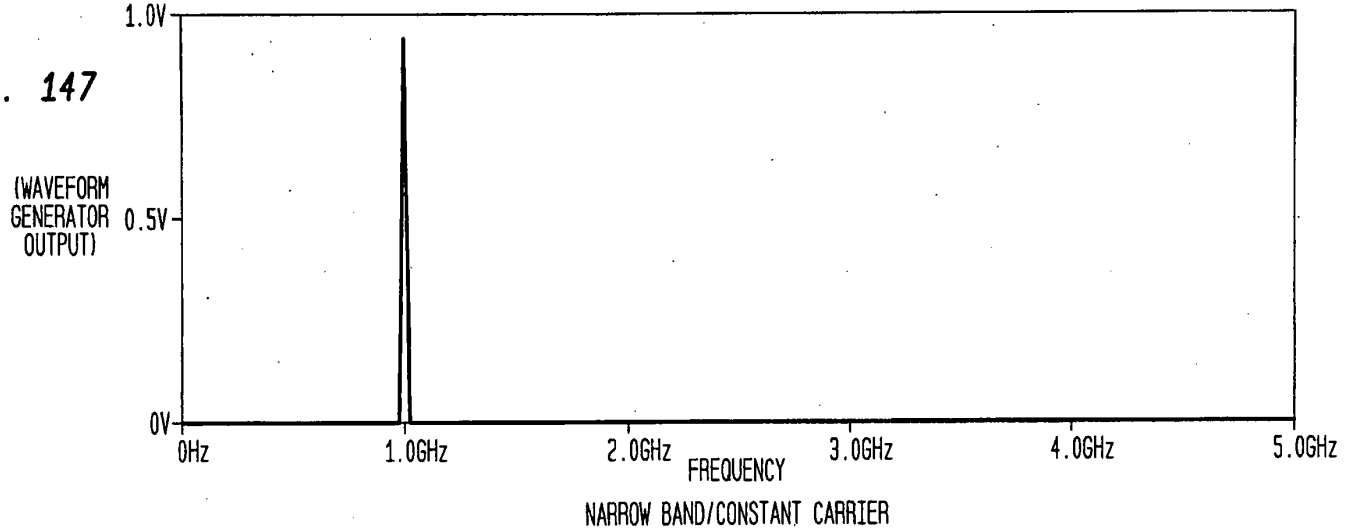


FIG. 148

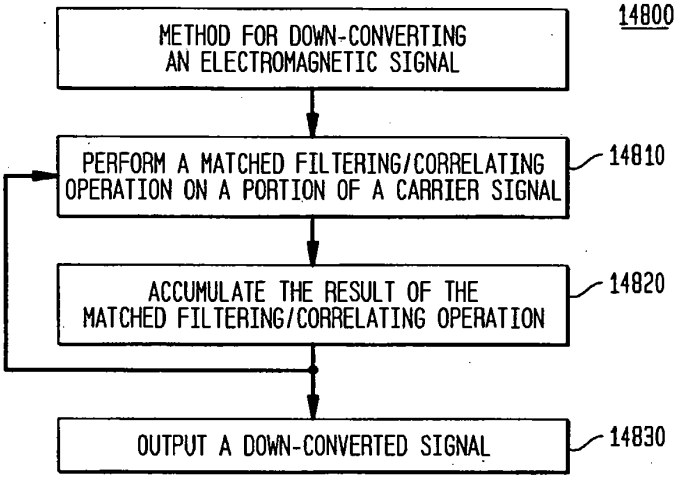


FIG. 149

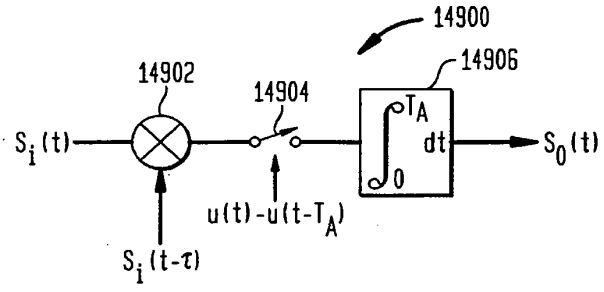


FIG. 150

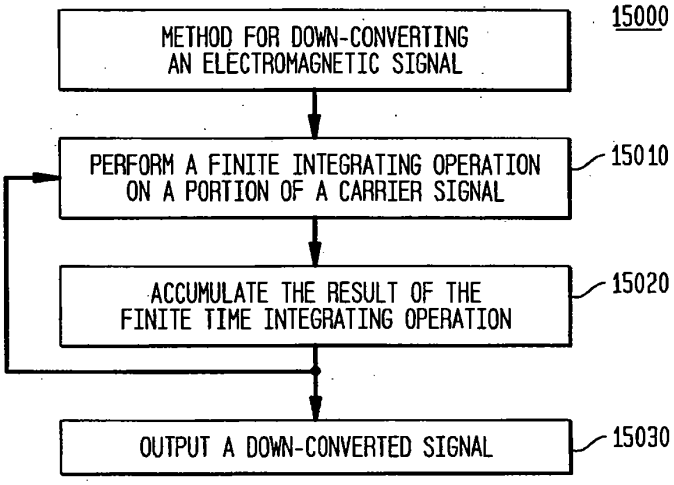


FIG. 151

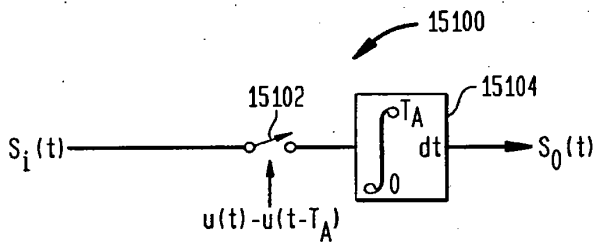


FIG. 152

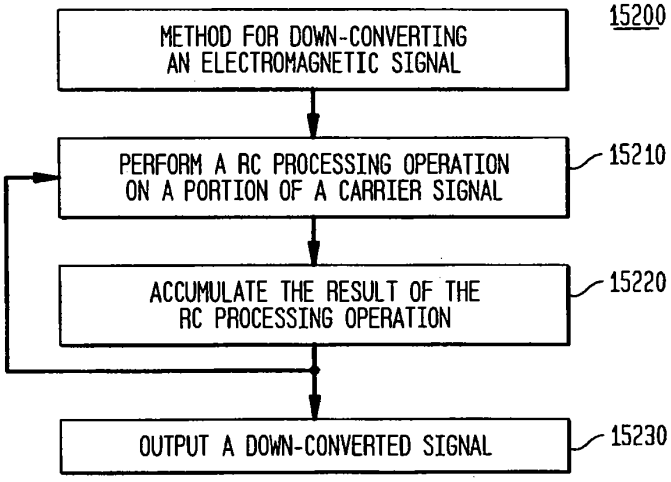


FIG. 153

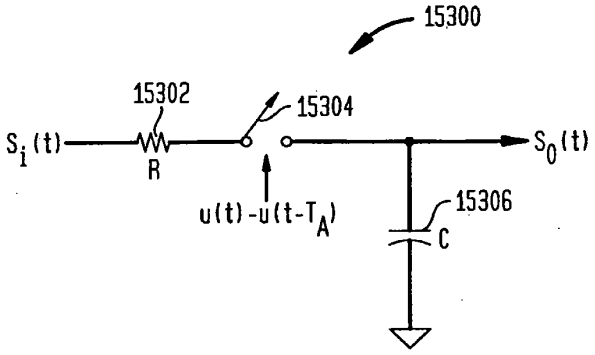


FIG. 154

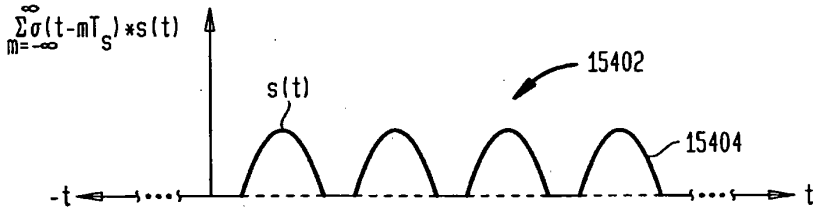


FIG. 155

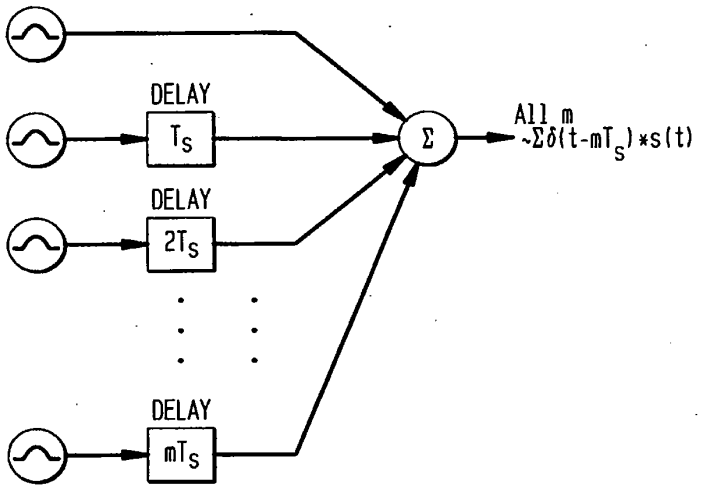


FIG. 156

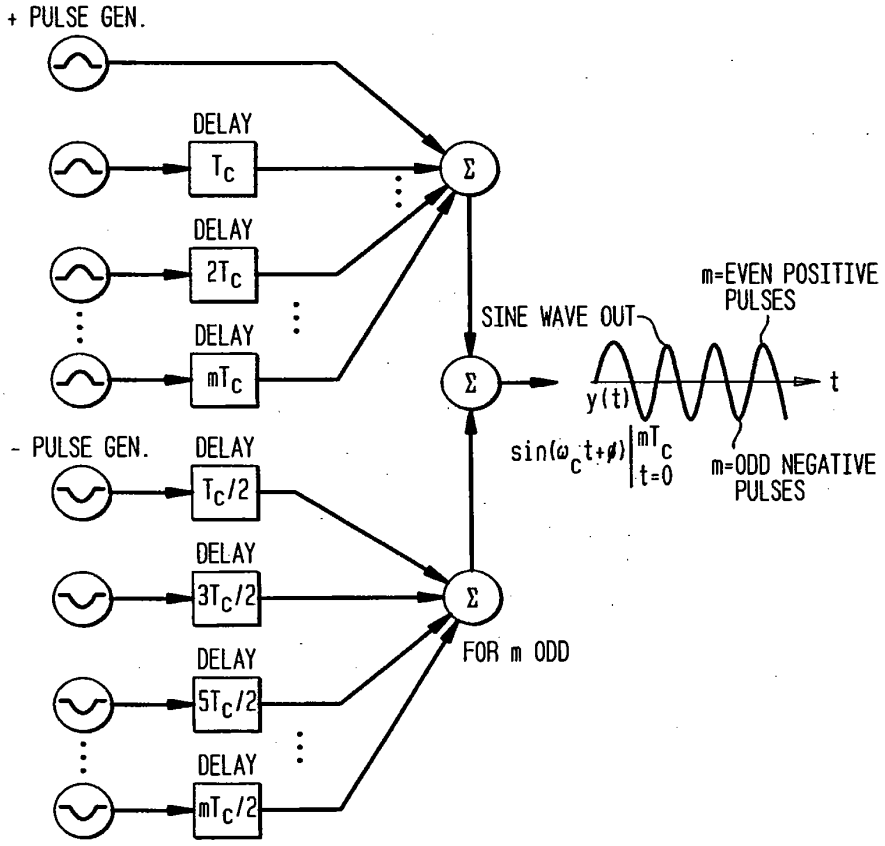
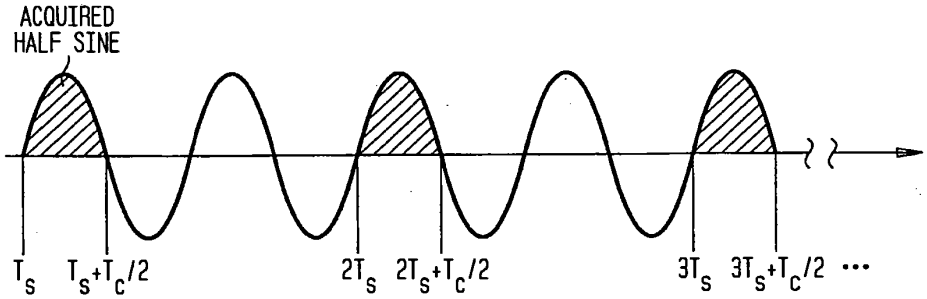


FIG. 157



CARRIER PROCESSED BY 3RD HARMONIC UFT PROCESSOR

FIG. 158

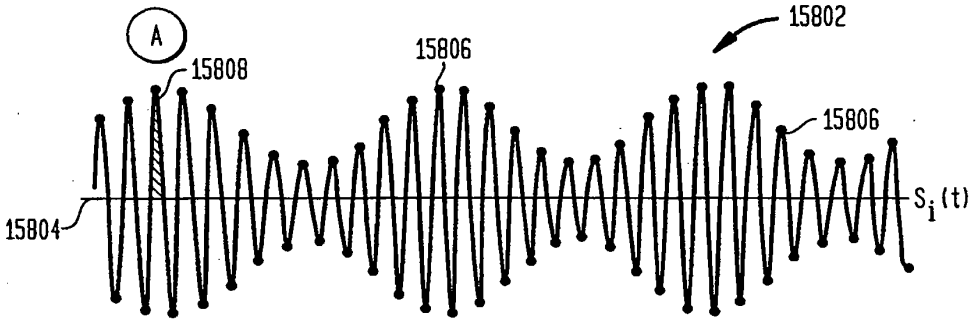


FIG. 159

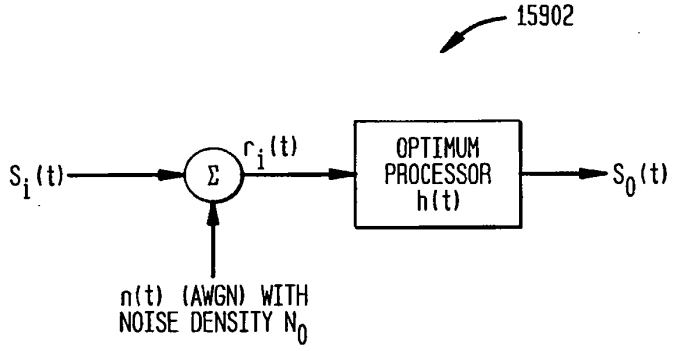
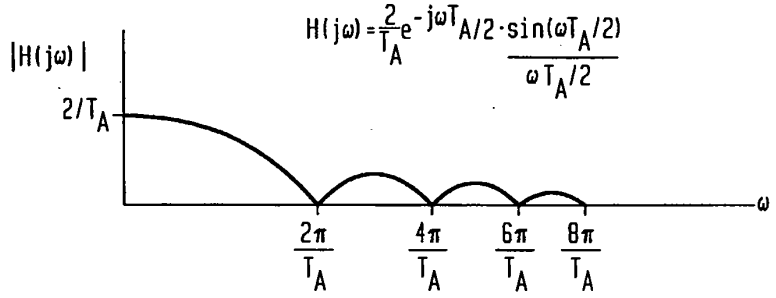
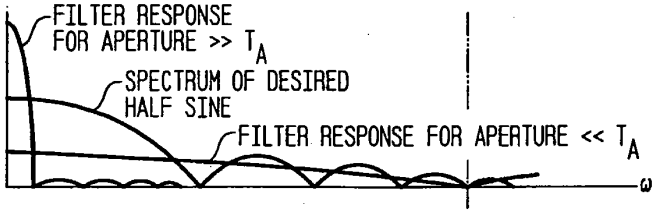


FIG. 160



MAG FREQUENCY RESPONSE OF
SAMPLING APERTURE WAVEFORM

FIG. 161



APERTURE FREQUENCY DOMAIN REPRESENTATION

FIG. 162

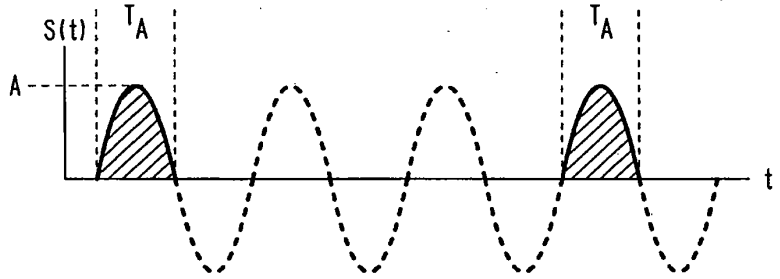


FIG. 163

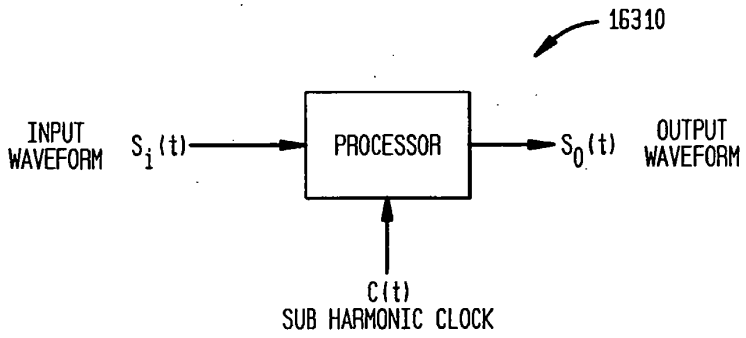


FIG. 164A

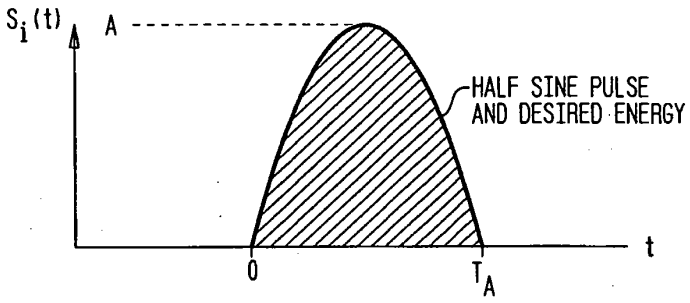


FIG. 164B

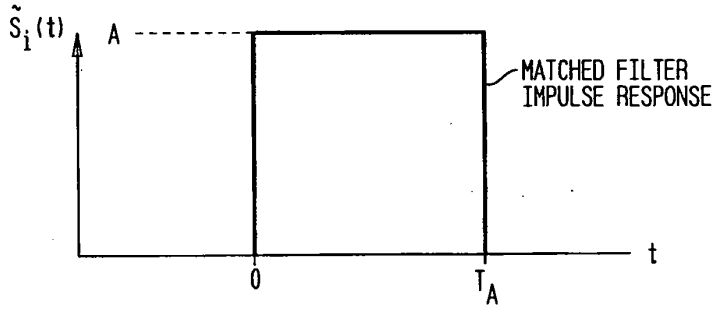


FIG. 164C

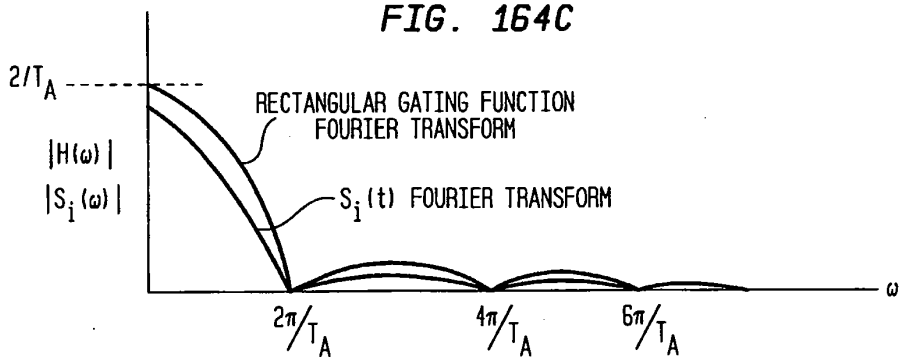


FIG. 165

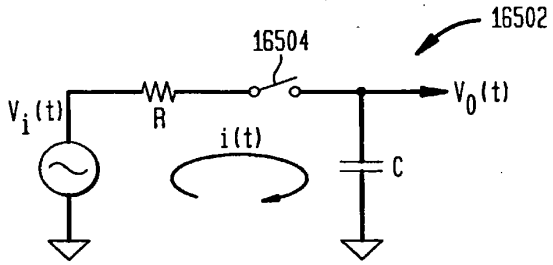


FIG. 166

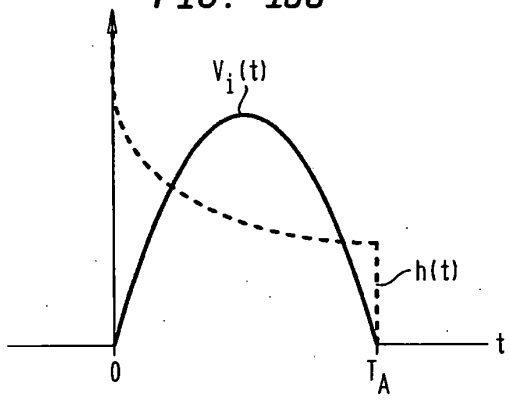


FIG. 167

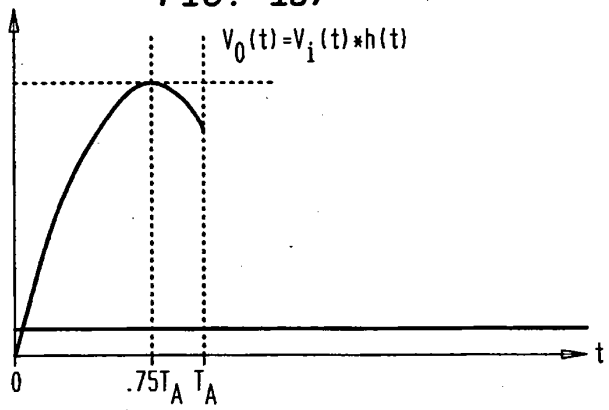


FIG. 168

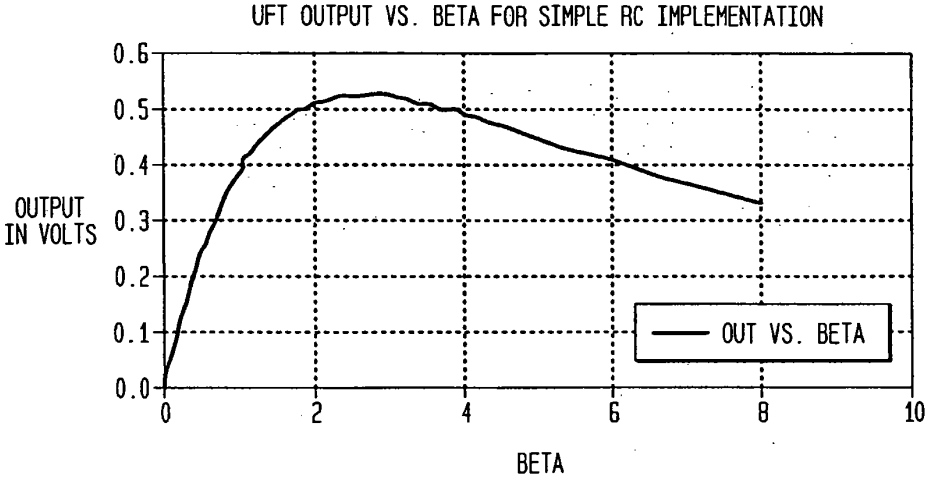


FIG. 169

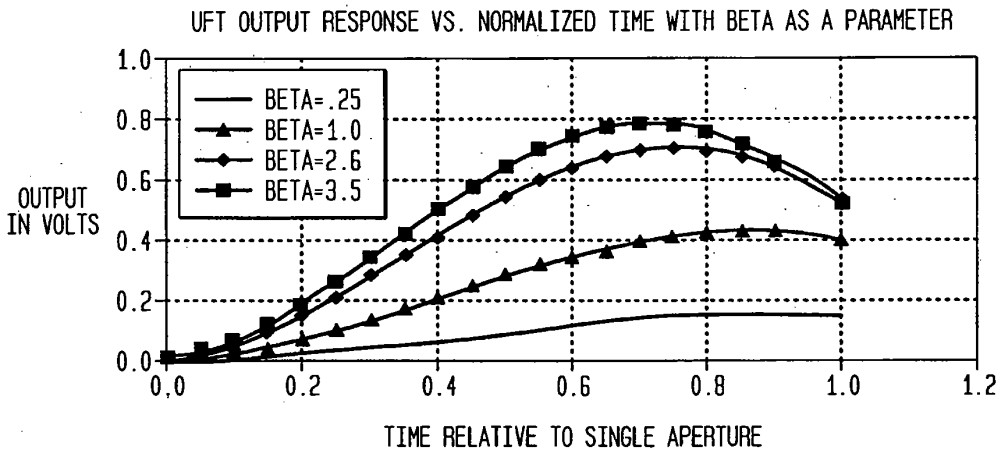


FIG. 170

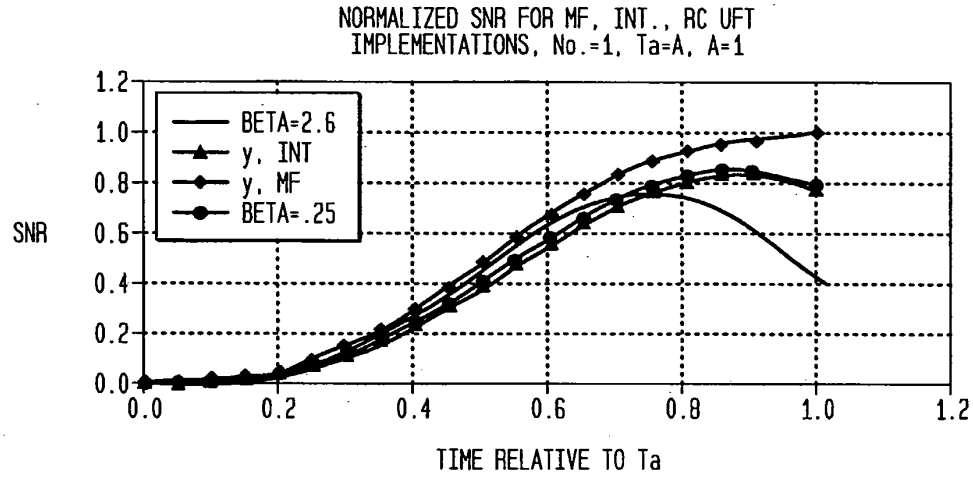


FIG. 171

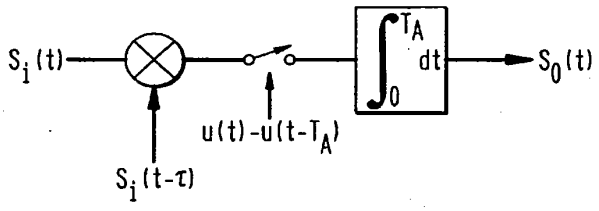


FIG. 172

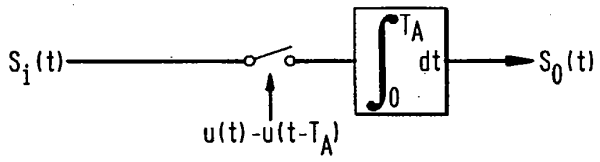


FIG. 173

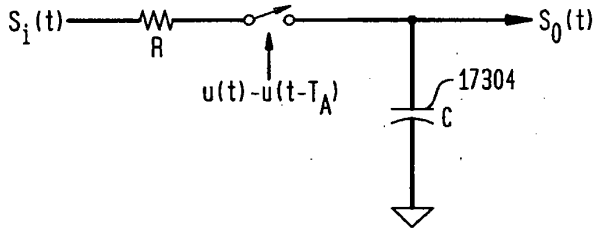


FIG. 174

UFT OUTPUT CHARGE TRANSFER

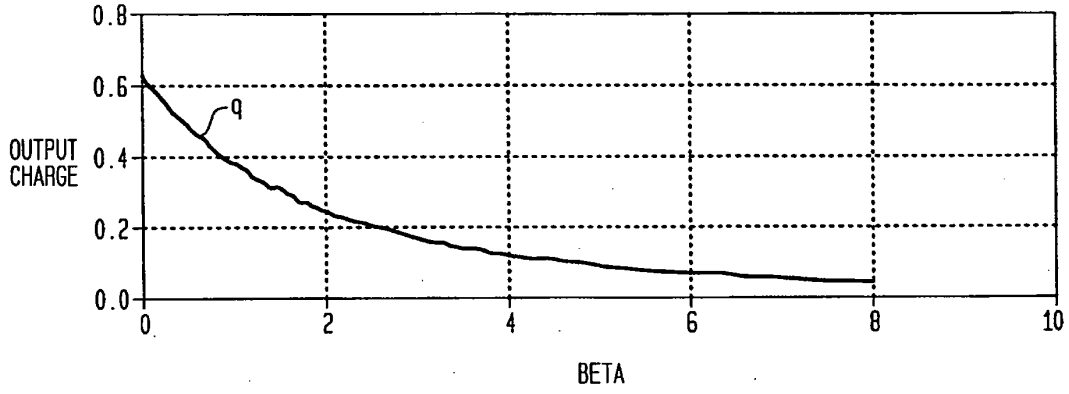


FIG. 175A

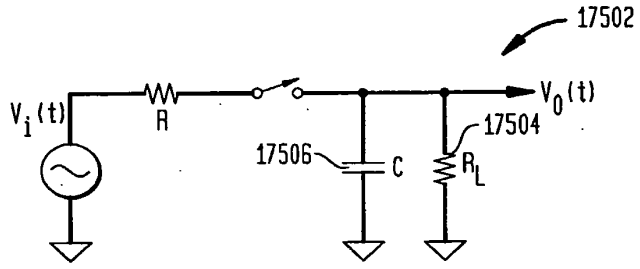


FIG. 175B

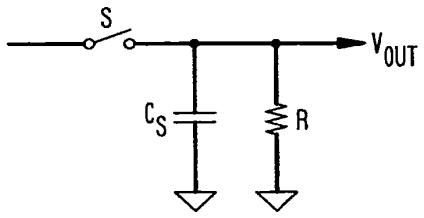


FIG. 175C

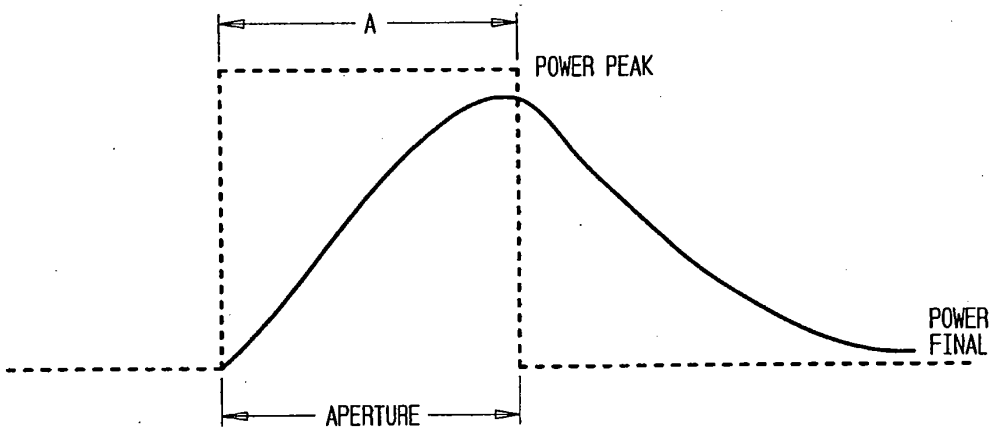


FIG. 175D

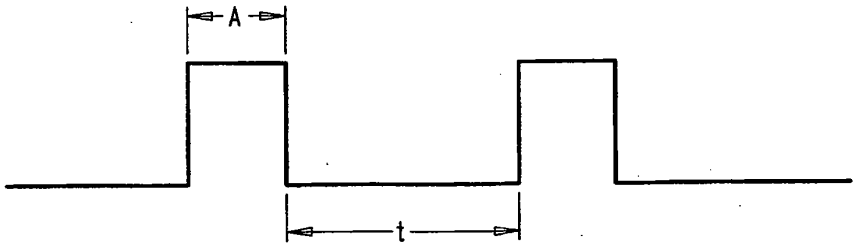


FIG. 176

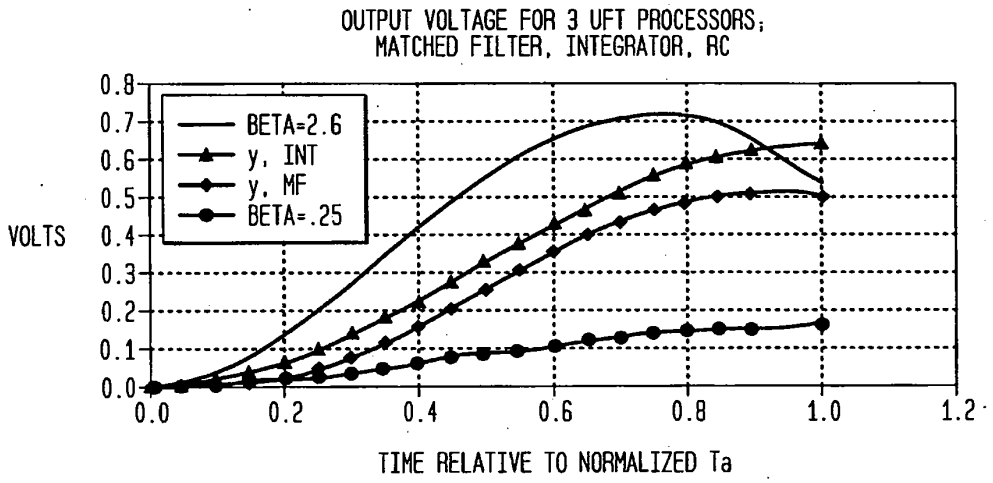

OUTPUT VOLTAGE FOR 3 UFT PROCESSORS;
MATCHED FILTER, INTEGRATOR, RC
BETA=2.6
y, INT
y, MF
BETA=.25
VOLTS
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.0
0.2
0.4
0.6
0.8
1.0
1.2
TIME RELATIVE TO NORMALIZED Ta

FIG. 177A

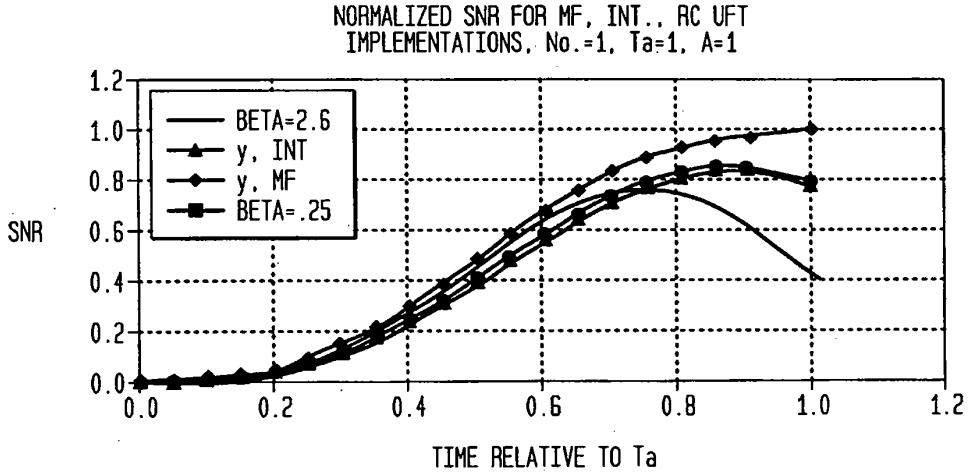

NORMALIZED SNR FOR MF, INT., RC UFT
IMPLEMENTATIONS, No.=1, Ta=1, A=1
BETA=2.6
y, INT
y, MF
BETA=.25
SNR
1.2
1.0
0.8
0.6
0.4
0.2
0.0
0.0
0.2
0.4
0.6
0.8
1.0
1.2
TIME RELATIVE TO Ta

FIG. 177B

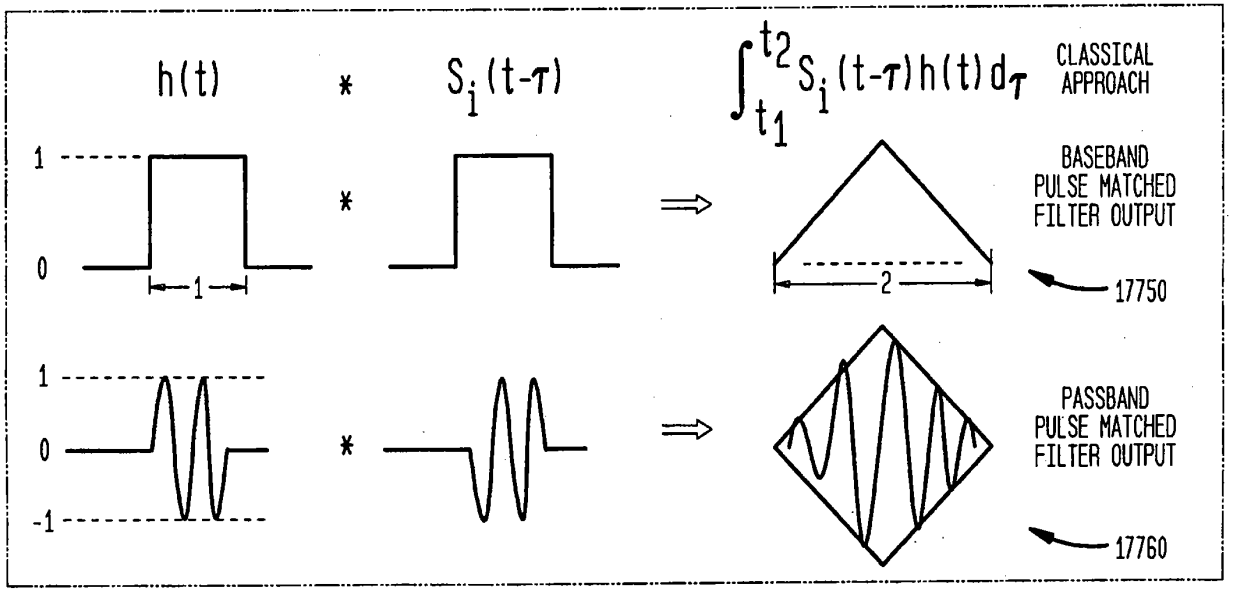


FIG. 177C

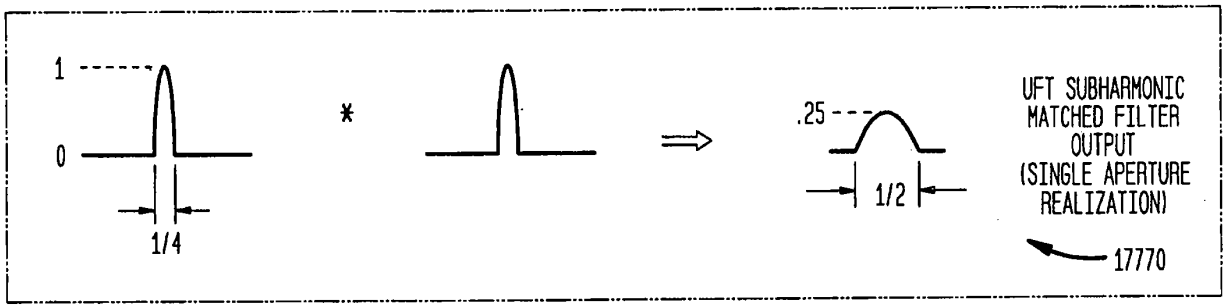


FIG. 177D

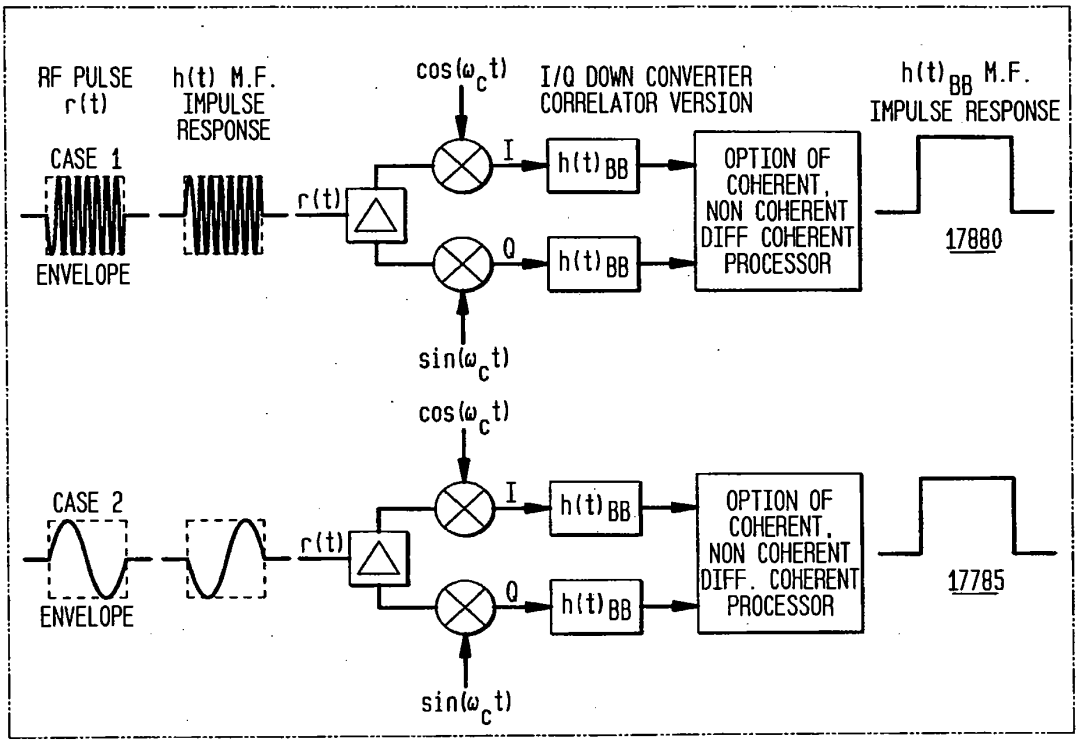


FIG. 177E

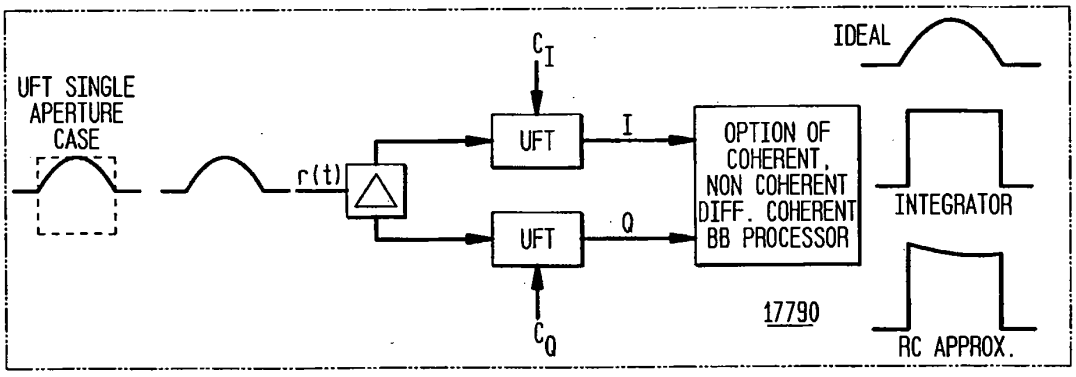
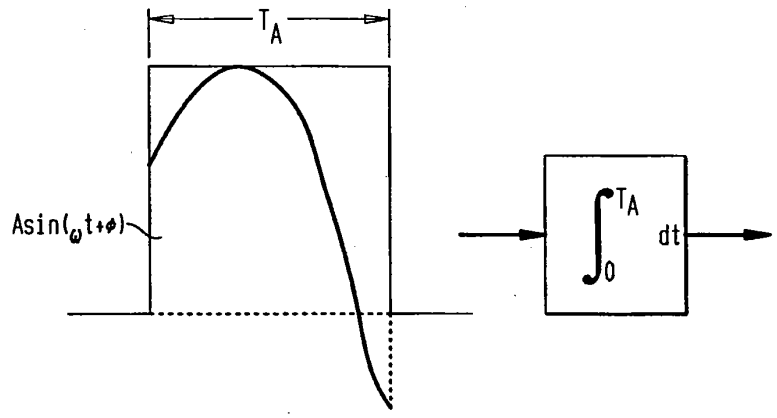


FIG. 177F



$$\int_0^{T_A} Au(t-T_A)\sin(\omega t+\phi)\,dt=\int_0^{T_A} A(u(t-T_A)\cos\phi\sin(\omega t)+u(t-T_A)\sin\phi\cos(\omega t))\,dt$$

$$=A\cos(\phi)\int_0^{T_A} u(t-T_A)\sin(\omega t)\,dt+A\sin(\phi)\int_0^{T_A} u(t-T_A)\cos(\omega t)\,dt$$

CONSTANT UFT CORRELATOR KERNEL — CONSTANT — =0

$$=A\cos(\phi)\int_0^{T_A} u(t-T_A)\sin(\omega t)\,dt$$

- A IS CONSTANT ON A SINE TO SINE BASIS
- ϕ IS CONSTANT ON A SINE TO SINE BASIS
- i.e., THE MODULATION RATE DUE TO INFORMATION FOR PHASE AND AMPLITUDE IS VERY SLOW COMPARED TO CARRIER FREQUENCY

FIG. 178A

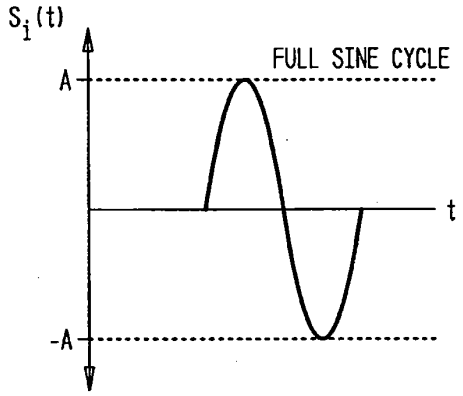


FIG. 178B

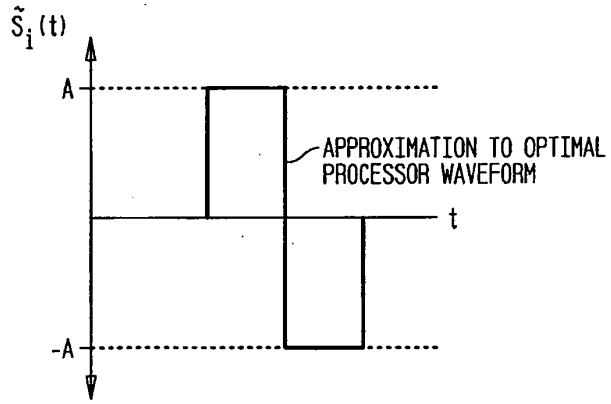


FIG. 179

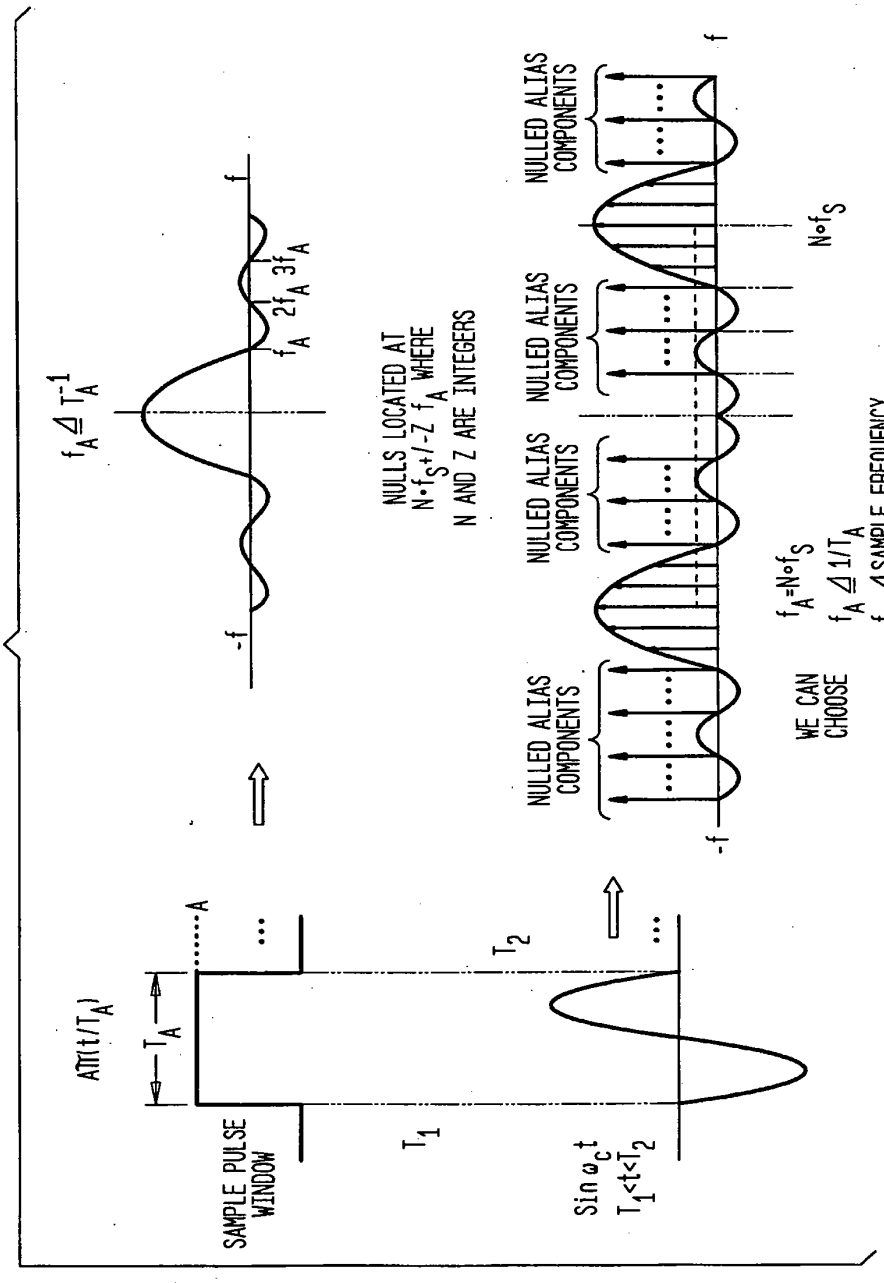

A Π(t/T_A)
T_A
A
SAMPLE PULSE WINDOW
T_1
T_2
Sin ω_c t
T_1<t<T_2
f_A ≜ T_A^-1
-f
f
f_A 2f_A 3f_A
NULLS LOCATED AT
N·f_S+/-Z f_A WHERE
N AND Z ARE INTEGERS
NULLED ALIAS COMPONENTS
NULLED ALIAS COMPONENTS
NULLED ALIAS COMPONENTS
NULLED ALIAS COMPONENTS
-f
f
N·f_S
WE CAN CHOOSE
f_A=N·f_S
f_A ≜ 1/T_A
f_S ≜ SAMPLE FREQUENCY

FIG. 180

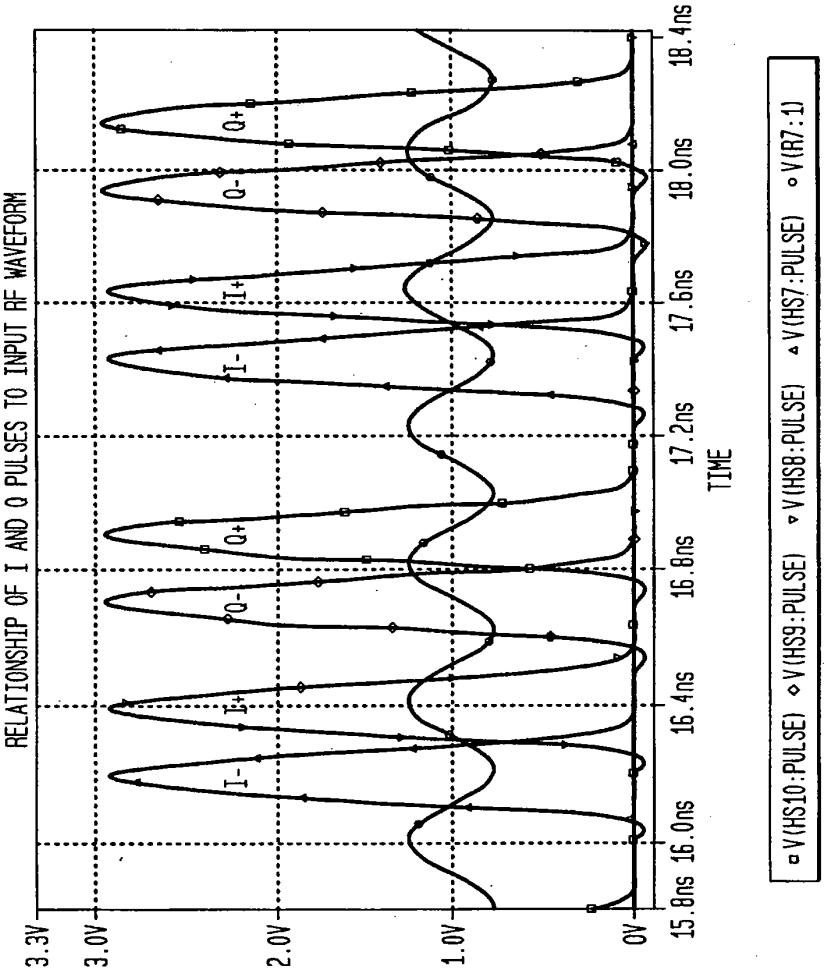

RELATIONSHIP OF I AND Q PULSES TO INPUT RF WAVEFORM
3.3V
3.0V
2.0V
1.0V
0V
15.8ns
16.0ns
16.4ns
16.8ns
17.2ns
17.6ns
18.0ns
18.4ns
TIME
I-
I+
Q-
Q+
V(HS10:PULSE)
V(HS9:PULSE)
V(HS8:PULSE)
V(HS7:PULSE)
V(R7:1)

FIG. 181

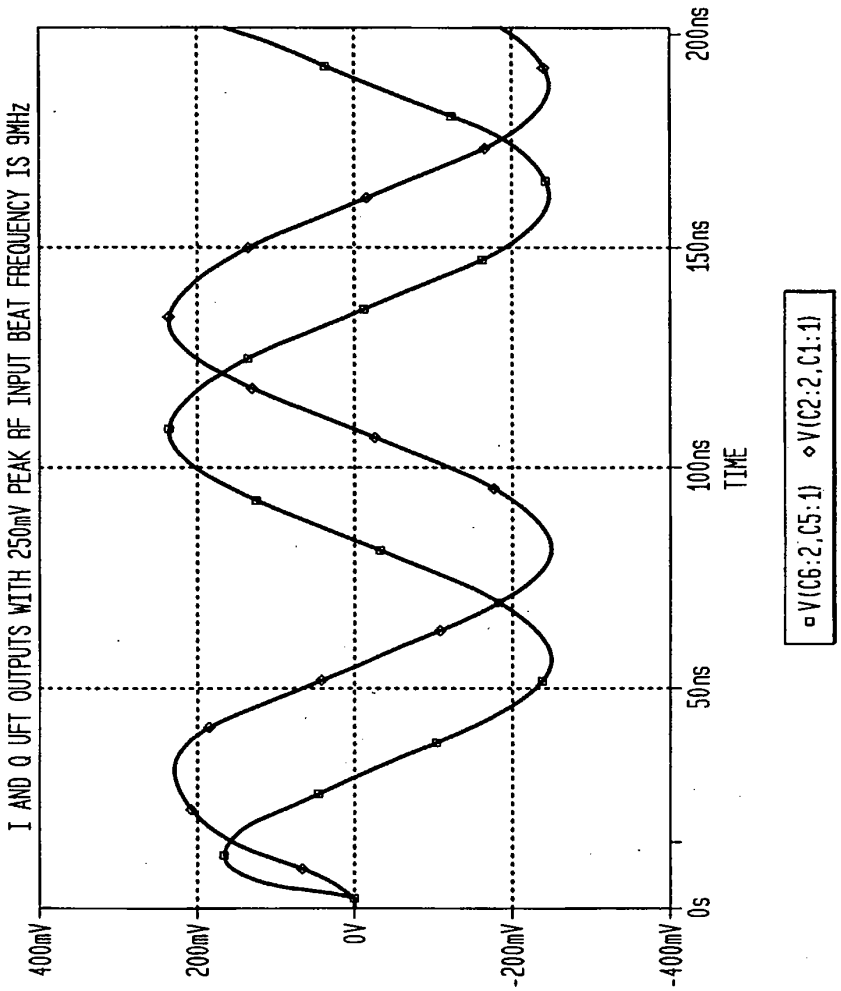

I AND Q UFT OUTPUTS WITH 250mV PEAK RF INPUT BEAT FREQUENCY IS 9MHz
400mV
200mV
0V
-200mV
-400mV
0s
50ns
100ns
150ns
200ns
TIME
V(C6:2,C5:1)
V(C2:2,C1:1)

FIG. 182

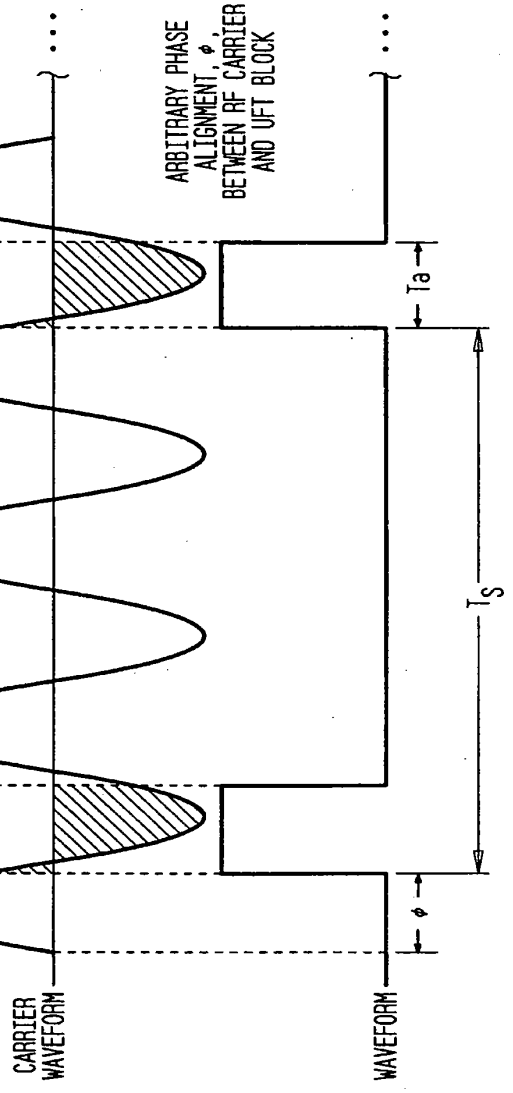

CARRIER WAVEFORM
WAVEFORM
ARBITRARY PHASE ALIGNMENT, ϕ, BETWEEN RF CARRIER AND UFT BLOCK
Ta
Ts
ϕ

FIG. 183

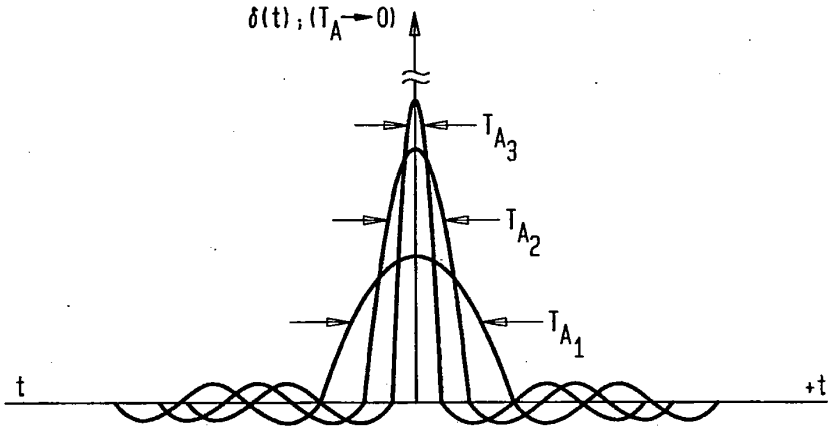


FIG. 184

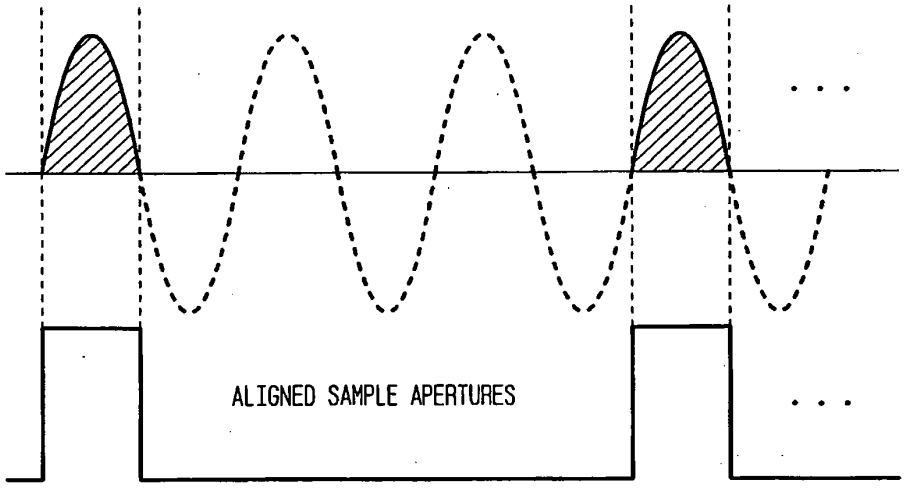


FIG. 185

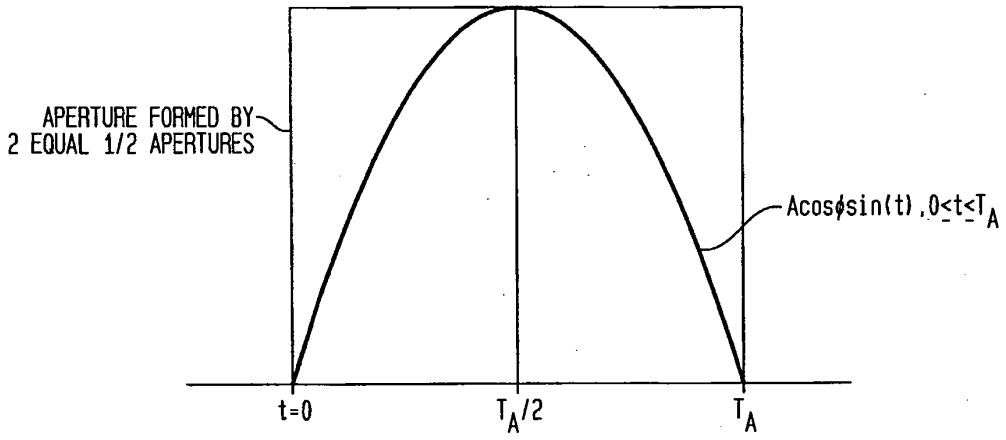


FIG. 186

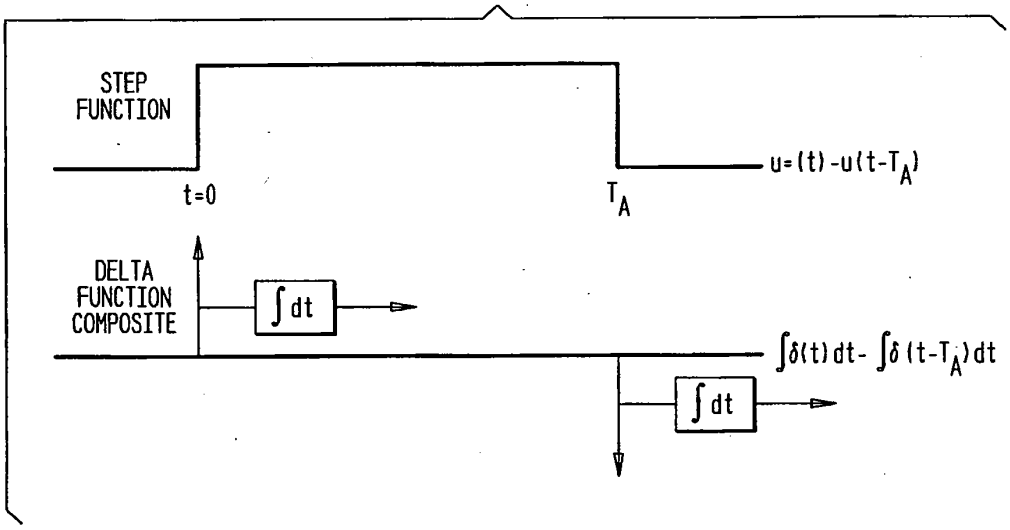


FIG. 187

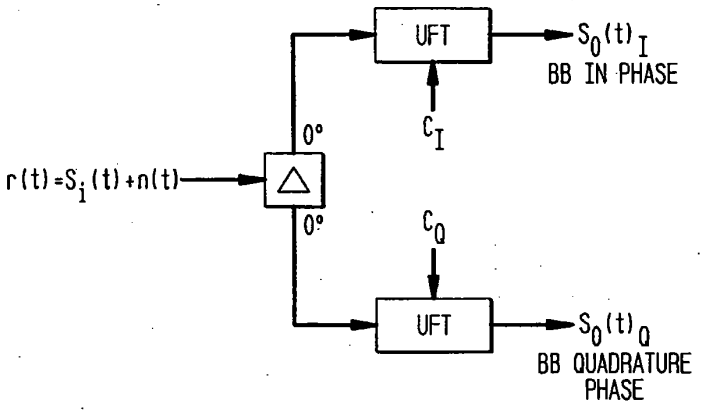


FIG. 188

$$C_I(t)=\sum_{m=-\infty}^{\infty}\delta(t-mT_S)*p_c(t)=\sum_{m=-\infty}^{\infty}p(t-mT_S) \qquad 18802$$

$$C_I(t)=\sum_{m=-\infty}^{\infty}(u(t)-u(t-T_A))*\delta(t-mT_S) \qquad 18804$$

$$C_Q(t)=\sum_{m=-\infty}^{\infty}(u[t-T_A/2]-u[t-3T_A/2])*\delta(t-(mT_S+T_A/2)) \qquad 18806$$

FIG. 189

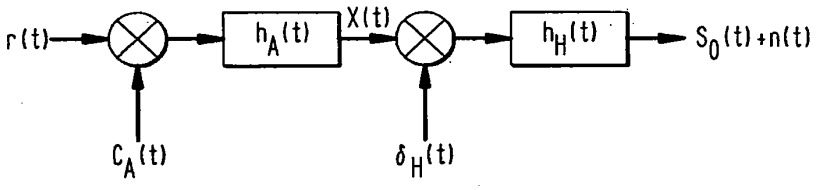


FIG. 190

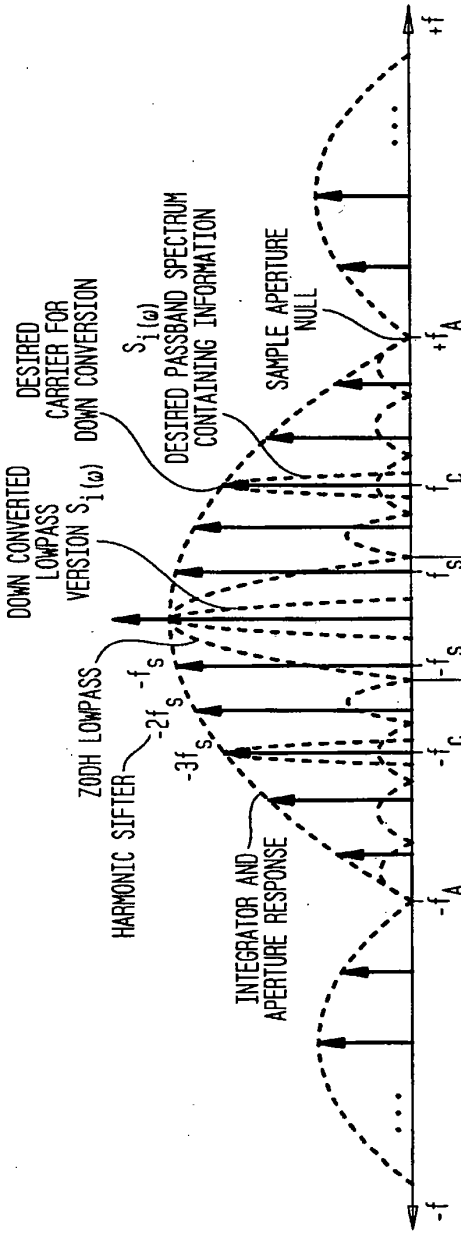

DESIRED CARRIER FOR DOWN CONVERSION
$S_{i(\omega)}$ DESIRED PASSBAND SPECTRUM CONTAINING INFORMATION
SAMPLE APERTURE NULL
DOWN CONVERTED LOWPASS VERSION $S_{i(\omega)}$
ZOH LOWPASS
HARMONIC SIFTER
INTEGRATOR AND APERTURE RESPONSE
$-2f_s$
$-3f_s$
$-f_s$
f_s
$-f_c$
f_c
$-f_A$
$+f_A$
$-(T_s-T_A)^{-1}$
$(T_s-T_A)^{-1}$
-f
+f

FIG. 191

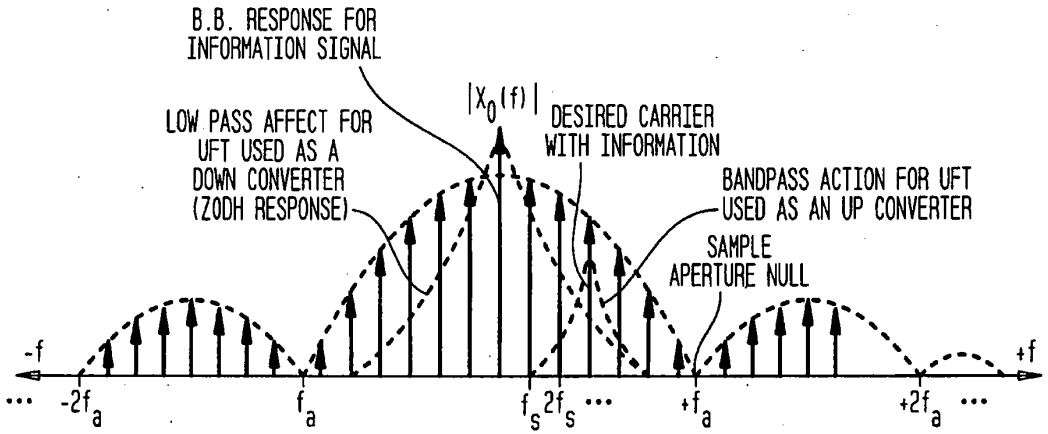


FIG. 192

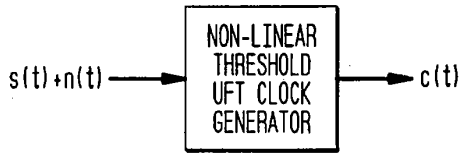


FIG. 193

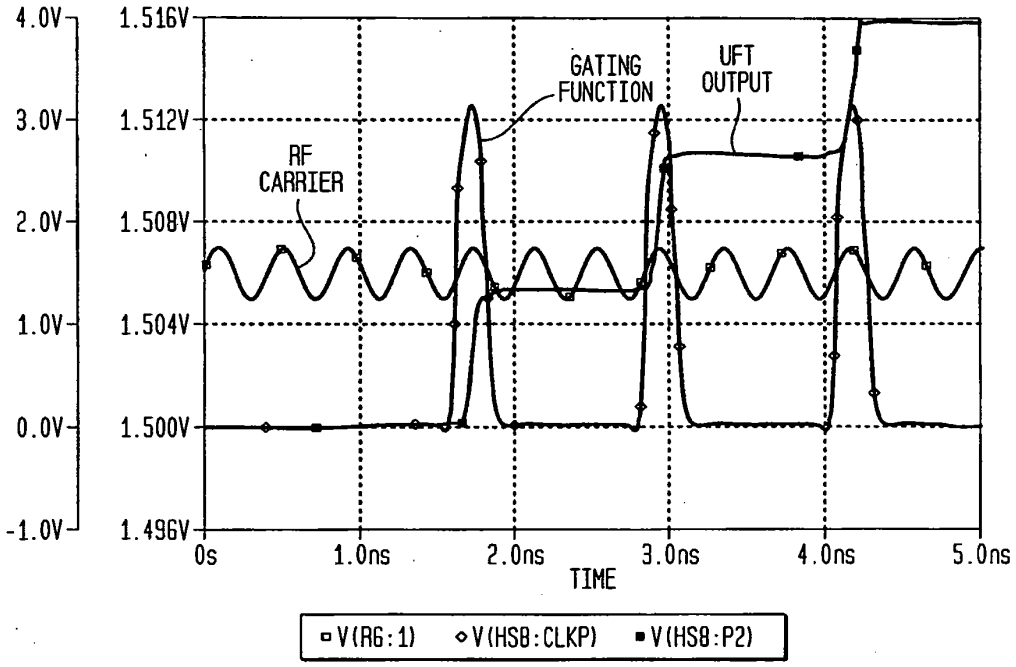

4.0V
3.0V
2.0V
1.0V
0.0V
-1.0V
1.516V
1.512V
1.508V
1.504V
1.500V
1.496V
RF CARRIER
GATING FUNCTION
UFT OUTPUT
0s
1.0ns
2.0ns
3.0ns
4.0ns
5.0ns
TIME
V(R6:1)
V(HS8:CLKP)
V(HS8:P2)

FIG. 194

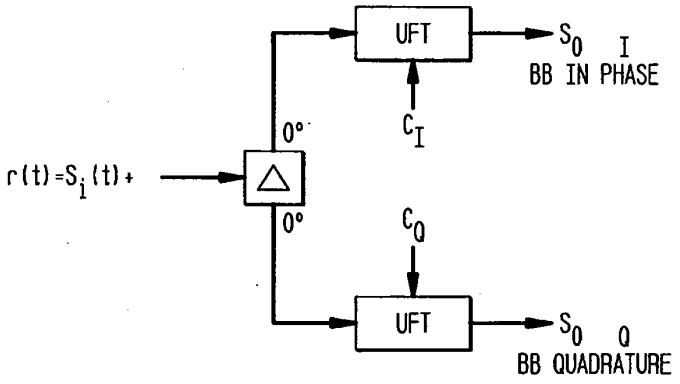


FIG. 195

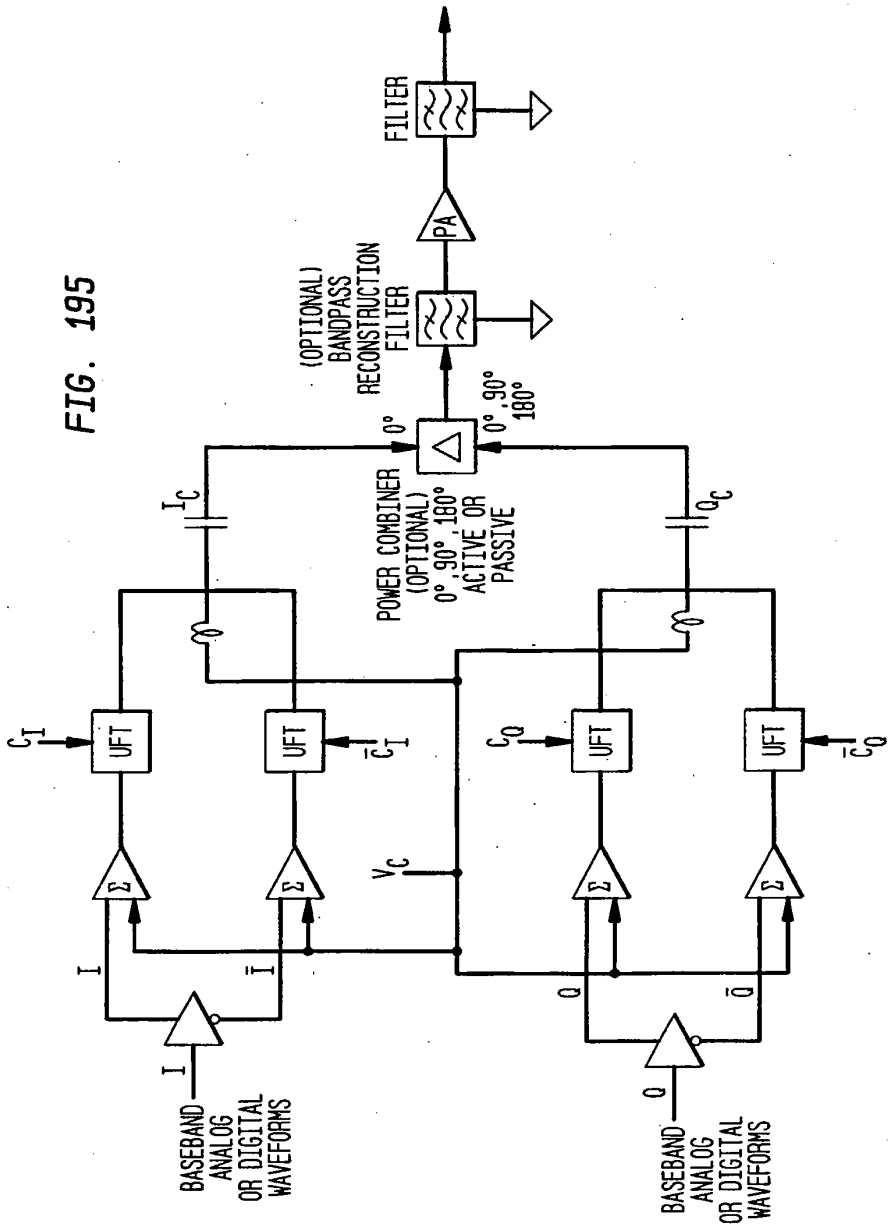

BASEBAND ANALOG OR DIGITAL WAVEFORMS
I
Ī
Q
Q̄
UFT
Σ
C_I
$\bar{C}_I$
C_Q
$\bar{C}_Q$
V_C
I_C
Q_C
POWER COMBINER (OPTIONAL) 0°,90°,180° ACTIVE OR PASSIVE
0°
0°,90° 180°
(OPTIONAL) BANDPASS RECONSTRUCTION FILTER
PA
FILTER

FIG. 196

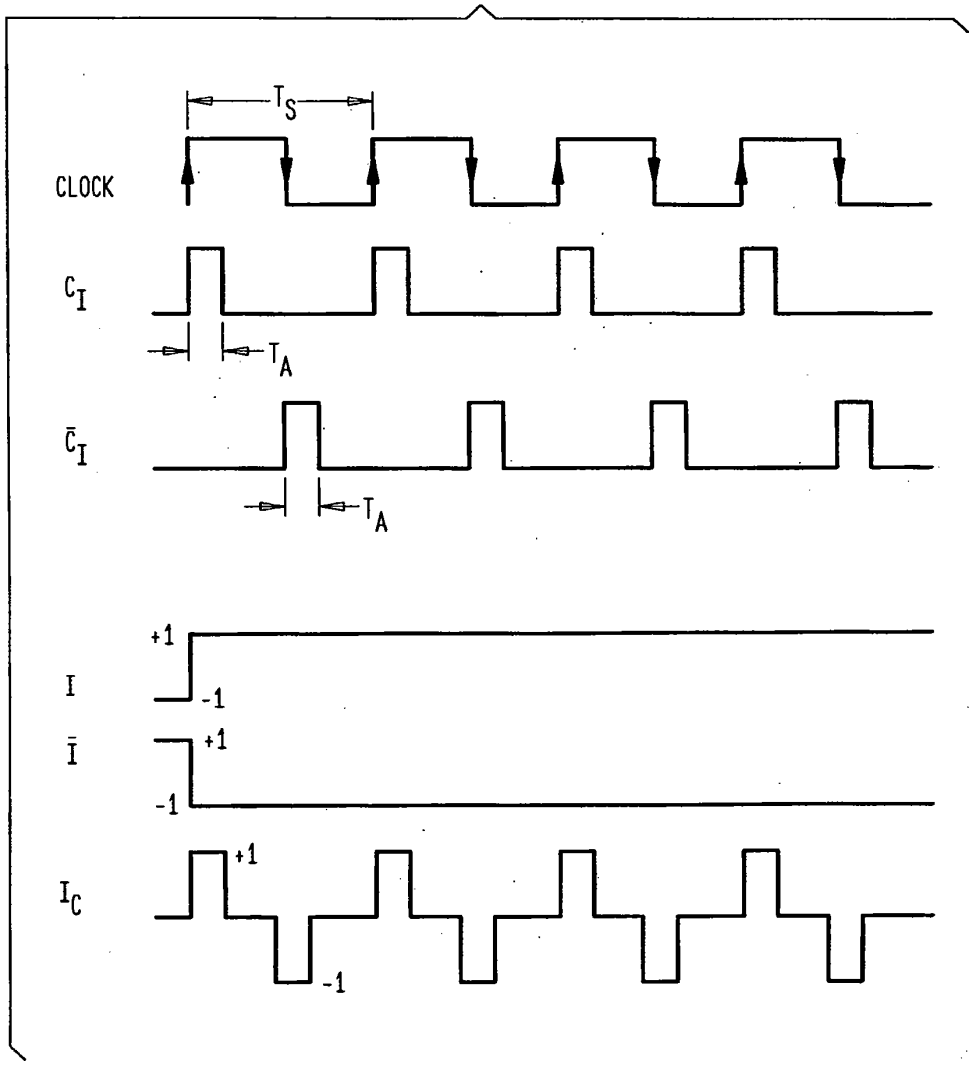


FIG. 197

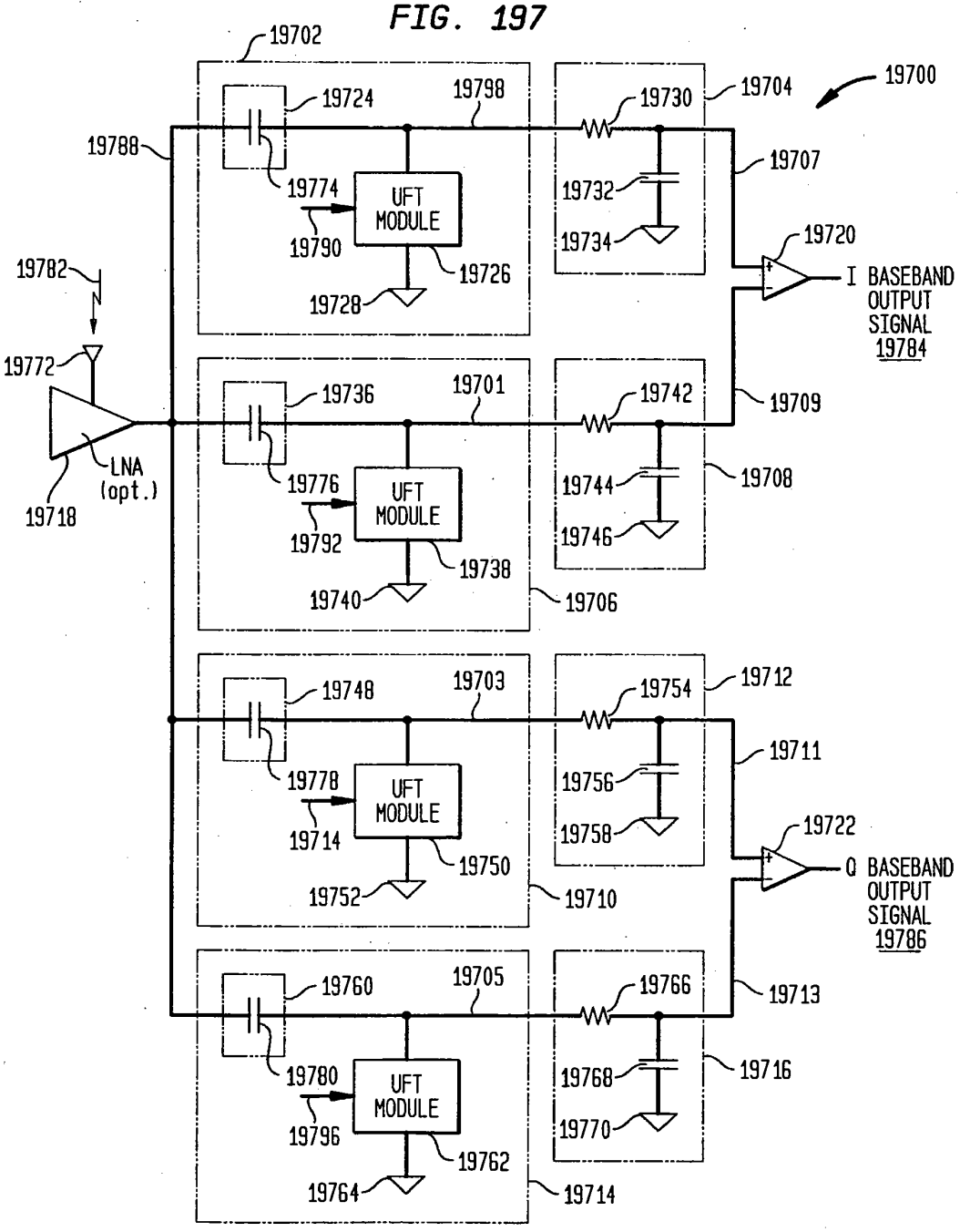

19702
19724
19798
19730
19704
19700
19788
19707
19774
UFT MODULE
19732
19720
19790
19726
19734
I BASEBAND OUTPUT SIGNAL 19784
19728
19782
19772
19736
19701
19742
19709
19776
UFT MODULE
19744
19708
LNA (opt.)
19718
19792
19738
19746
19740
19706
19748
19703
19754
19712
19778
UFT MODULE
19756
19711
19722
19714
19750
19758
Q BASEBAND OUTPUT SIGNAL 19786
19752
19710
19760
19705
19766
19713
19780
UFT MODULE
19768
19716
19796
19762
19770
19764
19714

FIG. 198

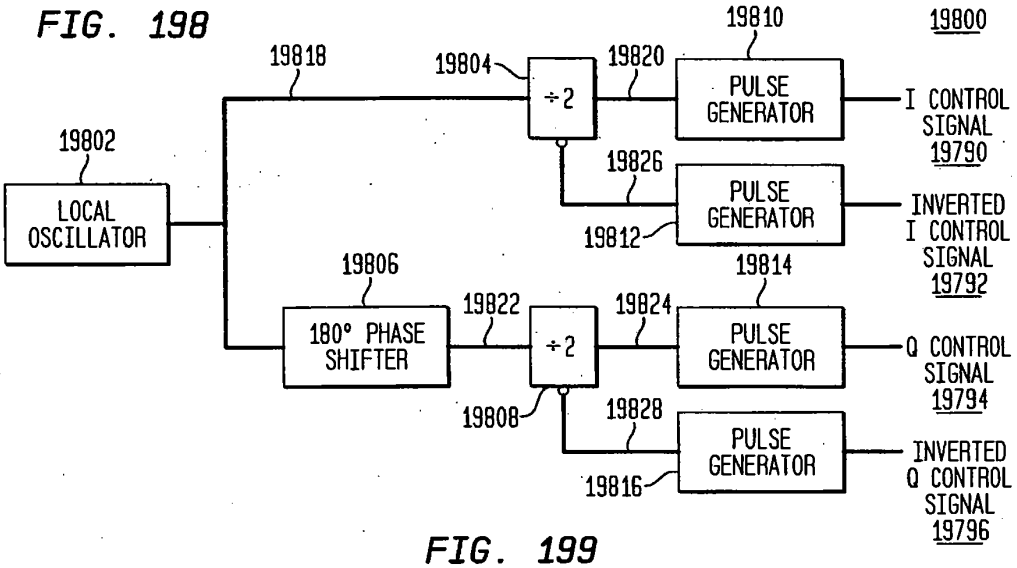


FIG. 199

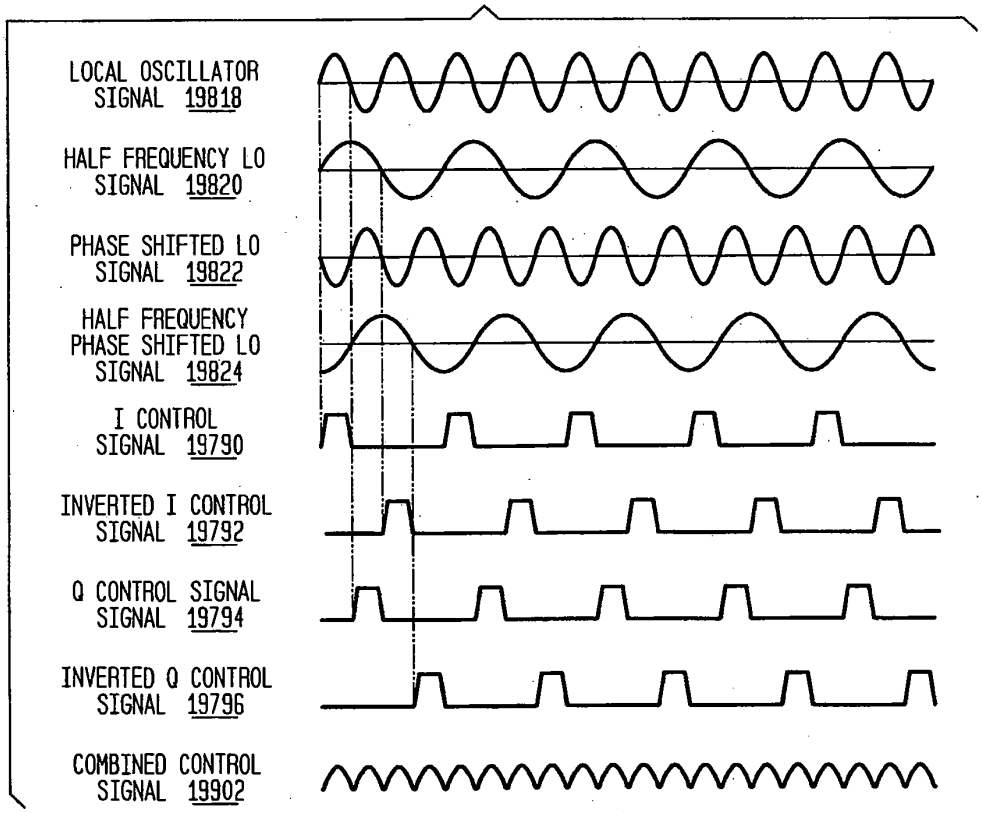


FIG. 200

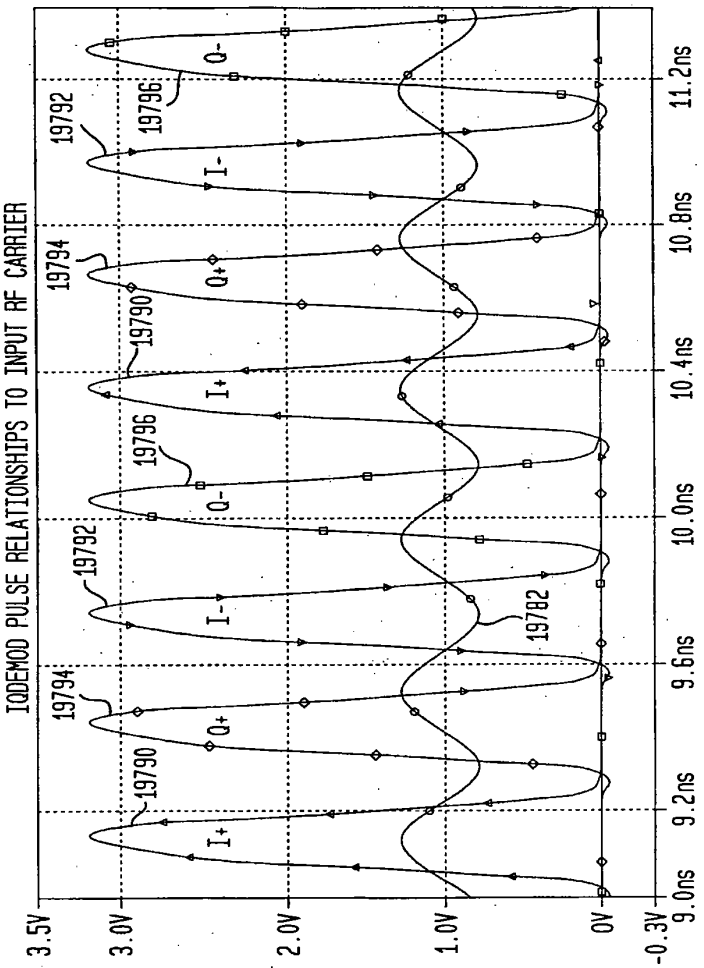

IQDEMOD PULSE RELATIONSHIPS TO INPUT RF CARRIER
3.5V
3.0V
2.0V
1.0V
0V
-0.3V
9.0ns
9.2ns
9.6ns
10.0ns
10.4ns
10.8ns
11.2ns
I+
Q+
I-
Q-
19790
19794
19792
19796
19782

FIG. 201

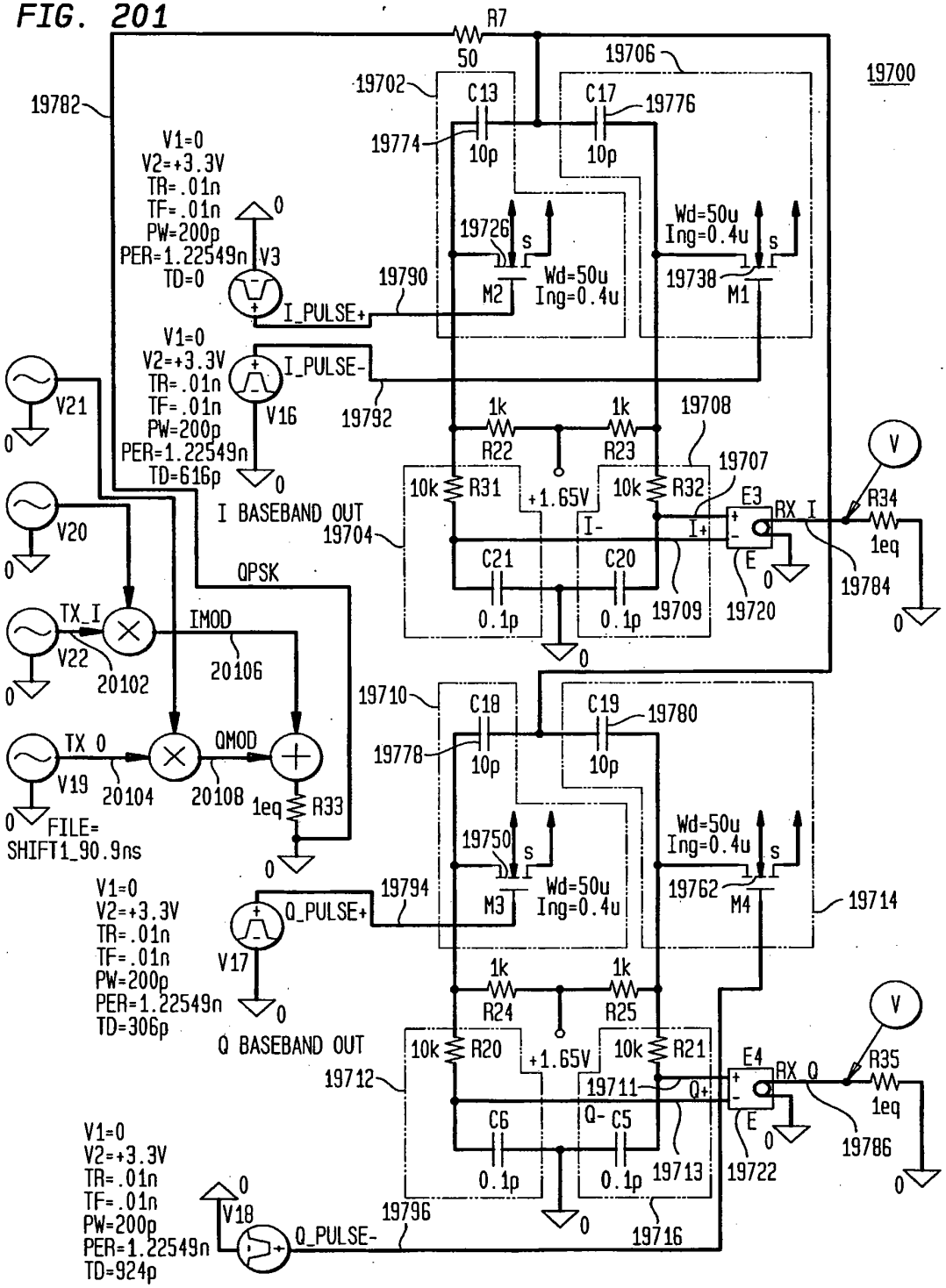

R7
50
19706
19700
19702
C13
C17
19776
19782
19774
10p
10p
V1=0
V2=+3.3V
TR=.01n
TF=.01n
PW=200p
PER=1.22549n
TD=0
V3
0
19726
s
Wd=50u
Ing=0.4u
s
19790
M2
Wd=50u
Ing=0.4u
19738
M1
I_PULSE+
V1=0
V2=+3.3V
TR=.01n
TF=.01n
PW=200p
PER=1.22549n
TD=616p
I_PULSE-
V16
19792
V21
1k
1k
19708
R22
R23
19707
10k R31
+1.65V
10k R32
E3
RX I
R34
V
V20
I-
I+
1eq
I BASEBAND OUT
19704
C21
C20
E
19784
QPSK
0.1p
0.1p
19709
19720
TX_I
IMOD
V22
20102
20106
19710
C18
C19
19780
19778
10p
10p
TX Q
QMOD
V19
20104
20108
1eq
R33
FILE=
SHIFT1_90.9ns
19750
s
Wd=50u
Ing=0.4u
s
19794
M3
Wd=50u
Ing=0.4u
19762
M4
19714
Q_PULSE+
V17
V1=0
V2=+3.3V
TR=.01n
TF=.01n
PW=200p
PER=1.22549n
TD=306p
1k
1k
R24
R25
Q BASEBAND OUT
10k R20
+1.65V
10k R21
E4
RX Q
R35
19712
19711
Q+
1eq
C6
Q- C5
E
19786
0.1p
0.1p
19713
19722
V1=0
V2=+3.3V
TR=.01n
TF=.01n
PW=200p
PER=1.22549n
TD=924p
V18
19796
Q_PULSE-
19716

FIG. 202

IQDEMOD SHOWING TIME RELATIONSHIP OF TX_I DATA

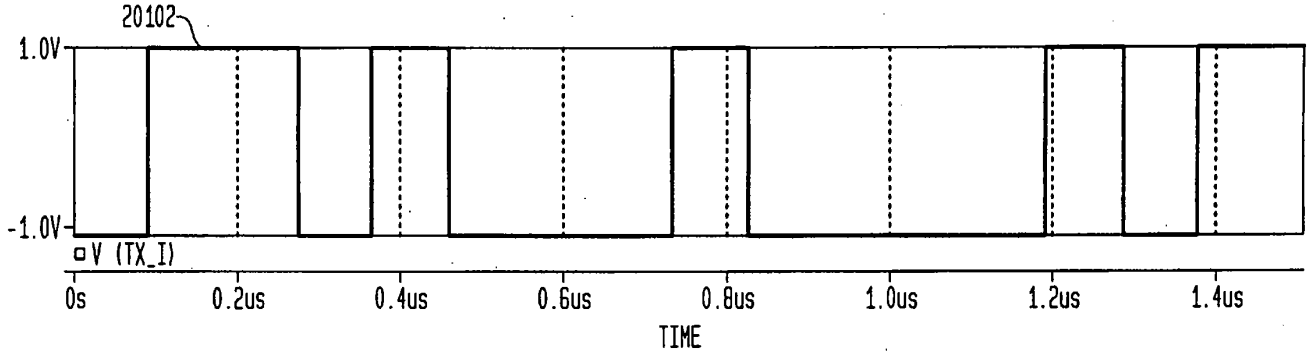


FIG. 203

IQDEMOD SHOWING TIME RELATIONSHIP OF TX_Q DATA

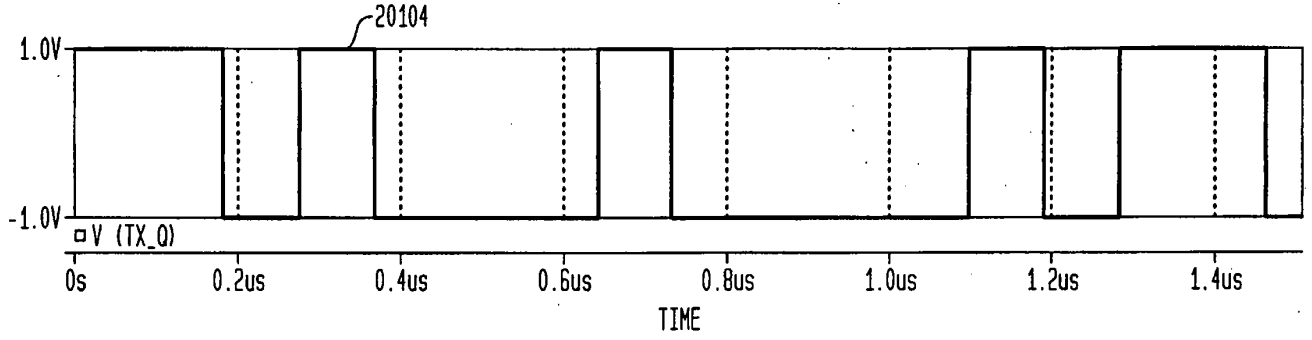


FIG. 204

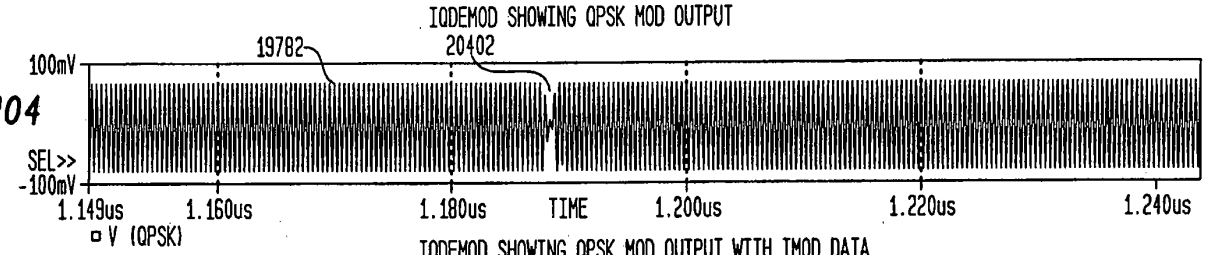


FIG. 205

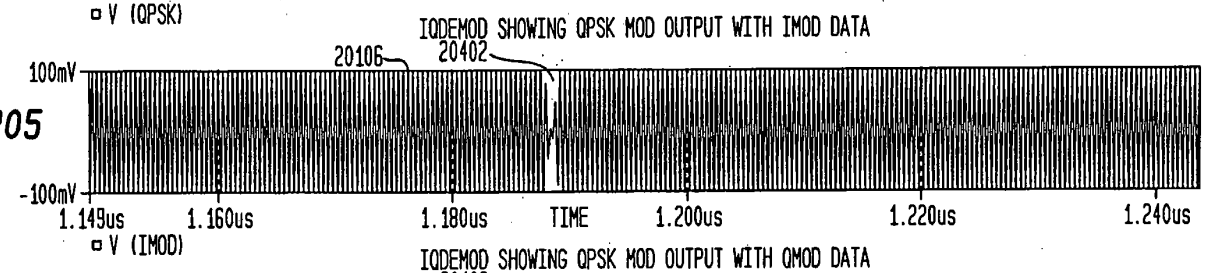


FIG. 206

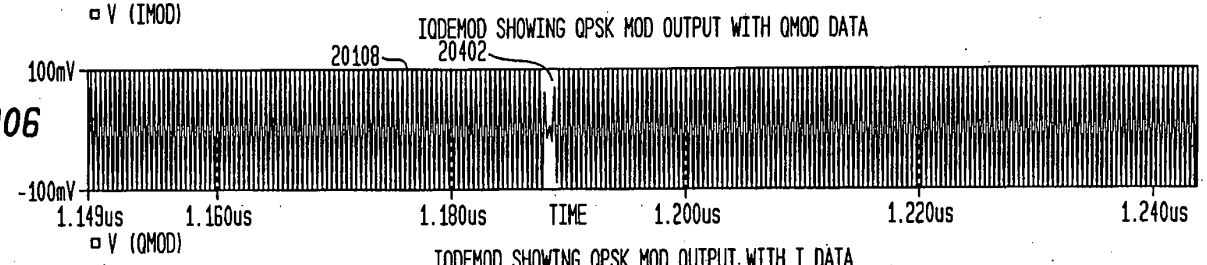


FIG. 207

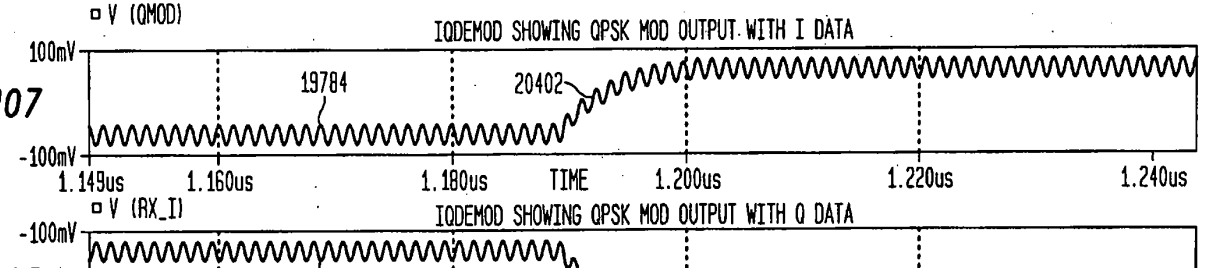


FIG. 208

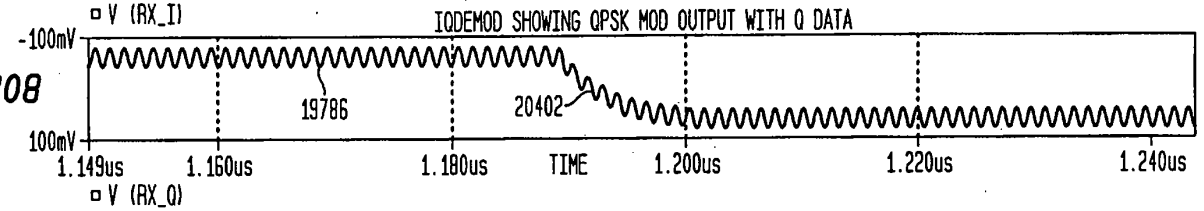


FIG. 209

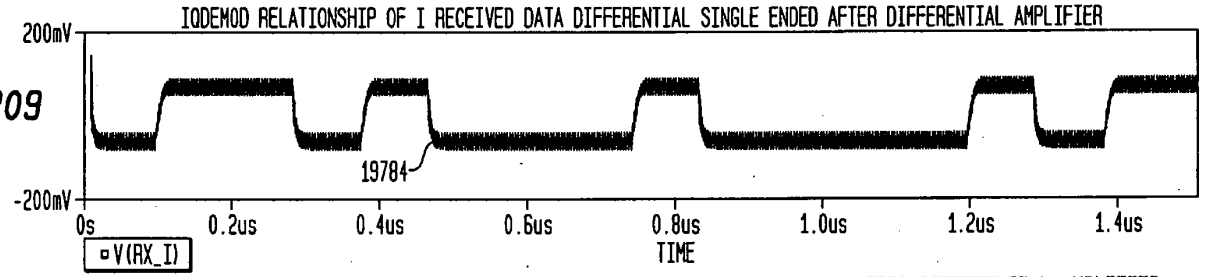
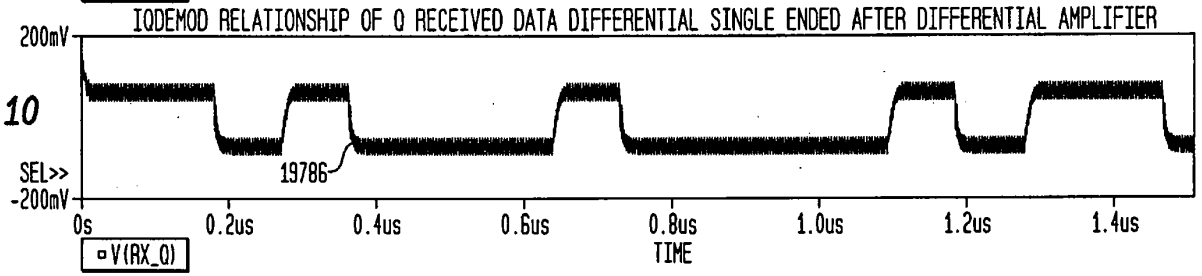


FIG. 210



GE

FIG. 211

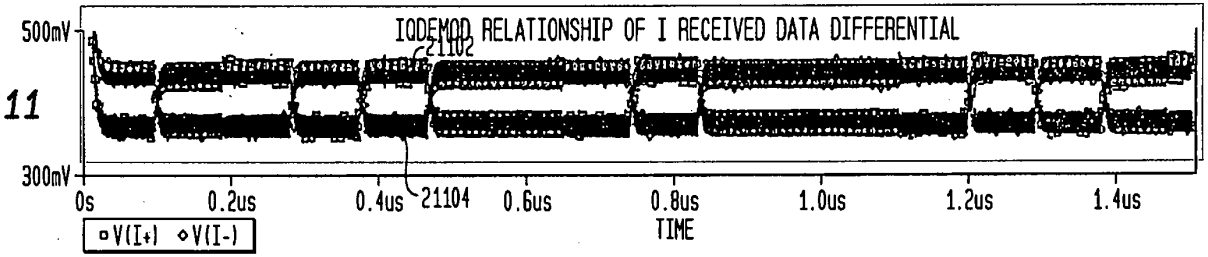


FIG. 212

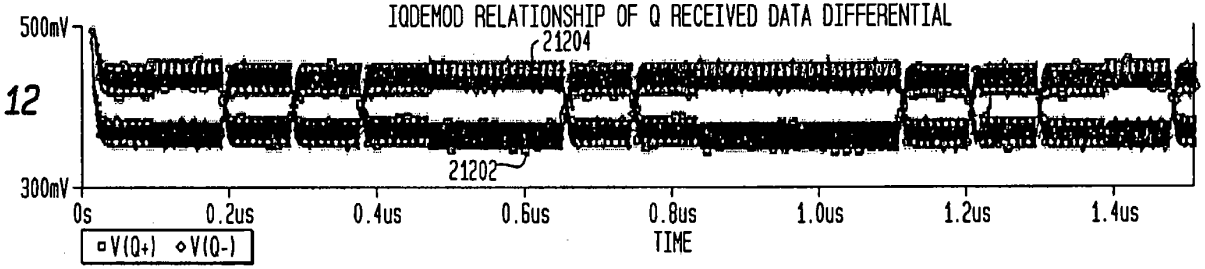
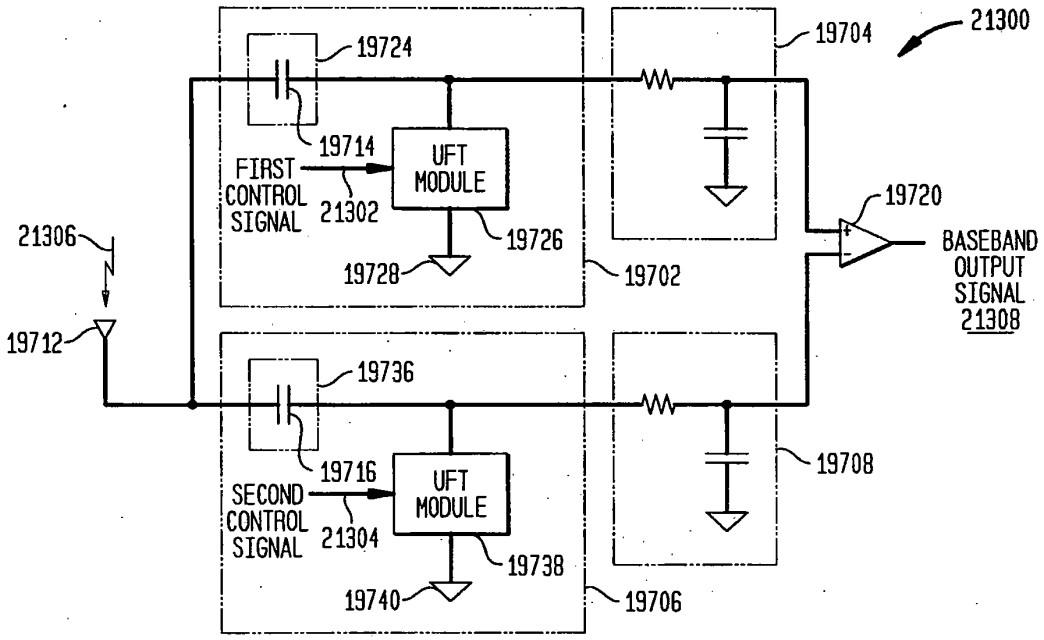


FIG. 213


21300
19704
19724
19714
FIRST CONTROL SIGNAL
21302
UFT MODULE
19726
19728
19702
19720
BASEBAND OUTPUT SIGNAL 21308
21306
19712
19736
19716
SECOND CONTROL SIGNAL
21304
UFT MODULE
19738
19740
19706
19708

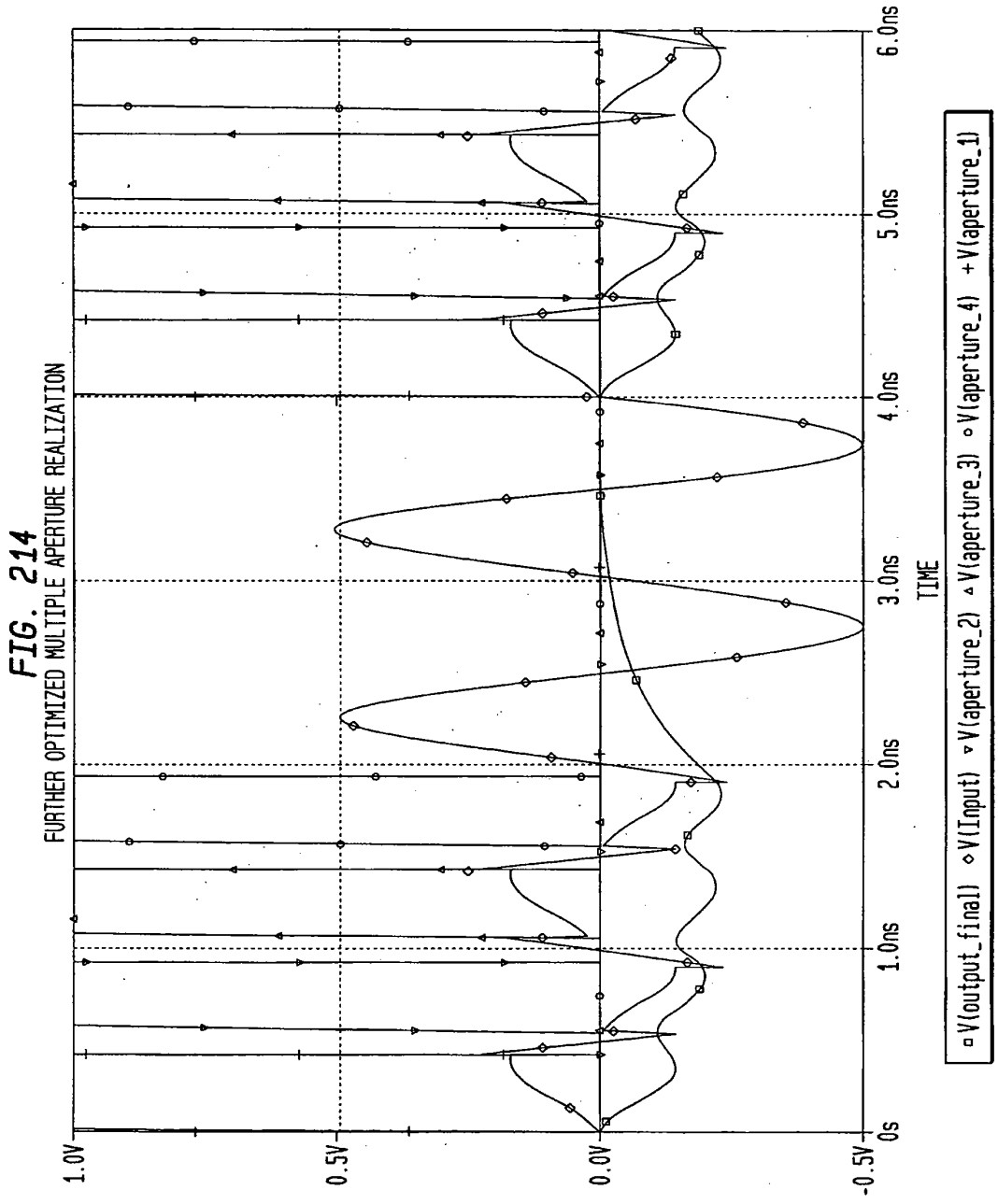

FIG. 214
FURTHER OPTIMIZED MULTIPLE APERTURE REALIZATION
1.0V
0.5V
0.0V
-0.5V
0s
1.0ns
2.0ns
3.0ns
4.0ns
5.0ns
6.0ns
TIME
V(output_final)
V(Input)
V(aperture_2)
V(aperture_3)
V(aperture_4)
V(aperture_1)

FIG. 215

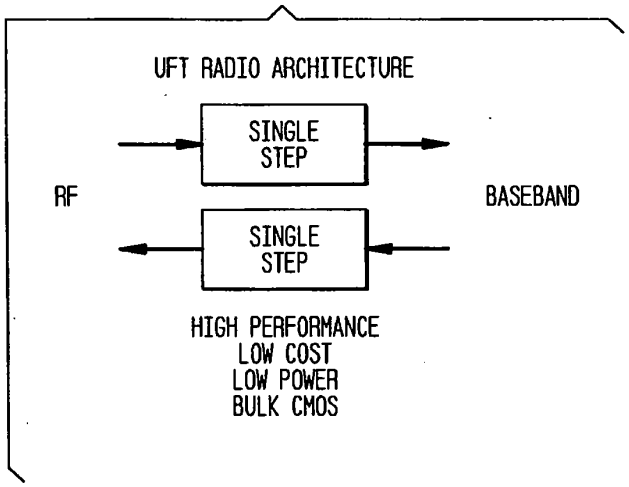


FIG. 216

WIRELESS TRADE-OFF DESIGN CONCERNS

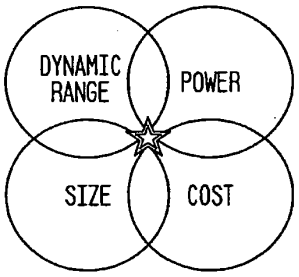


FIG. 217

NOISE FIGURE CALCULATIONS BASED ON RMS
VOLTAGE AND CURRENT NOISE SPECIFICATIONS

ENTER, THE VOLTAGE NOISE DENSITY, e_n, AND THE
CURRENT NOISE DENSITY, i_n, FOR THE AMPLIFIER CHOSEN:

$e_n := 6 \cdot 10^{-9}$ V/sqrt(Hz)
$i_n := 1 \cdot 10^{-12}$ A/sqrt(Hz)

ENTER THE SOURCE RESISTANCE DRIVING THE AMPLIFIER:

$K := 1.38 \cdot 10^{-23}$ J/K $T := 290K$

$PARALELL(x,y) := \frac{x \cdot y}{x+y}$ $NF(R_S) := 20 \cdot \log\left(\sqrt{\frac{e_n^2 + 4 \cdot K \cdot T \cdot R_S + i_n^2 \cdot R_S^2}{4 \cdot K \cdot T \cdot R_S}}\right)$

IF WE PLOT NOISE FIGURE VERSUS SOURCE RESISTANCE WE CAN GET
AN IDEA OF WHAT IS THE OPTIMUM SOURCE RESISTANCE.
IT IS NOT NECESSARILY THE LOWEST RESISTANCE!

$R_S := 100, 200 \ldots 100 \cdot 10^3$

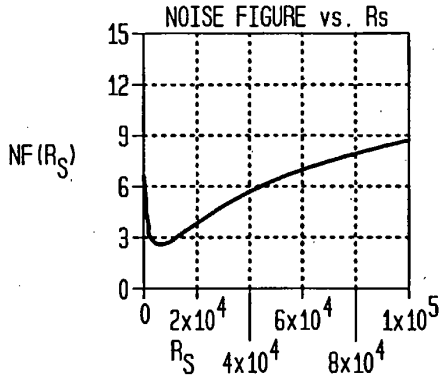


FIG. 218A

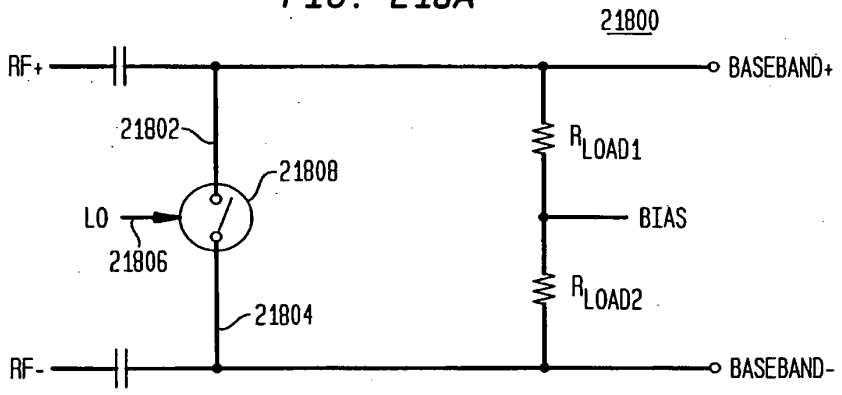


FIG. 218B

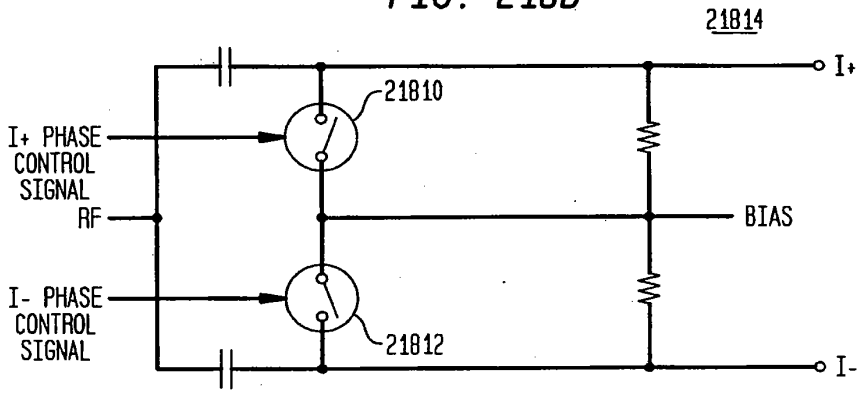


FIG. 218C

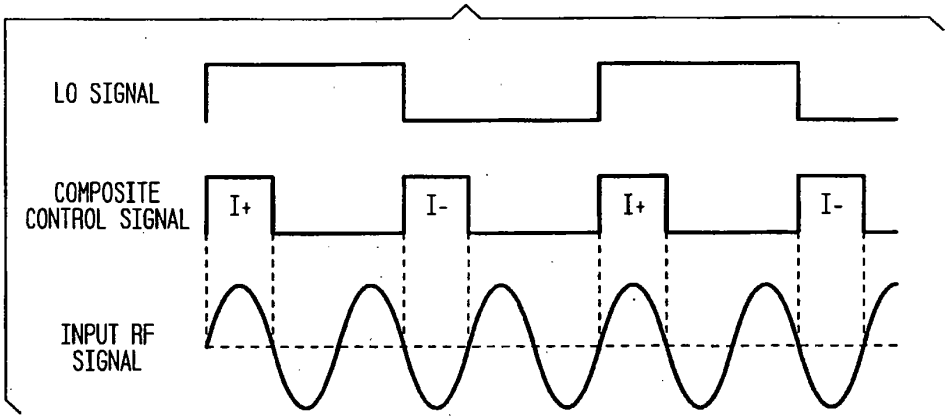


FIG. 218D

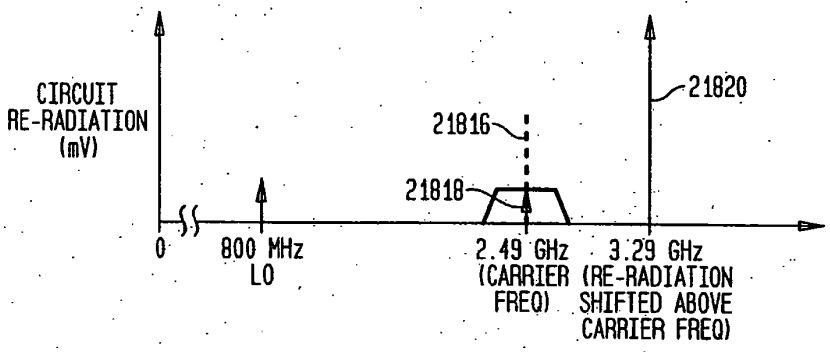


FIG. 218F

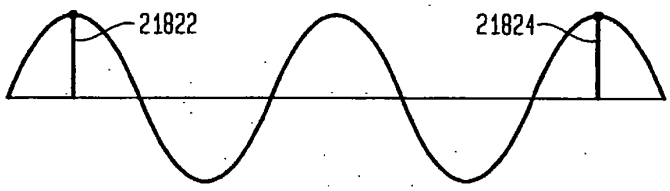


FIG. 218G

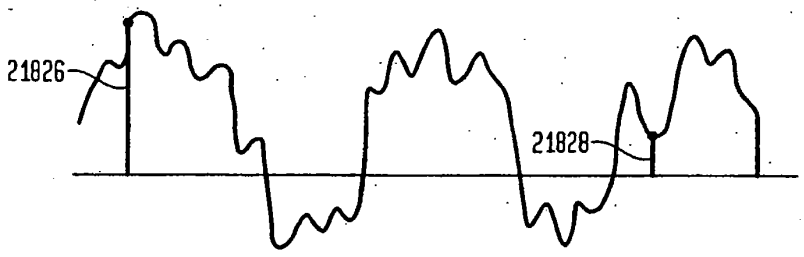


FIG. 218E

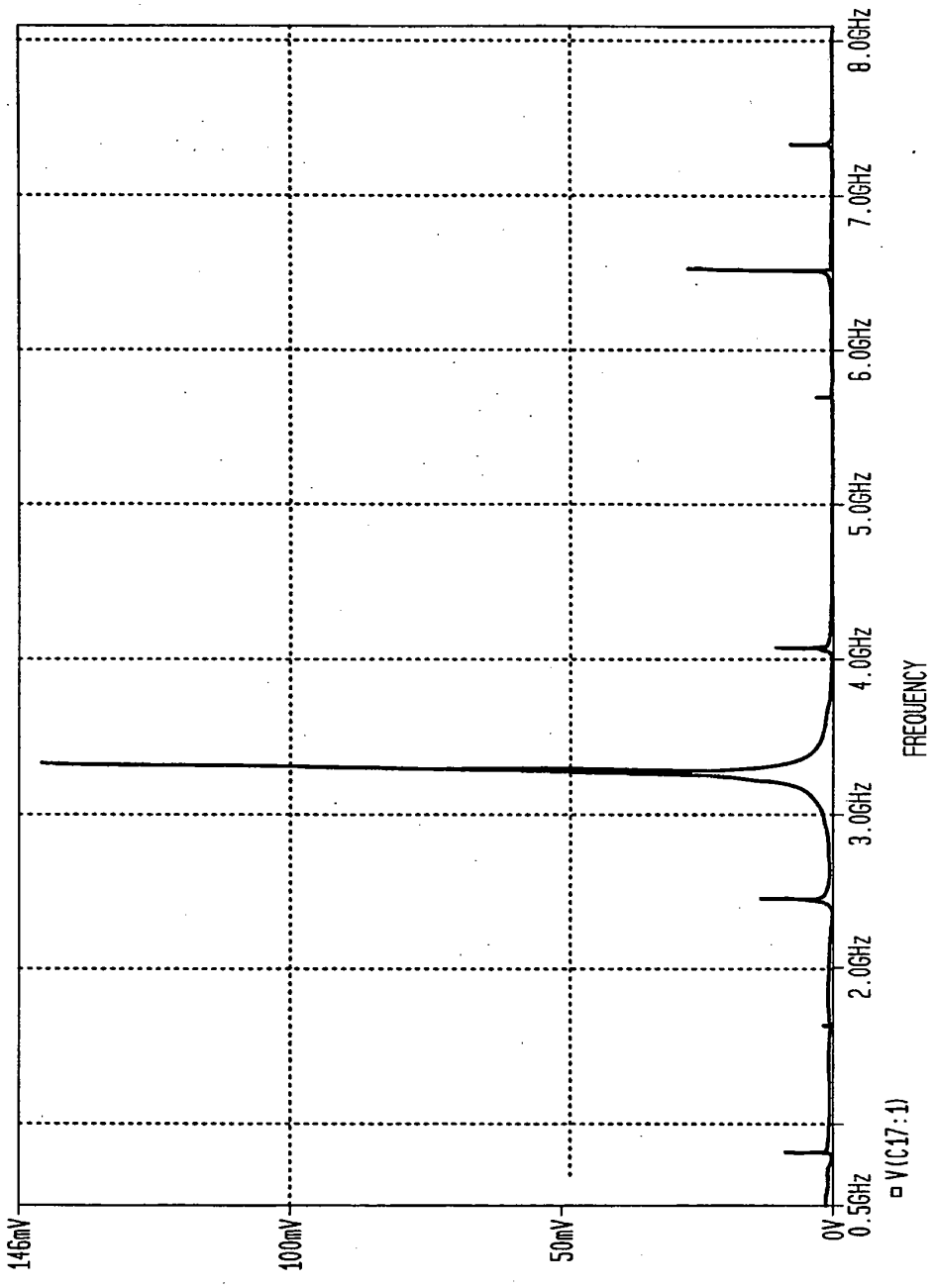

146mV
100mV
50mV
0V
0.5GHz
2.0GHz
3.0GHz
4.0GHz
5.0GHz
6.0GHz
7.0GHz
8.0GHz
FREQUENCY
V(C17:1)

FIG. 219

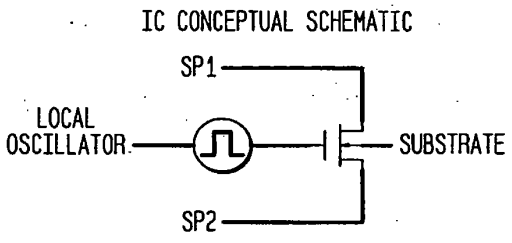
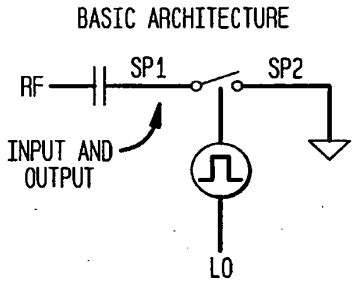


FIG. 220



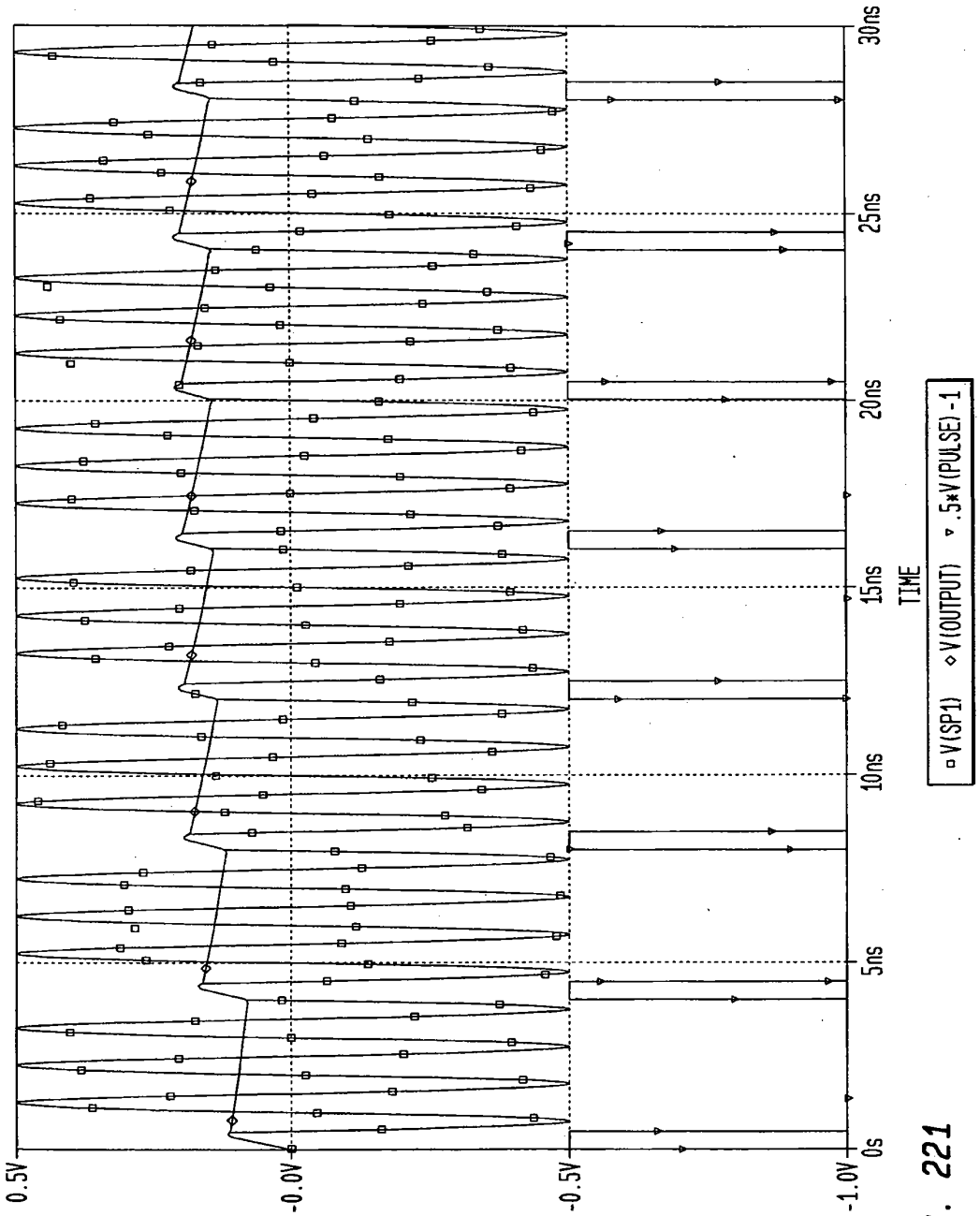

0.5V
-0.0V
-0.5V
-1.0V
0s
5ns
10ns
15ns
20ns
25ns
30ns
TIME
V(SP1)
V(OUTPUT)
.5*V(PULSE)-1

FIG. 221

FIG. 222

DC EQUATIONS

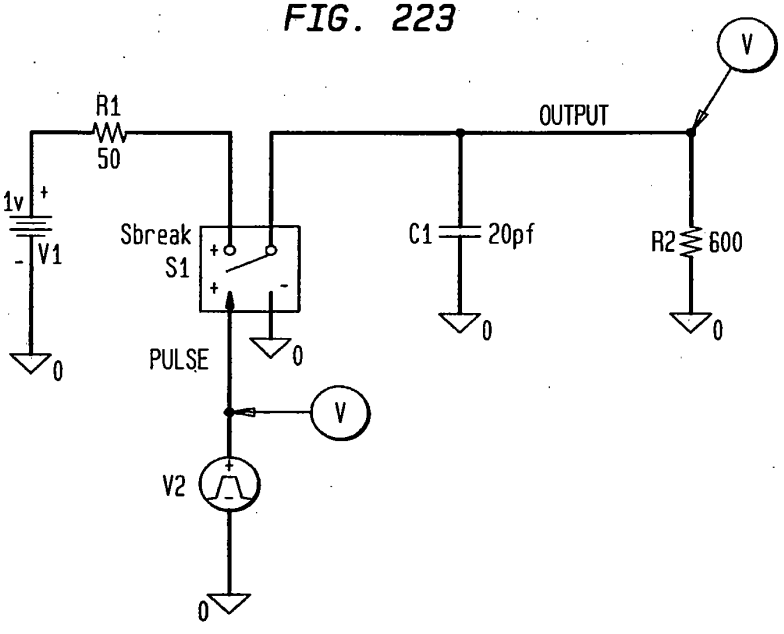
$$Vin = V \cdot \frac{Rout}{Rin + Rout}$$

$$Vc = Vin - (Vin - Vinit) \cdot \exp\left(\frac{-tc}{Rin \cdot C}\right)$$

$$Vd = Vc \cdot \exp\left(\frac{-td}{Rout \cdot C}\right)$$

DEFINITIONS:
- Rin - INPUT RESISTANCE
- Rout - OUTPUT RESISTANCE
- C - CAPACITOR
- tc - CHARGE TIME OR APERATURE
- td - DISCHARGE TIME OR LO PERIOD-tc
- V - INPUT VOLTAGE
- Vinit - INITIAL CAPACITOR VOLTAGE
- Vc - FINAL CHARGE CAPACITOR VOLTAGE
- Vd - FINAL DISCHARGE CAPACITOR VOLTAGE

FIG. 223



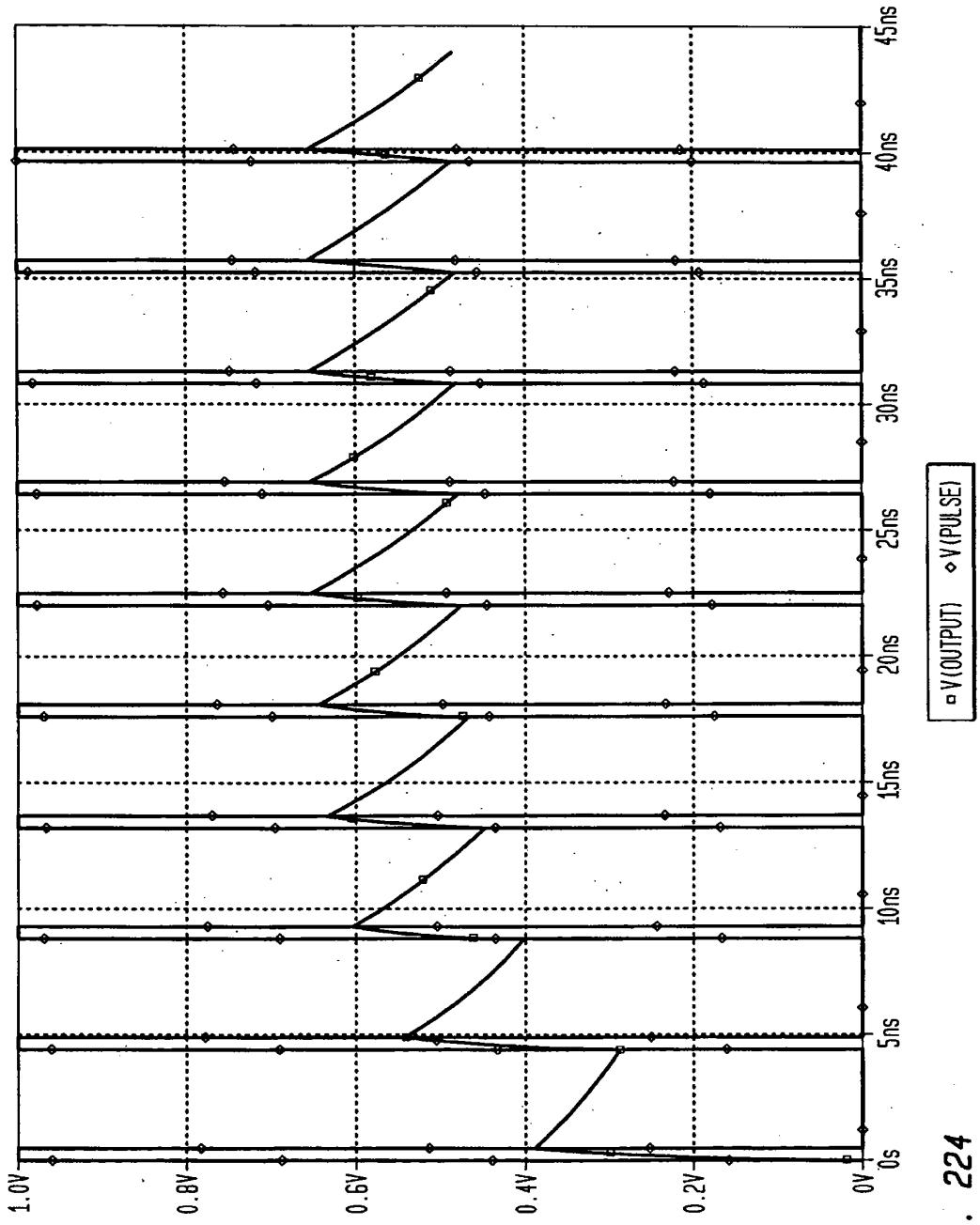
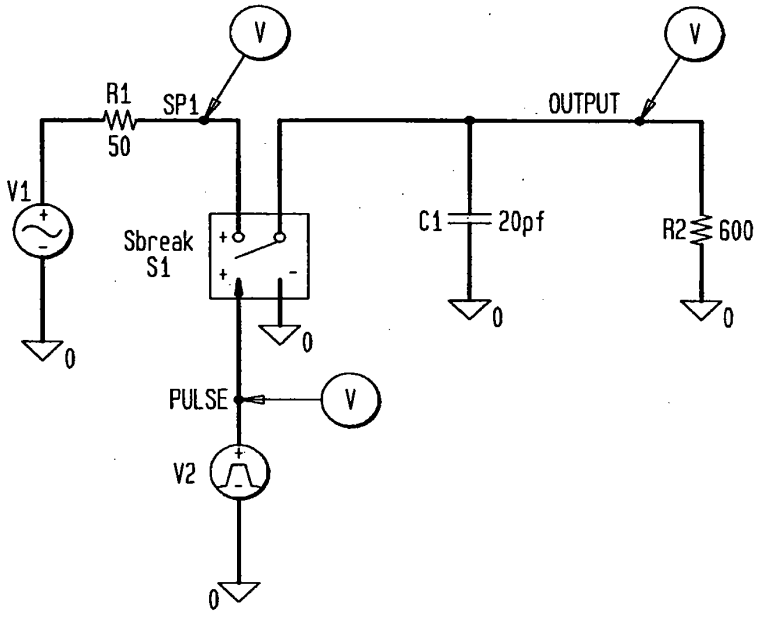

1.0V
0.8V
0.6V
0.4V
0.2V
0V
0s
5ns
10ns
15ns
20ns
25ns
30ns
35ns
40ns
45ns
V(OUTPUT)
V(PULSE)

FIG. 224

FIG. 225



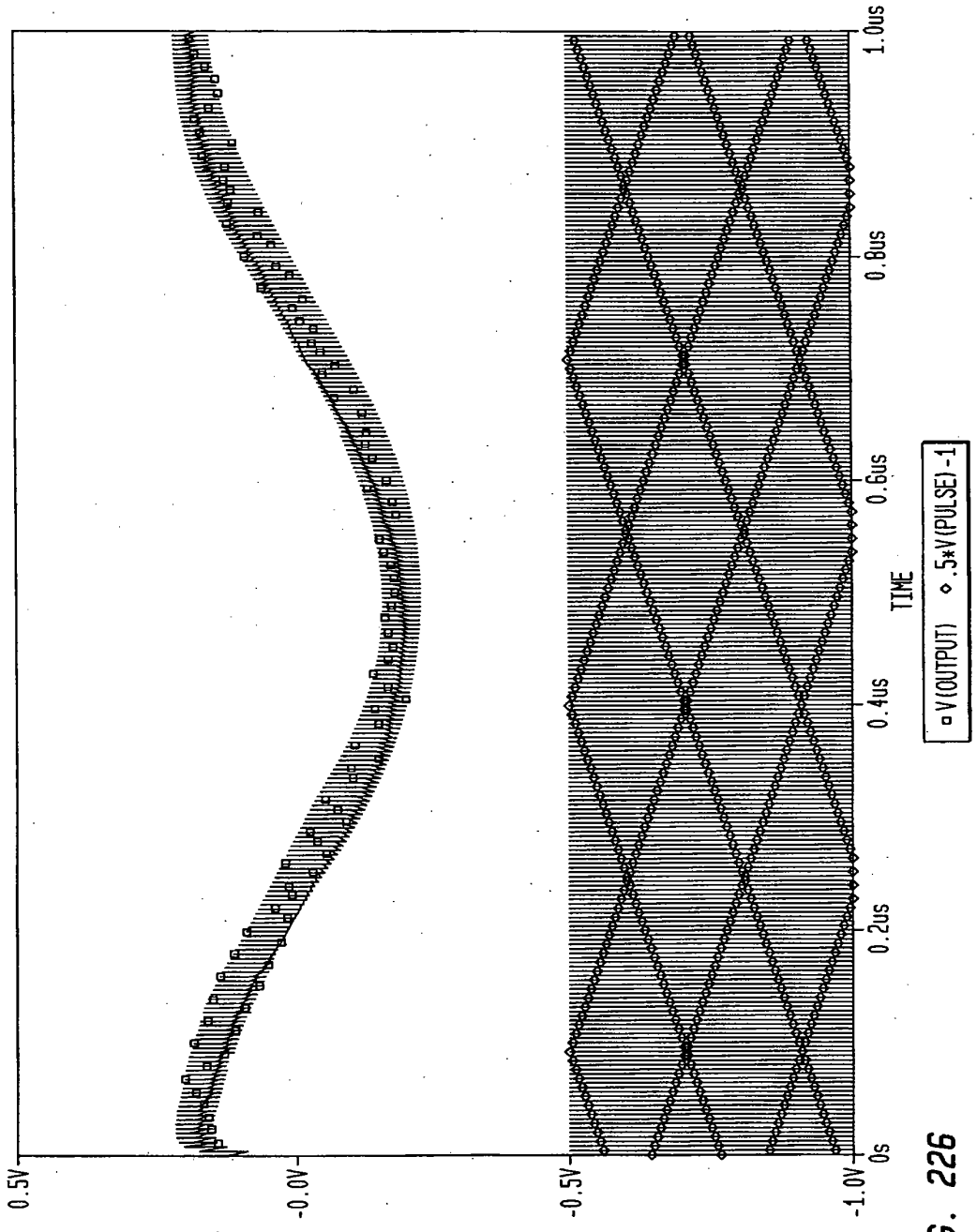

0.5V
-0.0V
-0.5V
-1.0V
0s
0.2us
0.4us
0.6us
0.8us
1.0us
TIME
V(OUTPUT)
.5*V(PULSE)-1

FIG. 226

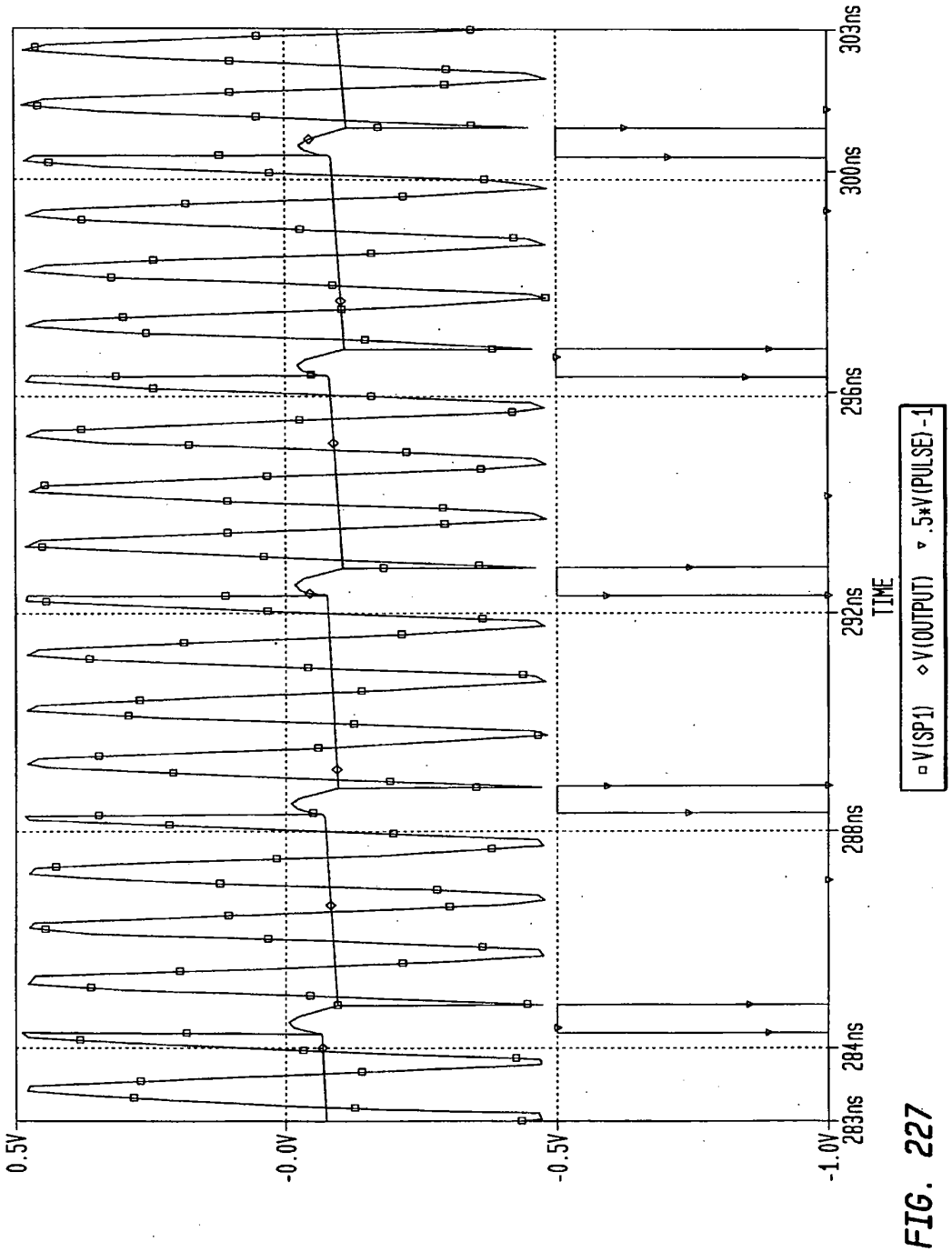

0.5V
-0.0V
-0.5V
-1.0V
283ns
284ns
288ns
292ns
296ns
300ns
303ns
TIME
V(SP1)
V(OUTPUT)
.5*V(PULSE)-1

FIG. 227

FIG. 228

CHARGE TRANSFER

DEFINITIONS:

q=CHARGE IN COULOMBS
C=CAPACITANCE IN FARADS
V=VOLTAGE IN VOLTS
A=INPUT SIGNAL AMPLITUDE

$q=C \cdot V$
$V=A \cdot \sin(t)$
$q(t)=C \cdot A \cdot \sin(t)$
$\Delta q(t)=C \cdot A \cdot \sin(t)-C \cdot A \cdot \sin(t-T)$
$\Delta q(t)=C \cdot A \cdot (\sin(t)-\sin(t-T))$ EQUATION A

$\Delta q(t)$ EXPRESSES THE CHANGE IN CHARGE ACROSS CAPACITOR C DURING APERTURE T. AS CAN BE SEEN, WHEN APERTURE T TENDS TOWARDS 0, $\Delta q(t)$ TENDS TOWARDS 0.

FIG. 229

USING THE SUM TO PRODUCT TRIGONOMETRIC IDENTITY,

$$\sin(\alpha)-\sin(\beta)=2\cdot\sin\left(\frac{\alpha-\beta}{2}\right)\cdot\cos\left(\frac{\alpha+\beta}{2}\right) \qquad \text{IDENTITY 1}$$

EQUATION 1 CAN BE RE-WRITTEN AS:

$$\Delta q(t)=2\cdot C\cdot A\cdot\sin\left[\frac{t-(t-T)}{2}\right]\cdot\cos\left[\frac{t+(t-T)}{2}\right]$$

$$\Delta q(t)=2\cdot C\cdot A\cdot\sin\left(\frac{1}{2}\cdot T\right)\cdot\cos\left(t-\frac{1}{2}\cdot T\right) \qquad \text{EQUATION B}$$

THE sin TERM IN EQUATION B IS A FUNCTION OF APERTURE T ONLY. IT IS EASILY SEEN THAT $\Delta q(t)$ WILL OBTAIN A MAXIMUM VALUE WHEN T IS EQUAL TO AN ODD MULTIPLE OF π i.e., π 3 π 5 π.. THEREFORE, CAPACITOR C EXPERIENCES THE GREATEST CHANGE IN CHARGE WHEN THE APERTURE HAS A VALUE OF π OR A TIME INTERVAL REPRESENTATIVE OF 180 DEGREES OF THE INPUT SINUSOID. CONVERSELY, WHEN T IS EQUAL TO 2π, 4π, 6π....MINIMAL CHARGE IS TRANSFERRED.

FIG. 230

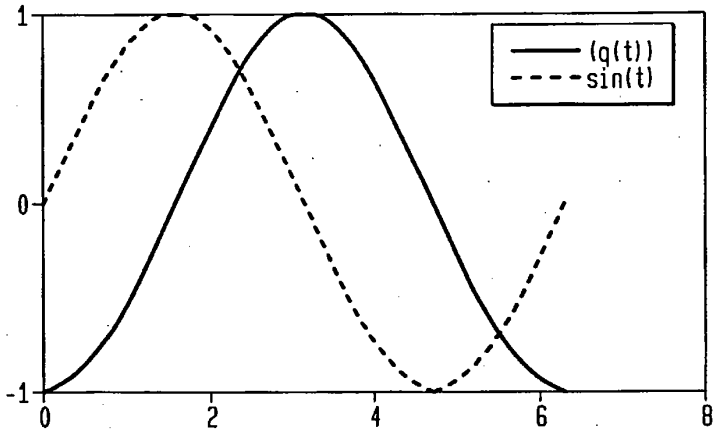
SOLVING FOR q(t) BY INTEGRATING EQUATION A ALLOWS THE CHARGE ON C WITH RESPECT TO TIME TO BE GRAPHED ON THE SAME AXIS AS THE INPUT SINUSOID sin(t).

$$q(t)=\int C\cdot A\cdot(\sin(t)-\sin(t-T))dt$$

$$q(t)=-\cos(t)\cdot C\cdot A+\cos(t-T)\cdot C\cdot A$$

$$q(t)=C\cdot A\cdot(\cos(t-T)-\cos(t)) \quad \text{EQUATION C}$$

FIG. 231



GRAPH 1

C=1; A=.5, T=π

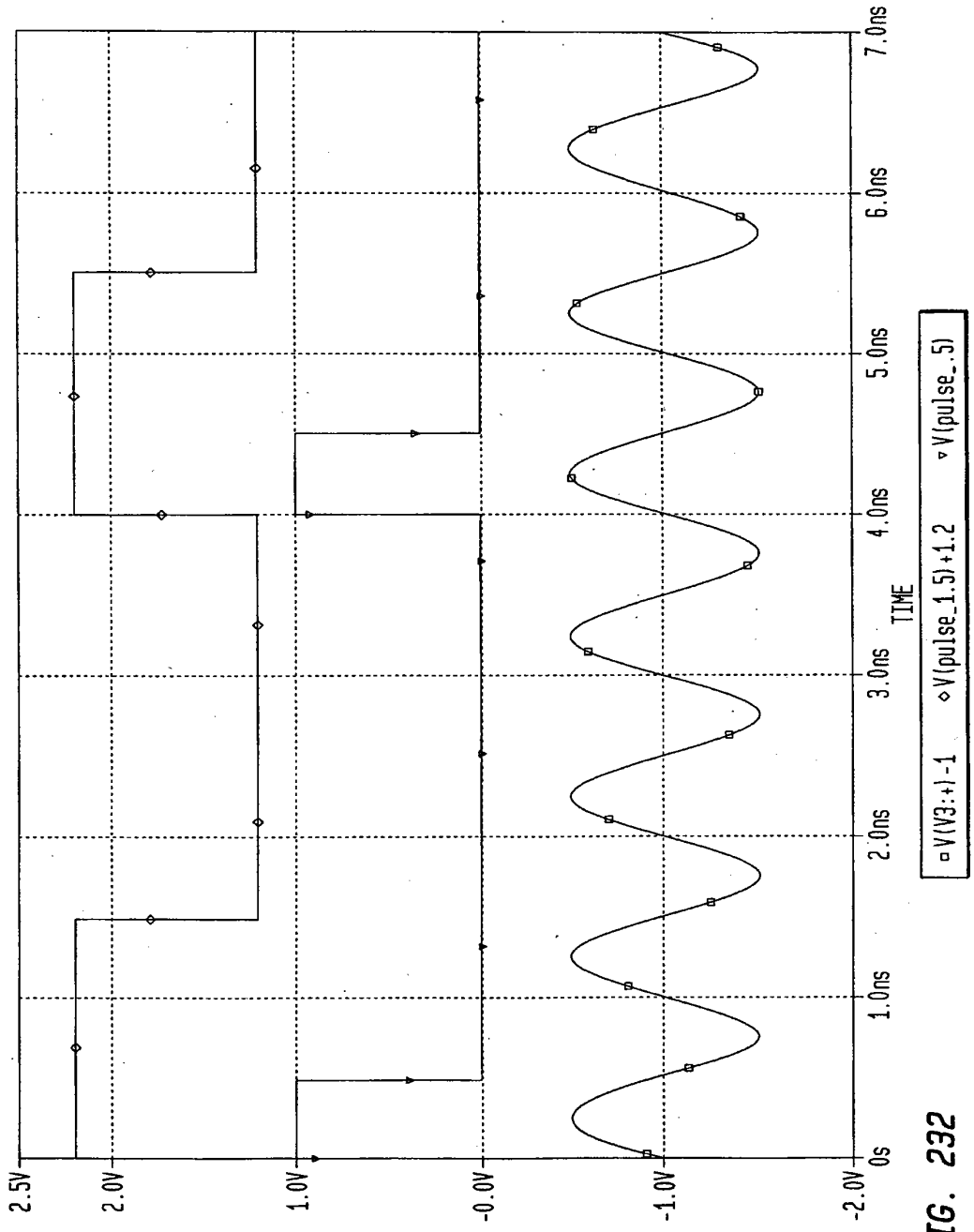

2.5V
2.0V
1.0V
-0.0V
-1.0V
-2.0V
0s
1.0ns
2.0ns
3.0ns
4.0ns
5.0ns
6.0ns
7.0ns
TIME
V(V3:+)-1
V(pulse_1.5)+1.2
V(pulse_.5)

FIG. 232

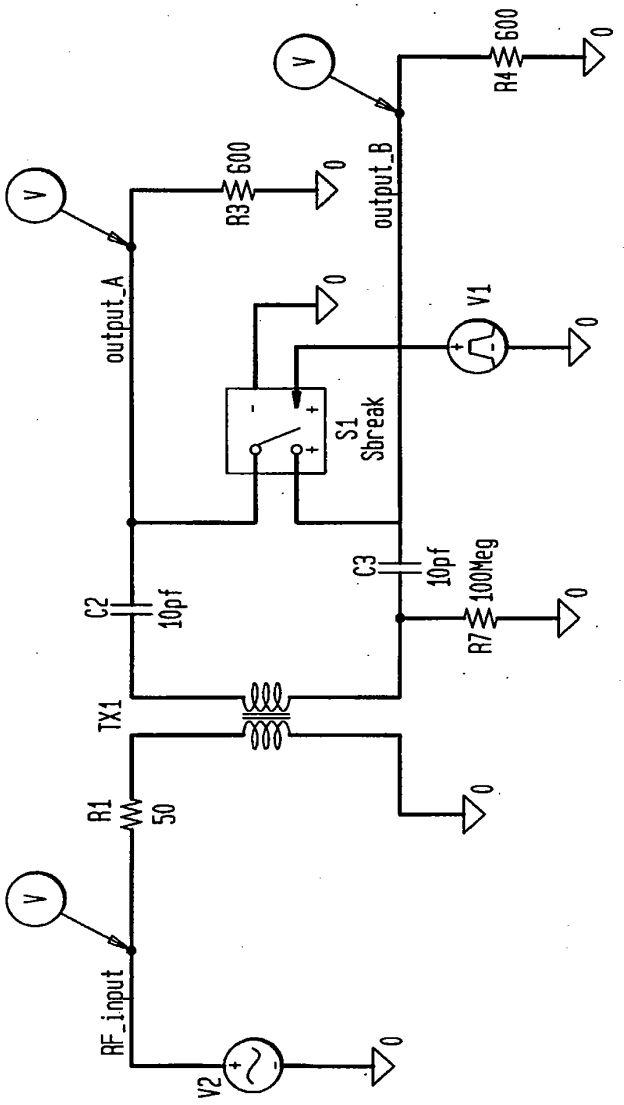

R4
600
0
output_B
R3
600
output_A
V1
S1
Sbreak
C3
10pf
100Meg
R7
C2
10pf
TX1
R1
50
RF_input
V2

FIG. 233

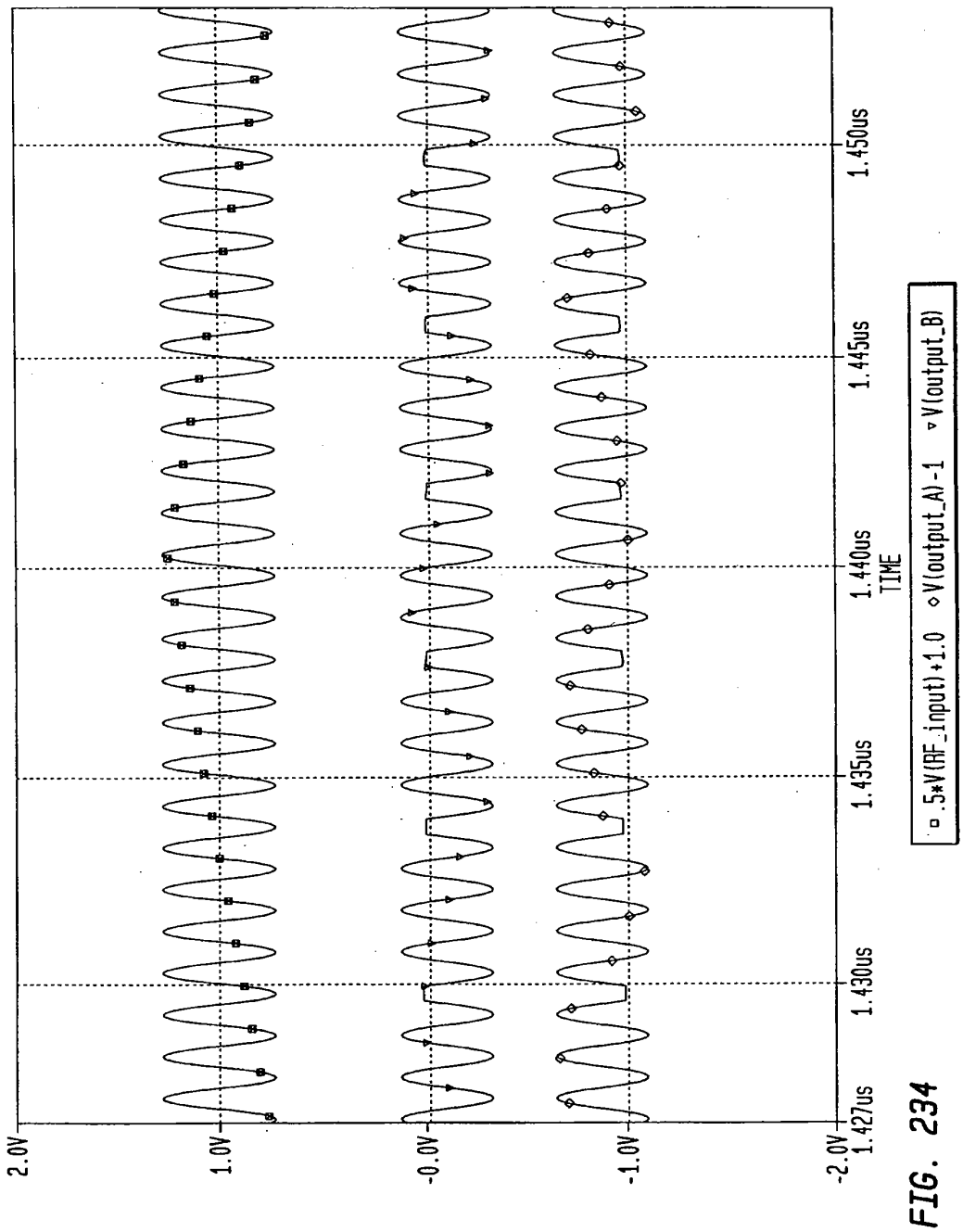

2.0V
1.0V
-0.0V
-1.0V
-2.0V
1.427us
1.430us
1.435us
1.440us
1.445us
1.450us
TIME
□ .5*V(RF_input)+1.0
◇ V(output_A)-1
▽ V(output_B)

FIG. 234

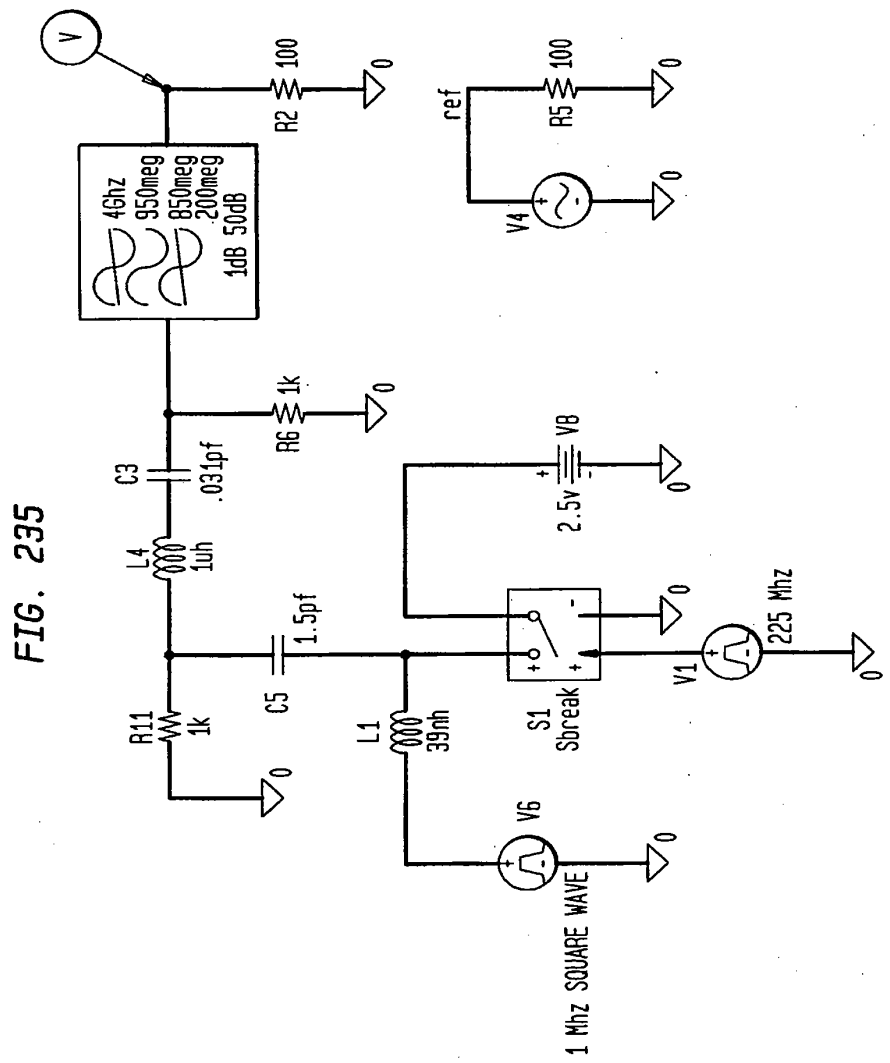

V
R2
100
0
4Ghz
950meg
850meg
200meg
1dB 50dB
ref
R5
100
V4
R6
1k
C3
.031pf
L4
1uh
VB
2.5v
C5
1.5pf
R11
1k
L1
39nh
S1
Sbreak
V1
225 Mhz
V6
1 Mhz SQUARE WAVE

FIG. 235

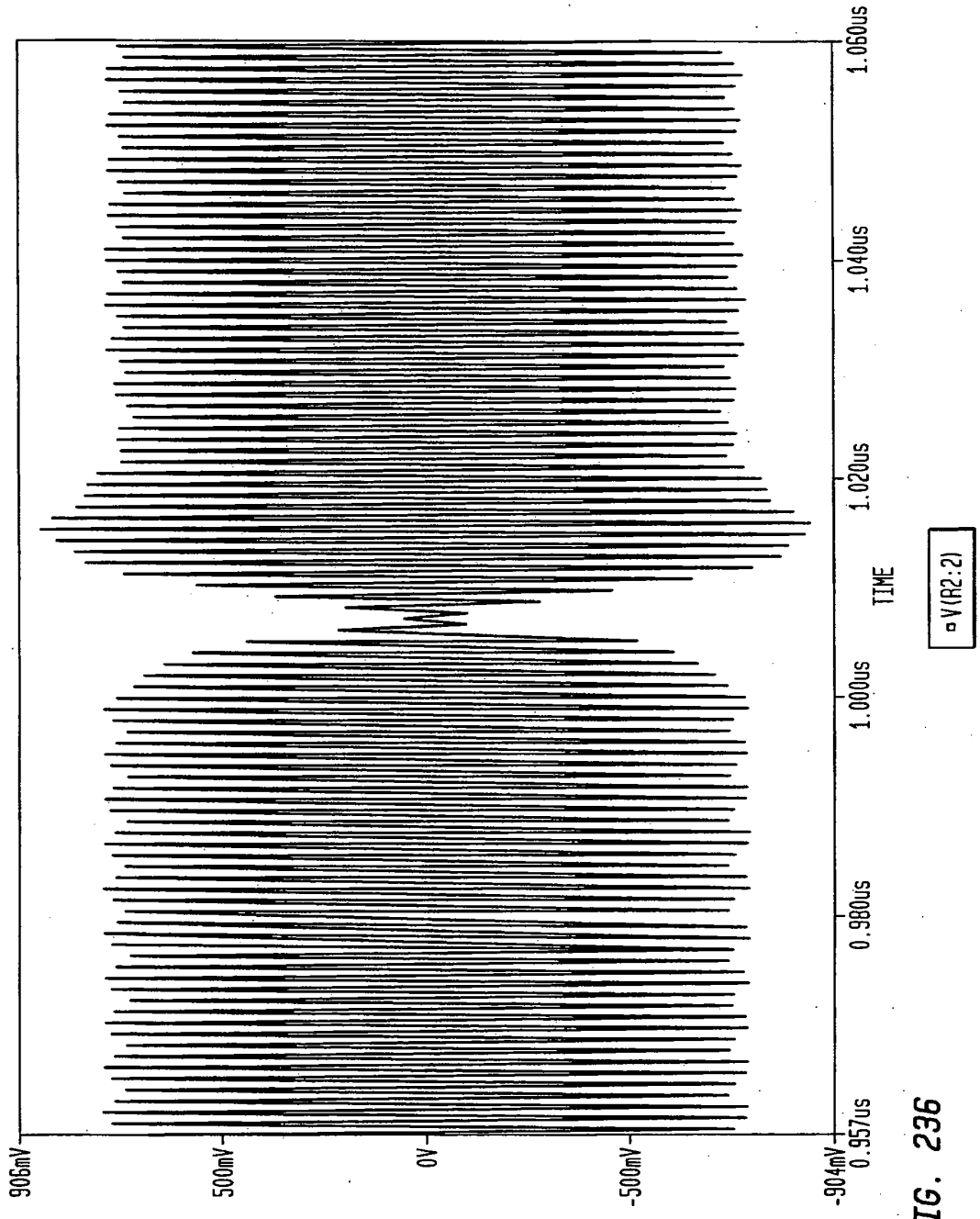

906mV
500mV
0V
-500mV
-904mV
0.957us
0.980us
1.000us
1.020us
1.040us
1.060us
TIME
V(R2:2)

FIG. 236

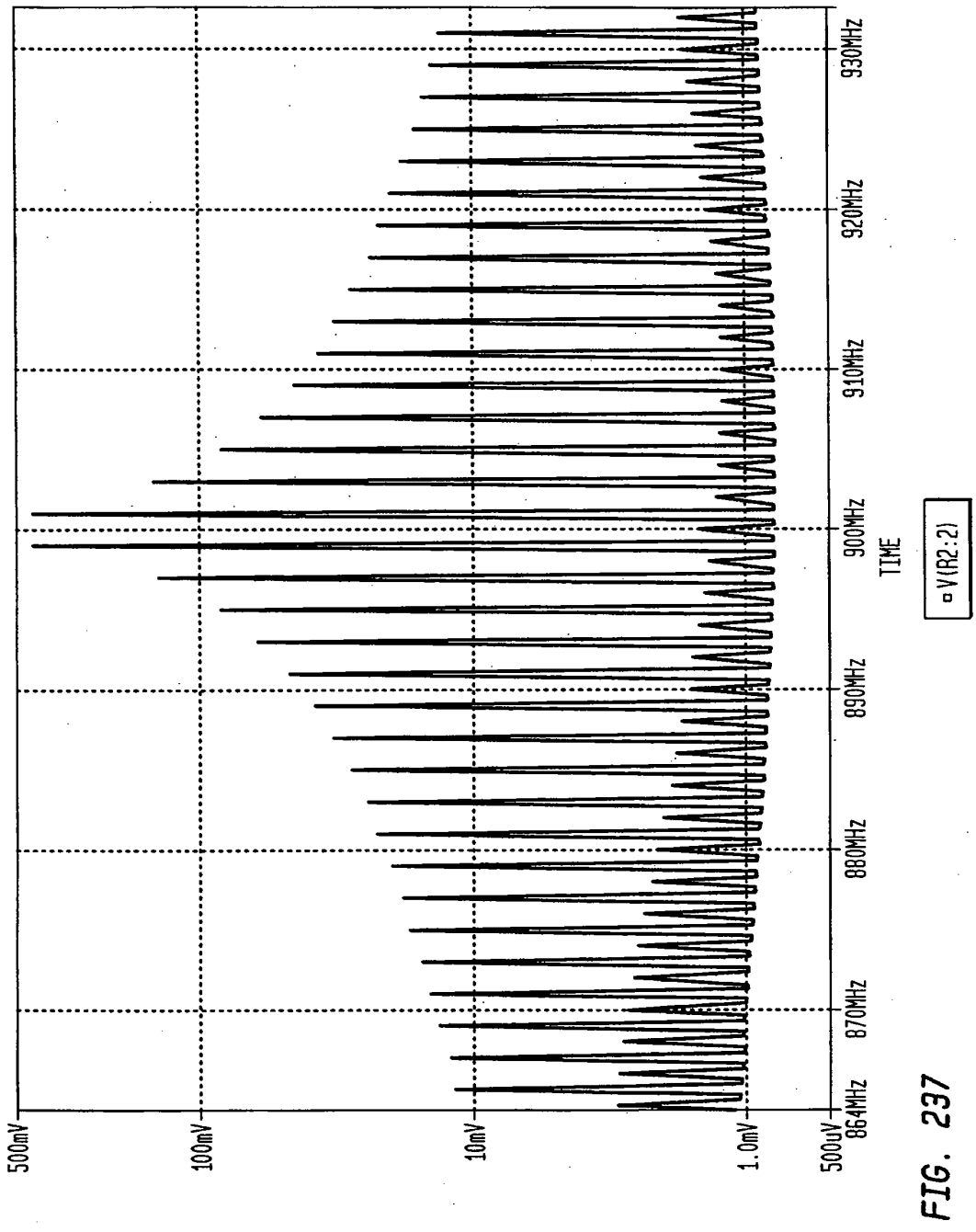

500mV
100mV
10mV
1.0mV
500uV
864MHz
870MHz
880MHz
890MHz
900MHz
910MHz
920MHz
930MHz
TIME
V(R2:2)

FIG. 237

FIG. 238

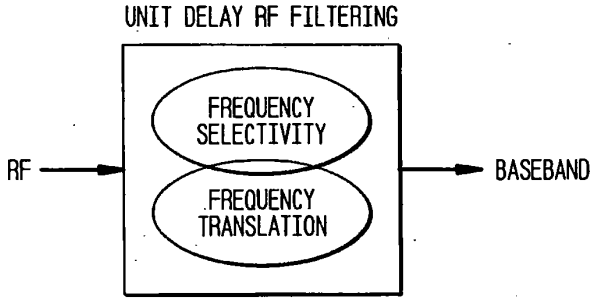


FIG. 239

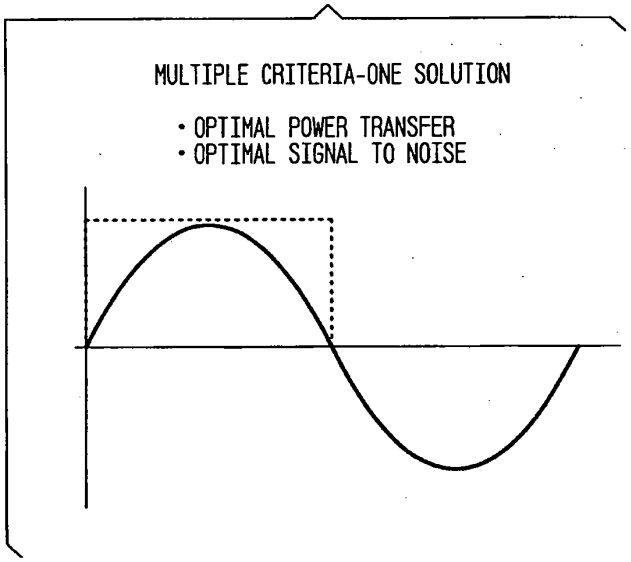


FIG. 240

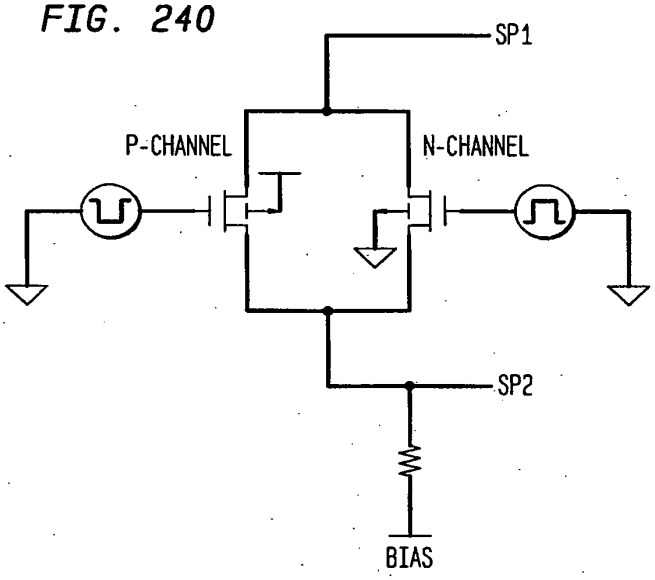


FIG. 241

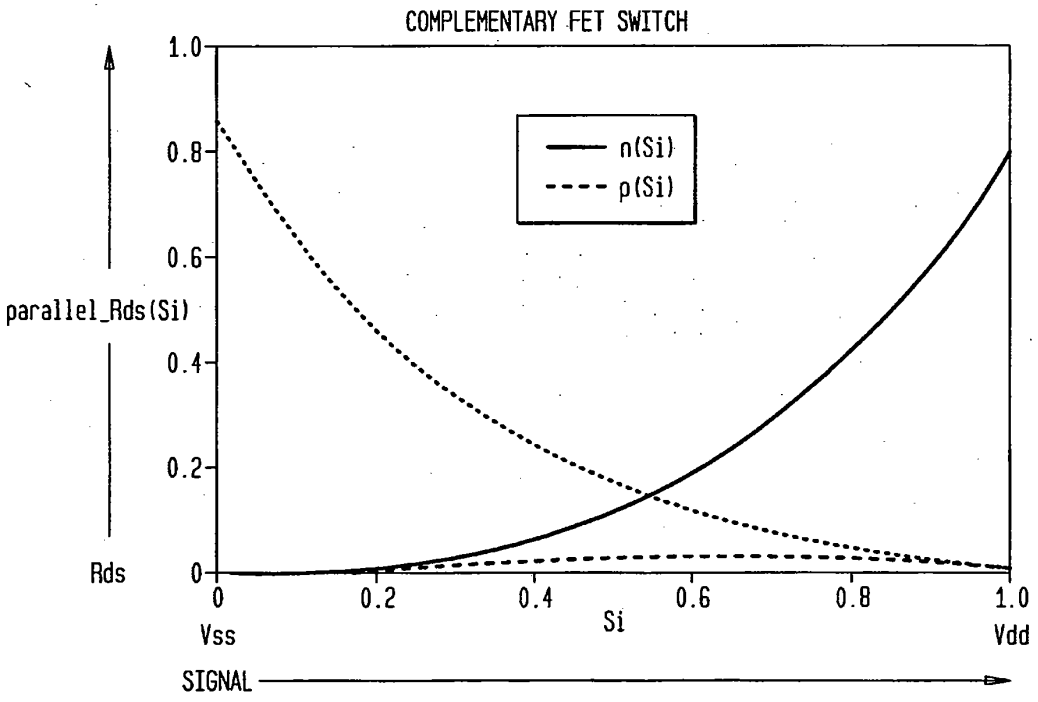
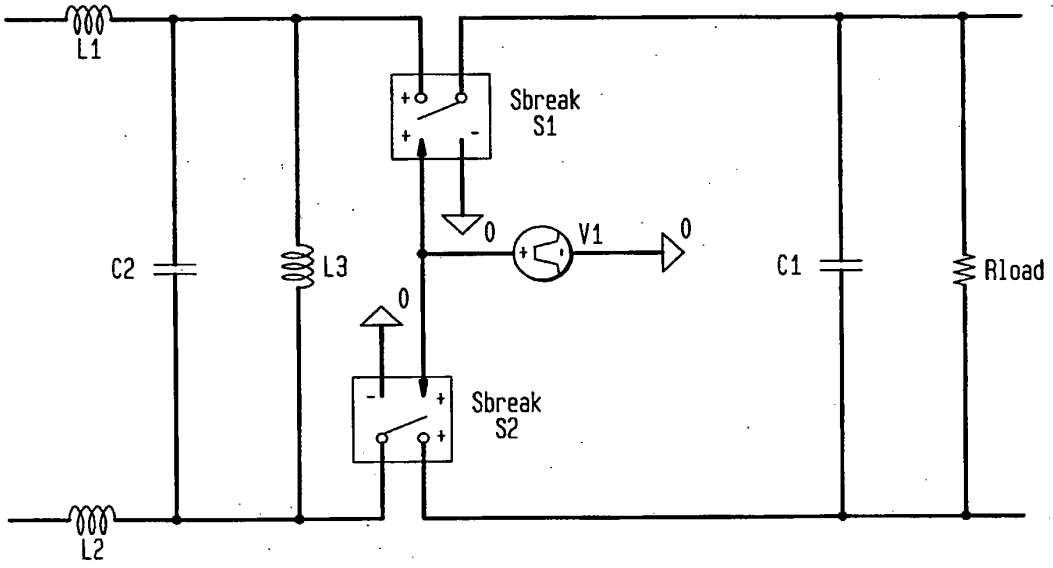


FIG. 242

DIFFERENTIAL CONFIGURATION



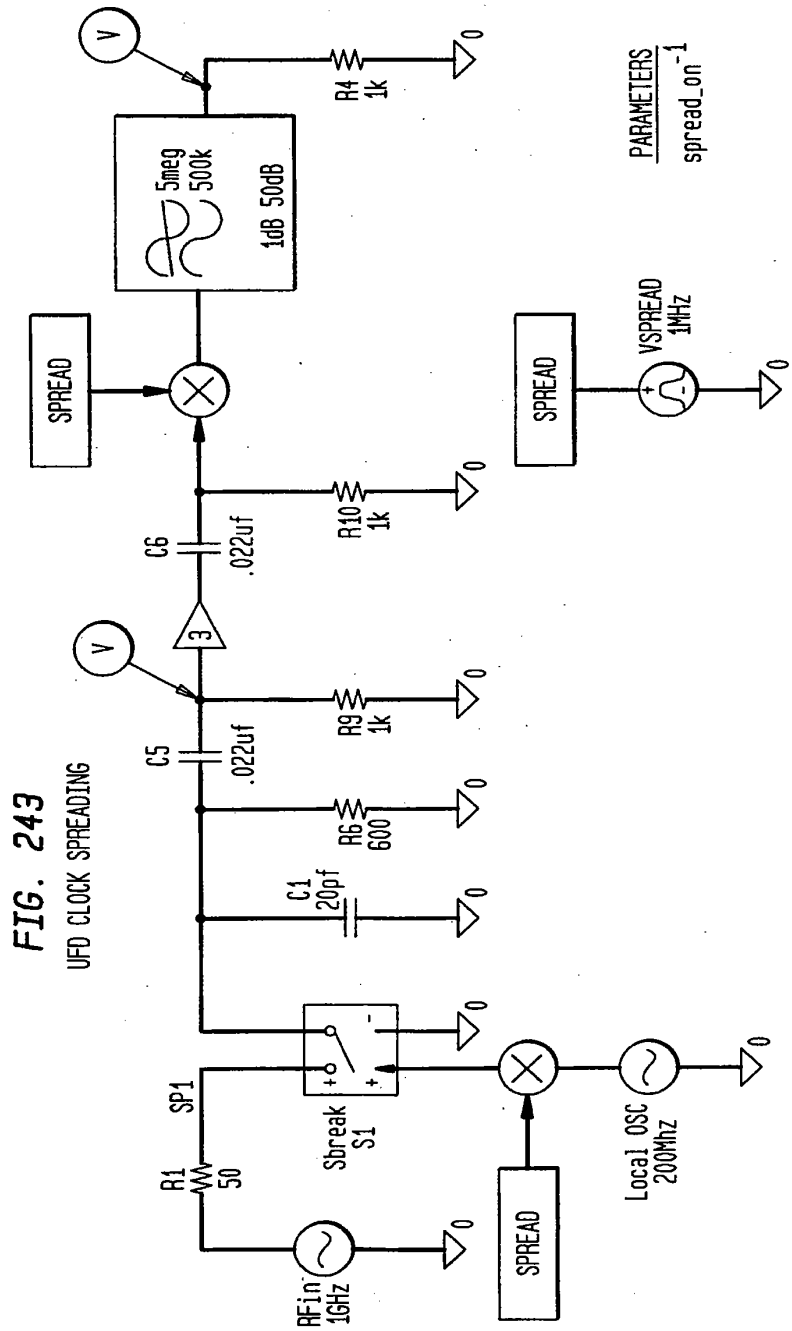


FIG. 243
UFD CLOCK SPREADING

FIG. 244

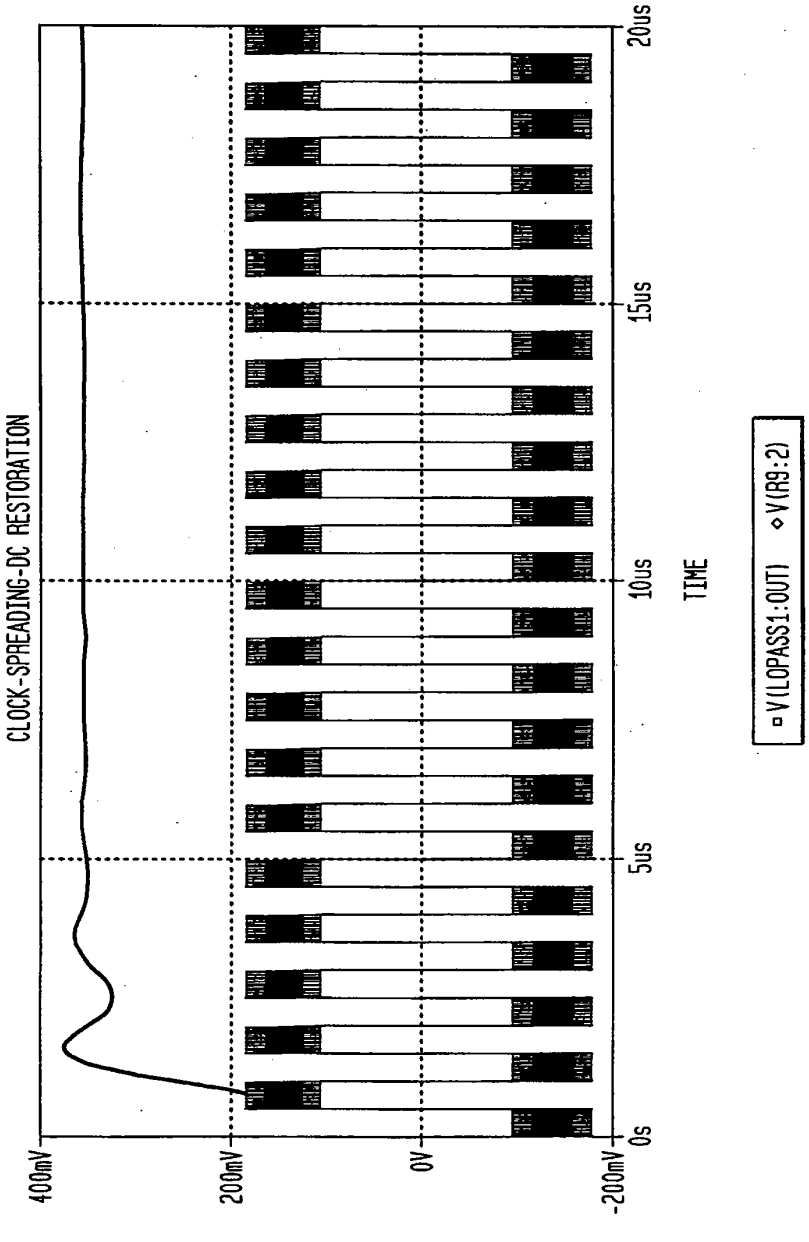

CLOCK-SPREADING-DC RESTORATION
400mV
200mV
0V
-200mV
0s
5us
10us
15us
20us
TIME
V(LOPASS1:OUT)
V(R9:2)

FIG. 245

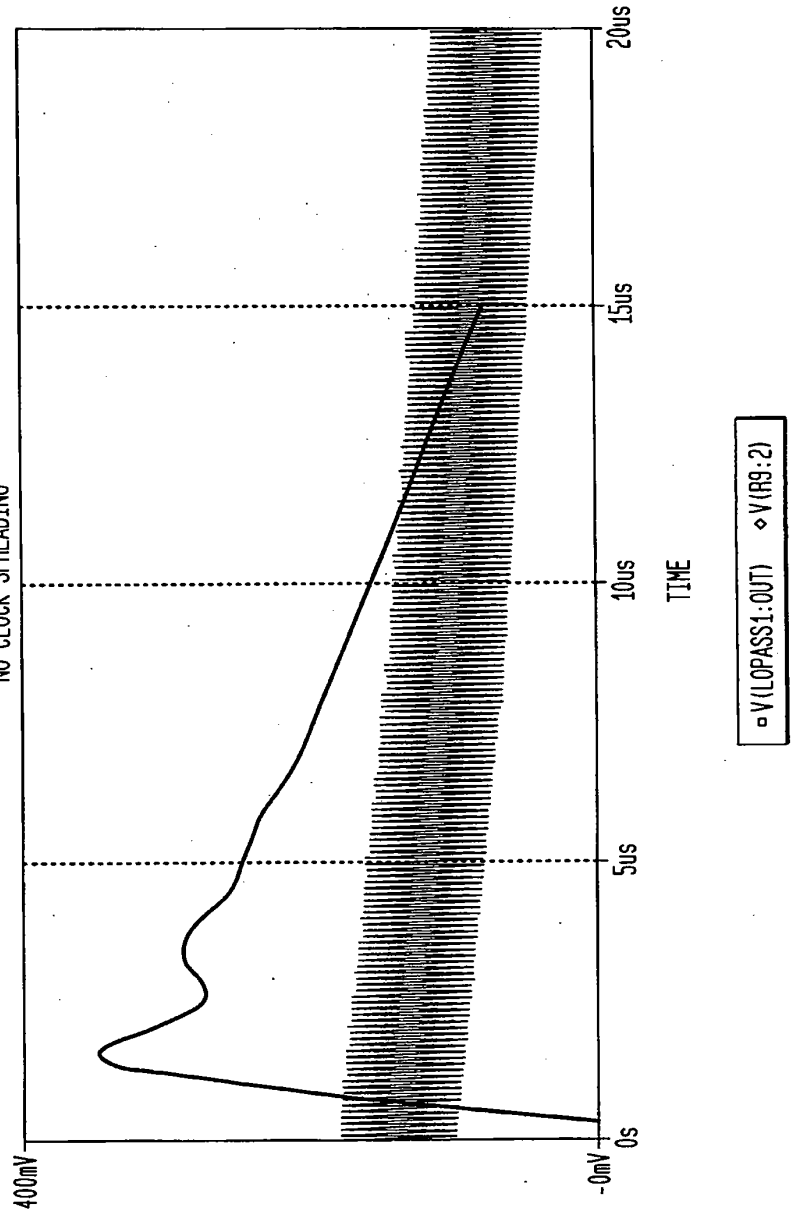

NO CLOCK SPREADING
400mV
-0mV
0s
5us
10us
15us
20us
TIME
V(LOPASS1:OUT)
V(R9:2)

FIG. 246

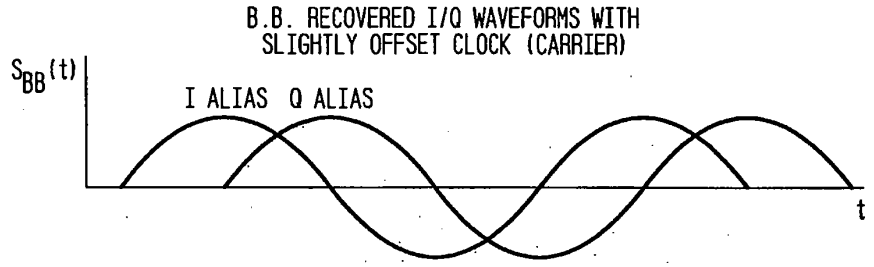


FIG. 247

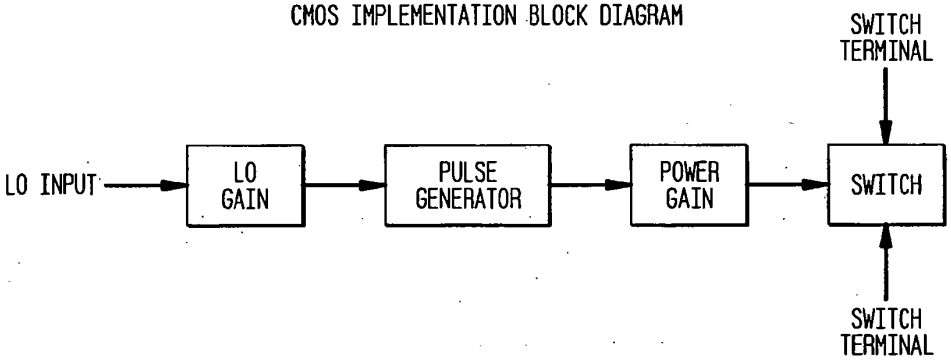


FIG. 248

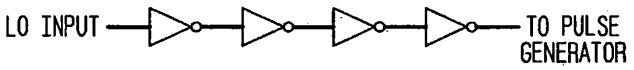


FIG. 249

LO GAIN BLOCK AT TRANSISTOR LEVEL

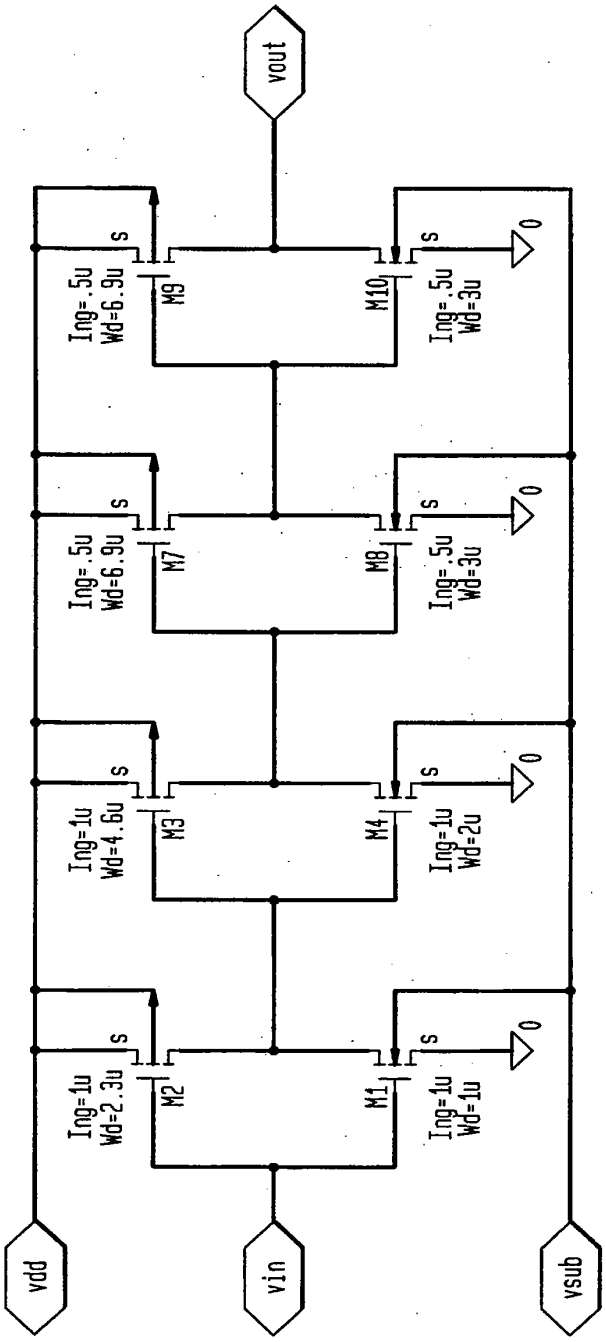


FIG. 250

PULSE GENERATOR#1 AT GATE LEVEL

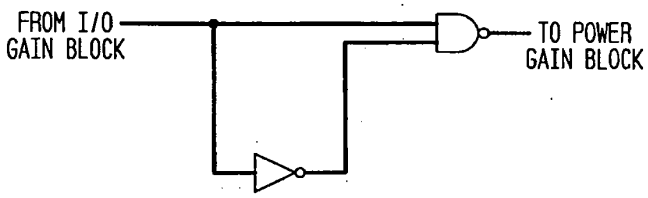


FIG. 251

PULSE GENERATOR#1 AT TRANSISTOR LEVEL

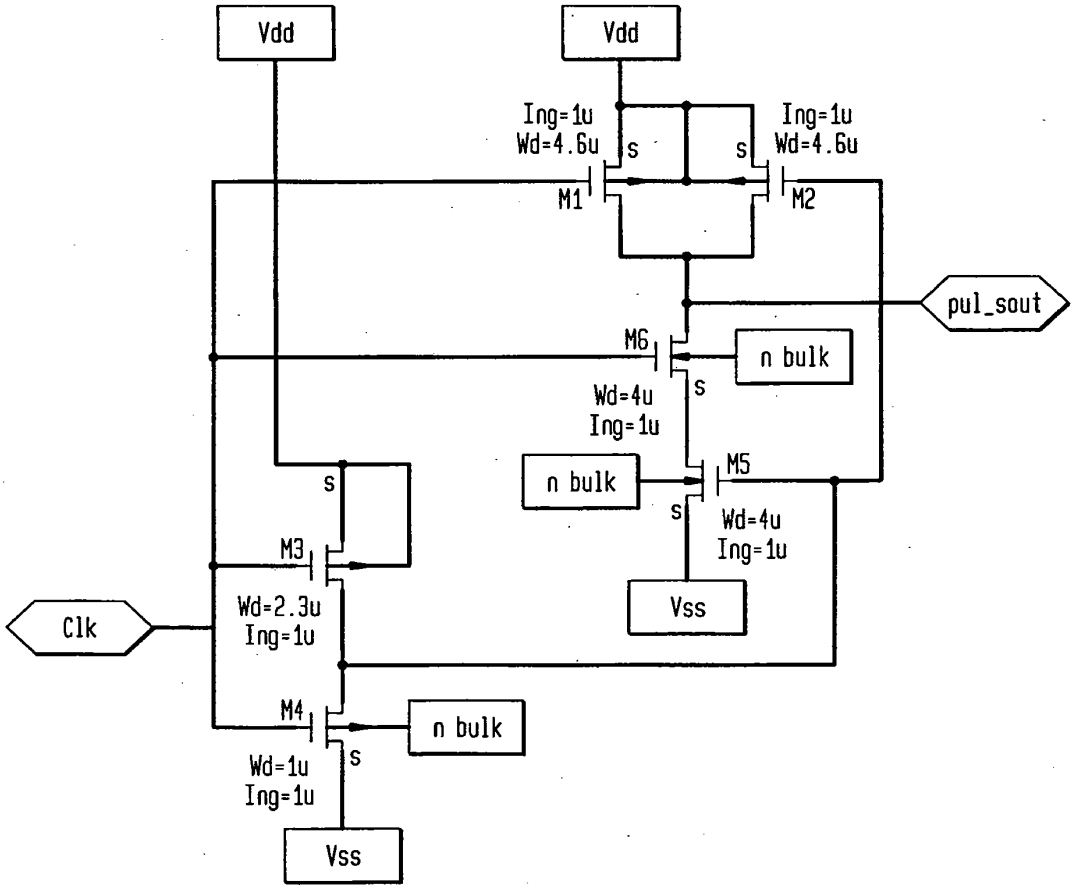


FIG. 252

POWER GAIN BLOCK AT GATE LEVEL

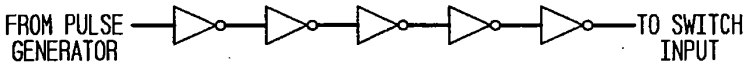
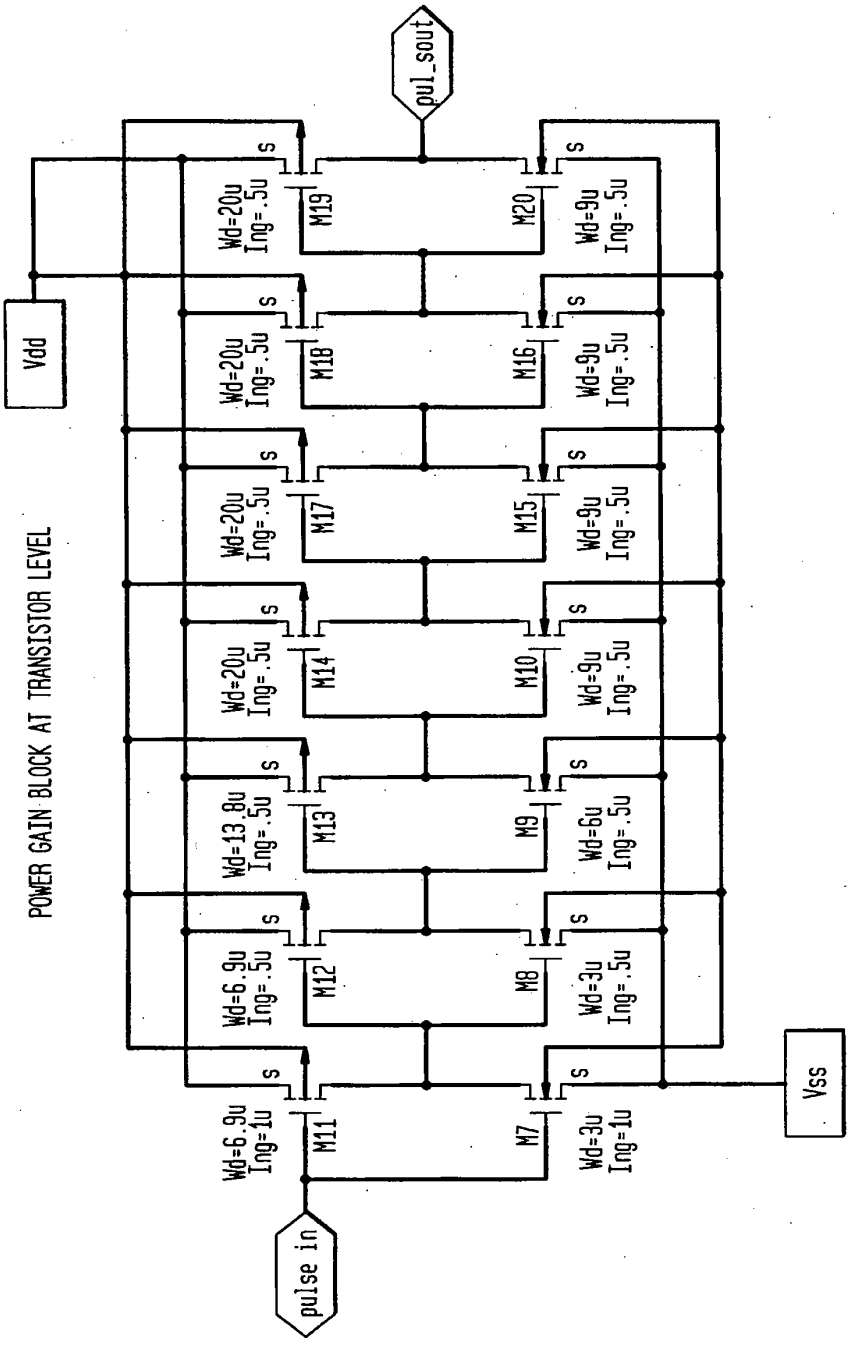


FIG. 253

POWER GAIN BLOCK AT TRANSISTOR LEVEL



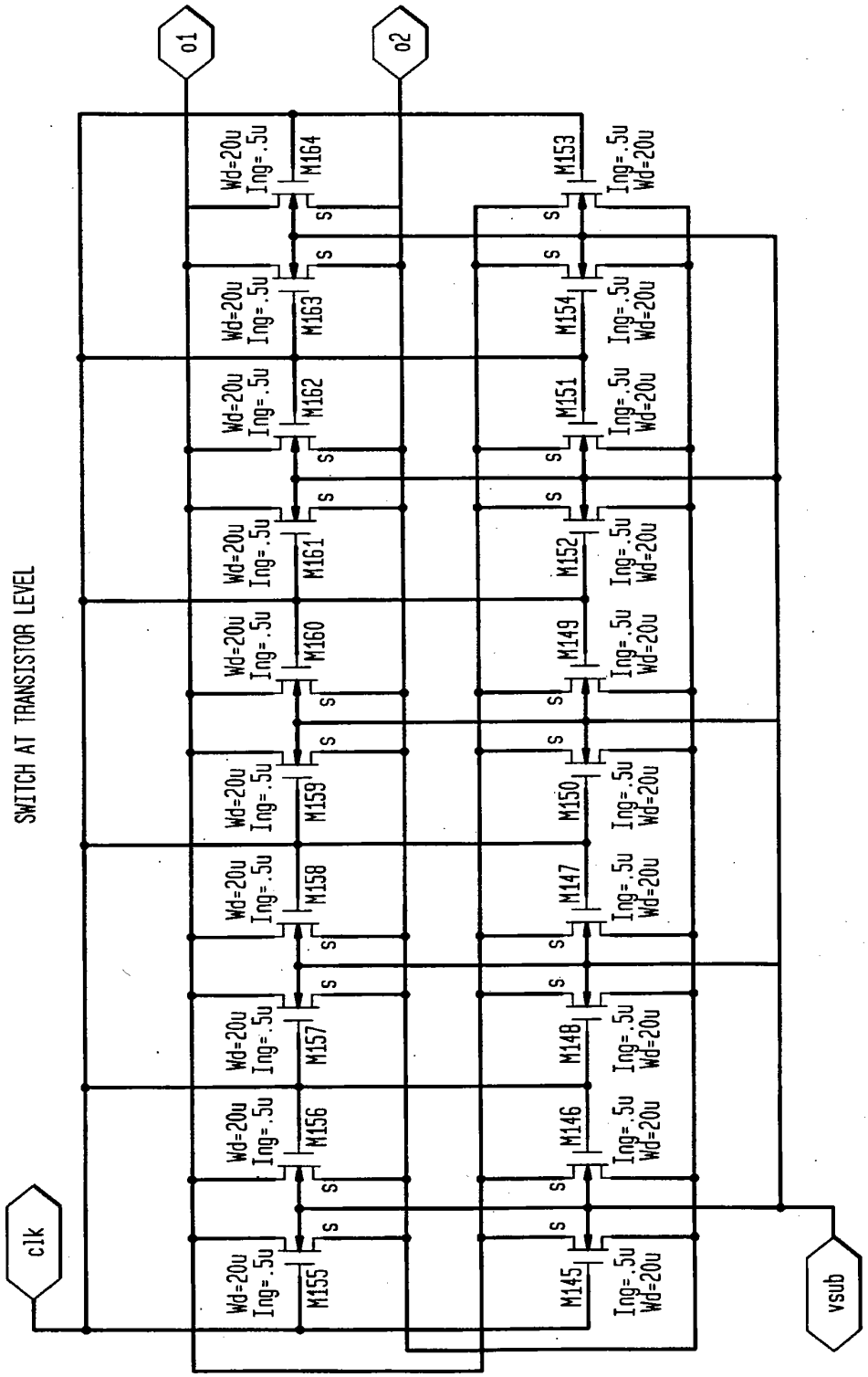


FIG. 254

SWITCH AT TRANSISTOR LEVEL

FIG. 255

CMOS "HOT CLOCK" BLOCK DIAGRAM

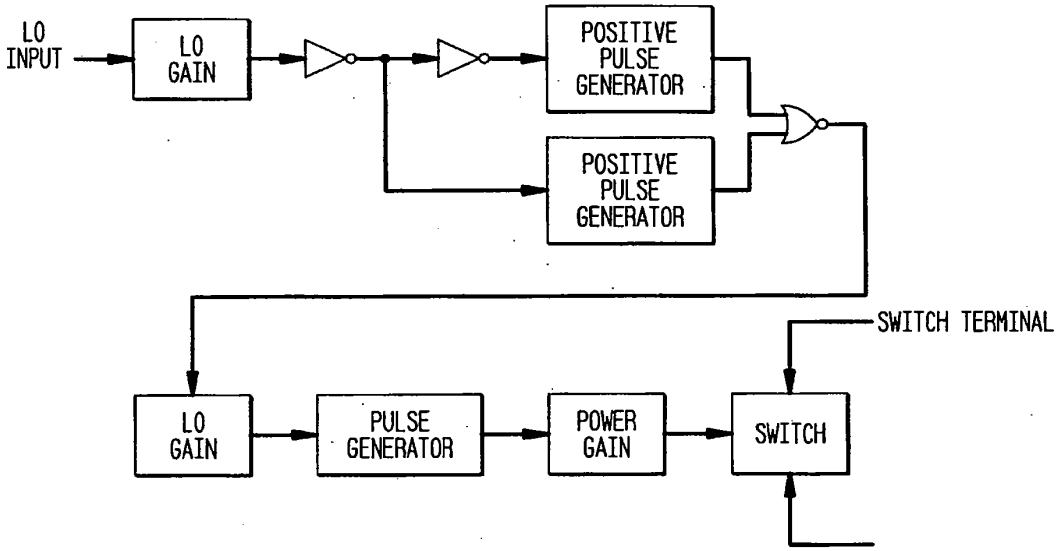


FIG. 256

POSITIVE PULSE GENERATOR AT GATE LEVEL

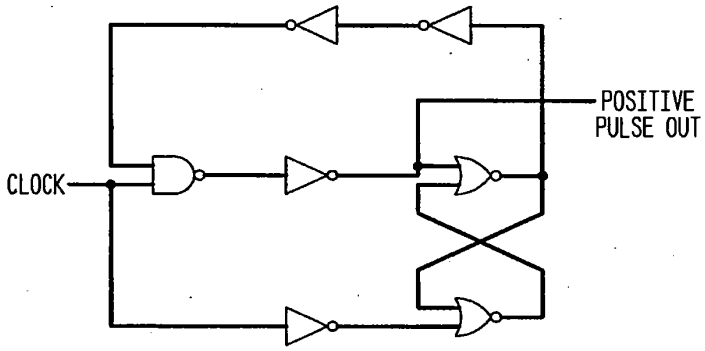


FIG. 257
POSITIVE PULSER AT TRANSISTOR LEVEL

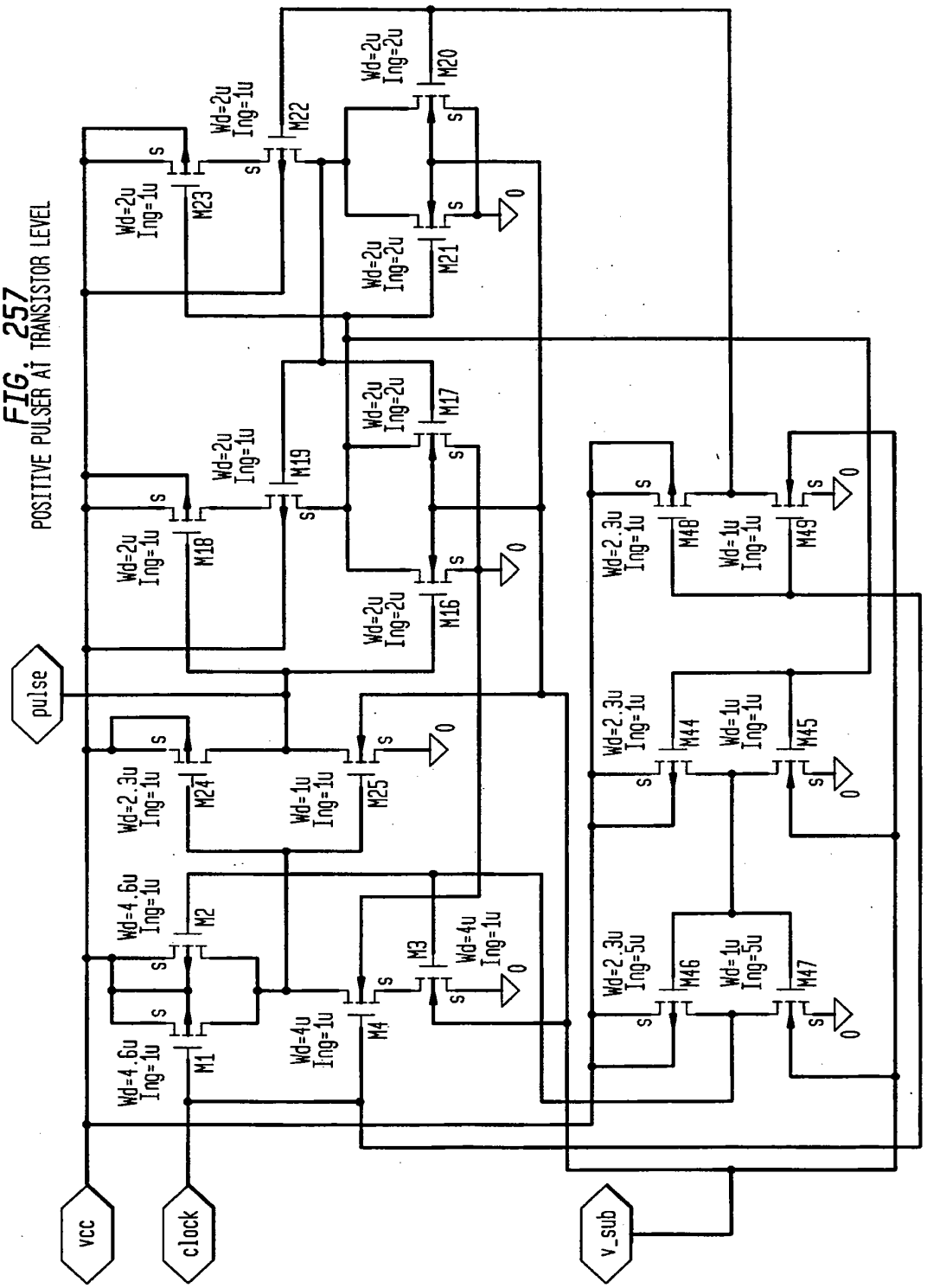
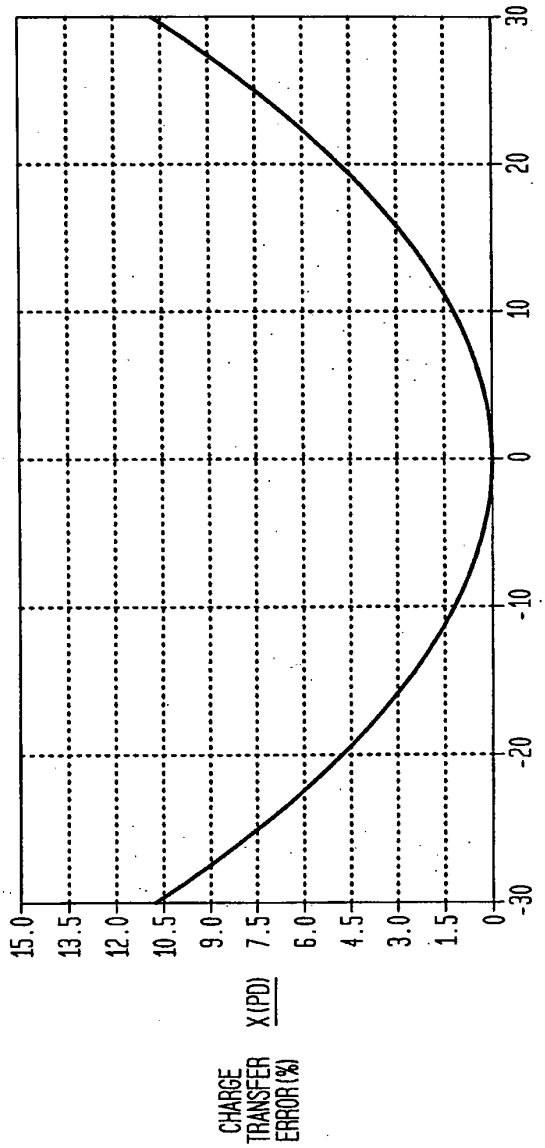


FIG. 25B

PULSE WIDTH ERROR EFFECT FOR 1/2 CYCLE



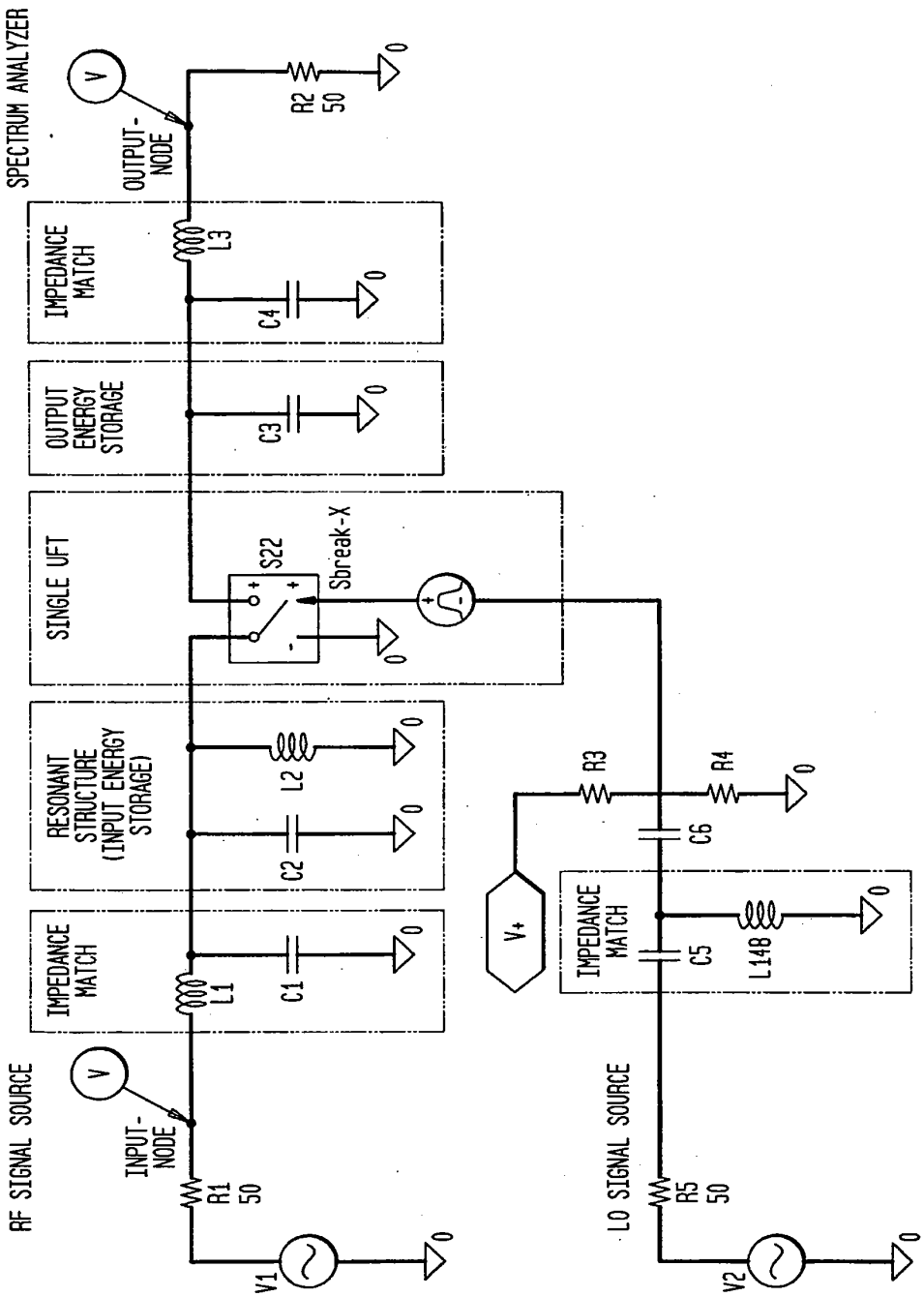


FIG. 259
SINGLE-ENDED UFD MODULE

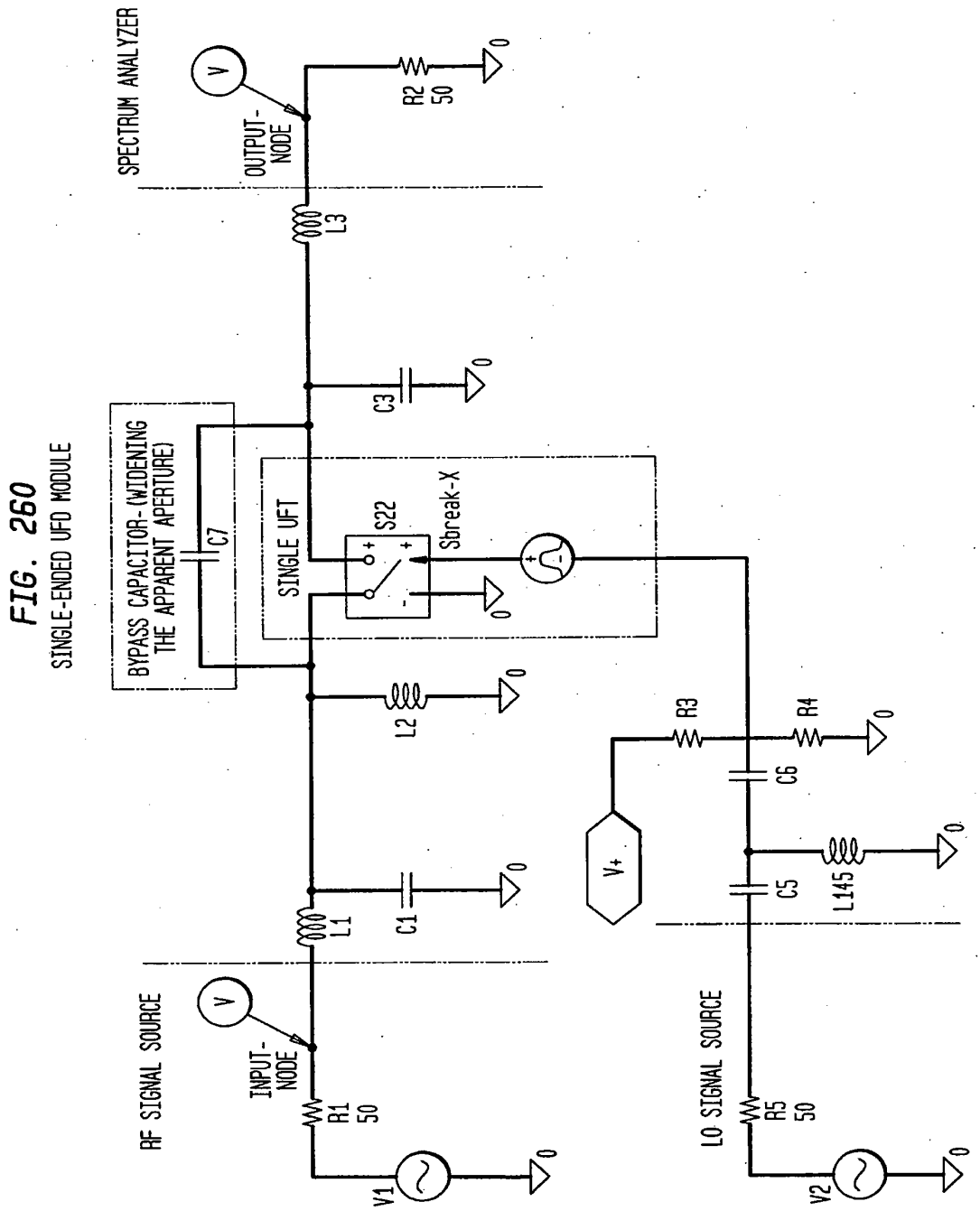


FIG. 26O
SINGLE-ENDED UFD MODULE

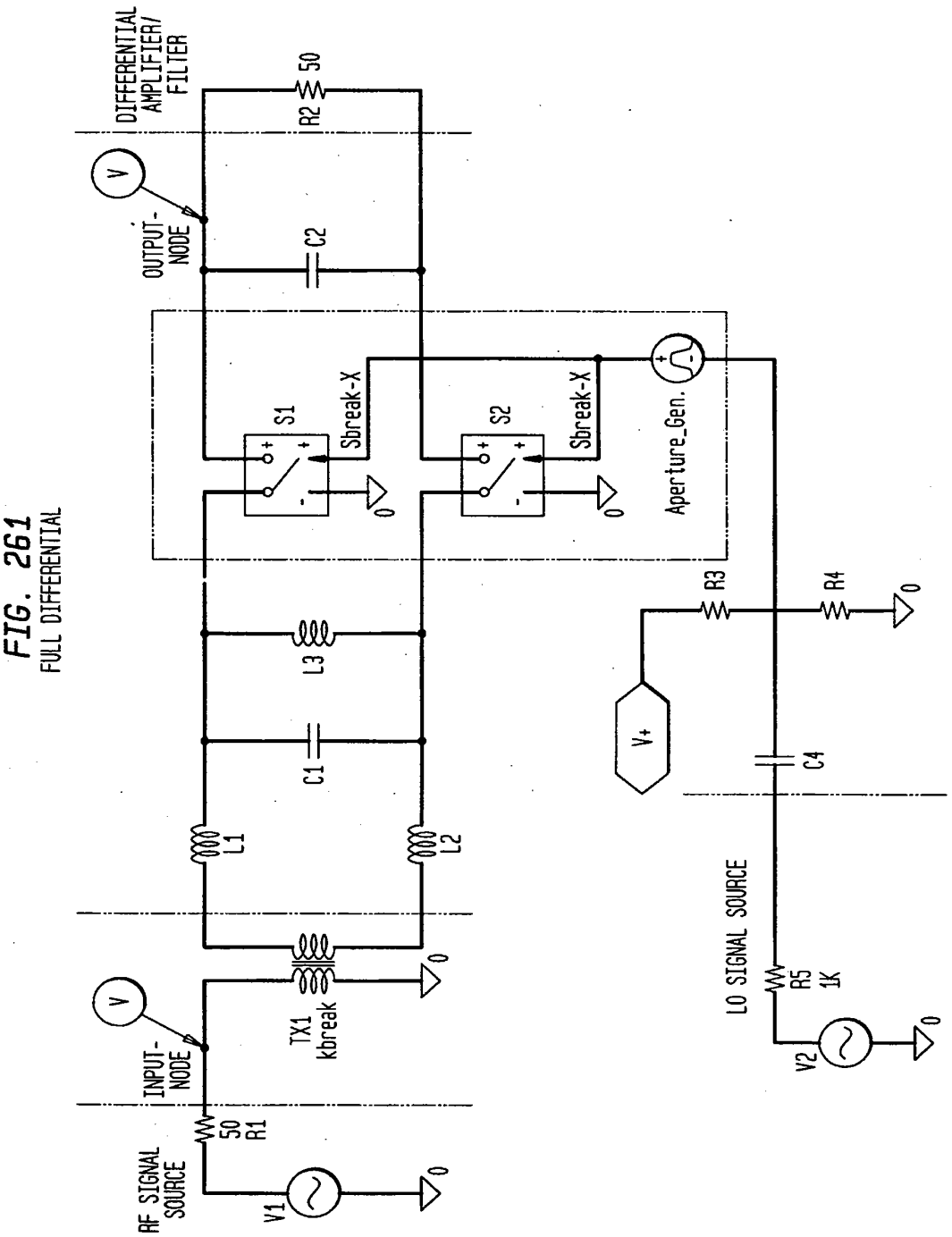


FIG. 261
FULL DIFFERENTIAL

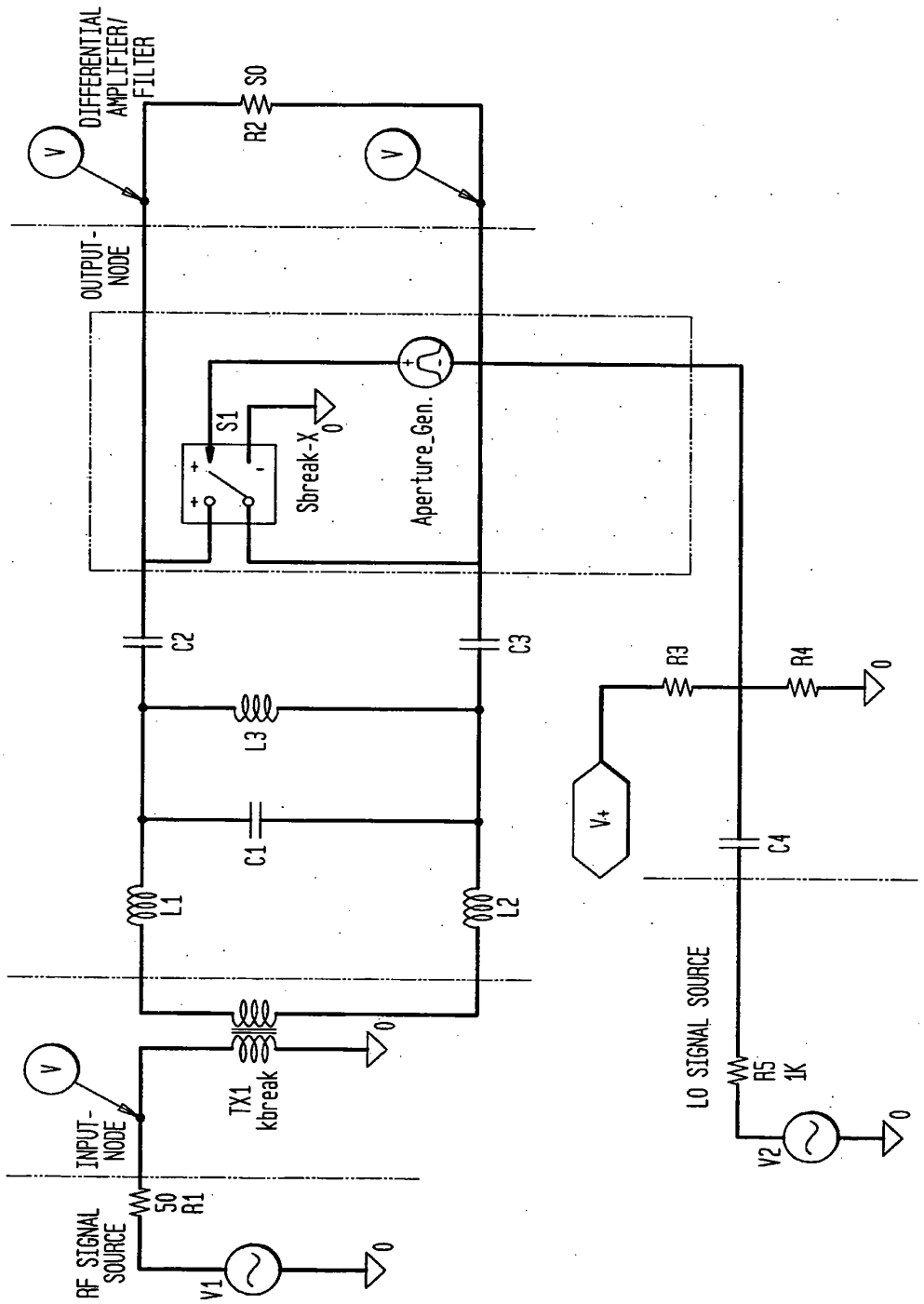


FIG. 262
FULL DIFFERENTIAL

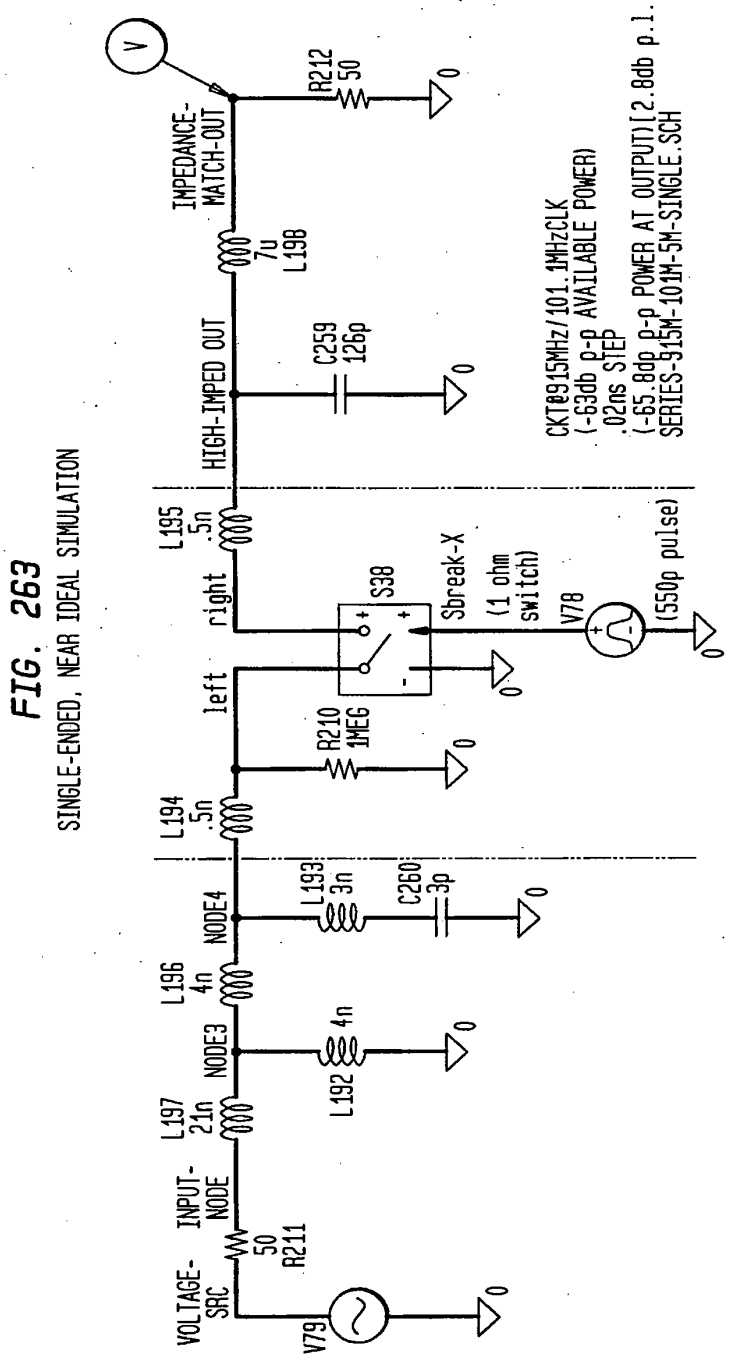


FIG. 263

SINGLE-ENDED, NEAR IDEAL SIMULATION

FIG. 264

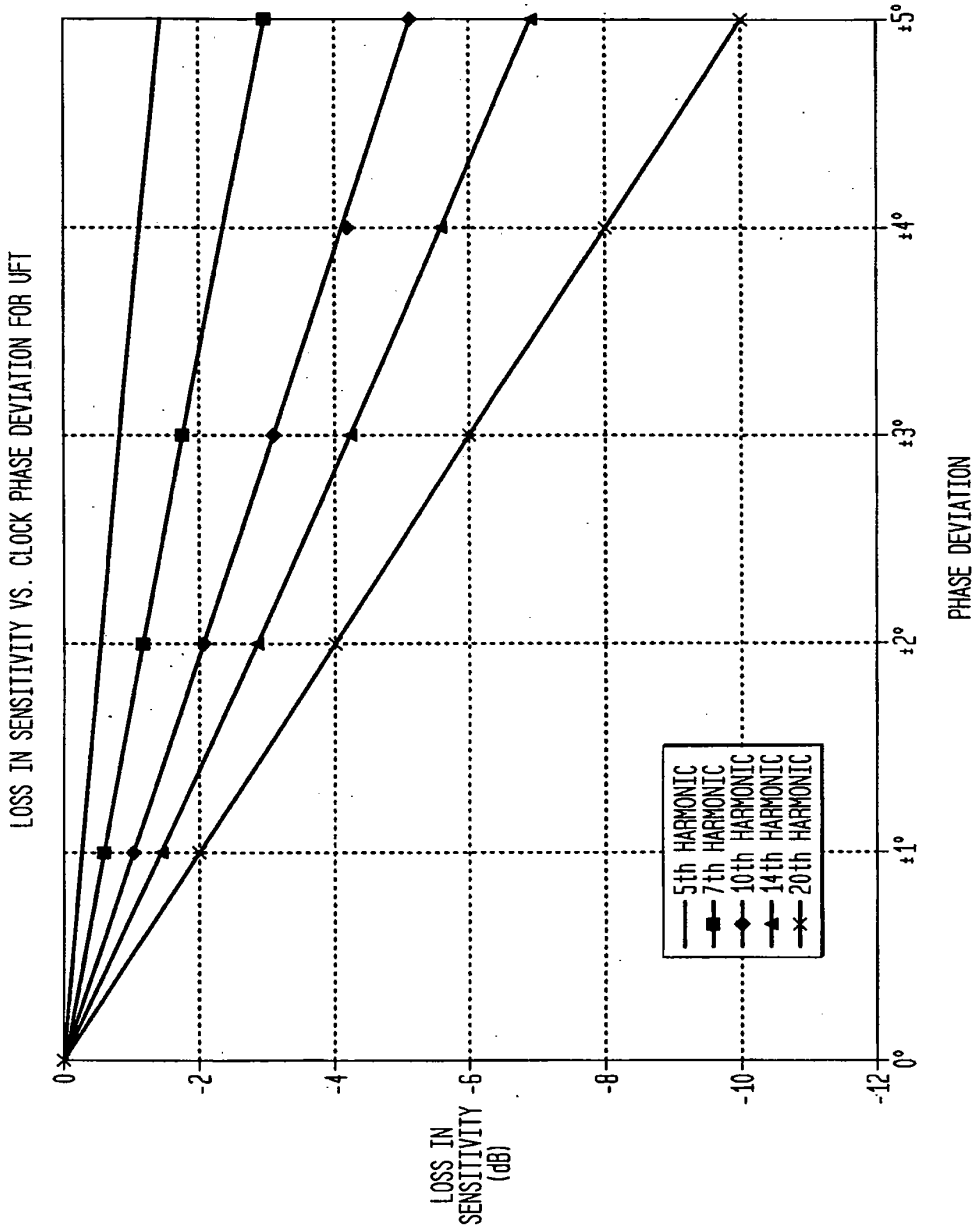
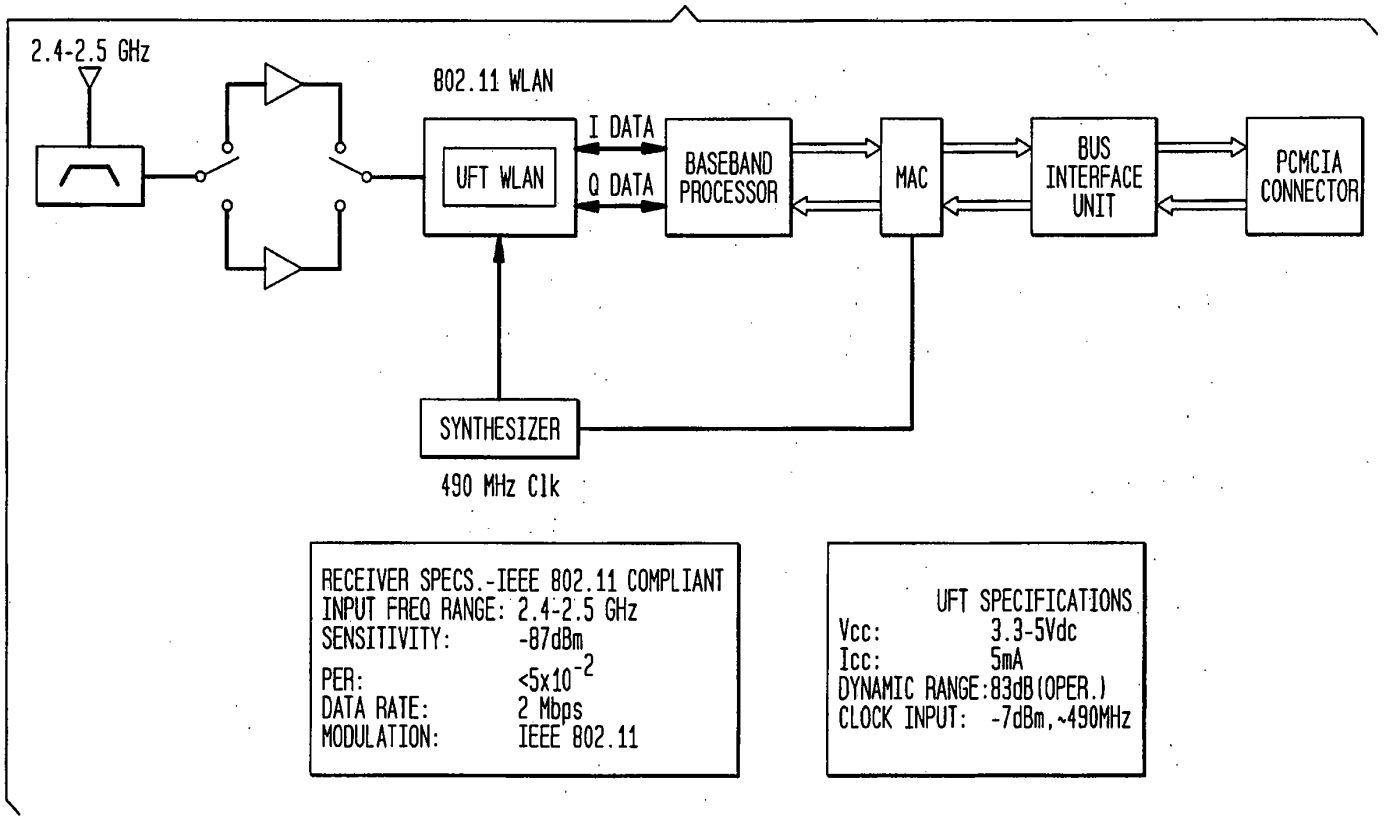

LOSS IN SENSITIVITY VS. CLOCK PHASE DEVIATION FOR UFT
LOSS IN SENSITIVITY (dB)
0
-2
-4
-6
-8
-10
-12
0°
±1°
±2°
±3°
±4°
±5°
PHASE DEVIATION
5th HARMONIC
7th HARMONIC
10th HARMONIC
14th HARMONIC
20th HARMONIC

FIG. 265


2.4-2.5 GHz
802.11 WLAN
UFT WLAN
I DATA
Q DATA
BASEBAND PROCESSOR
MAC
BUS INTERFACE UNIT
PCMCIA CONNECTOR
SYNTHESIZER
490 MHz Clk
RECEIVER SPECS.-IEEE 802.11 COMPLIANT
INPUT FREQ RANGE: 2.4-2.5 GHz
SENSITIVITY: -87dBm
PER: <5x10^-2
DATA RATE: 2 Mbps
MODULATION: IEEE 802.11
UFT SPECIFICATIONS
Vcc: 3.3-5Vdc
Icc: 5mA
DYNAMIC RANGE: 83dB(OPER.)
CLOCK INPUT: -7dBm,~490MHz

1013

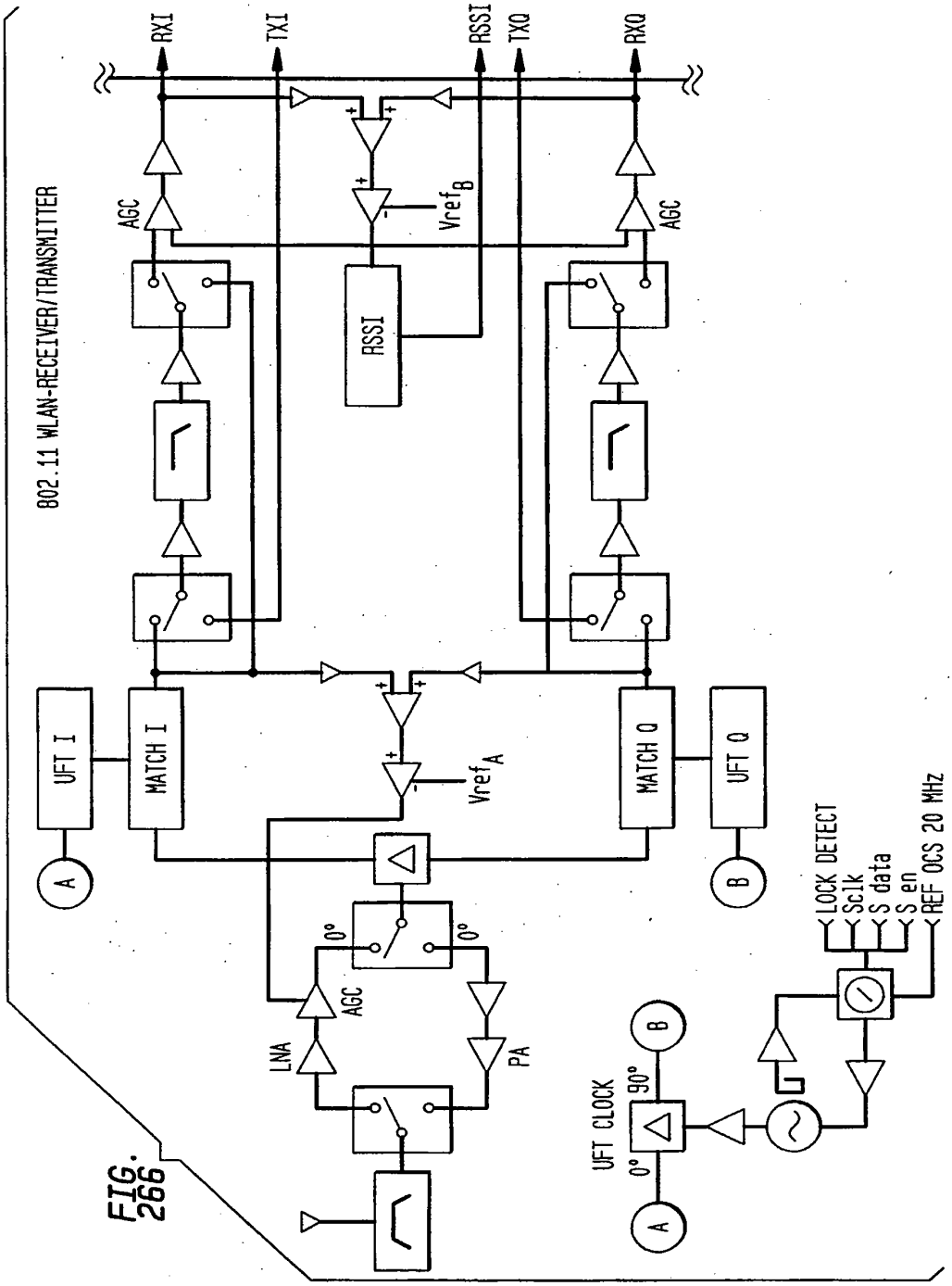

802.11 WLAN-RECEIVER/TRANSMITTER
RXI
TXI
RSSI
TXQ
RXQ
AGC
AGC
RSSI
Vref_B
UFT I
MATCH I
MATCH Q
UFT Q
Vref_A
A
B
0°
0°
LNA
AGC
PA
UFT CLOCK
90°
0°
B
A
LOCK DETECT
Sclk
S data
S en
REF OCS 20 MHz

FIG. 266

FIG. 267

PARAMETER	802.11 REQUIREMENT OR INDUSTRY PRACTICE	UFT MODULE BASED RX PERFORMANCE
OPERATING BAND	2.4-2.5 GHz	2.4-2.5 GHz
CHANNELS	2.402 TO 2.495 IN 1 MHz STEPS 2.412 TO 2.484 GHz IN 5 MHz STEPS	2.402 TO 2.495 IN 1 MHz STEPS 2.412 TO 2.484 GHz IN 5 MHz STEPS
MODULATION	BPSK,QPSK,(BARKER,CCK)	BPSK,QPSK
TX SPECTRAL MASK	FIRST SIDELOBE REJECT<-30,+15dBm SECOND SIDELOBE REJECT<-50,+15dBm	-35 dBr,-55dBr
EYE OPENING	Verr<.35 FOR 1000 COMPLEX SAMPLES	<.3
OPERATIONAL DYNAMIC RANGE	76 dB (DERIVED)	83 dB
MAX. INPUT, @, 8% PER	-4 dBm	-4 dBm
SENSITIVITY	-80 dBm @ <8% PER	-87 dBm @ <5% PER
ACQUISITION	802.11 DSS AND FH	802.11 DSS AND FH
IMAGE REJECTION	>80 dB	>80 dB
LO RERADIATION	< -50 dBm	< -50 dBm
ADJACENT CHANNEL REJECTION	> 35 dB @ 30 MHz OFFSET PER <8%	> 35 dB @ 30 MHz OFFSET PER <5%
POWER	3.3,5V 1.5W (RX MODE)	3.3,5V,700mW

FIG. 268

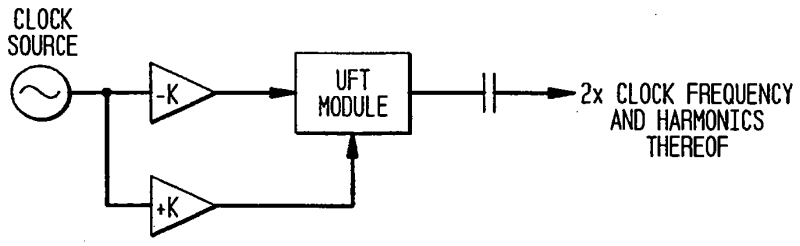


FIG. 269

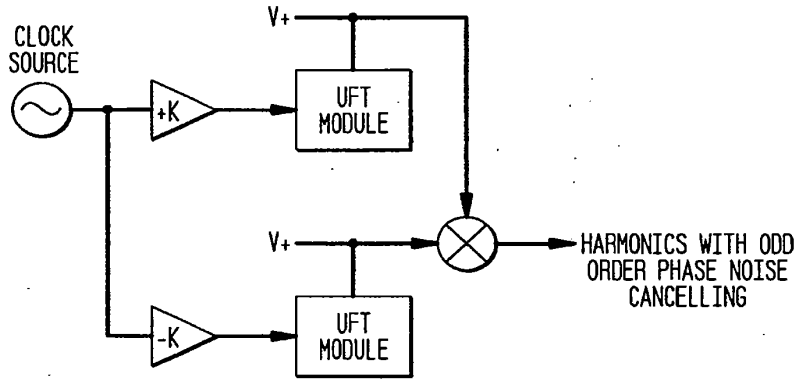


FIG. 270

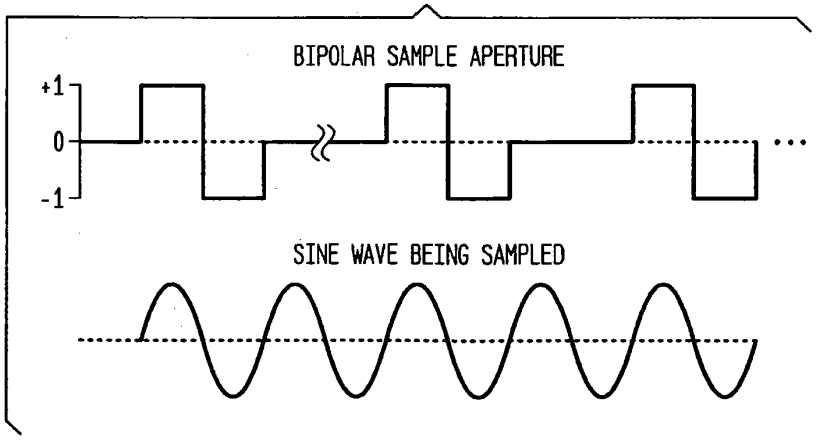


FIG. 271

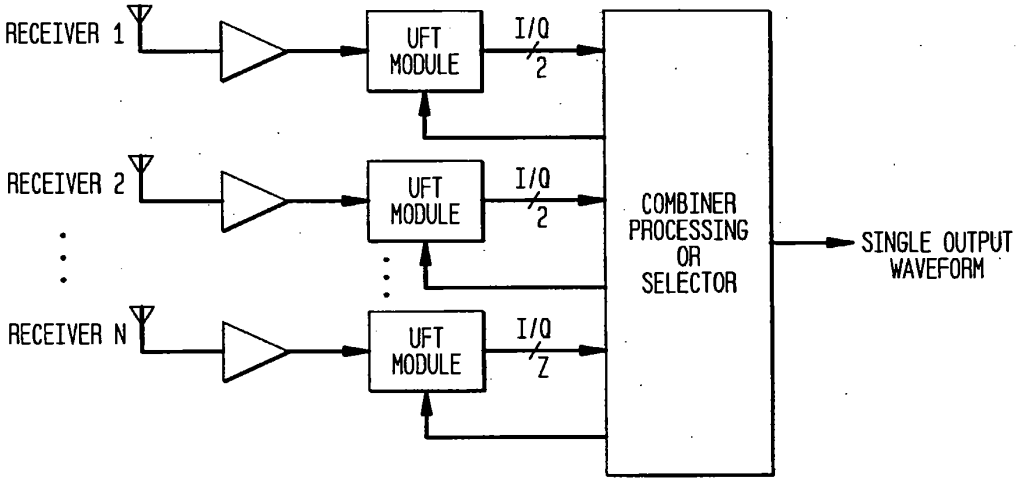


FIG. 272

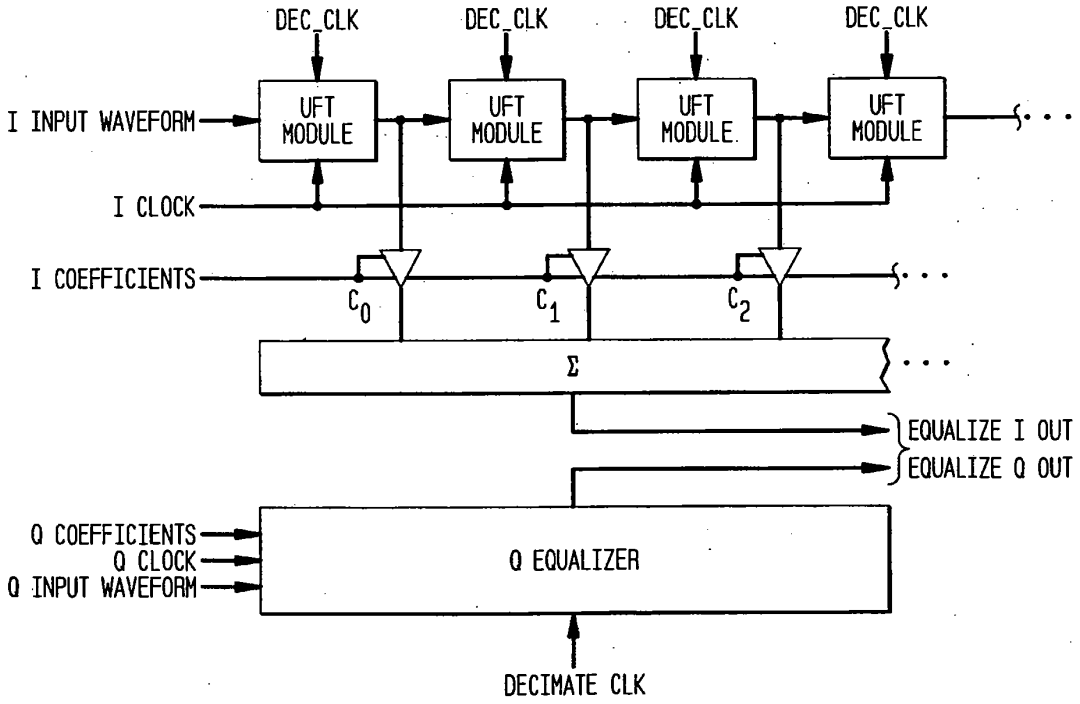


FIG. 273

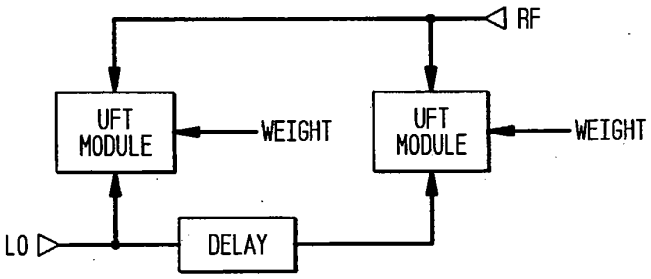


FIG. 274

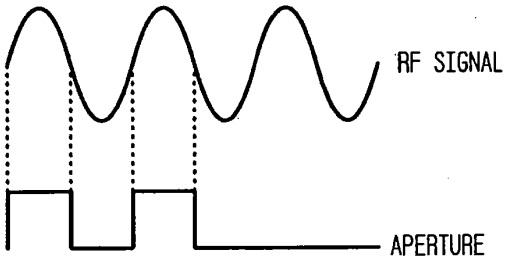


FIG. 275

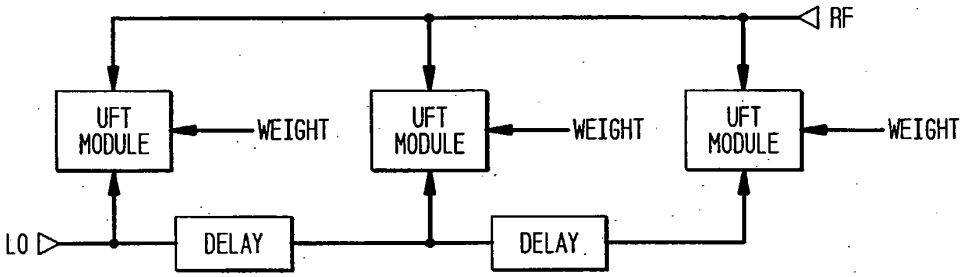


FIG. 276

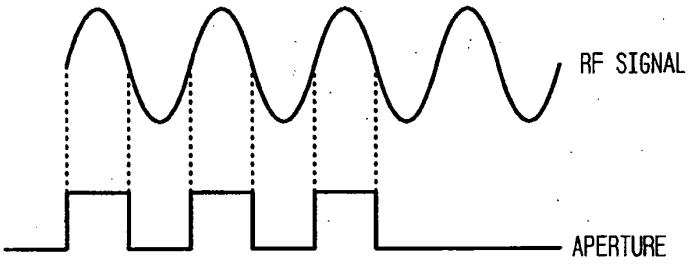


FIG. 277

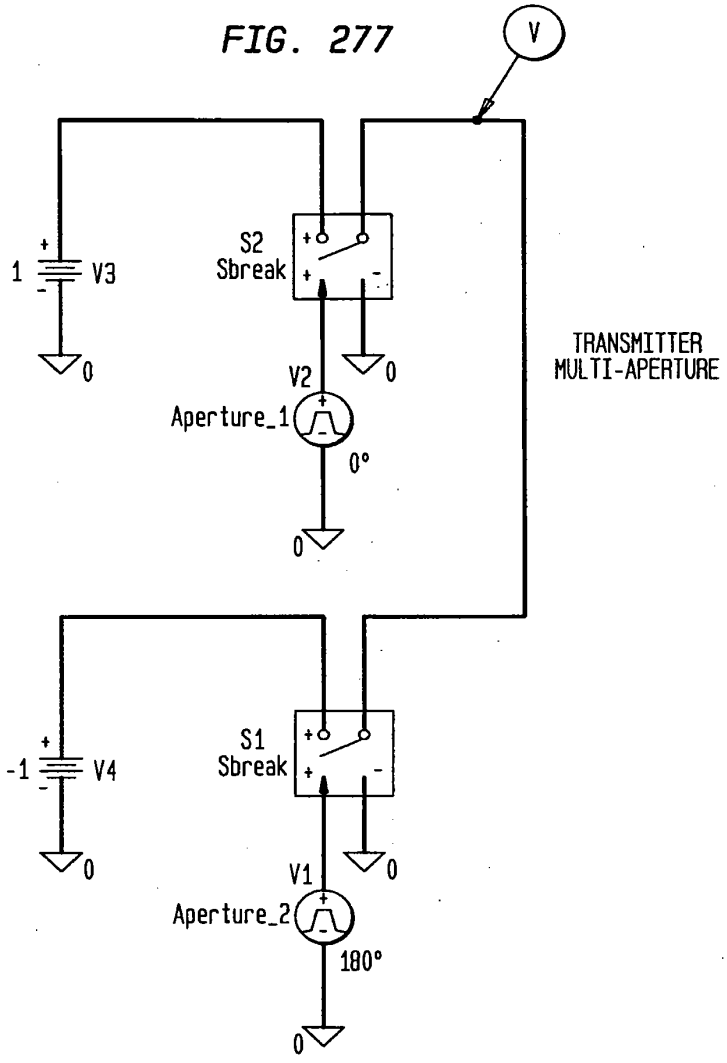

V
1
V3
0
S2
Sbreak
V2
Aperture_1
0°
0
0
TRANSMITTER
MULTI-APERTURE
-1
V4
0
S1
Sbreak
V1
Aperture_2
180°
0
0

FIG. 278

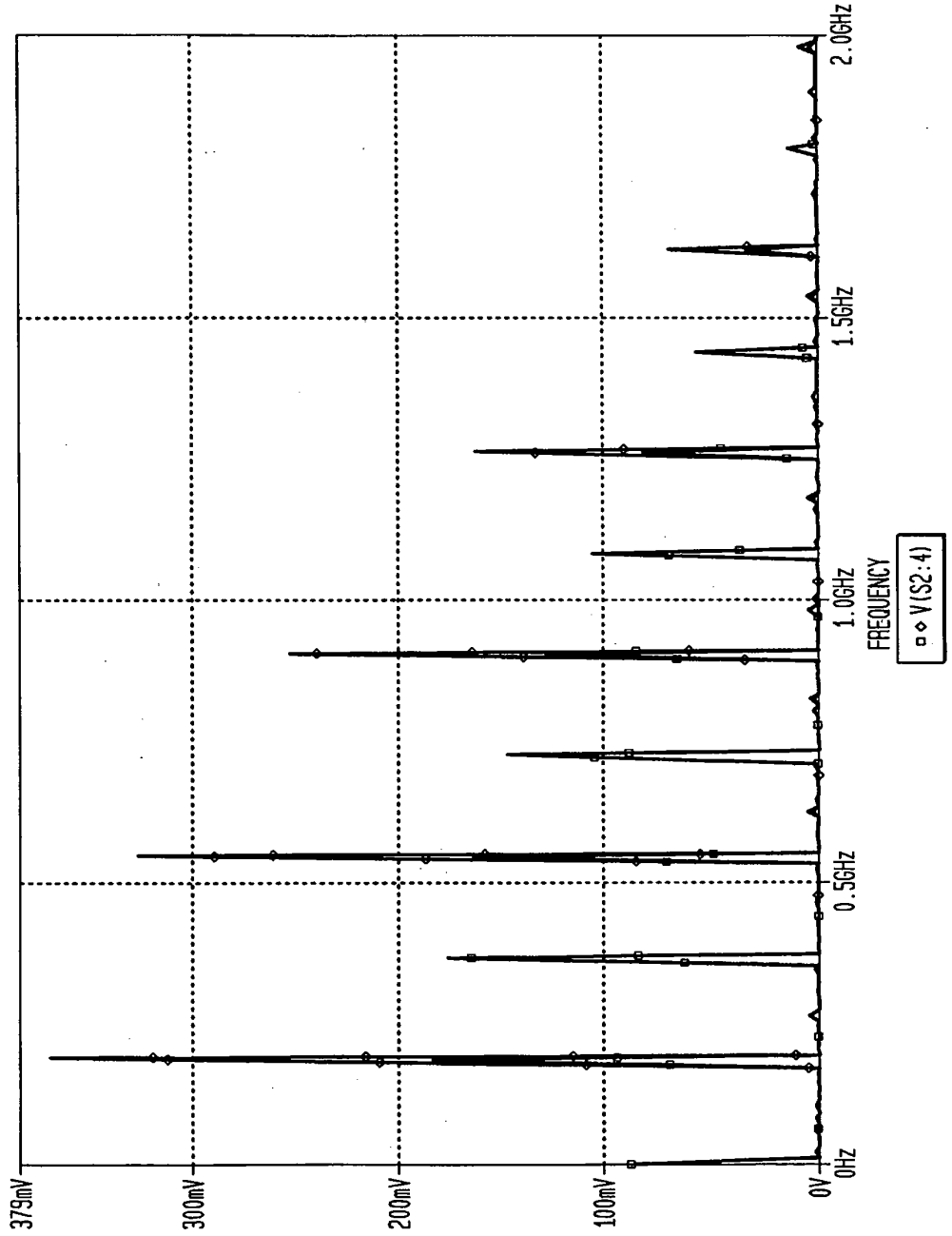

379mV
300mV
200mV
100mV
0V
0Hz
0.5GHz
1.0GHz
1.5GHz
2.0GHz
FREQUENCY
V(S2:4)

FIG. 279

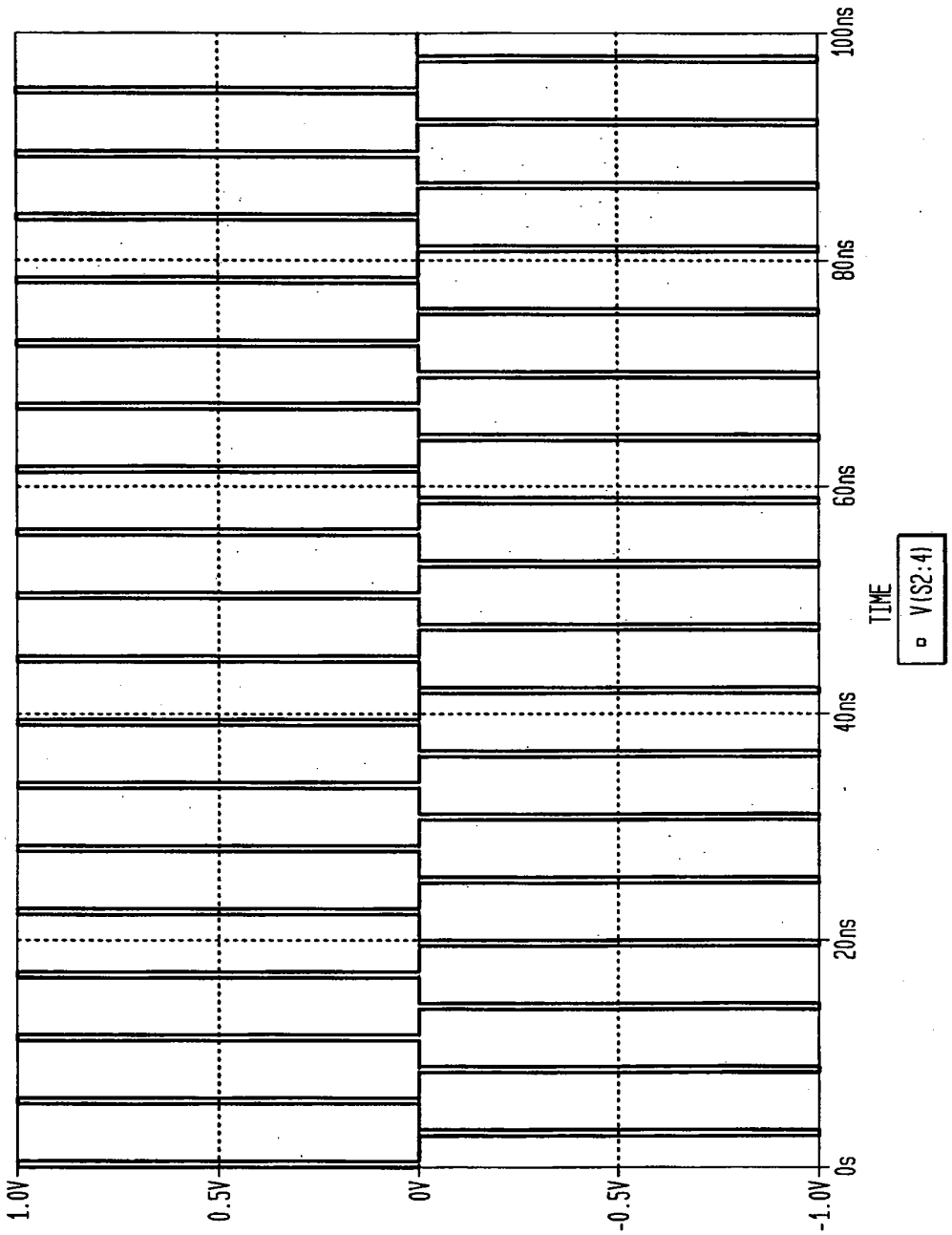


FIG. 280

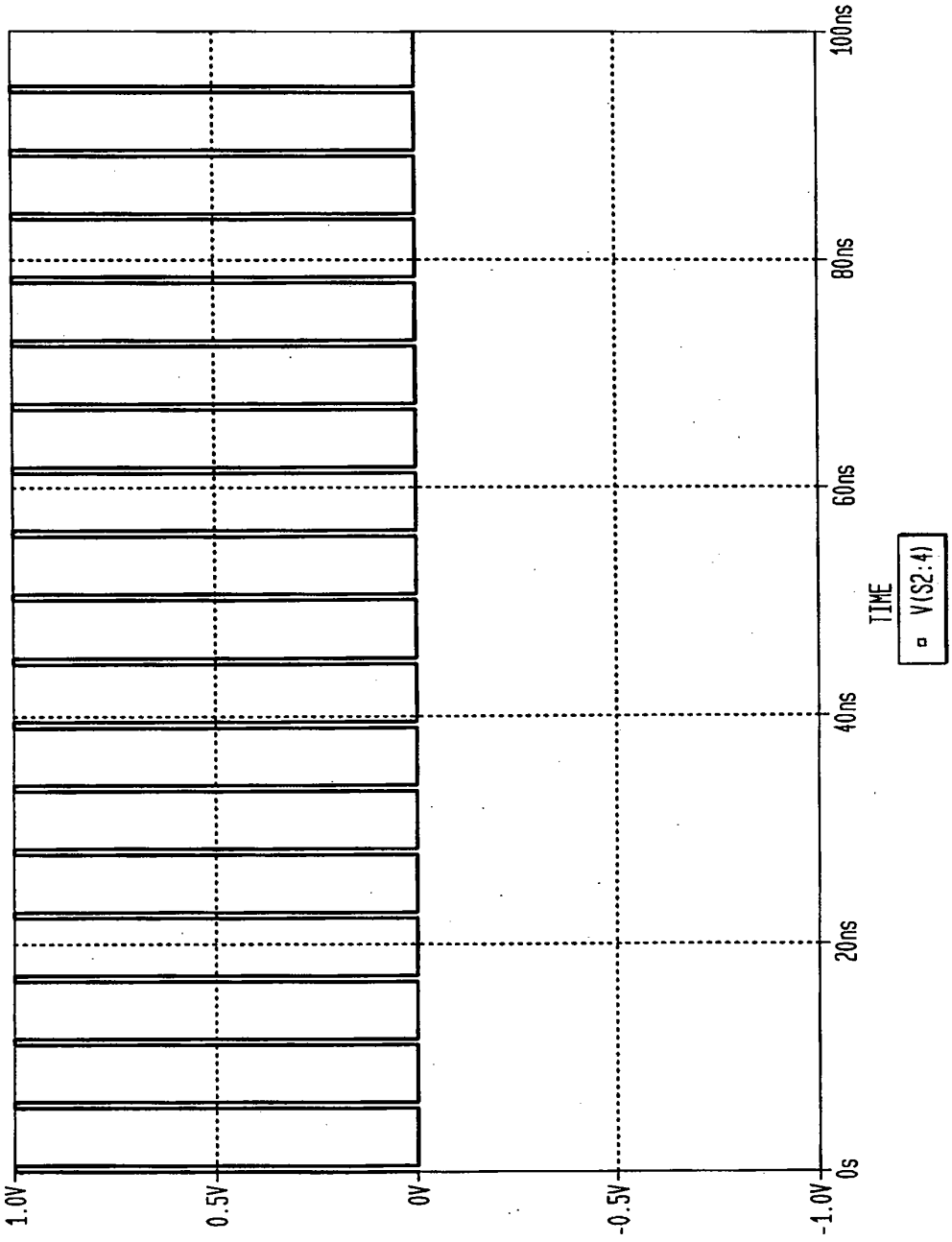
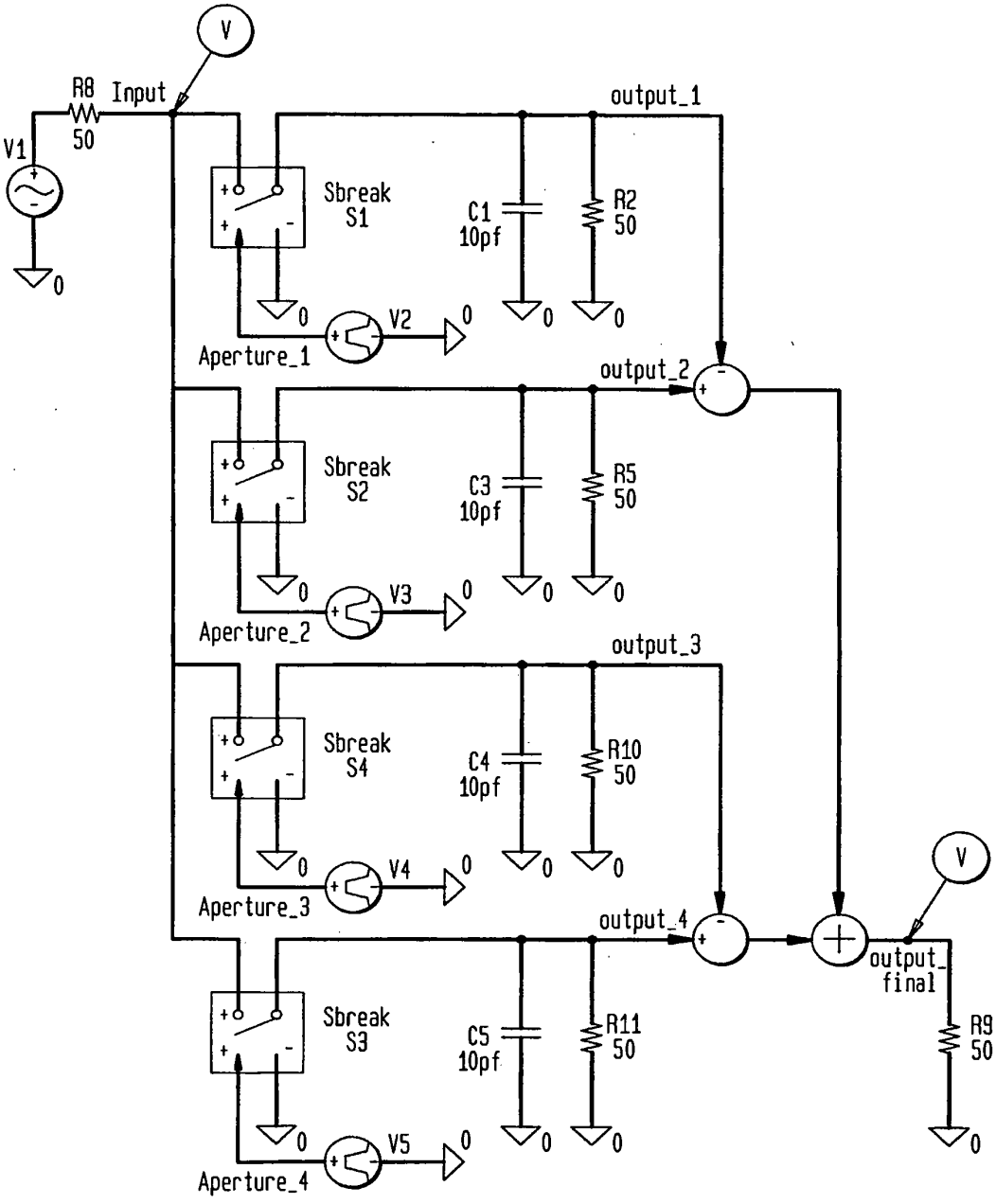


FIG. 281

MULTIPLE APERTURE RECEIVER IMPLEMENTATION



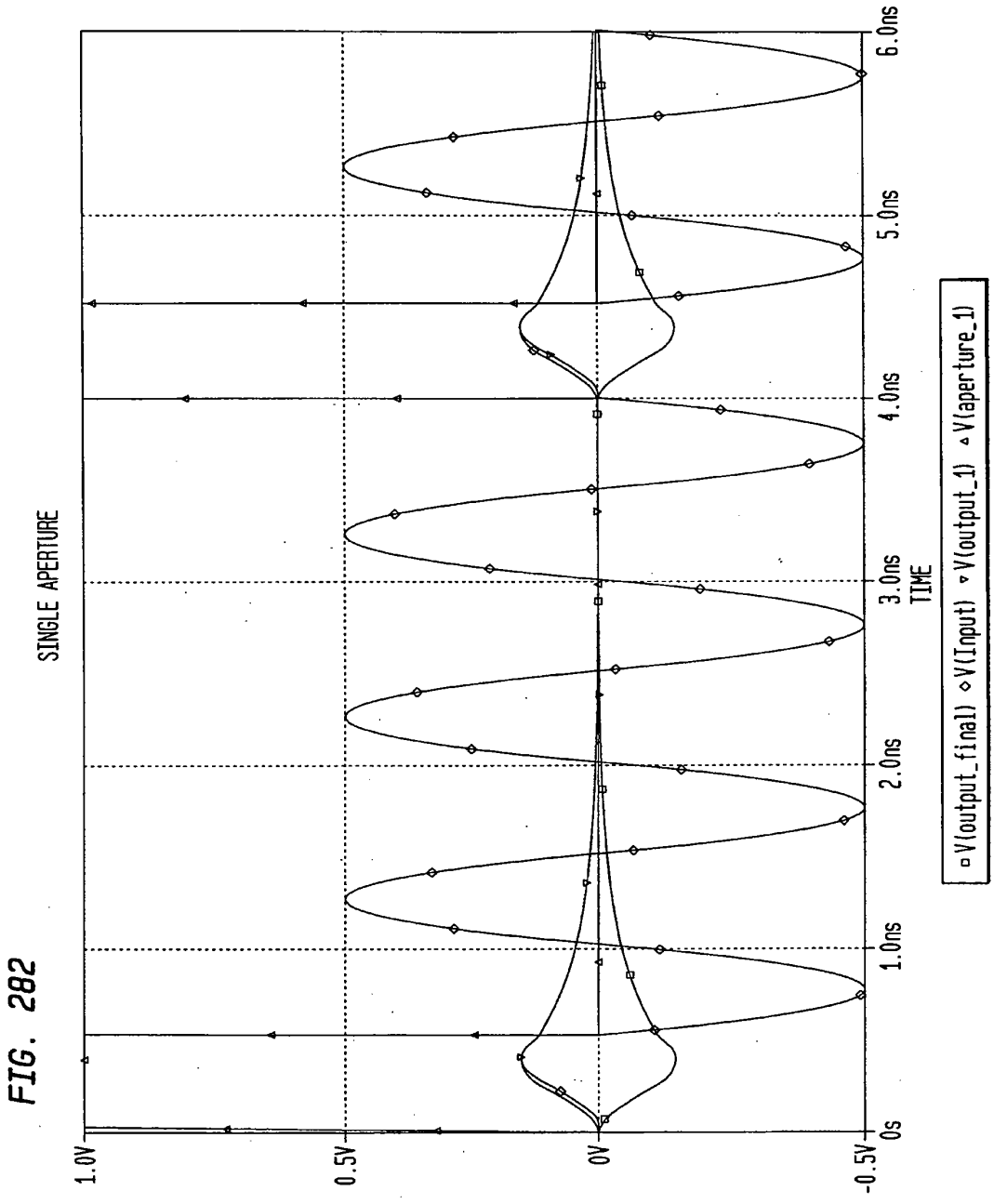

SINGLE APERTURE
1.0V
0.5V
0V
-0.5V
0s
1.0ns
2.0ns
3.0ns
4.0ns
5.0ns
6.0ns
TIME
V(output_final)
V(Input)
V(output_1)
V(aperture_1)

FIG. 282

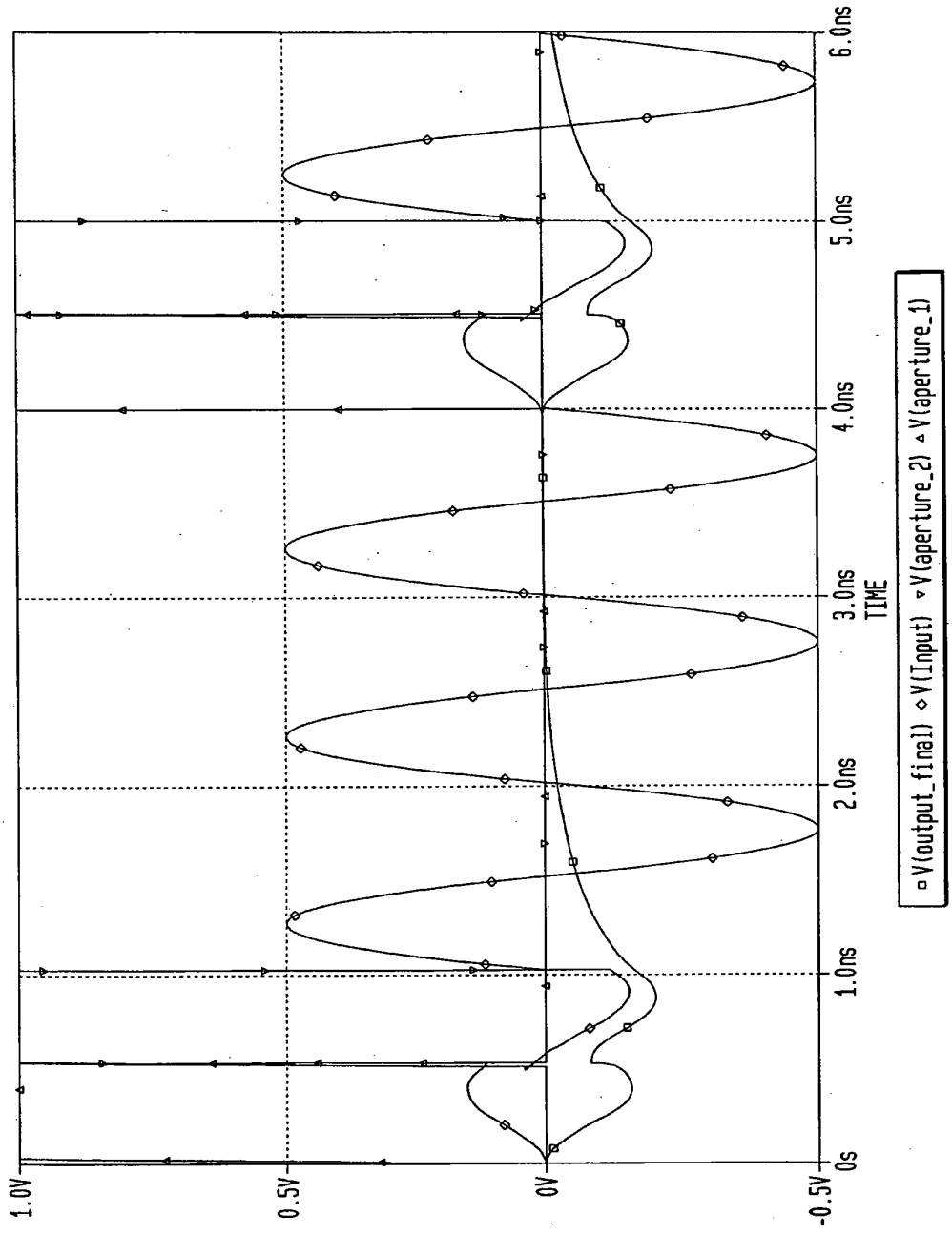

DUAL APERTURE
1.0V
0.5V
0V
-0.5V
0s
1.0ns
2.0ns
3.0ns
4.0ns
5.0ns
6.0ns
TIME
V(output_final)
V(Input)
V(aperture_2)
V(aperture_1)

FIG. 283

FIG. 284

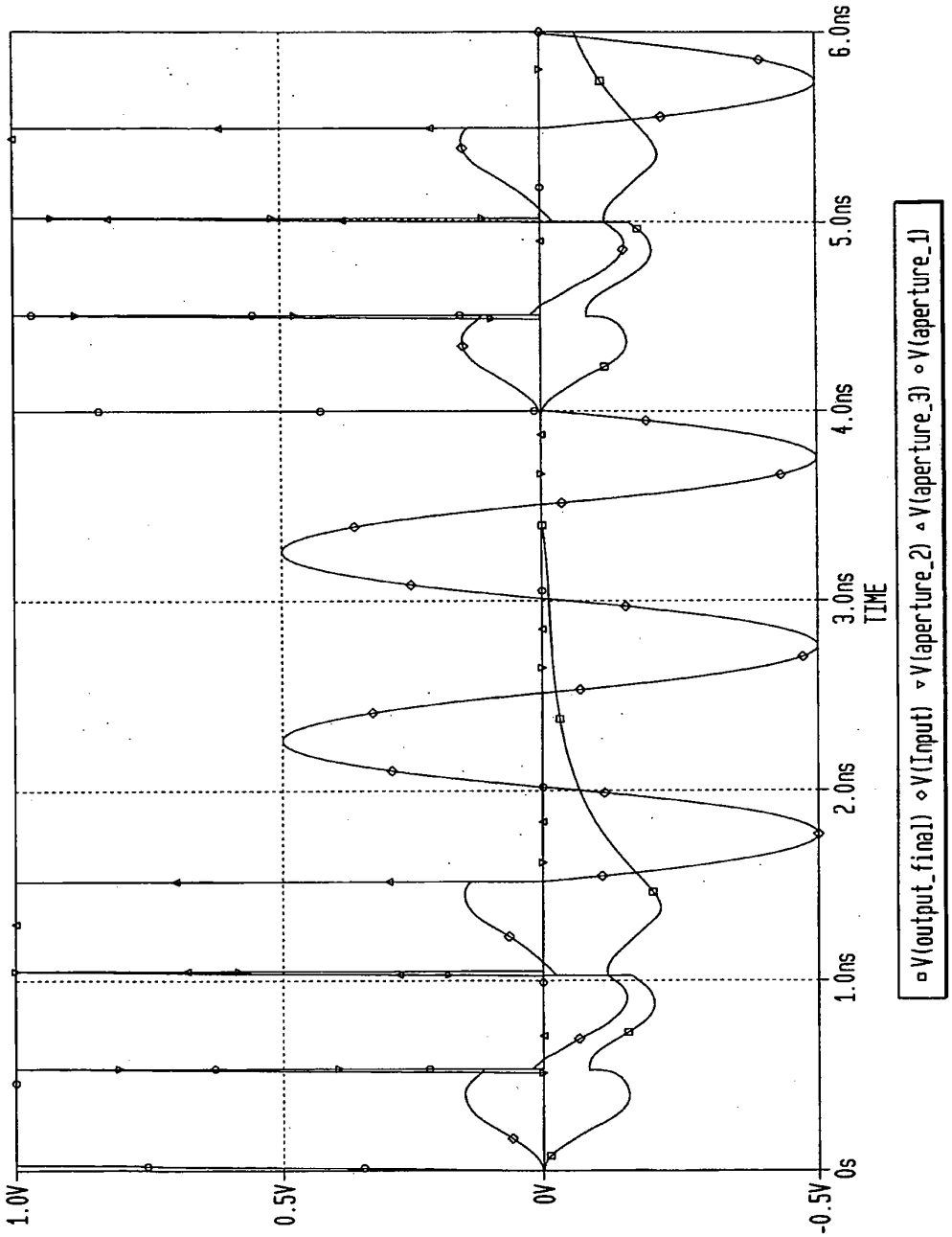
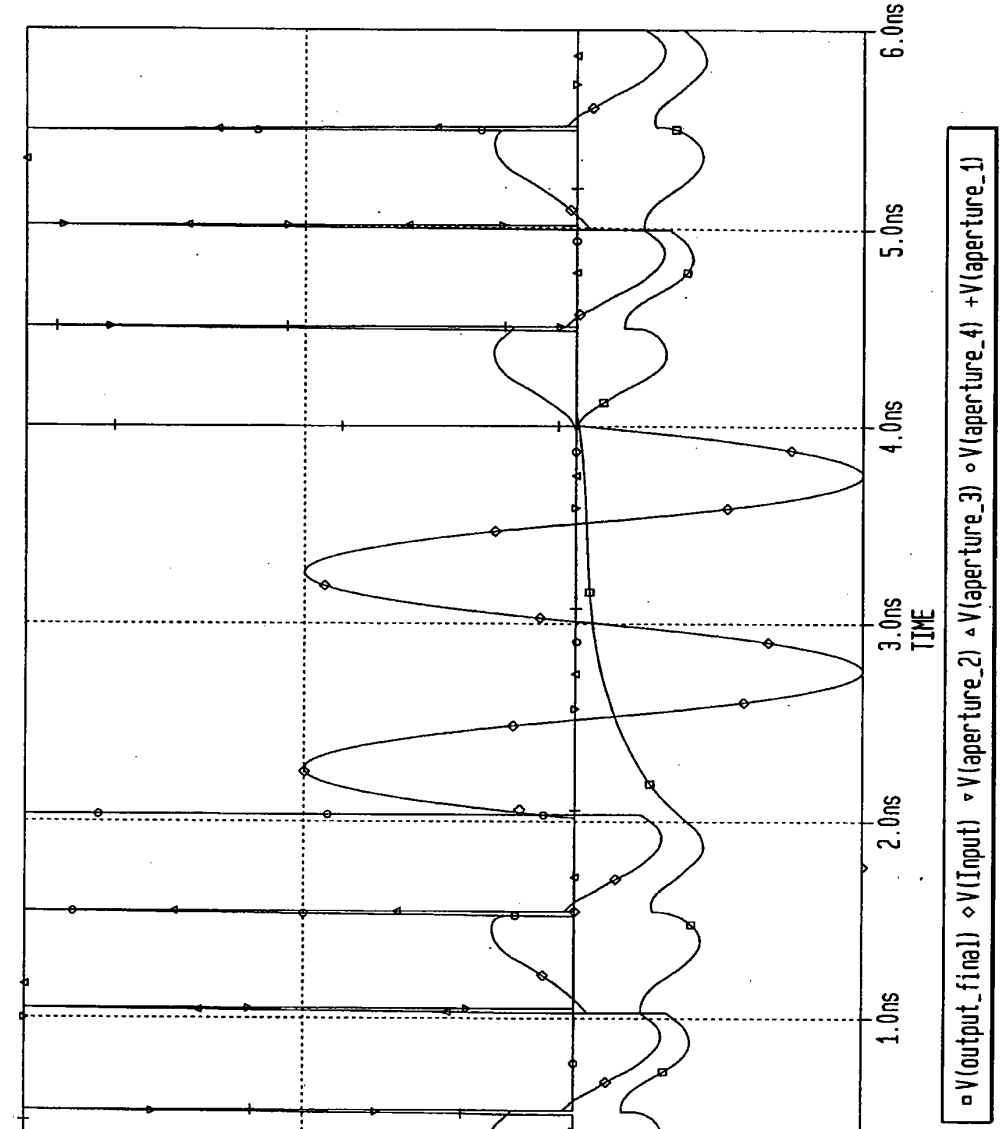

TRIPLE APERTURE
1.0V
0.5V
0V
-0.5V
0s
1.0ns
2.0ns
3.0ns
4.0ns
5.0ns
6.0ns
TIME
V(output_final)
V(Input)
V(aperture_2)
V(aperture_3)
V(aperture_1)

FIG. 285


QUAD APERTURE
1.0V
0.5V
0V
-0.5V
0s
1.0ns
2.0ns
3.0ns
4.0ns
5.0ns
6.0ns
TIME
V(output_final) V(Input) V(aperture_2) V(aperture_3) V(aperture_4) +V(aperture_1)

Electronic Acknowledgement Receipt

EFS ID:	4569714
Application Number:	12349802
International Application Number:	
Confirmation Number:	5719
Title of Invention:	Method and System For Down-Converting An Electromagnetic Signal, And Transforms For Same, And Aperture Relationships
First Named Inventor/Applicant Name:	David F. SORRELLS
Customer Number:	26111
Filer:	Michael Q. Lee/Brandei Davis
Filer Authorized By:	Michael Q. Lee
Attorney Docket Number:	1744.001000P
Receipt Date:	07-JAN-2009
Filing Date:	
Time Stamp:	15:20:38
Application Type:	Utility under 35 USC 111(a)

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1		1744001000Pnewapplicationfiling.pdf	535354 8919cfaa731d00ba22c02e42cd3708856a739a41	yes	16

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	3
	Transmittal of New Application	4	5
	Authorization for Extension of Time all replies	6	6
	Application Data Sheet	7	12
	Oath or Declaration filed	13	16

Warnings:					
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2	Specification	1744001000Pspecification.PDF	1388823 def1cdad41efd7b41e06ee3597eef6acc6c96805	no	372
Warnings:					
Information:					
3	Drawings-only black and white line drawings	1744FiguresDivisional.pdf	4905010 bd11bdd1620a9aa9957a2fbaa15c4c75e3a1d752	no	284
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Information:					
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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January 7, 2009

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Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: U.S. Non-Provisional Utility Patent Application under 37 C.F.R. § 1.53(b)
(Divisional of Appl. No. 09/550,644; Filed April 14, 2000)
Appl. No. To Be Assigned; Filed: January 7, 2009
For: **Method And System For Down-Converting An Electromagnetic Signal, And Transforms For Same, And Aperture Relationships**
Inventors: SORRELLS *et al.*
Our Ref: 1744.001000P

Sir:

The following documents are transmitted herewith for appropriate action by the U.S. Patent and Trademark Office:

1. Utility Patent Application Transmittal Form (PTO/SB/05);

2. Authorization to Treat a Reply As Incorporating An Extension of Time Under 37 C.F.R. § 1.136(a)(3);

3. U.S. Utility Patent Application entitled:

Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same, and Aperture Relationships

and naming as inventors:

David F. SORRELLS
Michael J. BULTMAN
Robert W. COOK
Richard C. LOOKE
Charley D. MOSES JR.

Gregory S. RAWLINS
Michael W. RAWLINS

the application consisting of:

a. An Application Data Sheet (37 C.F.R. § 1.76);

b. A copy of the executed combined Declaration and Power of Attorney, as originally filed in U.S. Appl. No. 09/550,644;

c. A specification containing:

i. Three-hundred and sixty-eight **(368)** pages of description prior to the claims;

ii. Three **(3)** pages of claims (12) claims;

iii. A one **(1)** page abstract;

d. Two-hundred and eighty-four **(284)** sheets of drawings: (Figures 1-4, 5A-5C, 6A-6C- 7A-7C, 8A-8C, 9A-9C, 10A-10C, 11, 12A-12D, 12, 14A-14D, 15A-15E, 16, 17, 18A-18E, 19A-19E, 20A-20E, 21A-21E, 22A-22E, 23A-23E, 24A-24C, 25A-25H, 26A026B, 27, 28A-28D, 29A-29L, 30, 31A-31C, 32A-32C, 33A-33D, 34A-34F, 35A-35E, 36A-36E, 38A-38E, 39A-39D, 40A-40E, 41A-41E, 42, 43, 44A-44E, 45A-45B, 46A-46D, 47A-47E, 48, 49A-49H, 50A-50G, 51A-51G, 52A-52G, 53A-53G, 54A-54G, 55A-55G, 56A-56D, 57A-57F, 58A-58F, 59A-59F, 60A-60F, 61A-6F, 63, 64A-64B, 65, 66A-66D, 67A-67C, 68A-68L, 69-70, 71A-71C, 72-74, 75A-75F, 76A-76E, 77A-77C, 78A-78B, 79A-7F, 80A-80F, 81A-81F, 82A-82B, 83A-83F, 84A-84D, 85A-85C, 86-93, 94A-94C, 95-97, 98A-98F, 99-106, 107A-107B, 108A-108B, 109A-109F, 110A-110B, 111A-111C, 112, 113A-113E, 114-123, 124A-124J, 125, 126A-126Q, 127A-127Q, 128A-128C, 129A-129Q, 130-163, 164A-164C, 165-177, 178A-178B, and 179-213, 214, 215, 216, 217, 218A-218E, 219-285);

The above-listed documents are filed electronically through EFS-Web.

This patent application is being submitted under 37 C.F.R. § 1.53(b) without filing fee.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael Q. Lee
Attorney for Applicants
Registration No. 35,239

MQL/VDT:bad
Enclosures

921323_1.DOC

PTO/SB/06 (12-04)

Filing Date: 01/07/09

Approved for use through 7/31/2006. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/349,802

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	**330**
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	**540**
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	**220**
TOTAL CLAIMS (37 CFR 1.16(i))	**12** minus 20 =		x$26		OR	x$52	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	**1** minus 3 =	*	x$110			x$220	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $270 ($135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			195			390	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	**1090**

APPLICATION AS AMENDED – PART II

AMENDMENT A		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDI-TIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDI-TIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

AMENDMENT B		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDI-TIONAL FEE ($)	OR	RATE ($)	ADDI-TIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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