IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	David F. Sorrells, et al	Attorney Docket No.: 12189-0091IP1
U.S. Patent No.:	7,865,177	
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Appl. Serial No.:	12/349,802	
Filing Date:	January 7, 2009	
Title:	METHOD AND SYSTEM FOR DOWN-CONVERTING AN ELECTROMAGNETIC SIGNAL, AND TRANSFORMS FOR SAME, AND APERTURE RELATIONSHIPS	

DECLARATION OF IAN GALTON, PH.D.

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LISTING OF CLAIM TERMS

Claim No.	Claim Element
14.P	A method for down-converting an electromagnetic signal, comprising:
14.1	receiving an input signal at a first matched filtering/correlating module;
14.2	down converting said input signal at said first matched filtering/correlating module according to a first control signal and outputting a first down-converted signal;
14.3	receiving said input signal at a second matched filtering/correlating module;
14.4	down-converting said input signal at said second matched filtering/correlating module according to a second control signal and outputting a second down-converted signal; and
14.5	combining said second down-converted signal and said first down-converted signal to output a first channel down-converted signal.

I, Dr. Ian Galton of La Jolla, CA, declare that:

I. ASSIGNMENT

1. I have been retained by Fish & Richardson P.C. as an independent expert on behalf of Petitioner Texas Instruments ("TI"). I understand that TI is petitioner in an *inter partes* review ("IPR") of U.S. Patent No. 7,865,177 ("the '177 patent") (EX1001) before the Patent Trial and Appeal Board ("PTAB" or "Board"). I understand the '177 patent is assigned to Patent Owner ParkerVision, Inc. ("ParkerVision"). I have been asked to provide my independent analysis of the '177 patent in light of the materials cited below and my knowledge and experience in this field during the relevant period. I have been asked to consider what a person of ordinary skill in the art (POSITA) at the time of the alleged invention of the '177 patent would have understood from the teachings of the '177 patent, including scientific and technical knowledge related to the '177 patent

2. I am not, and never have been, an employee of TI. I am being compensated at my standard consulting rate for my time providing my independent analysis, plus reasonable out-of-pocket expenses. I have received no additional compensation for my work in this matter, and my compensation does not depend upon the content of my opinions, any testimony that I may provide, or the ultimate outcome of the matter. All of the opinions set forth in this declaration are my own.

II. BACKGROUND AND QUALIFICATIONS

3. I am currently a Professor of Electrical Engineering at the University of California at San Diego (UCSD) where I manage the Integrated Signal Processing Group. My qualifications for formulating my analysis on this matter are summarized here with full descriptions of my educational background, professional work, qualifications, and publications set forth more fully in my *curriculum vitae*, which is attached to this declaration as Appendix A.

4. I received my Bachelor of Science in Electrical Engineering from Brown University in Providence, RI in 1984. I received my Masters and Ph.D. in Electrical Engineering from the California Institute of Technology in 1989 and 1992, respectively.

5. After receiving my B.S. degree, I worked as a design engineer at Mindset Corporation in Sunnyvale, CA, which was an early innovator in the personal computer market, from 1984 to 1985. I then worked as a design engineer at Mead Data Central in Menlo Park, CA, a leading database service responsible for services such as LEXIS and NEXIS, from 1985 to 1986. From 1986 to 1988 I worked as a design engineer for Acuson, Inc. in Mountain View, CA which leveraged current developments in computing technology to improve diagnostic ultrasound technology.

6. After receiving my Ph.D. in 1992 I began teaching at the University of California at Irvine as an Assistant Professor of Electrical Engineering before

moving to UCSD in 1996, initially joining as a tenured Associate Professor of Electrical Engineering prior to my current position as a tenured Professor of Electrical Engineering. I currently hold the "Skyworks Endowed Chair in High Performance Communications Devices and Circuits." My work at UCSD includes teaching and conducting research in the field of mixed-signal integrated circuits and systems for communications. My work with the Integrated Signal Processing Group at UCSD includes leading graduate and post-doctorial students in developing enabling technology for highly-integrated, high-performance, low-cost, communication systems. The research involves the invention, development, analysis, and proof-of-principle integrated circuit (IC) implementation of key communication system blocks such as data converters and frequency synthesizers. The emphases of the research are on the development of new digital signal processing techniques and new digital-like analog circuits that exploit the strengths of advanced IC technology to mitigate the effects of non-ideal analog circuit behavior in mixed-signal and radio frequency ICs.

7. In addition to my teaching and academic research responsibilities at UCSD, I regularly consult at several semiconductor companies and teach industry-oriented short courses on the design of mixed-signal integrated circuits. I am a Fellow of the IEEE, and have served on a corporate Board of Directors, on several corporate Technical Advisory Boards, as the Editor-in-Chief of the IEEE

Transactions on Circuits and Systems II: Analog and Digital Signal Processing, as a member of the IEEE Solid-State Circuits Society Administrative Committee, as a member of the IEEE Circuits and Systems Society Board of Governors, as a member of the IEEE International Solid-State Circuits Conference Technical Program Committee, and as a member of the IEEE Solid-State Circuits Society Distinguished Lecturer Program.

8. I have authored or co-authored well over 100 scientific papers in peer-reviewed academic journals and conferences. I am also a named inventor on 25 issued U.S. Patents. I have received numerous awards from leading organizations in the area of Electrical Engineering, including IEEE. A complete list of my publications, patents, awards, and recognitions is included in my CV (Appendix A).

9. In addition to gaining expertise via my academic training, professional experiences, and research accomplishments described above, I have kept abreast of the field of RF and other mixed-signal integrated circuits specifically and electrical engineering in general by reading technical literature, attending and presenting at conferences, and attending and presenting at symposia. I have been invited to participate in the peer review process for various technical journals, and conferences, and have reviewed manuscripts submitted by other engineers relating

to integrated circuit design and communications technology. Furthermore, I have collaborated with or have communicated with many other engineers in the field.

III. MATERIALS REVIEWED AND CONSIDERED

10. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field of the art, and have considered the viewpoint of a POSITA at the time of the alleged invention. I have also reviewed and considered the documents listed in the Exhibit List of this declaration. Although this declaration refers to selected portions of the cited references for the sake of brevity, it should be understood that these are examples, and that a POSITA would have viewed the references cited herein in their entirety and in combination with other references cited herein or cited within the references themselves. The references used in this declaration, therefore, should be viewed as being considered herein in their entireties.

11. Specifically, I have analyzed the following publications and materials, in addition to other materials I cite in my declaration:

- U.S. Patent No 7,865,177 (Exhibit 1001), and its accompanying prosecution history (Exhibit 1002)
- U.S. Patent No. 6,230,000 ("Tayloe") (TI-1004)

- SN74CBT3253 Dual 1-of-4 FET Multiplexer/Demultiplexer Datasheet (TI-1005)[1]
- Razavi, *A 900-MHz CMOS Direct Conversion Receiver* ("Razavi") (TI-1017)
- Uzunoglu et al., *The Synchronous Oscillator: A Synchronization and Tracking Network* ("Uzunoglu") (TI-1026)

12. Each of these foregoing article references indicate on their face that they were published in journals or conference proceedings that I am familiar with, and which would have been available to and disseminated to members of the general technical community prior to October 21, 1998. My understanding is that the TI Demux datasheet was available on TI's website as early as July 28, 1998.

IV. LEGAL UNDERSTANDING

13. I understand that issues such as invalidity and claim construction are analyzed based on certain legal standards. Counsel for TI has provided me with an

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[1] A POSITA reviewing Tayloe would have visited TI's website to find information pertaining to this mux/demux. I understand that TI datasheet was publicly accessible to those interested in the operation of TI products on TI's searchable website, beginning July 28, 1998.

understanding of these standards, and I have applied them in my analysis set forth in this declaration.

A. Anticipation

14. I have been informed that a patent claim is invalid as anticipated under 35 U.S.C. § 102 if each and every element of a claim, as properly construed, is found either explicitly or inherently in a single prior art reference. Under the principles of inherency, if the prior art necessarily functions in accordance with, or includes the claimed elements, it anticipates.

15. I have been informed that a claim is invalid under 35 U.S.C. § 102(a) if the claimed invention was known or used by others in the U.S., or was patented or published anywhere, before the Applicant's invention. I further have been informed that a claim is invalid under 35 U.S.C. § 102(b) if the invention was patented or published anywhere, or was in public use, on sale, or offered for sale in this country, more than one year prior to the filing date of the patent application (critical date). And a claim is invalid, as I have been informed, under 35 U.S.C. § 102(e), if an invention described by that claim was described in a U.S. patent granted on an application for a patent by another that was filed in the U.S. before the date of invention for such a claim.

B. Obviousness

16. I have been informed that a patent claim is invalid as "obvious" under 35 U.S.C. § 103 in light of one or more prior art references if it would have been obvious to a person of ordinary skill in the art at the time of the alleged invention ("POSITA"), taking into account (1) the scope and content of the prior art, (2) the differences between the prior art and the claims, (3) the level of ordinary skill in the art, and (4) any so called "secondary considerations" of non-obviousness, which include: (i) "long felt need" for the claimed invention, (ii) commercial success attributable to the claimed invention, (iii) unexpected results of the claimed invention, and (iv) "copying" of the claimed invention by others. For purposes of my analysis here, I have applied a date of October 21, 1998, as the date of the alleged invention in my obviousness analyses, although in many cases the same analysis would hold true even if the date of the alleged invention occurred earlier than February 2004 (especially given the earlier publication or filing dates of the prior art in Exhibits TI-1004, TI-1005, TI-1017, and TI-1026 as described below).

17. I have been informed that a claim can be obvious in light of a single prior art reference or multiple prior art references. To be obvious in light of a single prior art reference or multiple prior art references, there must be a reason that would have prompted a POSITA to modify the single prior art reference, or combine two or more references, in a manner that provides the elements of the claimed invention. This reason may come from a teaching, suggestion, or

motivation to combine, or may come from the reference(s) themselves, the knowledge or "common sense" of a POSITA, or from the nature of the problem to be solved, and this reason may be explicit or implicit from the prior art as a whole. I have been informed that, under the law, the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand it is improper to rely on hindsight in making the obviousness determination.

C. Claim Construction

18. I have been informed by counsel that, for purposes of my analysis in this *inter partes* review proceeding, the terms appearing in the patent claims should be interpreted according to their "ordinary and customary meaning." In determining the ordinary and custom meaning, the words of a claim are first given their plain meaning that those words would have had to a POSITA. I understand that the structure of the claims, the specification, and the file history also may be used to better construe a claim insofar as the plain meaning of the claims cannot be understood. Moreover, treatises and dictionaries may be used, albeit under limited circumstances, to determine the meaning attributed by a POSITA to a claim term at the time of filing. I have followed this approach in my analysis.

19. I also understand that the words of the claims should be interpreted as they would have been interpreted by a POSITA at the time the alleged invention was made (not today).

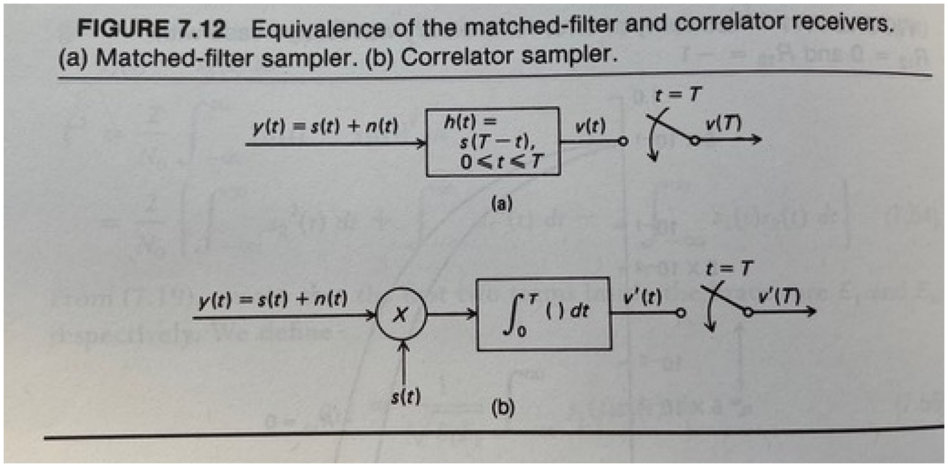
20. I have been informed by counsel that, for purposes of my analysis in this *inter partes* review proceeding, the terms appearing in the patent claims should be interpreted according to their "ordinary and customary meaning." In determining the ordinary and custom meaning, the words of a claim are first given their plain meaning that those words would have had to a POSITA. In that regard, I understand that the best indicator of claim meaning is its usage in the context of the patent specification as understood by a POSITA. I also understand that the words of the claims should be interpreted as they would have been interpreted by a POSITA at the time of the invention was made (not today). Because I do not know at what date the invention as claimed was made, I have used the earliest priority date of U.S. Patent No 7,865,177 as the point in time for claim interpretation purposes. That date was October 21, 1998. I have been asked to provide my interpretation of the following terms and phrases of the '177 patent set forth below. Claim 14 recites:

> A method for down-converting an electromagnetic signal, comprising:
> receiving an input signal at a first matched filtering/correlating module;
> down converting said input signal at said first matched filtering/correlating module according to a first control signal and outputting a first down-converted signal;

receiving said input signal at a second matched filtering/correlating module;
down-converting said input signal at said second matched filtering/correlating module according to a second control signal and outputting a second down-converted signal; and
combining said second down-converted signal and said first down-converted signal to output a first channel down-converted signal.

21. Claim 14 hinges on the definition of "matched filtering/correlating module" which is currently in dispute between the parties. The following is my analysis of the meaning of this claim term as implied by the specification in the context of the accepted meaning of "matched filter" and "correlator" to a POSITA at the time of the priority date.

22. The term "matched filter" was well-known to a POSITA at the time of the priority date. It was also well-known to a POSITA at that time that a matched filter can be implemented equivalently as either a linear time-invariant filter followed by a sampling operation or as a "correlator" followed by a sampling operation. Therefore, both terms had conventional meanings at the time of the priority date. For example, *see* Fig. 7.12 in the well-known communication textbook: Ziemer, Tranter, "Principles of Communications: Systems, Modulation, and Noise," Fourth Ed., John Wiley and Sons, 1995:



The explanations provided in the ’177 patent are consistent with the conventional meanings of “matched filter” and “correlator.” For example, Column 130 of ’177 states: “As will be apparent to persons skilled in the relevant arts based on the teachings contained herein, the description of the present invention contained herein is a unique and specific application of matched filter theory … .” This statement implies that a POSITA would recognize that the invention is an application of the pre-existing body of theory related to matched filters. Column 130 of '177 also states: “Embodiments of the present invention down-convert an electromagnetic signal by repeatedly performing a matched filtering or correlating operation on a received carrier signal.” The statement uses the word “or” in “a matched filtering <u>or</u> correlating operation,” which is consistent with the result depicted in Fig. 7.12 of the 1995 Zeimer and Tranter textbook that the operations of “matched filtering” and “correlating” are equivalent with respect to their input-output functionality. Furthermore, numerous figures and other comments in ’177

are consistent with the assertion that the term "Matched Filtering/Correlating Module" relates to the body of prior-art knowledge at the time of the priority date.

23. However, Column 132 of '177 patent states: "As will be apparent to persons skilled in the relevant arts given the discussion herein, the present invention is not a traditional realization of a matched filter/correlator." This is true for the following reasons:

24. The $s(t)$ signal in Fig. 7.12b of the Zeimer and Tranter textbook is a replica of a received baseband data symbol *after* frequency down-conversion, whereas the corresponding signal in '177, denoted $S_i(t-\tau)$ in '177, is a portion of one period of the received signal's carrier signal *prior to* frequency down-conversion (i.e., a fixed portion of one period of the fundamental of the local oscillator that the transmitter which generated the received signal used to up-convert the baseband version of the transmitted signal prior to transmission). Therefore, the application of the "Matched Filtering/Correlating Module" in '177 is different than that of a typical matched filter or corresponding correlator. Nevertheless, as '177 points out, the body of knowledge of matched filters and corresponding correlators as known at the time of the priority date applies to the invention claimed by '177. For example, Column 129 of '177 "describes the operation of the present invention mathematically using matched filter theory …."

25. The ideal "Matched Filtering/Correlating Module" diagram shown in Fig. 171 differs from that shown in Fig. 7.12b of the Ziemer and Tranter textbook in that a) the order of the sampling switch and integration operations is swapped, and b) instead of sampling a specific value of its input signal each period, the switch in Fig. 171 passes the signal prior to the integrator for a duration T_A each period corresponding to the non-zero portion of the correlating signal $S_i(t-\tau)$. It can be verified that the output of the system of Fig. 171 at each time when the switch opens is equal to the corresponding output of the system of Fig. 7.12b of the Zeimer and Tranter textbook. The various down-converter embodiments of the "Matched Filtering/Correlating Module" described or alluded to in '177 implement this structure to varying degrees of accuracy, with the exception of the in-phase and quadrature down-converter embodiment (described below).

26. In some of the embodiments described in '177, the correlation waveform, $S_i(t-\tau)$, is approximated as a square pulse as opposed to a portion of the sinusoid. As correctly explained in '177, this does not significantly change the behavior or mathematical analysis of the system (so the body of knowledge of matched filters and corresponding correlators as known at the time of the priority date applies in this case too).

27. In some of the embodiments described in '177, the integration operation is approximated as an RC network. As correctly explained in '177, this

does not significantly change the behavior or mathematical analysis of the system (so the body of knowledge of matched filters and corresponding correlators as known at the time of the priority date applies in this case too).

28. In conventional matched filters and the corresponding correlators, the correlation signal, $s(t)$, is synchronous with the received signal, and, correspondingly, for most of the claimed down-converter invention embodiments described in '177, the correlation signal, $S_i(t-\tau)$, is synchronous with the received signal's carrier. For example, Column 145 of '177 states that "the example matched filter/correlator of FIG. 171 operates in synchronism with the half sine pulse $S_i(t)$ over the aperture T_A," and this "synchronism" is depicted in several of the figures in '177 including but not limited to Fig. 72, Fig. 157, Fig. 158, Fig. 162, Fig. 166, Fig. 182, Fig. 184, and Fig. 193.

29. The one exception mentioned in the specification is the "I/Q modem embodiment." It is an exception in that it does not have the above-mentioned requirement that $S_i(t-\tau)$ is synchronous with the received signal's carrier signal. However, the specification does not define the UFT block, in isolation, to be a "Matched Filtering/Correlating Module" (which is correct given that synchronism is a key feature of a matched filter/correlator), and when $S_i(t-\tau)$ is not synchronous with the received signal's carrier signal, then the desired receiver information must be extracted from the I and Q outputs together (which is not included in Claim 14).

As the specification correctly does not suggest that a UFT block is a "Matched Filtering/Correlating Module", and Claim 14 does not mention or otherwise relate to a UFT block or extraction of information from I and Q outputs, it is clear that Claim 14 and its use of the term "Matched Filtering/Correlating Module" does not refer to the "I/Q modem embodiment" mentioned in the specification.

30. ParkerVision's Proposed construction of "matched filtering/correlating module" is: "linear time-variant circuitry that samples a modulated RF (radio frequency) carrier signal at an aliasing rate using a switch with an independent control input driven by a control signal with a non-negligible, periodic aperture, such that the samples, having non-negligible available energy, are accumulated and transferred to a load while the switch is closed and discharged through the load while the switch is open, thereby transferring available real power from the modulated RF carrier signal to the load and producing a downconverted signal with enhanced signal-to-noise power ratio."

31. Unfortunately for ParkerVision, this construction is not consistent with the specification in that it has no relationship to matched filtering or correlating, yet Column 130 of '177 states: "As will be apparent to persons skilled in the relevant arts based on the teachings contained herein, the description of the present invention contained herein is a unique and specific application of matched filter theory …," Column 130 of '177 states: "Embodiments of the present

invention down-convert an electromagnetic signal by repeatedly performing a matched filtering or correlating operation on a received carrier signal," and Column 129 of '177 states that it "describes the operation of the present invention mathematically using matched filter theory …". Additional issues with ParkerVision's claim construction are: not all the embodiments of the invention presented in the specification satisfy: "discharged through the load while the switch is open" and the phrase "enhanced signal-to-noise power ratio" is ambiguous (enhanced relative to what?).

32. Instead, an appropriate claim construction for "matched filtering/correlating" module would be: "A device with one or more features which are similar to those of a Matched-filter/Correlator in the plain-and-ordinary meaning of the term, wherein one of the similar features is that the aperture window is periodically non-zero with a phase that is synchronous with the carrier of the received signal."

V. THE PERSON OF ORDINARY SKILL IN THE ART

33. I understand that a Person of Ordinary Skill in the Art ("POSITA") is a hypothetical person who is presumed to be aware of all pertinent prior art, thinks along conventional wisdom in the art, and is a person of ordinary creativity—not an automaton.

34. I understand the level of ordinary skill in the art is evaluated based on various factors, including: the level of education and work experience of persons in the field; the type of problems encountered in the field; and the sophistication of the technology at issue.

35. As of the ’177 patent’s alleged priority date (October 21, 1998), a POSITA would have had at least a bachelor’s degree in electrical engineering or a related subject and two or more years of experience in the field of electromagnetic (EM) circuit design. Less work experience may be compensated by a higher level of education, such as a master’s degree.

VI. SUMMARY OF OPINIONS

36. This expert Declaration explains the conclusions that I have formed based on my analysis. To summarize those conclusions:

- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claim 14 of the ’177 patent is obvious in view of Tayloe.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claim 14 of the ’177 patent is obvious in view of Razavi under ParkerVision’s construction.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that I believe that claim 14 of

the ’177 patent is obvious in view of the Razaiv-Uzunoglu combination under a plain-meaning construction.

VII. TECHNOLOGY BACKGROUND

37. In this section, I provide a high-level overview of technical concepts and design principles underlying direct conversion technology and the ’177 Patent.

A. Heterodyne Receivers

38. A received radio frequency (RF) signal has a frequency spectrum that is centered at the signal’s carrier frequency, e.g., 900 MHz, and is non-zero over a band of frequencies, e.g. 5 MHz, centered about the carrier frequency. The objective of the down-conversion process in a wireless receiver is to shift the spectrum of the RF signal so that it is centered about zero-frequency, a process which is sometimes, albeit infrequently, referred to as “removing the carrier.” The down-converted signal is typically referred to as the baseband signal. As the frequency spectrum of the RF signal has real and imaginary parts that are not necessarily conjugate symmetric about the carrier frequency, usually the baseband signal must be represented as a pair of signals, one corresponding the baseband signal’s real component and one corresponding to the baseband signal’s imaginary component. These two signals are typically called the in-phase and quadrature baseband signal components.

39. Unwanted RF signals with different carrier frequencies are usually present in the signal captured by the antenna, so it is necessary for a receiver to filter out these unwanted signals in addition to performing frequency down-conversion. Furthermore, the power of the signal at the antenna is usually extremely low, so the receiver must provide a large amount of amplification in addition to down-conversion and filtering operations.

40. Practical circuits used to process analog information-bearing signals often have small unwanted DC components arising from non-ideal circuit behavior. However, despite these DC components being small, they are often much larger than the received signal at the receiver's antenna output. Unfortunately, the large gains required in radio receivers have the potential to amplify these offsets so much that they overload the circuitry within the receiver, thereby rendering the receiver non-functional. This was a significant problem ever since the early days of wireless receivers, and it was solved in the early part of the 20th century by Edwin H. Armstrong with an invention called the heterodyne receiver. The gist of the idea is to first perform frequency down-conversion to a non-zero intermediate frequency (IF) along with filtering and amplification. As the desired signal after this initial frequency down-conversion step, known is the IF signal, occupies a frequency band centered at the IF and does not overlap zero-frequency, any DC offset can be removed without affecting the desired signal. Typically, the IF signal

is passed through a so-called bandpass filter centered at the IF to suppress unwanted received signals above and below the spectrum of the desired signal (including the DC component), and the result is frequency down-converted from the IF to generate the in-phase and quadrature baseband signals mentioned above, along with additional amplification. Lowpass filtering is generally applied to the baseband signals to further suppress unwanted components.

B. Direct Conversion Receivers

41. Heterodyne receiver architectures are still used, and were extremely widely used until the 1990s. The shift away from heterodyne receivers arose because high-quality, low-power, low-noise, and low-area bandpass filters are not amenable to integrated circuit (IC) implementation. Therefore, IC-based heterodyne receivers generally require off-chip bandpass filters, typically surface acoustic wave (SAW) bandpass filters, to perform the necessary bandpass filtering. Such filters are expensive and their use requires dedicated IC input and output pins which are also expensive. These issues induced significant research and development efforts to develop direct conversion receivers, i.e., receivers that down-convert the received RF signal directly to baseband without first down-converting to a non-zero IF. The benefit of doing this is that lowpass filters, which are amenable to IC implementation can be applied to the baseband signals to remove unwanted signals without the need for bandpass filters.

C. Mixers

42. The term mixer in the context of wireless receivers refers to a class of circuits that perform the above-mentioned frequency shift operation. The classic communication system textbook definition of a mixer is a circuit that multiplies an input signal by a sinusoidal oscillator signal and filters the result. However, most modern practical mixer circuits perform multiplication by "squared-up" oscillator signals, i.e., by oscillator signals which resemble square waves that ideally have the same mid-point crossing times as the corresponding sinusoidal oscillator signals. In this case the multiplication function is equivalent to multiplying the sign of the mixer's input signal by 1 or −1 as a function of the sign of the mixer's squared-up oscillator signal and can be implemented using simple transistor switches as in the prior art discussed below. Not only are such switch-based ±1 multipliers far easier to implement than precise analog multipliers, but the use of squared up oscillator signals greatly improves noise performance. *See, e.g.*, I. Galton and C. Weltin-Wu, "Understanding Phase Error and Jitter: Definitions, Implications, Simulations, and Measurement," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 1, pp. 1-19, Jan. 2019.

43. The in-phase and quadrature baseband signals mentioned above are generated by applying the RF input signal or the IF input signal to the inputs of a pair of such mixers, where the squared up oscillator signals applied to the two

mixers differ in phase by 90 degrees. Lowpass filtering is always required following the mixer multiplication process, but engineers sometimes refer to just the ±1 multiplication process as the mixing process. Either way, by the 1990s it was commonly understood that lowpass filtering is essential following the ±1 multipliers in the baseband down-conversion process.

1. Synchrony

44. A well-known way to avoid the need to create two baseband signals, i.e., in-phase and quadrature baseband signals, is to use a single mixer that multiplies by ±1 with a frequency and phase which precisely matches those of the carrier of the received signal. In such cases, the required oscillator signal is generated by a carrier synchronization circuit (also know as a carrier recovery circuit). The carrier synchronization circuit's input is the RF or IF signal, and its output is an oscillator signal with a frequency and phase that ideally match those of the input signal.

D. Amplifiers

45. As mentioned above, amplification is essential to the wireless reception process. The overall amplification gain from the antenna through to a receiver's baseband signals is typically many orders of magnitude. Amplifier nonlinearity has the potential to convert power from unwanted signals to distortion components that land within the frequency band of the desired signal, thereby

corrupting the desired signal. As the distortion components grow disproportionately with the power of the unwanted signals and the unwanted signals often have much higher power than the desired signal, the amplifiers in wireless receivers must be designed to have a high degree of linearity.

1. Differential Circuits

46. IC implementations of circuit blocks such as amplifiers are often differential, meaning that they process pairs of signals wherein the signal information is represented as the difference between the two signals of each pair. For example, suppose the differential inputs to an amplifier circuit are denoted as v_{in+} and v_{in-}. Then the so-called differential-mode signal, defined as $v_{in} = v_{in+} - v_{in-}$, conveys the desired information content of the differential signal. Note that this definition implies $v_{in+} = v_{in\text{-}cm} + v_{in}/2$ and $v_{in-} = v_{in\text{-}cm} - v_{in}/2$, where $v_{in\text{-}cm} = (v_{in+} + v_{in-})/2$. The $v_{in\text{-}cm}$ signal is called the common-mode signal. Therefore, the differential-mode signal is the difference between the two voltages and the common-mode signal is the average of the two voltages. As the signal information is conveyed by the differential-mode signal and differential circuits are designed not to process the common-mode signal (e.g., a differential amplifier amplifies its differential-mode input signal but does not significantly amplify its common-mode input signal), differential circuits are not sensitive to noise and distortion that equally affects the two signals which make up each of its differential signals.

47. Differential circuits are designed and laid out on an IC as symmetrically as possible, so it is the case that much of the inevitable non-ideal circuit behavior which corrupts any given differential signal, does so in the same way to both of the differential signal's two constituent signals. For example, even order nonlinear distortion corrupts each signal nearly equally, so differential circuits tend to be insensitive to even order nonlinear distortion. However, this benefit requires good symmetry between the two halves of a differential circuit. For example two inputs of a differential amplifier must have matching input impedances for the above-mentioned benefit to occur.

48. Another benefit of a differential circuit is that it has twice the signal range as that of a comparable non-differential circuit. This quadruples the signal power, whereas it only doubles power of the noise introduced by the circuit, which corresponds to a signal-to-noise ratio (SNR) improvement of 3 dB. Modifying the non-differential circuit to improve its SNR by 3 dB would typically double its power consumption. As differential circuits typically consume less than twice the power of corresponding non-differential circuits with comparable SNRs, differential circuits are generally more efficient than non-differential circuits in terms of power consumption.

49. For the above reasons, differential circuits that are designed and laid out to be as symmetrical as possible are generally preferable to non-differential circuits in IC implementations.

2. Low-pass filter or Antialiasing filter

50. Lowpass filters are essential components in direct-conversion receivers as described above. In applications where the baseband signals are to be subsequently sampled, lowpass filters are also sometimes called an antialiasing filters.

51. One particular differential lowpass filter is shown in Fig. 1. It is the antialiasing filter presented in Macnally, which, as explained in Macnally, is a fourth-order Butterworth filter implemented as a cascade of two of the differential Rauch biquads. Each antialiasing filter described in Macnally has this form, although Macnally does not specify the component values. Instead, Macnally states that the filter is a Butterworth filter with a −3 dB bandwidth of 2.4 MHz, and a gain of 15.6 dB. The purpose of this section is to analyze the circuit shown in Figure 1 and choose component values, i.e., values of R_1, R_2, R_3, R_4, C_1, C_2, C_3, and C_4, which cause Fig. 1 to achieve the same −3 dB bandwidth and gain as the corresponding filter presented in Macnally under the constraint that the component values are appropriate for integration in a 0.6 micron CMOS process (the IC technology in which the circuit presented in Macnally was implemented)

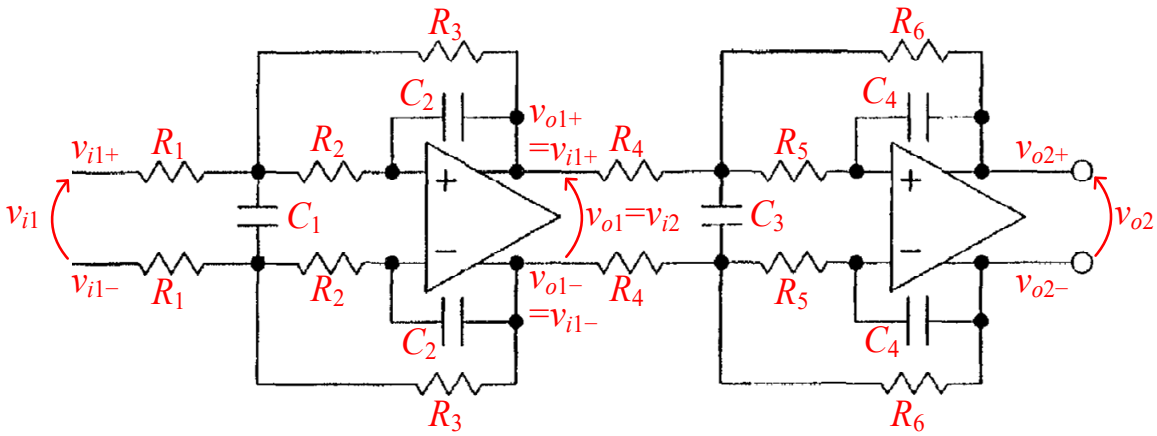


Figure 1: Annotated copy of the antialiasing filter shown in Fig. 3 of [Macnally].

52. A POSITA would recognize that differential-mode behavior of the circuit of Figure 1 can be analyzed via the differential-mode half circuit shown in Figure 2, and that each stage can be analyzed in isolation from the other stage [Laker], [Foster]. A POSITA would also recognize that each operational amplifier in such a circuit would be designed to have an open loop DC gain that is much higher than the closed-loop gain of each filter stage over the bandwidth of the filter, and, consequently, that

$$v_{m1}(s)=0 \quad \text{and} \quad v_{m2}(s)=0, \tag{1}$$

to a good approximation.

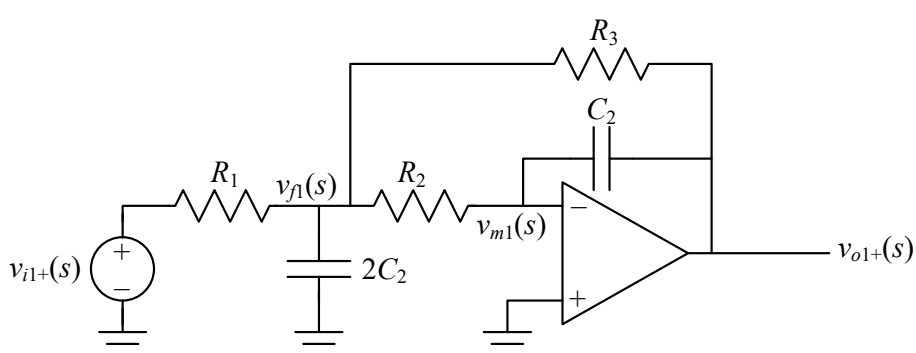


Figure 2: Differential-mode half-circuit corresponding to the first stage of Figure 1.

53. Applying Kirchoff's Current Law with (1) to the node at the negative terminal of the first op-amp and to the $v_{f1}(s)$ node in Fig. 1 yields

$$v_{o1+}(s)sC_2 + \frac{v_{f1}(s)}{R_2} = 0, \tag{2}$$

and

$$\frac{v_{f1}(s) - v_{i1+}(s)}{R_1} + v_{f1}(s)2sC_1 + \frac{v_{f1}(s) - v_{o1+}(s)}{R_3} + \frac{v_{f1}(s)}{R_2} = 0, \tag{3}$$

respectively. Equation (3) can be rearranged as

$$v_{f1}(s)\left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + 2sC_1\right] - \frac{v_{i1+}(s)}{R_1} - \frac{v_{o1+}(s)}{R_3} = 0, \tag{4}$$

Solving (2) for $v_{f1}(s)$ and substituting the result into (4) gives

$$-v_{o1+}(s)sR_2C_2\left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + 2sC_1\right] - \frac{v_{i1+}(s)}{R_1} - \frac{v_{o1+}(s)}{R_3} = 0, \tag{5}$$

Rearranging (5) gives

$$\frac{v_{o1+}(s)}{v_{i1+}(s)} = -\frac{1}{s^2\left(2R_1C_1R_2C_2\right) + s\left(R_1 + R_2 + \frac{R_1R_2}{R_3}\right)C_2 + \frac{R_1}{R_3}}, \tag{6}$$

By symmetry, it follows that

$$\frac{v_{o1-}(s)}{v_{i1-}(s)} = \frac{v_{o1+}(s)}{v_{i1+}(s)}, \tag{7}$$

54. By definition, the differential-mode input and output signals of the first filter stage are $v_{i1}(s) = v_{i1+}(s) - v_{i1-}(s)$ and $v_{o1}(s) = v_{o1+}(s) - v_{o1-}(s)$,

respectively, $v_{i1-}(s) = -v_{i1+}(s)$, and $v_{o1-}(s) = -v_{o1+}(s)$ (this is a small-signal analysis, so the common-mode voltages are taken to be zero). As this implies $v_{i1+}(s) = v_{i1}(s)/2$, and $v_{i1-}(s) = -v_{i1}(s)/2$, it follows from (7) that the differential-mode gain of the first stage, i.e., $A_1(s) = v_{o1}(s)/v_{i1}(s)$, is given by the right side of (6), i.e.,

$$A_1(s) = -\frac{1}{s^2\left(2R_1C_1R_2C_2\right) + s\left(R_1 + R_2 + \frac{R_1R_2}{R_3}\right)C_2 + \frac{R_1}{R_3}}, \tag{8}$$

55. By identical reasoning, the differential-mode gain of the second filter stage, i.e., $A_2(s) = v_{o2}(s)/v_{i2}(s)$, is

$$A_2(s) = -\frac{1}{s^2\left(2R_4C_3R_5C_4\right) + s\left(R_4 + R_5 + \frac{R_4R_5}{R_6}\right)C_4 + \frac{R_4}{R_6}}, \tag{9}$$

56. Therefore, the differential-mode frequency response of the filter shown in Fig. 1 is given by the product of (8) and (9) with s replaced by $j2\pi f$, i.e.,

$$A\left(j2\pi f\right) = A_1\left(j2\pi f\right)A_2\left(j2\pi f\right), \tag{10}$$

where f denotes frequency in Hz and j is the unit-magnitude imaginary number.

As shown in [Foster], the circuit with

$$R_1 = R_2 = R_3 = R_4 = R_5 = R_6 = R \tag{11}$$

for any positive value of R implements a Butterworth filter with a −3 dB bandwidth of f_0 and unity gain provided the capacitor values are chosen as:

$$C_1 = \frac{1}{2} \cdot \frac{3.91969}{2\pi f_0 R}, \quad C_2 = \frac{0.25512}{2\pi f_0 R}, \quad C_3 = \frac{1}{2} \cdot \frac{1.62359}{2\pi f_0 R}, \text{ and } C_4 = \frac{0.61592}{2\pi f_0 R}. \tag{12}$$

57. Given that f_0 = 2.4 MHz, choosing R = 1000 Ω in (12) yields capacitor values which are easily realizable in the 0.6 micron CMOS technology used in [1], and large enough that the circuit's noise performance is unlikely to be problematic. The resulting capacitor values are:

$$C_1 = 130 \text{ pF}, \quad C_2 = 17 \text{ pF}, \quad C_3 = 53.8 \text{ pF}, \text{ and } C_4 = 40.8 \text{ pF}. \tag{13}$$

58. While these component values in the circuit of Figure 1 yield a Butterworth filter with the desired −3 dB bandwidth, its DC gain is 0 dB whereas the target DC gain of the overall filter is 15.6 dB. Therefore, it is necessary to modify these component values. A generally good design choice is to have each filter stage contribute half the DC gain, i.e.,

$$A_1(0) = A_2(0) = A_0 \quad \text{where} \quad A_0 = 10^{\frac{15.6/2}{20}} = 2.4547. \tag{14}$$

59. Setting s = 0 in (8) and (9) shows that the DC gains of the first and second filter stages are given by $-R_3/R_1$ and $-R_6/R_4$, respectively. For good noise performance, it is preferable to increase the DC gain of the two stages by increasing R_3 and R_6 rather than decreasing R_1 and R_4. Therefore, setting $R_3 = R_6$ = 2454.7 Ω and keeping the other resistors at 1000 Ω gives the desired DC gain. However, to maintain the same frequency response, the capacitor values must be changed to maintain the original pole frequencies. This can be done by ensuring that the coefficients of s^2 and s in (8) and (9) change by the same factor of A_0^{-1} by

which the new values of R_3 and R_6 caused the s^0 coefficients to change. Inspection of (8) and (9) shows that this requirement is achieved if C_2 and C_4 are changed to

$$C_2 \frac{R_1 + R_2 + \frac{R_1 R_2}{R_3} A_0}{A_0 \left(R_1 + R_2 + \frac{R_1 R_2}{R_3} \right)}, \quad \text{and} \quad C_4 \frac{R_4 + R_5 + \frac{R_4 R_5}{R_6} A_0}{A_0 \left(R_4 + R_5 + \frac{R_4 R_5}{R_6} \right)}, \tag{15}$$

respectively, and C_1 and C_3 are changed to

$$C_1 \frac{R_1 + R_2 + \frac{R_1 R_2}{R_3}}{R_1 + R_2 + \frac{R_1 R_2}{R_3} A_0}, \quad \text{and} \quad C_3 \frac{R_4 + R_5 + \frac{R_4 R_5}{R_6}}{R_4 + R_5 + \frac{R_4 R_5}{R_6} A_0}, \tag{16}$$

respectively. Therefore, the revised component values are

$$R_1 = R_2 = R_4 = R_5 = 1000\Omega \quad \text{and} \quad R_3 = R_6 = 2454.7\Omega \tag{17}$$

and

$$C_1 = 104.3\,\text{pF}, \; C_2 = 8.6\,\text{pF}, \; C_3 = 43.2\,\text{pF}, \text{ and } C_4 = 20.7\,\text{pF}. \tag{18}$$

60. The above shows that circuit of Figure 1 with the component values given by (17) and (18) implements the desired filter. It also shows that the filter's frequency response is given by (10) with $A_1(s)$ and $A_2(s)$ given by (8) and (9), respectively, with component values given by (17) and (18) and s replaced by $j2\pi f$. Figure 3 shows a plot of the magnitude of the filter's frequency response in dB, i.e., a plot of $20\log(|A(j2\pi f)|)$, versus frequency in Hz on a log scale. As can be seen from the plot, the DC gain of the filter is 15.6 dB and the filter's −3 dB frequency is 2.4 MHz, as intended.

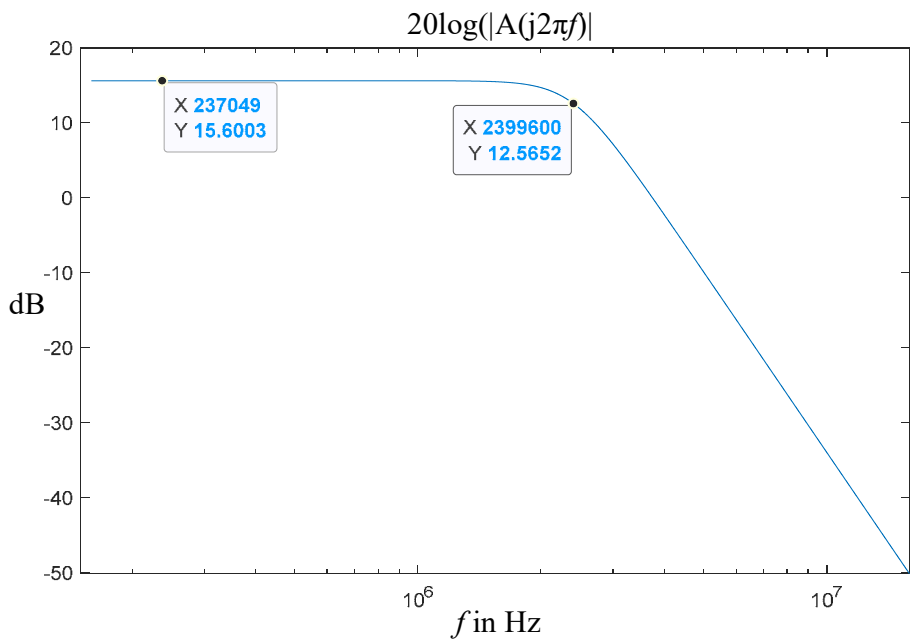


Figure 3: Magnitude of the differential-mode frequency response of the filter shown in Fig. 1 with component values given by (17) and (18).

VIII. THE '177 PATENT

A. Brief Description

61. The '177 Patent is directed to "down-converting an electromagnetic (EM) signal." TI-1001, Abstract. Claim 14 of the '177 patent claims a method for down-converting the EM signal using first and second matched filtering / correlating modules. *See, e.g.*, TI-1001, claim 14. The first and second matched filtering/correlating module each down-converts the input signal to produce first and second down-converted signals. The two down-converted signals are combined.

1. Matched Filtering/Correlating Module

62. The ’177 patent does not use the term “matched filtering/correlating module” in its specification. Instead, the ’177 patent describes a matched filtering/correlating process that is performed repeatedly on a received carrier signal. *See, e.g.*, TI-1001, 130:23-31. The ’177 patent recognizes practical design limitations associated with implementing “traditional” realizations of matched filtering/correlating modules, and therefore intends the meaning of “matched filtering/correlating module” to include various circuit implementations that perform the desired function, including both traditional matched filtering/correlating modules and the non-traditional realizations described in the specification. *See, e.g.*, TI-1001, 130:40-48, 132:15-17 (“the present invention is not a traditional realization of a matched filter/correlator”), FIGS. 148-154, 184, and accompanying text.

63. A POSITA reading the specification, in view of the departure from “traditional” realizations of a matched filtering/correlating module, would have understood the term to encompass core functional aspects of matched filtering or correlating. The key common characteristic across all implementations is that “a matched filtering/correlating operation is performed on a portion of a carrier signal,” wherein the correlation signal is synchronous with the received signal, and, correspondingly, for the claimed down-converter embodiments described in

'177, the correlation signal, $S_i(t-\tau)$, is synchronous with the received signal's carrier. For example, Column 145 of '177 states that "the example matched filter/correlator of FIG. 171 operates in synchronism with the half sine pulse $S_i(t)$ over the aperture T_A," and this "synchronism" is depicted in several of the figures in '177 including but not limited to Fig. 72, Fig. 157, Fig. 158, Fig. 162, Fig. 166, Fig. 182, Fig. 184, and Fig. 193. Another common characteristic is that "the result of the matched filtering/correlating operation … is accumulated, preferably in an energy storage device[,]" and that these steps "are repeated for additional half cycles [or portions thereof] of the carrier signal." *See, e.g.*, '177 patent, 131:17-44; 132:54-133:14; 133:62-134:22, FIGS. 148-154, 184 and accompanying text.

B. Prosecution History

64. Patent Application U.S. 12/349,802 (the 802 Application), resulting in the '177 patent, was filed on January 7, 2009. The 802 Application was a division of Application No. 09/550,644 (the 644 Application), now U.S. Pat. No. 7,515,896, filed on April 14, 2000. During prosecution of 644 Application, the examiner issued a Restriction Requirement to elect one species from a Group of 5:

1. This application contains claims directed to the following patentably distinct species of the claimed invention:

Claims 1-12 are directed to the matched filtering/accumulating embodiment in FIG. 149.

Claims 13-24 are directed to the finite time integrating/accumulating embodiment in FIG. 151.

Claims 25-35 are directed to the RC processing/accumulating embodiment in FIG. 153.

Claims 36-48 are directed to the matched filtering/subtracting embodiment in FIG. 197.

Claims 49-74 are directed to the finite time integrating/subtracting embodiment in FIG. 197.

644 Application File History, Requirement for Restriction/Election, 4. The applicant elected claims 1-12.

65. The originally filed claims of the 802 Application were directed to a method for down-converting an EM signal by "(1) performing a finite time integration operation on a portion of a carrier signal"; "(2) accumulating the result of the finite time integrating operation of step (1)"; and "(3) repeating steps (1) and (2) for additional portions of the carrier signal, whereby the accumulation results [from] a down-converted signal." 802 Application, Originally Filed Claims.

66. The originally filed claims were rejected under 35 U.S.C. § 101 for failing to claim statutory subject matter; and they were provisionally rejected under statutory and non-statutory double patenting. 802 Application, Non-final Rejection, 2-4. The claims were also indicated as allowable if rewritten to overcome the rejections. *Id.*, 5.

67. In response, the applicant cancelled all of the pending claims, and submitted new claims. 802 Application, Response to Non-final Rejection, 3. These new claims were allowed and resulted in the ’177 patent claims as they stand now.

IX. OVERVIEW OF THE PRIOR ART

1. U.S. Patent No. US 6,230,000 (“Tayloe”)

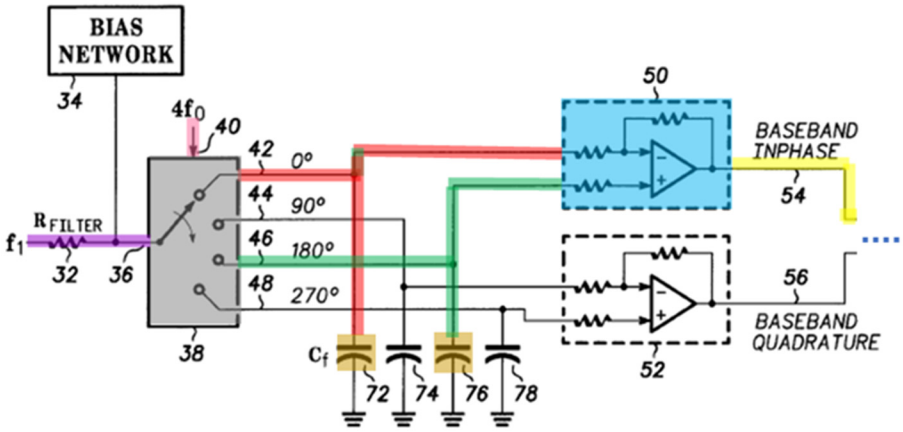
68. Tayloe is titled “*Product Detector and Method Thereof*.” EX1004. It was filed on October 15, 1998.

69. Tayloe describes a direct conversion (i.e., the product detector) “for converting a signal to baseband.” TI-1004, Abstract, 1:51-52 (de-scribing Figure 3). Tayloe explains that its direct conversion receiver:

> includes a commutating switch which serves to sample an RF waveform four times per period at the RF frequency. The samples are integrated over time to produce an average voltage at 0 degrees, 90 degrees, 180 degrees and 270 degrees. The average voltage at 0 degrees is the baseband in-phase signal . . . .

Id., Abstract. Tayloe discloses that, “to increase gain, the 0 degree average can be differentially summed with the 180 degree average to form the baseband in-phase signal . . . .” *Id.* Tayloe states that “[d]irect conversion receivers are desirable in part because they convert signals of interest directly to baseband (or near zero hertz) from a radio frequency (RF) or an intermediate frequency (IF).” *Id.* at 1:10–13.

70. In more detail, Tayloe discloses an example of a direct conversion receiver in Figure 3:



30 FIG. 3

TI-1004, Figure 3 (annotated).

71. The receiver receives an RF input signal f_1 and down-converts this signal. *Id.*, 2:13-67 ("[A]n RF … signal f_1 [purple] is received at resistor 32…. After passing through resistor 32, the input signal is received by commutating switch 38 [gray] at input 36. Commutating switch 38 switches input 36 to outputs 42 [red], 44, 46 [green], and 48…. As commutating switch 38 cycles through the four outputs, capacitors 72-78 charge to voltage values substantially equal to the average value of the input signal during their respective quadrants…. The outputs of commutating switch 38 are input to summing amplifiers 50 [light blue] and 52. Summing amplifier 50 [light blue] differentially sums the 0 degree output [42 (red)] and the 180 degree output [46 (green)], thereby producing baseband in-phase

signal 54 [yellow]. The resulting signals are then summed by summing amplifier 60 to produce the signal of interest 62").

72. Like the '177 Patent, Tayloe's receiver has four frequency down-conversion modules, labeled "0º," "90º," "180º," and "270º," each including a switch and a storage element (*e.g.*, capacitor).

73. The 0º frequency down-conversion module provides a 0º down-converted signal 42 (red). TI-1004, 2:13-18 ("[A]n RF … signal f_1 [purple] is received at resistor 32…. After passing through resistor 32, the input signal is received by commutating switch 38 [gray] at input 36. Commutating switch 38 switches input 36 to output[] 42 [red]…."), 2:46-48 ("Output 42 [red represents the average value of the [RF] input signal [f_1 (purple)] during the first quarter wave of the period [of the input signal f_1], and is termed the 0 degree output.").

74. The 0º frequency down-conversion module includes a switch 38 (gray), which periodically couples the input signal f_1 (purple) to the output 42. TI-1004,2:16-26. Moreover, the rate at which the switch 38 periodically couples the input signal f_1 at input 36 (purple) to the output 42 is determined by a control signal ($4f_0$, pink) supplied to a control input 40 of the switch. *Id.*, 2:18-20 ("The rate at which commutating switch 38 operates is controlled by a signal present at control input 40.").

75. While Tayloe shows commutating switch 38 as a single component without its specific structure. As explained below, a POSITA would have understood that Tayloe's commutating switch 38, especially in view of TI Datasheet and Kawada, comprises multiple switches. Accordingly, as noted below, a POSITA would understand that each down-conversion module includes its own switch within the commutating switch 38. Accordingly, as noted below, a POSITA would understand that each down-conversion module includes its own switch within the switch 38.

76. The 0º frequency down-conversion module also includes a capacitor 72 (brown). "During the time that [the] switch 38 connects input 36 [receiving the RF input signal f_1] to output 42, charge builds up on capacitor 72." TI-1004, 2:32-33. The voltage across the capacitor 72 corresponding to this charge constitutes the average value of the RF input signal f_1 during first quarter of the period of the signal f_1 and is output from the 0 degree frequency down-conversion module as the 0º down-converted signal 42 (red). *Id.*, 2:46-48 ("Output 42 [red] represents the average value of the input signal during the first quarter wave of the period, and is termed the 0 degree output."), 2:18-26.

77. Similarly, the 180º frequency down-conversion module provides a 180º down-converted signal 46 (green). TI-1004, 2:13-18 ("After passing through resistor 32, the [RF] input signal [f_1] is received by commutating switch 38 [gray]

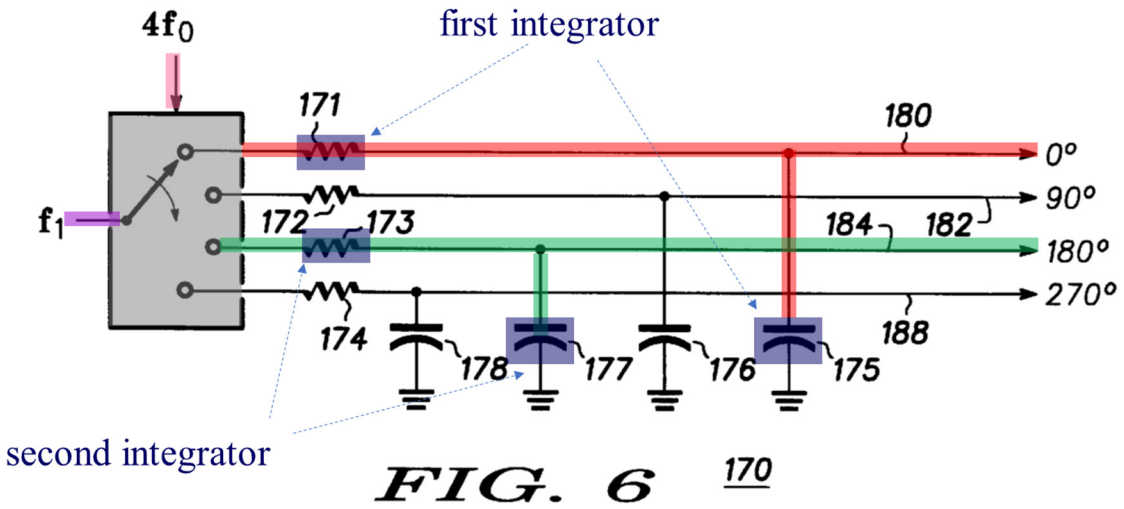
at input 36. Commutating switch 38 switches input 36 to output[] … 46 [green]….”), 2:50-53 (“Output 46 [green] represents the average value of the input signal [f_1 (purple)] during the third quarter wave of the period [of the input signal f_1], and is termed the 180 degree output.”), 2:18-26.

78. The 180º frequency down-conversion module includes the switch 38 (gray) and a capacitor 76 (brown). When the switch 38 couples the input signal f_1 (purple) to the output 46, charge builds up on the capacitor 76 (brown) in the same manner as charge builds up on the capacitor 72 described above. TI-1004, 2:18-38 (“During the time that commutating switch 38 connects input 36 to output 42, charge builds up on capacitor 72…. The same principle holds true for capacitor[] 76 … when commutating switch 38 connects input 36 to output[] 46….”).) Thus, voltage across the capacitor 76 constitutes the average values of the RF input signal f_1 during the third quarter of the period of the signal f_1 and is output from the 180º frequency down-conversion module as the 180º down-converted signal 46 (green). *Id.*, 2:50-53 (“Output 46 [green] represents the average value of the input signal during the third quarter wave of the period, and is termed the 180 degree output.”), 2:18-26.

79. The 90º and 270º frequency down-conversion modules each have a similar operation and structure. TI-1004, 2:35-39 (“Likewise, during the time commutating switch 38 connects input 36 to output 44, charge builds up on

capacitor 74. The same principle holds true for capacitor[] 78 when commutating switch 38 connects input 36 to output[] 48"). "As commutating switch 38 cycles through the four outputs, capacitors 72–78 charge to voltage values substantially equal to the average value of the input signal during their respective quadrants" *Id.*, 2:39-43. "Output 44 represents the average value of the input signal during the second quarter wave of the period, and is termed the 90 degree output." *Id.*, 2:48-50. "Output 48 represents the average value of the input signal during the fourth quarter wave of the period, and is termed the 270 degree output." *Id.*, 2:53-55.

80. Tayloe also discloses "an alternate embodiment in which each integrating capacitor has its own resistor." TI-1004, 4:48-49. Compared to Figure 3 (above), Figure 6 (below) of Tayloe shows "0 degree output 180 has a voltage controlled by the combination of capacitor 175 and resistor 171" and "180 degree output 184 has a voltage controlled by the combination of capacitor 177 and resistor 173." *Id.*, 4:49- 57 (further noting "90 degree output 182 has a voltage controlled by the combination of capacitor 176 and resistor 172" and "270 degree output 188 has a voltage controlled by the combination of capacitor 178 and resistor 174.").



TI-1004, Figure 6 (annotated)

81. "Resistor 171 and capacitor 175 form a first integrator [(dark blue) for the 0° output (red) where the switch (gray)] connects the input to this first integrator for substantially 90 degree of the input signal [f_1 (purple)]." TI-1004, 4:57-60. Tayloe explains that "the remaining resistor/capacitor pairs [in Figure 6] also form integrators [including a second integrator (dark blue) for the 180° output (green)], each of which preferably integrates for substantially 90 degrees of the input signal [f_1 (purple)]." *Id.*, 4:60-67 (noting the integrators can have same or different time constants).

82. Capacitors 72 and 74 are connected to the top inputs of 50 and 52, respectively as indicated in Fig. 3. Each of 50 and 52 is a differential-input summing amplifier implemented as an operational amplifier with a resistor that connects its output to its negative input terminal two input resistors connected to

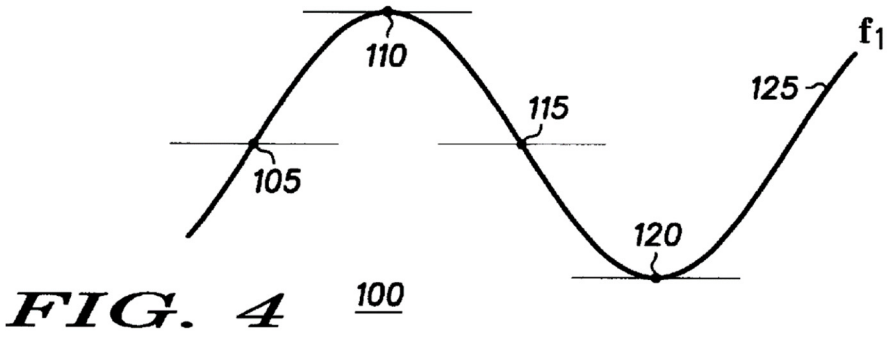
the two operational amplifier input terminals. A POSITA would recognize that the feedback around the operational amplifier in conjunction with the operational amplifier's high DC gain causes the node to which the negative terminal of the operational amplifier is connected to have a very low resistance (typically well below a few ohms). Therefore, the input resistance looking into the top input of each of 50 and 52 is approximately equal to the resistance of the top-left resistor. A POSITA would understand that these resistors would have resistances on the order of kilo-ohms or less, so the Capacitors 72 and 74 are not connected to high-impedances. In particular, they will discharge with a voltage proportional to $e^{-t/RC}$, where t is time, R is the above-mentioned resistance (on the order of kilo-ohms), and C is the capacitance value of Capacitors 72 an 74.

83. Returning to the example in Figure 3 annotated *supra*, Tayloe discloses:

> The outputs of commutating switch 38 are input to summing amplifiers 50 and 52. Summing amplifier 50 [light blue] differentially sums the 0 degree output [red] and the 180 degree output [green], thereby producing baseband in-phase signal 54. Summing amplifier 52 differentially sums the 90 degree output and the 270 degree output, thereby producing base band quadrature signal 56.
>
> (*Id.*, 2:56-67)

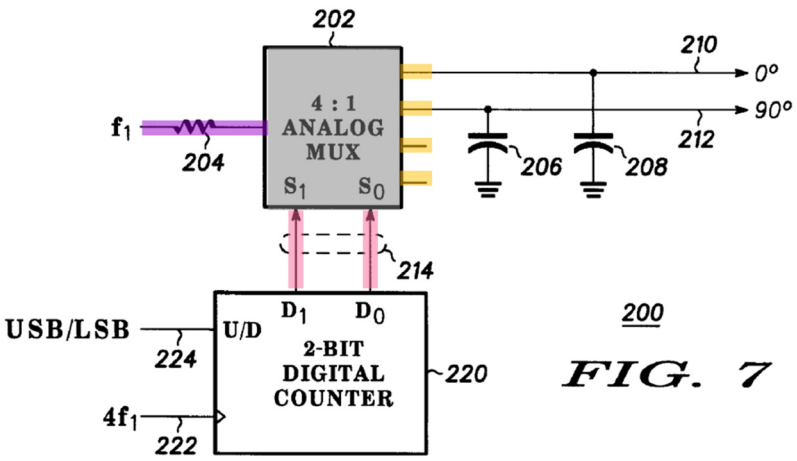
84. I have provided explanation of fully differential amplifiers in Section VII.D.

85. As explained above, the direct conversion receiver operates switch 38, which is "controlled by a signal [pink] present at control input 40." TI-1004, 2:17-20. This control signal (pink) causes switch 38 to couple the RF input signal f_1 to one of the four outputs 42, 44, 46, and 48 so that the RF input signal f_1 is sampled four times during a full cycle in which, as illustrated in Figure 4 (below), "[p]oint 105 represents the voltage to which capacitor 72 (FIG. 3) charges," "point 110 represents the voltage to which capacitor 74 charges, point 115 represents the voltage to which capacitor 76 charges, and point 120 represents the voltage to which capacitor 78 charges." *Id.*, 3:41-48.



TI-1004, Figure 4

86. Tayloe further expressly discloses implementing "direct conversion receiver 30 (FIG. 3) utilizing an analog multiplexer and a digital counter as shown in FIG. 7 [annotated below]." TI-1004, 5:33-37.



87. TI-1004, Figure 7 (annotated)

88. As an embodiment of switch 38 (Figure 3), multiplexer 202 (above) acts as a demultiplexer, connecting a single input signal f_1 (purple) to one of four outputs (orange) based on control signals 214 (pink) (corresponding to the control input 40 in Figure 3). Tayloe specifically discloses that "[t]he analog multiplexer is a Texas Instruments SN74BCT3253D." *Id.*, 5:33-37, 5:1-16 ("… input signal f_1 is connected to each of the four outputs of analog multiplexer 202 for substantially 90 degrees of the input signal.").

89. Tayloe specifically refers to a TI "SN74BCT3253D" multiplexer. The "BCT" lettering (as opposed to "CBT") appears a typographical error. The TI Datasheet is also descriptive of all SN74CBT3253 multiplexers, explaining that the "D" in the product number refers to a packaging option ("Plastic Small-Outline (D)") for the SN74CBT3253 multiplexer.

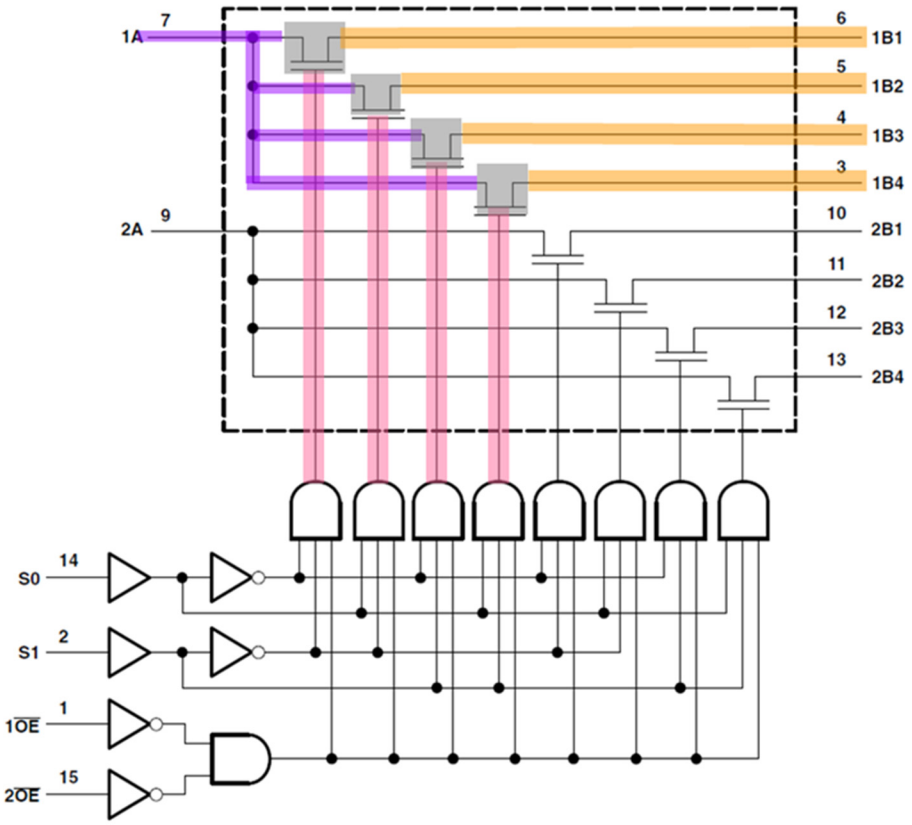
90. I discuss the implementation details of the SN74CBT3253D multiplexer/demultiplexer are disclosed in TI Datasheet (TI-1005) below.

2. TI Datasheet

91. The TI Datasheet describes the SN74CBT3253 multiplexer/demultiplexer, a commercially available electronic component that can be used in a radio receiver such as Tayloe's receiver. TI-1005, 1; TI-1004, 5:33-37 (describing radio receiver including the SN74CBT3253 multiplexer)).

92. Multiplexers are well-known electronic devices that receive multiple input signals and select one signal to be output. A multiplexer such as the one disclosed in TI Datasheet can also operate in reverse as a demultiplexer—receiving a single input signal and routing it to one of several output lines—as reflected in the device's name ("SN74CBT3253 Dual 1 of 4 FET ***Multiplexer/Demultiplexer***").

93. Tayler uses the SN74CBT3253 multiplexer/demultiplexer as a demultiplexer. This SN74CBT3253 multiplexer/demultiplexer shows additional details of how Tayloe's switch 38 would connect the single input signal to one of multiple output lines, and in particular, the demultiplexing operation is shown below.



94. The TI multiplexer/demultiplexer has four switches (gray) that selectively supply the input signal 1A (purple) to one of four outputs 1B1-1B4 (orange) according to four control signals (pink), respectively. The control signals are generated based on control logic that ensures only one of the four switches is turned on at a time. TI-1005, 1("1$\overline{\text{OE}}$, 2$\overline{\text{OE}}$, S0, and S1 select the appropriate output for the A-input data"). The functional mapping of the control signals is shown in Table 1 below:

FUNCTION TABLE

INPUTS				FUNCTION
$1\overline{OE}$	$2\overline{OE}$	S1	S0	
X	H	X	X	Disconnect 1A and 2A
H	X	X	X	Disconnect 1A and 2A
L	L	L	L	1A to 1B1 and 2A to 2B1
L	L	L	H	1A to 1B2 and 2A to 2B2
L	L	H	L	1A to 1B3 and 2A to 2B3
L	L	H	H	1A to 1B4 and 2A to 2B4

control signals values

TI-1005, Table 1

3. Razavi

95. Razavi describes a direct conversion receiver for down-converting a 900 MHz radio frequency signal to baseband. *See, e.g.*, Razavi, 1:1-3. The overall architecture of Razavi includes a low-noise amplifier (LNA), quadrature mixers, a local oscillator, and baseband amplifiers. *See, e.g.*, *id.*, 1:4-7. The architecture is shown in FIG. 1:

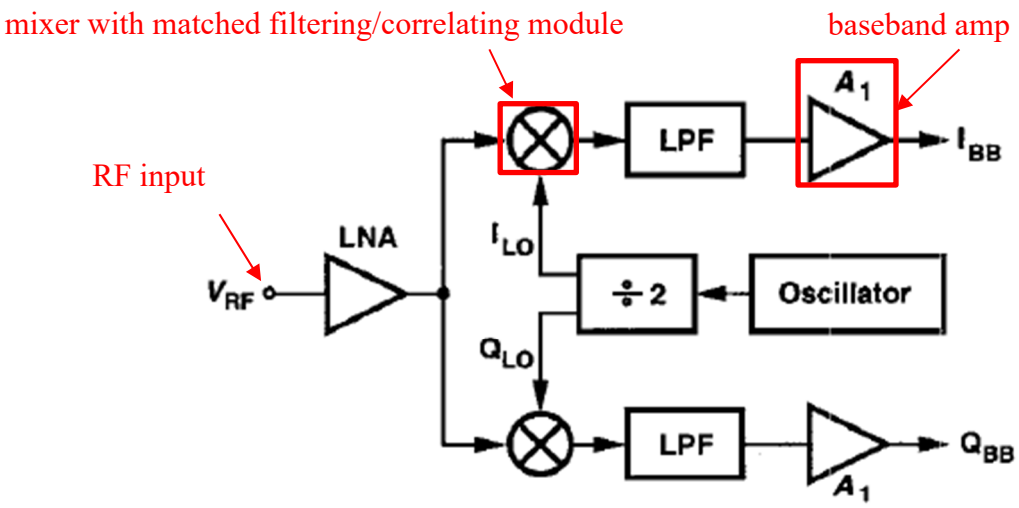


Fig. 1. Receiver architecture.

Razavi, FIG. 2 (annotated)

Each mixer (shown as a circle with an x) includes a matched filtering/correlating module. An example of an LNA and mixer are shown in FIG. 2, below:

first and second matched filtering/correlating modules

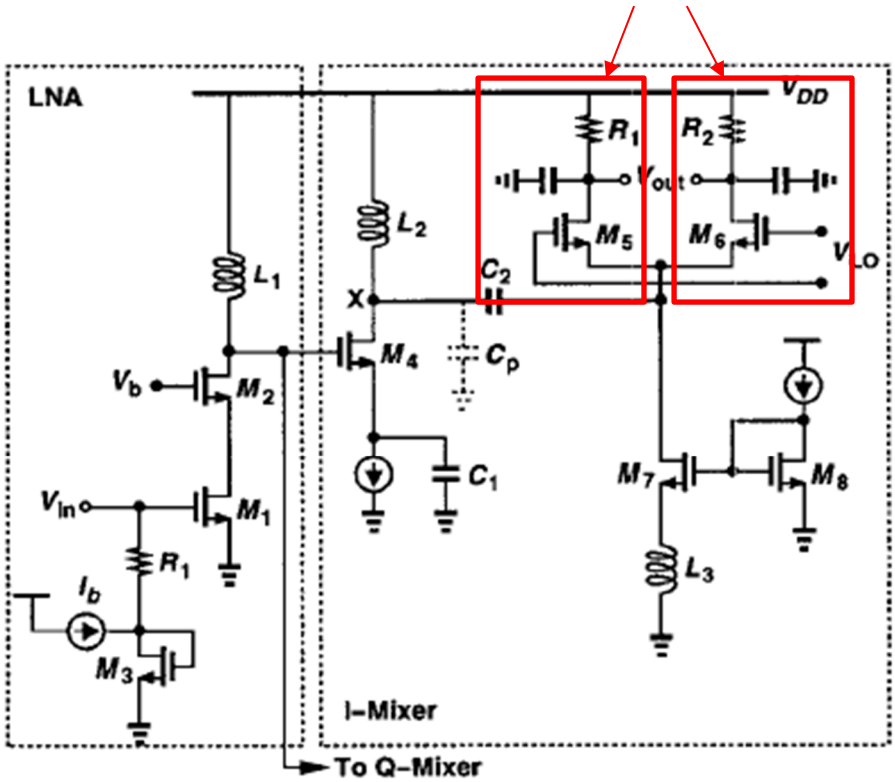


Fig. 2. LNA/mixer implementation.

Razavi, FIG. 2 (annotated)

96. As can be seen by FIG. 2, each matched filtering/correlating module of Razavi includes a switch (M5 and M6, respectively), a capacitor, and a load R1 and R2. When implementing both in-phase and quadrature circuits, each of the in-phase and quadrature circuits include a mixer shown above (although only the in-phase mixer circuit is shown in the figure). The output Vout of the matched filtering/correlating module is a downconverted differential baseband in-phase (or quadrature) signal.

97. The baseband in-phase signal is output to another circuit element, which can be an amplifier, a filter, or an analog-to-digital converter. Razavi, 2:21-34. An example architecture for a baseband amplifier is provided in FIG. 5 below:

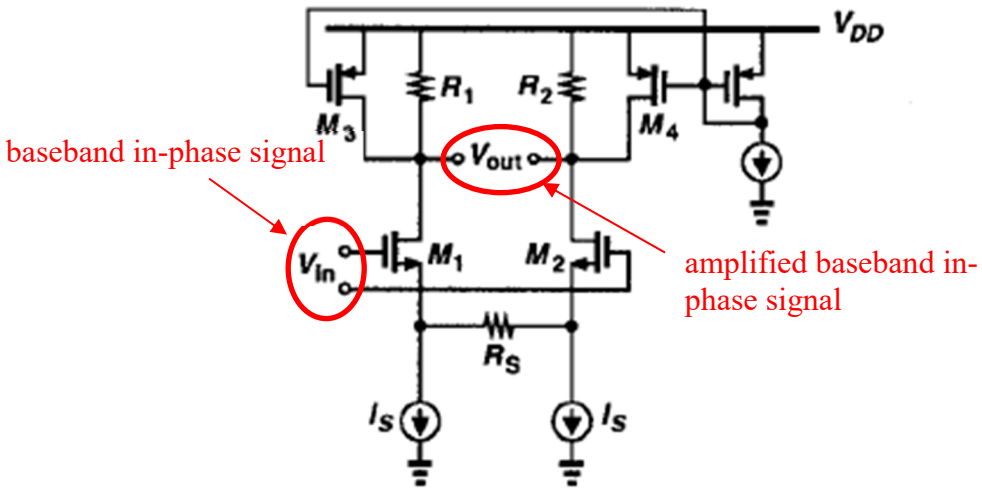


Fig. 5. Baseband amplifier.

Razavi, FIG. 5 (annotated).

Fig. 5 is "the implementation of the baseband amplifier, consisting of a degenerated differential pair M1-M2 and load devices R1-R2 and M3-M4." Razavi, 2:35-48, FIG. 5.

4. Uzunoglu

98. The circuit presented in Uzunoglu, referred to as a synchronous oscillator circuit, performs carrier synchronization (also known as carrier recovery). The circuit operates on a received RF input signal and generates an oscillatory output signal that closely matches both the frequency and phase of the

received RF input signal's carrier. The functional description of the circuit is shown in FIG. 1 below:

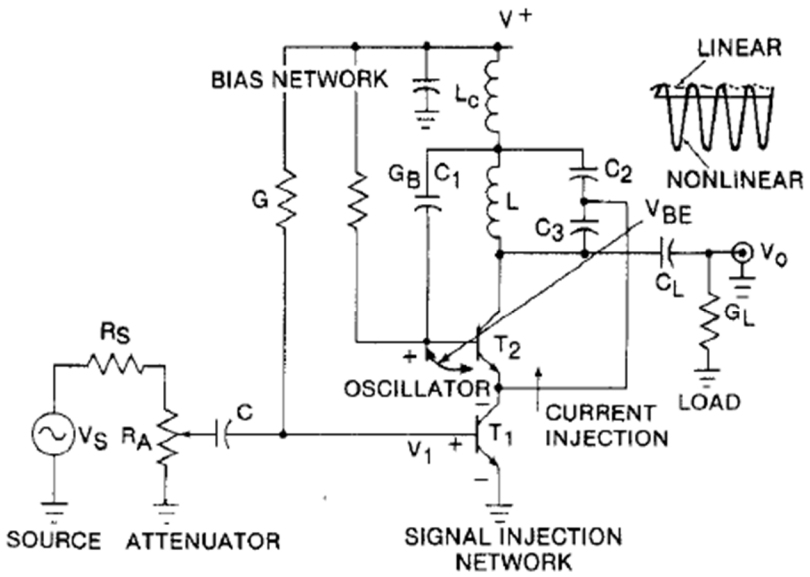


Fig. 1. Functional description of the SO circuit.

Uzunoglu, FIG. 1

FIG. 1 of Uzunoglu illustrates the basic injection-locked synchronous oscillator (SO) circuit and a functional description of its operation. According to Uzunoglu, a "synchronous oscillator (SO) is a free-running oscillator which oscillates at its natural frequency in the absence of an externally applied signal. In the presence of a signal, the oscillator synchronizes with and tracks the input waveform with an acquisition time inversely proportional to the tracking bandwidth." Uzunoglu, Abstract.

99. As explained in Uzunoglu, "[t]he synchronous oscillator (SO) is an important functional element for synchronization and tracking in communication systems," its "output signal amplitude remains constant and unaffected by variations in the input drive level; however, the output phase is modulated to synchronize and track the input signal." Uzunoglu, 11-12.

X. GROUNDS FOR UNPATENTABILITY OF CLAIM 14

A. GROUND 1 – Tayloe + TI SN74CBT3253 Renders Claim 14 Obvious

1. The Tayloe + TI SN74CBT3253 Combination

100. Based upon my review of the references and my knowledge and experience in this field, it is clear that a POSITA would have been motivated to combine the teachings of Tayloe and TI Datasheet.

101. As I explain above under §X.A, Tayloe discloses a direct conversion receiver using a commutating switch to "sample an RF waveform four times per period at the RF frequency" in which "[t]he samples are integrated over time to produce an average voltage at 0 degrees, 90 degrees, 180 degrees and 270 degrees" across the 360-degree full cycle. TI-1004, Abstract, *see also* 2:13-67 (for each of the four sampling events, charge builds up on a respective one of capacitors 72, 74, 76, and 78), Figs. 3 (diagram example), 4 (waveform example). Tayloe also discloses "an alternate embodiment in which each integrating capacitor has its own resistor." TI-1004, 4:48-57 (each resistor/capacitor pair in Figure 6 form an

integrator), Fig. 6. Tayloe further discloses that the switch 38 can be implemented using an analog multiplexer/demultiplexer, such as the Texas Instruments ("TI") SN74CBT3253D multiplexer/demultiplexer. TI-1004, 5:33-37, 5:1-16, Fig. 7 (multiplexer/demultiplexer example).

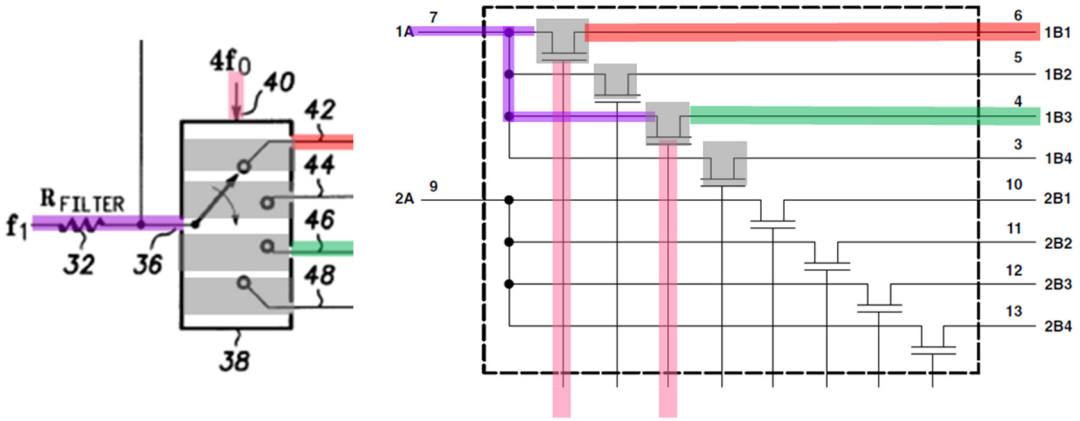
102. As I have explained under §X.B, TI Datasheet describes SN74CBT3253, a "dual 1-of-4 high-speed [transistor-transistor logic]-compatible [field-effect transistor] multiplexer/demultiplexer." TI-1005, 1. TI Datasheet states "[t]he low on-state resistance of the switch allows connections to be made with minimal propagation delay." *Id*.

103. A POSITA would have found it obvious to combine relevant teachings from Tayloe and the TI Datasheet.

104. ***First***, as a preliminary matter, Tayloe expressly teaches four switches in a "direct conversion receiver 30 (FIG. 3) utilizing an analog multiplexer … shown in FIG. 7" and specifically states "[t]he analog multiplexer is a Texas Instruments SN74BCT3253D." TI-1004, 5:33-37. The characteristics described in the TI Datasheet are expressly included in Tayloe's implementation, and as evidenced by at least Tayloe's reference to the TI Datasheet, POSITA knew the characteristics of the referenced TI multiplexer.

105. Additionally, a POSITA would have also found it obvious to combine Tayloe and the TI Datasheet, using any four of the multiplexer switches (gray)

from the multiplexer to implement Tayloe's switch box 38 of Figure 3, such as annotated below.



TI-1004, Fig 3 (switch 38), TI-1005, 1 (multiplexer/demultipler)

106. Because Tayloe expressly discloses the SN74CBT3253 multiplexer/demultiplexer and a datasheet is a well-known resource for learning detailed information of the multiplexer/demultiplexer, a POSITA would have been motivated to consult the TI Datasheet for a more complete understanding of Tayloe's express teachings of the SN74CBT3253 multiplexer, the only matching multiplexer available at the time, as evidenced by the declaration by Maureen Honeycutt, the TI Senior Paralegal.

107. A POSITA would have also been motivated to use the multiplexer of the TI Datasheet in Tayloe's implementation of switch box 38 at least because

Tayloe expressly teaches using a multiplexer, and the multiplexer of TI's datasheet is a suitable multiplexer because Tayloe demonstrated experimental results using it.

108. When viewing the detailed diagram of the SN74CBT3253 multiplexer, a POSITA would have been motivated to apply four of the multiplexer switches (gray squares (TI-1005, 1)) because the architecture of one multiplexer switch on the analog multiplexer is analogous to one of the four switching paths when using Tayloe's commutating switch 38 (gray stripes (TI-1004, Fig. 3)). Thus, a POSITA would have been inspired to implement the multiplexer switches from TI Datasheet in an analogous manner by "simple substitution of one known element for another."

109. A POSITA would have a reasonable expectation of success at combining Tayloe with TI Datasheet because the combination would have yielded only predictable results (e.g., "low on-state resistance of the switch [which] allows connections to be made with minimal propagation delay"). TI-1005, 1.

2. Analysis

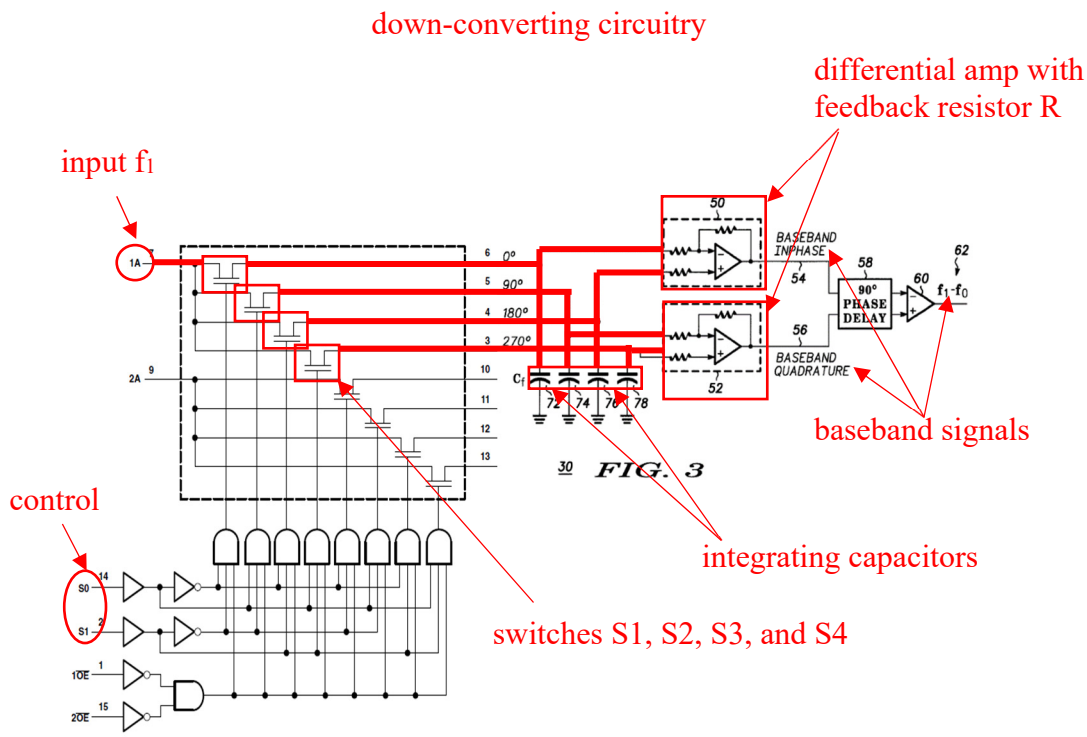
14.P A method for down-converting an electromagnetic signal, comprising:

110. It is my understanding that the preamble of a patent claim can limit the scope of the claim. Assuming that the preamble of claim 14 is limiting, Tayloe teaches a method for down-converting an electromagnetic (EM) signal. For

example, Tayloe describes a "method and apparatus" involving "a simple and inexpensive product detector which facilitates the conversion of a signal to baseband." *See, e.g.*, Tayloe, 1:64-67, 2:1-14 (describing input signal f_1 as an RF or IF signal). As stated in the '177 patent, converting an RF signal to baseband is "down-converting" of "an electromagnetic signal." *See, e.g.*, '177 patent, Abstract; Tayloe, 1:10-13, 5:61-64 (method and apparatus "for generating baseband in-phase and quadrature signals from an RF or IF signal).

14.1 receiving an input signal at a first matched filtering/correlating module;

111. Tayloe's down-conversion circuitry receives an RF or IF input signal f_1. *See, e.g.*, Tayloe, 2:13-14. FIG. 3 below shows one example of receiving an input f_1 into circuitry that performs down-converting, outlined in red:



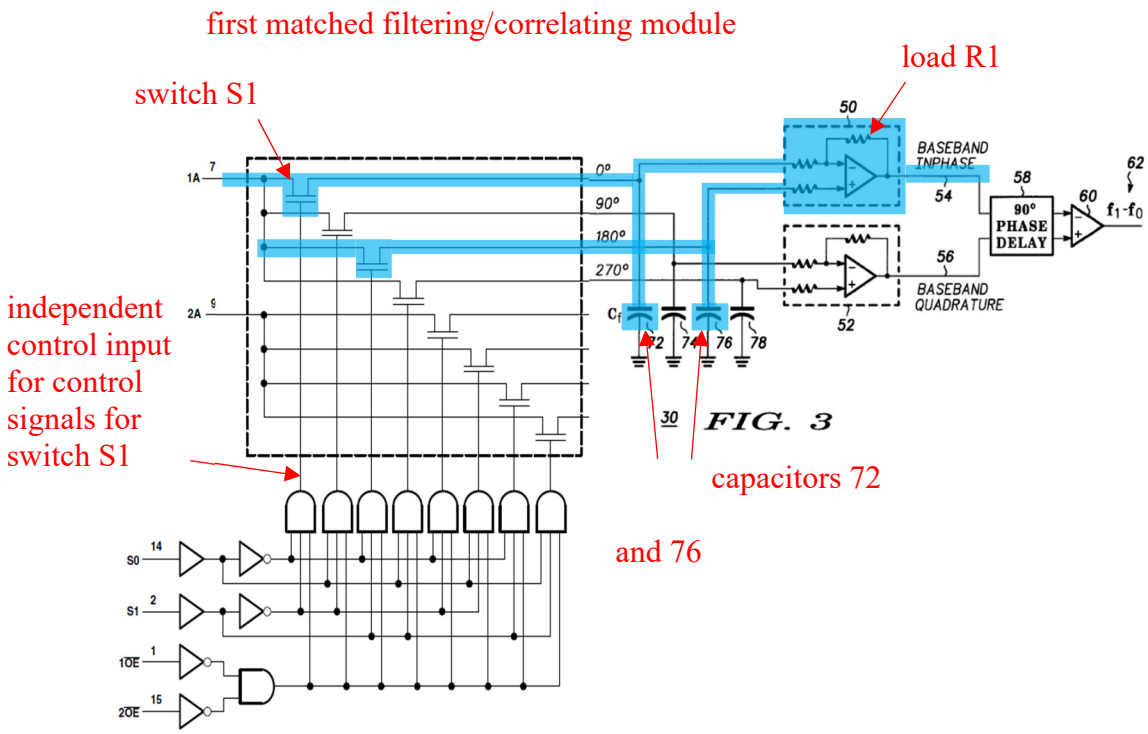
Tayloe, FIG. 3 + TI Datasheet (annotated)

In FIG. 3, the down-converting circuitry includes switches, integrating capacitors, and the differential summing amplifier circuitry (that includes a feedback resistor). *See, e.g.*, Tayloe, 2:8-12; *see also id*. FIG. 6.

112. As shown in FIG. 3 above, Tayloe's circuitry includes several down-converting circuits. The following describes how Tayloe renders claim 14 unpatentable under different constructions of the term matched filtering/correlating module. I first consider Patent Owner's proposed construction of the term "matched filtering/correlating module is considered. Then, later, I consider the plain meaning interpretation of matched filtering/correlating module.

(i) Patent Owner's Construction

113. Tayloe describes a first matched filtering/correlating module that performs down-conversion of an RF or IF signal into a baseband signal. The first matched filtering/correlating module is shown in Tayloe, FIG. 3 below, highlighted in light blue:



Tayloe, FIG. 3 (annotated)

The first matched filtering/correlating module includes a structure that, when operated, performs the method of Element 14.1 according to Patent Owner's constructions:

(a) linear, time-variant circuitry

114. Tayloe's circuit includes linear, time-variant circuitry. Tayloe's down-conversion circuitry includes resistors, capacitors, operational amplifier-based closed-loop amplifiers, a phase shifting network, a differencing amplifier, and a commutating switch, all of which a POSITA would have recognized as linear components to the extent that they are implemented ideally. A POSITA, therefore,

would have recognized the overall circuit as being linear in principle. *See, e.g.*, Tayloe, 1:67-2:2, 2:42-44, 4:9-13, 4:57-58. Tayloe's down-conversion receiver includes circuitry that is linear in an ideal sense, and approximate linear systems in practice.

115. Tayloe's down-conversion circuitry is time-variant because the switches reconfigure the circuit each time the commutating switch changes state. Specifically, Tayloe's down-conversion circuitry is a time-varying system because which capacitor is connected to the RF input signal changes over time (i.e., based on a periodic control signal). For example, in Tayloe, the switch 38 is controlled by a time-varying control signal $4f_0$. *See, e.g.*, Tayloe, 2:21-27, 3:62-65. *See, e.g.*, Tayloe, 3:62-65.

(b) that samples a modulated RF carrier signal at an aliasing rate using a switch with an independent control input driven by a control signal with a non-negligible, periodic aperture such that the samples, having non-negligible available energy, are accumulated and transferred to a load while the switch is closed while the switch is closed

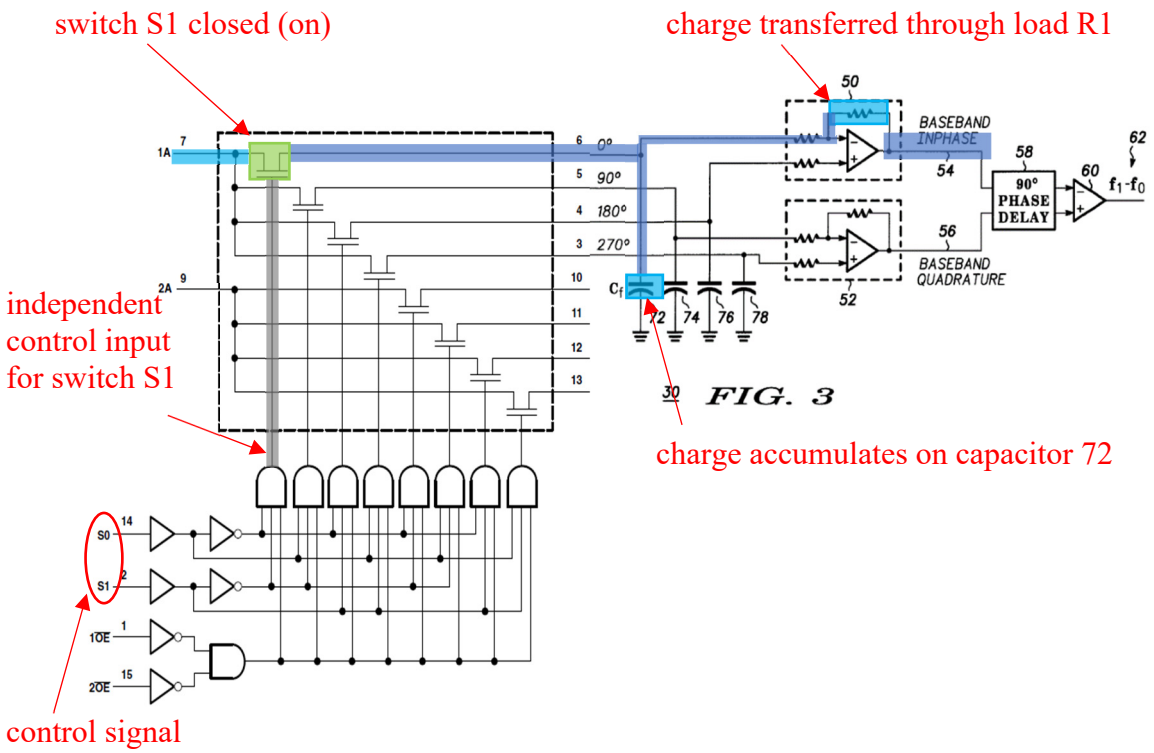
116. The input to Tayloe's circuit is a modulated RF carrier signal, referred to in Tayloe as f_1. *See, e.g.*, Tayloe, 2:13-14, 3:40-4:1 (describing f_1 as an input signal, f_0 as the carrier frequency, where f_1-f_0=0); *see also*, *id.*, 1:14-16. The Tayloe circuitry samples the input signal f_1 at an aliasing rate using a switch S1

with an independent control input driven by a control signal. *See, e.g.*, Tayloe, Abstract (describing a circuit "for converting a signal to baseband that includes a commutating switch which serves to sample an RF waveform), 3:48-54 (describing that "the carrier signal frequency is exactly equal to f_0," and "four evenly spaced samples will continuously be taken by the action of the Tayloe Product Detector"); *see also*, *id*., 2:18-19 ("The rate at which commutating switch 38 operates is controlled by a signal present at control input 40."). With Tayloe's control signal of $4f_0$, each switch is closed once per period defined by $4f_0$. When the switch is closed, a sample of the RF input signal is taken (accumulated and transferred to the load). Because Tayloe's direct-conversion receiver includes four switches (the four switches in TI's demux), the sampling is performed by each switch at rate equal to the carrier frequency f_0 (consider $f_0 = 4f_0/4$).

117. The '177 patent, allegedly "contrary to conventional wisdom," relies on under-sampling or "aliasing the EM signal." '177 patent, 26:22-35 (describing that the "carrier is not the item of interest"). The '177 patent defines the aliasing rate as "equal to, or less than, twice the frequency of the EM carrier signal." '177 patent, 29:59-61. Likewise, in Tayloe, the aliasing rate is equal to the carrier signal f_0, which is "less than" twice the frequency of the EM carrier signal. *See, e.g.*, Tayloe, 3:48-54. Each switch of the four switches periodically turns on for a

quarter of a $1/f_0$ period and turns off for the rest of the period, so it samples the modulated RF carrier signal at an aliasing rate of f_0.

118. For example, as shown in FIG. 3 below, the Tayloe circuitry samples the input signal f_1 using a control signal derived from the local oscillator $4f_0$ to control switch S1:



Tayloe, FIG. 3 with TI Datasheet (annotated)

As shown in FIG. 3 above, Tayloe's circuit includes a switch S1 with an independent control input driven by a control signal at an aliasing rate f_0.

119. The control signal samples using a non-negligible, periodic aperture. Tayloe teaches that sampling is done by closing the switch S1 for substantially 90

degrees at the frequency of the input signal f_1. The switch remains "closed at each of the four outputs for substantially 90 degrees at the frequency of the input signal." *See, e.g.*, Tayloe, 2:28-31. The aperture period (the duration when the switch is closed) is periodic because the aperture period is controlled by a periodic signal derived from $4f_0$.

120. Tayloe also explains that the aperture period is non-negligible. For example, Tayloe explains that "the control signal input to control input 40 is substantially equal to four times the local oscillator frequency," and as a result, "input 36 is switched to each of the four outputs substantially once during each period of the input signal f_1." *See, e.g.*, Tayloe, 2:21-26. Therefore, the aperture period is equal to a quarter period f_1, which is certainly non-negligible.

121. In addition, the samples, having non-negligible energy, are accumulated and are transferred to a load while the switch is closed. For example, as explained by Tayloe, during the time that the switch S1 connects input 36 to output 42, charge builds up on the capacitor 72. *See, e.g.*, Tayloe, 2:32-38. As switches of the demux cycle through connecting the four outputs, "capacitors 72-78 charge to voltage values substantially equal to the average value of the input signal during their respective quadrants." Tayloe, 2:38-44. The aperture period is sufficiently long in duration for an average value of the sample during that time period to be accumulated on the capacitor. *See, e.g.*, *id.*; *see also id.*, 2:45-55

(describing that the output of each phase "represents the average value of the input signal during the [corresponding] quarter wave of the period"). The capacitors charging to "the average value of the input signal" is how Tayloe satisfies the samples, having non-negligible available energy, being accumulated.

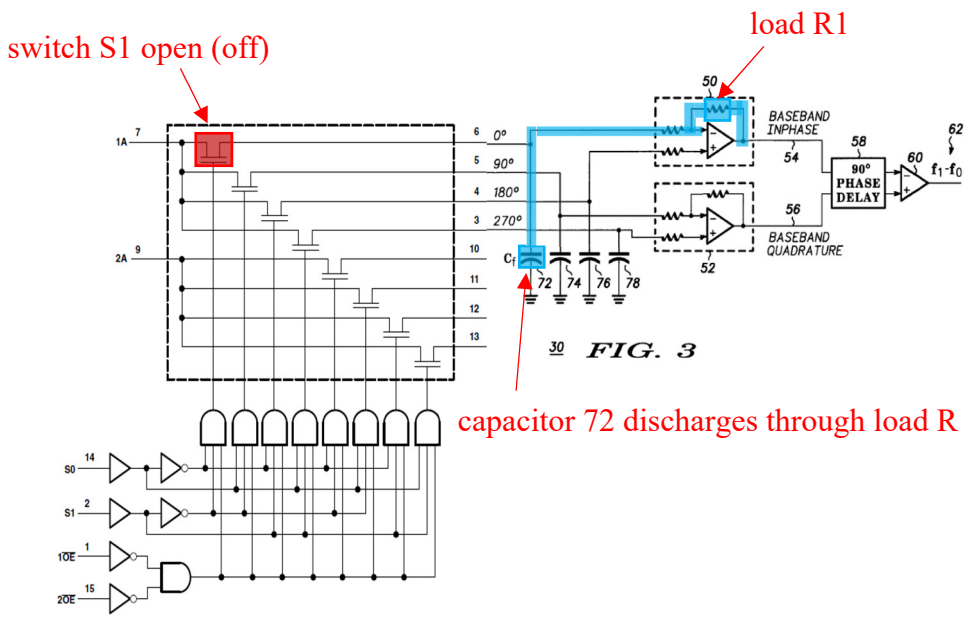
122. At the same time, while the switch S1 is closed, energy from the samples is also transferred to the load R1. Thus, while the switch S1 is closed, a non-negligible available energy—indeed, the entirety of the sample—is accumulated on the capacitor 72 and transferred to the load R1.

123. In addition, it is worth noting that Tayloe includes capacitors in its circuit deliberately. The purpose of capacitors, in general, is to store (or accumulate) energy or charge. If the capacitors of Tayloe stored only a negligible amount of energy, they could be removed from the circuit entirely with only a negligible change in the circuit's performance. That Tayloe sought to include these capacitors in his circuit, and speaks to their function repeatedly in the specification of his patent, indicates that the capacitors cannot be neglected. It follows, therefore, that the capacitors of Tayloe, such as capacitor 72, accumulates a non-negligible amount of available energy during the aperture period.

(c) and discharged through the load while the

switch is open,

124. Tayloe's capacitor 72 discharges when the switch is open. A POSITA reading Tayloe would have recognized that Tayloe's capacitor 72 inherently discharges through the feedback resistor when the switch is open. Tayloe teaches that, when the switch 38 is open, charged capacitor 72 will discharge through the load (*i.e.*, through the resistor shown in the figure below). *See, e.g.*, Tayloe, 2:56-57, FIG. 3. FIG. 3 is shown below illustrating the discharge path of capacitor 72 when the switch 38 is open to output 42:



Tayloe, FIG. 3 (annotated).

125. A POSITA would recognize that the triangle symbol in each of 50 and 52 is an operational amplifier with a high open-loop DC gain, and that 50 and 52 each implement a feedback system wherein the feedback through the resistor

connected between the operational amplifier's output and negative input terminal causes the resistance at the negative input terminal node to be extremely low (typically significantly less than a few ohms). Consequently, a POSITA would recognize that the input resistance to ground from each the top inputs of 50 and 52 is approximately equal to the resistance of the top-left resistor. Moreover, a POSITA would know that in practical implementations of 50 and 52, such resistors would typically have resistances on the order of kilo-ohms or less. Therefore, capacitors 72 and 74 discharge through these resistors when their corresponding switches are open.

(d) thereby transferring available real power from the modulated RF carrier signal to the load and

126. Tayloe teaches that the charge accumulated on each capacitor discharges through the load and transfers available real power from the modulated input signal f_1 to the load. As mentioned before, "[d]uring the time that commutating switch 38 connects input 36 to output 42, charge builds up on capacitor 72. Likewise, during the time commutating switch 38 connects input 36 to output 44, charge builds up on capacitor 74. The same principle holds true for capacitors 76 and 78 when commutating switch 38 connects input 36 to outputs 46 and 48 respectively. As commutating switch 38 cycles through the four outputs, capacitors 72-78 charge to voltage values substantially equal to the average value

of the input signal during their respective quadrants." Tayloe, 2:33-44; *see also id*., 2:46-55 (describing each output 42, 44, 46, and 48 being representative of the average value of the input signal at corresponding quarter waves of the period). As mentioned above, capacitors 72 and 74 discharge through the top-left resistors in 50 and 52, respectively. In each case, substantially all the discharged current also passes through the corresponding feedback resistor (because operational amplifier terminals have high impedance by design). Therefore, the capacitor discharges electrical charge through the load (feedback resistor), which a POSITA would know is available real power from the RF carrier signal.

127. The charge (or energy) that accumulates on the capacitor 72 and is transferred through the load R1 translates to available real power. First, it is the available power because it forms the measurable output signal of the amplifier. The power is "real" in the sense that it is equal at any given time instant to the product of the resistance value of the resistor and the square of the current through the resistor at that time instant. Both of these quantities in the product are real numbers (i.e., they are not so-called complex numbers with so-called imaginary components), so their product, i.e., the power, is real.

(e) producing a down-converted signal with enhanced signal-to-noise power ratio

i. producing a down-converted signal

128. Tayloe teaches producing a down-converted signal. For example, according to Tayloe, the "in-phase and quadrature signals that result represent the signal of interest at baseband." Tayloe, 2:2-3; *see also id*., 2:38-44. "Summing amplifier 50 differentially sums the 0 degree output and the 180 degree output, **thereby producing baseband in-phase signal 54**." Tayloe, 2:56-62 (also discussing the production of the baseband quadrature signal 56) (emphasis added).

ii. with enhanced signal-to-noise power ratio

129. Tayloe teaches that the produced baseband in-phase signal has an enhanced signal-to-noise power ratio (or SNR for short). First, Tayloe teaches that the capacitors perform averaging and act as integrators. *See, e.g.*, Tayloe, 2:38-44 ("As commutating switch 38 cycles through the four outputs, capacitors 72-78 charge to voltage values substantially equal to the average value of the input signal during their respective quadrants. Each of the capacitors functions as a separate integrator, each integrating a separate quarter wave of the input signal."). A POSITA would have recognized that the averaging performed by the integrators reduces noise on the signal because averaging attenuates high-frequency noise and interference while preserving the desired signal component. In other words, integrating or averaging is a form of low-pass filtering, which removes noise from the resulting signal, thereby resulting in an improved SNR.

130. Furthermore, note that one of the stated benefits of Tayloe is an improvement to noise. Tayloe states that its circuit "can exhibit less than 1 dB of conversion loss, which is 6-7 dB improvement over the typical conversion loss of 7-8 dB in the prior art. **This 6-7 dB conversion loss improvement translates into a 6-7 dB improvement in overall receiver noise figure**. The noise figure improvement results in substantial receiver performance gains, in part because a pre-amplifier may become unnecessary as a result." Tayloe, 3:6-13 (emphasis added). A POSITA would have recognized that the integrator circuit(s) of Tayloe (along with other aspects of Tayloe) produce a down-converted signal with enhanced SNR. The 6-7 dB improvement corresponds to a SNR improvement (expressed in terms of decibels, which is a monotonically increasing function of the signal to noise power ratio).

131. One way that Tayloe achieves enhanced SNR is by matching or correlating the local oscillator frequency f_0 with the carrier frequency of the received input signal f_1. Tayloe describes, in one embodiment, that the input signal f_1 is a carrier signal frequency "exactly equal to f_0". *See, e.g.*, Tayloe, 3:48-53. In that case, the input signal f_1 is synchronized to the carrier frequency f_0. As discussed above in the claim construction section, the correlation between the carrier signal frequency and the input signal can result in an improved SNR. *See,*

supra, §II.C.2. Thus, Tayloe's matched filtering/correlating module results in an enhanced SNR.

(ii) Plain Meaning Construction

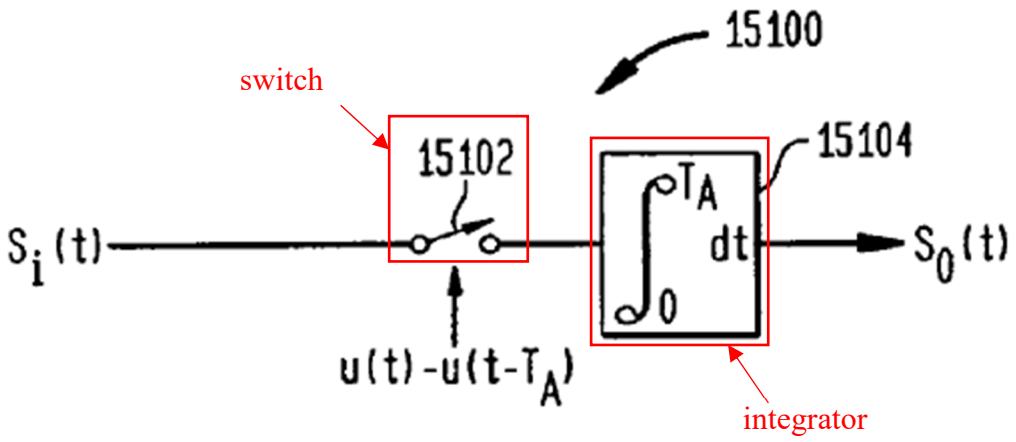
132. As will be described below, under the plain meaning construction, Tayloe's switch S1, and capacitor 72, controlled by control signal with frequency f_0, is the first matched filtering/correlating module. Tayloe's switch S3 and capacitor 76, controlled by control signal with frequency f_0, is the second matched filtering/correlating module. As shown in example FIG. 153 of the '177 patent, at least one embodiment of the matched filtering/correlating modules includes a switch controlled by a control signal, and a capacitor that acts as an integrator. *See, e.g.*, '177 patent, 134:32-51 ("Capacitor 15306 integrates the output of switching module 15304 and accumulates the energy of the processed portions of the received carrier signal."), FIG. 153.

133. Likewise, an embodiment of the down-conversion circuitry of Tayloe includes a switch S1 that is controlled by a control signal that is synchronized to the carrier frequency f_0. *See, e.g.*, 3:48-53 (describing "the carrier signal frequency is exactly equal to f_0"). Similarly, the other switches within the commutating switch are also controlled by a control signal that is synchronized to the carrier frequency f_0. *Id*. This is illustrated in FIG. 4 of Tayloe along with the explanation that "[o]utput 42 represents the average value of the input signal during the first

quarter wave of the period, and is termed the 0 degree output." Tayloe 2:45-55. "Output 44 represents the average value of the input signal during the Second quarter wave of the period, and is termed the 90 degree output. Output 46 represents the average value of the input signal during the third quarter wave of the period, and is termed the 180 degree output. Output 48 represents the average value of the input signal during the fourth quarter wave of the period, and is termed the 270 degree output." Tayloe 2:45-55. The FIG. 4 waveform is that of the received RF input signal, so FIG. 4 and the associated explanation above is only possible if the independent control signals within the commutating switch are synchronized to the carrier of the received RF input signal.

134. The '177 patent describes that the "matched filter/correlator is generally referred to as a finite time integrator." '177 patent, 132:37-38. The '177 patent states that a finite time integrator "can be implemented with, for example, a switching device controlled by a train of pulses having apertures substantially equal to the time interval defined for the waveform." '177 patent, 132:38-42. As shown in the '177 patent, FIGS. 151 and 153, the matched filtering/correlating module includes a switch with a capacitor that integrates:

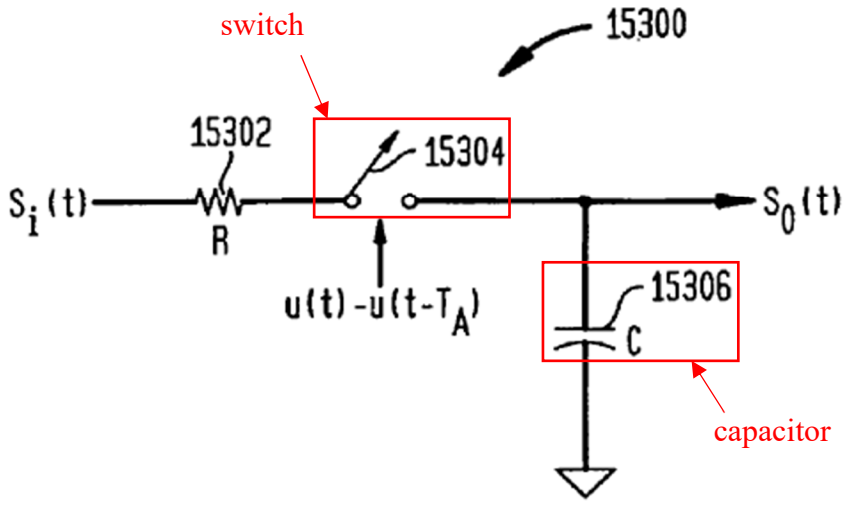
FIG. 151



’177 patent, FIG. 151 (annotated)

The ’177 patent describes FIG. 151 as showing a “finite time integrating system.” ’177 patent, 133, 22-23.

FIG. 153

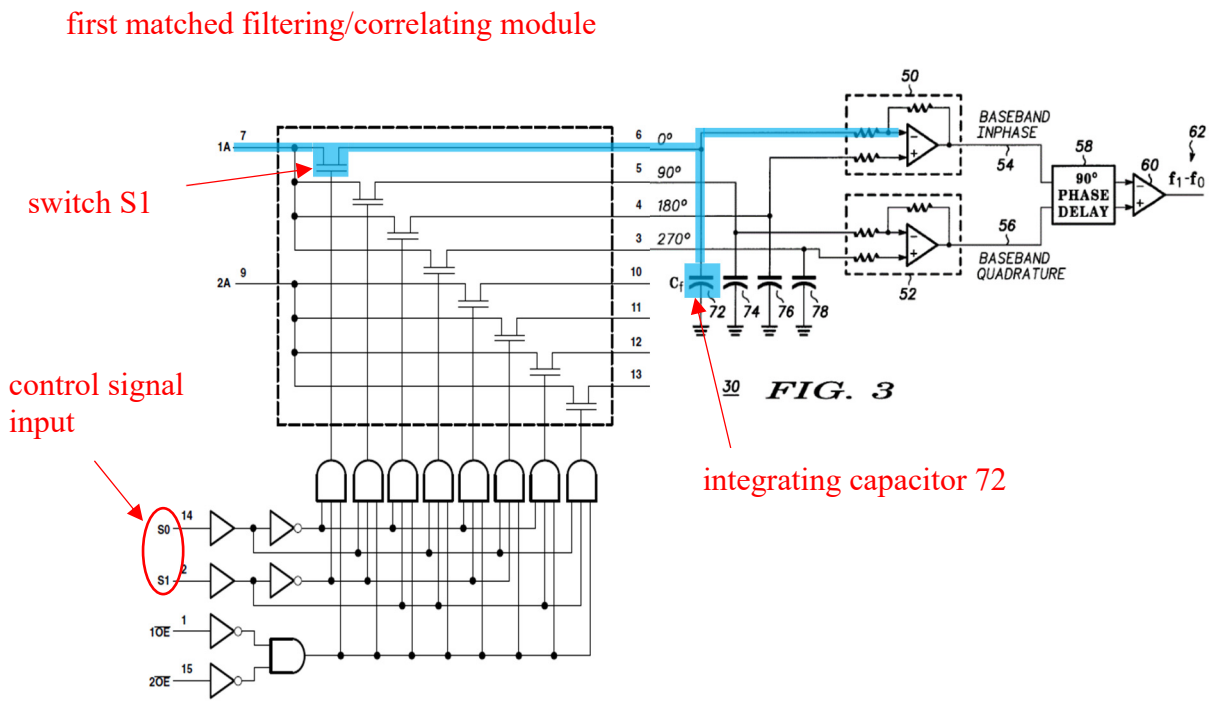


’177 patent, FIG. 153 (annotated)

135. The ’177 patent describes FIG. 153 as “an RC processing system,” which can be used to implement the method of “down-converting an electromagnetic signal using a matched filtering/correlating operation.” ’177 patent, 133:59-61, 134:31-34. As described by the ’177 patent, “Capacitor 15306 integrates the output of switching module 15304 and accumulates the energy of the processed portions of the received carrier signal.” ’177 patent, 134:45-48. Among the common characteristics of the matched filtering/correlating module embodiments of the ’177 patent is that the correlation signal must be synchronized to the input signal’s carrier frequency. As examples, Column 145 of '177 states that “the example matched filter/correlator of FIG. 171 operates in synchronism with the half sine pulse $S_i(t)$ over the aperture T_A,” and this “synchronism” is depicted in several of the figures in '177 including but not limited to Fig. 72, Fig. 157, Fig. 158, Fig. 162, Fig. 166, Fig. 182, Fig. 184, and Fig. 193.

136. The circuitry of Tayloe includes a switch S1 controlled by a control signal derived from f_0 and a capacitor 72 that performs integration, which is the same structure described by the ’177 patent. For example, Tayloe describes that each of the capacitors “functions as a separate integrator, each integrating a separate quarter wave of the input signal.” Tayloe, 2:42-45; *see also id.*, 1:67-2:2, 3:54-57, 4:46-63 (describing that “resistor/capacitor pairs also form integrators.”).

Thus, Tayloe describes a first matched filtering/correlating circuit according to the plain-and-ordinary meaning construction, as shown in FIG. 3 below, in light blue:



Tayloe FIG. 3 + TI Datasheet (annotated)

137. One way that Tayloe achieves enhanced SNR is by matching or correlating the local oscillator frequency f_0 with the carrier frequency of the received input signal f_1. Tayloe describes, in one embodiment, that the input signal f_1 is a carrier signal frequency "exactly equal to f_0". *See, e.g.*, Tayloe, 3:48-53. In that case, the input signal f_1 is synchronized to the carrier frequency f_0. As discussed above in the claim construction section, the correlation between the carrier signal frequency and the input signal can result in an improved SNR. *See, supra*, §II.C.2. Thus, Tayloe's matched filtering/correlating module results in an

enhanced SNR. As discussed above, in at least one embodiment of Tayloe, the control signal that controls the switch S1 is synchronized to the carrier of the received RF input signal because each switch is closed exactly once period of the received RF input signal's carrier frequency. Thus, Tayloe provides a matched filtering/correlator module consistent with the plain-and-ordinary meaning of the term.

14.2 down converting said input signal at said first matched filtering/correlating module according to a first control signal and outputting a first down-converted signal;

138. Tayloe teaches or renders obvious element 14.2. *See supra* 14.1. For example, Tayloe teaches that the matched filtering/correlating module samples the input signal f_1 according to the control signal derived from the local oscillator f_0. *See, e.g.*, Tayloe, 2:21-55. The switch "remains closed at each of the four outputs for substantially 90 degrees at the frequency of the input signal," during which time charge builds on each capacitor. *See, e.g.*, *id*. As the switches "cycle through the four outputs, capacitors 72-78 charge to voltage values substantially equal to the average value of the input signal during their respective quadrants." *See, e.g.*, *id*. "Summing amplifier 50 differentially sums the 0 degree output and the 180 degree output, thereby producing baseband in-phase signal 54." *See, e.g.*, *id*., 2:57-59. The first control signal turns the first switch on for a quarter period of the

carrier of the received RF input signal, i.e., for one period of the $4f_0$ control signal, corresponding to the 0° period.

139. Under a plain-and-ordinary construction, Tayloe's first matched filtering/correlating module outputs a first in-phase down-converted signal representative of the first quarter wave period (referred to as the 0 degree output). *See, e.g.*, Tayloe, 2:46-48. This 0 degree output is a first down-converted signal because energy from the received RF input signal is transferred to the capacitor only when the carrier signal is positive, i.e., "during the first quarter wave of the period" Tayloe 2:47, thereby aliasing the RF input signal to baseband. This portion of the in-phase baseband signal (first down-converted signal) is later combined with the 180 degree output from the third quarter wave of the period (second down-converted signal) to output a first channel down-converted signal. *See, e.g.*, Tayloe, 2:50-53, 2:56-67.

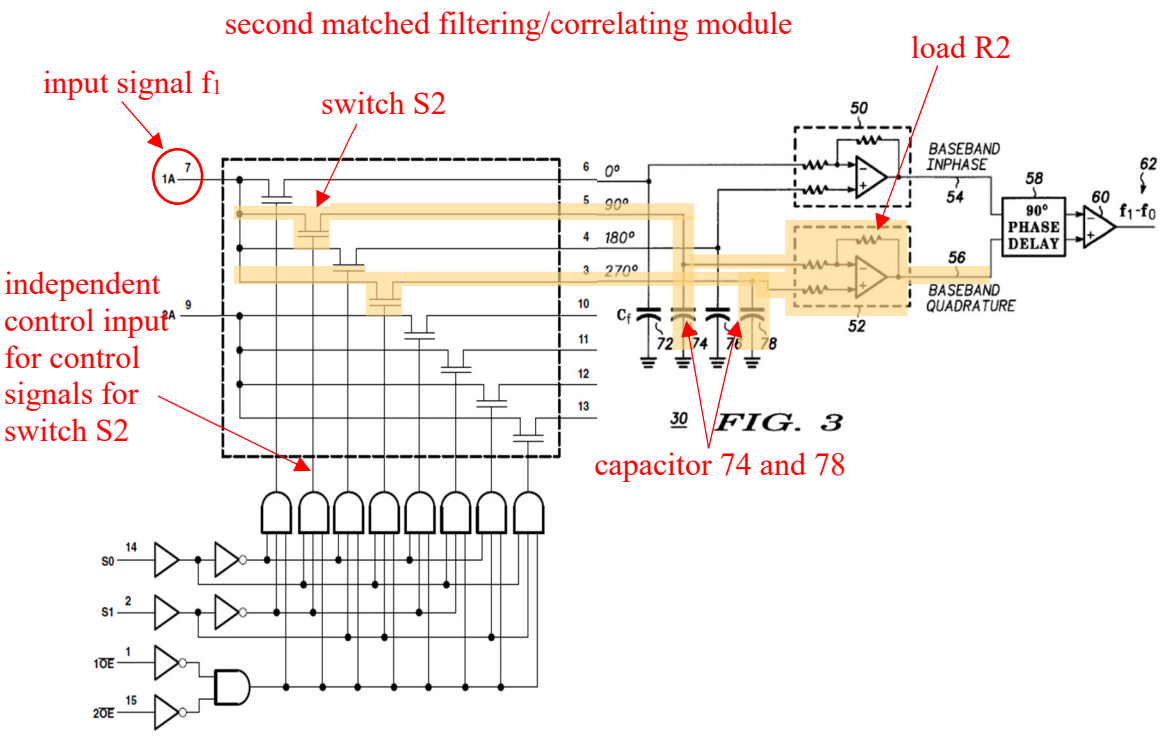
140. In 180 degree output case, energy from the received RF input signal is transferred to the capacitor only when the carrier signal is negative, specifically "during the third quarter wave of the period" Tayloe 2:51-52, thereby aliasing the RF input signal to baseband. The 0 degree output corresponds to energy transferred from the RF input signal between points 105 and 110 of Tayloe Fig. 4, and the 180 degree output corresponds to energy transferred from the RF signal between points 115 and 120 of Tayloe Fig. 4. As can be see from Tayloe Fig. 4, the portion of the

waveform between points 115 and 120 is the negative of that between points 105 and 110, so it follows that the 180 degree output is the negative of the 0 degree output. Summing amplifier 50 outputs an amplified version of the 0 degree output minus the 180 degree output, so the output of 50 is also a first down-converted signal.

14.3 receiving said input signal at a second matched filtering/correlating module;

(i) Patent Owner's Construction

141. Tayloe describes a second matched filtering/correlating module that performs down-conversion of an RF or IF signal into a baseband signal. The second matched filtering/correlating module is shown in Tayloe, FIG. 3 below, in orange. Tayloe teaches receiving input f_1 into a second matched filtering/correlating module, as shown in FIG. 3:

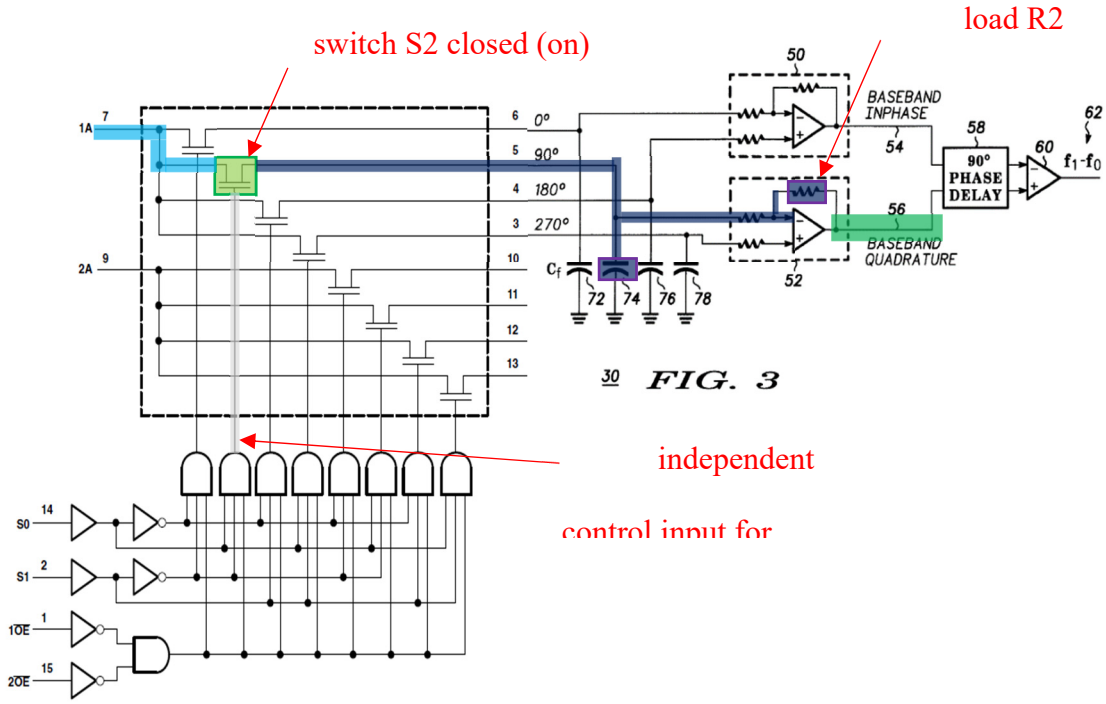


Tayloe, FIG. 3 + TI Datasheet (annotated)

142. The second matched filtering/correlating module is configured the same as and operates the same as the first matched filtering/correlating module. *See, supra*, Element Ground 1, 14.1. Like the first matched filtering/correlating module, the second module includes a switch S2 with an independent control input, capacitor 74, and differential summing amplifier 52 with feedback resistor R2 (the load). The output of the second matched filtering/correlating module is a baseband quadrature signal 56. *See, e.g.*, Tayloe, 2:8-12; *see also* text accompanying FIG. 6. Therefore, the second matched filtering/correlating module satisfies both Patent Owner's construction and the Plain Meaning Construction for

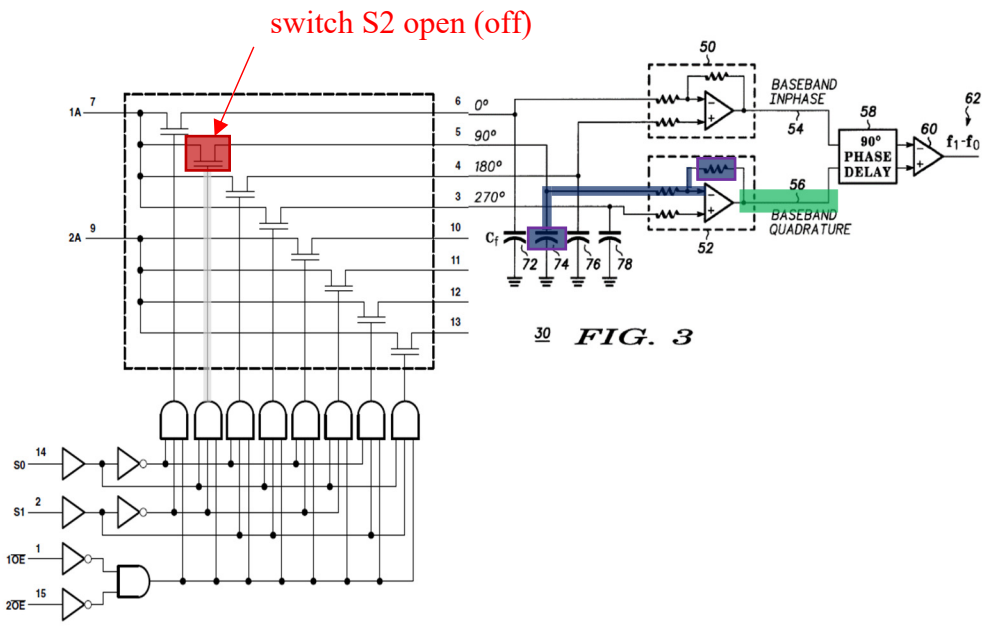
the same reasons as the first matched filtering/correlating module. *See supra* Ground 1, 14.1.

143. Beginning with the Patent Owner's constructions, in the combination of Tayloe and TI SN74CBT3253, the switch S2 is a transistor of the demultiplexer that has its own control input, as shown in the annotated figure below. When the switch is closed to the 90° output, charge is accumulated on the capcitor 74 and flows through the feedback resistor R2. For example, as shown in FIG. 3 below, the Tayloe circuitry samples the input signal f_1 using a control signal derived from the local oscillator $4f_0$ to control switch S2:



Tayloe FIG. 3 + TI-Datasheet (TI-1005, 2) (annotated)

When switch is open to the 90° output 44, the accumulated charge on capacitor 74 discharges though the feedback resistor R, as shown below:



Tayloe, FIG. 3 (annotated)

144. Summing amplifier 52 "differentially sums the 90 degree output and the 270 degree output, thereby producing baseband quadrature signal 56." *See, e.g.*, Tayloe, 2:60-62.

145. As shown in FIG. 3 above, Tayloe's circuit includes a switch S2 with an independent control input driven by a control signal at an aliasing rate f_0. The control signal samples using a non-negligible, periodic aperture by closing the switch S1 for substantially 90 degrees at the frequency of the input signal f_1. The switch remains "closed at each of the four outputs for substantially 90 degrees at the frequency of the input signal." *See, e.g.*, Tayloe, 2:28-31. That the aperture

period is periodic is self-evident. But Tayloe explains that the aperture period is non-negligible. For example, Tayloe explains that "the control signal input to control input 40 is substantially equal to four times the local oscillator frequency," and, as a result, "input 36 is switched to each of the four outputs substantially once during each period of the input signal f_1." *See, e.g.*, Tayloe, 2:21-26.

146. In addition, the samples, having non-negligible energy, are accumulated and are transferred to a load while the switch is closed. For example, as explained by Tayloe, during the time that the switch S2 connects input 36 to output 44, charge builds up on the capacitor 74. *See, e.g.*, Tayloe, 2:32-38. As switches of the demux cycle through connecting the four outputs, "capacitors 72-78 charge to voltage values substantially equal to the average value of the input signal during their respective quadrants." Tayloe, 2:38-44. The aperture period is sufficiently long in duration for an average value of the sample during that time period to be accumulated on the capacitor. *See, e.g.*, *id.*; *see also id.*, 2:45-55 (describing that the output of each phase "represents the average value of the input signal during the [corresponding] quarter wave of the period"). The capacitors charging to "the average value of the input signal" is the samples, having non-negligible available energy, being accumulated. At the same time, while the switch S1 is closed, energy from the samples is transferred to the load R2. Thus, while the switch S1 is closed, a non-negligible available energy—indeed, the

entirety of the sample—is accumulated on the capacitor 74 and transferred to the load R2.

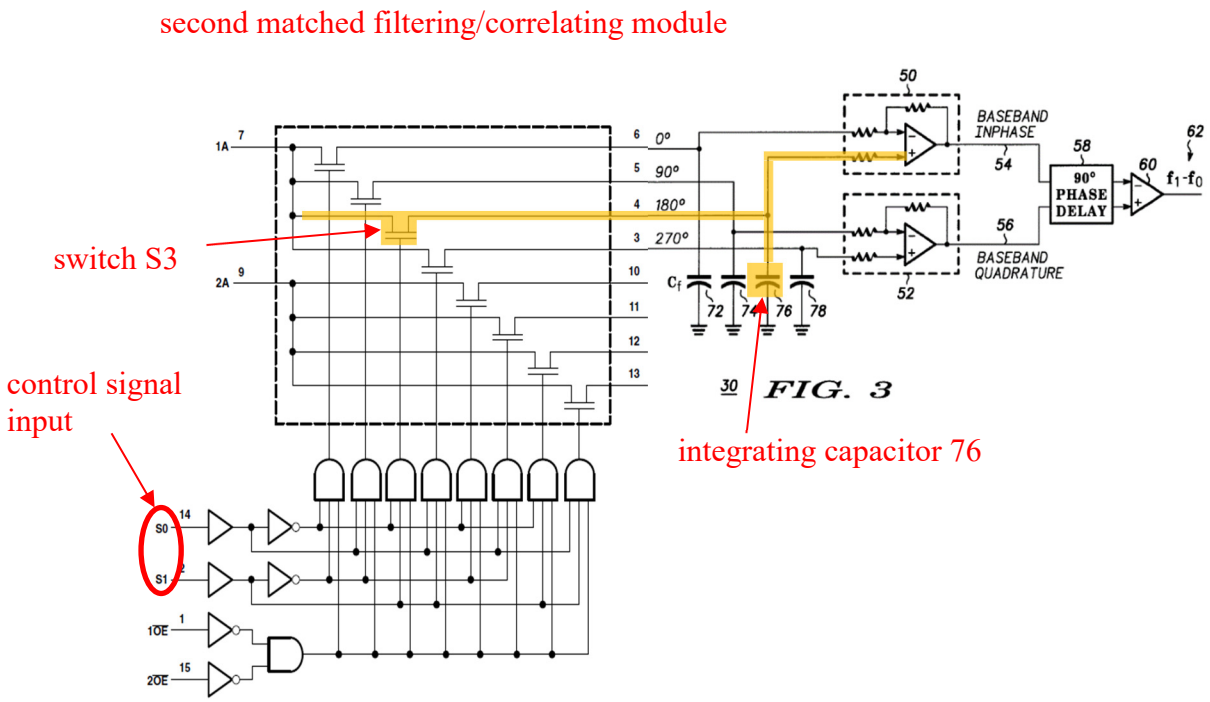
147. In addition, it is worth noting that Tayloe includes capacitors in its circuit deliberately. The purpose of capacitors, in general, is to store (or accumulate) energy or charge. If the capacitors of Tayloe stored only a negligible amount of energy, they could be removed from the circuit entirely with only a negligible change in the circuit's performance. That Tayloe sought to include these capacitors in his circuit, and speaks to their function repeatedly in the specification of his patent, indicates that the capacitors cannot be neglected. It follows, therefore, that the capacitors of Tayloe, such as capacitor 72, accumulates a non-negligible amount of available energy during the aperture period.The available energy during the aperture period is transferred to the load. The charge accumulated and transferred to the load translates to real physical power.

148. And likewise to the first matched filtering/correlating module, the second amtched filtering/correlating module results in an enhanced signal-to-noise power ratio.

(ii) Plain Meaning Construction

149. Tayloe teaches a second matched filtering/correlating module based on the plain-and-ordinary meaning construction, as well. The second matched filtering/correlating circuitry of Tayloe includes a switch S3 controlled by a control

signal and a capacitor 76 that performs integration. For example, Tayloe describes that each of the capacitors "functions as a separate integrator, each integrating a separate quarter wave of the input signal." Tayloe, 2:42-45; *see also id.*, 1:67-2:2, 3:54-57, 4:46-63 (describing that "resistor/capacitor pairs also form integrators."). Thus, the first matched filtering/correlating circuit of Tayloe is shown in FIG. 3 below, highlighted in orange:



Tayloe FIG. 3 + TI Datasheet (annotated)

150. The down-conversion circuitry of Tayloe includes a switch S2 that is controlled by a control signal that is correlated to the carrier frequency f0, and similarly for the other switches within the commutating switch. *See, e.g.*, 3:48-53 (de-scribing "the carrier signal frequency is exactly equal to f0"); FIG. 4, 2: 46-55

("Output 44 represents the average value of the in-put signal during the Second quarter wave of the period, and is termed the 90 degree output."). The FIG. 4 waveform is that of the received RF input signal, so FIG. 4 and the associated explanation above is only possible if the independent control signals within the commutating switch are synchronized to the carrier of the received RF input signal.

151. The circuitry of Tayloe includes a switch S2 controlled by a control signal derived from f_0 and a capacitor 72 that performs integration. For example, Tayloe describes that each of the capacitors "functions as a separate integrator, each integrating a separate quarter wave of the input signal." Tayloe, 2:42-45; *see also id*., 1:67-2:2, 3:54-57, 4:46-63 (describing that "resistor/capacitor pairs also form integrators."). Thus, Tayloe describes a second matched filtering/correlating circuit according to the plain-and-ordinary meaning construction, as shown in FIG. 3 above.

152. As discussed above, the control signal that controls the switch S3 is equal to f_0. And as described by Tayloe, in embodiments, $f_1 = f_0$. In that case, the local oscillator control signal is synchronized, *i.e.*, matched or correlated, with the input signal carrier.

14.4 down-converting said input signal at said second matched filtering/correlating module according to a second control signal and outputting a second down-converted signal; and

153. *See supra* Ground 1, 14.2-3. Tayloe teaches or renders obvious element 14.4. For example, Tayloe teaches that the matched filtering/correlating module samples the input signal f_1 according to the control signal derived from the local oscillator f_0. *See, e.g.*, Tayloe, 2:21-55. The switch "remains closed at each of the four outputs for substantially 90 degrees at the frequency of the input signal," during which time charge builds on each capacitor. *See, e.g.*, *id*. As the switches "cycle through the four outputs, capacitors 72-78 charge to voltage values substantially equal to the average value of the input signal during their respective quadrants." *See, e.g.*, *id*. "Summing amplifier 50 differentially sums the 0 degree output and the 180 degree output, thereby producing baseband in-phase signal 54." *See, e.g.*, *id*., 2:57-59. The first control signal turns the first switch on for a quarter period of the carrier of the received RF input signal, i.e., for one period of the $4f_0$ control signal, corresponding to the 0° period.

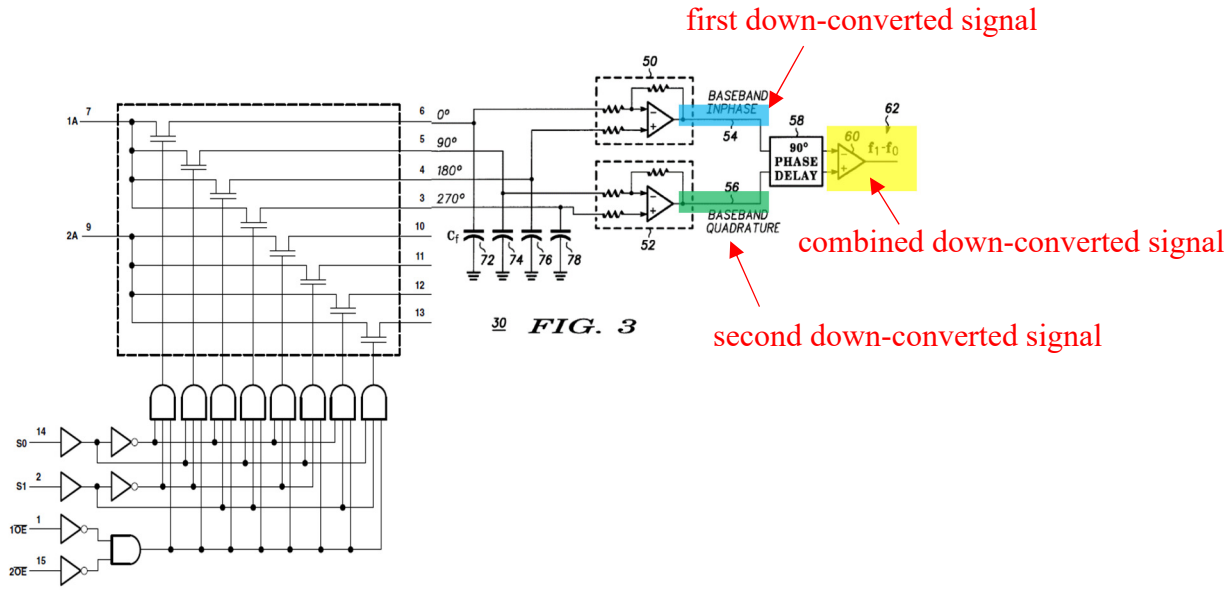
154. Under a plain-and-ordinary construction, Tayloe's second matched filtering/correlating module outputs a second in-phase down-converted signal representative of the third quarter wave period (referred to as the 180 degree output). *See, e.g.*, Tayloe, 2:44-55. This 180 degree output is a second down-converted signal because energy from the received RF input signal is transferred to the capacitor only when the carrier signal is negative, i.e., "during the third quarter wave of the period" Tayloe 2:50-53, thereby aliasing the RF input signal to

baseband. This portion of the in-phase baseband signal (second down-converted signal) is later combined with the 0 degree output from the first quarter wave of the period (first down-converted signal) to output a first channel down-converted signal. *See, e.g.*, Tayloe, 2:50-53, 2:56-67; *see also* Ground 1, Element 14.5, *infra*.

14.5 combining said second down-converted signal and said first down-converted signal to output a first channel down-converted signal.

(i) ParkerVision's Construction

155. Tayloe teaches element 14.5. For example, under ParkerVision's constructions, Tayloe describes that the baseband in-phase signal 54 and the baseband quadrature signal 56 are combined by the summing amplifier 60, as shown in FIG. 3. Tayloe, 2:65-67.

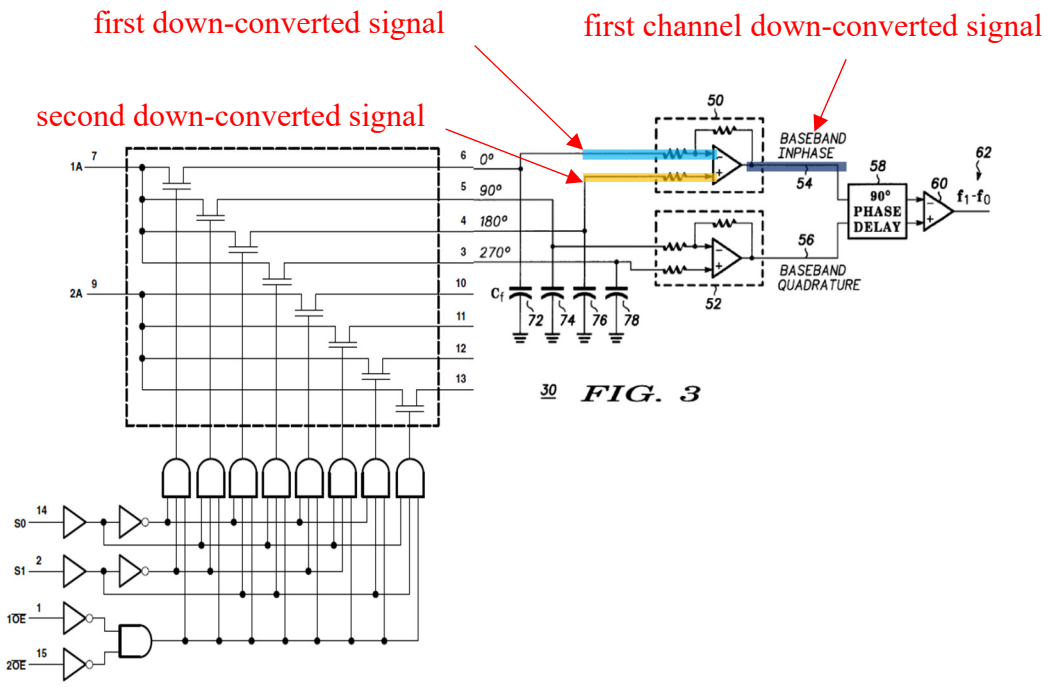


Tayloe, FIG. 3 + TI Datasheet (annotated)

The signal of interest 62 is a baseband signal where the input signal f_1 has the carrier signal f_0 removed. In cases where the carrier signal f_0 is tuned to the input signal f_1, the signal of interest f_1-f_0 is exactly at baseband, meaning that not even an intermediate frequency carrier is present.

(ii) Plain Meaning Construction

156. Tayloe teaches element 14.5 under TI's construction, where the first channel down-converted signal is the I-phase down-converted signal, for example. Tayloe teaches that the 0 degree output and the 180 degree output are differentially summed and amplified to output an in-phase (I-phase) down-converted signal, which is the first-channel down-converted signal. *See, e.g.*, Tayloe, 2:56-60 ("Summing amplifier 50 differentially sums the 0 degree output and the 180 degree output, thereby producing baseband in-phase signal 54."). This is shown in FIG. 3 below:



Tayloe FIG. 3 + TI Datasheet (annotated)

In the 180 degree output case, energy from the received RF input signal is transferred to the capacitor only when the carrier signal is negative, specifically "during the third quarter wave of the period" Tayloe 2:51-52, thereby aliasing the RF input signal to baseband. The 0 degree output corresponds to energy transferred from the RF input signal between points 105 and 110 of Tayloe Fig. 4, and the 180 degree output corresponds to energy transferred from the RF signal between points 115 and 120 of Tayloe FIG. 4. As can be see from Tayloe FIG. 4, the portion of the waveform between points 115 and 120 is the negative of that between points 105 and 110, so it follows that the 180 degree output is the negative of the 0 degree output. Summing amplifier 50 outputs an amplified version of the

0 degree output minus the 180 degree output, so the output of 50 is also a first down-converted signal.

B. GROUND 2A – Razavi Renders Claim 14 Obvious Under Patent Owner's Construction

1. Analysis

14.P A method for down-converting an electromagnetic signal, comprising:

157. To the extent that the preamble is limiting, Razavi teaches it. For example, Razavi teaches a circuit that when implemented down-coverts a 900 MHz electromagnetic signal to baseband. *See, e.g.*, Razavi, 1 (describing a "single-chip 900 MHz CMOS direct conversion receiver").

158. In Razavi, a radio frequency (RF) signal (centered at 900 MHz) is received at the input of a low noise amplifier (LNA), where the RF signal is amplified before it is directed to a mixer. *See, e.g.*, Razavi, 1:1-7, FIGS. 1-3. The mixer performs down-conversion of the radio frequency signal. *Id*. The "downconverted signal" can be directed to a baseband amplifier, like that shown in FIG. 5. *Id*., 2:21-22.

14.1 receiving an input signal at a first matched filtering/correlating module;

159. Razavi teaches element 14.1. The 900 MHz signal is received at the input Vin, Razavi, 1:1-3, shown in FIG. 2 below:

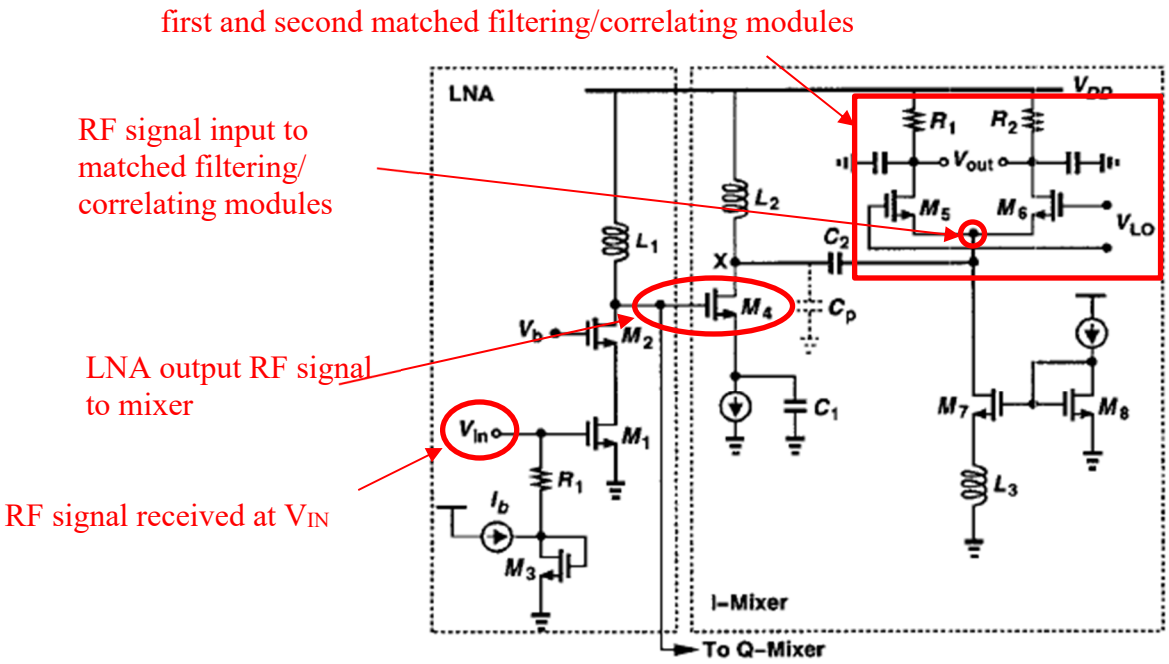


Fig. 2. LNA/mixer implementation.

Razavi, FIG. 2 (annotated)

According to Razavi, "Fig. 2 shows the implementation of the LNA and the quadrature mixers." Razavi, 1:16-17. FIG. 2 above shows the first and second matched filtering/correlating modules.

a. Patent Owner's Construction

(a) linear time-variant circuitry

160. Razavi's mixer includes circuitry that is well-modeled as linear and time-variant. First, as described by Razavi, the "mixer employs a single-balanced topology consisting of an input transistor M4 and a switching pair M5-M6." Razavi, 1:33-37. The mixer improves the "linearity of the voltage-to-current

conversion performed by the input stage" using capacitor C1 degenerates transistor M4 at 900 MHz." *Id*.

161. The mixer operates using a local oscillator LO that controls switches periodically via a divided-by-two version of the output signal from the oscillator shown in FIG. 2:

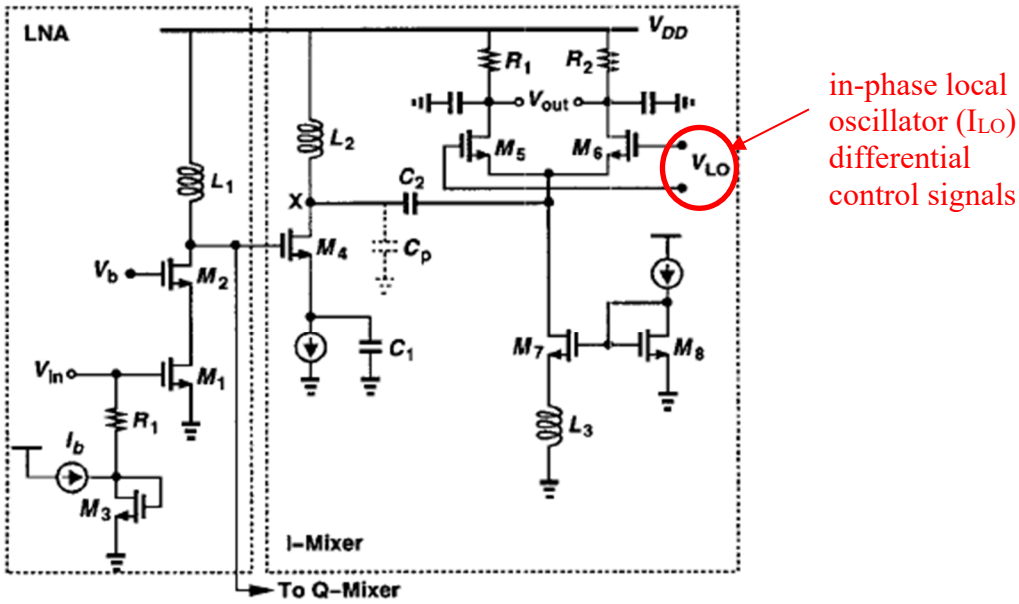


Fig. 2. LNA/mixer implementation.

Razavi, FIG. 2, (annotated)

162. In the example implementation shown in Razavi, the oscillator in FIG. 2 "operates at 1.8 GHz" and drives a divide-by-two circuit which generates the in-phase (I_{LO}) and quadrature (Q_{LO}) pairs of control signals shown in Fig. 1, both of which have a frequency of 900 MHz (which is an aliasing frequency in the terminology of '177 as it is less twice the highest frequency of the 900 MHz RF input signal). *See, e.g.*, Razavi, 2:11-14, FIGS. 1-3, 6. The differential control

signal, V_{LO}, in FIG. 2 corresponds to I_{LO} in FIG. 1, wherein the bottom V_{LO} signal is an inverted version of the top V_{LO} signal. *See, e.g.*, Razavi, FIG. 2. FIG. 1 is shown below:

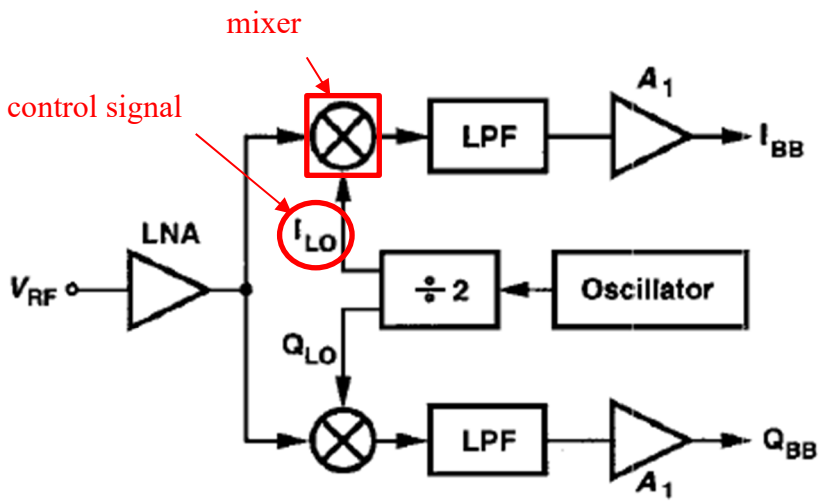


Fig. 1. Receiver architecture.

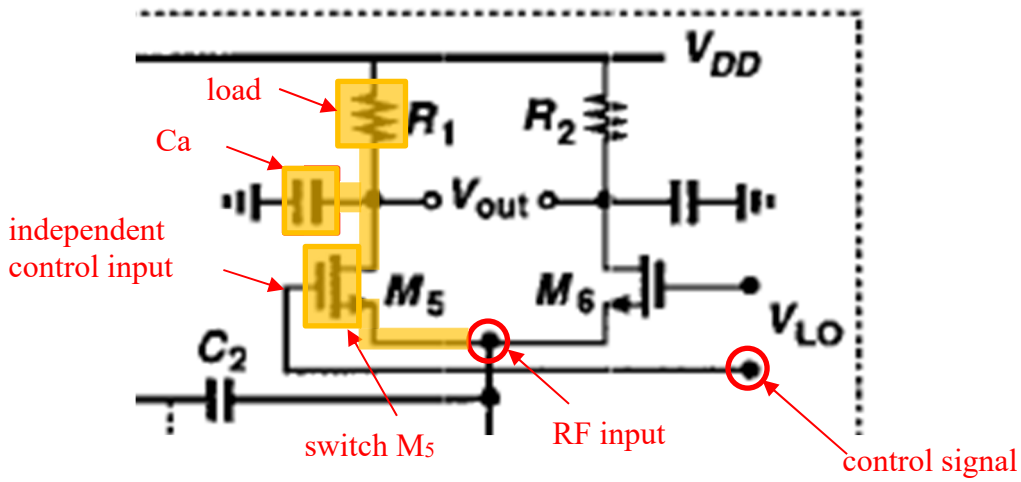
Razavi, FIG. 1 (annotated)

163. Turning back to FIG. 2, transistor switch M_5 is off when the bottom V_{LO} signal has a is substantially lower voltage than the top V_{LO} signal, and is fully on when the bottom V_{LO} signal has a substantially higher voltage than the top V_{LO} signal. *See, e.g.*, Razavi, FIG. 2. Similarly, transistor switch M_6 is off when the bottom V_{LO} signal has a is substantially higher voltage than the top V_{LO} signal, and is fully on when the bottom V_{LO} signal has a is substantially lower voltage than the top V_{LO} signal. *See, e.g.*, Razavi, FIG. 2. As each switch turns off and on once per 900 MHz cycle, the circuit is time-varying.

(b) that samples a modulated RF carrier signal at an aliasing rate using a switch with an independent control input driven by a control signal with a non-negligible, periodic aperture such that the samples, having non-negligible available energy, are accumulated and transferred to a load while the switch is closed

164. Razavi describes a direct conversion receiver, which a POSITA would have understood to be used for down-converting a modulated RF carrier signal. Razavi, 1:1-3. The circuitry samples the RF signal at an aliasing rate because the spectrum of the RF signal is centered at 900 MHz and the differential V_{LO} signal in FIG. 2 causes each switching transistor to open and close at a rate of 900 MHz. Razavi, 2:11-14 (describing 1.8 GHz oscillator driving divider); *see also* TI-1001, 29:59-61 (defining the aliasing rate as "equal to, or less than, twice the frequency of the EM carrier signal"). Here, 900 MHz is an aliasing rate because it is less than twice the EM carrier signal.

165. The circuitry includes a switch (transistor M_5) that has an independent control input for the local oscillator control signal, as shown in FIG. 2 below:



Razavi, FIG. 2 (partial, annotated)

166. According to Razavi, the "mixer employs a single-balanced topology consisting of an input transistor M4 and a switching pair M_5-M_6." *See, e.g.*, Razavi, 1:33-35. While the switch M_5 is closed, non-negligible energy from the RF input is accumulated on the capacitor labeled Ca in the above FIG. 2. *See, e.g.*, Razavi, 1:49-51 (describing maximizing voltage drop across resistors R1 and R2). The energy accumulated on the capacitor Ca and transferred to the load while the switch M_5 is closed is non-negligible because the receiver requires a non-negligible signal to function properly, i.e., to down-convert the RF input signal and subsequently decode the information contained in the received RF input signal. If the samples were to contain negligible energy, the receiver would not function to perform the down-conversion. Put differently, the energy of the sample is non-negligible because there must be a non-negligible amount of energy for the

receiver to perform its desired function of receiving, down-converting, and decoding the information contained in the received RF signal.

167. Indeed, the energy from the sampling window is accumulated and transferred to the load resistor during the aperture period. In the sense that all of the energy during the aperture period is accumulated on capacitor Ca and transferred to load R1, the sample has non-negligible energy.

168. In addition to accumulating charge on capacitor Ca, Razavi's circuit also transfers charge to the load (resistor R1) when the switch is closed. The load (resistor R1) is shown in FIG. 2 above.

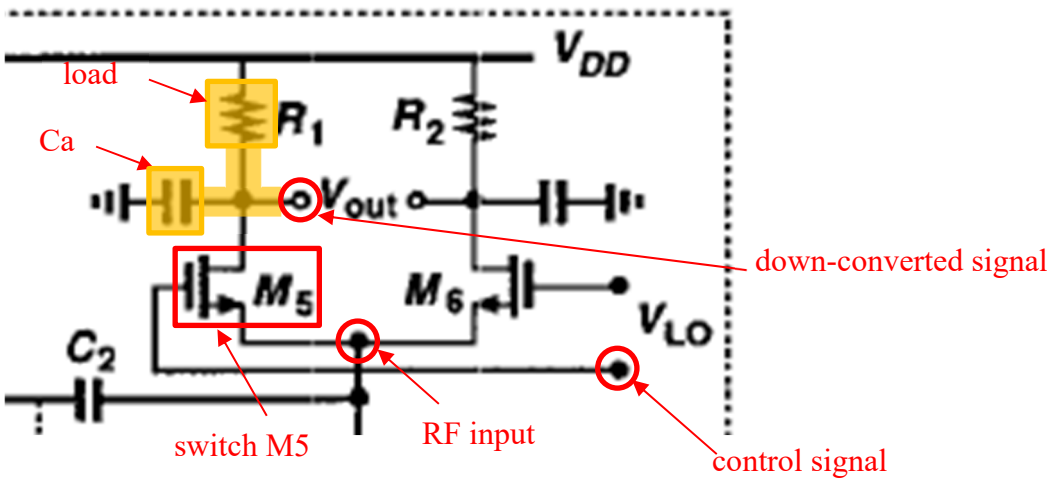
(c) and discharged through the load while the switch is open.

(d) thereby transferring available real power from the modulated RF carrier signal to the load and

(e) producing a down-converted signal with enhanced signal-to-noise power ratio

169. Elements (c)-(e) taken together:

170. The charge stored on the capacitor Ca discharges through the load R1 when the switch is open, as shown in FIG. 2 below:



Razavi, FIG. 2 (partial, annotated)

171. When no RF signal is applied to the system, each capacitor charges to the same voltage, called the quiescent voltage, and therefore each capacitor holds the same amount of charge, called the quiescent charge. When an RF signal is applied to the system, it results in a variation of the voltage of each capacitor about its quiescent voltage, called the signal voltage, and a corresponding variation of charge held by each capacitor about its quiescent charge, called the signal charge. Signal energy is accumulated on capacitor Ca as a result of its signal charge changing when the RF signal is sampled by the bottom control signal of V_{LO} for a given aperture period. When the switch M_5 is open, the signal charge on Ca discharges through the load R1, transferring charge through the load R1.

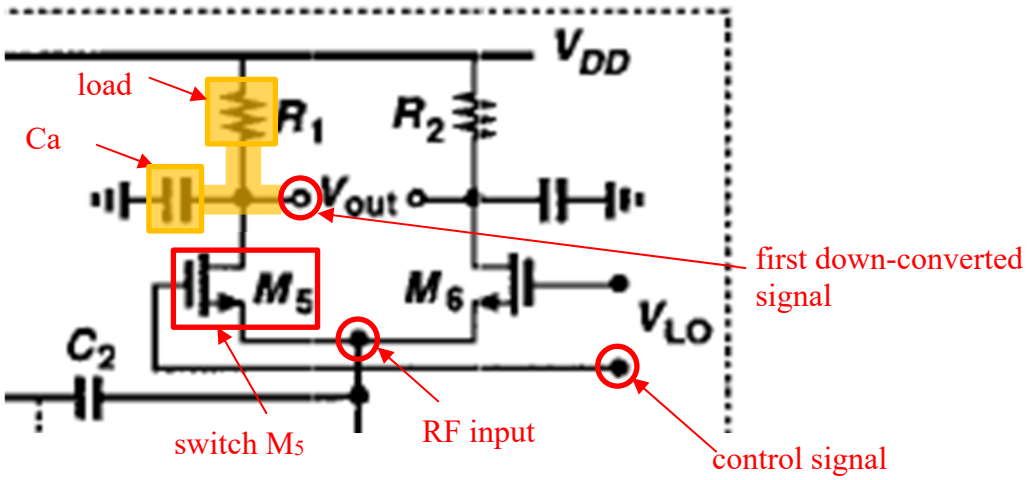
172. The resulting voltage signal across the resistor R1 is a first down-converted signal, that is "further processed by" the baseband amplifier. *See, e.g.*,

Razavi, 2:21-34. The resulting voltage is a down-converted signal because it periodically transfers energy from the RF signal to the capacitor for approximately half of each period of the 900 MHz V_{LO} control signal.

173. The combination of R_1 and Ca forms a lowpass filter: "The output nodes of the mixer are loaded with on-chip capacitors [one of which is Ca] to suppress high-frequency components" Razavi, 2:8-9. The "high frequency components" correspond to unwanted interference, so suppressing them enhances the signal to noise ratio.

14.2 down converting said input signal at said first matched filtering/correlating module according to a first control signal and outputting a first down-converted signal;

174. *See, supra*, Ground 2A, 14.1 (discussing the resulting voltage across resistor R1 being a down-converted signal). The first matched filtering/correlating module down-converts the RF signal according to the control signal V_{LO}, as shown in FIG. 2:



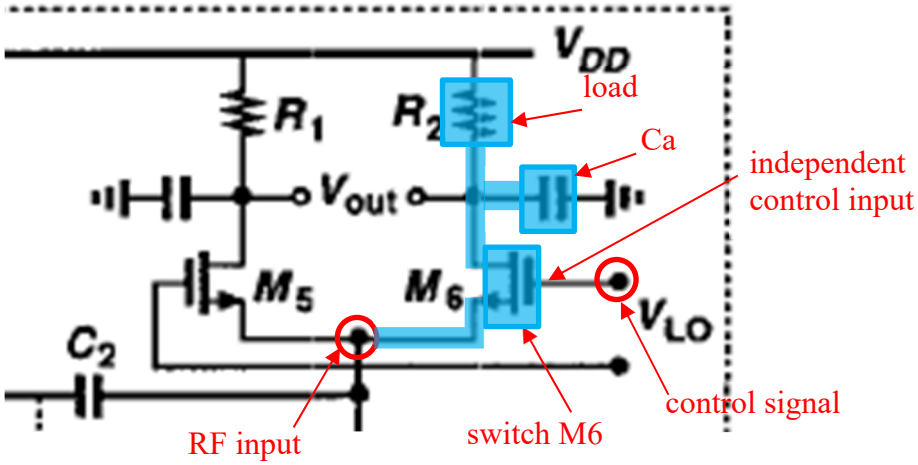
175. The switching operation of transistor M_5 produces a "downconverted signal" across resistor R_1, that is "further processed by" the baseband amplifier. *See, e.g.*, Razavi, 2:21-34. The circled left output of Vout in FIG. 2 above represents the output of a first down-converted signal. *See, e.g.*, Razavi, FIG. 2.

14.3 receiving said input signal at a second matched filtering/correlating module;

176. *See*, *supra*, Ground 2A, 14.1 (discussing Razavi's first matched filtering/correlation module, the analysis and discussion of which are relevant here for the similar second matched filtering/correlating module). As already discussed, the matched filtering/correlating module well-approximates a linear and time-variant. In addition, the Razavi down-conversion circuitry samples the RF signal at an aliasing rate because the spectrum of the RF signal is centered at 900 MHz and the differential VLO signal in FIG. 2 causes each switching transistor to open and close at a rate of 900 MHz (a rate which is obviously less than twice the

highest frequency of the 900 MHz RF input signal, so it is an aliasing rate). *See, e.g.*, Razavi, 2:11-14 (describing 1.8 GHz oscillator driving divider).

177. The circuitry includes a switch (transistor M_6) that has an independent control input for the local oscillator control signal, as shown in FIG. 2 below:

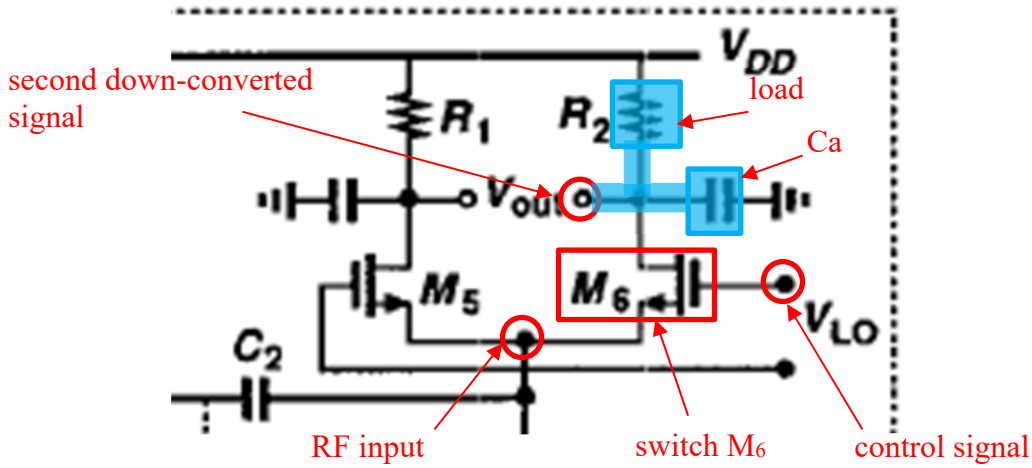


Razavi, FIG. 2 (partial, annotated)

178. According to Razavi, the "mixer employs a single-balanced topology consisting of an input transistor M4 and a switching pair M_5-M_6." *See, e.g.*, Razavi, 1:33-35. While the switch M_6 is closed, non-negligible energy from the RF input is accumulated on the capacitor labeled Ca in the above figure. *See, e.g.*, Razavi, 1:49-51 (describing maximizing voltage drop across resistors R1 and R2). In addition to accumulating charge on capacitor Ca, Razavi's circuit also transfers charge to the load (resistor R2) when the switch is closed. *See, e.g.*, Razavi, FIG. 2. The load (resistor R2) is shown in FIG. 2 above.

179. The energy accumulated on the capacitor Ca and transferred to the load while the switch M_6 is closed is non-negligible because the receiver requires a non-negligible signal to perform receiver functions, such as down-conversion of the RF input signal and decoding of the information contained in the received RF input signal. If the samples contained negligible energy, the receiver could not function to perform the down-conversion. Put differently, the energy of the sample is non-negligible because there must be a non-negligible amount of energy for the receiver to perform its desired function of receiving, down-converting, and decoding the information contained in the received RF signal.

180. The charge stored on the capacitor Ca discharges through the load R2 when the switch is open, as shown in FIG. 2 below:



Razavi, FIG. 2 (partial, annotated)

181. When no RF signal is applied to the system, each capacitor charges to the same voltage, called the quiescent voltage, and therefore each capacitor holds the same amount of charge, called the quiescent charge. *See, e.g.*, Razavi, FIG. 2. When an RF signal is applied to the system, it results in a variation of the voltage of each capacitor about its quiescent voltage, called the signal voltage, and a corresponding variation of charge held by each capacitor about its quiescent charge, called the signal charge. *See, e.g.*, Razavi, FIG. 2. Signal energy is accumulated on capacitor Ca as a result of its signal charge changing when the RF signal is sampled by the bottom control signal of V_{LO} for a given aperture period.

182. Indeed, the energy from the sampling window is accumulated and transferred during the aperture period. In the sense that all of the energy during the aperture period is accumulated on capacitor Ca and transferred to load R1, the sample has non-negligible energy.

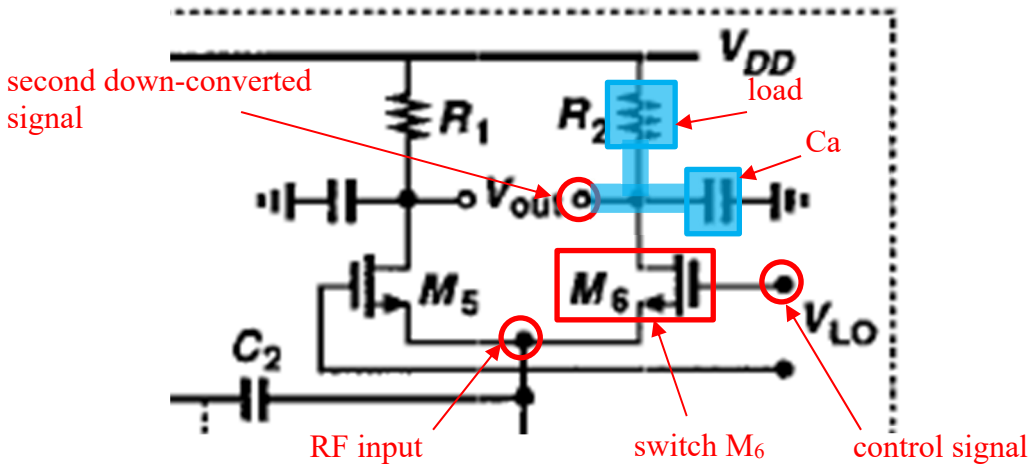
183. When the switch M_6 is open, the signal charge on Ca discharges through the load R2, transferring charge through the load R2. *See, e.g.*, Razavi, FIG. 2. The resulting voltage signal across the resistor R2 is a second down-converted signal, that is "further processed by" the baseband amplifier. *See, e.g.*, Razavi, 2:21-34.

184. The combination of R_2 and Ca form a lowpass filter: "The output nodes of the mixer are loaded with on-chip capacitors [one of which is Ca] to

suppress high-frequency components" Razavi, 2:8-9. The "high frequency components" correspond to unwanted interference, so suppressing them enhances the signal to noise ratio.

14.4 down-converting said input signal at said second matched filtering/correlating module according to a second control signal and outputting a second down-converted signal; and

185. *See, supra*, Ground 2A, 14.1-2 (discussing Razavi's receiver operation and how it performs down-conversion, which are applicable here). The second matched filtering/correlating module down-converts the RF signal according to the control signal V_{LO}, as shown in FIG. 2:



Razavi, FIG. 2 (partial, annotated)

The switching operation of transistor M_6 produces a down-converted signal across resistor R_2, that is "further processed by" the baseband amplifier. *See, e.g.*, Razavi,

2:21-34. The circled V_{out} in FIG. 2 above represents the output of a second down-converted signal.

14.5 combining said second down-converted signal and said first down-converted signal to output a first channel down-converted signal.

186. The down-converted signal output of the first matched filtering/correlating module (the left V_{out} terminal in Figure 2) and the inverted down-converted signal output of the second matched filtering/correlating module (the right V_{out} terminal in FIG. 2) are connected to the respective input terminals (labeled V_{in}) of the baseband amplifier shown in FIG. 5. *See, e.g.*, Razavi, 2:35-48, FIGS. 2, 5. As would be well understood by a POSITA, the baseband amplifier differentially amplifies its two V_{in} inputs while largely suppressing the common-mode component (i.e., the average) of its two V_{in} inputs, meaning that each of the baseband amplifier's V_{out} output signals contains an amplified version of the difference between the baseband amplifier's two V_{in} inputs, i.e., the difference between said down-converted signal and said inverted down-converted signal. *See, e.g.*, Razavi, 2:35-48, FIGS. 2, 5. The two V_{out} signals differ in that their above-mentioned amplified differences between the two V_{in} signals have different signs. *See, e.g.*, Razavi, 2:35-48, FIGS. 2, 5. Consequently, the difference between the two V_{out} signals is an amplified version of the difference between the two V_{in} signals. *See, e.g.*, Razavi, 2:35-48, FIGS. 2, 5.

187. A POSITA would have recognized that it follows that each of the two V_{out} signals is a combined version of said first and second down-converted signals, and, furthermore, the two V_{out} signals taken together represent a differential version of the combination of said first and second down-converted signals.

C. GROUND 2B – Razavi and Uzunoglu Render Claim 14 Obvious Under the Plain Meaning

1. The Razavi and Uzunoglu Combination

188. Razavi describes a 900 Mhz direct conversion receiver that uses first and second down-conversion circuitry to down-convert an RF signal to baseband. While Razavi's control signal (from its local oscillator) is nominally set to 900 MHz, which is the same as the carrier frequency of the RF input signal, Razavi, does not describe synchronizing the control signal with the frequency of the input signal. In the combination, the control signal of Razavi that controls the operation of the switches in the down-conversion circuitry is synchronized to the frequency of the carrier signal of the input signal in a manner similar to that described by Uzunolgu.

2. Motivation to Combine Razavi and Uzunoglu

189. A POSITA would have been motivated to combine Razavi with Uzunoglu to synchronize the control signal from the local oscillator signal of Razavi with the carrier frequency of the RF input signal. A POSITA would have recognized that any transmitter that generates the type of 900 MHz RF input signal

that the Razavi circuit is designed to receive typically has its own local oscillator. If the local oscillator were to have exactly the right frequency, then the transmitted RF input signal spectrum would be centered exactly at 900 MHz. In this case, if the V_{LO} control signals derived from the oscillator signal in the Razavi circuit were to have a frequency of exactly 900 MHz, then the RF input signal would be down-converted to exactly zero-frequency.

190. It is difficult for independent oscillators to have exactly the frequencies they are designed to have (a result of inevitable non-ideal circuit behavior). Therefore, the center frequency of the received RF input signal will deviate slightly from the frequency of the V_{LO} control signals. In this case, further processing typically is necessary to compensate for this unwanted deviation. In many cases the further processing is done via digital signal processing after analog-to-digital conversion. However, it can instead be done by synchronizing the V_{LO} control signals to the carrier frequency (i.e., the center frequency) of the received RF input signal via a carrier synchronization circuit (such as the Uzunoglu circuit). For example, if non-ideal circuit behavior in the transmitter were to cause the actual carrier frequency of the received RF input signal to be 901 MHz, instead of 900 MHz, then the carrier synchronization circuit would cause the frequency of the V_{LO} control signals to be 901 MHz too. This would not only eliminate the need for the additional processing mentioned above, but if the carrier

synchronization circuit were designed to cause the phase of one of V_{LO} control signals to precisely match that of the carrier of the received RF input signal (the Uzunoglu circuit is one of many such circuits deigned to have this functionality), then only one of the mixers (e.g., just the circuit labeled I-Mixer in FIG. 2 of Razavi) would be necessary. A POSITA would recognize this as a well-known technique, and would know that receivers which use the technique are said perform synchronous demodulation. *See, e.g.*, TI-1019, 183, 455.

191. In addition, a POSITA would have recognized that synchronization offers the potential advantage of reducing circuit complexity. For example, a POSITA would have recognized that using an SO like that of Uzunoglu in Razavi would have reduced the circuit complexity by allowing the elimination of one of the mixer circuits (e.g., the quadrature mixer), as well as the circuitry following that mixer circuit (e.g., lowpass filter, amplifier, analog-to-digital converter, and subsequent digital signal processing). Additionally, using SO eliminates (or at least, reduces) the need for post processing of the two baseband signals to correct for the difference between the RF input signal's carrier frequency and the frequency of V_{LO}.

192. A POSITA would have had a reasonable expectation of success implementing SO circuitry, like that of Uzunoglu. First, Uzunoglu provides details for how its SO should be implemented and discusses implementation and

configuration details. *See, e.g.*, Uzunoglu, 4-12 (discussing experimental results). In addition, Uzunoglu also provides other circuit designs that a POSITA could try to use as an alternative, while also teaching the advantages of its own design. Uzunoglu, 1, 12 (listing prior art references).

193. A POSITA at the time of the priority date of the '177 patent would have recognized that a synchronous oscillator such as that presented in Uzunoglu is just one of many circuits which perform carrier synchronization, yet would understand that, as explained in Uzunoglu, the synchronous oscillator represents an attractive option in that it has several desirable properties. Uzunoglu, 1-2 (describing various SO designs). These desirable properties include but are not limited to a "very narrow resolution bandwidth [that] permits the extraction of information from signals with extremely low carrier-to-noise ratios, such as –40 dB while tracking at several hundred kilohertz to permit rapid phase acquisition," the ability to "track the input signal even to power levels as low as –100 dBm," and reduction of "steady-state phase error in synchronization to a low value." Uzunoglu, Abstract. A POSITA also would have recognized that other known circuits which perform carrier synchronization offer different performance tradeoffs and benefits, so while the Uzunoglu circuit is an attractive option, other options might be even more attractive for certain applications. Therefore, the

Uzunoglu circuit is considered herein as a representative example of a carrier synchronization circuit.

3. Analysis

14.P A method for down-converting an electromagnetic signal, comprising:

194. *See, supra*, Ground 2A, 14.P.

14.1 receiving an input signal at a first matched filtering/correlating module;

195. The combination provides 14.1 under the plain meaning of "matched filtering/correlating module." As discussed in Ground 2A, 14.1, *supra*, Razavi describes all of the circuit components of a first matched filtering/correlating module, as claimed by the '177 patent. In the combination, Razavi's control signal is synchronized, i.e., matched or correlated, to the carrier frequency of the RF input signal, as described by Uzunoglu. The output of the Uzunoglu circuit directly generates one of the V_{LO} control signals in Razavi. It does this through the principle of injection locking. The synchronous oscillator is coupled to the RF input signal in such a way that it is injection locked, also known as pulled, to the frequency and phase of the RF input signal's carrier. It's narrow locking bandwidth ensures that it is relatively unaffected by the modulation of the RF signal and instead locks to the carrier.

196. The Razavi down-conversion circuitry described in Ground 2A operates the same way in the combination. With the application of Uzunoglu's circuitry to synchronize the control signal with the carrier frequency of the RF

input signal, the Razavi mixer operates to down-convert the RF signal using the switch M_5, capacitor Ca and load R1. The only difference is the matching or correlating of the control signal to the carrier frequency of the RF input signal.

14.2 down converting said input signal at said first matched filtering/correlating module according to a first control signal and outputting a first down-converted signal;

197. *See, supra*, Ground 2A, 14.2.

14.3 receiving said input signal at a second matched filtering/correlating module;

198. The combination provides 14.3 under the plain meaning of "matched filtering/correlating module." As discussed in Ground 2A, 14.1-3, *supra*, Razavi describes all of the circuit components of a first and second matched filtering/correlating modules, as claimed by the '177 patent. In the combination, Razavi's control signal is synchronized to the carrier frequency of the RF input signal, as described by Uzunoglu. The output of the Uzunoglu circuit directly generates one of the V_{LO} control signals in Razavi. The SO does this through the principle of injection locking. Uzunoglu, 1. The synchronous oscillator is coupled to the RF input signal in such a way that it is injection locked, also known as pulled, to the frequency and phase of the RF input signal's carrier. *Id*. The SO circuitry has a narrow locking bandwidth that ensures that it is relatively unaffected by the modulation of the RF signal, and instead the circuitry locks to the carrier. *Id*. The output, therefore, is a signal that is synchronized with the carrier

frequency. The synchronization between the control signal and the carrier frequency means that the operation of the circuitry in the Razavi-Uzunoglu combination is the same operation of a matched filtering/correlating module.

199. The Razavi down-conversion circuitry described in Ground 2A operates the same way in the combination. With the application of Uzunoglu's circuitry to synchronize the control signal with the carrier frequency of the RF input signal, the Razavi mixer operates to down-convert the RF signal using the switch M_6, capacitor Ca and load R2. The only difference is the synchronization of the control signal to the carrier frequency of the RF input signal.

14.4 down-converting said input signal at said second matched filtering/correlating module according to a second control signal and outputting a second down-converted signal; and

200. *See, supra*, Ground 2A, 14.4.

14.5 combining said second down-converted signal and said first down-converted signal to output a first channel down-converted signal.

201. *See, supra*, Ground 2A, 14.5.

XI. ADDITIONAL REMARKS

202. I currently hold the opinions set expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

203. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code.

Dated: May 17, 2024 By: /Dr. Ian Galton/
Dr. Ian Galton

APPENDIX A

Ian Galton

Education

Brown University, Providence, RI	**ScB** in Electrical Engineering	1984
California Institute of Technology, Pasadena, CA	**MS/PhD** in Electrical Engineering	1989/1992

Employment

Professor of Electrical Engineering, **University of California at San Diego**, La Jolla, CA	7/02 – present
Associate Professor of Electrical Engineering, **University of California at San Diego**, La Jolla,	11/96 – 6/02
Assistant Professor of Electrical Engineering, **University of California at Irvine**, Irvine, CA	7/92 – 10/96
Design Engineer, **Acuson, Inc.**, Mountain View, CA	8/86 – 9/88
Design Engineer, **Mead Data Central**, Menlo Park, CA	2/85 – 8/86
Design Engineer, **Mindset Corporation**, Sunnyvale, CA	7/84 – 1/85

UCSD Research Overview

Ian Galton manages the Integrated Signal Processing Group at the University of California, San Diego (UCSD). The group develops enabling technology for highly-integrated, high-performance, low-cost, communication systems. The research involves the invention, development, analysis, and proof-of-principle integrated circuit (IC) implementation of key communication system blocks such as data converters and frequency synthesizers. The emphases of the research are on the development of new digital signal processing techniques and new digital-like analog circuits that exploit the strengths of advanced IC technology to mitigate the effects of non-ideal analog circuit behavior in mixed-signal and radio frequency ICs.

Selected Accomplishments, Activities, Honors, and Awards

- Author or co-author of ~100 scientific papers in peer-reviewed academic journals and conferences
- Inventor or co-inventor on ~22 U.S. Patents
  Holder of the "Skyworks Endowed Chair in High Performance Communications Devices and Circuits"
- Fellow of the Institute of Electrical and Electronics Engineers (IEEE)
- Recipient of the 2015-2016 and the 2016-2017 UCSD Electrical and Computer Engineering Department "Best Graduate Teacher" award
- Co-recipient of the 2015 IEEE International Solid-State Circuits Conference (ISSCC) Lewis Winner Award
- Recipient of the Brown Engineering Alumni Medal, 2012
- Co-recipient of the 2008 IEEE Transactions on Circuits and Systems Darlington Award
- Co-recipient of the 2008 IEEE ISSCC Jack Kilby Award
- Member of the IEEE Solid-State Circuits Society Distinguished Lecturer Program, 2007-2010
- Organizer of the IEEE ISSCC Short Courses, 2007-2010
- Member of the IEEE ISSCC Technical Program Committee, 2005-2011
- Recipient of the 2005-2006 UCSD Electrical and Computer Engineering Department "Best Teacher Award"
- IEEE Solid State Circuits Society Administrative Committee, 2002-2005
- IEEE Circuits and Systems Society Board of Governors, 1998-2001, 2002-2005
- Editor-in-Chief of the *IEEE Transactions on Circuits and Systems II: Analog to Digital Signal Processing*, 2001-2003
- Board of Directors of innoCOMM Wireless, San Diego, CA, through its 2001 purchase by National Semiconductor Corporation
- Technical consultant and/or Technical Advisory Board member for several semiconductor and communications companies
- Instructor in over 80 industry-oriented short courses on the design of data converters, PLLs, and wireless transceivers at IEEE conferences and through Mead Education
- Recipient of the California Institute of Technology Charles Wilts PhD Thesis Prize, 1992

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