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(12) **United States Patent**
Sorrells et al.

(10) **Patent No.: US 9,118,528 B2**
(45) **Date of Patent: *Aug. 25, 2015**

(54) **METHOD AND SYSTEM FOR DOWN-CONVERTING AN ELECTROMAGNETIC SIGNAL, AND TRANSFORMS FOR SAME, AND APERTURE RELATIONSHIPS**

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(73) Assignee: **ParkerVision, Inc.**, Jacksonville, FL (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **14/172,392**

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(65) **Prior Publication Data**

US 2014/0241464 A1 Aug. 28, 2014

Related U.S. Application Data

(60) Continuation of application No. 13/549,213, filed on Jul. 13, 2012, now Pat. No. 8,660,513, which is a

(Continued)

(51) **Int. Cl.**
H04L 27/12 (2006.01)
H03C 1/62 (2006.01)

(Continued)

(52) **U.S. Cl.**
CPC ***H04L 27/12*** (2013.01); ***H03C 1/62*** (2013.01); ***H03D 7/00*** (2013.01); ***H04B 1/0025*** (2013.01); ***H04B 1/28*** (2013.01); ***H04B 7/12*** (2013.01); ***H04L 27/00*** (2013.01)

(58) **Field of Classification Search**
USPC 455/413, 113, 118, 130, 131, 182.1, 455/190.1, 191.1, 313, 323, 343, 350; 327/113; 375/130, 142, 143, 150, 152, 375/316, 343
See application file for complete search history.

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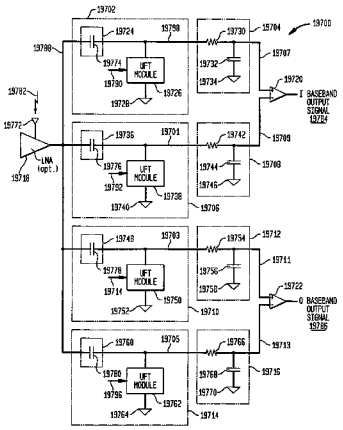
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(57) **ABSTRACT**

Methods, systems, and apparatuses, and combinations and sub-combinations thereof, for down-converting an electromagnetic (EM) signal are described herein. Briefly stated, in embodiments the invention operates by receiving an EM signal and recursively operating on approximate half cycles (½, 1½, 2½, etc) of the carrier signal. The recursive operations can be performed at a sub-harmonic rate of the carrier signal. The invention accumulates the results of the recursive operations and uses the accumulated results to form a down-converted signal. In an embodiment, the EM signal is down-converted to an intermediate frequency (IF) signal. In another embodiment, the EM signal is down-converted to a baseband information signal. In another embodiment, the EM signal is a frequency modulated (FM) signal, which is down-converted to a non-FM signal, such as a phase modulated (PM) signal or an amplitude modulated (AM) signal.

36 Claims, 284 Drawing Sheets



Related U.S. Application Data

continuation of application No. 12/976,839, filed on Dec. 22, 2010, now Pat. No. 8,340,618, which is a continuation of application No. 12/349,802, filed on Jan. 7, 2009, now Pat. No. 7,865,177, which is a division of application No. 09/550,644, filed on Apr. 14, 2000, now Pat. No. 7,515,896, which is a continuation-in-part of application No. 09/293,342, filed on Apr. 16, 1999, now Pat. No. 6,687,493, which is a continuation-in-part of application No. 09/176,022, filed on Oct. 21, 1998, now Pat. No. 6,061,551.

(51) **Int. Cl.**

H03D 7/00	(2006.01)
H04B 1/00	(2006.01)
H04B 1/28	(2006.01)
H04B 7/12	(2006.01)
H04L 27/00	(2006.01)

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FIG. 1

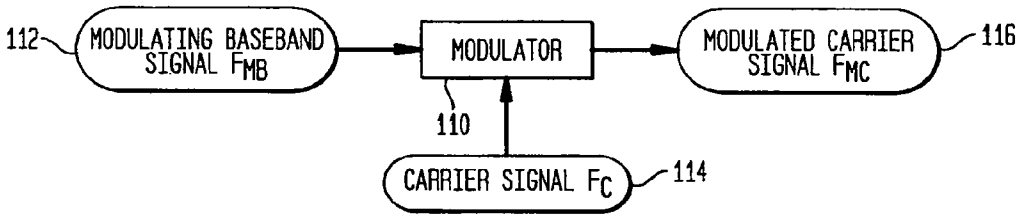


FIG. 2

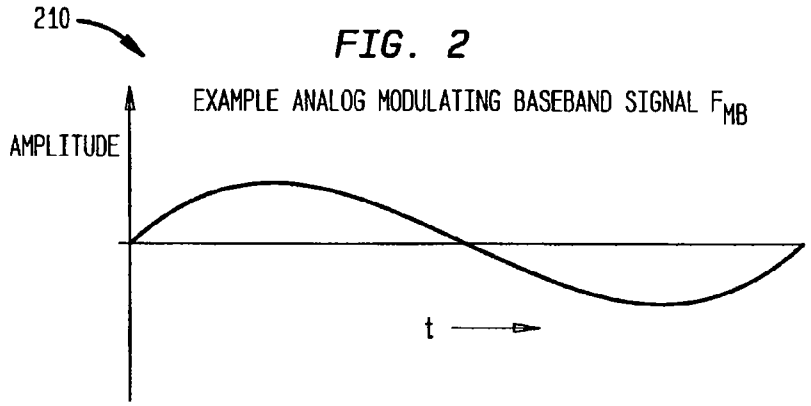


FIG. 3

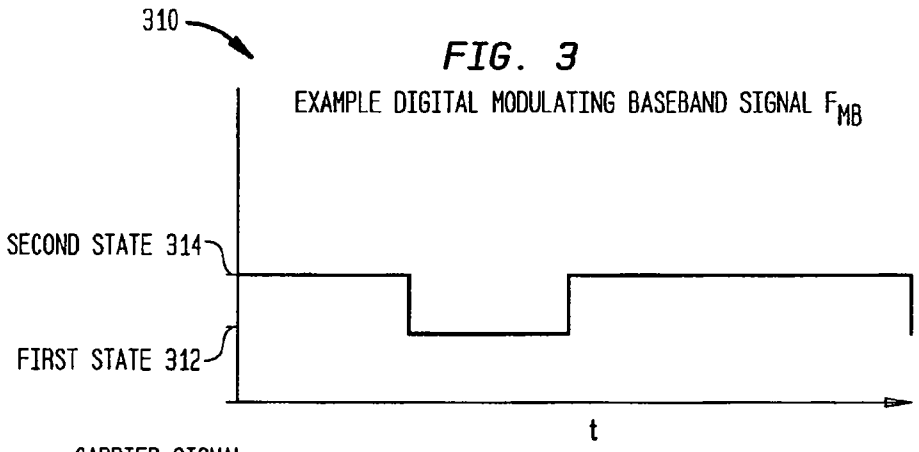
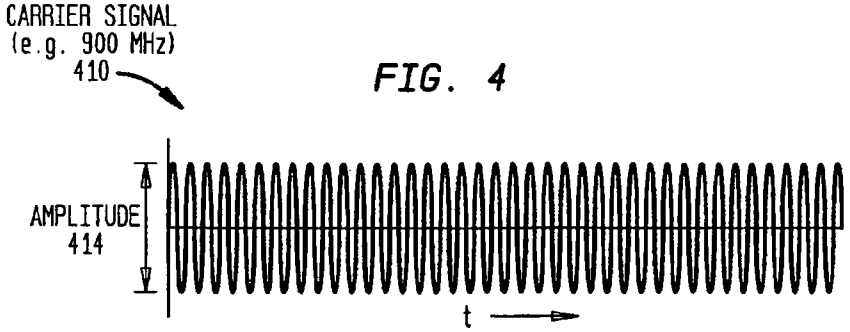


FIG. 4



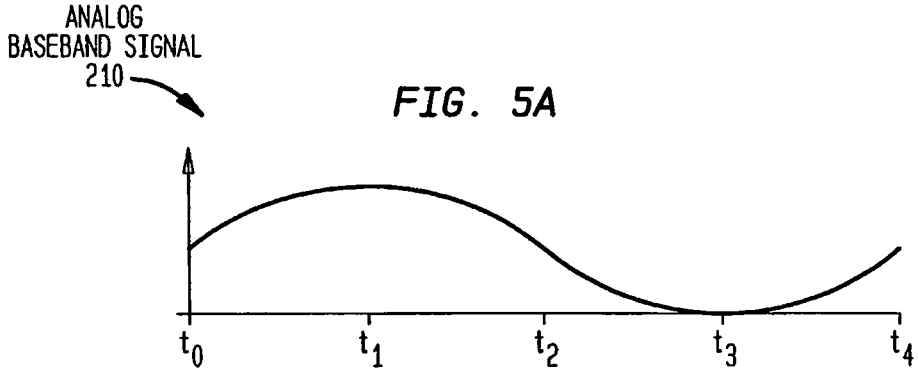


FIG. 5A

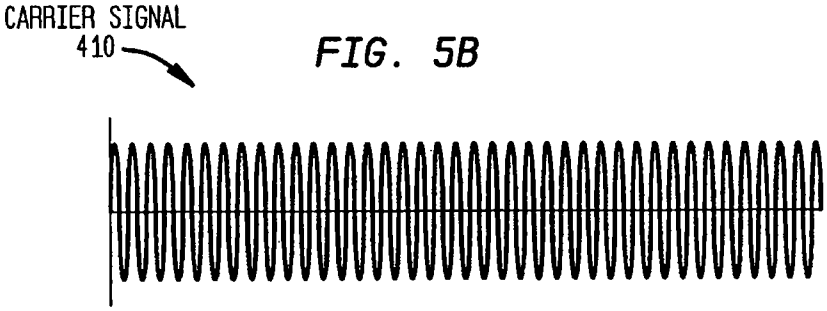


FIG. 5B

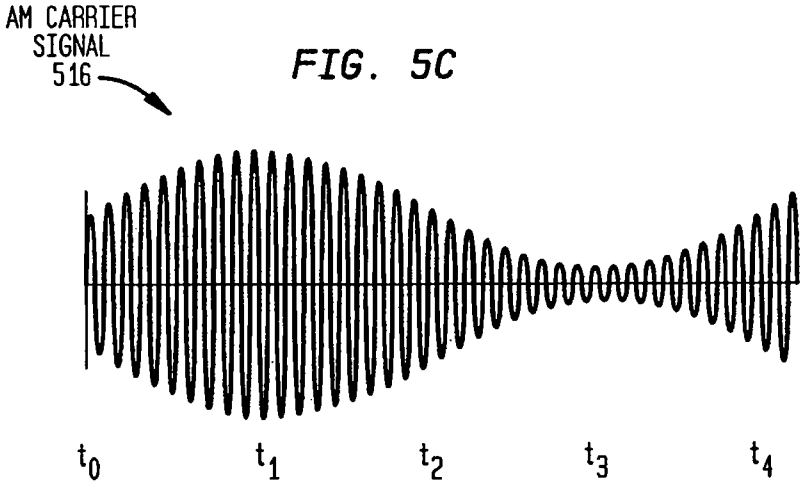


FIG. 5C

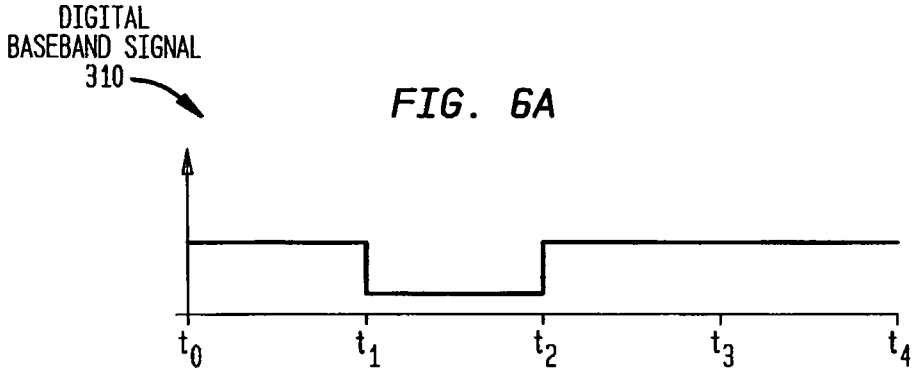


FIG. 6A

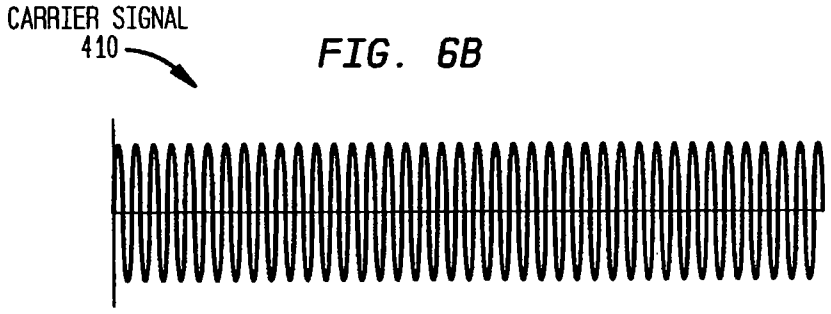


FIG. 6B

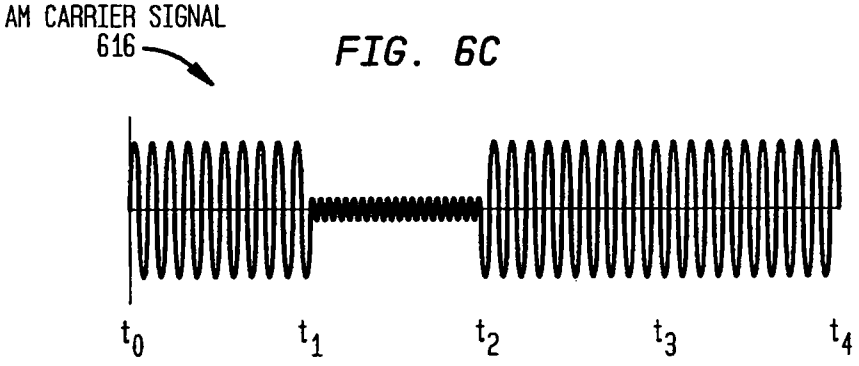


FIG. 6C

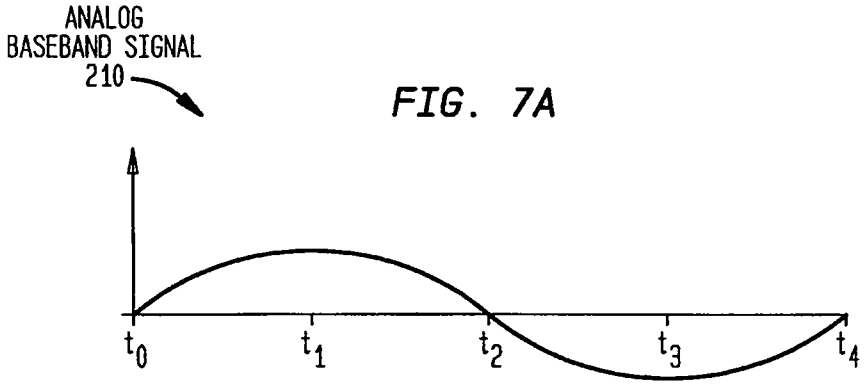


FIG. 7A

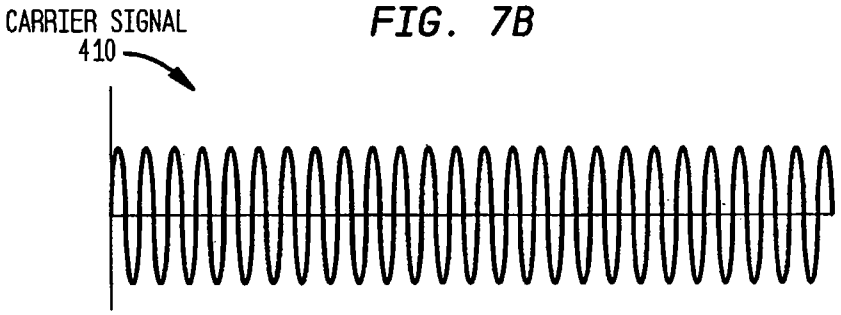


FIG. 7B

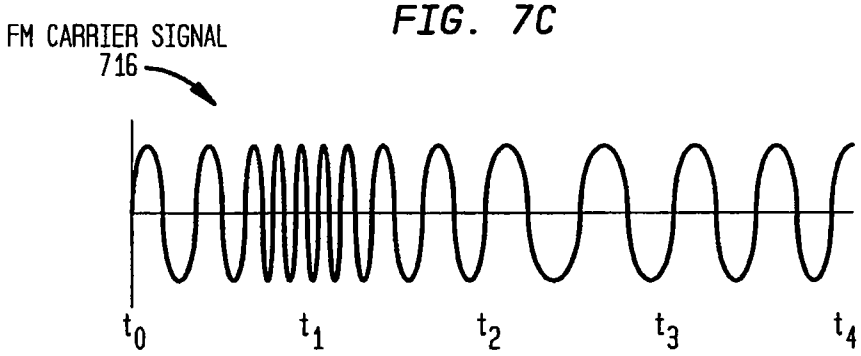


FIG. 7C

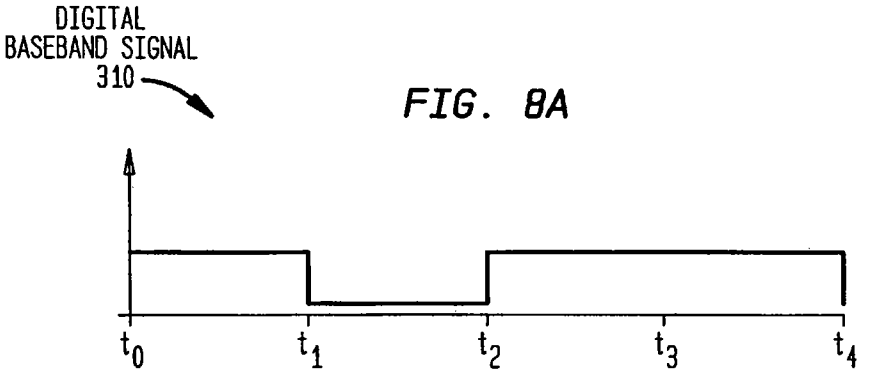


FIG. 8A

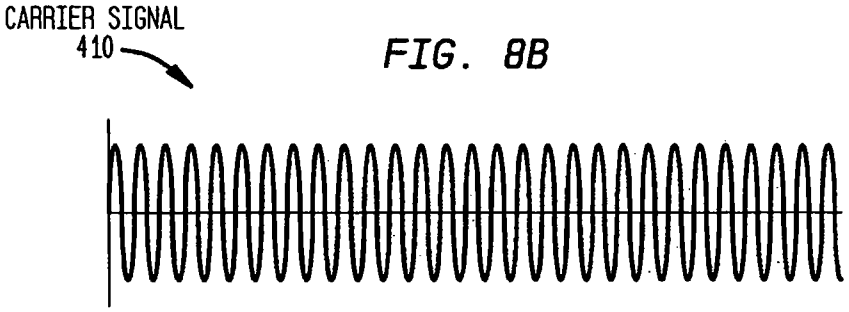


FIG. 8B

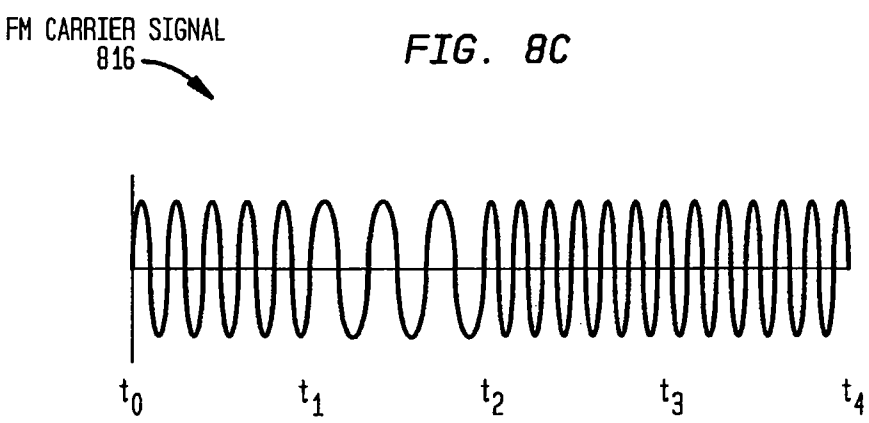


FIG. 8C

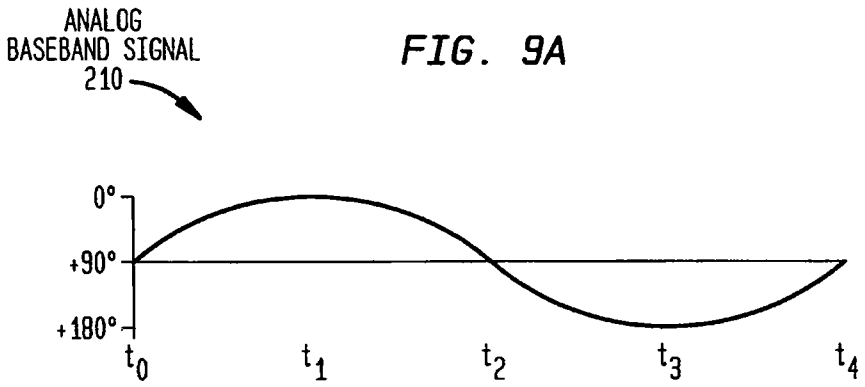
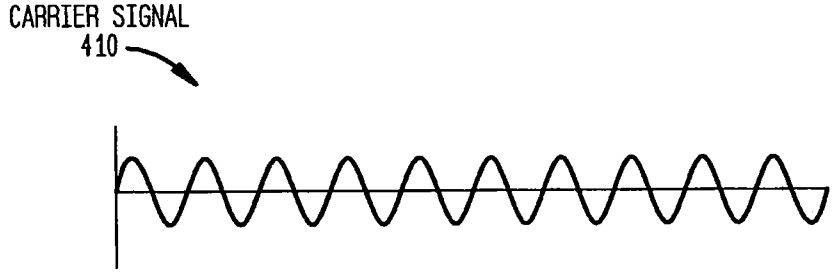


FIG. 9A

FIG. 9B



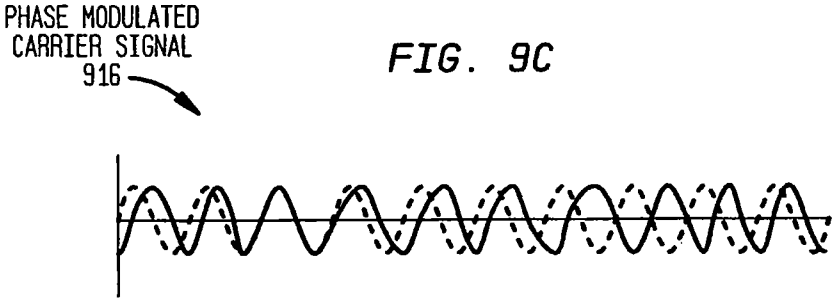


FIG. 9C

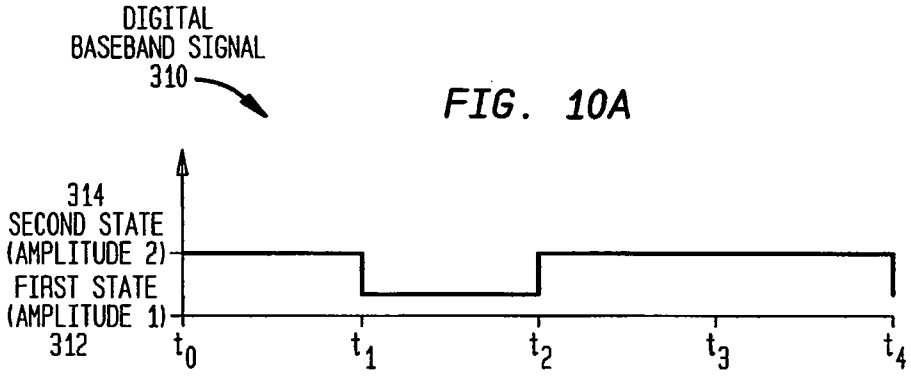


FIG. 10A

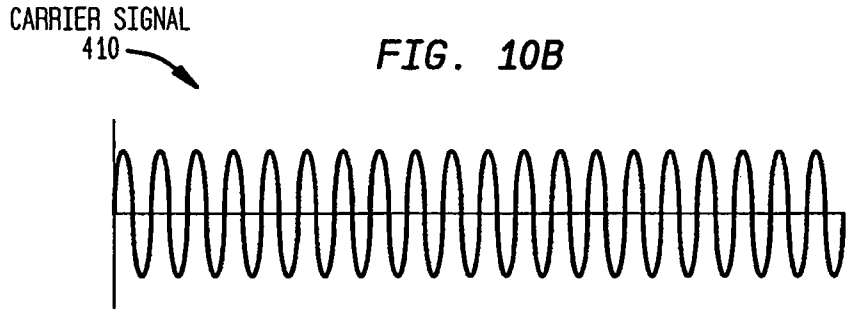


FIG. 10B

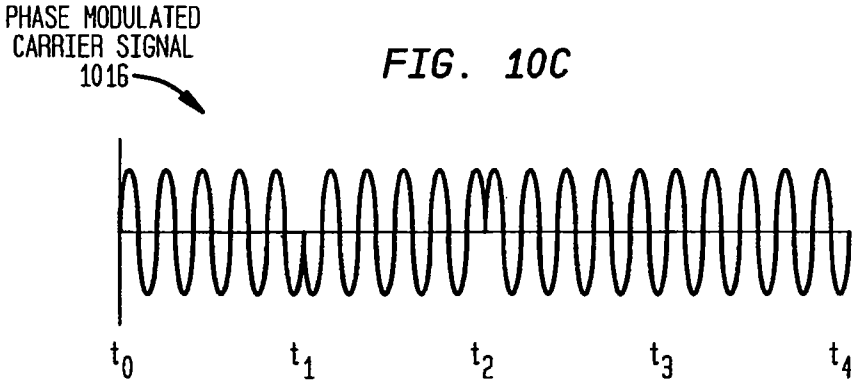


FIG. 10C

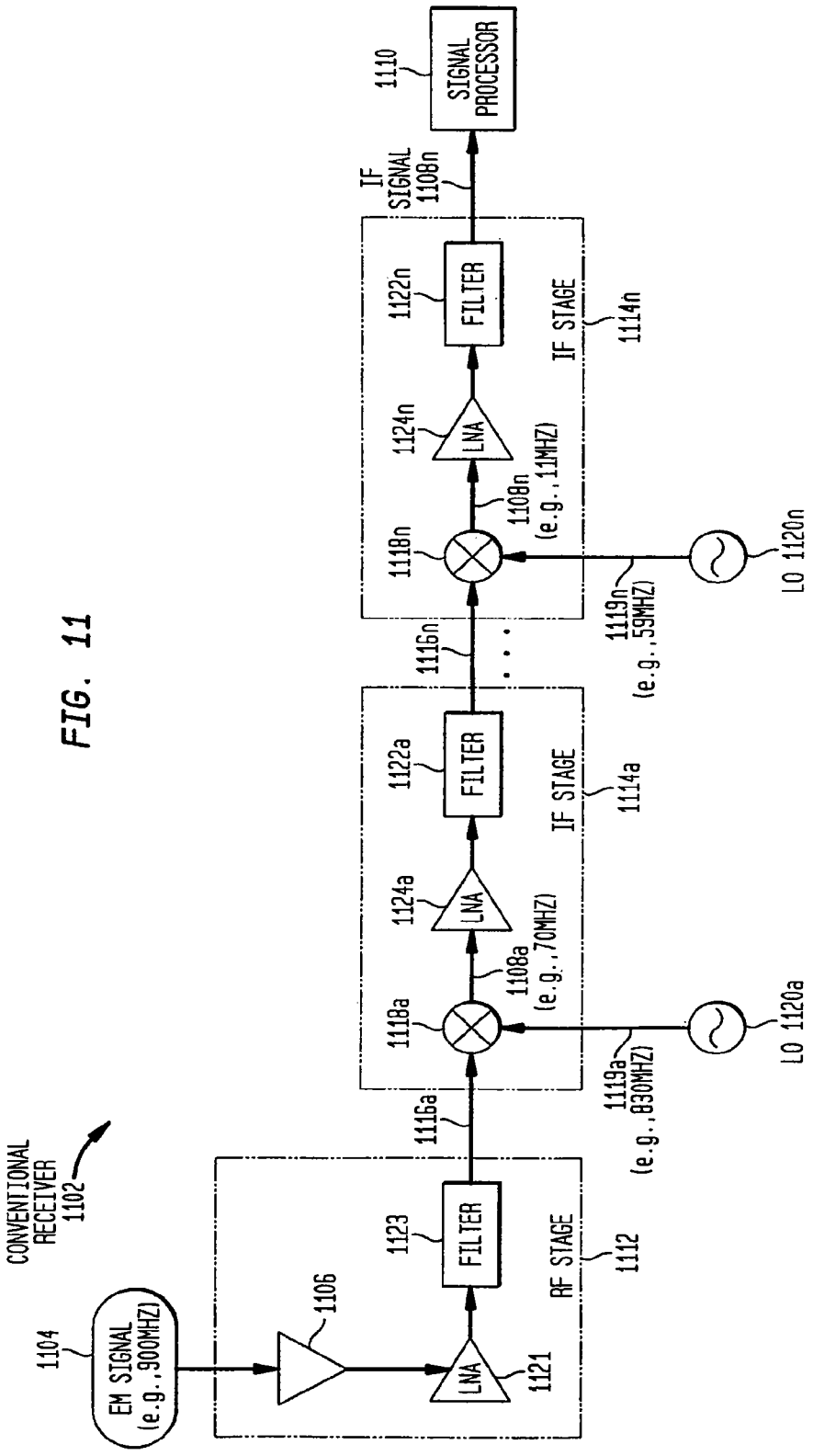
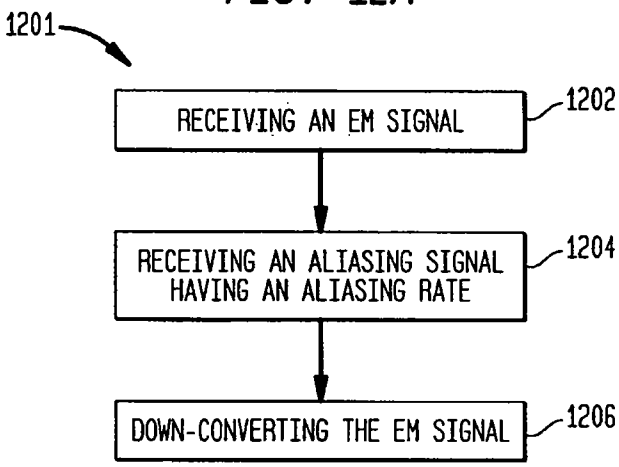

CONVENTIONAL RECEIVER 1102
1104
EM SIGNAL (e.g., 900MHZ)
1106
1121
LNA
1123
FILTER
RF STAGE
1112
1116a
1118a
1108a (e.g., 70MHZ)
1124a
LNA
1122a
FILTER
IF STAGE
1114a
1119a (e.g., 830MHZ)
LO 1120a
1116n
1118n
1108n (e.g., 11MHZ)
1124n
LNA
1122n
FILTER
IF STAGE
1114n
1119n (e.g., 59MHZ)
LO 1120n
IF SIGNAL 1108n
1110
SIGNAL PROCESSOR

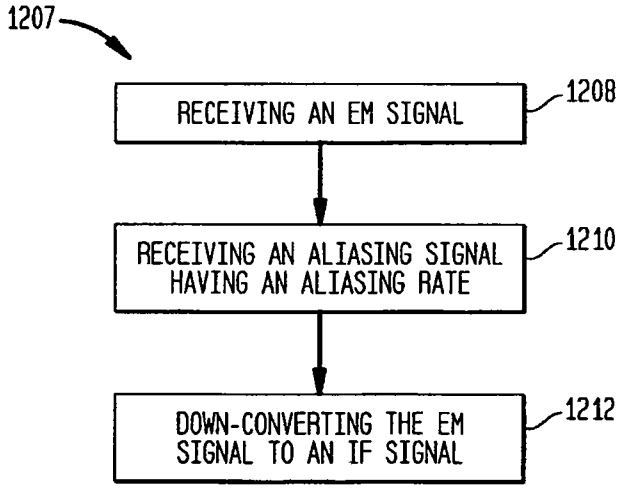
FIG. 11

FIG. 12A



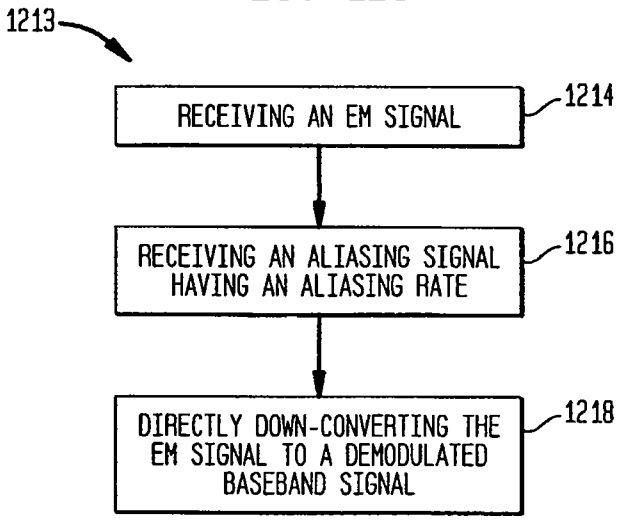
GENERIC DOWN-CONVERTING FLOWCHART

FIG. 12B



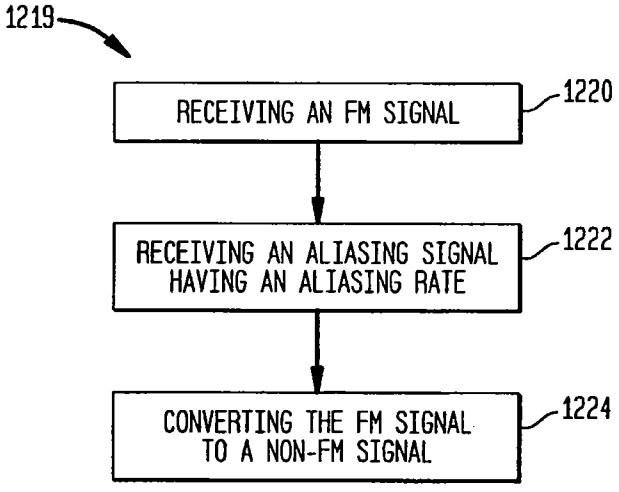
DOWN-CONVERTING AN EM SIGNAL TO AN IF SIGNAL

FIG. 12C



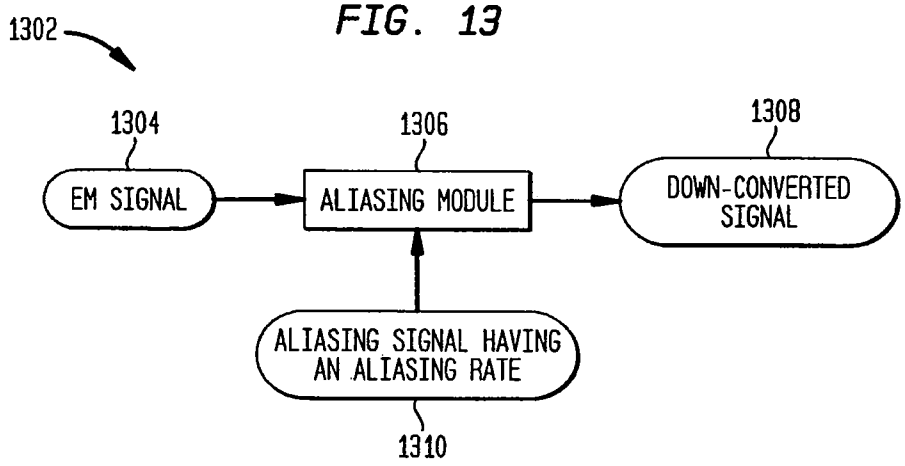
DIRECTLY DOWN-CONVERTING AN EM SIGNAL TO A DEMODULATED BASEBAND SIGNAL

FIG. 12D



MODULATION CONVERSION

FIG. 13



GENERIC DOWN-CONVERTING SYSTEM

FIG. 14A

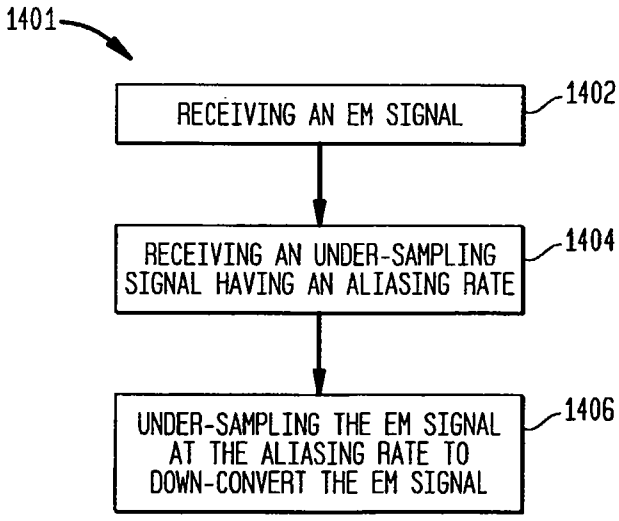


FIG. 14B

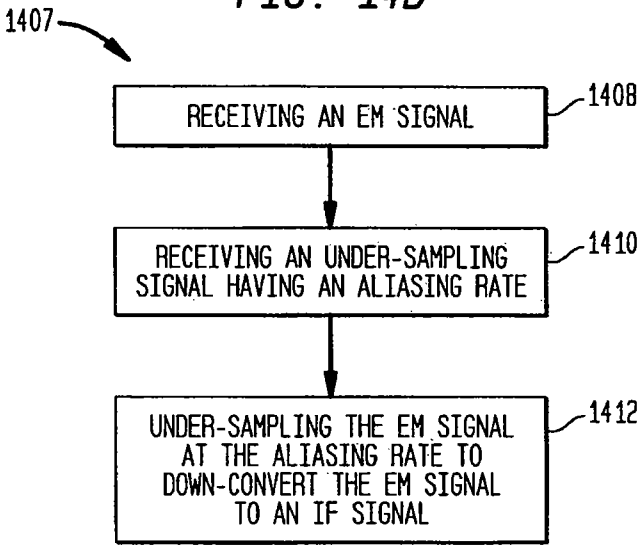


FIG. 14C

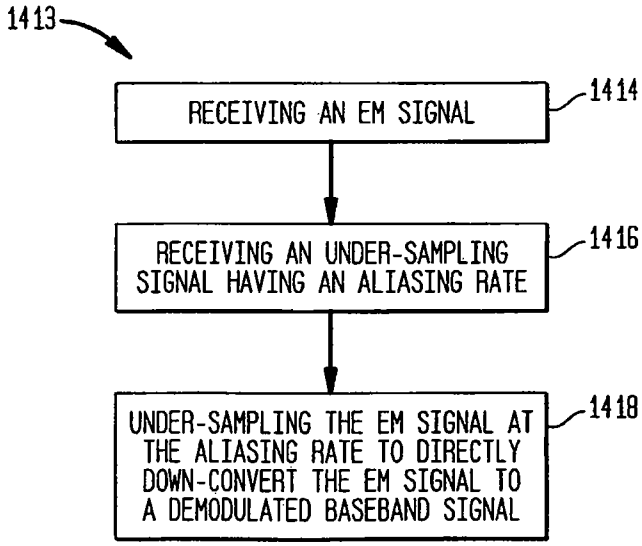


FIG. 14D

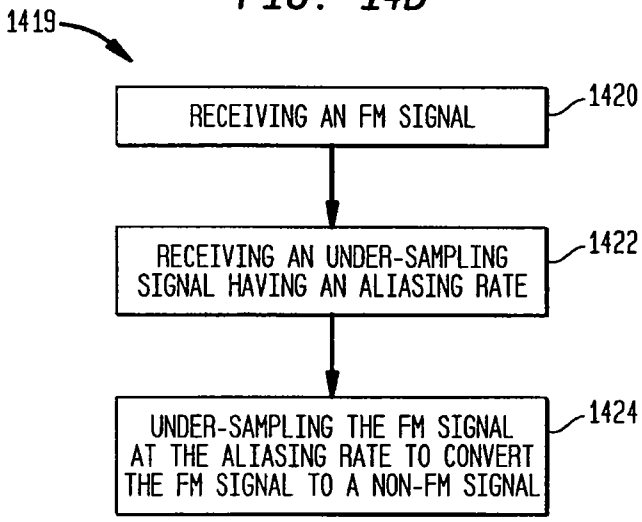

1419
RECEIVING AN FM SIGNAL
1420
RECEIVING AN UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE
1422
UNDER-SAMPLING THE FM SIGNAL AT THE ALIASING RATE TO CONVERT THE FM SIGNAL TO A NON-FM SIGNAL
1424

FIG. 15E

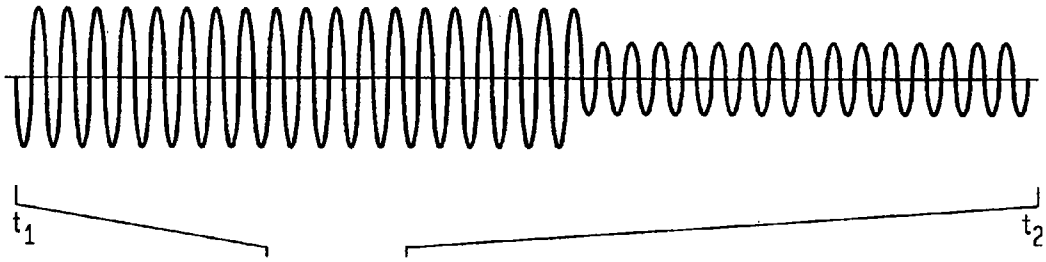


FIG. 15A

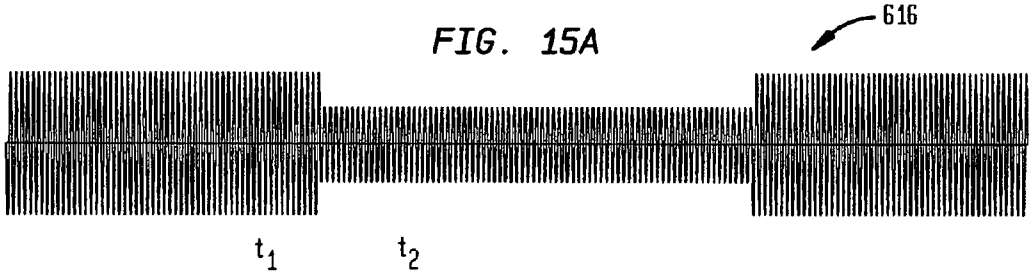


FIG. 15B

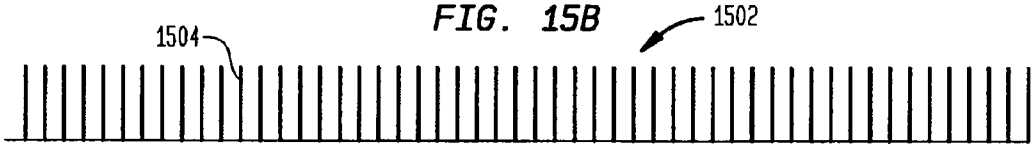


FIG. 15C

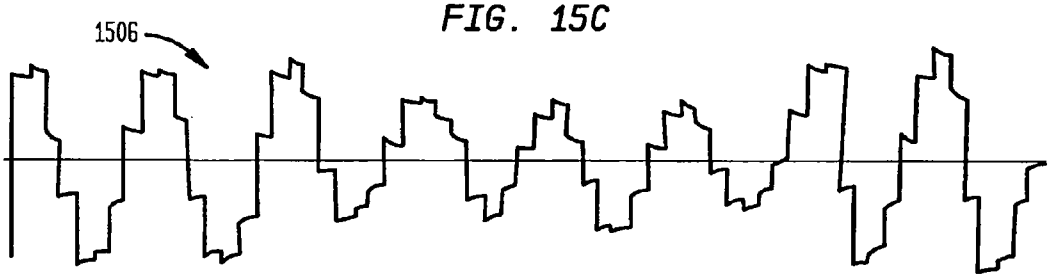


FIG. 15D

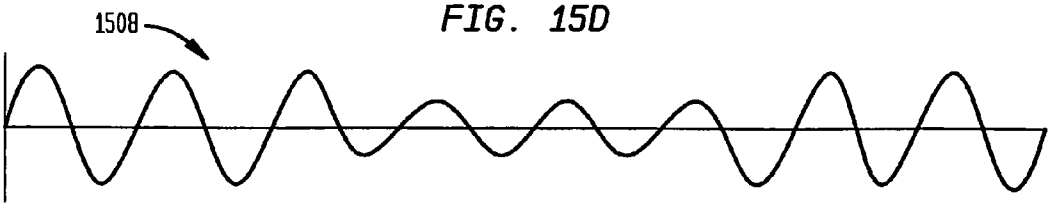


FIG. 16

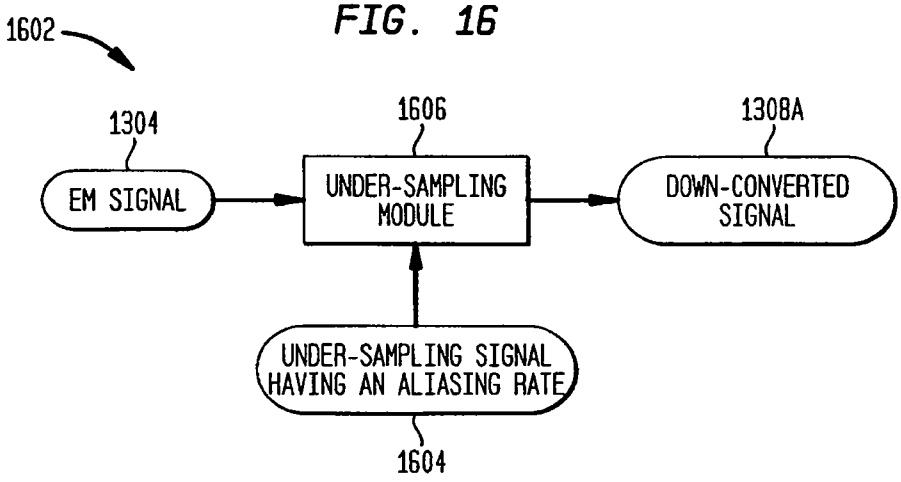

1602
1304
EM SIGNAL
1606
UNDER-SAMPLING MODULE
1308A
DOWN-CONVERTED SIGNAL
UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE
1604

FIG. 17

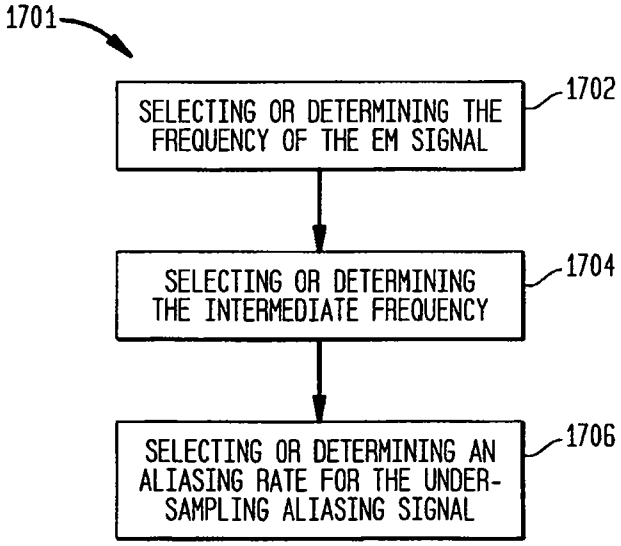

1701
SELECTING OR DETERMINING THE FREQUENCY OF THE EM SIGNAL
1702
SELECTING OR DETERMINING THE INTERMEDIATE FREQUENCY
1704
SELECTING OR DETERMINING AN ALIASING RATE FOR THE UNDER-SAMPLING ALIASING SIGNAL
1706

FIG. 18A

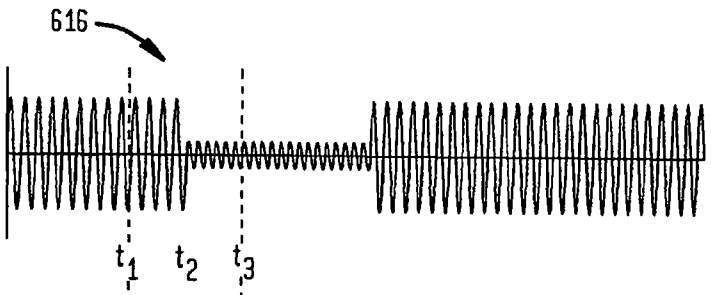


FIG. 18B

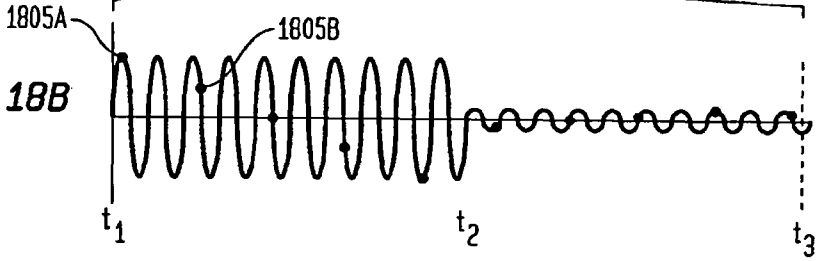


FIG. 18C

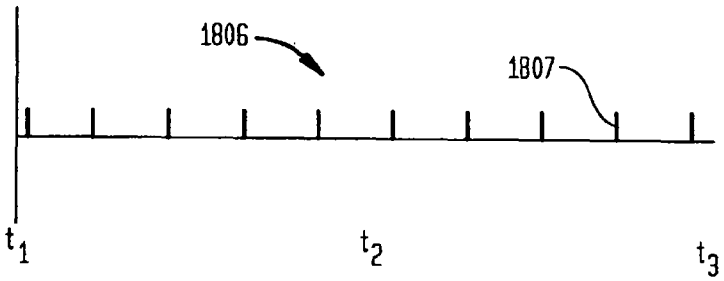


FIG. 18D

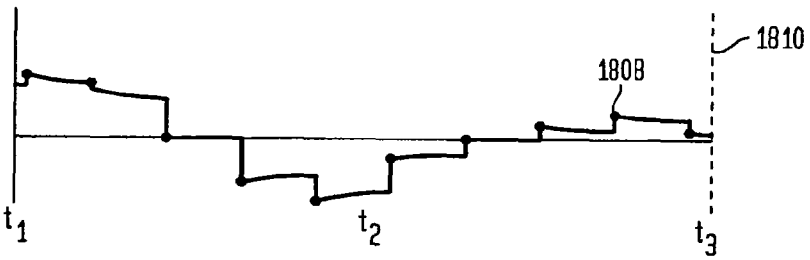


FIG. 18E

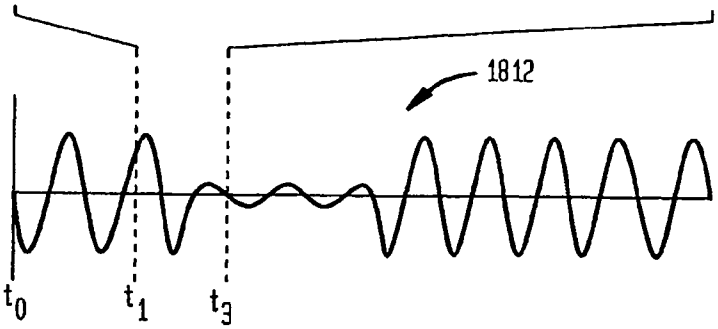


FIG. 19A

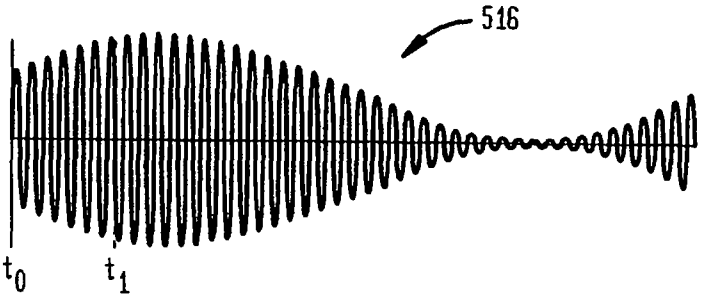


FIG. 19B

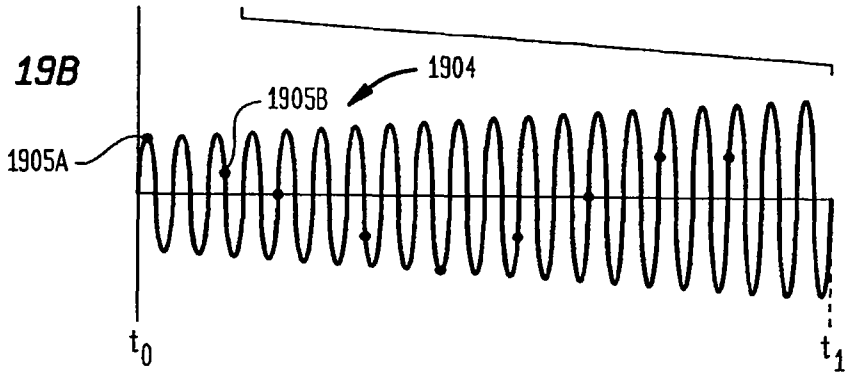


FIG. 19C

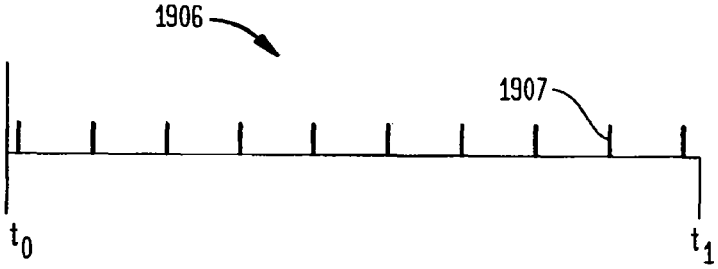


FIG. 19D

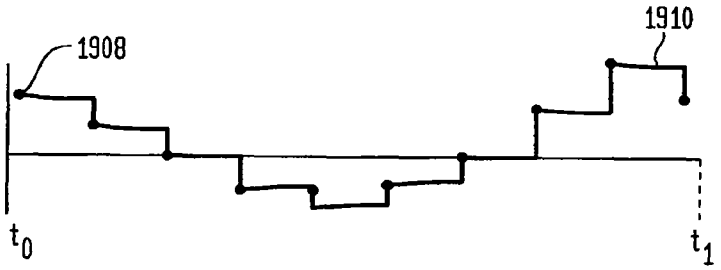


FIG. 19E

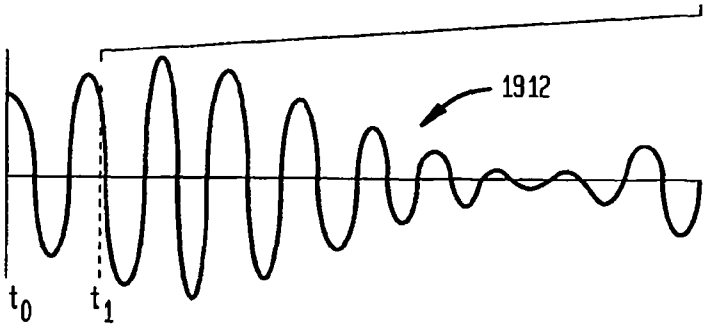


FIG. 20A

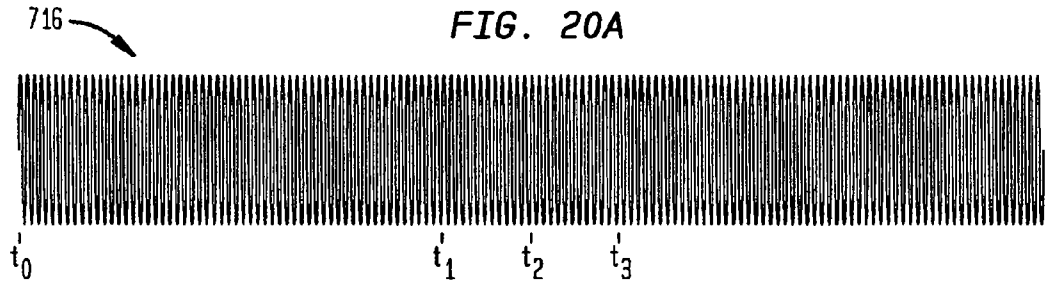


FIG. 20B

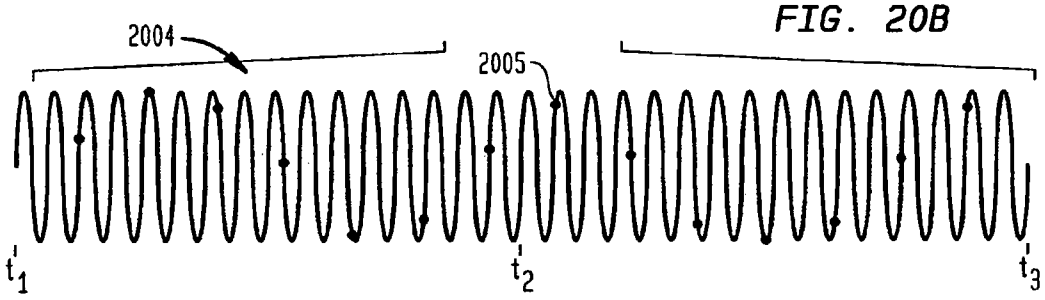


FIG. 20C

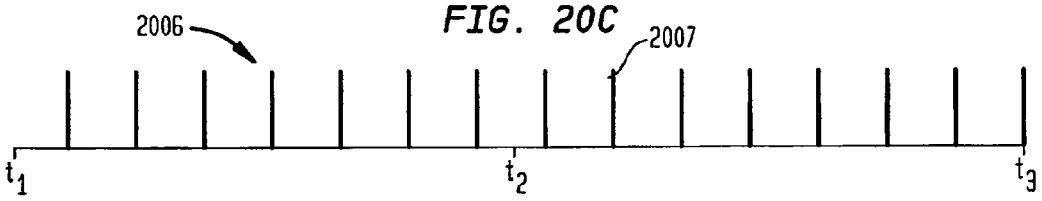


FIG. 20D

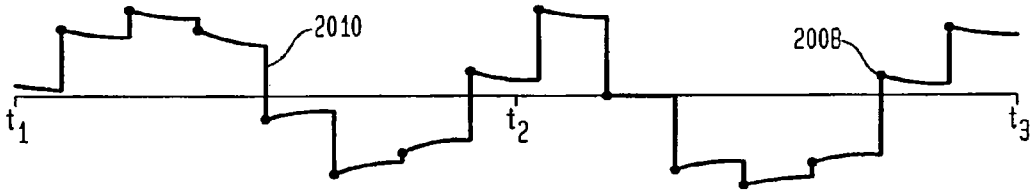


FIG. 20E

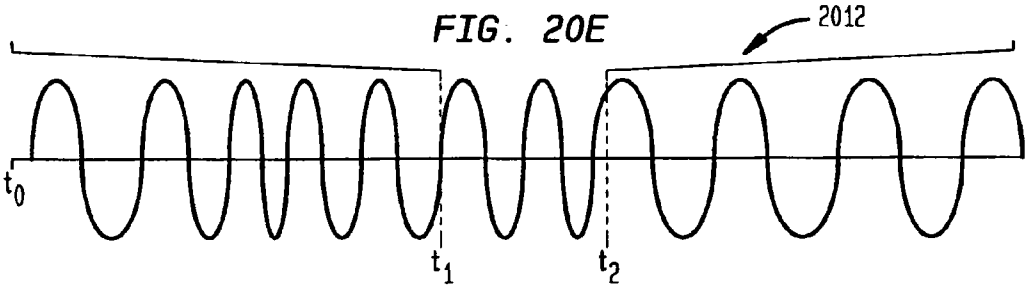


FIG. 21A

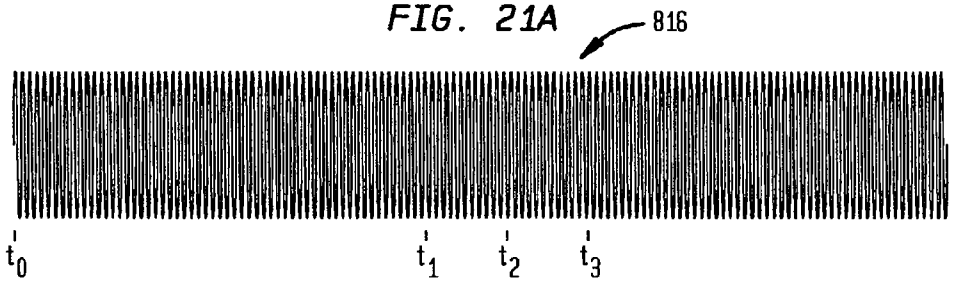


FIG. 21B

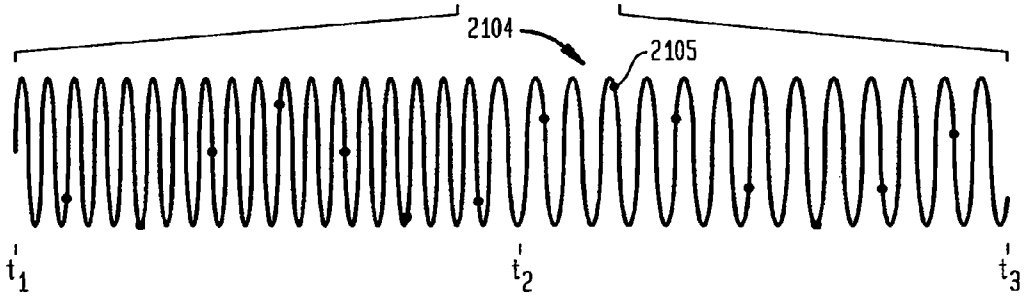


FIG. 21C

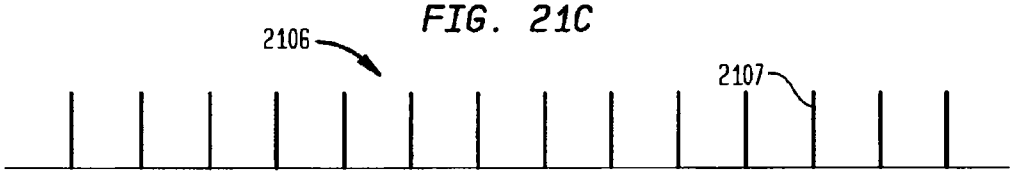


FIG. 21D

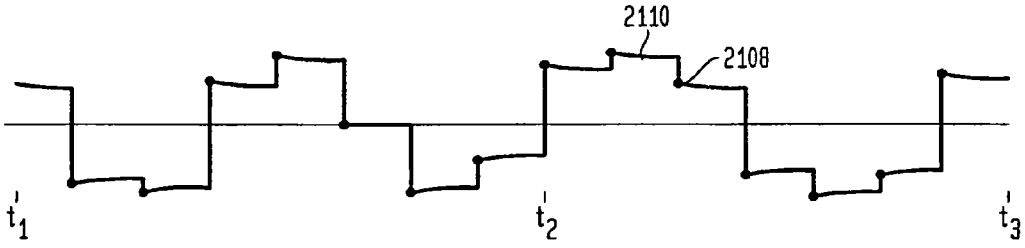


FIG. 21E

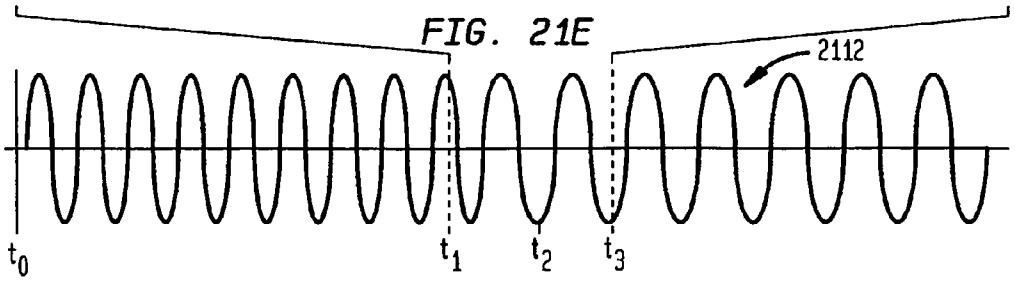


FIG. 22A

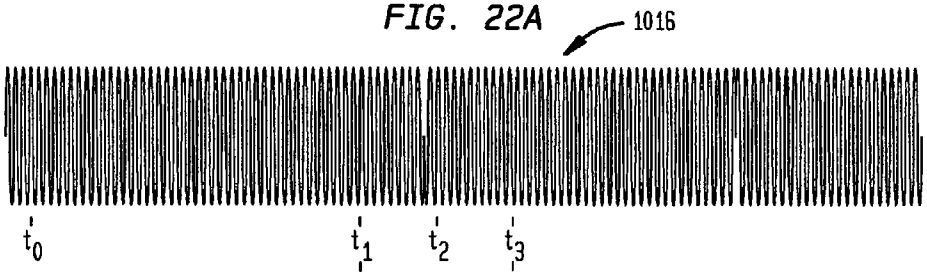


FIG. 22B

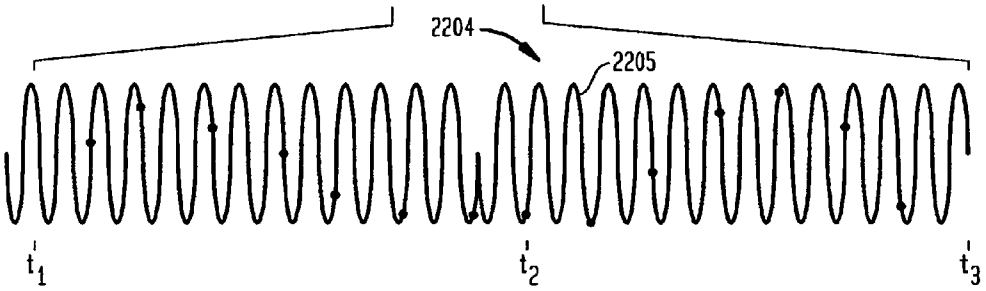


FIG. 22C

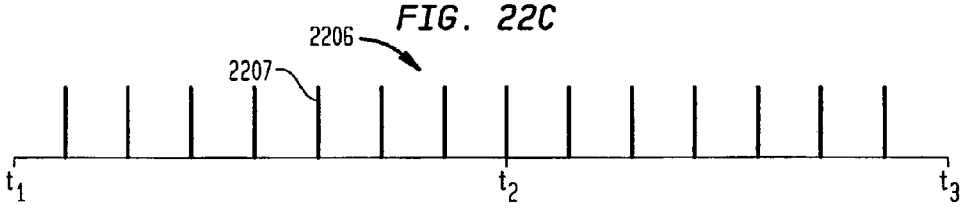


FIG. 22D

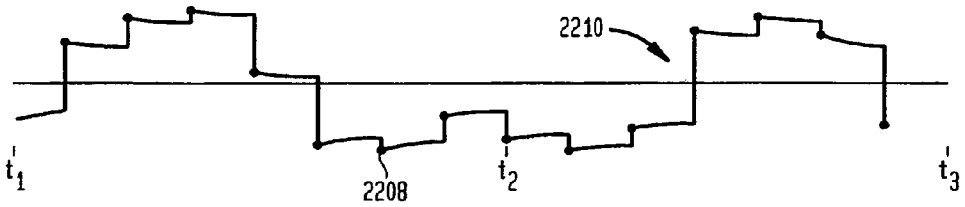


FIG. 22E

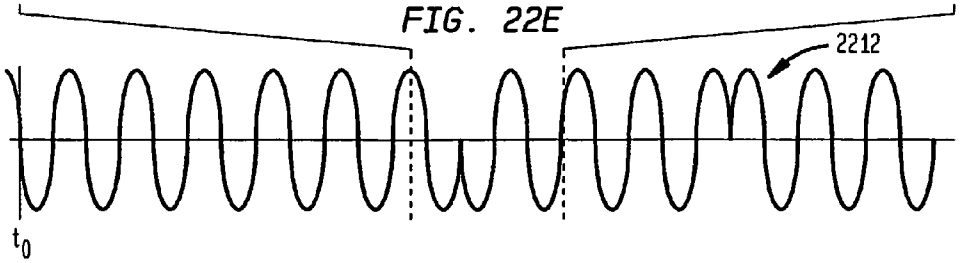


FIG. 23A

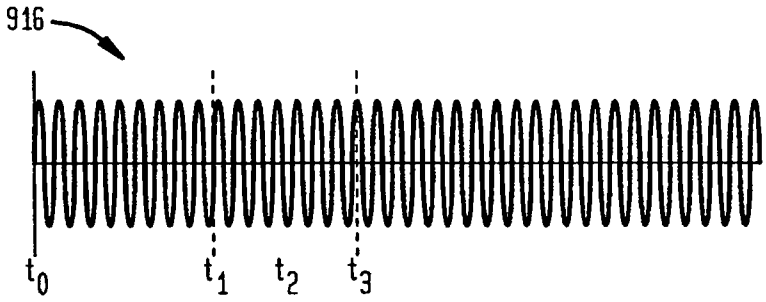


FIG. 23B

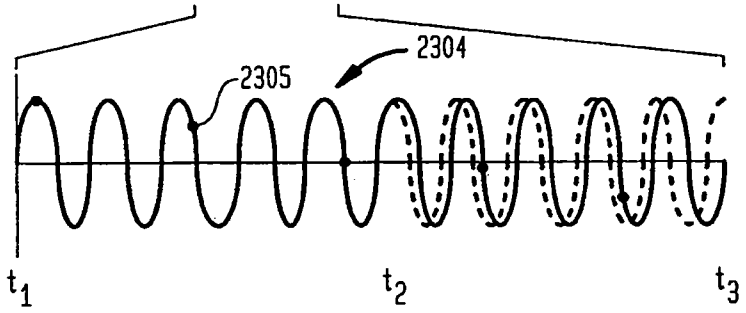


FIG. 23C

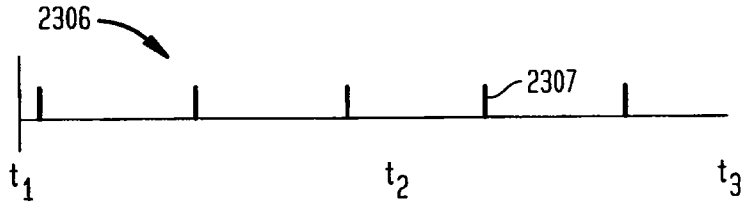


FIG. 23D

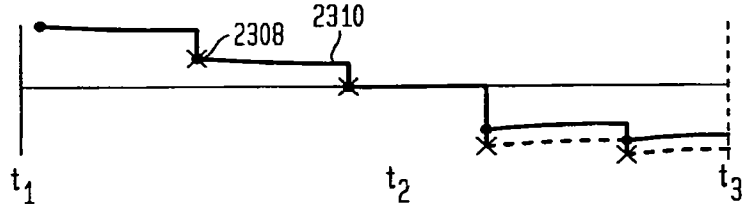
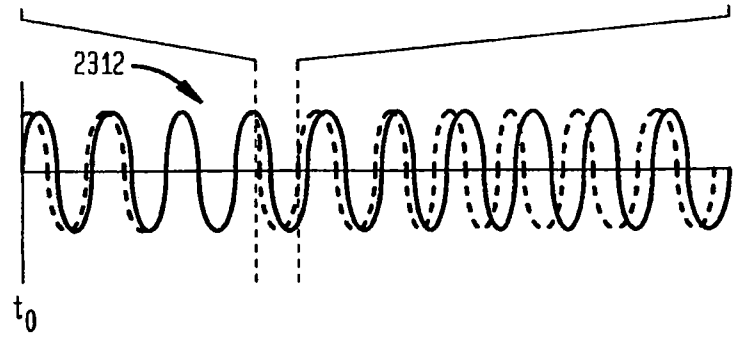


FIG. 23E



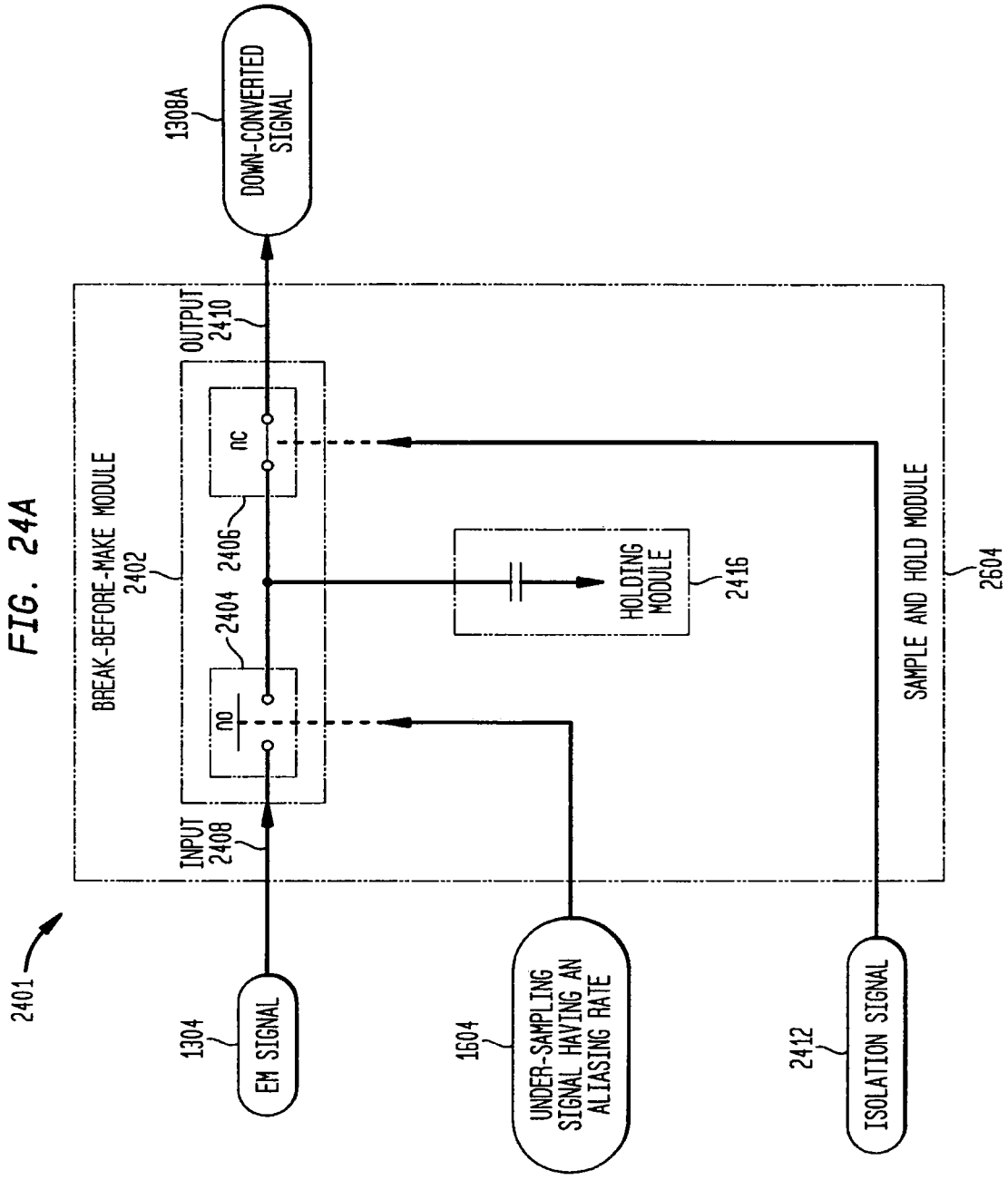

2401
1304
EM SIGNAL
1604
UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE
2412
ISOLATION SIGNAL
BREAK-BEFORE-MAKE MODULE
2402
INPUT 2408
OUTPUT 2410
2404
2406
no
nc
HOLDING MODULE
2416
SAMPLE AND HOLD MODULE
2604
1308A
DOWN-CONVERTED SIGNAL

FIG. 24A

FIG. 24B

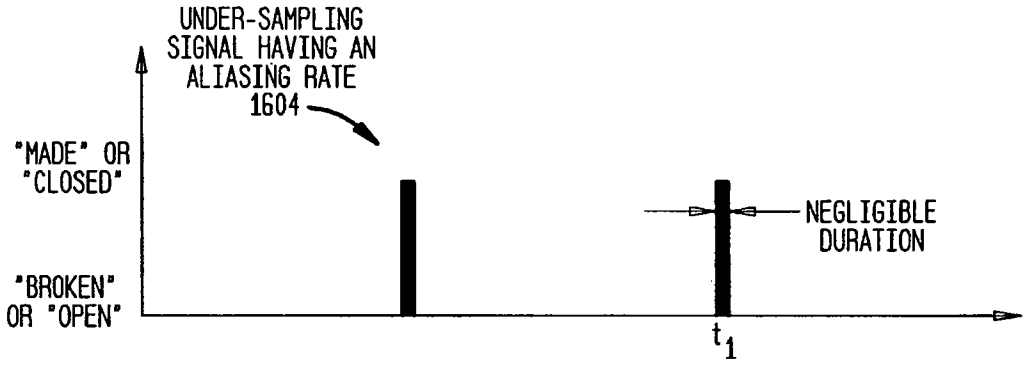
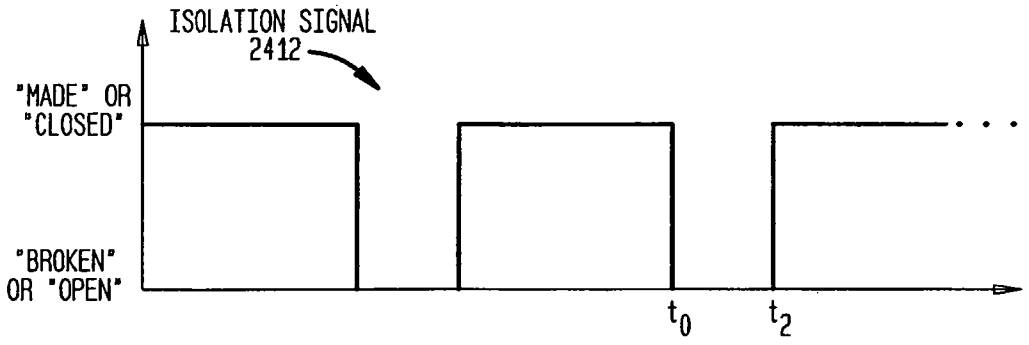


FIG. 24C



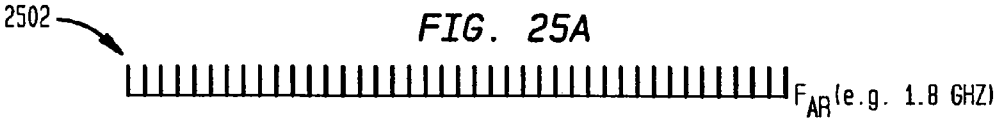


FIG. 25A

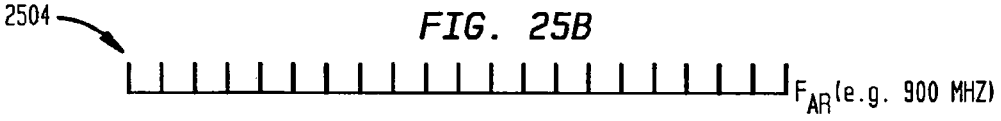


FIG. 25B

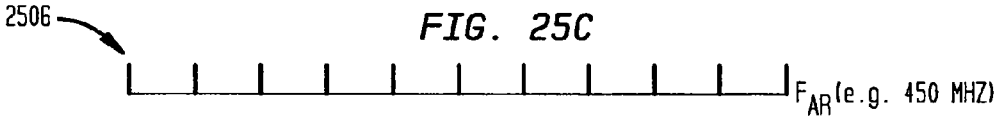


FIG. 25C

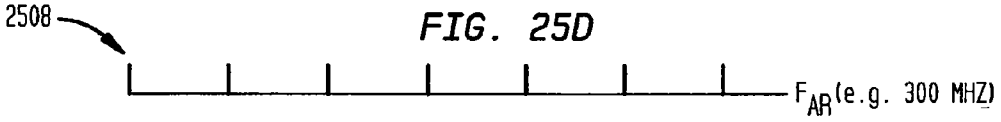


FIG. 25D

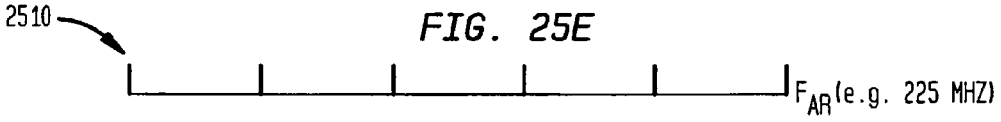


FIG. 25E

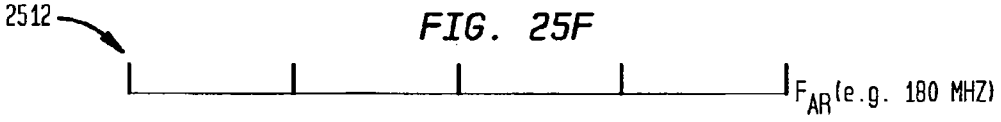


FIG. 25F

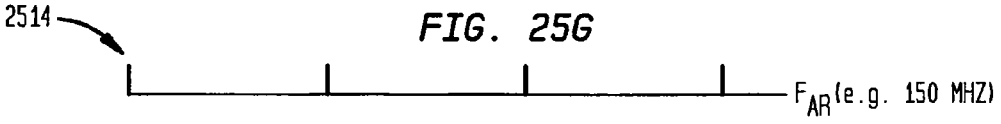


FIG. 25G

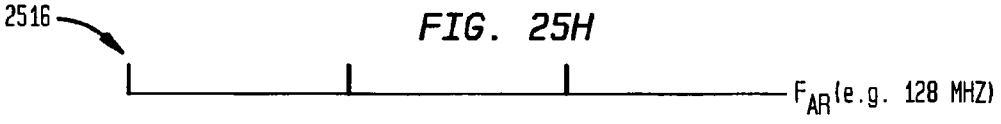


FIG. 25H

FIG. 26A

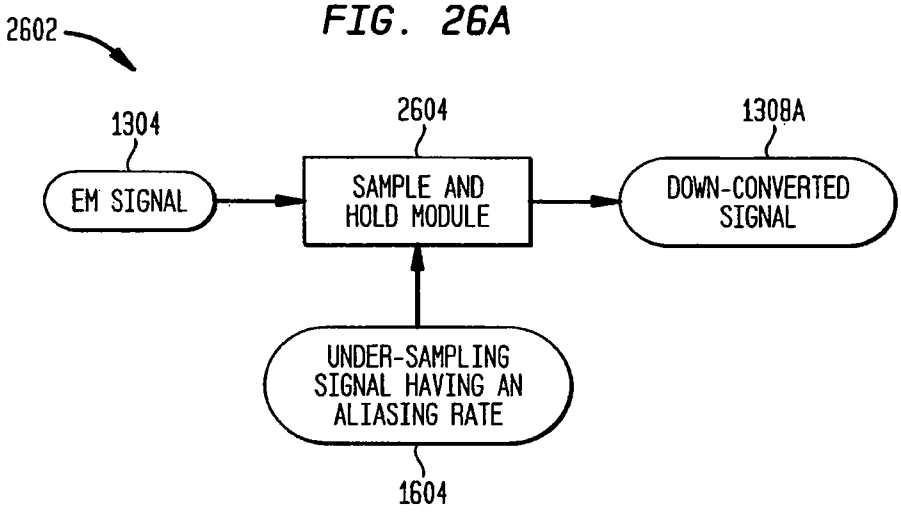
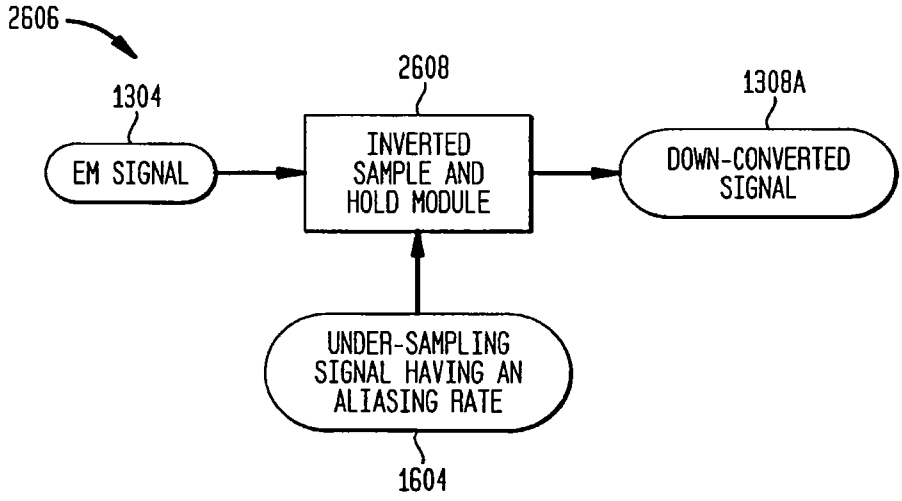


FIG. 26B



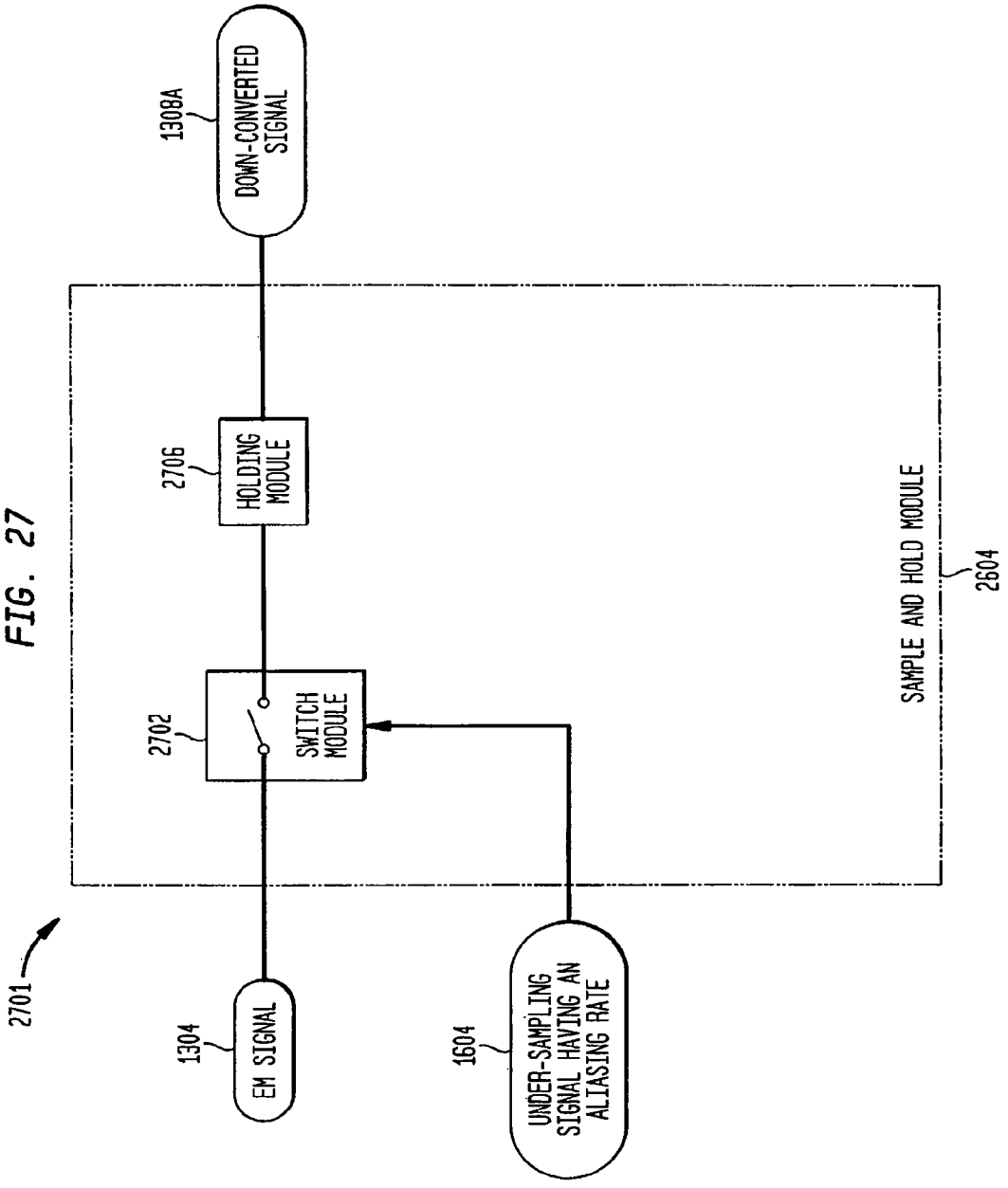

2701
1304
EM SIGNAL
1604
UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE
2702
SWITCH MODULE
2706
HOLDING MODULE
1308A
DOWN-CONVERTED SIGNAL
SAMPLE AND HOLD MODULE
2604

FIG. 27

FIG. 28A

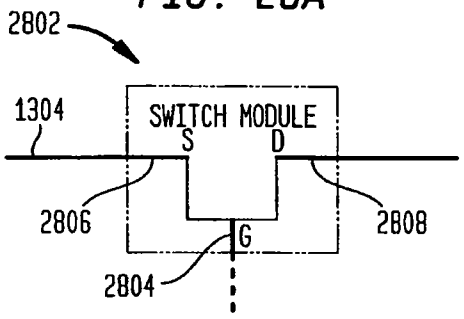


FIG. 28B

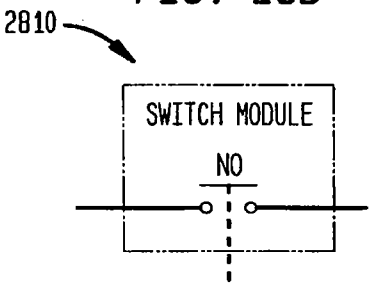


FIG. 28C

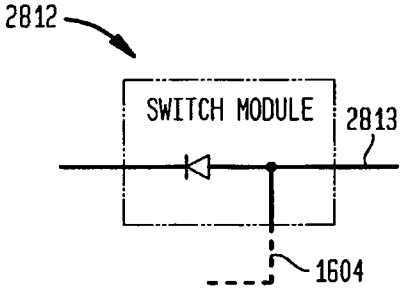


FIG. 28D

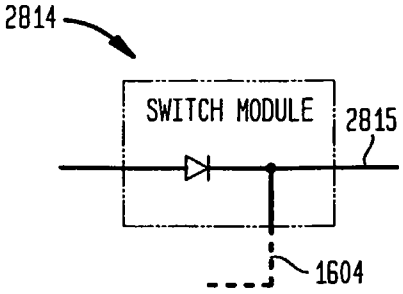


FIG. 29A

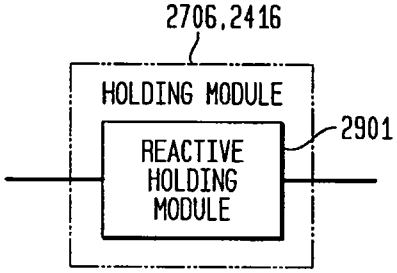


FIG. 29B

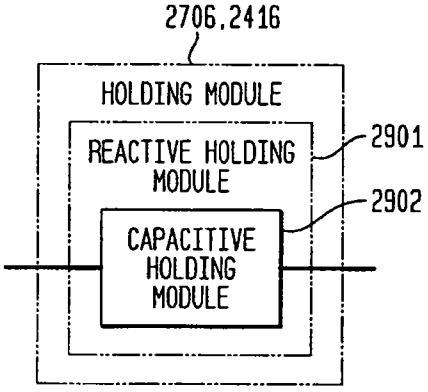


FIG. 29C

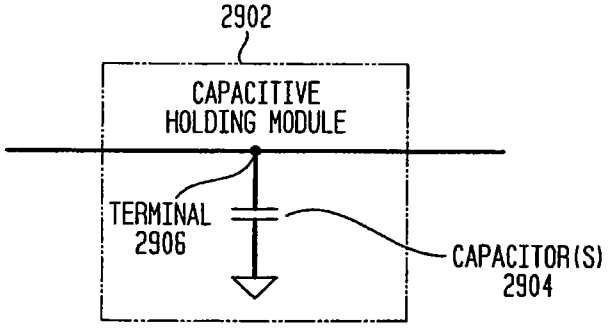


FIG. 29D

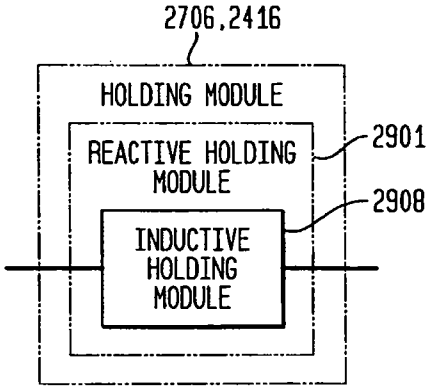


FIG. 29E

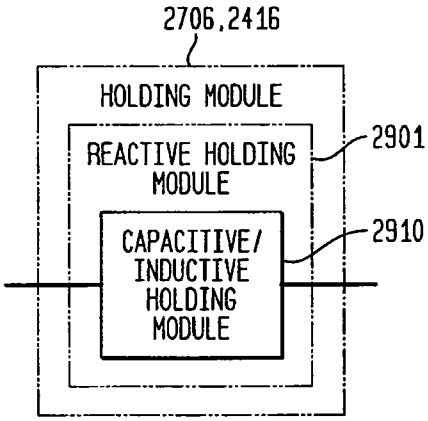


FIG. 29F

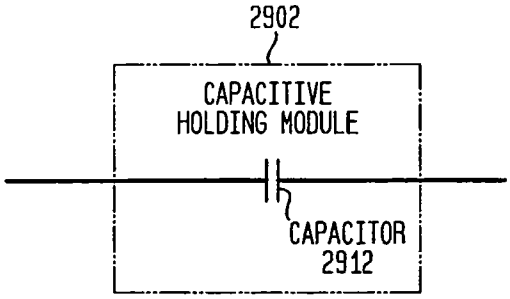


FIG. 29G

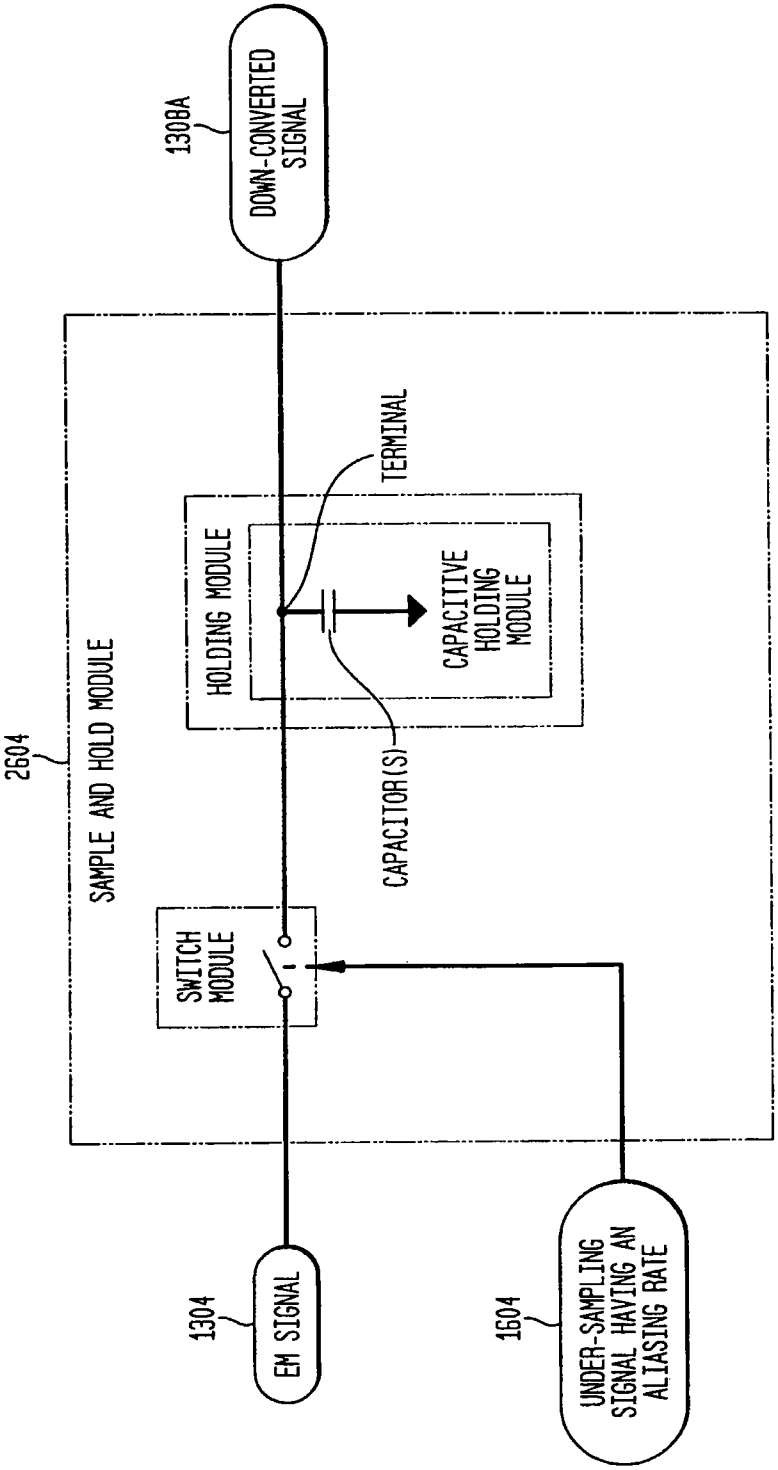
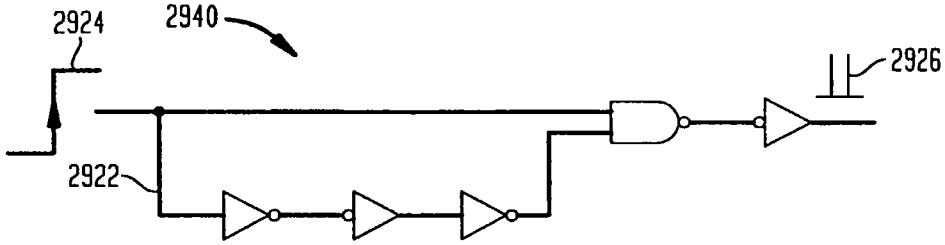
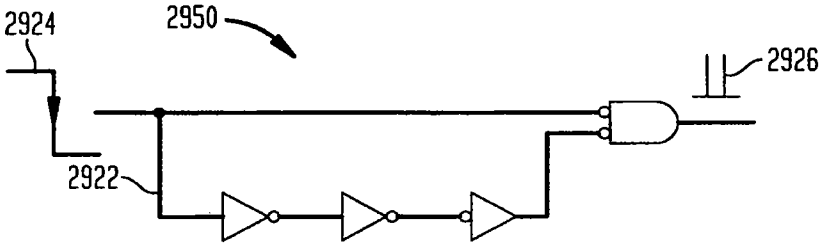

1308A
DOWN-CONVERTED SIGNAL
2604
SAMPLE AND HOLD MODULE
HOLDING MODULE
TERMINAL
CAPACITIVE HOLDING MODULE
CAPACITOR(S)
SWITCH MODULE
1304
EM SIGNAL
1604
UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE

FIG. 29H



A. RISING EDGE PULSE GENERATOR

FIG. 29I



B. FALLING-EDGE PULSE GENERATOR

FIG. 29J

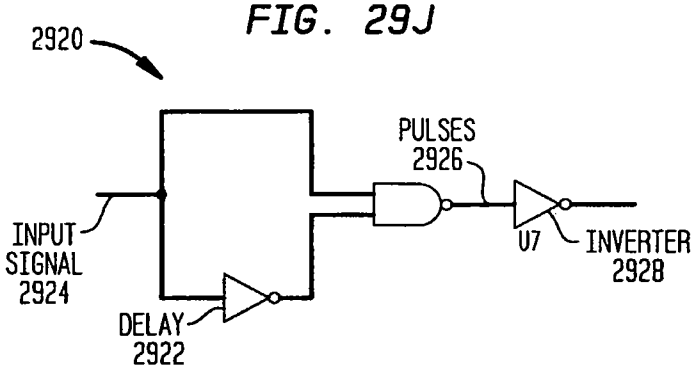


FIG. 29K

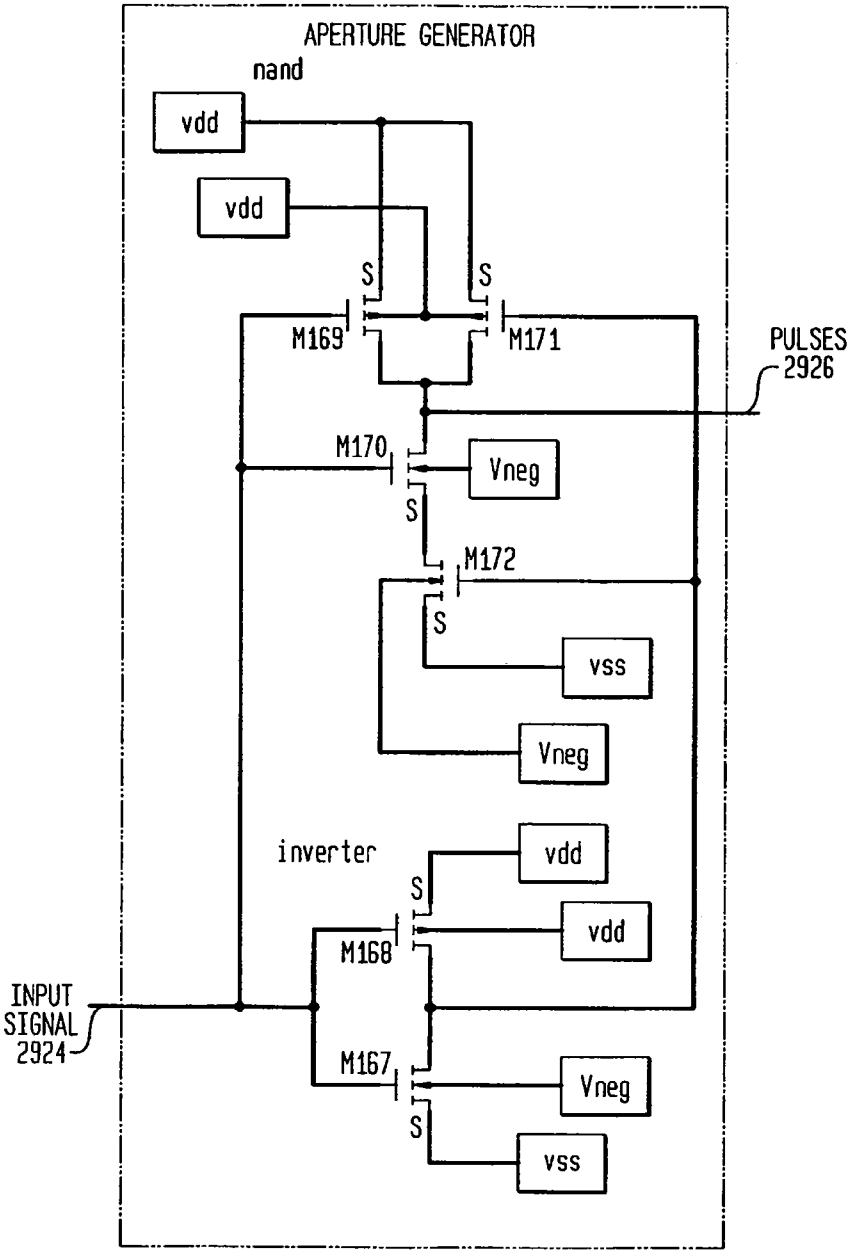


FIG. 29L

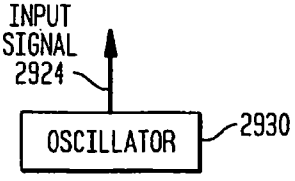


FIG. 30

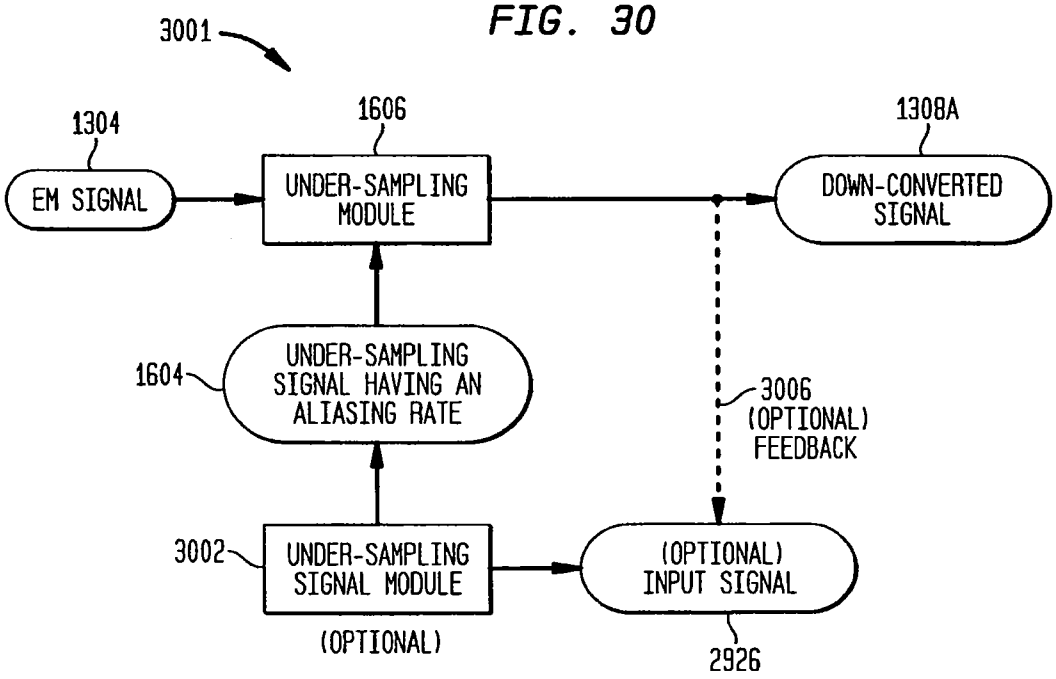

3001
1304
EM SIGNAL
1606
UNDER-SAMPLING MODULE
1308A
DOWN-CONVERTED SIGNAL
1604
UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE
3006
(OPTIONAL) FEEDBACK
3002
UNDER-SAMPLING SIGNAL MODULE
(OPTIONAL)
(OPTIONAL) INPUT SIGNAL
2926

FIG. 31A

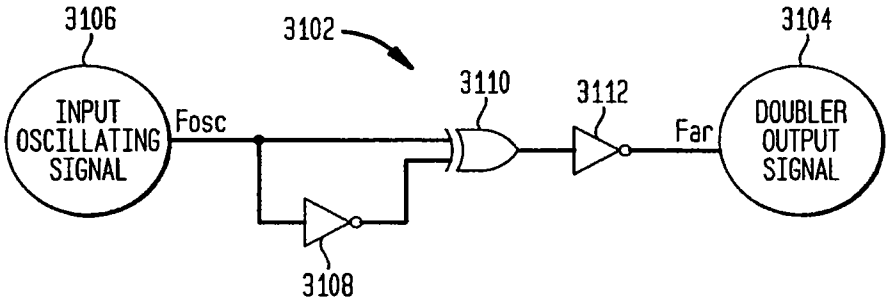

3106
3102
3104
3110
3112
INPUT OSCILLATING SIGNAL
Fosc
Far
DOUBLER OUTPUT SIGNAL
3108

FIG. 31B

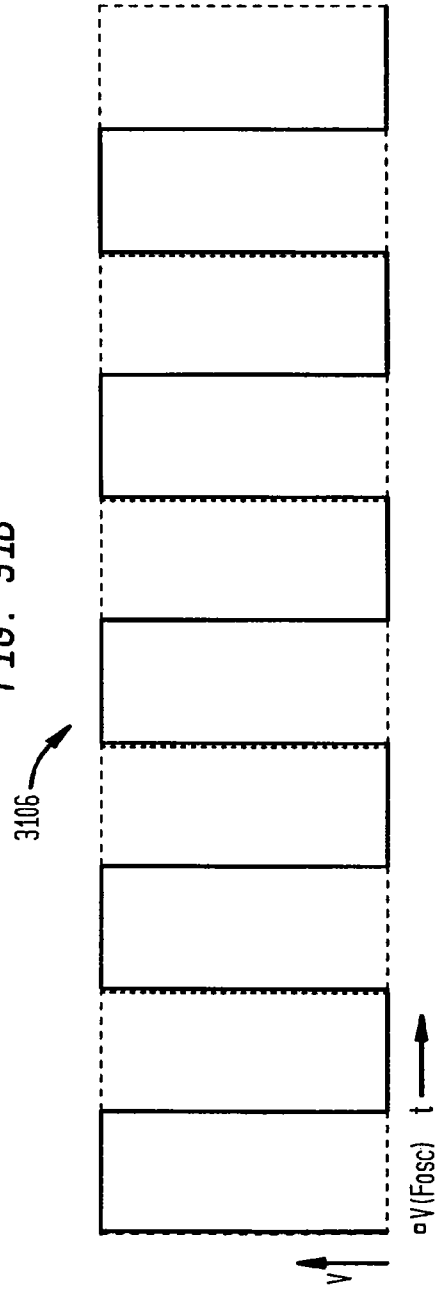


FIG. 31C

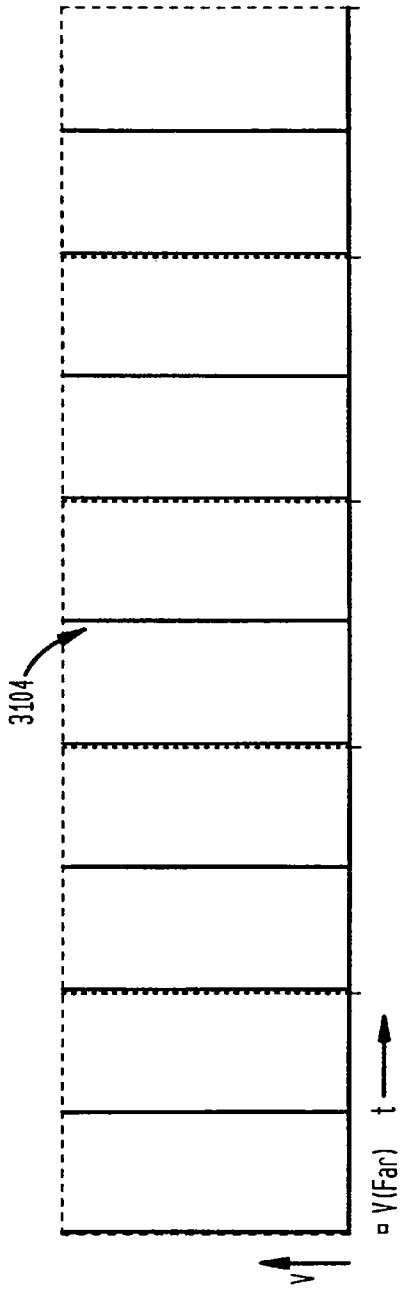


FIG. 32A

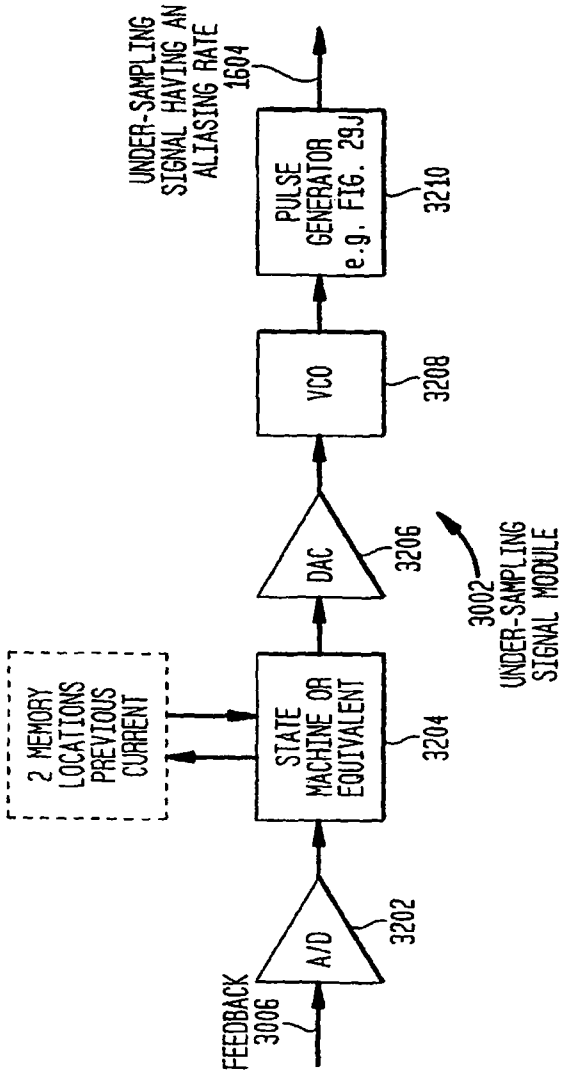
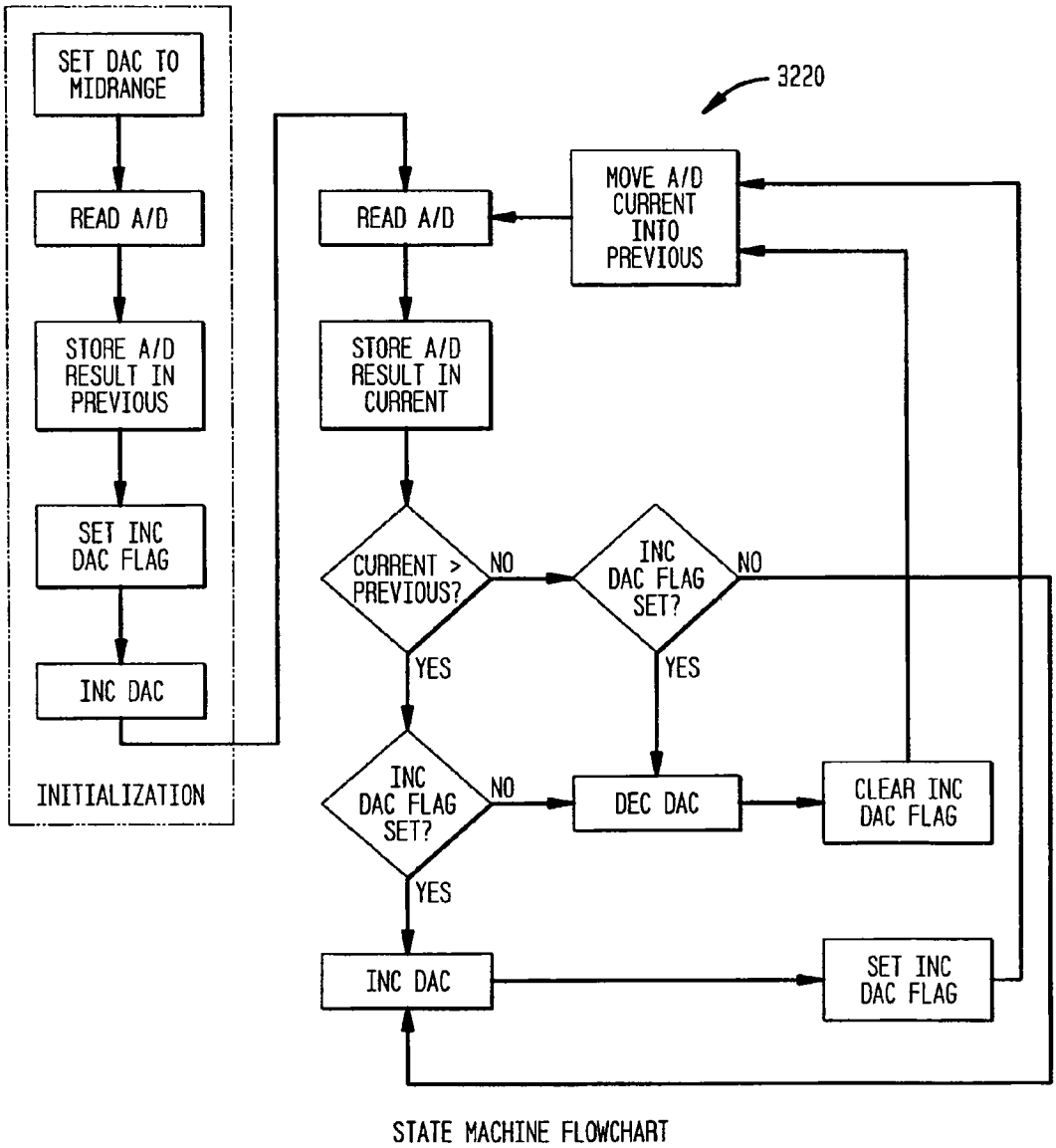
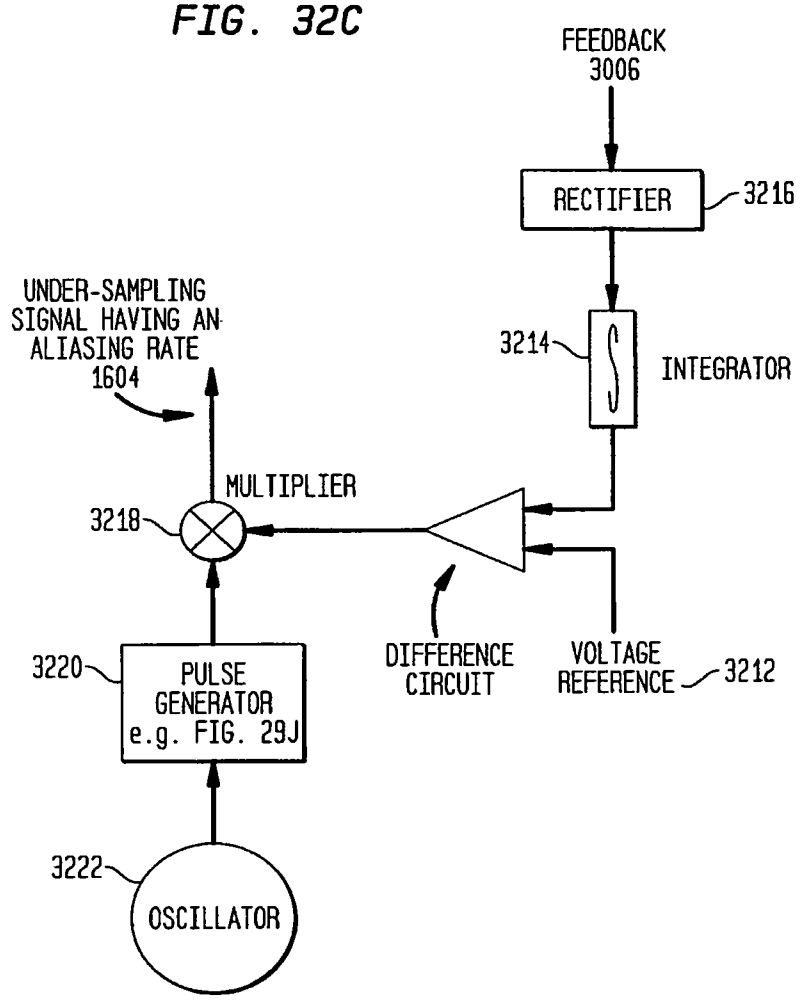

UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE
1604
PULSE GENERATOR e.g. FIG. 29J
3210
VCO
3208
DAC
3206
3002
UNDER-SAMPLING SIGNAL MODULE
2 MEMORY LOCATIONS PREVIOUS CURRENT
STATE MACHINE OR EQUIVALENT
3204
A/D
3202
FEEDBACK
3006

FIG. 32B



STATE MACHINE FLOWCHART

FIG. 32C



ENERGY TRANSFER SIGNAL MODULE 3002

FIG. 33A

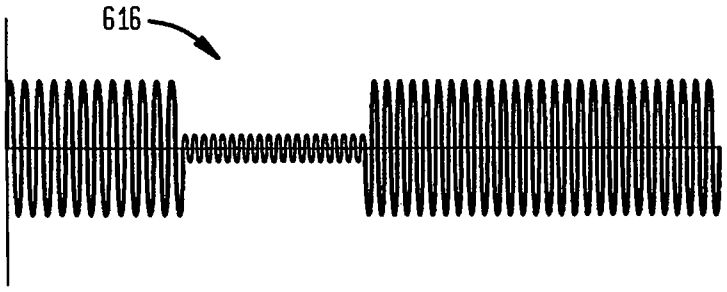


FIG. 33B

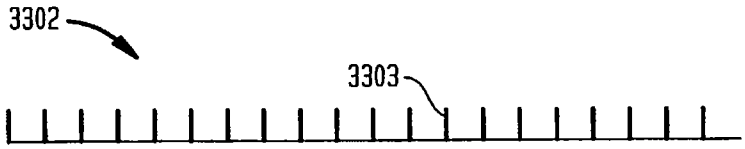


FIG. 33C

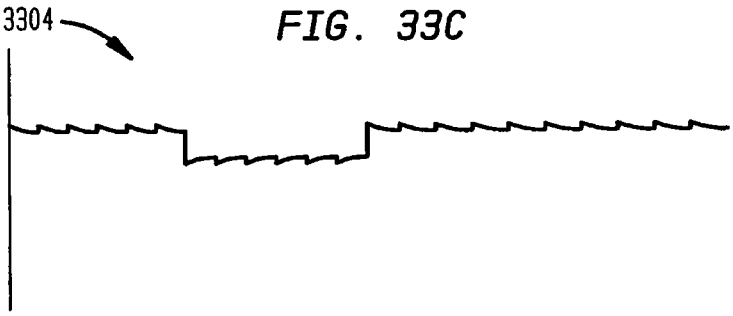
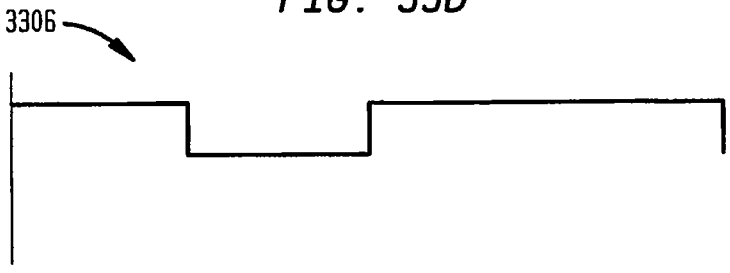


FIG. 33D



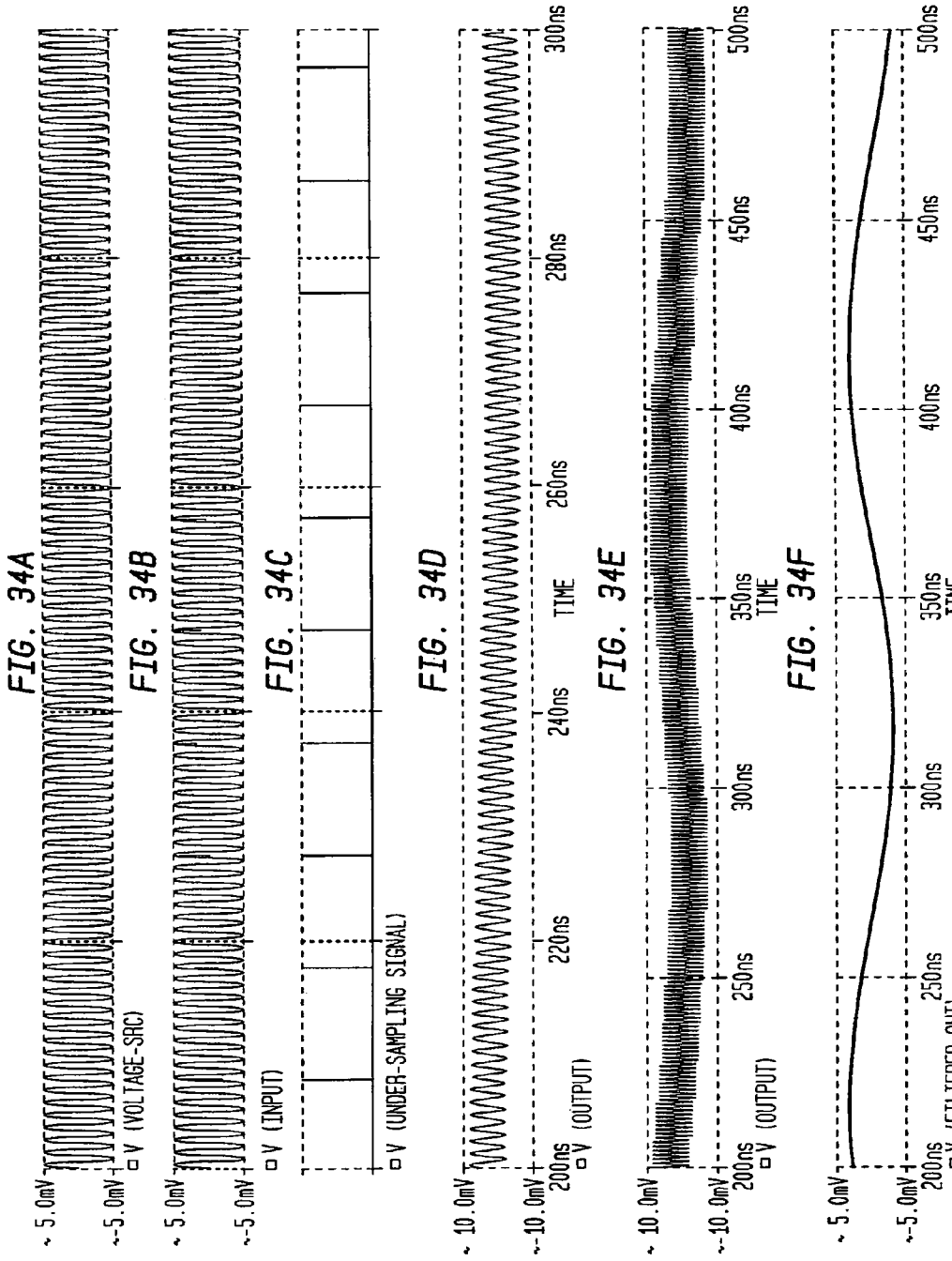


FIG. 34A

FIG. 34B

FIG. 34C

FIG. 34D

FIG. 34E

FIG. 34F

FIG. 35A

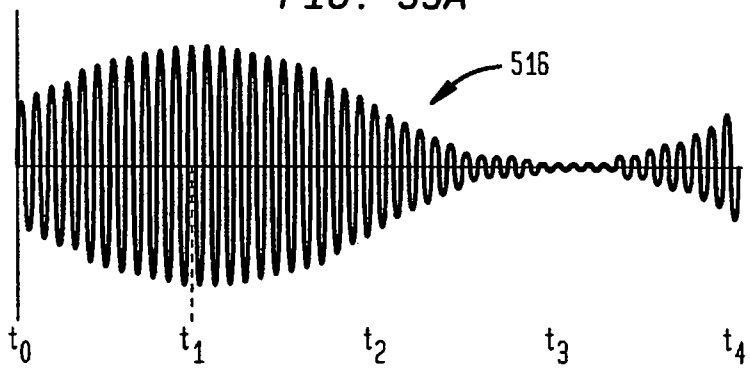


FIG. 35B

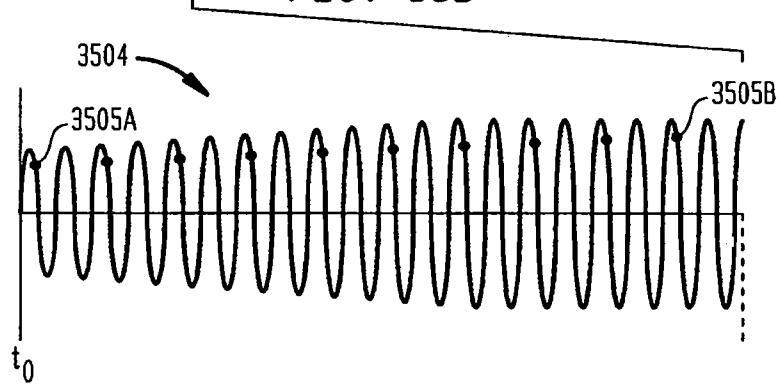


FIG. 35C



FIG. 35D

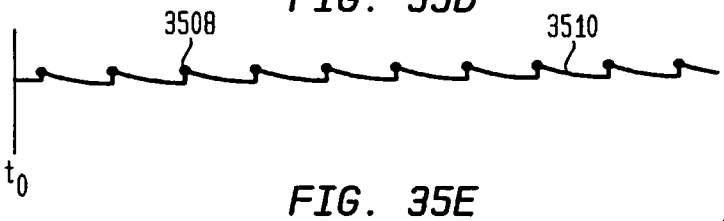


FIG. 35E

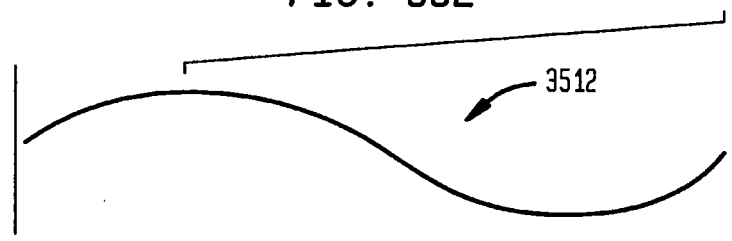


FIG. 36A

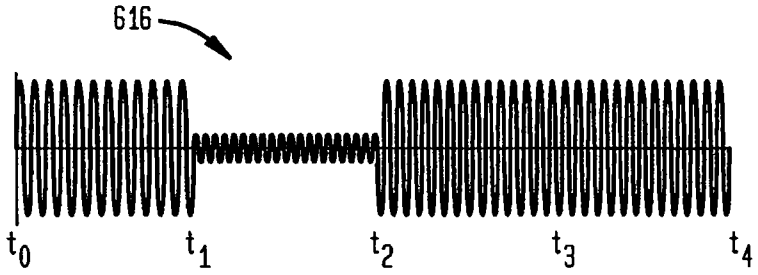


FIG. 36B

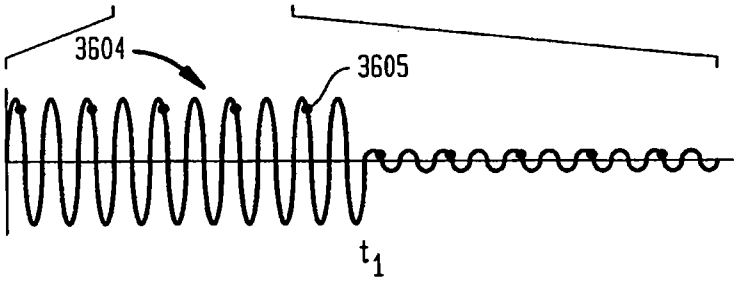


FIG. 36C

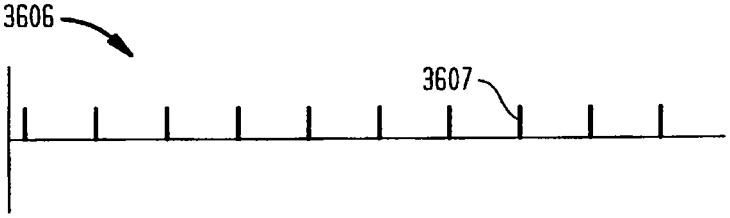


FIG. 36D

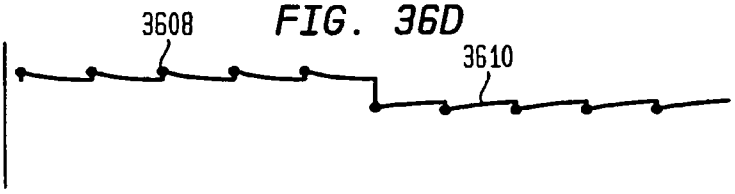


FIG. 36E

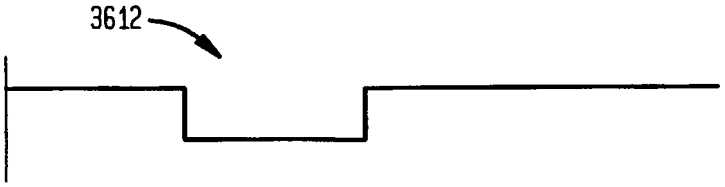


FIG. 37A

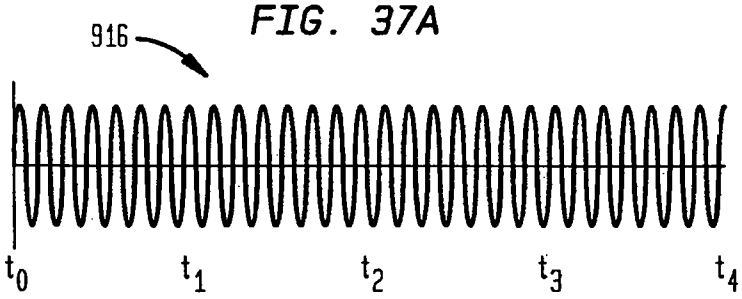


FIG. 37B

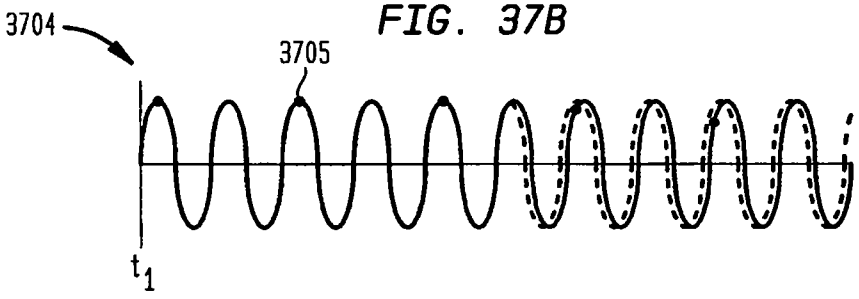


FIG. 37C

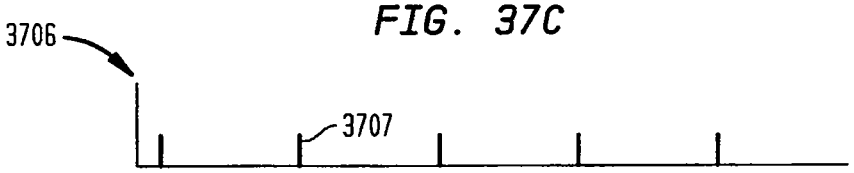


FIG. 37D

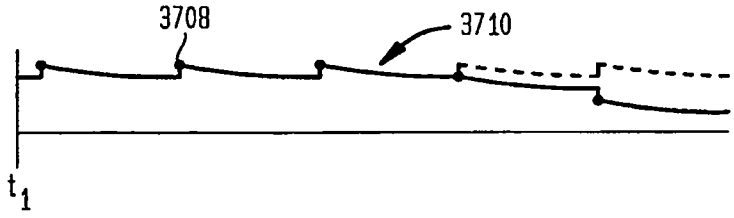


FIG. 37E

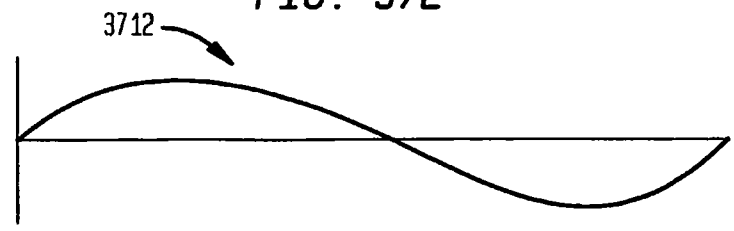


FIG. 38A

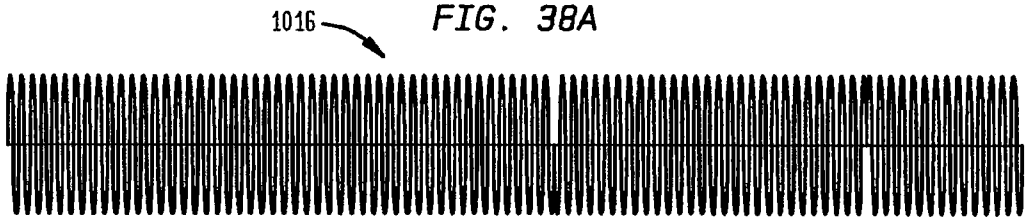


FIG. 38B

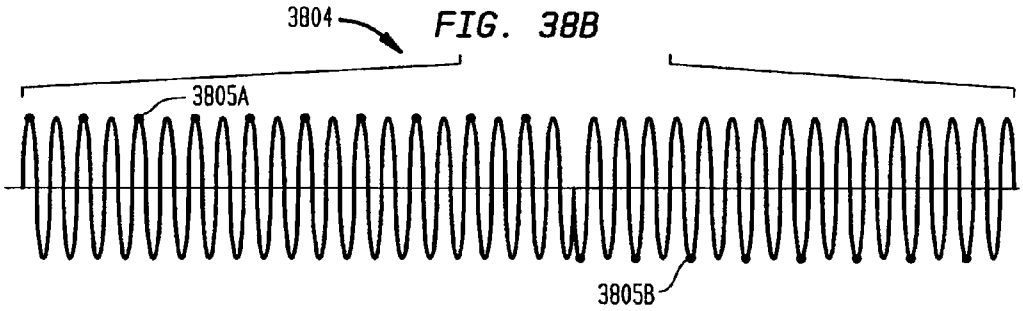


FIG. 38C

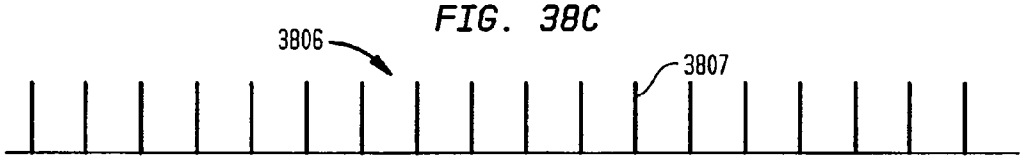


FIG. 38D

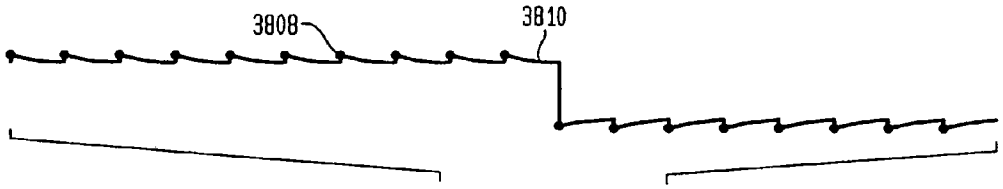


FIG. 38E

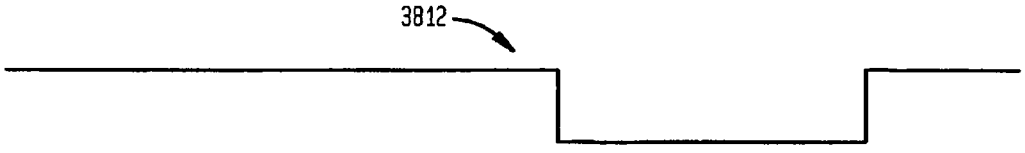


FIG. 39A

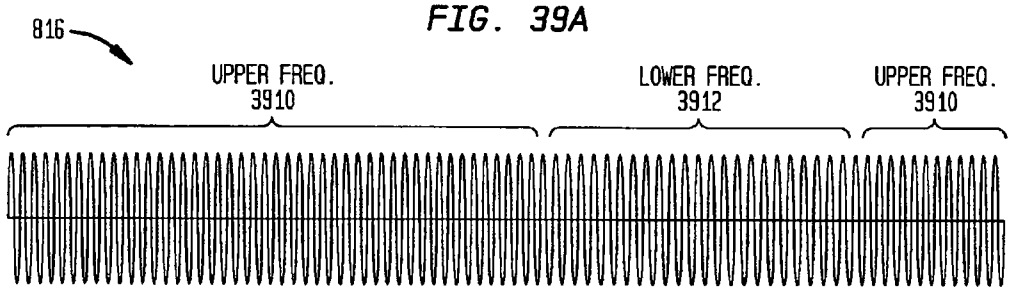


FIG. 39B

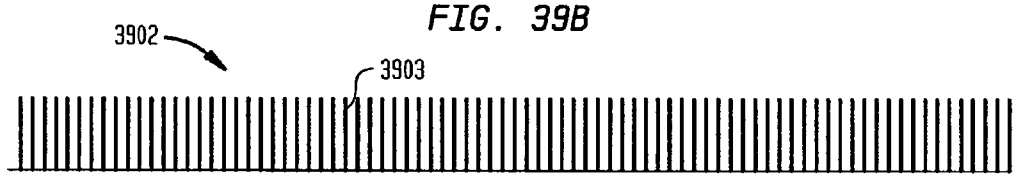


FIG. 39C

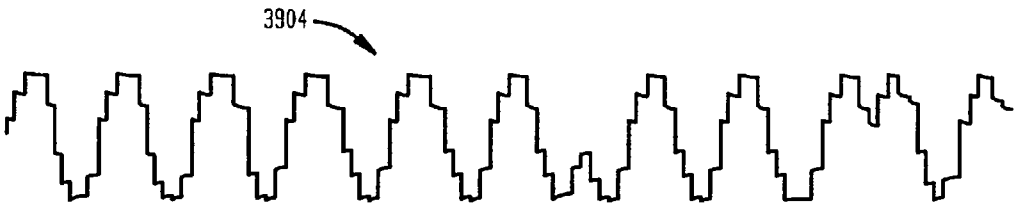


FIG. 39D

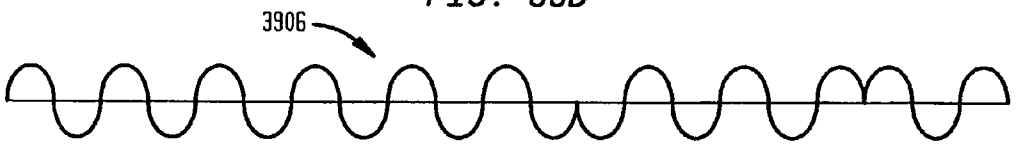


FIG. 40A

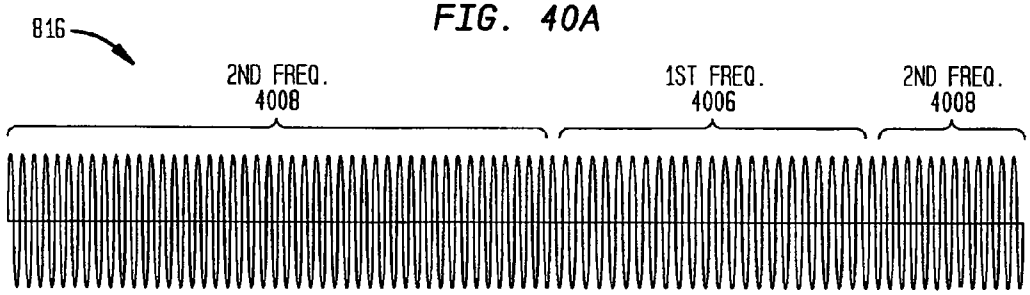


FIG. 40B

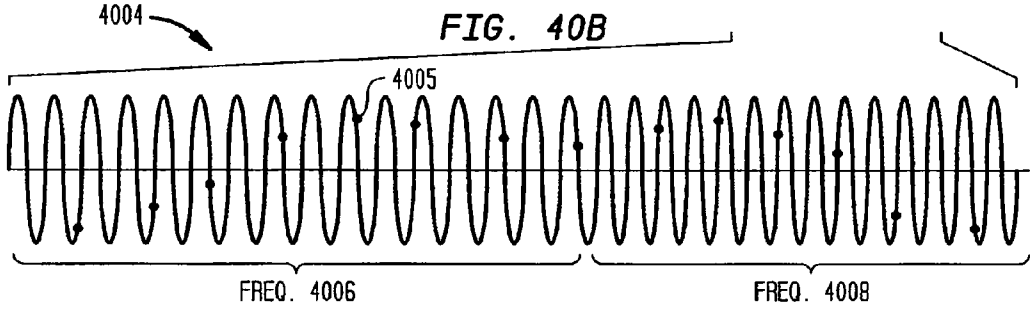


FIG. 40C

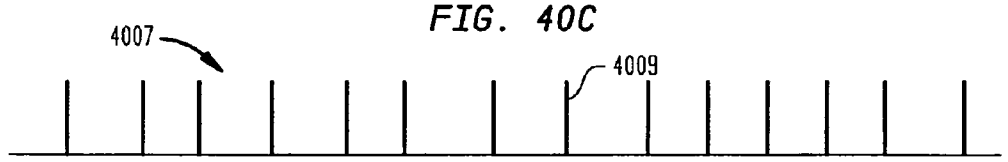


FIG. 40D

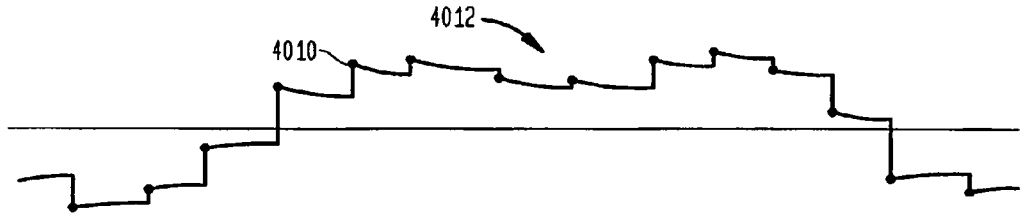
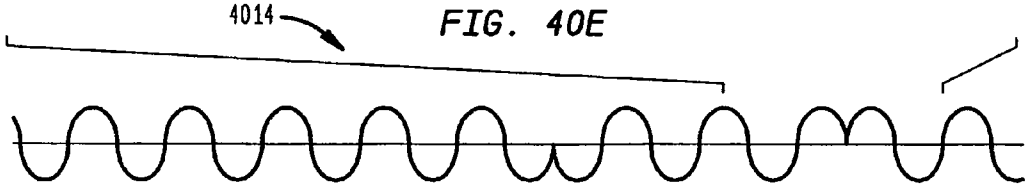


FIG. 40E



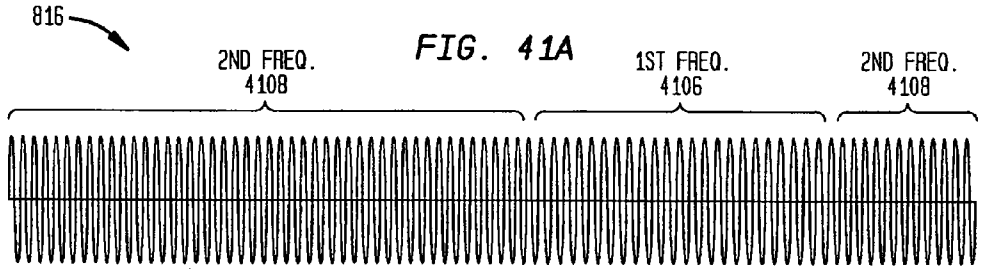


FIG. 41A

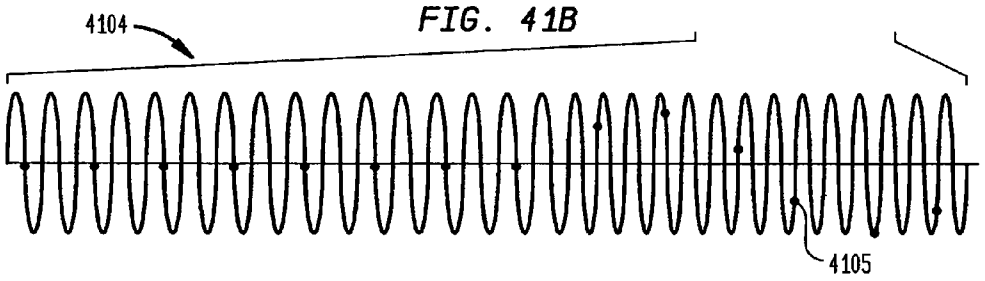


FIG. 41B

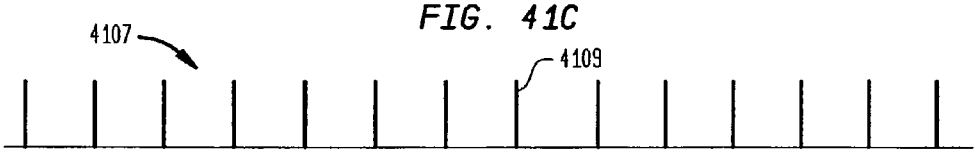


FIG. 41C

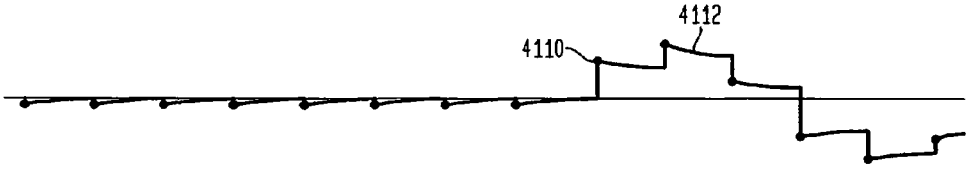


FIG. 41D

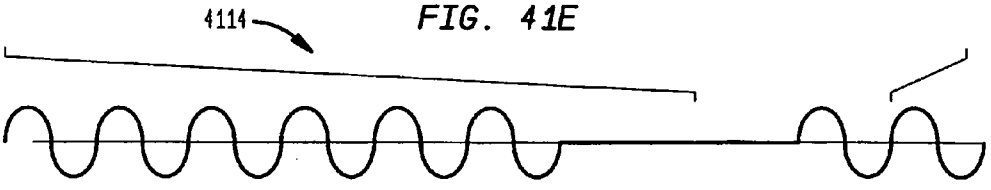


FIG. 41E

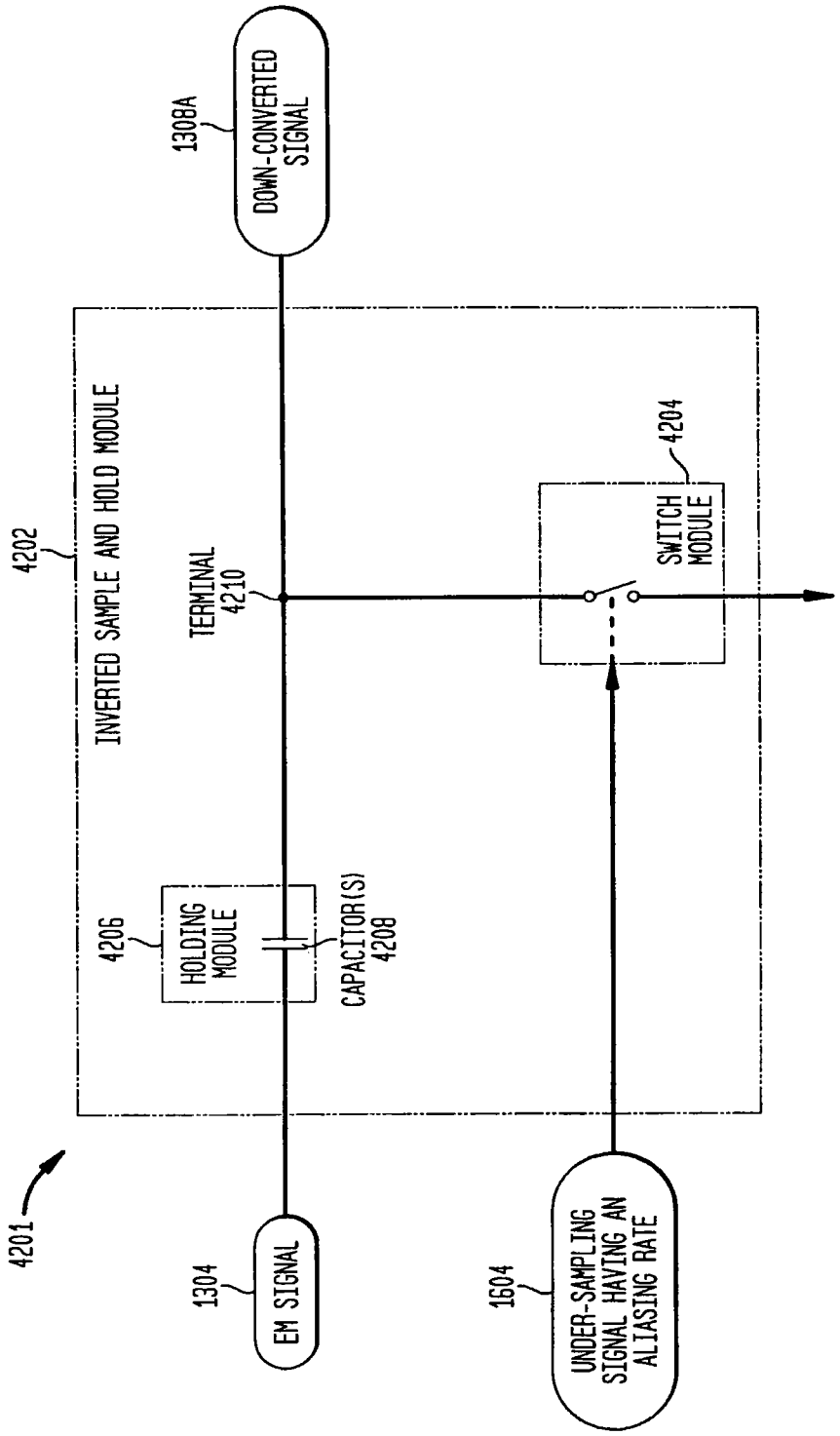

1308A
DOWN-CONVERTED SIGNAL
4202
INVERTED SAMPLE AND HOLD MODULE
TERMINAL 4210
4204
SWITCH MODULE
4206
HOLDING MODULE
CAPACITOR(S) 4208
4201
1304
EM SIGNAL
1604
UNDER-SAMPLING SIGNAL HAVING AN ALIASING RATE

FIG. 42

FIG. 43

$$\Delta q(t) = 2 \cdot C \cdot A \cdot \sin\left(\frac{1}{2} \cdot T\right) \cdot \cos\left(t - \frac{1}{2} \cdot T\right)$$

FIG. 44A

DIFFERENTIAL CONFIGURATION

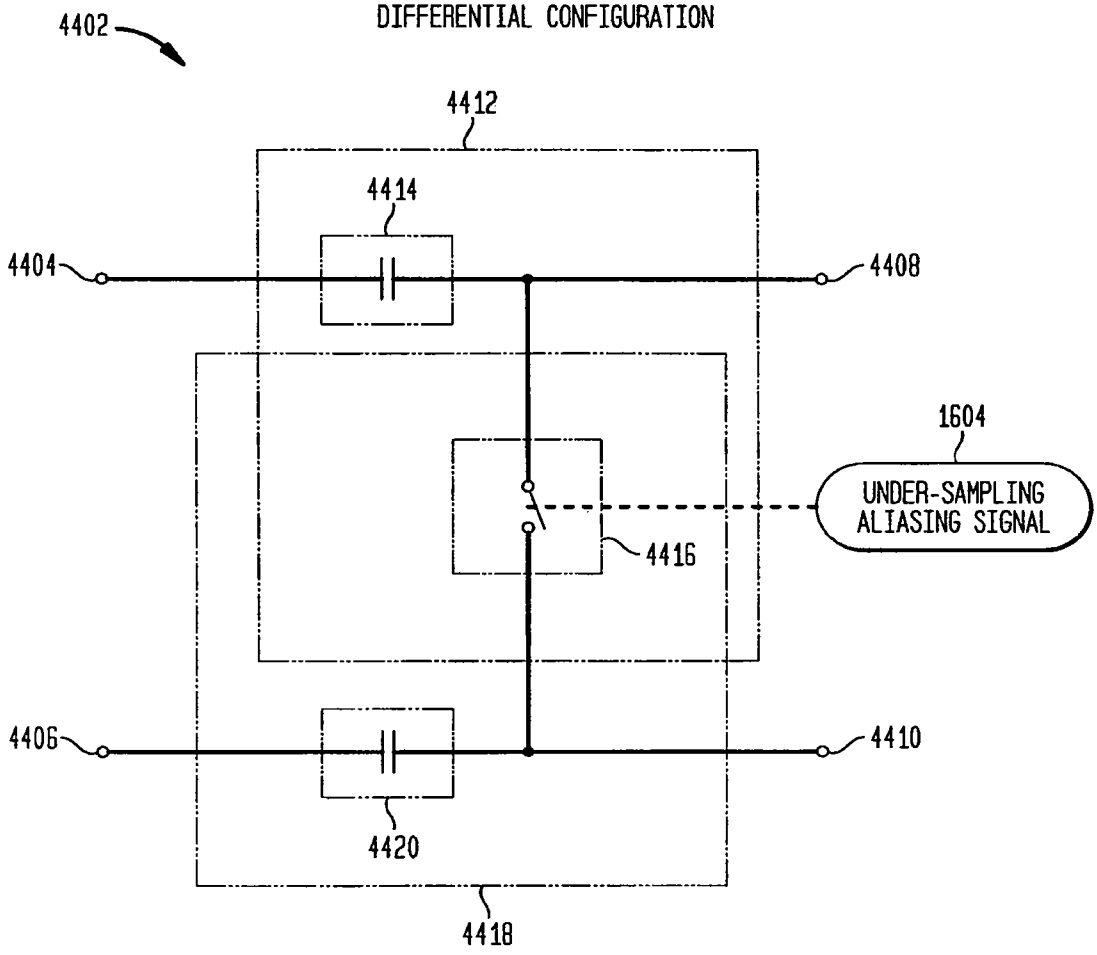


FIG. 44B

DIFFERENTIAL INPUT TO DIFFERENTIAL OUTPUT

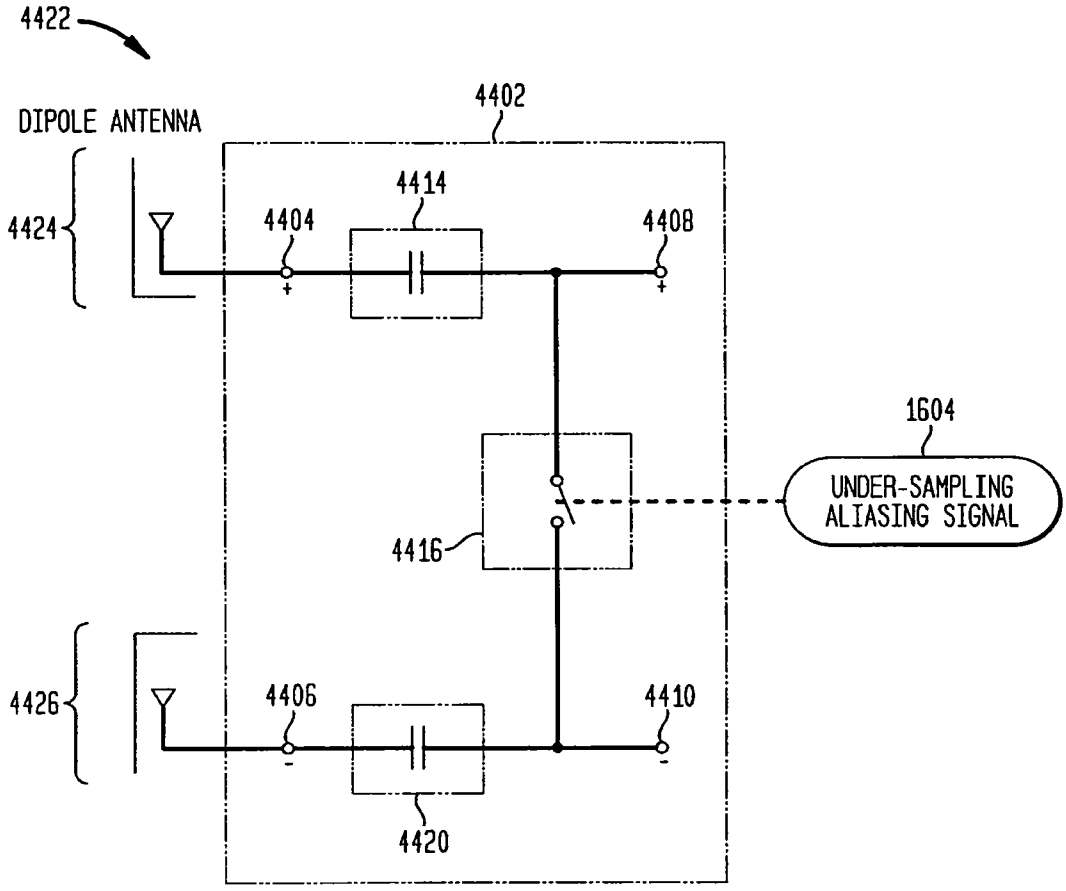


FIG. 44C

SINGLE INPUT TO DIFFERENTIAL OUTPUT

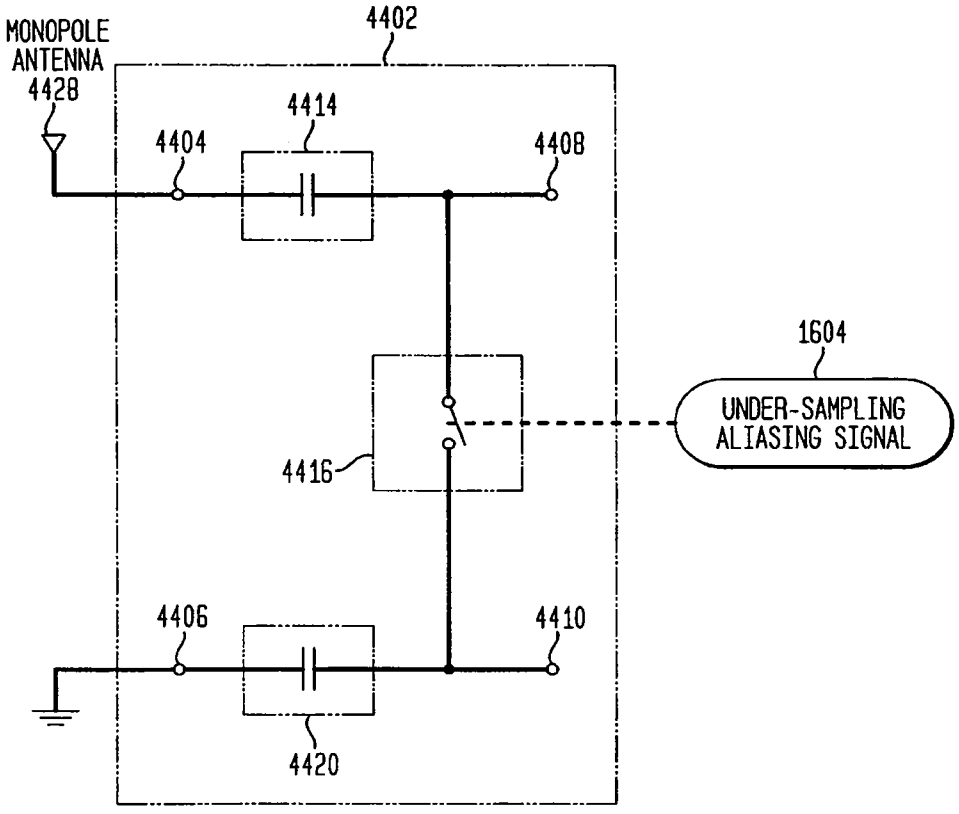


FIG. 44D

DIFFERENTIAL INPUT TO SINGLE OUTPUT

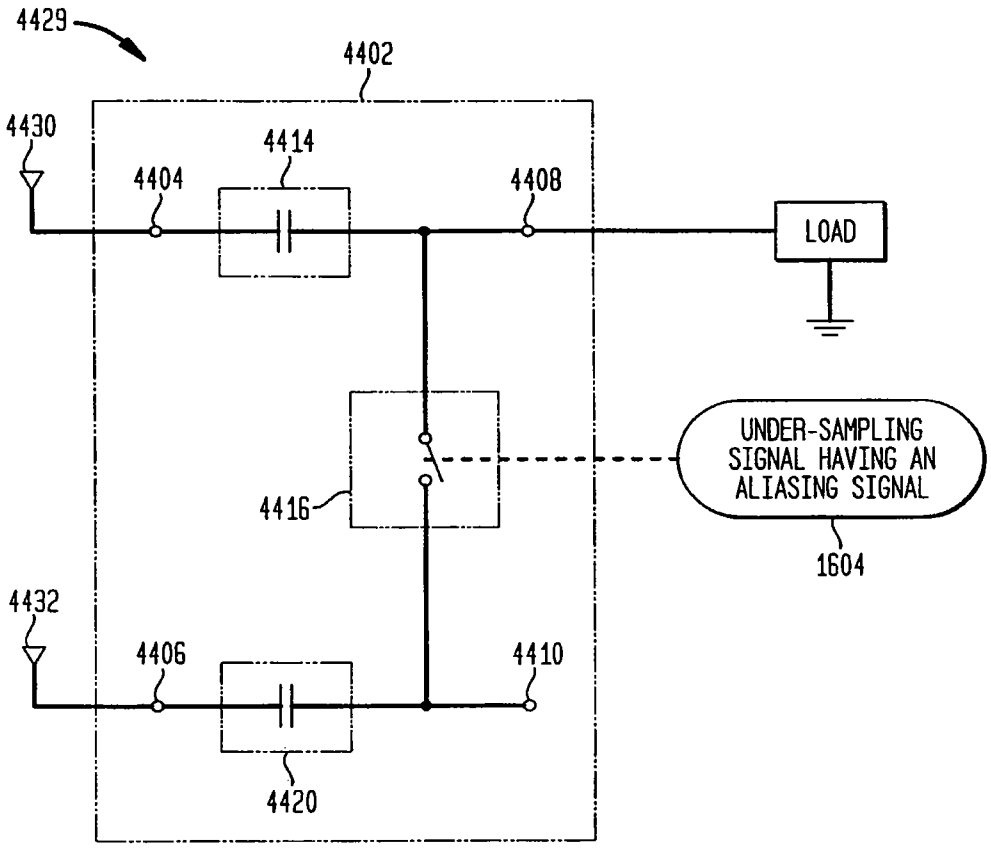


FIG. 44E

EXAMPLE INPUT/OUTPUT CIRCUITRY

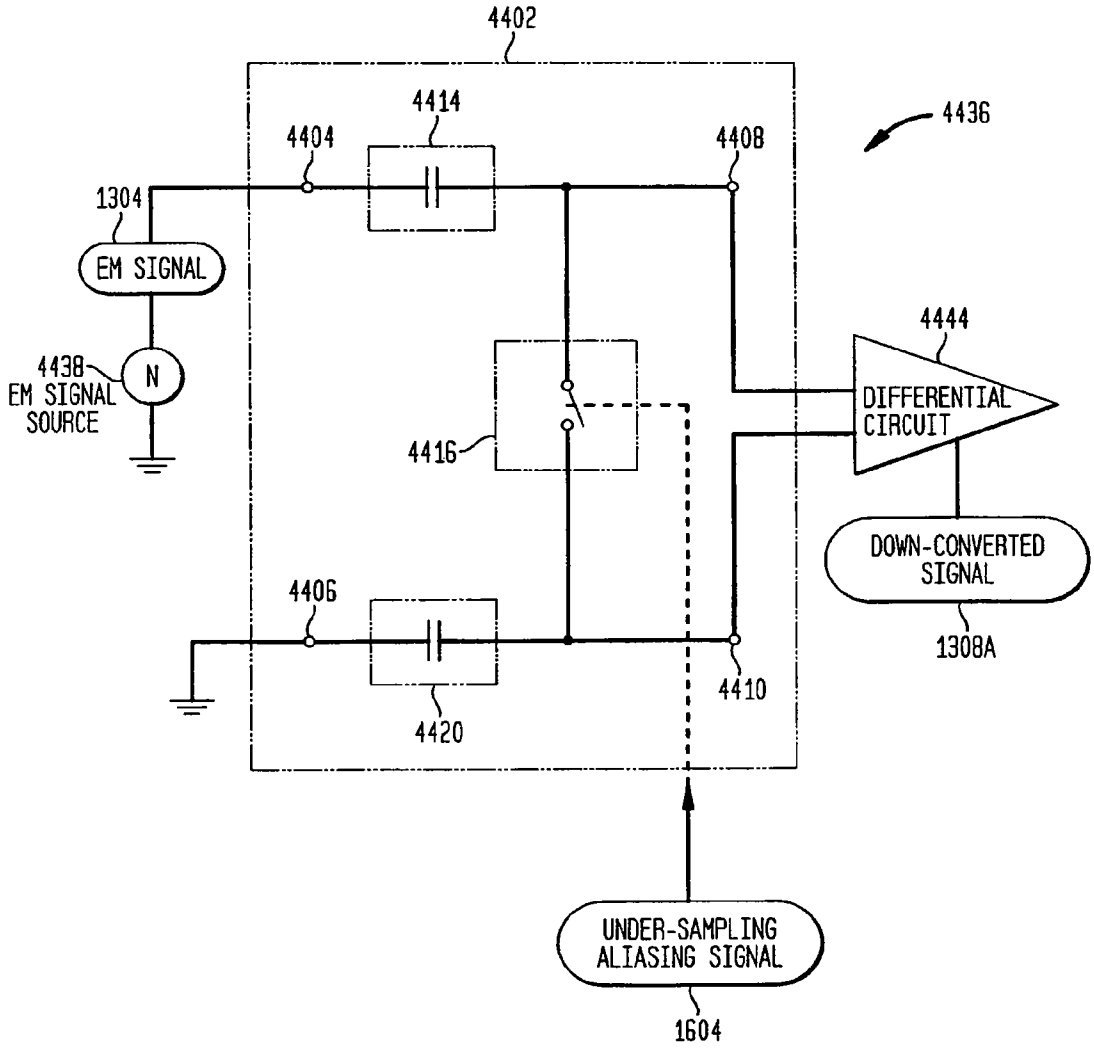


FIG. 45A

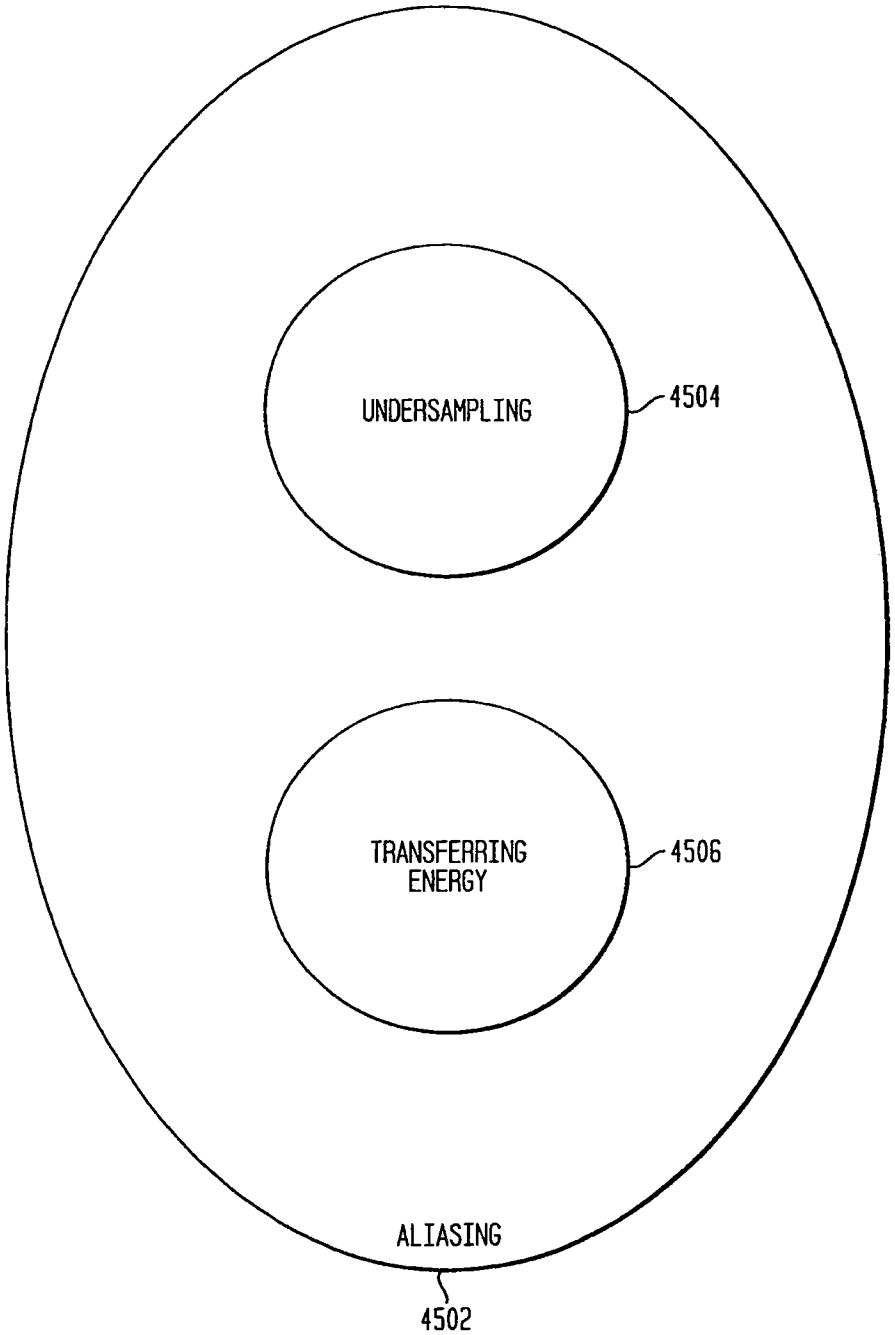

UNDERSAMPLING
4504
TRANSFERRING ENERGY
4506
ALIASING
4502

FIG. 45B

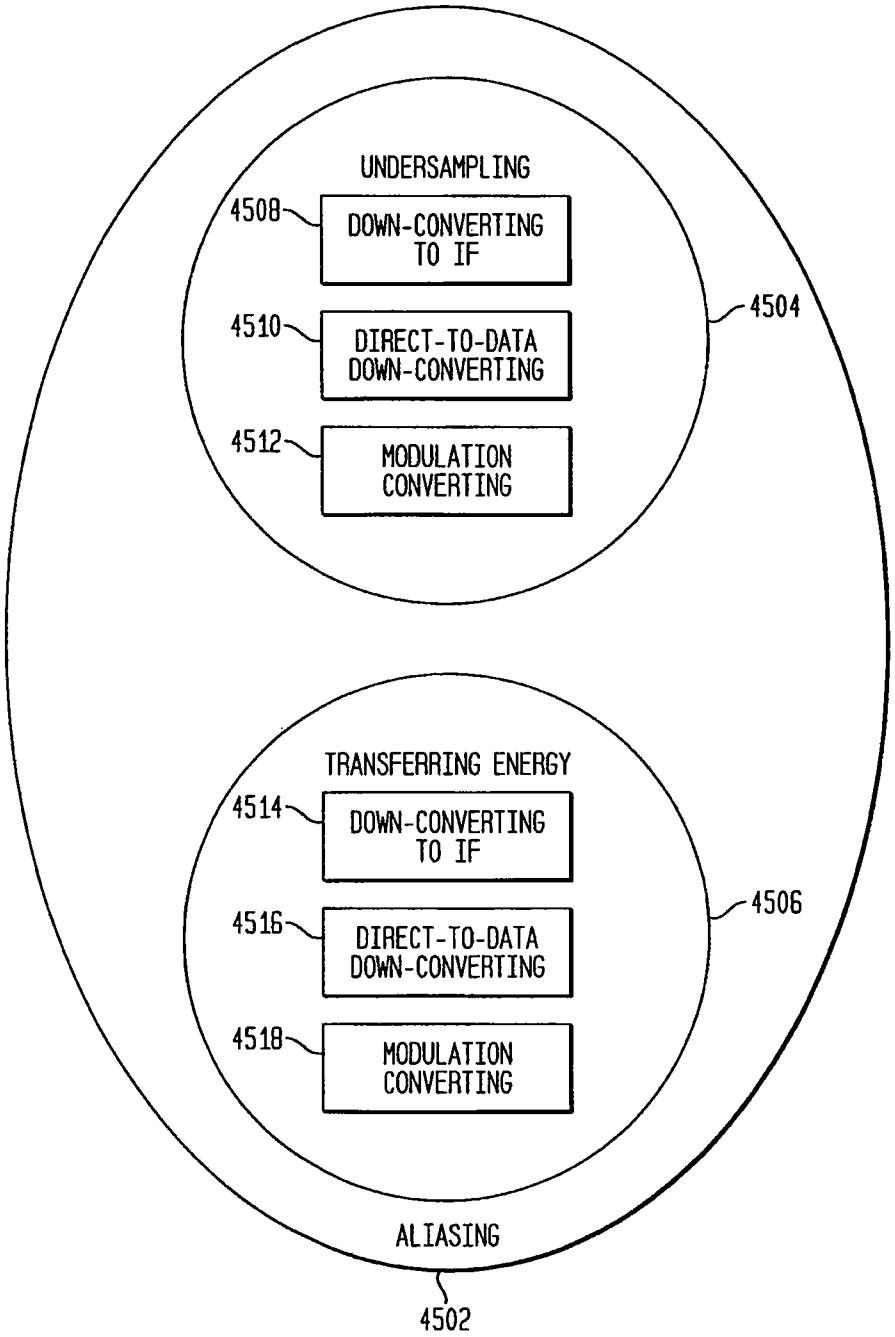

UNDERSAMPLING
4508
DOWN-CONVERTING TO IF
4510
DIRECT-TO-DATA DOWN-CONVERTING
4512
MODULATION CONVERTING
4504
TRANSFERRING ENERGY
4514
DOWN-CONVERTING TO IF
4516
DIRECT-TO-DATA DOWN-CONVERTING
4518
MODULATION CONVERTING
4506
ALIASING
4502

FIG. 46A

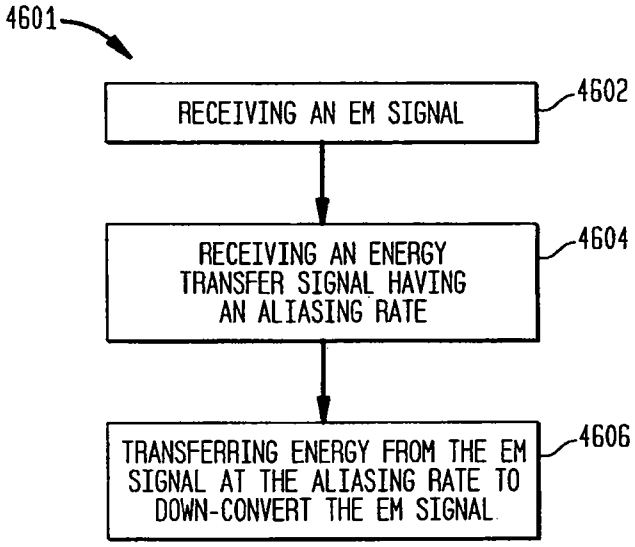


FIG. 46B

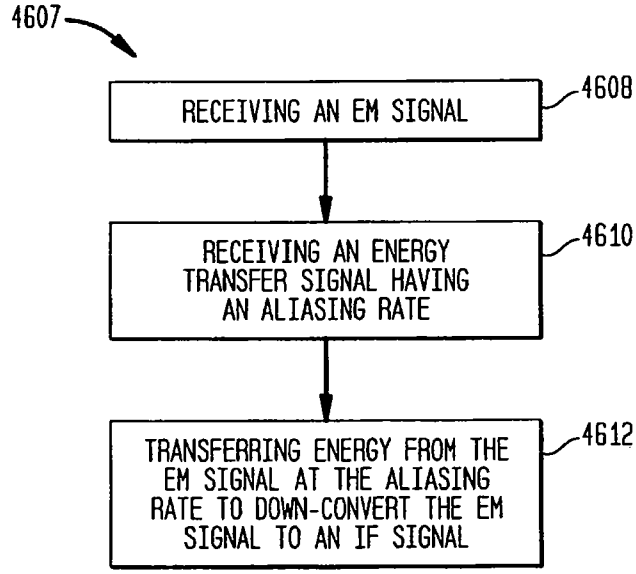


FIG. 46C

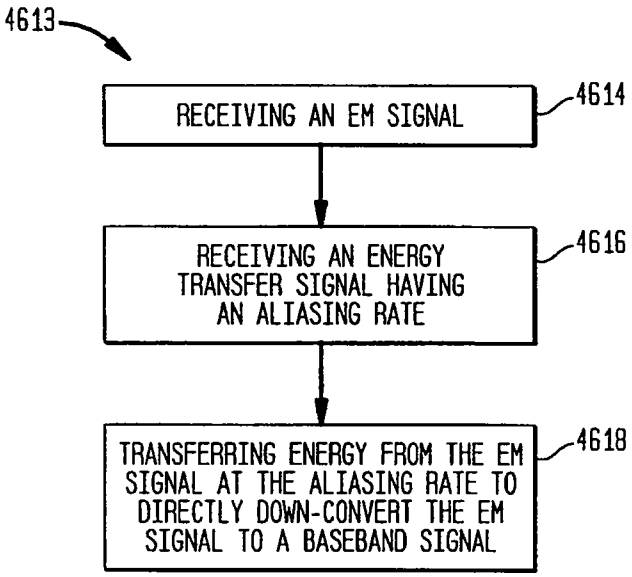


FIG. 46D

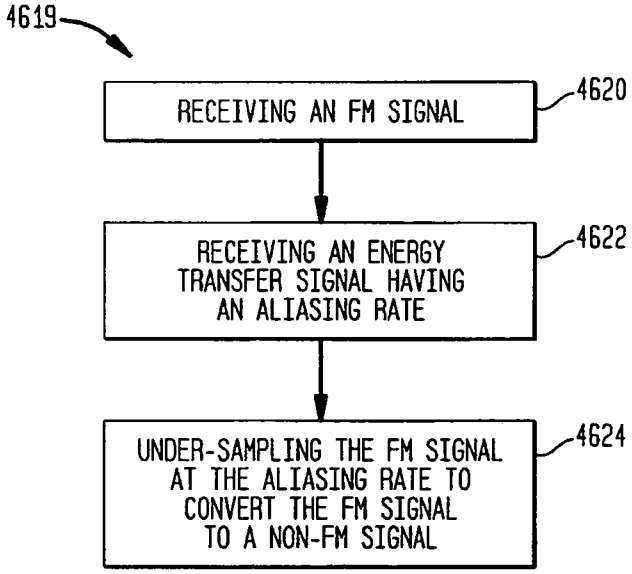


FIG. 47E

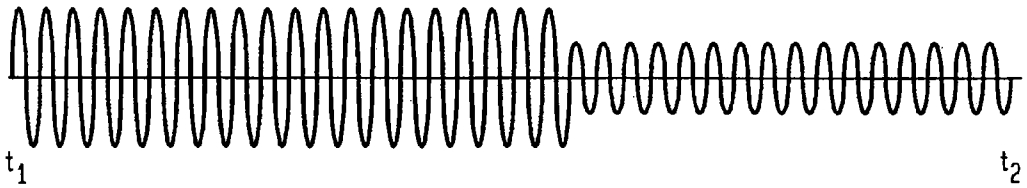


FIG. 47A

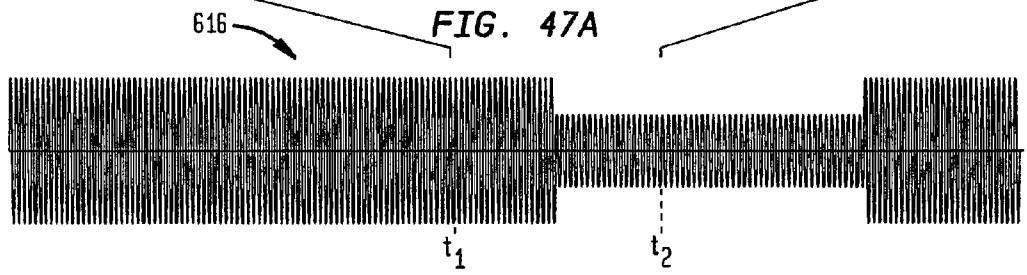


FIG. 47B

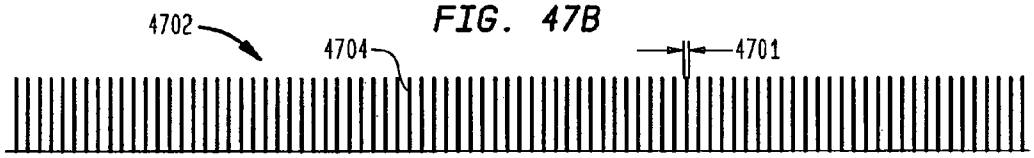


FIG. 47C

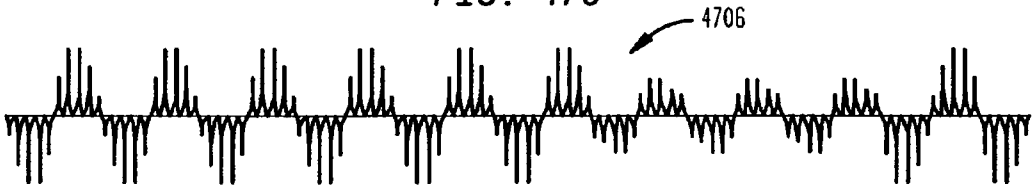


FIG. 47D

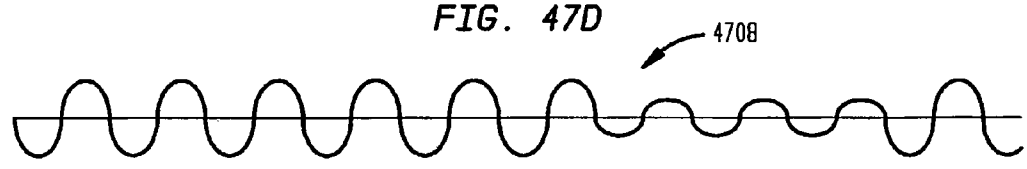
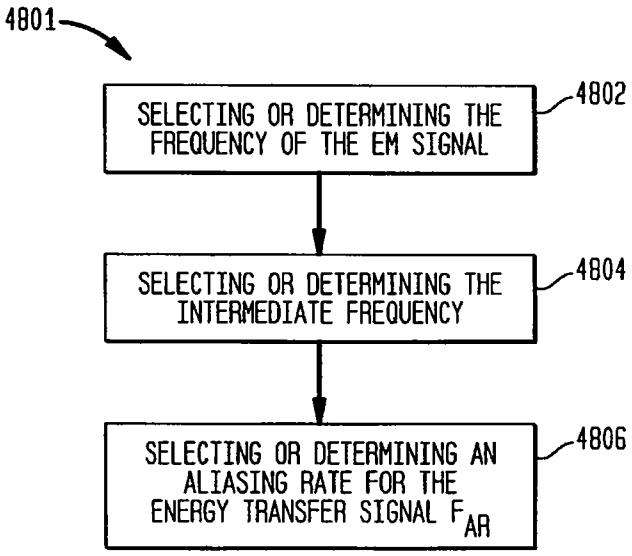
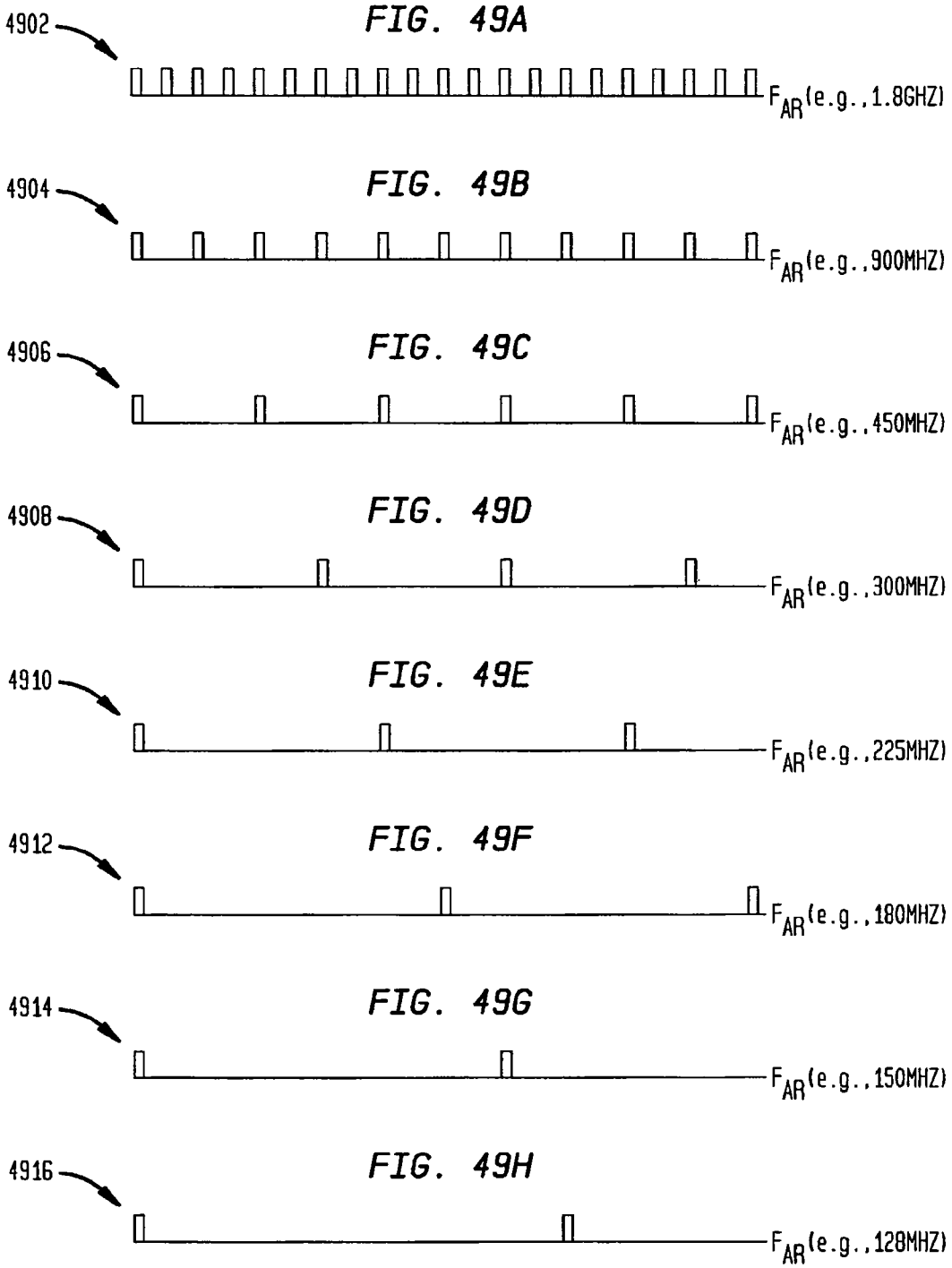
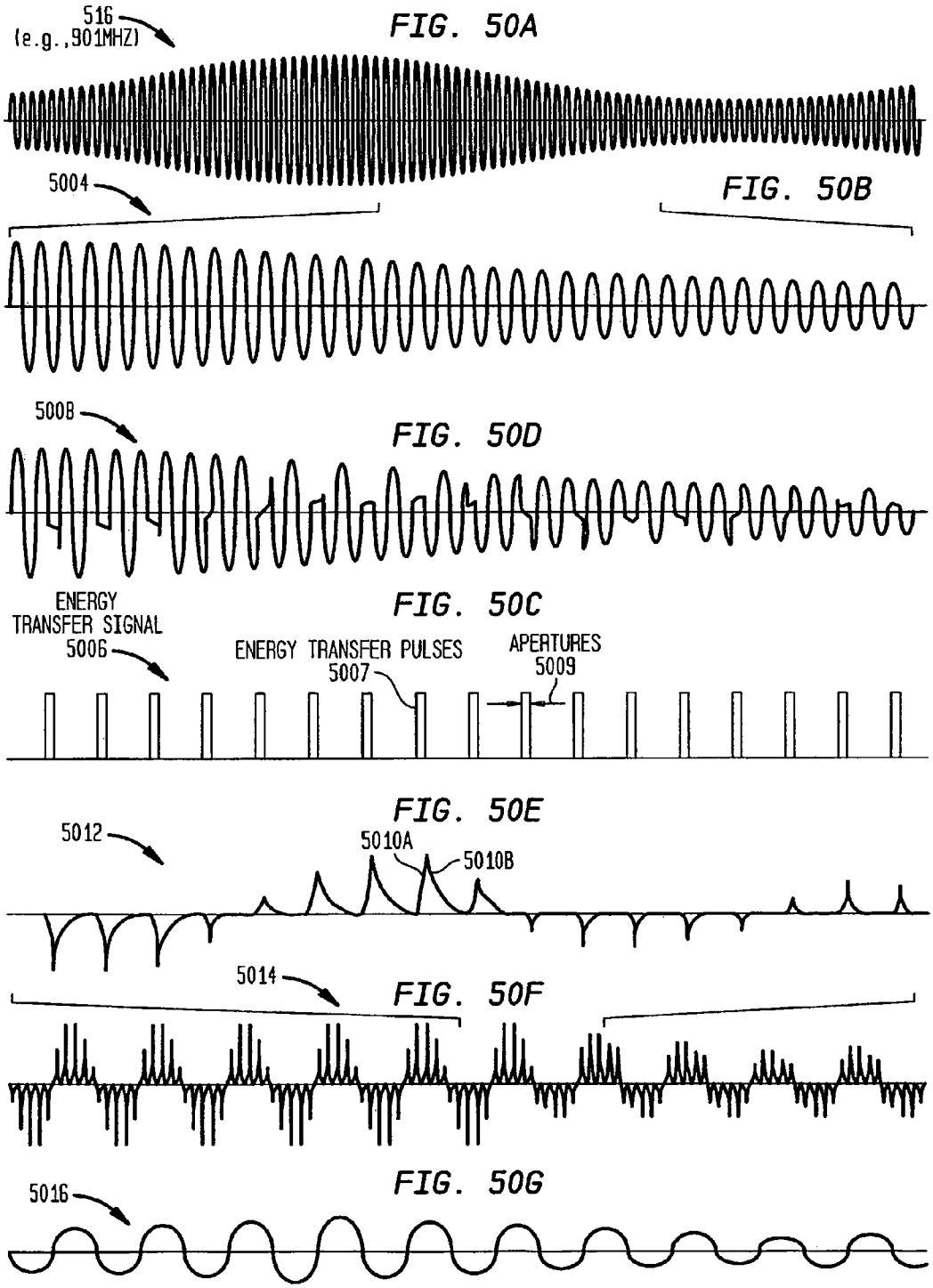


FIG. 48


4801
SELECTING OR DETERMINING THE FREQUENCY OF THE EM SIGNAL
4802
SELECTING OR DETERMINING THE INTERMEDIATE FREQUENCY
4804
SELECTING OR DETERMINING AN ALIASING RATE FOR THE ENERGY TRANSFER SIGNAL F_{AR}
4806


4902
FIG. 49A
F_{AR}(e.g.,1.8GHZ)
4904
FIG. 49B
F_{AR}(e.g.,900MHZ)
4906
FIG. 49C
F_{AR}(e.g.,450MHZ)
4908
FIG. 49D
F_{AR}(e.g.,300MHZ)
4910
FIG. 49E
F_{AR}(e.g.,225MHZ)
4912
FIG. 49F
F_{AR}(e.g.,180MHZ)
4914
FIG. 49G
F_{AR}(e.g.,150MHZ)
4916
FIG. 49H
F_{AR}(e.g.,128MHZ)


516
(e.g.,901MHZ)
FIG. 50A
5004
FIG. 50B
5008
FIG. 50D
ENERGY
TRANSFER SIGNAL
5006
ENERGY TRANSFER PULSES
5007
APERTURES
5009
FIG. 50C
5012
5010A
5010B
FIG. 50E
5014
FIG. 50F
5016
FIG. 50G

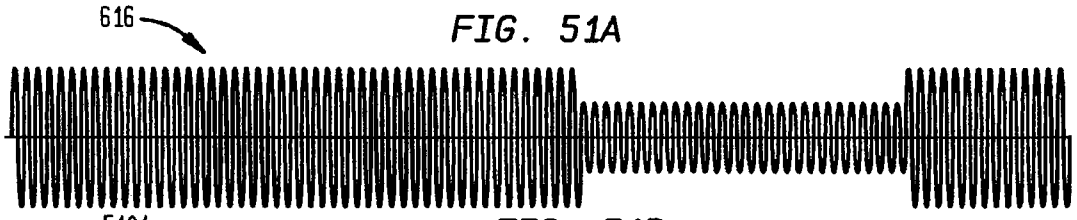


FIG. 51A

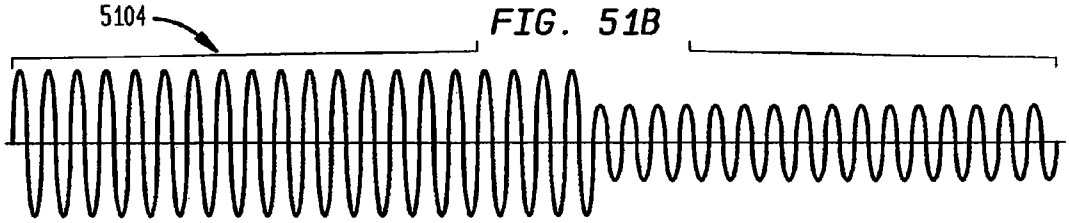


FIG. 51B

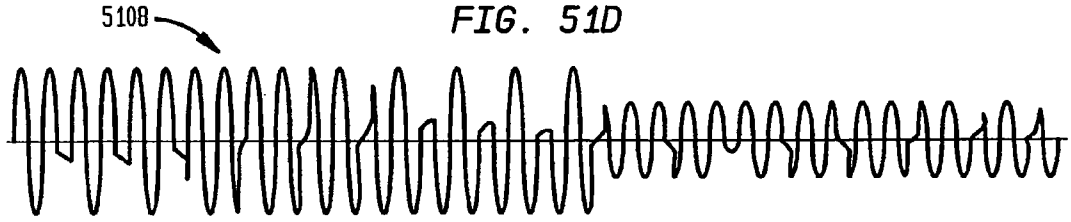


FIG. 51D

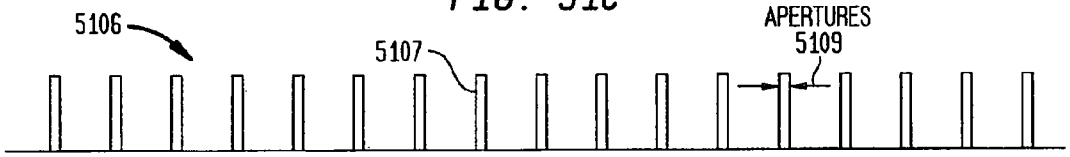


FIG. 51C

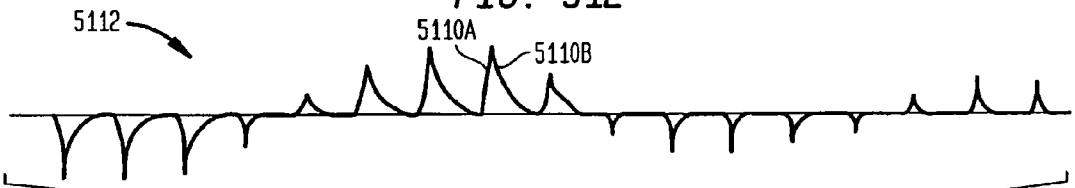


FIG. 51E

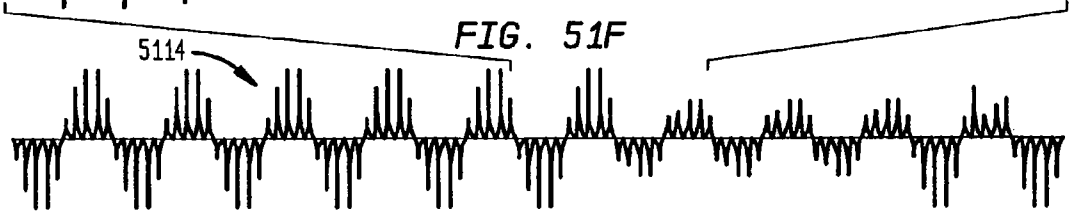


FIG. 51F

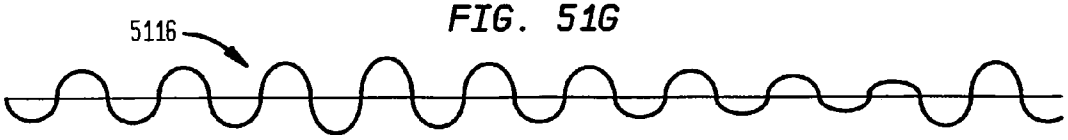
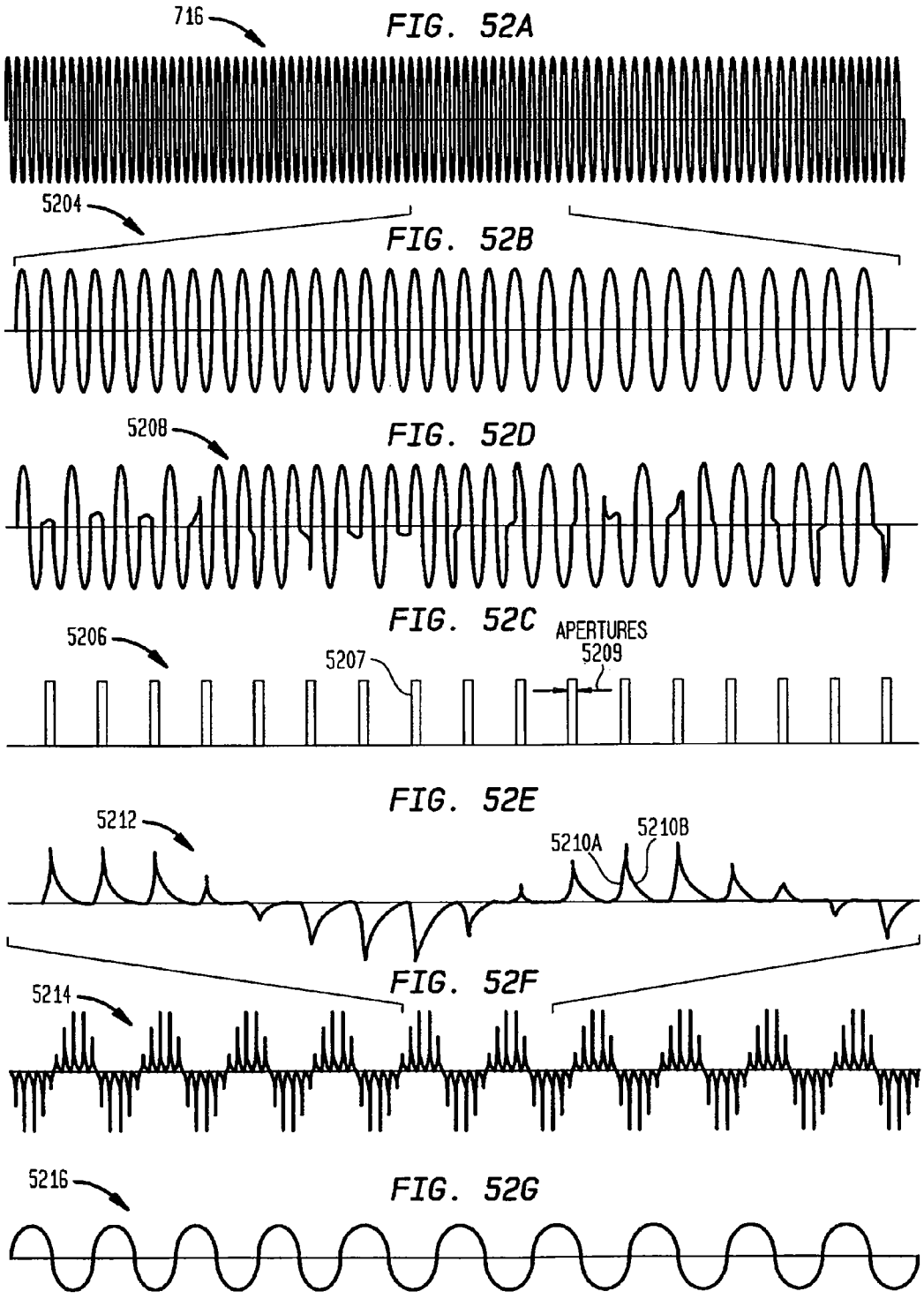
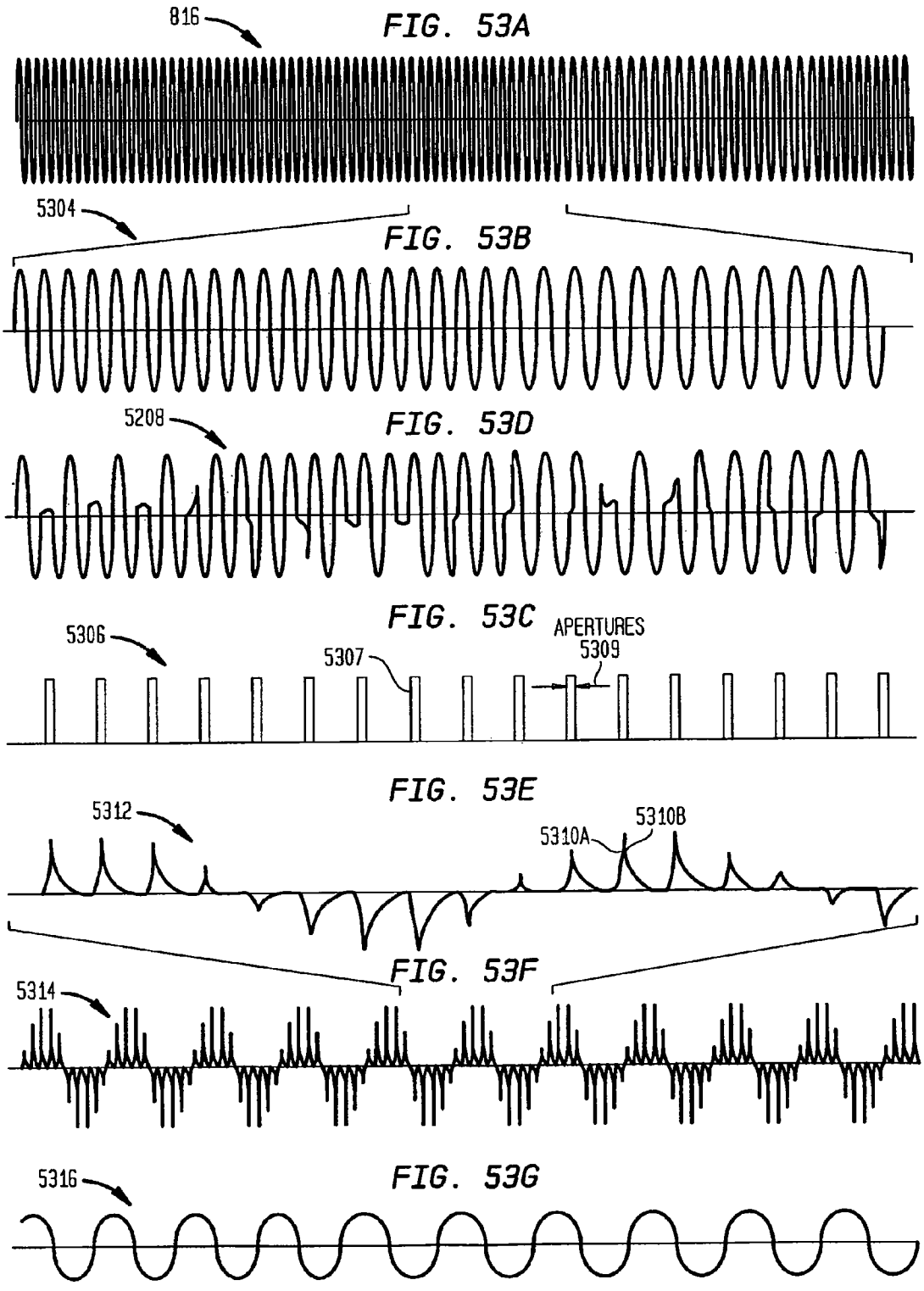


FIG. 51G


716
FIG. 52A
5204
FIG. 52B
5208
FIG. 52D
5206
5207
APERTURES
5209
FIG. 52C
5212
5210A
5210B
FIG. 52E
5214
FIG. 52F
5216
FIG. 52G


816
FIG. 53A
5304
FIG. 53B
5208
FIG. 53D
FIG. 53C
5306
5307
APERTURES
5309
FIG. 53E
5312
5310A
5310B
FIG. 53F
5314
5316
FIG. 53G

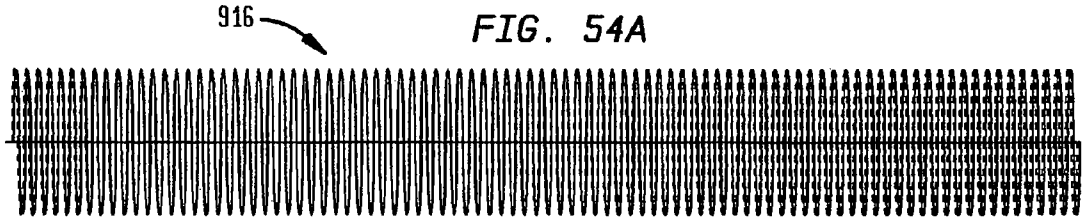


FIG. 54A

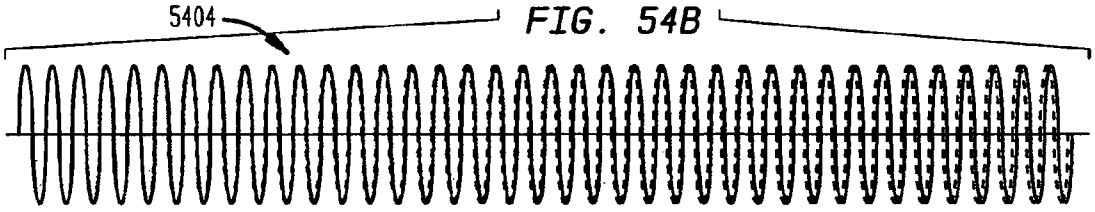


FIG. 54B

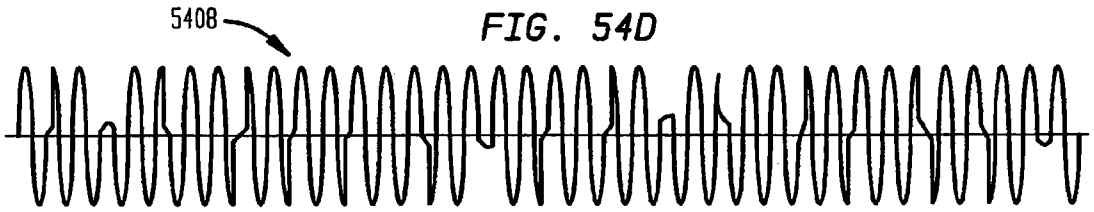


FIG. 54D

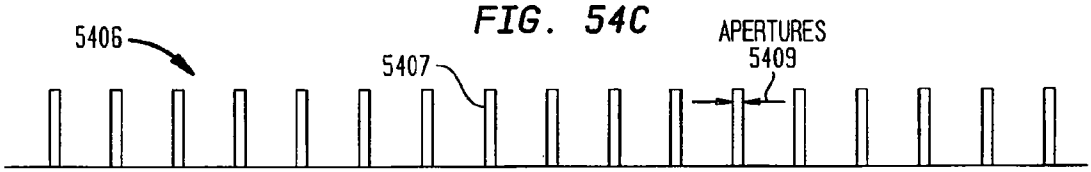


FIG. 54C

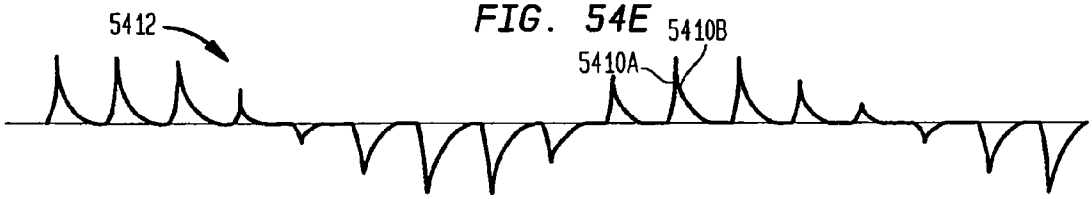


FIG. 54E

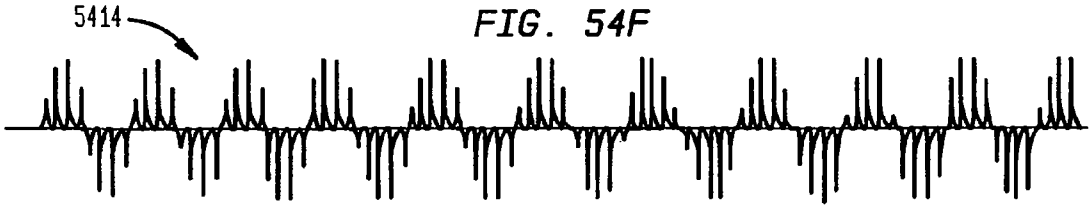


FIG. 54F

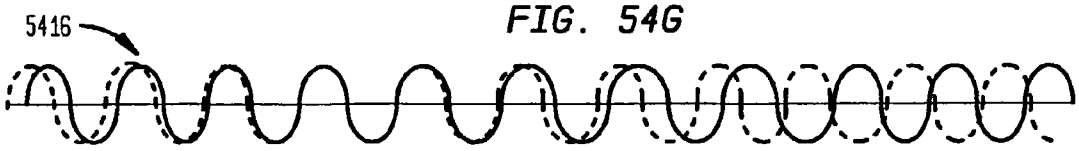


FIG. 54G

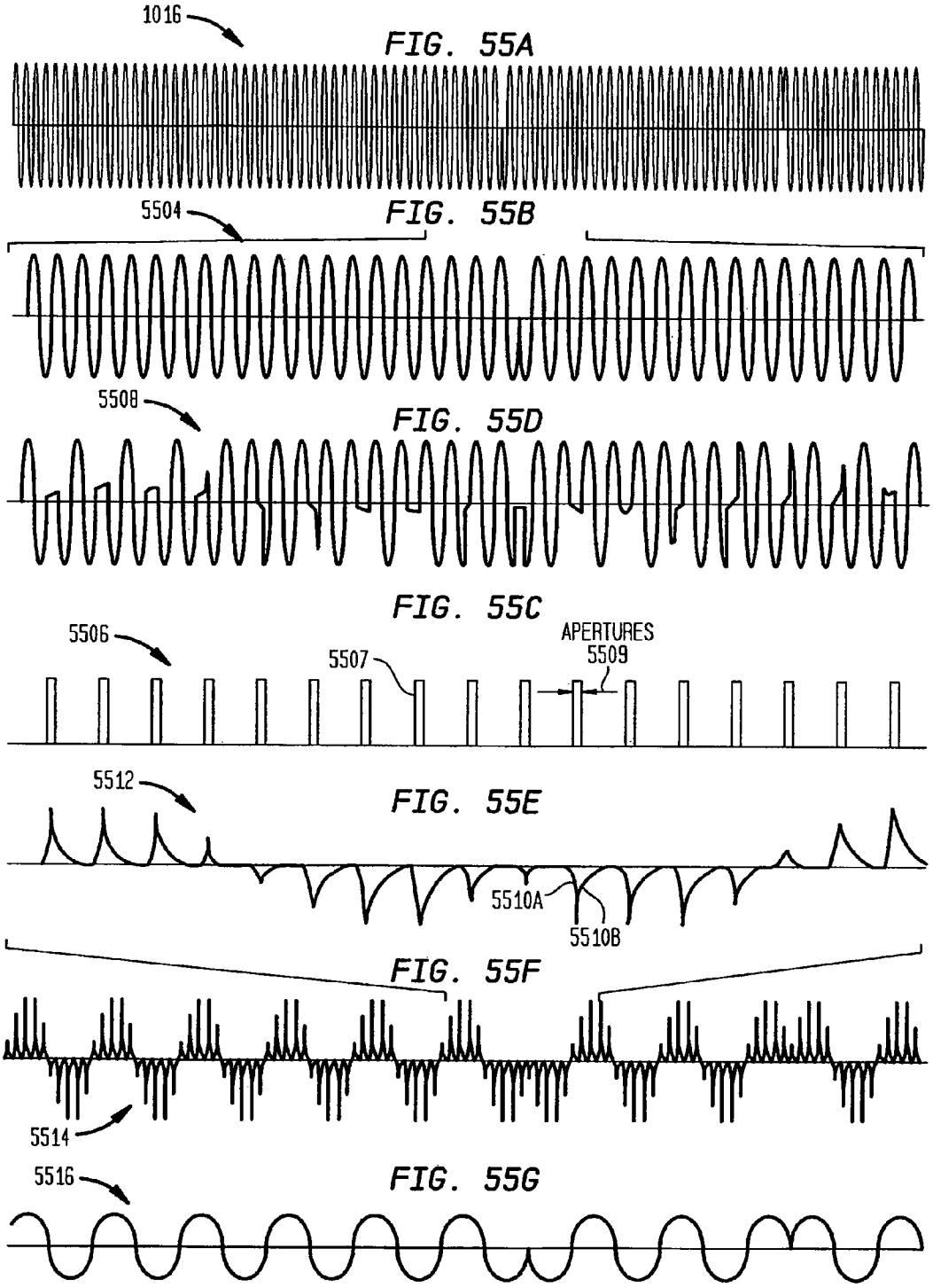

1016
FIG. 55A
5504
FIG. 55B
5508
FIG. 55D
FIG. 55C
5506
5507
APERTURES
5509
5512
FIG. 55E
5510A
5510B
FIG. 55F
5514
5516
FIG. 55G

FIG. 56A

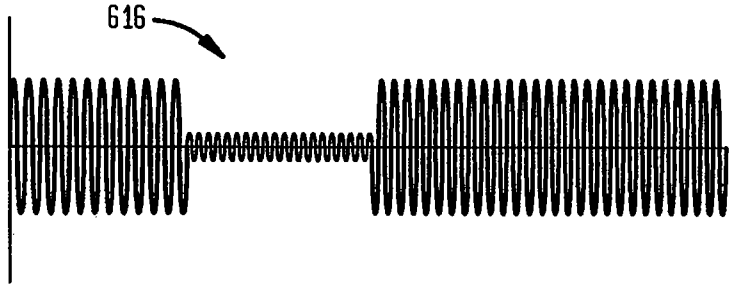


FIG. 56B

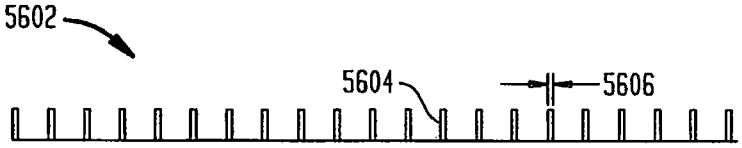


FIG. 56C

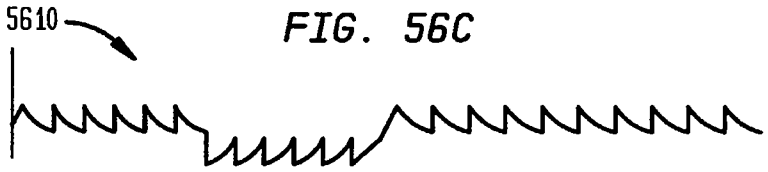


FIG. 56D

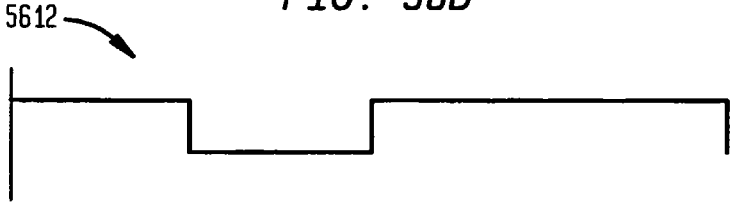


FIG. 57A

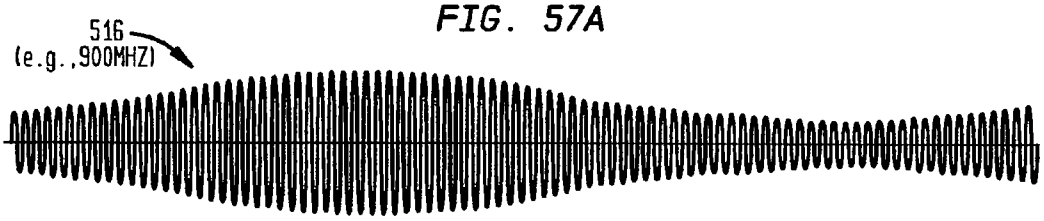


FIG. 57B

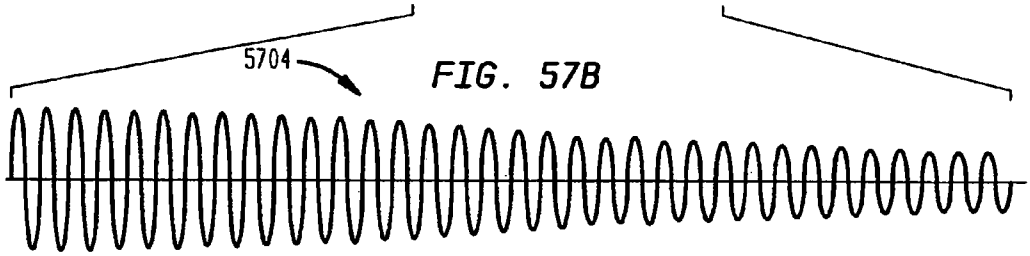


FIG. 57D

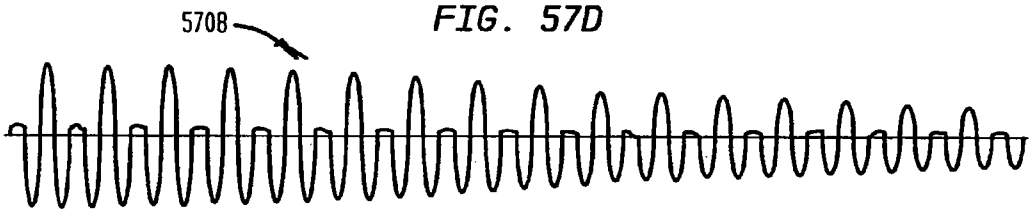


FIG. 57C

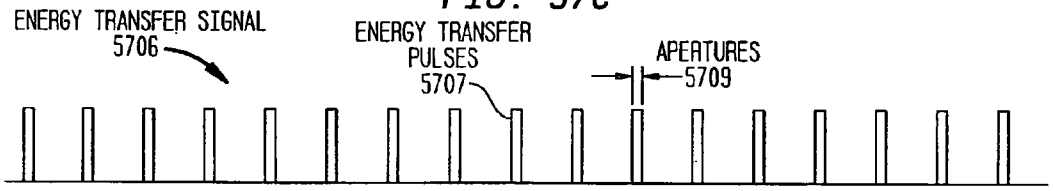


FIG. 57E

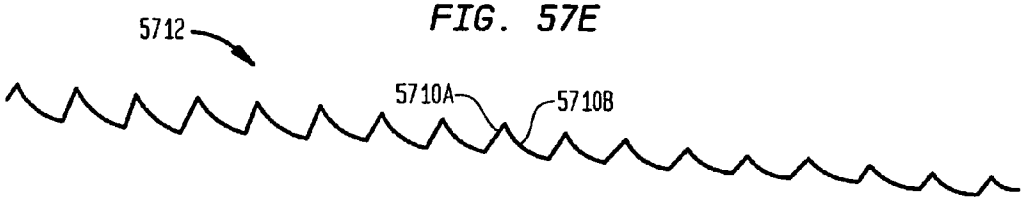


FIG. 57F

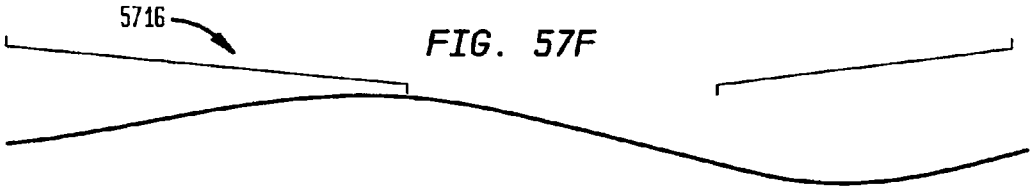


FIG. 58A

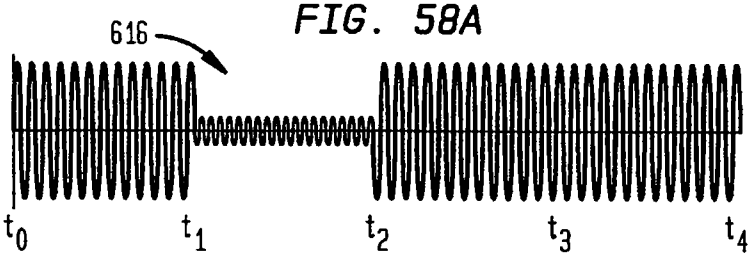


FIG. 58B

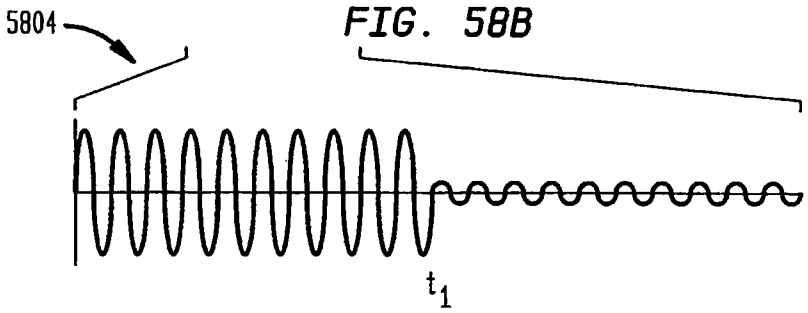


FIG. 58D

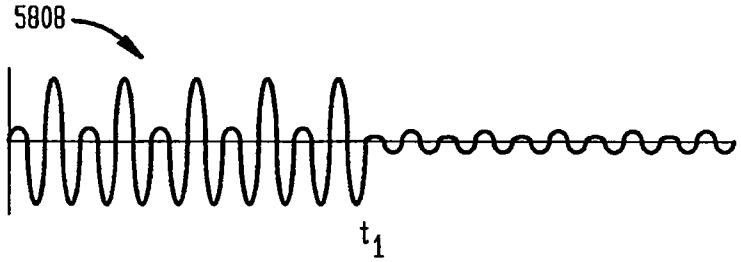


FIG. 58C

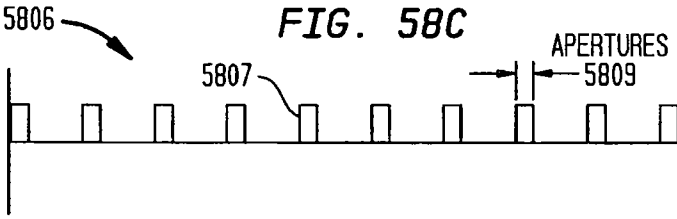


FIG. 58E

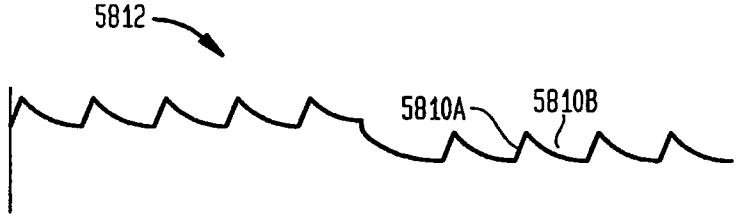


FIG. 58F

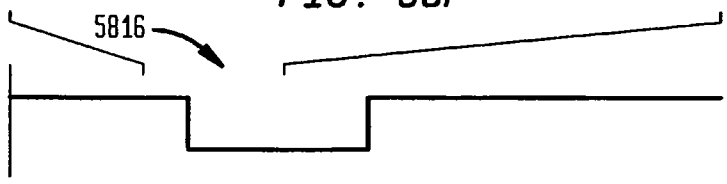


FIG. 59A

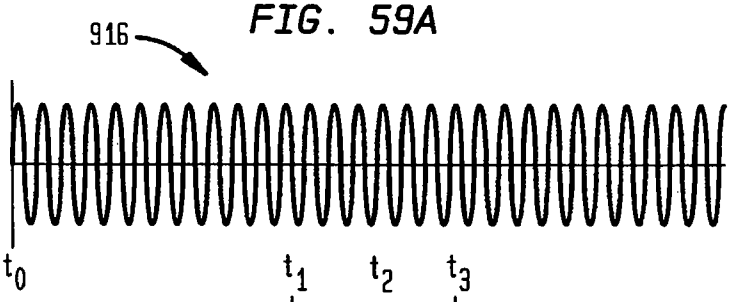


FIG. 59B

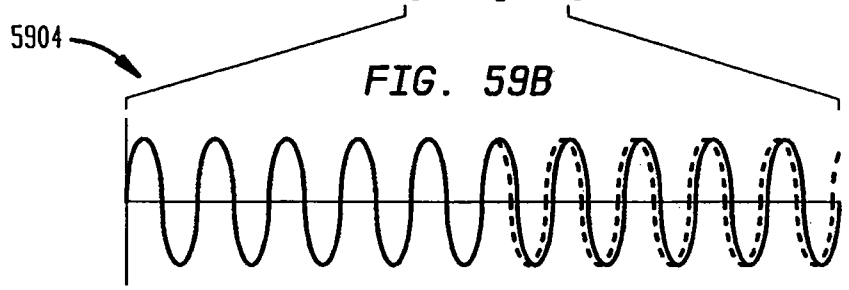


FIG. 59D

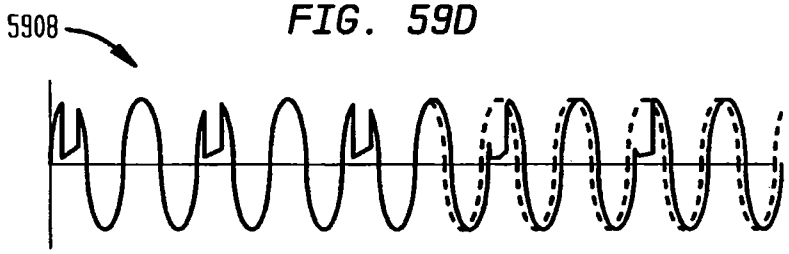


FIG. 59C

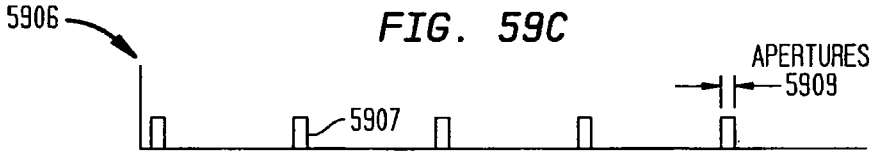
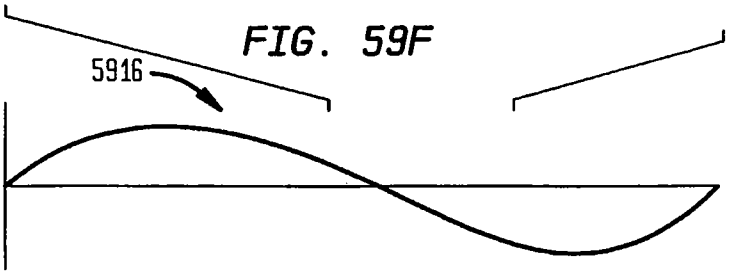


FIG. 59E



FIG. 59F



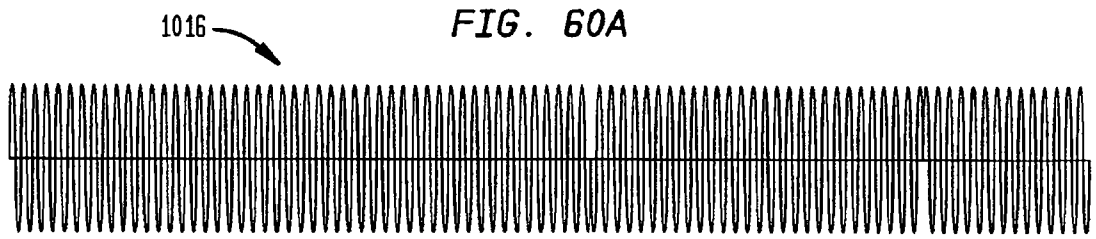


FIG. 60A

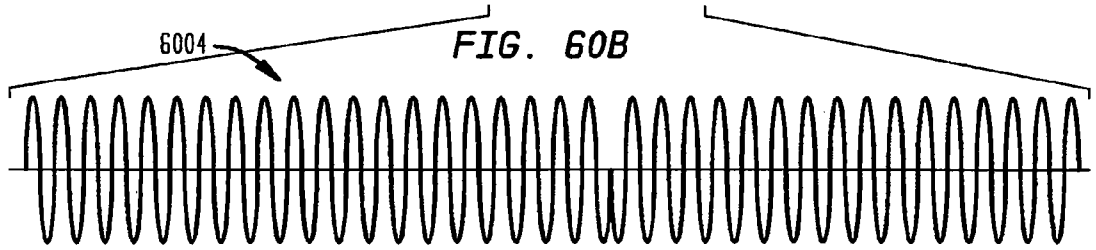


FIG. 60B

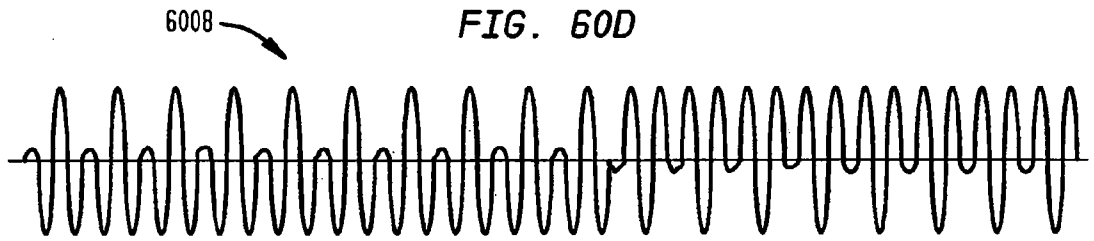


FIG. 60D

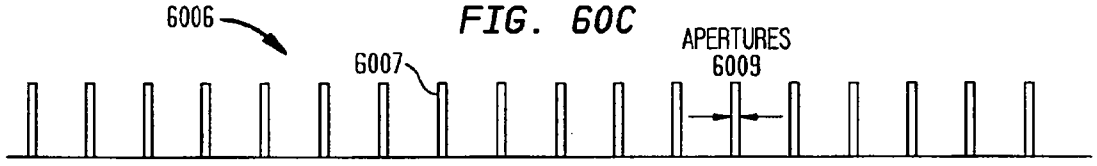


FIG. 60C



FIG. 60E

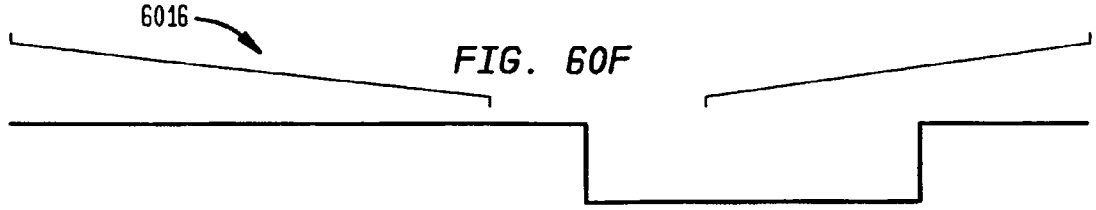
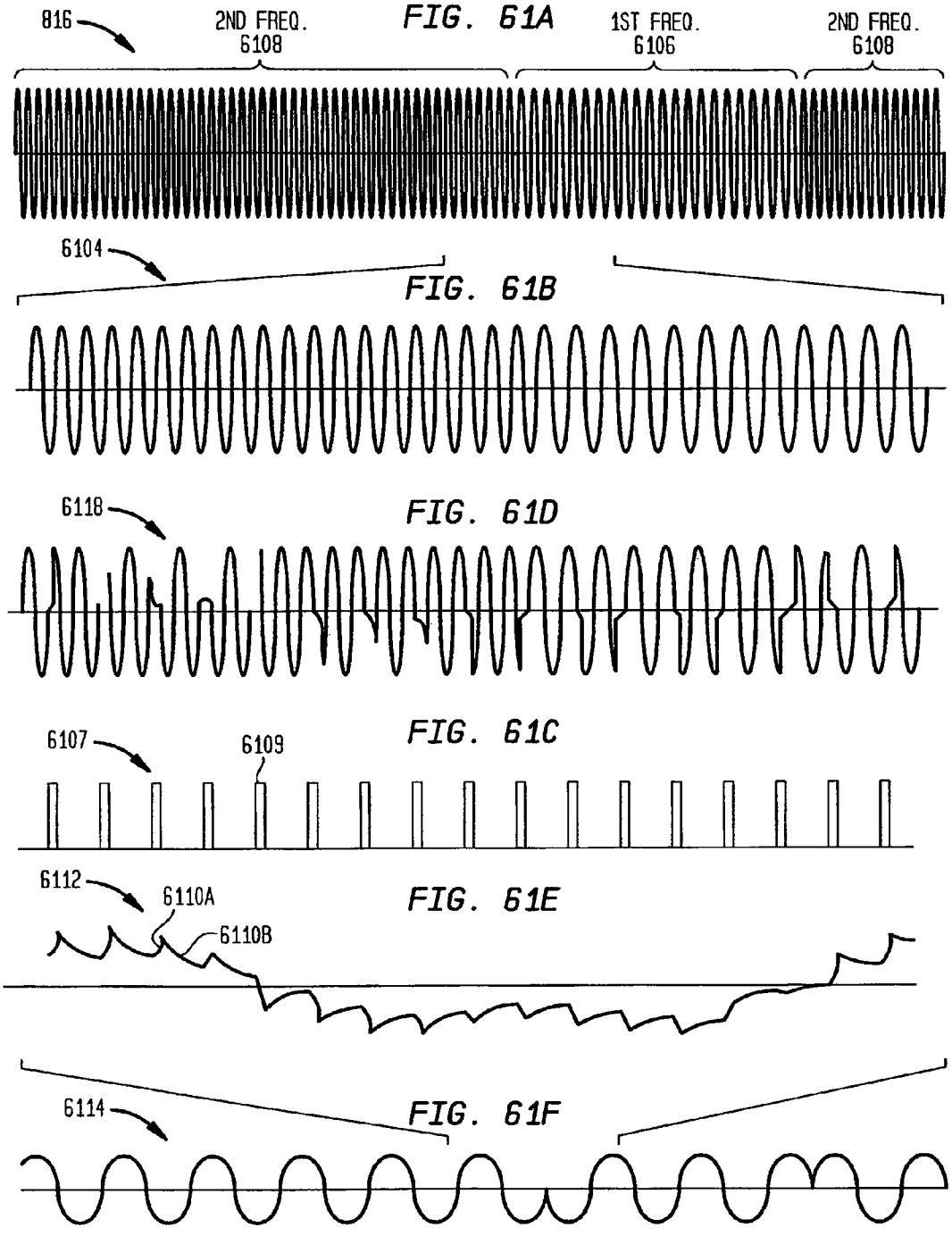


FIG. 60F


816
2ND FREQ.
6108
1ST FREQ.
6106
2ND FREQ.
6108
FIG. 61A
6104
FIG. 61B
6118
FIG. 61D
6107
6109
FIG. 61C
6112
6110A
6110B
FIG. 61E
6114
FIG. 61F

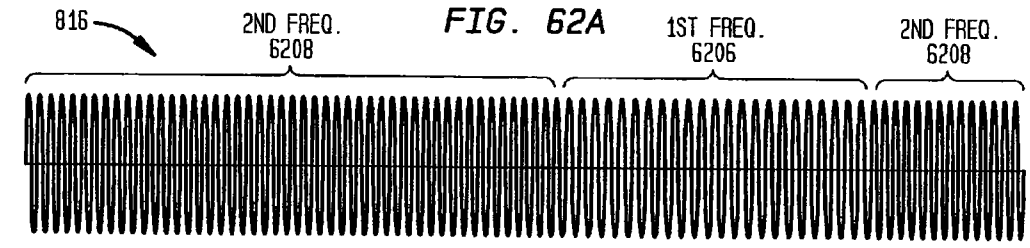


FIG. 62A

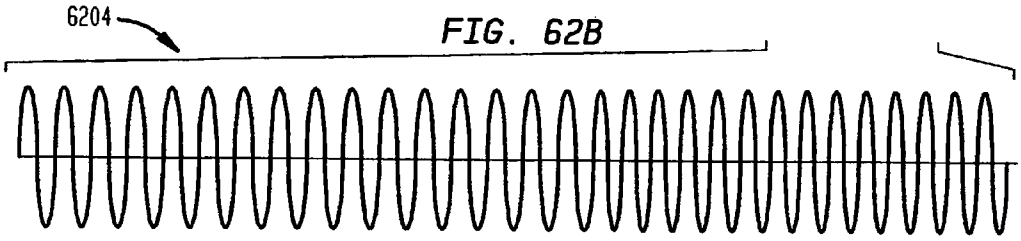


FIG. 62B

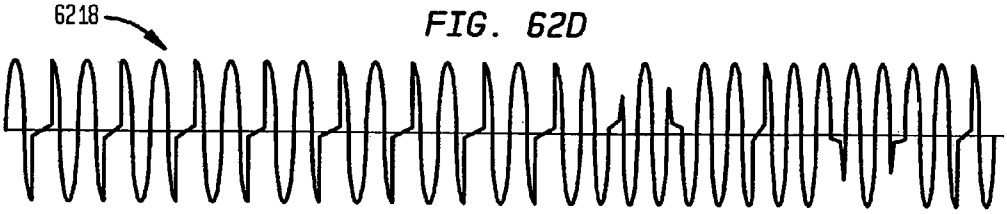


FIG. 62D

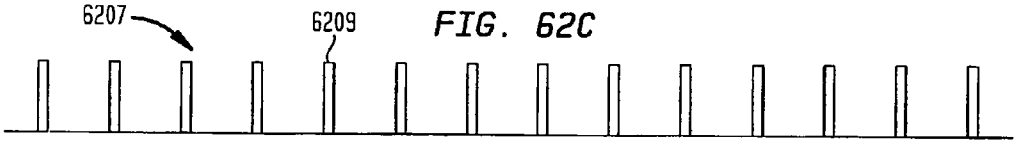


FIG. 62C

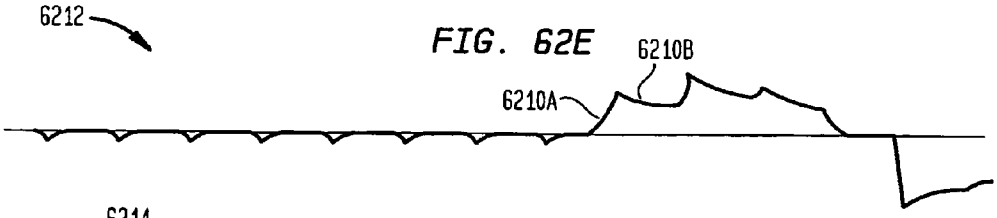


FIG. 62E

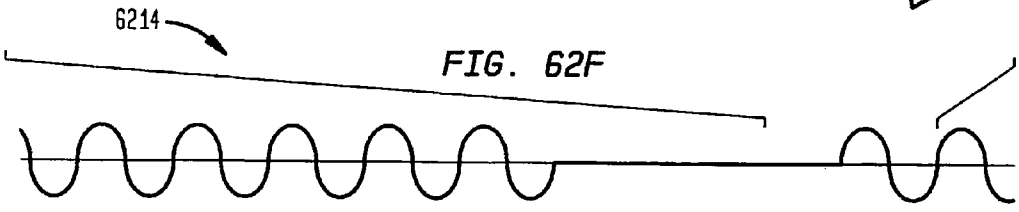


FIG. 62F

FIG. 63

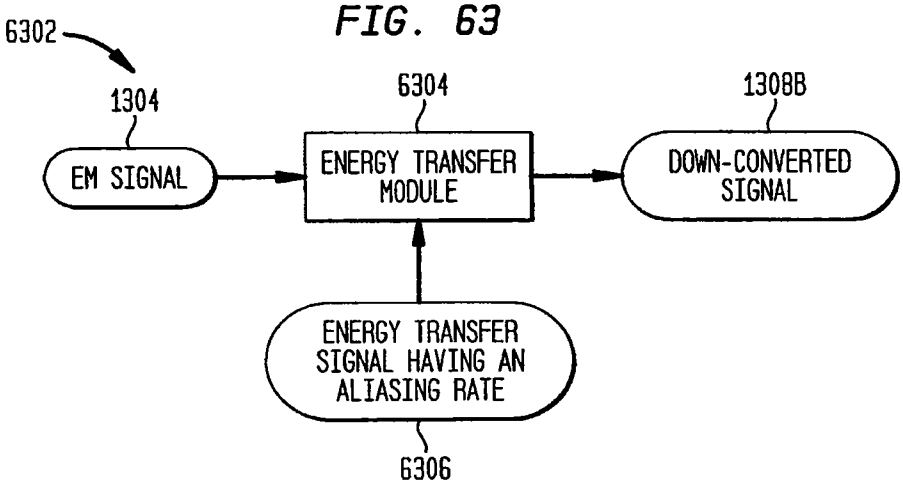


FIG. 64A

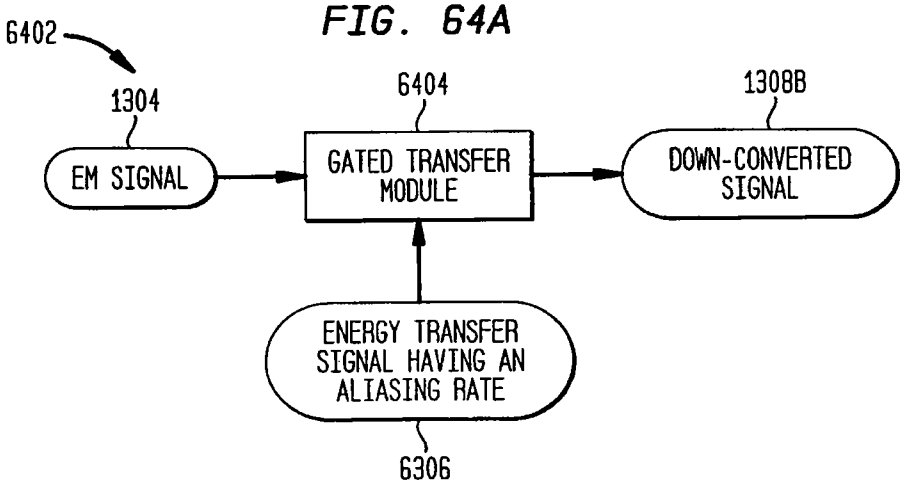


FIG. 64B

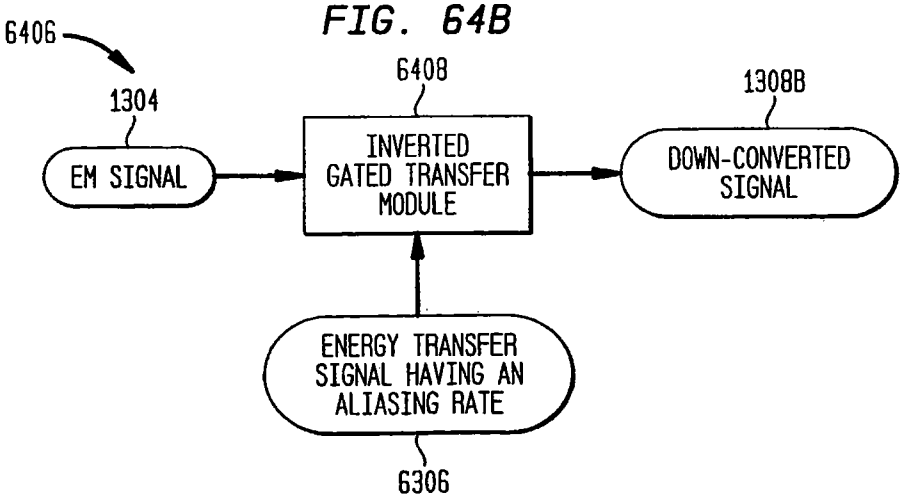


FIG. 65

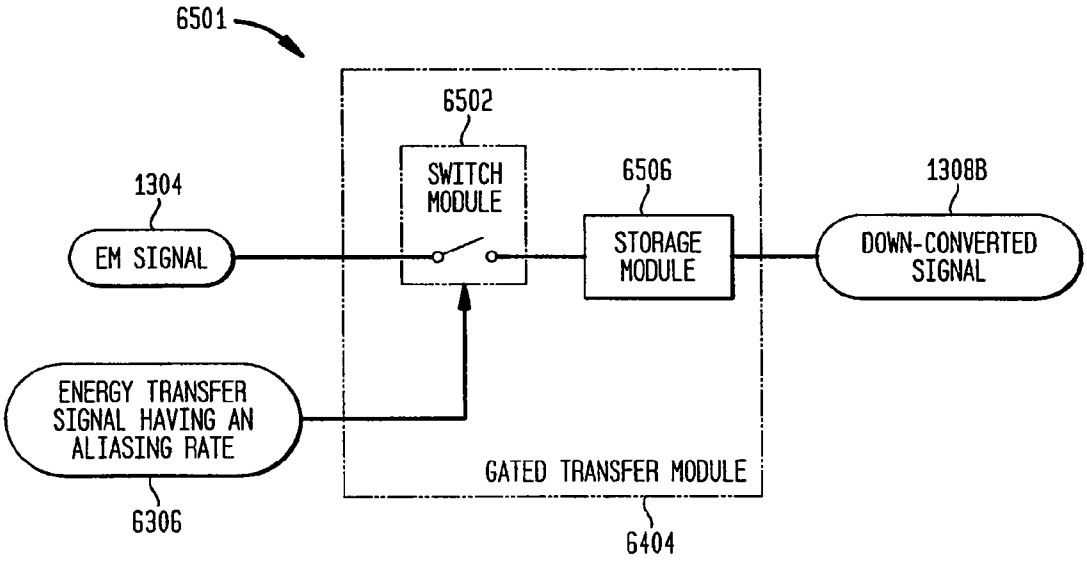


FIG. 66A

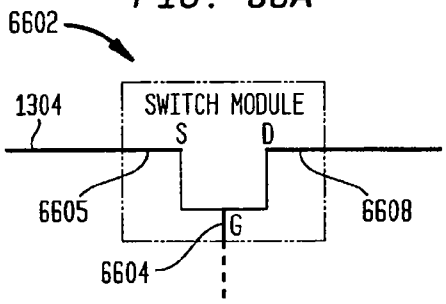


FIG. 66B

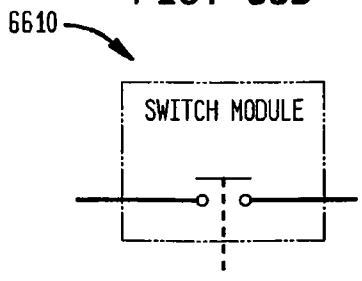


FIG. 66C

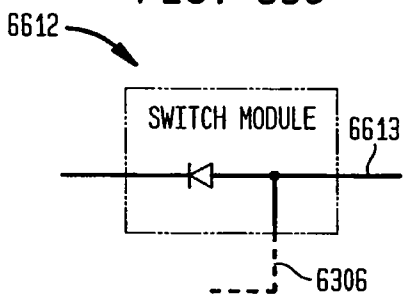


FIG. 66D

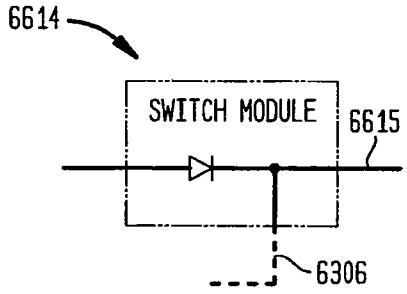


FIG. 67A

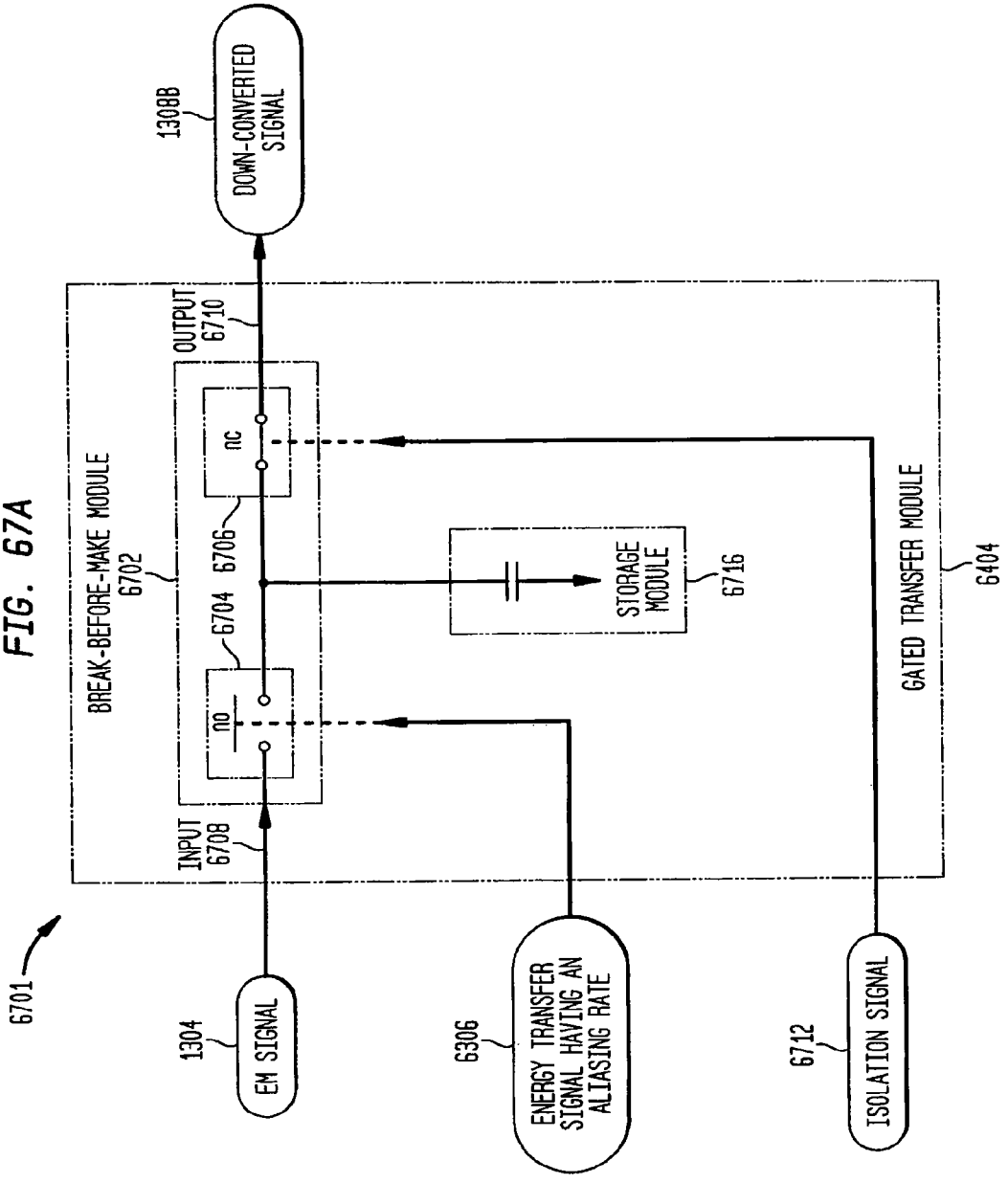

6701
1304
EM SIGNAL
6306
ENERGY TRANSFER SIGNAL HAVING AN ALIASING RATE
6712
ISOLATION SIGNAL
BREAK-BEFORE-MAKE MODULE
6702
INPUT
6708
OUTPUT
6710
no
nc
6704
6706
STORAGE MODULE
6716
GATED TRANSFER MODULE
6404
1308B
DOWN-CONVERTED SIGNAL

FIG. 67B

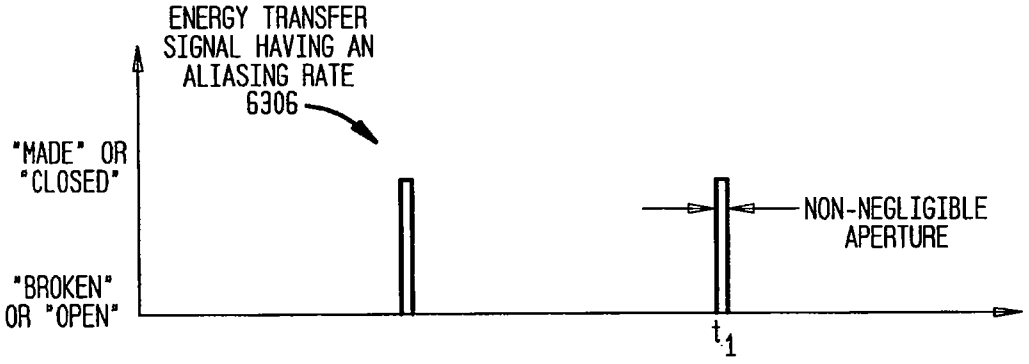


FIG. 67C

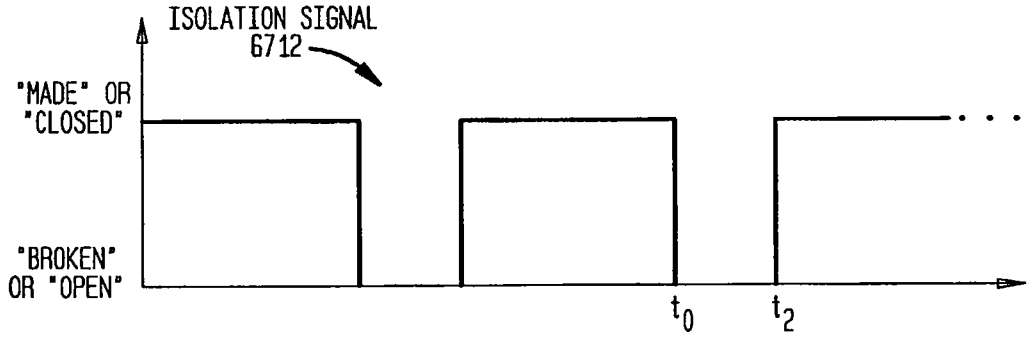


FIG. 68A

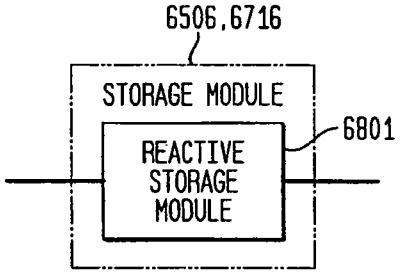


FIG. 68B

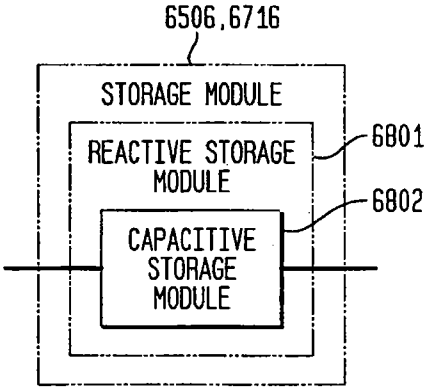


FIG. 68C

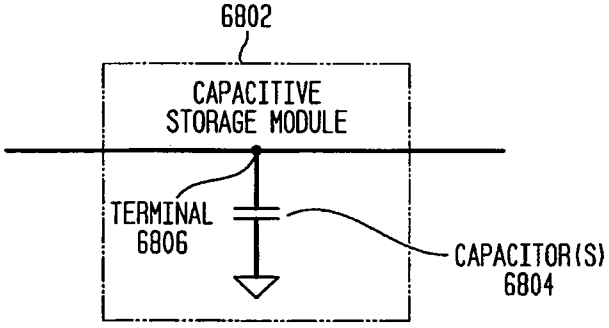


FIG. 68D

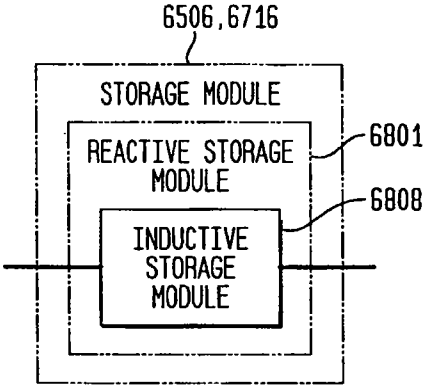


FIG. 68E

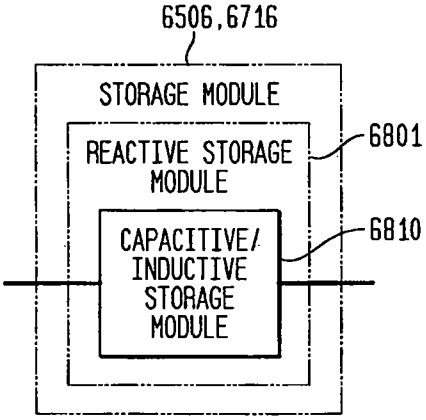


FIG. 68F

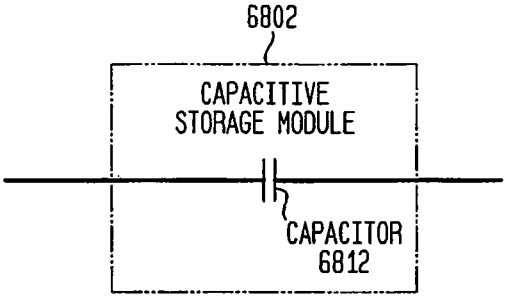


FIG. 68G

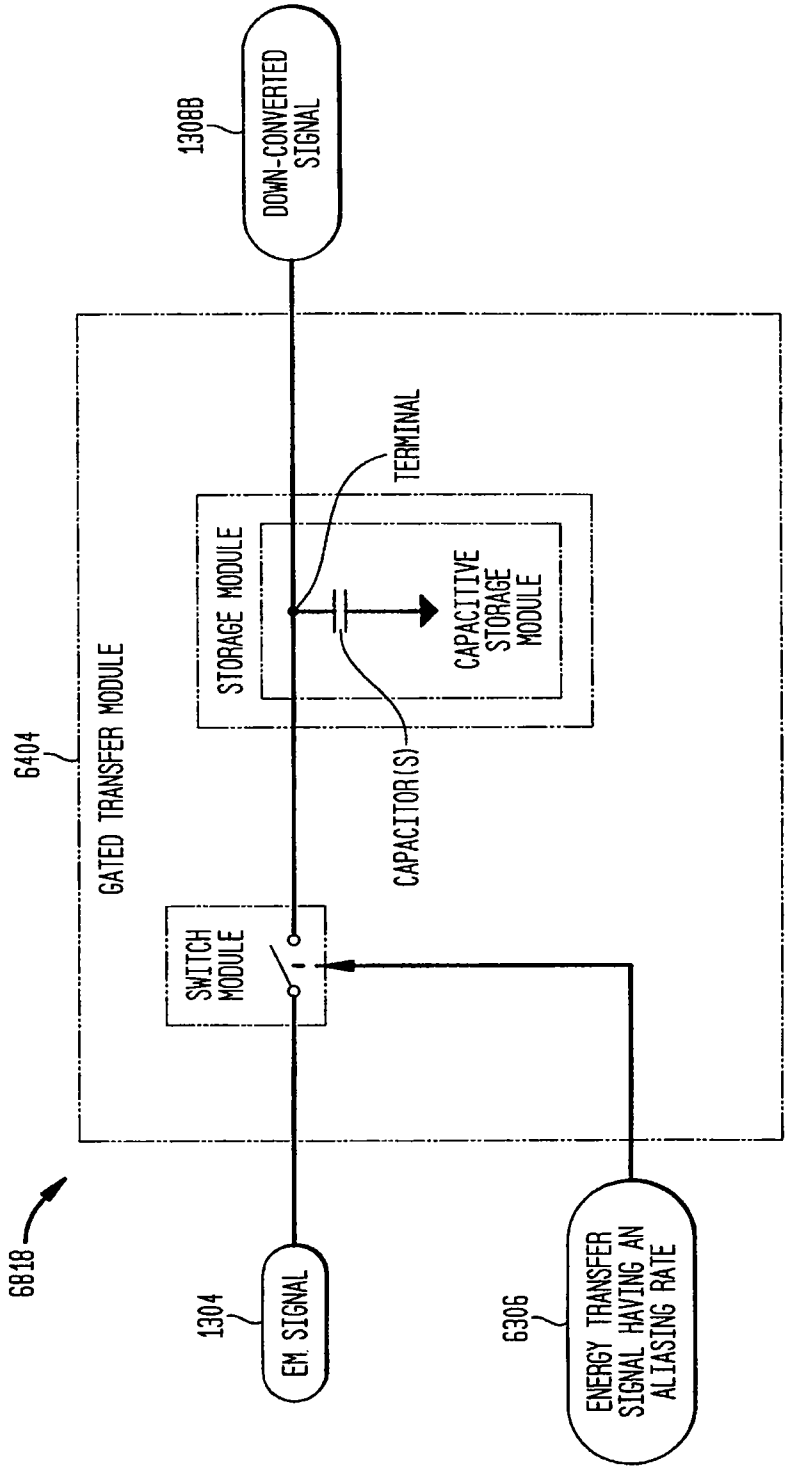
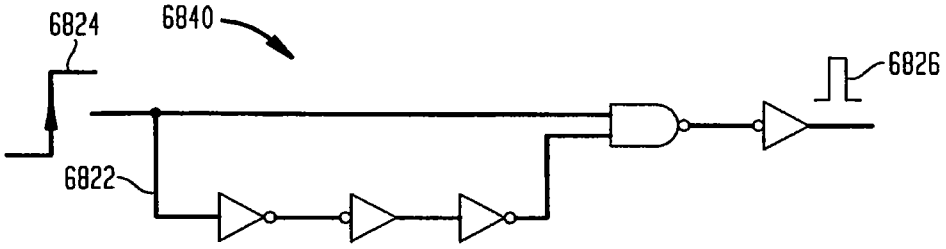
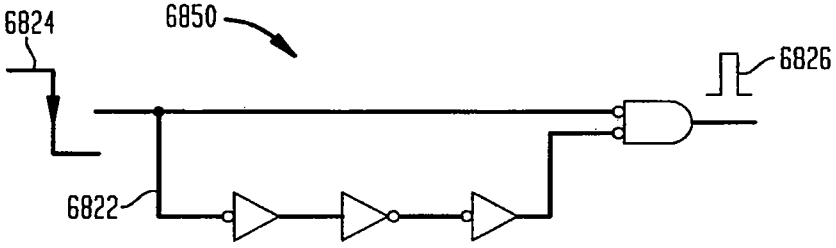

1308B
DOWN-CONVERTED SIGNAL
6404
GATED TRANSFER MODULE
STORAGE MODULE
TERMINAL
CAPACITIVE STORAGE MODULE
CAPACITOR(S)
SWITCH MODULE
6818
1304
EM SIGNAL
6306
ENERGY TRANSFER SIGNAL HAVING AN ALIASING RATE

FIG. 68H



A. RISING EDGE PULSE GENERATOR

FIG. 68I



B. FALLING-EDGE PULSE GENERATOR

FIG. 68J

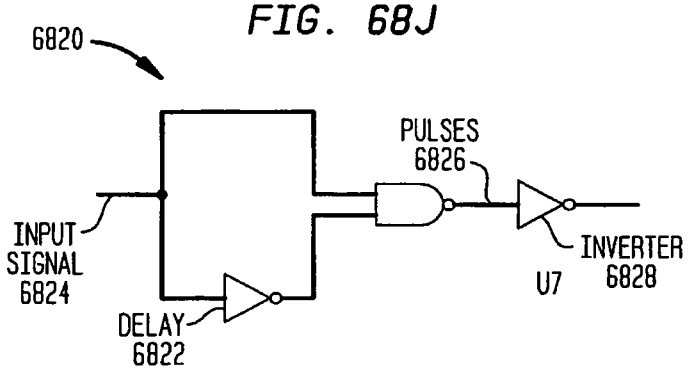


FIG. 68K

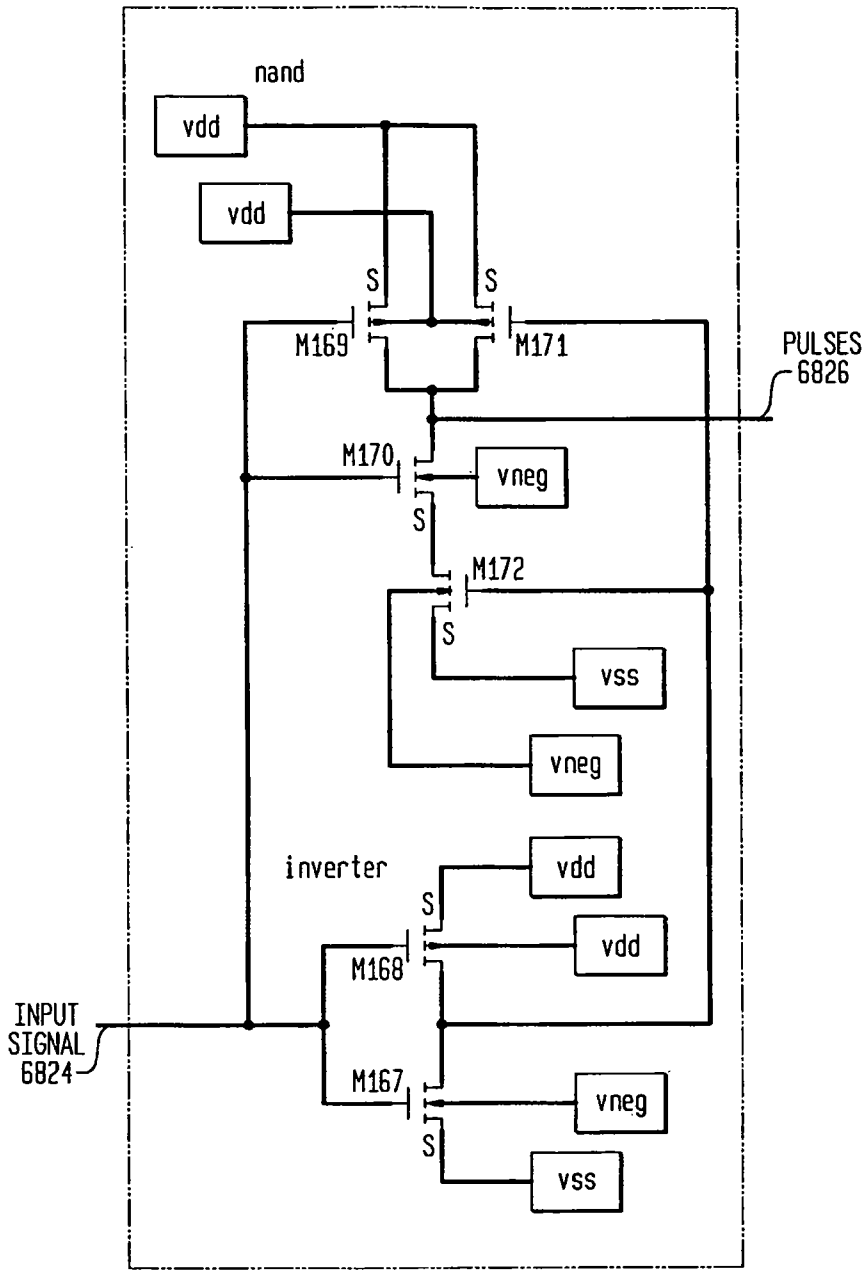


FIG. 68L

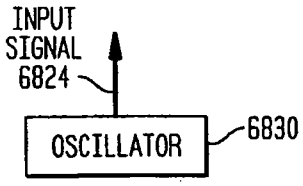


FIG. 69

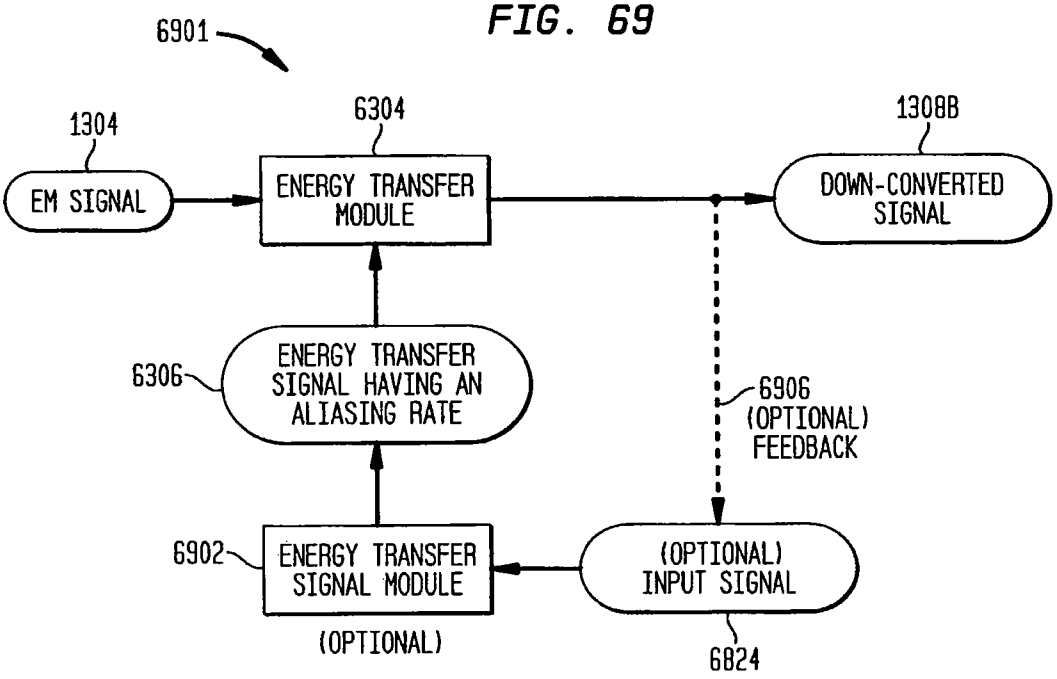

6901
1304
EM SIGNAL
6304
ENERGY TRANSFER MODULE
1308B
DOWN-CONVERTED SIGNAL
6306
ENERGY TRANSFER SIGNAL HAVING AN ALIASING RATE
6906
(OPTIONAL) FEEDBACK
6902
ENERGY TRANSFER SIGNAL MODULE
(OPTIONAL)
(OPTIONAL) INPUT SIGNAL
6824

FIG. 70

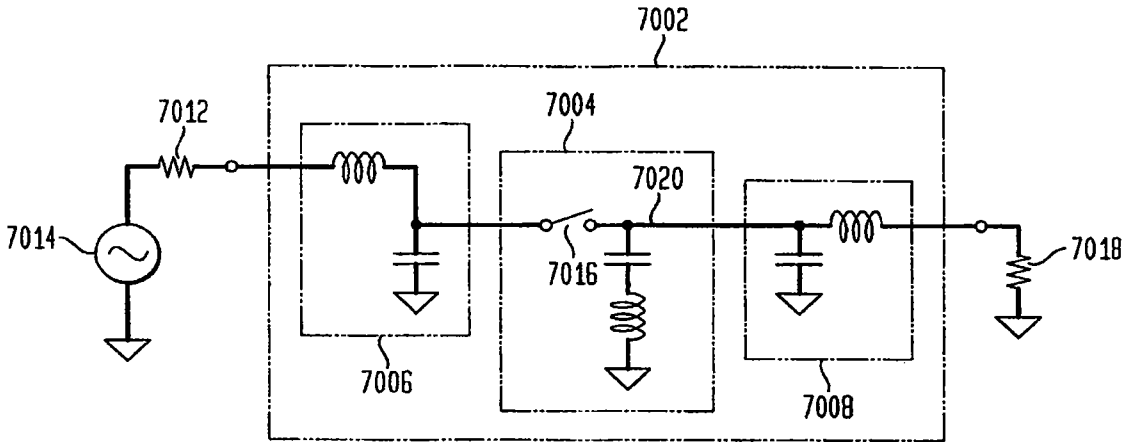


FIG. 71A

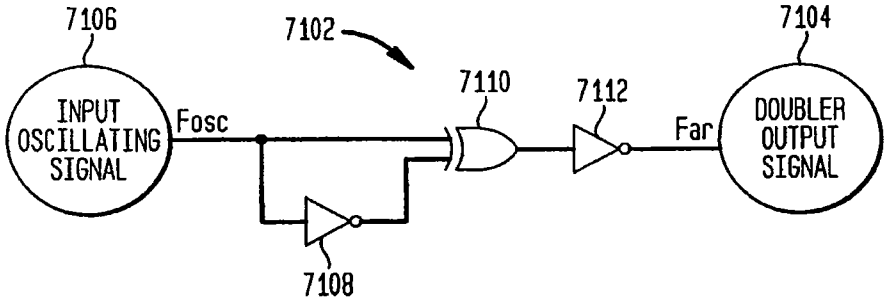


FIG. 71B

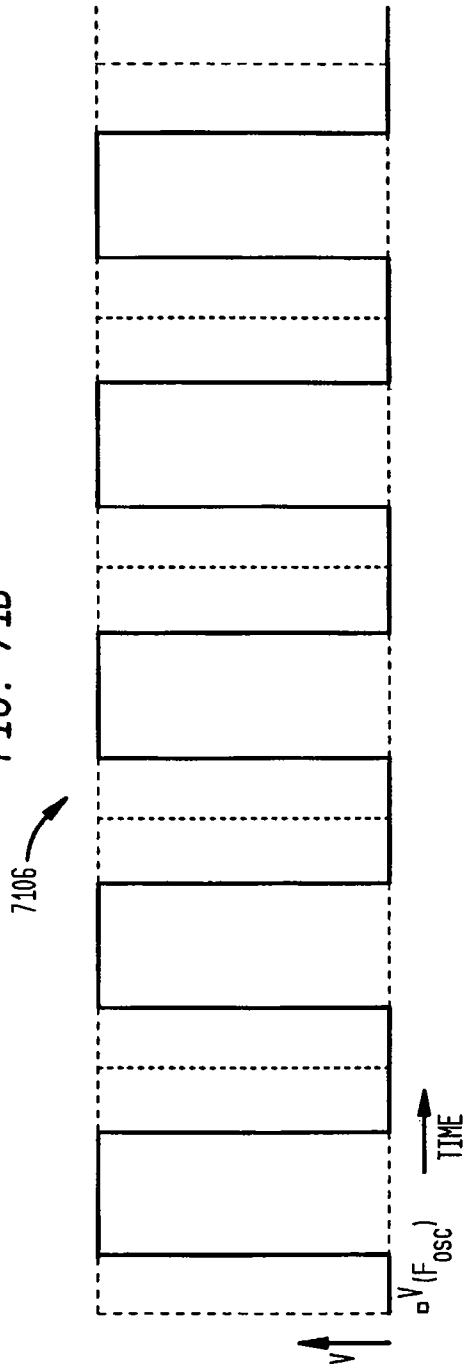


FIG. 71C

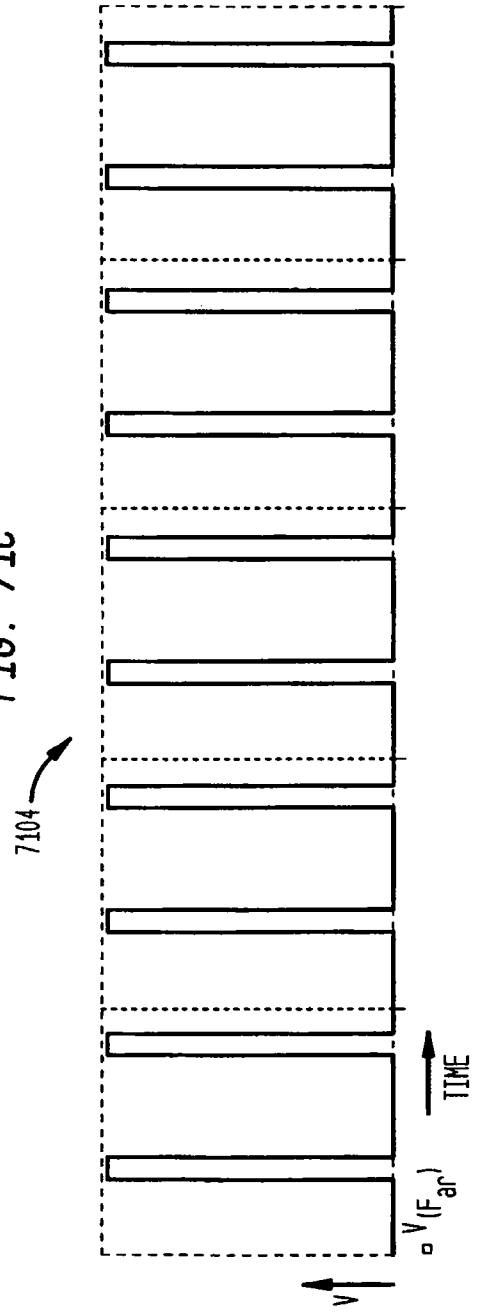


FIG. 72

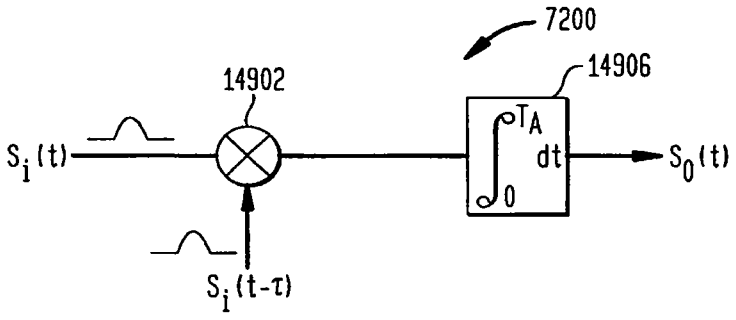


FIG. 73

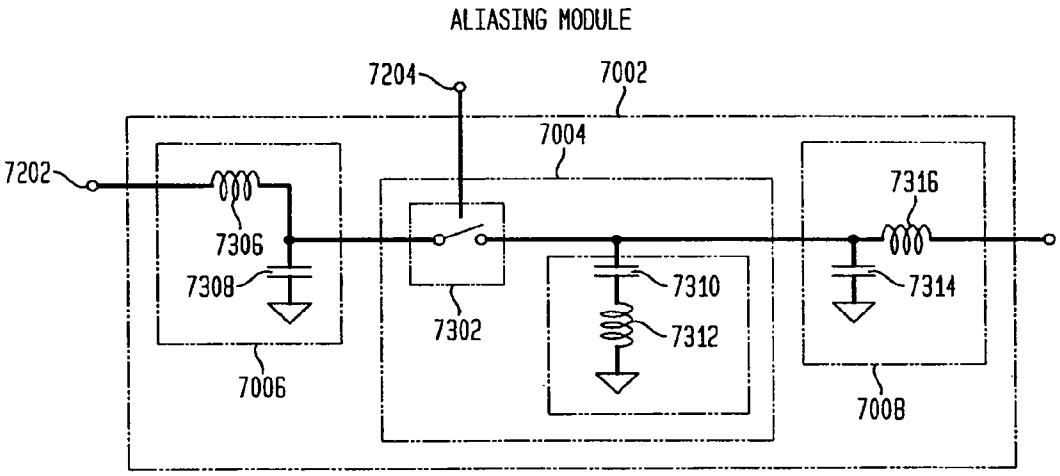
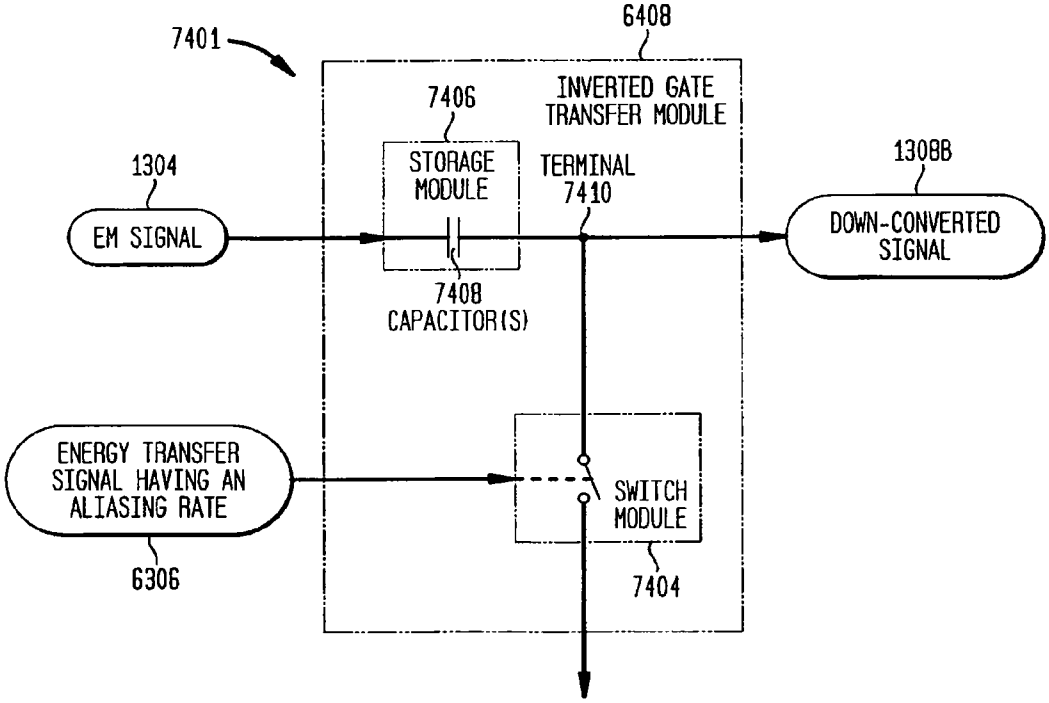

ALIASING MODULE
7204
7002
7004
7202
7306
7308
7316
7310
7312
7314
7302
7006
7008

FIG. 74


7401
6408
7406
INVERTED GATE TRANSFER MODULE
1304
STORAGE MODULE
TERMINAL 7410
1308B
EM SIGNAL
DOWN-CONVERTED SIGNAL
7408 CAPACITOR(S)
ENERGY TRANSFER SIGNAL HAVING AN ALIASING RATE
SWITCH MODULE
6306
7404

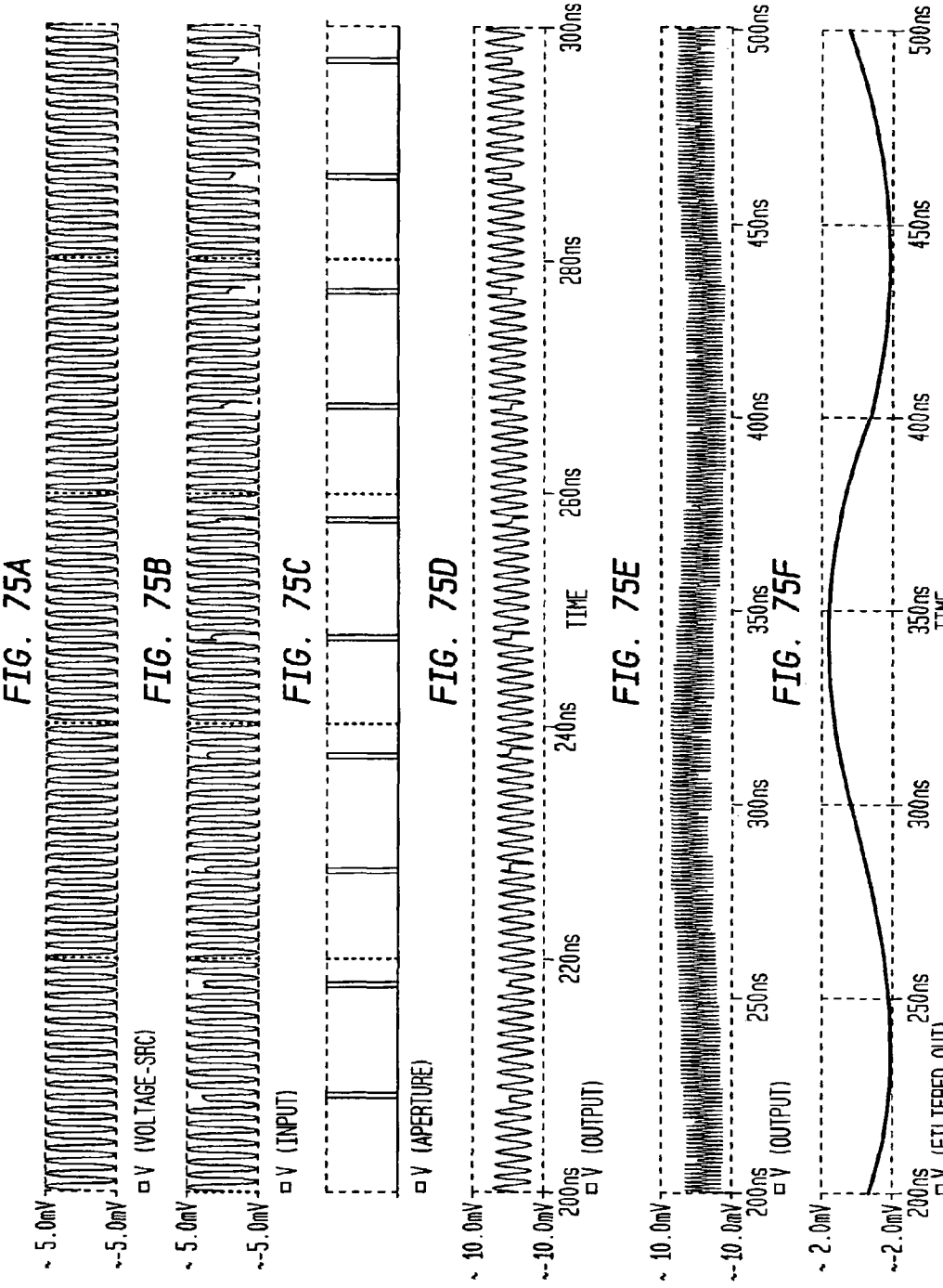


FIG. 75A

FIG. 75B

FIG. 75C

FIG. 75D

FIG. 75E

FIG. 75F

FIG. 76A

DIFFERENTIAL ENERGY TRANSFER CONFIGURATION

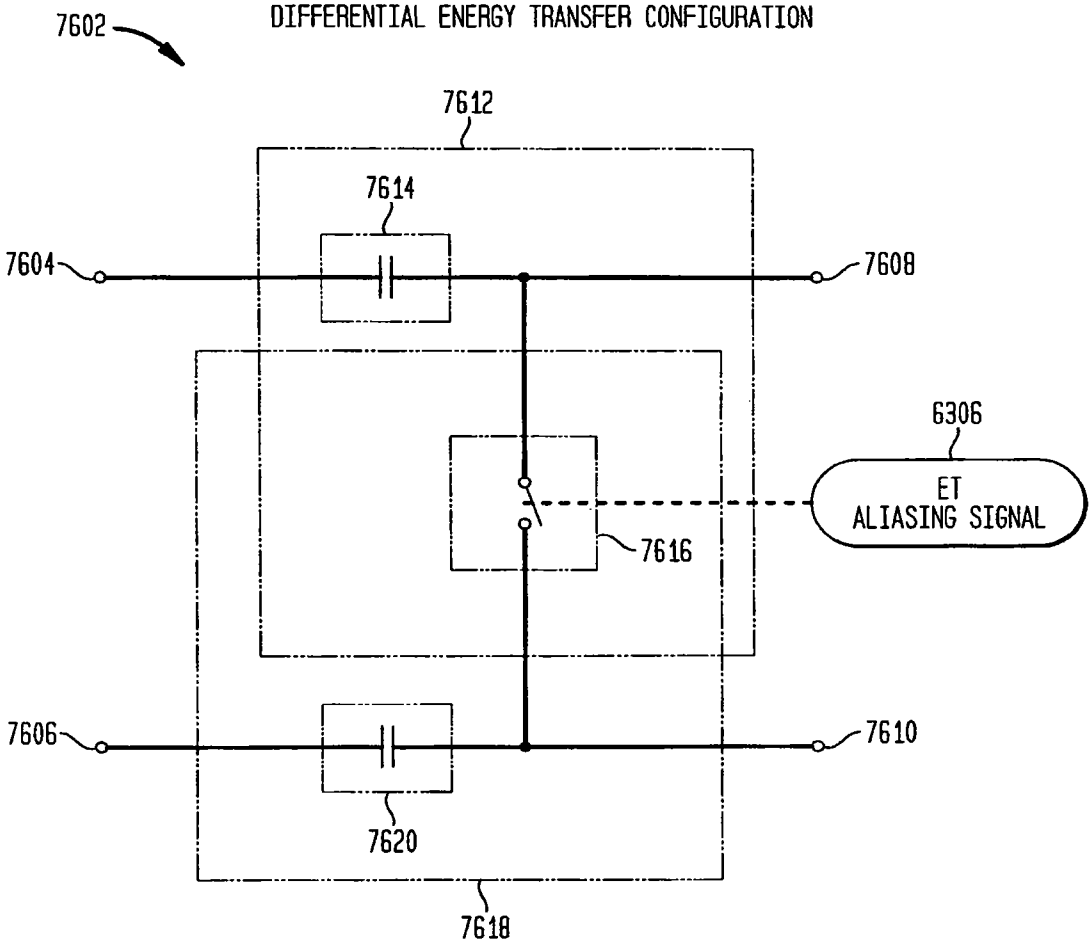


FIG. 76B

DIFFERENTIAL INPUT TO DIFFERENTIAL OUTPUT

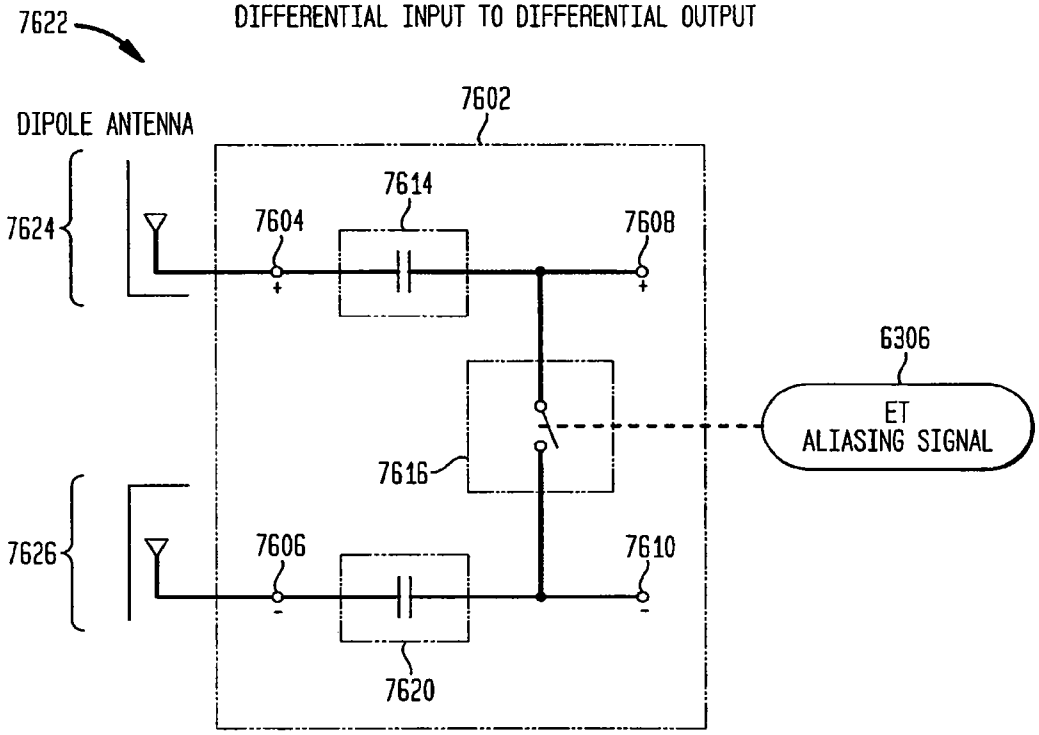


FIG. 76C

SINGLE INPUT TO DIFFERENTIAL OUTPUT

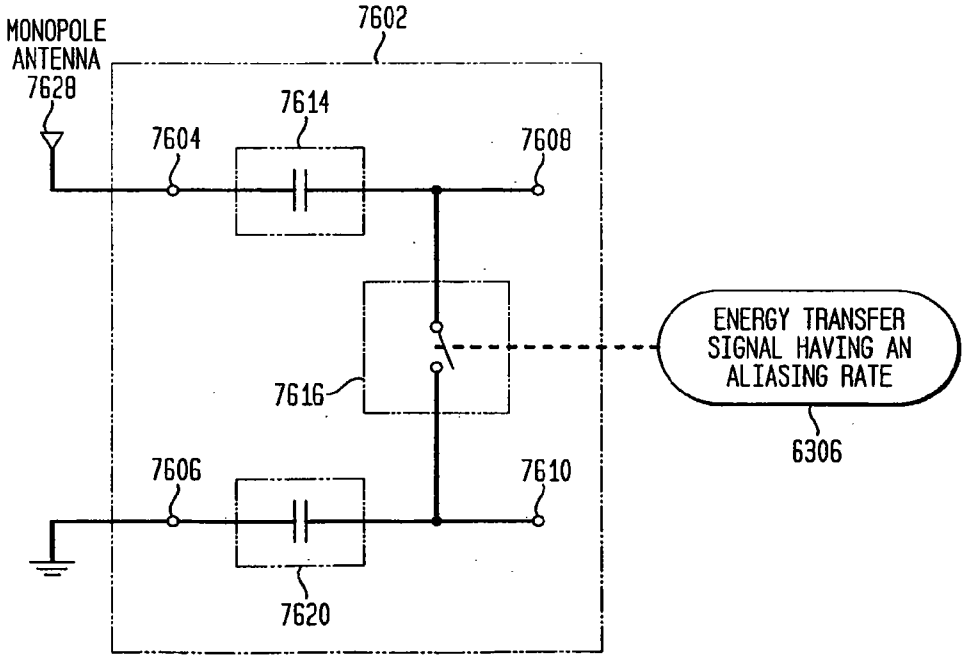


FIG. 76D

DIFFERENTIAL INPUT TO SINGLE OUTPUT

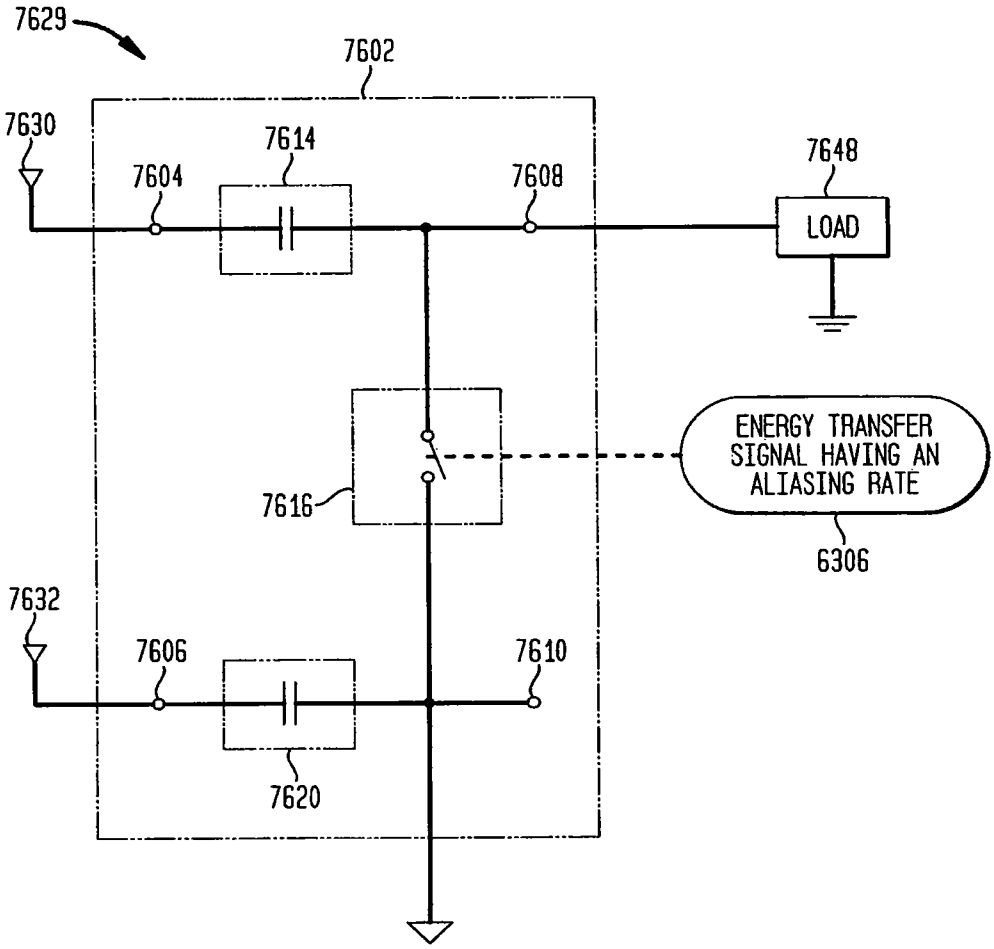


FIG. 76E

EXAMPLE INPUT/OUTPUT CIRCUITRY

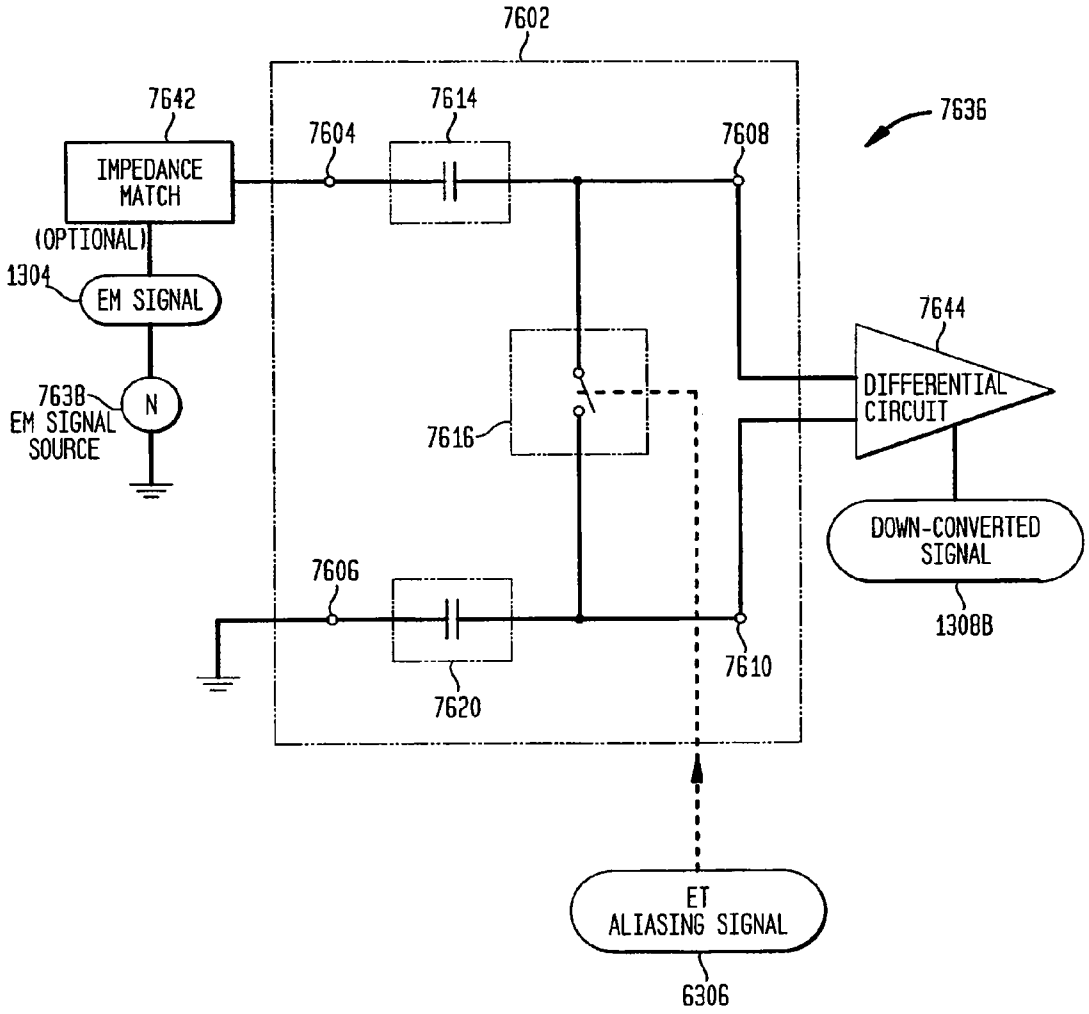


FIG. 77A

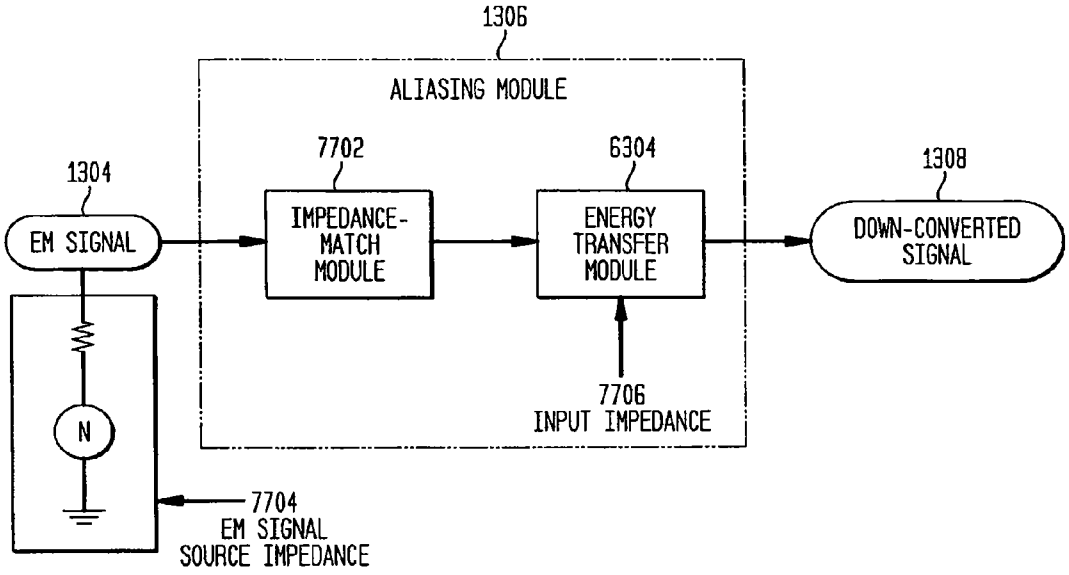


FIG. 77B

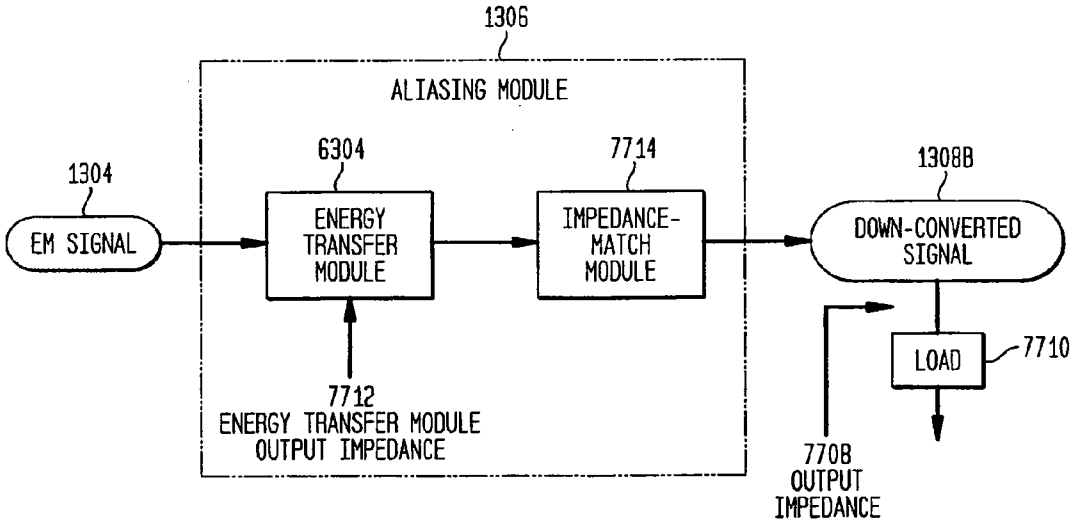


FIG. 77C

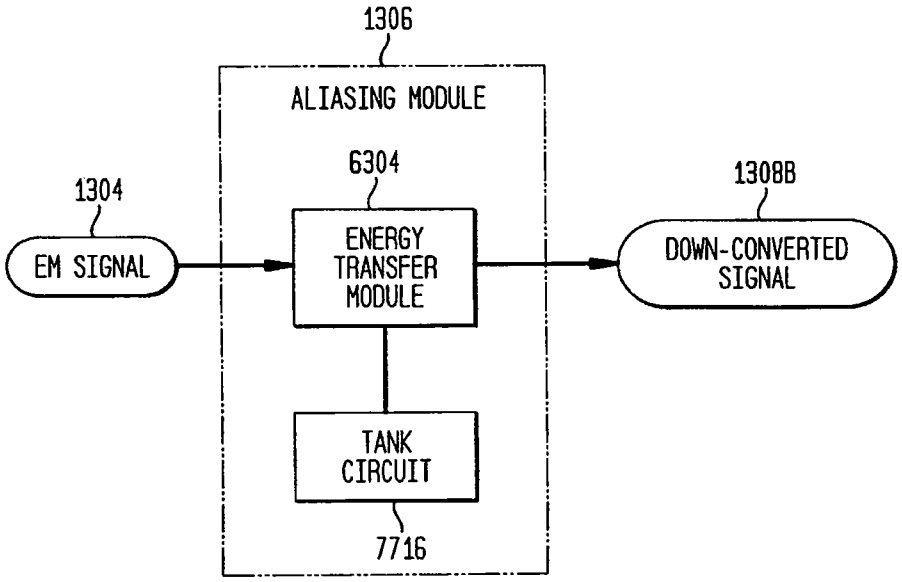

1306
ALIASING MODULE
6304
1304
EM SIGNAL
ENERGY TRANSFER MODULE
1308B
DOWN-CONVERTED SIGNAL
TANK CIRCUIT
7716

FIG. 78A

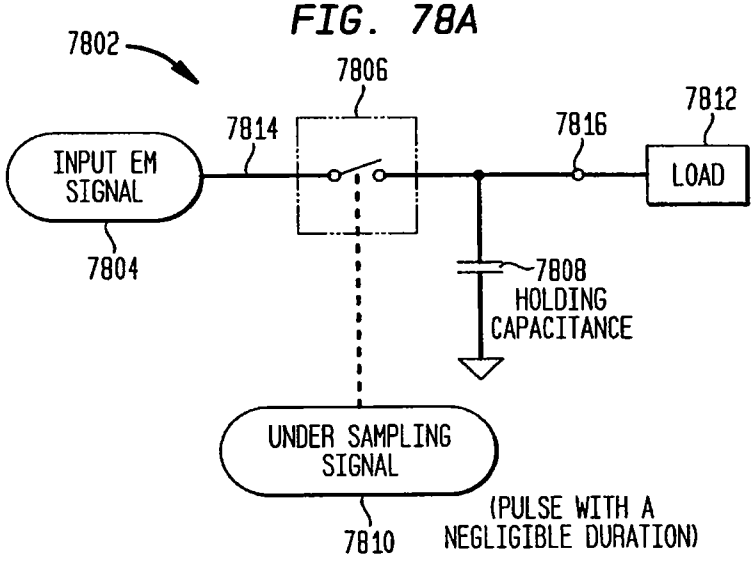
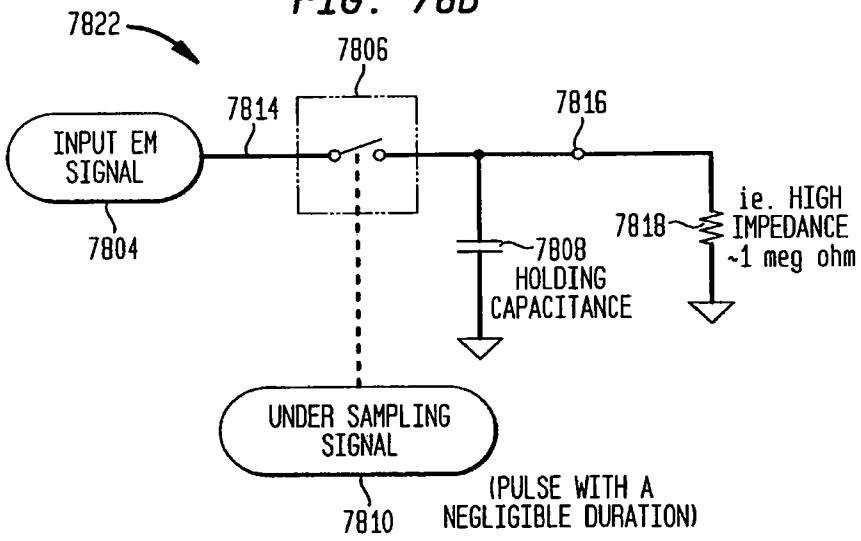
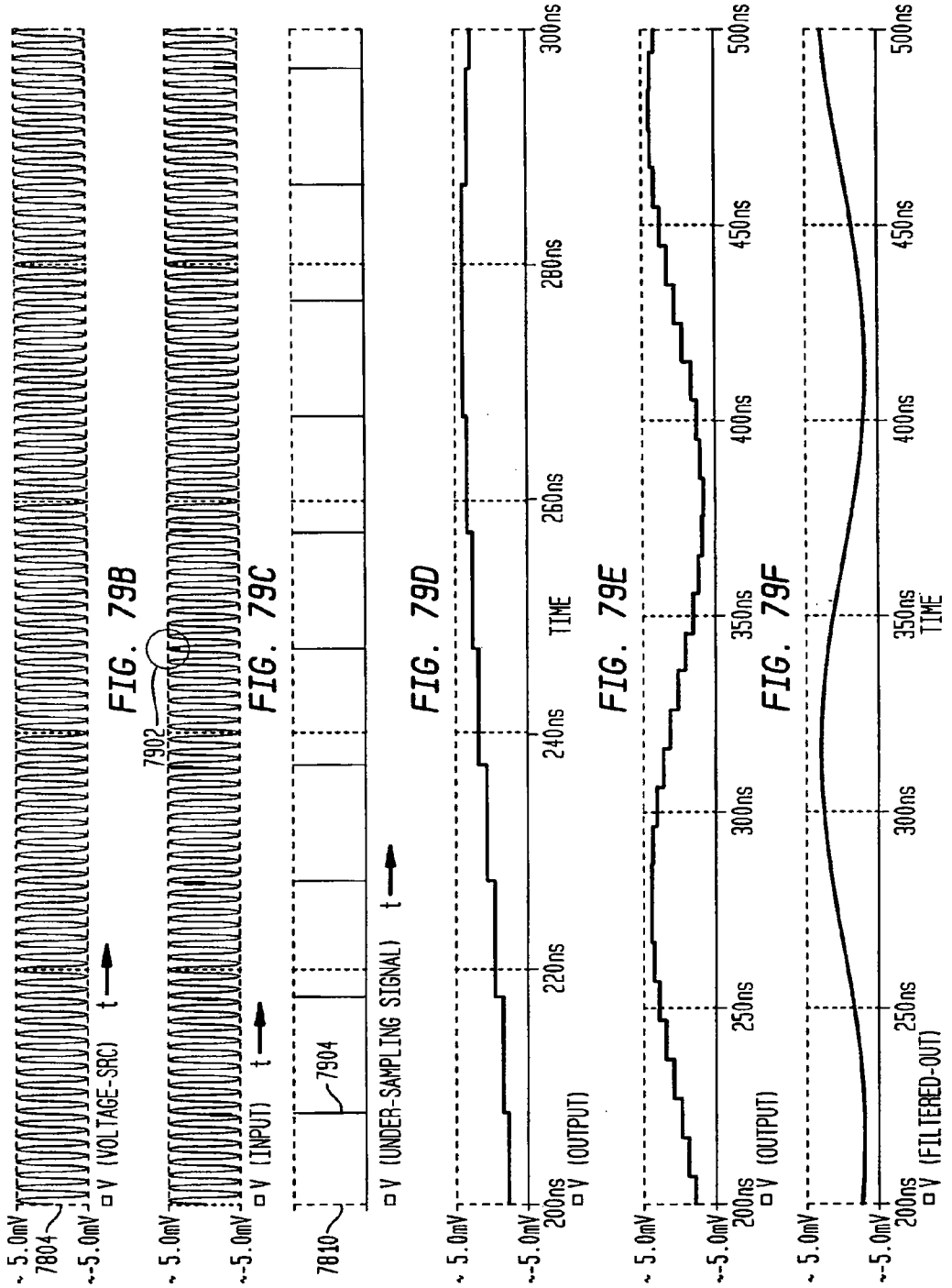
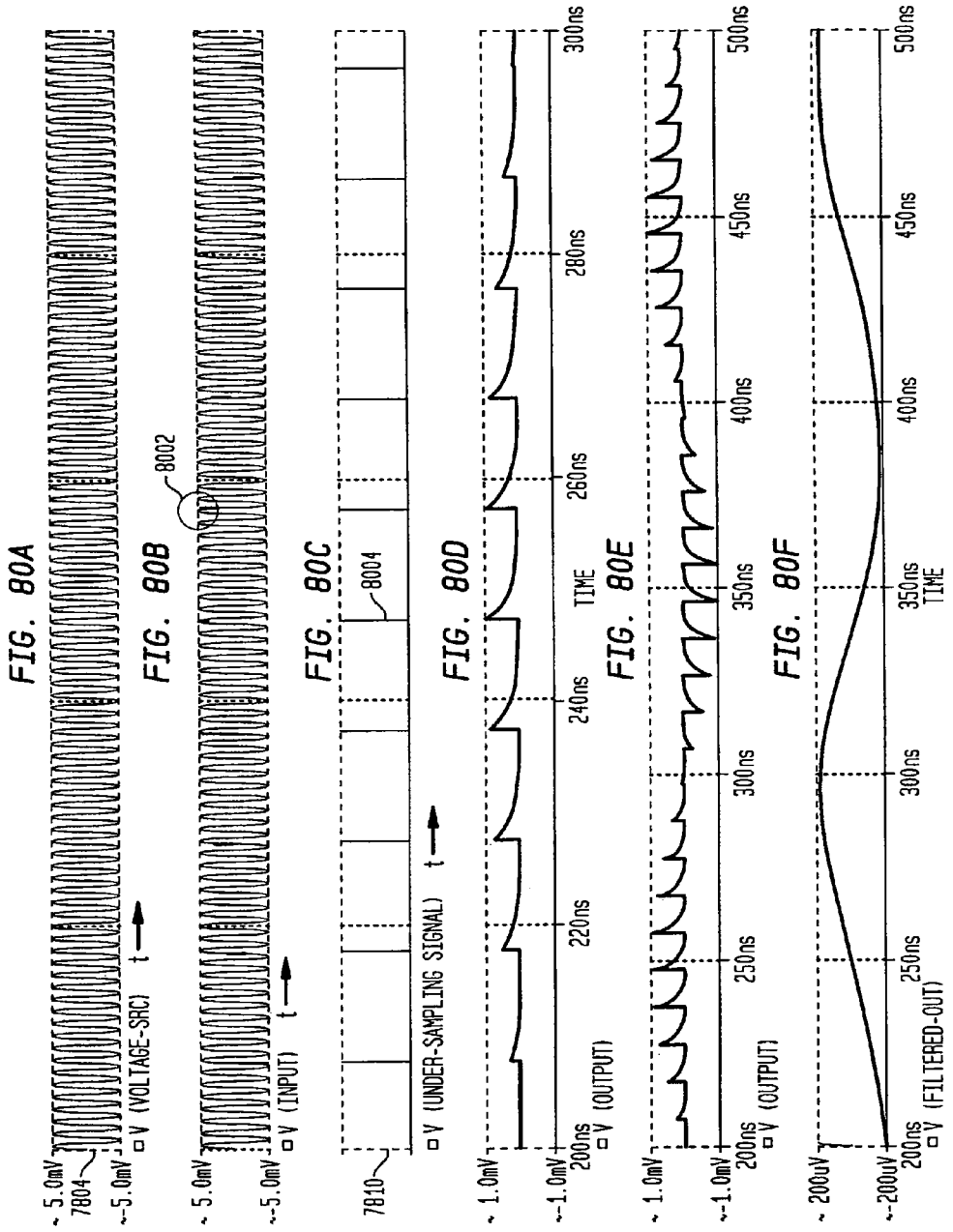


FIG. 78B




FIG. 79A
~ 5.0mV
7804
--5.0mV
V (VOLTAGE-SRC)
t
FIG. 79B
7902
~ 5.0mV
--5.0mV
V (INPUT)
t
FIG. 79C
7904
7810
V (UNDER-SAMPLING SIGNAL)
t
FIG. 79D
~ 5.0mV
--5.0mV
200ns
220ns
240ns
260ns
280ns
300ns
TIME
V (OUTPUT)
FIG. 79E
~ 5.0mV
--5.0mV
200ns
250ns
300ns
350ns
400ns
450ns
500ns
V (OUTPUT)
FIG. 79F
~ 5.0mV
--5.0mV
200ns
250ns
300ns
350ns
400ns
450ns
500ns
TIME
V (FILTERED-OUT)


FIG. 80A
~ 5.0mV
7804
~-5.0mV
V (VOLTAGE-SRC)
t
FIG. 80B
8002
~ 5.0mV
~-5.0mV
V (INPUT)
t
FIG. 80C
8004
7810
V (UNDER-SAMPLING SIGNAL)
t
FIG. 80D
~ 1.0mV
~-1.0mV
200ns
220ns
240ns
260ns
280ns
300ns
TIME
V (OUTPUT)
FIG. 80E
~ 1.0mV
~-1.0mV
200ns
250ns
300ns
350ns
400ns
450ns
500ns
V (OUTPUT)
FIG. 80F
~ 200uV
~-200uV
200ns
250ns
300ns
350ns
400ns
450ns
500ns
TIME
V (FILTERED-OUT)

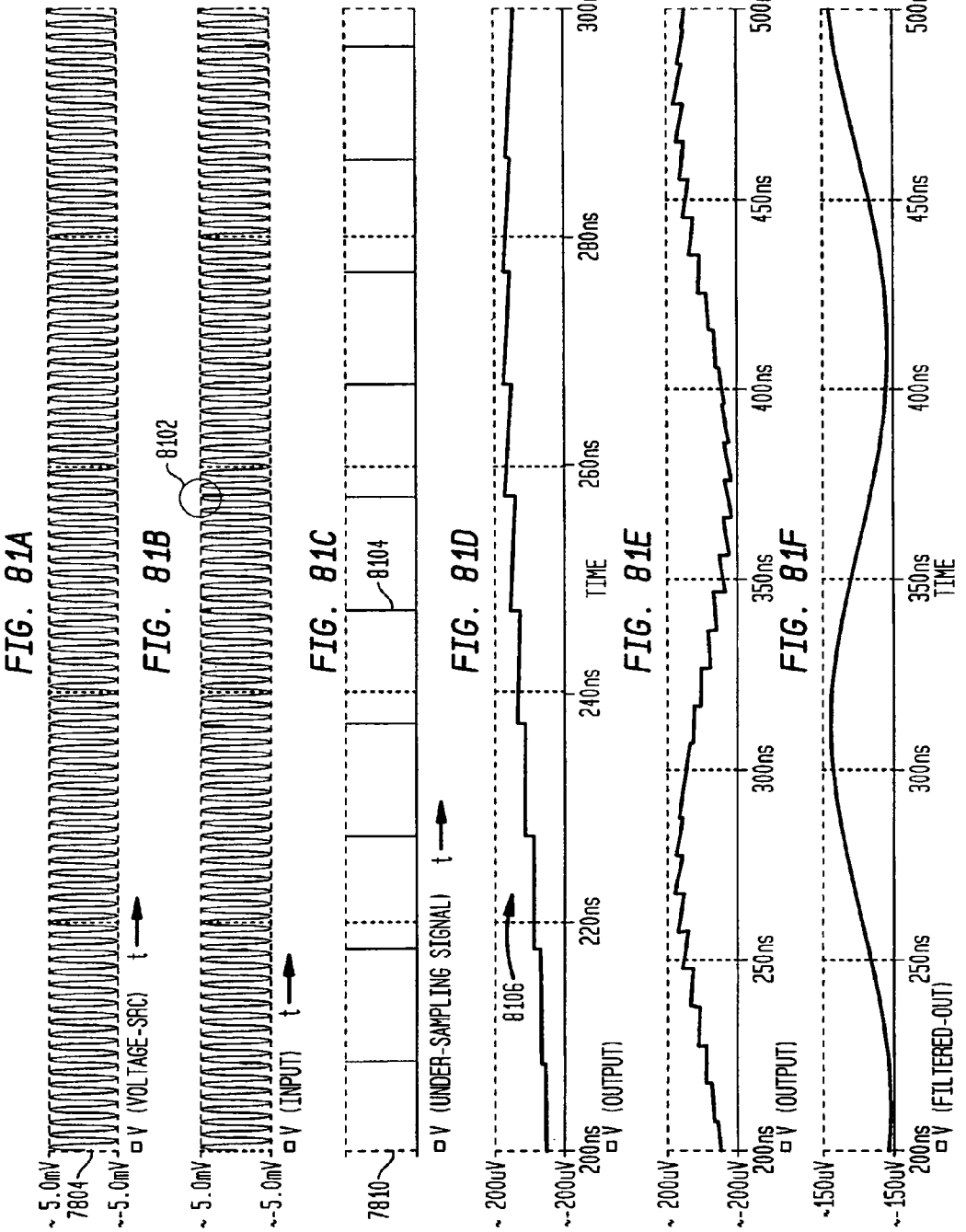

FIG. 81A
~5.0mV
7804
~-5.0mV
V (VOLTAGE-SRC) t
FIG. 81B
8102
~5.0mV
~-5.0mV
V (INPUT) t
FIG. 81C
8104
7810
V (UNDER-SAMPLING SIGNAL) t
FIG. 81D
~200uV
8106
~-200uV
200ns
220ns
240ns
260ns
280ns
300ns
V (OUTPUT)
TIME
FIG. 81E
~200uV
~-200uV
200ns
250ns
300ns
350ns
400ns
450ns
500ns
V (OUTPUT)
FIG. 81F
~150uV
~-150uV
200ns
250ns
300ns
350ns
400ns
450ns
500ns
V (FILTERED-OUT)
TIME

FIG. 82A

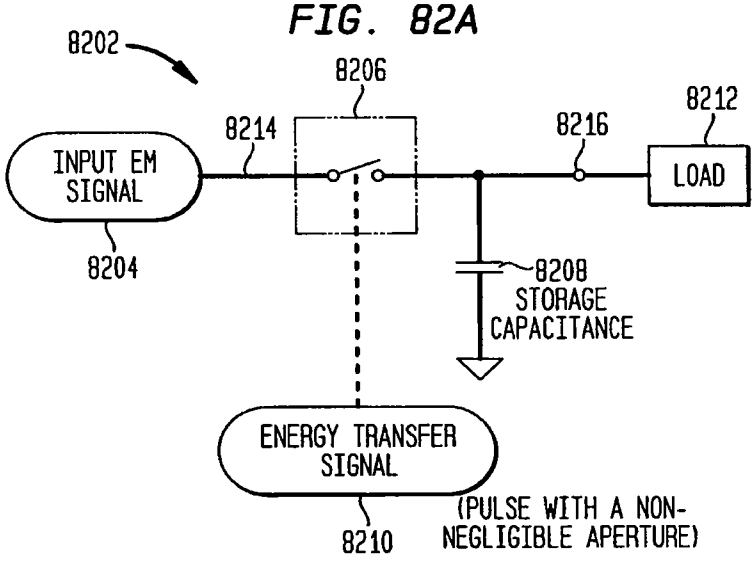
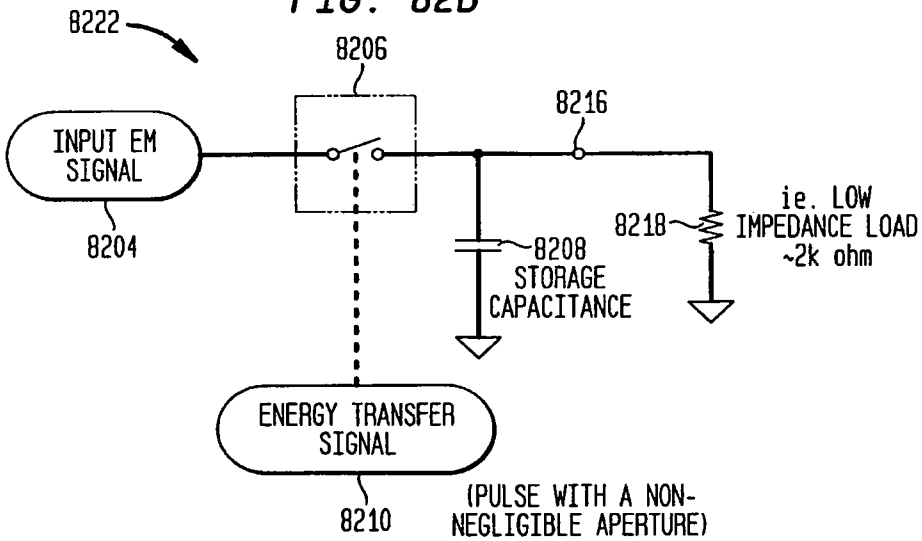


FIG. 82B



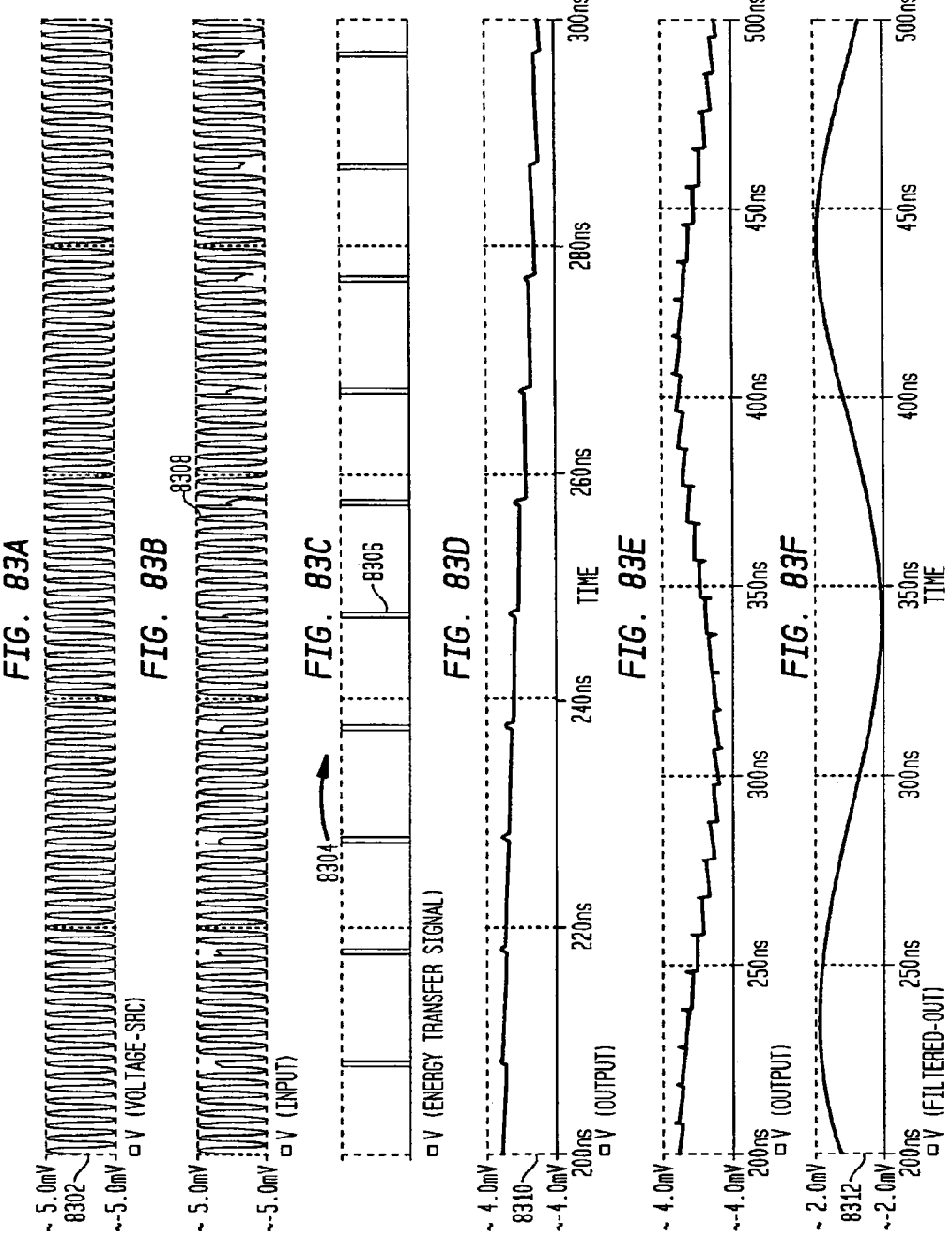

FIG. 83A
~ 5.0mV
8302
--5.0mV
V (VOLTAGE-SRC)
FIG. 83B
8308
~ 5.0mV
--5.0mV
V (INPUT)
FIG. 83C
8304
8306
V (ENERGY TRANSFER SIGNAL)
FIG. 83D
~ 4.0mV
8310
--4.0mV
200ns
220ns
240ns
260ns
280ns
300ns
TIME
V (OUTPUT)
FIG. 83E
~ 4.0mV
--4.0mV
200ns
250ns
300ns
350ns
400ns
450ns
500ns
V (OUTPUT)
FIG. 83F
~ 2.0mV
8312
--2.0mV
200ns
250ns
300ns
350ns
400ns
450ns
500ns
TIME
V (FILTERED-OUT)

FIG. 84A

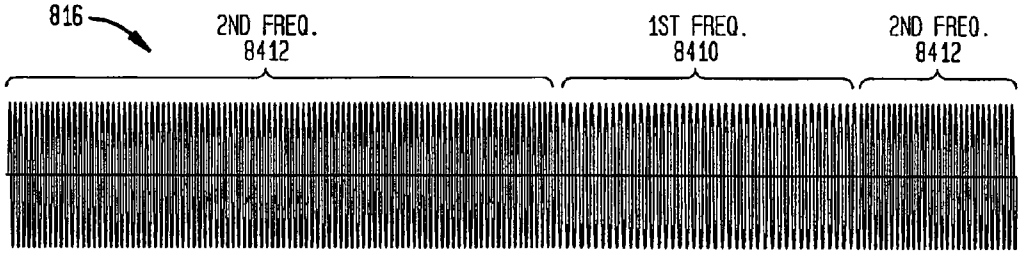
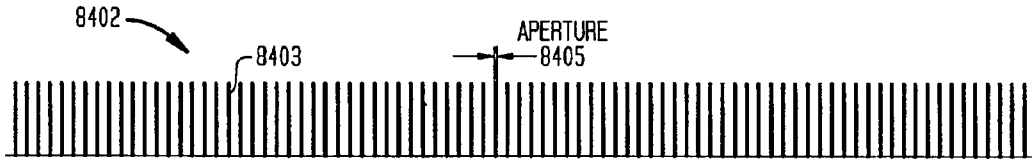


FIG. 84B



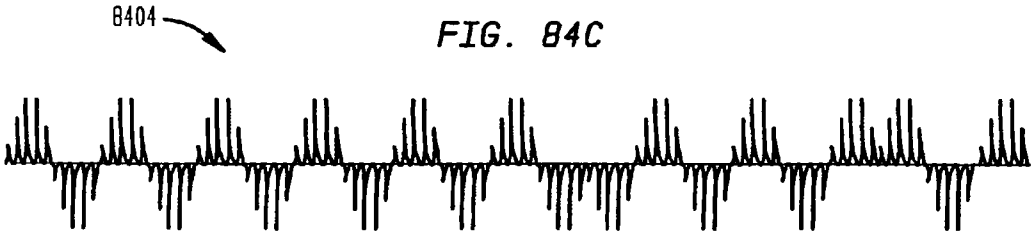


FIG. 84C

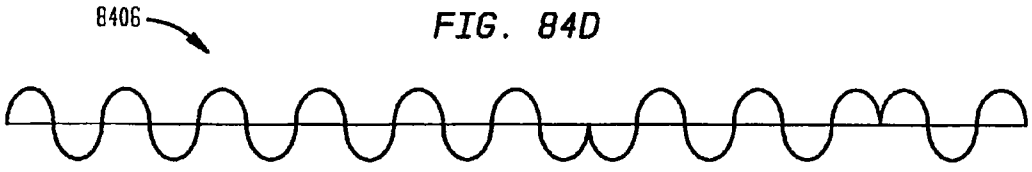


FIG. 84D

FIG. 85A

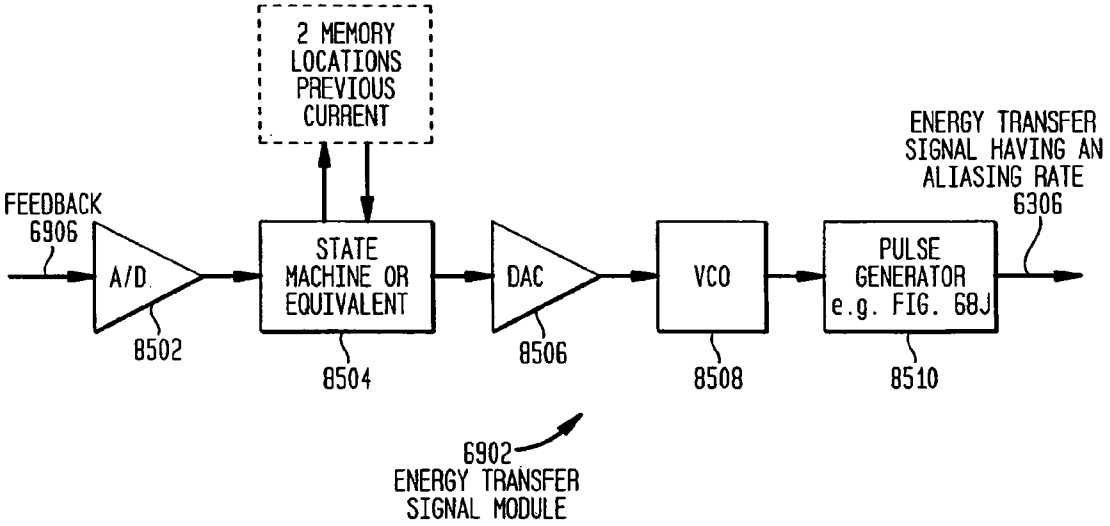

2 MEMORY LOCATIONS PREVIOUS CURRENT
ENERGY TRANSFER SIGNAL HAVING AN ALIASING RATE
6306
FEEDBACK
6906
A/D
8502
STATE MACHINE OR EQUIVALENT
8504
DAC
8506
VCO
8508
PULSE GENERATOR e.g. FIG. 68J
8510
6902
ENERGY TRANSFER SIGNAL MODULE

FIG. 85B

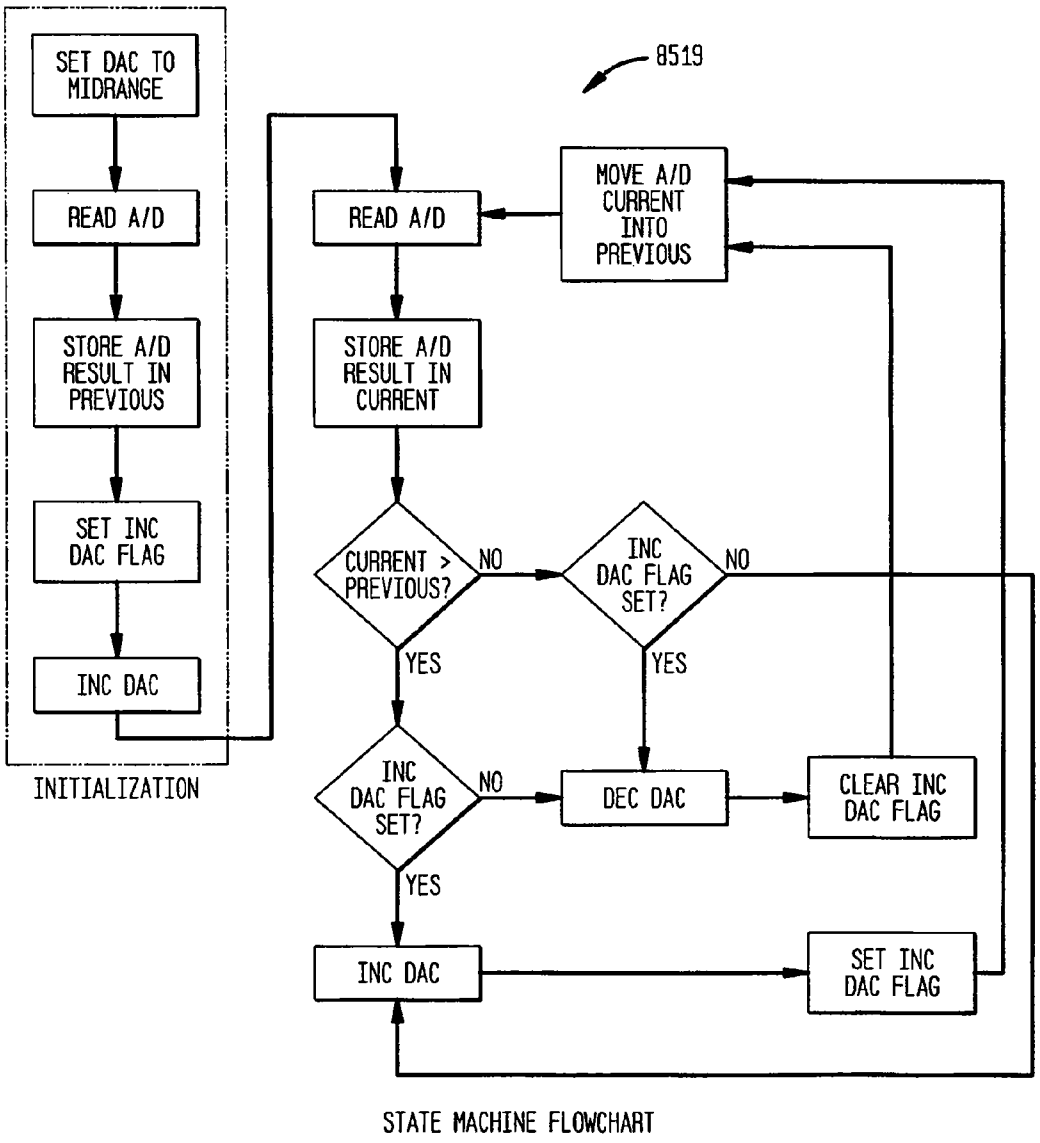
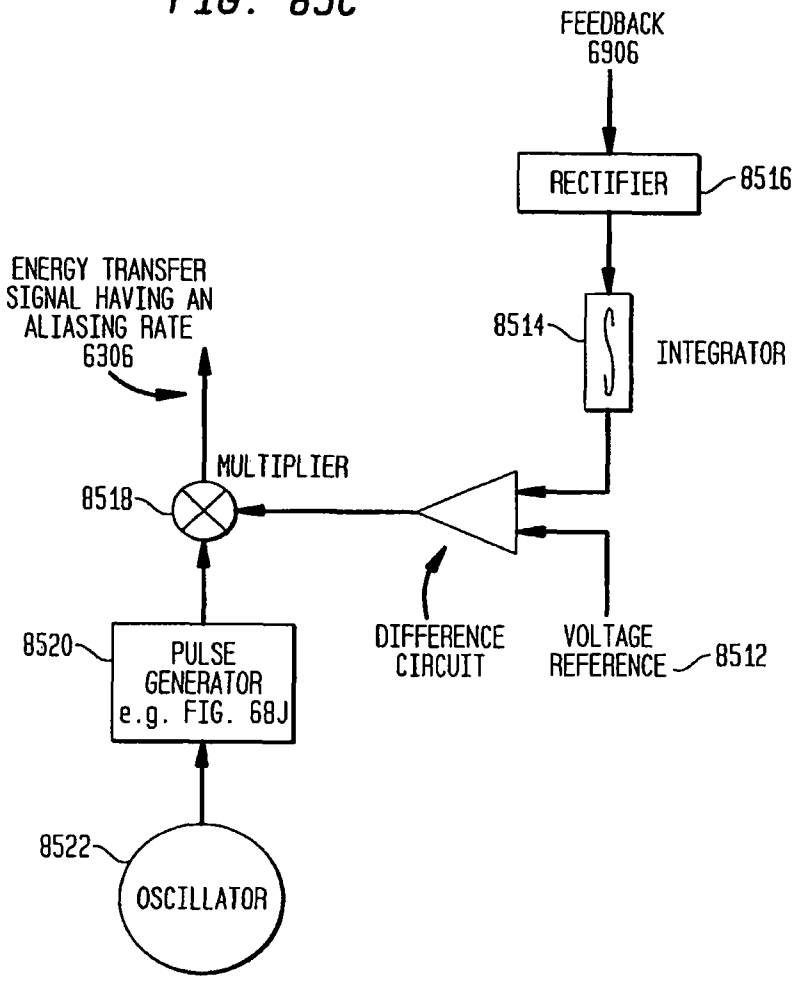

SET DAC TO MIDRANGE
READ A/D
STORE A/D RESULT IN PREVIOUS
SET INC DAC FLAG
INC DAC
INITIALIZATION
8519
READ A/D
MOVE A/D CURRENT INTO PREVIOUS
STORE A/D RESULT IN CURRENT
CURRENT > PREVIOUS?
NO
INC DAC FLAG SET?
NO
YES
YES
INC DAC FLAG SET?
NO
DEC DAC
CLEAR INC DAC FLAG
YES
INC DAC
SET INC DAC FLAG
STATE MACHINE FLOWCHART

FIG. 85C



ENERGY TRANSFER SIGNAL MODULE 6902

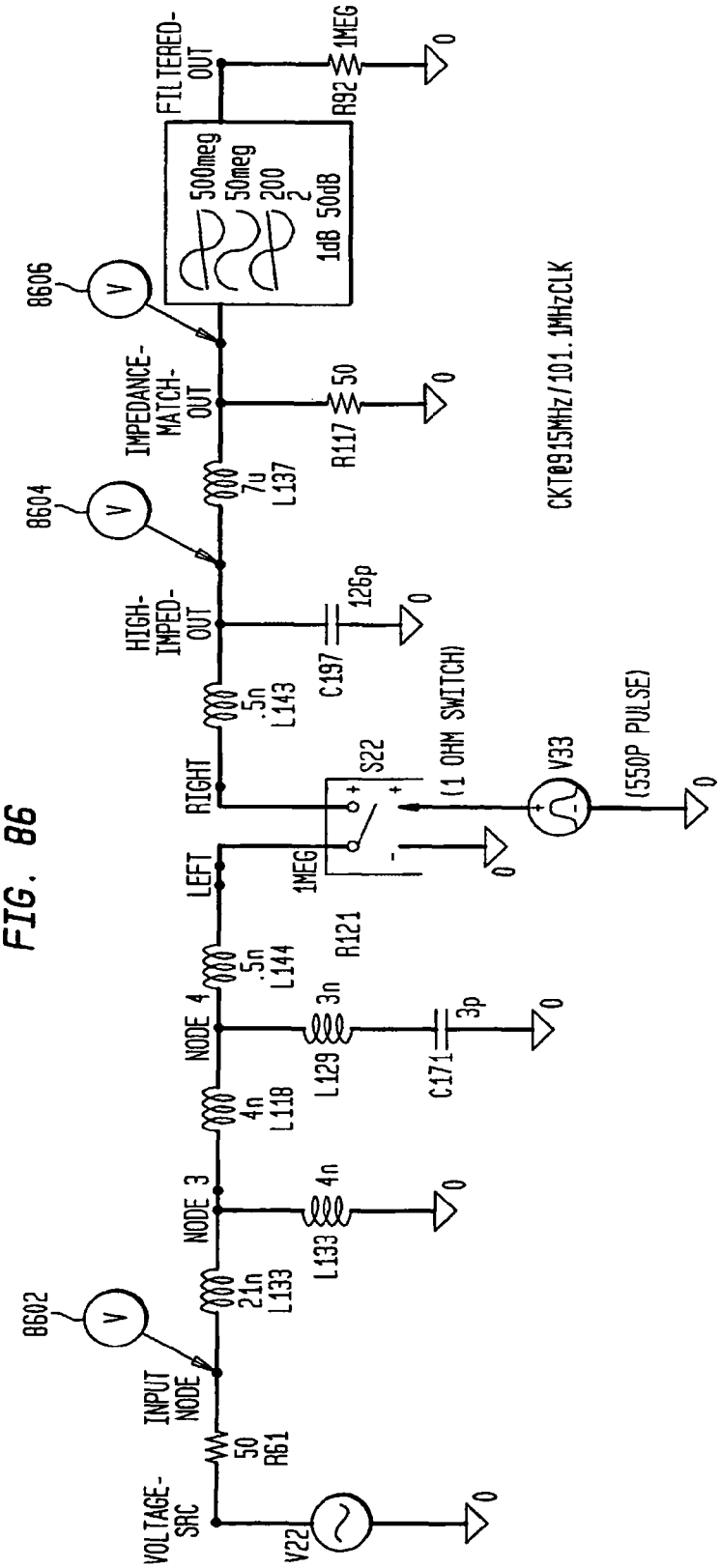
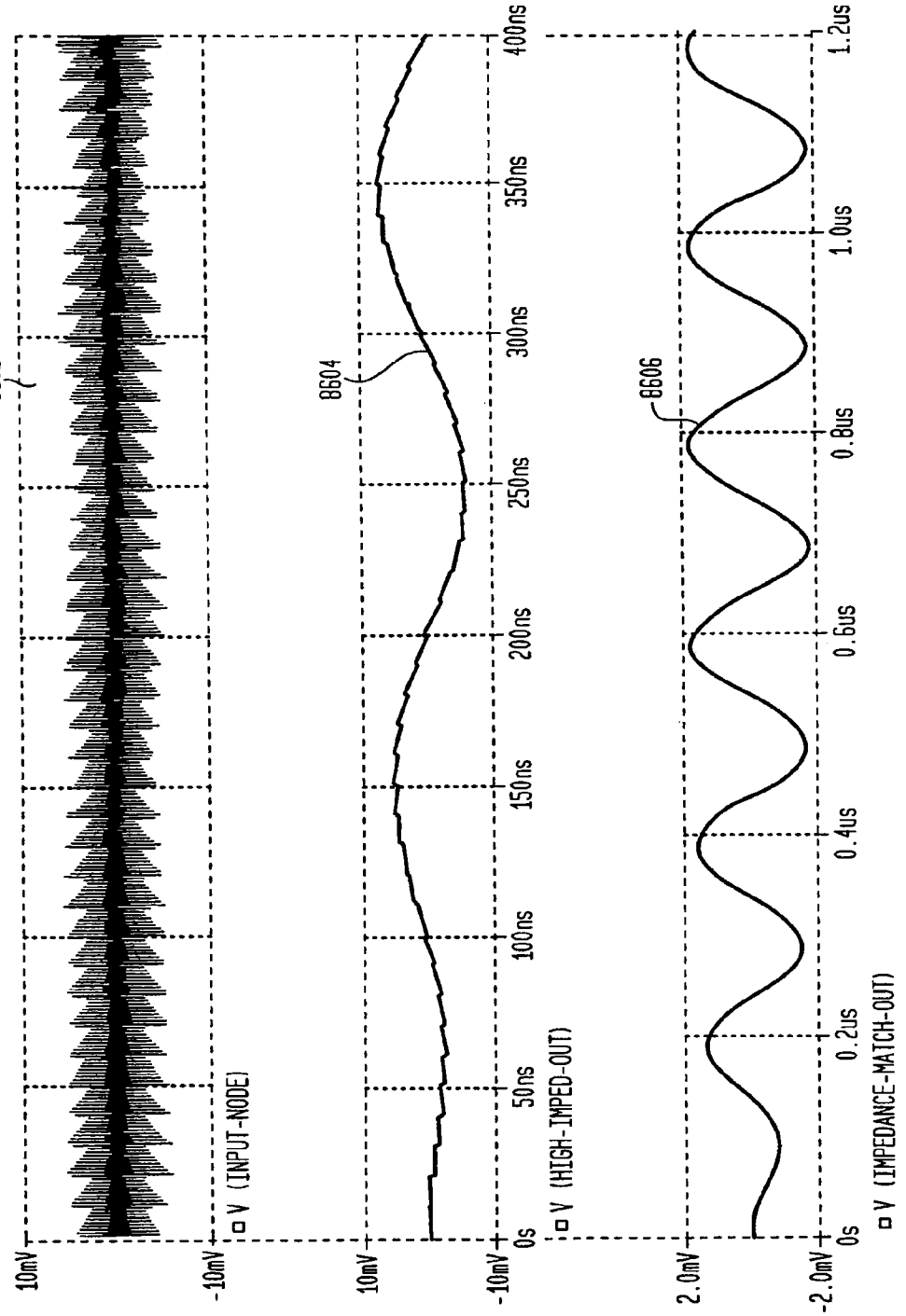

VOLTAGE-SRC
V22
50
R61
INPUT NODE
B602
21n
L133
NODE 3
4n
L133
4n
L118
NODE 4
3n
L129
3p
C171
.5n
L144
R121
LEFT
1MEG
S22
(1 OHM SWITCH)
V33
(550P PULSE)
RIGHT
.5n
L143
C197
126p
HIGH-IMPED-OUT
B604
7u
L137
IMPEDANCE-MATCH-OUT
R117
50
B606
500meg
50meg
200
2
10B 50dB
FILTERED-OUT
R92
1MEG
CKT@915MHz/101.1MHzCLK
0

FIG. 86

FIG. 87


8602
8604
8606
10mV
-10mV
V (INPUT-NODE)
10mV
-10mV
0s
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
V (HIGH-IMPED-OUT)
2.0mV
-2.0mV
0s
0.2us
0.4us
0.6us
0.8us
1.0us
1.2us
V (IMPEDANCE-MATCH-OUT)

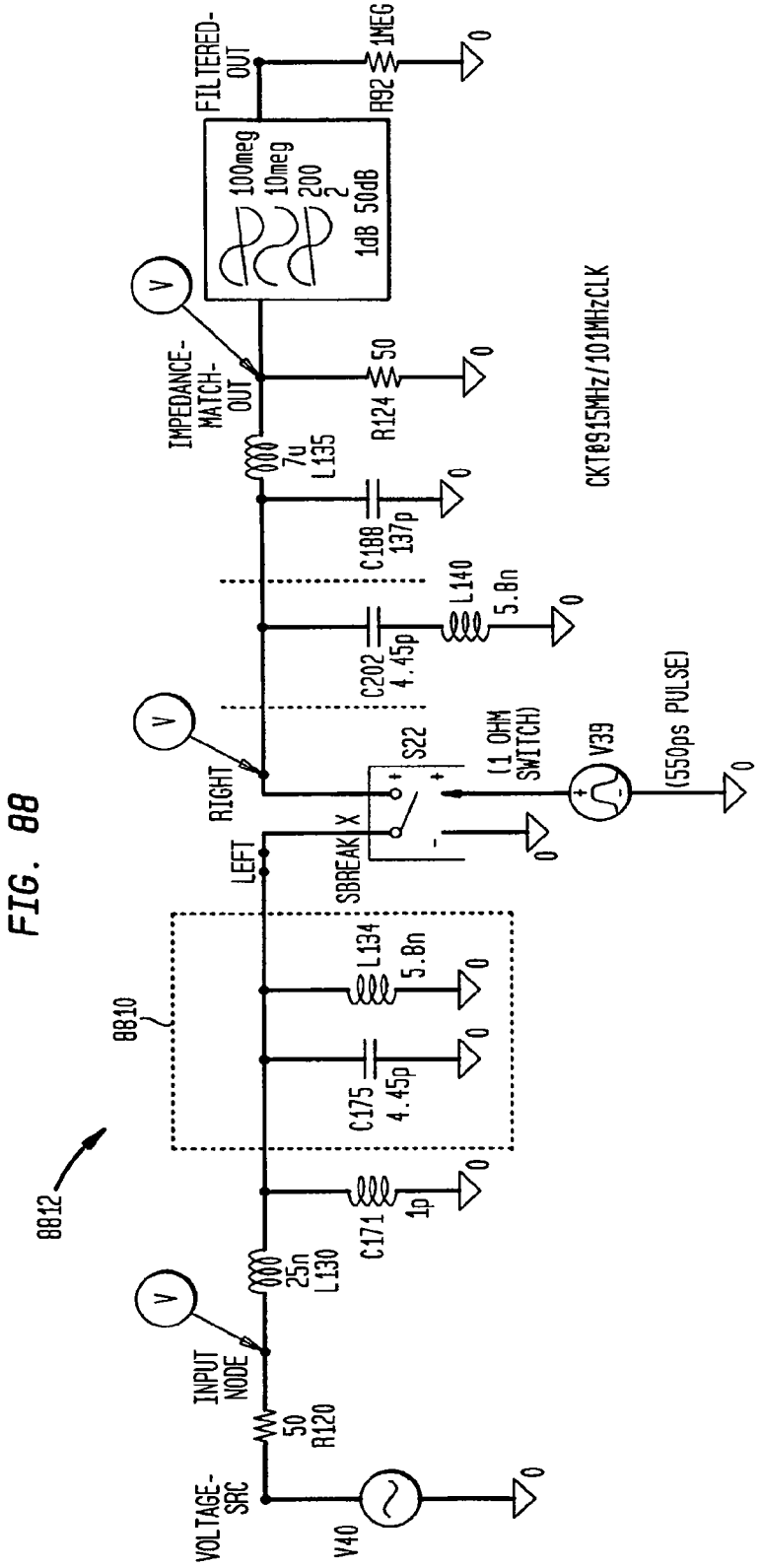
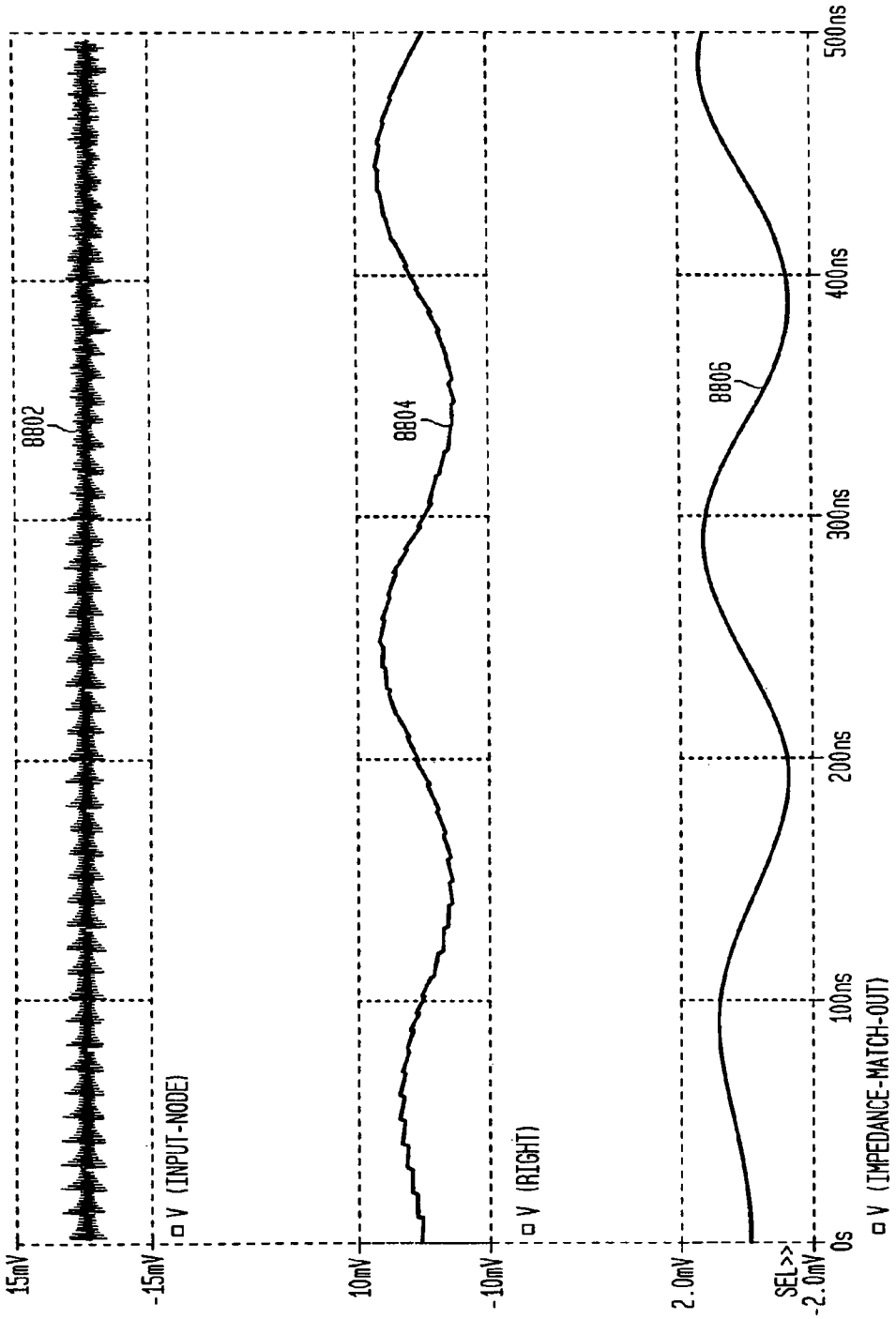

FILTERED-OUT
R92
1MEG
100meg
10meg
200
2
1dB 50dB
IMPEDANCE-MATCH-OUT
R124
50
7u
L135
C188
137p
L140
5.8n
C202
4.45p
RIGHT
S22
(1 OHM SWITCH)
V39
(550ps PULSE)
CKT@915MHz/101MHzCLK
LEFT
SBREAK
X
L134
5.8n
8810
C175
4.45p
8812
C171
1p
25n
L130
INPUT NODE
50
R120
VOLTAGE-SRC
V40
0

FIG. 88

FIG. 89


8802
8804
8806
15mV
-15mV
10mV
-10mV
2.0mV
SEL>>
-2.0mV
0s
100ns
200ns
300ns
400ns
500ns
V (INPUT-NODE)
V (RIGHT)
V (IMPEDANCE-MATCH-OUT)

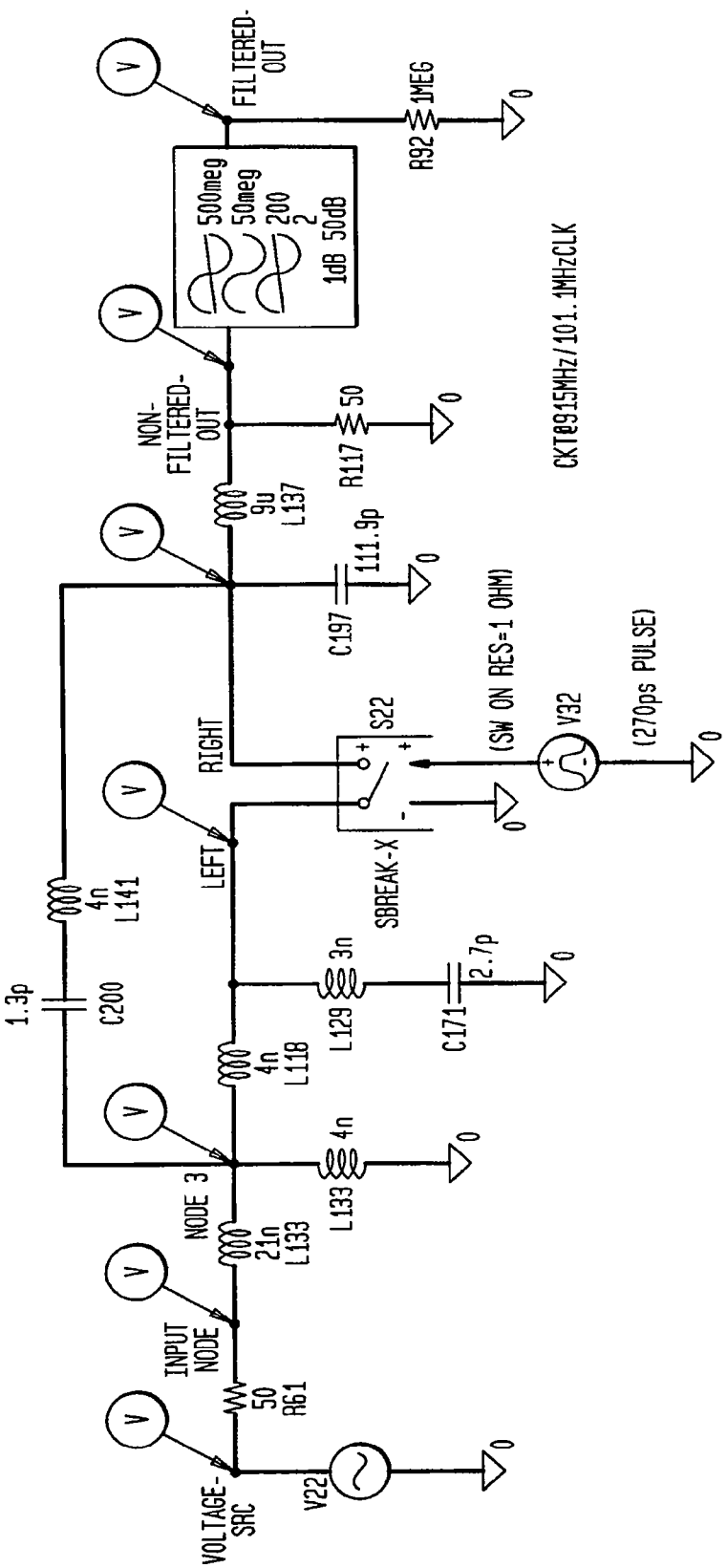
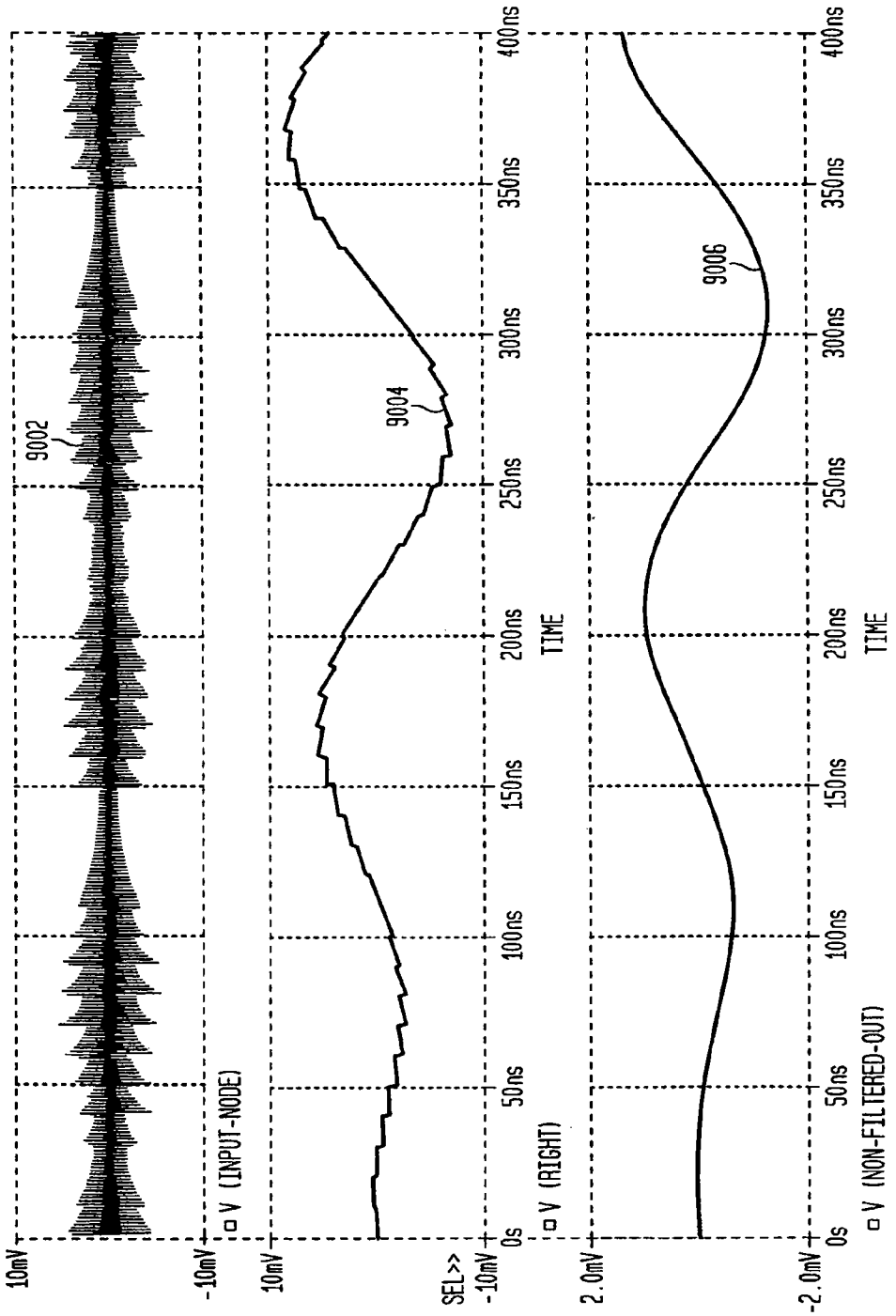

FILTERED-OUT
R92
1MEG
500meg
50meg
200
2
1dB 50dB
NON-FILTERED-OUT
R117
50
L137
9u
C197
111.9p
CKT@915MHz/101.1MHzCLK
RIGHT
S22
(SW ON RES=1 OHM)
V32
(270ps PULSE)
LEFT
SBREAK-X
L141
4n
C200
1.3p
L129
3n
C171
2.7p
L118
4n
L133
4n
NODE 3
L133
21n
INPUT NODE
R61
50
VOLTAGE-SRC
V22
0

FIG. 90

FIG. 91


9002
9004
9006
10mV
-10mV
V (INPUT-NODE)
10mV
SEL>>
-10mV
0s
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
TIME
V (RIGHT)
2.0mV
-2.0mV
V (NON-FILTERED-OUT)

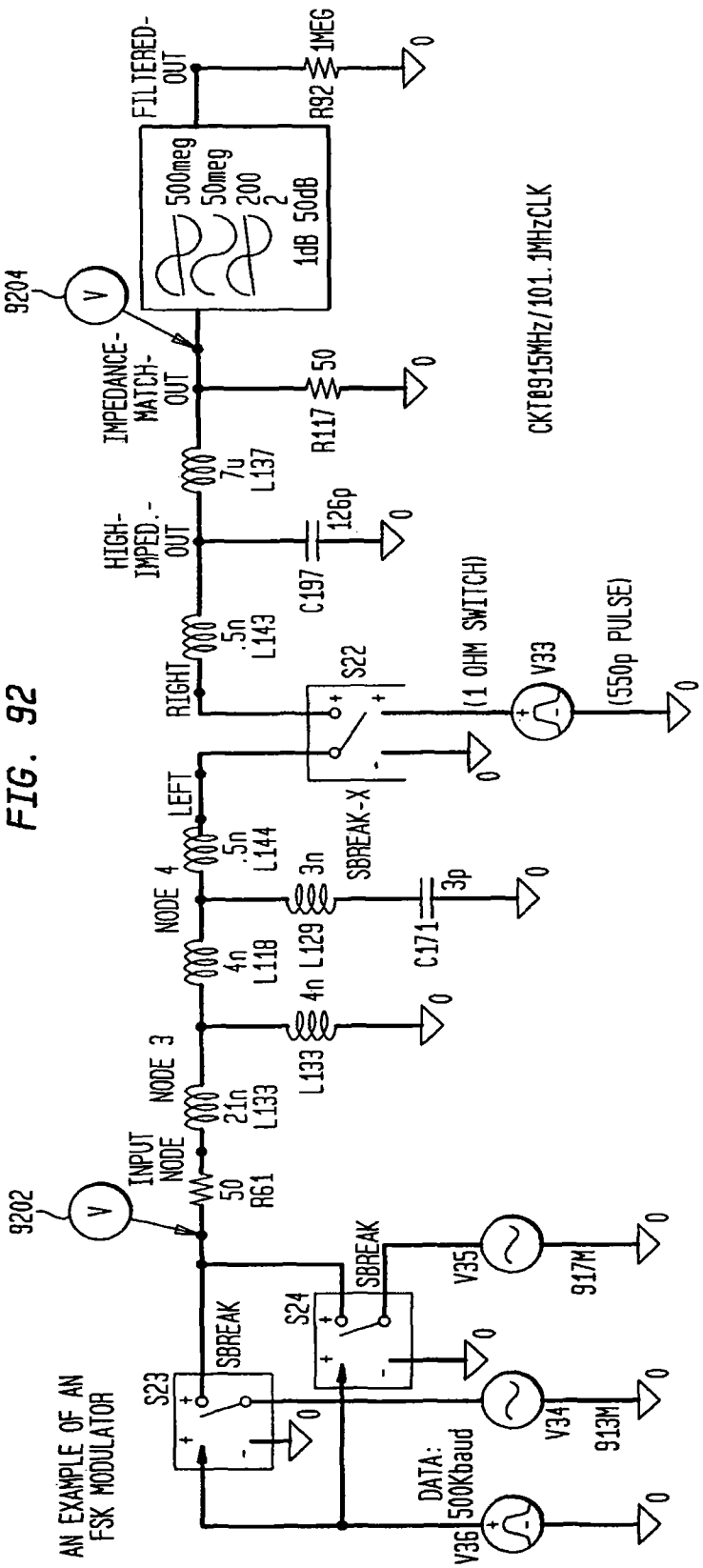

AN EXAMPLE OF AN FSK MODULATOR
9202
INPUT NODE
50 R61
21n L133
NODE 3
4n L118
NODE 4
4n L129
3n L133
.5n L144
LEFT
.5n L143
RIGHT
7u L137
IMPEDANCE-MATCH-OUT
HIGH-IMPED.-OUT
FILTERED-OUT
9204
500meg 50meg 200 2 1dB 50dB
1MEG R82
50 R117
126p C197
3p C171
SBREAK-X
S22
S23
S24
SBREAK
V33 (1 OHM SWITCH)
(550p PULSE)
V35 917M
V34 913M
V36 DATA: 500Kbaud
CKT@915MHz/101.1MHzCLK
0

FIG. 92

FIG. 93

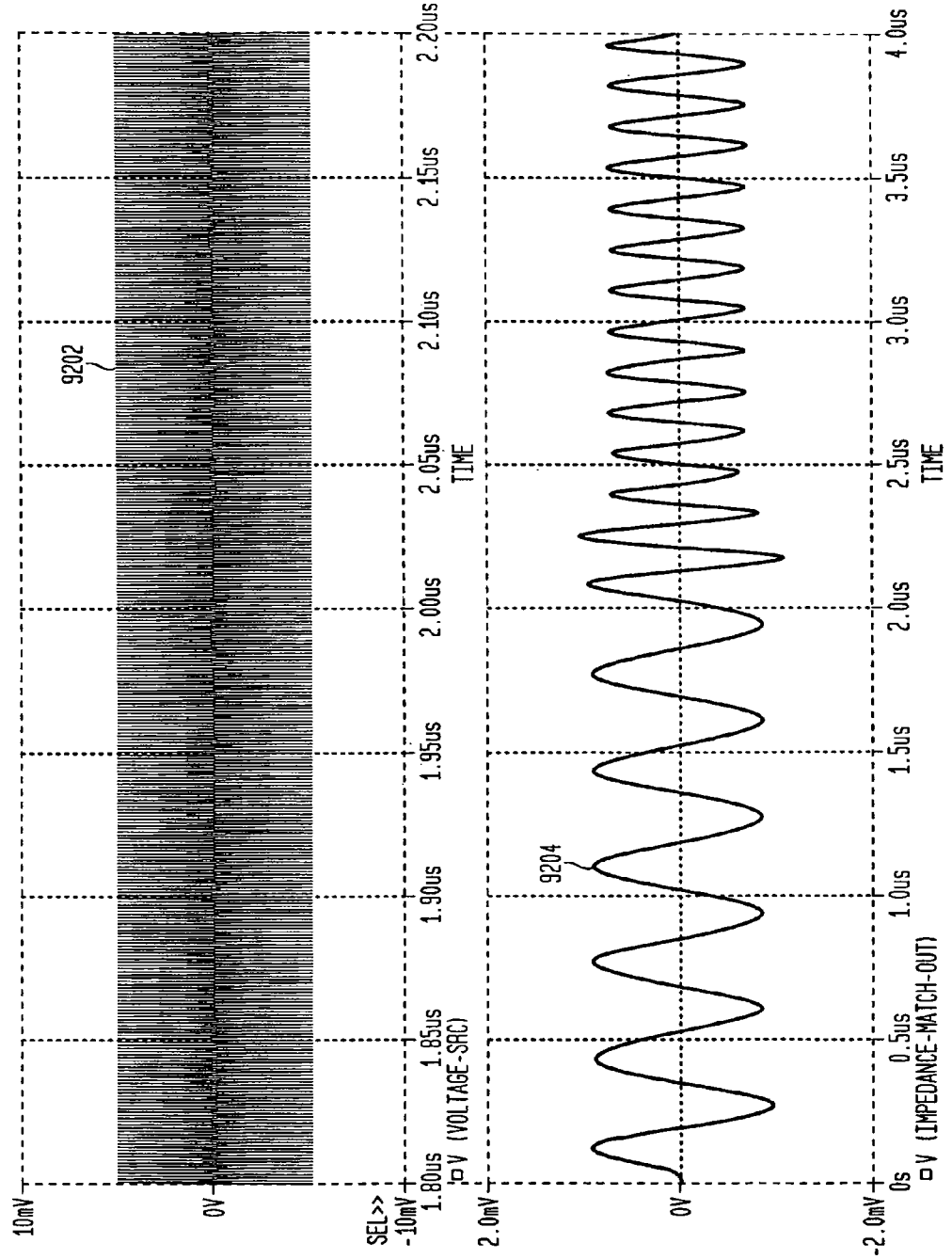
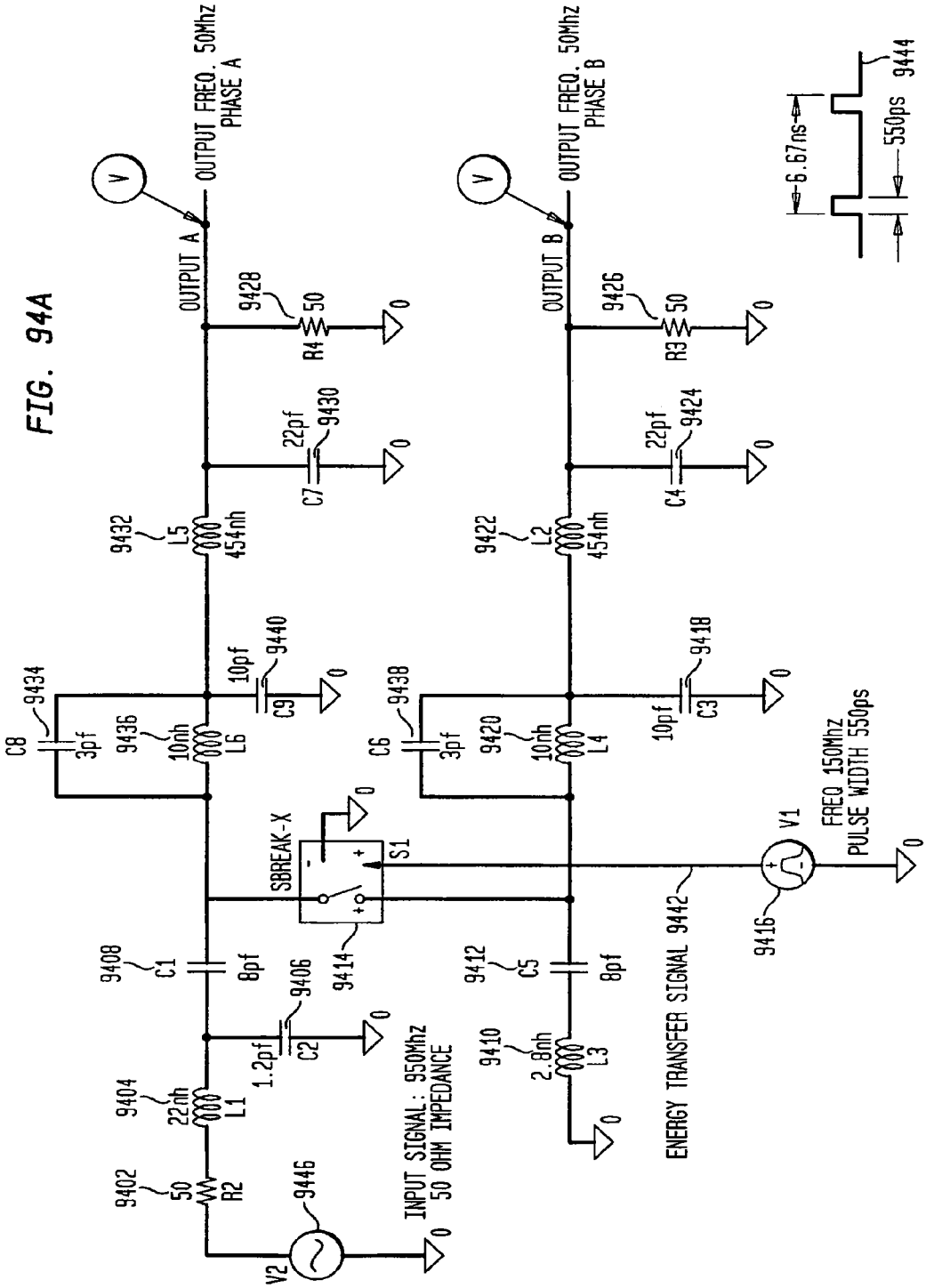

9202
9204
10mV
0V
SEL>>
-10mV
2.0mV
0V
-2.0mV
1.80us
1.85us
1.90us
1.95us
2.00us
2.05us
2.10us
2.15us
2.20us
TIME
V (VOLTAGE-SRC)
0s
0.5us
1.0us
1.5us
2.0us
2.5us
3.0us
3.5us
4.0us
TIME
V (IMPEDANCE-MATCH-OUT)

FIG. 94A


OUTPUT FREQ. 50Mhz
PHASE A
OUTPUT A
9428
R4
50
22pf
9430
C7
9432
L5
454nh
10pf
9440
C9
9434
C8
3pf
9436
10nh
L6
SBREAK-X
S1
9414
9408
C1
8pf
9406
1.2pf
C2
9404
22nh
L1
9402
R2
9446
V2
INPUT SIGNAL: 950Mhz
50 OHM IMPEDANCE
OUTPUT FREQ. 50Mhz
PHASE B
OUTPUT B
9426
R3
22pf
9424
C4
9422
L2
454nh
10pf
9418
C3
9438
C6
3pf
9420
10nh
L4
9412
C5
8pf
9410
2.8nh
L3
ENERGY TRANSFER SIGNAL 9442
9416
V1
FREQ 150Mhz
PULSE WIDTH 550ps
6.67ns
550ps
9444

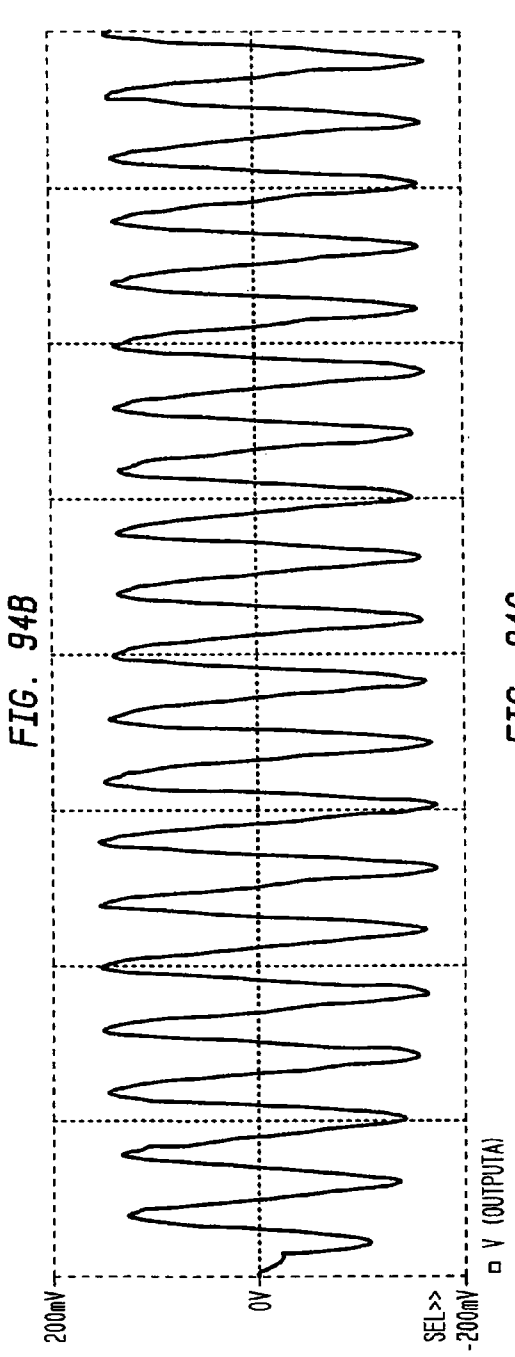


FIG. 94B

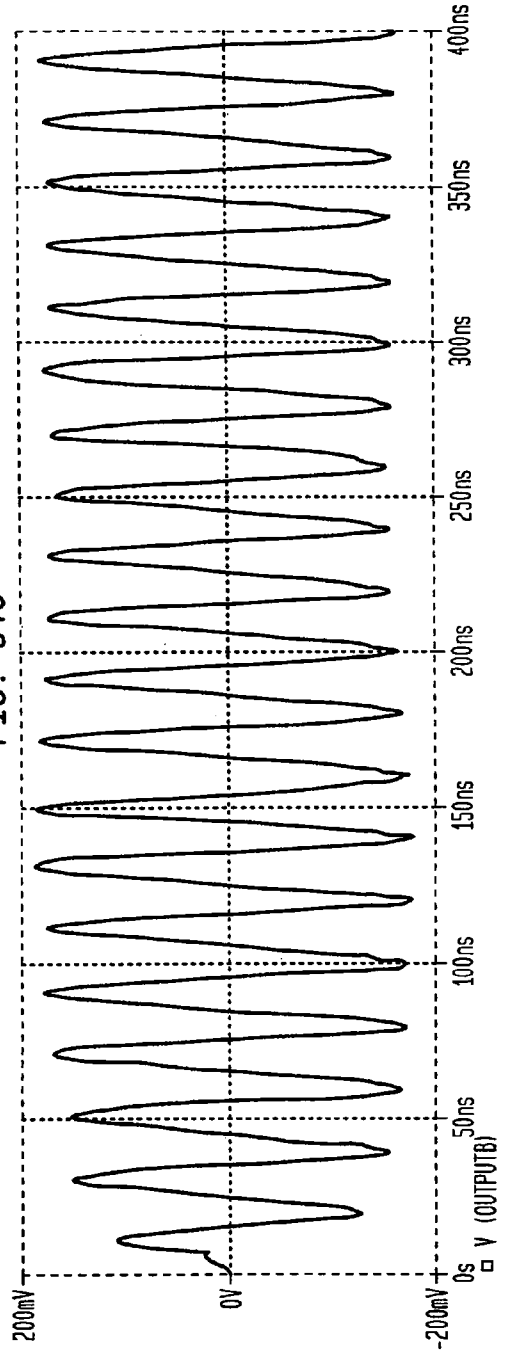


FIG. 94C

FIG. 95

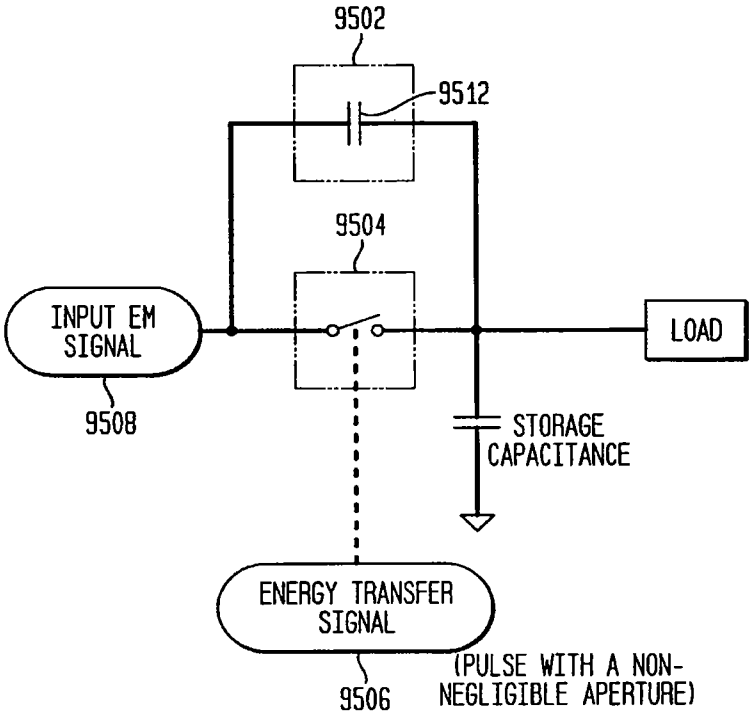

9502
9512
9504
INPUT EM SIGNAL
9508
LOAD
STORAGE CAPACITANCE
ENERGY TRANSFER SIGNAL
9506
(PULSE WITH A NON-NEGLIGIBLE APERTURE)

FIG. 96

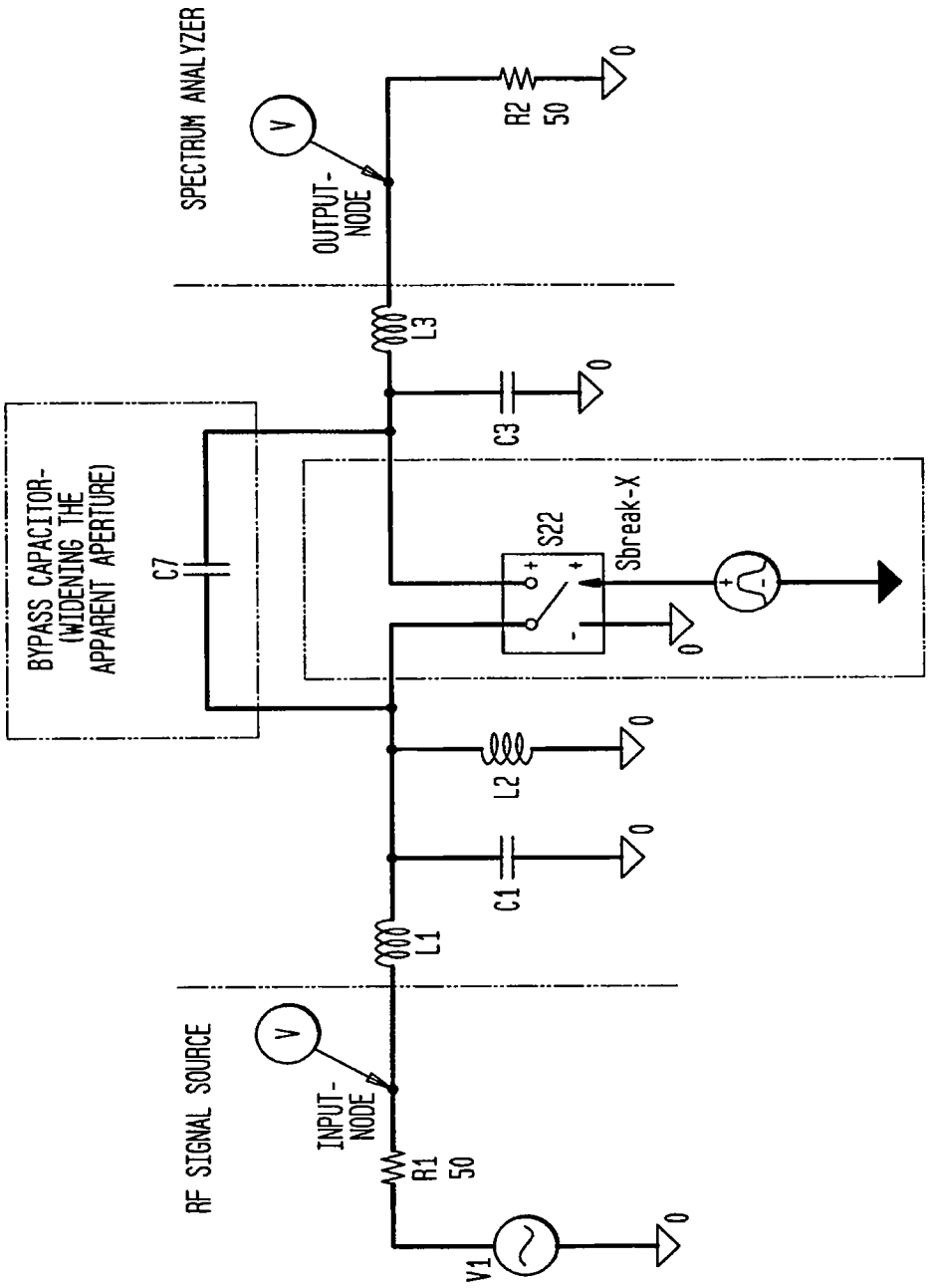

SPECTRUM ANALYZER
OUTPUT-NODE
R2
50
0
L3
C3
BYPASS CAPACITOR-(WIDENING THE APPARENT APERTURE)
C7
S22
Sbreak-X
L2
C1
L1
RF SIGNAL SOURCE
INPUT-NODE
R1
50
V1

FIG. 97

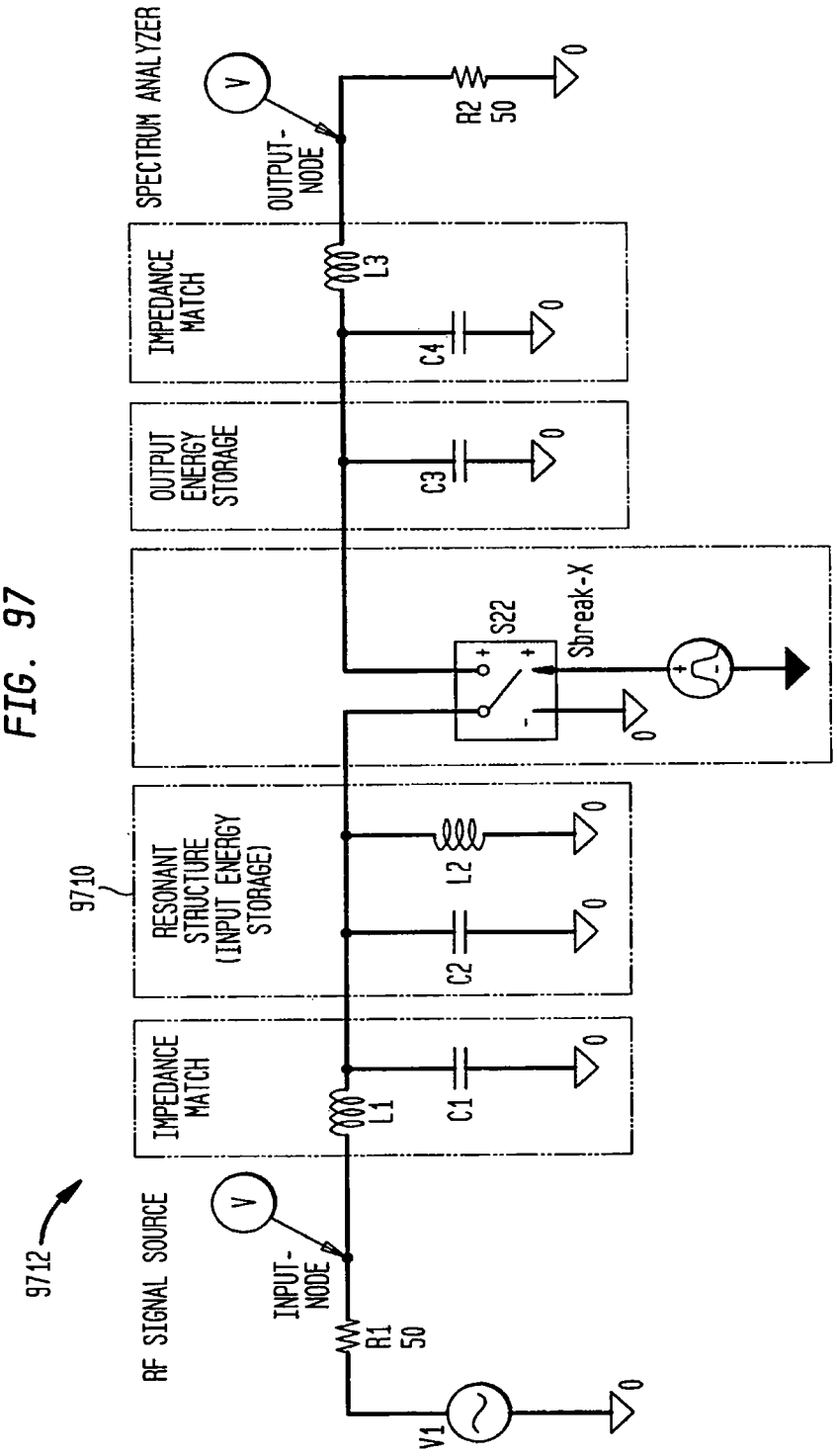
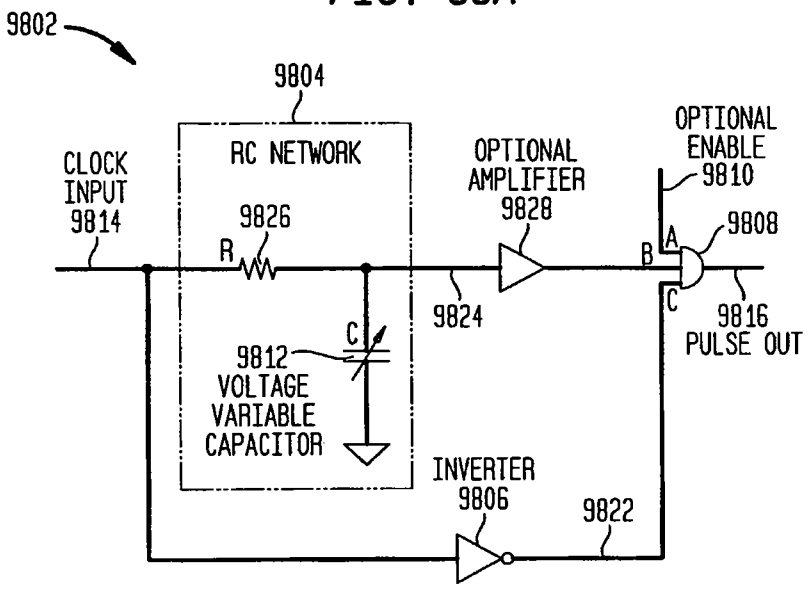

9712
RF SIGNAL SOURCE
INPUT-NODE
R1
50
V1
9710
IMPEDANCE MATCH
L1
C1
RESONANT STRUCTURE (INPUT ENERGY STORAGE)
L2
C2
OUTPUT ENERGY STORAGE
C3
IMPEDANCE MATCH
L3
C4
SPECTRUM ANALYZER
OUTPUT-NODE
R2
50
S22
Sbreak-X
0

FIG. 98A


9802
9804
RC NETWORK
CLOCK INPUT 9814
9826
R
C
9812 VOLTAGE VARIABLE CAPACITOR
OPTIONAL AMPLIFIER 9828
9824
OPTIONAL ENABLE 9810
9808
A
B
C
9816 PULSE OUT
INVERTER 9806
9822

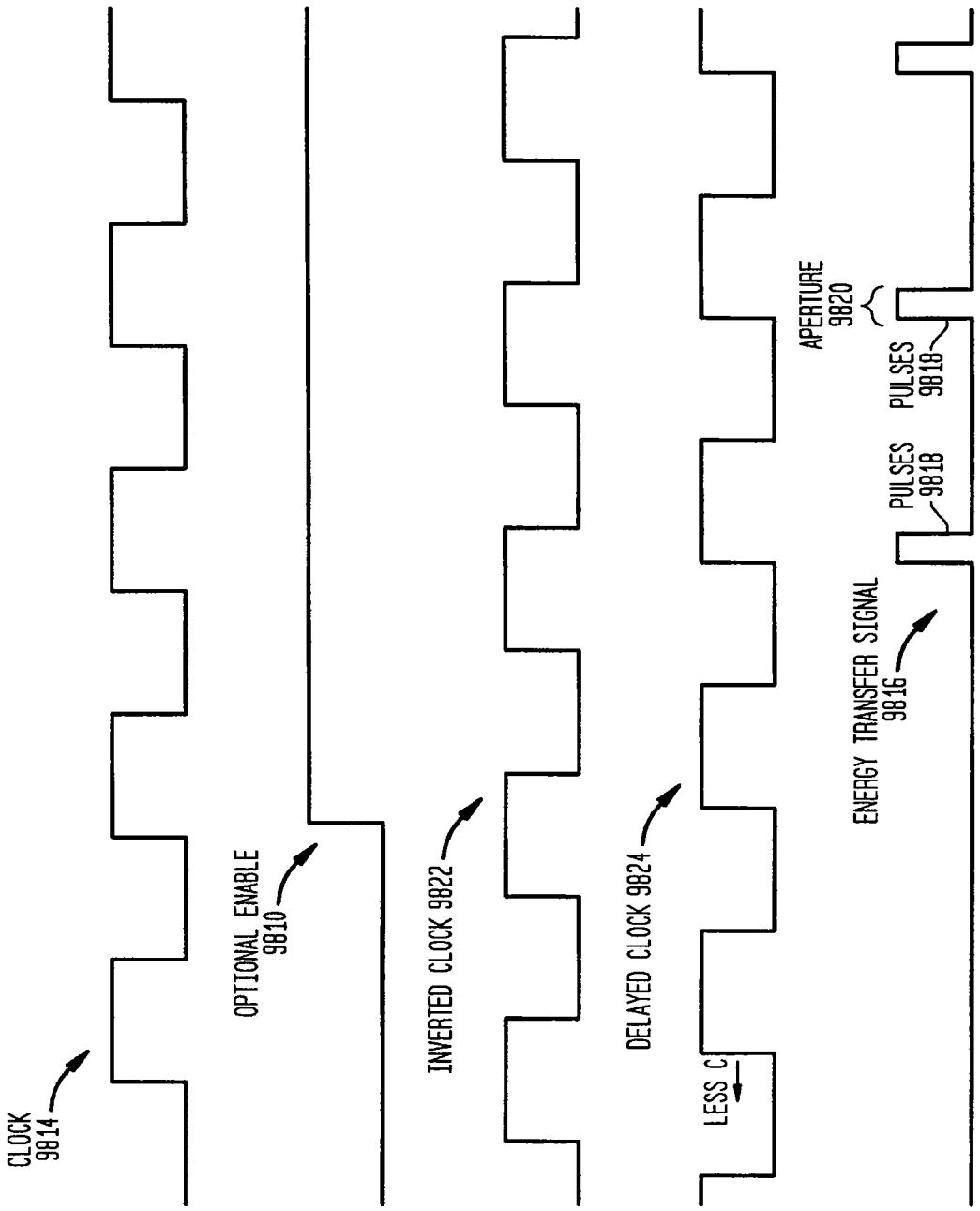


FIG. 98B FIG. 98C FIG. 98D FIG. 98E FIG. 98F

FIG. 99

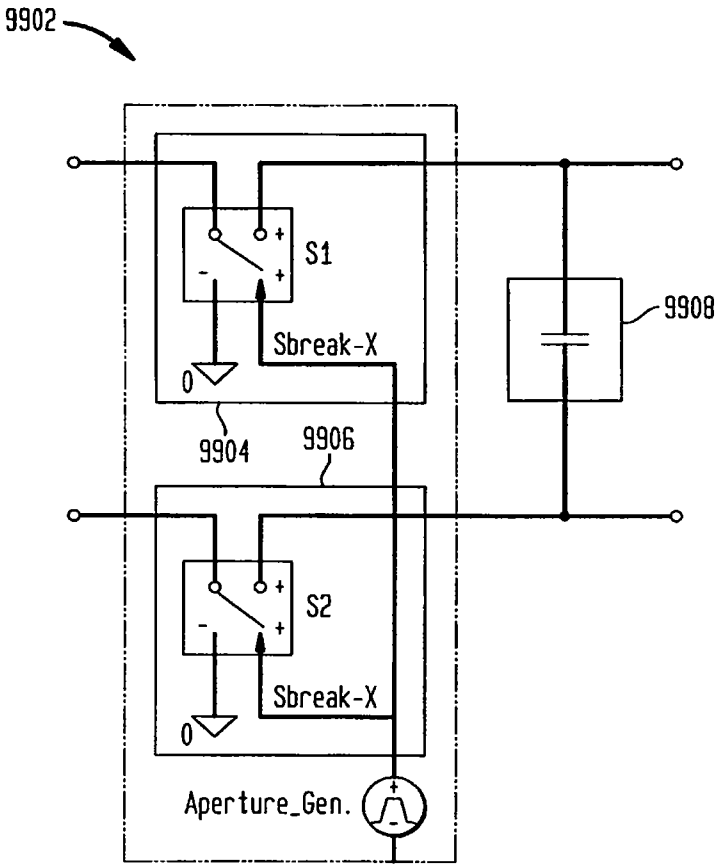


FIG. 100

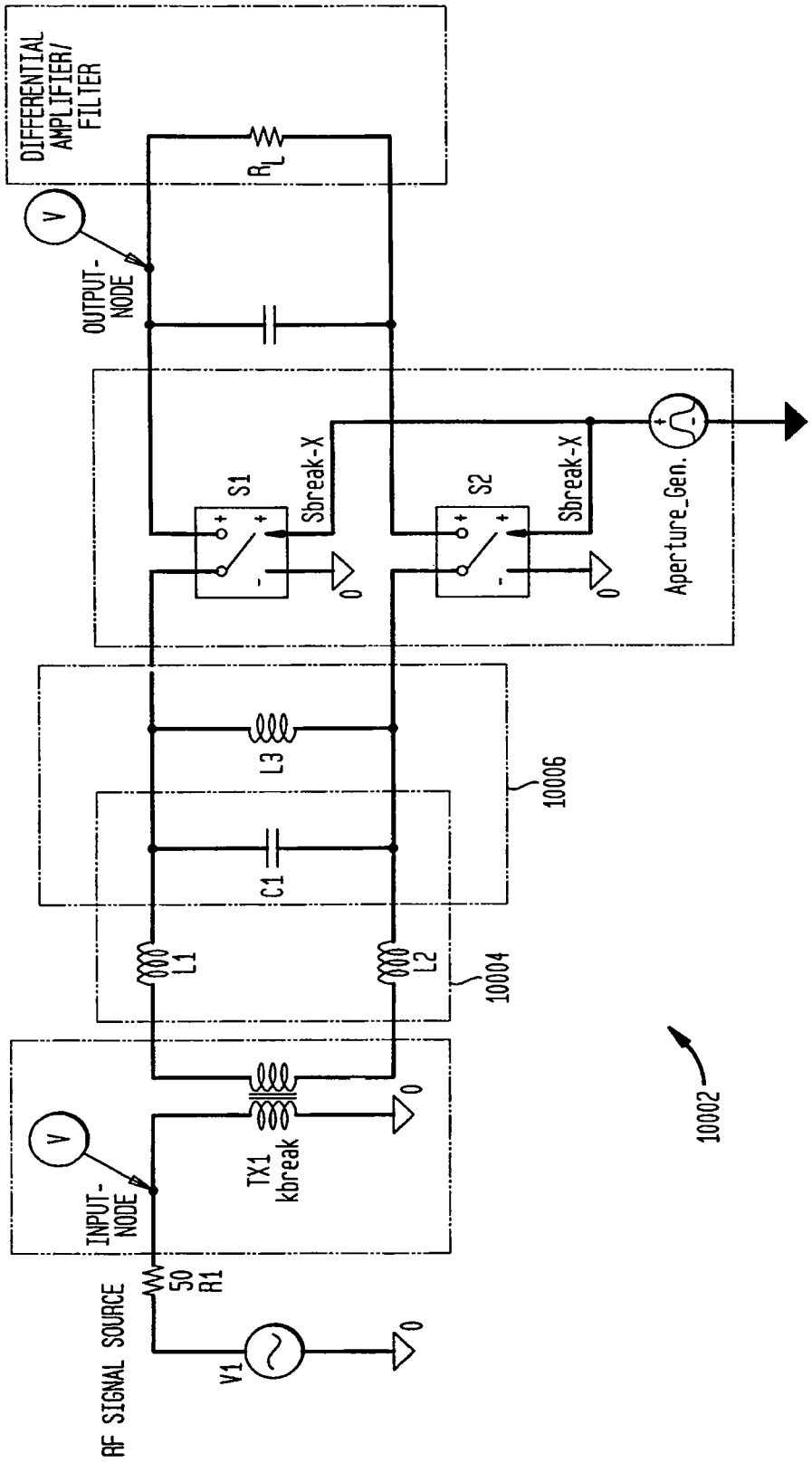
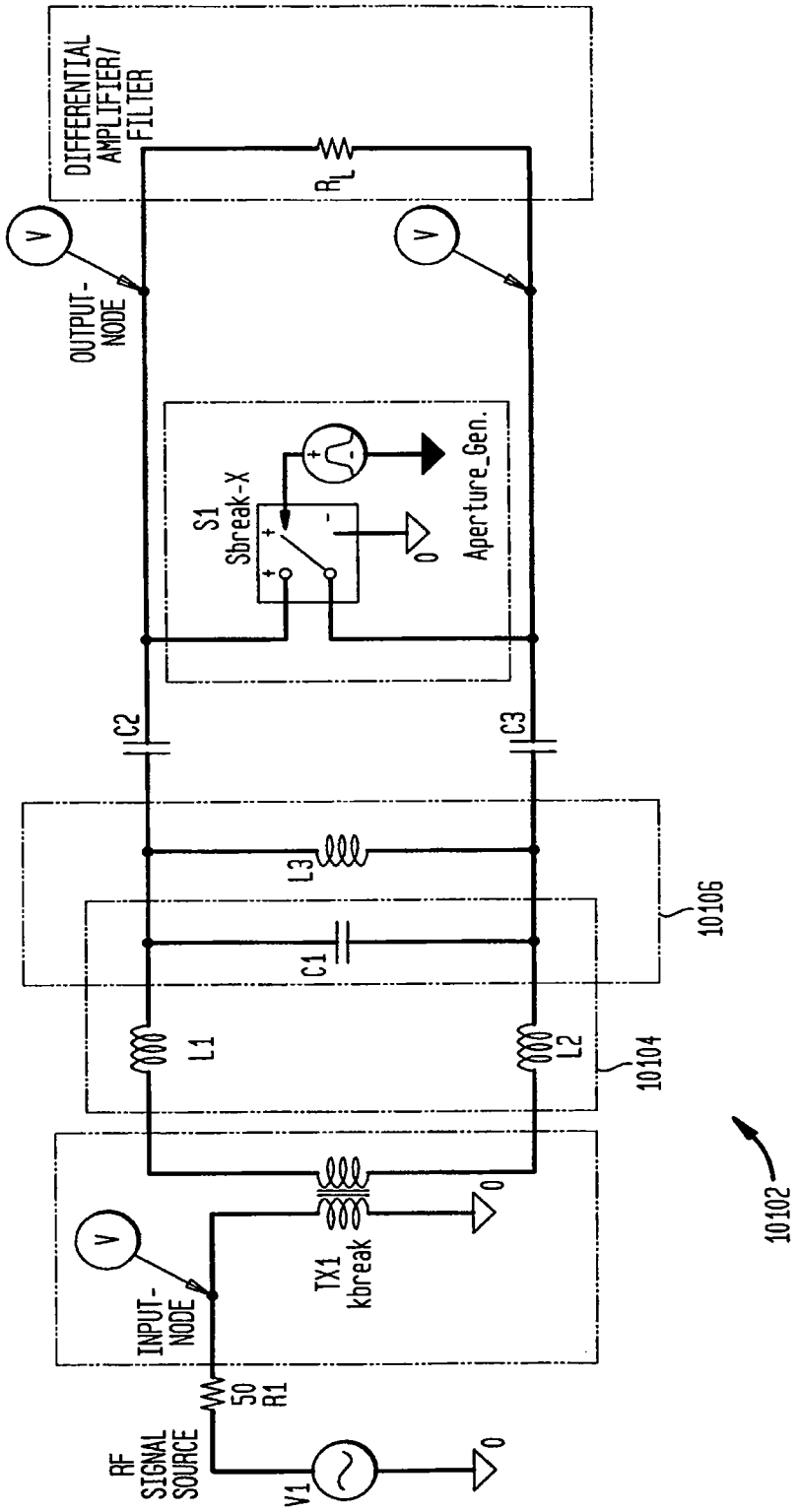

DIFFERENTIAL AMPLIFIER/ FILTER
R_L
V
OUTPUT-NODE
S1
Sbreak-X
S2
Sbreak-X
Aperture_Gen.
0
L3
C1
10006
L1
L2
10004
TX1
kbreak
INPUT-NODE
50
R1
RF SIGNAL SOURCE
V1
10002

FIG. 101


DIFFERENTIAL AMPLIFIER/ FILTER
R_L
V
OUTPUT-NODE
S1
Sbreak-X
Aperture_Gen.
0
C2
C3
L3
C1
L1
L2
10106
10104
10102
TX1
kbreak
INPUT-NODE
50
R1
RF SIGNAL SOURCE
V1

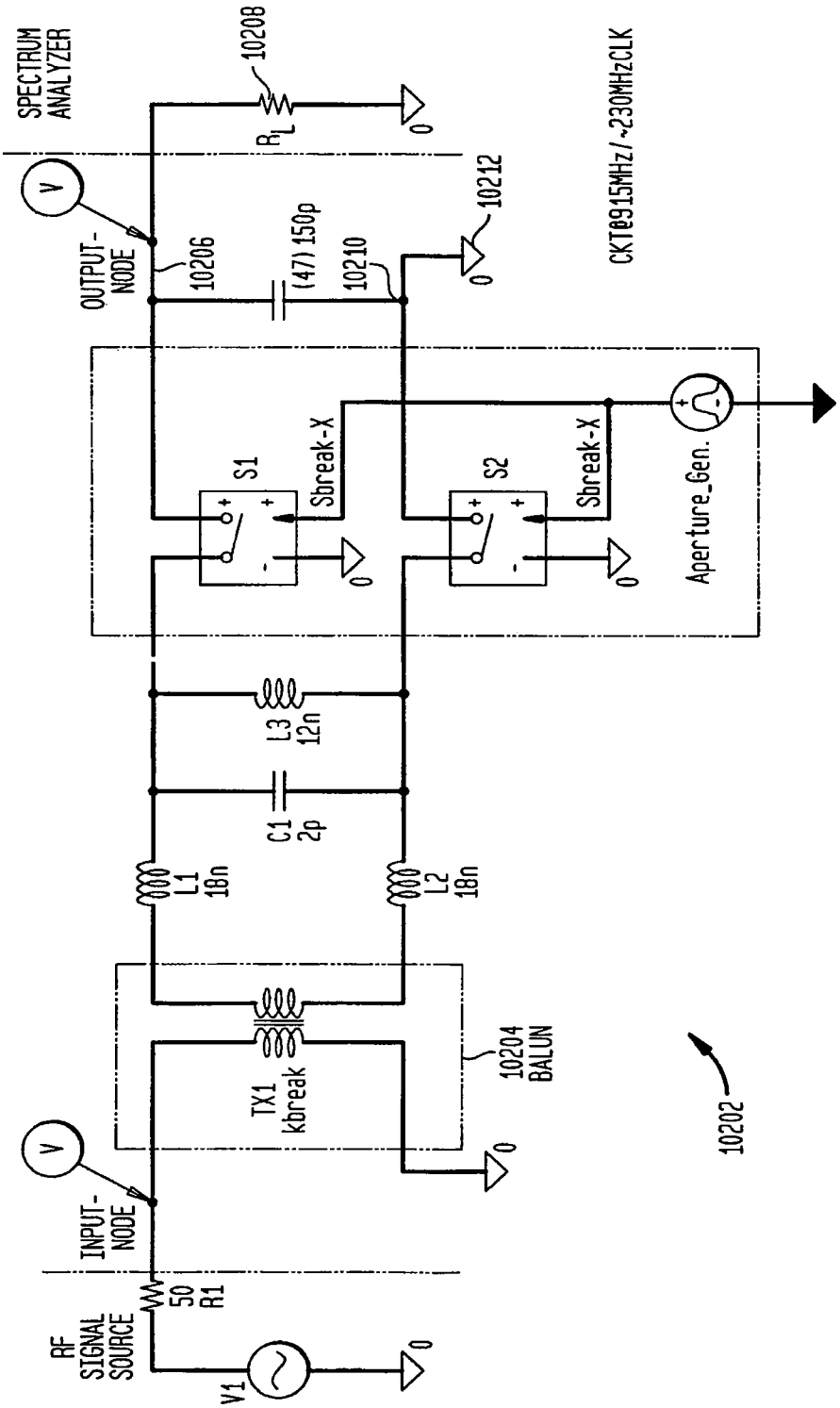

SPECTRUM ANALYZER
10208
R_L
0
10212
CKT@915MHz/~230MHzCLK
OUTPUT-NODE
10206
(47) 150p
10210
S1
Sbreak-X
S2
Sbreak-X
Aperture_Gen.
L3 12n
C1 2p
L1 18n
L2 18n
TX1 kbreak
10204 BALUN
10202
INPUT-NODE
RF SIGNAL SOURCE
50 R1
V1

FIG. 102

FIG. 103

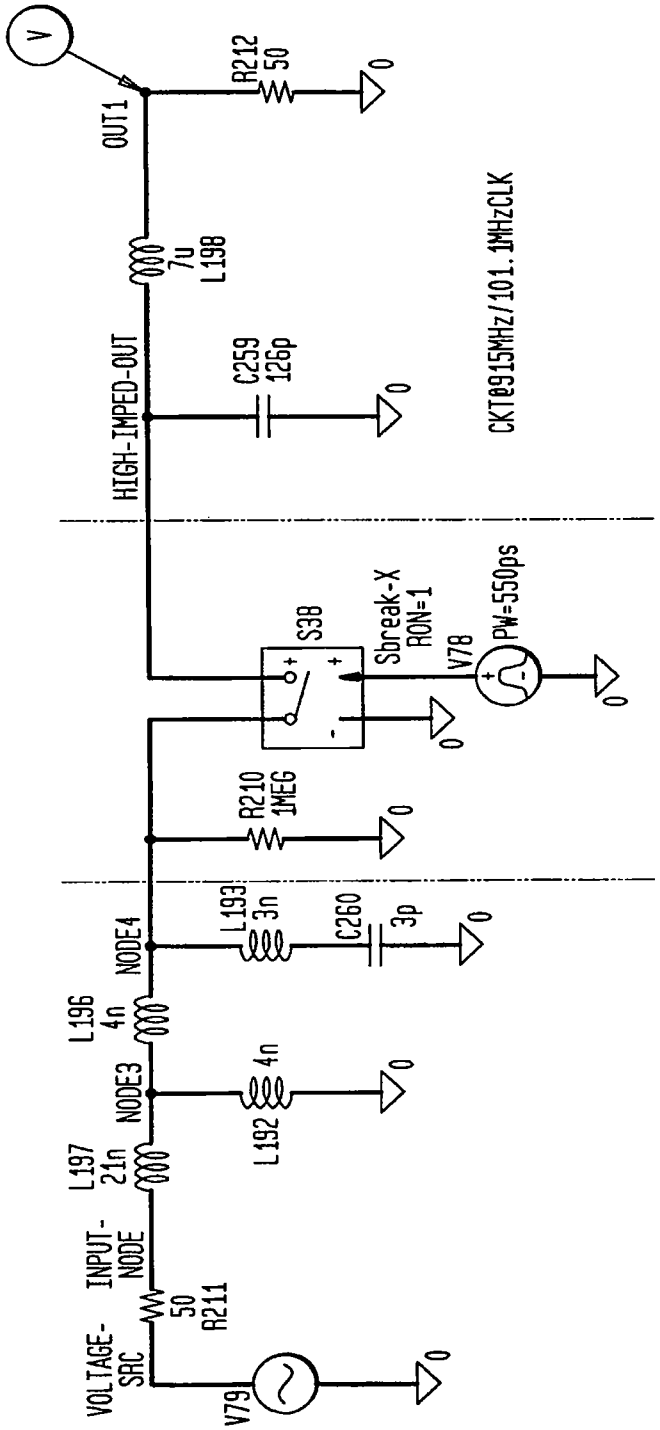
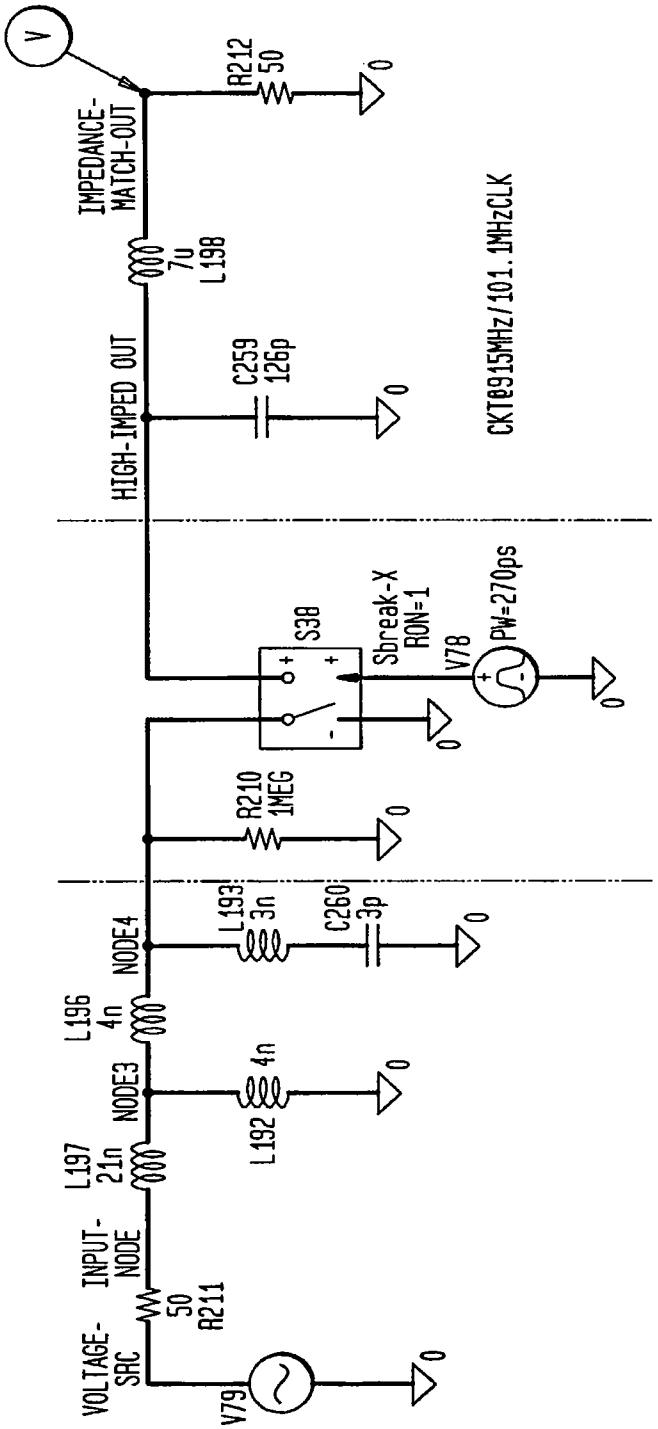

V
OUT1
R212
50
0
L198
7u
HIGH-IMPED-OUT
C259
126p
0
CKT0915MHz/101.1MHzCLK
S38
Sbreak-X
RON=1
V78
PW=550ps
0
0
R210
1MEG
0
L193
3n
NODE4
C260
3p
0
L196
4n
NODE3
4n
L192
0
L197
21n
INPUT-
NODE
50
R211
VOLTAGE-
SRC
V79
0

FIG. 104


V
R212
50
0
IMPEDANCE-MATCH-OUT
7u
L198
HIGH-IMPED OUT
C259
126p
0
CKT@915MHz/101.1MHzCLK
S38
Sbreak-X
RON=1
V78
PW=270ps
0
0
R210
1MEG
0
L193
3n
C260
3p
0
NODE4
L196
4n
NODE3
4n
L192
0
L197
21n
INPUT-NODE
50
R211
VOLTAGE-SRC
V79
0

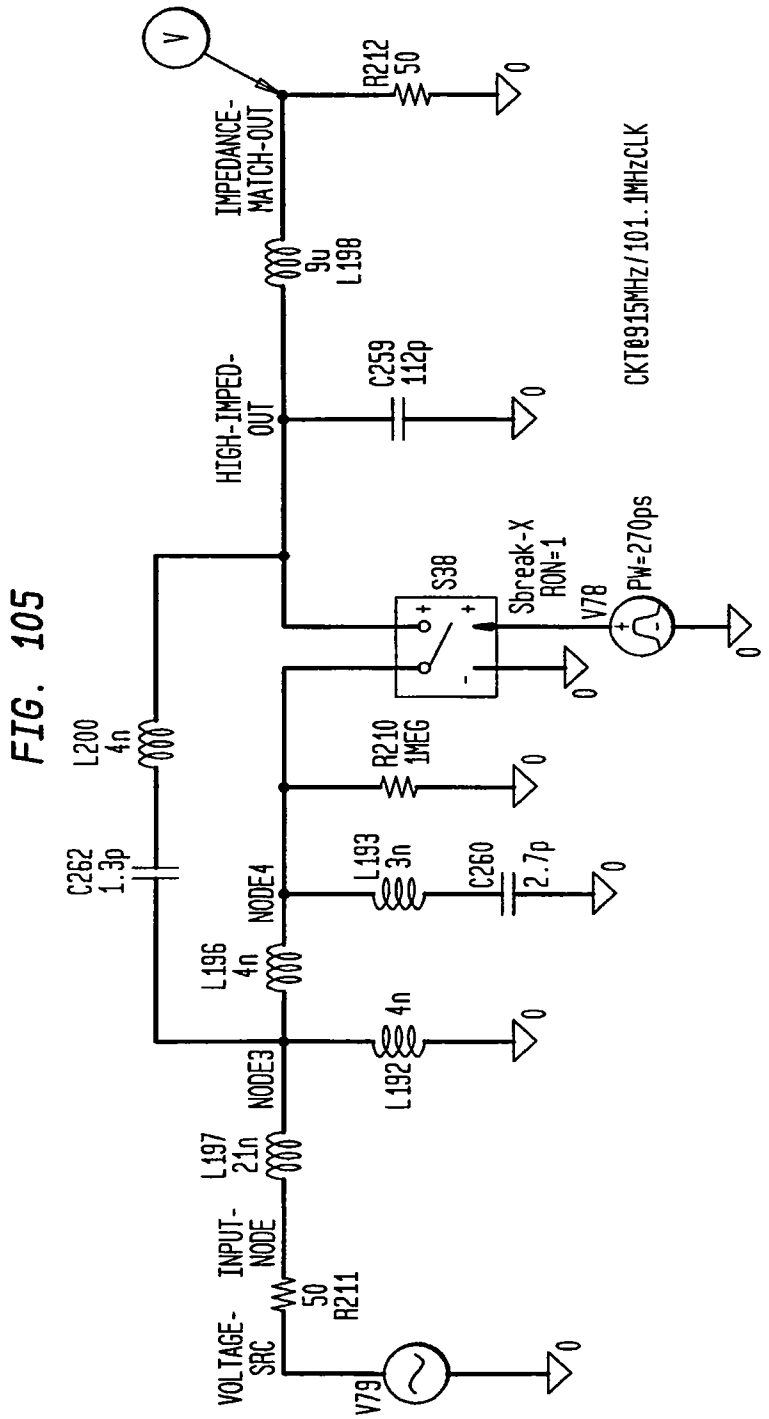
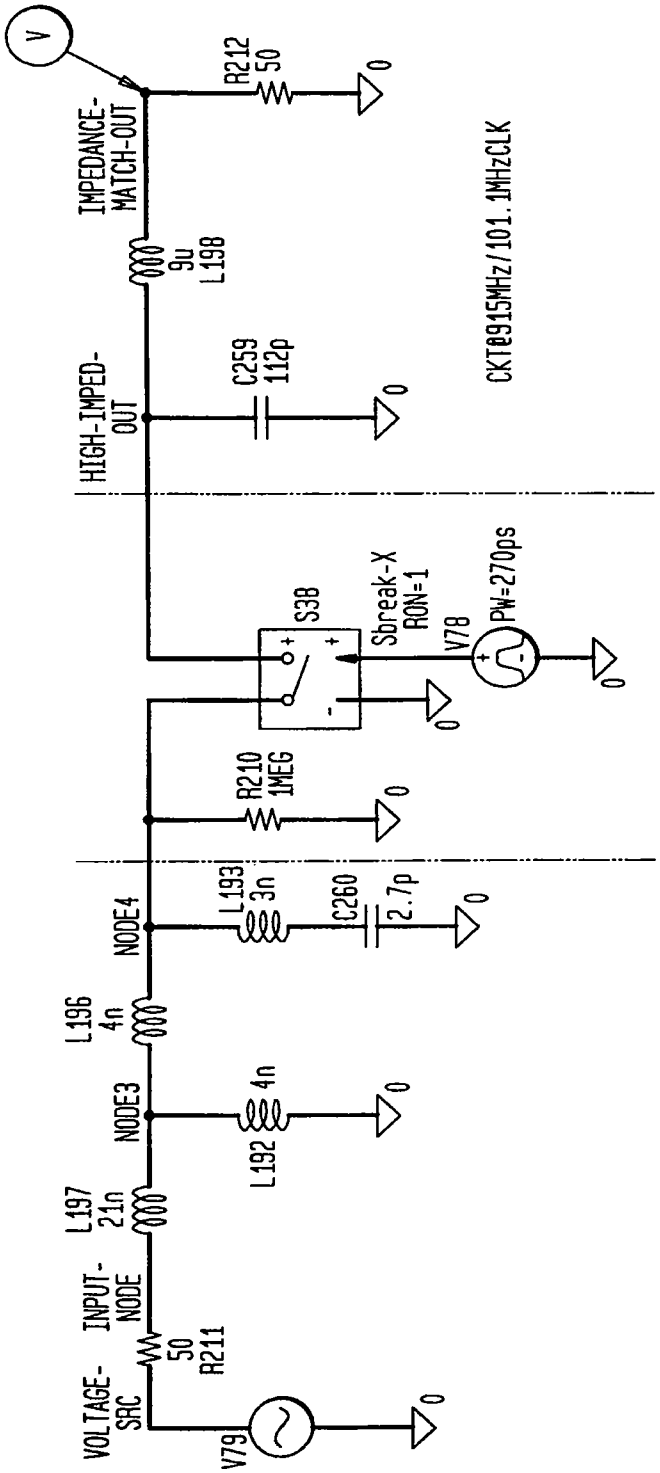

V
IMPEDANCE-MATCH-OUT
R212 50
0
9u L198
HIGH-IMPED-OUT
C259 112p
0
CKT@915MHz/101.1MHzCLK
S38
Sbreak-X RON=1
V78 PW=270ps
0
0
L200 4n
R210 1MEG
0
C262 1.3p
NODE4
L193 3n
C260 2.7p
0
L196 4n
4n
0
NODE3
L192
L197 21n
INPUT-NODE
50 R211
VOLTAGE-SRC
V79
0

FIG. 105

FIG. 106


V
R212
50
0
IMPEDANCE-
MATCH-OUT
9u
L198
HIGH-IMPED-
OUT
C259
112p
0
CKT@915MHz/101.1MHzCLK
S38
Sbreak-X
RON=1
V78
PW=270ps
0
0
R210
1MEG
0
L193
3n
C260
2.7p
0
NODE4
L196
4n
NODE3
4n
L192
0
L197
21n
INPUT-
NODE
50
R211
VOLTAGE-
SRC
V79
0

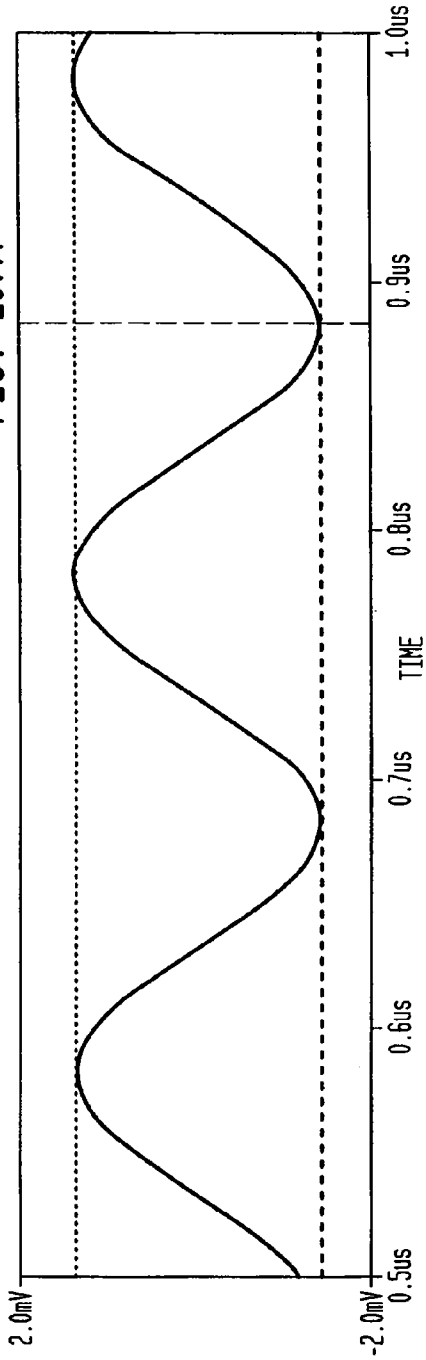


FIG. 107A

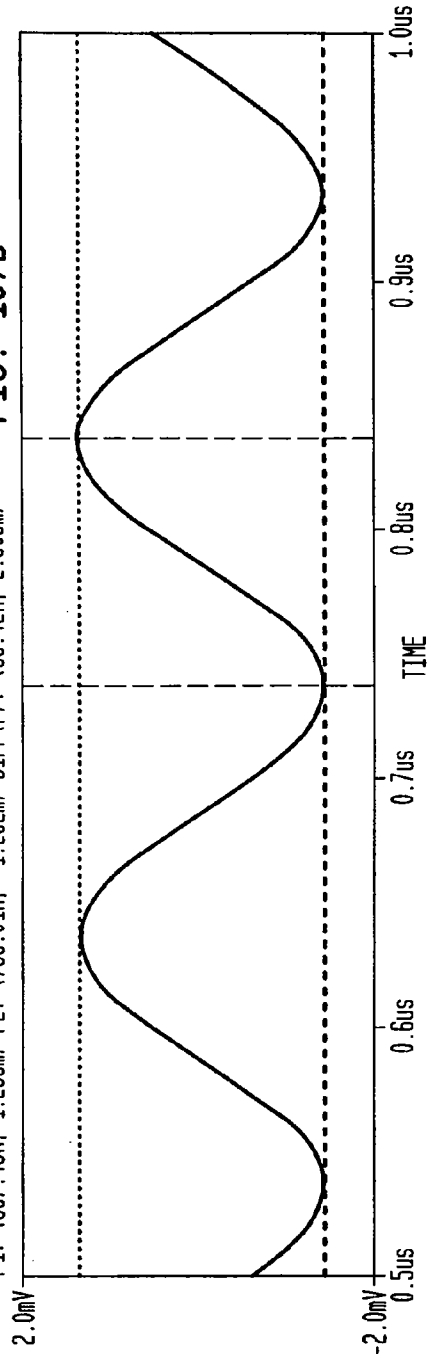


FIG. 107B

FIG. 108A

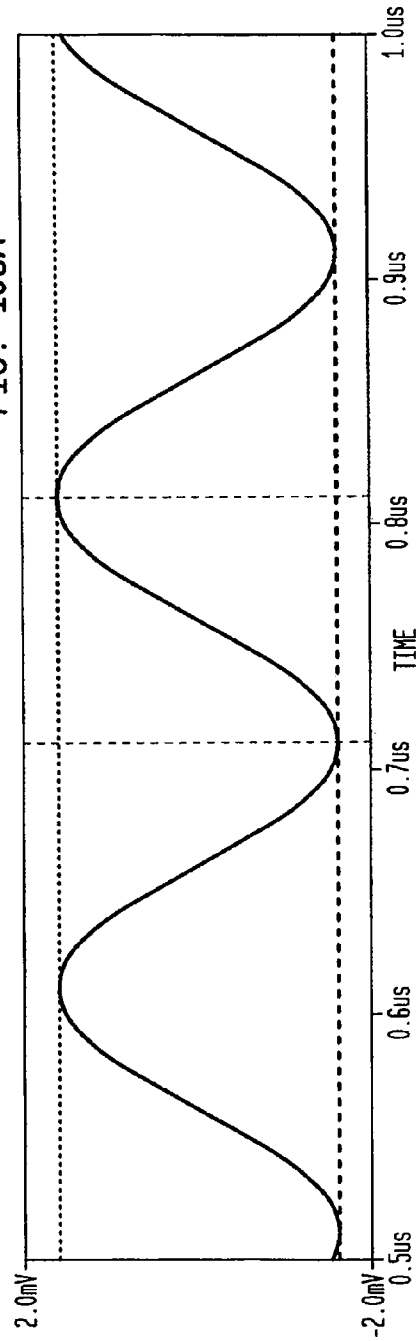


FIG. 108B

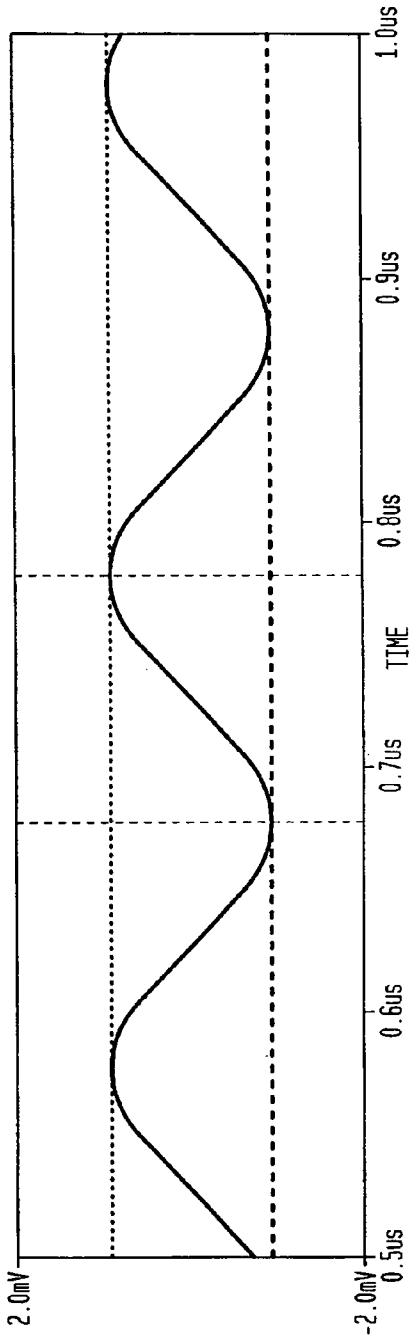


FIG. 109A

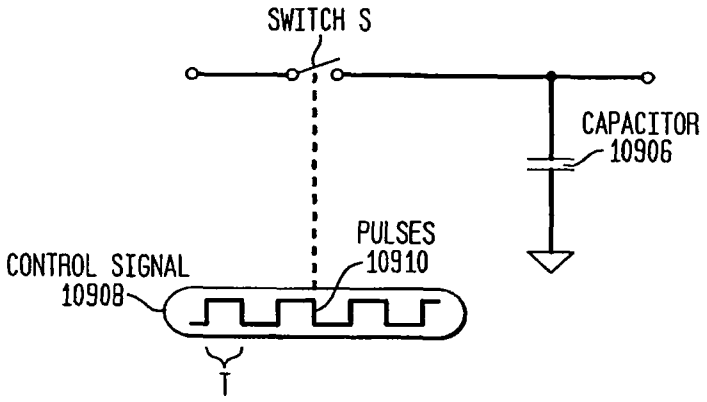


FIG. 109B

$$q=C\cdot V \qquad \text{EQ. 10}$$

$$V=A\cdot\sin(t) \qquad \text{EQ. 11}$$

$$q(t)=C\cdot A\cdot\sin(t) \qquad \text{EQ. 12}$$

$$\Delta q(t)=C\cdot A\cdot\sin(t)-C\cdot A\cdot\sin(t-T) \qquad \text{EQ. 13}$$

$$\Delta q(t)=C\cdot A\cdot(\sin(t)-\sin(t-T)) \qquad \text{EQ. 14}$$

$$\sin(\alpha)-\sin(\beta)=2\cdot\sin\left(\frac{\alpha-\beta}{2}\right)\cdot\cos\left(\frac{\alpha+\beta}{2}\right) \qquad \text{EQ. 15}$$

$$\Delta q(t)=2\cdot C\cdot A\cdot\sin\left[\frac{t-(t-T)}{2}\right]\cdot\cos\left[\frac{t+(t-T)}{2}\right] \qquad \text{EQ. 16}$$

$$\Delta q(t)=2\cdot C\cdot A\cdot\sin\left(\frac{1}{2}\cdot T\right)\cdot\cos\left(t-\frac{1}{2}\cdot T\right) \qquad \text{EQ. 17}$$

$$q(t)=\int_{\cdot}^{\cdot} C\cdot A\cdot(\sin(t)-\sin(t-T))\,dt \qquad \text{EQ. 18}$$

$$q(t)=-\cos(t)\cdot C\cdot A+\cos(t-T)\cdot C\cdot A \qquad \text{EQ. 19}$$

$$q(t)=C\cdot A\cdot(\cos(t-T)-\cos(t)) \qquad \text{EQ. 20}$$

FIG. 109C

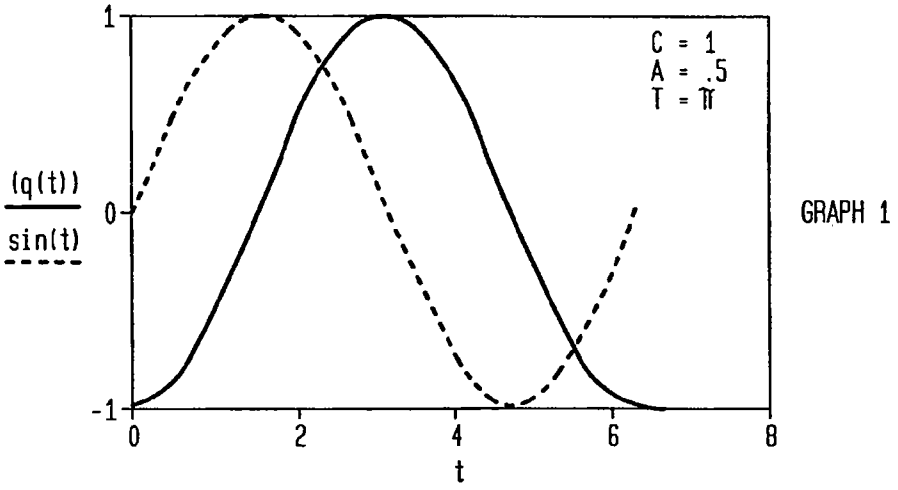


FIG. 109D

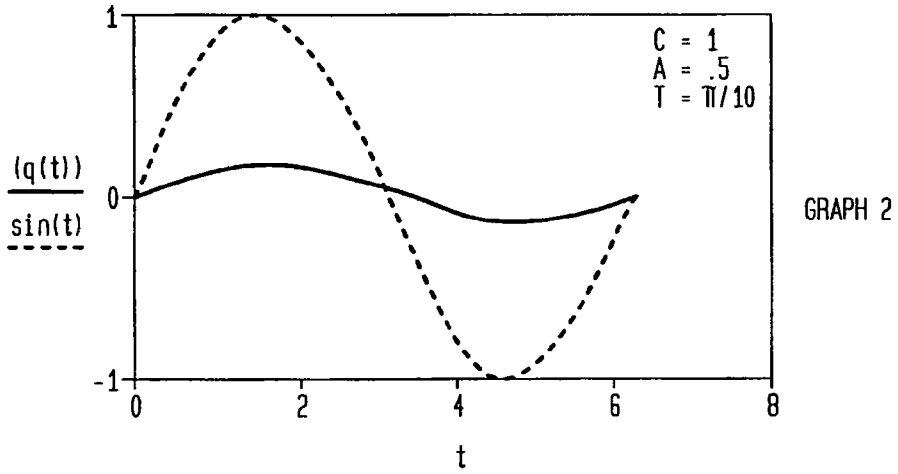


FIG. 109E

POWER-CHARGE RELATIONSHIP

$q=C \cdot V$	EQ. 21
$V=q/C$	EQ. 22
$V=J/C$	EQ. 23
$J=q^2/C$	EQ. 24
$P=J/S$	EQ. 25
$P=\frac{q^2}{C \cdot S}$	EQ. 26

FIG. 109F

INSERTION LOSS

INSERTION LOSS IN dB IS EXPRESSED BY:

$$ILdB=10 \cdot \log\left(\frac{Pin}{Pout}\right) \text{ or}$$

$$ILdB=10 \cdot \log\left[\frac{\left(\frac{Vin^2}{Rin}\right)}{\left(\frac{Vout^2}{Rout}\right)}\right]$$

FIG. 110A

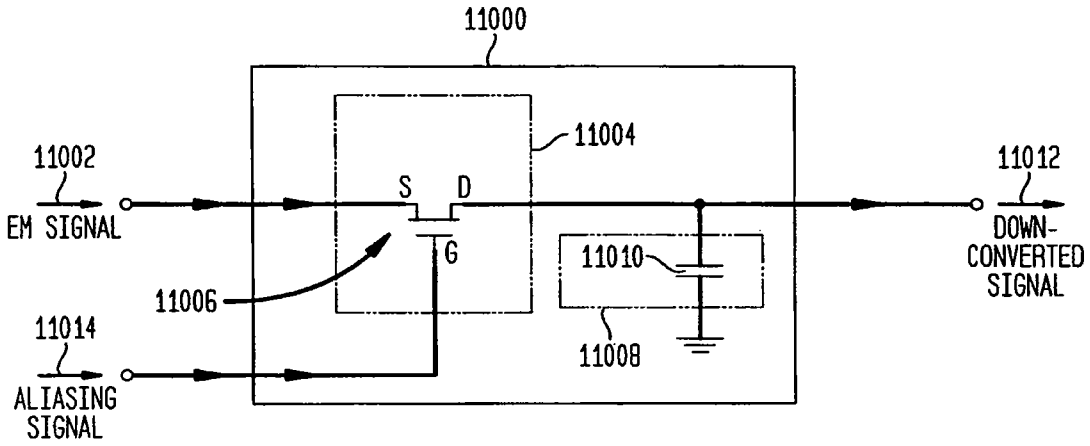
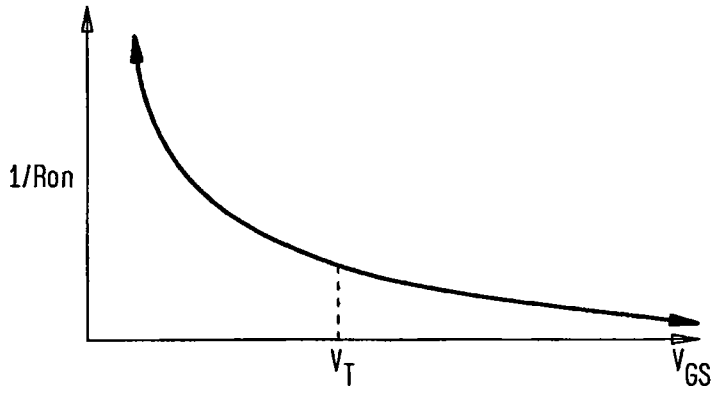


FIG. 110B



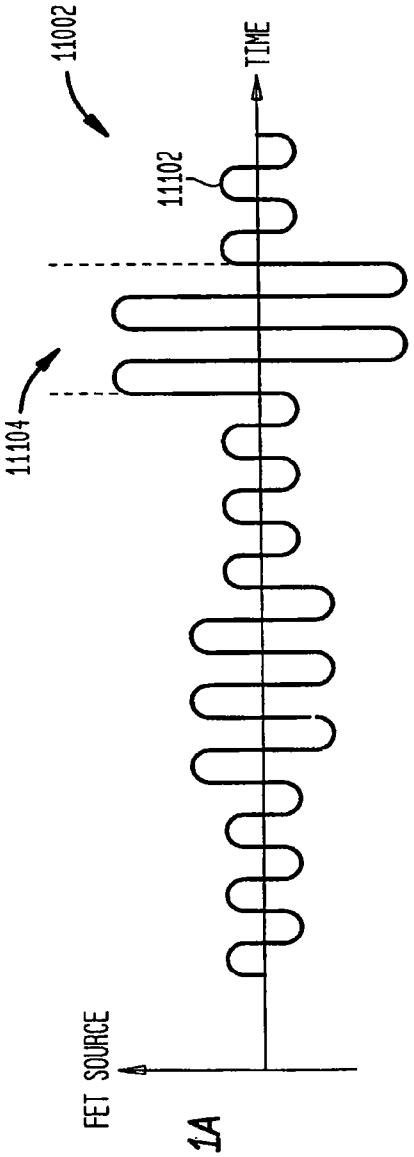


FIG. 111A

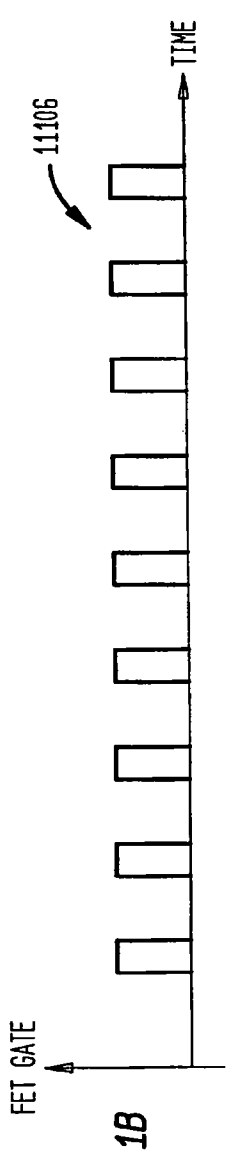


FIG. 111B

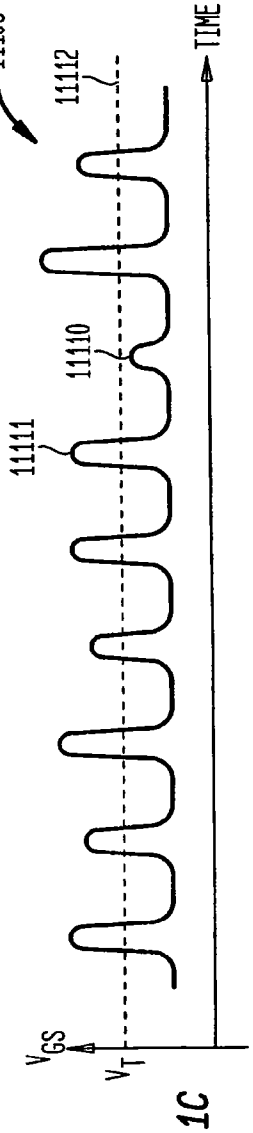


FIG. 111C

FIG. 112

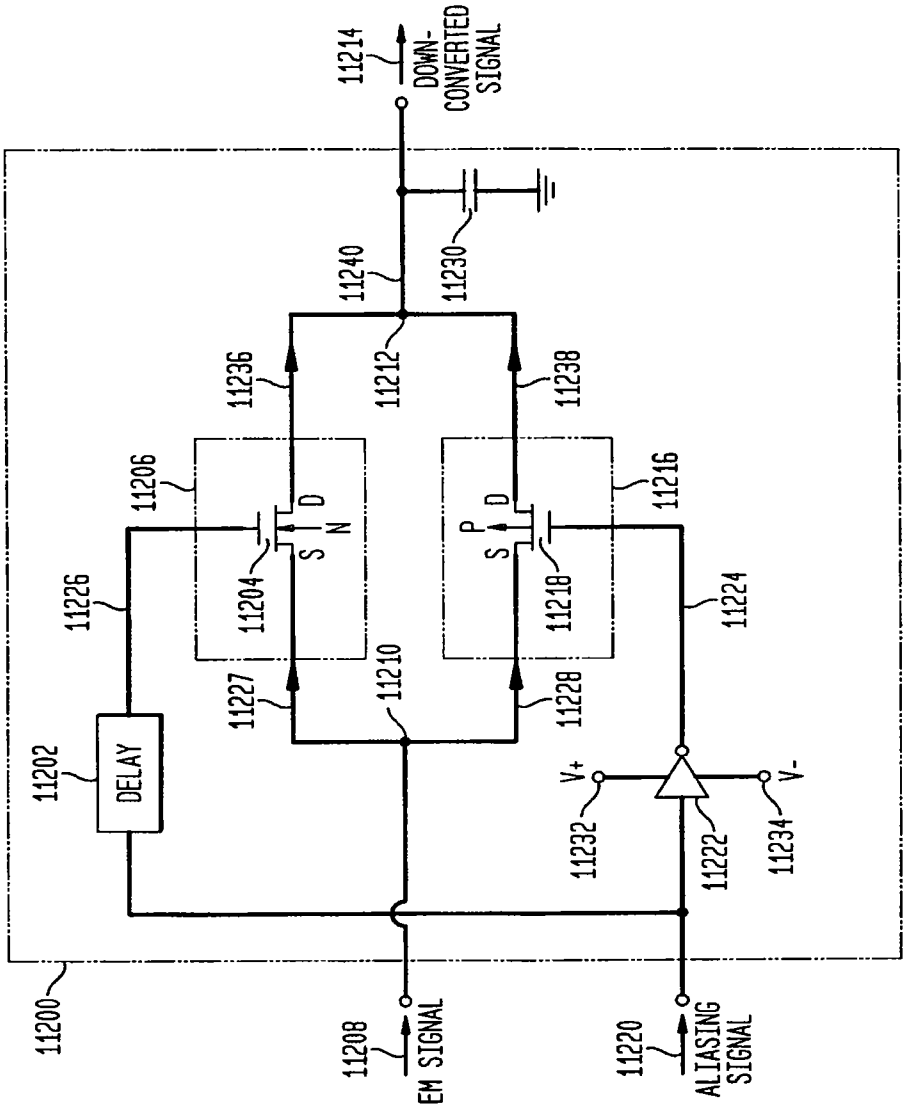

11214
DOWN-CONVERTED SIGNAL
11230
11240
11212
11236
11238
11206
11216
D
S
N
P
11204
11218
11226
11224
11227
11210
11228
11202
DELAY
V+
V-
11232
11222
11234
11200
11208
EM SIGNAL
11220
ALIASING SIGNAL

FIG. 113A

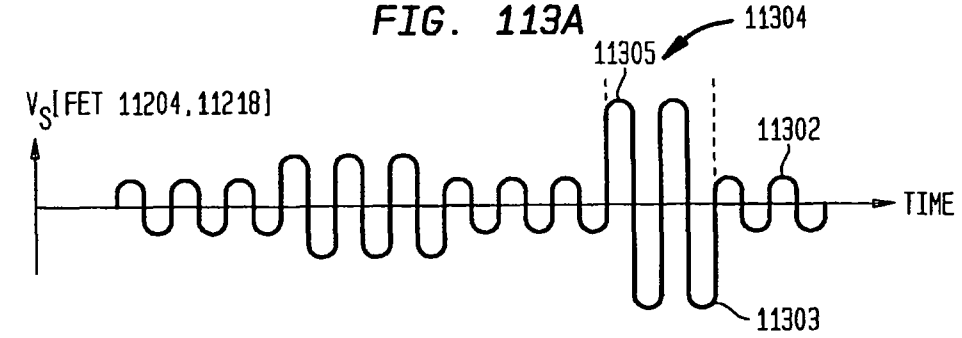


FIG. 113B

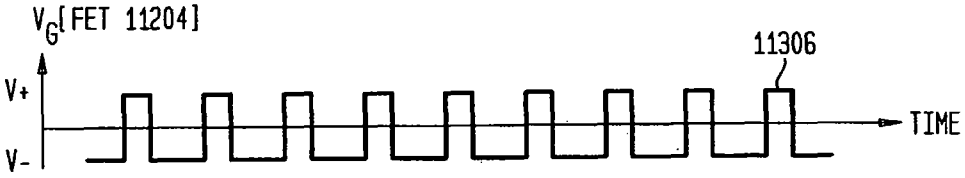


FIG. 113C

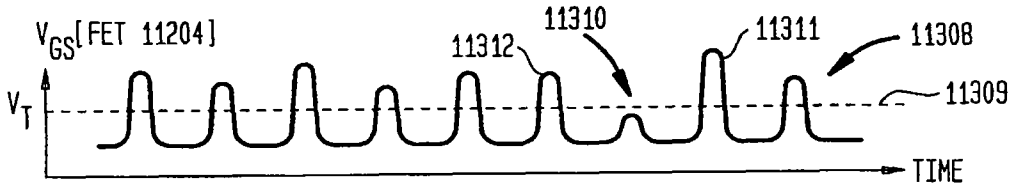


FIG. 113D

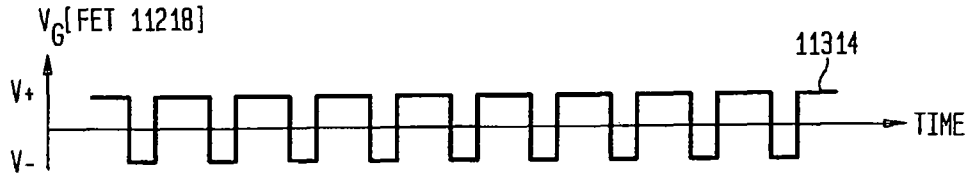


FIG. 113E

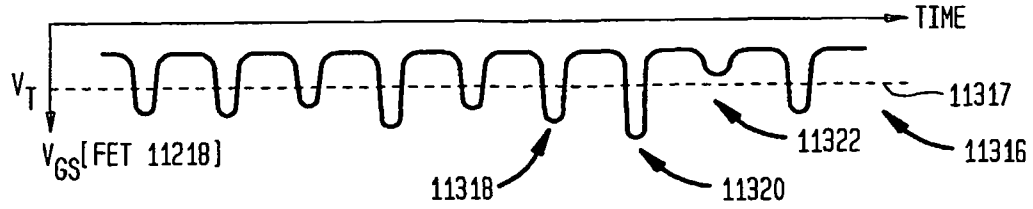


FIG. 114

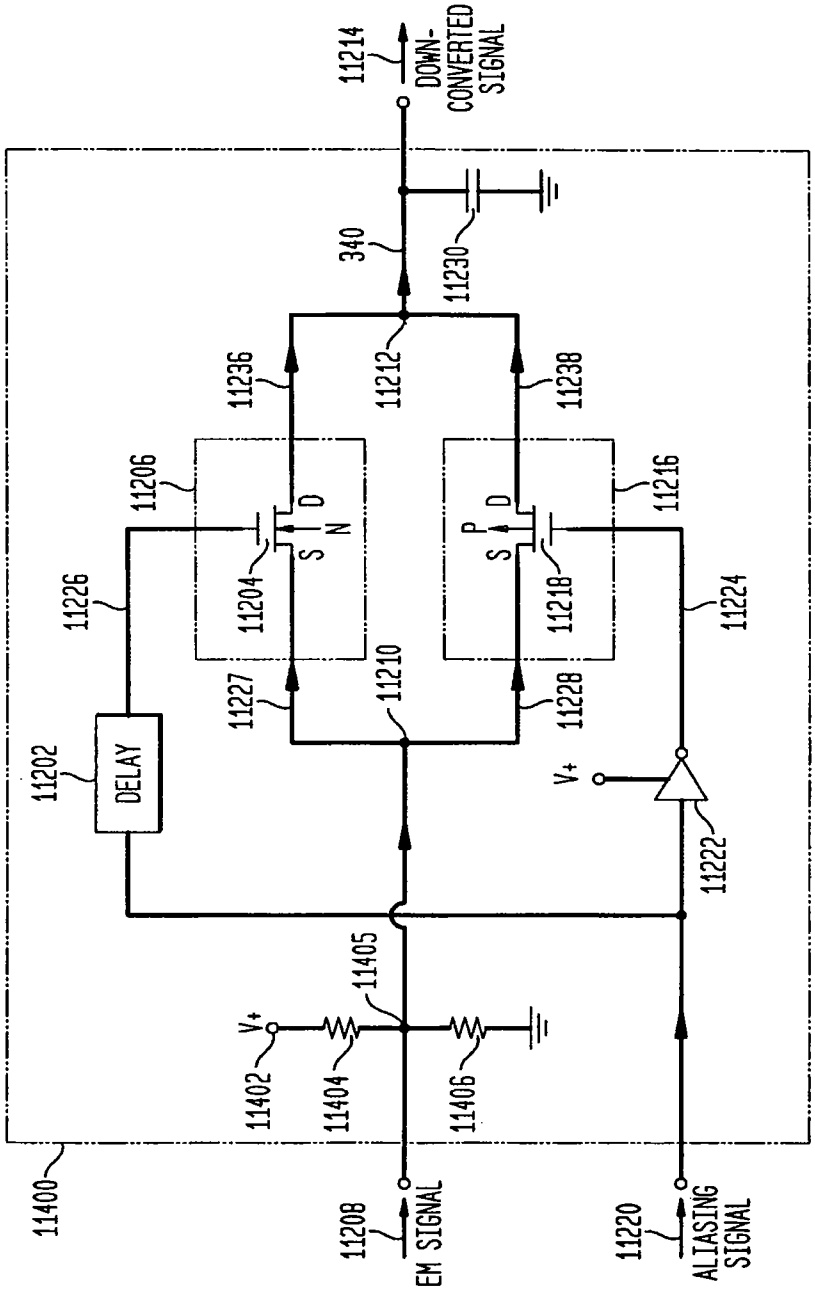

11214
DOWN-CONVERTED SIGNAL
340
11230
11212
11236
11238
11206
11216
11204
11218
11226
11224
11227
11210
11228
11202
DELAY
V+
11222
11405
11402
11404
11406
11400
11208
EM SIGNAL
11220
ALIASING SIGNAL

FIG. 115

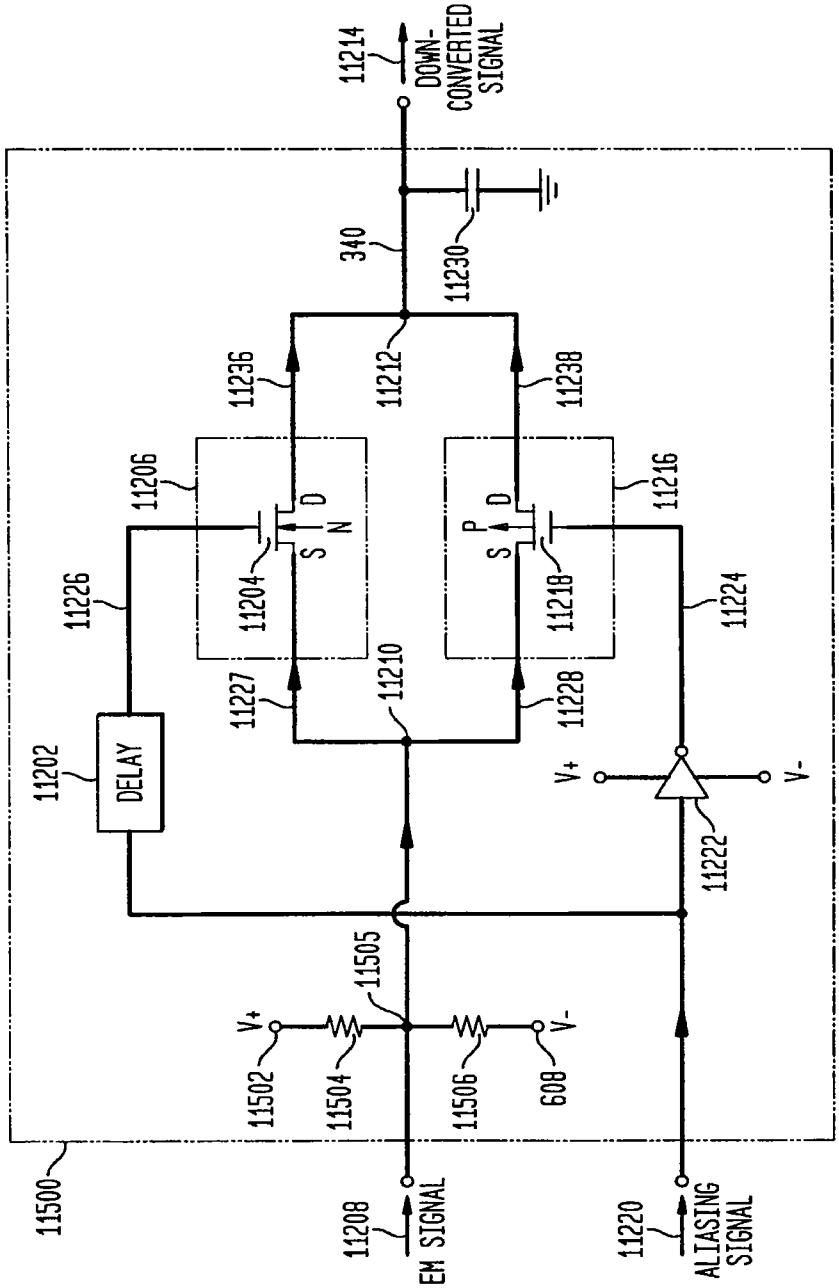

11214
DOWN-CONVERTED SIGNAL
340
11230
11212
11236
11238
11206
11216
11204
11218
11226
11224
11227
11210
11228
11202
DELAY
V+
V-
11222
11505
11502
11504
11506
608
11500
11208
EM SIGNAL
11220
ALIASING SIGNAL

FIG. 116

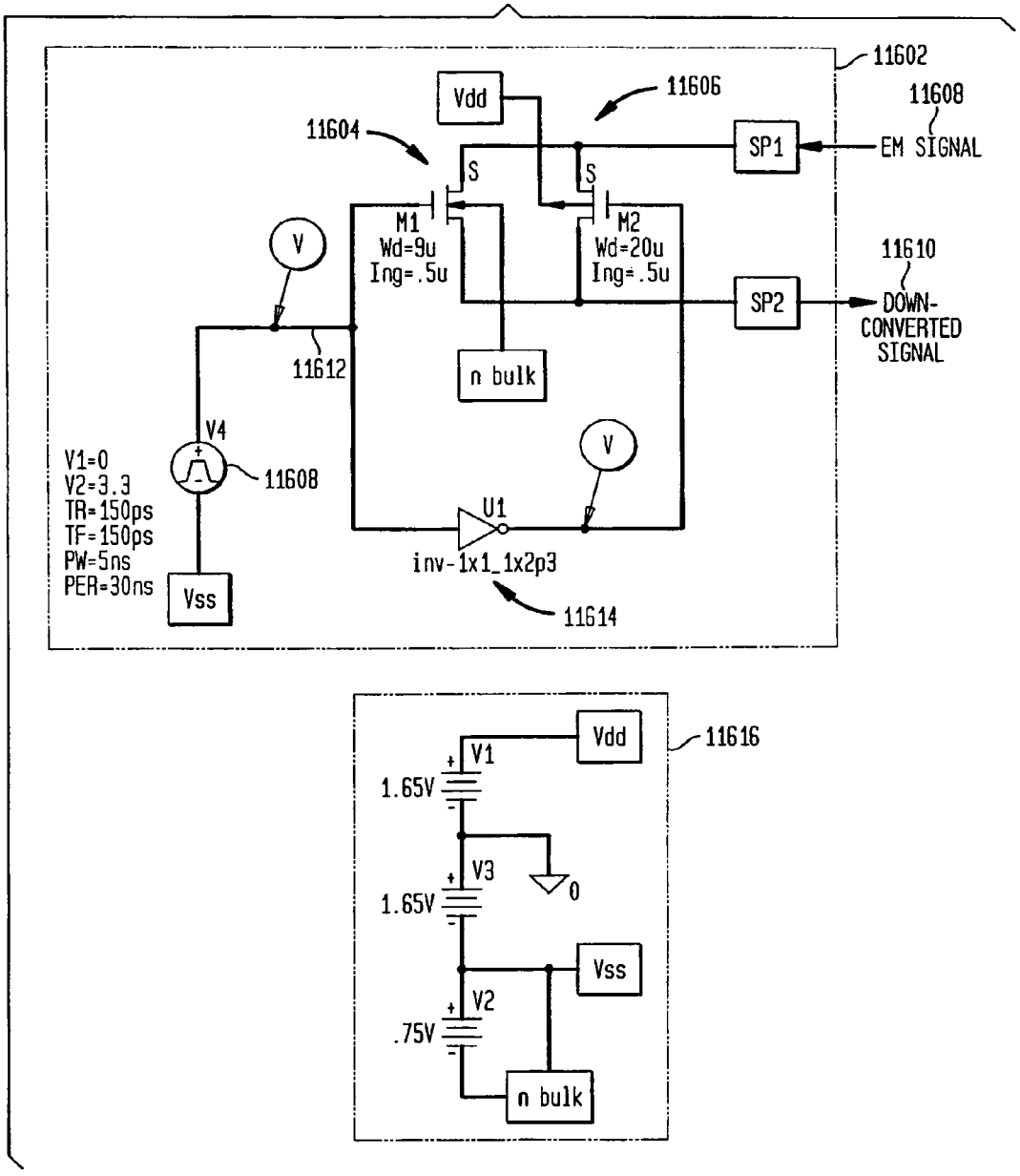
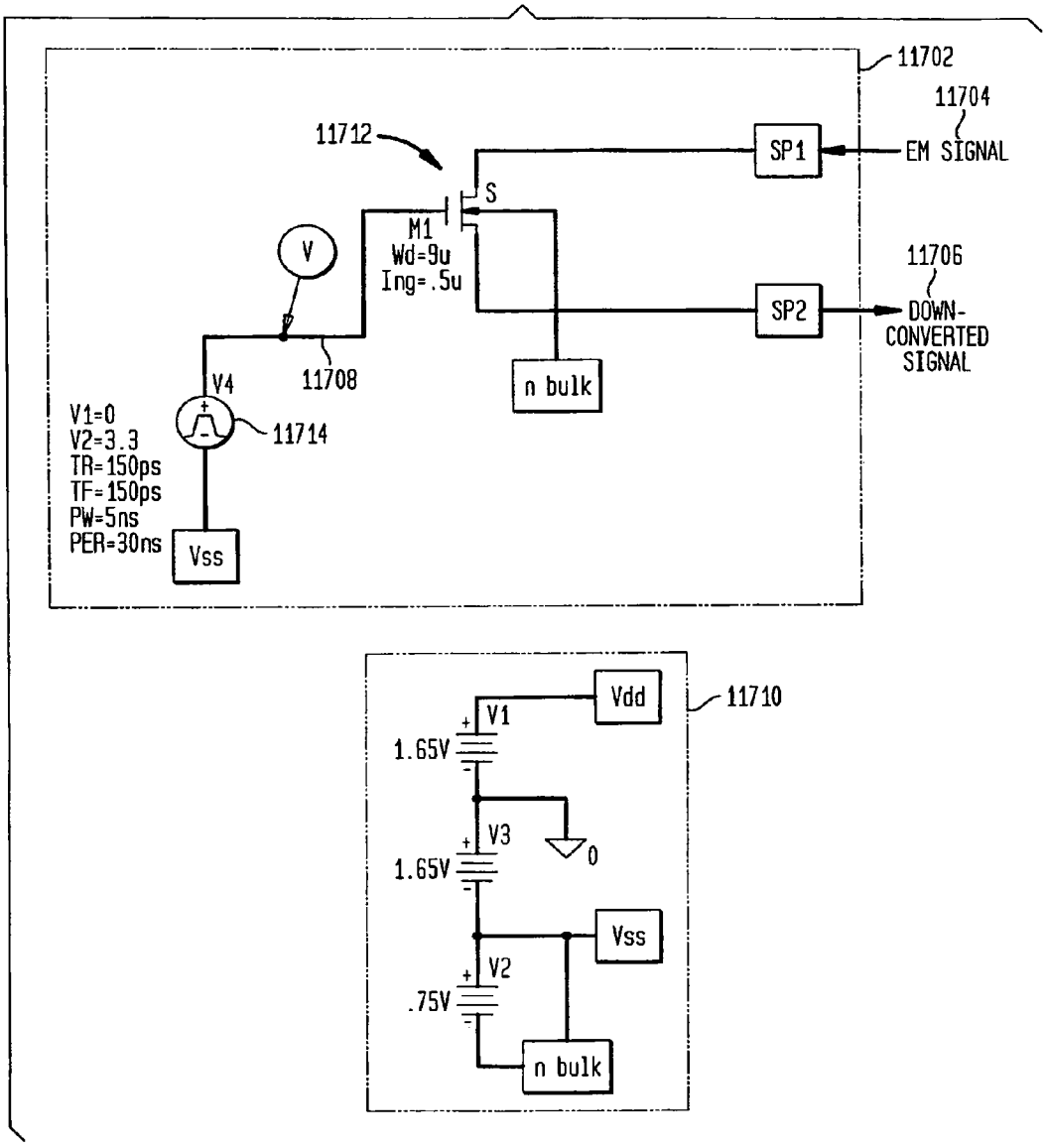
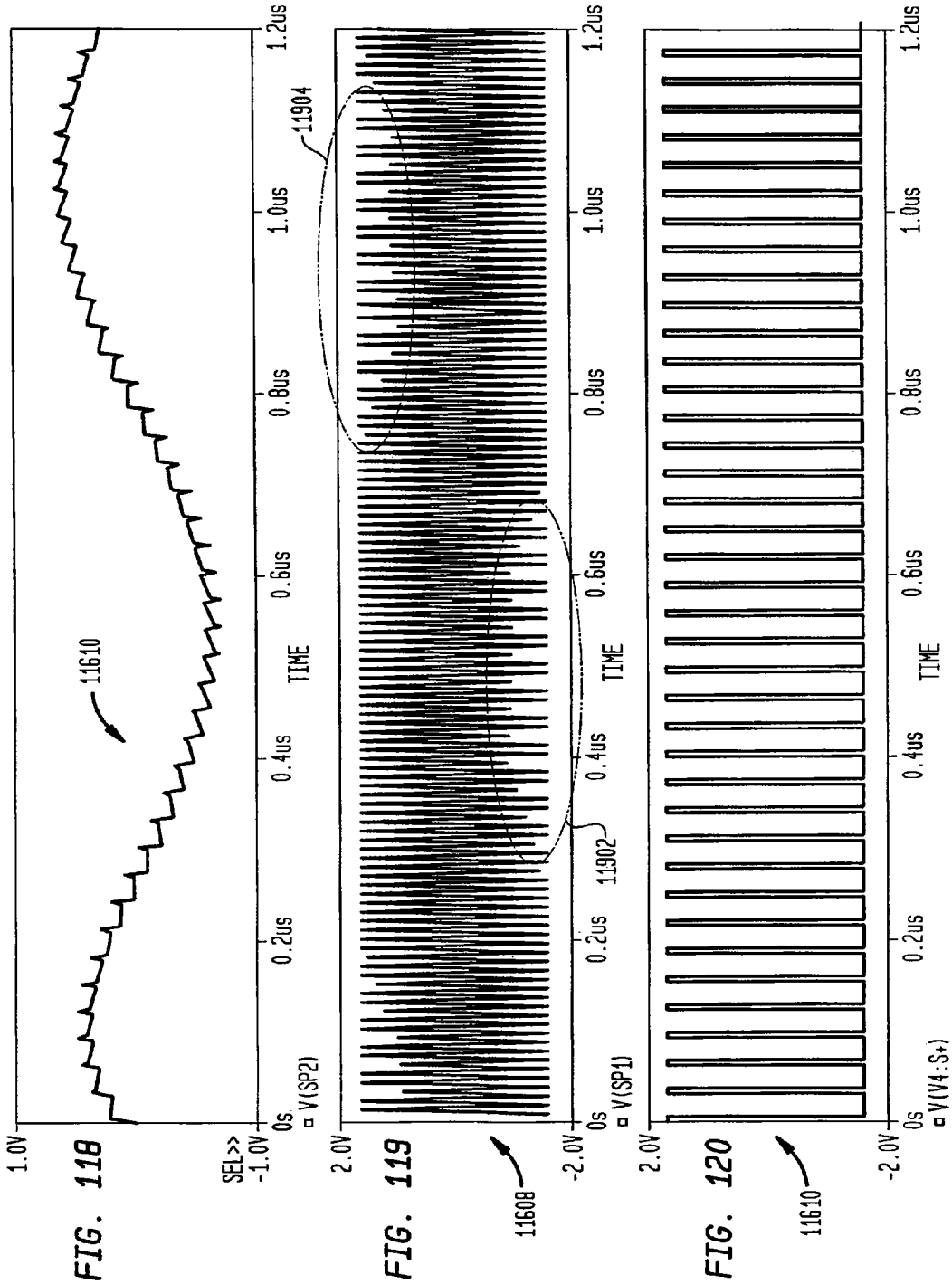

11602
11606
11608
Vdd
11604
SP1
EM SIGNAL
S
S
M1
Wd=9u
Lng=.5u
M2
Wd=20u
Lng=.5u
V
11610
SP2
DOWN-
CONVERTED
SIGNAL
11612
n bulk
V4
V1=0
V2=3.3
TR=150ps
TF=150ps
PW=5ns
PER=30ns
11608
V
U1
inv-1x1_1x2p3
Vss
11614
11616
Vdd
V1
1.65V
V3
1.65V
0
Vss
V2
.75V
n bulk

FIG. 117


11702
11704
11712
SP1
EM SIGNAL
S
M1
Wd=9u
Lng=.5u
V
11706
SP2
DOWN-
CONVERTED
SIGNAL
V4
11708
n bulk
V1=0
V2=3.3
TR=150ps
TF=150ps
PW=5ns
PER=30ns
11714
Vss
Vdd
11710
V1
1.65V
V3
1.65V
0
Vss
V2
.75V
n bulk


1.0V
SEL>>
-1.0V
11610
0s
0.2us
0.4us
0.6us
0.8us
1.0us
1.2us
TIME
V(SP2)
FIG. 118
2.0V
-2.0V
11904
11902
11608
V(SP1)
FIG. 119
2.0V
-2.0V
11610
V(V4:S+)
FIG. 120

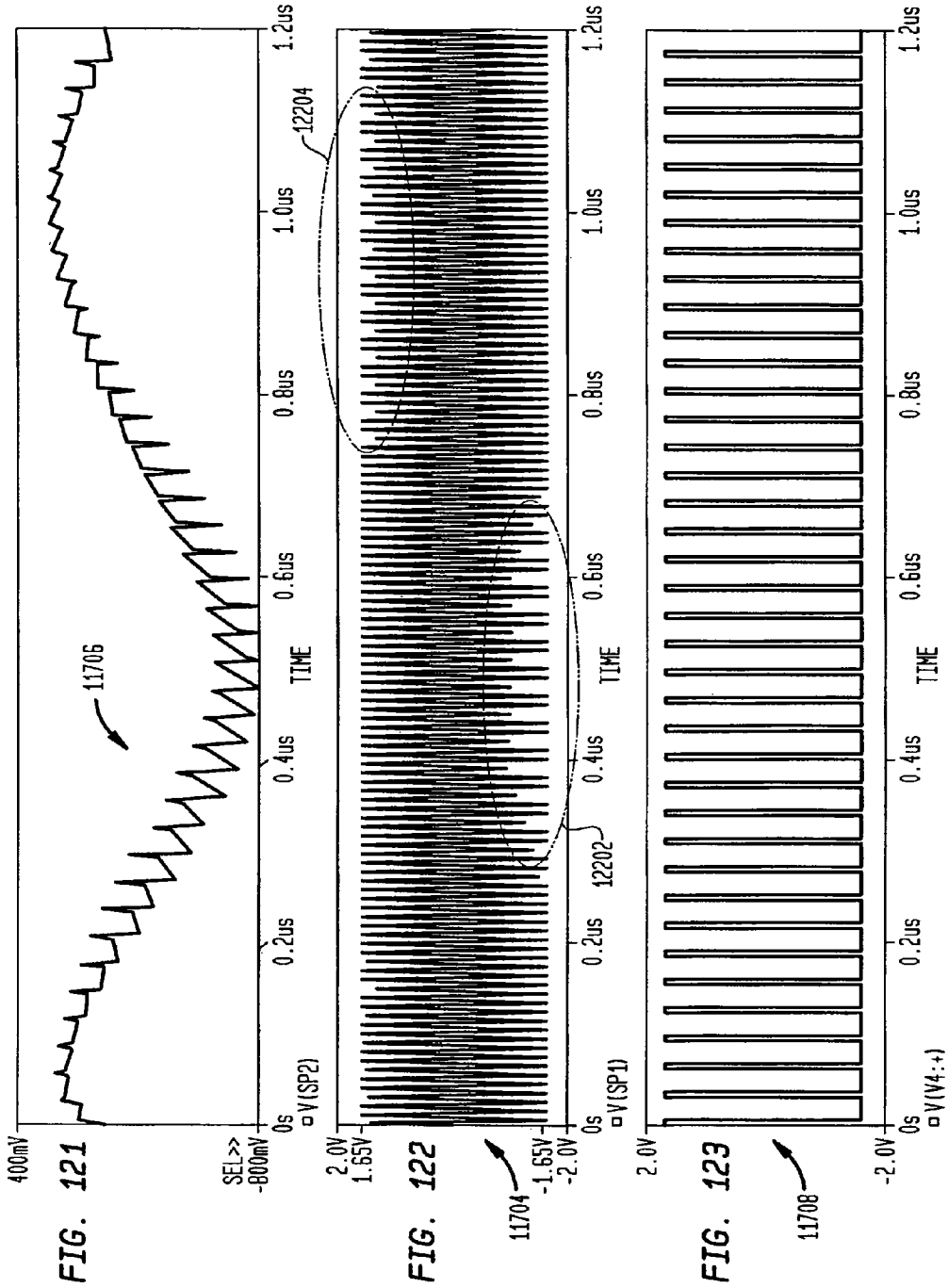

400mV
SEL>>
-800mV
11706
0s
0.2us
0.4us
0.6us
0.8us
1.0us
1.2us
TIME
V(SP2)
FIG. 121
2.0V
1.65V
12204
12202
-1.65V
-2.0V
11704
V(SP1)
FIG. 122
2.0V
-2.0V
11708
V(V4:+)
FIG. 123

FIG. 124A

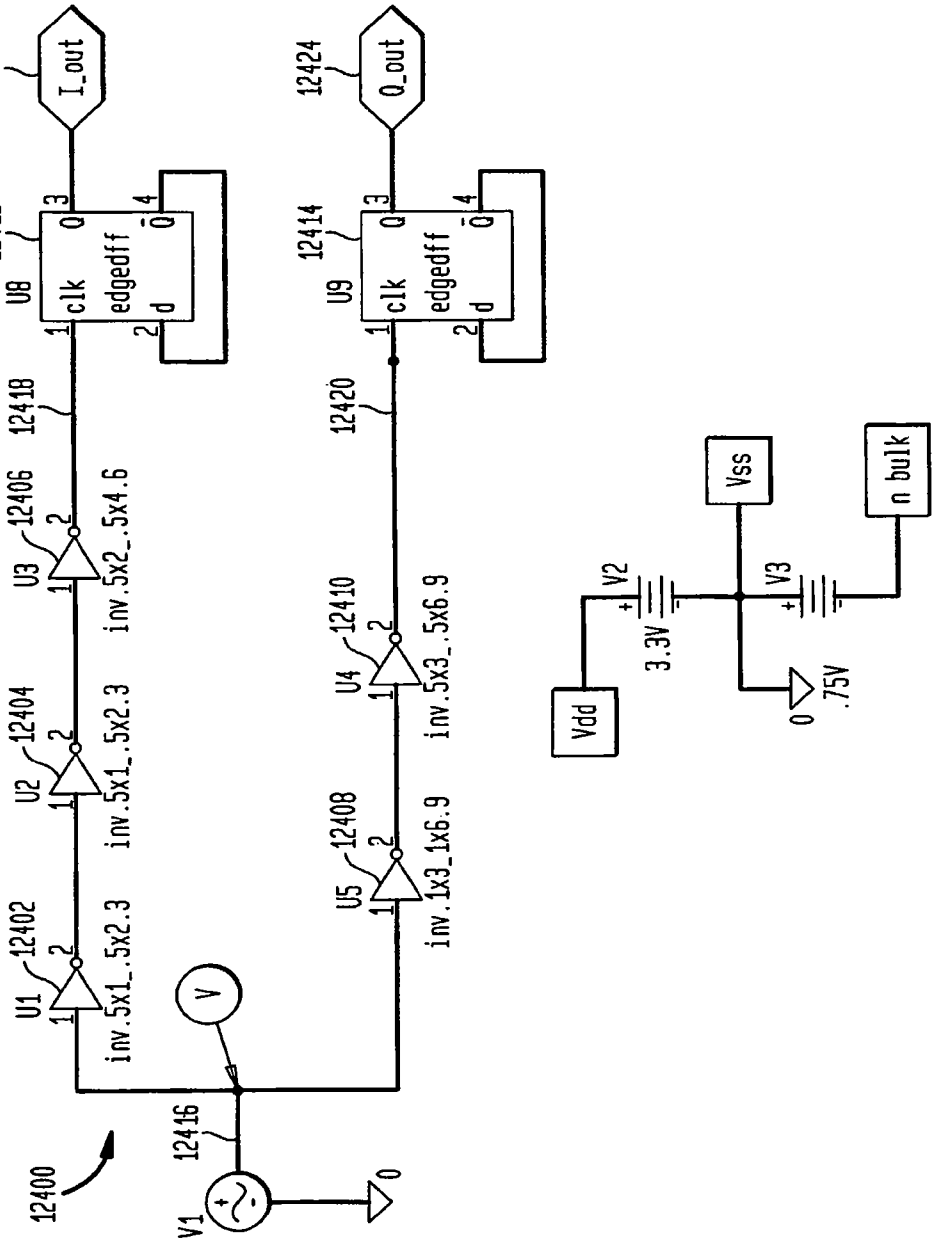
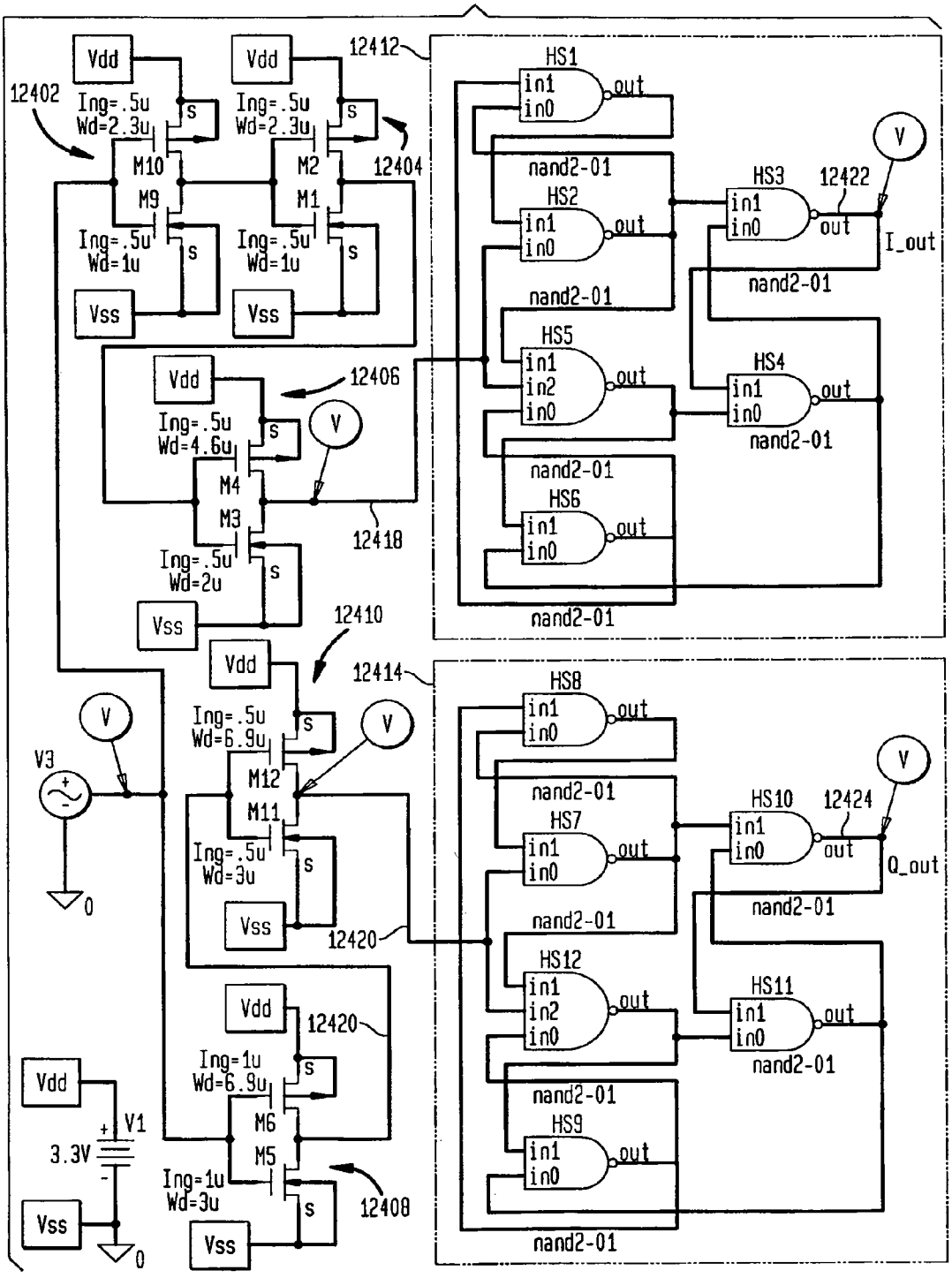

12400
12402
U1
inv.5x1_.5x2.3
12404
U2
inv.5x1_.5x2.3
12406
U3
inv.5x2_.5x4.6
12408
U5
inv.1x3_1x6.9
12410
U4
inv.5x3_.5x6.9
12412
U8
clk
edgedff
d
12414
U9
clk
edgedff
d
12416
V1
V
12418
12420
12422
I_out
12424
Q_out
Vdd
3.3V
V2
Vss
V3
.75V
n bulk
0

FIG. 124B


12402
12404
12406
12408
12410
12412
12414
12418
12420
12422
12424
Vdd
Vss
M10
M9
M2
M1
M4
M3
M12
M11
M6
M5
Ing=.5u
Wd=2.3u
Ing=.5u
Wd=1u
Ing=.5u
Wd=4.6u
Ing=.5u
Wd=2u
Ing=.5u
Wd=6.9u
Ing=.5u
Wd=3u
Ing=1u
Wd=6.9u
Ing=1u
Wd=3u
V3
V1
3.3V
0
V
HS1
HS2
HS3
HS4
HS5
HS6
HS7
HS8
HS9
HS10
HS11
HS12
in1
in2
in0
out
nand2-01
I_out
Q_out

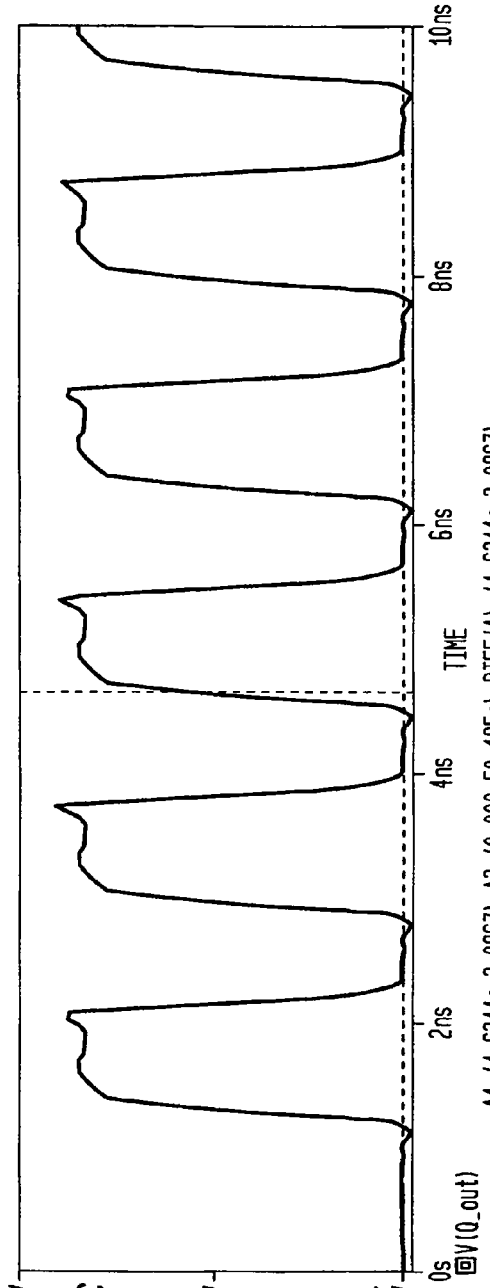


FIG. 124C

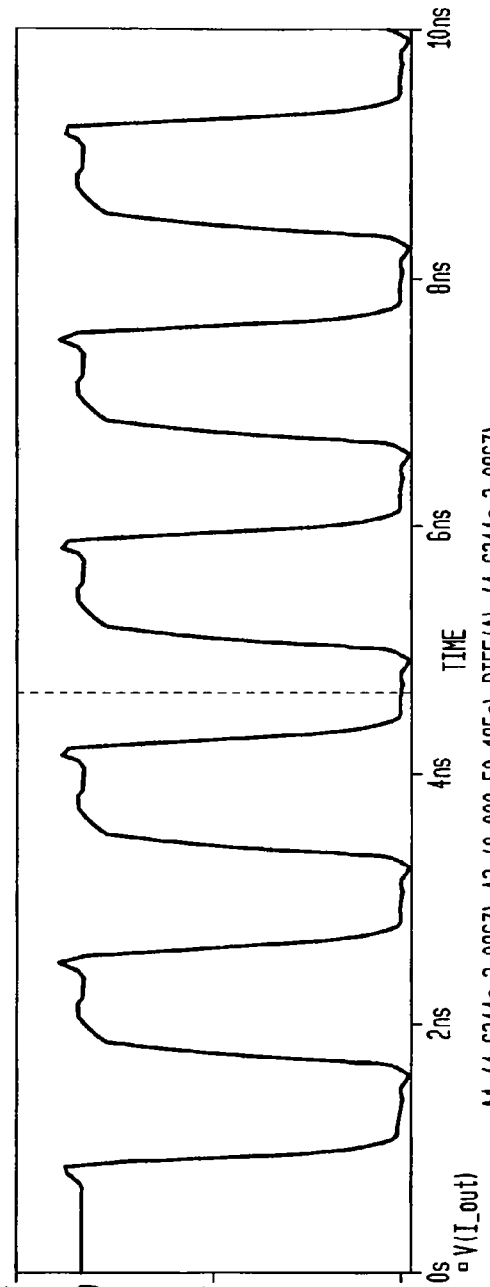


FIG. 124D

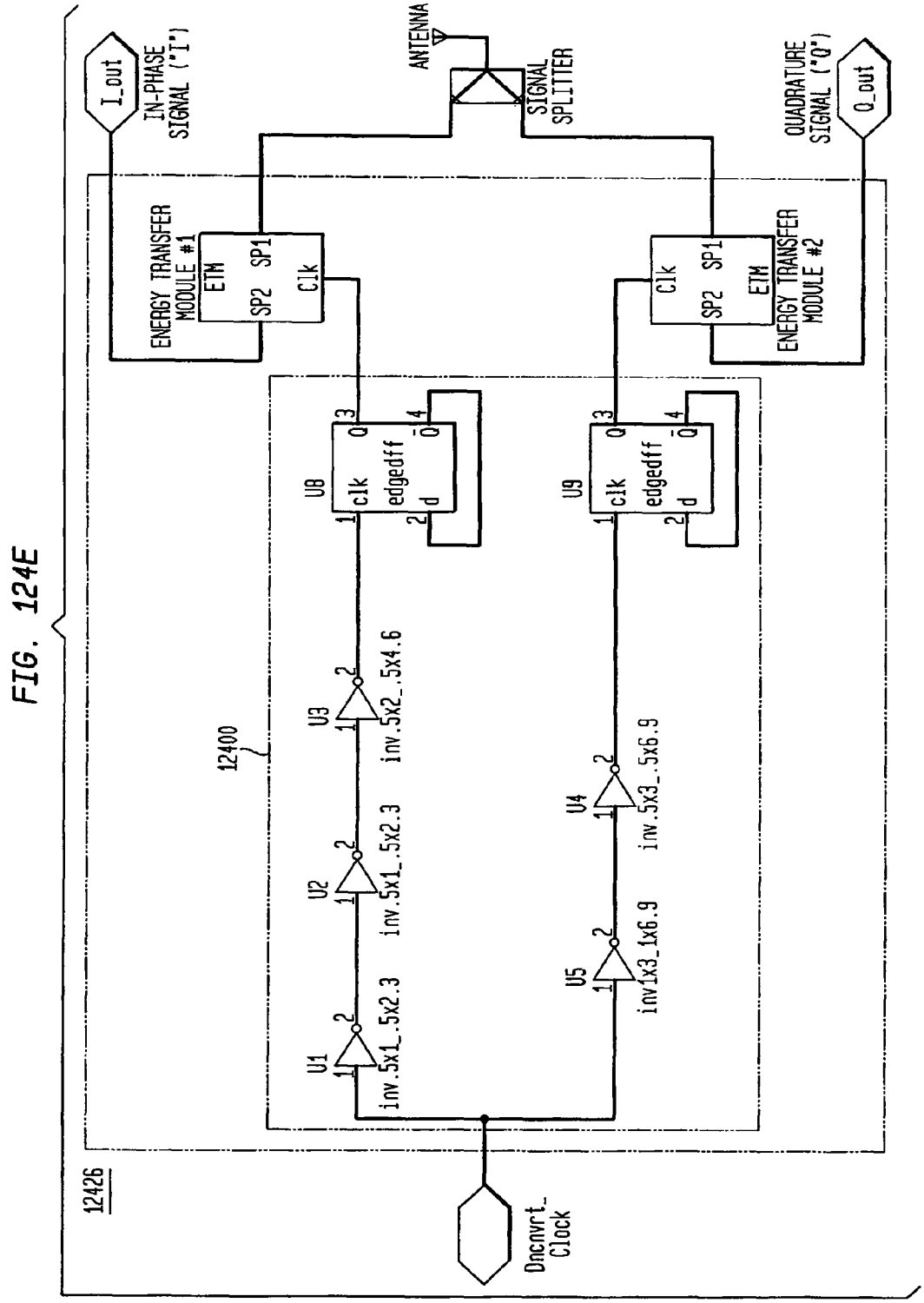

I_out
IN-PHASE SIGNAL ("I")
ANTENNA
SIGNAL SPLITTER
Q_out
QUADRATURE SIGNAL ("Q")
ENERGY TRANSFER MODULE #1
ETM
SP1
SP2
Clk
ENERGY TRANSFER MODULE #2
U8
U9
clk
edgedff
d
U1
U2
U3
U4
U5
inv.5x1_.5x2.3
inv.5x1_.5x2.3
inv.5x2_.5x4.6
inv.5x3_.5x6.9
inv1x3_1x6.9
12400
12426
Dncnvrt_ Clock

FIG. 124E

FIG. 124F

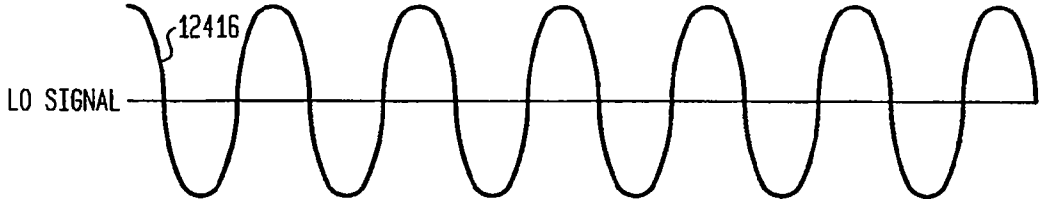


FIG. 124G

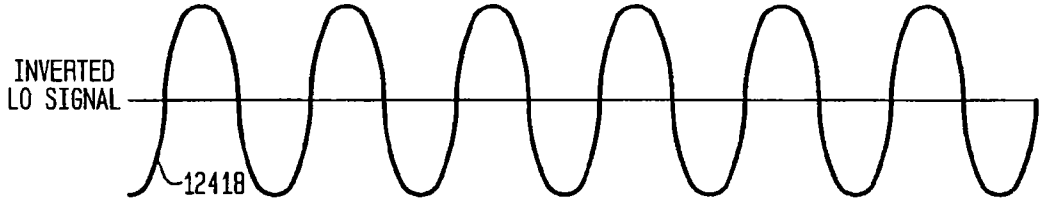


FIG. 124H

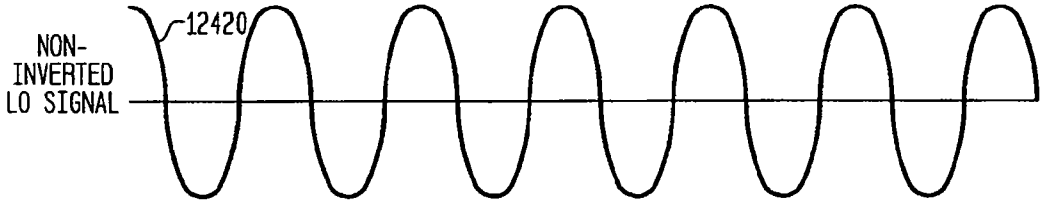


FIG. 124I

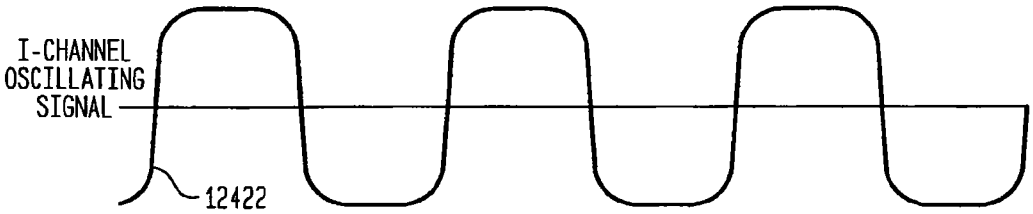


FIG. 124J

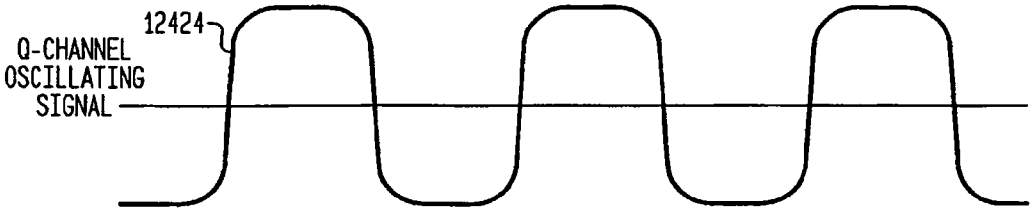
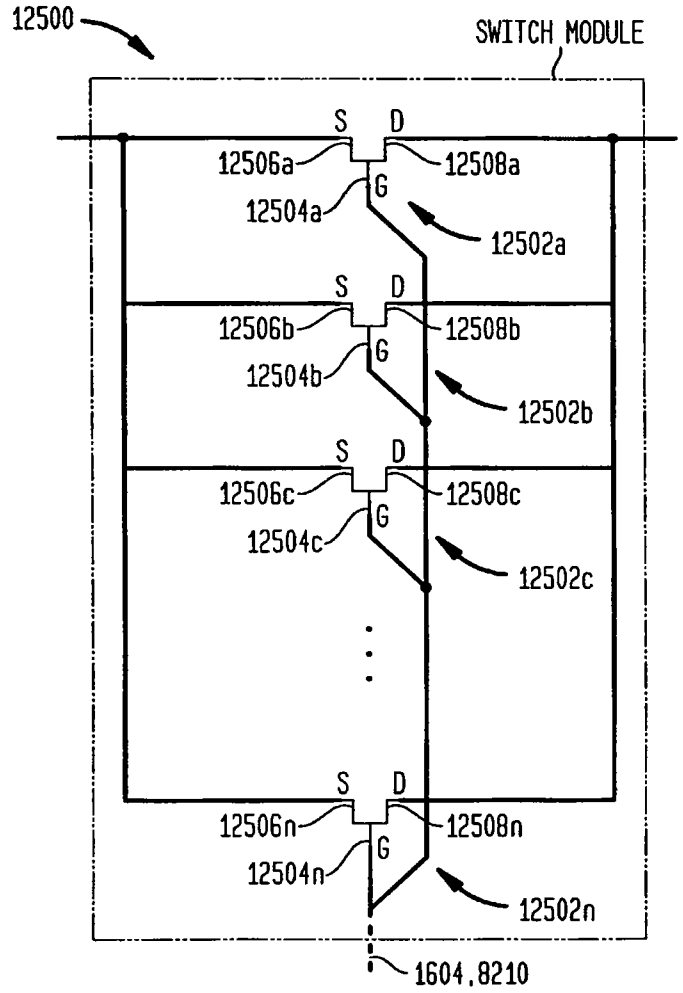


FIG. 125


12500
SWITCH MODULE
S
D
12506a
12508a
G
12504a
12502a
S
D
12506b
12508b
G
12504b
12502b
S
D
12506c
12508c
G
12504c
12502c
S
D
12506n
12508n
G
12504n
12502n
1604,8210

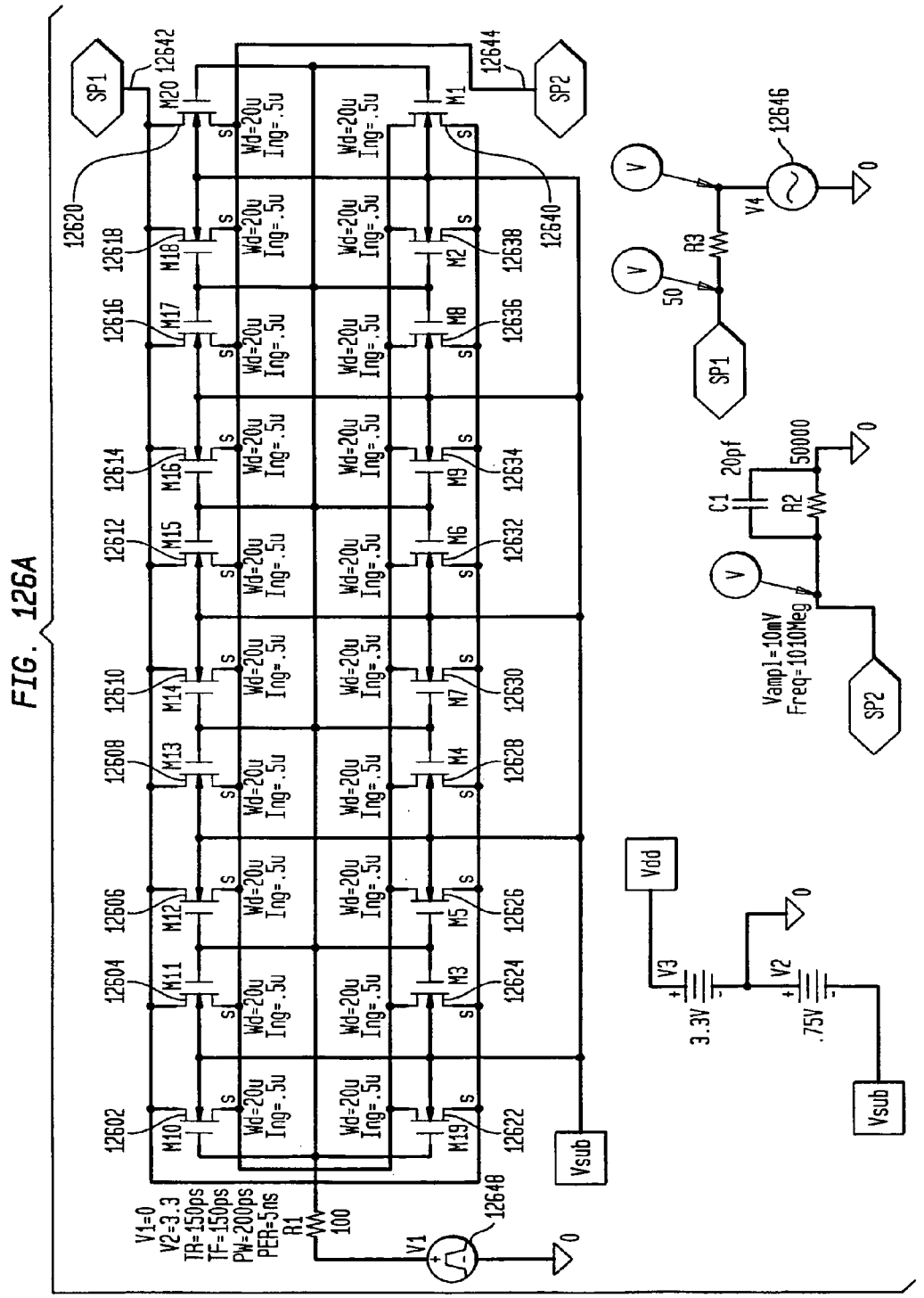

SP1
SP2
12620
12640
12642
12644
12646
12648
12602
12604
12606
12608
12610
12612
12614
12616
12618
12622
12624
12626
12628
12630
12632
12634
12636
12638
M10
M11
M12
M13
M14
M15
M16
M17
M18
M19
M20
M1
M2
M3
M4
M5
M6
M7
M8
M9
Wd=20u
Lng=.5u
V1=0
V2=3.3
TR=150ps
TF=150ps
PW=200ps
PER=5ns
R1
100
V1
0
Vsub
Vdd
V3
3.3V
V2
.75V
V
50
R3
V4
C1
20pf
R2
50000
Vampl=10mV
Freq=1010Meg

FIG. 126A

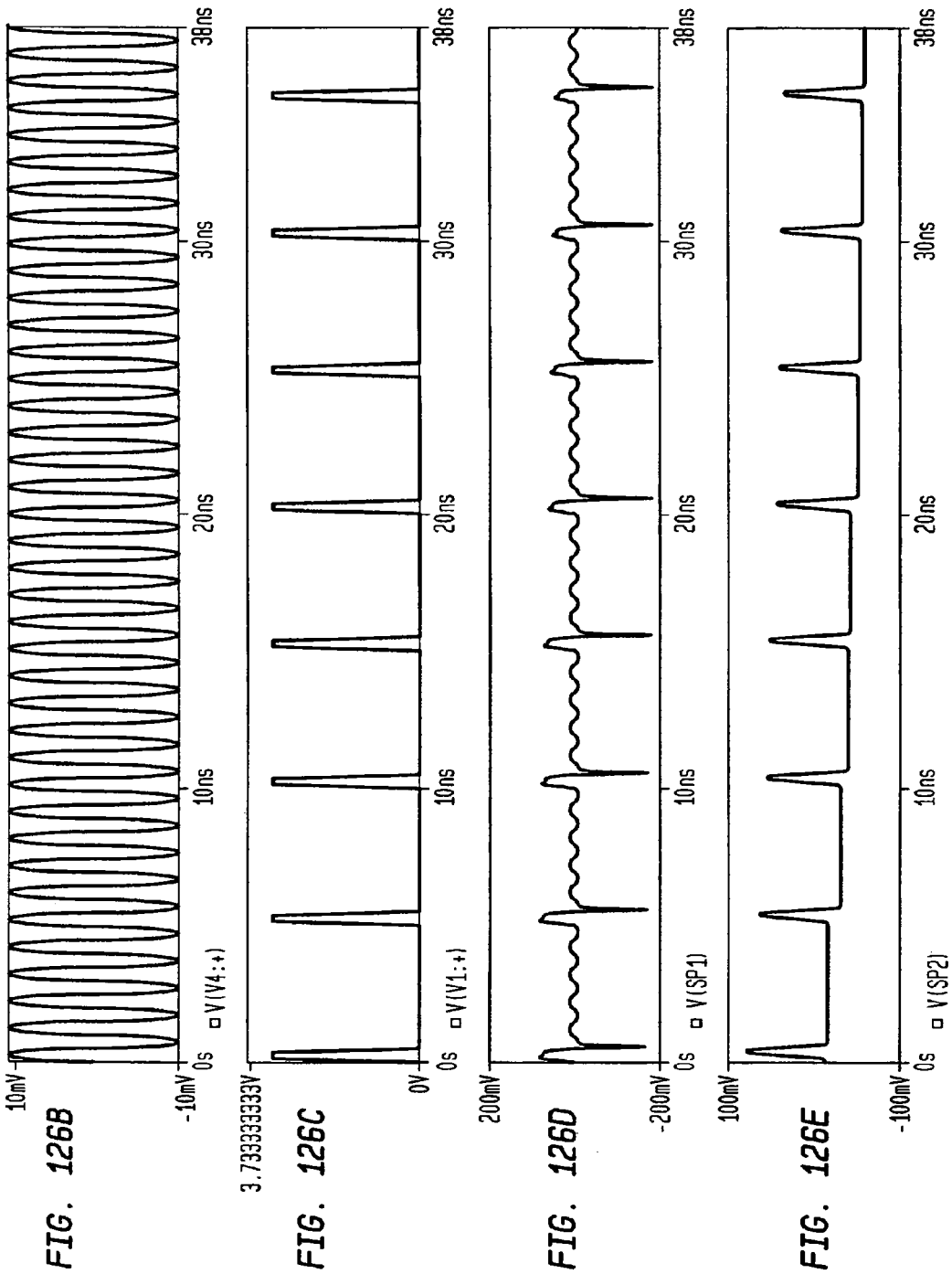


FIG. 126B

FIG. 126C

FIG. 126D

FIG. 126E

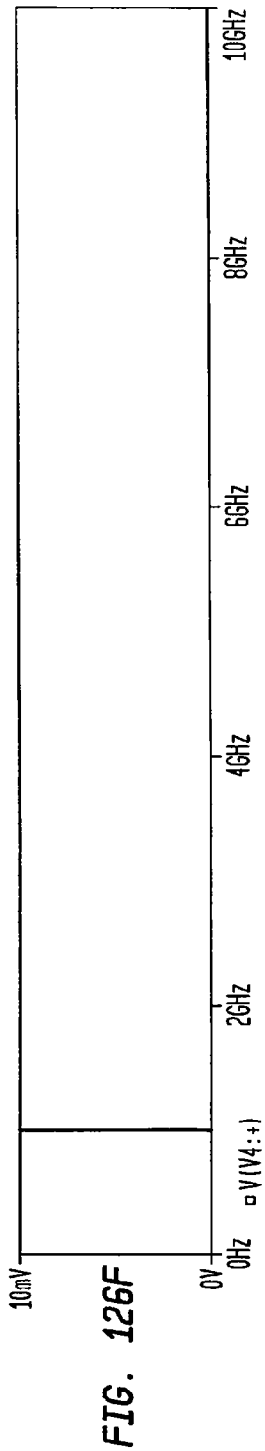


FIG. 126F

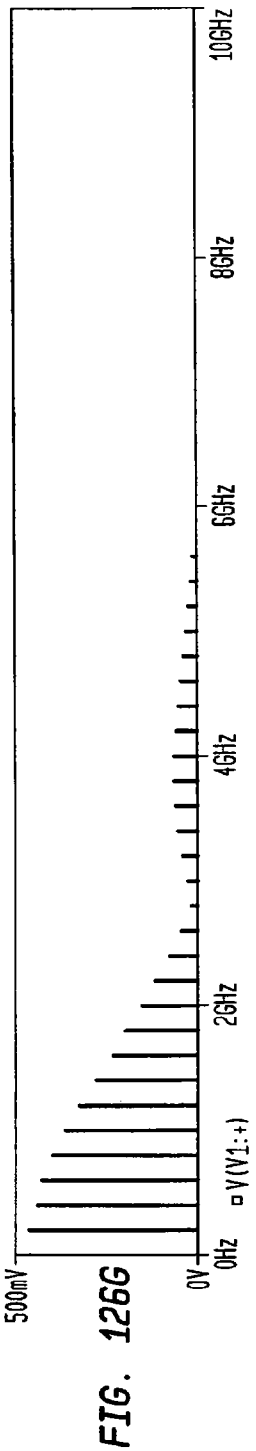


FIG. 126G

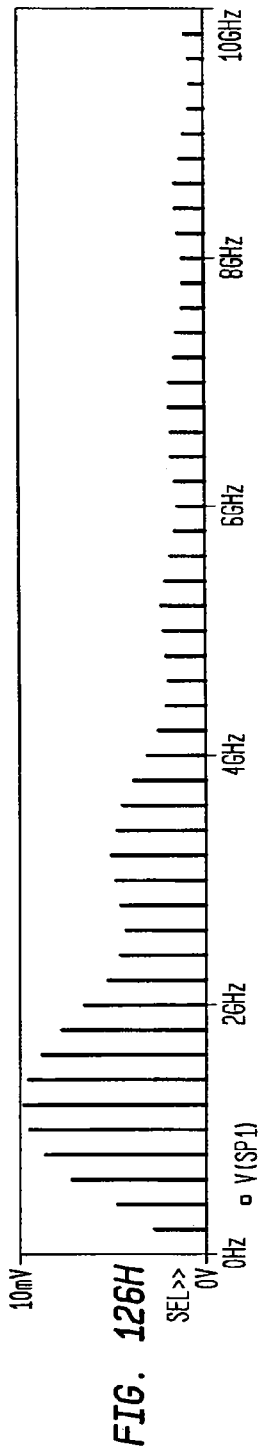


FIG. 126H

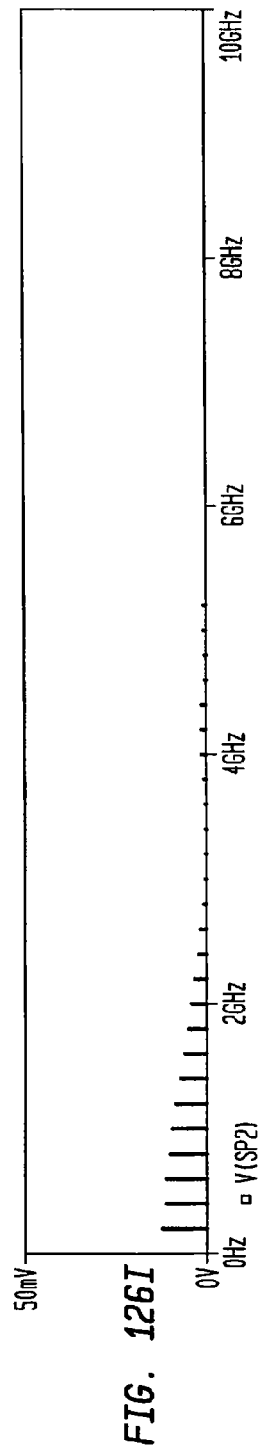


FIG. 126I

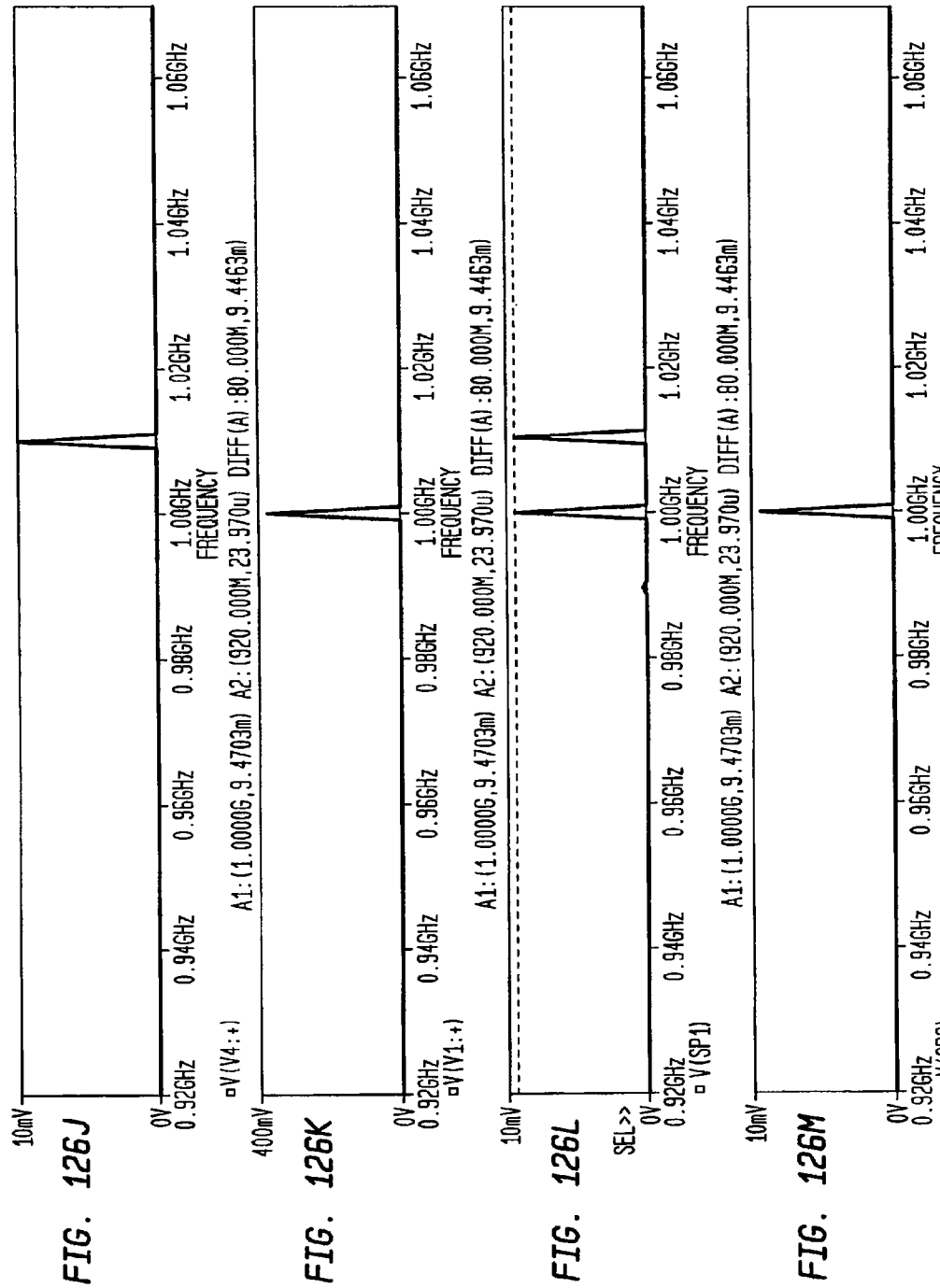
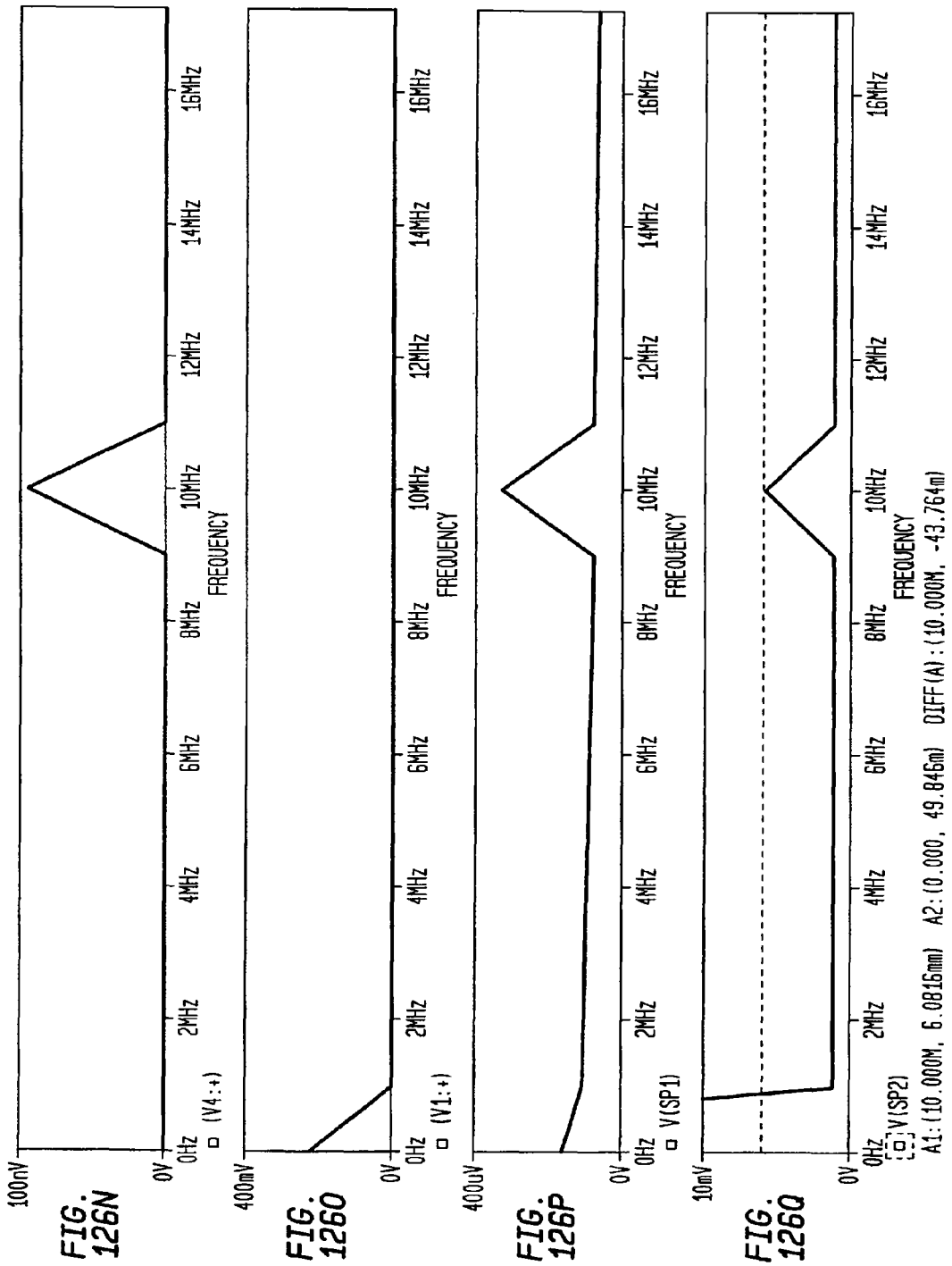


FIG. 126J

FIG. 126K

FIG. 126L

FIG. 126M


100nV
0V
0Hz
2MHz
4MHz
6MHz
8MHz
10MHz
12MHz
14MHz
16MHz
FREQUENCY
V(V4:+)
FIG. 126N
400mV
0V
0Hz
2MHz
4MHz
6MHz
8MHz
10MHz
12MHz
14MHz
16MHz
FREQUENCY
V(V1:+)
FIG. 126O
400uV
0V
0Hz
2MHz
4MHz
6MHz
8MHz
10MHz
12MHz
14MHz
16MHz
FREQUENCY
V(SP1)
FIG. 126P
10mV
0V
0Hz
2MHz
4MHz
6MHz
8MHz
10MHz
12MHz
14MHz
16MHz
FREQUENCY
V(SP2)
A1: (10.000M, 6.0815mm) A2: (0.000, 49.846m) DIFF(A): (10.000M, -43.764m)
FIG. 126Q

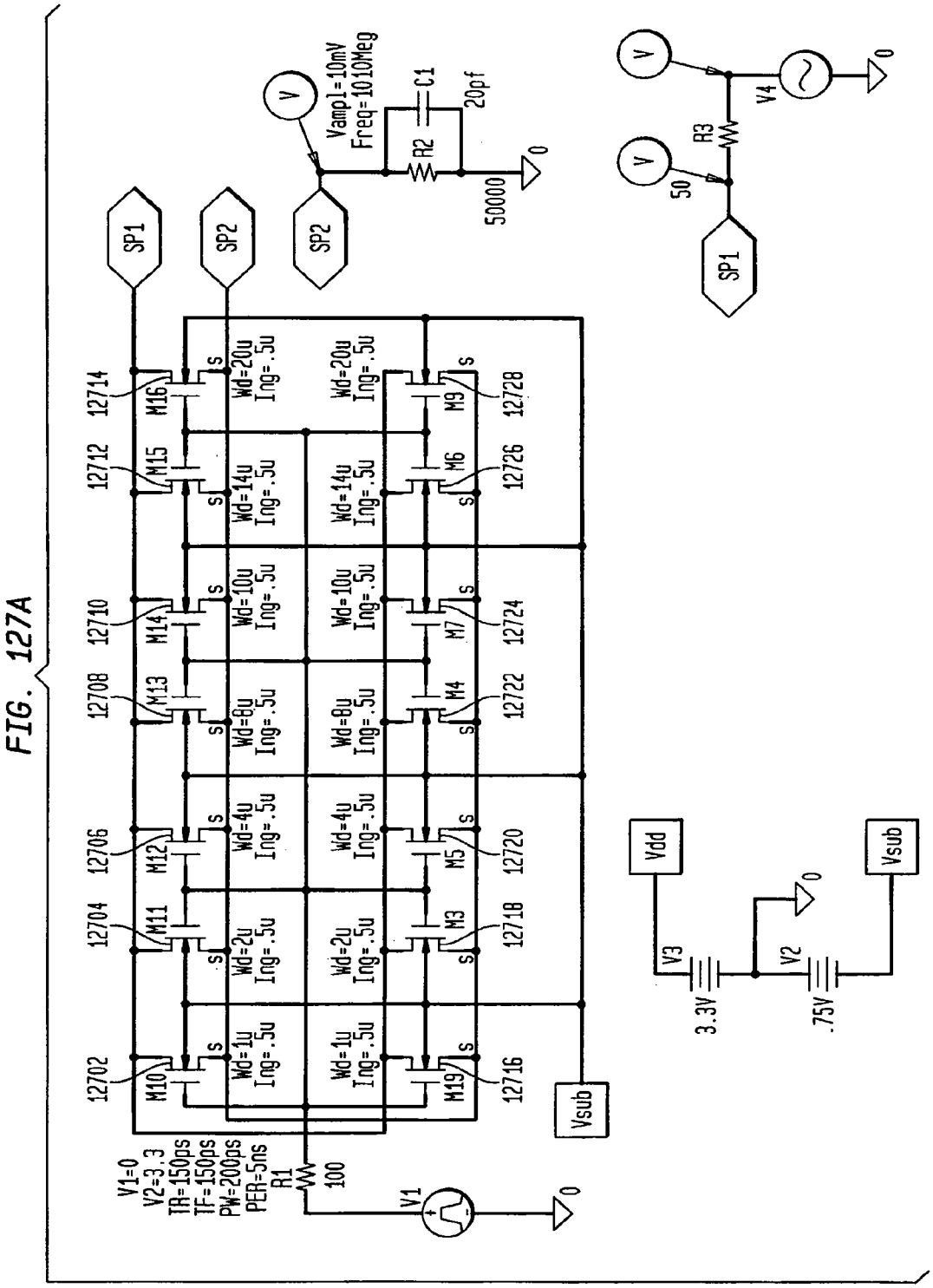

SP1
SP2
SP2
SP1
V
Vampl=10mV
Freq=1010Meg
C1
20pf
R2
50000
0
V
V4
R3
50
V
0
12714
12712
12710
12708
12706
12704
12702
M16
M15
M14
M13
M12
M11
M10
M9
M6
M7
M4
M5
M3
M19
12728
12726
12724
12722
12720
12718
12716
Wd=20u
Wd=14u
Wd=10u
Wd=8u
Wd=4u
Wd=2u
Wd=1u
Lng=.5u
V1=0
V2=3.3
TR=150ps
TF=150ps
PW=200ps
PER=5ns
R1
100
V1
0
Vsub
Vdd
V3
3.3V
0
V2
.75V
Vsub

FIG. 127A

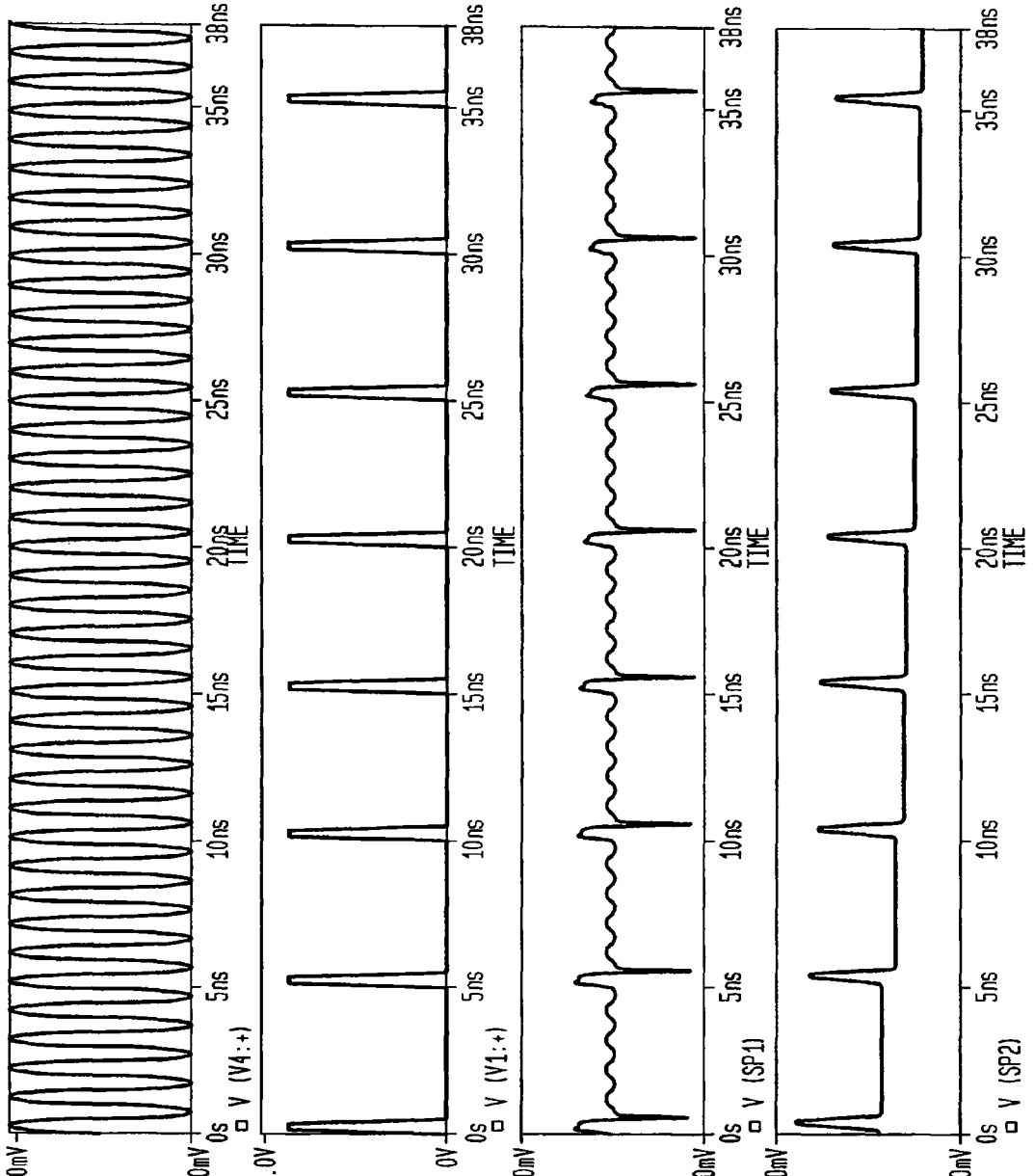


FIG. 127B

FIG. 127C

FIG. 127D

FIG. 127E

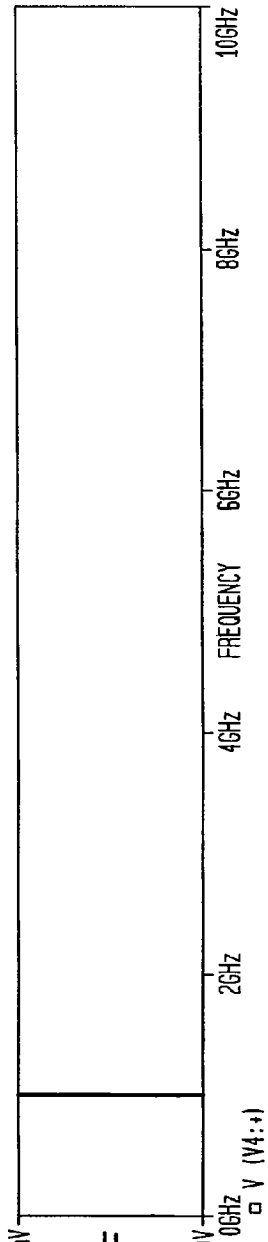


FIG. 127F

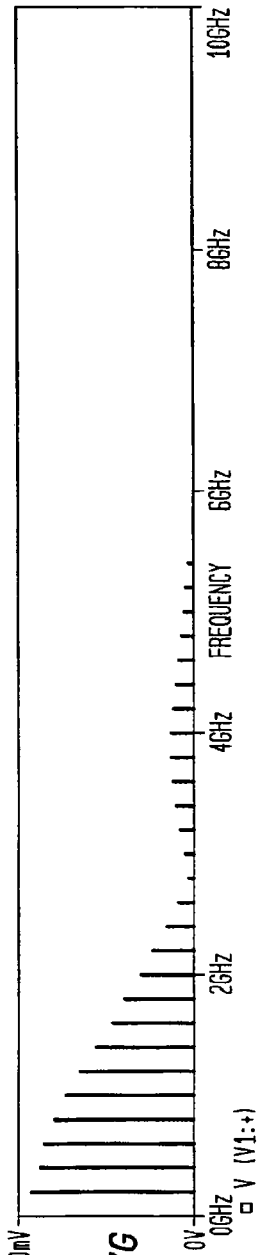


FIG. 127G

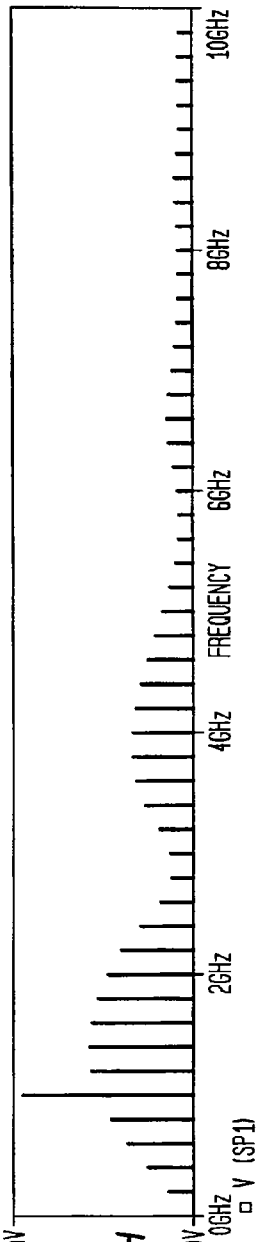


FIG. 127H

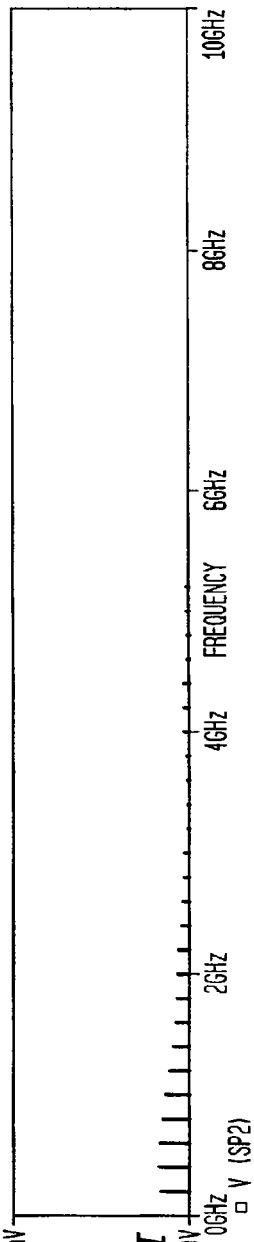
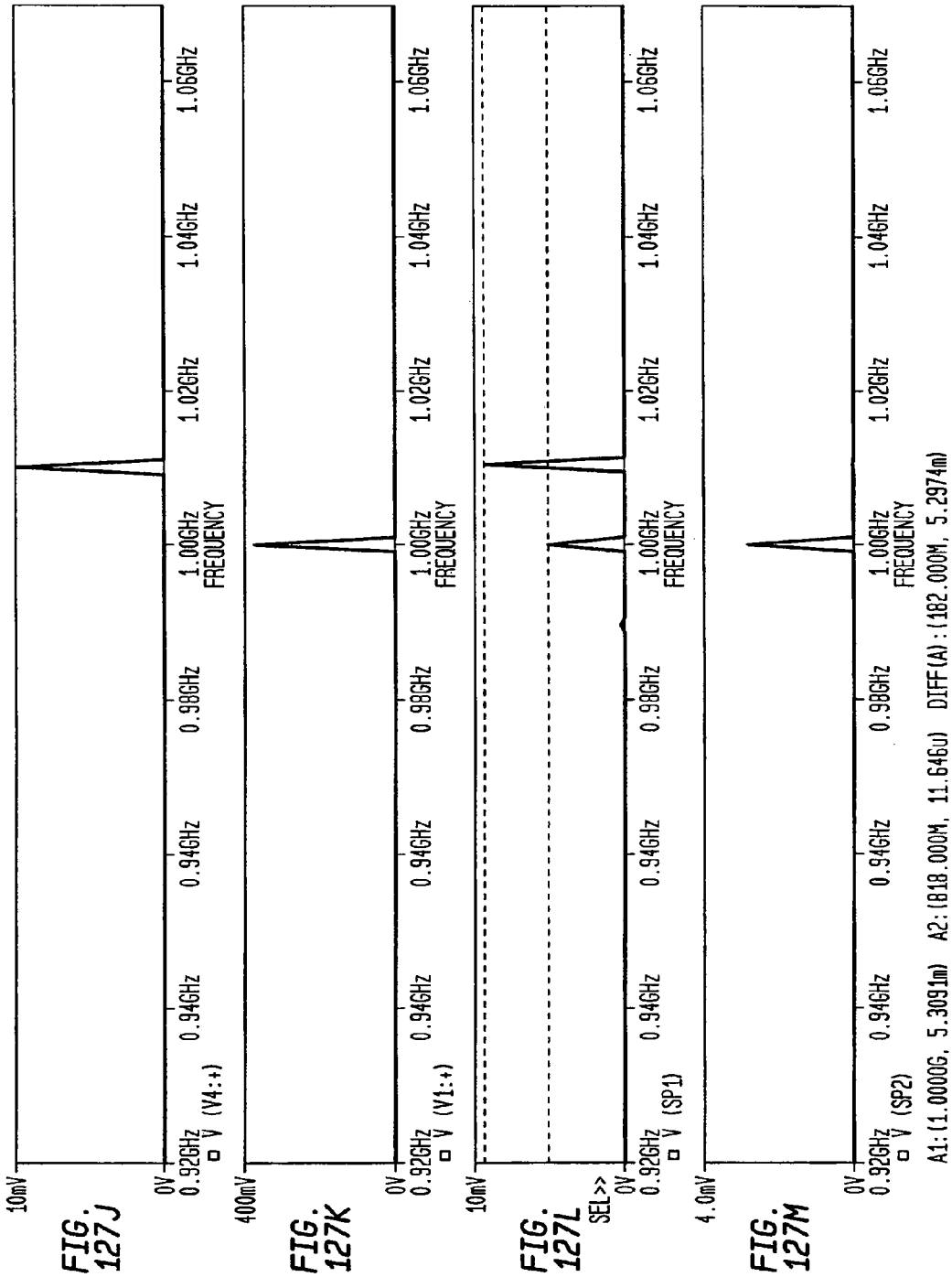


FIG. 127I


10mV
0V
0.92GHz
0.94GHz
0.96GHz
0.98GHz
1.00GHz
1.02GHz
1.04GHz
1.06GHz
FREQUENCY
V (V4:+)
FIG. 127J
400mV
V (V1:+)
FIG. 127K
SEL>>
V (SP1)
FIG. 127L
4.0mV
V (SP2)
A1: (1.0000G, 5.3091m) A2: (818.000M, 11.646u) DIFF(A): (182.000M, 5.2974m)
FIG. 127M

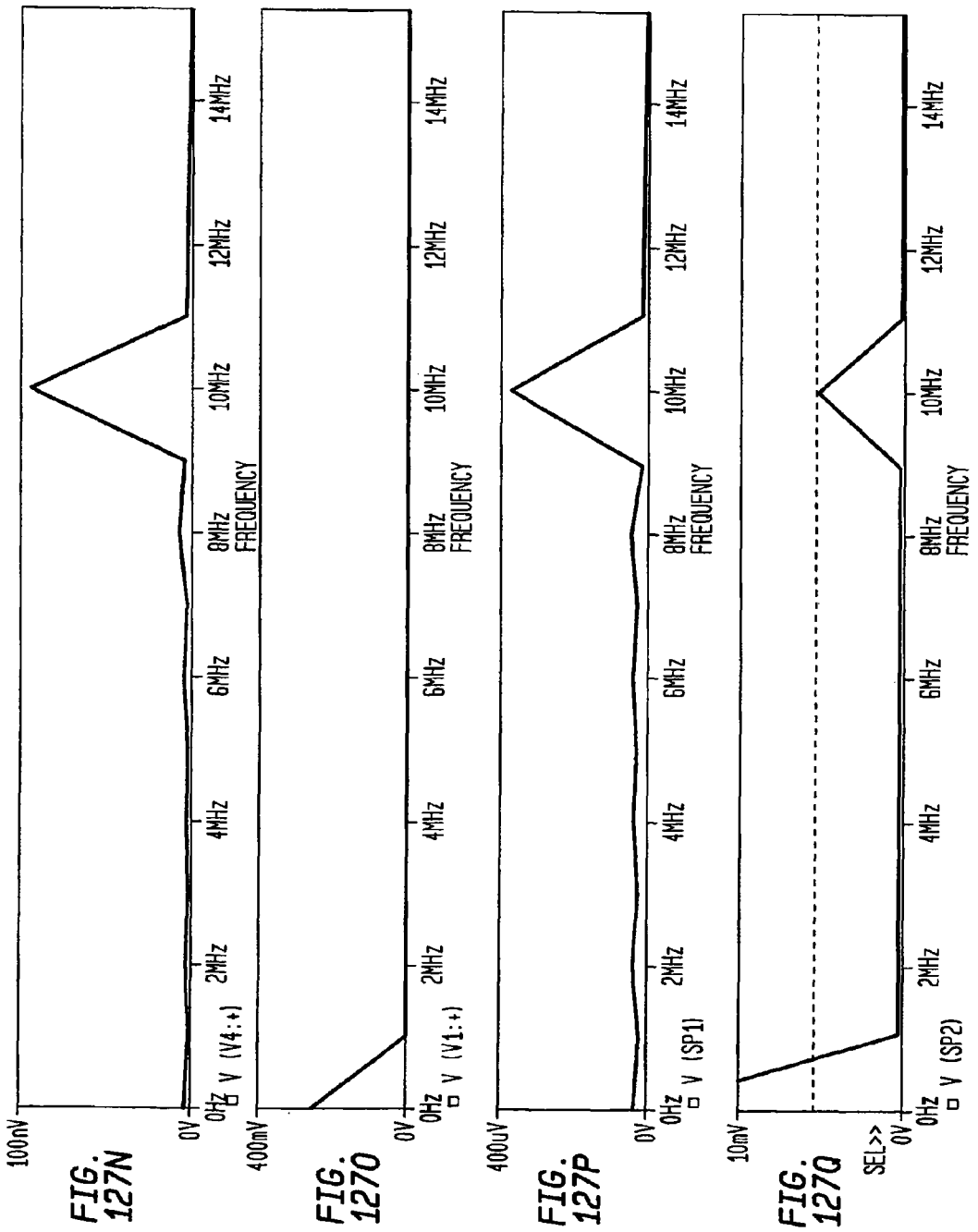


FIG. 127N

FIG. 127O

FIG. 127P

FIG. 127Q

FIG. 128A

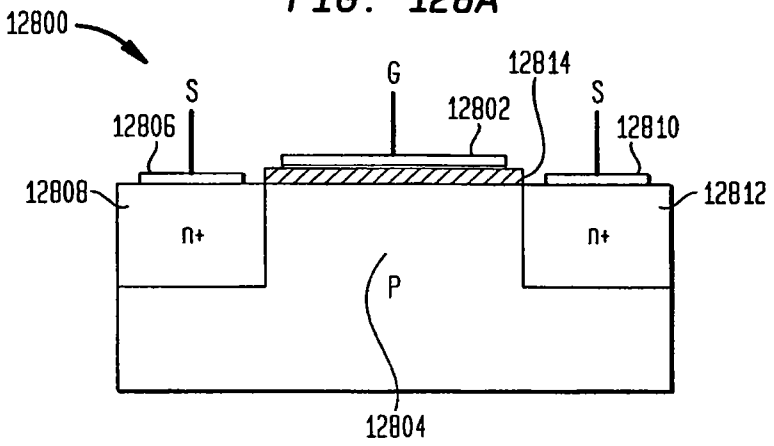
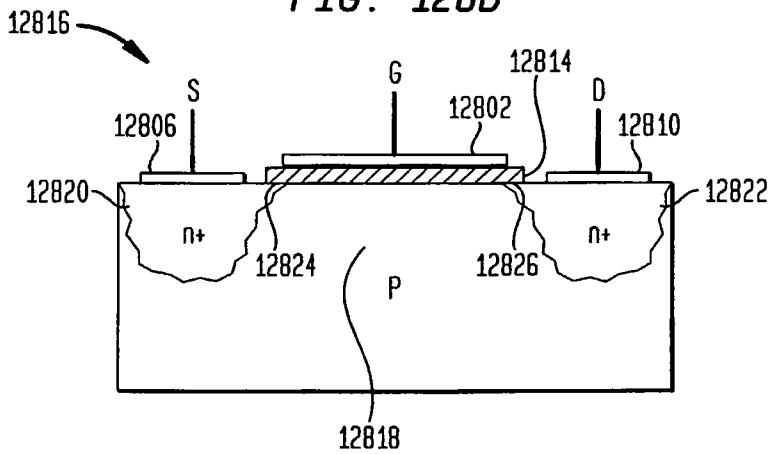


FIG. 128B



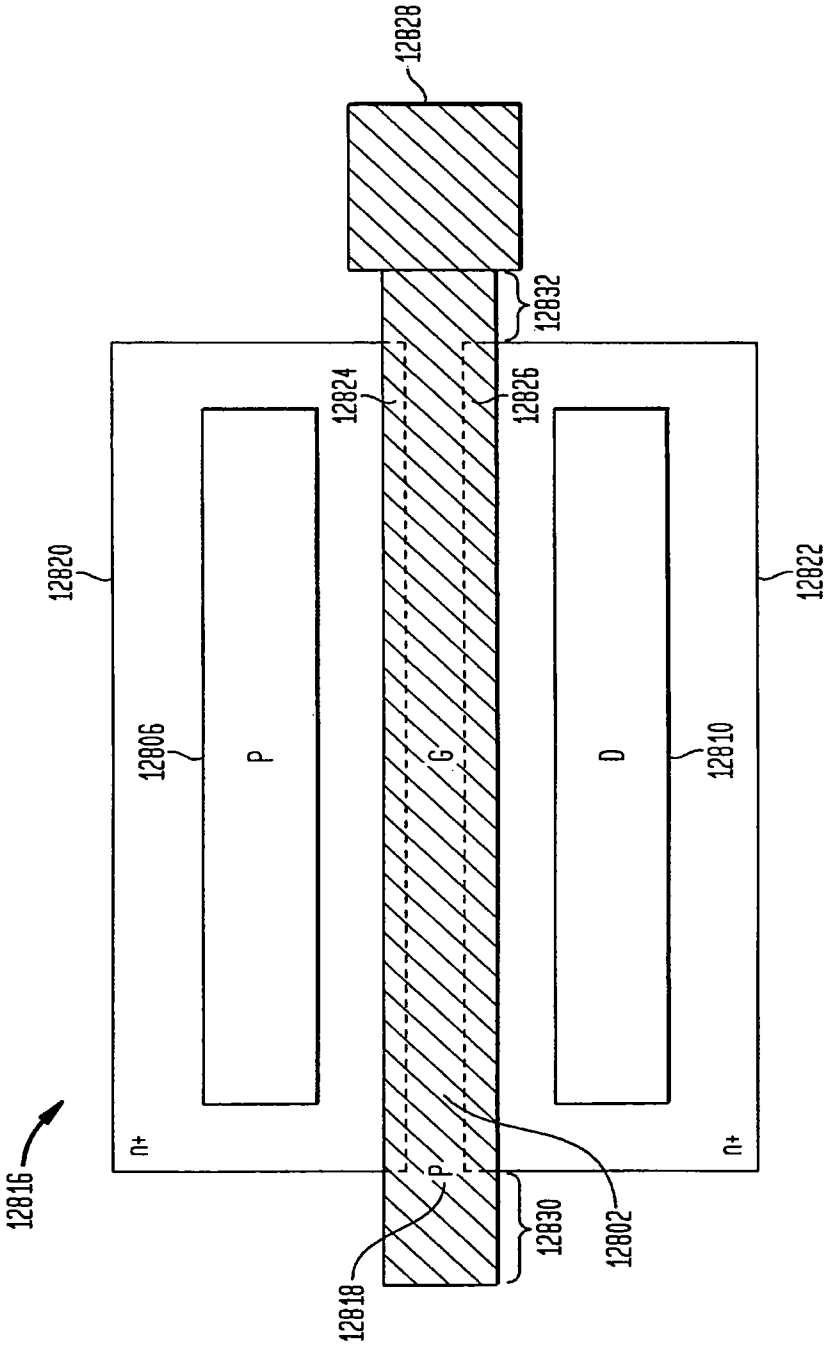

12828
12832
12824
12826
12820
12822
12806
P
G
D
12810
n+
n+
12816
P
12830
12802
12818

FIG. 128C

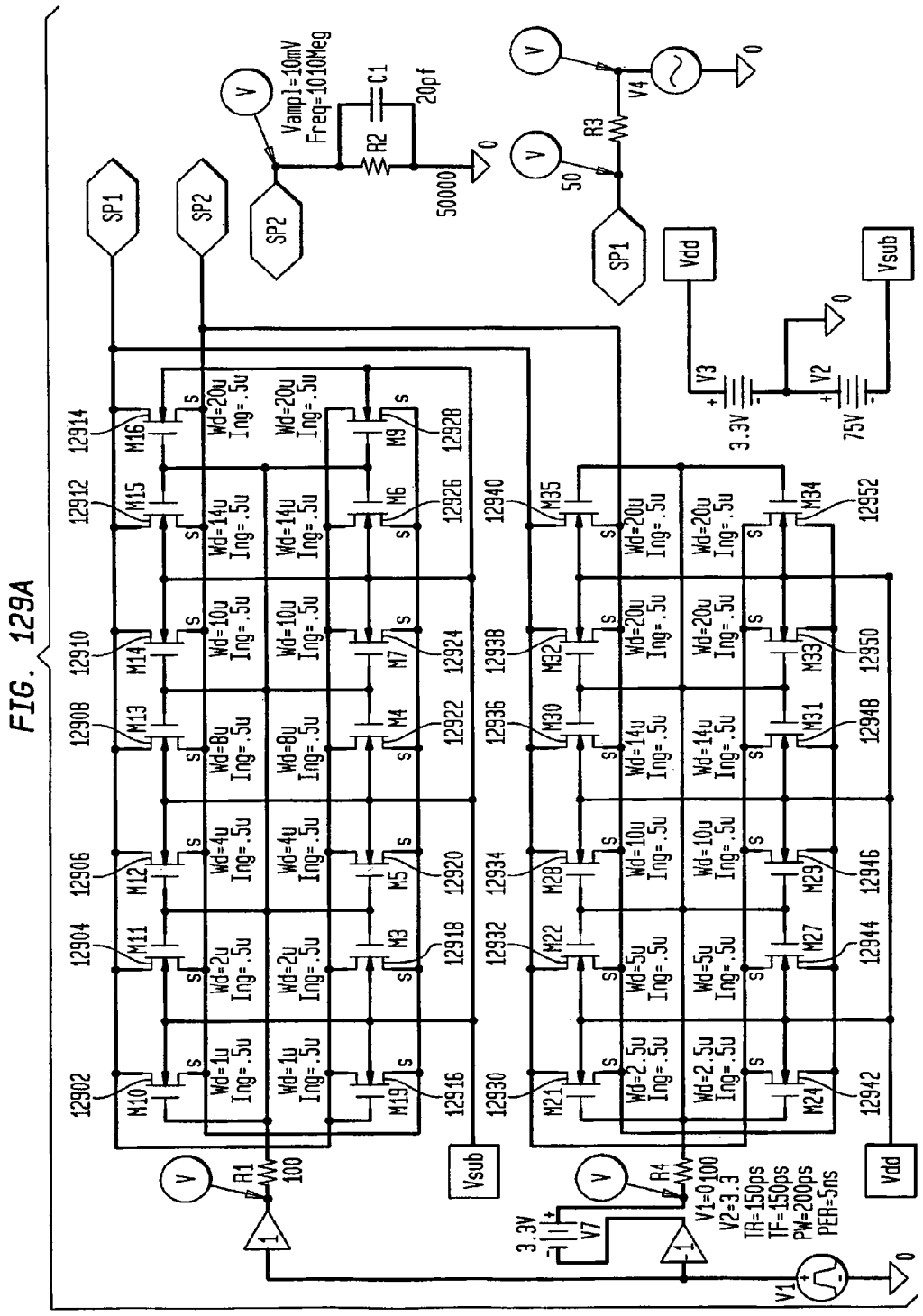

SP1
SP2
SP2
SP1
Vampl=10mV
Freq=1010Meg
C1
20pf
R2
50000
R3
50
V4
Vdd
Vsub
V3
3.3V
V2
75V
R1
100
R4
Vsub
Vdd
3.3V
V7
V1=0
V2=3.3
TR=150ps
TF=150ps
PW=200ps
PER=5ns
V1
12902
12904
12906
12908
12910
12912
12914
12916
12918
12920
12922
12924
12926
12928
12930
12932
12934
12936
12938
12940
12942
12944
12946
12948
12950
12952

FIG. 129A

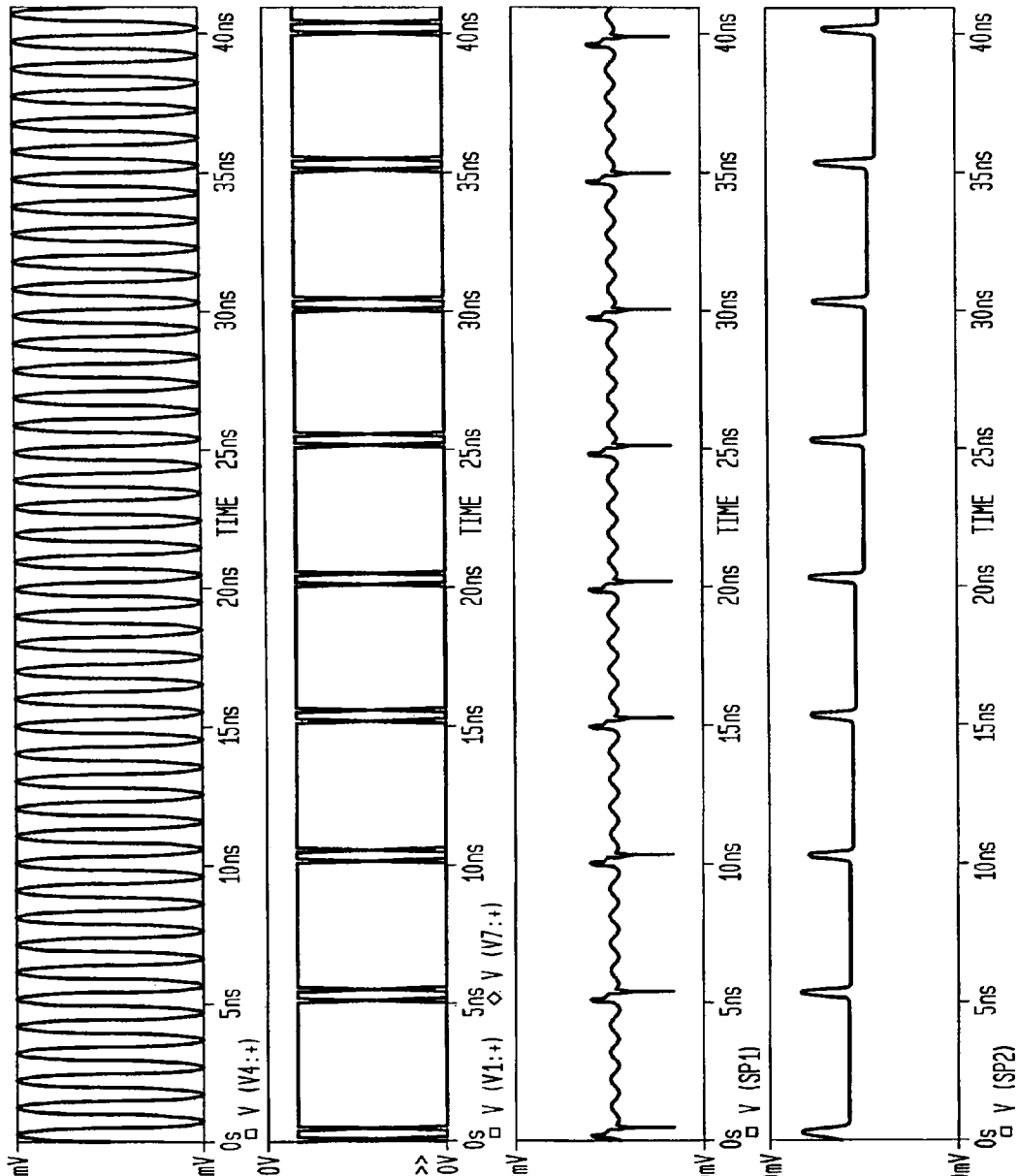
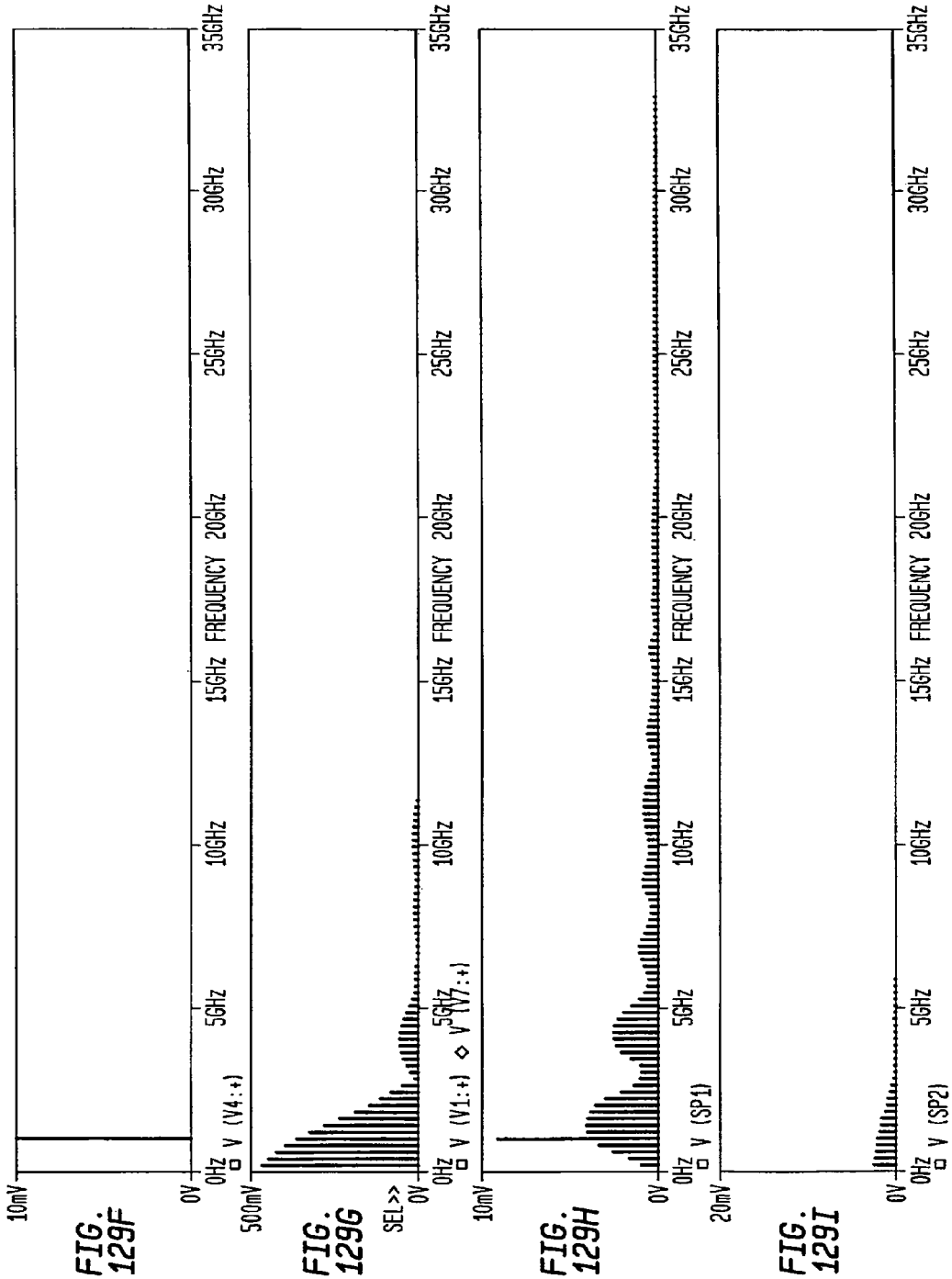


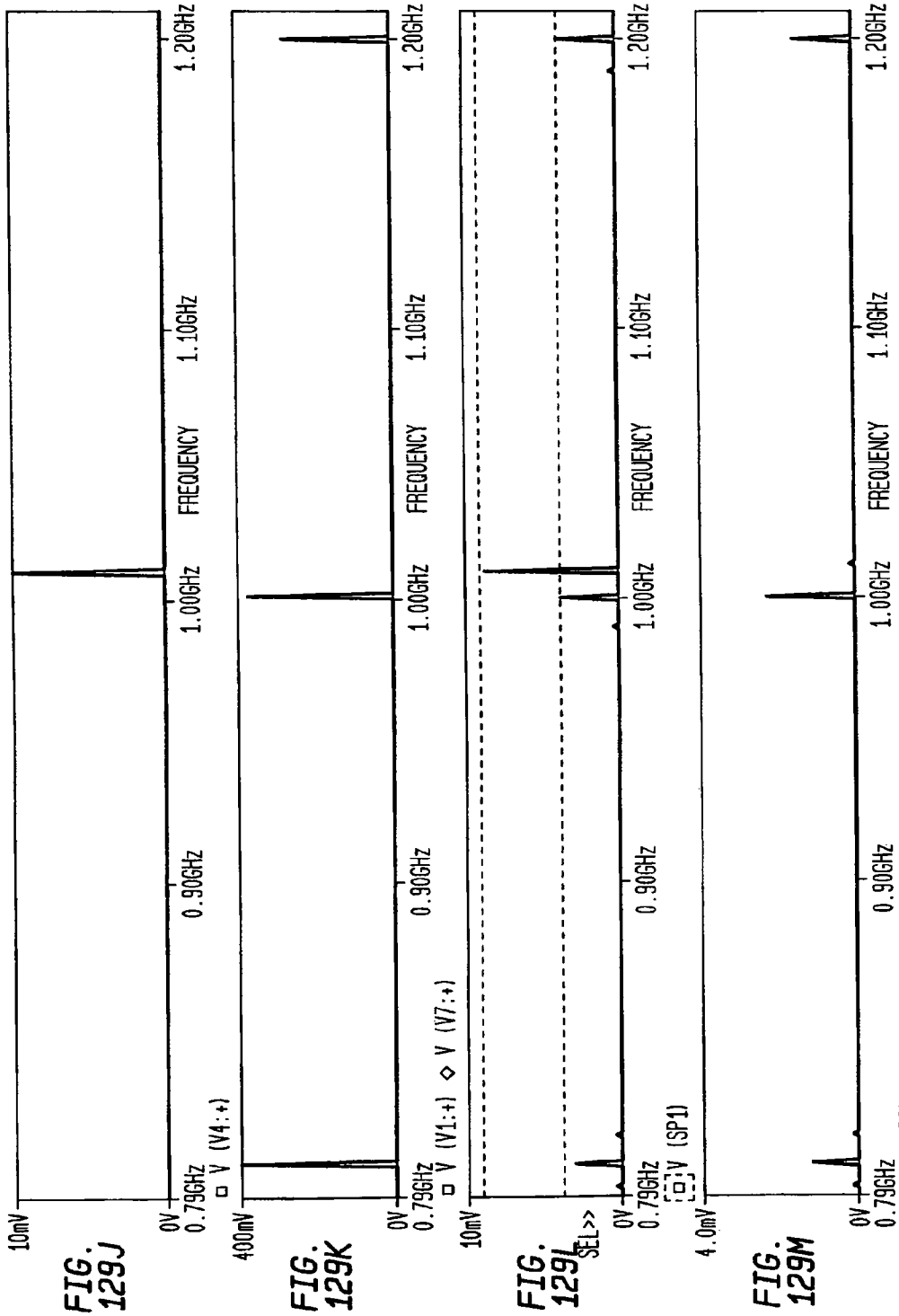
FIG. 129B

FIG. 129C

FIG. 129D

FIG. 129E


10mV
0V
0Hz
5GHz
10GHz
15GHz
20GHz
25GHz
30GHz
35GHz
FREQUENCY
V (V4:+)
FIG. 129F
500mV
0V
SEL>>
V (V1:+)
V (V7:+)
FIG. 129G
10mV
0V
FIG. 129H
20mV
0V
V (SP1)
FIG. 129I
V (SP2)


10mV
0V
0.79GHz
V (V4:+)
0.90GHz
1.00GHz
FREQUENCY
1.10GHz
1.20GHz
FIG. 129J
400mV
0V
0.79GHz
V (V1:+)
V (V7:+)
0.90GHz
1.00GHz
FREQUENCY
1.10GHz
1.20GHz
FIG. 129K
10mV
0V
0.79GHz
SEL>>
V (SP1)
0.90GHz
1.00GHz
FREQUENCY
1.10GHz
1.20GHz
FIG. 129L
4.0mV
0V
0.79GHz
V (SP2)
0.90GHz
1.00GHz
FREQUENCY
1.10GHz
1.20GHz
A1:(1.0000G, 3.9326m) A2:(788.000M, 9.0941u) DIFF(A):(212.000M, -3.9235m)
FIG. 129M

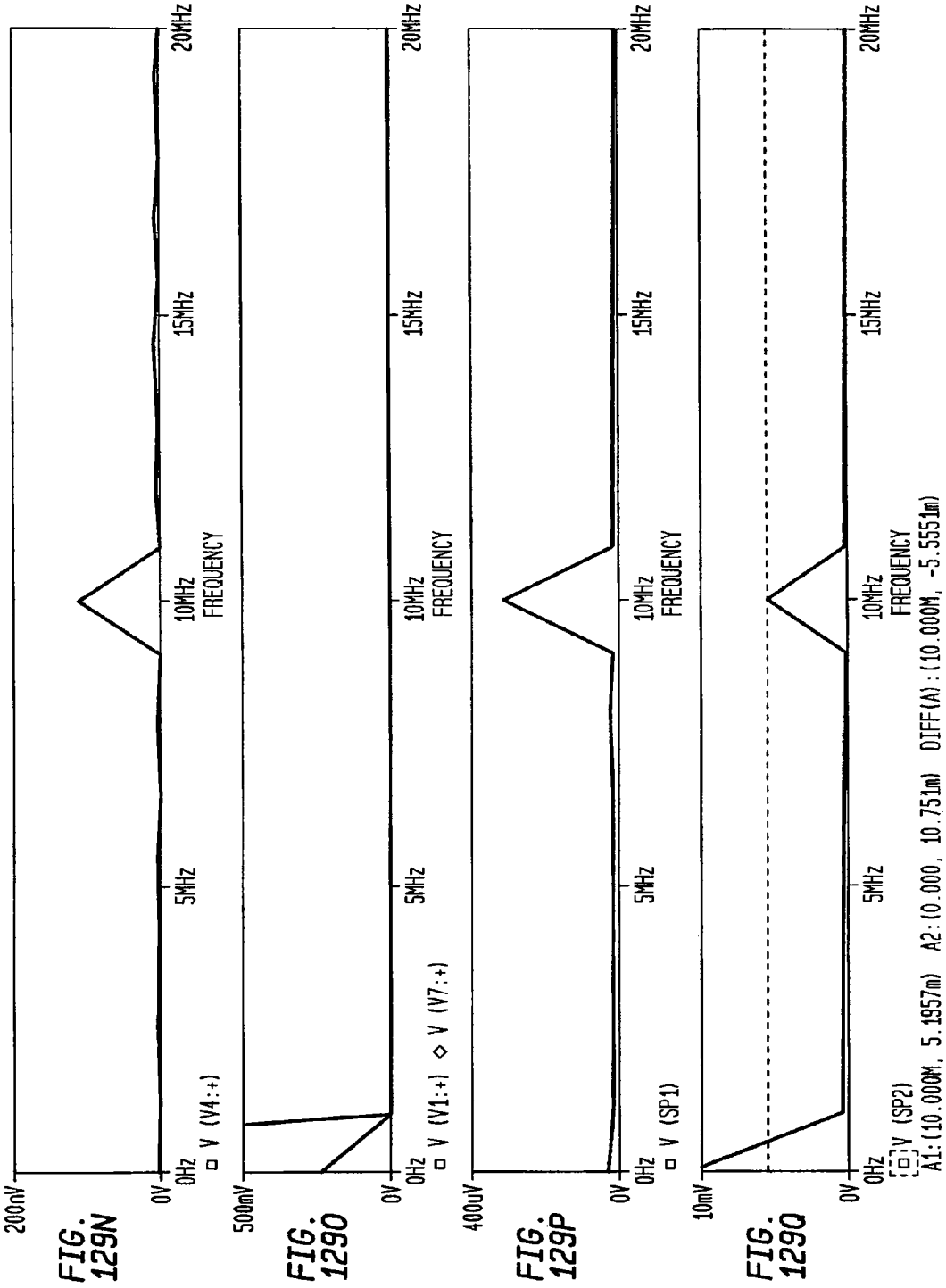
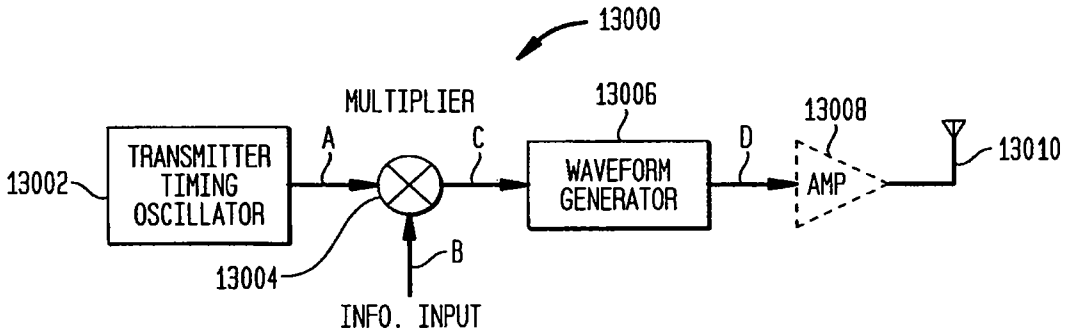

200nV
0V
0Hz
5MHz
10MHz
15MHz
20MHz
FREQUENCY
V (V4:+)
FIG. 129N
500mV
0V
0Hz
5MHz
10MHz
15MHz
20MHz
FREQUENCY
V (V1:+)
V (V7:+)
FIG. 129O
400uV
0V
0Hz
5MHz
10MHz
15MHz
20MHz
FREQUENCY
V (SP1)
FIG. 129P
10mV
0V
0Hz
5MHz
10MHz
15MHz
20MHz
FREQUENCY
V (SP2)
A1:(10.000M, 5.1957m) A2:(10.000, 10.751m) DIFF(A):(10.000M, -5.5551m)
FIG. 129Q

FIG. 130


13000
MULTIPLIER
13006
13008
13002
TRANSMITTER TIMING OSCILLATOR
A
C
WAVEFORM GENERATOR
D
AMP
13010
13004
B
INFO. INPUT

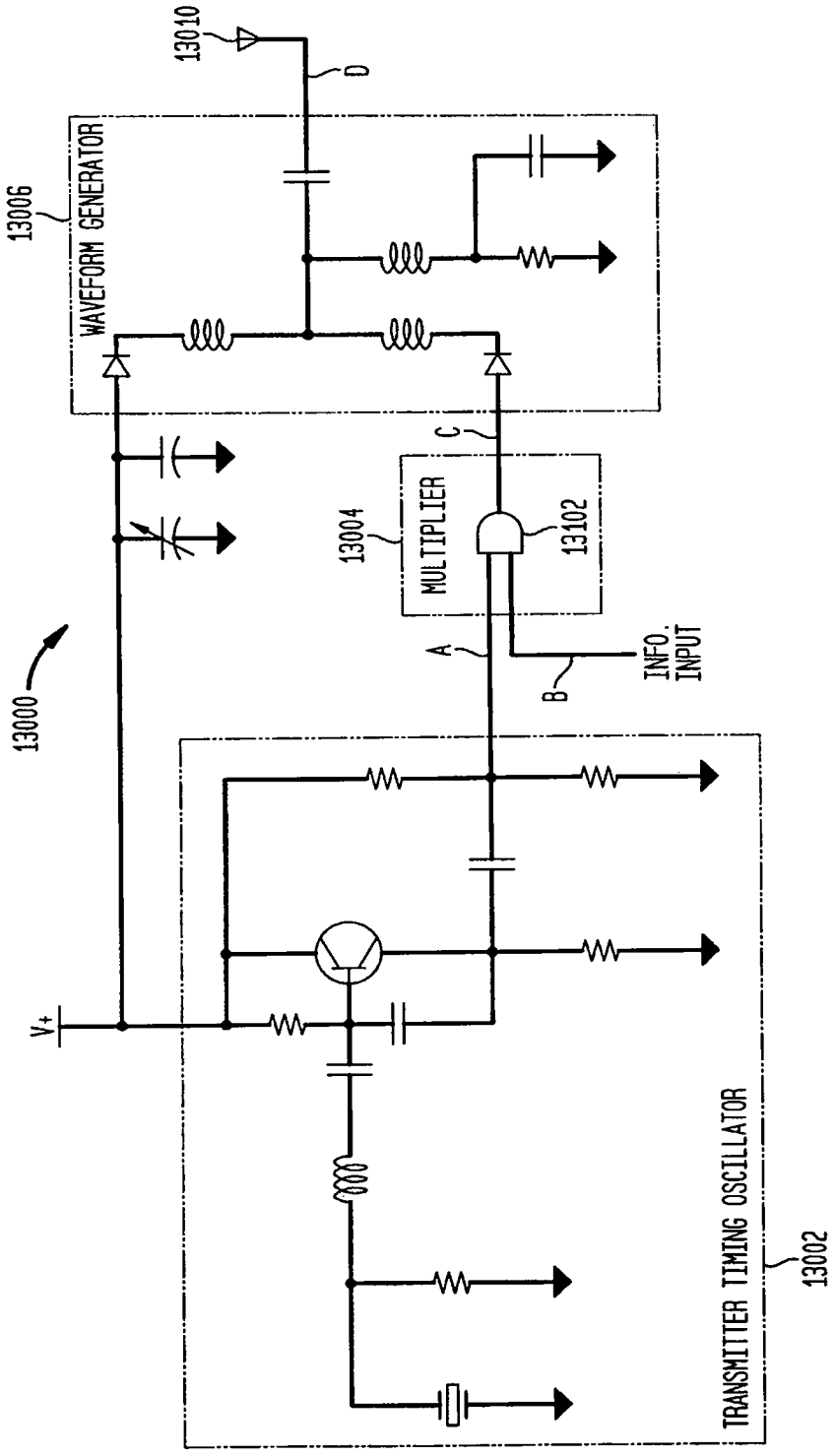

13010
D
13006
WAVEFORM GENERATOR
C
13004
MULTIPLIER
13102
A
B
INFO. INPUT
13000
V+
TRANSMITTER TIMING OSCILLATOR
13002

FIG. 131

FIG. 132A

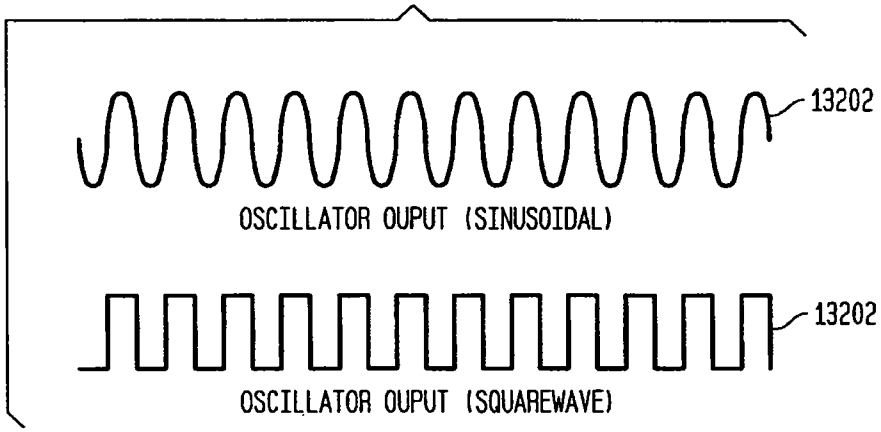


FIG. 132B

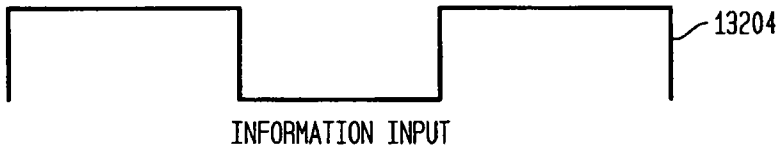


FIG. 132C

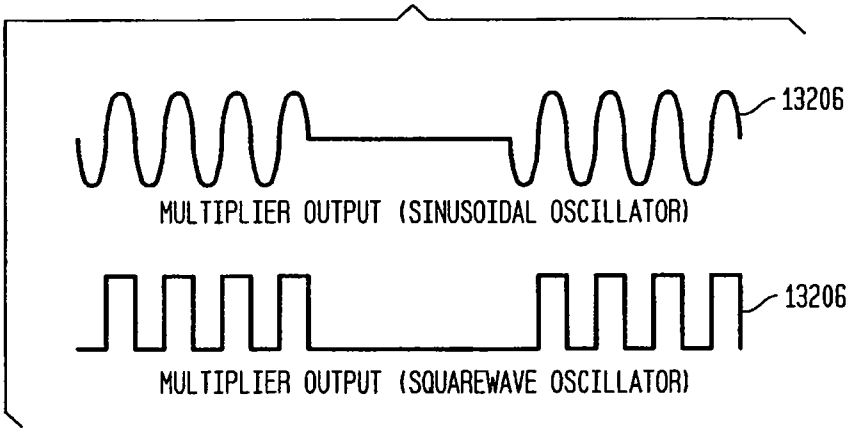
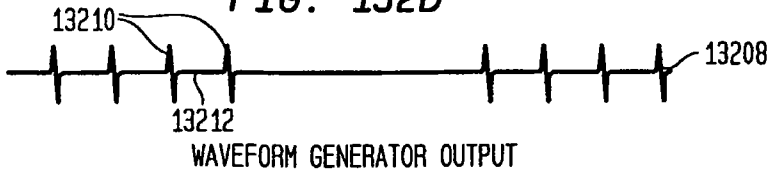


FIG. 132D



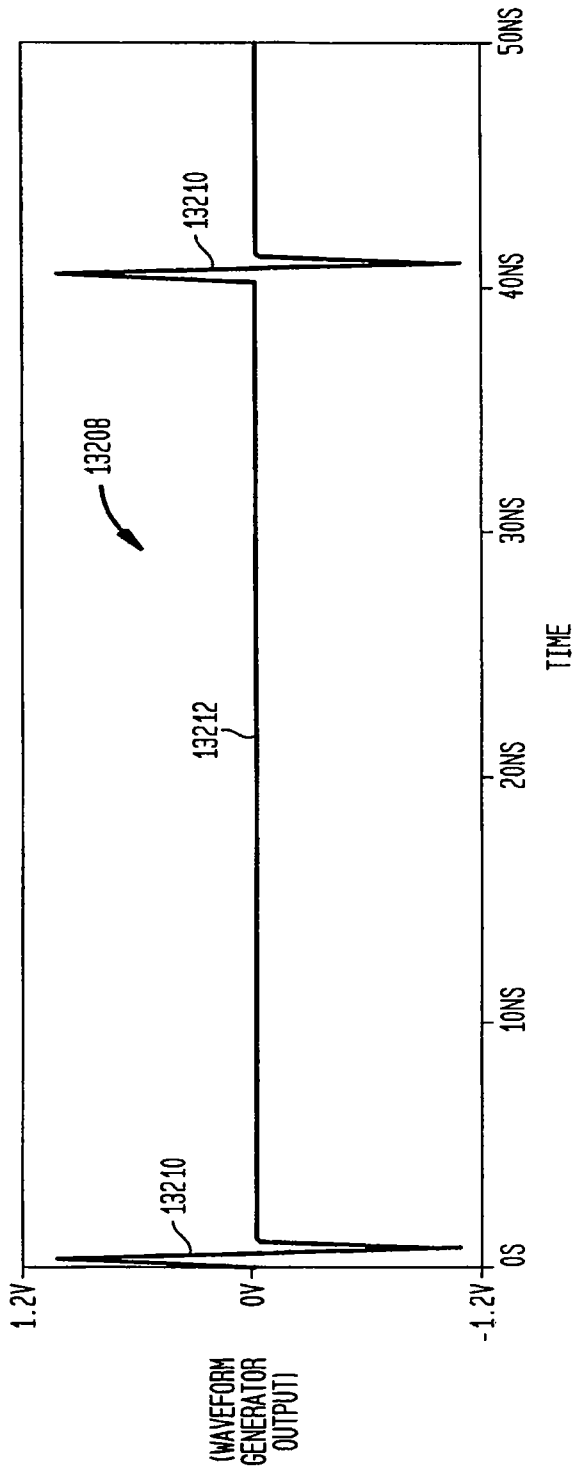

1.2V
0V
-1.2V
(WAVEFORM GENERATOR OUTPUT)
0S
10NS
20NS
30NS
40NS
50NS
TIME
13210
13212
13208
13210

FIG. 133

FIG. 134

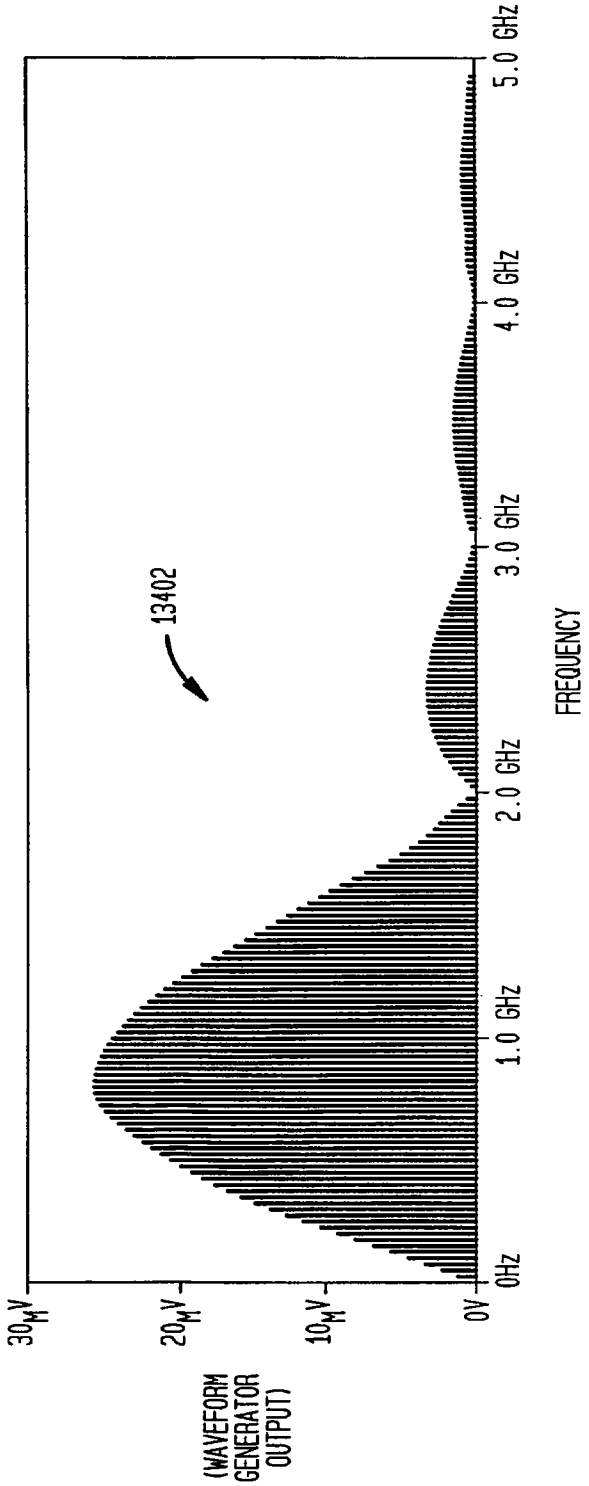

13402
30 MV
20 MV
10 MV
0V
(WAVEFORM GENERATOR OUTPUT)
0Hz
1.0 GHz
2.0 GHz
3.0 GHz
4.0 GHz
5.0 GHz
FREQUENCY

FIG. 135

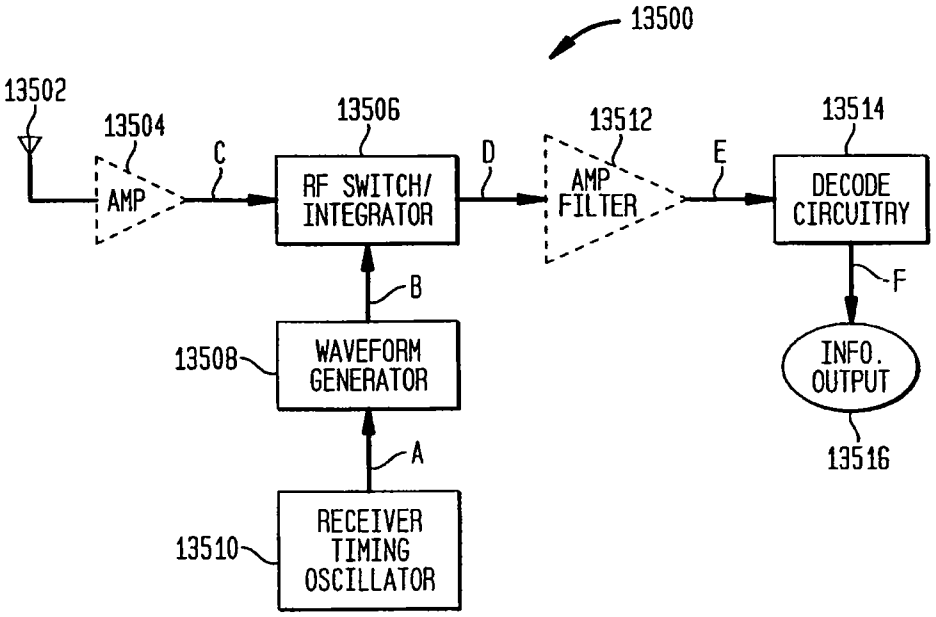
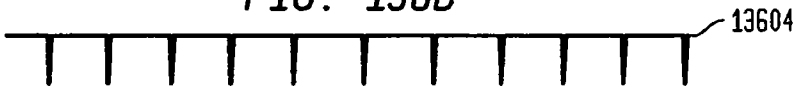

13500
13502
13504
AMP
C
13506
RF SWITCH/
INTEGRATOR
D
13512
AMP
FILTER
E
13514
DECODE
CIRCUITRY
F
INFO.
OUTPUT
13516
B
13508
WAVEFORM
GENERATOR
A
13510
RECEIVER
TIMING
OSCILLATOR

FIG. 136A



RECEIVER TIMING OSCILLATOR OUTPUT

FIG. 136B



WAVEFORM GENERATOR OUTPUT

FIG. 136C



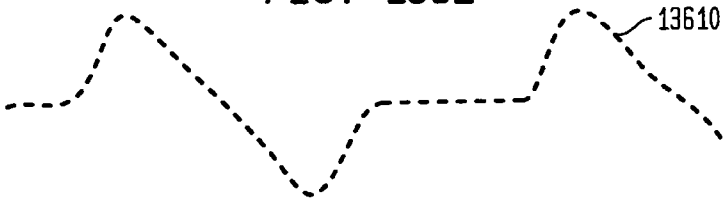
RF INPUT

FIG. 136D



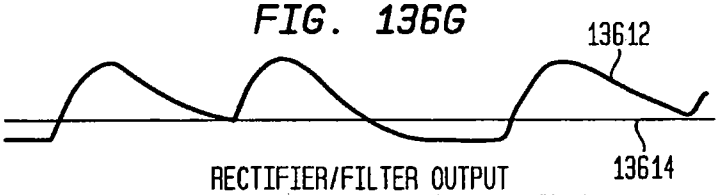
RF SWITCH/INTEGRATOR OUTPUT

FIG. 136E



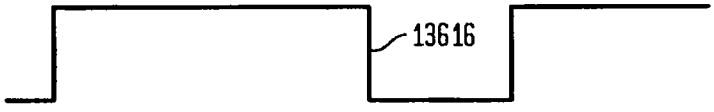
OPTIONAL AMPLIFIER/FILTER OUTPUT

FIG. 136G



RECTIFIER/FILTER OUTPUT
VARIABLE THRESHOLD GENERATOR OUTPUT

FIG. 136F



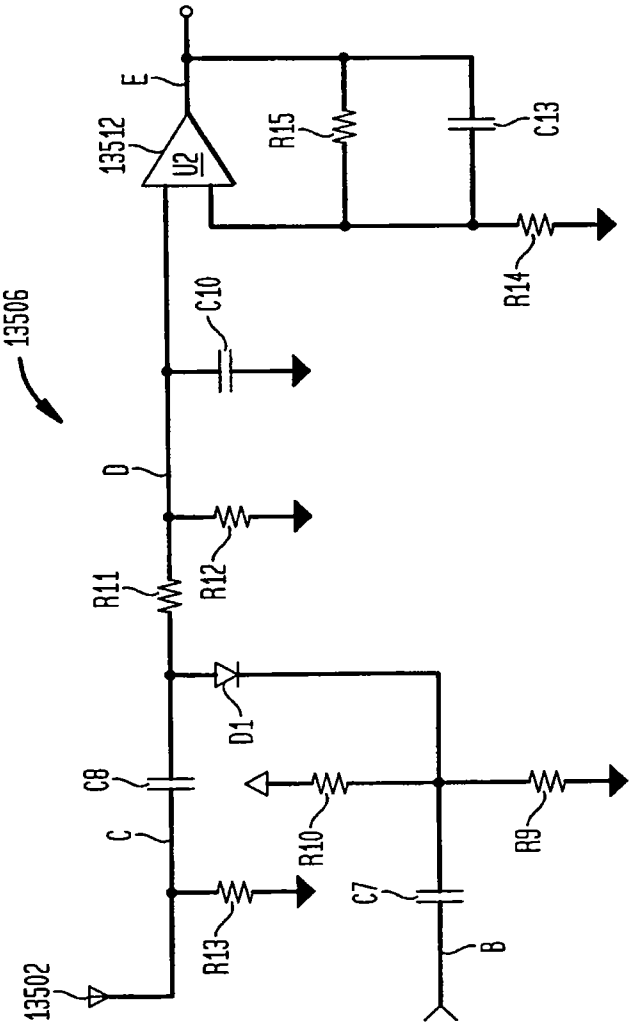

13506
E
13512
U2
R15
C13
R14
C10
D
R11
R12
D1
C8
C
R10
R9
C7
B
R13
13502

FIG. 137

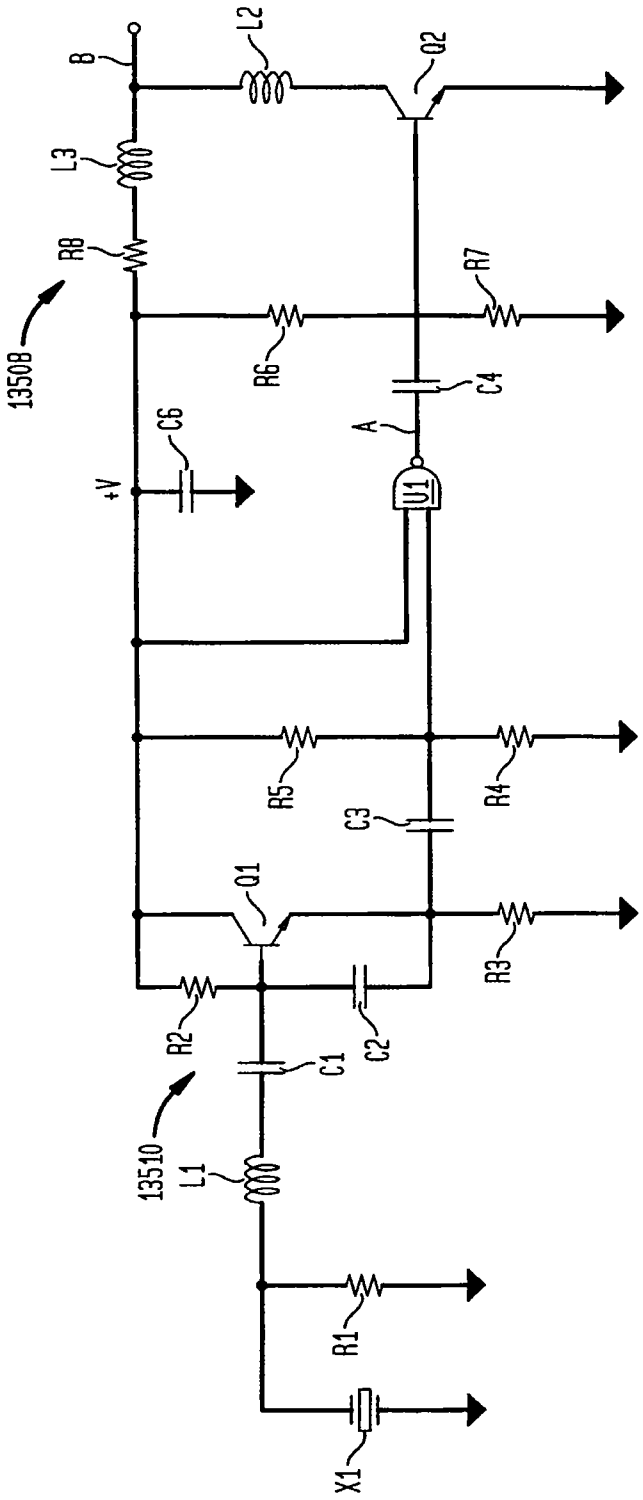

B
L2
Q2
L3
R8
13508
R7
R6
C4
A
C6
+V
U1
R5
R4
C3
Q1
R3
R2
C2
C1
13510
L1
R1
X1

FIG. 138

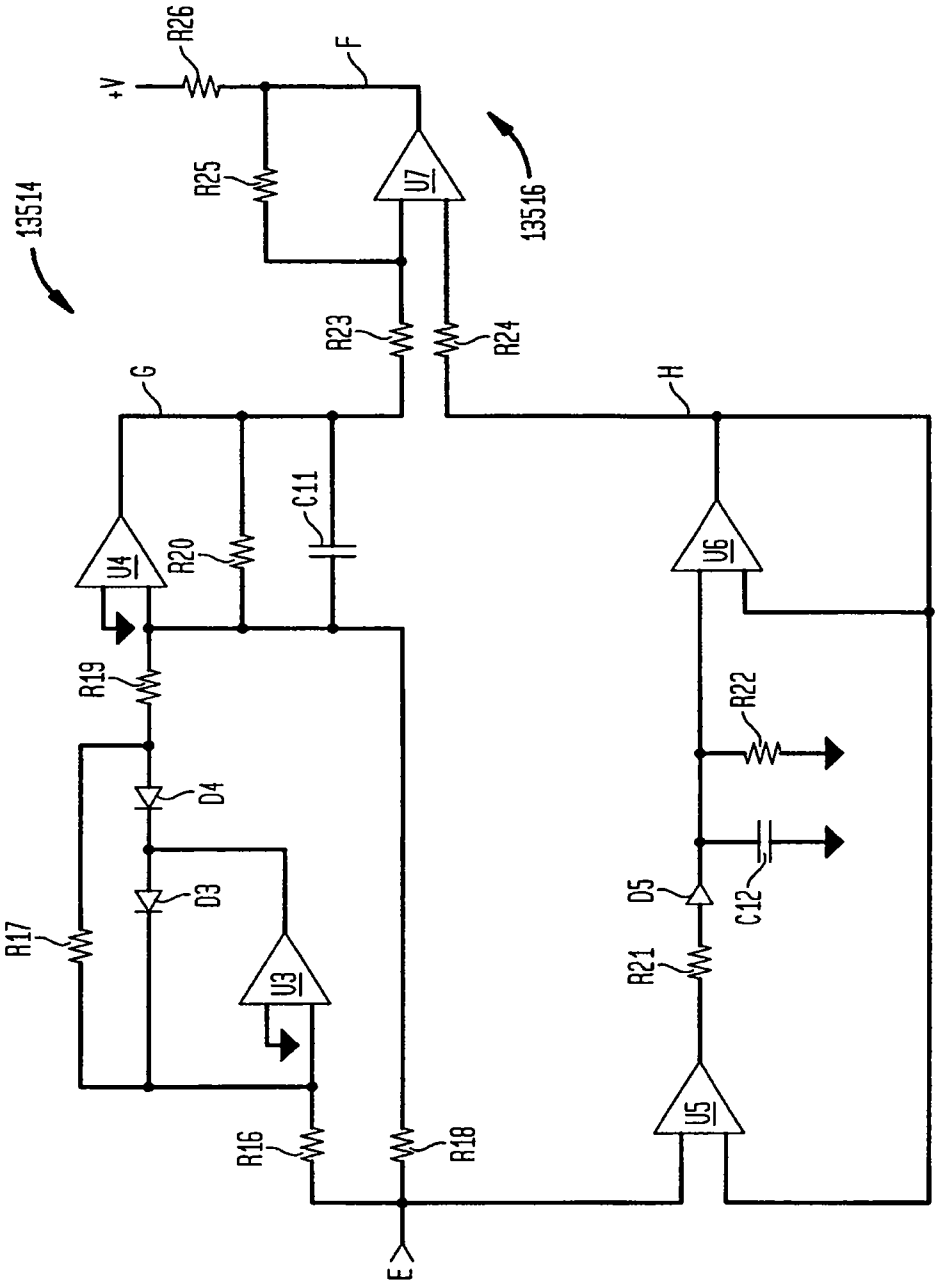

13514
13516
+V
R26
F
R25
U7
R23
R24
G
H
C11
U4
R20
U6
R19
R22
D4
D3
C12
D5
R17
U3
R21
U5
R16
R18
E

FIG. 139

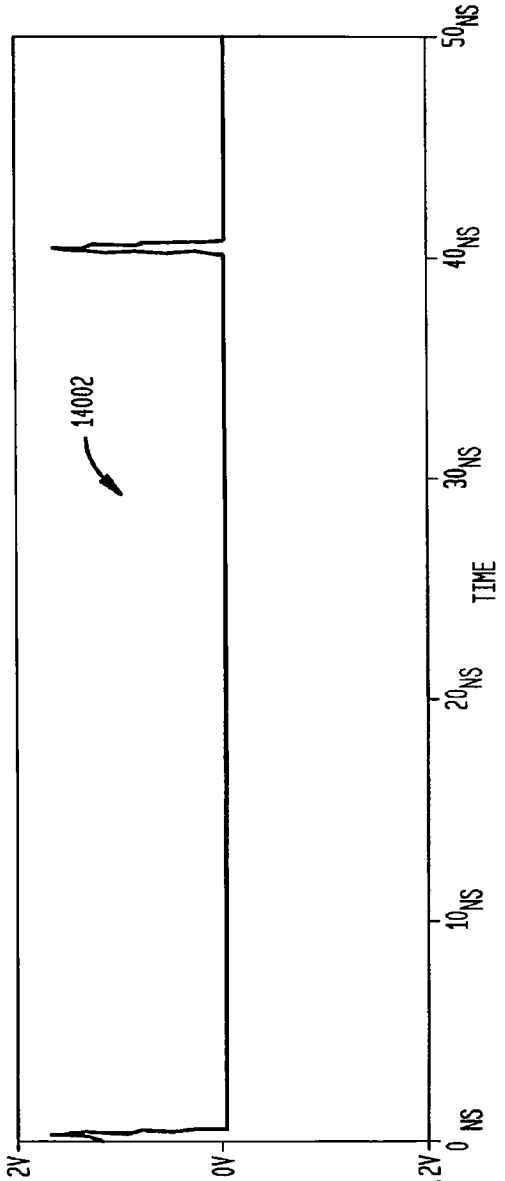


FIG. 140

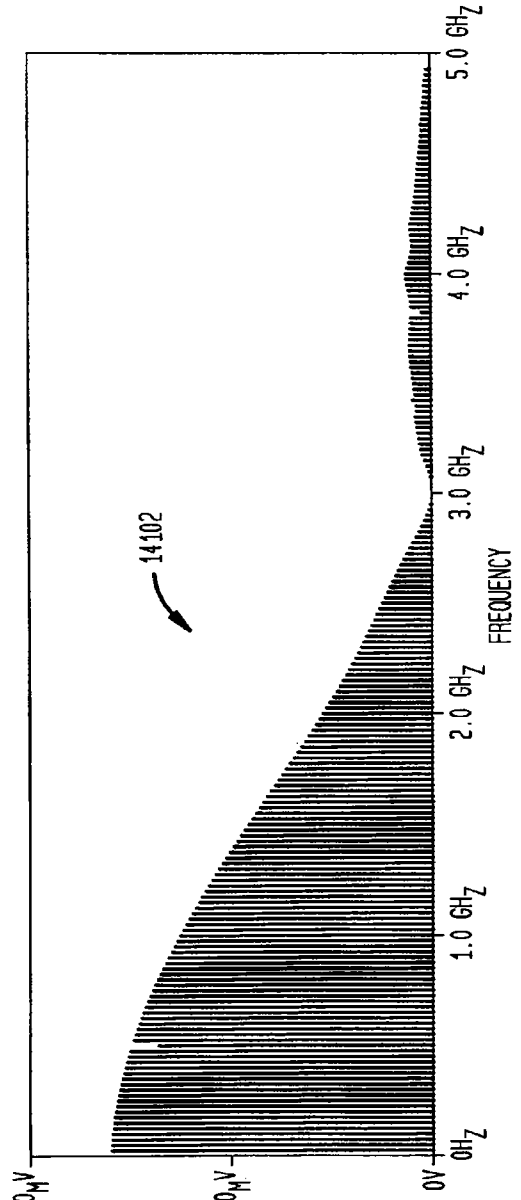


FIG. 141

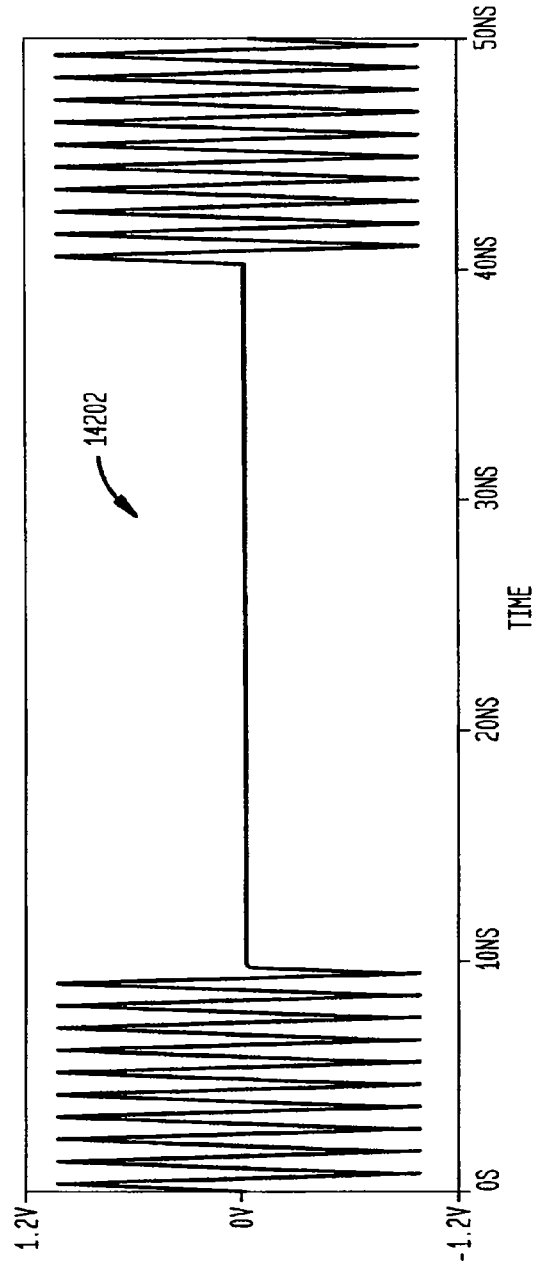


FIG. 142

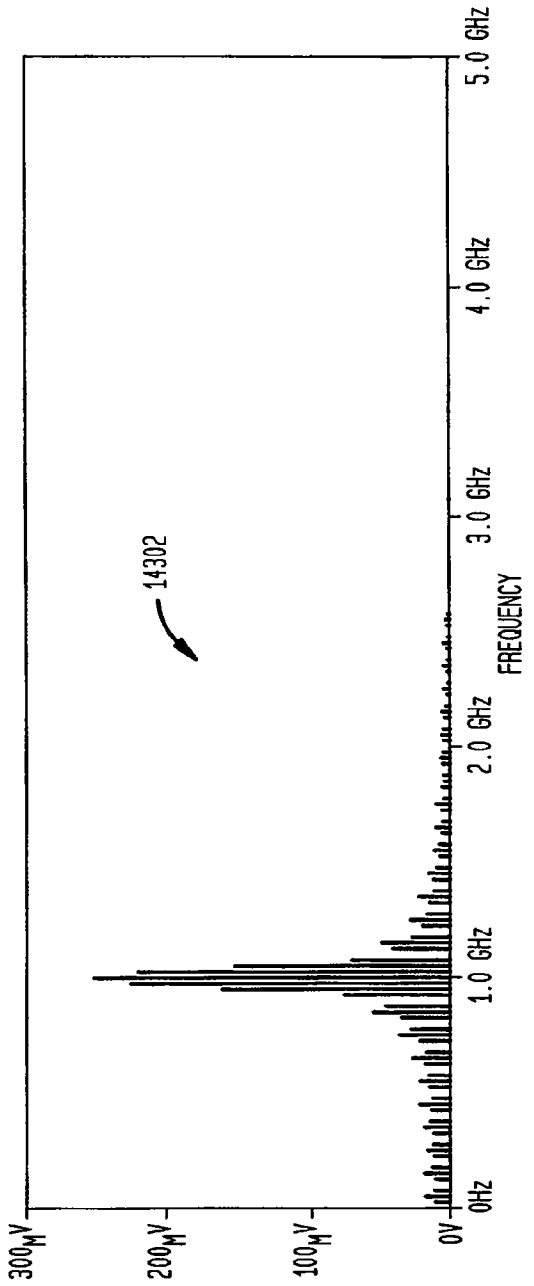


FIG. 143

FIG. 144

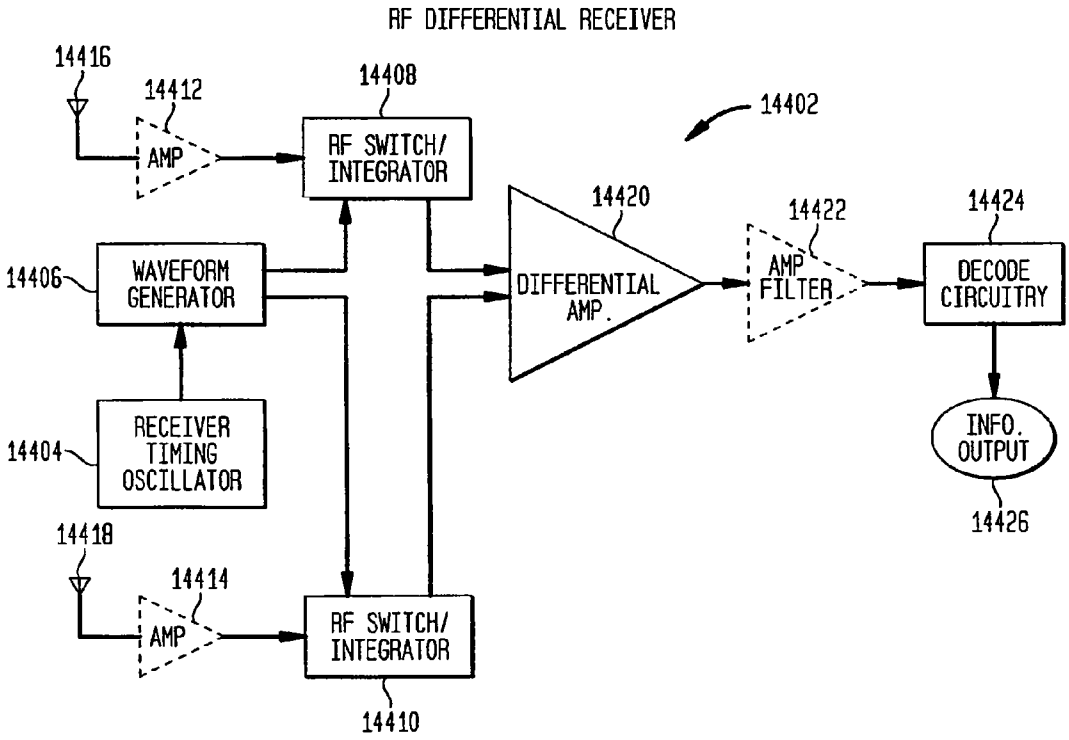
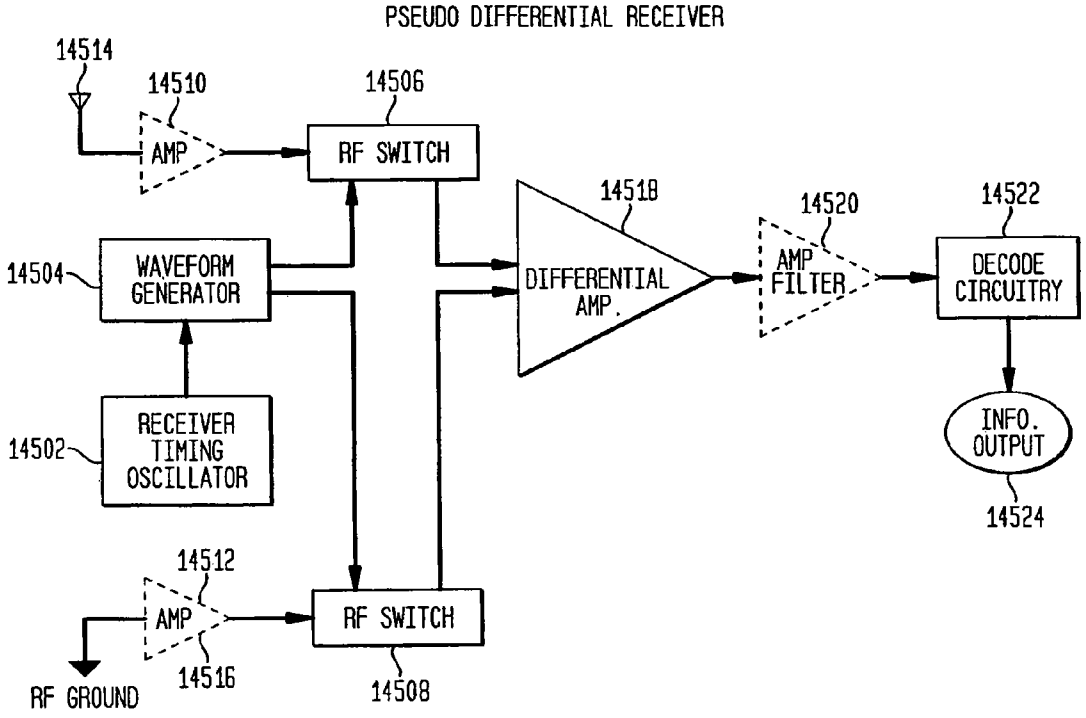

RF DIFFERENTIAL RECEIVER
14416
14412
AMP
14408
RF SWITCH/ INTEGRATOR
14402
14420
14422
14424
14406
WAVEFORM GENERATOR
DIFFERENTIAL AMP.
AMP FILTER
DECODE CIRCUITRY
RECEIVER TIMING OSCILLATOR
14404
INFO. OUTPUT
14426
14418
14414
AMP
RF SWITCH/ INTEGRATOR
14410

FIG. 145


PSEUDO DIFFERENTIAL RECEIVER
14514
14510
AMP
14506
RF SWITCH
14518
DIFFERENTIAL AMP.
14520
AMP FILTER
14522
DECODE CIRCUITRY
INFO. OUTPUT
14524
14504
WAVEFORM GENERATOR
14502
RECEIVER TIMING OSCILLATOR
14512
AMP
14516
RF GROUND
RF SWITCH
14508

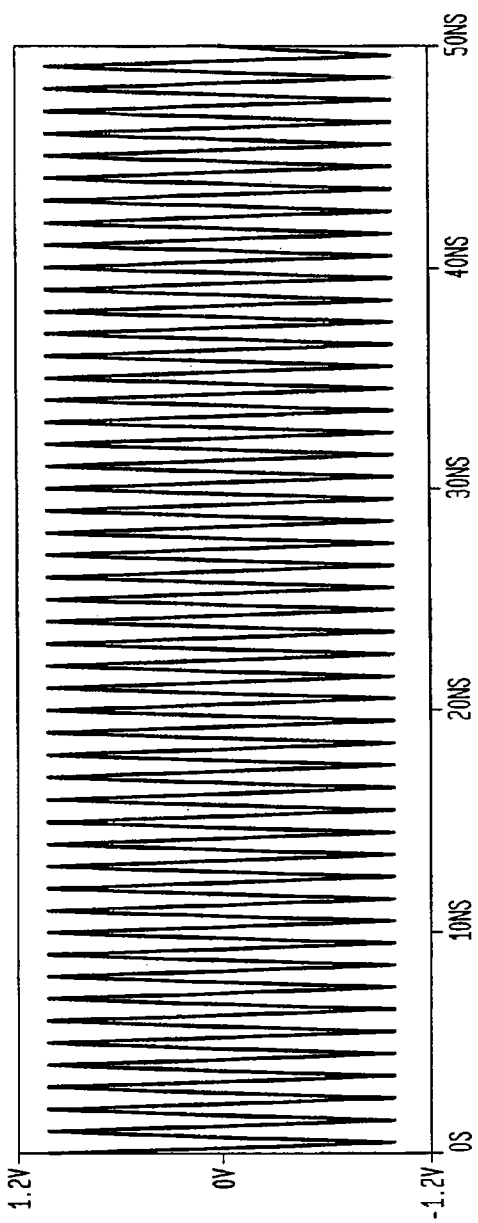


FIG. 146

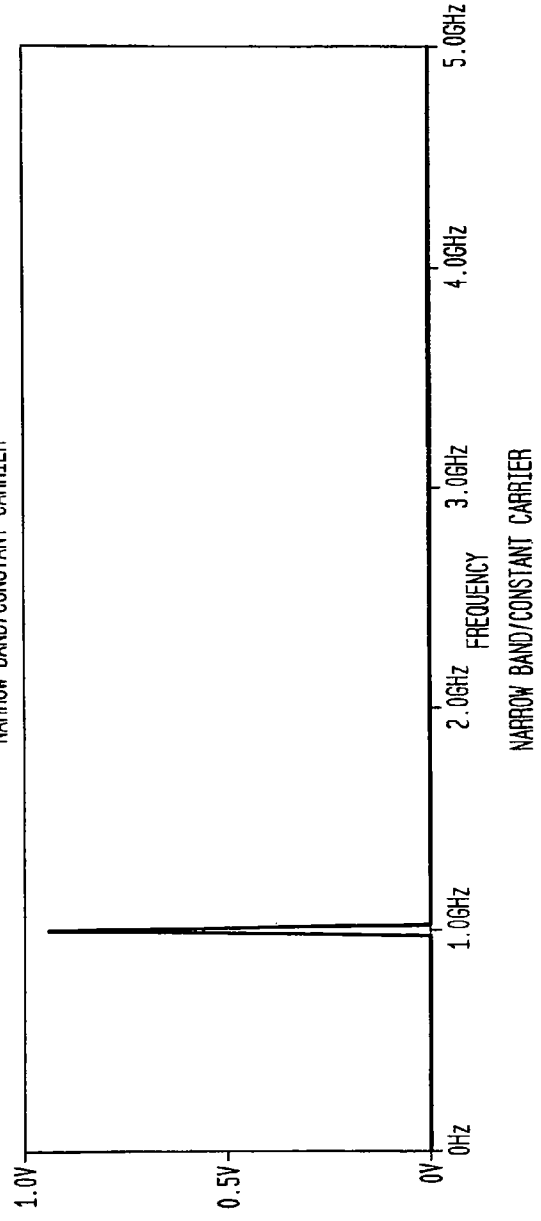


FIG. 147

FIG. 148

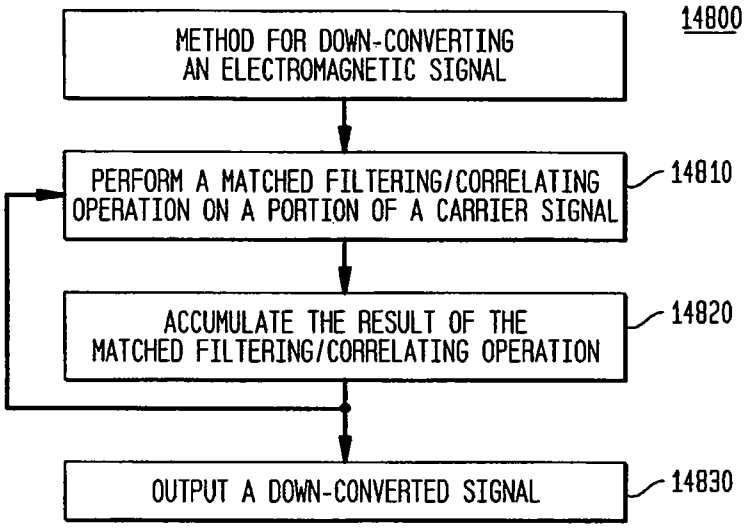


FIG. 149

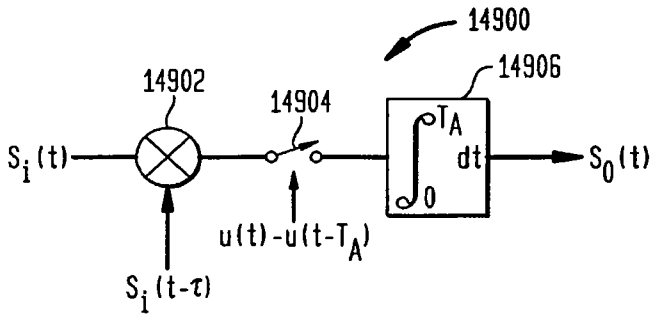


FIG. 150

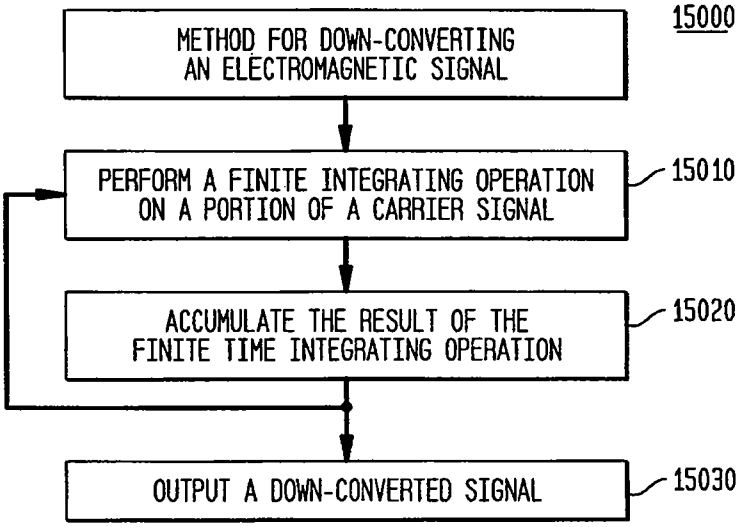


FIG. 151

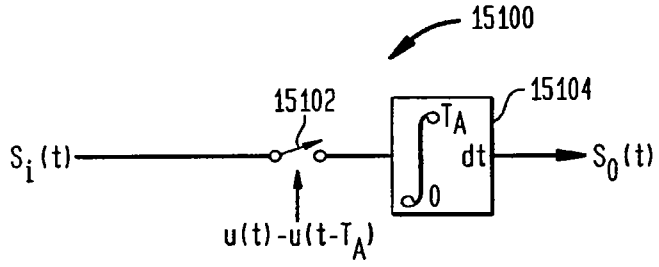


FIG. 152

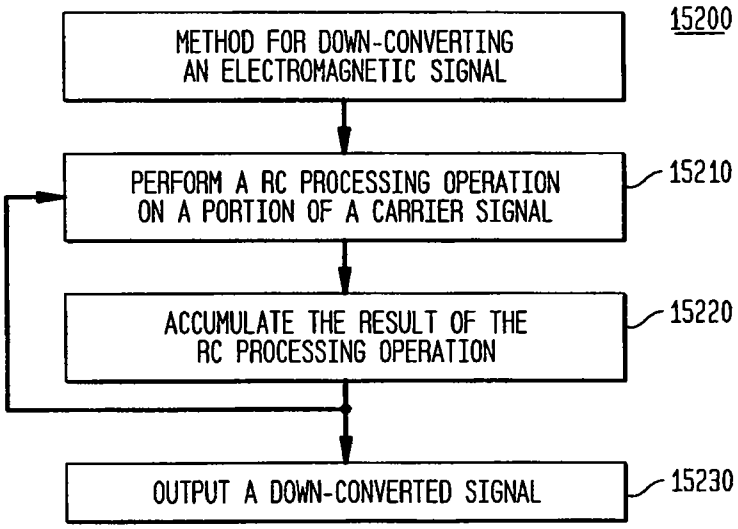


FIG. 153

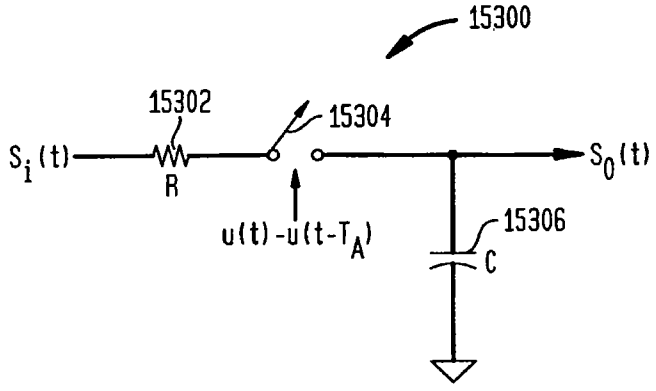


FIG. 154

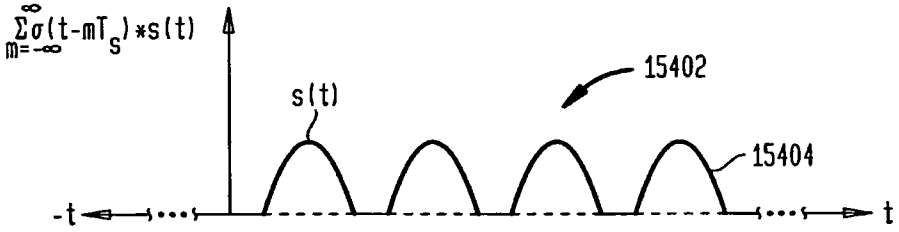


FIG. 155

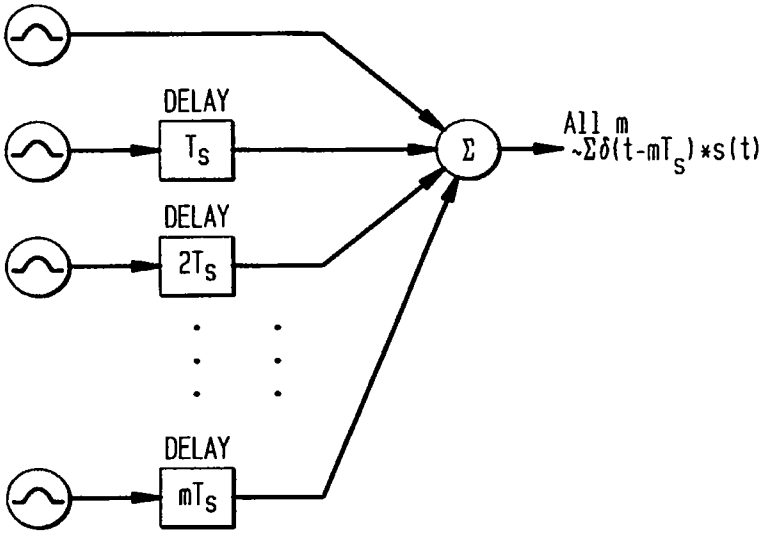


FIG. 156

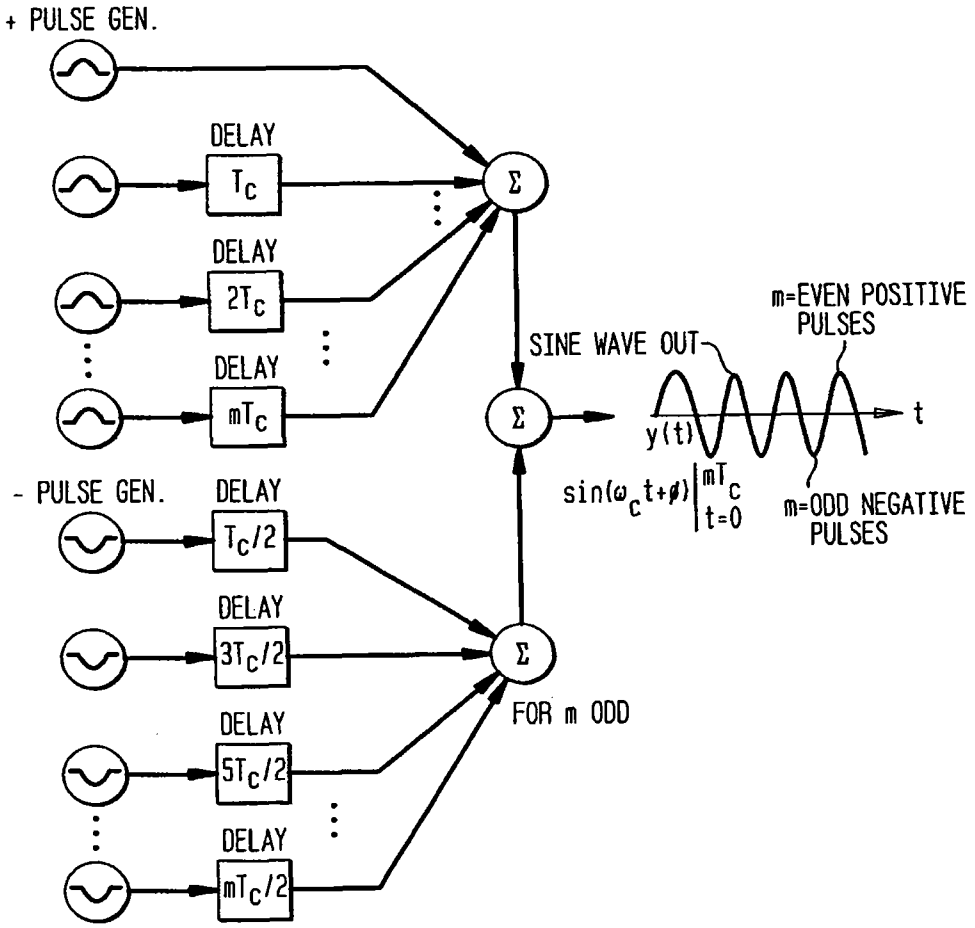
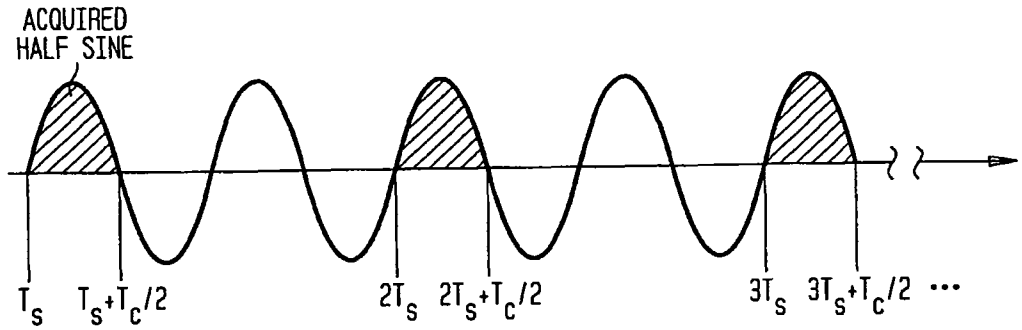


FIG. 157



CARRIER PROCESSED BY 3RD HARMONIC UFT PROCESSOR

FIG. 158

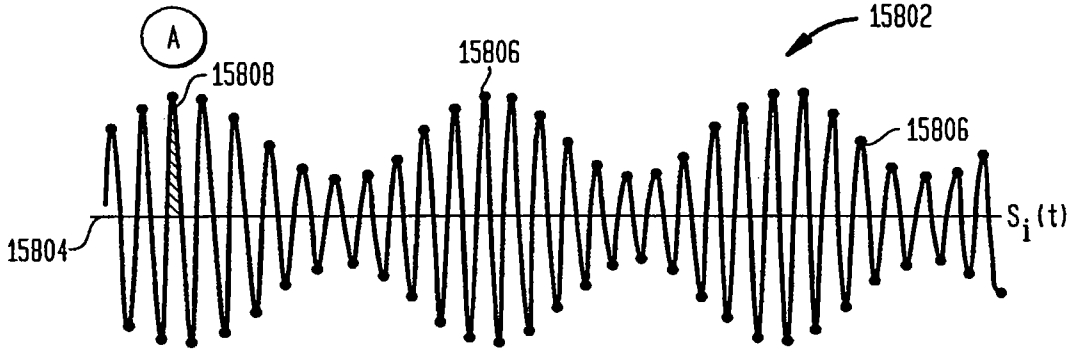


FIG. 159

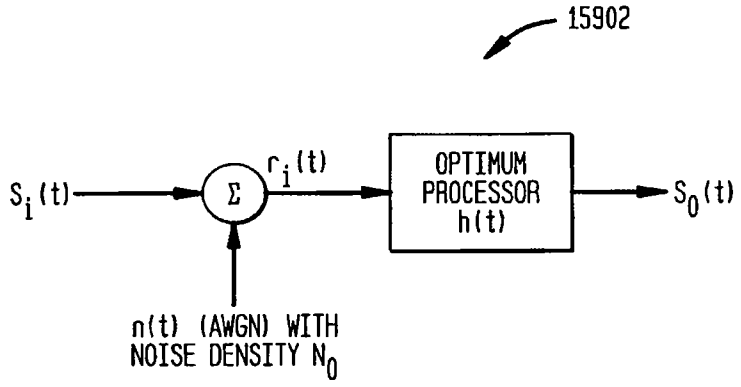
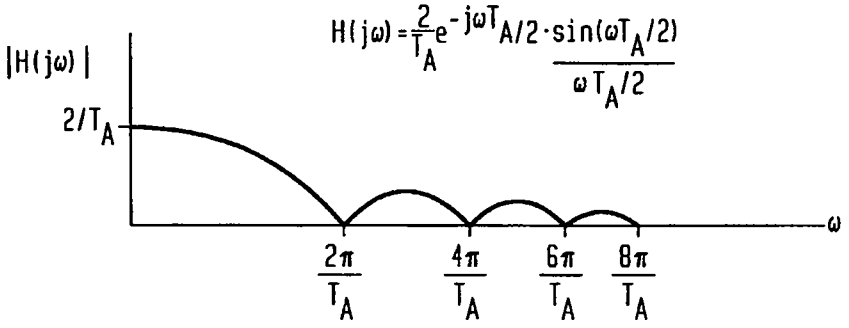
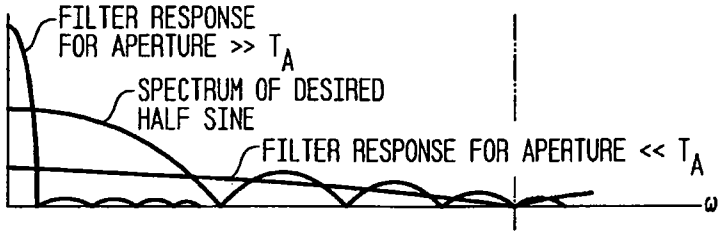


FIG. 160



MAG FREQUENCY RESPONSE OF SAMPLING APERTURE WAVEFORM

FIG. 161



APERTURE FREQUENCY DOMAIN REPRESENTATION

FIG. 162

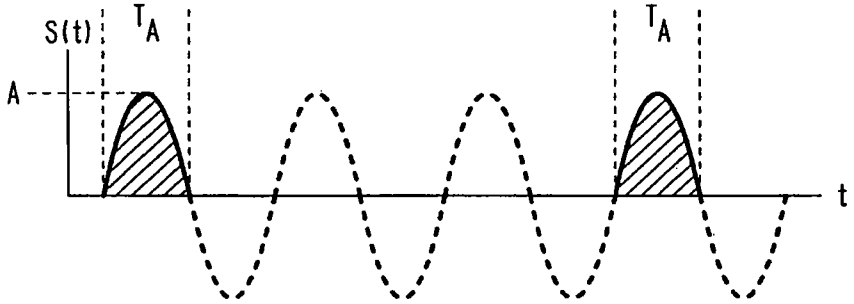


FIG. 163

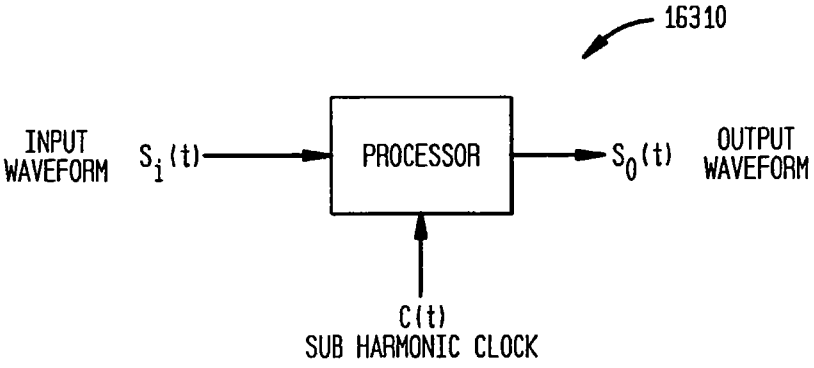


FIG. 164A

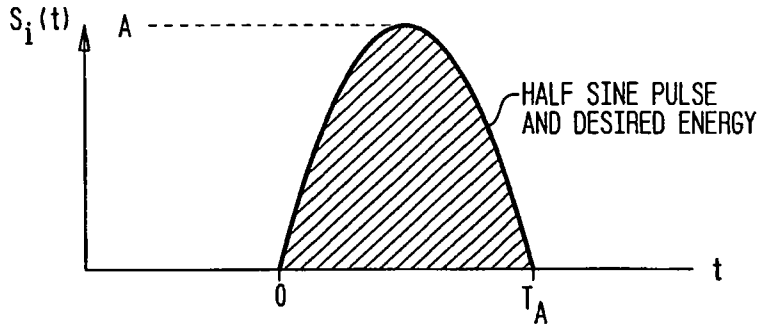


FIG. 164B

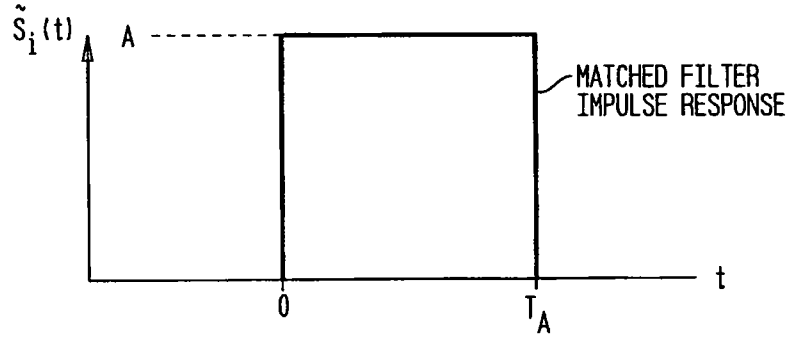


FIG. 164C

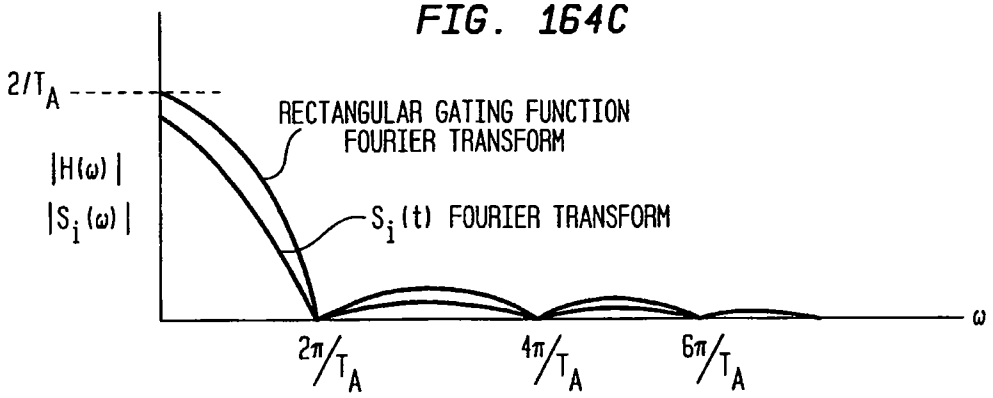


FIG. 165

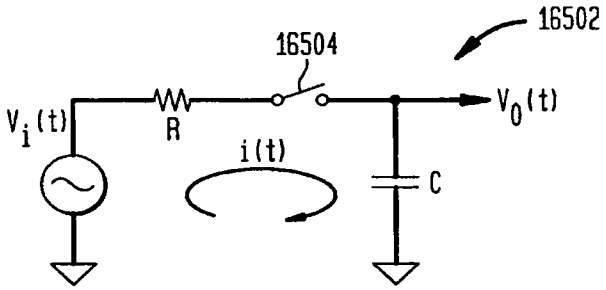


FIG. 166

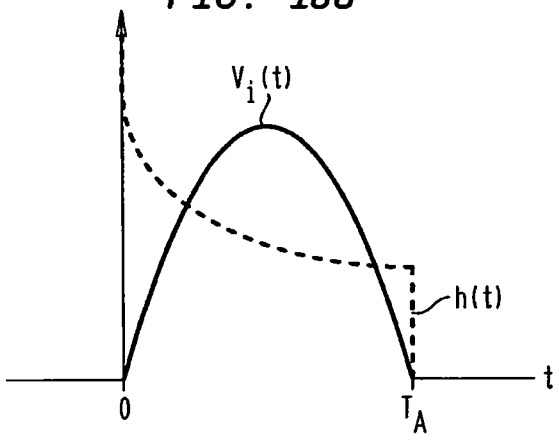


FIG. 167

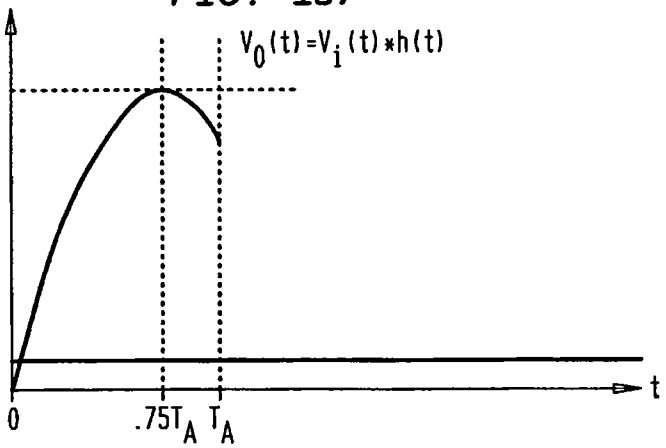


FIG. 168

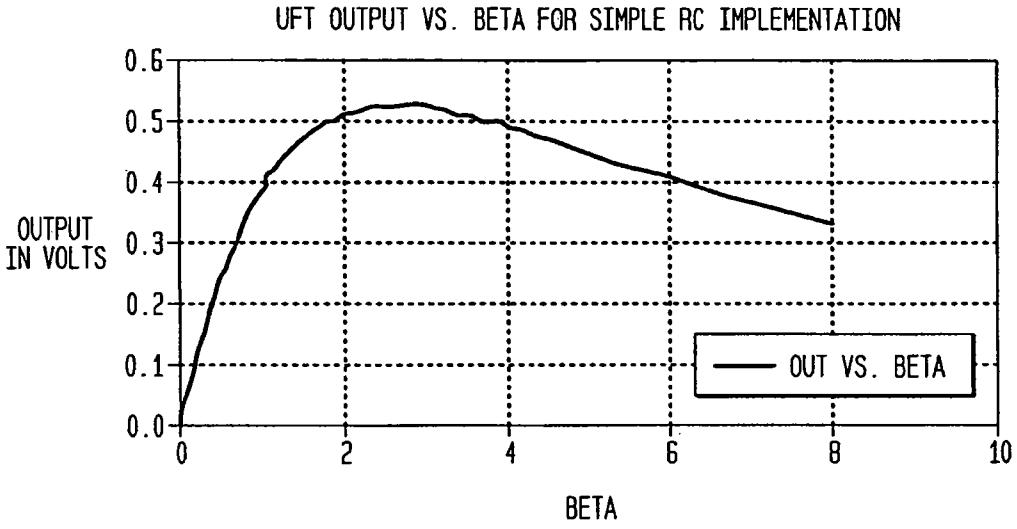


FIG. 169

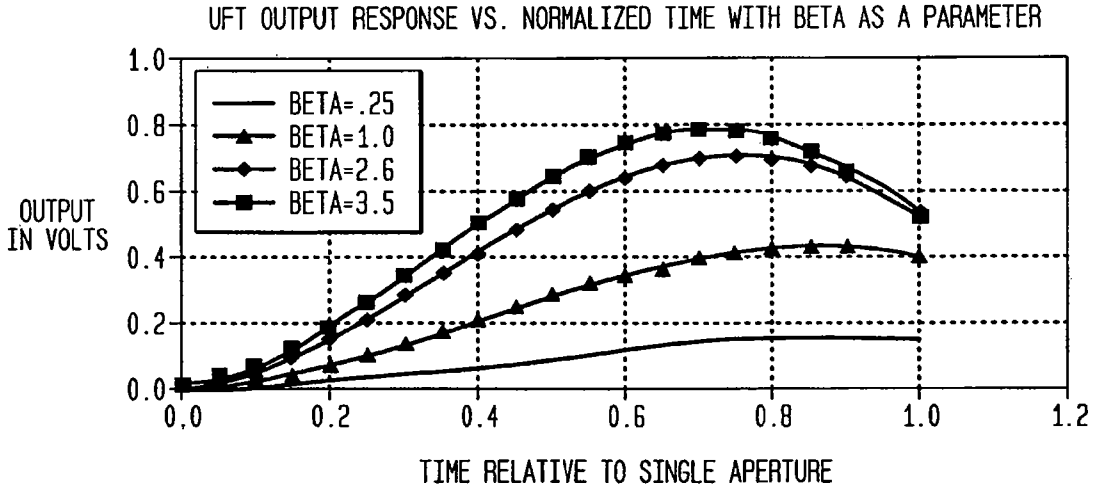


FIG. 170

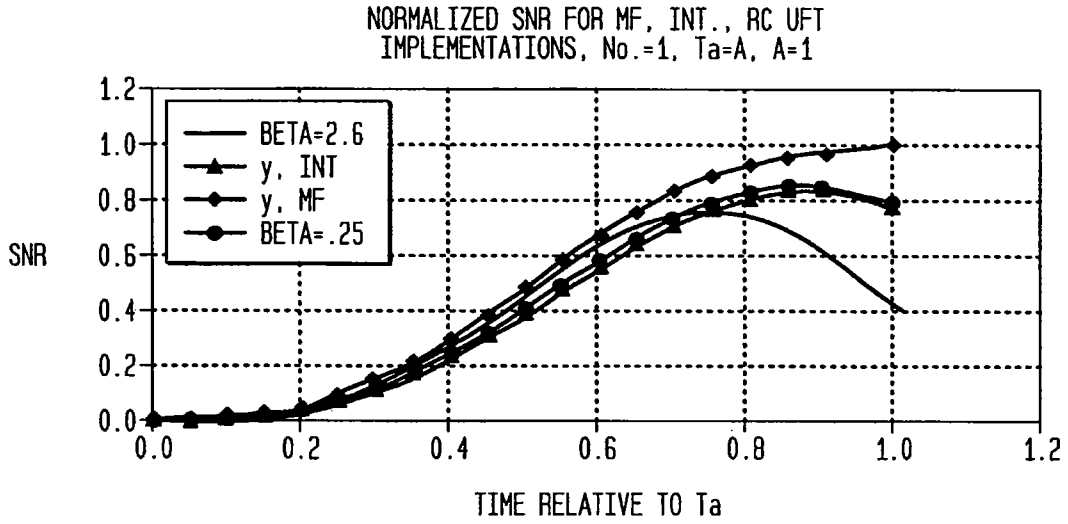


FIG. 171

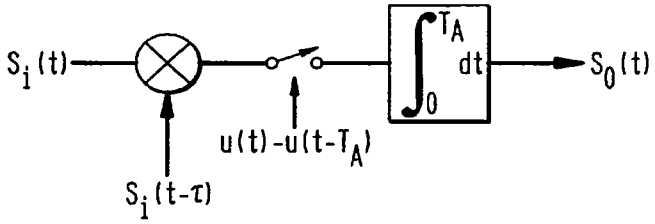


FIG. 172

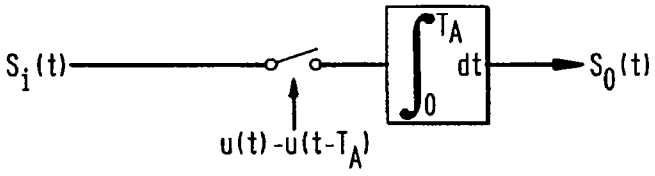


FIG. 173

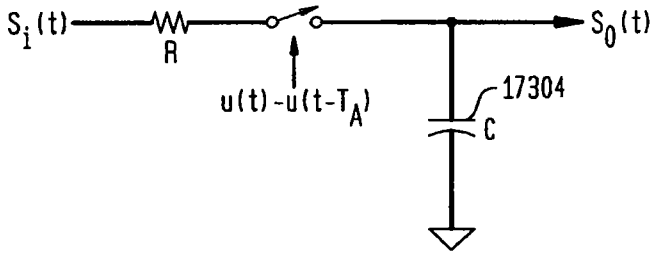


FIG. 174

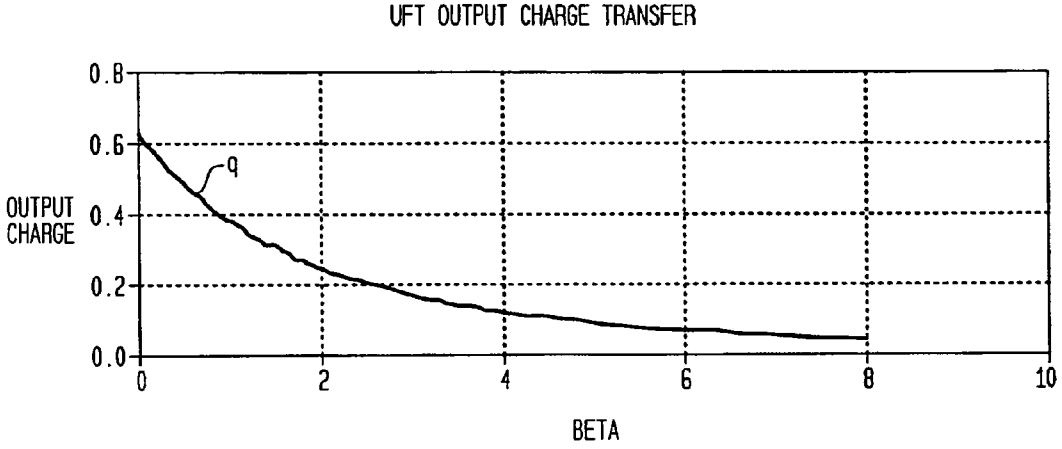


FIG. 175A

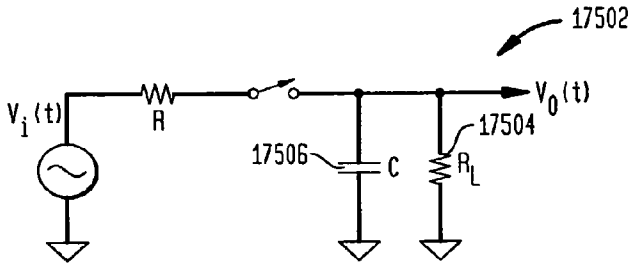


FIG. 175B

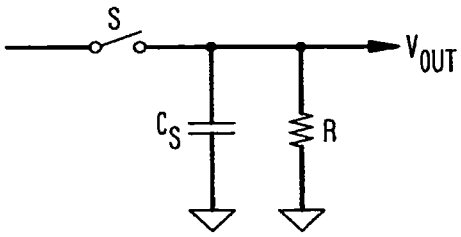


FIG. 175C

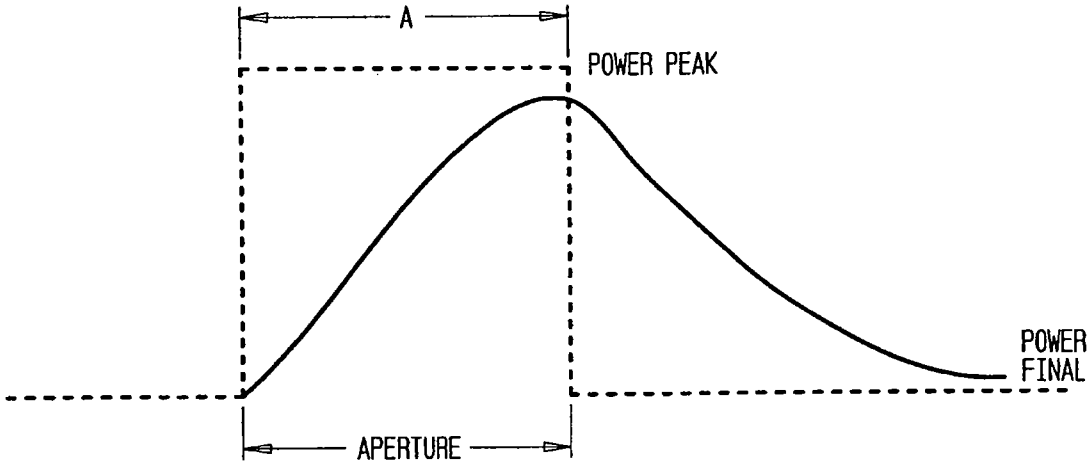


FIG. 175D

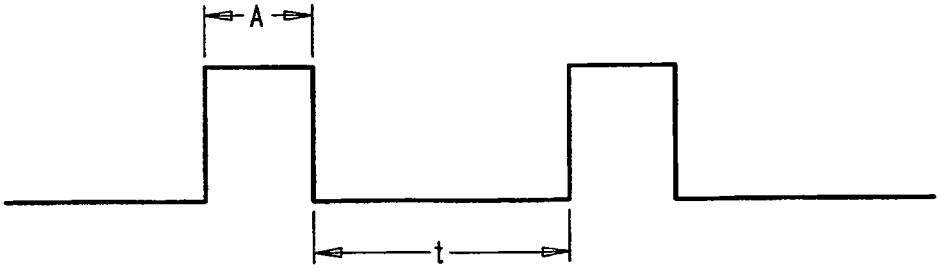


FIG. 176

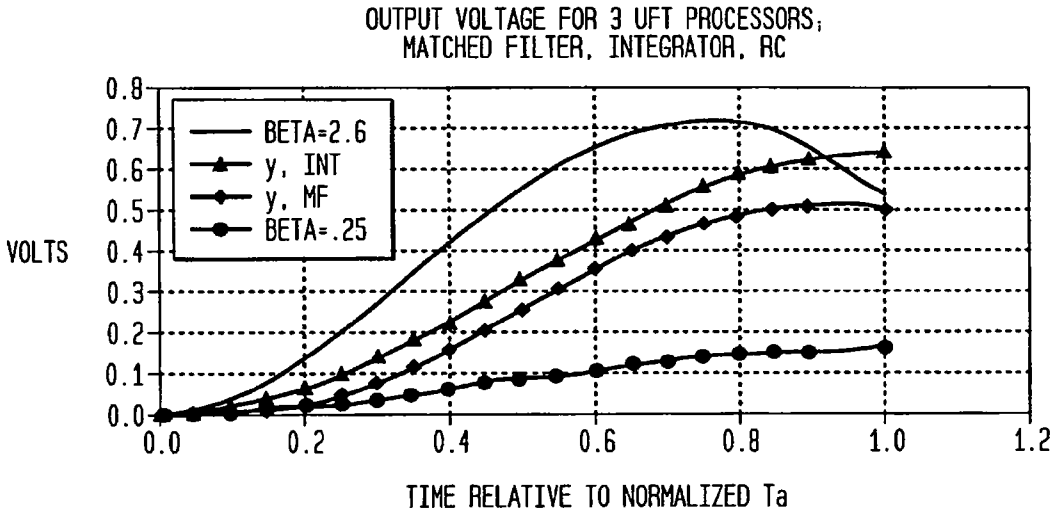
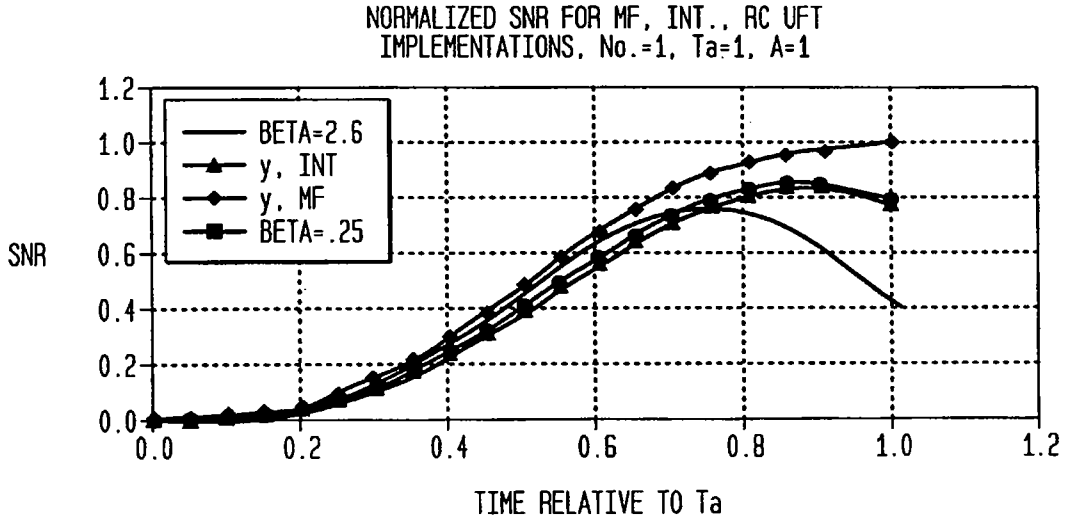

OUTPUT VOLTAGE FOR 3 UFT PROCESSORS;
MATCHED FILTER, INTEGRATOR, RC
BETA=2.6
y, INT
y, MF
BETA=.25
VOLTS
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.0
0.2
0.4
0.6
0.8
1.0
1.2
TIME RELATIVE TO NORMALIZED Ta

FIG. 177A


NORMALIZED SNR FOR MF, INT., RC UFT
IMPLEMENTATIONS, No.=1, Ta=1, A=1
SNR
TIME RELATIVE TO Ta
BETA=2.6
y, INT
y, MF
BETA=.25
0.0
0.2
0.4
0.6
0.8
1.0
1.2

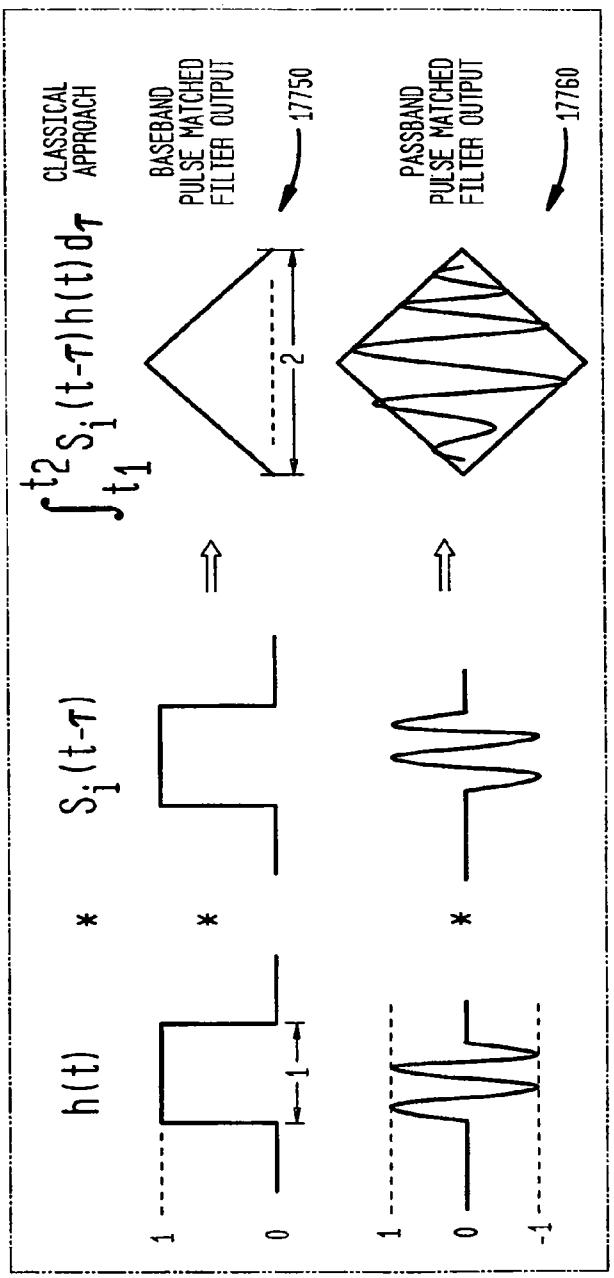


FIG. 177B

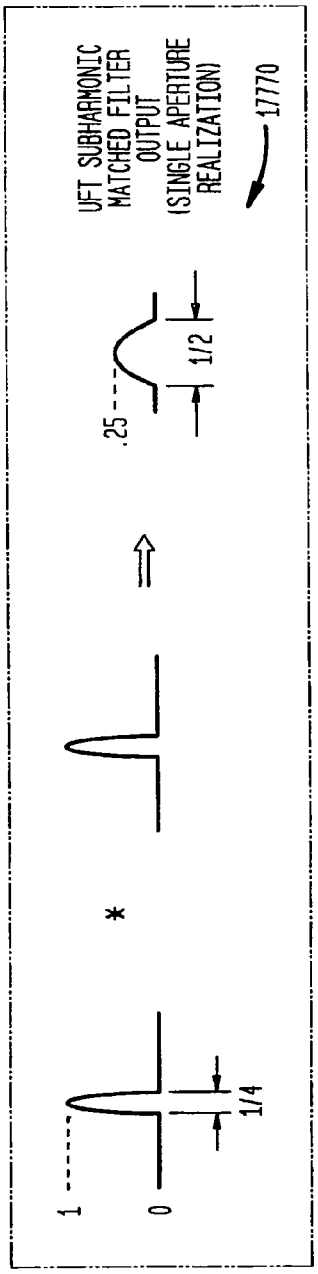


FIG. 177C

FIG. 177D

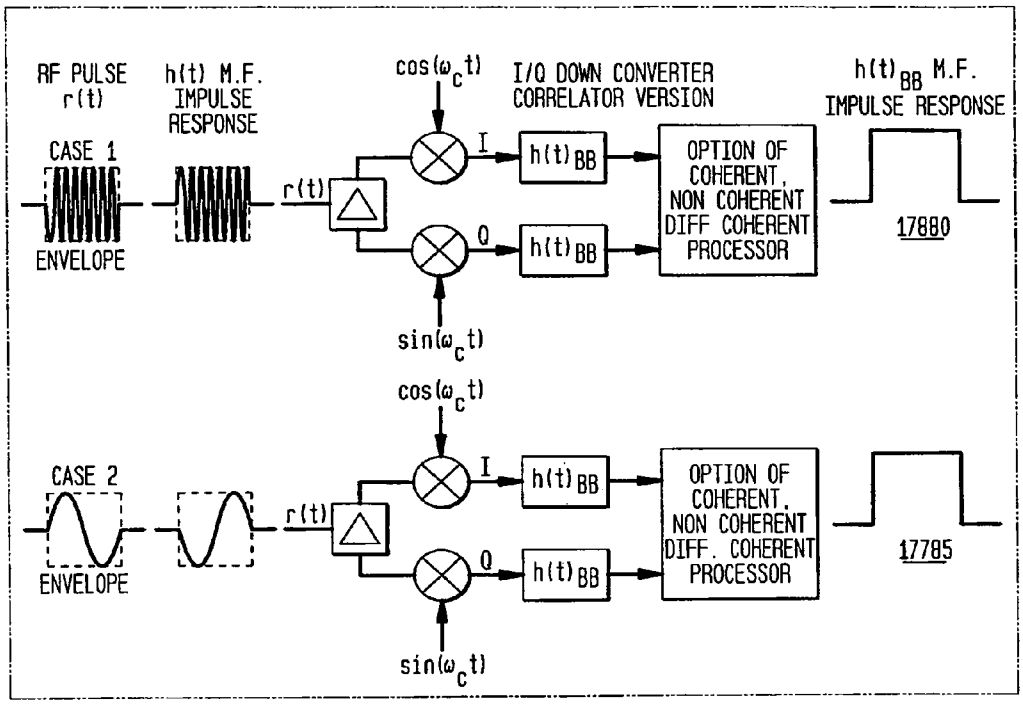


FIG. 177E

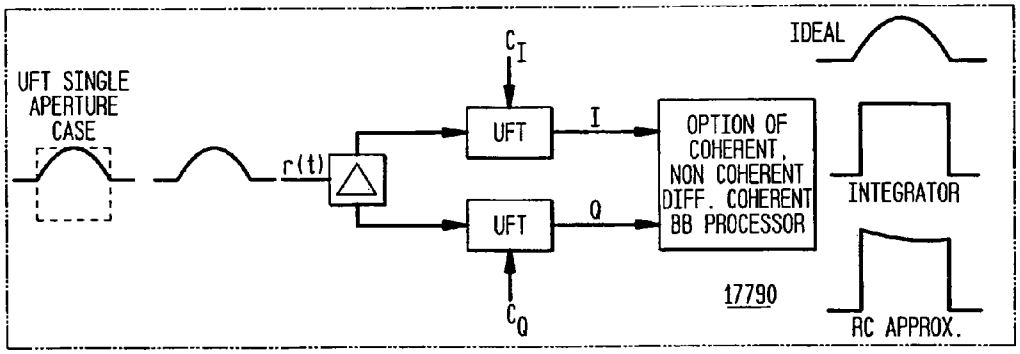


FIG. 177F

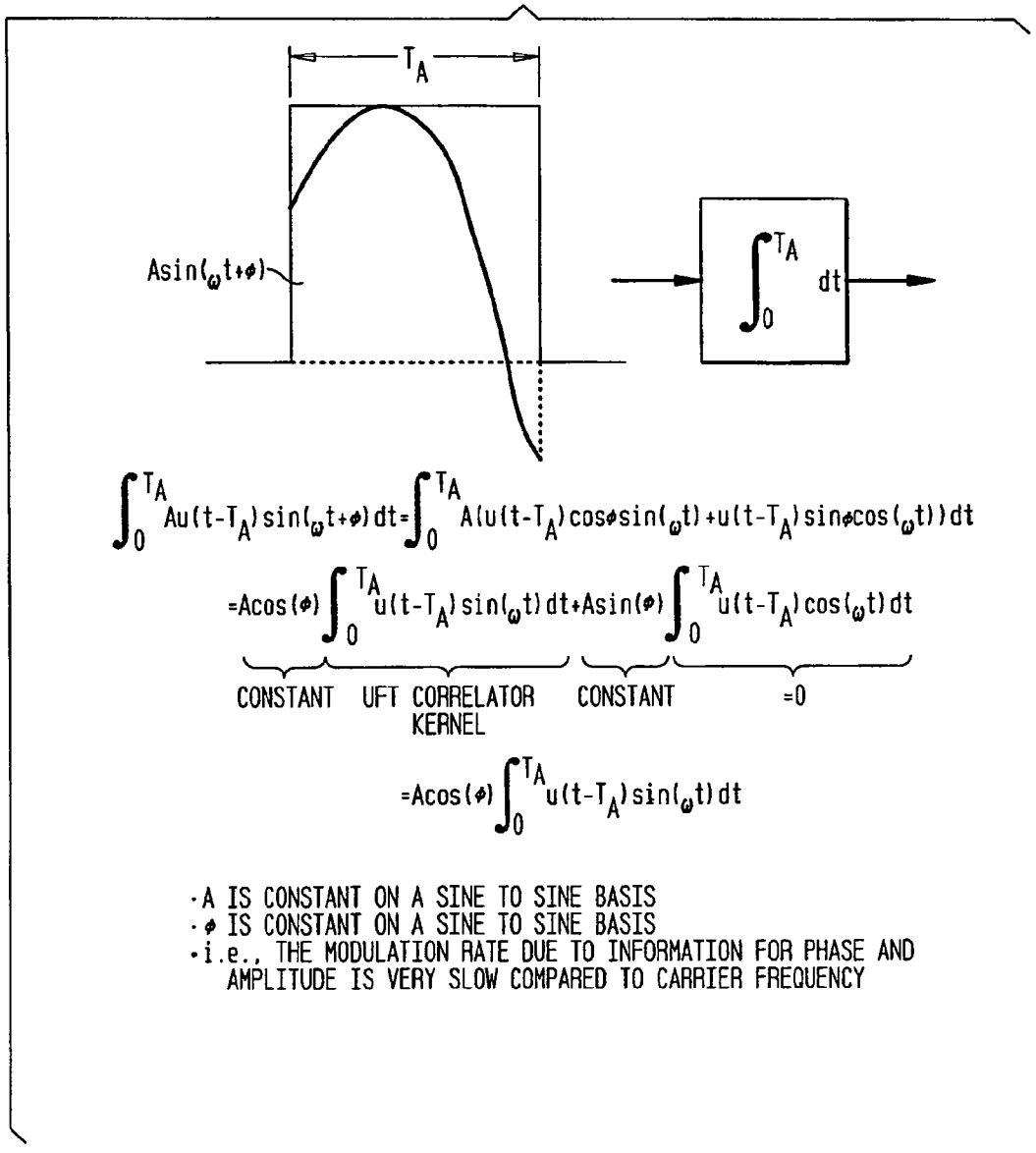

T_A
$A\sin(\omega t+\phi)$
$\int_0^{T_A} dt$
$\int_0^{T_A} Au(t-T_A)\sin(\omega t+\phi)\,dt = \int_0^{T_A} A(u(t-T_A)\cos\phi\sin(\omega t)+u(t-T_A)\sin\phi\cos(\omega t))\,dt$
$=A\cos(\phi)\int_0^{T_A} u(t-T_A)\sin(\omega t)\,dt + A\sin(\phi)\int_0^{T_A} u(t-T_A)\cos(\omega t)\,dt$
CONSTANT
UFT CORRELATOR KERNEL
CONSTANT
=0
$=A\cos(\phi)\int_0^{T_A} u(t-T_A)\sin(\omega t)\,dt$
·A IS CONSTANT ON A SINE TO SINE BASIS
·ϕ IS CONSTANT ON A SINE TO SINE BASIS
·i.e., THE MODULATION RATE DUE TO INFORMATION FOR PHASE AND AMPLITUDE IS VERY SLOW COMPARED TO CARRIER FREQUENCY

FIG. 178A

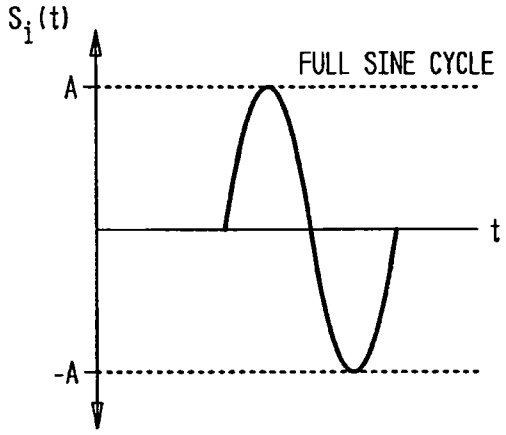


FIG. 178B

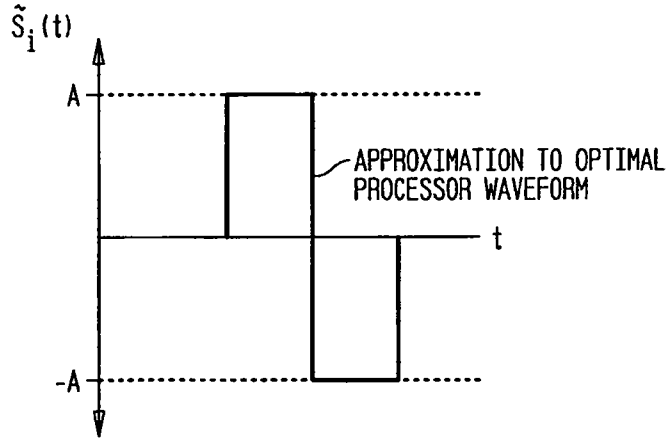


FIG. 179

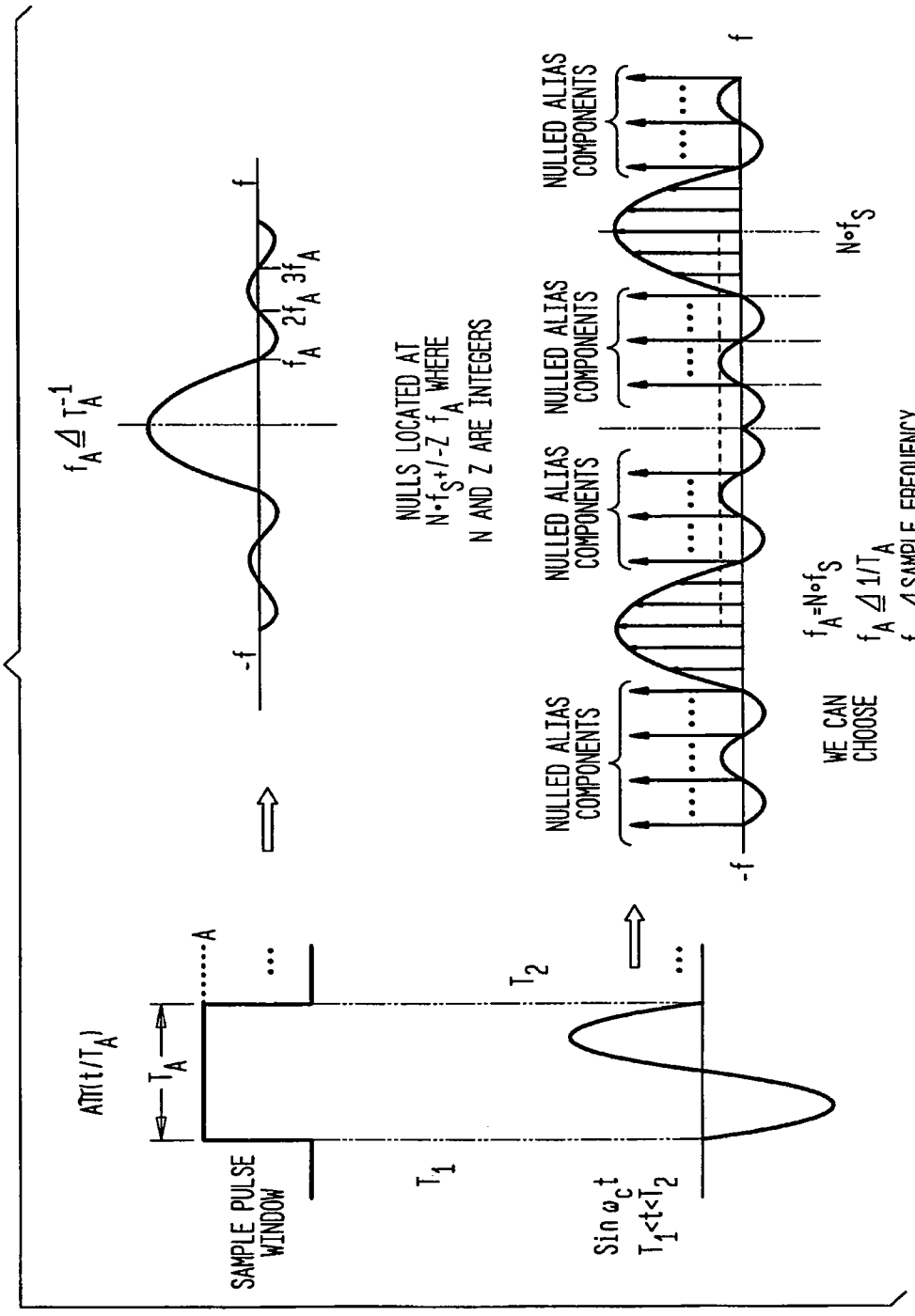

A Π(t/T_A)
T_A
A
SAMPLE PULSE WINDOW
T_1
T_2
Sin ω_c t
T_1<t<T_2
f_A ≜ T_A^-1
-f
f
f_A 2f_A 3f_A
NULLS LOCATED AT
N•f_S+/-Z f_A WHERE
N AND Z ARE INTEGERS
NULLED ALIAS COMPONENTS
NULLED ALIAS COMPONENTS
NULLED ALIAS COMPONENTS
NULLED ALIAS COMPONENTS
N•f_S
WE CAN CHOOSE
f_A=N•f_S
f_A ≜ 1/T_A
f_S ≜ SAMPLE FREQUENCY

FIG. 180

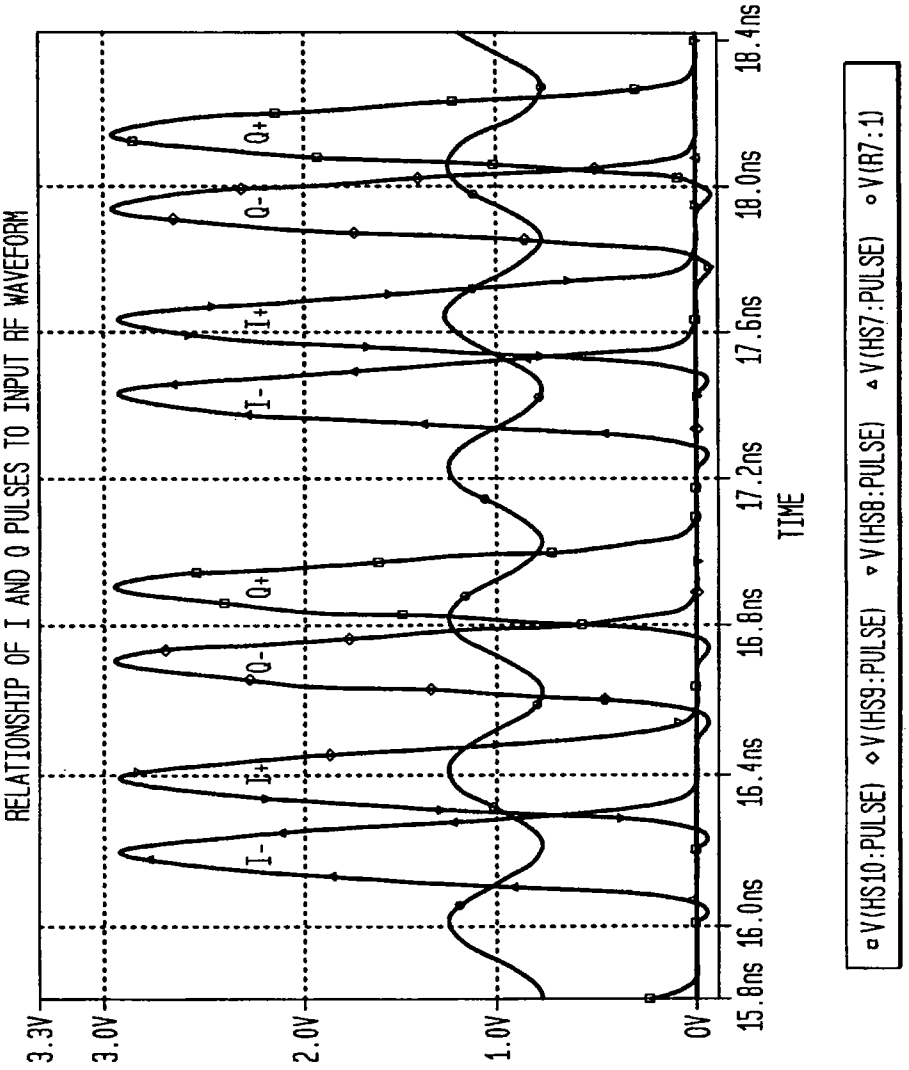

RELATIONSHIP OF I AND Q PULSES TO INPUT RF WAVEFORM
3.3V
3.0V
2.0V
1.0V
0V
15.8ns
16.0ns
16.4ns
16.8ns
17.2ns
17.6ns
18.0ns
18.4ns
TIME
I-
I+
Q-
Q+
V(HS10:PULSE)
V(HS9:PULSE)
V(HS8:PULSE)
V(HS7:PULSE)
V(R7:1)

FIG. 181

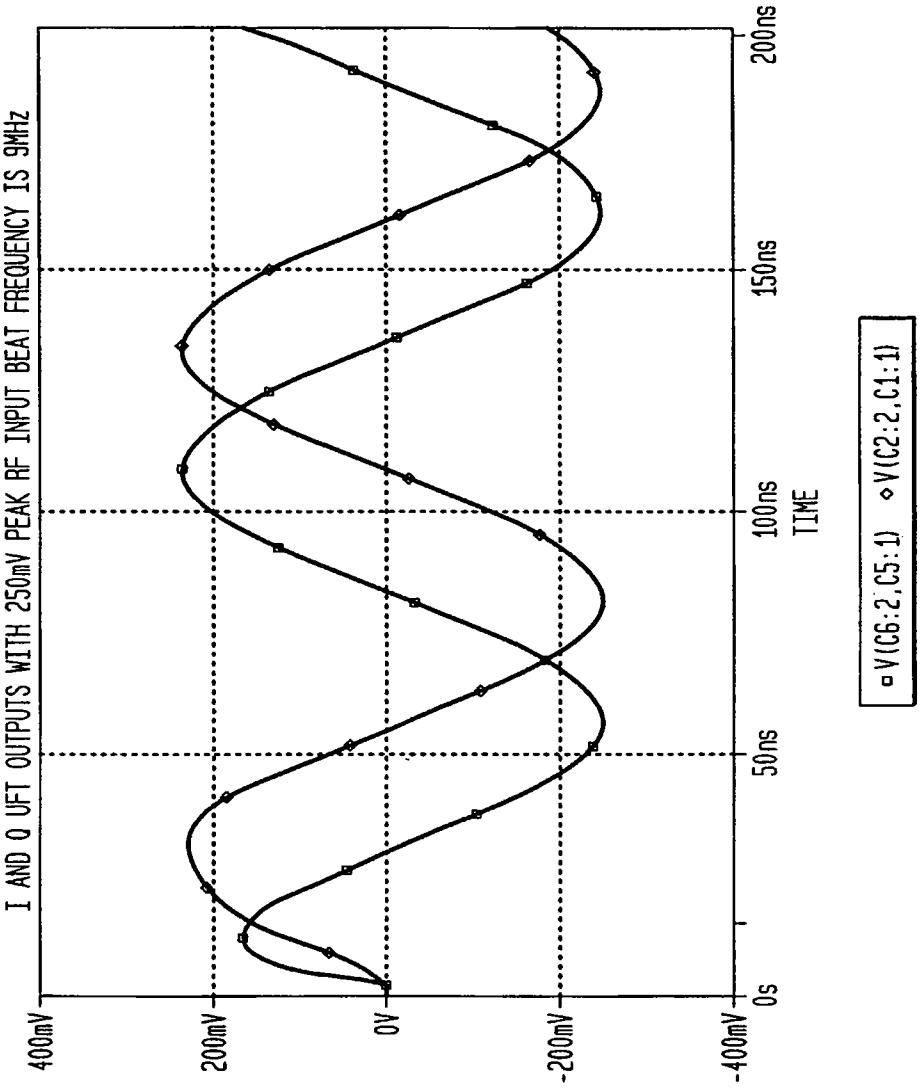

I AND Q UFT OUTPUTS WITH 250mV PEAK RF INPUT BEAT FREQUENCY IS 9MHz
400mV
200mV
0V
-200mV
-400mV
0s
50ns
100ns
150ns
200ns
TIME
V(C6:2,C5:1)
V(C2:2,C1:1)

FIG. 182

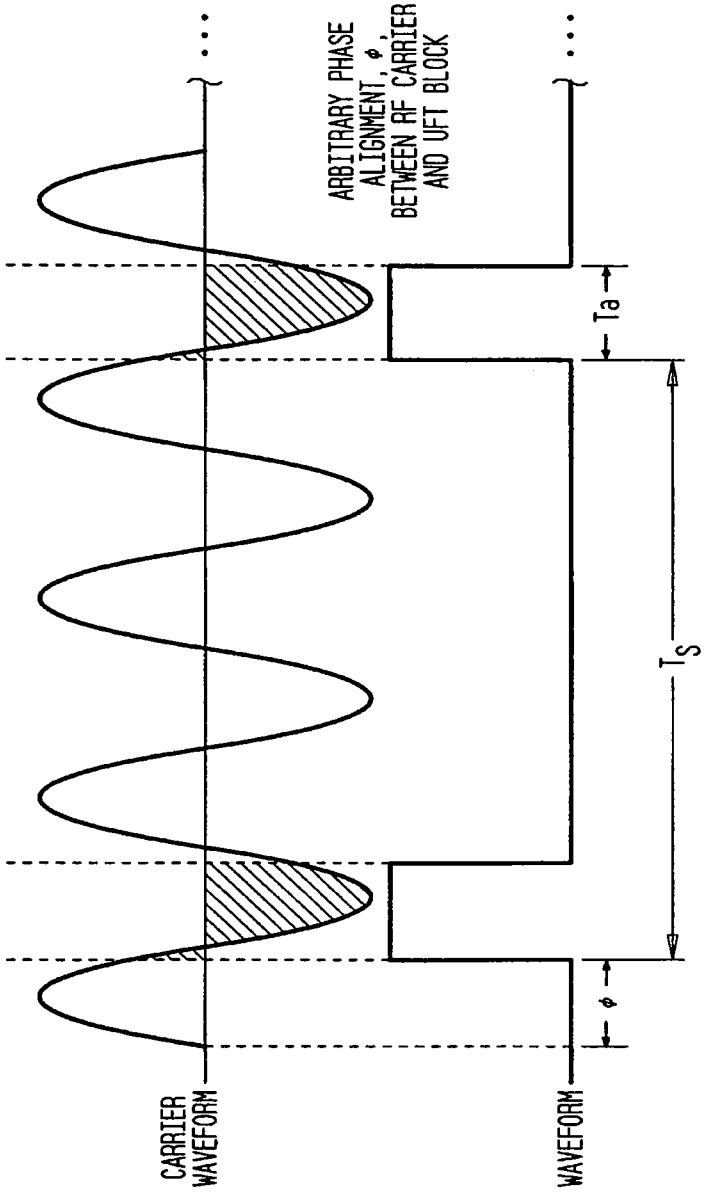

ARBITRARY PHASE ALIGNMENT, ϕ, BETWEEN RF CARRIER AND UFT BLOCK
Ta
Ts
ϕ
CARRIER WAVEFORM
WAVEFORM

FIG. 183

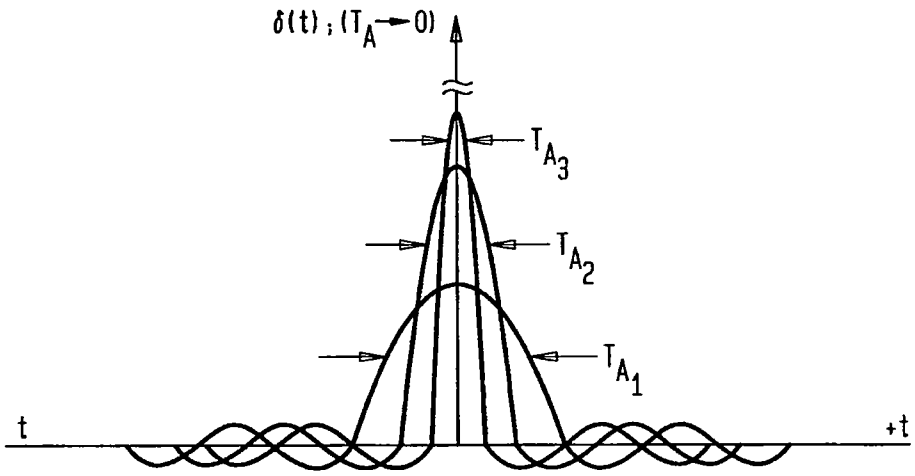


FIG. 184

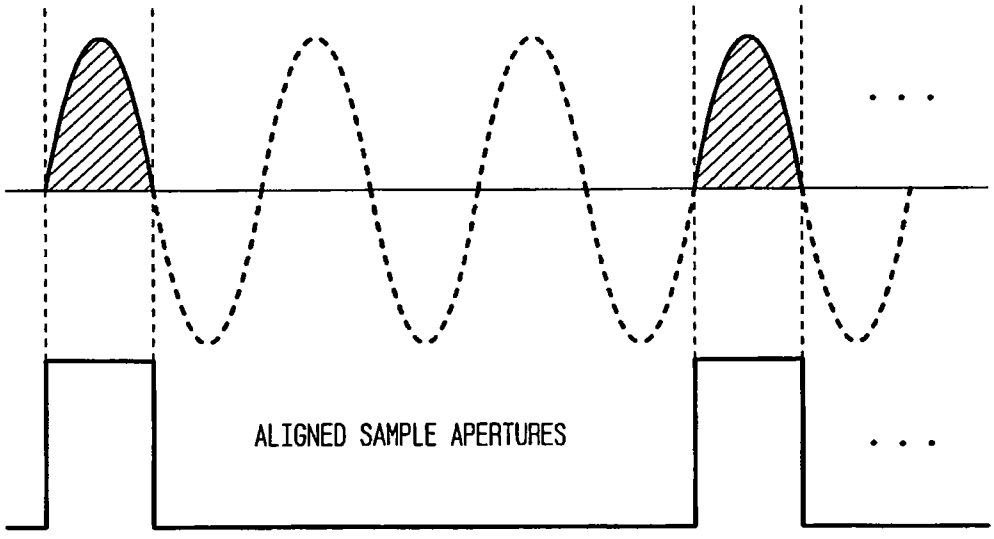


FIG. 185

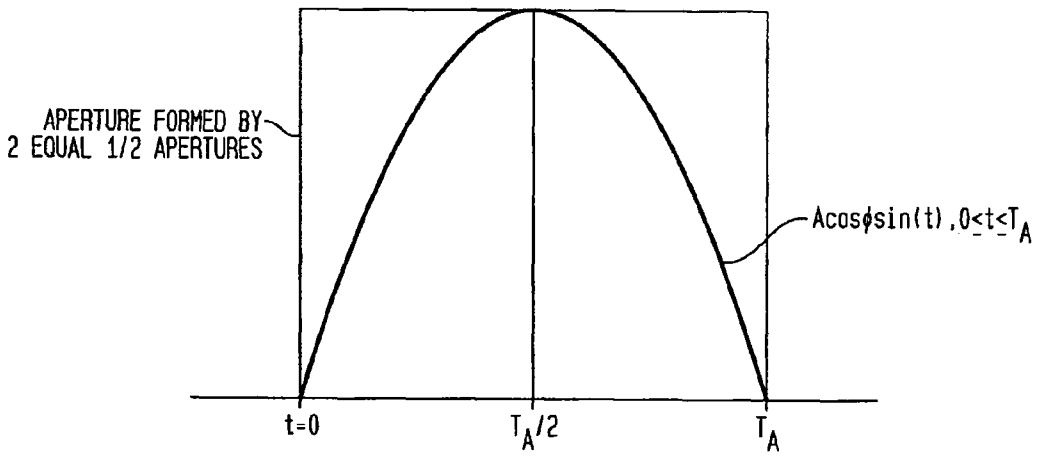


FIG. 186

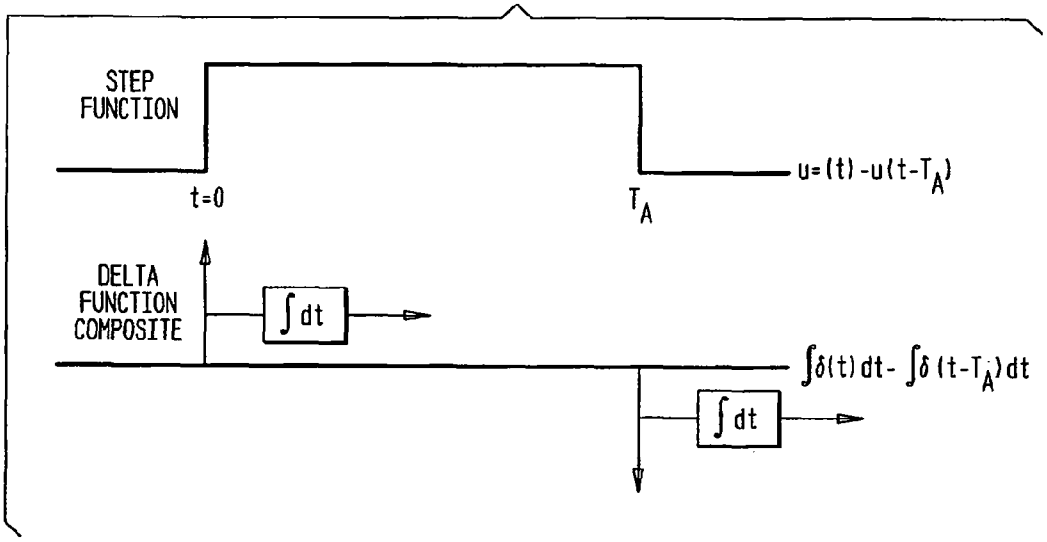


FIG. 187

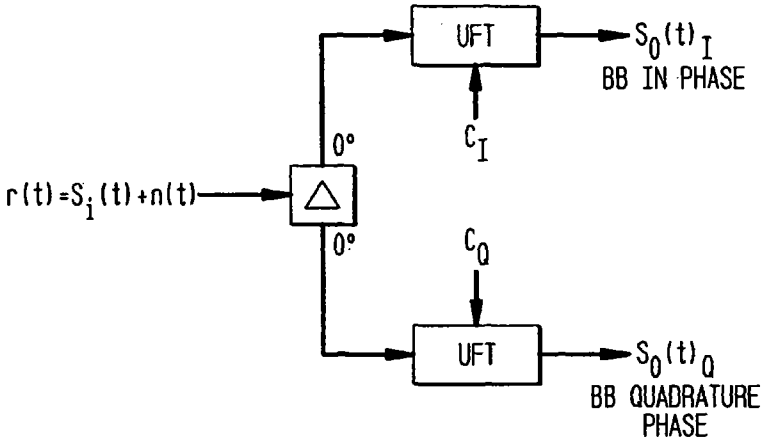


FIG. 188

$$C_I(t)=\sum_{m=-\infty}^{\infty}\delta(t-mT_S)*p_c(t)=\sum_{m=-\infty}^{\infty}p(t-mT_S) \quad 18802$$

$$C_I(t)=\sum_{m=-\infty}^{\infty}(u(t)-u(t-T_A))*\delta(t-mT_S) \quad 18804$$

$$C_Q(t)=\sum_{m=-\infty}^{\infty}(u[t-T_A/2]-u[t-3T_A/2])*\delta(t-(mT_S+T_A/2)) \quad 18806$$

FIG. 189

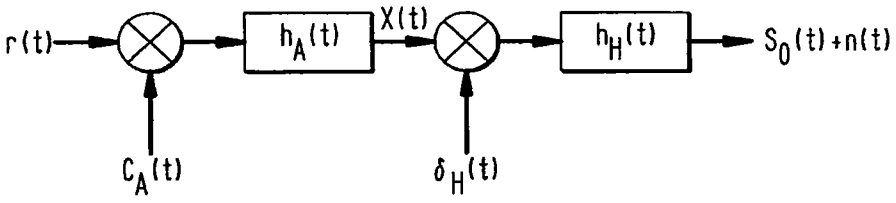


FIG. 190

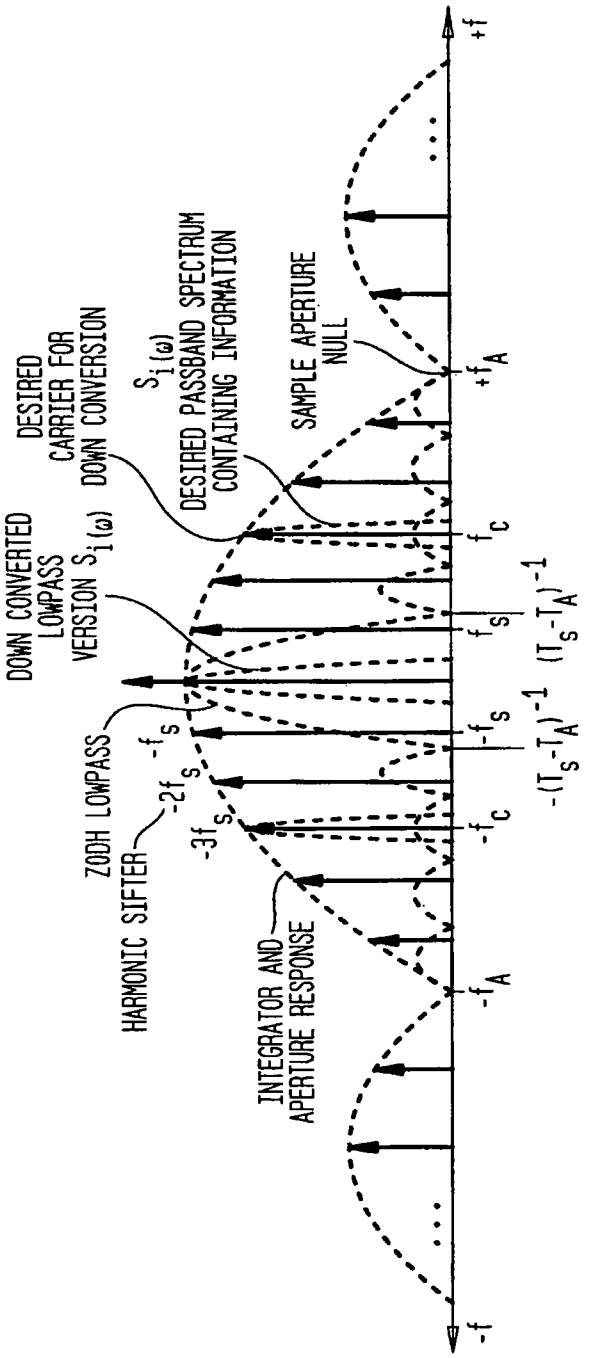

DESIRED CARRIER FOR DOWN CONVERSION
$S_{i(\omega)}$ DESIRED PASSBAND SPECTRUM CONTAINING INFORMATION
SAMPLE APERTURE NULL
DOWN CONVERTED LOWPASS VERSION $S_{i(\omega)}$
ZOOH LOWPASS HARMONIC SIFTER
INTEGRATOR AND APERTURE RESPONSE
$-f_s$
$-2f_s$
$-3f_s$
$-f_c$
$-f_A$
f_c
f_s
$+f_A$
$-(T_s-T_A)^{-1}$
$(T_s-T_A)^{-1}$
$-f$
$+f$

FIG. 191

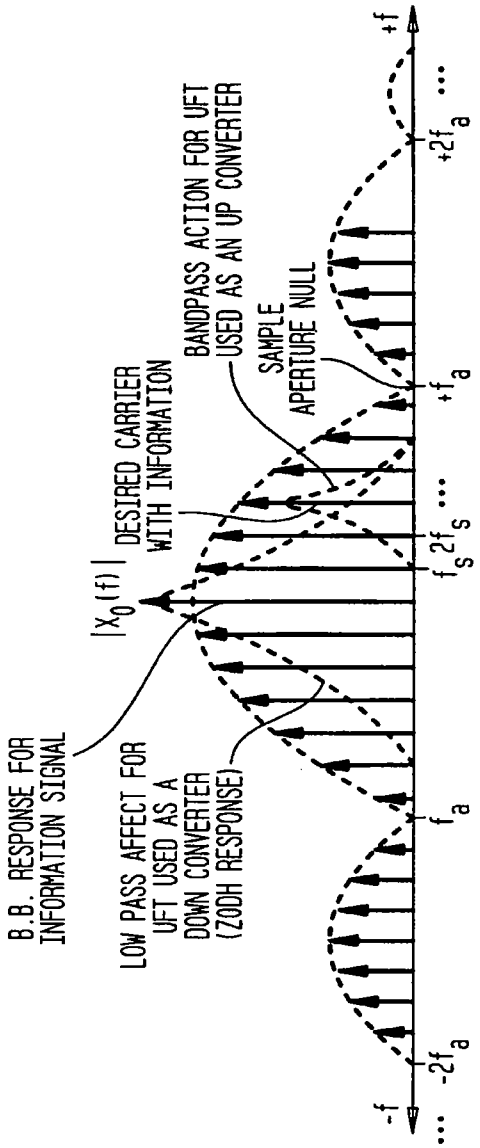


FIG. 192

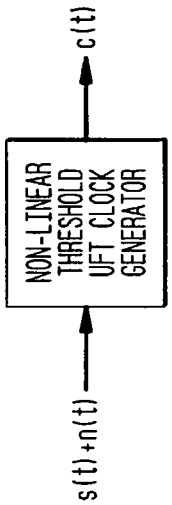


FIG. 193

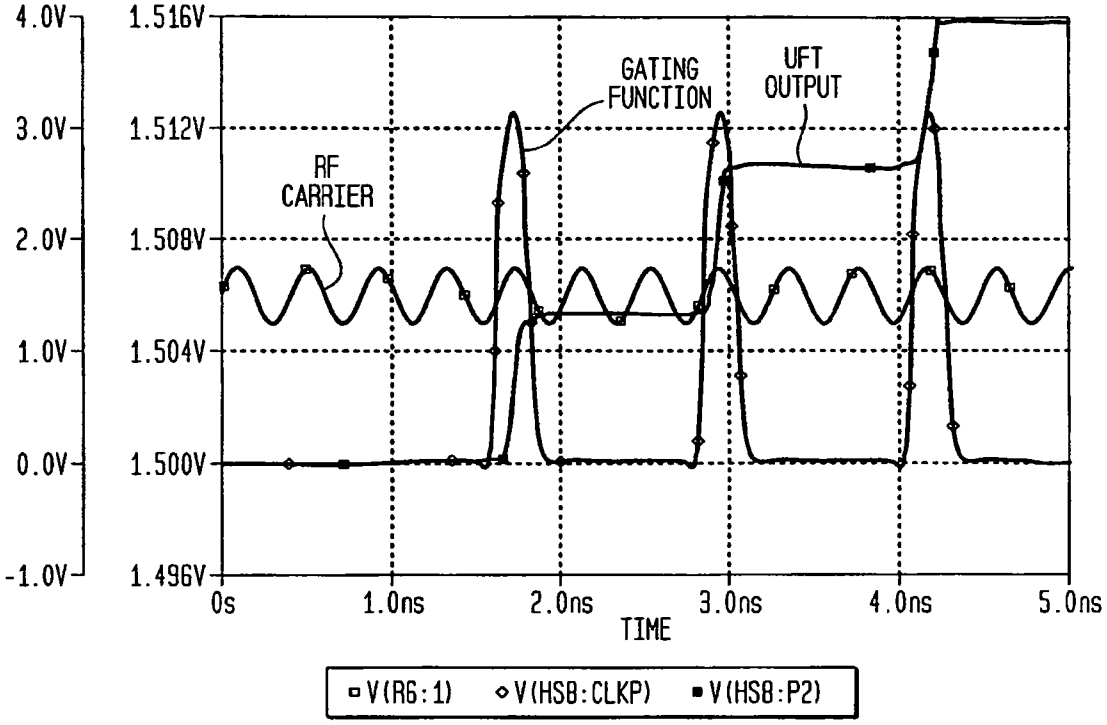

4.0V
3.0V
2.0V
1.0V
0.0V
-1.0V
1.516V
1.512V
1.508V
1.504V
1.500V
1.496V
GATING FUNCTION
UFT OUTPUT
RF CARRIER
0s
1.0ns
2.0ns
3.0ns
4.0ns
5.0ns
TIME
V(R6:1)
V(HSB:CLKP)
V(HSB:P2)

FIG. 194

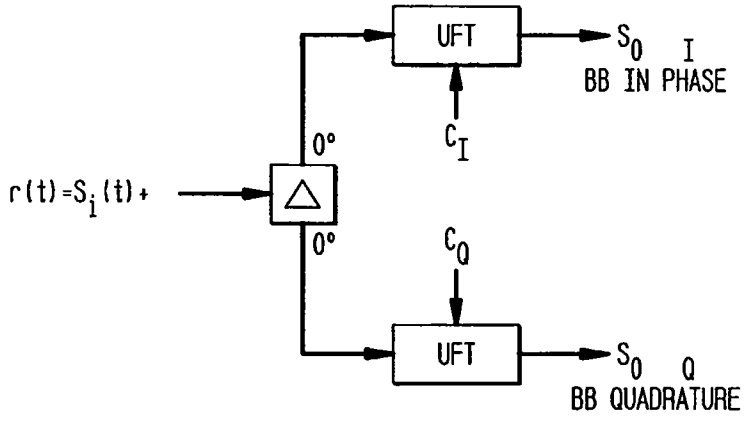


FIG. 195

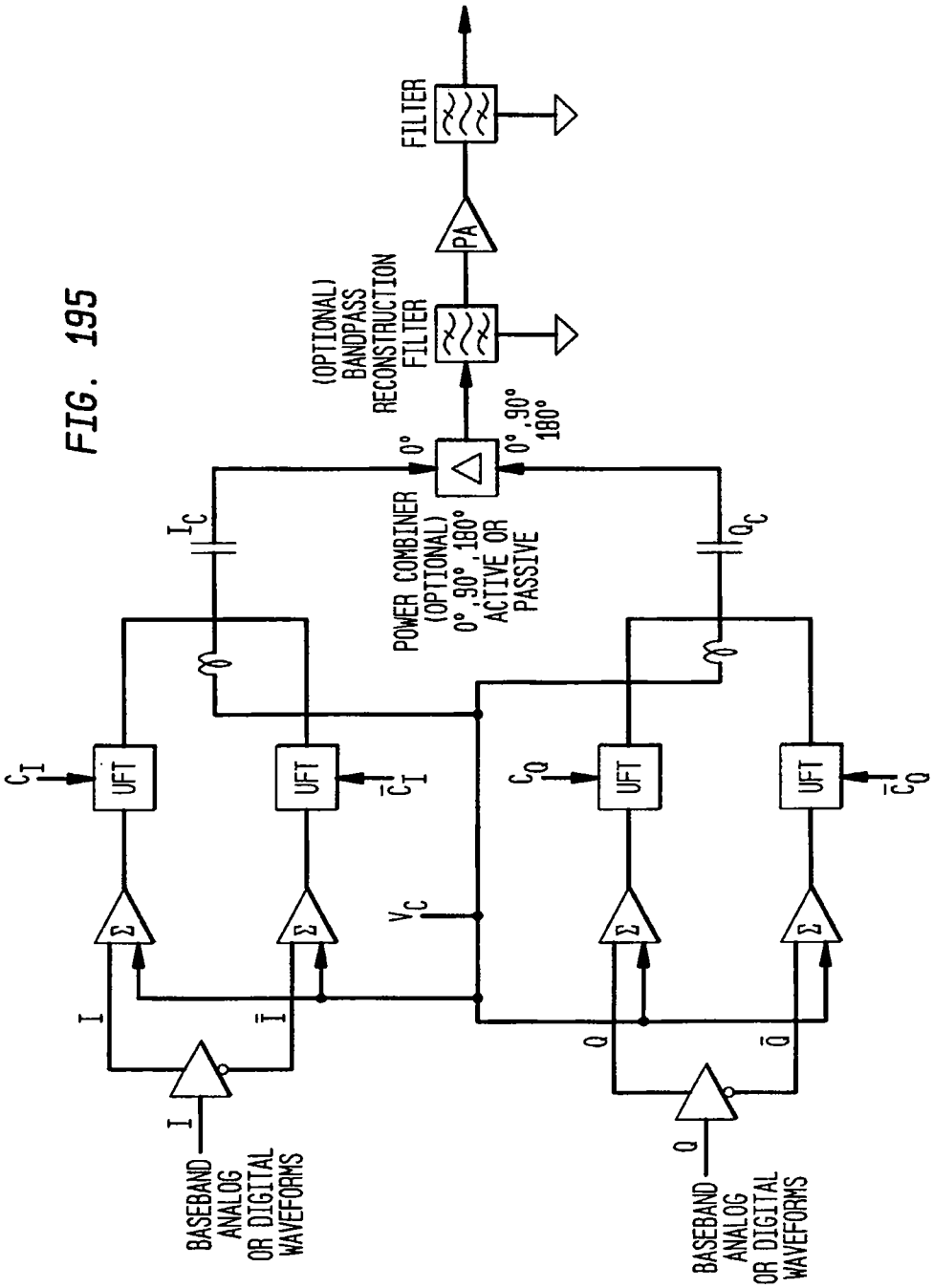

FILTER
PA
(OPTIONAL) BANDPASS RECONSTRUCTION FILTER
0°
0°,90°,180°
POWER COMBINER (OPTIONAL) 0°,90°,180° ACTIVE OR PASSIVE
I_C
Q_C
C_I
$\bar{C}_I$
C_Q
$\bar{C}_Q$
UFT
V_C
I
$\bar{I}$
Q
$\bar{Q}$
BASEBAND ANALOG OR DIGITAL WAVEFORMS
BASEBAND ANALOG OR DIGITAL WAVEFORMS

FIG. 196

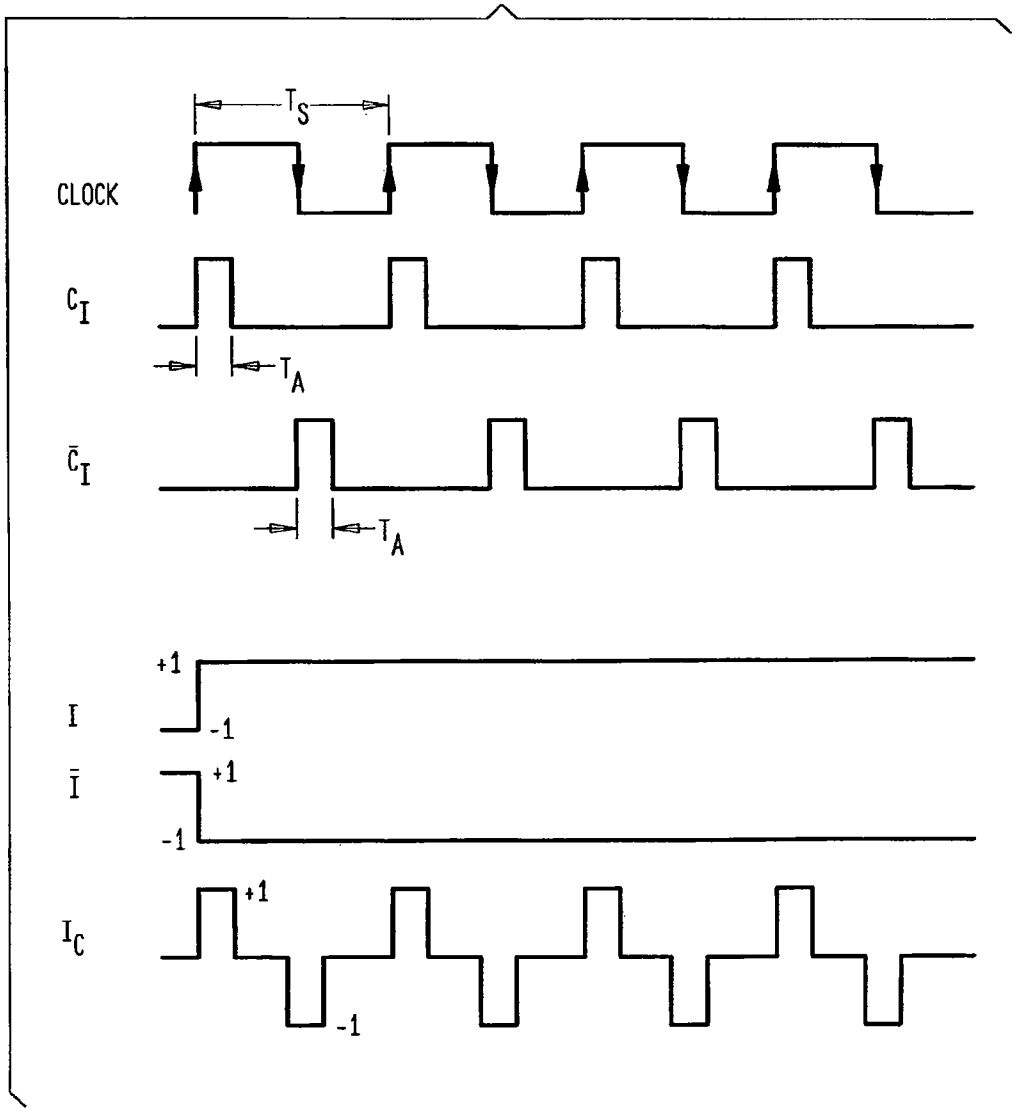


FIG. 197

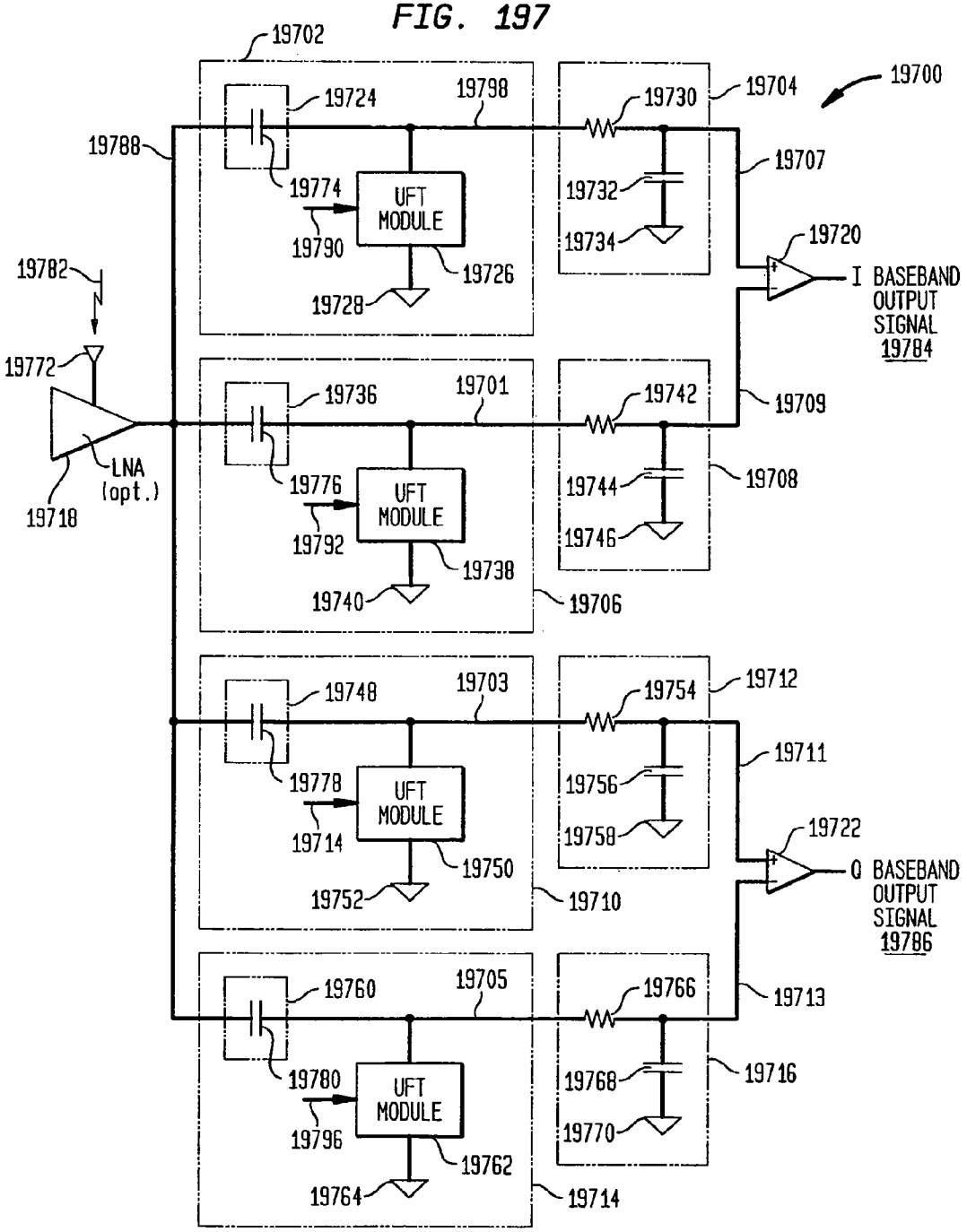

19702
19724
19798
19730
19704
19700
19788
19707
19774
UFT MODULE
19732
19790
19734
19720
19726
I BASEBAND OUTPUT SIGNAL 19784
19728
19782
19772
19736
19701
19742
19709
19776
UFT MODULE
19744
19708
LNA (opt.)
19718
19792
19746
19738
19740
19706
19748
19703
19754
19712
19778
UFT MODULE
19756
19711
19714
19758
19722
19750
Q BASEBAND OUTPUT SIGNAL 19786
19752
19710
19760
19705
19766
19713
19780
UFT MODULE
19768
19716
19796
19770
19762
19764
19714

FIG. 198

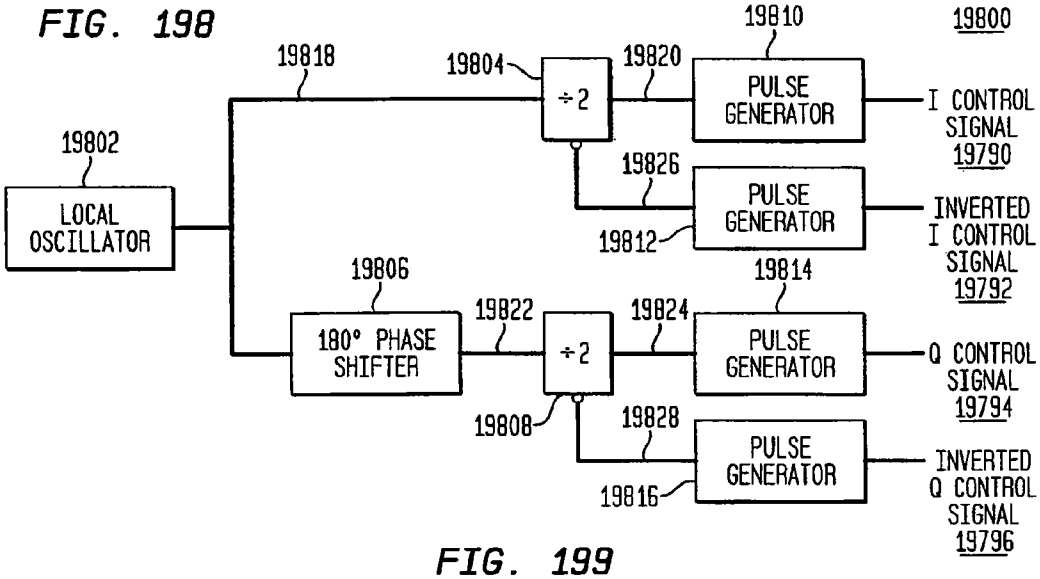


FIG. 199

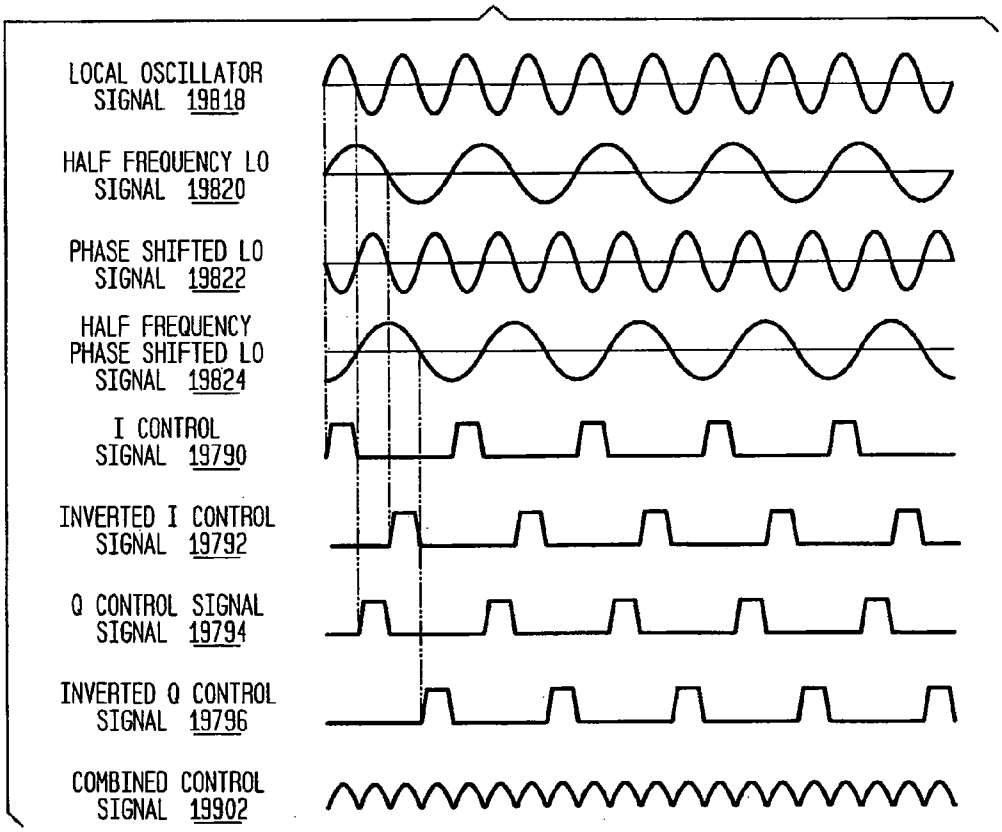


FIG. 200

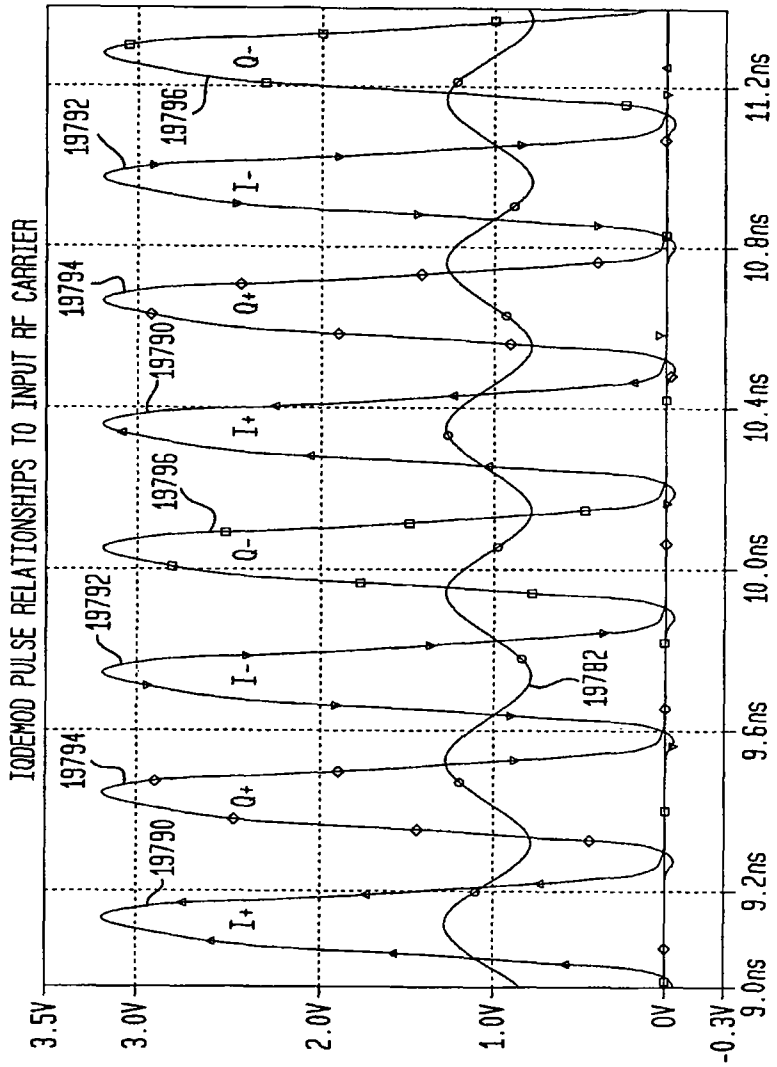
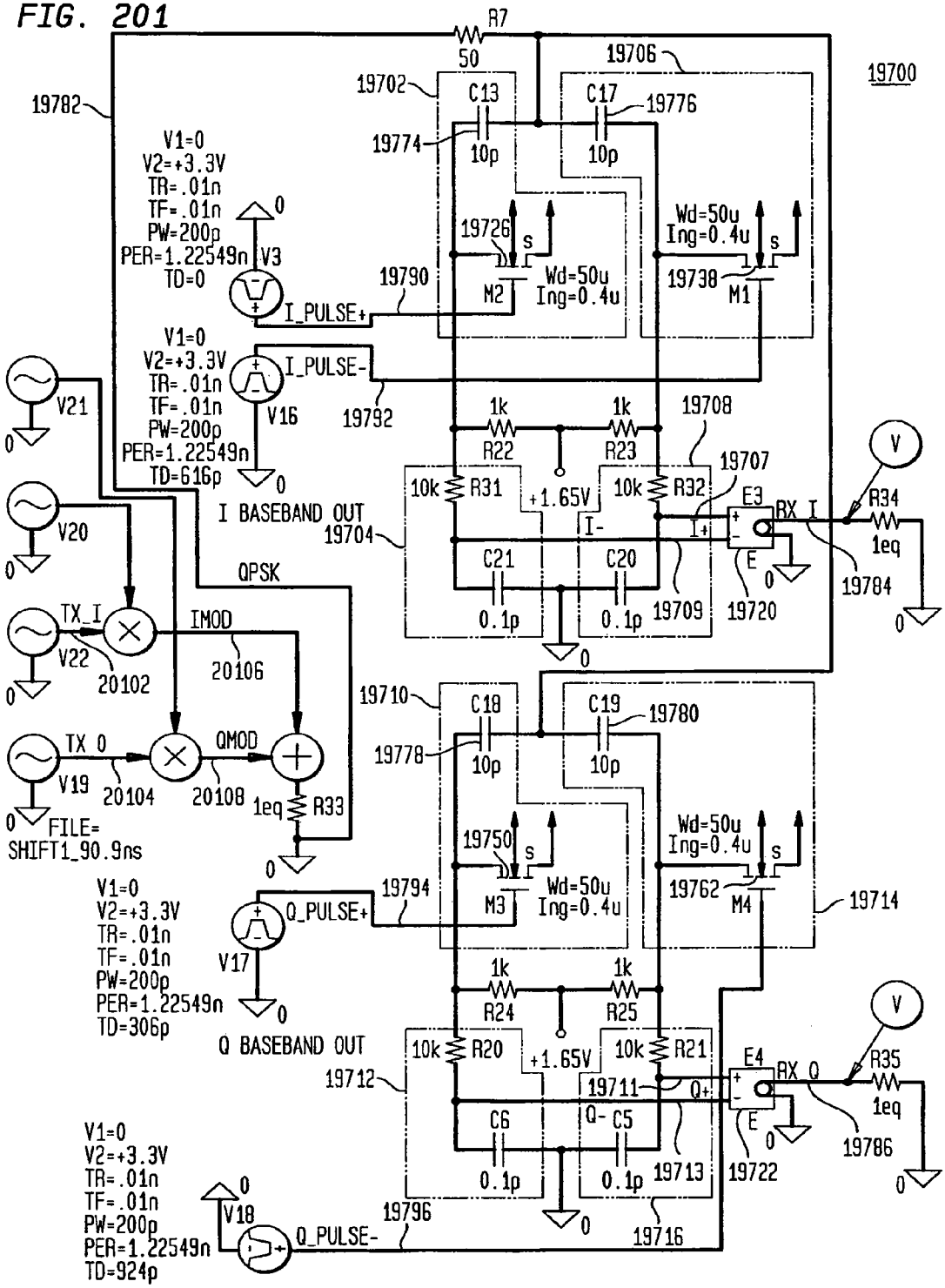

IQDEMOD PULSE RELATIONSHIPS TO INPUT RF CARRIER
3.5V
3.0V
2.0V
1.0V
0V
-0.3V
9.0ns
9.2ns
9.6ns
10.0ns
10.4ns
10.8ns
11.2ns
19790
19794
19792
19796
19782
I+
Q+
I-
Q-

FIG. 201


R7
50
19706
19700
19702
C13
C17
19776
19782
19774
10p
10p
V1=0
V2=+3.3V
TR=.01n
TF=.01n
PW=200p
PER=1.22549n
TD=0
V3
0
19726
s
Wd=50u
Lng=0.4u
s
19790
M2
Wd=50u
Lng=0.4u
19738
M1
I_PULSE+
V1=0
V2=+3.3V
TR=.01n
TF=.01n
PW=200p
PER=1.22549n
TD=616p
V16
I_PULSE-
19792
V21
1k
1k
19708
R22
R23
10k
R31
+1.65V
10k
R32
19707
V
I BASEBAND OUT
19704
I-
I+
E3
RX_I
R34
1eq
V20
C21
C20
E
0
19720
19784
0.1p
0.1p
19709
QPSK
TX_I
IMOD
V22
20102
20106
19710
C18
C19
19780
19778
10p
10p
TX_Q
QMOD
V19
20104
20108
1eq
R33
FILE=
SHIFT1_90.9ns
19750
s
Wd=50u
Lng=0.4u
s
V1=0
V2=+3.3V
TR=.01n
TF=.01n
PW=200p
PER=1.22549n
TD=306p
19794
Q_PULSE+
V17
M3
Wd=50u
Lng=0.4u
19762
M4
19714
1k
1k
R24
R25
Q BASEBAND OUT
10k
R20
+1.65V
10k
R21
E4
RX_Q
R35
19712
19711
Q+
Q-
C5
C6
E
0
19722
19786
1eq
0.1p
0.1p
19713
V1=0
V2=+3.3V
TR=.01n
TF=.01n
PW=200p
PER=1.22549n
TD=924p
V18
Q_PULSE-
19796
19716

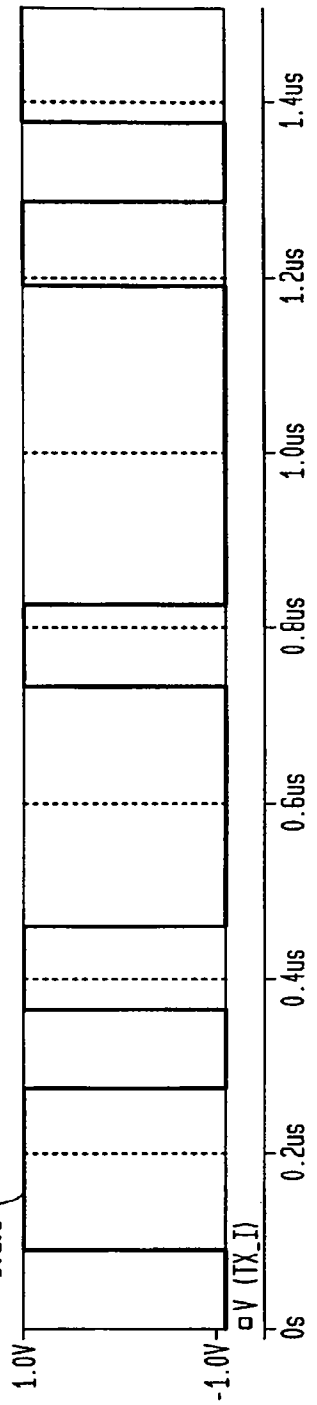


FIG. 202
IQDEMOD SHOWING TIME RELATIONSHIP OF TX_I DATA

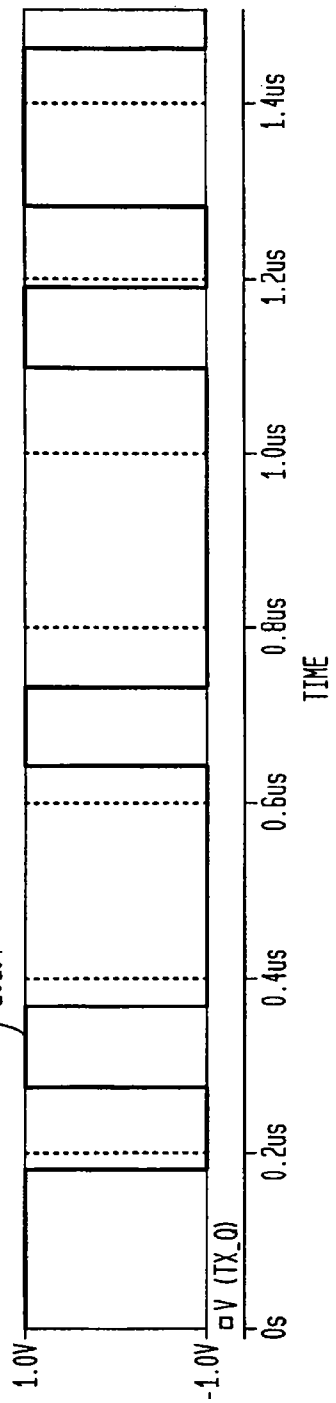


FIG. 203
IQDEMOD SHOWING TIME RELATIONSHIP OF TX_Q DATA

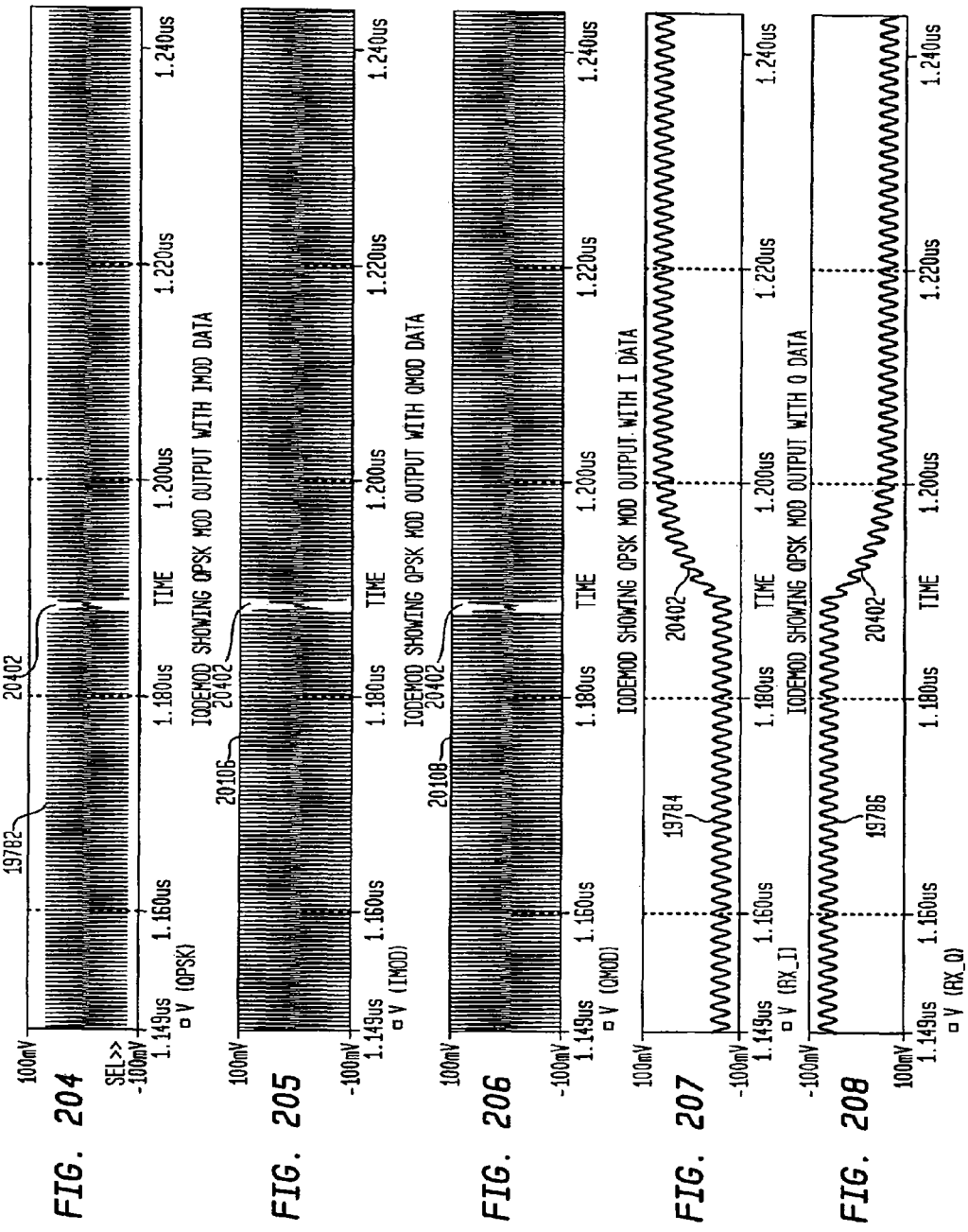


FIG. 204

FIG. 205

FIG. 206

FIG. 207

FIG. 208

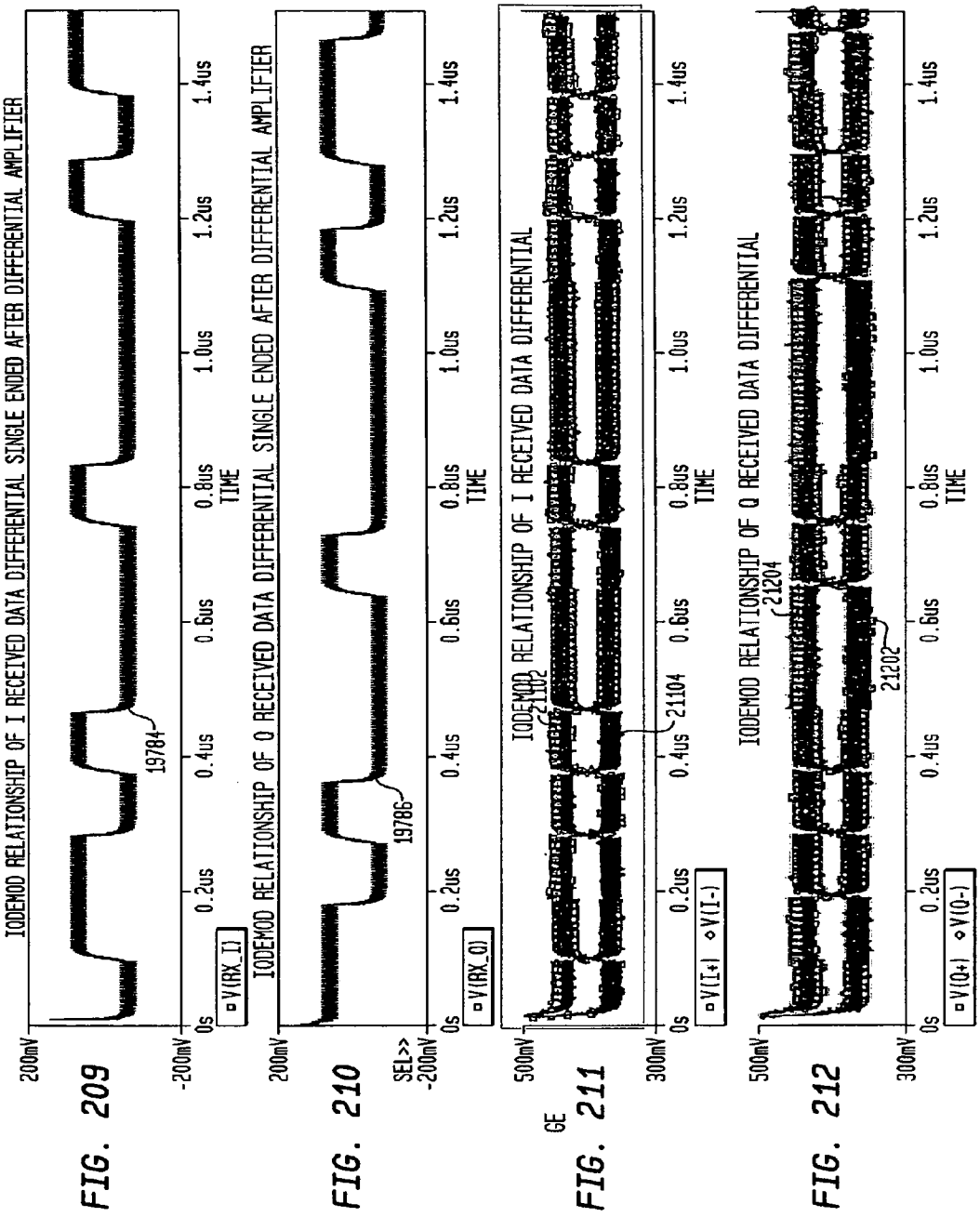


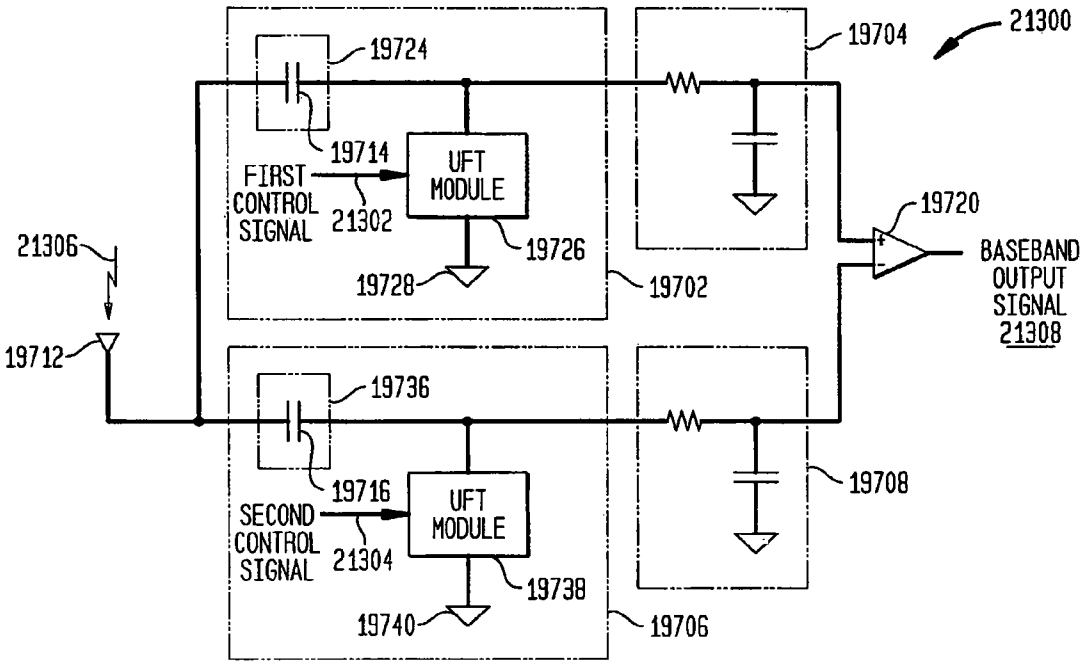
FIG. 209

FIG. 210

FIG. 211

FIG. 212

FIG. 213


21300
19704
19724
19714
FIRST CONTROL SIGNAL
21302
UFT MODULE
19726
19728
19702
19720
BASEBAND OUTPUT SIGNAL 21308
21306
19712
19736
19716
SECOND CONTROL SIGNAL
21304
UFT MODULE
19738
19740
19706
19708

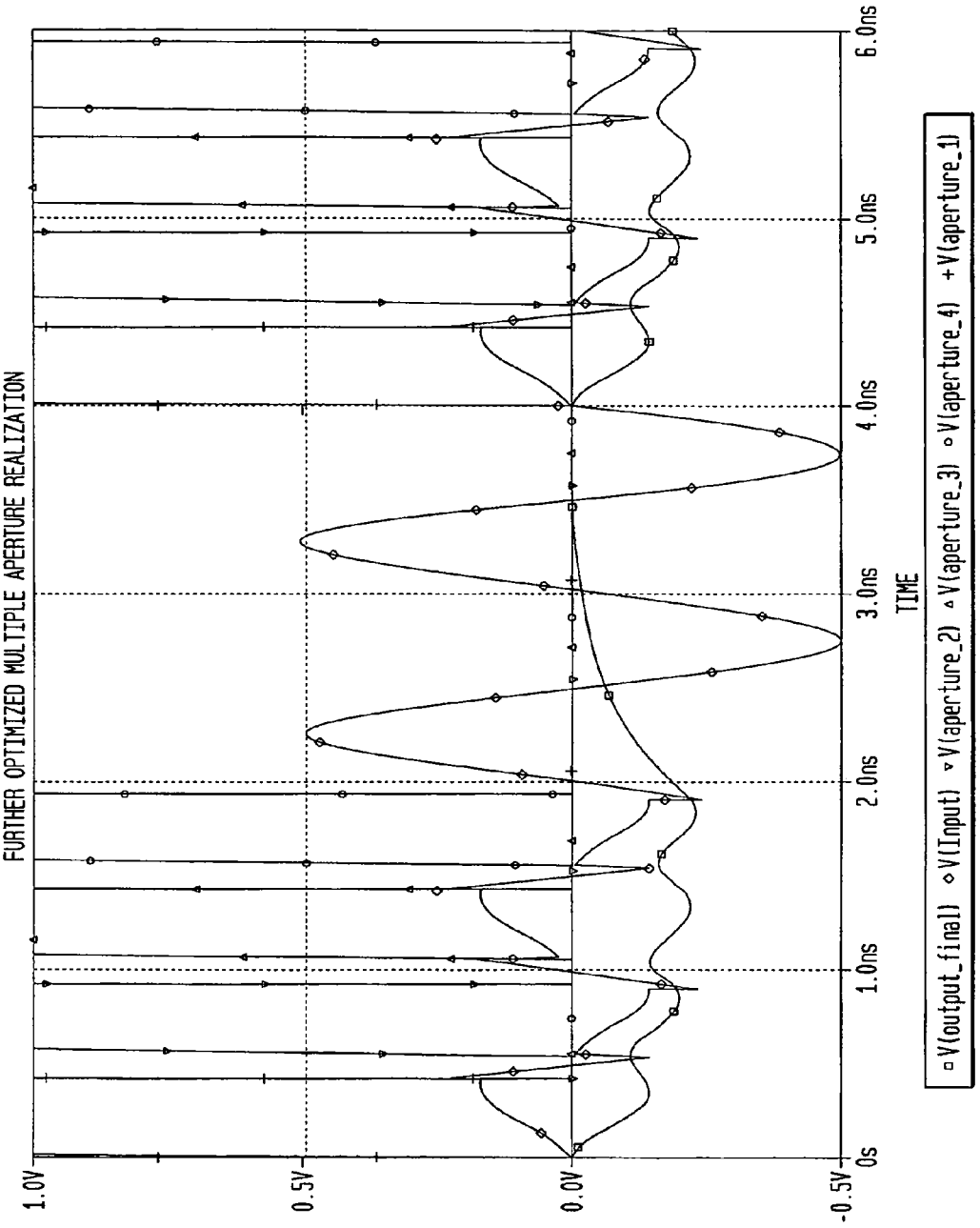

FURTHER OPTIMIZED MULTIPLE APERTURE REALIZATION
1.0V
0.5V
0.0V
-0.5V
0s
1.0ns
2.0ns
3.0ns
4.0ns
5.0ns
6.0ns
TIME
V(output_final) V(Input) V(aperture_2) V(aperture_3) V(aperture_4) +V(aperture_1)

FIG. 214

FIG. 215

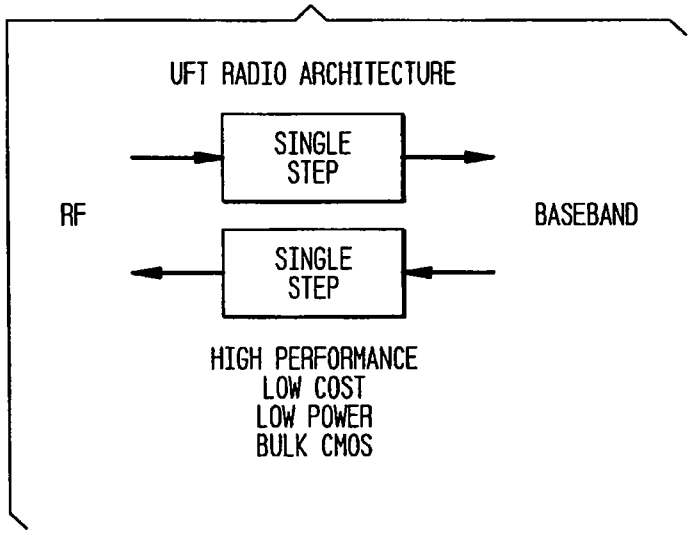


FIG. 216

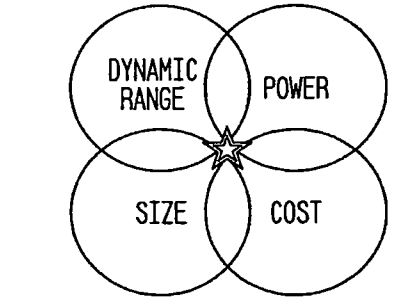


FIG. 217

NOISE FIGURE CALCULATIONS BASED ON RMS
VOLTAGE AND CURRENT NOISE SPECIFICATIONS

ENTER, THE VOLTAGE NOISE DENSITY, e_n, AND THE
CURRENT NOISE DENSITY, i_n, FOR THE AMPLIFIER CHOSEN:

$e_n := 6 \cdot 10^{-9}$ V/sqrt(Hz)
$i_n := 1 \cdot 10^{-12}$ A/sqrt(Hz)

ENTER THE SOURCE RESISTANCE DRIVING THE AMPLIFIER:

$K := 1.38 \cdot 10^{-23}$ J/K $T := 290K$

$PARALELL(x,y) := \frac{x \cdot y}{x+y}$ $NF(R_S) := 20 \cdot \log\left(\sqrt{\frac{e_n^2 + 4 \cdot K \cdot T \cdot R_S + i_n^2 \cdot R_S^2}{4 \cdot K \cdot T \cdot R_S}}\right)$

IF WE PLOT NOISE FIGURE VERSUS SOURCE RESISTANCE WE CAN GET
AN IDEA OF WHAT IS THE OPTIMUM SOURCE RESISTANCE.
IT IS NOT NECESSARILY THE LOWEST RESISTANCE!

$R_S := 100, 200 \ldots 100 \cdot 10^3$

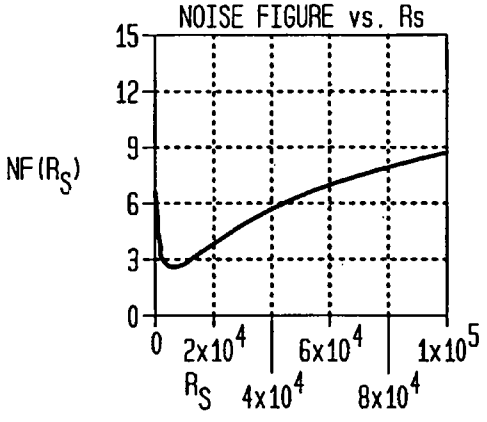


FIG. 218A

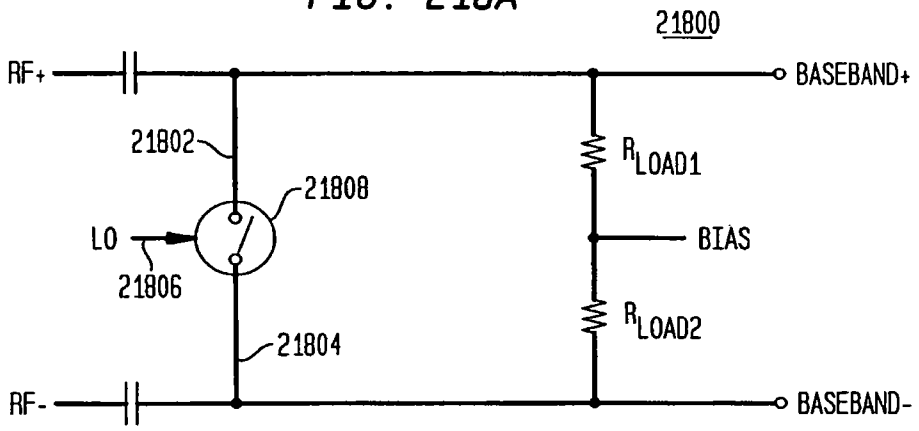


FIG. 218B

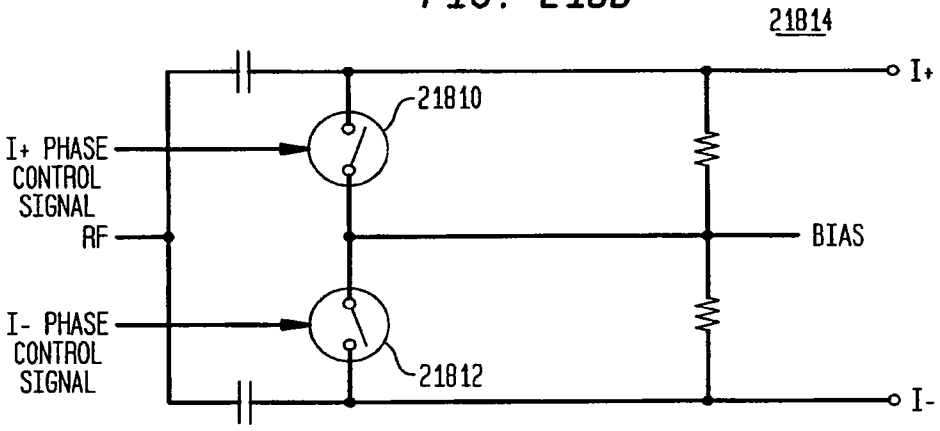


FIG. 218C

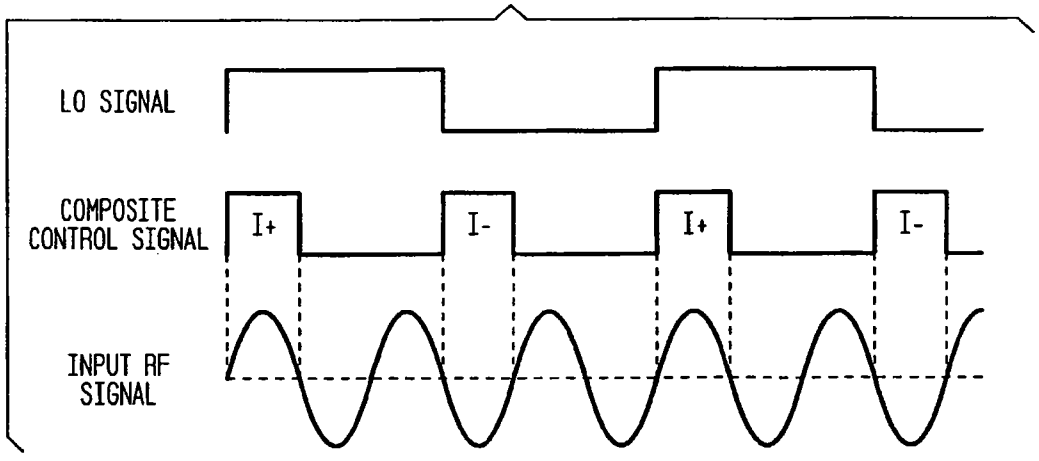
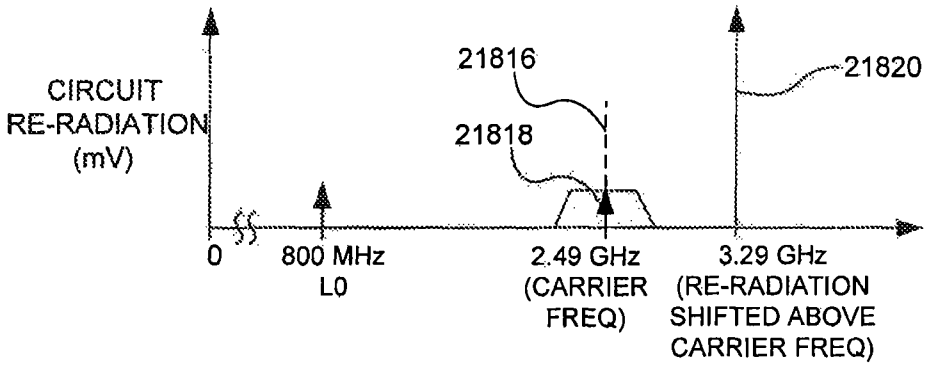


FIG. 218D



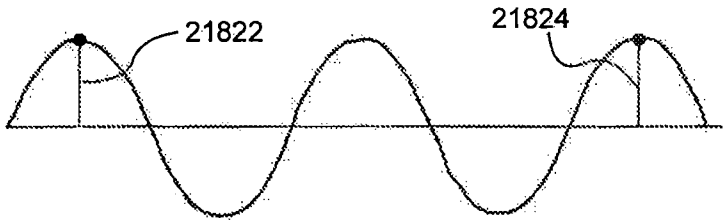


FIG. 218F

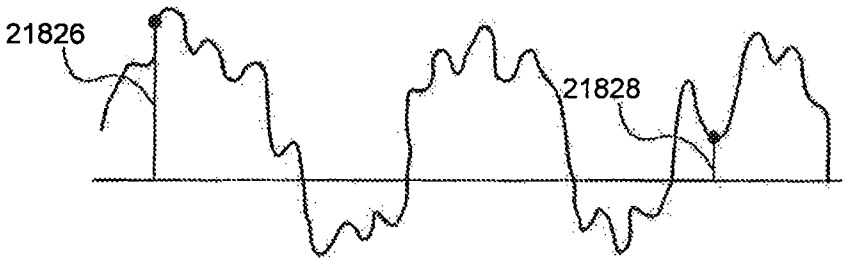


FIG. 218G

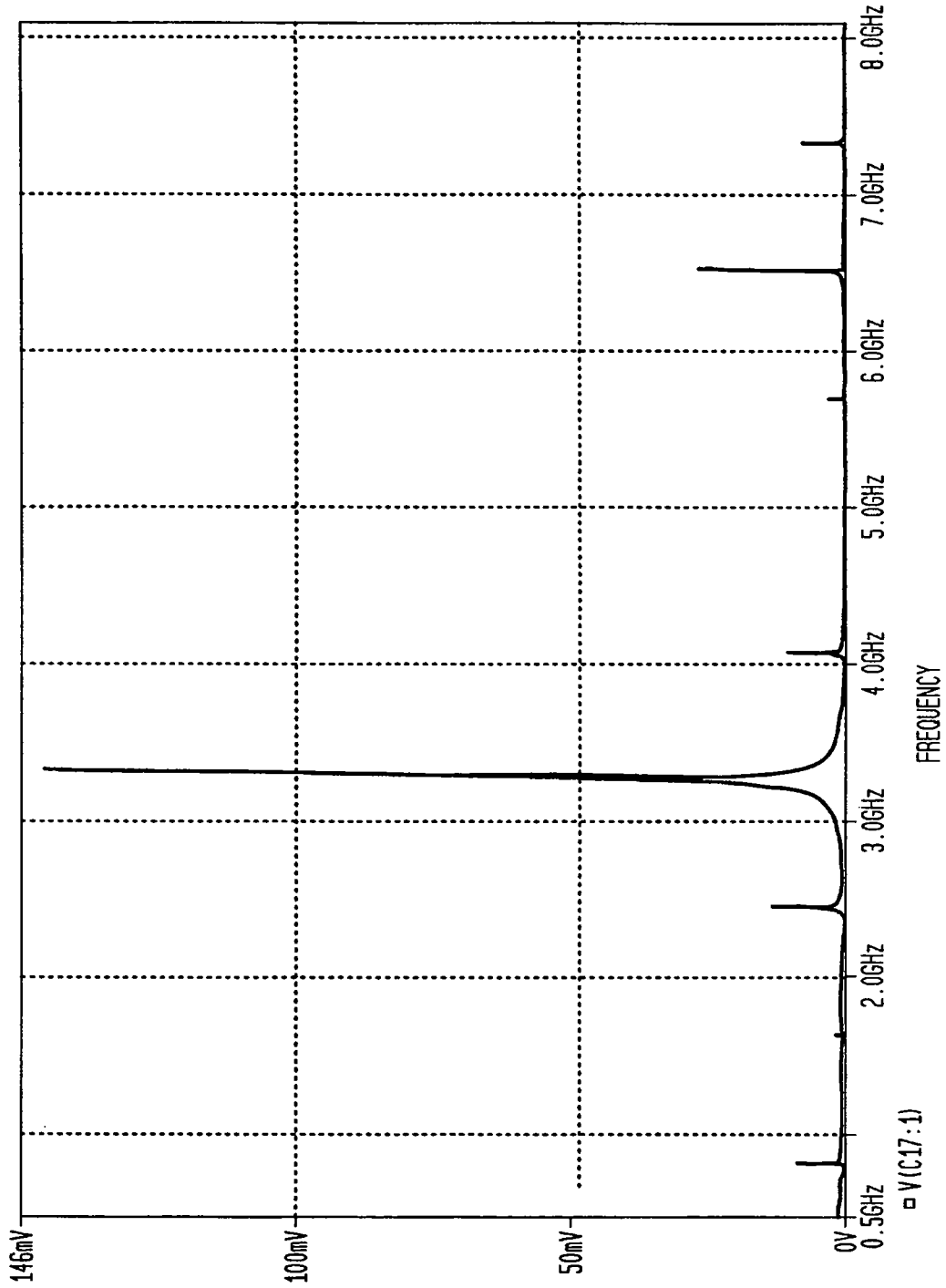

146mV
100mV
50mV
0V
0.5GHz
2.0GHz
3.0GHz
4.0GHz
5.0GHz
6.0GHz
7.0GHz
8.0GHz
FREQUENCY
V(C17:1)

FIG. 218E

FIG. 219

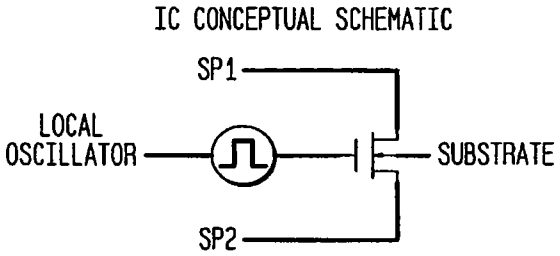
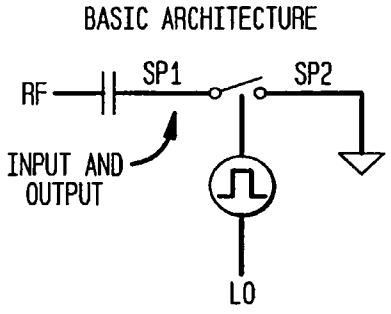


FIG. 220



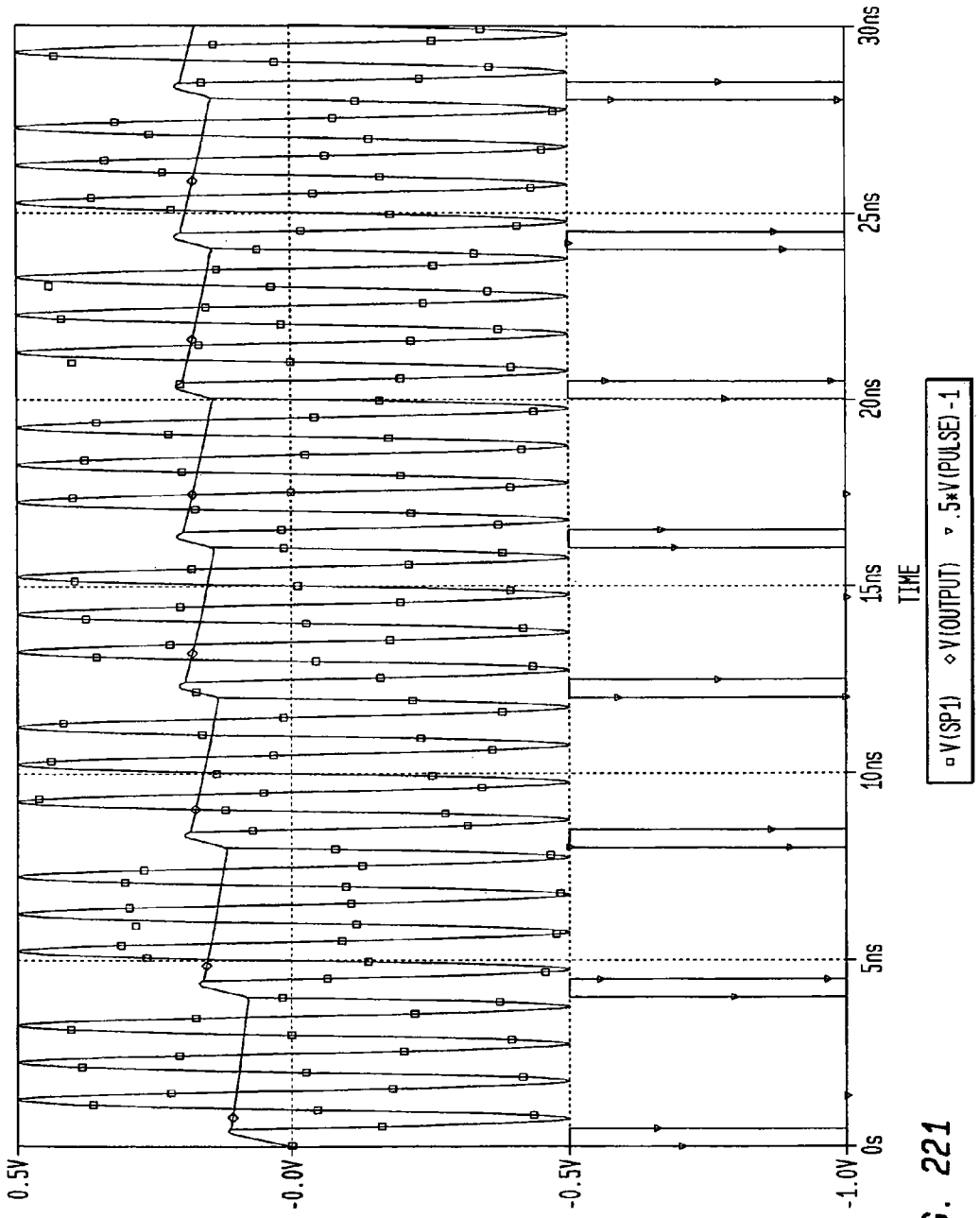

0.5V
-0.0V
-0.5V
-1.0V
0s
5ns
10ns
15ns
20ns
25ns
30ns
TIME
V(SP1)
V(OUTPUT)
.5*V(PULSE)-1

FIG. 221

FIG. 222

DC EQUATIONS

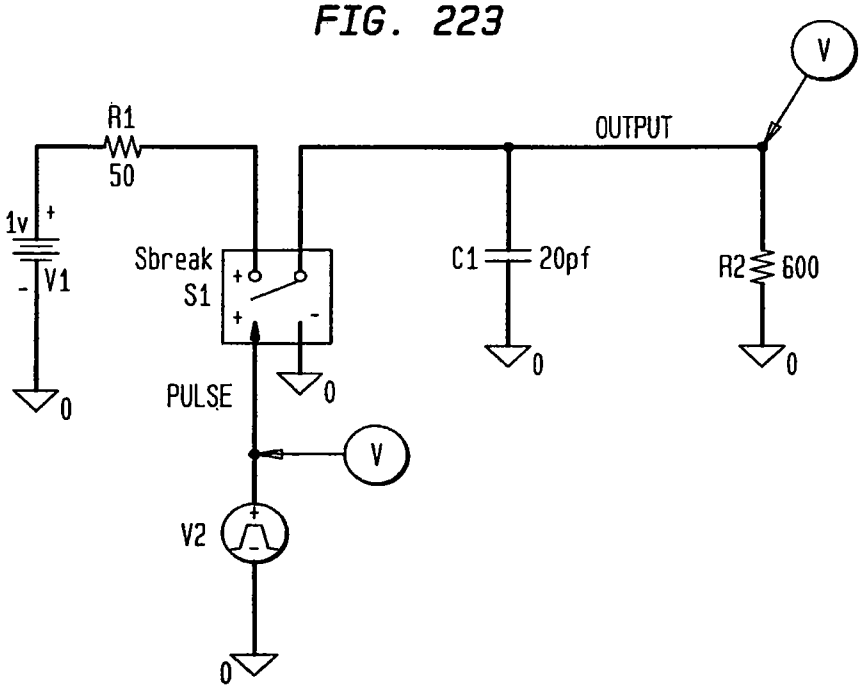
$$Vin=V\cdot\frac{Rout}{Rin+Rout}$$

$$Vc=Vin-(Vin-Vinit)\cdot\exp\left(\frac{-tc}{Rin\cdot C}\right)$$

$$Vd=Vc\cdot\exp\left(\frac{-td}{Rout\cdot C}\right)$$

DEFINITIONS:
- Rin - INPUT RESISTANCE
- Rout - OUTPUT RESISTANCE
- C - CAPACITOR
- tc - CHARGE TIME OR APERATURE
- td - DISCHARGE TIME OR LO PERIOD-tc
- V - INPUT VOLTAGE
- Vinit - INITIAL CAPACITOR VOLTAGE
- Vc - FINAL CHARGE CAPACITOR VOLTAGE
- Vd - FINAL DISCHARGE CAPACITOR VOLTAGE

FIG. 223



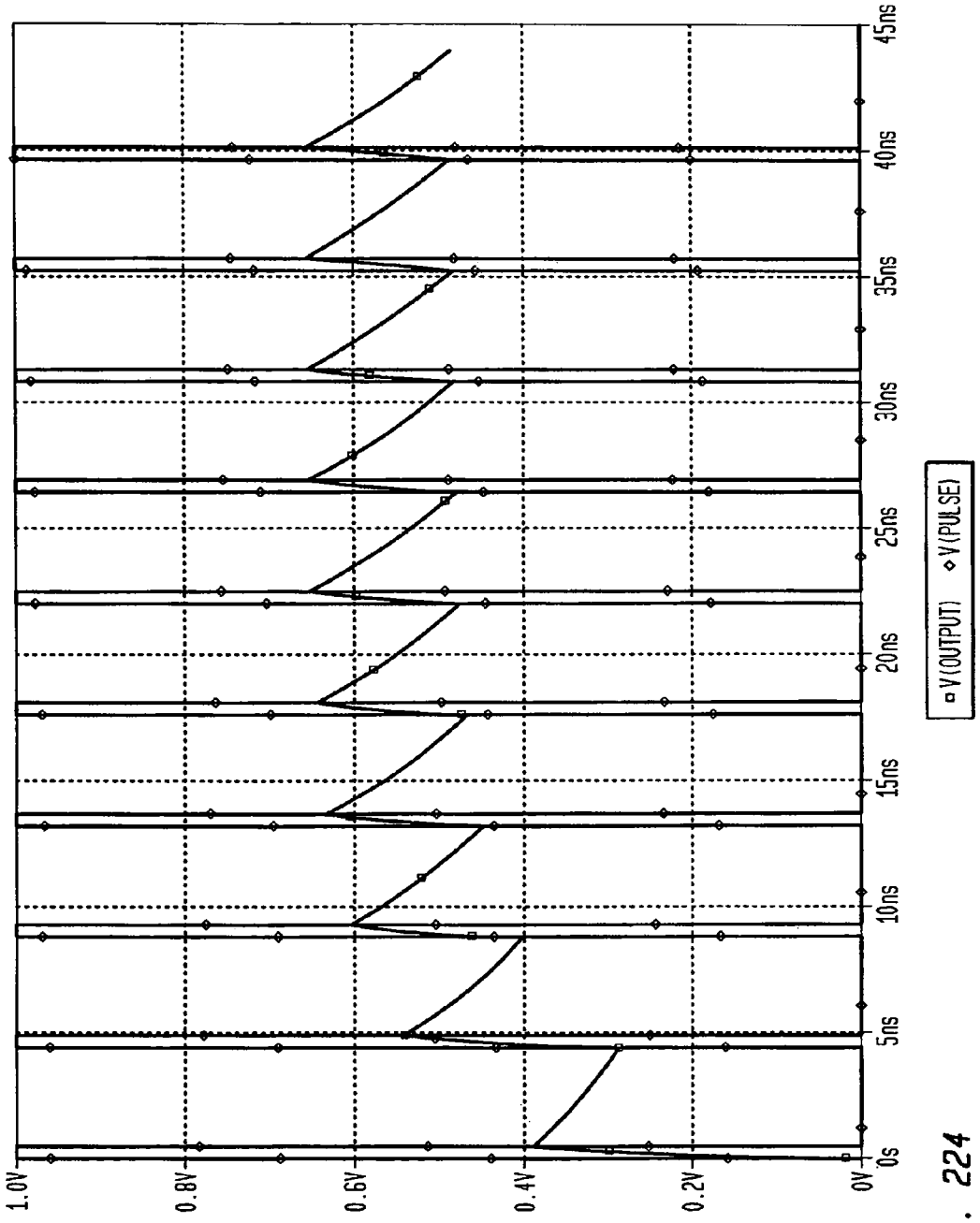
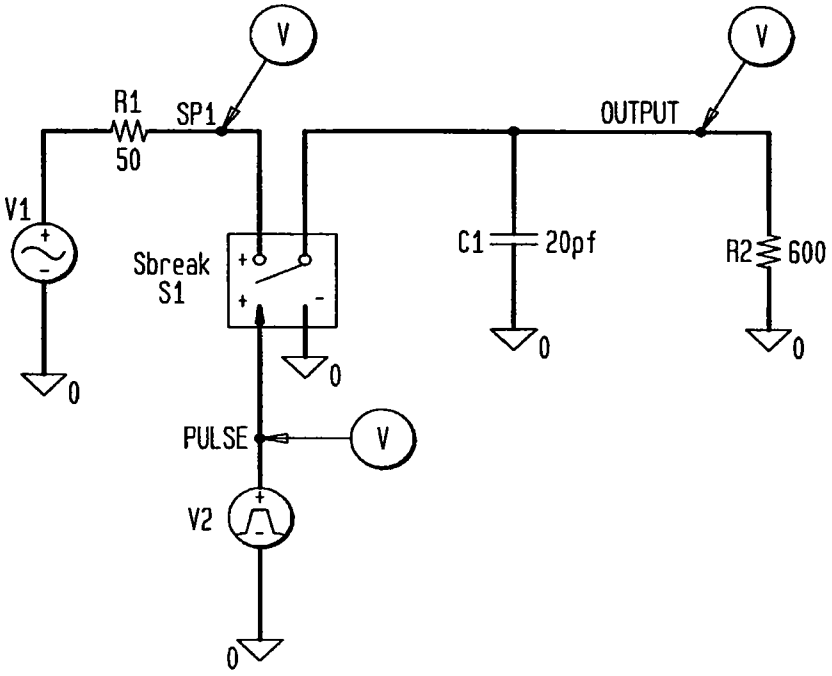

1.0V
0.8V
0.6V
0.4V
0.2V
0V
0s
5ns
10ns
15ns
20ns
25ns
30ns
35ns
40ns
45ns
V(OUTPUT)
V(PULSE)

FIG. 224

FIG. 225



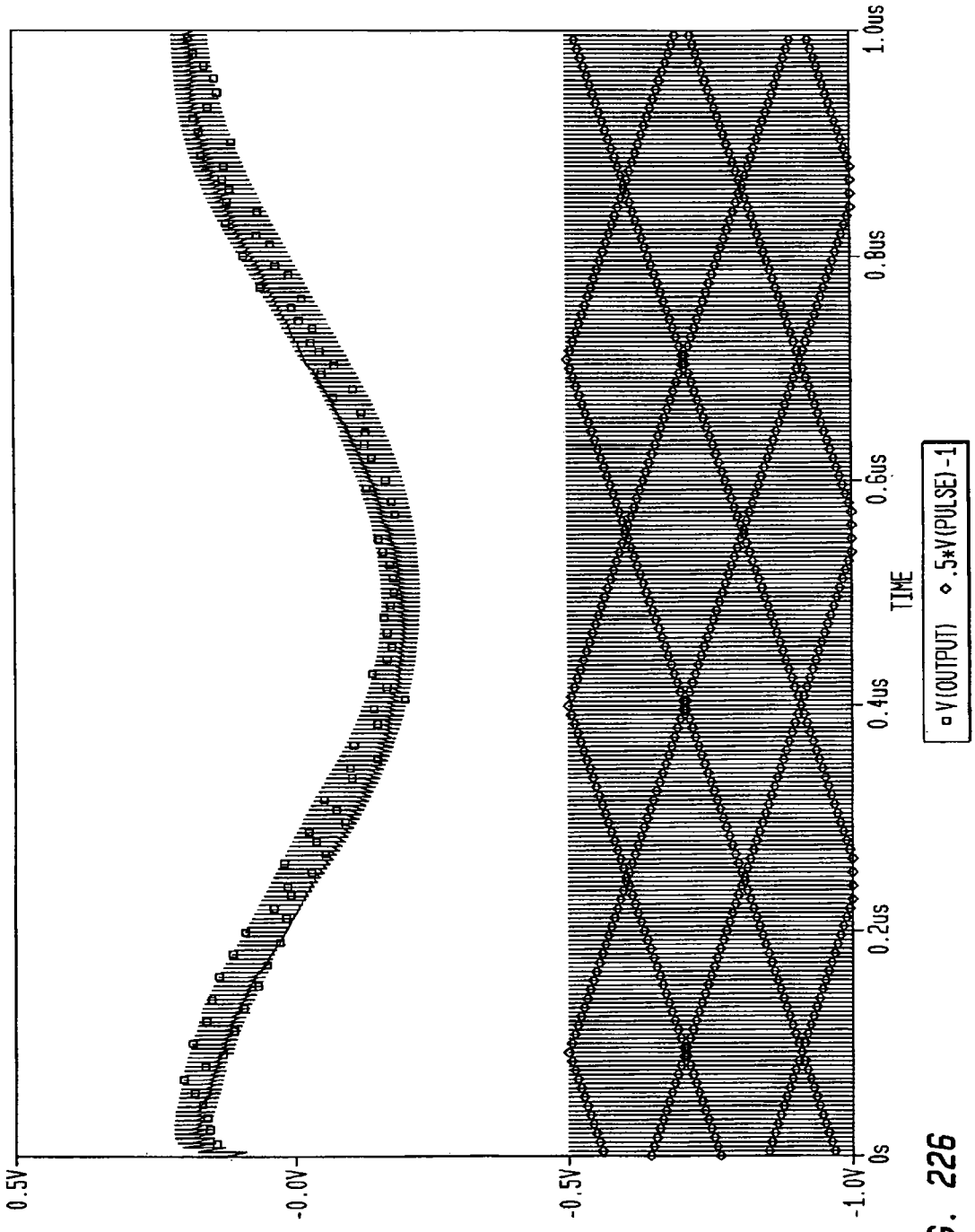

0.5V
-0.0V
-0.5V
-1.0V
0s
0.2us
0.4us
0.6us
0.8us
1.0us
TIME
V(OUTPUT)
.5*V(PULSE)-1

FIG. 226

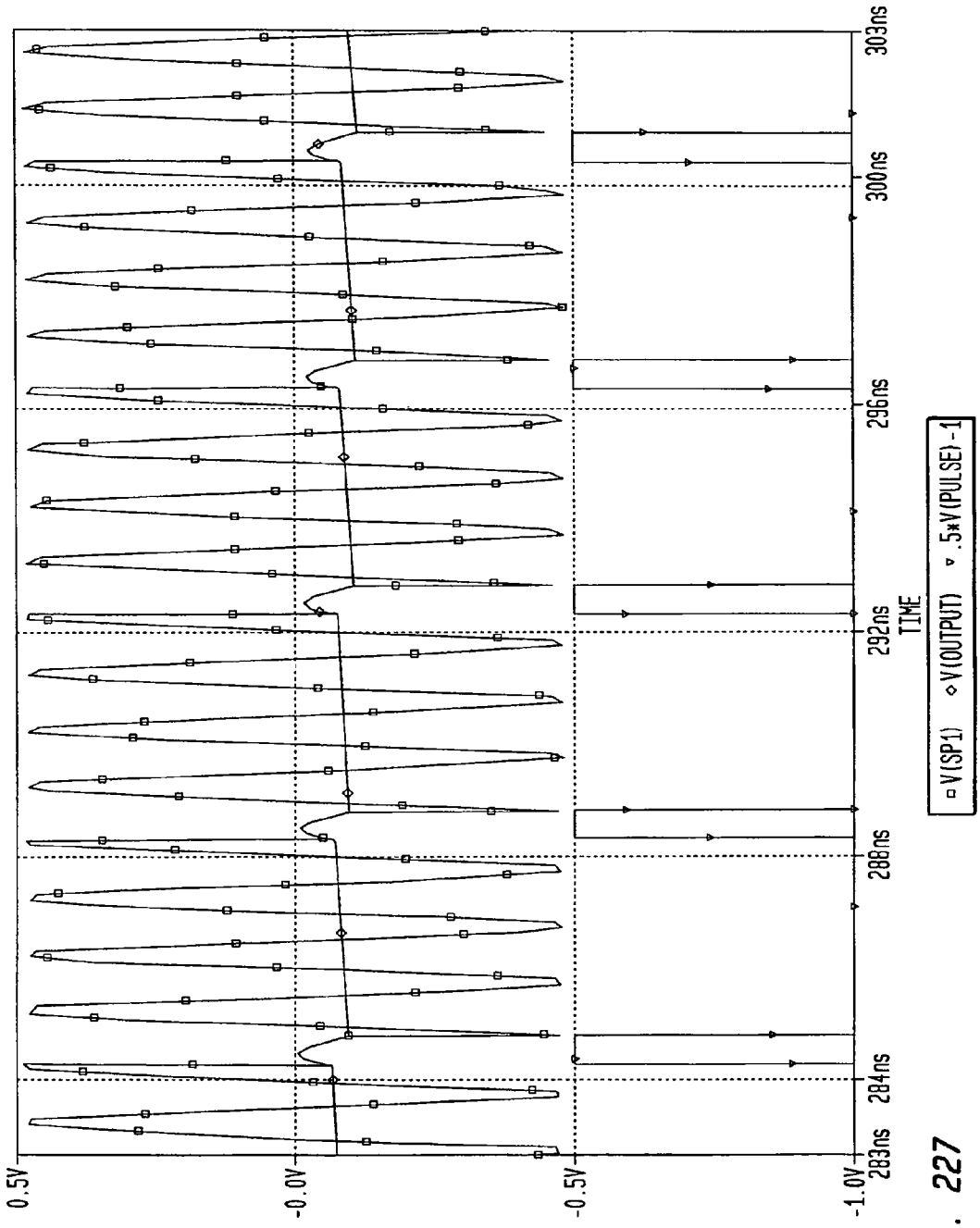

0.5V
-0.0V
-0.5V
-1.0V
283ns
284ns
288ns
292ns
296ns
300ns
303ns
TIME
V(SP1)
V(OUTPUT)
.5*V(PULSE)-1

FIG. 227

FIG. 228

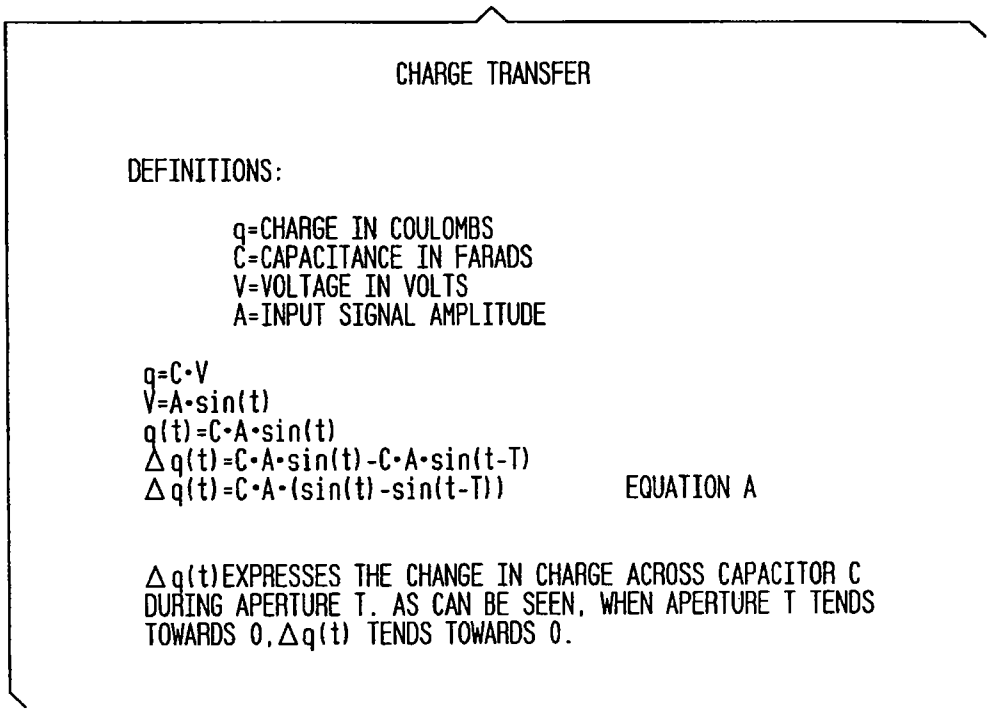

CHARGE TRANSFER
DEFINITIONS:
q=CHARGE IN COULOMBS
C=CAPACITANCE IN FARADS
V=VOLTAGE IN VOLTS
A=INPUT SIGNAL AMPLITUDE
q=C•V
V=A•sin(t)
q(t)=C•A•sin(t)
Δq(t)=C•A•sin(t)-C•A•sin(t-T)
Δq(t)=C•A•(sin(t)-sin(t-T))
EQUATION A
Δq(t)EXPRESSES THE CHANGE IN CHARGE ACROSS CAPACITOR C DURING APERTURE T. AS CAN BE SEEN, WHEN APERTURE T TENDS TOWARDS 0, Δq(t) TENDS TOWARDS 0.

FIG. 229

USING THE SUM TO PRODUCT TRIGONOMETRIC IDENTITY,

$$\sin(\alpha)-\sin(\beta)=2\cdot\sin\left(\frac{\alpha-\beta}{2}\right)\cdot\cos\left(\frac{\alpha+\beta}{2}\right) \qquad \text{IDENTITY 1}$$

EQUATION 1 CAN BE RE-WRITTEN AS:

$$\Delta q(t)=2\cdot C\cdot A\cdot\sin\left[\frac{t-(t-T)}{2}\right]\cdot\cos\left[\frac{t+(t-T)}{2}\right]$$

$$\Delta q(t)=2\cdot C\cdot A\cdot\sin\left(\frac{1}{2}\cdot T\right)\cdot\cos\left(t-\frac{1}{2}\cdot T\right) \qquad \text{EQUATION B}$$

THE sin TERM IN EQUATION B IS A FUNCTION OF APERTURE T ONLY. IT IS EASILY SEEN THAT $\Delta q(t)$ WILL OBTAIN A MAXIMUM VALUE WHEN T IS EQUAL TO AN ODD MULTIPLE OF π i.e., π 3 π 5 π.. THEREFORE, CAPACITOR C EXPERIENCES THE GREATEST CHANGE IN CHARGE WHEN THE APERTURE HAS A VALUE OF π OR A TIME INTERVAL REPRESENTATIVE OF 180 DEGREES OF THE INPUT SINUSOID. CONVERSELY, WHEN T IS EQUAL TO 2π, 4π, 6π....MINIMAL CHARGE IS TRANSFERRED.

FIG. 230

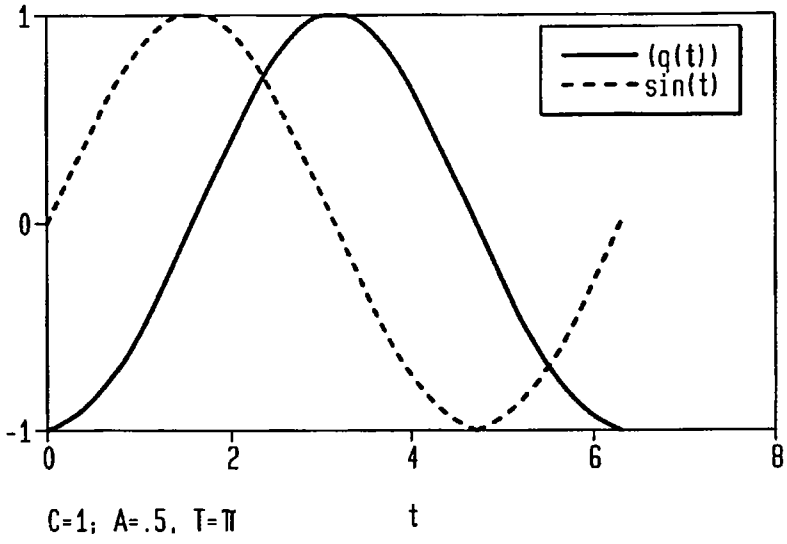
SOLVING FOR q(t) BY INTEGRATING EQUATION A ALLOWS THE CHARGE ON C WITH RESPECT TO TIME TO BE GRAPHED ON THE SAME AXIS AS THE INPUT SINUSOID sin(t).

$$q(t)=\int C\cdot A\cdot(\sin(t)-\sin(t-T))dt$$

$$q(t)=-\cos(t)\cdot C\cdot A+\cos(t-T)\cdot C\cdot A$$

$$q(t)=C\cdot A\cdot(\cos(t-T)-\cos(t)) \quad \text{EQUATION C}$$

FIG. 231



GRAPH 1

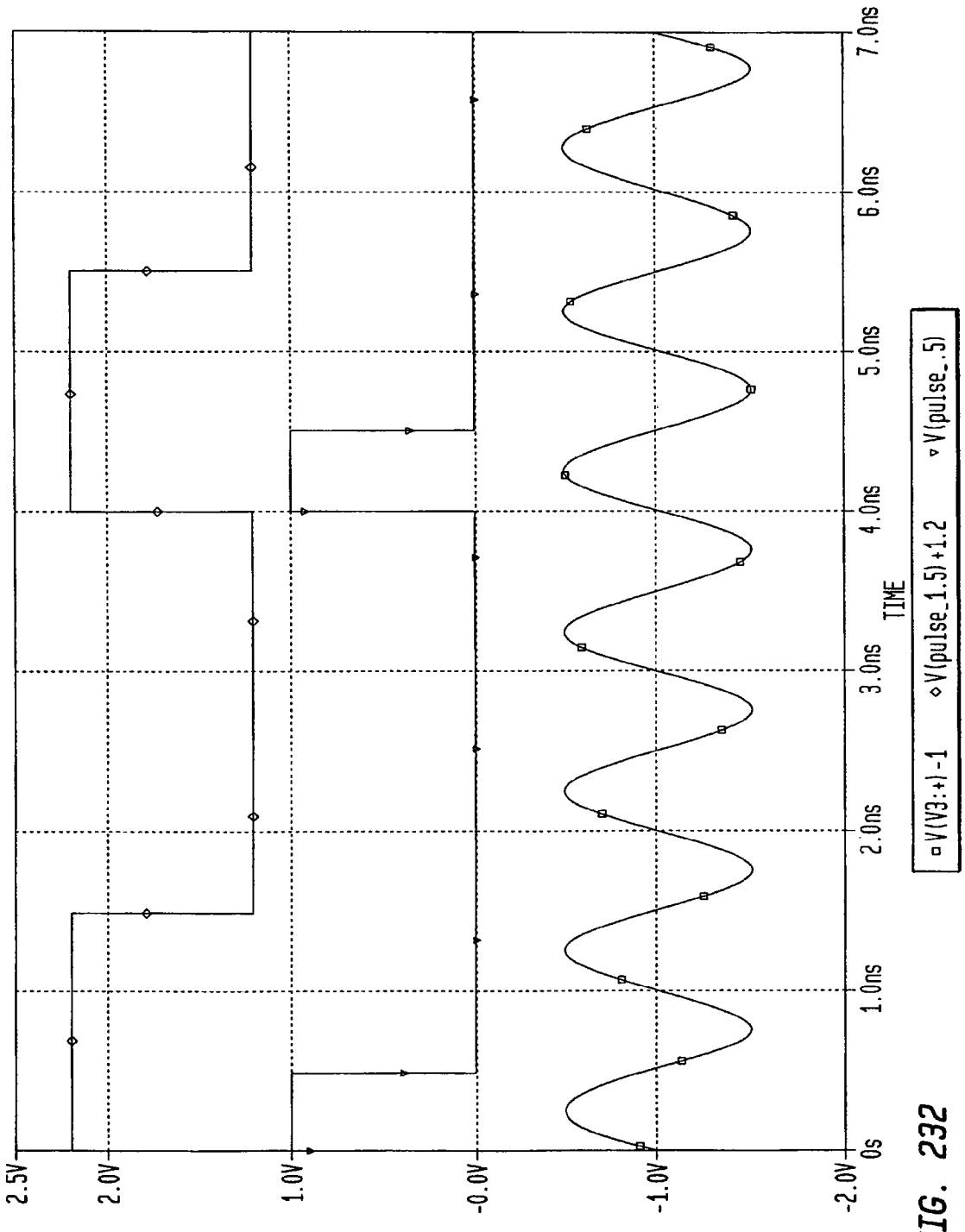

2.5V
2.0V
1.0V
-0.0V
-1.0V
-2.0V
0s
1.0ns
2.0ns
3.0ns
4.0ns
5.0ns
6.0ns
7.0ns
TIME
V(V3:+)-1
V(pulse_1.5)+1.2
V(pulse_.5)

FIG. 232

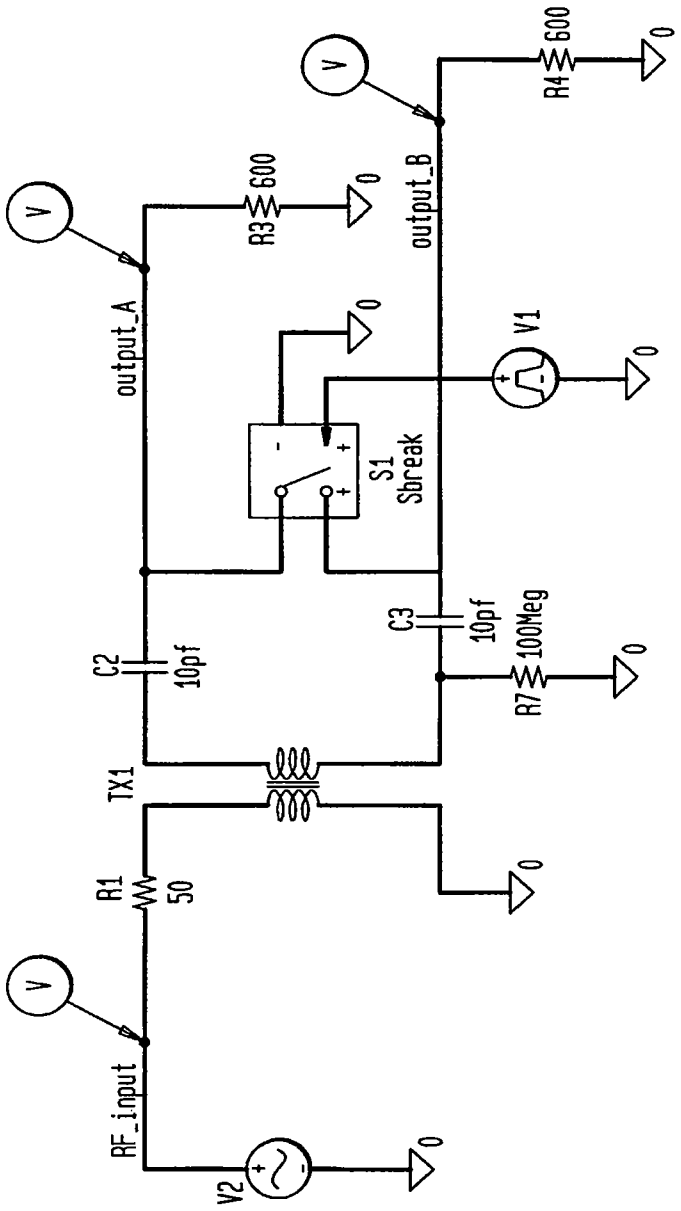

R4
600
0
output_B
R3
600
output_A
V1
S1
Sbreak
C3
10pf
100Meg
C2
10pf
TX1
R1
50
RF_input
V2

FIG. 233

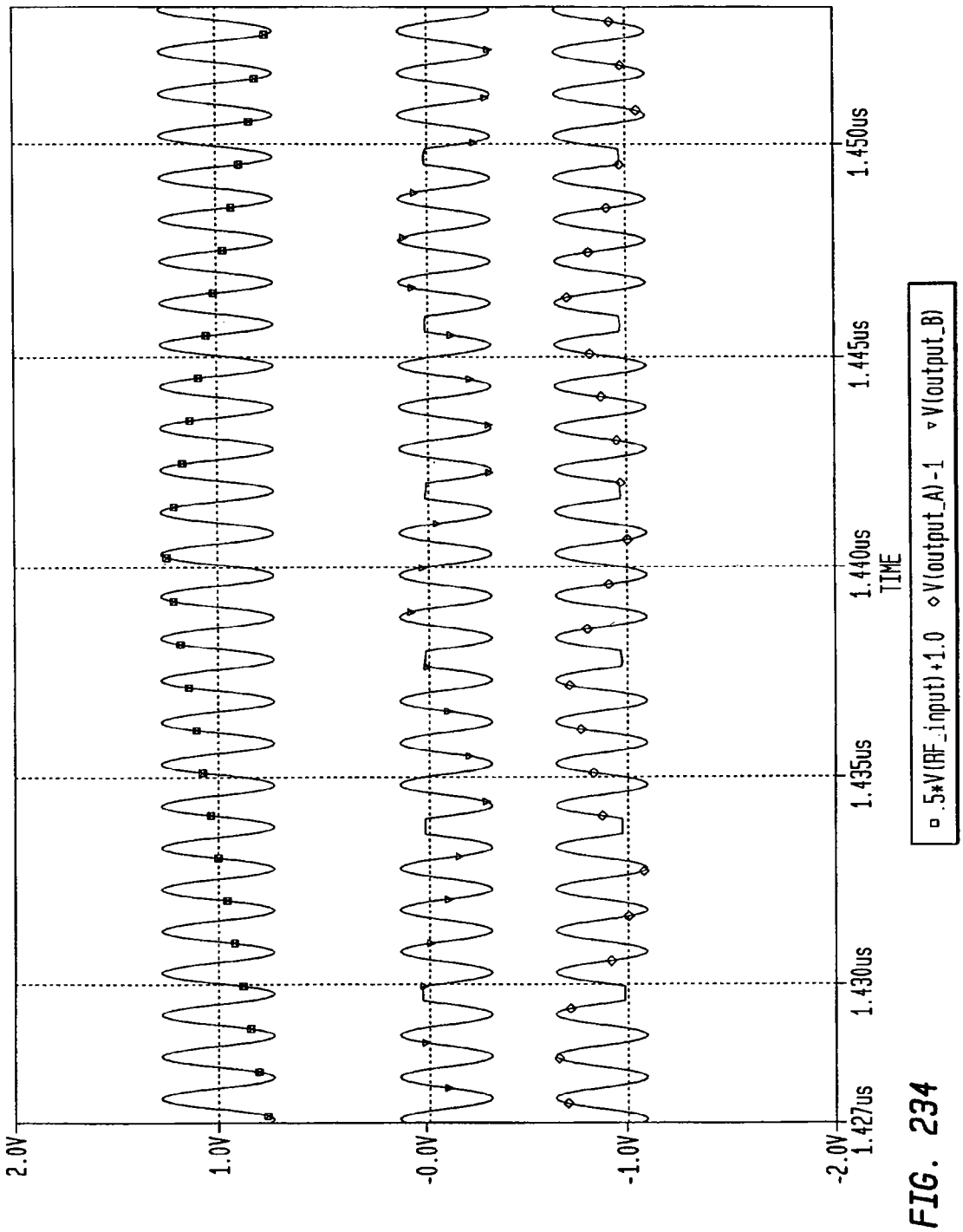

2.0V
1.0V
-0.0V
-1.0V
-2.0V
1.427us
1.430us
1.435us
1.440us
1.445us
1.450us
TIME
□ .5*V(RF_input)+1.0
◇ V(output_A)-1
▽ V(output_B)

FIG. 234

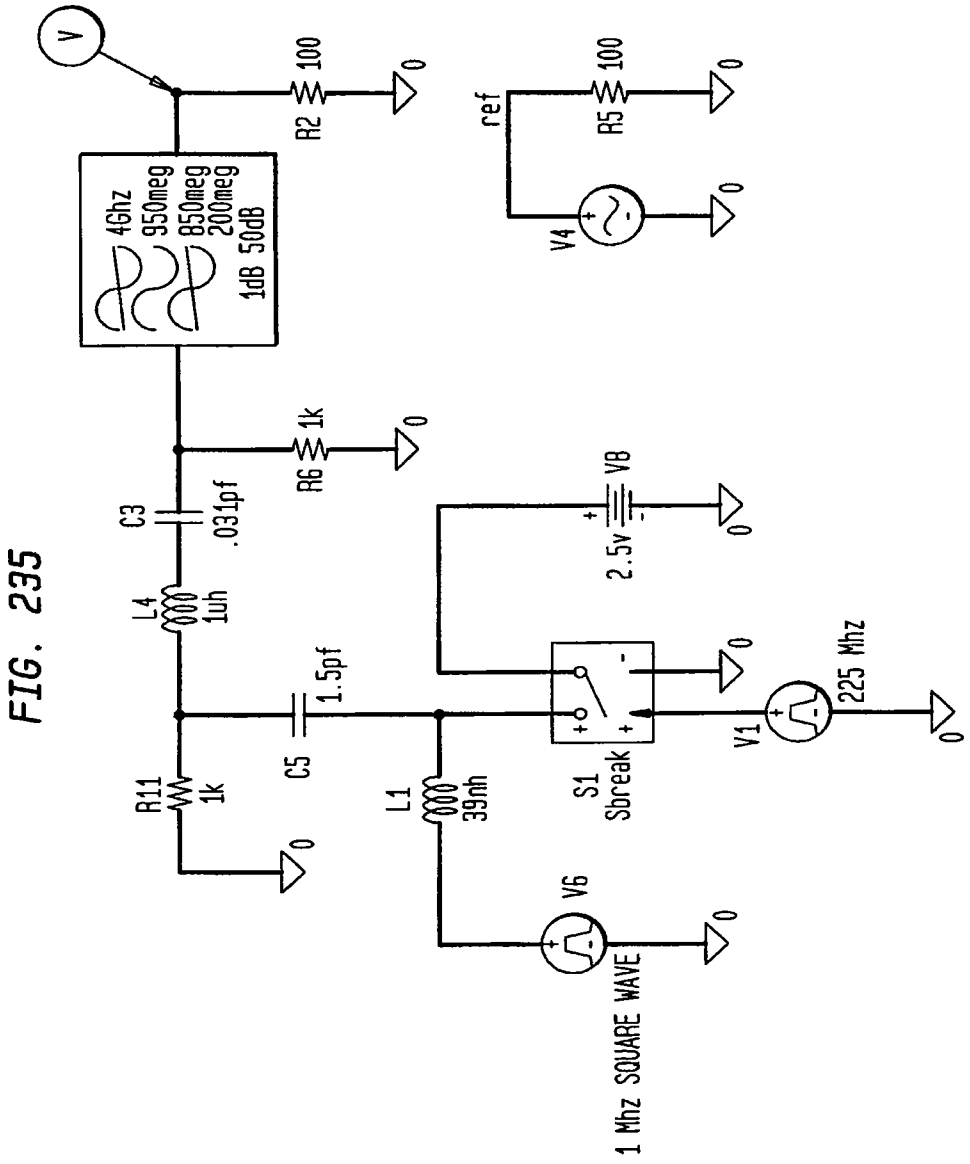

V
R2
100
0
4Ghz
950meg
850meg
200meg
1dB 50dB
ref
R5
100
V4
R6
1k
C3
.031pf
L4
1uh
V8
2.5v
C5
1.5pf
S1
Sbreak
V1
225 Mhz
R11
1k
L1
39nh
V6
1 Mhz SQUARE WAVE

FIG. 235

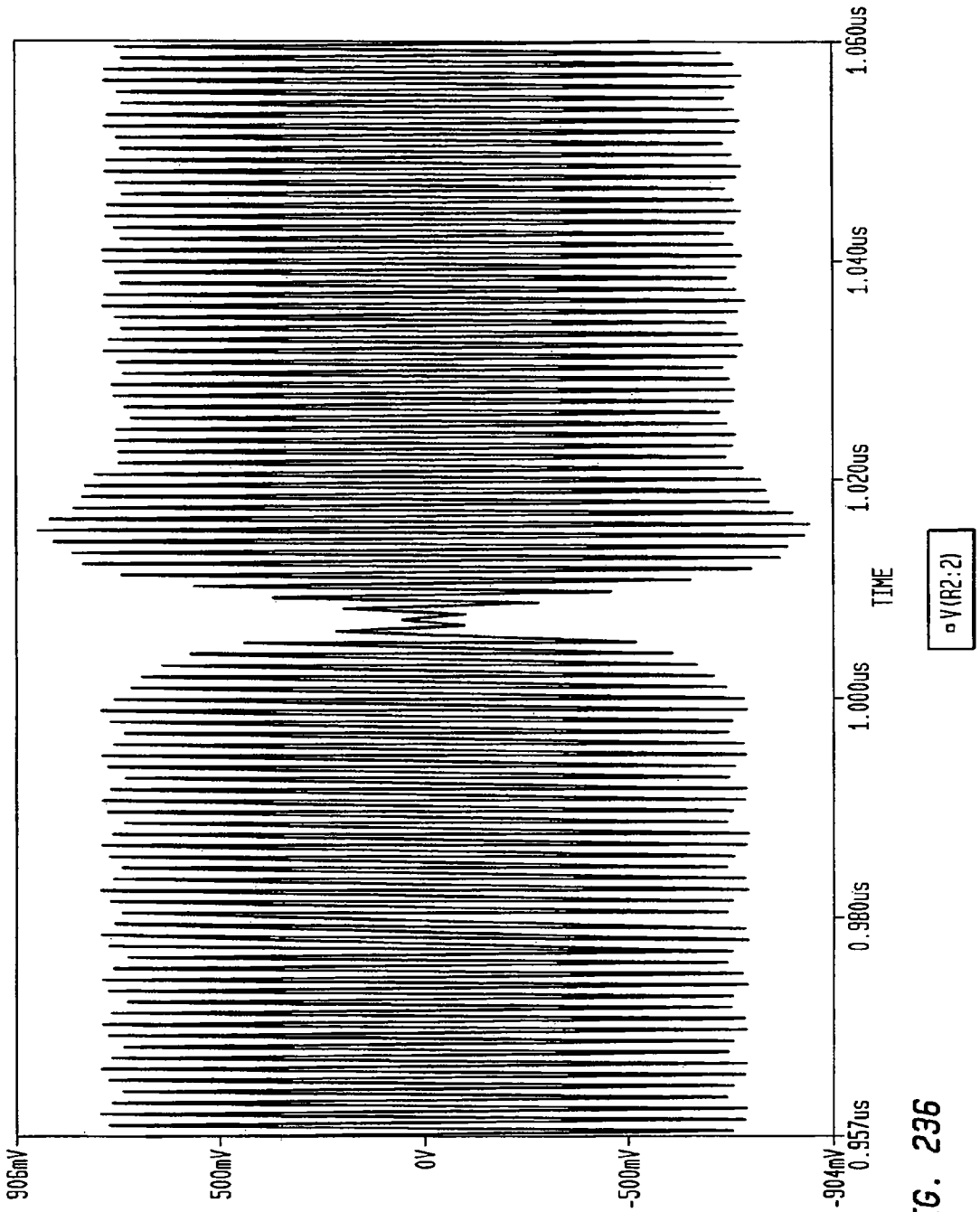

906mV
500mV
0V
-500mV
-904mV
0.957us
0.980us
1.000us
1.020us
1.040us
1.060us
TIME
V(R2:2)

FIG. 236

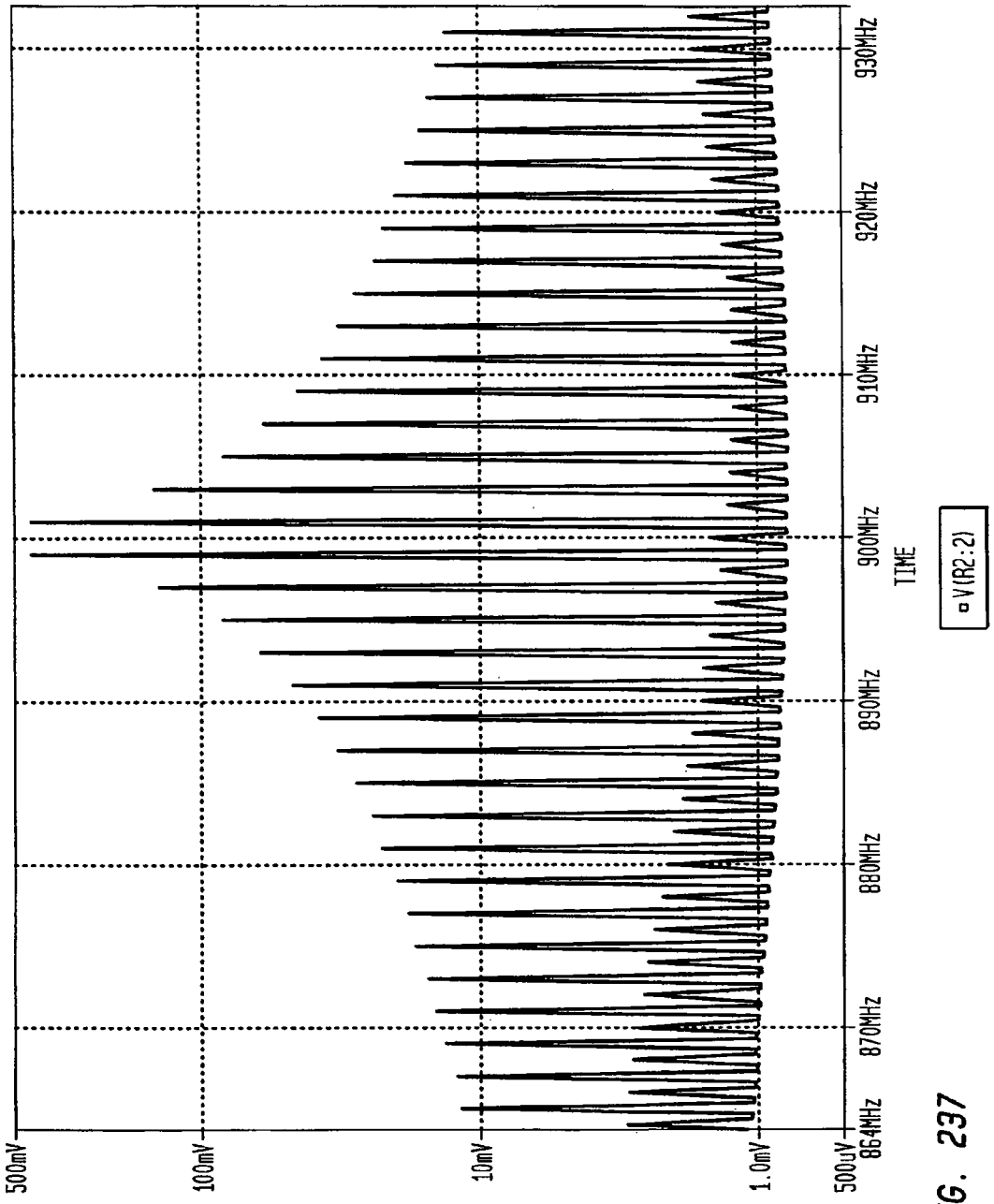

500mV
100mV
10mV
1.0mV
500uV
864MHz
870MHz
880MHz
890MHz
900MHz
910MHz
920MHz
930MHz
TIME
V(R2:2)

FIG. 237

FIG. 238

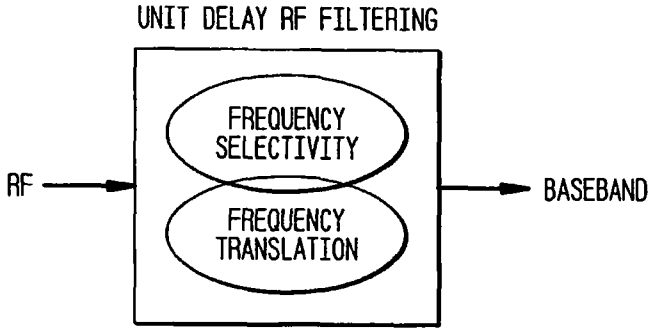


FIG. 239

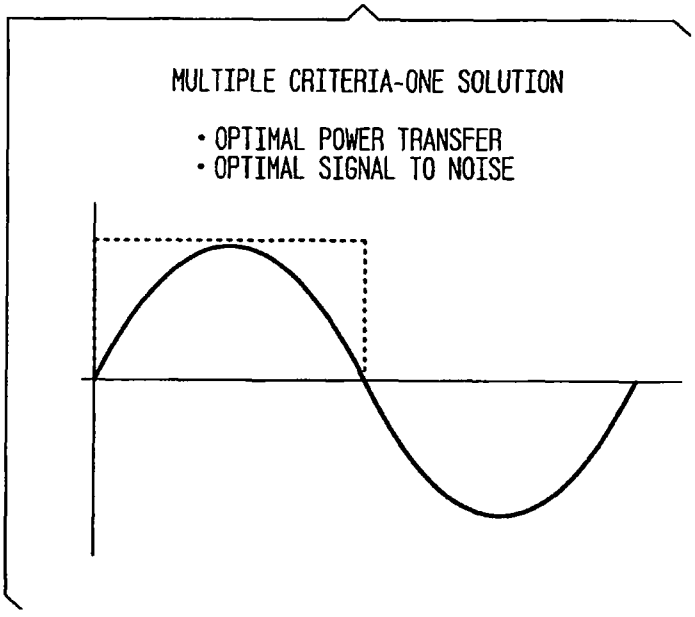


FIG. 240

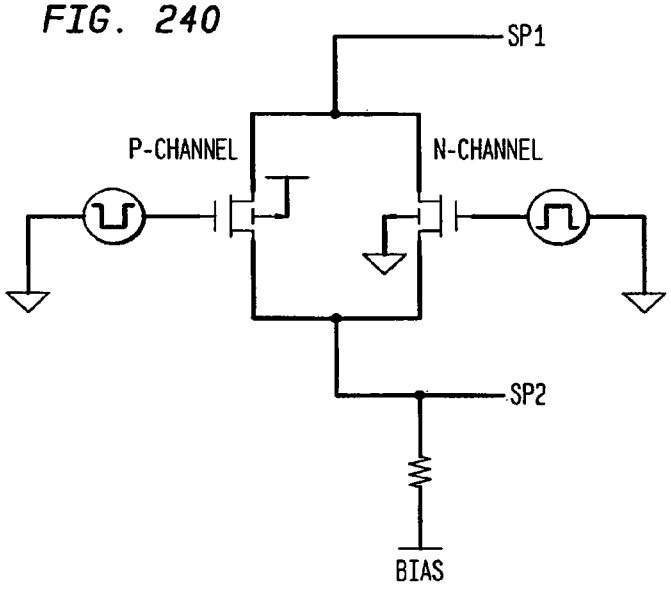


FIG. 241

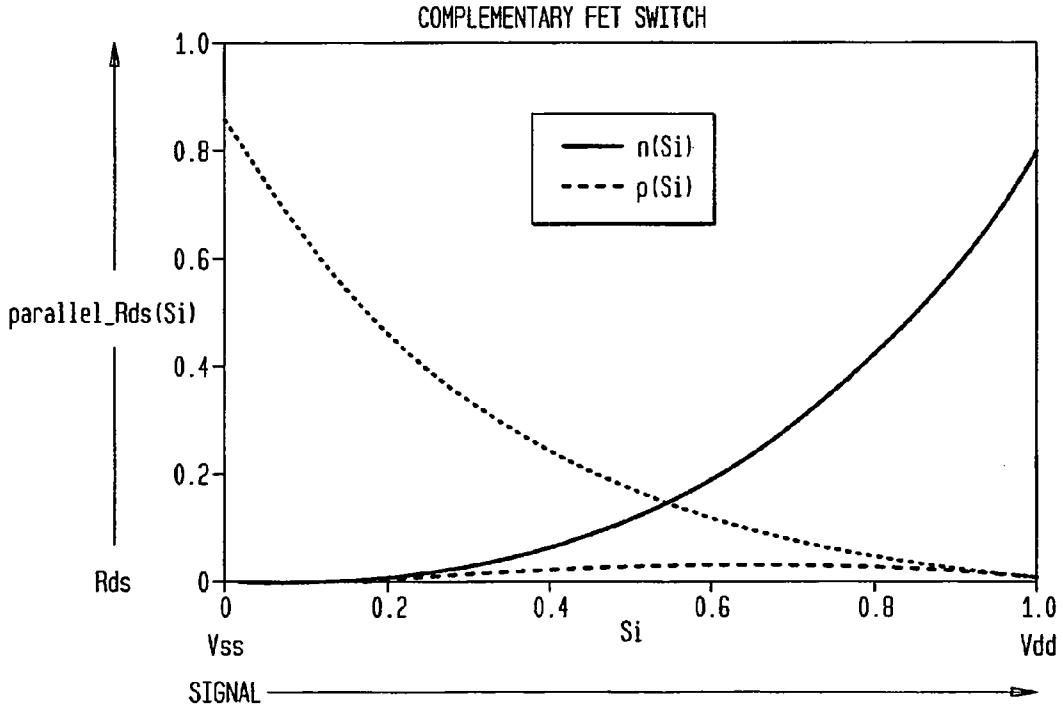
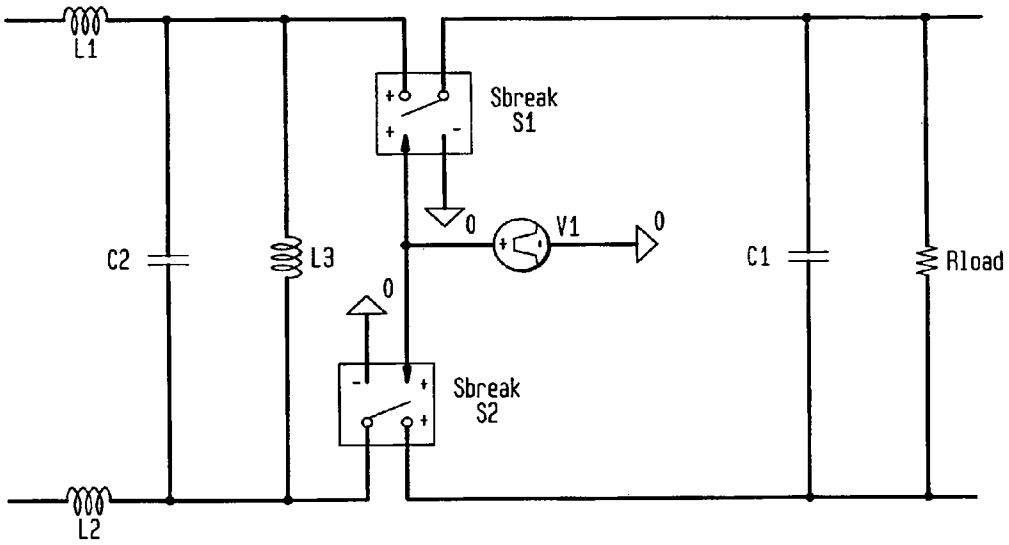


FIG. 242

DIFFERENTIAL CONFIGURATION



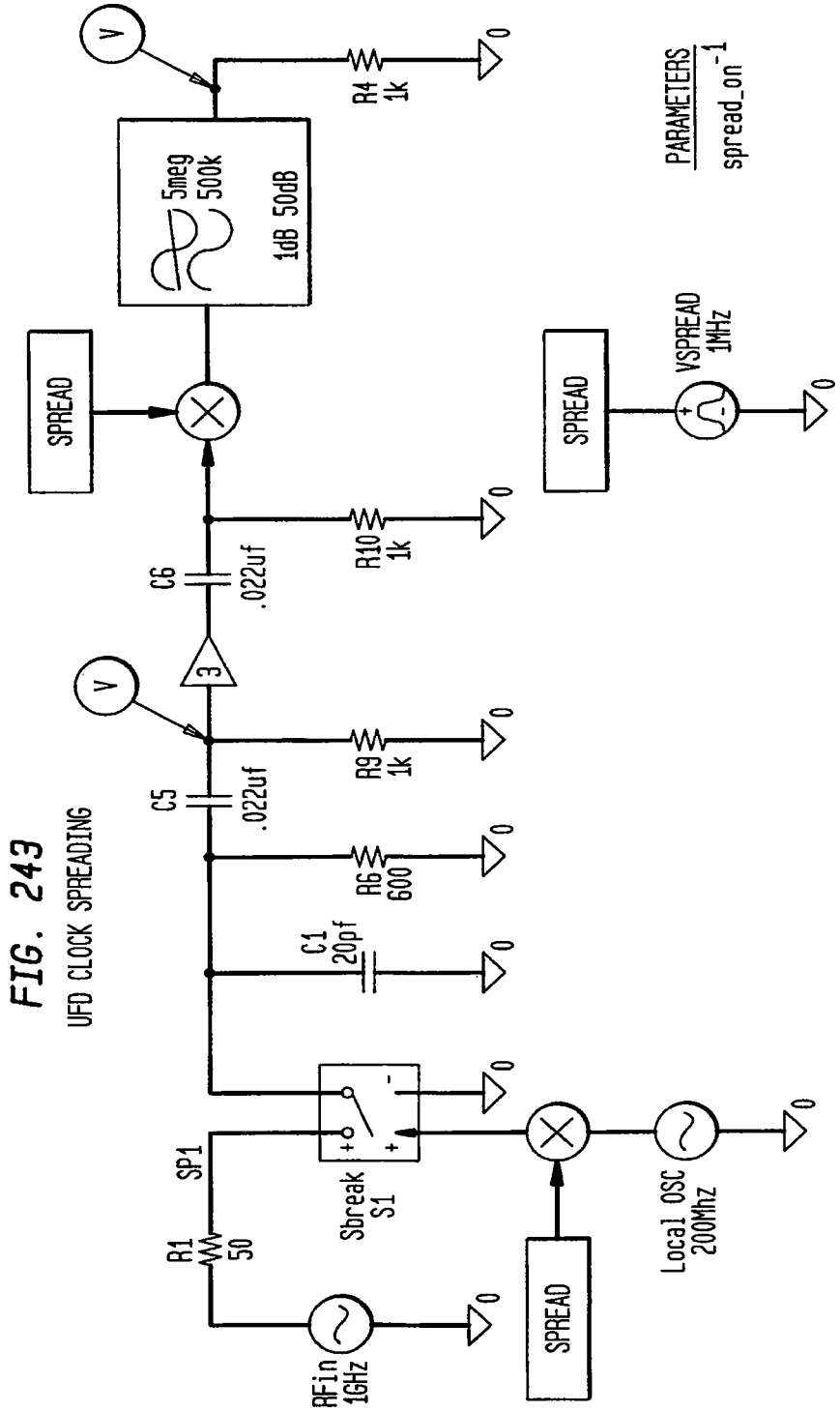


FIG. 243
UFD CLOCK SPREADING

FIG. 244

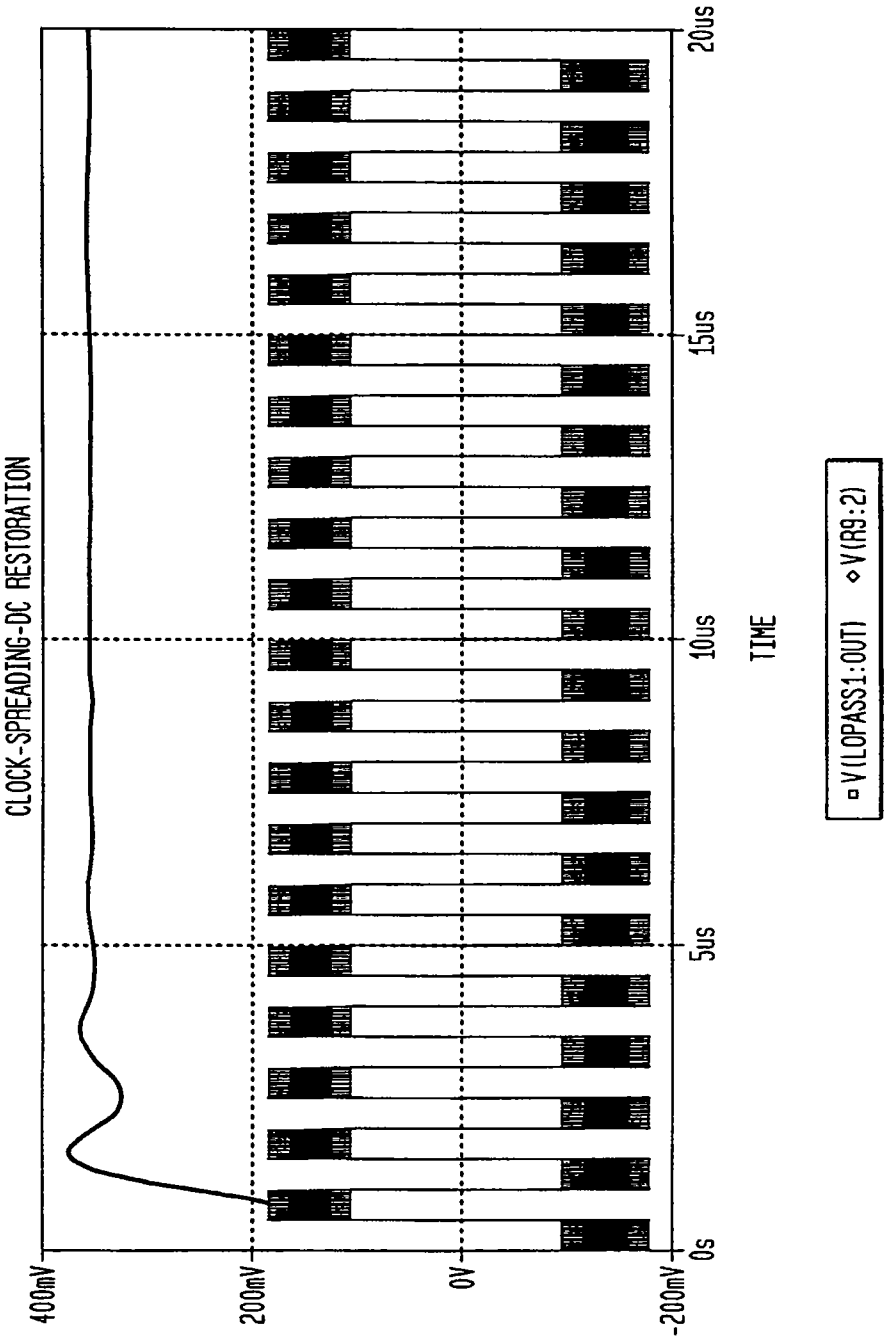

CLOCK-SPREADING-DC RESTORATION
400mV
200mV
0V
-200mV
0s
5us
10us
15us
20us
TIME
V(LOPASS1:OUT)
V(R9:2)

FIG. 245

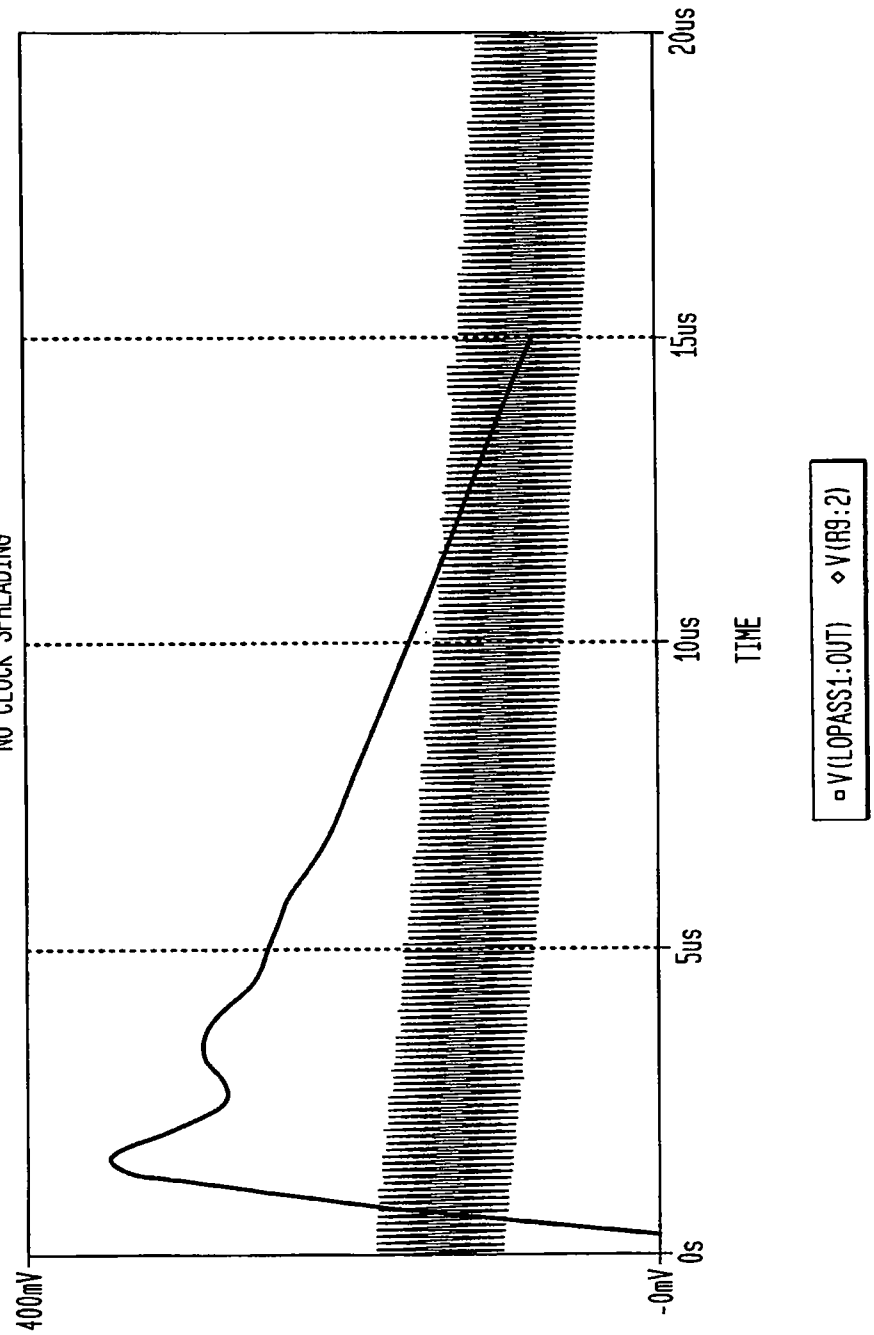

NO CLOCK SPREADING
400mV
-0mV
0s
5us
10us
15us
20us
TIME
V(LOPASS1:OUT)
V(R9:2)

FIG. 246

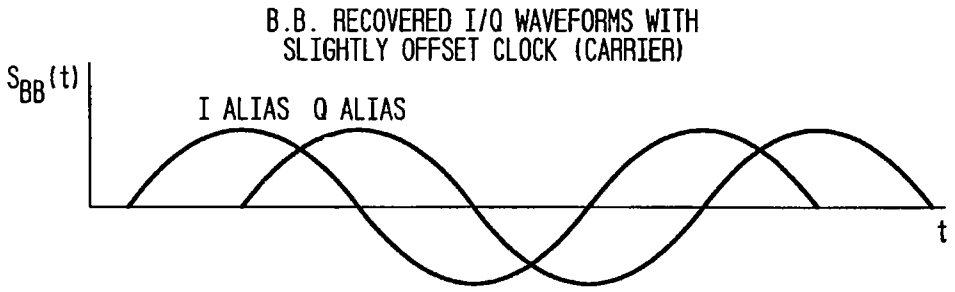


FIG. 247

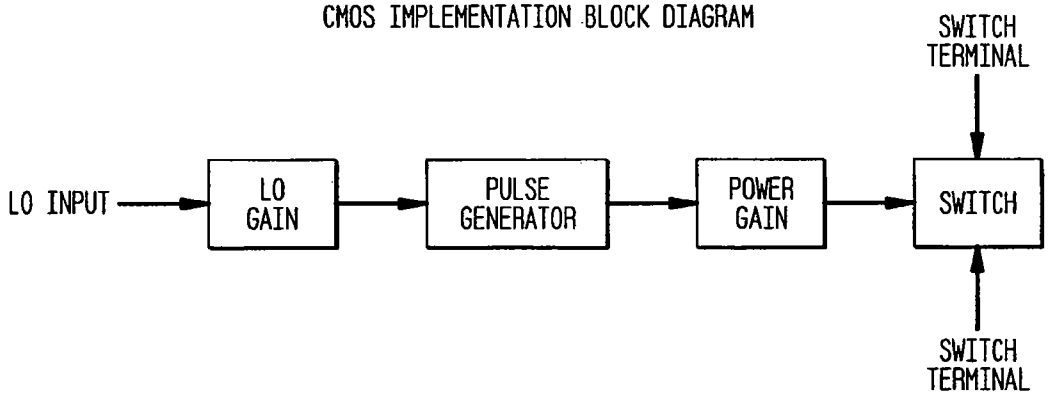


FIG. 248

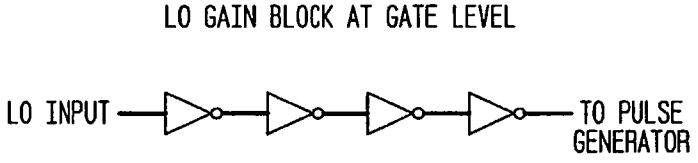


FIG. 249

LO GAIN BLOCK AT TRANSISTOR LEVEL

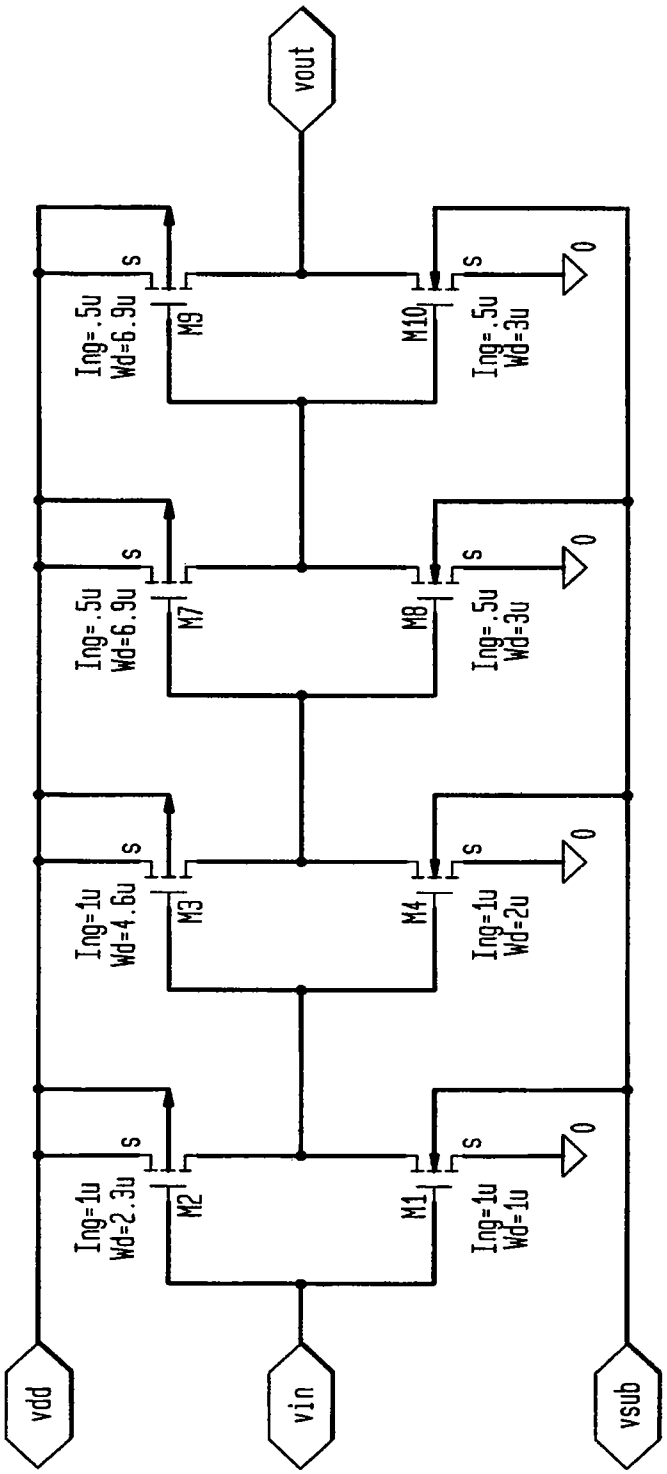


FIG. 250

PULSE GENERATOR#1 AT GATE LEVEL

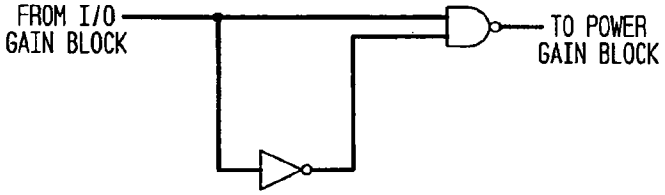


FIG. 251

PULSE GENERATOR#1 AT TRANSISTOR LEVEL

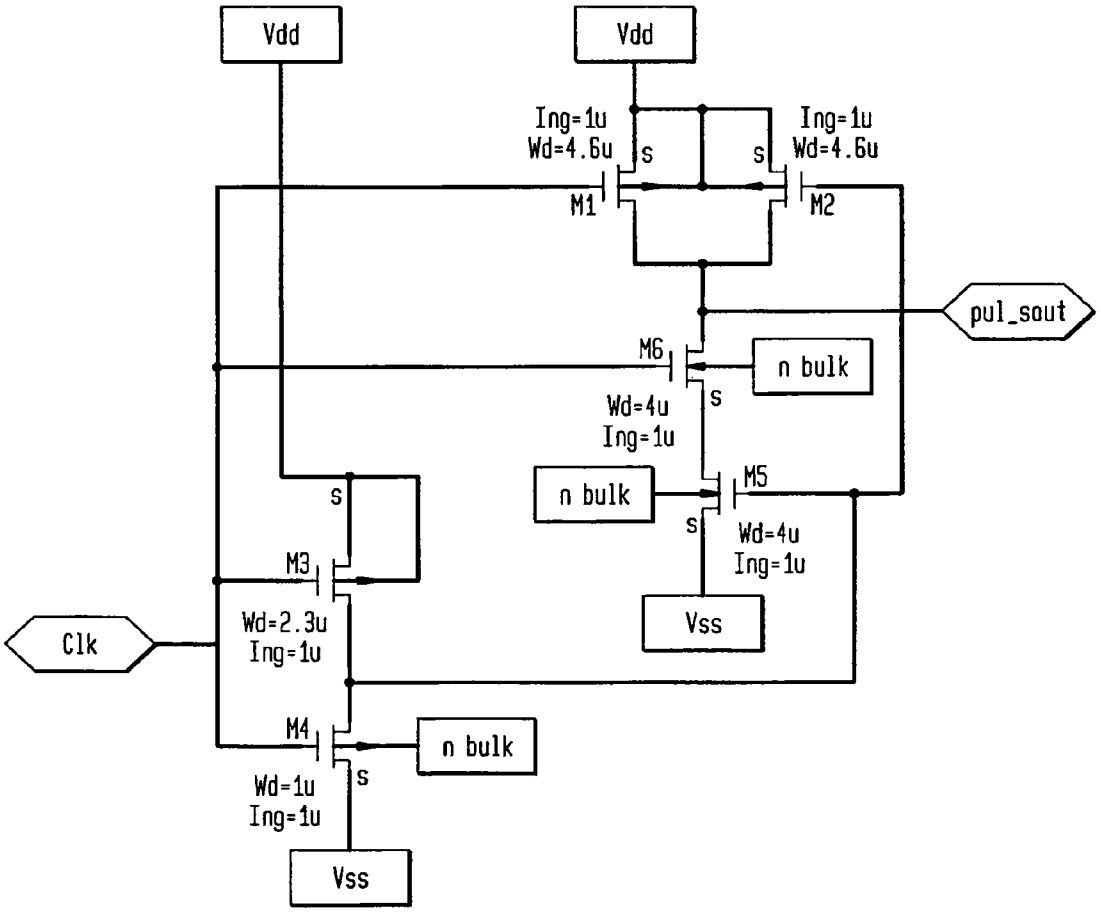


FIG. 252

POWER GAIN BLOCK AT GATE LEVEL

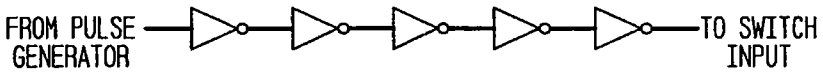


FIG. 253

POWER GAIN BLOCK AT TRANSISTOR LEVEL

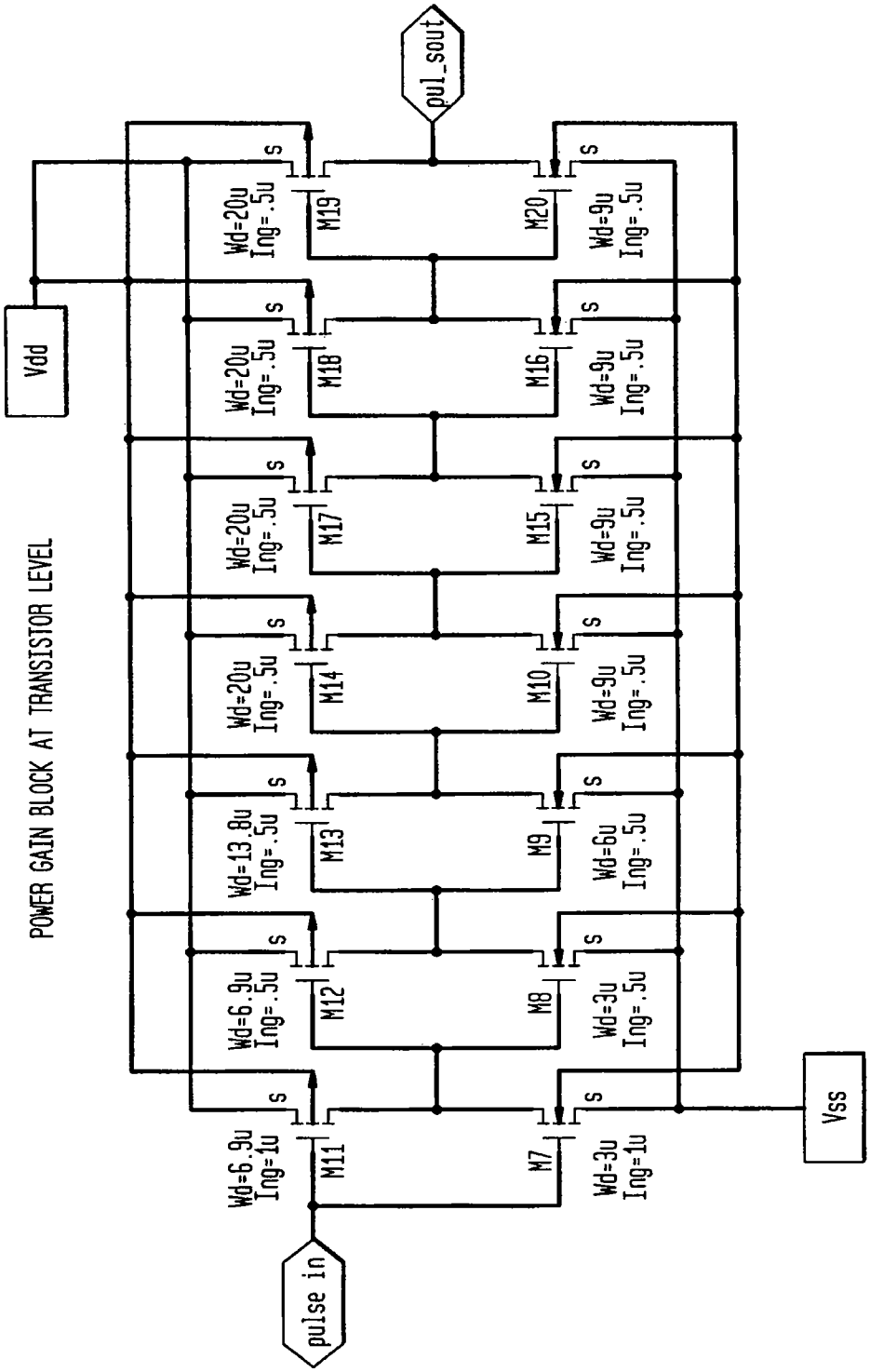


FIG. 254

SWITCH AT TRANSISTOR LEVEL

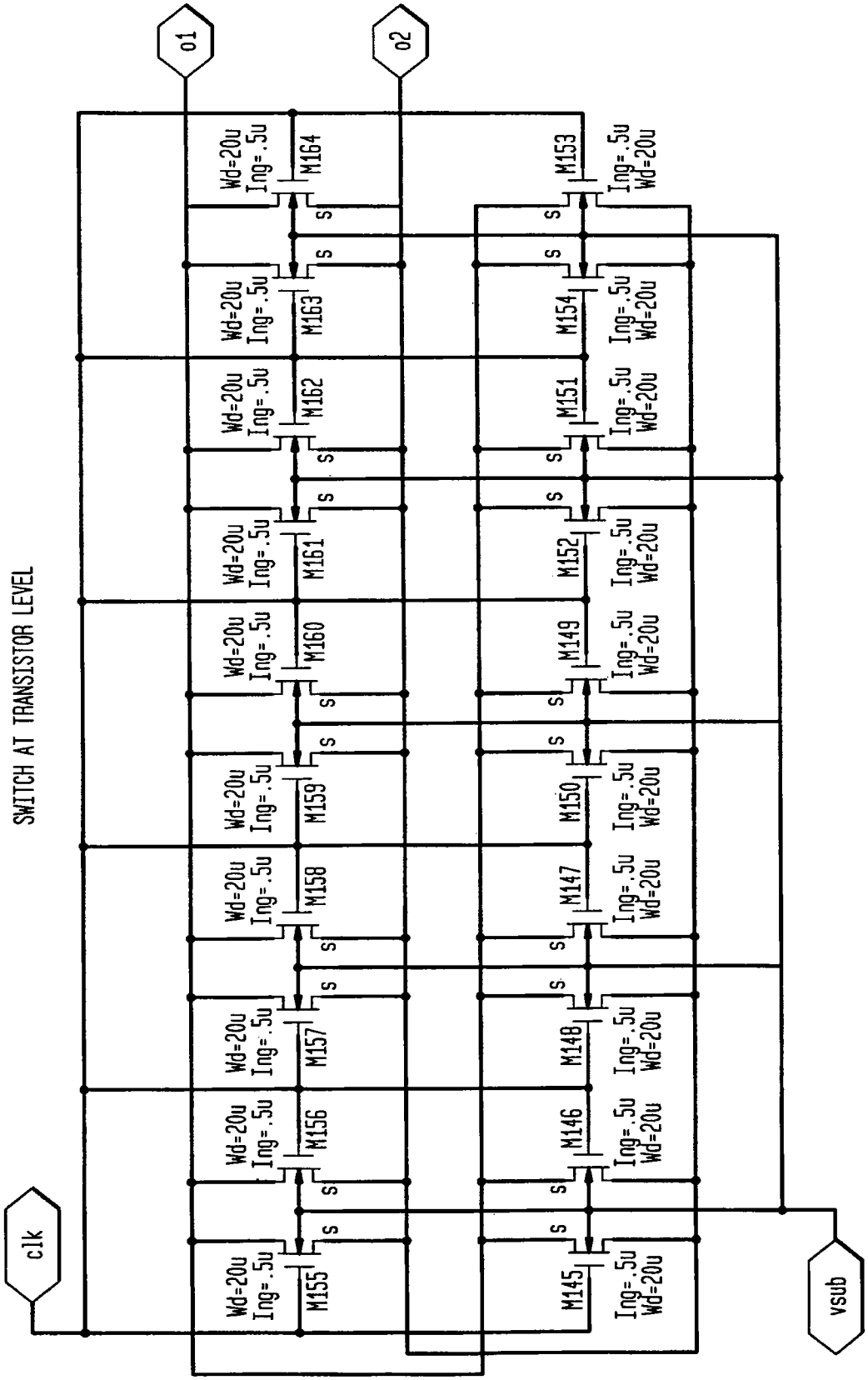


FIG. 255

CMOS "HOT CLOCK" BLOCK DIAGRAM

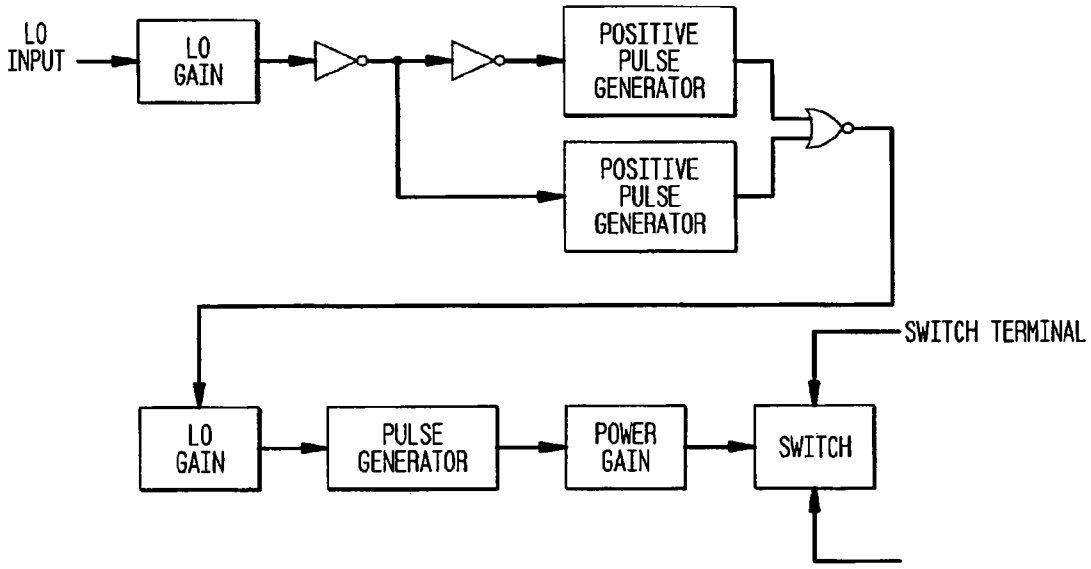


FIG. 256

POSITIVE PULSE GENERATOR AT GATE LEVEL

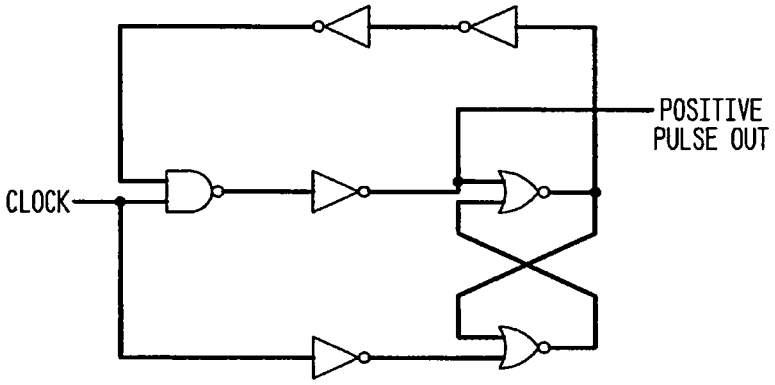


FIG. 257
POSITIVE PULSER AT TRANSISTOR LEVEL

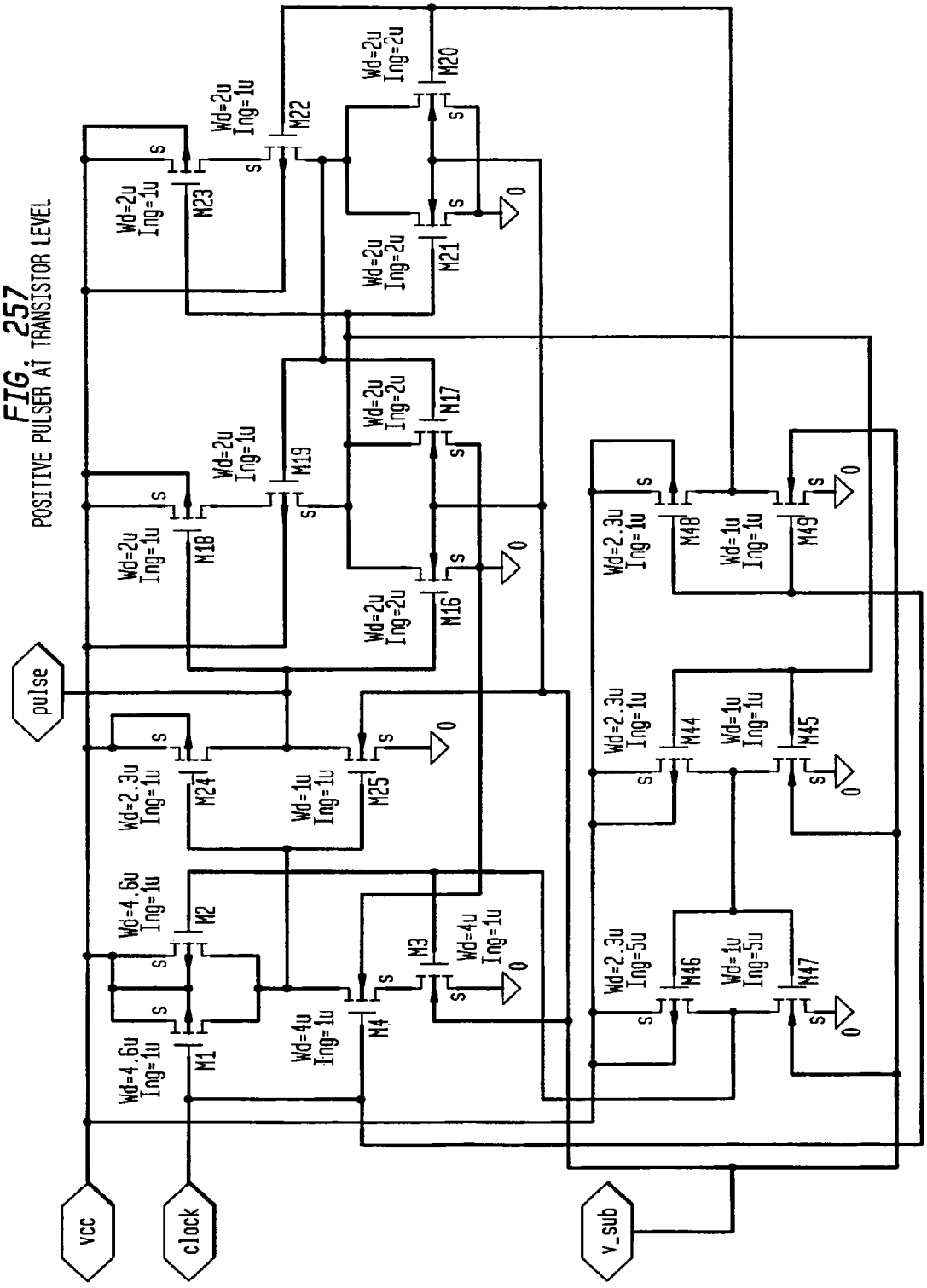
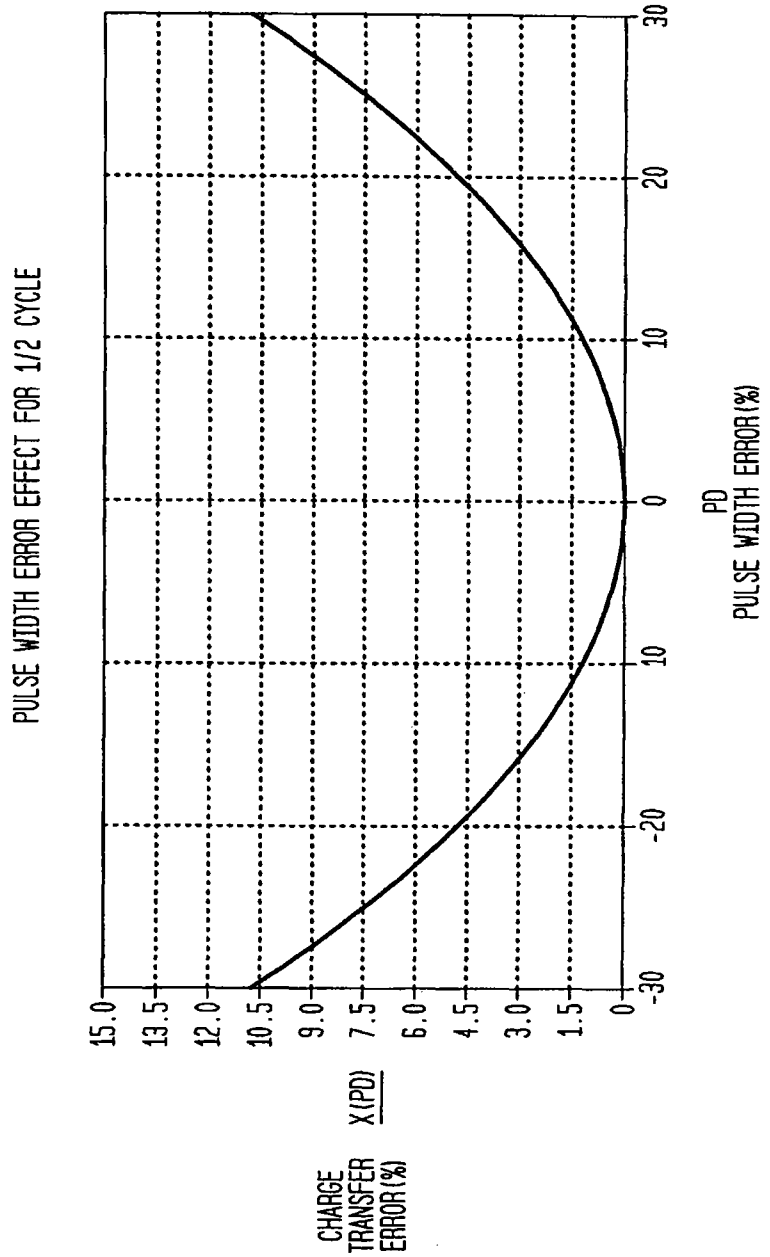


FIG. 25B


PULSE WIDTH ERROR EFFECT FOR 1/2 CYCLE
CHARGE TRANSFER ERROR(%)
X(PD)
15.0
13.5
12.0
10.5
9.0
7.5
6.0
4.5
3.0
1.5
0
-30
-20
-10
0
10
20
30
PD
PULSE WIDTH ERROR(%)

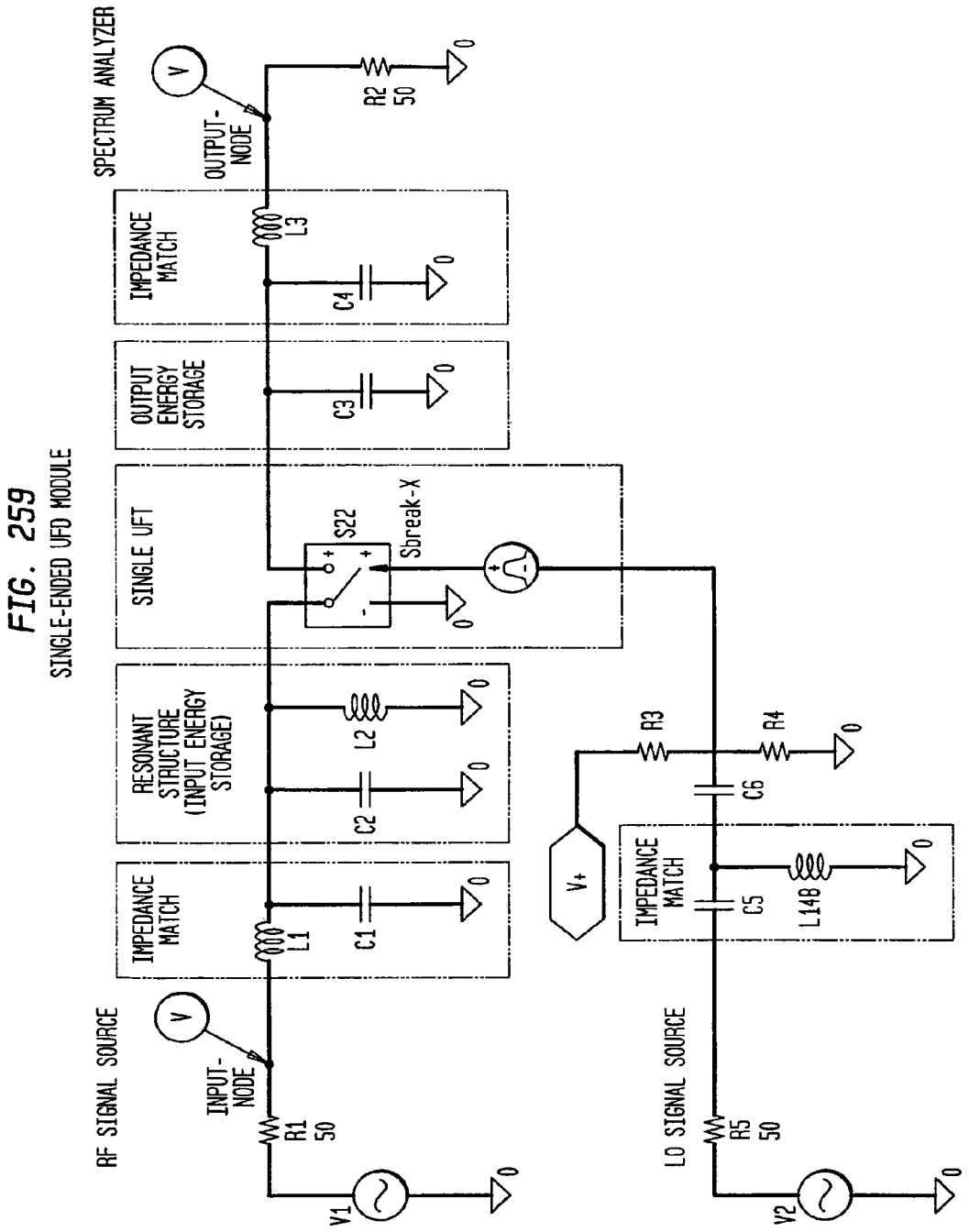
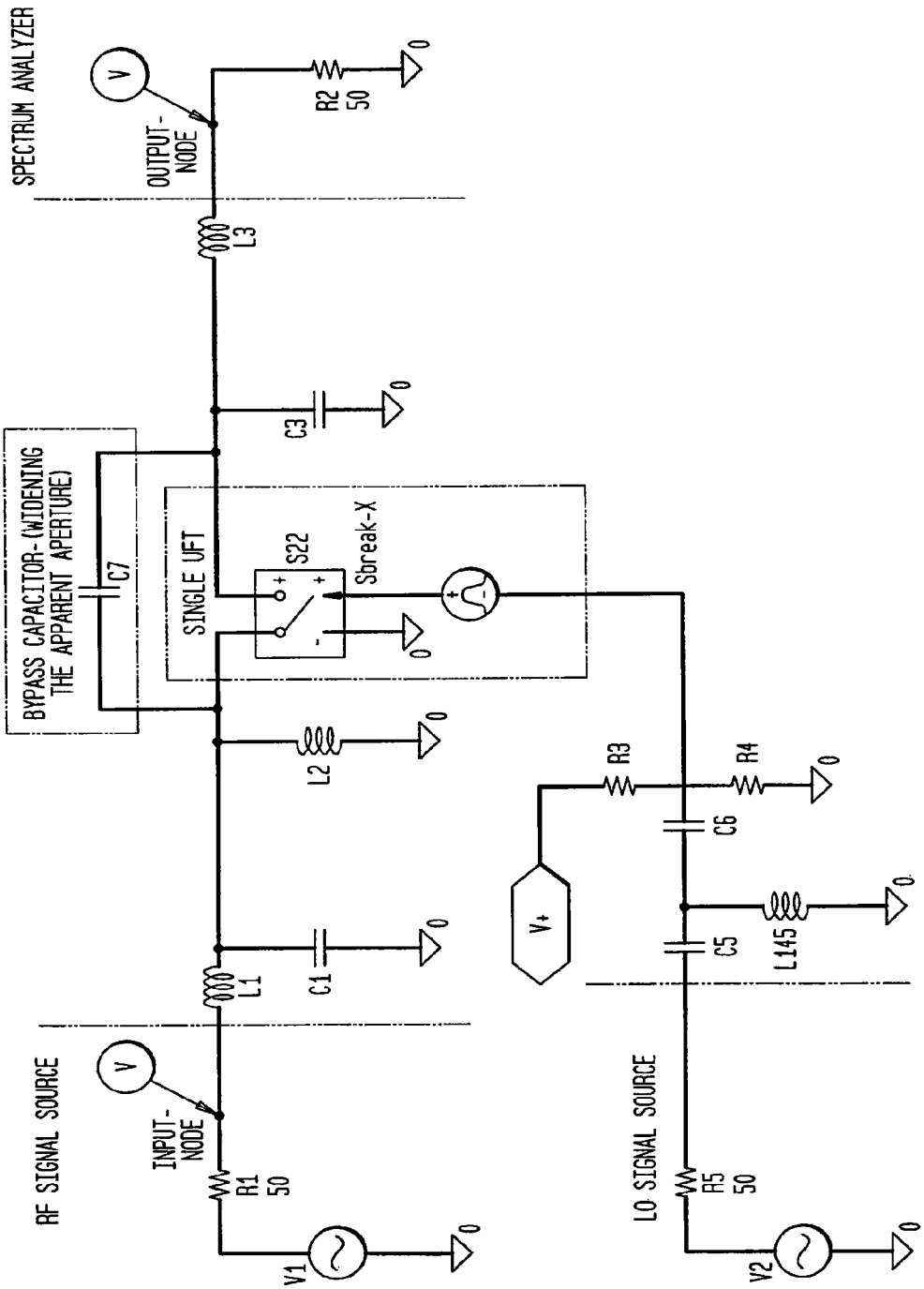

SINGLE-ENDED UFD MODULE
SPECTRUM ANALYZER
OUTPUT-NODE
R2 50
IMPEDANCE MATCH
L3
C4
OUTPUT ENERGY STORAGE
C3
SINGLE UFT
S22
Sbreak-X
RESONANT STRUCTURE (INPUT ENERGY STORAGE)
L2
C2
IMPEDANCE MATCH
L1
C1
RF SIGNAL SOURCE
INPUT-NODE
R1 50
V1
R3
R4
C6
V+
IMPEDANCE MATCH
C5
L148
LO SIGNAL SOURCE
R5 50
V2

FIG. 259

FIG. 260
SINGLE-ENDED UFD MODULE



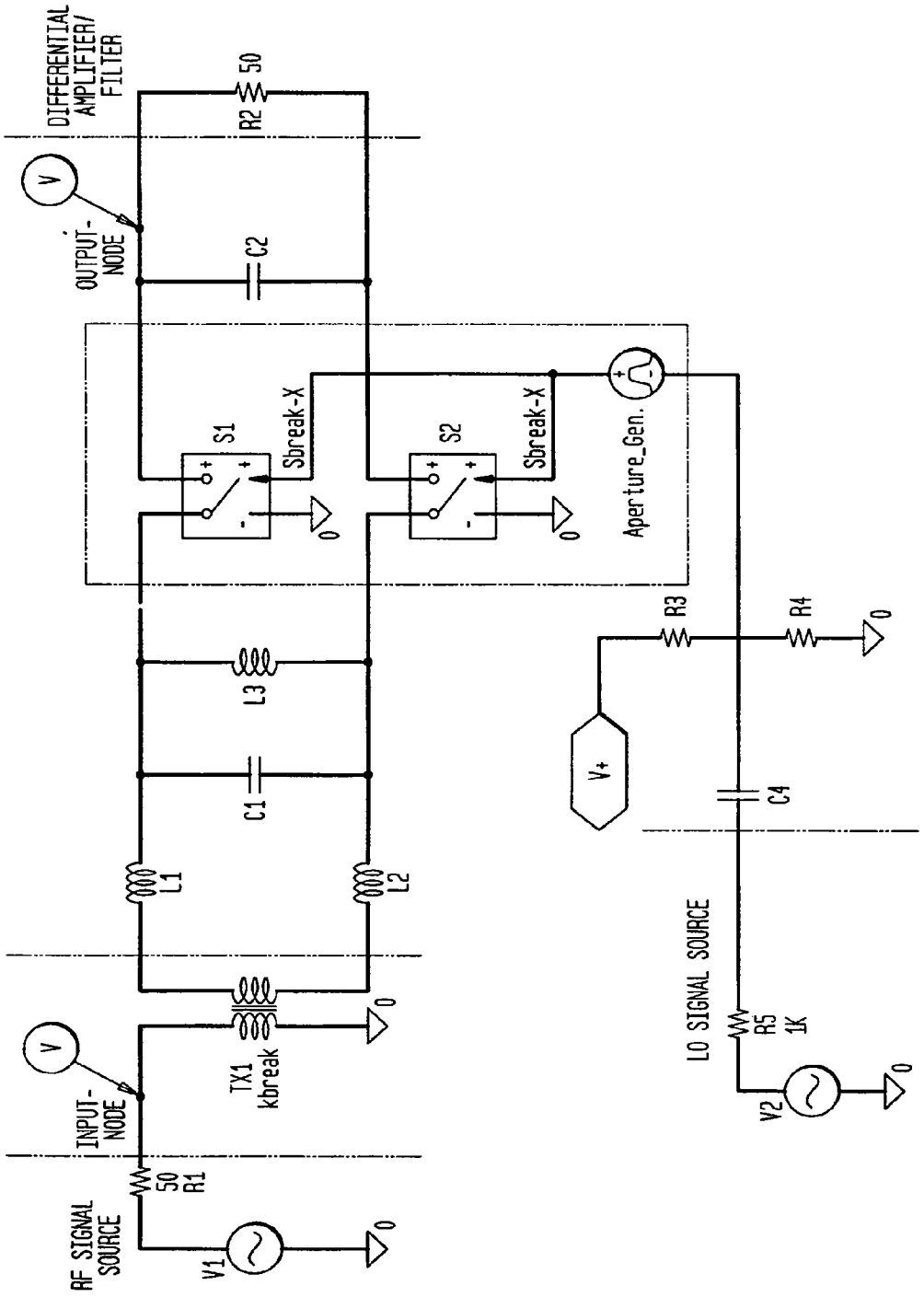


FIG. 261
FULL DIFFERENTIAL

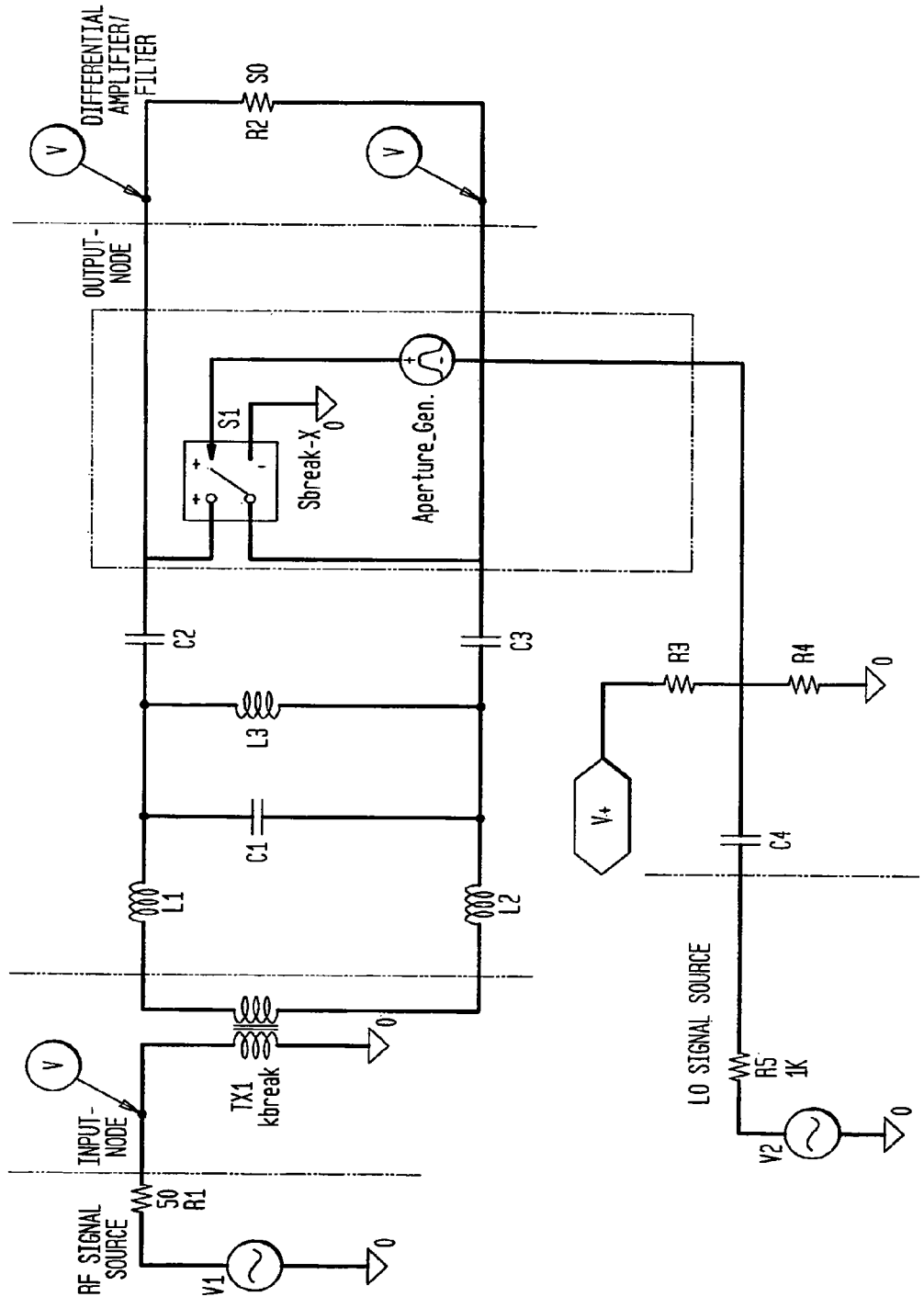


FIG. 262
FULL DIFFERENTIAL

FIG. 263

SINGLE-ENDED, NEAR IDEAL SIMULATION

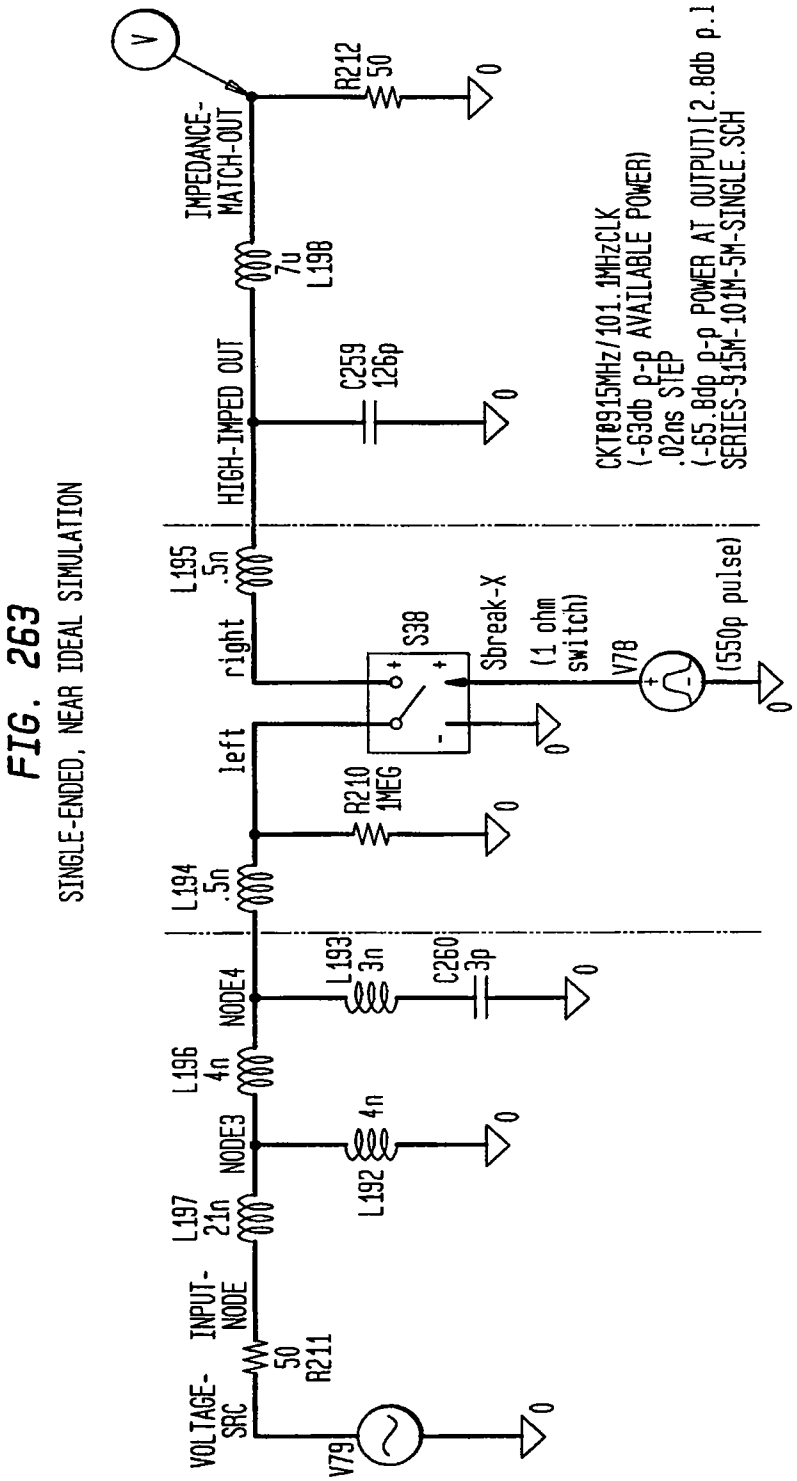


FIG. 264

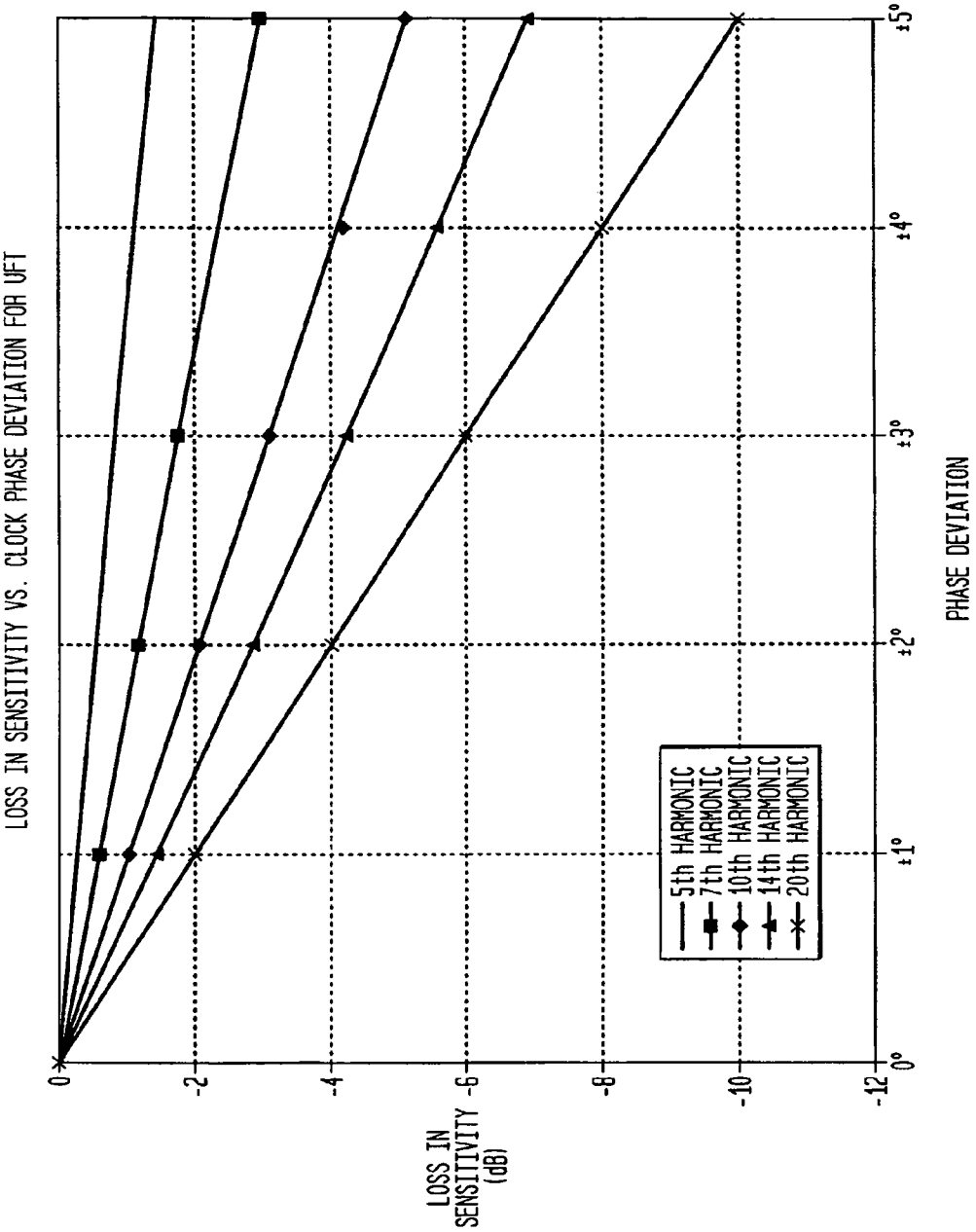
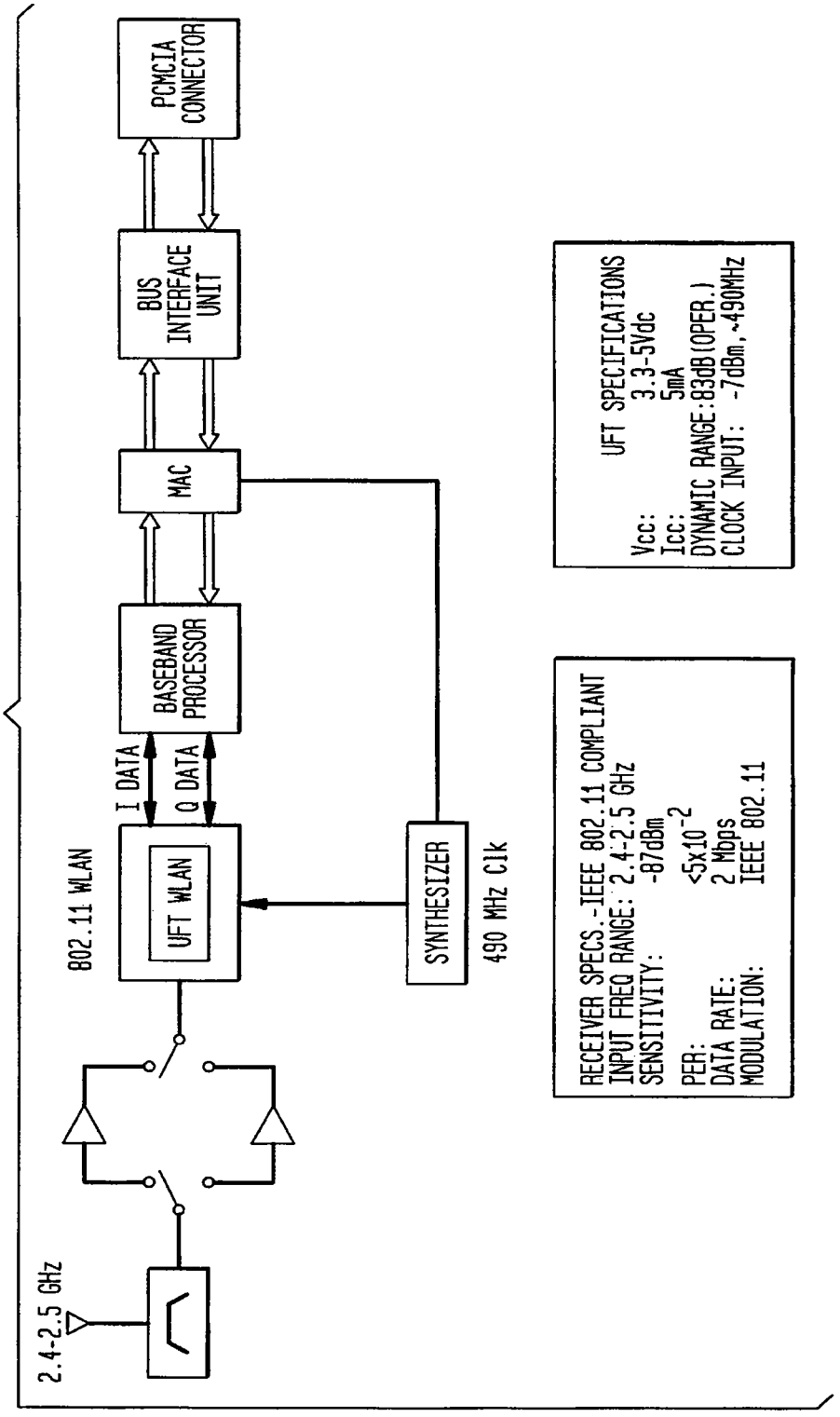

LOSS IN SENSITIVITY VS. CLOCK PHASE DEVIATION FOR UFT
LOSS IN SENSITIVITY (dB)
0
-2
-4
-6
-8
-10
-12
0°
±1°
±2°
±3°
±4°
±5°
PHASE DEVIATION
5th HARMONIC
7th HARMONIC
10th HARMONIC
14th HARMONIC
20th HARMONIC

FIG. 265


PCMCIA CONNECTOR
BUS INTERFACE UNIT
MAC
BASEBAND PROCESSOR
I DATA
Q DATA
802.11 WLAN
UFT WLAN
SYNTHESIZER
490 MHz Clk
2.4-2.5 GHz
UFT SPECIFICATIONS
3.3-5Vdc
5mA
DYNAMIC RANGE:83dB(OPER.)
CLOCK INPUT: -7dBm,~490MHz
RECEIVER SPECS.-IEEE 802.11 COMPLIANT
INPUT FREQ RANGE: 2.4-2.5 GHz
SENSITIVITY: -87dBm
PER: $<5x10^{-2}$
DATA RATE: 2 Mbps
MODULATION: IEEE 802.11

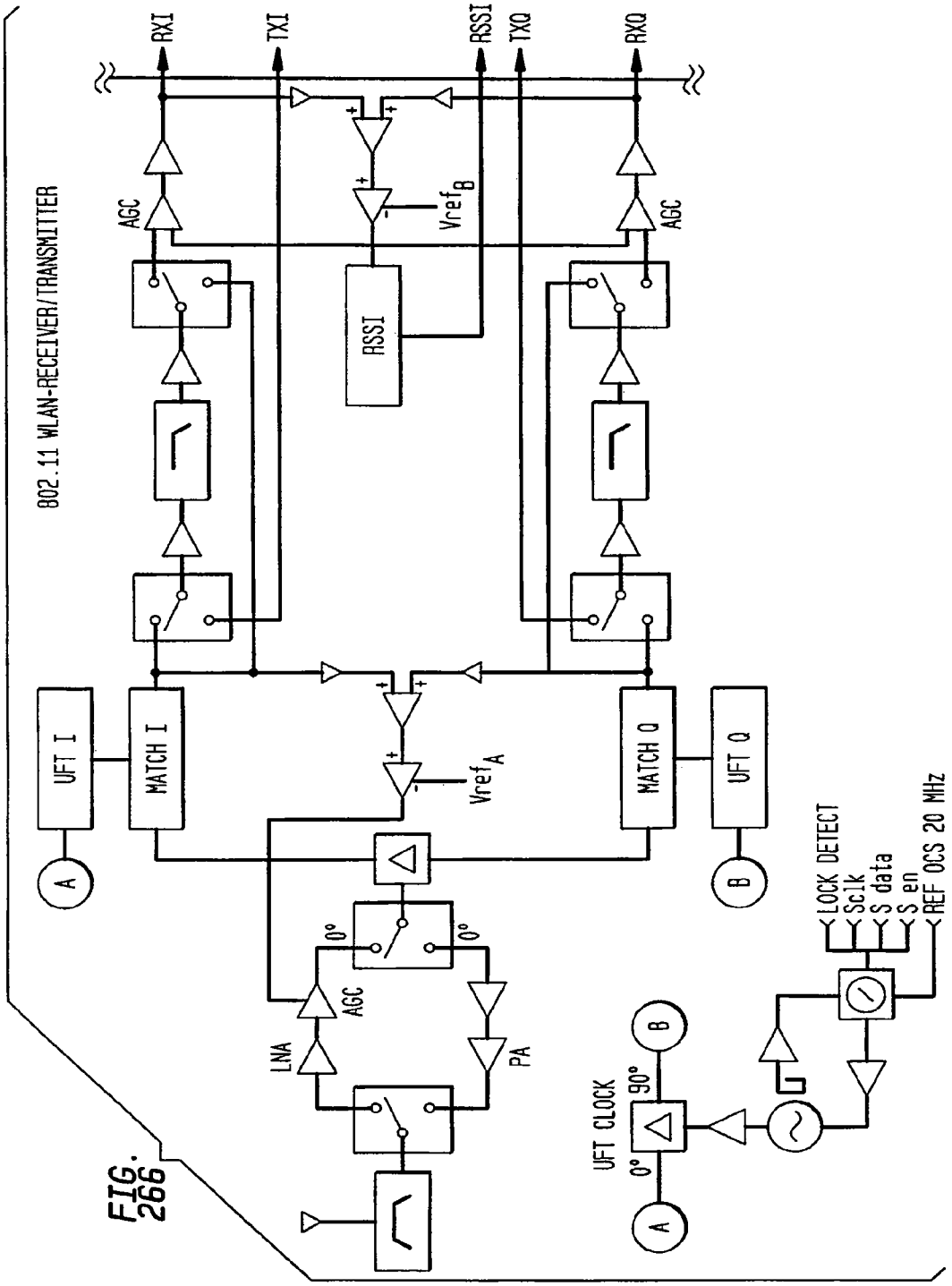

802.11 WLAN-RECEIVER/TRANSMITTER
RXI
TXI
RSSI
TXQ
RXQ
AGC
AGC
Vref B
RSSI
UFT I
MATCH I
Vref A
MATCH Q
UFT Q
A
B
0°
0°
AGC
LNA
PA
LOCK DETECT
Sclk
S data
S en
REF OCS 20 MHz
UFT CLOCK
90°
0°
B
A

FIG. 266

FIG. 267

PARAMETER	802.11 REQUIREMENT OR INDUSTRY PRACTICE	UFT MODULE BASED RX PERFORMANCE
OPERATING BAND	2.4-2.5 GHz	2.4-2.5 GHz
CHANNELS	2.402 TO 2.495 IN 1 MHz STEPS 2.412 TO 2.484 GHz IN 5 MHz STEPS	2.402 TO 2.495 IN 1 MHz STEPS 2.412 TO 2.484 GHz IN 5 MHz STEPS
MODULATION	BPSK,QPSK,(BARKER,CCK)	BPSK,QPSK
TX SPECTRAL MASK	FIRST SIDELOBE REJECT<-30,+15dBm SECOND SIDELOBE REJECT<-50,+15dBm	-35 dBr,-55dBr
EYE OPENING	Verr<.35 FOR 1000 COMPLEX SAMPLES	<.3
OPERATIONAL DYNAMIC RANGE	76 dB (DERIVED)	83 dB
MAX. INPUT, @, 8% PER	-4 dBm	-4 dBm
SENSITIVITY	-80 dBm @ <8% PER	-87 dBm @ <5% PER
ACQUISITION	802.11 DSS AND FH	802.11 DSS AND FH
IMAGE REJECTION	>80 dB	>80 dB
LO RERADIATION	< -50 dBm	< -50 dBm
ADJACENT CHANNEL REJECTION	> 35 dB @ 30 MHz OFFSET PER <8%	> 35 dB @ 30 MHz OFFSET PER <5%
POWER	3.3,5V 1.5W (RX MODE)	3.3,5V,700mW

FIG. 268

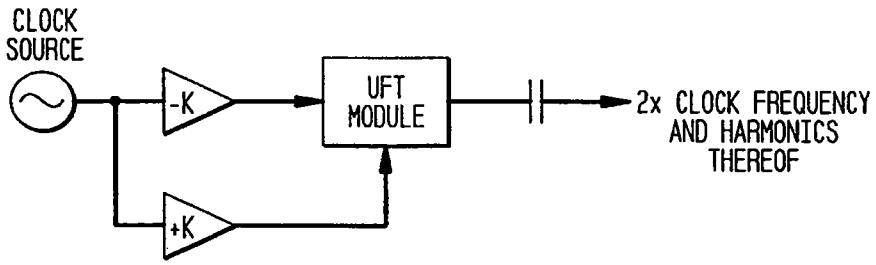


FIG. 269

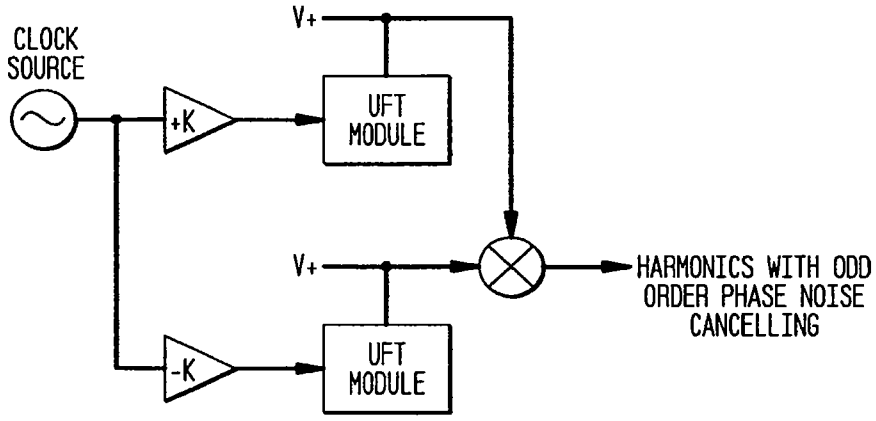


FIG. 270

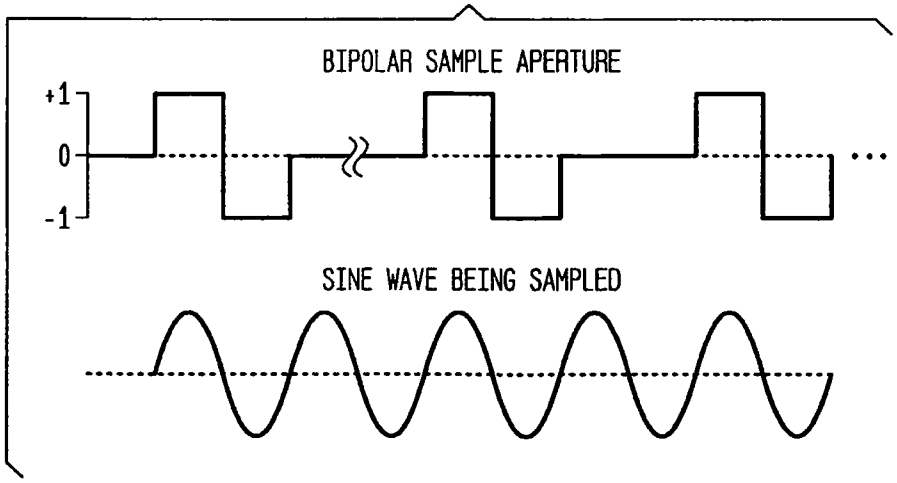


FIG. 271

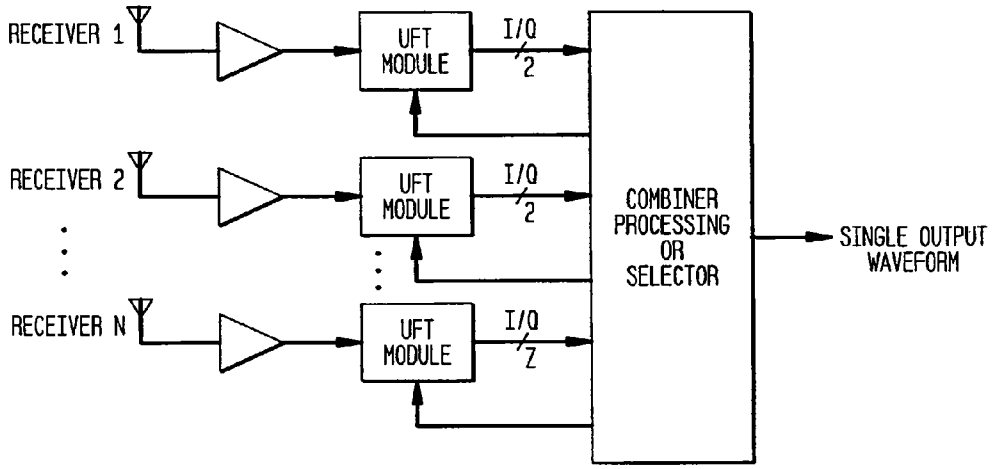


FIG. 272

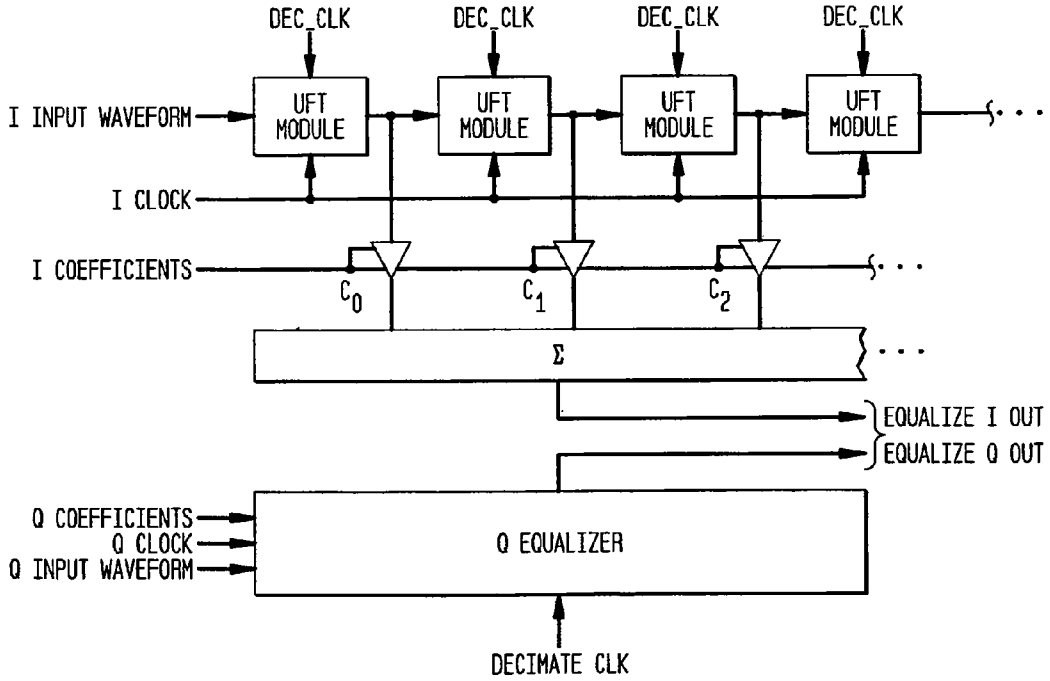


FIG. 273

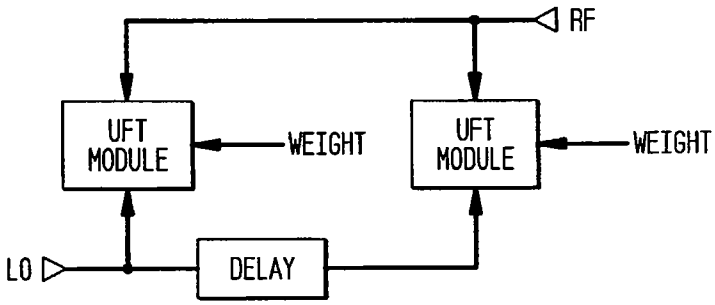


FIG. 274

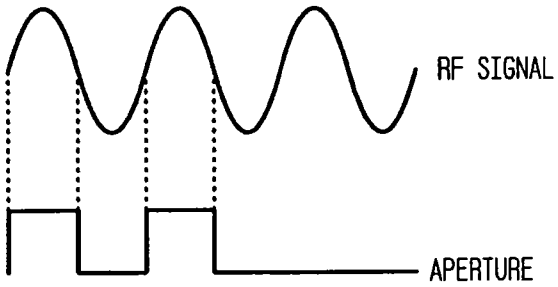


FIG. 275

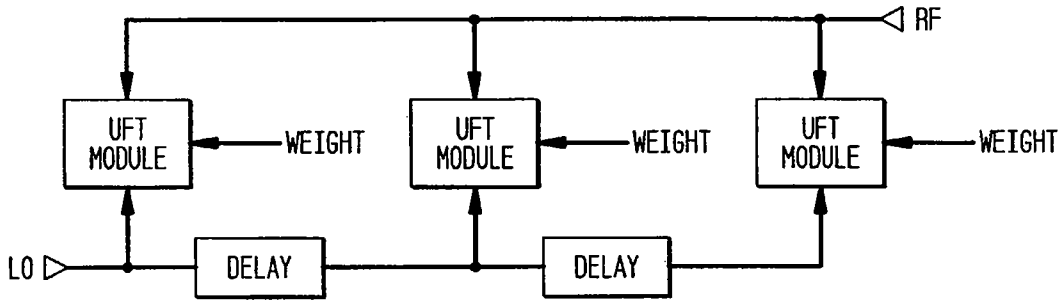


FIG. 276

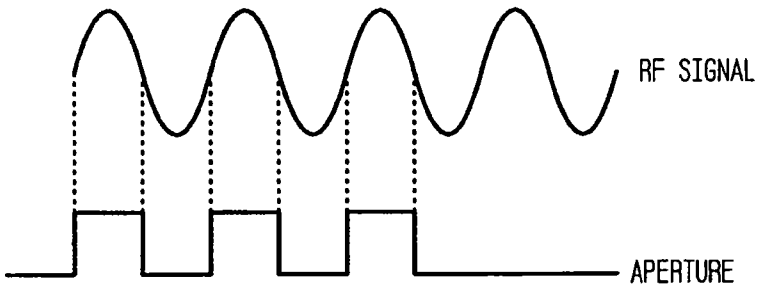


FIG. 277

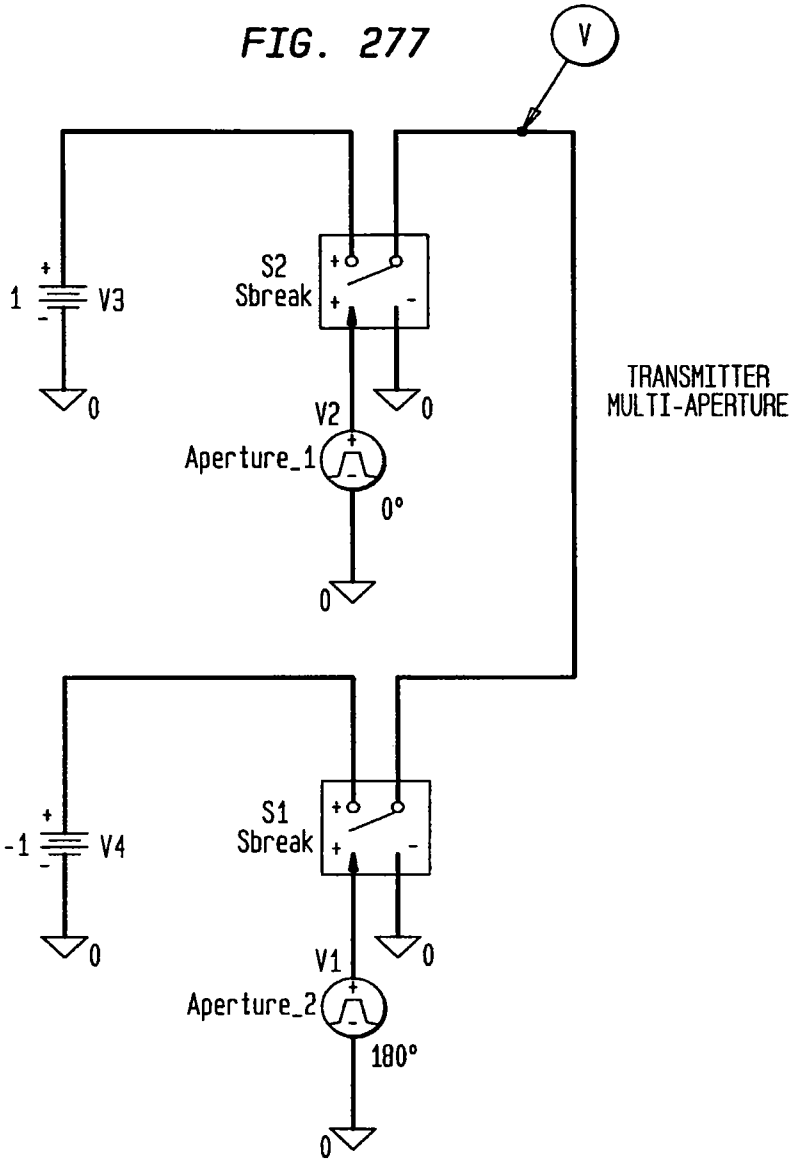

V
1
V3
0
S2
Sbreak
V2
0
Aperture_1
0°
0
TRANSMITTER
MULTI-APERTURE
-1
V4
0
S1
Sbreak
V1
0
Aperture_2
180°
0

FIG. 278

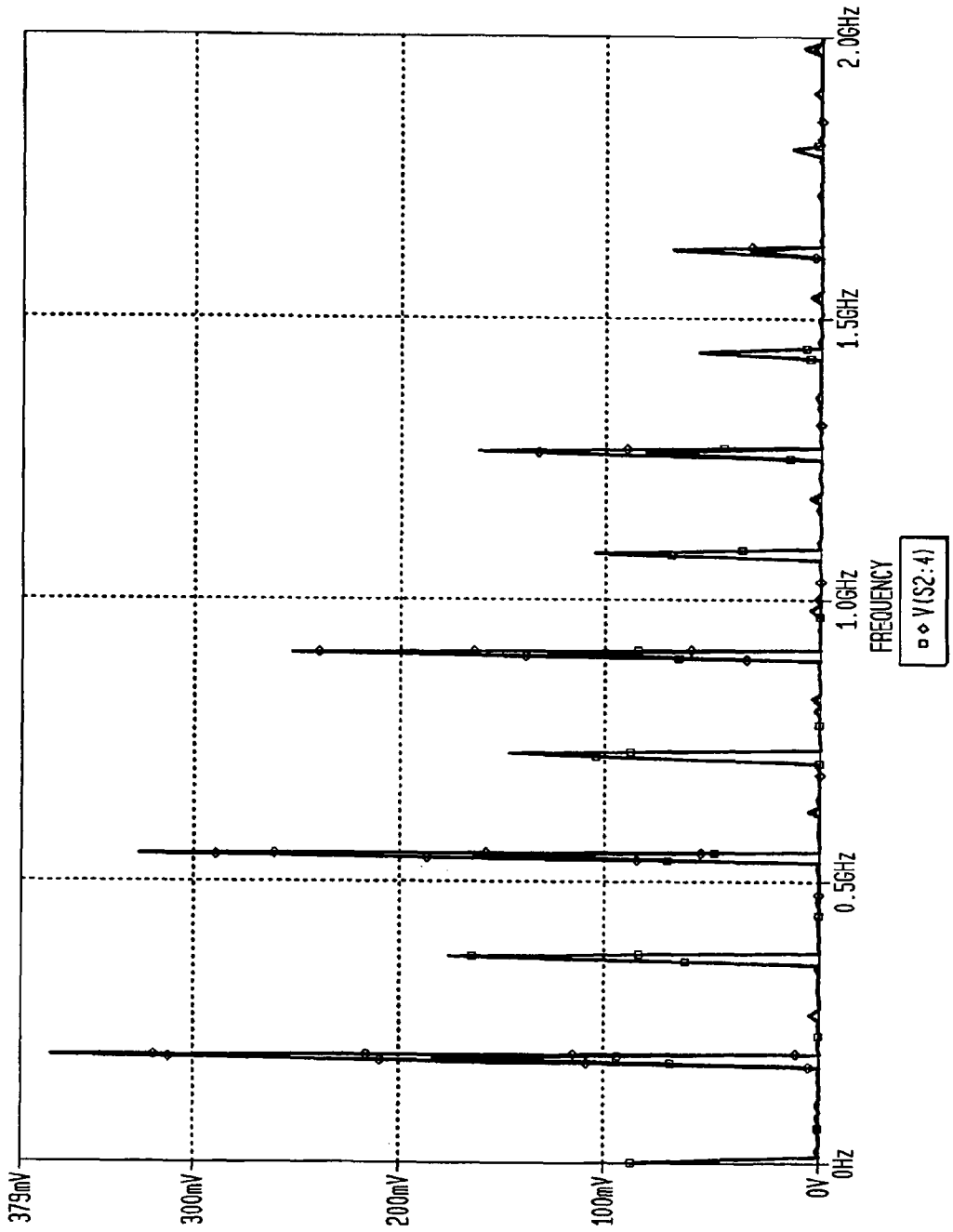
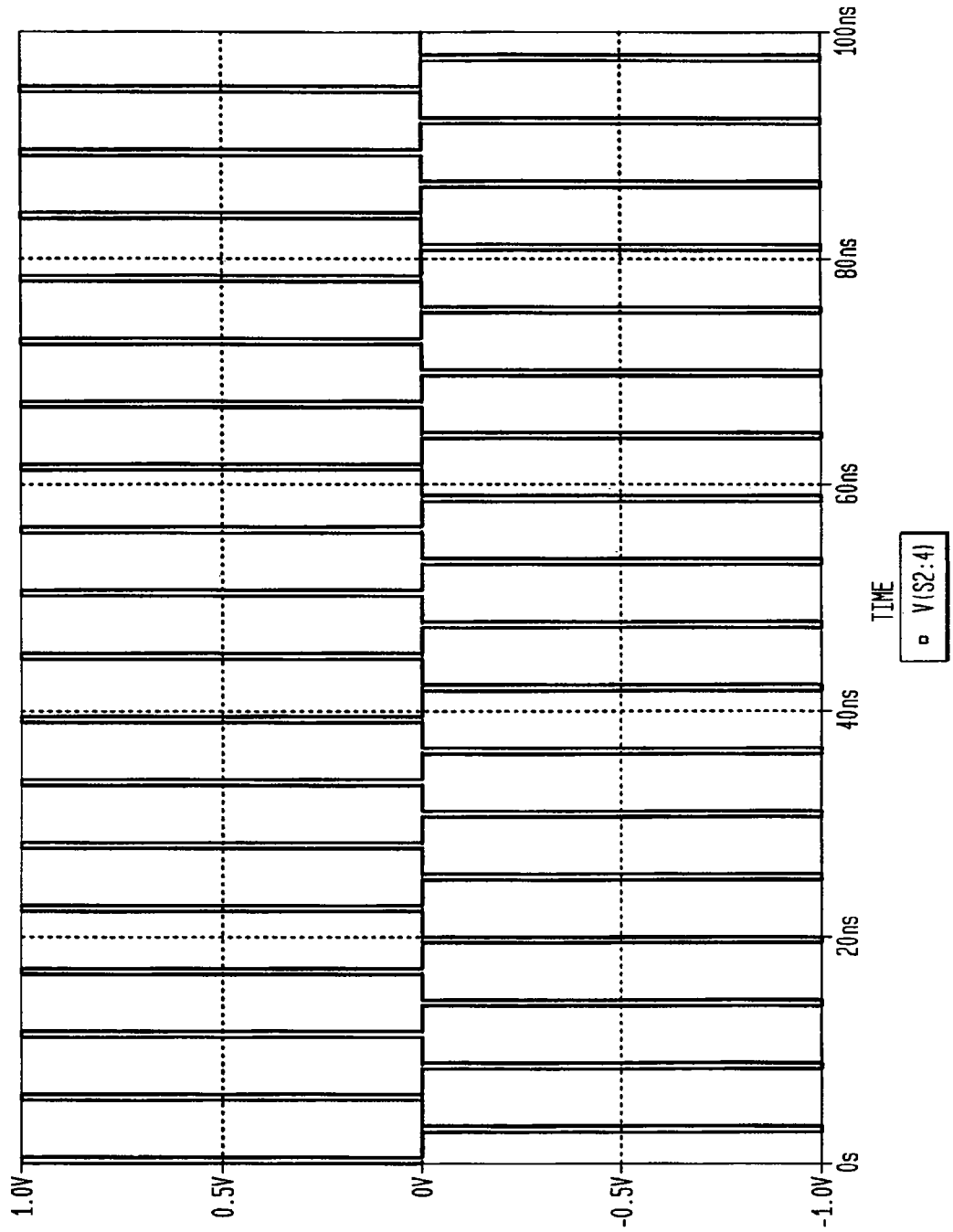

379mV
300mV
200mV
100mV
0V
0Hz
0.5GHz
1.0GHz
1.5GHz
2.0GHz
FREQUENCY
V(S2:4)

FIG. 279



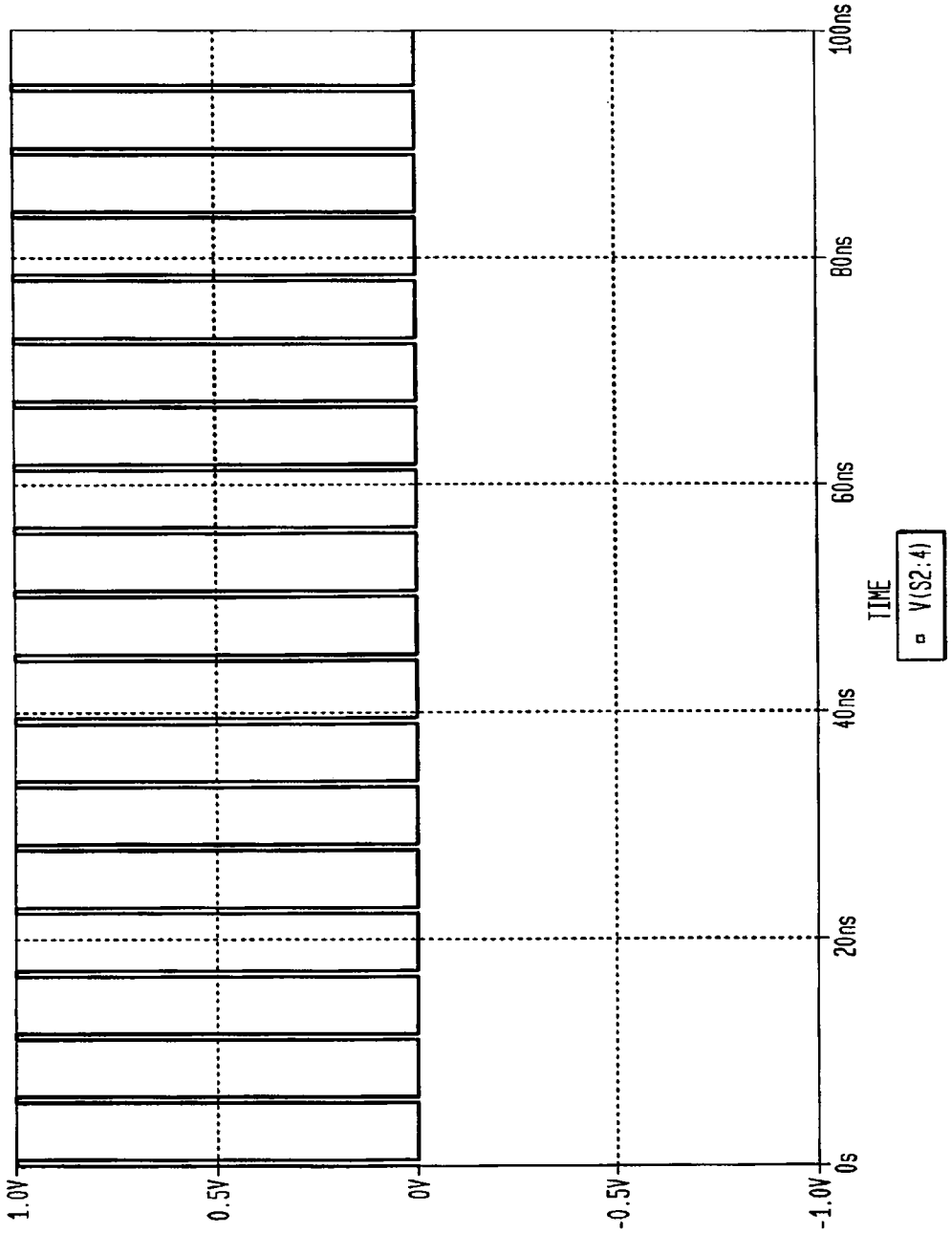
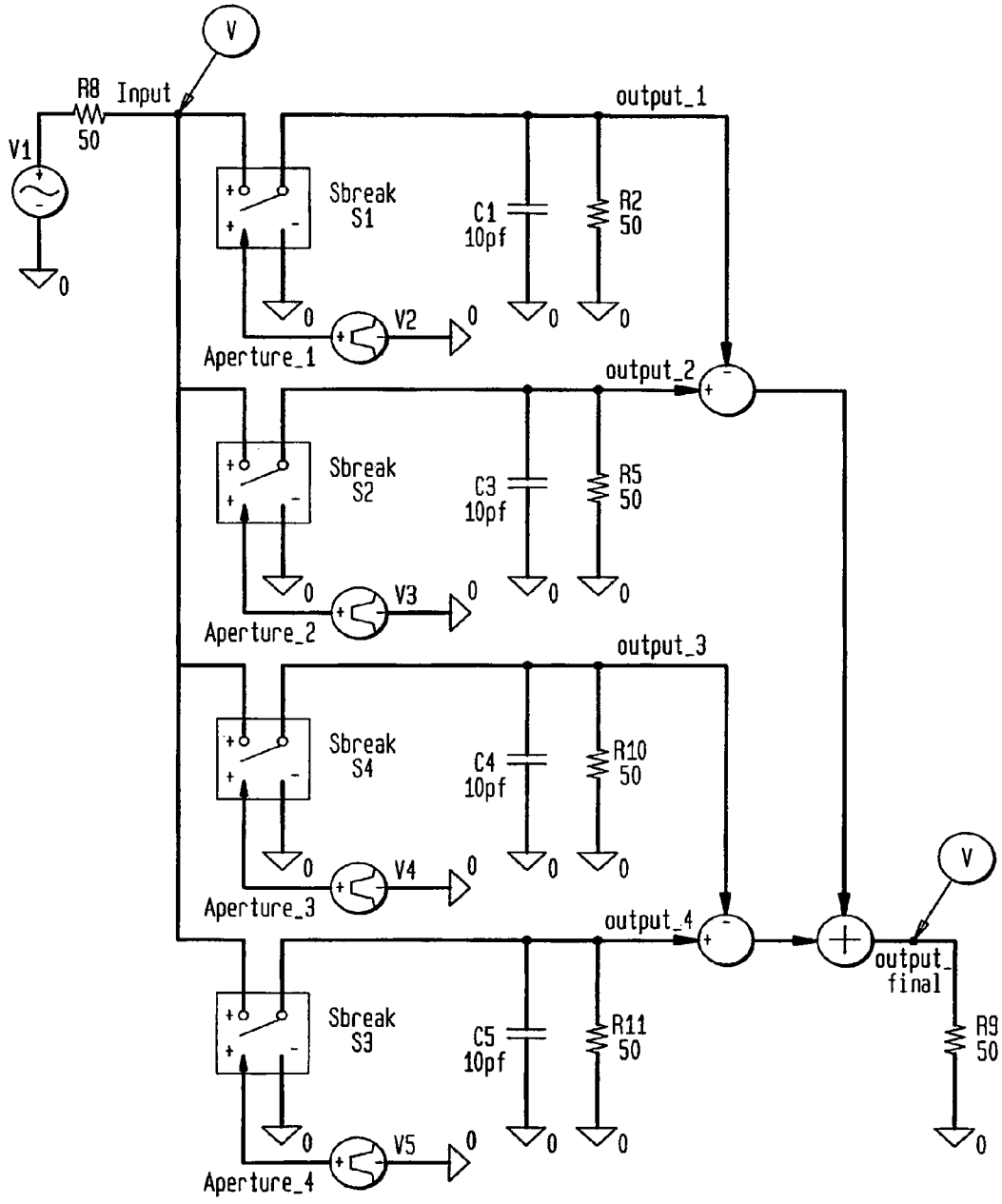


FIG. 280

FIG. 281

MULTIPLE APERTURE RECEIVER IMPLEMENTATION



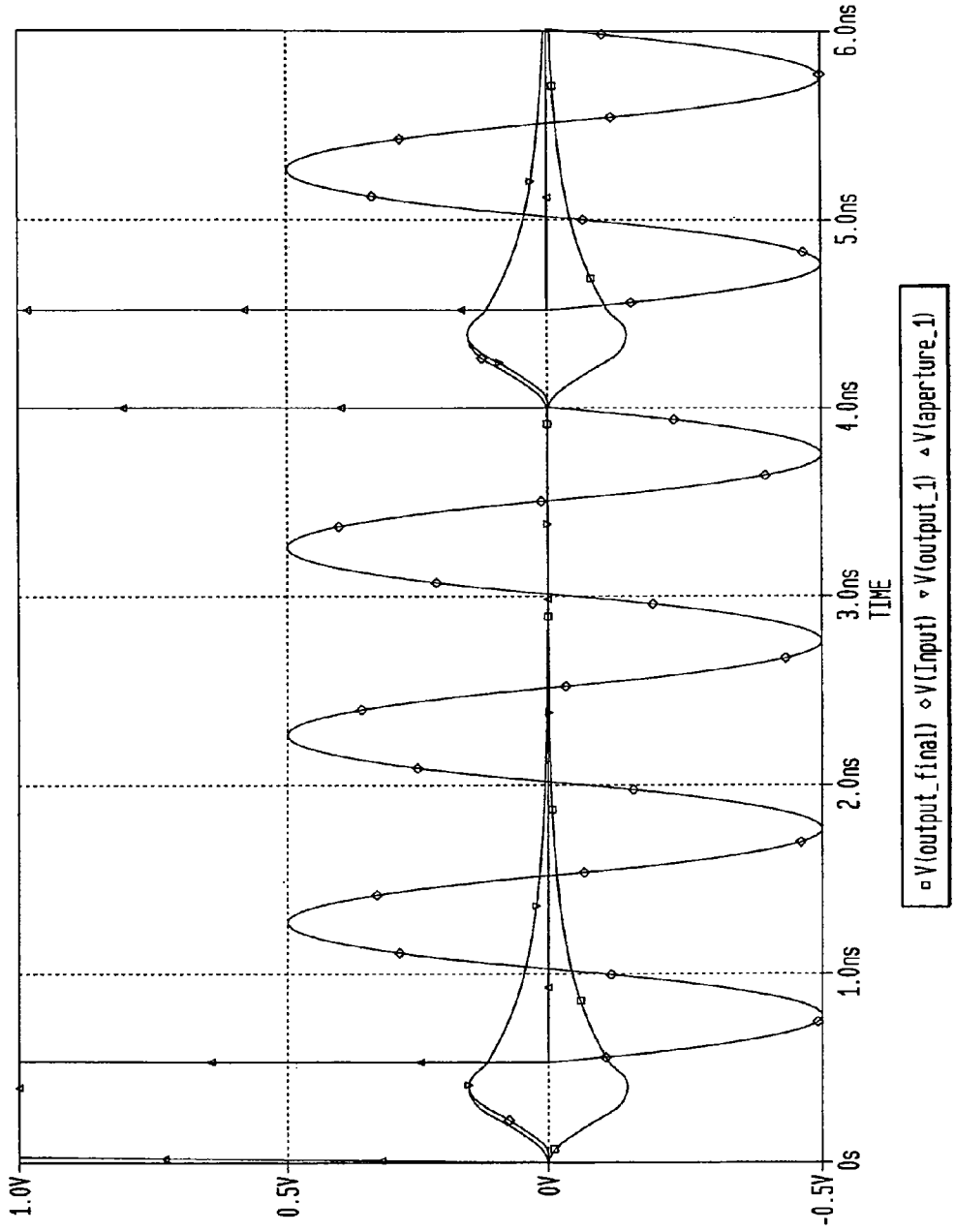

SINGLE APERTURE
1.0V
0.5V
0V
-0.5V
0s
1.0ns
2.0ns
3.0ns
4.0ns
5.0ns
6.0ns
TIME
V(output_final)
V(Input)
V(output_1)
V(aperture_1)

FIG. 282

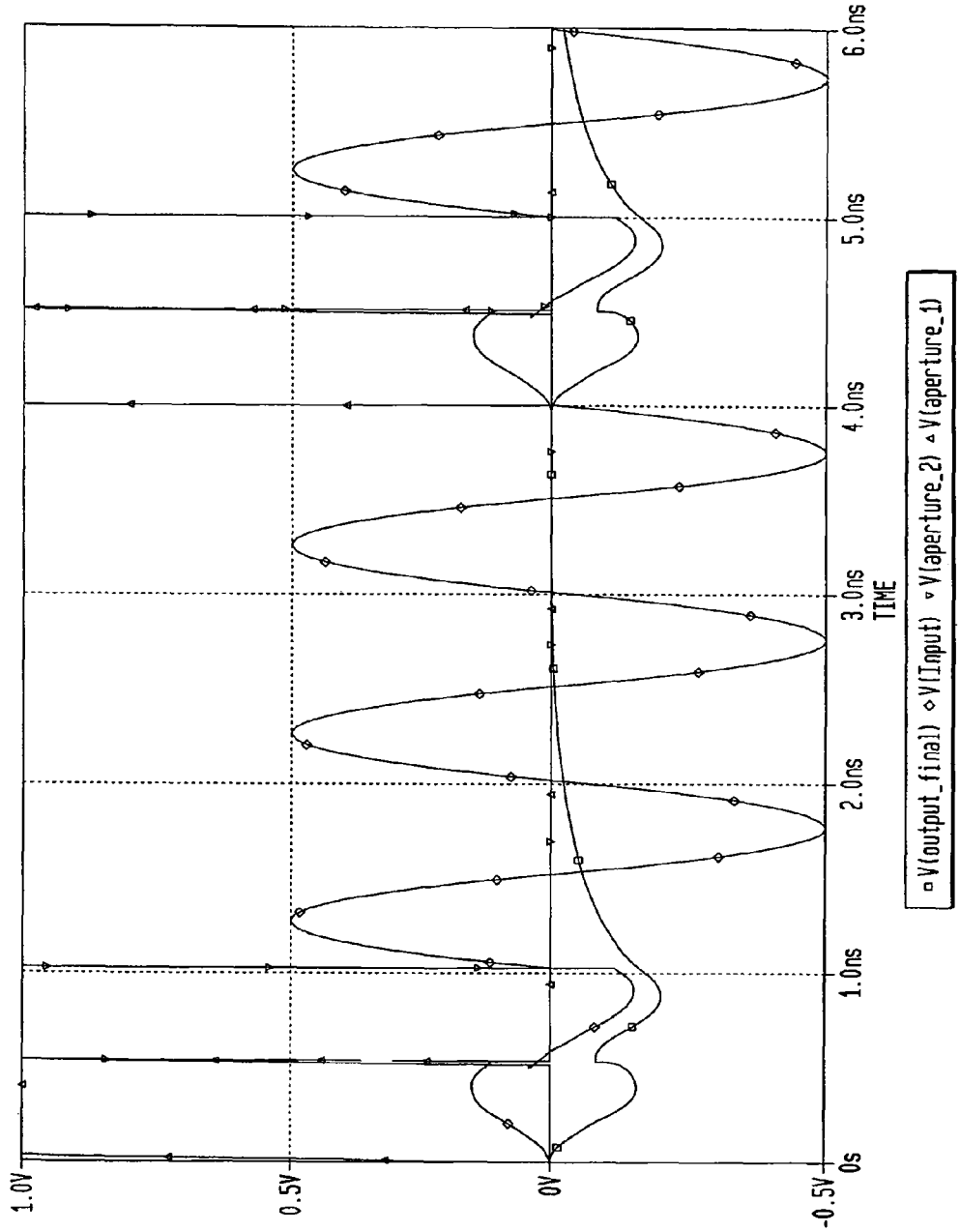

DUAL APERTURE
1.0V
0.5V
0V
-0.5V
0s
1.0ns
2.0ns
3.0ns
4.0ns
5.0ns
6.0ns
TIME
V(output_final)
V(Input)
V(aperture_2)
V(aperture_1)

FIG. 283

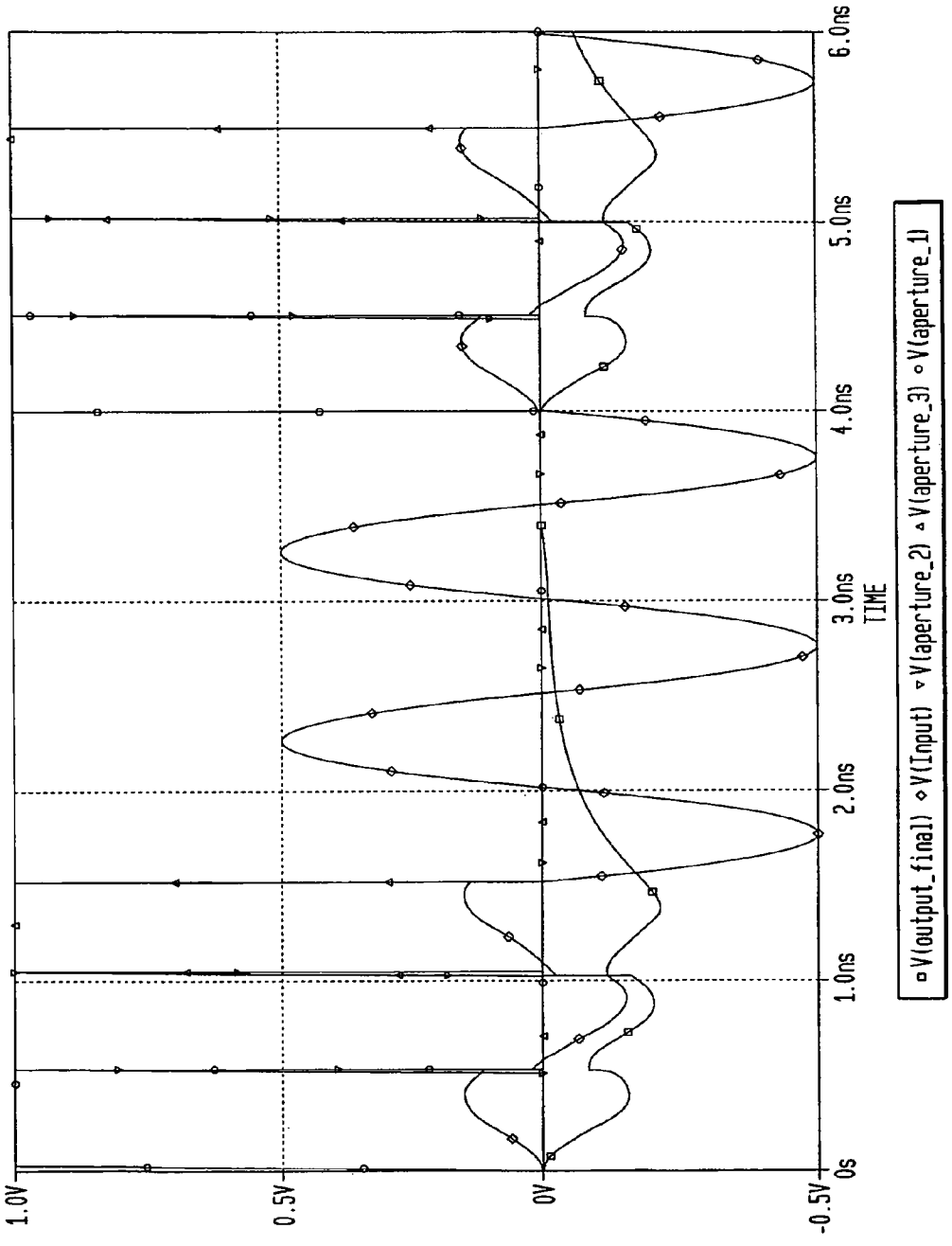

TRIPLE APERTURE
1.0V
0.5V
0V
-0.5V
0s
1.0ns
2.0ns
3.0ns
4.0ns
5.0ns
6.0ns
TIME
V(output_final)
V(Input)
V(aperture_2)
V(aperture_3)
V(aperture_1)

FIG. 284

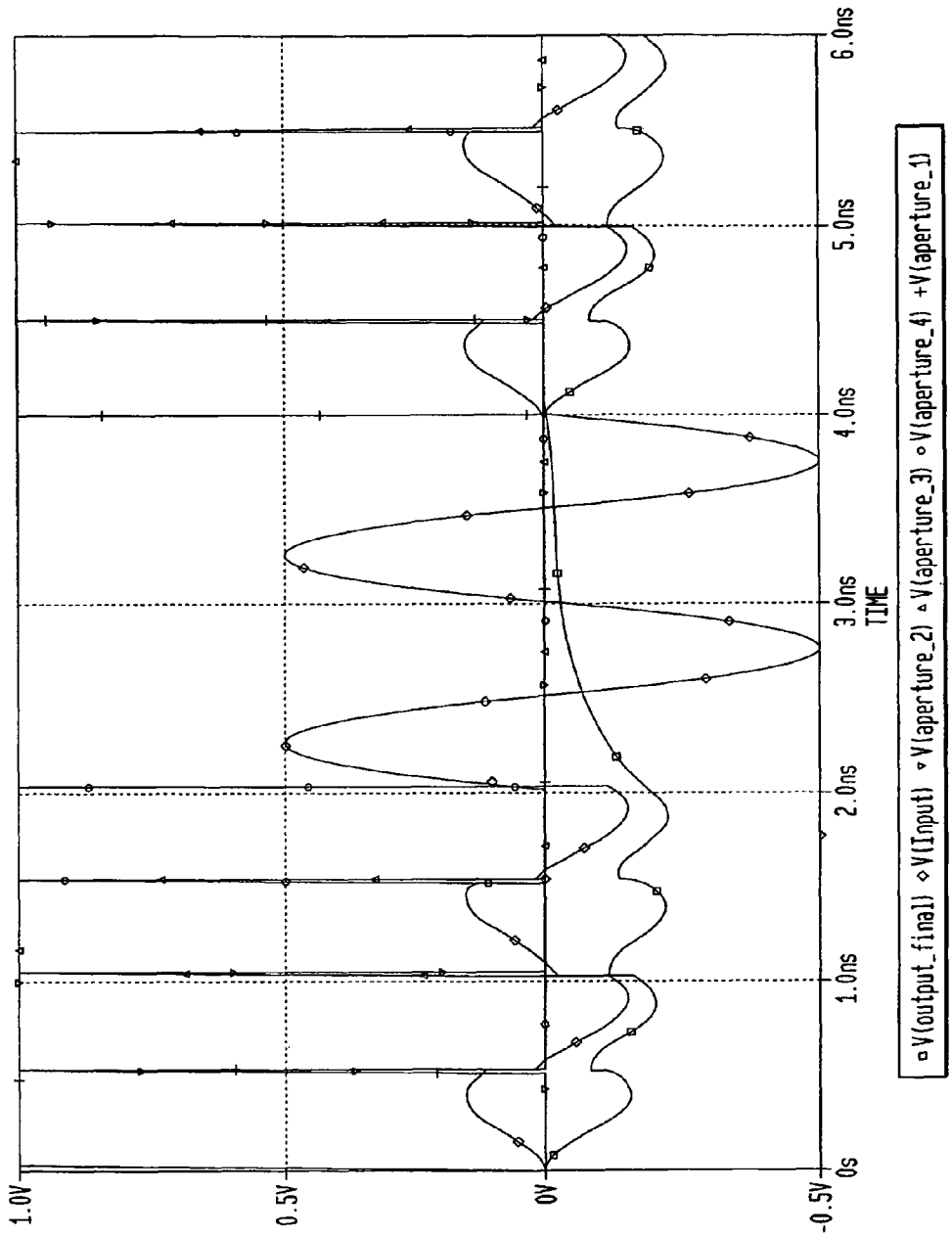

QUAD APERTURE
1.0V
0.5V
0V
-0.5V
0s
1.0ns
2.0ns
3.0ns
4.0ns
5.0ns
6.0ns
TIME
V(output_final) V(Input) V(aperture_2) V(aperture_3) V(aperture_4) +V(aperture_1)

FIG. 285

METHOD AND SYSTEM FOR DOWN-CONVERTING AN ELECTROMAGNETIC SIGNAL, AND TRANSFORMS FOR SAME, AND APERTURE RELATIONSHIPS

CROSS-REFERENCE TO OTHER APPLICATIONS

The present application is a continuation of pending U.S. application "Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same, and Aperture Relationships", Ser. No. 13/549,213, filed Jul. 13, 2012, which is a continuation of "Method and System for Down-Converting an Electromagnetic Signal and Transforms for the Same, and Aperture Relationships", Ser. No. 12/976,839, filed Dec. 22, 2010, which is a continuation of U.S. application "Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same, and Aperture Relationships," Ser. No. 12/349,802, filed Jan. 7, 2009 (now U.S. Pat. No. 7,865,177), which is a divisional application of U.S. application "Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same, and Aperture Relationships," Ser. No. 09/550,644, filed Apr. 14, 2000 (now U.S. Pat. No. 7,515,896), which is a continuation-in-part application of U.S. application "Method and System for Down-Converting an Electromagnetic Signal Including Resonant Structures for Enhanced Energy Transfer," Ser. No. 09/293,342, filed Apr. 16, 1999 (now U.S. Pat. No. 6,687,493), which is a continuation-in-part application of U.S. application "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed Oct. 21, 1998 (now U.S. Pat. No. 6,061,551), each of which is herein incorporated by reference in their entireties.

The following applications of common assignee are related to the present application, and are herein incorporated by reference in their entireties:

"Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed Oct. 21, 1998 (now U.S. Pat. No. 6,091,940);

"Method and System for Ensuring Reception of a Communications Signal," Ser. No. 09/176,415, filed Oct. 21, 1998 (now U.S. Pat. No. 6,061,555);

"Integrated Frequency Translation and Selectivity," Ser. No. 09/175,966, filed Oct. 21, 1998 (now U.S. Pat. No. 6,049,706);

"Universal Frequency Translation, and Applications of Same," Ser. No. 09/176,027, filed Oct. 21, 1998 (now abandoned);

"Method and System for Down-Converting Electromagnetic Signals Having Optimized Switch Structures," Ser. No. 09/293,095, filed Apr. 16, 1999 (now U.S. Pat. No. 6,580,902);

"Method and System for Frequency Up-Conversion with a Variety of Transmitter Configurations," Ser. No. 09/293,580, filed Apr. 16, 1999 (U.S. Pat. No. 6,542,722); and

"Integrated Frequency Translation and Selectivity with a Variety of Filter Embodiments," Ser. No. 09/293,283, filed Apr. 16, 1999 (now U.S. Pat. No. 6,560,301).

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to down-conversion of electromagnetic (EM) signals. More particularly, the present invention relates to down-conversion of EM signals to intermediate frequency signals, to direct down-conversion of EM modulated carrier signals to demodulated baseband signals, and to conversion of FM signals to non-FM signals. The present invention also relates to under-sampling and to transferring energy at aliasing rates.

2. Related Art

Electromagnetic (EM) information signals (baseband signals) include, but are not limited to, video baseband signals, voice baseband signals, computer baseband signals, etc. Baseband signals include analog baseband signals and digital baseband signals.

It is often beneficial to propagate EM signals at higher frequencies. This is generally true regardless of whether the propagation medium is wire, optic fiber, space, air, liquid, etc. To enhance efficiency and practicality, such as improved ability to radiate and added ability for multiple channels of baseband signals, up-conversion to a higher frequency is utilized. Conventional up-conversion processes modulate higher frequency carrier signals with baseband signals. Modulation refers to a variety of techniques for impressing information from the baseband signals onto the higher frequency carrier signals. The resultant signals are referred to herein as modulated carrier signals. For example, the amplitude of an AM carrier signal varies in relation to changes in the baseband signal, the frequency of an FM carrier signal varies in relation to changes in the baseband signal, and the phase of a PM carrier signal varies in relation to changes in the baseband signal.

In order to process the information that was in the baseband signal, the information must be extracted, or demodulated, from the modulated carrier signal. However, because conventional signal processing technology is limited in operational speed, conventional signal processing technology cannot easily demodulate a baseband signal from higher frequency modulated carrier signal directly. Instead, higher frequency modulated carrier signals must be down-converted to an intermediate frequency (IF), from where a conventional demodulator can demodulate the baseband signal.

Conventional down-converters include electrical components whose properties are frequency dependent. As a result, conventional down-converters are designed around specific frequencies or frequency ranges and do not work well outside their designed frequency range.

Conventional down-converters generate unwanted Image signals and thus must include filters for filtering the unwanted image signals. However, such filters reduce the power level of the modulated carrier signals. As a result, conventional down-converters include power amplifiers, which require external energy sources.

When a received modulated carrier signal is relatively weak, as in, for example, a radio receiver, conventional down-converters include additional power amplifiers, which require additional external energy.

What is needed includes, without limitation:

an improved method and system for down-converting EM signals;

a method and system for directly down-converting modulated carrier signals to demodulated baseband signals;

a method and system for transferring energy and for augmenting such energy transfer when down-converting EM signals;

a controlled impedance method and system for down-converting an EM signal;

a controlled aperture under-sampling method and system for down-converting an EM signal;

a method and system for down-converting EM signals using a universal down-converter design that can be easily configured for different frequencies;

a method and system for down-converting EM signals using a local oscillator frequency that is substantially lower than the carrier frequency;

a method and system for down-converting EM signals using only one local oscillator;

a method and system for down-converting EM signals that uses fewer filters than conventional down-converters;

a method and system for down-converting EM signals using less power than conventional down-converters;

a method and system for down-converting EM signals that uses less space than conventional down-converters;

a method and system for down-converting EM signals that uses fewer components than conventional down-converters;

a method and system for down-converting EM signals that can be implemented on an integrated circuit (IC); and

a method and system for down-converting EM signals that can also be used as a method and system for up-converting a baseband signal.

SUMMARY OF THE INVENTION

Briefly stated, the present invention is directed to methods, systems, and apparatuses for down-converting an electromagnetic (EM), and applications thereof.

Generally, in an embodiment, the invention operates by receiving an EM signal and recursively operating on approximate half cycles of a carrier signal. The recursive operations are typically performed at a sub-harmonic rate of the carrier signal. The invention accumulates the results of the recursive operations and uses the accumulated results to form a down-converted signal.

In an embodiment, the invention down-converts the EM signal to an intermediate frequency (IF) signal.

In another embodiment, the invention down-converts the EM signal to a demodulated baseband information signal.

In another embodiment, the EM signal is a frequency modulated (FM) signal, which is down-converted to a non-FM signal, such as a phase modulated (PM) signal or an amplitude modulated (AM) signal.

The invention is applicable to any type of EM signal, including but not limited to, modulated carrier signals (the invention is applicable to any modulation scheme or combination thereof) and unmodulated carrier signals.

Further features and advantages of the invention, as well as the structure and operation of various embodiments of the invention, are described in detail below with reference to the accompanying drawings. It is noted that the invention is not limited to the specific embodiments described herein. Such embodiments are presented herein for illustrative purposes only. Additional embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

BRIEF DESCRIPTION OF THE DRAWINGS

The drawing in which an element first appears is typically indicated by the leftmost digit(s) in the corresponding reference number.

The present invention will be described with reference to the accompanying drawings wherein:

FIG. **1** illustrates a structural block diagram of an example modulator;

FIG. **2** illustrates an example analog modulating baseband signal;

FIG. **3** illustrates an example digital modulating baseband signal;

FIG. **4** illustrates an example carrier signal;

FIGS. **5**A-**5**C illustrate example signal diagrams related to amplitude modulation;

FIGS. **6**A-**6**C illustrate example signal diagrams related to amplitude shift keying modulation;

FIGS. **7**A-**7**C illustrate example signal diagrams related to frequency modulation;

FIGS. **8**A-**8**C illustrate example signal diagrams related to frequency shift keying modulation;

FIGS. **9**A-**9**C illustrate example signal diagrams related to phase modulation;

FIGS. **10**A-**10**C illustrate example signal diagrams related to phase shift keying modulation;

FIG. **11** illustrates a structural block diagram of a conventional receiver;

FIG. **12**A-D illustrate various flowcharts for down-converting an EM-signal according to embodiments of the invention;

FIG. **13** illustrates a structural block diagram of an aliasing system according to an embodiment of the invention;

FIGS. **14**A-D illustrate various flowcharts for down-converting an EM signal by under-sampling the EM signal according to embodiments of the invention;

FIGS. **15**A-E illustrate example signal diagrams associated with flowcharts in FIGS. **14**A-D according to embodiments of the invention;

FIG. **16** illustrates a structural block diagram of an under-sampling system according to an embodiment of the invention;

FIG. **17** illustrates a flowchart of an example process for determining an aliasing rate according to an embodiment of the invention;

FIGS. **18**A-E illustrate example signal diagrams associated with down-converting a digital AM signal to an intermediate frequency signal by under-sampling according to embodiments of the invention;

FIGS. **19**A-E illustrate example signal diagrams associated with down-converting an analog AM signal to an intermediate frequency signal by under-sampling according to embodiments of the invention;

FIGS. **20**A-E illustrate example signal diagrams associated with down-converting an analog FM signal to an intermediate frequency signal by under-sampling according to embodiments of the invention;

FIGS. **21**A-E illustrate example signal diagrams associated with down-converting a digital FM signal to an intermediate frequency signal by under-sampling according to embodiments of the invention;

FIGS. **22**A-E illustrate example signal diagrams associated with down-converting a digital PM signal to an intermediate frequency signal by under-sampling according to embodiments of the invention;

FIGS. **23**A-E illustrate example signal diagrams associated with down-converting an analog PM signal to an intermediate frequency signal by under-sampling according to embodiments of the invention;

FIG. **24**A illustrates a structural block diagram of a make before break under-sampling system according to an embodiment of the invention;

FIG. **24**B illustrates an example timing diagram of an under sampling signal according to an embodiment of the invention;

FIG. **24**C illustrates an example timing diagram of an isolation signal according to an embodiment of the invention;

FIGS. **25**A-H illustrate example aliasing signals at various aliasing rates according to embodiments of the invention;

FIG. **26**A illustrates a structural block diagram of an exemplary sample and hold system according to an embodiment of the invention;

FIG. **26**B illustrates a structural block diagram of an exemplary inverted sample and hold system according to an embodiment of the invention;

FIG. **27** illustrates a structural block diagram of sample and hold module according to an embodiment of the invention;

FIGS. **28**A-D illustrate example implementations of a switch module according to embodiments of the invention;

FIGS. **29**A-F illustrate example implementations of a holding module according to embodiments of the present invention;

FIG. **29**G illustrates an integrated under-sampling system according to embodiments of the invention;

FIGS. **29**H-K illustrate example implementations of pulse generators according to embodiments of the invention;

FIG. **29**L illustrates an example oscillator;

FIG. **30** illustrates a structural block diagram of an under-sampling system with an under-sampling signal optimizer according to embodiments of the invention;

FIG. **31**A illustrates a structural block diagram of an under-sampling signal optimizer according to embodiments of the present invention;

FIGS. **31**B and **31**C illustrate example waveforms present in the circuit of FIG. **31**A;

FIG. **32**A illustrates an example of an under-sampling signal module according to an embodiment of the invention;

FIG. **32**B illustrates a flowchart of a state machine operation associated with an under-sampling module according to embodiments of the invention;

FIG. **32**C illustrates an example under-sampling module that includes an analog circuit with automatic gain control according to embodiments of the invention;

FIGS. **33**A-D illustrate example signal diagrams associated with direct down-conversion of an EM signal to a baseband signal by under-sampling according to embodiments of the present invention;

FIGS. **34**A-F illustrate example signal diagrams associated with an inverted sample and hold module according to embodiments of the invention;

FIGS. **35**A-E illustrate example signal diagrams associated with directly down-converting an analog AM signal to a demodulated baseband signal by under-sampling according to embodiments of the invention;

FIGS. **36**A-E illustrate example signal diagrams associated with down-converting a digital AM signal to a demodulated baseband signal by under-sampling according to embodiments of the invention;

FIGS. **37**A-E illustrate example signal diagrams associated with directly down-converting an analog PM signal to a demodulated baseband signal by under-sampling according to embodiments of the invention;

FIGS. **38**A-E illustrate example signal diagrams associated with down-converting a digital PM signal to a demodulated baseband signal by under-sampling according to embodiments of the invention;

FIGS. **39**A-D illustrate down-converting a FM signal to a non-FM signal by under-sampling according to embodiments of the invention;

FIGS. **40**A-E illustrate down-converting a FSK signal to a PSK signal by under-sampling according to embodiments of the invention;

FIGS. **41**A-E illustrate down-converting a FSK signal to an ASK signal by under-sampling according to embodiments of the invention;

FIG. **42** illustrates a structural block diagram of an inverted sample and hold according to an embodiment of the present invention;

FIG. **43** illustrates an equation that represents the change in charge in an storage device of embodiments of a UFT module.

FIG. **44**A illustrates a structural block diagram of a differential system according to embodiments of the invention;

FIG. **44**B illustrates a structural block diagram of a differential system with a differential input and a differential output according to embodiments of the invention;

FIG. **44**C illustrates a structural block diagram of a differential system with a single input and a differential output according to embodiments of the invention;

FIG. **44**D illustrates a differential input with a single output according to embodiments of the invention;

FIG. **44**E illustrates an example differential input to single output system according to embodiments of the invention;

FIGS. **45**A-B illustrate a conceptual illustration of aliasing including under-sampling and energy transfer according to embodiments of the invention;

FIGS. **46**A-D illustrate various flowchart for down-converting an EM signal by transferring energy from the EM signal at an aliasing rate according to embodiments of the invention;

FIGS. **47**A-E illustrate example signal diagrams associated with the flowcharts in FIGS. **46**A-D according to embodiments of the invention;

FIG. **48** is a flowchart that illustrates an example process for determining an aliasing rate associated with an aliasing signal according to an embodiment of the invention;

FIG. **49**A-H illustrate example energy transfer signals according to embodiments of the invention;

FIGS. **50**A-G illustrate example signal diagrams associated with down-converting an analog AM signal to an intermediate frequency by transferring energy at an aliasing rate according to embodiments of the invention;

FIGS. **51**A-G illustrate example signal diagrams associated with down-converting an digital AM signal to an intermediate frequency by transferring energy at an aliasing rate according to embodiments of the invention;

FIGS. **52**A-G illustrate example signal diagrams associated with down-converting an analog FM signal to an intermediate frequency by transferring energy at an aliasing rate according to embodiments of the invention;

FIGS. **53**A-G illustrate example signal diagrams associated with down-converting an digital FM signal to an intermediate frequency by transferring energy at an aliasing rate according to embodiments of the invention;

FIGS. **54**A-G illustrate example signal diagrams associated with down-converting an analog PM signal to an intermediate frequency by transferring energy at an aliasing rate according to embodiments of the invention;

FIGS. **55**A-G illustrate example signal diagrams associated with down-converting an digital PM signal to an intermediate frequency by transferring energy at an aliasing rate according to embodiments of the invention;

FIGS. **56**A-D illustrate an example signal diagram associated with direct down-conversion according to embodiments of the invention;

FIGS. **57**A-F illustrate directly down-converting an analog AM signal to a demodulated baseband signal according to embodiments of the invention;

FIGS. **58**A-F illustrate directly down-converting an digital AM signal to a demodulated baseband signal according to embodiments of the invention;

FIGS. **59**A-F illustrate directly down-converting an analog PM signal to a demodulated baseband signal according to embodiments of the invention;

FIGS. **60**A-F illustrate directly down-converting an digital PM signal to a demodulated baseband signal according to embodiments of the invention;

FIGS. **61**A-F illustrate down-converting an FM signal to a PM signal according to embodiments of the invention;

FIGS. **62**A-F illustrate down-converting an FM signal to a AM signal according to embodiments of the invention;

FIG. **63** illustrates a block diagram of an energy transfer system according to an embodiment of the invention;

FIG. **64**A illustrates an exemplary gated transfer system according to an embodiment of the invention;

FIG. **64**B illustrates an exemplary inverted gated transfer system according to an embodiment of the invention;

FIG. **65** illustrates an example embodiment of the gated transfer module according to an embodiment of the invention;

FIGS. **66**A-D illustrate example implementations of a switch module according to embodiments of the invention;

FIG. **67**A illustrates an example embodiment of the gated transfer module as including a break-before-make module according to an embodiment of the invention;

FIG. **67**B illustrates an example timing diagram for an energy transfer signal according to an embodiment of the invention;

FIG. **67**C illustrates an example timing diagram for an isolation signal according to an embodiment of the invention;

FIGS. **68**A-F illustrate example storage modules according to embodiments of the invention;

FIG. **68**G illustrates an integrated gated transfer system according to an embodiment of the invention;

FIGS. **68**H-K illustrate example aperture generators;

FIG. **68**L illustrates an oscillator according to an embodiment of the present invention;

FIG. **69** illustrates an energy transfer system with an optional energy transfer signal module according to an embodiment of the invention;

FIG. **70** illustrates an aliasing module with input and output impedance match according to an embodiment of the invention;

FIG. **71**A illustrates an example pulse generator;

FIGS. **71** B and C illustrate example waveforms related to the pulse generator of FIG. **71**A;

FIG. **72** illustrates an example embodiment where preprocessing is used to select a portion of the carrier signal to be operated upon;

FIG. **73** illustrates an example energy transfer module with a switch module and a reactive storage module according to an embodiment of the invention;

FIG. **74** illustrates an example inverted gated transfer module as including a switch module and a storage module according to an embodiment of the invention;

FIGS. **75**A-F illustrate an example signal diagrams associated with an inverted gated energy transfer module according to embodiments of the invention;

FIGS. **76**A-E illustrate energy transfer modules in configured in various differential configurations according to embodiments of the invention;

FIGS. **77**A-C illustrate example impedance matching circuits according to embodiments of the invention;

FIGS. **78**A-B illustrate example under-sampling systems according to embodiments of the invention;

FIGS. **79**A-F illustrate example timing diagrams for under-sampling systems according to embodiments of the invention;

FIGS. **80**A-F illustrate example timing diagrams for an under-sampling system when the load is a relatively low impedance load according to embodiments of the invention;

FIGS. **81**A-F illustrate example timing diagrams for an under-sampling system when the holding capacitance has a larger value according to embodiments of the invention;

FIGS. **82**A-B illustrate example energy transfer systems according to embodiments of the invention;

FIGS. **83**A-F illustrate example timing diagrams for energy transfer systems according to embodiments of the present invention;

FIGS. **84**A-D illustrate down-converting an FSK signal to a PSK signal according to embodiments of the present invention;

FIG. **85**A illustrates an example energy transfer signal module according to an embodiment of the present invention;

FIG. **85**B illustrates a flowchart of state machine operation according to an embodiment of the present invention;

FIG. **85**C is an example energy transfer signal module;

FIG. **86** is a schematic diagram of a circuit to down-convert a 915 MHZ signal to a 5 MHZ signal using a 101.1 MHZ clock according to an embodiment of the present invention;

FIG. **87** shows simulation waveforms for the circuit of FIG. **86** according to embodiments of the present invention;

FIG. **88** is a schematic diagram of a circuit to down-convert a 915 MHZ signal to a 5 MHz signal using a 101 MHZ clock according to an embodiment of the present invention;

FIG. **89** shows simulation waveforms for the circuit of FIG. **88** according to embodiments of the present invention;

FIG. **90** is a schematic diagram of a circuit to down-convert a 915 MHZ signal to a 5 MHZ signal using a 101.1 MHZ clock according to an embodiment of the present invention;

FIG. **91** shows simulation waveforms for the circuit of FIG. **90** according to an embodiment of the present invention;

FIG. **92** shows a schematic of the circuit in FIG. **86** connected to an FSK source that alternates between 913 and 917 MHZ at a baud rate of 500 Kbaud according to an embodiment of the present invention;

FIG. **93** shows the original FSK waveform **9202** and the down-converted waveform **9204** at the output of the load impedance match circuit according to an embodiment of the present invention;

FIG. **94**A illustrates an example energy transfer system according to an embodiment of the invention;

FIGS. **94**B-C illustrate example timing diagrams for the example system of FIG. **94**A;

FIG. **95** illustrates an example bypass network according to an embodiment of the invention;

FIG. **96** illustrates an example bypass network according to an embodiment of the invention;

FIG. **97** illustrates an example embodiment of the invention;

FIG. **98**A illustrates an example real time aperture control circuit according to an embodiment of the invention;

FIG. **98**B illustrates a timing diagram of an example clock signal for real time aperture control, according to an embodiment of the invention;

FIG. **98**C illustrates a timing diagram of an example optional enable signal for real time aperture control, according to an embodiment of the invention;

FIG. **98**D illustrates a timing diagram of an inverted clock signal for real time aperture control, according to an embodiment of the invention;

FIG. **98**E illustrates a timing diagram of an example delayed clock signal for real time aperture control, according to an embodiment of the invention;

FIG. **98**F illustrates a timing diagram of an example energy transfer including pulses having apertures that are controlled in real time, according to an embodiment of the invention;

FIG. **99** is a block diagram of a differential system that utilizes non-inverted gated transfer units, according to an embodiment of the invention;

FIG. **100** illustrates an example embodiment of the invention;

FIG. **101** illustrates an example embodiment of the invention;

FIG. **102** illustrates an example embodiment of the invention;

FIG. **103** illustrates an example embodiment of the invention;

FIG. **104** illustrates an example embodiment of the invention;

FIG. **105** illustrates an example embodiment of the invention;

FIG. **106** illustrates an example embodiment of the in invention;

FIG. **107**A is a timing diagram for the example embodiment of FIG. **103**;

FIG. **107**B is a timing diagram for the example embodiment of FIG. **104**;

FIG. **108**A is a timing diagram for the example embodiment of FIG. **105**;

FIG. **108**B is a timing diagram for the example embodiment of FIG. **106**;

FIG. **109**A illustrates and example embodiment of the invention;

FIG. **109**B illustrates equations for determining charge transfer, in accordance with the present invention;

FIG. **109**C illustrates relationships between capacitor charging and aperture, in accordance with the present invention;

FIG. **109**D illustrates relationships between capacitor charging and aperture, in accordance with the present invention;

FIG. **109**E illustrates power-charge relationship equations, in accordance with the present invention;

FIG. **109**F illustrates insertion loss equations, in accordance with the present invention;

FIG. **110**A illustrates aliasing module **11000** a single FET configuration;

FIG. **110**B illustrates FET conductivity vs. V_{GS};

FIGS. **111**A-C illustrate signal waveforms associated with aliasing module **11000**;

FIG. **112** illustrates aliasing module **11200** with a complementary FET configuration;

FIGS. **113**A-E illustrate signal waveforms associated with aliasing module **11200**;

FIG. **114** illustrates aliasing module **11400**;

FIG. **115** illustrates aliasing module **11500**;

FIG. **116** illustrates aliasing module **11602**;

FIG. **117** illustrates aliasing module **11702**;

FIGS. **118-120** illustrate signal waveforms associated with aliasing module **11602**;

FIGS. **121-123** illustrate signal waveforms associated with aliasing module **11702**.

FIG. **124**A is a block diagram of a splitter according to an embodiment of the invention;

FIG. **124**B is a more detailed diagram of a splitter according to an embodiment of the invention;

FIGS. **124**C and **124**D are example waveforms related to the splitter of FIGS. **124**A and **124**B;

FIG. **124**E is a block diagram of an I/Q circuit with a splitter according to an embodiment of the invention;

FIGS. **124**F-**124**J are example waveforms related to the diagram of FIG. **124**A;

FIG. **125** is a block diagram of a switch module according to an embodiment of the invention;

FIG. **126**A is an implementation example of the block diagram of FIG. **125**;

FIGS. **126**B-**126**Q are example waveforms related to FIG. **126**A;

FIG. **127**A is another implementation example of the block diagram of FIG. **125**;

FIGS. **127**B-**127**Q are example waveforms related to FIG. **127**A;

FIG. **128**A is an example MOSFET embodiment of the invention;

FIG. **128**B is an example MOSFET embodiment of the invention;

FIG. **128**C is an example MOSFET embodiment of the invention;

FIG. **129**A is another implementation example of the block diagram of FIG. **125**;

FIGS. **129**B-**129**Q are example waveforms related to FIG. **127**A;

FIGS. **130** and **131** illustrate the amplitude and pulse width modulated transmitter according to embodiments of the present invention;

FIGS. **132**A-**132**D, **133**, and **134** illustrate example signal diagrams associated with the amplitude and pulse width modulated transmitter according to embodiments of the present invention;

FIG. **135** shows an embodiment of a receiver block diagram to recover the amplitude or pulse width modulated information;

FIGS. **136**A-**136**G illustrate example signal diagrams associated with a waveform generator according to embodiments of the present invention;

FIGS. **137-139** are example schematic diagrams illustrating various circuits employed in the receiver of FIG. **135**;

FIGS. **140-143** illustrate time and frequency domain diagrams of alternative transmitter output waveforms;

FIGS. **144** and **145** illustrate differential receivers in accord with embodiments of the present invention;

FIGS. **146** and **147** illustrate time and frequency domains for a narrow bandwidth/constant carrier signal in accord with an embodiment of the present invention;

FIG. **148** illustrates a method for down-converting an electromagnetic signal according to an embodiment of the present invention using a matched filtering/correlating operation;

FIG. **149** illustrates a matched filtering/correlating processor according to an embodiment of the present invention;

FIG. **150** illustrates a method for down-converting an electromagnetic signal according to an embodiment of the present invention using a finite time integrating operation;

FIG. **151** illustrates a finite time integrating processor according to an embodiment of the present invention;

FIG. **152** illustrates a method for down-converting an electromagnetic signal according to an embodiment of the present invention using an RC processing operation.

FIG. **153** illustrates an RC processor according to an embodiment of the present invention;

FIG. **154** illustrates an example pulse train;

FIG. **155** illustrates combining a pulse train of energy signals to produce a power signal according to an embodiment of the invention;

FIG. **156** illustrates an example piecewise linear reconstruction of a sine wave.

FIG. **157** illustrates how certain portions of a carrier signal or sine waveform are selected for processing according to an embodiment of the present invention;

FIG. **158** illustrates an example double sideband large carrier AM waveform;

FIG. **159** illustrates a block diagram of an example optimum processor system;

FIG. **160** illustrates the frequency response of an optimum processor according to an embodiment of the present invention;

FIG. **161** illustrates example frequency responses for a processor at various apertures;

FIGS. **162-163** illustrates an example processor embodiment according to the present invention;

FIGS. **164**A-C illustrate example impulse responses of a matched filter processor and a finite time integrator;

FIG. **165** illustrates a basic circuit for an RC processor according to an embodiment of the present invention;

FIGS. **166-167** illustrate example plots of voltage signals;

FIGS. **168-170** illustrate the various characteristics of a processor according to an embodiment of the present invention;

FIGS. **171-173** illustrate example processor embodiments according to the present invention;

FIG. **174** illustrates the relationship between beta and the output charge of a processor according to an embodiment of the present invention;

FIG. **175**A illustrates an RC processor according to an embodiment of the present invention coupled to a load resistance;

FIG. **175**B illustrates an example implementation of the present invention;

FIG. **175**C illustrates an example charge/discharge timing diagram according to an embodiment of the present invention;

FIG. **175**D illustrates example energy transfer pulses according to an embodiment of the present invention;

FIG. **176** illustrates example performance characteristics of an embodiment of the present invention;

FIG. **177** A illustrates example performance characteristics of an embodiment of the present invention;

FIG. **177**B illustrates example waveforms for elementary matched filters.

FIG. **177**C illustrates a waveform for an embodiment of a UFT subharmonic matched filter of the present invention.

FIG. **177**D illustrates example embodiments of complex matched filter/correlator processor;

FIG. **177**E illustrates an embodiment of a complex matched filter/correlator processor of the present invention;

FIG. **177**F illustrates an embodiment of the decomposition of a non-ideal correlator alignment into an ideally aligned UFT correlator component of the present invention;

FIGS. **178**A-**178**B illustrate example processor waveforms according to an embodiment of the present invention;

FIG. **179** illustrates the Fourier transforms of example waveforms waveforms according to an embodiment of the present invention;

FIGS. **180-181** illustrates actual waveforms from an embodiment of the present invention;

FIG. **182** illustrates a relationship between an example UFT waveform and an example carrier waveform;

FIG. **183** illustrates example impulse samplers having various apertures;

FIG. **184** illustrates the alignment of sample apertures according to an embodiment of the present invention;

FIG. **185** illustrates an ideal aperture according to an embodiment of the present invention;

FIG. **186** illustrates the relationship of a step function and delta functions;

FIG. **187** illustrates an embodiment of a receiver with bandpass filter for complex down-converting of the present invention;

FIG. **188** illustrates Fourier transforms used to analyze a clock embodiment in accordance with the present invention;

FIG. **189** illustrates an acquisition and hold processor according to an embodiment of the present invention;

FIGS. **190-191** illustrate frequency representations of transforms according to an embodiment of the present invention;

FIG. **192** illustrates an example clock generator;

FIG. **193** illustrates the down-conversion of an electromagnetic signal according to an embodiment of the present invention;

FIG. **194** illustrates a receiver according to an embodiment of the present invention;

FIG. **195** illustrates a vector modulator according to an embodiment of the present invention;

FIG. **196** illustrates example waveforms for the vector modulator of FIG. **195**;

FIG. **197** illustrates an exemplary I/Q modulation receiver, according to an embodiment of the present invention;

FIG. **198** illustrates a I/Q modulation control signal generator, according to an embodiment of the present invention;

FIG. **199** illustrates example waveforms related to the I/Q modulation control signal generator of FIG. **198**;

FIG. **200** illustrates example control signal waveforms overlaid upon an example input RF signal;

FIG. **201** illustrates a I/Q modulation receiver circuit diagram, according to an embodiment of the present invention;

FIGS. **202-212** illustrate example waveforms related to a receiver implemented in accordance with the present invention;

FIG. **213** illustrates a single channel receiver, according to an embodiment of the present invention;

FIG. **214** illustrates exemplary waveforms associated with quad aperture implementations of the receiver of FIG. **281**, according to embodiments of the present invention;

FIG. **215** illustrates a high-level example UFT module radio architecture, according to an embodiment of the present invention;

FIG. **216** illustrates wireless design considerations;

FIG. **217** illustrates noise figure calculations based on RMS voltage and current noise specifications;

FIG. **218**A illustrates an example differential input, differential output receiver configuration, according to an embodiment of the present invention;

FIG. **218**B illustrates a example receiver implementation, configured as an I-phase channel, according to an embodiment of the present invention;

FIG. **218**C illustrates example waveforms related to the receiver of FIG. **218**B;

FIG. **218**D illustrates an example re-radiation frequency spectrum related to the receiver of FIG. **218**B, according to an embodiment of the present invention;

FIG. **218**E illustrates an example re-radiation frequency spectral plot related to the receiver of FIG. **218**B, according to an embodiment of the present invention;

FIG. **218**F illustrates example impulse sampling of an input signal;

FIG. **218**G illustrates example impulse sampling of an input signal in a environment with more noise relative to that of FIG. **218**F;

FIG. **219** illustrates an example integrated circuit conceptual schematic, according to an embodiment of the present invention;

FIG. **220** illustrates an example receiver circuit architecture, according to an embodiment of the present invention;

FIG. **221** illustrates example waveforms related to the receiver of FIG. **220**, according to an embodiment of the present invention;

FIG. **222** illustrates DC equations, according to an embodiment of the present invention;

FIG. **223** illustrates an example receiver circuit, according to an embodiment of the present invention;

FIG. **224** illustrates example waveforms related to the receiver of FIG. **223**;

FIG. **225** illustrates an example receiver circuit, according to an embodiment of the present invention;

FIGS. **226** and **227** illustrate example waveforms related to the receiver of FIG. **225**;

FIGS. **228-230** illustrate equations and information related to charge transfer;

FIG. **231** illustrates a graph related to the equations of FIG. **230**;

FIG. **232** illustrates example control signal waveforms and an example input signal waveform, according to embodiments of the present invention;

FIG. **233** illustrates an example differential output receiver, according to an embodiment of the present invention;

FIG. **234** illustrates example waveforms related to the receiver of FIG. **233**;

FIG. **235** illustrates an example transmitter circuit, according to an embodiment of the present invention;

FIG. **236** illustrates example waveforms related to the transmitter of FIG. **235**;

FIG. **237** illustrates an example frequency spectrum related to the transmitter of FIG. **235**;

FIG. **238** illustrates an intersection of frequency selectivity and frequency translation, according to an embodiment of the present invention;

FIG. **239** illustrates a multiple criteria, one solution aspect of the present invention;

FIG. **240** illustrates an example complementary FET switch structure, according to an embodiment of the present invention;

FIG. **241** illustrates example waveforms related to the complementary FET switch structure of FIG. **240**;

FIG. **242** illustrates an example differential configuration, according to an embodiment of the present invention;

FIG. **243** illustrates an example receiver implementing clock spreading, according to an embodiment of the present invention;

FIG. **244** illustrates example waveforms related to the receiver of FIG. **243**;

FIG. **245** illustrates waveforms related to the receiver of FIG. **243** implemented without clock spreading, according to an embodiment of the present invention;

FIG. **246** illustrates an example recovered I/Q waveforms, according to an embodiment of the present invention;

FIG. **247** illustrates an example CMOS implementation, according to an embodiment of the present invention;

FIG. **248** illustrates an example LO gain stage of FIG. **247** at a gate level, according to an embodiment of the present invention;

FIG. **249** illustrates an example LO gain stage of FIG. **247** at a transistor level, according to an embodiment of the present invention;

FIG. **250** illustrates an example pulse generator of FIG. **247** at a gate level, according to an embodiment of the present invention;

FIG. **251** illustrates an example pulse generator of FIG. **247** at a transistor level, according to an embodiment of the present invention;

FIG. **252** illustrates an example power gain block of FIG. **247** at a gate level, according to an embodiment of the present invention;

FIG. **253** illustrates an example power gain block of FIG. **247** at a transistor level, according to an embodiment of the present invention;

FIG. **254** illustrates an example switch of FIG. **247** at a transistor level, according to an embodiment of the present invention;

FIG. **255** illustrates an example CMOS "hot clock" block diagram, according to an embodiment of the present invention;

FIG. **256** illustrates an example positive pulse generator of FIG. **255** at a gate level, according to an embodiment of the present invention;

FIG. **257** illustrates an example positive pulse generator of FIG. **255** at a transistor level, according to an embodiment of the present invention;

FIG. **258** illustrates pulse width error effect for ½ cycle;

FIG. **259** illustrates an example single-ended receiver circuit implementation, according to an embodiment of the present invention;

FIG. **260** illustrates an example single-ended receiver circuit implementation, according to an embodiment of the present invention;

FIG. **261** illustrates an example full differential receiver circuit implementation, according to an embodiment of the present invention;

FIG. **262** illustrates an example full differential receiver implementation, according to an embodiment of the present invention;

FIG. **263** illustrates an example single-ended receiver implementation, according to an embodiment of the present invention;

FIG. **264** illustrates a plot of loss in sensitivity vs. clock phase deviation, according to an example embodiment of the present invention;

FIGS. **265** and **266** illustrate example 802.11 WLAN receiver/transmitter implementations, according to embodiments of the present invention;

FIG. **267** illustrates 802.11 requirements in relation to embodiments of the present invention;

FIG. **268** illustrates an example doubler implementation for phase noise cancellation, according to an embodiment of the present invention;

FIG. **269** illustrates an example doubler implementation for phase noise cancellation, according to an embodiment of the present invention;

FIG. **270** illustrates a example bipolar sampling aperture, according to an embodiment of the present invention;

FIG. **271** illustrates an example diversity receiver, according to an embodiment of the present invention;

FIG. **272** illustrates an example equalizer implementation, according to an embodiment of the present invention;

FIG. **273** illustrates an example multiple aperture receiver using two apertures, according to an embodiment of the present invention;

FIG. **274** illustrates exemplary waveforms related to the multiple aperture receiver of FIG. **273**, according to an embodiment of the present invention;

FIG. **275** illustrates an example multiple aperture receiver using three apertures, according to an embodiment of the present invention;

FIG. **276** illustrates exemplary waveforms related to the multiple aperture receiver of FIG. **275**, according to an embodiment of the present invention;

FIG. **277** illustrates an example multiple aperture transmitter, according to an embodiment of the present invention;

FIG. **278** illustrates example frequency spectrums related to the transmitter of FIG. **277**;

FIG. **279** illustrates an example output waveform in a double aperture implementation of the transmitter of FIG. **277**;

FIG. **280** illustrates an example output waveform in a single aperture implementation of the transmitter of FIG. **277**;

FIG. **281** illustrates an example multiple aperture receiver implementation, according to an embodiment of the present invention;

FIG. **282** illustrates exemplary waveforms in a single aperture implementation of the receiver of FIG. **281**, according to an embodiment of the present invention;

FIG. **283** illustrates exemplary waveforms in a dual aperture implementation of the receiver of FIG. **281**, according to an embodiment of the present invention;

FIG. **284** illustrates exemplary waveforms in a triple aperture implementation of the receiver of FIG. **281**, according to an embodiment of the present invention; and

FIG. **285** illustrates exemplary waveforms in quad aperture implementations of the receiver of FIG. **281**, according to embodiments of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

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1. INTRODUCTION

1. General Terminology

For illustrative purposes, the operation of the invention is often represented by flowcharts, such as flowchart **1201** in FIG. **12**A. It should be understood, however, that the use of flowcharts is for illustrative purposes only, and is not limiting. For example, the invention is not limited to the operational embodiment(s) represented by the flowcharts. Instead, alternative operational embodiments will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein. Also, the use of flowcharts should not be interpreted as limiting the invention to discrete or digital operation. In practice, as will be appreciated by persons skilled in the relevant art(s) based on the herein discussion, the invention can be achieved via discrete or continuous operation, or a combination thereof. Further, the flow of control represented by the flowcharts is provided for illustrative purposes only. As will be appreciated by persons skilled in the relevant art(s), other operational control flows are within the scope and spirit of the present invention. Also, the ordering of steps may differ in various embodiments.

Various terms used in this application are generally described in this section. The description in this section is provided for illustrative and convenience purposes only, and is not limiting. The meaning of these terms will be apparent to persons skilled in the relevant art(s) based on the entirety of the teachings provided herein. These terms may be discussed throughout the specification with additional detail.

The term modulated carrier signal, when used herein, refers to a earlier signal that is modulated by a baseband signal.

The term unmodulated carrier signal, when used herein, refers to a signal having an amplitude that oscillates at a substantially uniform frequency and phase.

The term baseband signal, when used herein, refers to an information signal including, but not limited to, analog information signals, digital information signals and direct current (DC) information signals.

The term carrier signal, when used herein, and unless otherwise specified when used herein, refers to modulated carrier signals and unmodulated carrier signals, information signals, digital information signals, and direct current (DC) information signals.

The term electromagnetic (EM) signal, when used herein, refers to a signal in the EM spectrum. EM spectrum includes all frequencies greater than zero hertz. EM signals generally include waves characterized by variations in electric and magnetic fields. Such waves may be propagated in any medium, both natural and manmade, including but not limited to air, space, wire, cable, liquid, waveguide, micro-strip, strip-line, optical fiber, etc. Unless stated otherwise, all signals discussed herein are EM signals, even when not explicitly designated as such.

The term intermediate frequency (IF) signal, when used herein, refers to an EM signal that is substantially similar to another EM signal except that the IF signal has a lower frequency than the other signal. An IF signal frequency can be any frequency above zero HZ. Unless otherwise stated, the terms lower frequency, intermediate frequency, intermediate and IF are used interchangeably herein.

The term analog signal, when used herein, refers to a signal that is constant or continuously variable, as contrasted to a signal that changes between discrete states.

The term baseband, when used herein, refers to a frequency band occupied by any generic information signal desired for transmission and/or reception.

The term baseband signal, when used herein, refers to any generic information signal desired for transmission and/or reception.

The term carrier frequency, when used herein, refers to the frequency of a carrier signal. Typically, it is the center frequency of a transmission signal that is generally modulated.

The term carrier signal, when used herein, refers to an EM wave having at least one characteristic that may be varied by modulation, that is capable of carrying information via modulation.

The term demodulated baseband signal, when used herein, refers to a signal that results from processing a modulated signal. In some cases, for example, the demodulated baseband signal results from demodulating an intermediate frequency (IF) modulated signal, which results from down converting a modulated carrier signal. In another case, a signal that results from a combined down conversion and demodulation step.

The term digital signal, when used herein, refers to a signal that changes between discrete states, as contrasted to a signal that is continuous. For example, the voltage of a digital signal may shift between discrete levels.

The term electromagnetic (EM) spectrum, when used herein, refers to a spectrum comprising waves characterized by variations in electric and magnetic fields. Such waves may be propagated in any communication medium, both natural and manmade, including but not limited to air, space, wire, cable, liquid, waveguide, microstrip, stripline, optical fiber, etc. The EM spectrum includes all frequencies greater than zero hertz.

The term electromagnetic (EM) signal, when used herein, refers to a signal in the EM spectrum. Also generally called an EM wave. Unless stated otherwise, all signals discussed herein are EM signals, even when not explicitly designated as such.

The term modulating baseband signal, when used herein, refers to any generic information signal that is used to modulate an oscillating signal, or carrier signal.

1.1 Modulation

It is often beneficial to propagate electromagnetic (EM) signals at higher frequencies. This includes baseband signals, such as digital data information signals and analog information signals. A baseband signal can be up-converted to a higher frequency EM signal by using the baseband signal to modulate a higher frequency carrier signal, F_C. When used in this manner, such a baseband signal is herein called a modulating baseband signal F_{MB}.

Modulation imparts changes to the carrier signal F_C that represent information in the modulating baseband signal F_{MB}. The changes can be in the form of amplitude changes, frequency changes, phase changes, etc., or any combination thereof. The resultant signal is referred to herein as a modulated carrier signal F_{MC}. The modulated carrier signal F_{MC} includes the carrier signal F_C modulated by the modulating baseband signal, F_{MB}, as in:

$$F_{MB} \text{ combined with } F_C \rightarrow F_{MC}$$

The modulated carrier signal F_{MC} oscillates at, or near the frequency of the carrier signal F_C and can thus be efficiently propagated.

FIG. **1** illustrates an example modulator **110**, wherein the carrier signal F_C is modulated by the modulating baseband signal F_{MB}, thereby generating the modulated carrier signal F_{MC}.

Modulating baseband signal F_{MB} can be an analog baseband signal, a digital baseband signal, or a combination thereof.

FIG. **2** illustrates the modulating baseband signal F_{MB} as an exemplary analog modulating baseband signal **210**. The exemplary analog modulating baseband signal **210** can represent any type of analog information including, but not limited to, voice/speech data, music data, video data, etc. The amplitude of analog modulating baseband signal **210** varies in time.

Digital information includes a plurality of discrete states. For ease of explanation, digital information signals are discussed below as having two discrete states. But the invention is not limited to this embodiment.

FIG. **3** illustrates the modulating baseband signal F_{MB} as an exemplary digital modulating baseband signal **310**. The digital modulating baseband signal **310** can represent any type of digital data including, but not limited to, digital computer information and digitized analog information. The digital modulating baseband signal **310** includes a first state **312** and a second state **314**. In an embodiment, first state **312** represents binary state 0 and second state **314** represents binary state 1. Alternatively, first state **312** represents binary state 1 and second state **314** represents binary state 0. Throughout the remainder of this disclosure, the former convention is followed, whereby first state **312** represents binary state zero and second state **314** represents binary state one. But the invention is not limited to this embodiment. First state **312** is thus referred to herein as a low state and second state **314** is referred to herein as a high state.

Digital modulating baseband signal **310** can change between first state **312** and second state **314** at a data rate, or baud rate, measured as bits per second.

Carrier signal F_C is modulated by the modulating baseband signal F_{MB}, by any modulation technique, including, but not limited to, amplitude modulation (AM), frequency modulation (FM), phase modulation (PM), etc., or any combination thereof. Examples are provided below for amplitude modulating, frequency modulating, and phase modulating the analog modulating baseband signal **210** and the digital modulating baseband signal **310**, on the carrier signal F_C. The

examples are used to assist in the description of the invention. The invention is not limited to, or by, the examples.

FIG. **4** illustrates the carrier signal F_C as a carrier signal **410**. In the example of FIG. **4**, the carrier signal **410** is illustrated as a 900 MHZ carrier signal. Alternatively, the carrier signal **410** can be any other frequency. Example modulation schemes are provided below, using the examples signals from FIGS. **2**, **3** and **4**.

1.1.1 Amplitude Modulation

In amplitude modulation (AM), the amplitude of the modulated carrier signal F_{MC} is a function of the amplitude of the modulating baseband signal F_{MB}. FIGS. **5**A-**5**C illustrate example timing diagrams for amplitude modulating the carrier signal **410** with the analog modulating baseband signal **210**. FIGS. **6**A-**6**C illustrate example timing diagrams for amplitude modulating the carrier signal **410** with the digital modulating baseband signal **310**.

FIG. **5**A illustrates the analog modulating baseband signal **210**. FIG. **5**B illustrates the carrier signal **410**. FIG. **5**C illustrates an analog AM carrier signal **516**, which is generated when the carrier signal **410** is amplitude modulated using the analog modulating baseband signal **210**. As used herein, the term "analog AM carrier signal" is used to indicate that the modulating baseband signal is an analog signal.

The analog AM carrier signal **516** oscillates at the frequency of carrier signal **410**. The amplitude of the analog AM carrier signal **516** tracks the amplitude of analog modulating baseband signal **210**, illustrating that the information contained in the analog modulating baseband signal **210** is retained in the analog AM carrier signal **516**.

FIG. **6**A illustrates the digital modulating baseband signal **310**. FIG. **6**B illustrates the carrier signal **410**. FIG. **6**C illustrates a digital AM carrier signal **616**, which is generated when the carrier signal **410** is amplitude modulated using the digital modulating baseband signal **310**. As used herein, the term "digital AM carrier signal" is used to indicate that the modulating baseband signal is a digital signal.

The digital AM carrier signal **616** oscillates at the frequency of carrier signal **410**. The amplitude of the digital AM carrier signal **616** tracks the amplitude of digital modulating baseband signal **310**, illustrating that the information contained in the digital modulating baseband signal **310** is retained in the digital AM signal **616**. As the digital modulating baseband signal **310** changes states, the digital AM signal **616** shifts amplitudes. Digital amplitude modulation is often referred to as amplitude shift keying (ASK), and the two terms are used interchangeably throughout the specification.

1.1.2 Frequency Modulation

In frequency modulation (FM), the frequency of the modulated carrier signal F_{MC} varies as a function of the amplitude of the modulating baseband signal F_{MB}. FIGS. **7**A-**7**C illustrate example timing diagrams for frequency modulating the carrier signal **410** with the analog modulating baseband signal **210**. FIGS. **8**A-**8**C illustrate example timing diagrams for frequency modulating the carrier signal **410** with the digital modulating baseband signal **310**.

FIG. **7**A illustrates the analog modulating baseband signal **210**. FIG. **7**B illustrates the carrier signal **410**. FIG. **7**C illustrates an analog FM carrier signal **716**, which is generated when the carrier signal **410** is frequency modulated using the analog modulating baseband signal **210**. As used herein, the term "analog FM carrier signal" is used to indicate that the modulating baseband signal is an analog signal.

The frequency of the analog FM carrier signal **716** varies as a function of amplitude changes on the analog baseband signal **210**. In the illustrated example, the frequency of the analog FM carrier signal **716** varies in proportion to the amplitude of the analog modulating baseband signal **210**. Thus, at time t1, the amplitude of the analog baseband signal **210** and the frequency of the analog FM carrier signal **716** are at maximums. At time t3, the amplitude of the analog baseband signal **210** and the frequency of the analog AM carrier signal **716** are at minimums.

The frequency of the analog FM carrier signal **716** is typically centered around the frequency of the carrier signal **410**. Thus, at time t2, for example, when the amplitude of the analog baseband signal **210** is at a mid-point, illustrated here as zero volts, the frequency of the analog FM carrier signal **716** is substantially the same as the frequency of the carrier signal **410**.

FIG. **8**A illustrates the digital modulating baseband signal **310**. FIG. **8**B illustrates the carrier signal **410**. FIG. **8**C illustrates a digital FM carrier signal **816**, which is generated when the carrier signal **410** is frequency modulated using the digital baseband signal **310**. As used herein, the term "digital FM carrier signal" is used to indicate that the modulating baseband signal is a digital signal.

The frequency of the digital FM carrier signal **816** varies as a function of amplitude changes on the digital modulating baseband signal **310**. In the illustrated example, the frequency of the digital FM carrier signal **816** varies in proportion to the amplitude of the digital modulating baseband signal **310**. Thus, between times t0 and t1, and between times t2 and t4, when the amplitude of the digital baseband signal **310** is at the higher amplitude second state, the frequency of the digital FM carrier signal **816** is at a maximum. Between times t1 and t2, when the amplitude of the digital baseband signal **310** is at the lower amplitude first state, the frequency of the digital FM carrier signal **816** is at a minimum. Digital frequency modulation is often referred to as frequency shift keying (FSK), and the terms are used interchangeably throughout the specification.

Typically, the frequency of the digital FM carrier signal **816** is centered about the frequency of the carrier signal **410**, and the maximum and minimum frequencies are equally offset from the center frequency. Other variations can be employed but, for ease of illustration, this convention will be followed herein.

1.1.3 Phase Modulation

In phase modulation (PM), the phase of the modulated carrier signal F_{MC} varies as a function of the amplitude of the modulating baseband signal F_{MB}. FIGS. **9**A-**9**C illustrate example timing diagrams for phase modulating the carrier signal **410** with the analog modulating baseband signal **210**. FIGS. **10**A-**10**C illustrate example timing diagrams for phase modulating the carrier signal **410** with the digital modulating baseband signal **310**.

FIG. **9**A illustrates the analog modulating baseband signal **210**. FIG. **9**B illustrates the carrier signal **410**. FIG. **9**C illustrates an analog PM carrier signal **916**, which is generated by phase modulating the carrier signal **410** with the analog baseband signal **210**. As used herein, the term "analog PM carrier signal" is used to indicate that the modulating baseband signal is an analog signal.

Generally, the frequency of the analog PM carrier signal **916** is substantially the same as the frequency of carrier signal **410**. But the phase of the analog PM carrier signal **916** varies with amplitude changes on the analog modulating baseband signal **210**. For relative comparison, the carrier signal **410** is illustrated in FIG. **9**C by a dashed line.

The phase of the analog PM carrier signal **916** varies as a function of amplitude changes of the analog baseband signal **210**. In the illustrated example, the phase of the analog PM signal **916** lags by a varying amount as determined by the

amplitude of the baseband signal **210**. For example, at time t1, when the amplitude of the analog baseband signal **210** is at a maximum, the analog PM carrier signal **916** is in phase with the carrier signal **410**. Between times t1 and t3, when the amplitude of the analog baseband signal **210** decreases to a minimum amplitude, the phase of the analog PM carrier signal **916** lags the phase of the carrier signal **410**, until it reaches a maximum out of phase value at time t3. In the illustrated example, the phase change is illustrated as approximately 180 degrees. Any suitable amount of phase change, varied in any manner that is a function of the baseband signal, can be utilized.

FIG. **10**A illustrates the digital modulating baseband signal **310**. FIG. **10**B illustrates the carrier signal **410**. FIG. **10**C illustrates a digital PM carrier signal **1016**, which is generated by phase modulating the carrier signal **410** with the digital baseband signal **310**. As used herein, the term "digital PM carrier signal" is used to indicate that the modulating baseband signal is a digital signal.

The frequency of the digital PM carrier signal **1016** is substantially the same as the frequency of carrier signal **410**. The phase of the digital PM carrier signal **1016** varies as a function of amplitude changes on the digital baseband signal **310**. In the illustrated example, when the digital baseband signal **310** is at the first state **312**, the digital PM carrier signal **1016** is out of phase with the carrier signal **410**. When the digital baseband signal **310** is at the second state **314**, the digital PM carrier signal **1016** is in-phase with the carrier signal **410**. Thus, between times t1 and t2, when the amplitude of the digital baseband signal **310** is at the first state **312**, the digital PM carrier signal **1016** is out of phase with the carrier signal **410**. Between times t0 and t1, and between times t2 and t4, when the amplitude of the digital baseband signal **310** is at the second state **314**, the digital PM carrier signal **1016** is in phase with the carrier signal **410**.

In the illustrated example, the out of phase value between times t1 and t3 is illustrated as approximately 180 degrees out of phase. Any suitable amount of phase change, varied in any manner that is a function of the baseband signal, can be utilized. Digital phase modulation is often referred to as phase shift keying (PSK), and the terms are used interchangeably throughout the specification.

1.2 Demodulation

When the modulated carrier signal F_{MC} is received, it can be demodulated to extract the modulating baseband signal F_{MB}. Because of the typically high frequency of modulated carrier signal F_{MC}, however, it is generally impractical to demodulate the baseband signal F_{MB} directly from the modulated carrier signal F_{MC}. Instead, the modulated carrier signal F_{MC} must be down-converted to a lower frequency signal that contains the original modulating baseband signal.

When a modulated carrier signal is down-converted to a lower frequency signal, the lower frequency signal is referred to herein as an intermediate frequency (IF) signal F_{IF}. The IF signal F_{IF} oscillates at any frequency, or frequency band, below the frequency of the modulated carrier frequency F_{MC}. Down-conversion of F_{MC} to F_{IF} is illustrated as:

$$F_{MC} \rightarrow F_{IF}$$

After F_{MC} is down-converted to the IF modulated carrier signal F_{IF}, F_{IF} can be demodulated to a baseband signal F_{DMB}, as illustrated by:

$$F_{IF} \rightarrow F_{DMB}$$

F_{DMB} is intended to be substantially similar to the modulating baseband signal F_{MB}, illustrating that the modulating baseband signal F_{MB} can be substantially recovered.

It will be emphasized throughout the disclosure that the present invention can be implemented with any type of EM signal, including, but not limited to, modulated carrier signals and unmodulated carrier signals. The above examples of modulated carrier signals are provided for illustrative purposes only. Many variations to the examples are possible. For example, a carrier signal can be modulated with a plurality of the modulation types described above. A carrier signal can also be modulated with a plurality of baseband signals, including analog baseband signals, digital baseband signals, and combinations of both analog and digital baseband signals.

2. Overview of the Invention

Conventional signal processing techniques follow the Nyquist sampling theorem, which states that, in order to faithfully reproduce a sampled signal, the signal must be sampled at a rate that is greater than twice the frequency of the signal being sampled. When a signal is sampled at less than or equal to twice the frequency of the signal, the signal is said to be undersampled, or aliased. Conventional signal processing thus teaches away from under-sampling and aliasing, in order to faithfully reproduce a sampled signal.

2.1 Aspects of the Invention

Contrary to conventional wisdom, the present invention is a method and system for down-converting an electromagnetic (EM) signal by aliasing the EM signal. Aliasing is represented generally in FIG. **45**A as **4502**.

By taking a carrier and aliasing it at an aliasing rate, the invention can down-convert that carrier to lower frequencies. One aspect that can be exploited by this invention is realizing that the carrier is not the item of interest, the lower baseband signal is of interest to reproduce sufficiently. This baseband signal's frequency content, even though its carrier may be aliased, does satisfy the Nyquist criteria and as a result, the baseband information can be sufficiently reproduced.

FIG. **12**A depicts a flowchart **1201** that illustrates a method for aliasing an EM signal to generate a down-converted signal. The process begins at step **1202**, which includes receiving the EM signal. Step **1204** includes receiving an aliasing signal having an aliasing rate. Step **1206** includes aliasing the EM signal to down-convert the EM signal. The term aliasing, as used herein, refers to both down-converting an EM signal by under-sampling the EM signal at an aliasing rate and to down-converting an EM signal by transferring energy from the EM signal at the aliasing rate. These concepts are described below.

FIG. **13** illustrates a block diagram of a generic aliasing system **1302**, which includes an aliasing module **1306**. In an embodiment, the aliasing system **1302** operates in accordance with the flowchart **1201**. For example, in step **1202**, the aliasing module **1306** receives an EM signal **1304**. In step **1204**, the aliasing module **1306** receives an aliasing signal **1310**. In step **1206**, the aliasing module **1306** down-converts the EM signal **1304** to a down-converted signal **1308**. The generic aliasing system **1302** can also be used to implement any of the flowcharts **1207**, **1213** and **1219**.

In an embodiment, the invention down-converts the EM signal to an intermediate frequency (IF) signal. FIG. **12**B depicts a flowchart **1207** that illustrates a method for under-sampling the EM signal at an aliasing rate to down-convert the EM signal to an IF signal. The process begins at step **1208**, which includes receiving an EM signal. Step **1210** includes receiving an aliasing signal having an aliasing rate F_{AR}. Step **1212** includes under-sampling the EM signal at the aliasing rate to down-convert the EM signal to an IF signal.

In another embodiment, the invention down-converts the EM signal to a demodulated baseband information signal.

FIG. **12**C depicts a flowchart **1213** that illustrates a method for down-converting the EM signal to a demodulated baseband signal. The process begins at step **1214**, which includes receiving an EM signal. Step **1216** includes receiving an aliasing signal having an aliasing rate F_{AR}. Step **1218** includes down-converting the EM signal to a demodulated baseband signal. The demodulated baseband signal can be processed without further down-conversion or demodulation.

In another embodiment, the EM signal is a frequency modulated (FM) signal, which is down-converted to a non-FM signal, such as a phase modulated (PM) signal or an amplitude modulated (AM) signal. FIG. **12**D depicts a flowchart **1219** that illustrates a method for down-converting the FM signal to a non-FM signal. The process begins at step **1220**, which includes receiving an EM signal. Step **1222** includes receiving an aliasing signal having an aliasing rate. Step **1224** includes down-converting the FM signal to a non-FM signal.

The invention down-converts any type of EM signal, including, but not limited to, modulated carrier signals and unmodulated carrier signals. For ease of discussion, the invention is further described herein using modulated carrier signals for examples. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention can be implemented to down-convert signals other than carrier signals as well. The invention is not limited to the example embodiments described above.

In an embodiment, down-conversion is accomplished by under-sampling an EM signal. This is described generally in Section I.2.2. below and in detail in Section II and its subsections. In another embodiment, down-conversion is achieved by transferring non-negligible amounts of energy from an EM signal. This is described generally in Section I.2.3. below and in detail in Section III.

2.2 Down-Converting by Under-Sampling

The term aliasing, as used herein, refers both to down-converting an EM signal by under-sampling the EM signal at an aliasing rate and to down-converting an EM signal by transferring energy from the EM signal at the aliasing rate. Methods for under-sampling an EM signal to down-convert the EM signal are now described at an overview level. FIG. **14**A depicts a flowchart **1401** that illustrates a method for under-sampling the EM signal at an aliasing rate to down-convert the EM signal. The process begins at step **1402**, which includes receiving an EM signal. Step **1404** includes receiving an under-sampling signal having an aliasing rate. Step **1406** includes under-sampling the EM signal at the aliasing rate to down-convert the EM signal.

Down-converting by under-sampling is illustrated by **4504** in FIG. **45**A and is described in greater detail in Section II.

2.2.1 Down-Converting to an Intermediate Frequency (IF) Signal

In an embodiment, an EM signal is under-sampled at an aliasing rate to down-convert the EM signal to a lower, or intermediate frequency (IF) signal. The EM signal can be a modulated carrier signal or an unmodulated carrier signal. In an exemplary example, a modulated carrier signal F_{MC} is down-converted to an IF signal F_{IF}.

$$F_{MC} \rightarrow F_{IF}$$

FIG. **14**B depicts a flowchart **1407** that illustrates a method for undersampling the EM signal at an aliasing rate to down-convert the EM signal to an IF signal. The process begins at step **1408**, which includes receiving an EM signal. Step **1410** includes receiving an under-sampling signal having an aliasing rate. Step **1412** includes under-sampling the EM signal at the aliasing rate to down-convert the EM signal to an IF signal.

This embodiment is illustrated generally by **4508** in FIG. **45**B and is described in Section II.1.

2.2.2 Direct-to-Data Down-Converting

In another embodiment, an EM signal is directly down-converted to a demodulated baseband signal (direct-to-data down-conversion), by undersampling the EM signal at an aliasing rate. The EM signal can be a modulated EM signal or an unmodulated EM signal. In an exemplary embodiment, the EM signal is the modulated carrier signal F_{MC}, and is directly down-converted to a demodulated baseband signal F_{DMB}.

$$F_{MC} \rightarrow F_{DMB}$$

FIG. **14**C depicts a flowchart **1413** that illustrates a method for under-sampling the EM signal at an aliasing rate to directly down-convert the EM signal to a demodulated baseband signal. The process begins at step **1414**, which includes receiving an EM signal. Step **1416** includes receiving an under-sampling signal having an aliasing rate. Step **1418** includes under-sampling the EM signal at the aliasing rate to directly down-convert the EM signal to a baseband information signal.

This embodiment is illustrated generally by **4510** in FIG. **45**B and is described in Section II.2.

2.2.3 Modulation Conversion

In another embodiment, a frequency modulated (FM) carrier signal F_{FMC} is converted to a non-FM signal $F_{(NON\text{-}FM)}$, by under-sampling the FM carrier signal F_{FMC}.

$$F_{FMC} \rightarrow F_{(NON\text{-}FM)}$$

FIG. **14**D depicts a flowchart **1419** that illustrates a method for under-sampling an FM signal to convert it to a non-FM signal. The process begins at step **1420**, which includes receiving the FM signal. Step **1422** includes receiving an under-sampling signal having an aliasing rate. Step **1424** includes under-sampling the FM signal at the aliasing rate to convert the FM signal to a non-FM signal. For example, the FM signal can be under-sampled to convert it to a PM signal or an AM signal.

This embodiment is illustrated generally by **4512** in FIG. **45**B, and described in Section II.3

2.3 Down-Converting by Transferring Energy

The term aliasing, as used herein, refers both to down-converting an EM signal by under-sampling the EM signal at an aliasing rate and to down-converting an EM signal by transferring non-negligible amounts energy from the EM signal at the aliasing rate. Methods for transferring energy from an EM signal to down-convert the EM signal are now described at an overview level. More detailed descriptions are provided in Section III.

FIG. **46**A depicts a flowchart **4601** that illustrates a method for transferring energy from the EM signal at an aliasing rate to down-convert the EM signal. The process begins at step **4602**, which includes receiving an EM signal. Step **4604** includes receiving an energy transfer signal having an aliasing rate. Step **4606** includes transferring energy from the EM signal at the aliasing rate to down-convert the EM signal.

Down-converting by transferring energy is illustrated by **4506** in FIG. **45**A and is described in greater detail in Section III.

2.3.1 Down-Converting to an Intermediate Frequency (IF) Signal

In an embodiment, EM signal is down-converted to a lower, or intermediate frequency (IF) signal, by transferring energy from the EM signal at an aliasing rate. The EM signal

can be a modulated carrier signal or an unmodulated carrier signal. In an exemplary example, a modulated carrier signal F_{MC} is down-converted to an IF signal F_F.

$$F_{MC} \rightarrow F_{IF}$$

FIG. **46**B depicts a flowchart **4607** that illustrates a method for transferring energy from the EM signal at an aliasing rate to down-convert the EM signal to an IF signal. The process begins at step **4608**, which includes receiving an EM signal. Step **4610** includes receiving an energy transfer signal having an aliasing rate. Step **4612** includes transferring energy from the EM signal at the aliasing rate to down-convert the EM signal to an IF signal.

This embodiment is illustrated generally by **4514** in FIG. **45**B and is described in Section III.1.

2.3.2 Direct-to-Data Down-Converting

In another embodiment, an EM signal is down-converted to a demodulated baseband signal by transferring energy from the EM signal at an aliasing rate. This embodiment is referred to herein as direct-to-data down-conversion. The EM signal can be a modulated EM signal or an unmodulated EM signal. In an exemplary embodiment, the EM signal is the modulated carrier signal F_{MC}, and is directly down-converted to a demodulated baseband signal F_{DMB}.

$$F_{MC} \rightarrow F_{DMB}$$

FIG. **46**C depicts a flowchart **4613** that illustrates a method for transferring energy from the EM signal at an aliasing rate to directly down-convert the EM signal to a demodulated baseband signal. The process begins at step **4614**, which includes receiving an EM signal. Step **4616** includes receiving an energy transfer signal having an aliasing rate. Step **4618** includes transferring energy from the EM signal at the aliasing rate to directly down-convert the EM signal to a baseband signal.

This embodiment is illustrated generally by **4516** in FIG. **45**B and is described in Section III.2

2.3.3 Modulation Conversion

In another embodiment, a frequency modulated (FM) carrier signal F_{FMC} is converted to a non-FM signal $F_{(NON\text{-}FM)}$, by transferring energy from the FM carrier signal F_{FMC} at an aliasing rate.

$$F_{FMC} \rightarrow F_{(NON\text{-}FM)}$$

The FM carrier signal F_{FMC} can be converted to, for example, a phase modulated (PM) signal or an amplitude modulated (AM) signal. FIG. **46**D depicts a flowchart **4619** that illustrates a method for transferring energy from an FM signal to convert it to a non-FM signal. Step **4620** includes receiving the FM signal. Step **4622** includes receiving an energy transfer signal having an aliasing rate. In FIG. **46**D, step **4612** includes transferring energy from the FM signal to convert it to a non-FM signal. For example, energy can be transferred from an FSK signal to convert it to a PSK signal or an ASK signal.

This embodiment is illustrated generally by **4518** in FIG. **45**B, and described in Section III.3

2.3 Determining the Aliasing Rate

In accordance with the definition of aliasing, the aliasing rate is equal to, or less than, twice the frequency of the EM carrier signal. Preferably, the aliasing rate is much less than the frequency of the carrier. The aliasing rate is preferably more than twice the highest frequency component of the modulating baseband signal F_{MB} that is to be reproduced. The above requirements are illustrated in EQ. (1).

$$2 \cdot F_{MC} \geq F_{AR} > 2 \cdot (\text{Highest Freq. Component of } F_{MB}) \quad \text{EQ. (1)}$$

In other words, by taking a carrier and aliasing it at an aliasing rate, the invention can down-convert that carrier to lower frequencies. One aspect that can be exploited by this invention is that the carrier is not the item of interest; instead the lower baseband signal is of interest to be reproduced sufficiently. The baseband signal's frequency content, even though its carrier may be aliased, satisfies the Nyquist criteria and as a result, the baseband information can be sufficiently reproduced, either as the intermediate modulating carrier signal F_{IF} or as the demodulated direct-to-data baseband signal F_{DMB}.

In accordance with the invention, relationships between the frequency of an EM carrier signal, the aliasing rate, and the intermediate frequency of the down-converted signal, are illustrated in EQ. (2).

$$F_C = n \cdot F_{AR} \pm F_{IF} \quad \text{EQ. (2)}$$

Where:

F_C is the frequency of the EM carrier signal that is to be aliased;

F_{AR} is the aliasing rate;

n identifies a harmonic or sub-harmonic of the aliasing rate (generally, n=0.5, 1, 2, 3, 4, . . .); and

F_{IF} is the intermediate frequency of the down-converted signal.

Note that as $(n \cdot F_{AR})$ approaches F_C, F_{IF} approaches zero. This is a special case where an EM signal is directly down-converted to a demodulated baseband signal. This special case is referred to herein as Direct-to-Data down-conversion. Direct-to-Data down-conversion is described in later sections.

High level descriptions, exemplary embodiments and exemplary implementations of the above and other embodiments of the invention are provided in sections below.

3. Benefits of the Invention Using an Example Conventional Receiver for Comparison

FIG. **11** illustrates an example conventional receiver system **1102**. The conventional system **1102** is provided both to help the reader to understand the functional differences between conventional systems and the present invention, and to help the reader to understand the benefits of the present invention.

The example conventional receiver system **1102** receives an electromagnetic (EM) signal **1104** via an antenna **1106**. The EM signal **1104** can include a plurality of EM signals such as modulated carrier signals. For example, the EM signal **1104** includes one or more radio frequency (RF) EM signals, such as a 900 MHZ modulated carrier signal. Higher frequency RF signals, such as 900 MHZ signals, generally cannot be directly processed by conventional signal processors. Instead, higher frequency RF signals are typically down-converted to lower intermediate frequencies (IF) for processing. The receiver system **1102** down-converts the EM signal **1104** to an intermediate frequency (IF) signal **1108***n*, which can be provided to a signal processor **1110**. When the EM signal **1104** includes a modulated carrier signal, the signal processor **1110** usually includes a demodulator that demodulates the IF signal **1108***n* to a baseband information signal (demodulated baseband signal).

Receiver system **1102** includes an RF stage **1112** and one or more IF stages **1114**. The RF stage **1112** receives the EM signal **1104**. The RF stage **1112** includes the antenna **1106** that receives the EM signal **1104**.

The one or more IF stages **1114***a*-**1114***n* down-convert the EM signal **1104** to consecutively lower intermediate frequencies. Each of the one or more IF sections **1114***a*-**1114***n* includes a mixer **1118***a*-**1118***n* that down-converts an input

EM signal **1116** to a lower frequency IF signal **1108**. By cascading the one or more mixers **1118***a*-**1118***n*, the EM signal **1104** is incrementally down-converted to a desired IF signal **1108***n*.

In operation, each of the one or more mixers **1118** mixes an input EM signal **1116** with a local oscillator (LO) signal **1119**, which is generated by a local oscillator (LO) **1120**. Mixing generates sum and difference signals from the input EM signal **1116** and the LO signal **1119**. For example, mixing an input EM signal **1116***a*, having a frequency of 900 MHZ, with a LO signal **1119***a*, having a frequency of 830 MHZ, results in a sum signal, having a frequency of 900 MHZ+830 MHZ=1.73 GHZ, and a difference signal, having a frequency of 900 MHZ−830 MHZ=70 MHZ.

Specifically, in the example of FIG. **11**, the one or more mixers **1118** generate a sum and difference signals for all signal components in the input EM signal **1116**. For example, when the EM signal **1116***a* includes a second EM signal, having a frequency of 760 MHZ, the mixer **1118***a* generates a second sum signal, having a frequency of 760 MHZ+830 MHZ=1.59 GHZ, and a second difference signal, having a frequency of 830 MHZ−760 MHZ=70 MHZ. In this example, therefore, mixing two input EM signals, having frequencies of 900 MHZ and 760 MHZ, respectively, with an LO signal having a frequency of 830 MHZ, results in two IF signals at **70** MHZ.

Generally, it is very difficult, if not impossible, to separate the two 70 MHZ signals. Instead, one or more filters **1122** and **1123** are provided upstream from each mixer **1118** to filter the unwanted frequencies, also known as image frequencies. The filters **1122** and **1123** can include various filter topologies and arrangements such as bandpass filters, one or more high pass filters, one or more low pass filters, combinations thereof, etc.

Typically, the one or more mixers **1118** and the one or more filters **1122** and **1123** attenuate or reduce the strength of the EM signal **1104**. For example, a typical mixer reduces the EM signal strength by 8 to 12 dB. A typical filter reduces the EM signal strength by 3 to 6 dB.

As a result, one or more low noise amplifiers (LNAs) **1121** and **1124***a*-**1124***n* are provided upstream of the one or more filters **1123** and **1122***a*-**1122***n*. The LNAs and filters can be in reversed order. The LNAs compensate for losses in the mixers **1118**, the filters **1122** and **1123**, and other components by increasing the EM signal strength prior to filtering and mixing. Typically, for example, each LNA contributes 15 to 20 dB of amplification.

However, LNAs require substantial power to operate. Higher frequency LNAs require more power than lower frequency LNAs.

When the receiver system **1102** is intended to be portable, such as a cellular telephone receiver, for example, the LNAs require a substantial portion of the total power.

At higher frequencies, impedance mismatches between the various stages further reduce the strength of the EM signal **1104**. In order to optimize power transferred through the receiver system **1102**, each component should be impedance matched with adjacent components. Since no two components have the exact same impedance characteristics, even for components that were manufactured with high tolerances, impedance matching must often be individually fine tuned for each receiver system **1102**. As a result, impedance matching in conventional receivers tends to be labor intensive and more art than science. Impedance matching requires a significant amount of added time and expense to both the design and manufacture of conventional receivers. Since many of the components, such as LNA, filters, and impedance matching circuits, are highly frequency dependent, a receiver designed for one application is generally not suitable for other applications. Instead, a new receiver must be designed, which requires new impedance matching circuits between many of the components.

Conventional receiver components are typically positioned over multiple IC substrates instead of on a single IC substrate. This is partly because there is no single substrate that is optimal for both RF, IF, and baseband frequencies. Other factors may include the sheer number of components, their various sizes and different inherent impedance characteristics, etc. Additional signal amplification is often required when going from chip to chip. Implementation over multiple substrates thus involves many costs in addition to the cost of the ICs themselves.

Conventional receivers thus require many components, are difficult and time consuming to design and manufacture, and require substantial external power to maintain sufficient signal levels. Conventional receivers are thus expensive to design, build, and use.

In an embodiment, the present invention is implemented to replace many, if not all, of the components between the antenna **1106** and the signal processor **1110**, with an aliasing module that includes a universal frequency translator (UFT) module. (More generally, the phrase "universal frequency translator," "universal frequency translation," "UFT," "UFT transform," and "UFT technology" (or similar phrases) are used herein to refer to the frequency translation technology/concepts described herein.) The UFT is able to down-convert a wide range of EM signal frequencies using very few components. The UFT is easy to design and build, and requires very little external power. The UFT design can be easily tailored for different frequencies or frequency ranges. For example, UFT design can be easily impedance matched with relatively little tuning. In a direct-to-data embodiment of the invention, where an EM signal is directly down-converted to a demodulated baseband signal, the invention also eliminates the need for a demodulator in the signal processor **1110**.

When the invention is implemented in a receiver system, such as the receiver system **1102**, power consumption is significantly reduced and signal to noise ratio is significantly increased.

In an embodiment, the invention can be implemented and tailored for specific applications with easy to calculate and easy to implement impedance matching circuits. As a result, when the invention is implemented as a receiver, such as the receiver **1102**, specialized impedance matching experience is not required.

In conventional receivers, components in the IF sections comprise roughly eighty to ninety percent of the total components of the receivers. The UFT design eliminates the IF section(s) and thus eliminates the roughly eighty to ninety percent of the total components of conventional receivers.

Other advantages of the invention include, but are not limited to:

The invention can be implemented as a receiver with only a single local oscillator;

The invention can be implemented as a receiver with only a single, lower frequency, local oscillator;

The invention can be implemented as a receiver using few filters;

The invention can be implemented as a receiver using unit delay filters;

The invention can be implemented as a receiver that can change frequencies and receive different modulation formats with no hardware changes;

The invention can be also be implemented as frequency up-converter in an EM signal transmitter;

The invention can be also be implemented as a combination up-converter (transmitter) and down-converter (receiver), referred to herein as a transceiver;

The invention can be implemented as a method and system for ensuring reception of a communications signal, as disclosed in co-pending patent application titled, "Method and System for Ensuring Reception of a Communications Signal," Ser. No. 09/176,415 (now U.S. Pat. No. 6,091,940), incorporated herein by reference in its entirety;

The invention can be implemented in a differential configuration, whereby signal to noise ratios are increased;

A receiver designed in accordance with the invention can be implemented on a single IC substrate, such as a silicon-based IC substrate;

A receiver designed in accordance with the invention and implemented on a single IC substrate, such as a silicon-based IC substrate, can down-convert EM signals from frequencies in the giga Hertz range;

A receiver built in accordance with the invention has a relatively flat response over a wide range of frequencies. For example, in an embodiment, a receiver built in accordance with the invention to operate around 800 MHZ has a substantially flat response (i.e., plus or minus a few dB of power) from 100 MHZ to 1 GHZ. This is referred to herein as a wide-band receiver; and

A receiver built in accordance with the invention can include multiple, user-selectable, Impedance match modules, each designed for a different wide-band of frequencies, which can be used to scan an ultra-wide-band of frequencies.

II. DOWN-CONVERTING BY UNDER-SAMPLING

1. Down-Converting an EM Carrier Signal to an EM Intermediate Signal by Under-Sampling the EM Carrier Signal at the Aliasing Rate

In an embodiment, the invention down-converts an EM signal to an IF signal by under-sampling the EM signal. This embodiment is illustrated by **4508** in FIG. **45**B.

This embodiment can be implemented with modulated and unmodulated EM signals. This embodiment is described herein using the modulated carrier signal F_{MC} in FIG. **1**, as an example. In the example, the modulated carrier signal F_{MC} is down-converted to an IF signal F_{IF}. The IF signal F_{IF} can then be demodulated, with any conventional demodulation technique to obtain a demodulated baseband signal F_{DMB}. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention can be implemented to down-convert any EM signal, including but not limited to, modulated carrier signals and unmodulated carrier signals.

The following sections describe example methods for down-converting the modulated carrier signal F_{MC} to the IF signal F_{IF}, according to embodiments of the invention. Exemplary structural embodiments for implementing the methods are also described. It should be understood that the invention is not limited to the particular embodiments described below. Equivalents, extensions, variations, deviations, etc., of the following will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such equivalents, extensions, variations, deviations, etc., are within the scope and spirit of the present invention.

The following sections include a high level discussion, example embodiments, and implementation examples.

1.1 High Level Description

This section (including its subsections) provides a high-level description of down-converting an EM signal to an IF signal F_{IF}, according to an embodiment of the invention. In particular, an operational process of under-sampling a modulated carrier signal F_{MC} to down-convert it to the IF signal F_{IF}, is described at a high-level. Also, a structural implementation for implementing this process is described at a high-level. This structural implementation is described herein for illustrative purposes, and is not limiting. In particular, the process described in this section can be achieved using any number of structural implementations, one of which is described in this section. The details of such structural implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

1.1.1 Operational Description

FIG. **14**B depicts a flowchart **1407** that illustrates an exemplary method for under-sampling an EM signal to down-convert the EM signal to an intermediate signal F_{IF}. The exemplary method illustrated in the flowchart **1407** is an embodiment of the flowchart **1401** in FIG. **14**A.

Any and all combinations of modulation techniques are valid for this invention. For ease of discussion, the digital AM carrier signal **616** is used to illustrate a high level operational description of the invention. Subsequent sections provide detailed flowcharts and descriptions for AM, FM and PM example embodiments. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention can be implemented to down-convert any type of EM signal, including any form of modulated carrier signal and unmodulated carrier signals.

The method illustrated in the flowchart **1407** is now described at a high level using the digital AM carrier signal **616** of FIG. **6**C. The digital AM carrier signal **616** is re-illustrated in FIG. **15**A for convenience. FIG. **15**E illustrates a portion **1510** of the AM carrier signal **616**, between time t1 and t2, on an expanded time scale.

The process begins at step **1408**, which includes receiving an EM signal. Step **1408** is represented by the digital AM carrier signal **616**.

Step **1410** includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. **5**B illustrates an example under-sampling signal **1502**, which includes a train of pulses **1504** having negligible apertures that tend toward zero time in duration. The pulses **1504** repeat at the aliasing rate, or pulse repetition rate. Aliasing rates are discussed below.

Step **1412** includes under-sampling the EM signal at the aliasing rate to down-convert the EM signal to the intermediate signal F_{IF}. When down-converting an EM signal to an IF signal, the frequency or aliasing rate of the pulses **1504** sets the IF.

FIG. **15**C illustrates a stair step AM intermediate signal **1506**, which is generated by the down-conversion process. The AM intermediate signal **1506** is similar to the AM carrier signal **616** except that the AM intermediate signal **1506** has a lower frequency than the AM carrier signal **616**. The AM carrier signal **616** has thus been down-converted to the AM intermediate signal **1506**. The AM intermediate signal **1506** can be generated at any frequency below the frequency of the AM carrier signal **616** by adjusting the aliasing rate.

FIG. **15**D depicts the AM intermediate signal **1506** as a filtered output signal **1508**. In an alternative embodiment, the invention outputs a stair step, non-filtered or partially filtered output signal. The choice between filtered, partially filtered and non-filtered output signals is generally a design choice that depends upon the application of the invention.

The intermediate frequency of the down-converted signal F_{IF}, which in this example is the AM intermediate signal **1506**, can be determined from EQ. (2), which is reproduced below for convenience.

$$F_C = n \cdot F_{AR} \pm F_{IF} \quad \text{EQ. (2)}$$

A suitable aliasing rate F_{AR} can be determined in a variety of ways. An example method for determining the aliasing rate F_{AR}, is provided below. After reading the description herein, one skilled in the relevant art(s) will understand how to determine appropriate aliasing rates for EM signals, including ones in addition to the modulated carrier signals specifically illustrated herein.

In FIG. **17**, a flowchart **1701** illustrates an example process for determining an aliasing rate F_{AR}. But a designer may choose, or an application may dictate, that the values be determined in an order that is different than the illustrated order. The process begins at step **1702**, which includes determining, or selecting, the frequency of the EM signal. The frequency of the FM carrier signal **616** can be, for example, 901 MHZ.

Step **1704** includes determining, or selecting, the intermediate frequency. This is the frequency to which the EM signal will be down-converted. The intermediate frequency can be determined, or selected, to match a frequency requirement of a down-stream demodulator. The intermediate frequency can be, for example, 1 MHZ.

Step **1706** includes determining the aliasing rate or rates that will down-convert the EM signal to the IF specified in step **1704**.

EQ. (2) can be rewritten as EQ. (3):

$$n \cdot F_{AR} = F_C \pm F_{IF} \quad \text{EQ. (3)}$$

Which can be rewritten as EQ. (4):

$$n = \frac{F_C \pm F_{IF}}{F_{AR}} \quad \text{EQ. (4)}$$

or as EQ. (5):

$$F_{AR} = \frac{F_C \pm F_{IF}}{n} \quad \text{EQ. (5)}$$

$(F_C \pm F_{IF})$ can be defined as a difference value F_{DIFF}, as illustrated in EQ. (6):

$$(F_C \pm F_{IF}) = F_{DIFF} \quad \text{EQ. (6)}$$

EQ. (4) can be rewritten as EQ. (7):

$$n = \frac{F_{DIFF}}{F_{AR}} \quad \text{EQ. (7)}$$

From EQ. (7), it can be seen that, for a given n and a constant F_{AR}, F_{DIFF} is constant. For the case of $F_{DIFF}=F_C-F_{IF}$, and for a constant F_{DIFF}, as F_C increases, F_{IF} necessarily increases. For the case of $F_{DIFF}=F_C+F_{IF}$, and for a constant F_{DIFF}, as F_C increases, F_{IF} necessarily decreases. In the latter case of $F_{DIFF}=F_C+F_{IF}$, any phase or frequency changes on F_C correspond to reversed or inverted phase or frequency changes on F_{IF}. This is mentioned to teach the reader that $F_{DIFF}=F_C-F_{IF}$, is used, the above effect will affect the phase and frequency response of the modulated intermediate signal F_{IF}.

EQs. (2) through (7) can be solved for any valid n. A suitable n can be determined for any given difference frequency F_{DIFF} and for any desired aliasing rate $F_{AR(Desired)}$. EQs. (2) through (7) can be utilized to identify a specific harmonic closest to a desired aliasing rate $F_{AR(Desired)}$ that will generate the desired intermediate signal F_{IF}.

An example is now provided for determining a suitable n for a given difference frequency F_{DIFF} and for a desired aliasing rate $F_{AR(Desired)}$. For ease of illustration, only the case of (F_C-F_{IF}) is illustrated in the example below.

$$n = \frac{F_C - F_{IF}}{F_{AR(Desired)}} = \frac{F_{DIFF}}{F_{AR(Desired)}}$$

The desired aliasing rate $F_{AR(DESIRED)}$ can be, for example, 140 MHZ. Using the previous examples, where the carrier frequency is 901 MHZ and the IF is 1 MHZ, an initial value of n is determined as:

$$n = \frac{901\ \text{MHZ} - 1\ \text{MHZ}}{140\ \text{MHZ}} = \frac{900}{140} = 6.4$$

The initial value 6.4 can be rounded up or down to the valid nearest n, which was defined above as including (0.5, 1, 2, 3, . . .). In this example, 6.4 is rounded down to 6.0, which is inserted into EQ. (5) for the case of $(F_C-F_{IF})=F_{DIFF}$.:

$$F_{AR} = \frac{F_C - F_{IF}}{n}$$

$$F_{AR} = \frac{901\ \text{MHZ} - 1\ \text{MHZ}}{n} = \frac{900\ \text{MHZ}}{n} = 150\ \text{MHZ}$$

In other words, under-sampling a 901 MHZ EM carrier signal at 150 MHZ generates an intermediate signal at 1 MHZ. When the under-sampled EM carrier signal is a modulated carrier signal, the intermediate signal will also substantially include the modulation. The modulated intermediate signal can be demodulated through any conventional demodulation technique.

Alternatively, instead of starting from a desired aliasing rate, a list of suitable aliasing rates can be determined from the modified form of EQ. (5), by solving for various values of n. Example solutions are listed below.

$$F_{AR} = \frac{(F_C - F_{IF})}{n} = \frac{F_{DIFF}}{n} = \frac{901\ \text{MHZ} - 1\ \text{MHZ}}{n} = \frac{900\ \text{MHZ}}{n}$$

Solving for n=0.5, 1, 2, 3, 4, 5 and 6:

900 MHZ/0.5=1.8 GHZ (i.e., second harmonic, illustrated in FIG. **25**A as **2502**);

900 MHZ/1=900 MHZ (i.e., fundamental frequency, illustrated in FIG. **25**B as **2504**);

900 MHZ/2=450 MHZ (i.e., second sub-harmonic, illustrated in FIG. **25**C as **2506**);

900 MHZ/2=300 MHZ (i.e., third sub-harmonic, illustrated in FIG. **25**D as **2508**);

900 MHZ/4=225 MHZ (i.e., fourth sub-harmonic, illustrated in FIG. **25**E as **2510**);

900 MHZ/5=180 MHZ (i.e., fifth sub-harmonic, illustrated in FIG. **25**F as **2512**); and

900 MHZ/6=150 MHZ (i.e., sixth sub-harmonic, illustrated in FIG. **250** as **2514**).

The steps described above can be performed for the case of (F_C+F_{IF}) in a similar fashion. The results can be compared to the results obtained from the case of (F_C−F_{IF}) to determine which provides better result for an application.

In an embodiment, the invention down-converts an EM signal to a relatively standard IF in the range of, for example, 100 KHZ to 200 MHZ. In another embodiment, referred to herein as a small off-set implementation, the invention down-converts an EM signal to a relatively low frequency of, for example, less than 100 KHZ. In another embodiment, referred to herein as a large off-set implementation, the invention down-converts an EM signal to a relatively higher IF signal, such as, for example, above 200 MHZ.

The various off-set implementations provide selectivity for different applications. Generally, lower data rate applications can operate at lower intermediate frequencies. But higher intermediate frequencies can allow more information to be supported for a given modulation technique.

In accordance with the invention, a designer picks an optimum information bandwidth for an application and an optimum intermediate frequency to support the baseband signal. The intermediate frequency should be high enough to support the bandwidth of the modulating baseband signal F_{MB}.

Generally, as the aliasing rate approaches a harmonic or sub-harmonic frequency of the EM signal, the frequency of the down-converted IF signal decreases. Similarly, as the aliasing rate moves away from a harmonic or sub-harmonic frequency of the EM signal, the IF increases.

Aliased frequencies occur above and below every harmonic of the aliasing frequency. In order to avoid mapping other aliasing frequencies in the band of the aliasing frequency (IF) of interest, the IF of interest is preferably not near one half the aliasing rate.

As described in example implementations below, an aliasing module, including a universal frequency translator (UFT) module built in accordance with the invention, provides a wide range of flexibility in frequency selection and can thus be implemented in a wide range of applications. Conventional systems cannot easily offer, or do not allow, this level of flexibility in frequency selection.

1.1.2 Structural Description

FIG. **16** illustrates a block diagram of an under-sampling system **1602** according to an embodiment of the invention. The under-sampling system **1602** is an example embodiment of the generic aliasing system **1302** in FIG. **13**. The under-sampling system **1602** includes an under-sampling module **1606**. The under-sampling module **1606** receives the EM signal **1304** and an under-sampling signal **1604**, which includes under-sampling pulses having negligible apertures that tend towards zero time, occurring at a frequency equal to the aliasing rate F_{AR}. The under-sampling signal **1604** is an example embodiment of the aliasing signal **1310**. The under-sampling module **1606** under-samples the EM signal **1304** at the aliasing rate F_{AR} of the under-sampling signal **1604**. The under-sampling system **1602** outputs a down-converted signal **1308**A.

Preferably, the under-sampling module **1606** under-samples the EM signal **1304** to down-convert it to the intermediate signal F_{IF} in the manner shown in the operational flowchart **1407** of FIG. **14**B. But it should be understood that the scope and spirit of the invention includes other structural embodiments for performing the steps of the flowchart **1407**. The specifics of the other structural embodiments will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein. In an embodiment, the aliasing rate F_{AR} of the under-sampling signal **1604** is chosen in the manner discussed in Section II.1.1.1 so that the under-sampling module **1606** under-samples the EM carrier signal **1304** generating the intermediate frequency F_{IF}.

The operation of the under-sampling system **1602** is now described with reference to the flowchart **1407** and to the timing diagrams in FIGS. **15**A-D. In step **1408**, the under-sampling module **1606** receives the AM signal **616** (FIG. **15**A). In step **1410**, the under-sampling module **1606** receives the under-sampling signal **1502** (FIG. **15**B). In step **1412**, the under-sampling module **1606** under-samples the AM carrier signal **616** at the aliasing rate of the under-sampling signal **1502**, or a multiple thereof, to down-convert the AM carrier signal **616** to the intermediate signal **1506** (FIG. **15**D).

Example implementations of the under-sampling module **1606** are provided in Sections 4 and 5 below.

1.2 Example Embodiments

Various embodiments related to the method(s) and structures) described above are presented in this section (and its subsections). These embodiments are described herein for purposes of illustration, and not limitation. The invention is not limited to these embodiments. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

The method for down-converting the EM signal **1304** to the intermediate signal F_{IF}, illustrated in the flowchart **1407** of FIG. **14**B, can be implemented with any type of EM signal, including unmodulated EM carrier signals and modulated carrier signals including, but not limited to, AM, FM, PM, etc., or any combination thereof. Operation of the flowchart **1407** of FIG. **14**B is described below for AM, FM and PM carrier signals. The exemplary descriptions below are intended to facilitate an understanding of the present invention. The present invention is not limited to or by the exemplary embodiments below.

1.2.1 First Example Embodiment: Amplitude Modulation

1.2.1.1 Operational Description

Operation of the exemplary process of the flowchart **1407** in FIG. **14**B is described below for the analog AM carrier signal **516**, illustrated in FIG. **5**C, and for the digital AM carrier signal **616**, illustrated in FIG. **6**C.

1.2.1.1.1 Analog AM Carrier Signal

A process for down-converting the analog AM carrier signal **516** in FIG. **5**C to an analog AM intermediate signal is now described with reference to the flowchart **1407** in FIG. **14**B. The analog AM carrier signal **516** is re-illustrated in FIG. **19**A for convenience. For this example, the analog AM carrier signal **516** oscillates at approximately 901 MHZ. In FIG. **19**B, an analog AM carrier signal **1904** illustrates a portion of the analog AM carrier signal **516** on an expanded time scale.

The process begins at step **1408**, which includes receiving the EM signal. This is represented by the analog AM carrier signal **516** in FIG. **19**A.

Step **1410** includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. **19**C illustrates an example under-sampling signal **1906** on approximately the same time scale as FIG. **19**B. The under-sampling signal **1906** includes a train of pulses **1907** having negligible apertures that tend towards zero time in duration. The pulses **1907** repeat at the aliasing rate, or pulse repetition rate, which is determined or selected as previously described. Generally, when down-converting to an intermediate signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-

harmonic of the difference frequency F_{DIFF}. For this example, the aliasing rate is approximately 450 MHZ.

Step **1412** includes under-sampling the EM signal at the aliasing rate to down-convert the EM signal to the intermediate signal F_{IF}. Step **1412** is illustrated in FIG. **19**B by under-sample points **1905**.

Because a harmonic of the aliasing rate is off-set from the AM carrier signal **516**, the under-sample points **1905** "walk through" the analog AM carrier signal **516**. In this example, the under-sample points **1905** "walk through" the analog AM carrier signal **516** at approximately a one megahertz rate. In other words, the under-sample points **1905** occur at different locations on subsequent cycles of the AM carrier signal **516**. As a result, the under-sample points **1905** capture varying amplitudes of the analog AM signal **516**. For example, under-sample point **1905**A has a larger amplitude than under-sample point **1905**B.

In FIG. **19**D, the under-sample points **1905** correlate to voltage points **1908**. In an embodiment, the voltage points **1908** form an analog AM intermediate signal **1910**. This can be accomplished in many ways. For example, each voltage point **1908** can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as discussed below.

In FIG. **19**E, an AM intermediate signal **1912** represents the AM intermediate signal **1910**, after filtering, on a compressed time scale. Although FIG. **19**E illustrates the AM intermediate signal **1912** as a filtered output signal, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications.

The AM intermediate signal **1912** is substantially similar to the AM carrier signal **516**, except that the AM intermediate signal **1912** is at the 1 MHZ intermediate frequency. The AM intermediate signal **1912** can be demodulated through any conventional AM demodulation technique.

The drawings referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the AM intermediate signal **1910** in FIG. **19**D and the AM intermediate signal **1912** in FIG. **19**E illustrate that the AM carrier signal **516** was successfully down-converted to an intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.1.1.2 Digital AM Carrier Signal

A process for down-converting the digital AM carrier signal **616** in FIG. **6**C to a digital AM intermediate signal is now described with reference to the flowchart **1407** in FIG. **14**B. The digital AM carrier signal **616** is re-illustrated in FIG. **18**A for convenience. For this example, the digital AM carrier signal **616** oscillates at approximately 901 MHZ. In FIG. **18**B, an AM carrier signal **1804** illustrates a portion of the AM signal **616**, from time t0 to t1, on an expanded time scale.

The process begins at step **1408**, which includes receiving an EM signal. This is represented by the AM signal **616** in FIG. **18**A.

Step **1410** includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. **18**C illustrates an example under-sampling signal **1806** on approximately the same time scale as FIG. **18**B. The under-sampling signal **1806** includes a train of pulses **1807** having negligible apertures that tend towards zero time in duration. The pulses **1807** repeat at the aliasing rate, or pulse repetition rate, which is determined or selected as previously described. Generally, when down-converting to an intermediate signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency F_{DIFF}. For this example, the aliasing rate is approximately 450 MHZ.

Step **1412** includes under-sampling the EM signal at the aliasing rate to down-convert the EM signal to the intermediate signal F_{IF}. Step **1412** is illustrated in FIG. **18**B by under-sample points **1805**.

Because a harmonic of the aliasing rate is off-set from the AM carrier signal **616**, the under-sample points **1805** walk through the AM carrier signal **616**. In other words, the under-sample points **1805** occur at different locations of subsequent cycles of the AM signal **616**. As a result, the under-sample points **1805** capture various amplitudes of the AM signal **616**. In this example, the under-sample points **1805** walk through the AM carrier signal **616** at approximately a 1 MHZ rate. For example, under-sample point **1805**A has a larger amplitude than under-sample point **1805**B.

In FIG. **18**D, the under-sample points **1805** correlate to voltage points **1808**. In an embodiment, the voltage points **1805** form an AM intermediate signal **1810**. This can be accomplished in many ways. For example, each voltage point **1808** can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as discussed below.

In FIG. **18**E, an AM intermediate signal **1812** represents the AM intermediate signal **1810**, after filtering, on a compressed time scale. Although FIG. **18**E illustrates the AM intermediate signal **1812** as a filtered output signal, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications.

The AM intermediate signal **1812** is substantially similar to the AM carrier signal **616**, except that the AM intermediate signal **1812** is at the 1 MHZ intermediate frequency. The AM intermediate signal **1812** can be demodulated through any conventional AM demodulation technique.

The drawings referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the AM intermediate signal **1810** in FIG. **18**D and the AM intermediate signal **1812** in FIG. **18**E illustrate that the AM carrier signal **616** was successfully down-converted to an intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.1.2 Structural Description

The operation of the under-sampling system **1602** is now described for the analog AM carrier signal **516**, with reference to the flowchart **1407** and to the timing diagrams of FIGS. **19**A-E. In step **1408**, the under-sampling module **1606** receives the AM carrier signal **516** (FIG. **19**A). In step **1410**, the under-sampling module **1606** receives the under-sampling signal **1906** (FIG. **19**C). In step **1412**, the under-sampling module **1606** under-samples the AM carrier signal **516** at the aliasing rate of the under-sampling signal **1906** to down-convert it to the AM intermediate signal **1912** (FIG. **19**E).

The operation of the under-sampling system **1602** is now described for the digital AM carrier signal **616**, with reference to the flowchart **1407** and to the timing diagrams of FIGS. **18**A-E. In step **1408**, the under-sampling module **1606** receives the AM carrier signal **616** (FIG. **18**A). In step **1410**, the under-sampling module **1606** receives the under-sampling signal **1806** (FIG. **18**C). In step **1412**, the under-sampling module **1606** under-samples the AM carrier signal **616** at the aliasing rate of the under-sampling signal **1806** to down-convert it to the AM intermediate signal **1812** (FIG. **18**E).

Example implementations of the under-sampling module **1606** are provided in Sections 4 and 5 below.

1.2.2 Second Example Embodiment: Frequency Modulation

1.2.2.1 Operational Description

Operation of the exemplary process of the flowchart **1407** in FIG. **14**B is described below for the analog FM carrier signal **716**, illustrated in FIG. **7**C, and for the digital FM carrier signal **816**, illustrated in FIG. **8**C.

1.2.2.1.1 Analog FM Carrier Signal

A process for down-converting the analog FM carrier signal **716** to an analog FM intermediate signal is now described with reference to the flowchart **1407** in FIG. **14**B. The analog FM carrier signal **716** is re-illustrated in FIG. **20**A for convenience. For this example, the analog FM carrier signal **716** oscillates at approximately 901 MHZ. In FIG. **20**B, an FM carrier signal **2004** illustrates a portion of the analog FM carrier signal **716**, from time t1 to t3, on an expanded time scale.

The process begins at step **1408**, which includes receiving an EM signal. This is represented in FIG. **20**A by the FM carrier signal **716**.

Step **1410** includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. **20**C illustrates an example under-sampling signal **2006** on approximately the same time scale as FIG. **20**B. The under-sampling signal **2006** includes a train of pulses **2007** having negligible apertures that tend towards zero time in duration. The pulses **2007** repeat at the aliasing rate or pulse repetition rate, which is determined or selected as previously described. Generally, when down-converting to an intermediate signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency F_{DIFF}. For this example, where the FM carrier signal **716** is centered around 901 MHZ, the aliasing rate is approximately 450 MHZ.

Step **1412** includes under-sampling the EM signal at the aliasing rate to down-convert the EM signal to the intermediate signal F_{IF}. Step **1412** is illustrated in FIG. **20**B by under-sample points **2005**.

Because a harmonic of the aliasing rate is off-set from the FM carrier signal **716**, the under-sample points **2005** occur at different locations of subsequent cycles of the under-sampled signal **716**. In other words, the under-sample points **2005** walk through the signal **716**. As a result, the under-sample points **2005** capture various amplitudes of the FM carrier signal **716**.

In FIG. **20**D, the under-sample points **2005** correlate to voltage points **2008**. In an embodiment, the voltage points **2005** form an analog FM intermediate signal **2010**. This can be accomplished in many ways. For example, each voltage point **2008** can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as discussed below.

In FIG. **20**E, an FM intermediate signal **2012** illustrates the FM intermediate signal **2010**, after filtering, on a compressed time scale. Although FIG. **20**E illustrates the FM intermediate signal **2012** as a filtered output signal, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications.

The FM intermediate signal **2012** is substantially similar to the FM carrier signal **716**, except that the FM intermediate signal **2012** is at the 1 MHZ intermediate frequency. The FM intermediate signal **2012** can be demodulated through any conventional FM demodulation technique.

The drawings referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the FM intermediate signal **2010** in FIG. **20**D and the FM intermediate signal **2012** in FIG. **20**E illustrate that the FM carrier signal **716** was successfully down-converted to an intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.2.1.2 Digital FM Carrier Signal

A process for down-converting the digital FM carrier signal **816** to a digital FM intermediate signal is now described with reference to the flowchart **1407** in FIG. **14**B. The digital FM carrier signal **816** is re-illustrated in FIG. **21**A for convenience. For this example, the digital FM carrier signal **816** oscillates at approximately 901 MHZ. In FIG. **21**B, an FM carrier signal **2104** illustrates a portion of the FM carrier signal **816**, from time t1 to t3, on an expanded time scale.

The process begins at step **1408**, which includes receiving an EM signal. This is represented in FIG. **21**A, by the FM carrier signal **816**.

Step **1410** includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. **21**C illustrates an example under-sampling signal **2106** on approximately the same time scale as FIG. **21**B. The under-sampling signal **2106** includes a train of pulses **2107** having negligible apertures that tend toward zero time in duration. The pulses **2107** repeat at the aliasing rate, or pulse repetition rate, which is determined or selected as previously described. Generally, when down-converting to an intermediate signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency F_{DIFF}. In this example, where the FM carrier signal **816** is centered around 901 MHZ, the aliasing rate is selected as approximately 450 MHZ, which is a sub-harmonic of 900 MHZ, which is off-set by 1 MHZ from the center frequency of the FM carrier signal **816**.

Step **1412** includes under-sampling the EM signal at the aliasing rate to down-convert the EM signal to an intermediate signal F_{IF}. Step **1412** is illustrated in FIG. **21**B by under-sample points **2105**.

Because a harmonic of the aliasing rate is off-set from the FM carrier signal **816**, the under-sample points **2105** occur at different locations of subsequent cycles of the FM carrier signal **816**. In other words, the under-sample points **2105** walk through the signal **816**. As a result, the under-sample points **2105** capture various amplitudes of the signal **816**.

In FIG. **21**D, the under-sample points **2105** correlate to voltage points **2108**. In an embodiment, the voltage points **2108** form a digital FM intermediate signal **2110**. This can be accomplished in many ways. For example, each voltage point **2108** can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as described below.

In FIG. **21**E, an FM intermediate signal **2112** represents the FM intermediate signal **2110**, after filtering, on a compressed time scale. Although FIG. **21**E illustrates the FM intermediate signal **2112** as a filtered output signal, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications.

The FM intermediate signal **2112** is substantially similar to the FM carrier signal **816**, except that the FM intermediate signal **2112** is at the 1 MHZ intermediate frequency. The FM intermediate signal **2112** can be demodulated through any conventional FM demodulation technique.

The drawings referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the FM intermediate signal **2110** in FIG. **21**D and the FM inter-

mediate signal **2112** in FIG. **21**E illustrate that the FM carrier signal **816** was successfully down-converted to an intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.2.2 Structural Description

The operation of the under-sampling system **1602** is now described for the analog FM carrier signal **716**, with reference to the flowchart **1407** and the timing diagrams of FIGS. **20**A-E. In step **1408**, the under-sampling module **1606** receives the FM carrier signal **716** (FIG. **20**A). In step **1410**, the under-sampling module **1606** receives the under-sampling signal **2006** (FIG. **20**C). In step **1412**, the under-sampling module **1606** under-samples the FM carrier signal **716** at the aliasing rate of the under-sampling signal **2006** to down-convert the FM carrier signal **716** to the FM intermediate signal **2012** (FIG. **20**E).

The operation of the under-sampling system **1602** is now described for the digital FM carrier signal **816**, with reference to the flowchart **1407** and the timing diagrams of FIGS. **21**A-E. In step **1408**, the under-sampling module **1606** receives the FM carrier signal **816** (FIG. **21**A). In step **1410**, the under-sampling module **1606** receives the under-sampling signal **2106** (FIG. **21**C). In step **1412**, the under-sampling module **1606** under-samples the FM carrier signal **816** at the aliasing rate of the under-sampling signal **2106** to down-convert the FM carrier signal **816** to the FM intermediate signal **2112** (FIG. **21**E).

Example implementations of the under-sampling module **1606** are provided in Sections 4 and 5 below.

1.2.3 Third Example Embodiment: Phase Modulation

1.2.3.1 Operational Description

Operation of the exemplary process of the flowchart **1407** in FIG. **14**B is described below for the analog PM carrier signal **916**, illustrated in FIG. **9**C, and for the digital PM carrier signal **1016**, illustrated in FIG. **10**C.

1.2.3.1.1 Analog PM Carrier Signal

A process for down-converting the analog PM carrier signal **916** to an analog PM intermediate signal is now described with reference to the flowchart **1407** in FIG. **14**B. The analog PM carrier signal **916** is re-illustrated in FIG. **23**A for convenience. For this example, the analog PM carrier signal **916** oscillates at approximately 901 MHZ. In FIG. **23**B, a PM carrier signal **2304** illustrates a portion of the analog PM carrier signal **916**, from time t1 to t3, on an expanded time scale.

The process of down-converting the PM carrier signal **916** to a PM intermediate signal begins at step **1408**, which includes receiving an EM signal. This is represented in FIG. **23**A, by the analog PM carrier signal **916**.

Step **1410** includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. **23**C illustrates an example under-sampling signal **2306** on approximately the same time scale as FIG. **23**B. The under-sampling signal **2306** includes a train of pulses **2307** having negligible apertures that tend towards zero time in duration. The pulses **2307** repeat at the aliasing rate, or pulse repetition rate, which is determined or selected as previously described. Generally, when down-converting to an intermediate signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency F_{DIFF}. In this example, the aliasing rate is approximately 450 MHZ.

Step **1412** includes under-sampling the EM signal at the aliasing rate to down-convert the EM signal to the intermediate signal F_{IF}. Step **1412** is illustrated in FIG. **23**B by under-sample points **2305**.

Because a harmonic of the aliasing rate is off-set from the PM carrier signal **916**, the under-sample points **2305** occur at different locations of subsequent cycles of the PM carrier signal **916**. As a result, the under-sample points capture various amplitudes of the PM carrier signal **916**.

In FIG. **23**D, voltage points **2308** correlate to the under-sample points **2305**. In an embodiment, the voltage points **2308** form an analog PM intermediate signal **2310**. This can be accomplished in many ways. For example, each voltage point **2308** can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as described below.

In FIG. **23**E, an analog PM intermediate signal **2312** illustrates the analog PM intermediate signal **2310**, after filtering, on a compressed time scale. Although FIG. **23**E illustrates the PM intermediate signal **2312** as a filtered output signal, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications.

The analog PM intermediate signal **2312** is substantially similar to the analog PM carrier signal **916**, except that the analog PM intermediate signal **2312** is at the 1 MHZ intermediate frequency. The analog PM intermediate signal **2312** can be demodulated through any conventional PM demodulation technique.

The drawings referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the analog PM intermediate signal **2310** in FIG. **23**D and the analog PM intermediate signal **2312** in FIG. **23**E illustrate that the analog PM carrier signal **2316** was successfully down-converted to an intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.3.1.2 Digital PM Carrier Signal

A process for down-converting the digital PM carrier signal **1016** to a digital PM intermediate signal is now described with reference to the flowchart **1407** in FIG. **14**B. The digital PM carrier signal **1016** is re-illustrated in FIG. **22**A for convenience. For this example, the digital PM carrier signal **1016** oscillates at approximately 901 MHZ. In FIG. **22**B, a PM carrier signal **2204** illustrates a portion of the digital PM carrier signal **1016**, from time t1 to t3, on an expanded time scale.

The process begins at step **1408**, which includes receiving an EM signal. This is represented in FIG. **22**A by the digital PM carrier signal **1016**.

Step **1408** includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. **22**C illustrates example under-sampling signal **2206** on approximately the same time scale as FIG. **22**B. The under-sampling signal **2206** includes a train of pulses **2207** having negligible apertures that tend towards zero time in duration. The pulses **2207** repeat at the aliasing rate, or a pulse repetition rate, which is determined or selected as previously described. Generally, when down-converting to an intermediate signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency F_{DIFF}. In this example, the aliasing rate is approximately 450 MHZ.

Step **1412** includes under-sampling the EM signal at the aliasing rate to down-convert the EM signal to an intermediate signal F_{IF}. Step **1412** is illustrated in FIG. **22**B by under-sample points **2205**.

Because a harmonic of the aliasing rate is off-set from the PM carrier signal **1016**, the under-sample points **2205** occur at different locations of subsequent cycles of the PM carrier signal **1016**.

In FIG. **22**D, voltage points **2208** correlate to the under-sample points **2205**. In an embodiment, the voltage points **2208** form a digital analog PM intermediate signal **2210**. This

can be accomplished in many ways. For example, each voltage point **2208** can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as described below.

In FIG. **22**E, a digital PM intermediate signal **2212** represents the digital PM intermediate signal **2210** on a compressed time scale. Although FIG. **22**E illustrates the PM intermediate signal **2212** as a filtered output signal, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications.

The digital PM intermediate signal **2212** is substantially similar to the digital PM carrier signal **1016**, except that the digital PM intermediate signal **2212** is at the 1 MHZ intermediate frequency. The digital PM carrier signal **2212** can be demodulated through any conventional PM demodulation technique.

The drawings referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the digital PM intermediate signal **2210** in FIG. **22**D and the digital PM intermediate signal **2212** in FIG. **22**E illustrate that the digital PM carrier signal **1016** was successfully down-converted to an intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.3.2 Structural Description

The operation of the under-sampling system **1602** is now described for the analog PM carrier signal **916**, with reference to the flowchart **1407** and the timing diagrams of FIGS. **23**A-E. In step **1408**, the under-sampling module **1606** receives the PM carrier signal **916** (FIG. **23**A). In step **1410**, the under-sampling module **1606** receives the under-sampling signal **2306** (FIG. **23**C). In step **1412**, the under-sampling module **1606** under-samples the PM carrier signal **916** at the aliasing rate of the under-sampling signal **2306** to down-convert the PM carrier signal **916** to the PM intermediate signal **2312** (FIG. **23**E).

The operation of the under-sampling system **1602** is now described for the digital PM carrier signal **1016**, with reference to the flowchart **1407** and the timing diagrams of FIGS. **22**A-E. In step **1408**, the under-sampling module **1606** receives the PM carrier signal **1016** (FIG. **22**A). In step **1410**, the under-sampling module **1606** receives the under-sampling signal **2206** (FIG. **22**C). In step **1412**, the under-sampling module **1606** under-samples the PM carrier signal **1016** at the aliasing rate of the under-sampling signal **2206** to down-convert the PM carrier signal **1016** to the PM intermediate signal **2212** (FIG. **22**E).

Example implementations of the under-sampling module **1606** are provided in Sections 4 and 5 below.

1.2.4 Other Embodiments

The embodiments described above are provided for purposes of illustration. These embodiments are not intended to limit the invention. Alternate embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate embodiments fall within the scope and spirit of the present invention. Example implementations of the under-sampling module **1606** are provided in Sections 4 and 5 below.

1.3 Implementation Examples

Exemplary operational and/or structural implementations related to the method(s), structure(s), and/or embodiments described above are presented in Sections 4 and 5 below. The implementations are presented for purposes of illustration, and not limitation. The invention is not limited to the particular implementation examples described therein. Alternate implementations (including equivalents, extensions, variations, deviations, etc., of those described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

2. Directly Down-Converting an EM Signal to a Baseband Signal (Direct-to-Data)

In an embodiment, the invention directly down-converts an EM signal to a baseband signal, by under-sampling the EM signal. This embodiment is referred to herein as direct-to-data down-conversion and is illustrated in FIG. **45**B as **4510**.

This embodiment can be implemented with modulated and unmodulated EM signals. This embodiment is described herein using the modulated carrier signal F_{MC} in FIG. **1**, as an example. In the example, the modulated carrier signal F_{MC} is directly down-converted to the demodulated baseband signal F_{DMB}. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention is applicable to down-convert any EM signal, including but not limited to, modulated carrier signals and unmodulated carrier signals.

The following sections describe example methods for directly down-converting the modulated carrier signal F_{MC} to the demodulated baseband signal F_{DMB}. Exemplary structural embodiments for implementing the methods are also described. It should be understood that the invention is not limited to the particular embodiments described below. Equivalents, extensions, variations, deviations, etc., of the following will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such equivalents, extensions, variations, deviations, etc., are within the scope and spirit of the present invention.

The following sections include a high level discussion, example embodiments, and implementation examples.

2.1 High Level Description

This section (including its subsections) provides a high-level description of directly down-converting the modulated carrier signal F_{MC} to the demodulated baseband signal F_{DMB}, according to the invention. In particular, an operational process of directly down-converting the modulated carrier signal F_{MC} to the demodulated baseband signal F_{DMB} is described at a high-level. Also, a structural implementation for implementing this process is described at a high-level. The structural implementation is described herein for illustrative purposes, and is not limiting. In particular, the process described in this section can be achieved using any number of structural implementations, one of which is described in this section. The details of such structural implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

2.1.1 Operational Description

FIG. **14**C depicts a flowchart **1413** that illustrates an exemplary method for directly down-converting an EM signal to a demodulated baseband signal F_{DMB}. The exemplary method illustrated in the flowchart **1413** is an embodiment of the flowchart **1401** in FIG. **14**A.

Any and all combinations of modulation techniques are valid for this invention. For ease of discussion, the digital AM carrier signal **616** is used to illustrate a high level operational description of the invention. Subsequent sections provide detailed descriptions for AM and PM example embodiments. FM presents special considerations that are dealt with separately in Section II.3, below. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention can be implemented to down-convert any type of EM signal, including any form of modulated carrier signal and unmodulated carrier signals.

The method illustrated in the flowchart **1413** is now described at a high level using the digital AM carrier signal **616**, from FIG. **6**C. The digital AM carrier signal **616** is re-illustrated in FIG. **33**A for convenience.

The process of the flowchart **1413** begins at step **1414**, which includes receiving an EM signal. Step **1414** is represented by the digital AM carrier signal **616** in FIG. **33**A.

Step **1416** includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. **33**B illustrates an example under-sampling signal **3302** which includes a train of pulses **3303** having negligible apertures that tend towards zero time in duration. The pulses **3303** repeat at the aliasing rate or pulse repetition rate. The aliasing rate is determined in accordance with EQ. (2), reproduced below for convenience.

$$F_C = n \cdot F_{AR} \pm F_{IF} \quad \text{EQ. (2)}$$

When directly down-converting an EM signal to baseband (i.e., zero IF), EQ. (2) becomes:

$$F_C = n \cdot F_{AR} \quad \text{EQ. (8)}$$

Thus, to directly down-convert the AM signal **616** to a demodulated baseband signal, the aliasing rate is substantially equal to the frequency of the AM signal **616** or to a harmonic or sub-harmonic thereof. Although the aliasing rate is too low to permit reconstruction of higher frequency components of the AM signal **616** (i.e., the carrier frequency), it is high enough to permit substantial reconstruction of the lower frequency modulating baseband signal **310**.

Step **1418** includes under-sampling the EM signal at the aliasing rate to directly down-convert it to the demodulated baseband signal F_{DMB}. FIG. **33**C illustrates a stair step demodulated baseband signal **3304**, which is generated by the direct down-conversion process. The demodulated baseband signal **3304** is similar to the digital modulating baseband signal **310** in FIG. **3**.

FIG. **33**D depicts a filtered demodulated baseband signal **3306**, which can be generated from the stair step demodulated baseband signal **3304**. The invention can thus generate a filtered output signal, a partially filtered output signal, or a relatively unfiltered stair step output signal. The choice between filtered, partially filtered and non-filtered output signals is generally a design choice that depends upon the application of the invention.

2.1.2 Structural Description

FIG. **16** illustrates the block diagram of the under-sampling system **1602** according to an embodiment of the invention. The under-sampling system **1602** is an example embodiment of the generic aliasing system **1302** in FIG. **13**.

In a direct to data embodiment, the frequency of the under-sampling signal **1604** is substantially equal to a harmonic of the EM signal **1304** or, more typically, a sub-harmonic thereof Preferably, the under-sampling module **1606** under-samples the EM signal **1304** to directly down-convert it to the demodulated baseband signal F_{DMB}, in the manner shown in the operational flowchart **1413**. But it should be understood that the scope and spirit of the invention includes other structural embodiments for performing the steps of the flowchart **1413**. The specifics of the other structural embodiments will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

The operation of the aliasing system **1602** is now described for the digital AM carrier signal **616**, with reference to the flowchart **1413** and to the timing diagrams in FIGS. **33**A-D. In step **1414**, the under-sampling module **1606** receives the AM carrier signal **616** (FIG. **33**A). In step **1416**, the under-sampling module **1606** receives the under-sampling signal **3302** (FIG. **33**B). In step **1418**, the under-sampling module **1606** under-samples the AM carrier signal **616** at the aliasing rate of the under-sampling signal **3302** to directly down-convert the AM carrier signal **616** to the demodulated baseband signal **3304** in FIG. **33**C or the filtered demodulated baseband signal **3306** in FIG. **33**D.

Example implementations of the under-sampling module **1606** are provided in Sections 4 and 5 below.

2.2 Example Embodiments

Various embodiments related to the method(s) and structure(s) described above are presented in this section (and its subsections). These embodiments are described herein for purposes of illustration, and not limitation. The invention is not limited to these embodiments. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

The method for down-converting the EM signal **1304** to the demodulated baseband signal F_{DMB}, illustrated in the flowchart **1413** of FIG. **14**C, can be implemented with any type EM signal, including modulated carrier signals, including but not limited to, AM, PM, etc., or any combination thereof. Operation of the flowchart **1413** of FIG. **14**C is described below for AM and PM carrier signals. The exemplary descriptions below are intended to facilitate an understanding of the present invention. The present invention is not limited to or by the exemplary embodiments below.

2.2.1 First Example Embodiment: Amplitude Modulation

2.2.1.1 Operational Description

Operation of the exemplary process of the flowchart **1413** in FIG. **14**C is described below for the analog AM carrier signal **516**, illustrated in FIG. **5**C and for the digital AM carrier signal **616**, illustrated in FIG. **6**C.

2.2.1.1.1 Analog AM Carrier Signal

A process for directly down-converting the analog AM carrier signal **516** to a demodulated baseband signal is now described with reference to the flowchart **1413** in FIG. **14**C. The analog AM carrier signal **516** is re-illustrated in **35**A for convenience. For this example, the analog AM carrier signal **516** oscillates at approximately 900 MHZ. In FIG. **35**B, an analog AM carrier signal **3504** illustrates a portion of the analog AM carrier signal **516** on an expanded time scale.

The process begins at step **1414**, which includes receiving an EM signal. This is represented by the analog AM carrier signal **516**.

Step **1416** includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. **35**C illustrates an example under-sampling signal **3506** on approximately the same time scale as FIG. **35**B. The under-sampling signal **3506** includes a train of pulses **3507** having negligible apertures that tend towards zero time in duration. The pulses **3507** repeat at the aliasing rate or pulse repetition rate, which is determined or selected as previously described. Generally, when directly down-converting to a demodulated baseband signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the under-sampled signal. In this example, the aliasing rate is approximately 450 MHZ.

Step **1418** includes under-sampling the EM signal at the aliasing rate to directly down-convert it to the demodulated baseband signal F_{DMB}. Step **1418** is illustrated in FIG. **35**B by under-sample points **3505**. Because a harmonic of the aliasing rate is substantially equal to the frequency of the signal **516**, essentially no IF is produced. The only substantial aliased component is the baseband signal.

In FIG. **35**D, voltage points **3508** correlate to the under-sample points **3505**. In an embodiment, the voltage points

3508 form a demodulated baseband signal 3510. This can be accomplished in many ways. For example, each voltage point 3508 can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as described below.

In FIG. 35E, a demodulated baseband signal 3512 represents the demodulated baseband signal 3510, after filtering, on a compressed time scale. Although FIG. 35E illustrates the demodulated baseband signal 3512 as a filtered output signal, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications.

The demodulated baseband signal 3512 is substantially similar to the modulating baseband signal 210. The demodulated baseband signal 3512 can be processed using any signal processing technique(s) without further down-conversion or demodulation.

The aliasing rate of the under-sampling signal is preferably controlled to optimize the demodulated baseband signal for amplitude output and polarity, as desired.

In the example above, the under-sample points 3505 occur at positive locations of the AM carrier signal 516. Alternatively, the under-sample points 3505 can occur at other locations including negative points of the analog AM carrier signal 516. When the under-sample points 3505 occur at negative locations of the AM carrier signal 516, the resultant demodulated baseband signal is inverted relative to the modulating baseband signal 210.

The drawings referred to herein illustrate direct to data down-conversion in accordance with the invention. For example, the demodulated baseband signal 3510 in FIG. 35D and the demodulated baseband signal 3512 in FIG. 35E illustrate that the AM carrier signal 516 was successfully down-converted to the demodulated baseband signal 3510 by retaining enough baseband information for sufficient reconstruction.

2.2.1.1.2 Digital AM Carrier Signal

A process for directly down-converting the digital AM carrier signal 616 to a demodulated baseband signal is now described with reference to the flowchart 1413 in FIG. 14C. The digital AM carrier signal 616 is re-illustrated in FIG. 36A for convenience. For this example, the digital AM carrier signal 616 oscillates at approximately 901 MHZ. In FIG. 36B, a digital AM carrier signal 3604 illustrates a portion of the digital AM carrier signal 616 on an expanded time scale.

The process begins at step 1414, which includes receiving an EM signal. This is represented by the digital AM carrier signal 616.

Step 1416 includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. 36C illustrates an example under-sampling signal 3606 on approximately the same time scale as FIG. 36B. The under-sampling signal 3606 includes a train of pulses 3607 having negligible apertures that tend towards zero time in duration. The pulses 3607 repeat at the aliasing rate or pulse repetition rate, which is determined or selected as previously described. Generally, when directly down-converting to a demodulated baseband signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the under-sampled signal. In this example, the aliasing rate is approximately 450 MHZ.

Step 1418 includes under-sampling the EM signal at the aliasing rate to directly down-convert it to the demodulated baseband signal F_{DMB}. Step 1418 is illustrated in FIG. 36B by under-sample points 3605. Because the aliasing rate is substantially equal to the AM carrier signal 616, or to a harmonic or sub-harmonic thereof, essentially no IF is produced. The only substantial aliased component is the baseband signal.

In FIG. 36D, voltage points 3608 correlate to the under-sample points 3605. In an embodiment, the voltage points 3608 form a demodulated baseband signal 3610. This can be accomplished in many ways. For example, each voltage point 3608 can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as described below.

In FIG. 36E, a demodulated baseband signal 3612 represents the demodulated baseband signal 3610, after filtering, on a compressed time scale. Although FIG. 36E illustrates the demodulated baseband signal 3612 as a filtered output signal, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications.

The demodulated baseband signal 3612 is substantially similar to the digital modulating baseband signal 310. The demodulated analog baseband signal 3612 can be processed using any signal processing technique(s) without further down-conversion or demodulation.

The aliasing rate of the under-sampling signal is preferably controlled to optimize the demodulated baseband signal for amplitude output and polarity, as desired.

In the example above, the under-sample points 3605 occur at positive locations of signal portion 3604. Alternatively, the under-sample points 3605 can occur at other locations including negative locations of the signal portion 3604. When the under-sample points 3605 occur at negative points, the resultant demodulated baseband signal is inverted with respect to the modulating baseband signal 310.

The drawings referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the demodulated baseband signal 3610 in FIG. 36D and the demodulated baseband signal 3612 in FIG. 36E illustrate that the digital AM carrier signal 616 was successfully down-converted to the demodulated baseband signal 3610 by retaining enough baseband information for sufficient reconstruction.

2.2.1.2 Structural Description

The operation of the under-sampling module 1606 is now described for the analog AM carrier signal 516, with reference to the flowchart 1413 and the timing diagrams of FIGS. 35A-E. In step 1414, the under-sampling module 1606 receives the analog AM carrier signal 516 (FIG. 35A). In step 1416, the under-sampling module 1606 receives the under-sampling signal 3506 (FIG. 35C). In step 1418, the under-sampling module 1606 under-samples the analog AM carrier signal 516 at the aliasing rate of the under-sampling signal 3506 to directly to down-convert the AM carrier signal 516 to the demodulated analog baseband signal 3510 in FIG. 35D or to the filtered demodulated analog baseband signal 3512 in FIG. 35E.

The operation of the under-sampling system 1602 is now described for the digital AM carrier signal 616, with reference to the flowchart 1413 and the timing diagrams of FIGS. 36A-E. In step 1414, the under-sampling module 1606 receives the digital AM carrier signal 616 (FIG. 36A). In step 1416, the under-sampling module 1606 receives the under-sampling signal 3606 (FIG. 36C). In step 1418, the under-sampling module 1606 under-samples the digital AM carrier signal 616 at the aliasing rate of the under-sampling signal 3606 to down-convert the digital AM carrier signal 616 to the demodulated digital baseband signal 3610 in FIG. 36D or to the filtered demodulated digital baseband signal 3612 in FIG. 36E.

Example implementations of the under-sampling module **1606** are provided in Sections 4 and 5 below.

2.2.2 Second Example Embodiment: Phase Modulation

2.2.2.1 Operational Description

Operation of the exemplary process of the flowchart **1413** in FIG. **14**C is described below for the analog PM carrier signal **916**, illustrated in FIG. **9**C, and for the digital PM carrier signal **1016**, illustrated in FIG. **10**C.

2.2.2.1.1 Analog PM Carrier Signal

A process for directly down-converting the analog PM carrier signal **916** to a demodulated baseband signal is now described with reference to the flowchart **1413** in FIG. **14**C. The analog PM carrier signal **916** is re-illustrated in **37**A for convenience. For this example, the analog PM carrier signal **916** oscillates at approximately 900 MHZ. In FIG. **37**B, an analog PM carrier signal **3704** illustrates a portion of the analog PM carrier signal **916** on an expanded time scale.

The process begins at step **1414**, which includes receiving an EM signal. This is represented by the analog PM signal **916**.

Step **1416** includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. **37**C illustrates an example under-sampling signal **3706** on approximately the same time scale as FIG. **37**B. The under-sampling signal **3706** includes a train of pulses **3707** having negligible apertures that tend towards zero time in duration. The pulses **3707** repeat at the aliasing rate or pulse repetition rate, which is determined or selected as previously described. Generally, when directly down-converting to a demodulated baseband signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the under-sampled signal. In this example, the aliasing rate is approximately 450 MHZ.

Step **1418** includes under-sampling the analog PM carrier signal **916** at the aliasing rate to directly down-convert it to a demodulated baseband signal. Step **1418** is illustrated in FIG. **37**B by under-sample points **3705**.

Because a harmonic of the aliasing rate is substantially equal to the frequency of the signal **916**, or substantially equal to a harmonic or sub-harmonic thereof, essentially no IF is produced. The only substantial aliased component is the baseband signal.

In FIG. **37**D, voltage points **3708** correlate to the under-sample points **3705**. In an embodiment, the voltage points **3708** form a demodulated baseband signal **3710**. This can be accomplished in many ways. For example, each voltage point **3708** can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as described below.

In FIG. **37**E, a demodulated baseband signal **3712** represents the demodulated baseband signal **3710**, after filtering, on a compressed time scale. Although FIG. **37**E illustrates the demodulated baseband signal **3712** as a filtered output signal, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications.

The demodulated baseband signal **3712** is substantially similar to the analog modulating baseband signal **210**. The demodulated baseband signal **3712** can be processed without further down-conversion or demodulation.

The aliasing rate of the under-sampling signal is preferably controlled to optimize the demodulated baseband signal for amplitude output and polarity, as desired.

In the example above, the under-sample points **3705** occur at positive locations of the analog PM carrier signal **916**. Alternatively, the under-sample points **3705** can occur at other locations include negative points of the analog PM carrier signal **916**. When the under-sample points **3705** occur at negative locations of the analog PM carrier signal **916**, the resultant demodulated baseband signal is inverted relative to the modulating baseband signal **210**.

The drawings referred to herein illustrate direct to data down-conversion in accordance with the invention. For example, the demodulated baseband signal **3710** in FIG. **37**D and the demodulated baseband signal **3712** in FIG. **37**E illustrate that the analog PM carrier signal **916** was successfully down-converted to the demodulated baseband signal **3710** by retaining enough baseband information for sufficient reconstruction.

2.2.2.1.2 Digital PM Carrier Signal

A process for directly down-converting the digital PM carrier signal **1016** to a demodulated baseband signal is now described with reference to the flowchart **1413** in FIG. **14**C. The digital PM carrier signal **1016** is re-illustrated in **38**A for convenience. For this example, the digital PM carrier signal **1016** oscillates at approximately 900 MHZ. In FIG. **38**B, a digital PM carrier signal **3804** illustrates a portion of the digital PM carrier signal **1016** on an expanded time scale.

The process begins at step **1414**, which includes receiving an EM signal. This is represented by the digital PM signal **1016**.

Step **1416** includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. **38**C illustrates an example under-sampling signal **3806** on approximately the same time scale as FIG. **38**B. The under-sampling signal **3806** includes a train of pulses **3807** having negligible apertures that tend towards zero time in duration. The pulses **3807** repeat at the aliasing rate or pulse repetition rate, which is determined or selected as described above. Generally, when directly down-converting to a demodulated baseband signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the under-sampled signal. In this example, the aliasing rate is approximately 450 MHZ.

Step **1418** includes under-sampling the digital PM carrier signal **1016** at the aliasing rate to directly down-convert it to a demodulated baseband signal. This is illustrated in FIG. **38**B by under-sample points **3705**.

Because a harmonic of the aliasing rate is substantially equal to the frequency of the signal **1016**, essentially no IF is produced. The only substantial aliased component is the baseband signal.

In FIG. **38**D, voltage points **3808** correlate to the under-sample points **3805**. In an embodiment, the voltage points **3808** form a demodulated baseband signal **3810**. This can be accomplished in many ways. For example, each voltage point **3808** can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as described below.

In FIG. **38**E, a demodulated baseband signal **3812** represents the demodulated baseband signal **3810**, after filtering, on a compressed time scale. Although FIG. **38**E illustrates the demodulated baseband signal **3812** as a filtered output signal, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications.

The demodulated baseband signal **3812** is substantially similar to the digital modulating baseband signal **310**. The demodulated baseband signal **3812** can be processed without further down-conversion or demodulation.

The aliasing rate of the under-sampling signal is preferably controlled to optimize the demodulated baseband signal for amplitude output and polarity, as desired.

In the example above, the under-sample points **3805** occur at positive locations of the digital PM carrier signal **1016**. Alternatively, the under-sample points **3805** can occur at other locations include negative points of the digital PM carrier signal **1016**. When the under-sample points **3805** occur at negative locations of the digital PM carrier signal **1016**, the resultant demodulated baseband signal is inverted relative to the modulating baseband signal **310**.

The drawings referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the demodulated baseband signal **3810** in FIG. **38**D and the demodulated baseband signal **3812** in FIG. **38**E illustrate that the digital PM carrier signal **1016** was successfully down-converted to the demodulated baseband signal **3810** by retaining enough baseband information for sufficient reconstruction.

2.2.2.2 Structural Description

The operation of the under-sampling system **1602** is now described for the analog PM carrier signal **916**, with reference to the flowchart **1413** and the timing diagrams of FIGS. **37**A-E. In step **1414**, the under-sampling module **1606** receives the analog PM carrier signal **916** (FIG. **37**A). In step **1416**, the under-sampling module **1606** receives the under-sampling signal **3706** (FIG. **37**C). In step **1418**, the under-sampling module **1606** under-samples the analog PM carrier signal **916** at the aliasing rate of the under-sampling signal **3706** to down-convert the PM carrier signal **916** to the demodulated analog baseband signal **3710** in FIG. **37**D or to the filtered demodulated analog baseband signal **3712** in FIG. **37**E.

The operation of the under-sampling system **1602** is now described for the digital PM carrier signal **1016**, with reference to the flowchart **1413** and the timing diagrams of FIGS. **38**A-E. In step **1414**, the under-sampling module **1606** receives the digital PM carrier signal **1016** (FIG. **38**A). In step **1416**, the under-sampling module **1606** receives the under-sampling signal **3806** (FIG. **38**C). In step **1418**, the under-sampling module **1606** under-samples the digital PM carrier signal **1016** at the aliasing rate of the under-sampling signal **3806** to down-convert the digital PM carrier signal **1016** to the demodulated digital baseband signal **3810** in FIG. **38**D or to the filtered demodulated digital baseband signal **3812** in FIG. **38**E.

2.2.3 Other Embodiments

The embodiments described above are provided for purposes of illustration. These embodiments are not intended to limit the invention. Alternate embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate embodiments fall within the scope and spirit of the present invention.

2.3 Implementation Examples

Exemplary operational and/or structural implementations related to the method(s), structure(s), and/or embodiments described above are presented in Sections 4 and 5 below. These implementations are presented for purposes of illustration, and not limitation. The invention is not limited to the particular implementation examples described therein. Alternate implementations (including equivalents, extensions, variations, deviations, etc., of those described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

3. Modulation Conversion

In an embodiment, the invention down-converts an FM carrier signal F_{FMC} to a non-FM signal $F_{(NON\text{-}FM)}$, by under-sampling the FM carrier signal F_{Fmc}. This embodiment is illustrated in FIG. **45**B as **4512**.

In an example embodiment, the FM carrier signal F_{MC} is down-converted to a phase modulated (PM) signal F_{PM}. In another example embodiment, the FM carrier signal F_{FMC} is down-converted to an amplitude modulated (AM) signal F_{AM}. The invention is not limited to these embodiments. The down-converted signal can be demodulated with any conventional demodulation technique to obtain a demodulated baseband signal F_{DMB}.

The invention can be implemented with any type of FM signal. Exemplary embodiments are provided below for down-converting a frequency shift keying (FSK) signal to a non-FSK signal. FSK is a sub-set of FM, wherein an FM signal shifts or switches between two or more frequencies. FSK is typically used for digital modulating baseband signals, such as the digital modulating baseband signal **310** in FIG. **3**. For example, in FIG. **8**, the digital FM signal **816** is an FSK signal that shifts between an upper frequency and a lower frequency, corresponding to amplitude shifts in the digital modulating baseband signal **310**. The FSK signal **816** is used in example embodiments below.

In a first example embodiment, the FSK signal **816** is under-sampled at an aliasing rate that is based on a mid-point between the upper and lower frequencies of the FSK signal **816**. When the aliasing rate is based on the mid-point, the FSK signal **816** is down-converted to a phase shift keying (PSK) signal. PSK is a sub-set of phase modulation, wherein a PM signal shifts or switches between two or more phases. PSK is typically used for digital modulating baseband signals. For example, in FIG. **10**, the digital PM signal **1016** is a PSK signal that shifts between two phases. The PSK signal **1016** can be demodulated by any conventional PSK demodulation technique(s).

In a second example embodiment, the FSK signal **816** is under-sampled at an aliasing rate that is based upon either the upper frequency or the lower frequency of the FSK signal **816**. When the aliasing rate is based upon the upper frequency or the lower frequency of the FSK signal **816**, the FSK signal **816** is down-converted to an amplitude shift keying (ASK) signal. ASK is a sub-set of amplitude modulation, wherein an AM signal shifts or switches between two or more amplitudes. ASK is typically used for digital modulating baseband signals. For example, in FIG. **6**, the digital AM signal **616** is an ASK signal that shifts between the first amplitude and the second amplitude. The ASK signal **616** can be demodulated by any conventional ASK demodulation technique(s).

The following sections describe methods for under-sampling an FM carrier signal F_{FMC} to down-convert it to the non-FM signal $F_{(NON\text{-}FM)}$. Exemplary structural embodiments for implementing the methods are also described. It should be understood that the invention is not limited to the particular embodiments described below. Equivalents, extensions, variations, deviations, etc., of the following will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such equivalents, extensions, variations, deviations, etc., are within the scope and spirit of the present invention.

The following sections include a high level discussion, example embodiments, and implementation examples.

3.1 High Level Description

This section (including its subsections) provides a high-level description of under-sampling the FM carrier signal F_{FM} to down-convert it to the non-FM signal $F_{(NON\text{-}FM)}$, according to the invention. In particular, an operational process for down-converting the FM carrier signal F_{FM} to the non-FM signal $F_{(NON\text{-}FM)}$ is described at a high-level. Also, a structural implementation for implementing this process is described at a high-level. The structural implementation is described

herein for illustrative purposes, and is not limiting. In particular, the process described in this section can be achieved using any number of structural implementations, one of which is described in this section. The details of such structural implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

3.1.1 Operational Description

FIG. **14**D depicts a flowchart **1419** that illustrates an exemplary method for down-converting the FM carrier signal F_{FMC} to the non-FM signal $F_{(NON\text{-}FM)}$. The exemplary method illustrated in the flowchart **1419** is an embodiment of the flowchart **1401** in FIG. **14**A.

Any and all forms of frequency modulation techniques are valid for this invention. For ease of discussion, the digital FM carrier (FSK) signal **816** is used to illustrate a high level operational description of the invention. Subsequent sections provide detailed flowcharts and descriptions for the FSK signal **816**. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention can be implemented to down-convert any type of FM signal.

The method illustrated in the flowchart **1419** is described below at a high level for down-converting the FSK signal **816** in FIG. **8**C to a PSK signal. The FSK signal **816** is re-illustrated in FIG. **39**A for convenience.

The process of the flowchart **1419** begins at step **1420**, which includes receiving an FM signal. This is represented by the FSK signal **816**. The FSK signal **816** shifts between an upper frequency **3910** and a lower frequency **3912**. In an exemplary embodiment, the upper frequency **3910** is approximately 901 MHZ and the lower frequency **3912** is approximately 899 MHZ.

Step **1422** includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. **39**B illustrates an example under-sampling signal **3902** which includes a train of pulses **3903** having negligible apertures that tend towards zero time in duration. The pulses **3903** repeat at the aliasing rate or pulse repetition rate.

When down-converting an FM carrier signal F_{FMC} to a non-FM signal $F_{(NON\text{-}FM)}$, the aliasing rate is substantially equal to a frequency contained within the FM signal, or substantially equal to a harmonic or sub-harmonic thereof. In this example overview embodiment, where the FSK signal **816** is to be down-converted to a PSK signal, the aliasing rate is based on a mid-point between the upper frequency **3910** and the lower frequency **3912**. For this example, the mid-point is approximately 900 MHZ. In another embodiment described below, where the FSK signal **816** is to be down-converted to an ASK signal, the aliasing rate is based on either the upper frequency **3910** or the lower frequency **3912**, not the mid-point.

Step **1424** includes under-sampling the FM signal F_{FMC} at the aliasing rate to down-convert the FM carrier signal F_{FMC} to the non-FM signal $F_{(NON\text{-}FM)}$. Step **1424** is illustrated in FIG. **39**C, which illustrates a stair step PSK signal **3904**, which is generated by the modulation conversion process.

When the upper frequency **3910** is under-sampled, the PSK signal **3904** has a frequency of approximately 1 MHZ and is used as a phase reference. When the lower frequency **3912** is under-sampled, the PSK signal **3904** has a frequency of 1 MHZ and is phase shifted 180 degrees from the phase reference.

FIG. **39**D depicts a PSK signal **3906**, which is a filtered version of the PSK signal **3904**. The invention can thus generate a filtered output signal, a partially filtered output signal, or a relatively unfiltered stair step output signal. The choice between filtered, partially filtered and non-filtered output signals is generally a design choice that depends upon the application of the invention.

The aliasing rate of the under-sampling signal is preferably controlled to optimize the down-converted signal for amplitude output and polarity, as desired.

Detailed exemplary embodiments for down-converting an FSK signal to a PSK signal and for down-converting an FSK signal to an ASK signal are provided below.

3.1.2 Structural Description

FIG. **16** illustrates the block diagram of the under-sampling system **1602** according to an embodiment of the invention. The under-sampling system **1602** includes the under-sampling module **1606**. The under-sampling system **1602** is an example embodiment of the generic aliasing system **1302** in FIG. **13**.

In a modulation conversion embodiment, the EM signal **1304** is an FM carrier signal and the under-sampling module **1606** under-samples the FM carrier signal at a frequency that is substantially equal to a harmonic of a frequency within the FM signal or, more typically, substantially equal to a sub-harmonic of a frequency within the FM signal. Preferably, the under-sampling module **1606** under-samples the FM carrier signal F_{FMC} to down-convert it to a non-FM signal $F_{(NON\text{-}FM)}$ in the manner shown in the operational flowchart **1419**. But it should be understood that the scope and spirit of the invention includes other structural embodiments for performing the steps of the flowchart **1419**. The specifics of the other structural embodiments will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

The operation of the under-sampling system **1602** shall now be described with reference to the flowchart **1419** and the timing diagrams of FIGS. **39**A-**39**D. In step **1420**, the under-sampling module **1606** receives the FSK signal **816**. In step **1422**, the under-sampling module **1606** receives the under-sampling signal **3902**. In step **1424**, the under-sampling module **1606** under-samples the FSK signal **816** at the aliasing rate of the under-sampling signal **3902** to down-convert the FSK signal **816** to the PSK signal **3904** or **3906**.

Example implementations of the under-sampling module **1606** are provided in Section 4 below.

3.2 Example Embodiments

Various embodiments related to the method(s) and structure(s) described above are presented in this section (and its subsections). These embodiments are described herein for purposes of illustration, and not limitation. The invention is not limited to these embodiments. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

The method for down-converting an FM carrier signal F_{FMC} to a non-FM signal, $F_{(NON\text{-}FM)}$, illustrated in the flowchart **1419** of FIG. **14**D, can be implemented with any type of FM carrier signal including, but not limited to, FSK signals. The flowchart **1419** is described in detail below for down-converting an FSK signal to a PSK signal and for down-converting a PSK signal to an ASK signal. The exemplary descriptions below are intended to facilitate an understanding of the present invention. The present invention is not limited to or by the exemplary embodiments below.

3.2.1 First Example Embodiment: Down-Converting an FM Signal to a PM Signal

3.2.1.1 Operational Description

Operation of the exemplary process of the flowchart **1419** in FIG. **14**D is now described for down-converting the FSK

signal **816** illustrated in FIG. **8**C to a PSK signal. The FSK signal **816** is re-illustrated in FIG. **40**A for convenience.

The FSK signal **816** shifts between a first frequency **4006** and a second frequency **4008**. In the exemplary embodiment, the first frequency **4006** is lower than the second frequency **4008**. In an alternative embodiment, the first frequency **4006** is higher than the second frequency **4008**. For this example, the first frequency **4006** is approximately 899 MHZ and the second frequency **4008** is approximately 901 MHZ.

FIG. **40**B illustrates an FSK signal portion **4004** that represents a portion of the FSK signal **816** on an expanded time scale.

The process of down-converting the FSK signal **816** to a PSK signal begins at step **1420**, which includes receiving an FM signal. This is represented by the FSK signal **816**.

Step **1422** includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. **40**C illustrates an example under-sampling signal **4007** on approximately the same time scale as FIG. **40**B. The under-sampling signal **4007** includes a train of pulses **4009** having negligible apertures that tend towards zero time in duration. The pulses **4009** repeat at the aliasing rate, which is determined or selected as described above. Generally, when down-converting an FM signal to a non-FM signal, the aliasing rate is substantially equal to a harmonic or, more typically, a sub-harmonic of a frequency contained within the FM signal.

In this example, where an FSK signal is being down-converted to a PSK signal, the aliasing rate is substantially equal to a harmonic of the mid-point between the frequencies **4006** and **4008** or, more typically, substantially equal to a sub-harmonic of the mid-point between the frequencies **4006** and **4008**. In this example, where the first frequency **4006** is 899 MHZ and second frequency **4008** is 901 MHZ, the mid-point is approximately 900 MHZ. Suitable aliasing rates include 1.8 GHZ, 900 MHZ, 450 MHZ, etc. In this example, the aliasing rate of the under-sampling signal **4008** is approximately 450 MHZ.

Step **1424** includes under-sampling the FM signal at the aliasing rate to down-convert it to the non-FM signal $F_{(NON\text{-}FM)}$. Step **1424** is illustrated in FIG. **40**B by under-sample points **4005**. The under-sample points **4005** occur at the aliasing rate of the pulses **4009**.

In FIG. **40**D, voltage points **4010** correlate to the under-sample points **4005**. In an embodiment, the voltage points **4010** form a PSK signal **4012**. This can be accomplished in many ways. For example, each voltage point **4010** can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as described below.

When the first frequency **4006** is under-sampled, the PSK signal **4012** has a frequency of approximately 1 MHZ and is used as a phase reference. When the second frequency **4008** is under-sampled, the PSK signal **4012** has a frequency of 1 MHZ and is phase shifted 180 degrees from the phase reference.

In FIG. **40**E, a PSK signal **4014** illustrates the PSK signal **4012**, after filtering, on a compressed time scale. Although FIG. **40**E illustrates the PSK signal **4012** as a filtered output signal **4014**, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications. The PSK signal **4014** can be demodulated through any conventional phase demodulation technique.

The aliasing rate of the under-sampling signal is preferably controlled to optimize the down-converted signal for amplitude output and polarity, as desired.

In the example above, the under-sample points **4005** occur at positive locations of the FSK signal **816**. Alternatively, the under-sample points **4005** can occur at other locations including negative points of the FSK signal **816**. When the under-sample points **4005** occur at negative locations of the FSK signal **816**, the resultant PSK signal is inverted relative to the PSK signal **4014**.

The drawings referred to herein illustrate modulation conversion in accordance with the invention. For example, the PSK signal **4014** in FIG. **40**E illustrates that the FSK signal **816** was successfully down-converted to the PSK signal **4012** and **4014** by retaining enough baseband information for sufficient reconstruction.

3.2.1.2 Structural Description

The operation of the under-sampling system **1602** is now described for down-converting the FSK signal **816** to a PSK signal, with reference to the flowchart **1419** and to the timing diagrams of FIGS. **40**A-E. In step **1420**, the under-sampling module **1606** receives the FSK signal **816** (FIG. **40**A). In step **1422**, the under-sampling module **1606** receives the under-sampling signal **4007** (FIG. **40**C). In step **1424**, the under-sampling module **1606** under-samples the FSK signal **816** at the aliasing rate of the under-sampling signal **4007** to down-convert the FSK signal **816** to the PSK signal **4012** in FIG. **40**D or the PSK signal **4014** in FIG. **40**E.

3.2.2 Second Example Embodiment: Down-Converting an FM Signal to an AM Signal

3.2.2.1 Operational Description

Operation of the exemplary process of FIG. **14**D is now described for down-converting the FSK signal **816**, illustrated in FIG. **8**C, to an ASK signal. The FSK signal **816** is re-illustrated in FIG. **41**A for convenience.

The FSK signal **816** shifts between a first frequency **4106** and a second frequency **4108**. In the exemplary embodiment, the first frequency **4106** is lower than the second frequency **4108**. In an alternative embodiment, the first frequency **4106** is higher than the second frequency **4108**. For this example, the first frequency **4106** is approximately 899 MHZ and the second frequency **4108** is approximately 901 MHZ.

FIG. **41**B illustrates an FSK signal portion **4104** that represents a portion of the FSK signal **816** on an expanded time scale.

The process of down-converting the FSK signal **816** to an ASK signal begins at step **1420**, which includes receiving an FM signal. This is represented by the FSK signal **816**.

Step **1422** includes receiving an under-sampling signal having an aliasing rate F_{AR}. FIG. **41**C illustrates an example under-sampling signal **4107** illustrated on approximately the same time scale as FIG. **42**B. The under-sampling signal **4107** includes a train of pulses **4109** having negligible apertures that tend towards zero time in duration. The pulses **4109** repeat at the aliasing rate, or pulse repetition rate. The aliasing rate is determined or selected as described above.

Generally, when down-converting an FM signal to a non-FM signal, the aliasing rate is substantially equal to a harmonic of a frequency within the FM signal or, more typically, to a sub-harmonic of a frequency within the FM signal. When an FSK signal **816** is being down-converted to an ASK signal, the aliasing rate is substantially equal to a harmonic of the first frequency **4106** or the second frequency **4108** or, more typically, substantially equal to a sub-harmonic of the first frequency **4106** or the second frequency **4108**. In this example, where the first frequency **4106** is 899 MHZ and the second frequency **4108** is 901 MHZ, the aliasing rate can be substantially equal to a harmonic or sub-harmonic of 899 MHZ or

901 MHZ. In this example the aliasing rate is approximately 449.5 MHZ, which is a sub-harmonic of the first frequency **4106**.

Step **1424** includes under-sampling the FM signal at the aliasing rate to down-convert it to a non-FM signal $F_{(NON\text{-}FM)}$. Step **1424** is illustrated in FIG. **41**B by under-sample points **4105**. The under-sample points **4105** occur at the aliasing rate of the pulses **4109**. When the first frequency **4106** is under-sampled, the aliasing pulses **4109** and the under-sample points **4105** occur at the same location of subsequent cycles of the FSK signal **816**. This generates a relatively constant output level. But when the second frequency **4108** is under-sampled, the aliasing pulses **4109** and the under-sample points **4005** occur at different locations of subsequent cycles of the FSK signal **816**. This generates an oscillating pattern at approximately (901 MHZ−899 MHZ)=2 MHZ.

In FIG. **41**D, voltage points **4110** correlate to the under-sample points **4105**. In an embodiment, the voltage points **4110** form an ASK signal **4112**. This can be accomplished in many ways. For example, each voltage point **4110** can be held at a relatively constant level until the next voltage point is received. This results in a stair-step output which can be smoothed or filtered if desired, as described below.

In FIG. **41**E, an ASK signal **4114** illustrates the ASK signal **4112**, after filtering, on a compressed time scale. Although FIG. **41**E illustrates the ASK signal **4114** as a filtered output signal, the output signal does not need to be filtered or smoothed to be within the scope of the invention. Instead, the output signal can be tailored for different applications. The ASK signal **4114** can be demodulated through any conventional amplitude demodulation technique

When down-converting from FM to AM, the aliasing rate of the under-sampling signal is preferably controlled to optimize the demodulated baseband signal for amplitude output and/or polarity, as desired.

In an alternative embodiment, the aliasing rate is based on the second frequency and the resultant ASK signal is reversed relative to the ASK signal **4114**.

The drawings referred to herein illustrate modulation conversion in accordance with the invention. For example, the ASK signal **4114** in FIG. **41**E illustrates that the FSK carrier signal **816** was successfully down-converted to the ASK signal **4114** by retaining enough baseband information for sufficient reconstruction.

3.2.2.2 Structural Description

The operation of the under-sampling system **1602** is now described for down-converting the FSK signal **816** to an ASK signal, with reference to the flowchart **1419** and to the timing diagrams of FIGS. **41**A-E. In step **1420**, the under-sampling module **1606** receives the FSK signal **816** (FIG. **41**A). In step **1422**, the under-sampling module **1606** receives the under-sampling signal **4107** (FIG. **41**C). In step **1424**, the under-sampling module **1606** under-samples the FSK signal **816** at the aliasing of the under-sampling signal **4107** to down-convert the FSK signal **816** to the ASK signal **4112** of FIG. **41**D or the ASK signal **4114** in FIG. **41**E.

3.2.3 Other Example Embodiments

The embodiments described above are provided for purposes of illustration. These embodiments are not intended to limit the invention. Alternate embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate embodiments fall within the scope and spirit of the present invention.

3.3 Implementation Examples

Exemplary operational and/or structural implementations related to the method(s), structure(s), and/or embodiments described above are presented in Sections 4 and 5 below. These implementations are presented for purposes of illustration, and not limitation. The invention is not limited to the particular implementation examples described therein. Alternate implementations (including equivalents, extensions, variations, deviations, etc., of those described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

4. Implementation Examples

Exemplary operational and/or structural implementations related to the method(s), structure(s), and/or embodiments described in the Sub-Sections above are presented in this section (and its subsections). These implementations are presented herein for purposes of illustration, and not limitation. The invention is not limited to the particular implementation examples described herein. Alternate implementations (including equivalents, extensions, variations, deviations, etc., of those described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

FIG. **13** illustrates a generic aliasing system **1302**, including an aliasing module **1306**. FIG. **16** illustrates an under-sampling system **1602**, which includes an under-sampling module **1606**. The under-sampling module **1606** receives an under-sampling signal **1604** having an aliasing rate F_{AR}. The under-sampling signal **1604** includes a train of pulses having negligible apertures that tend towards zero time in duration. The pulses repeat at the aliasing rate F_{AR}. The under-sampling system **1602** is an example implementation of the generic aliasing system **1303**. The under-sampling system **1602** outputs a down-converted signal **1308**A.

FIG. **26**A illustrates an exemplary sample and hold system **2602**, which is an exemplary implementation of the under-sampling system **1602**. The sample and hold system **2602** is described below.

FIG. **26**B illustrates an exemplary inverted sample and hold system **2606**, which is an alternative example implementation of the under-sampling system **1602**. The inverted sample and hold system **2606** is described below.

4.1 the Under-Sampling System as a Sample and Hold System

FIG. **26**A is a block diagram of a the sample and hold system **2602**, which is an example embodiment of the under-sampling module **1606** in FIG. **16**, which is an example embodiment of the generic aliasing module **1306** in FIG. **13**.

The sample and hold system **2602** includes a sample and hold module **2604**, which receives the EM signal **1304** and the under-sampling signal **1604**. The sample and hold module **2604** under-samples the EM signal at the aliasing rate of the under-sampling signal **1604**, as described in the sections above with respect to the flowcharts **1401** in FIG. **14**A, **1407** in FIG. **14**B, **1413** in FIG. **14**C and **1419** in FIG. **14**D. The under-sampling system **1602** outputs a down-converted signal **1308**A.

FIG. **27** illustrates an under-sampling system **2701** as a sample and hold system, which is an example implementation of the under-sampling system **2602**. The under-sampling system **2701** includes a switch module **2702** and a holding module **2706**. The under-sampling system **2701** is described below.

FIG. **24**A illustrates an under-sampling system **2401** as a break before make under-sampling system, which is an alternative implementation of the under-sampling system **2602**. The break before make under-sampling system **2401** is described below.

4.4.1 The Sample and Hold System as a Switch Module and a Holding Module

FIG. **27** illustrates an exemplary embodiment of the sample and hold module **2604** from FIG. **26**A. In the exemplary embodiment, the sample and hold module **2604** includes a switch module **2702**, and a holding module **2706**.

Preferably, the switch module **2702** and the holding module **2706** under-sample the EM signal **1304** to down-convert it in any of the manners shown in the operation flowcharts **1401**, **1407**, **1413** and **1419**. For example, the sample and hold module **2604** can receive and under-sample any of the modulated carrier signal signals described above, including, but not limited to, the analog AM signal **516**, the digital AM signal **616**, the analog FM signal **716**, the digital FM signal **816**, the analog PM signal **916**, the digital PM signal **1016**, etc., and any combinations thereof.

The switch module **2702** and the holding module **2706** down-convert the EM signal **1304** to an intermediate signal, to a demodulated baseband or to a different modulation scheme, depending upon the aliasing rate.

For example, operation of the switch module **2702** and the holding module **2706** are now described for down-converting the EM signal **1304** to an intermediate signal, with reference to the flowchart **1407** and the example timing diagrams in FIG. **79**A-F.

In step **1408**, the switch module **2702** receives the EM signal **1304** (FIG. **79**A). In step **1410**, the switch module **2702** receives the under-sampling signal **1604** (FIG. **79**C). In step **1412**, the switch module **2702** and the holding module **2706** cooperate to under-sample the EM signal **1304** and down-convert it to an intermediate signal. More specifically, during step **1412**, the switch module **2702** closes during each under-sampling pulse to couple the EM signal **1304** to the holding module **2706**. In an embodiment, the switch module **2702** closes on rising edges of the pulses. In an alternative embodiment, the switch module **2702** closes on falling edges of the pulses. When the EM signal **1304** is coupled to the holding module **2706**, the amplitude of the EM signal **1304** is captured by the holding module **2706**. The holding module **2706** is designed to capture and hold the amplitude of the EM signal **1304** within the short time frame of each negligible aperture pulse. FIG. **79**B illustrates the EM signal **1304** after under-sampling.

The holding module **2706** substantially holds or maintains each under-sampled amplitude until a subsequent under-sample. (FIG. **79**D). The holding module **2706** outputs the under-sampled amplitudes as the down-converted signal **1308**A. The holding module **2706** can output the down-converted signal **1308**A as an unfiltered signal, such as a stair step signal (FIG. **79**E), as a filtered down-converted signal (FIG. **79**F) or as a partially filtered down-converted signal.

4.1.2 The Sample and Hold System as Break-Before-Make Module

FIG. **24**A illustrates a break-before-make under-sampling system **2401**, which is an alternative implementation of the under-sampling system **2602**.

Preferably, the break-before-make under-sampling system **2401** under-samples the EM signal **1304** to down-convert it in any of the manners shown in the operation flowcharts **1401**, **1407**, **1413** and **1419**. For example, the sample and hold module **2604** can receive and under-sample any of the unmodulated or modulated carrier signal signals described above, including, but not limited to, the analog AM signal **516**, the digital AM signal **616**, the analog FM signal **716**, the digital FM signal **816**, the analog PM signal **916**, the digital PM signal **1016**, etc., and combinations thereof.

The break-before-make under-sampling system **2401** down-converts the EM signal **1304** to an intermediate signal, to a demodulated baseband or to a different modulation scheme, depending upon the aliasing rate.

FIG. **24**A includes a break-before-make switch **2402**. The break-before-make switch **2402** includes a normally open switch **2404** and a normally closed switch **2406**. The normally open switch **2404** is controlled by the under-sampling signal **1604**, as previously described. The normally closed switch **2406** is controlled by an isolation signal **2412**. In an embodiment, the isolation signal **2412** is generated from the under-sampling signal **1604**. Alternatively, the under-sampling signal **1604** is generated from the isolation signal **2412**. Alternatively, the isolation signal **2412** is generated independently from the under-sampling signal **1604**. The break-before-make module **2402** substantially isolates a sample and hold input **2408** from a sample and hold output **2410**.

FIG. **24**B illustrates an example timing diagram of the under-sampling signal **1604** that controls the normally open switch **2404**. FIG. **24**C illustrates an example timing diagram of the isolation signal **2412** that controls the normally closed switch **2406**. Operation of the break-before-make module **2402** is described with reference to the example timing diagrams in FIGS. **24**B and **24**C.

Prior to time t0, the normally open switch **2404** and the normally closed switch **2406** are at their normal states.

At time t0, the isolation signal **2412** in FIG. **24**C opens the normally closed switch **2406**. Then, just after time t0, the normally open switch **2404** and the normally closed switch **2406** are open and the input **2408** is isolated from the output **2410**.

At time t1, the under-sampling signal **1604** in FIG. **24**B briefly closes the normally open switch **2404**. This couples the EM signal **1304** to the holding module **2416**.

Prior to t2, the under-sampling signal **1604** in FIG. **24**B opens the normally open switch **2404**. This de-couples the EM signal **1304** from the holding module **2416**.

At time t2, the isolation signal **2412** in FIG. **24**C closes the normally closed switch **2406**. This couples the holding module **2416** to the output **2410**.

The break-before-make under-sampling system **2401** includes a holding module **2416**, which can be similar to the holding module **2706** in FIG. **27**. The break-before-make under-sampling system **2401** down-converts the EM signal **1304** in a manner similar to that described with reference to the under-sampling system **2702** in FIG. **27**.

4.1.3 Example Implementations of the Switch Module

The switch module **2702** in FIG. **27** and the switch modules **2404** and **2406** in FIG. **24**A can be any type of switch device that preferably has a relatively low impedance when closed and a relatively high impedance when open. The switch modules **2702**, **2404** and **2406** can be implemented with normally open or normally closed switches. The switch device need not be an ideal switch device. FIG. **28**B illustrates the switch modules **2702**, **2404** and **2406** as, for example, a switch module **2810**.

The switch device **2810** (e.g., switch modules **2702**, **2404** and **2406**) can be implemented with any type of suitable switch device, including, but not limited to mechanical switch devices and electrical switch devices, optical switch devices, etc., and combinations thereof. Such devices include, but are not limited to transistor switch devices, diode switch devices, relay switch devices, optical switch devices, micro-machine switch devices, etc.

In an embodiment, the switch module **2810** can be implemented as a transistor, such as, for example, a field effect transistor (FET), a bi-polar transistor, or any other suitable circuit switching device.

In FIG. **28**A, the switch module **2810** is illustrated as a FET **2802**. The FET **2802** can be any type of FET, including, but not limited to, a MOSFET, a JFET, a GaAsFET, etc. The FET **2802** includes a gate **2804**, a source **2806** and a drain **2808**. The gate **2804** receives the under-sampling signal **1604** to control the switching action between the source **2806** and the drain **2808**. Generally, the source **2806** and the drain **2808** are interchangeable.

It should be understood that the illustration of the switch module **2810** as a FET **2802** in FIG. **28**A is for example purposes only. Any device having switching capabilities could be used to implement the switch module **2810** (e.g., switch modules **2702**, **2404** and **2406**), as will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

In FIG. **28**C, the switch module **2810** is illustrated as a diode switch **2812**, which operates as a two lead device when the under-sampling signal **1604** is coupled to the output **2813**.

In FIG. **28**D, the switch module **2810** is illustrated as a diode switch **2814**, which operates as a two lead device when the under-sampling signal **1604** is coupled to the output **2815**.

4.1.4 Example Implementations of the Holding Module

The holding modules **2706** and **2416** preferably captures and holds the amplitude of the original, unaffected, EM signal **1304** within the short time frame of each negligible aperture under-sampling signal pulse.

In an exemplary embodiment, holding modules **2706** and **2416** are implemented as a reactive holding module **2901** in FIG. **29**A, although the invention is not limited to this embodiment. A reactive holding module is a holding module that employs one or more reactive electrical components to preferably quickly charge to the amplitude of the EM signal **1304**. Reactive electrical components include, but are not limited to, capacitors and inductors.

In an embodiment, the holding modules **2706** and **2416** include one or more capacitive holding elements, illustrated in FIG. **29**B as a capacitive holding module **2902**. In FIG. **29**C, the capacitive holding module **2902** is illustrated as one or more capacitors illustrated generally as capacitor(s) **2904**. Recall that the preferred goal of the holding modules **2706** and **2416** is to quickly charge to the amplitude of the EM signal **1304**. In accordance with principles of capacitors, as the negligible aperture of the under-sampling pulses tends to zero time in duration, the capacitive value of the capacitor **2904** can tend towards zero Farads. Example values for the capacitor **2904** can range from tens of pico Farads to fractions of pico Farads. A terminal **2906** serves as an output of the sample and hold module **2604**. The capacitive holding module **2902** provides the under-samples at the terminal **2906**, where they can be measured as a voltage. FIG. **29**F illustrates the capacitive holding module **2902** as including a series capacitor **2912**, which can be utilized in an inverted sample and hold system as described below.

In an alternative embodiment, the holding modules **2706** and **2416** include one or more inductive holding elements, illustrated in FIG. **29**D as an inductive holding module **2908**.

In an alternative embodiment, the holding modules **2706** and **2416** include a combination of one or more capacitive holding elements and one or more inductive holding elements, illustrated in FIG. **29**E as a capacitive/inductive holding module **2910**.

FIG. **29**G illustrates an integrated under-sampling system that can be implemented to down-convert the EM signal **1304** as illustrated in, and described with reference to, FIGS. **79**A-F.

4.1.5 Optional Under-Sampling Signal Module

FIG. **30** illustrates an under-sampling system **3001**, which is an example embodiment of the under-sampling system **1602**. The under-sampling system **3001** includes an optional under-sampling signal module **3002** that can perform any of a variety of functions or combinations of functions, including, but not limited to, generating the under-sampling signal **1604**.

In an embodiment, the optional under-sampling signal module **3002** includes an aperture generator, an example of which is illustrated in FIG. **29**J as an aperture generator **2920**. The aperture generator **2920** generates negligible aperture pulses **2926** from an input signal **2924**. The input signal **2924** can be any type of periodic signal, including, but not limited to, a sinusoid, a square wave, a saw-tooth wave, etc. Systems for generating the input signal **2924** are described below.

The width or aperture of the pulses **2926** is determined by delay through the branch **2922** of the aperture generator **2920**. Generally, as the desired pulse width decreases, the tolerance requirements of the aperture generator **2920** increase. In other words, to generate negligible aperture pulses for a given input EM frequency, the components utilized in the example aperture generator **2920** require greater reaction times, which are typically obtained with more expensive elements, such as gallium arsenide (GaAs), etc.

The example logic and implementation shown in the aperture generator **2920** are provided for illustrative purposes only, and are not limiting. The actual logic employed can take many forms. The example aperture generator **2920** includes an optional inverter **2928**, which is shown for polarity consistency with other examples provided herein. An example implementation of the aperture generator **2920** is illustrated in FIG. **29**K.

Additional examples of aperture generation logic is provided in FIGS. **29**H and **29**I. FIG. **29**H illustrates a rising edge pulse generator **2940**, which generates pulses **2926** on rising edges of the input signal **2924**. FIG. **29**I illustrates a falling edge pulse generator **2950**, which generates pulses **2926** on falling edges of the input signal **2924**.

In an embodiment, the input signal **2924** is generated externally of the under-sampling signal module **3002**, as illustrated in FIG. **30**. Alternatively, the input signal **2924** is generated internally by the under-sampling signal module **3002**. The input signal **2924** can be generated by an oscillator, as illustrated in FIG. **29**L by an oscillator **2930**. The oscillator **2930** can be internal to the under-sampling signal module **3002** or external to the under-sampling signal module **3002**. The oscillator **2930** can be external to the under-sampling system **3001**.

The type of down-conversion performed by the under-sampling system **3001** depends upon the aliasing rate of the under-sampling signal **1604**, which is determined by the frequency of the pulses **2926**. The frequency of the pulses **2926** is determined by the frequency of the input signal **2924**. For example, when the frequency of the input signal **2924** is substantially equal to a harmonic or a sub-harmonic of the EM signal **1304**, the EM signal **1304** is directly down-converted to baseband (e.g. when the EM signal is an AM signal or a PM signal), or converted from FM to a non-FM signal. When the frequency of the input signal **2924** is substantially equal to a harmonic or a sub-harmonic of a difference frequency, the EM signal **1304** is down-converted to an intermediate signal.

The optional under-sampling signal module **3002** can be implemented in hardware, software, firmware, or any combination thereof.

4.2 the Under-Sampling System as an Inverted Sample and Hold

FIG. **26**B illustrates an exemplary inverted sample and hold system **2606**, which is an alternative example implementation of the under-sampling system **1602**.

FIG. **42** illustrates a inverted sample and hold system **4201**, which is an example implementation of the inverted sample and hold system **2606** in FIG. **26**B. The sample and hold system **4201** includes a sample and hold module **4202**, which includes a switch module **4204** and a holding module **4206**. The switch module **4204** can be implemented as described above with reference to FIGS. **28**A-D.

The holding module **4206** can be implemented as described above with reference to FIGS. **29**A-F, for the holding modules **2706** and **2416**. In the illustrated embodiment, the holding module **4206** includes one or more capacitors **4208**. The capacitor(s) **4208** are selected to pass higher frequency components of the EM signal **1304** through to a terminal **4210**, regardless of the state of the switch module **4204**. The capacitor **4202** stores charge from the EM signal **1304** during aliasing pulses of the under-sampling signal **1604** and the signal at the terminal **4210** is thereafter off-set by an amount related to the charge stored in the capacitor **4206**.

Operation of the inverted sample and hold system **4201** is illustrated in FIGS. **34**A-F. FIG. **34**A illustrates an example EM signal **1304**. FIG. **34**B illustrates the EM signal **1304** after under-sampling. FIG. **34**C illustrates the under-sampling signal **1606**, which includes a train of aliasing pulses having negligible apertures.

FIG. **34**D illustrates an example down-converted signal **1308**A. FIG. **34**E illustrates the down-converted signal **1308**A on a compressed time scale. Since the holding module **4206** is series element, the higher frequencies (e.g., RF) of the EM signal **1304** can be seen on the down-converted signal. This can be filtered as illustrated in FIG. **34**F.

The inverted sample and hold system **4201** can be used to down-convert any type of EM signal, including modulated carrier signals and unmodulated carrier signals, to IF signals and to demodulated baseband signals.

4.3 Other Implementations

The implementations described above are provided for purposes of illustration. These implementations are not intended to limit the invention. Alternate implementations, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

5. Optional Optimizations of Under-Sampling at an Aliasing Rate

The methods and systems described in sections above can be optionally optimized with one or more of the optimization methods or systems described below.

5.1 Doubling the Aliasing Rate (FAR) of the Under-Sampling Signal

In an embodiment, the optional under-sampling signal module **3002** in FIG. **30** includes a pulse generator module that generates aliasing pulses at a multiple of the frequency of the oscillating source, such as twice the frequency of the oscillating source. The input signal **2926** may be any suitable oscillating source.

FIG. **31**A illustrates an example circuit **3102** that generates a doubler output signal **3104** (FIGS. **31**A and C) that may be used as an under-sampling signal **1604**. The example circuit **3102** generates pulses on rising and falling edges of the input oscillating signal **3106** of FIG. **31**B. Input oscillating signal **3106** is one embodiment of optional input signal **2926**. The circuit **3102** can be implemented as a pulse generator and aliasing rate (F_{AR}) doubler, providing the under-sampling signal **1604** to under-sampling module **1606** in FIG. **30**.

The aliasing rate is twice the frequency of the input oscillating signal F_{osc} **3106**, as shown by EQ. (9) below.

$$F_{AR}=2\cdot F_{osc} \quad \text{EQ. (9)}$$

The aperture width of the aliasing pulses is determined by the delay through a first inverter **3108** of FIG. **31**A. As the delay is increased, the aperture is increased. A second inverter **3112** is shown to maintain polarity consistency with examples described elsewhere. In an alternate embodiment inverter **3112** is omitted. Preferably, the pulses have negligible aperture widths that tend toward zero time. The doubler output signal **3104** may be further conditioned as appropriate to drive a switch module with negligible aperture pulses. The circuit **3102** may be implemented with integrated circuitry, discretely, with equivalent logic circuitry, or with any valid fabrication technology.

5.2 Differential Implementations

The invention can be implemented in a variety of differential configurations. Differential configurations are useful for reducing common mode noise. This can be very useful in receiver systems where common mode interference can be caused by intentional or unintentional radiators such as cellular phones, CB radios, electrical appliances etc. Differential configurations are also useful in reducing any common mode noise due to charge injection of the switch in the switch module or due to the design and layout of the system in which the invention is used. Any spurious signal that is induced in equal magnitude and equal phase in both input leads of the invention will be substantially reduced or eliminated. Some differential configurations, including some of the configurations below, are also useful for increasing the voltage and/or for increasing the power of the down-converted signal **1308**A. While an example of a differential under-sampling module is shown below, the example is shown for the purpose of illustration, not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc.) of the embodiment described herein will be apparent to those skilled in the relevant art based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

FIG. **44**A illustrates an example differential system **4402** that can be included in the under-sampling module **1606**. The differential system **4202** includes an inverted under-sampling design similar to that described with reference to FIG. **42**. The differential system **4402** includes inputs **4404** and **4406** and outputs **4408** and **4410**. The differential system **4402** includes a first inverted sample and hold module **4412**, which includes a holding module **4414** and a switch module **4416**. The differential system **4402** also includes a second inverted sample and hold module **4418**, which includes a holding module **4420** and the switch module **4416**, which it shares in common with sample and hold module **4412**.

One or both of the inputs **4404** and **4406** are coupled to an EM signal source. For example, the inputs can be coupled to an EM signal source, wherein the input voltages at the inputs **4404** and **4406** are substantially equal in amplitude but 180 degrees out of phase with one another. Alternatively, where dual inputs are unavailable, one of the inputs **4404** and **4406** can be coupled to ground.

In operation, when the switch module **4416** is closed, the holding modules **4414** and **4420** are in series and, provided they have similar capacitive values, they charge to equal amplitudes but opposite polarities. When the switch module **4416** is open, the voltage at the output **4408** is relative to the input **4404**, and the voltage at the output **4410** is relative to the voltage at the input **4406**.

Portions of the voltages at the outputs **4408** and **4410** include voltage resulting from charge stored in the holding modules **4414** and **4420**, respectively, when the switch module **4416** was closed. The portions of the voltages at the outputs **4408** and **4410** resulting from the stored charge are generally equal in amplitude to one another but 180 degrees out of phase.

Portions of the voltages at the outputs **4408** and **4410** also include ripple voltage or noise resulting from the switching action of the switch module **4416**. But because the switch module is positioned between the two outputs, the noise introduced by the switch module appears at the outputs **4408** and **4410** as substantially equal and in-phase with one another. As a result, the ripple voltage can be substantially filtered out by inverting the voltage at one of the outputs **4408** or **4410** and adding it to the other remaining output. Additionally, any noise that is impressed with substantially equal amplitude and equal phase onto the input terminals **4404** and **4406** by any other noise sources will tend to be canceled in the same way.

The differential system **4402** is effective when used with a differential front end (inputs) and a differential back end (outputs). It can also be utilized in the following configurations, for example:

a) A single-input front end and a differential back end; and

b) A differential front end and single-output back end.

Examples of these system are provided below.

5.2.1 Differential Input-to-Differential Output

FIG. **44**B illustrates the differential system **4402** wherein the inputs **4404** and **4406** are coupled to equal and opposite EM signal sources, illustrated here as dipole antennas **4424** and **4426**. In this embodiment, when one of the outputs **4408** or **4410** is inverted and added to the other output, the common mode noise due to the switching module **4416** and other common mode noise present at the input terminals **4404** and **4406** tend to substantially cancel out.

5.2.2 Single Input-to-Differential Output

FIG. **44**C illustrates the differential system **4402** wherein the input **4404** is coupled to an EM signal source such as a monopole antenna **4428** and the input **4406** is coupled to ground.

FIG. **44**E illustrates an example single input to differential output receiver/down-converter system **4436**. The system **4436** includes the differential system **4402** wherein the input **4406** is coupled to ground. The input **4404** is coupled to an EM signal source **4438**.

The outputs **4408** and **4410** are coupled to a differential circuit **4444** such as a filter, which preferably inverts one of the outputs **4408** or **4410** and adds it to the other output **4408** or **4410**. This substantially cancels common mode noise generated by the switch module **4416**. The differential circuit **4444** preferably filters the higher frequency components of the EM signal **1304** that pass through the holding modules **4414** and **4420**. The resultant filtered signal is output as the down-converted signal **1308**A.

5.2.3 Differential Input-to-Single Output

FIG. **44**D illustrates the differential system **4402** wherein the inputs **4404** and **4406** are coupled to equal and opposite EM signal sources illustrated here as dipole antennas **4430** and **4432**. The output is taken from terminal **4408**.

5.3 Smoothing the Down-Converted Signal

The down-converted signal **1308**A may be smoothed by filtering as desired. The differential circuit **4444** implemented as a filter in FIG. **44**E illustrates but one example. Filtering may be accomplished in any of the described embodiments by hardware, firmware and software implementation as is well known by those skilled in the arts.

5.4 Load Impedance and Input/Output Buffering

Some of the characteristics of the down-converted signal **1308**A depend upon characteristics of a load placed on the down-converted signal **1308**A. For example, in an embodiment, when the down-converted signal **1308**A is coupled to a high impedance load, the charge that is applied to a holding module such as holding module **2706** in FIG. **27** or **2416** in FIG. **24**A during a pulse generally remains held by the holding module until the next pulse. This results in a substantially stair-step-like representation of the down-converted signal **1308**A as illustrated in FIG. **15**C, for example. A high impedance load enables the under-sampling system **1606** to accurately represent the voltage of the original unaffected input signal.

The down-converted signal **1308**A can be buffered with a high impedance amplifier, if desired.

Alternatively, or in addition to buffering the down-converted signal **1308**A, the input EM signal may be buffered or amplified by a low noise amplifier.

5.5 Modifying the Under-Sampling Signal Utilizing Feedback

FIG. **30** shows an embodiment of a system **3001** which uses down-converted signal **1308**A as feedback **3006** to control various characteristics of the under-sampling module **1606** to modify the down-converted signal **1308**A.

Generally, the amplitude of the down-converted signal **1308**A varies as a function of the frequency and phase differences between the EM signal **1304** and the under-sampling signal **1604**. In an embodiment, the down-converted signal **1308**A is used as the feedback **3006** to control the frequency and phase relationship between the EM signal **1304** and the under-sampling signal **1604**. This can be accomplished using the example block diagram shown in FIG. **32**A. The example circuit illustrated in FIG. **32**A can be included in the under-sampling signal module **3002**. Alternate implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Alternate implementations fall within the scope and spirit of the present invention. In this embodiment a state-machine is used for clarity, and is not limiting.

In the example of FIG. **32**A, a state machine **3204** reads an analog to digital converter, A/D **3202**, and controls a digital to analog converter (DAC) **3206**. In an embodiment, the state machine **3204** includes 2 memory locations, Previous and Current, to store and recall the results of reading A/D **3202**. In an embodiment, the state machine **3204** utilizes at least one memory flag.

DAC **3206** controls an input to a voltage controlled oscillator, VCO **3208**. VCO **3208** controls a frequency input of a pulse generator **3210**, which, in an embodiment, is substantially similar to the pulse generator shown in FIG. **29**J. The pulse generator **3210** generates the under-sampling signal **1604**.

In an embodiment, the state machine **3204** operates in accordance with the state machine flowchart **3220** in FIG. **32**B. The result of this operation is to modify the frequency and phase relationship between the under-sampling signal **1604** and the EM signal **1304**, to substantially maintain the amplitude of the down-converted signal **1308**A at an optimum level.

The amplitude of the down-converted signal **1308**A can be made to vary with the amplitude of the under-sampling signal **1604**. In an embodiment where Switch Module **2702** is a FET as shown in FIG. **28**A, wherein the gate **2804** receives the under-sampling signal **1604**, the amplitude of the under-sampling signal **1604** can determine the "on" resistance of the FET, which affects the amplitude of down-converted signal **1308**A. Under-sampling signal module **3002**, as shown in FIG. **32**C, can be an analog circuit that enables an automatic gain control function. Alternate implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Alternate implementations fall within the scope and spirit of the present invention.

III. DOWN-CONVERTING BY TRANSFERRING ENERGY

The energy transfer embodiments of the invention provide enhanced signal to noise ratios and sensitivity to very small signals, as well as permitting the down-converted signal to drive lower impedance loads unassisted. The energy transfer aspects of the invention are represented generally by **4506** in FIGS. **45**A and **45**B. Fundamental descriptions of how this is accomplished is presented step by step beginning with a comparison with an under-sampling system.

0.1 Energy Transfer Compared to Under-Sampling

Section II above disclosed methods and systems for down-converting an EM signal by under-sampling. The under-sampling systems utilize a sample and hold system controlled by an under-sampling signal. The under-sampling signal includes a train of pulses having negligible apertures that tend towards zero time in duration. The negligible aperture pulses minimize the amount of energy transferred from the EM signal. This protects the under-sampled EM signal from distortion or destruction. The negligible aperture pulses also make the sample and hold system a high impedance system. An advantage of under-sampling is that the high impedance input allows accurate voltage reproduction of the under-sampled EM signal. The methods and systems disclosed in Section II are thus useful for many situations including, but not limited to, monitoring EM signals without distorting or destroying them.

Because the under-sampling systems disclosed in Section II transfer only negligible amounts of energy, they are not suitable for all situations. For example, in radio communications, received radio frequency (RF) signals are typically very weak and must be amplified in order to distinguish them over noise. The negligible amounts of energy transferred by the under-sampling systems disclosed in Section II may not be sufficient to distinguish received RF signals over noise.

In accordance with an aspect of the invention, methods and systems are disclosed below for down-converting EM signals by transferring non-negligible amounts of energy from the EM signals. The resultant down-converted signals have sufficient energy to allow the down-converted signals to be distinguishable from noise. The resultant down-converted signals also have sufficient energy to drive lower impedance circuits without buffering.

Down-converting by transferring energy is introduced below in an incremental fashion to distinguish it from under-sampling. The introduction begins with further descriptions of under-sampling.

0.1.1 Review of Under-Sampling

FIG. **78**A illustrates an exemplary under-sampling system **7802** for down-converting an input EM signal **7804**. The under-sampling system **7802** includes a switching module **7806** and a holding module shown as a holding capacitance **7808**. An under-sampling signal **7810** controls the switch module **7806**. The under-sampling signal **7810** includes a train of pulses having negligible pulse widths that tend toward zero time. An example of a negligible pulse width or duration can be in the range of 1-10 psec for under-sampling a 900 MHZ signal. Any other suitable negligible pulse duration can be used as well, where accurate reproduction of the original unaffected input signal voltage is desired without substantially affecting the original input signal voltage.

In an under-sampling environment, the holding capacitance **7808** preferably has a small capacitance value. This allows the holding capacitance **7808** to substantially charge to the voltage of the input EM signal **7804** during the negligible apertures of the under-sampling signal pulses. For example, in an embodiment, the holding capacitance **7808** has a value in the range of 1 pF. Other suitable capacitance values can be used to achieve substantially the voltage of the original unaffected input signal. Various capacitances can be employed for certain effects, which are described below. The under-sampling system is coupled to a load **7812**. In FIG. **78**B, the load **7812** of FIG. **78**A is illustrated as a high impedance load **7818**. A high impedance load is one that is relatively insignificant to an output drive impedance of the system for a given output frequency. The high impedance load **7818** allows the holding capacitance **7808** to substantially maintain the charge accumulated during the under-sampling pulses.

FIGS. **79**A-F illustrate example timing diagrams for the under-sampling system **7802**. FIG. **79**A illustrates an example input EM signal **7804**.

FIG. **79**C illustrates an example under-sampling signal **7810**, including pulses **7904** having negligible apertures that tend towards zero time in duration.

FIG. **79**B illustrates the negligible effects to the input EM signal **7804** when under-sampled, as measured at a terminal **7814** of the under-sampling system **7802**. In FIG. **79**B, negligible distortions **7902** correlate with the pulses of the under-sampling signal **7810**. In this embodiment, the negligible distortions **7902** occur at different locations of subsequent cycles of the input EM signal **7804**. As a result, the input EM signal will be down-converted. The negligible distortions **7902** represent negligible amounts of energy, in the form of charge that is transferred to the holding capacitance **7808**.

When the load **7812** is a high impedance load, the holding capacitance **7808** does not significantly discharge between pulses **7904**. As a result, charge that is transferred to the holding capacitance **7808** during a pulse **7904** tends to "hold" the voltage value sampled constant at the terminal **7816** until the next pulse **7904**. When voltage of the input EM signal **7804** changes between pulses **7904**, the holding capacitance **7808** substantially attains the new voltage and the resultant voltage at the terminal **7816** forms a stair step pattern, as illustrated in FIG. **79**D.

FIG. **79**E illustrates the stair step voltage of FIG. **79**D on a compressed time scale. The stair step voltage illustrated in FIG. **79**E can be filtered to produce the signal illustrated in FIG. **79**F. The signals illustrated in FIGS. **79**D, E, and F have substantially all of the baseband characteristics of the input EM signal **7804** in FIG. **79**A, except that the signals illustrated in FIGS. **79**D, E, and F have been successfully down-converted.

Note that the voltage level of the down-converted signals illustrated in FIGS. **79**E and **79**F are substantially close to the voltage level of the input EM signal **7804**. The under-sampling system **7802** thus down-converts the input EM signal **7804** with reasonable voltage reproduction, without substantially affecting the input EM signal **7804**. But also note that the power available at the output is relatively negligible (e.g.

:V^2/R; ~5 mV and 1 MOhm), given the input EM signal **7804** would typically have a driving impedance, in an RF environment, of 50 Ohms (e.g.: V^2/R; ~5 mV and 50 Ohms).

0.1.1.1 Effects of Lowering the Impedance of the Load

Effects of lowering the impedance of the load **7812** are now described. FIGS. **80**A-E illustrate example timing diagrams for the under-sampling system **7802** when the load **7812** is a relatively low impedance load, one that is significant relative to the output drive impedance of the system for a given output frequency.

FIG. **80**A illustrates an example input EM signal **7804**, which is substantially similar to that illustrated in FIG. **79**A.

FIG. **80**C illustrates an example under-sampling signal **7810**, including pulses **8004** having negligible apertures that tend towards zero time in duration. The example under-sampling signal **7810** illustrated in FIG. **80**C is substantially similar to that illustrated in FIG. **79**C.

FIG. **80**B illustrates the negligible effects to the input EM signal **7804** when under-sampled, as measured at a terminal **7814** of the under-sampling system **7802**. In FIG. **80**B, negligible distortions **8002** correlate with the pulses **8004** of the under-sampling signal **7810** in FIG. **80**C. In this example, the negligible distortions **8002** occur at different locations of subsequent cycles of the input EM signal **7804**. As a result, the input EM signal **7804** will be down-converted. The negligible distortions **8002** represent negligible amounts of energy, in the form of charge that is transferred to the holding capacitance **7808**.

When the load **7812** is a low impedance load, the holding capacitance **7808** is significantly discharged by the load between pulses **8004** (FIG. **80**C). As a result, the holding capacitance **7808** cannot reasonably attain or "hold" the voltage of the original EM input signal **7804**, as was seen in the case of FIG. **79**D. Instead, the charge appears as the output illustrated in FIG. **80**D.

FIG. **80**E illustrates the output from FIG. **80**D on a compressed time scale. The output in FIG. **80**E can be filtered to produce the signal illustrated in FIG. **80**F. The down-converted signal illustrated in FIG. **80**F is substantially similar to the down-converted signal illustrated in FIG. **79**F, except that the signal illustrated in FIG. **80**F is substantially smaller in magnitude than the amplitude of the down-converted signal illustrated in FIG. **79**F. This is because the low impedance of the load **7812** prevents the holding capacitance **7808** from reasonably attaining or "holding" the voltage of the original EM input signal **7804**. As a result, the down-converted signal illustrated in FIG. **80**F cannot provide optimal voltage reproduction, and has relatively negligible power available at the output (e.g.: V^2/R; ~200V and 2 KOhms), given the input EM signal **7804** would typically have a driving impedance, in an RF environment, of 50 Ohms (e.g.: V^2/R; ~5 mV and 50 Ohms).

0.1.1.2 Effects of Increasing the Value of the Holding Capacitance

Effects of increasing the value of the holding capacitance **7808**, while having to drive a low impedance load **7812**, is now described. FIGS. **81**A-F illustrate example timing diagrams for the under-sampling system **7802** when the holding capacitance **7808** has a larger value, in the range of 18 pF for example.

FIG. **81** A illustrates an example input EM signal **7804**, which is substantially similar to that illustrated in FIGS. **79**A and **80**A.

FIG. **81**C illustrates an example under-sampling signal **7810**, including pulses **8104** having negligible apertures that tend towards zero time in duration. The example under-sampling signal **7810** illustrated in FIG. **81**C is substantially similar to that illustrated in FIGS. **79**C and **80**C.

FIG. **81**B illustrates the negligible effects to the input EM signal **7804** when under-sampled, as measured at a terminal **7814** of the under-sampling system **7802**. In FIG. **81**B, negligible distortions **8102** correlate with the pulses **8104** of the under-sampling signal **7810** in FIG. **81**C. Upon close inspection, the negligible distortions **8102** occur at different locations of subsequent cycles of the input EM signal **7804**. As a result, the input EM signal **7804** will be down-converted. The negligible distortions **8102** represent negligible amounts of energy, in the form of charge that is transferred to the holding capacitance **7808**.

FIG. **81**D illustrates the voltage measured at the terminal **7816**, which is a result of the holding capacitance **7808** attempting to attain and "hold" the original input EM signal voltage, but failing to do so, during the negligible apertures of the pulses **8104** illustrated in FIG. **81**C.

Recall that when the load **7812** is a low impedance load, the holding capacitance **7808** is significantly discharged by the load between pulses **8104** (FIG. **81**C), this again is seen in FIGS. **81**D and E. As a result, the holding capacitance **7808** cannot reasonably attain or "hold" the voltage of the original EM input signal **7804**, as was seen in the case of FIG. **79**D. Instead, the charge appears as the output illustrated in FIG. **81**D.

FIG. **81**E illustrates the down-converted signal **8106** on a compressed time scale. Note that the amplitude of the down-converted signal **8106** is significantly less than the amplitude of the down-converted signal illustrated in FIGS. **80**D and **80**E. This is due to the higher capacitive value of the holding capacitance **7808**. Generally, as the capacitive value increases, it requires more charge to increase the voltage for a given aperture. Because of the negligible aperture of the pulses **8104** in FIG. **81**C, there is insufficient time to transfer significant amounts of energy or charge from the input EM signal **7804** to the holding capacitance **7808**. As a result, the amplitudes attained by the holding capacitance **7808** are significantly less than the amplitudes of the down-converted signal illustrated in FIGS. **80**D and **80**E.

In FIGS. **80**E and **80**F, the output signal, non-filtered or filtered, cannot provide optimal voltage reproduction, and has relatively negligible power available at the output (e.g.: V^2/R; ~150V and 2 KOhms), given the input EM signal **7804** would typically have a driving impedance, in an RF environment, of 50 Ohms (e.g.: V^2/R; ~5 mV and 50 Ohms).

In summary, under-sampling systems, such as the under-sampling system **7802** illustrated in FIG. **78**, are well suited for down-converting EM signals with relatively accurate voltage reproduction. Also, they have a negligible affect on the original input EM signal. As illustrated above, however, the under-sampling systems, such as the under-sampling system **7802** illustrated in FIG. **78**, are not well suited for transferring energy or for driving lower impedance loads.

0.1.2 Introduction to Energy Transfer

In an embodiment, the present invention transfers energy from an EM signal by utilizing an energy transfer signal instead of an under-sampling signal. Unlike under-sampling signals that have negligible aperture pulses, the energy transfer signal includes a train of pulses having non-negligible apertures that tend away from zero. This provides more time to transfer energy from an EM input signal. One direct benefit is that the input impedance of the system is reduced so that practical impedance matching circuits can be implemented to further improve energy transfer and thus overall efficiency. The non-negligible transferred energy significantly improves the signal to noise ratio and sensitivity to very small signals,

as well as permitting the down-converted signal to drive lower impedance loads unassisted. Signals that especially benefit include low power ones typified by RF signals. One benefit of a non-negligible aperture is that phase noise within the energy transfer signal does not have as drastic of an effect on the down-converted output signal as under-sampling signal phase noise or conventional sampling signal phase noise does on their respective outputs.

FIG. **82**A illustrates an exemplary energy transfer system **8202** for down-converting an input EM signal **8204**. The energy transfer system **8202** includes a switching module **8206** and a storage module illustrated as a storage capacitance **8208**. The terms storage module and storage capacitance, as used herein, are distinguishable from the terms holding module and holding capacitance, respectively. Holding modules and holding capacitances, as used above, identify systems that store negligible amounts of energy from an under-sampled input EM signal with the intent of "holding" a voltage value. Storage modules and storage capacitances, on the other hand, refer to systems that store non-negligible amounts of energy from an input EM signal.

The energy transfer system **8202** receives an energy transfer signal **8210**, which controls the switch module **8206**. The energy transfer signal **8210** includes a train of energy transfer pulses having non-negligible pulse widths that tend away from zero time in duration. The non-negligible pulse widths can be any non-negligible amount. For example, the non-negligible pulse widths can be ½ of a period of the input EM signal. Alternatively, the non-negligible pulse widths can be any other fraction of a period of the input EM signal, or a multiple of a period plus a fraction. In an example embodiment, the input EM signal is approximately 900 MHZ and the non-negligible pulse width is approximately 550 pico seconds. Any other suitable non-negligible pulse duration can be used.

In an energy transfer environment, the storage module, illustrated in FIG. **82** as a storage capacitance **8208**, preferably has the capacity to handle the power being transferred, and to allow it to accept a non-negligible amount of power during a non-negligible aperture period. This allows the storage capacitance **8208** to store energy transferred from the input EM signal **8204**, without substantial concern for accurately reproducing the original, unaffected voltage level of the input EM signal **8204**. For example, in an embodiment, the storage capacitance **8208** has a value in the range of 18 pF. Other suitable capacitance values and storage modules can be used.

One benefit of the energy transfer system **8202** is that, even when the input EM signal **8204** is a very small signal, the energy transfer system **8202** transfers enough energy from the input EM signal **8204** that the input EM signal can be efficiently down-converted.

The energy transfer system **8202** is coupled to a load **8212**. Recall from the overview of under-sampling that loads can be classified as high impedance loads or low impedance loads. A high impedance load is one that is relatively insignificant to an output drive impedance of the system for a given output frequency. A low impedance load is one that is relatively significant. Another benefit of the energy transfer system **8202** is that the non-negligible amounts of transferred energy permit the energy transfer system **8202** to effectively drive loads that would otherwise be classified as low impedance loads in under-sampling systems and conventional sampling systems. In other words, the non-negligible amounts of transferred energy ensure that, even for lower impedance loads, the storage capacitance **8208** accepts and maintains sufficient energy or charge to drive the load **8202**. This is illustrated below in the timing diagrams of FIGS. **83**A-F.

FIGS. **83**A-F illustrate example timing diagrams for the energy transfer system **8202** in FIG. **82**. FIG. **83**A illustrates an example input EM signal **8302**.

FIG. **83**C illustrates an example under-sampling signal **8304**, including energy transfer pulses **8306** having non-negligible apertures that tend away from zero time in duration.

FIG. **83**B illustrates the effects to the input EM signal **8302**, as measured at a terminal **8214** in FIG. **82**A, when non-negligible amounts of energy are transfer from it. In FIG. **83**B, non-negligible distortions **8308** correlate with the energy transfer pulses **8306** in FIG. **83**C. In this example, the non-negligible distortions **8308** occur at different locations of subsequent cycles of the input EM signal **8302**. The non-negligible distortions **8308** represent non-negligible amounts of transferred energy, in the form of charge that is transferred to the storage capacitance **8208** in FIG. **82**.

FIG. **83**D illustrates a down-converted signal **8310** that is formed by energy transferred from the input EM signal **8302**.

FIG. **83**E illustrates the down-converted signal **8310** on a compressed time scale. The down-converted signal **8310** can be filtered to produce the down-converted signal **8312** illustrated in FIG. **83**F. The down-converted signal **8312** is similar to the down-converted signal illustrated in FIG. **79**F, except that the down-converted signal **8312** has substantially more power (e.g.: V^2/R; approximately (~) 2 mV and 2K Ohms) than the down-converted signal illustrated in FIG. **79**F (e.g.: V^2/R; ~5 mV and 1M Ohms). As a result, the down-converted signals **8310** and **8312** can efficiently drive lower impedance loads, given the input EM signal **8204** would typically have a driving impedance, in an RF environment, of 50 Ohms (V^2/R; ~5 mV and 50 Ohms).

The energy transfer aspects of the invention are represented generally by **4506** in FIGS. **45**A and **45**B.

1. Down-Converting an EM Signal to an IF EM Signal by Transferring Energy from the EM Signal at an Aliasing Rate

In an embodiment, the invention down-converts an EM signal to an IF signal by transferring energy from the EM signal at an aliasing rate. This embodiment is illustrated by **4514** in FIG. **45**B.

This embodiment can be implemented with any type of EM signal, including, but not limited to, modulated carrier signals and unmodulated carrier signals. This embodiment is described herein using the modulated carrier signal F_{MC} in FIG. **1** as an example. In the example, the modulated carrier signal F_{MC} is down-converted to an intermediate frequency (IF) signal F_{IF}. The intermediate frequency signal F_{IF} can be demodulated to a baseband signal F_{DMB} using conventional demodulation techniques. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention can be implemented to down-convert any EM signal, including, but not limited to, modulated carrier signals and unmodulated carrier signals.

The following sections describe methods for down-converting an EM signal to an IF signal F_{IF} by transferring energy from the EM signal at an aliasing rate. Exemplary structural embodiments for implementing the methods are also described. It should be understood that the invention is not limited to the particular embodiments described below. Equivalents, extensions, variations, deviations, etc., of the following will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such equivalents, extensions, variations, deviations, etc., are within the scope and spirit of the present invention.

The following sections include a high level discussion, example embodiments, and implementation examples.

1.1 High Level Description

This section (including its subsections) provides a high-level description of down-converting an EM signal to an IF signal F_{IF} by transferring energy, according to the invention. In particular, an operational process of down-converting the modulated carrier signal F_{MC} to the IF modulated carrier signal F_{IF}, by transferring energy, is described at a high-level. Also, a structural implementation for implementing this process is described at a high-level. This structural implementation is described herein for illustrative purposes, and is not limiting. In particular, the process described in this section can be achieved using any number of structural implementations, one of which is described in this section. The details of such structural implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

1.1.1 Operational Description

FIG. **46**B depicts a flowchart **4607** that illustrates an exemplary method for down-converting an EM signal to an intermediate signal F_{IF}, by transferring energy from the EM signal at an aliasing rate. The exemplary method illustrated in the flowchart **4607** is an embodiment of the flowchart **4601** in FIG. **46**A.

Any and all combinations of modulation techniques are valid for this invention. For ease of discussion, the digital AM carrier signal **616** is used to illustrate a high level operational description of the invention. Subsequent sections provide detailed flowcharts and descriptions for AM, FM and PM example embodiments. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention can be implemented to down-convert any type of EM signal, including any form of modulated carrier signal and unmodulated carrier signals.

The method illustrated in the flowchart **4607** is now described at a high level using the digital AM carrier signal **616** of FIG. **6**C. Subsequent sections provide detailed flowcharts and descriptions for AM, FM and PM example embodiments. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention can be implemented to down-convert any type of EM signal, including any form of modulated carrier signal and unmodulated carrier signals.

The process begins at step **4608**, which includes receiving an EM signal. Step **4608** is illustrated by the digital AM carrier signal **616**. The digital AM carrier signal **616** of FIG. **6**C is re-illustrated in FIG. **47**A for convenience. FIG. **47**E illustrates a portion of the digital AM carrier signal **616** on an expanded time scale.

Step **4610** includes receiving an energy transfer signal having an aliasing rate F_{AR}. FIG. **47**B illustrates an example energy transfer signal **4702**. The energy transfer signal **4702** includes a train of energy transfer pulses **4704** having non-negligible apertures **4701** that tend away from zero time duration. Generally, the apertures **4701** can be any time duration other than the period of the EM signal. For example, the apertures **4701** can be greater or less than a period of the EM signal. Thus, the apertures **4701** can be approximately 1/10, 1/4, 1/2, 3/4, etc., or any other fraction of the period of the EM signal. Alternatively, the apertures **4701** can be approximately equal to one or more periods of the EM signal plus 1/10, 1/4, 1/2, 3/4, etc., or any other fraction of a period of the EM signal. The apertures **4701** can be optimized based on one or more of a variety of criteria, as described in sections below.

The energy transfer pulses **4704** repeat at the aliasing rate. A suitable aliasing rate can be determined or selected as described below. Generally, when down-converting an EM signal to an intermediate signal, the aliasing rate is substantially equal to a difference frequency, which is described below, or substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency.

Step **4612** includes transferring energy from the EM signal at the aliasing rate to down-convert the EM signal to the intermediate signal F_{IF}. FIG. **47**C illustrates transferred energy **4706**, which is transferred from the EM signal during the energy transfer pulses **4704**. Because a harmonic of the aliasing rate occurs at an off-set of the frequency of the AM signal **616**, the pulses **4704** "walk through" the AM signal **616** at the off-set frequency. By "walking through" the AM signal **616**, the transferred energy **4706** forms an AM intermediate signal **4706** that is similar to the AM carrier signal **616**, except that the AM intermediate signal has a lower frequency than the AM carrier signal **616**. The AM carrier signal **616** can be down-converted to any frequency below the AM carrier signal **616** by adjusting the aliasing rate F_{AR}, as described below.

FIG. **47**D depicts the AM intermediate signal **4706** as a filtered output signal **4708**. In an alternative embodiment, the invention outputs a stair step, or non-filtered output signal. The choice between filtered, partially filtered and non-filtered output signals is generally a design choice that depends upon the application of the invention.

The intermediate frequency of the down-converted signal F_{IF}, which, in this example, is the intermediate signal **4706** and **4708**, can be determined from EQ. (2), which is reproduced below for convenience.

$$F_C = n \cdot F_{AR} \pm F_{IF} \quad \text{EQ. (2)}$$

A suitable aliasing rate F_{AR} can be determined in a variety of ways. An example method for determining the aliasing rate F_{AR}, is provided below. After reading the description herein, one skilled in the relevant art(s) will understand how to determine appropriate aliasing rates for EM signals, including ones in addition to the modulated carrier signals specifically illustrated herein.

In FIG. **48**, a flowchart **4801** illustrates an example process for determining an aliasing rate F_{AR}. But a designer may choose, or an application may dictate, that the values be determined in an order that is different than the illustrated order. The process begins at step **4802**, which includes determining, or selecting, the frequency of the EM signal. The frequency of the AM carrier signal **616** can be, for example, 901 MHZ.

Step **4804** includes determining, or selecting, the intermediate frequency. This is the frequency to which the EM signal will be down-converted The intermediate frequency can be determined, or selected, to match a frequency requirement of a down-stream demodulator. The intermediate frequency can be, for example, 1 MHZ.

Step **4806** includes determining the aliasing rate or rates that will down-convert the EM signal to the IF specified in step **4804**. EQ. (2) can be rewritten as EQ. (3):

$$n \cdot F_{AR} = F_C \pm F_{IF} \quad \text{EQ. (3)}$$

Which can be rewritten as EQ. (4):

$$n = \frac{F_C \pm F_{IF}}{F_{AR}} \quad \text{EQ. (4)}$$

or as EQ. (5):

$$F_{AR} = \frac{F_C \pm F_{IF}}{n} \quad \text{EQ. (5)}$$

$(F_C \pm F_{IF})$ can be defined as a difference value F_{DIFF}, as illustrated in EQ. (6):

$$(F_C \pm F_{IF}) = F_{DIFF} \quad \text{EQ. (6)}$$

EQ. (4) can be rewritten as EQ. (7):

$$n = \frac{F_{DIFF}}{F_{AR}} \quad \text{EQ. (7)}$$

From EQ. (7), it can be seen that, for a given n and a constant F_{AR}, F_{DIFF} is constant. For the case of $F_{DIFF}=F_C-F_{IF}$, and for a constant F_{DIFF}, as F_C increases, F_{IF} necessarily increases. For the case of $F_{DIFF}=F_C+F_{IF}$, and for a constant F_{DIFF}, as F_C increases, F_{IF} necessarily decreases. In the latter case of $F_{DIFF}=F_C+F_{IF}$, any phase or frequency changes on F_C correspond to reversed or inverted phase or frequency changes on F_{IF}. This is mentioned to teach the reader that if $F_{DIFF}=F_C+F_{IF}$ is used, the above effect will occur to the phase and frequency response of the modulated intermediate signal F_{IF}.

EQs. (2) through (7) can be solved for any valid n. A suitable n can be determined for any given difference frequency F_{DIFF} and for any desired aliasing rate $F_{AR(Desired)}$. EQs. (2) through (7) can be utilized to identify a specific harmonic closest to a desired aliasing rate $F_{AR(Desired)}$ that will generate the desired intermediate signal F_{IF}.

An example is now provided for determining a suitable n for a given difference frequency F_{DIFF} and for a desired aliasing rate $F_{AR(Desired)}$. For ease of illustration, only the case of (F_C-F_{IF}) is illustrated in the example below.

$$n = \frac{F_C - F_{IF}}{F_{AR(Desired)}} = \frac{F_{DIFF}}{F_{AR(Desired)}}$$

The desired aliasing rate $F_{AR(Desired)}$ can be, for example, 140 MHZ. Using the previous examples, where the carrier frequency is 901 MHZ and the IF is 1 MHZ, an initial value of n is determined as:

$$n = \frac{901\ \text{MHZ} - 1\ \text{MHZ}}{140\ \text{MHZ}} = \frac{900}{140} = 6.4$$

The initial value 6.4 can be rounded up or down to the valid nearest n, which was defined above as including (0.5, 1, 2, 3, . . .). In this example, 6.4 is rounded down to 6.0, which is inserted into EQ. (5) for the case of $(F_c-F_{IF})=F_{DIFF}$:

$$F_{AR} = \frac{F_C - F_{IF}}{n}$$

$$F_{AR} = \frac{901\ \text{MHZ} - 1\ \text{MHZ}}{6} = \frac{900\ \text{MHZ}}{6} = 150\ \text{MHZ}$$

In other words, transferring energy from a 901 MHZ EM carrier signal at 150 MHZ generates an intermediate signal at 1 MHZ. When the EM carrier signal is a modulated carrier signal, the intermediate signal will also substantially include the modulation. The modulated intermediate signal can be demodulated through any conventional demodulation technique.

Alternatively, instead of starting from a desired aliasing rate, a list of suitable aliasing rates can be determined from the modified form of EQ. (5). by solving for various values of n. Example solutions are listed below.

$$F_{AR} = \frac{(F_C - F_{IF})}{n} = \frac{F_{DIFF}}{n} = \frac{901\ \text{MHZ} - 1\ \text{MHZ}}{n} = \frac{900\ \text{MHZ}}{n}$$

Solving for n=0.5, 1, 2, 3,. 4, 5 and 6:
900 MHZ/0.5=1.8 GHZ (i.e., second harmonic);
900 MHZ/1=900 MHZ (i.e., fundamental frequency);
900 MHZ/2=450 MHZ (i.e., second sub-harmonic);
900 MhZ/3=300 MHZ (i.e., third sub-harmonic);
900 MHZ/4=225 MHZ (i.e., fourth sub-harmonic);
900 MHZ/5=180 MHZ(i.e., fifth sub-harmonic); and
900 MHZ/6=150 MHZ(i.e., sixth sub-harmonic).

The steps described above can be performed for the case of (F_C+F_{IF}) in a similar fashion. The results can be compared to the results obtained from the case of (F_C-F_{IF}) to determine which provides better result for an application.

In an embodiment, the invention down-converts an EM signal to a relatively standard IF in the range of, for example, 100 KHZ to 200 MHZ. In another embodiment, referred to herein as a small off-set implementation, the invention down-converts an EM signal to a relatively low frequency of, for example, less than 100 KHZ. In another embodiment, referred to herein as a large off-set implementation, the invention down-converts an EM signal to a relatively higher IF signal, such as, for example, above 200 MHZ.

The various off-set implementations provide selectivity for different applications. Generally, lower data rate applications can operate at lower intermediate frequencies. But higher intermediate frequencies can allow more information to be supported for a given modulation technique.

In accordance with the invention, a designer picks an optimum information bandwidth for an application and an optimum intermediate frequency to support the baseband signal. The intermediate frequency should be high enough to support the bandwidth of the modulating baseband signal F_{MB}.

Generally, as the aliasing rate approaches a harmonic or sub-harmonic frequency of the EM signal, the frequency of the down-converted IF signal decreases. Similarly, as the aliasing rate moves away from a harmonic or sub-harmonic frequency of the EM signal, the IF increases.

Aliased frequencies occur above and below every harmonic of the aliasing frequency. In order to avoid mapping other aliasing frequencies in the band of the aliasing frequency (IF) of interest, the IF of interest should not be near one half the aliasing rate.

As described in example implementations below, an aliasing module, including a universal frequency translator (UFT) module built in accordance with the invention provides a wide range of flexibility in frequency selection and can thus be implemented in a wide range of applications. Conventional systems cannot easily offer, or do not allow, this level of flexibility in frequency selection.

1.1.2 Structural Description

FIG. **63** illustrates a block diagram of an energy transfer system **6302** according to an embodiment of the invention. The energy transfer system **6302** is an example embodiment of the generic aliasing system **1302** in FIG. **13**. The energy

transfer system **6302** includes an energy transfer module **6304**. The energy transfer module **6304** receives the EM signal **1304** and an energy transfer signal **6306**, which includes a train of energy transfer pulses having non-negligible apertures that tend away from zero time in duration, occurring at a frequency equal to the aliasing rate F_{AR}. The energy transfer signal **6306** is an example embodiment of the aliasing signal **1310** in FIG. **13**. The energy transfer module **6304** transfers energy from the EM signal **1304** at the aliasing rate F_{AR} of the energy transfer signal **6306**.

Preferably, the energy transfer module **6304** transfers energy from the EM signal **1304** to down-convert it to the intermediate signal F_{IF} in the manner shown in the operational flowchart **4607** of FIG. **46**B. But it should be understood that the scope and spirit of the invention includes other structural embodiments for performing the steps of the flowchart **4607**. The specifics of the other structural embodiments will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

The operation of the energy transfer system **6302** is now described in detail with reference to the flowchart **4607** and to the timing diagrams illustrated in FIGS. **47**A-E. In step **4608**, the energy transfer module **6304** receives the AM carrier signal **616**. In step **4610**, the energy transfer module **6304** receives the energy transfer signal **4702**. In step **4612**, the energy transfer module **6304** transfers energy from the AM carrier signal **616** at the aliasing rate to down-convert the AM carrier signal **616** to the intermediate signal **4706** or **4708**.

Example implementations of the energy transfer system **6302** are provided in Sections 4 and 5 below.

1.2 Example Embodiments

Various embodiments related to the method(s) and structure(s) described above are presented in this section (and its subsections). These embodiments are described herein for purposes of illustration, and not limitation. The invention is not limited to these embodiments. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

The method for down-converting the EM signal **1304** by transferring energy can be implemented with any type of EM signal, including modulated carrier signals and unmodulated carrier signals. For example, the method of the flowchart **4601** can be implemented to down-convert AM signals, FM signals, PM signals, etc., or any combination thereof. Operation of the flowchart **4601** of FIG. **46**A is described below for down-converting AM, FM and PM. The down-conversion descriptions include down-converting to intermediate signals, directly down-converting to demodulated baseband signals, and down-converting FM signals to non-FM signals. The exemplary descriptions below are intended to facilitate an understanding of the present invention. The present invention is not limited to or by the exemplary embodiments below.

1.2.1 First Example Embodiment: Amplitude Modulation

1.2.1.1 Operational Description

Operation of the exemplary process of the flowchart **4607** in FIG. **46**B is described below for the analog AM carrier signal **516**, illustrated in FIG. **5**C, and for the digital AM carrier signal **616**, illustrated in FIG. **6**C.

1.2.1.1.1 Analog AM Carrier Signal

A process for down-converting the analog AM carrier signal **516** in FIG. **5**C to an analog AM intermediate signal is now described for the flowchart **4607** in FIG. **46**B. The analog AM carrier signal **516** is re-illustrated in FIG. **50**A for convenience. For this example, the analog AM carrier signal **516** oscillates at approximately 901 MHZ. In FIG. **50**B, an analog AM carrier signal **5004** illustrates a portion of the analog AM carrier signal **516** on an expanded time scale.

The process begins at step **4608**, which includes receiving the EM signal. This is represented by the analog AM carrier signal **516**.

Step **4610** includes receiving an energy transfer signal having an aliasing rate F_{AR}. FIG. **50**C illustrates an example energy transfer signal **5006** on approximately the same time scale as FIG. **50**B. The energy transfer signal **5006** includes a train of energy transfer pulses **5007** having non-negligible apertures **5009** that tend away from zero time in duration. The energy transfer pulses **5007** repeat at the aliasing rate F_{AR}, which is determined or selected as previously described. Generally, when down-converting to an intermediate signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency F_{DIFF}.

Step **4612** includes transferring energy from the EM signal at the aliasing rate to down-convert the EM signal to an intermediate signal F_{IF}. In FIG. **50**D, an affected analog AM carrier signal **5008** illustrates effects of transferring energy from the analog AM carrier signal **516** at the aliasing rate F_{AR}. The affected analog AM carrier signal **5008** is illustrated on substantially the same time scale as FIGS. **50**B and **50**C.

FIG. **50**E illustrates a down-converted AM intermediate signal **5012**, which is generated by the down-conversion process. The AM intermediate signal **5012** is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

The down-converted signal **5012** includes portions **5010**A, which correlate with the energy transfer pulses **5007** in FIG. **50**C, and portions **5010**B, which are between the energy transfer pulses **5007**. Portions **5010**A represent energy transferred from the AM analog signal **516** to a storage device, while simultaneously driving an output load. The portions **5010**A occur when a switching module is closed by the energy transfer pulses **5007**. Portions **5010**B represent energy stored in a storage device continuing to drive the load. Portions **5010**B occur when the switching module is opened after energy transfer pulses **5007**.

Because a harmonic of the aliasing rate is off-set from the analog AM carrier signal **516**, the energy transfer pulses **5007** "walk through" the analog AM carrier signal **516** at the difference frequency F_{DIFF}. In other words, the energy transfer pulses **5007** occur at different locations of subsequent cycles of the AM carrier signal **516**. As a result, the energy transfer pulses **5007** capture varying amounts of energy from the analog AM carrier signal **516**, as illustrated by portions **5010**A, which provides the AM intermediate signal **5012** with an oscillating frequency F_{IF}.

In FIG. **50**F, an AM intermediate signal **5014** illustrates the AM intermediate signal **5012** on a compressed time scale. In FIG. **50**G, an AM intermediate signal **5016** represents a filtered version of the AM intermediate signal **5014**. The AM intermediate signal **5016** is substantially similar to the AM carrier signal **516**, except that the AM intermediate signal **5016** is at the intermediate frequency. The AM intermediate signal **5016** can be demodulated through any conventional demodulation technique.

The present invention can output the unfiltered AM intermediate signal **5014**, the filtered AM intermediate signal **5016**, a partially filtered AM intermediate signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention.

The signals referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the

AM intermediate signals **5014** in FIG. **50**F and **5016** in FIG. **50**G illustrate that the AM carrier signal **516** was successfully down-converted to an intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.1.1.2 Digital AM Carrier Signal

A process for down-converting the digital AM carrier signal **616** to a digital AM intermediate signal is now described for the flowchart **4607** in FIG. **46**B. The digital AM carrier signal **616** is re-illustrated in FIG. **51**A for convenience. For this example, the digital AM carrier signal **616** oscillates at approximately 901 MHZ. In FIG. **51**B, a digital AM carrier signal **5104** illustrates a portion of the digital AM carrier signal **616** on an expanded time scale.

The process begins at step **4608**, which includes receiving an EM signal. This is represented by the digital AM carrier signal **616**.

Step **4610** includes receiving an energy transfer signal having an aliasing rate F_{AR}. FIG. **51**C illustrates an example energy transfer signal **5106** on substantially the same time scale as FIG. **51**B. The energy transfer signal **5106** includes a train of energy transfer pulses **5107** having non-negligible apertures **5109** that tend away from zero time in duration. The energy transfer pulses **5107** repeat at the aliasing rate, which is determined or selected as previously described. Generally, when down-converting to an intermediate signal, the aliasing rate is substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency F_{DIFF}.

Step **4612** includes transferring energy from the EM signal at the aliasing rate to down-convert the EM signal to the intermediate signal F_{IF}. In FIG. **51**D, an affected digital AM carrier signal **5108** illustrates effects of transferring energy from the digital AM carrier signal **616** at the aliasing rate F_{AR}. The affected digital AM carrier signal **5108** is illustrated on substantially the same time scale as FIGS. **51**B and **51**C.

FIG. **51** E illustrates a down-converted AM intermediate signal **5112**, which is generated by the down-conversion process. The AM intermediate signal **5112** is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

The down-converted signal **5112** includes portions **5110**A, which correlate with the energy transfer pulses **5107** in FIG. **51**C, and portions **5110**B, which are between the energy transfer pulses **5107**. Portions **5110**A represent energy transferred from the digital AM carrier signal **616** to a storage device, while simultaneously driving an output load. The portions **5110**A occur when a switching module is closed by the energy transfer pulses **5107**. Portions **5110**B represent energy stored in a storage device continuing to drive the load. Portions **5110**B occur when the switching module is opened after energy transfer pulses **5107**.

Because a harmonic of the aliasing rate is off-set from the frequency of the digital AM carrier signal **616**, the energy transfer pulses **5107** "walk through" the digital AM signal **616** at the difference frequency F_{DIFF}. In other words, the energy transfer pulse **5107** occur at different locations of subsequent cycles of the digital AM carrier signal **616**. As a result, the energy transfer pulses **5107** capture varying amounts of energy from the digital AM carrier signal **616**, as illustrated by portions **5110**, which provides the AM intermediate signal **5112** with an oscillating frequency F_{IF}.

In FIG. **51**F, a digital AM intermediate signal **5114** illustrates the AM intermediate signal **5112** on a compressed time scale. In FIG. **51** G, an AM intermediate signal **5116** represents a filtered version of the AM intermediate signal **5114**. The AM intermediate signal **5116** is substantially similar to the AM carrier signal **616**, except that the AM intermediate signal **5116** is at the intermediate frequency. The AM intermediate signal **5116** can be demodulated through any conventional demodulation technique.

The present invention can output the unfiltered AM intermediate signal **5114**, the filtered AM intermediate signal **5116**, a partially filtered AM intermediate signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention.

The signals referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the AM intermediate signals **5114** in FIG. **51**F and **5116** in FIG. **51**G illustrate that the AM carrier signal **616** was successfully down-converted to an intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.1.2 Structural Description

The operation of the energy transfer system **6302** is now described for the analog AM carrier signal **516**, with reference to the flowchart **4607** and to the timing diagrams in FIGS. **50**A-G. In step **4608**, the energy transfer module **6304** receives the analog AM carrier signal **516**. In step **4610**, the energy transfer module **6304** receives the energy transfer signal **5006**. In step **4612**, the energy transfer module **6304** transfers energy from the analog AM carrier signal **516** at the aliasing rate of the energy transfer signal **5006**, to down-convert the analog AM carrier signal **516** to the AM intermediate signal **5012**.

The operation of the energy transfer system **6302** is now described for the digital AM carrier signal **616**, with reference to the flowchart **1401** and the timing diagrams in FIGS. **51**A-G. In step **4608**, the energy transfer module **6304** receives the digital AM carrier signal **616**. In step **4610**, the energy transfer module **6304** receives the energy transfer signal **5106**. In step **4612**, the energy transfer module **6304** transfers energy from the digital AM carrier signal **616** at the aliasing rate of the energy transfer signal **5106**, to down-convert the digital AM carrier signal **616** to the AM intermediate signal **5112**.

Example embodiments of the energy transfer module **6304** are disclosed in Sections 4 and 5 below.

1.2.2 Second Example Embodiment: Frequency Modulation

1.2.2.1 Operational Description

Operation of the exemplary process of the flowchart **4607** in FIG. **46**B is described below for the analog FM carrier signal **716**, illustrated in FIG. **7**C, and for the digital FM carrier signal **816**, illustrated in FIG. **8**C.

1.2.2.1.1 Analog FM Carrier Signal

A process for down-converting the analog FM carrier signal **716** in FIG. **7**C to an FM intermediate signal is now described for the flowchart **4607** in FIG. **46**B. The analog FM carrier signal **716** is re-illustrated in FIG. **52**A for convenience. For this example, the analog FM carrier signal **716** oscillates around approximately 901 MHZ. In FIG. **52**B, an analog FM carrier signal **5204** illustrates a portion of the analog FM carrier signal **716** on an expanded time scale.

The process begins at step **4608**, which includes receiving an EM signal. This is represented by the analog FM carrier signal **716**.

Step **4610** includes receiving an energy transfer signal having an aliasing rate F_{AR}. FIG. **52**C illustrates an example energy transfer signal **5206** on approximately the same time scale as FIG. **52**B. The energy transfer signal **5206** includes a train of energy transfer pulses **5207** having non-negligible apertures that tend away from zero time in duration. The energy transfer pulses **5207** repeat at the aliasing rate F_{AR}, which is determined or selected as previously described. Generally, when down-converting to an intermediate signal, the

aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency F_{DIFF}.

Step **4612** includes transferring energy from the EM signal at the aliasing rate to down-convert the EM signal to an intermediate signal F_{IF}. In FIG. **52**D, an affected analog FM carrier signal **5208** illustrates effects of transferring energy from the analog FM carrier signal **716** at the aliasing rate F_{AR}. The affected analog FM carrier signal **5208** is illustrated on substantially the same time scale as FIGS. **52**B and **52**C.

FIG. **52**E illustrates a down-converted FM intermediate signal **5212**, which is generated by the down-conversion process. The FM intermediate signal **5212** is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

The down-converted signal **5212** includes portions **5210**A, which correlate with the energy transfer pulses **5207** in FIG. **52**C, and portions **5210**B, which are between the energy transfer pulses **5207**. Portions **5210**A represent energy transferred from the analog FM carrier signal **716** to a storage device, while simultaneously driving an output load. The portions **5210**A occur when a switching module is closed by the energy transfer pulses **5207**. Portions **5210**B represent energy stored in a storage device continuing to drive the load. Portions **5210**B occur when the switching module is opened after energy transfer pulses **5207**.

Because a harmonic of the aliasing rate is off-set from the frequency of the analog FM carrier signal **716**, the energy transfer pulses **5207** "walk through" the analog FM carrier signal **716** at the difference frequency F_{DIFF}. In other words, the energy transfer pulse **5207** occur at different locations of subsequent cycles of the analog FM carrier signal **716**. As a result, the energy transfer pulses **5207** capture varying amounts of energy from the analog FM carrier signal **716**, as illustrated by portions **5210**, which provides the FM intermediate signal **5212** with an oscillating frequency F_{IF}.

In FIG. **52**F, an analog FM intermediate signal **5214** illustrates the FM intermediate signal **5212** on a compressed time scale. In FIG. **52**G, an FM intermediate signal **5216** represents a filtered version of the FM intermediate signal **5214**. The FM intermediate signal **5216** is substantially similar to the analog FM carrier signal **716**, except that the FM intermediate signal **5216** is at the intermediate frequency. The FM intermediate signal **5216** can be demodulated through any conventional demodulation technique.

The present invention can output the unfiltered FM intermediate signal **5214**, the filtered FM intermediate signal **5216**, a partially filtered FM intermediate signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention.

The signals referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the FM intermediate signals **5214** in FIG. **52**F and **5216** in FIG. **52**G illustrate that the FM carrier signal **716** was successfully down-converted to an intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.2.1.2 Digital FM Carrier Signal

A process for down-converting the digital FM carrier signal **816** in FIG. **8**C is now described for the flowchart **4607** in FIG. **46**B. The digital FM carrier signal **816** is re-illustrated in FIG. **53**A for convenience. For this example, the digital FM carrier signal **816** oscillates at approximately 901 MHZ. In FIG. **53**B, a digital FM carrier signal **5304** illustrates a portion of the digital FM carrier signal **816** on an expanded time scale.

The process begins at step **4608**, which includes receiving an EM signal. This is represented by the digital FM carrier signal **816**.

Step **4610** includes receiving an energy transfer signal having an aliasing rate F_{AR}. FIG. **53**C illustrates an example energy transfer signal **5306** on substantially the same time scale as FIG. **53**B. The energy transfer signal **5306** includes a train of energy transfer pulses **5307** having non-negligible apertures **5309** that tend away from zero time in duration. The energy transfer pulses **5307** repeat at the aliasing rate, which is determined or selected as previously described. Generally, when down-converting to an intermediate signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency F_{DIFF}.

Step **4612** includes transferring energy from the EM signal at the aliasing rate to down-convert the EM signal to the an intermediate signal F_{IF}. In FIG. **53**D, an affected digital FM carrier signal **5308** illustrates effects of transferring energy from the digital FM carrier signal **816** at the aliasing rate F_{AR}. The affected digital FM carrier signal **5308** is illustrated on substantially the same time scale as FIGS. **53**B and **53**C.

FIG. **53**E illustrates a down-converted FM intermediate signal **5312**, which is generated by the down-conversion process. The down-converted signal **5312** includes portions **5310**A, which correlate with the energy transfer pulses **5307** in FIG. **53**C, and portions **5310**B, which are between the energy transfer pulses **5307**. Down-converted signal **5312** is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

Portions **5310**A represent energy transferred from the digital FM carrier signal **816** to a storage device, while simultaneously driving an output load. The portions **5310**A occur when a switching module is closed by the energy transfer pulses **5307**.

Portions **5310**B represent energy stored in a storage device continuing to drive the load. Portions **5310**B occur when the switching module is opened after energy transfer pulses **5307**.

Because a harmonic of the aliasing rate is off-set from the frequency of the digital FM carrier signal **816**, the energy transfer pulses **5307** "walk through" the digital FM carrier signal **816** at the difference frequency F_{DIFF}. In other words, the energy transfer pulse **5307** occur at different locations of subsequent cycles of the digital FM carrier signal **816**. As a result, the energy transfer pulses **5307** capture varying amounts of energy from the digital FM carrier signal **816**, as illustrated by portions **5310**, which provides the FM intermediate signal **5312** with an oscillating frequency F_{IF}.

In FIG. **53**F, a digital FM intermediate signal **5314** illustrates the FM intermediate signal **5312** on a compressed time scale. In FIG. **53**G, an FM intermediate signal **5316** represents a filtered version of the FM intermediate signal **5314**. The FM intermediate signal **5316** is substantially similar to the digital FM carrier signal **816**, except that the FM intermediate signal **5316** is at the intermediate frequency. The FM intermediate signal **5316** can be demodulated through any conventional demodulation technique.

The present invention can output the unfiltered FM intermediate signal **5314**, the filtered FM intermediate signal **5316**, a partially filtered FM intermediate signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention.

The signals referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the FM intermediate signals **5314** in FIG. **53**F and **5316** in FIG. **53**G illustrate that the FM carrier signal **816** was successfully down-converted to an intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.2.2 Structural Description

The operation of the energy transfer system **6302** is now described for the analog FM carrier signal **716**, with reference to the flowchart **4607** and the timing diagrams in FIGS. **52**A-G. In step **4608**, the energy transfer module **6304** receives the analog FM carrier signal **716**. In step **4610**, the energy transfer module **6304** receives the energy transfer signal **5206**. In step **4612**, the energy transfer module **6304** transfers energy from the analog FM carrier signal **716** at the aliasing rate of the energy transfer signal **5206**, to down-convert the analog FM carrier signal **716** to the FM intermediate signal **5212**.

The operation of the energy transfer system **6302** is now described for the digital FM carrier signal **816**, with reference to the flowchart **4607** and the timing diagrams in FIGS. **53**A-G. In step **4608**, the energy transfer module **6304** receives the digital FM carrier signal **816**. In step **4610**, the energy transfer module **6304** receives the energy transfer signal **5306**. In step **4612**, the energy transfer module **6304** transfers energy from the digital FM carrier signal **816** at the aliasing rate of the energy transfer signal **5306**, to down-convert the digital FM carrier signal **816** to the FM intermediate signal **5212**.

Example embodiments of the energy transfer module **6304** are disclosed in Sections 4 and 5 below.

1.2.3 Third Example Embodiment: Phase Modulation

1.2.3.1 Operational Description

Operation of the exemplary process of the flowchart **4607** in FIG. **46**B is described below for the analog PM carrier signal **916**, illustrated in FIG. **9**C, and for the digital PM carrier signal **1016**, illustrated in FIG. **10**C.

1.2.3.1.1 Analog PM Carrier Signal

A process for down-converting the analog PM carrier signal **916** in FIG. **9**C to an analog PM intermediate signal is now described for the flowchart **4607** in FIG. **46**B. The analog PM carrier signal **916** is re-illustrated in FIG. **54**A for convenience. For this example, the analog PM carrier signal **916** oscillates at approximately 901 MHZ. In FIG. **54**B, an analog PM carrier signal **5404** illustrates a portion of the analog PM carrier signal **916** on an expanded time scale.

The process begins at step **4608**, which includes receiving an EM signal. This is represented by the analog PM carrier signal **916**.

Step **4610** includes receiving an energy transfer signal having an aliasing rate F_{AR}. FIG. **54**C illustrates an example energy transfer signal **5406** on approximately the same time scale as FIG. **54**B. The energy transfer signal **5406** includes a train of energy transfer pulses **5407** having non-negligible apertures that tend away from zero time in duration. The energy transfer pulses **5407** repeat at the aliasing rate, which is determined or selected as previously described. Generally, when down-converting to an intermediate signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency F_{DIFF}.

Step **4612** includes transferring energy from the EM signal at the aliasing rate to down-convert the EM signal to the IF signal F_{IF}. In FIG. **54**D, an affected analog PM carrier signal **5408** illustrates effects of transferring energy from the analog PM carrier signal **916** at the aliasing rate F_{AR}. The affected analog PM carrier signal **5408** is illustrated on substantially the same time scale as FIGS. **54**B and **54**C.

FIG. **54**E illustrates a down-converted PM intermediate signal **5412**, which is generated by the down-conversion process. The down-converted PM intermediate signal **5412** includes portions **5410**A, which correlate with the energy transfer pulses **5407** in FIG. **54**C, and portions **5410**B, which are between the energy transfer pulses **5407**. Down-converted signal **5412** is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

Portions **5410**A represent energy transferred from the analog PM carrier signal **916** to a storage device, while simultaneously driving an output load. The portions **5410**A occur when a switching module is closed by the energy transfer pulses **5407**.

Portions **5410**B represent energy stored in a storage device continuing to drive the load. Portions **5410**B occur when the switching module is opened after energy transfer pulses **5407**.

Because a harmonic of the aliasing rate is off-set from the frequency of the analog PM carrier signal **716**, the energy transfer pulses **5407** "walk through" the analog PM carrier signal **916** at the difference frequency F_{DIFF}. In other words, the energy transfer pulse **5407** occur at different locations of subsequent cycles of the analog PM carrier signal **916**. As a result, the energy transfer pulses **5407** capture varying amounts of energy from the analog PM carrier signal **916**, as illustrated by portions **5410**, which provides the PM intermediate signal **5412** with an oscillating frequency F_{IF}.

In FIG. **54**F, an analog PM intermediate signal **5414** illustrates the PM intermediate signal **5412** on a compressed time scale. In FIG. **54**G, an PM intermediate signal **5416** represents a filtered version of the PM intermediate signal **5414**. The PM intermediate signal **5416** is substantially similar to the analog PM carrier signal **916**, except that the PM intermediate signal **5416** is at the intermediate frequency. The PM intermediate signal **5416** can be demodulated through any conventional demodulation technique.

The present invention can output the unfiltered PM intermediate signal **5414**, the filtered PM intermediate signal **5416**, a partially filtered PM intermediate signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention.

The signals referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the PM intermediate signals **5414** in FIG. **54**F and **5416** in FIG. **54**G illustrate that the PM carrier signal **916** was successfully down-converted to an intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.3.1.2 Digital PM Carrier Signal

A process for down-converting the digital PM carrier signal **1016** in FIG. **10**C to a digital PM signal is now described for the flowchart **3607** in FIG. **46**B. The digital PM carrier signal **1016** is re-illustrated in FIG. **55**A for convenience. For this example, the digital PM carrier signal **1016** oscillates at approximately 901 MHZ. In FIG. **55**B, a digital PM carrier signal **5504** illustrates a portion of the digital PM carrier signal **1016** on an expanded time scale.

The process begins at step **4608**, which includes receiving an EM signal. This is represented by the digital PM carrier signal **1016**.

Step **4610** includes receiving an energy transfer signal having an aliasing rate F_{AR}. FIG. **55**C illustrates an example energy transfer signal **5506** on substantially the same time scale as FIG. **55**B. The energy transfer signal **5506** includes a train of energy transfer pulses **5507** having non-negligible apertures **5509** that tend away from zero time in duration. The energy transfer pulses **5507** repeat at an aliasing rate, which is determined or selected as previously described. Generally, when down-converting to an intermediate signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the difference frequency F_{DIFF}.

Step **4612** includes transferring energy from the EM signal at the aliasing rate to down-convert the EM signal to an

intermediate signal F_{IF}. In FIG. **55**D, an affected digital PM carrier signal **5508** illustrates effects of transferring energy from the digital PM carrier signal **1016** at the aliasing rate F_{AR}. The affected digital PM carrier signal **5508** is illustrated on substantially the same time scale as FIGS. **55**B and **55**C.

FIG. **55**E illustrates a down-converted PM intermediate signal **5512**, which is generated by the down-conversion process. The down-converted PM intermediate signal **5512** includes portions **5510**A, which correlate with the energy transfer pulses **5507** in FIG. **55**C, and portions **5510**B, which are between the energy transfer pulses **5507**. Down-converted signal **5512** is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

Portions **5510**A represent energy transferred from the digital PM carrier signal **1016** to a storage device, while simultaneously driving an output load. The portions **5510**A occur when a switching module is closed by the energy transfer pulses **5507**.

Portions **5510**B represent energy stored in a storage device continuing to drive the load. Portions **5510**B occur when the switching module is opened after energy transfer pulses **5507**.

Because a harmonic of the aliasing rate is off-set from the frequency of the digital PM carrier signal **716**, the energy transfer pulses **5507** "walk through" the digital PM carrier signal **1016** at the difference frequency F_{DIFF}. In other words, the energy transfer pulse **5507** occur at different locations of subsequent cycles of the digital PM carrier signal **1016**. As a result, the energy transfer pulses **5507** capture varying amounts of energy from the digital PM carrier signal **1016**, as illustrated by portions **5510**, which provides the PM intermediate signal **5512** with an oscillating frequency F_{IF}.

In FIG. **55**F, a digital PM intermediate signal **5514** illustrates the PM intermediate signal **5512** on a compressed time scale. In FIG. **55**G, an PM intermediate signal **5516** represents a filtered version of the PM intermediate signal **5514**. The PM intermediate signal **5516** is substantially similar to the digital PM carrier signal **1016**, except that the PM intermediate signal **5516** is at the intermediate frequency. The PM intermediate signal **5516** can be demodulated through any conventional demodulation technique.

The present invention can output the unfiltered PM intermediate signal **5514**, the filtered PM intermediate signal **5516**, a partially filtered PM intermediate signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention.

The signals referred to herein illustrate frequency down-conversion in accordance with the invention. For example, the PM intermediate signals **5514** in FIG. **55**F and **5516** in FIG. **55**G illustrate that the PM carrier signal **1016** was successfully down-converted to an intermediate signal by retaining enough baseband information for sufficient reconstruction.

1.2.3.2 Structural Description

Operation of the energy transfer system **6302** is now described for the analog PM carrier signal **916**, with reference to the flowchart **4607** and the timing diagrams in FIGS. **54**A-G. In step **4608**, the energy transfer module **6304** receives the analog PM carrier signal **916**. In step **4610**, the energy transfer module **6304** receives the energy transfer signal **5406**. In step **4612**, the energy transfer module **6304** transfers energy from the analog PM carrier signal **916** at the aliasing rate of the energy transfer signal **5406**, to down-convert the analog PM carrier signal **916** to the PM intermediate signal **5412**.

Operation of the energy transfer system **6302** is now described for the digital PM carrier signal **1016**, with reference to the flowchart **1401** and the timing diagrams in FIGS. **55**A-G. In step **4608**, the energy transfer module **6304** receives the digital PM carrier signal **1016**. In step **4610**, the energy transfer module **6304** receives the energy transfer signal **5506**. In step **4612**, the energy transfer module **6304** transfers energy from the digital PM carrier signal **1016** at the aliasing rate of the energy transfer signal **5506**, to down-convert the digital PM carrier signal **1016** to the PM intermediate signal **5512**.

Example embodiments of the energy transfer module **6304** are disclosed in Sections 4 and 5 below.

1.2.4 Other Embodiments

The embodiments described above are provided for purposes of illustration. These embodiments are not intended to limit the invention. Alternate embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate embodiments fall within the scope and spirit of the present invention. Example implementations of the energy transfer module **6304** are disclosed in Sections 4 and 5 below.

1.3 Implementation Examples

Exemplary operational and/or structural implementations related to the method(s), structure(s), and/or embodiments described above are presented in Sections 4 and 5 below. These implementations are presented for purposes of illustration, and not limitation. The invention is not limited to the particular implementation examples described therein. Alternate implementations (including equivalents, extensions, variations, deviations, etc., of those described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

2. Directly Down-Converting an EM Signal to an Demodulated Baseband Signal by Transferring Energy from the EM Signal

In an embodiment, the invention directly down-converts an EM signal to a baseband signal, by transferring energy from the EM signal. This embodiment is referred to herein as direct-to-data down-conversion and is illustrated by **4516** in FIG. **45**B.

This embodiment can be implemented with modulated and unmodulated EM signals. This embodiment is described herein using the modulated carrier signal FMC in FIG. **1**, as an example. In the example, the modulated carrier signal F_{MC} is directly down-converted to the demodulated baseband signal F_{DMB}. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention can be implemented to down-convert any EM signal, including but not limited to, modulated carrier signals and unmodulated carrier signals.

The following sections describe methods for directly down-converting the modulated carrier signal F_{MC} to the demodulated baseband signal F_{DMB}. Exemplary structural embodiments for implementing the methods are also described. It should be understood that the invention is not limited to the particular embodiments described below. Equivalents, extensions, variations, deviations, etc., of the following will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such equivalents, extensions, variations, deviations, etc., are within the scope and spirit of the present invention.

The following sections include a high level discussion, example embodiments, and implementation examples.

2.1 High Level Description

This section (including its subsections) provides a high-level description of transferring energy from the modulated carrier signal F_{MC} to directly down-convert the modulated

carrier signal F_{MC} to the demodulated baseband signal F_{DMB}, according to the invention. In particular, an operational process of directly down-converting the modulated carrier signal F_{MC} to the demodulated baseband signal F_{DMB} is described at a high-level. Also, a structural implementation for implementing this process is described at a high-level. The structural implementation is described herein for illustrative purposes, and is not limiting. In particular, the process described in this section can be achieved using any number of structural implementations, one of which is described in this section. The details of such structural implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

2.1.1 Operational Description

FIG. **46**C depicts a flowchart **4613** that illustrates an exemplary method for transferring energy from the modulated carrier signal F_{MC} to directly down-convert the modulated carrier signal F_{MC} to the demodulated baseband signal F_{DMB}. The exemplary method illustrated in the flowchart **4613** is an embodiment of the flowchart **4601** in FIG. **46**A.

Any and all combinations of modulation techniques are valid for this invention. For ease of discussion, the digital AM carrier signal **616** is used to illustrate a high level operational description of the invention. Subsequent sections provide detailed flowcharts and descriptions for AM and PM example embodiments. FM presents special considerations that are dealt with separately in Section III.3. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention can be implemented to down-convert any type of EM signal, including any form of modulated carrier signal and unmodulated carrier signals.

The high-level process illustrated in the flowchart **4613** is now described at a high level using the digital AM carrier signal **616**, from FIG. **6**C. The digital AM carrier signal **616** is re-illustrated in FIG. **56**A for convenience.

The process of the flowchart **4613** begins at step **4614**, which includes receiving an EM signal. Step **4613** is represented by the digital AM carrier signal **616**.

Step **4616** includes receiving an energy transfer signal having an aliasing rate F_{AR}. FIG. **56**B illustrates an example energy transfer signal **5602**, which includes a train of energy transfer pulses **5604** having apertures **5606** that are optimized for energy transfer. The optimized apertures **5606** are non-negligible and tend away from zero.

The non-negligible apertures **5606** can be any width other than the period of the EM signal, or a multiple thereof. For example, the non-negligible apertures **5606** can be less than the period of the signal **616** such as, ⅛, ¼, ½, ¾, etc., of the period of the signal **616**. Alternatively, the non-negligible apertures, **5606** can be greater than the period of the signal **616**. The width and amplitude of the apertures **5606** can be optimized based on one or more of a variety of criteria, as described in sections below.

The energy transfer pulses **5604** repeat at the aliasing rate or pulse repetition rate. The aliasing rate is determined in accordance with EQ. (2), reproduced below for convenience.

$$F_C = n \cdot F_{AR} \pm F_{IF} \quad \text{EQ. (2)}$$

When directly down-converting an EM signal to baseband (i.e., zero IF), EQ. (2) becomes:

$$F_C = n \cdot F_{AR} \quad \text{EQ. (8)}$$

Thus, to directly down-convert the AM signal **616** to a demodulated baseband signal, the aliasing rate is substantially equal to the frequency of the AM signal **616** or to a harmonic or sub-harmonic thereof. Although the aliasing rate is too low to permit reconstruction of higher frequency components of the AM signal **616** (i.e., the carrier frequency), it is high enough to permit substantial reconstruction of the lower frequency modulating baseband signal **310**.

Step **4618** includes transferring energy from the EM signal at the aliasing rate to directly down-convert the EM signal to a demodulated baseband signal F_{DMB}. FIG. **56**C illustrates a demodulated baseband signal **5610** that is generated by the direct down-conversion process. The demodulated baseband signal **5610** is similar to the digital modulating baseband signal **310** in FIG. **3**.

FIG. **56**D depicts a filtered demodulated baseband signal **5612**, which can be generated from the demodulated baseband signal **5610**. The invention can thus generate a filtered output signal, a partially filtered output signal, or a relatively unfiltered output signal. The choice between filtered, partially filtered and non-filtered output signals is generally a design choice that depends upon the application of the invention.

2.1.2 Structural Description

In an embodiment, the energy transfer system **6302** transfers energy from any type of EM signal, including modulated carrier signals and unmodulated carrier signal, to directly down-convert the EM signal to a demodulated baseband signal. Preferably, the energy transfer system **6302** transfers energy from the EM signal **1304** to down-convert it to demodulated baseband signal in the manner shown in the operational flowchart **4613**. However, it should be understood that the scope and spirit of the invention includes other structural embodiments for performing the steps of the flowchart **4613**. The specifics of the other structural embodiments will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

Operation of the energy transfer system **6302** is now described in at a high level for the digital AM carrier signal **616**, with reference to the flowchart **4613** and the timing diagrams illustrated in FIGS. **56**A-D. In step **4614**, the energy transfer module **6304** receives the digital AM carrier signal **616**. In step **4616**, the energy transfer module **6304** receives the energy transfer signal **5602**. In step **4618**, the energy transfer module **6304** transfers energy from the digital AM carrier signal **616** at the aliasing rate to directly down-convert it to the demodulated baseband signal **5610**.

Example implementations of the energy transfer module **6302** are disclosed in Sections 4 and 5 below.

2.2 Example Embodiments

Various embodiments related to the method(s) and structure(s) described above are presented in this section (and its subsections). These embodiments are described herein for purposes of illustration, and not limitation. The invention is not limited to these embodiments. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

The method for down-converting the EM signal to the demodulated baseband signal F_{DMB}, illustrated in the flowchart **4613** of FIG. **46**C, can be implemented with various types of modulated carrier signals including, but not limited to, AM, PM, etc., or any combination thereof. The flowchart **4613** of FIG. **46**C is described below for AM and PM. The exemplary descriptions below are intended to facilitate an understanding of the present invention. The present invention is not limited to or by the exemplary embodiments below.

2.2.1 First Example Embodiment: Amplitude Modulation

2.2.1.1 Operational Description

Operation of the exemplary process of the flowchart **4613** in FIG. **46**C is described below for the analog AM carrier

signal **516**, illustrated in FIG. **5**C, and for the digital AM carrier signal **616**, illustrated in FIG. **6**C.

2.2.1.1.1 Analog AM Carrier Signal

A process for directly down-converting the analog AM carrier signal **516** in FIG. **5**C to a demodulated baseband signal is now described with reference to the flowchart **4613** in FIG. **46**C. The analog AM carrier signal **516** is re-illustrated in **57**A for convenience. For this example, the analog AM carrier signal **516** oscillates at approximately 900 MHZ. In FIG. **57**B, an analog AM carrier signal portion **5704** illustrates a portion of the analog AM carrier signal **516** on an expanded time scale.

The process begins at step **4614**, which includes receiving an EM signal. This is represented by the analog AM carrier signal **516**.

Step **4616** includes receiving an energy transfer signal having an aliasing rate F_{AR}. In FIG. **57**C, an example energy transfer signal **5706** is illustrated on approximately the same time scale as FIG. **57**B. The energy transfer signal **5706** includes a train of energy transfer pulses **5707** having non-negligible apertures that tend away from zero time in duration. The energy transfer pulses **5707** repeat at the aliasing rate, which is determined or selected as previously described. Generally, when down-converting an EM signal to a demodulated baseband signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the EM signal.

Step **4618** includes transferring energy from the EM signal at the aliasing rate to directly down-convert the EM signal to the demodulated baseband signal F_{DMB}. In FIG. **57**D, an affected analog AM carrier signal **5708** illustrates effects of transferring energy from the analog AM carrier signal **516** at the aliasing rate F_{AR}. The affected analog AM carrier signal **5708** is illustrated on substantially the same time scale as FIGS. **57**B and **57**C.

FIG. **57**E illustrates a demodulated baseband signal **5712**, which is generated by the down-conversion process. Because a harmonic of the aliasing rate is substantially equal to the frequency of the signal **516**, essentially no IF is produced. The only substantial aliased component is the baseband signal. The demodulated baseband signal **5712** is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

The demodulated baseband signal **5712** includes portions **5710**A, which correlate with the energy transfer pulses **5707** in FIG. **57**C, and portions **5710**B, which are between the energy transfer pulses **5707**. Portions **5710**A represent energy transferred from the analog AM carrier signal **516** to a storage device, while simultaneously driving an output load. The portions **5710**A occur when a switching module is closed by the energy transfer pulses **5707**. Portions **5710**B represent energy stored in a storage device continuing to drive the load. Portions **5710**B occur when the switching module is opened after energy transfer pulses **5707**.

In FIG. **57**F, a demodulated baseband signal **5716** represents a filtered version of the demodulated baseband signal **5712**, on a compressed time scale. The demodulated baseband signal **5716** is substantially similar to the modulating baseband signal **210** and can be further processed using any signal processing technique(s) without further down-conversion or demodulation.

The present invention can output the unfiltered demodulated baseband signal **5712**, the filtered demodulated baseband signal **5716**, a partially filtered demodulated baseband signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention.

The aliasing rate of the energy transfer signal is preferably controlled to optimize the demodulated baseband signal for amplitude output and polarity, as desired.

The drawings referred to herein illustrate direct down-conversion in accordance with the invention. For example, the demodulated baseband signals **5712** in FIG. **57**E and **5716** in FIG. **57**F illustrate that the analog AM carrier signal **516** was directly down-converted to a demodulated baseband signal by retaining enough baseband information for sufficient reconstruction.

2.2.1.1.2 Digital AM Carrier Signal

A process for directly down-converting the digital AM carrier signal **616** in FIG. **6**C to a demodulated baseband signal is now described for the flowchart **4613** in FIG. **46**C. The digital AM carrier signal **616** is re-illustrated in **58**A for convenience. For this example, the digital AM carrier signal **616** oscillates at approximately 900 MHZ. In FIG. **58**B, a digital AM carrier signal portion **5804** illustrates a portion of the digital AM carrier signal **616** on an expanded time scale.

The process begins at step **4614**, which includes receiving an EM signal. This is represented by the digital AM carrier signal **616**.

Step **4616** includes receiving an energy transfer signal having an aliasing rate F_{AR}. In FIG. **58**C, an example energy transfer signal **5806** is illustrated on approximately the same time scale as FIG. **58**B. The energy transfer signal **5806** includes a train of energy transfer pulses **5807** having non-negligible apertures that tend away from zero time in duration. The energy transfer pulses **5807** repeat at the aliasing rate, which is determined or selected as previously described. Generally, when directly down-converting an EM signal to a demodulated baseband signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the EM signal.

Step **4618** includes transferring energy from the EM signal at the aliasing rate to directly down-convert the EM signal to the demodulated baseband signal F_{DMB}. In FIG. **58**D, an affected digital AM carrier signal **5808** illustrates effects of transferring energy from the digital AM carrier signal **616** at the aliasing rate F_{AR}. The affected digital AM carrier signal **5808** is illustrated on substantially the same time scale as FIGS. **58**B and **58**C.

FIG. **58**E illustrates a demodulated baseband signal **5812**, which is generated by the down-conversion process. Because a harmonic of the aliasing rate is substantially equal to the frequency of the signal **616**, essentially no IF is produced. The only substantial aliased component is the baseband signal. The demodulated baseband signal **5812** is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

The demodulated baseband signal **5812** includes portions **5810**A, which correlate with the energy transfer pulses **5807** in FIG. **58**C, and portions **5810**B, which are between the energy transfer pulses **5807**.

Portions **5810**A represent energy transferred from the digital AM carrier signal **616** to a storage device, while simultaneously driving an output load. The portions **5810**A occur when a switching module is closed by the energy transfer pulses **5807**. Portions **5810**B represent energy stored in a storage device continuing to drive the load. Portions **5810**B occur when the switching module is opened after energy transfer pulses **5807**.

In FIG. **58**F, a demodulated baseband signal **5816** represents a filtered version of the demodulated baseband signal **5812**, on a compressed time scale. The demodulated baseband signal **5816** is substantially similar to the modulating

baseband signal **310** and can be further processed using any signal processing technique(s) without further down-conversion or demodulation.

The present invention can output the unfiltered demodulated baseband signal **5812**, the filtered demodulated baseband signal **5816**, a partially filtered demodulated baseband signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention.

The aliasing rate of the energy transfer signal is preferably controlled to optimize the down-converted signal for amplitude output and polarity, as desired.

The drawings referred to herein illustrate direct down-conversion in accordance with the invention. For example, the demodulated baseband signals **5812** in FIG. **58**E and **5816** in FIG. **58**F illustrate that the digital AM carrier signal **616** was directly down-converted to a demodulated baseband signal by retaining enough baseband information for sufficient reconstruction.

2.2.1.2 Structural Description

In an embodiment, the energy transfer module **6304** preferably transfers energy from the EM signal to directly down-convert it to a demodulated baseband signal in the manner shown in the operational flowchart **4613**. But it should be understood that the scope and spirit of the invention includes other structural embodiments for performing the steps of the flowchart **1413**. The specifics of the other structural embodiments will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

Operation of the energy transfer system **6302** is now described for the digital AM carrier signal **516**, with reference to the flowchart **4613** and the timing diagrams in FIGS. **57**A-F. In step **4612**, the energy transfer module **6404** receives the analog AM carrier signal **516**. In step **4614**, the energy transfer module **6404** receives the energy transfer signal **5706**. In step **4618**, the energy transfer module **6404** transfers energy from the analog AM carrier signal **516** at the aliasing rate of the energy transfer signal **5706**, to directly down-convert the digital AM carrier signal **516** to the demodulated baseband signals **5712** or **5716**.

The operation of the energy transfer system **6402** is now described for the digital AM carrier signal **616**, with reference to the flowchart **4613** and the timing diagrams in FIGS. **58**A-F. In step **4614**, the energy transfer module **6404** receives the digital AM carrier signal **616**. In step **4616**, the energy transfer module **6404** receives the energy transfer signal **5806**. In step **4618**, the energy transfer module **6404** transfers energy from the digital AM carrier signal **616** at the aliasing rate of the energy transfer signal **5806**, to directly down-convert the digital AM carrier signal **616** to the demodulated baseband signals **5812** or **5816**.

Example implementations of the energy transfer module **6302** are disclosed in Sections 4 and 5 below.

2.2.2 Second Example Embodiment: Phase Modulation

2.2.2.1 Operational Description

Operation of the exemplary process of flowchart **4613** in FIG. **46**C is described below for the analog PM carrier signal **916**, illustrated in FIG. **9**C and for the digital PM carrier signal **1016**, illustrated in FIG. **10**C.

2.2.2.1.1 Analog PM Carrier Signal

A process for directly down-converting the analog PM carrier signal **916** to a demodulated baseband signal is now described for the flowchart **4613** in FIG. **46**C. The analog PM carrier signal **916** is re-illustrated in **59**A for convenience. For this example, the analog PM carrier signal **916** oscillates at approximately 900 MHZ. In FIG. **59**B, an analog PM carrier signal portion **5904** illustrates a portion of the analog PM carrier signal **916** on an expanded time scale.

The process begins at step **4614**, which includes receiving an EM signal. This is represented by the analog PM carrier signal **916**.

Step **4616** includes receiving an energy transfer signal having an aliasing rate F_{AR}. In FIG. **59**C, an example energy transfer signal **5906** is illustrated on approximately the same time scale as FIG. **59**B. The energy transfer signal **5906** includes a train of energy transfer pulses **5907** having non-negligible apertures that tend away from zero time in duration. The energy transfer pulses **5907** repeat at the aliasing rate, which is determined or selected as previously described. Generally, when directly down-converting an EM signal to a demodulated baseband signal, the aliasing rate FAR is substantially equal to a harmonic or, more typically, a sub-harmonic of the EM signal.

Step **4618** includes transferring energy from the EM signal at the aliasing rate to directly down-convert the EM signal to the demodulated baseband signal F_{DMB}. In FIG. **59**D, an affected analog PM carrier signal **5908** illustrates effects of transferring energy from the analog PM carrier signal **916** at the aliasing rate F_{AR}. The affected analog PM carrier signal **5908** is illustrated on substantially the same time scale as FIGS. **59**B and **59**C.

FIG. **59**E illustrates a demodulated baseband signal **5912**, which is generated by the down-conversion process. Because a harmonic of the aliasing rate is substantially equal to the frequency of the signal **516**, essentially no IF is produced. The only substantial aliased component is the baseband signal. The demodulated baseband signal **5912** is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

The demodulated baseband signal **5912** includes portions **5910**A, which correlate with the energy transfer pulses **5907** in FIG. **59**C, and portions **5910**B, which are between the energy transfer pulses **5907**. Portions **5910**A represent energy transferred from the analog PM carrier signal **916** to a storage device, while simultaneously driving an output load. The portions **5910**A occur when a switching module is closed by the energy transfer pulses **5907**. Portions **5910**B represent energy stored in a storage device continuing to drive the load. Portions **5910**B occur when the switching module is opened after energy transfer pulses **5907**.

In FIG. **59**F, a demodulated baseband signal **5916** represents a filtered version of the demodulated baseband signal **5912**, on a compressed time scale. The demodulated baseband signal **5916** is substantially similar to the modulating baseband signal **210** and can be further processed using any signal processing technique(s) without further down-conversion or demodulation.

The present invention can output the unfiltered demodulated baseband **5912**, the filtered demodulated baseband signal **5916**, a partially filtered demodulated baseband signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention.

The aliasing rate of the energy transfer signal is preferably controlled to optimize the down-converted signal for amplitude output and polarity, as desired.

The drawings referred to herein illustrate direct down-conversion in accordance with the invention. For example, the demodulated baseband signals **5912** in FIG. **59**E and **5916** in FIG. **59**F illustrate that the analog PM carrier signal **916** was successfully down-converted to a demodulated baseband signal by retaining enough baseband information for sufficient reconstruction.

2.2.2.1.2 Digital PM Carrier Signal

A process for directly down-converting the digital PM carrier signal **1016** in FIG. **6**C to a demodulated baseband signal is now described for the flowchart **4613** in FIG. **46**C. The digital PM carrier signal **1016** is re-illustrated in **60**A for convenience. For this example, the digital PM carrier signal **1016** oscillates at approximately 900 MHZ. In FIG. **60**B, a digital PM carrier signal portion **6004** illustrates a portion of the digital PM carrier signal **1016** on an expanded time scale. The process begins at step **4614**, which includes receiving an EM signal. This is represented by the digital PM carrier signal **1016**.

Step **4616** includes receiving an energy transfer signal F_{AR}. In FIG. **60**C, an example energy transfer signal **6006** is illustrated on approximately the same time scale as FIG. **60**B. The energy transfer signal **6006** includes a train of energy transfer pulses **6007** having non-negligible apertures that tend away from zero time in duration. The energy transfer pulses **6007** repeat at the aliasing rate, which is determined or selected as previously described. Generally, when directly down-converting an EM signal to a demodulated baseband signal, the aliasing rate F_{AR} is substantially equal to a harmonic or, more typically, a sub-harmonic of the EM signal.

Step **4618** includes transferring energy from the EM signal at the aliasing rate to directly down-convert the EM signal to the demodulated baseband signal F_{DMB}. In FIG. **60**D, an affected digital PM carrier signal **6008** illustrates effects of transferring energy from the digital PM carrier signal **1016** at the aliasing rate F_{AR}. The affected digital PM carrier signal **6008** is illustrated on substantially the same time scale as FIGS. **60**B and **60**C.

FIG. **60**E illustrates a demodulated baseband signal **6012**, which is generated by the down-conversion process. Because a harmonic of the aliasing rate is substantially equal to the frequency of the signal **1016**, essentially no IF is produced. The only substantial aliased component is the baseband signal. The demodulated baseband signal **6012** is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

The demodulated baseband signal **6012** includes portions **6010**A, which correlate with the energy transfer pulses **6007** in FIG. **60**C, and portions **6010**B, which are between the energy transfer pulses **6007**. Portions **6010**A represent energy transferred from the digital PM carrier signal **1016** to a storage device, while simultaneously driving an output load. The portions **6010**A occur when a switching module is closed by the energy transfer pulses **6007**. Portions **6010**B represent energy stored in a storage device continuing to drive the load. Portions **6010**B occur when the switching module is opened after energy transfer pulses **6007**.

In FIG. **60**F, a demodulated baseband signal **6016** represents a filtered version of the demodulated baseband signal **6012**, on a compressed time scale. The demodulated baseband signal **6016** is substantially similar to the modulating baseband signal **310** and can be further processed using any signal processing technique(s) without further down-conversion or demodulation.

The present invention can output the unfiltered demodulated baseband signal **6012**, the filtered demodulated baseband signal **6016**, a partially filtered demodulated baseband signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention.

The aliasing rate of the energy transfer signal is preferably controlled to optimize the down-converted signal for amplitude output and polarity, as desired.

The drawings referred to herein illustrate direct down-conversion in accordance with the invention. For example, the demodulated baseband signals **6012** in FIG. **60**E and **6016** in FIG. **60**F illustrate that the digital PM carrier signal **1016** was successfully down-converted to a demodulated baseband signal by retaining enough baseband information for sufficient reconstruction.

2.2.2.2 Structural Description

In an embodiment, the energy transfer system **6302** preferably transfers energy from an EM signal to directly down-convert it to a demodulated baseband signal in the manner shown in the operational flowchart **4613**. But it should be understood that the scope and spirit of the invention includes other structural embodiments for performing the steps of the flowchart **1413**. The specifics of the other structural embodiments will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

Operation of the energy transfer system **6302** is now described for the analog PM carrier signal **916**, with reference to the flowchart **4613** and the timing diagrams in FIGS. **59**A-F. In step **4614**, the energy transfer module **6304** receives the analog PM carrier signal **916**. In step **4616**, the energy transfer module **6304** receives the energy transfer signal **5906**. In step **4618**, the energy transfer module **6304** transfers energy from the analog PM carrier signal **916** at the aliasing rate of the energy transfer signal **5906**, to directly down-convert the analog PM carrier signal **916** to the demodulated baseband signals **5912** or **5916**.

Operation of the energy transfer system **6302** is now described for the digital PM carrier signal **1016**, with reference to the flowchart **4613** and to the timing diagrams in FIGS. **60**A-F. In step **4614**, the energy transfer module **6404** receives the digital PM carrier signal **1016**. In step **4616**, the energy transfer module **6404** receives the energy transfer signal **6006**. In step **4618**, the energy transfer module **6404** transfers energy from the digital PM carrier signal **1016** at the aliasing rate of the energy transfer signal **6006**, to directly down-convert the digital PM carrier signal **1016** to the demodulated baseband signal **6012** or **6016**.

Example implementations of the energy transfer module **6302** are disclosed in Sections 4 and 5 below.

2.2.3 Other Embodiments

The embodiments described above are provided for purposes of illustration. These embodiments are not intended to limit the invention. Alternate embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate embodiments fall within the scope and spirit of the present invention. Example implementations of the energy transfer module **6302** are disclosed in Sections 4 and 5 below.

2.3 Implementation Examples

Exemplary operational and/or structural implementations related to the method(s), structure(s), and/or embodiments described above are presented in Sections 4 and 5 below. These implementations are presented for purposes of illustration, and not limitation. The invention is not limited to the particular implementation examples described therein. Alternate implementations (including equivalents, extensions, variations, deviations, etc., of those described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

3. Modulation Conversion

In an embodiment, the invention down-converts an FM carrier signal F_{FMC} to a non-FM signal $F_{(NON\text{-}FM)}$, by trans-

ferring energy from the FM carrier signal F_{FMC} at an aliasing rate. This embodiment is illustrated in FIG. **45**B as **4518**.

In an example embodiment, the FM carrier signal F_{FMC} is down-converted to a phase modulated (PM) signal F_{PM}. In another example embodiment, the FM carrier signal F_{FMC} is down-converted to an amplitude modulated (AM) signal F_{AM}. The down-converted signal can be demodulated with any conventional demodulation technique to obtain a demodulated baseband signal F_{DMB}.

The invention can be implemented with any type of FM signal. Exemplary embodiments are provided below for down-converting a frequency shift keying (FSK) signal to a non-FSK signal. FSK is a sub-set of FM, wherein an FM signal shifts or switches between two or more frequencies. FSK is typically used for digital modulating baseband signals, such as the digital modulating baseband signal **310** in FIG. **3**. For example, in FIG. **8**, the digital FM signal **816** is an FSK signal that shifts between an upper frequency and a lower frequency, corresponding to amplitude shifts in the digital modulating baseband signal **310**. The FSK signal **816** is used in example embodiments below.

In a first example embodiment, energy is transferred from the FSK signal **816** at an aliasing rate that is based on a mid-point between the upper and lower frequencies of the FSK signal **816**. When the aliasing rate is based on the mid-point, the FSK signal **816** is down-converted to a phase shift keying (PSK) signal. PSK is a sub-set of phase modulation, wherein a PM signal shifts or switches between two or more phases. PSK is typically used for digital modulating baseband signals. For example, in FIG. **10**, the digital PM signal **1016** is a PSK signal that shifts between two phases. The PSK signal **1016** can be demodulated by any conventional PSK demodulation technique(s).

In a second example embodiment, energy is transferred from the FSK signal **816** at an aliasing rate that is based upon either the upper frequency or the lower frequency of the FSK signal **816**. When the aliasing rate is based upon the upper frequency or the lower frequency of the FSK signal **816**, the FSK signal **816** is down-converted to an amplitude shift keying (ASK) signal. ASK is a sub-set of amplitude modulation, wherein an AM signal shifts or switches between two or more amplitudes. ASK is typically used for digital modulating baseband signals. For example, in FIG. **6**, the digital AM signal **616** is an ASK signal that shifts between the first amplitude and the second amplitude. The ASK signal **616** can be demodulated by any conventional ASK demodulation technique(s).

The following sections describe methods for transferring energy from an FM carrier signal F_{FMC} to down-convert it to the non-FM signal $F_{(NON\text{-}FM)}$. Exemplary structural embodiments for implementing the methods are also described. It should be understood that the invention is not limited to the particular embodiments described below. Equivalents, extensions, variations, deviations, etc., of the following will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such equivalents, extensions, variations, deviations, etc., are within the scope and spirit of the present invention.

The following sections include a high level discussion, example embodiments, and implementation examples.

3.1 High Level Description

This section (including its subsections) provides a high-level description of transferring energy from the FM carrier signal F_{FM} to down-convert it to the non-FM signal $F_{(NON\text{-}FM)}$, according to the invention. In particular, an operational process for down-converting the FM carrier signal F_{FM} to the non-FM signal $F_{(NON\text{-}FM)}$ is described at a high-level. Also, a structural implementation for implementing this process is described at a high-level. The structural implementation is described herein for illustrative purposes, and is not limiting. In particular, the process described in this section can be achieved using any number of structural implementations, one of which is described in this section. The details of such structural implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

3.1.1 Operational Description

FIG. **46**D depicts a flowchart **4619** that illustrates an exemplary method for down-converting the FM carrier signal F_{FMC} to the non-FM signal $F_{(NON\text{-}FM)}$. The exemplary method illustrated in the flowchart **4619** is an embodiment of the flowchart **4601** in FIG. **46**A.

Any and all forms of frequency modulation techniques are valid for this invention. For ease of discussion, the digital FM carrier (FSK) signal **816** is used to illustrate a high level operational description of the invention. Subsequent sections provide detailed flowcharts and descriptions for the FSK signal **816**. Upon reading the disclosure and examples therein, one skilled in the relevant art(s) will understand that the invention can be implemented to down-convert any type of FM signal.

The method illustrated in the flowchart **4619** is described below at a high level for down-converting the FSK signal **816** in FIG. **8**C to a PSK signal. The FSK signal **816** is re-illustrated in FIG. **84**A for convenience.

The process of the flowchart **4619** begins at step **4620**, which includes receiving an FM signal. This is represented by the FSK signal **816**. The FSK signal **816** shifts between a first frequency **8410** and a second frequency **8412**. The first frequency **8410** can be higher or lower than the second frequency **8412**. In an exemplary embodiment, the first frequency **8410** is approximately 899 MHZ and the second frequency **8412** is approximately 901 MHZ.

Step **4622** includes receiving an energy transfer signal having an aliasing rate F_{AR}. FIG. **84**B illustrates an example energy transfer signal **8402** which includes a train of energy transfer pulses **8403** having non-negligible apertures **8405** that tend away from zero time in duration.

The energy transfer pulses **8403** repeat at the aliasing rate F_{AR}, which is determined or selected as previously described. Generally, when down-converting an FM carrier signal F_{FMC} to a non-FM signal $F_{(NON\text{-}FM)}$, the aliasing rate is substantially equal to a harmonic or, more typically, a sub-harmonic of a frequency within the FM signal. In this example overview embodiment, where the FSK signal **816** is to be down-converted to a PSK signal, the aliasing rate is substantially equal to a harmonic or, more typically, a sub-harmonic of the mid-point between the first frequency **8410** and the second frequency **8412**. For the present example, the mid-point is approximately 900 MHZ.

Step **4624** includes transferring energy from the FM carrier signal F_{FMC} at the aliasing rate to down-convert the FM carrier signal F_{FMC} to the non-FM signal $F_{(NON\text{-}FM)}$. FIG. **84**C illustrates a PSK signal **8404**, which is generated by the modulation conversion process.

When the second frequency **8412** is under-sampled, the PSK signal **8404** has a frequency of approximately 1 MHZ and is used as a phase reference. When the first frequency **8410** is under-sampled, the PSK signal **8404** has a frequency of 1 MHZ and is phase shifted 180 degrees from the phase reference.

FIG. **84**D depicts a PSK signal **8406**, which is a filtered version of the PSK signal **8404**. The invention can thus generate a filtered output signal, a partially filtered output signal, or a relatively unfiltered stair step output signal. The choice

between filtered, partially filtered and non-filtered output signals is generally a design choice that depends upon the application of the invention.

The aliasing rate of the energy transfer signal is preferably controlled to optimize the down-converted signal for amplitude output and polarity, as desired.

Detailed exemplary embodiments for down-converting an FSK signal to a PSK signal and for down-converting an FSK signal to an ASK signal are provided below.

3.1.2 Structural Description

FIG. **63** illustrates the energy transfer system **6302** according to an embodiment of the invention. The energy transfer system **6302** includes the energy transfer module **6304**. The energy transfer system **6302** is an example embodiment of the generic aliasing system **1302** in FIG. **13**.

In a modulation conversion embodiment, the EM signal **1304** is an FM carrier signal F_{FMC} and the energy transfer module **6304** transfers energy from FM carrier signal at a harmonic or, more typically, a sub-harmonic of a frequency within the FM frequency band. Preferably, the energy transfer module **6304** transfers energy from the FM carrier signal F_{FMC} to down-convert it to a non-FM signal $F_{(NON\text{-}FM)}$ in the manner shown in the operational flowchart **4619**. But it should be understood that the scope and spirit of the invention includes other structural embodiments for performing the steps of the flowchart **4619**. The specifics of the other structural embodiments will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

The operation of the energy transfer system **6302** shall now be described with reference to the flowchart **4619** and the timing diagrams of FIGS. **84**A-**84**D. In step **4620**, the energy transfer module **6304** receives the FSK signal **816**. In step **4622**, the energy transfer module **6304** receives the energy transfer signal **8402**. In step **4624**, the energy transfer module **6304** transfers energy from the FSK signal **816** at the aliasing rate of the energy transfer signal **8402** to down-convert the FSK signal **816** to the PSK signal **8404** or **8406**.

Example implementations of the energy transfer module **6302** are provided in Section 4 below.

3.2 Example Embodiments

Various embodiments related to the method(s) and structure(s) described above are presented in this section (and its subsections). These embodiments are described herein for purposes of illustration, and not limitation. The invention is not limited to these embodiments. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

The method for down-converting an FM carrier signal F_{FMC} to a non-FM signal, $F_{(NON\text{-}FM)}$, illustrated in the flowchart **4619** of FIG. **46**D, can be implemented with any type of FM carrier signal including, but not limited to, FSK signals. The flowchart **4619** is described in detail below for down-converting an FSK signal to a PSK signal and for down-converting a PSK signal to an ASK signal. The exemplary descriptions below are intended to facilitate an understanding of the present invention. The present invention is not limited to or by the exemplary embodiments below.

3.2.1 First Example Embodiment: Down-Converting an FM Signal to a PM Signal

3.2.1.1 Operational Description

A process for down-converting the FSK signal **816** in FIG. **8**C to a PSK signal is now described for the flowchart **4619** in FIG. **46**D.

The FSK signal **816** is re-illustrated in FIG. **61**A for convenience. The FSK signal **816** shifts between a first frequency **6106** and a second frequency **6108**. In the exemplary embodiment, the first frequency **6106** is lower than the second frequency **6108**. In an alternative embodiment, the first frequency **6106** is higher than the second frequency **6108**. For this example, the first frequency **6106** is approximately 899 MHZ and the second frequency **6108** is approximately 901 MHZ.

FIG. **61**B illustrates an FSK signal portion **6104** that represents a portion of the FSK signal **816** on an expanded time scale.

The process begins at step **4620**, which includes receiving an FM signal. This is represented by the FSK signal **816**.

Step **4622** includes receiving an energy transfer signal having an aliasing rate F_{AR}. FIG. **61**C illustrates an example energy transfer signal **6107** on approximately the same time scale as FIG. **61**B. The energy transfer signal **6107** includes a train of energy transfer pulses **6109** having non-negligible apertures that tend away from zero time in duration. The energy transfer pulses **6109** repeat at the aliasing rate F_{AR}, which is determined or selected as described above. Generally, when down-converting an FM signal to a non-FM signal, the aliasing rate is substantially equal to a harmonic or, more typically, a sub-harmonic of a frequency within the FM signal.

In this example, where an FSK signal is being down-converted to a PSK signal, the aliasing rate is substantially equal to a harmonic or, more typically, a sub-harmonic, of the mid-point between the frequencies **6106** and **6108**. In this example, where the first frequency **6106** is 899 MHZ and second frequency **6108** is 901 MHZ, the mid-point is approximately 900 MHZ. Suitable aliasing rates thus include 1.8 GHZ, 900 MHZ, 450 MHZ, etc.

Step **4624** includes transferring energy from the FM signal at the aliasing rate to down-convert it to the non-FM signal $F_{(NON\text{-}FM)}$. In FIG. **61**D, an affected FSK signal **6118** illustrates effects of transferring energy from the FSK signal **816** at the aliasing rate F_{AR}. The affected FSK signal **6118** is illustrated on substantially the same time scale as FIGS. **61**B and **61**C.

FIG. **61**E illustrates a PSK signal **6112**, which is generated by the modulation conversion process. PSK signal **6112** is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

The PSK signal **6112** includes portions **6110**A, which correlate with the energy transfer pulses **6107** in FIG. **61**C. The PSK signal **6112** also includes portions **6110**B, which are between the energy transfer pulses **6109**. Portions **6110**A represent energy transferred from the FSK **816** to a storage device, while simultaneously driving an output load. The portions **6110**A occur when a switching module is closed by the energy transfer pulses **6109**. Portions **6110**B represent energy stored in a storage device continuing to drive the load. Portions **6110**B occur when the switching module is opened after energy transfer pulses **6107**.

In FIG. **61**F, a PSK signal **6114** represents a filtered version of the PSK signal **6112**, on a compressed time scale. The present invention can output the unfiltered demodulated baseband signal **6112**, the filtered demodulated baseband signal **6114**, a partially filtered demodulated baseband signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention. The PSK signals **6112** and **6114** can be demodulated with a conventional demodulation technique(s).

The aliasing rate of the energy transfer signal is preferably controlled to optimize the down-converted signal for amplitude output and polarity, as desired.

The drawings referred to herein illustrate modulation conversion in accordance with the invention. For example, the PSK signals **6112** in FIG. **61**E and **6114** in FIG. **61**F illustrate that the FSK signal **816** was successfully down-converted to a PSK signal by retaining enough baseband information for sufficient reconstruction.

3.2.1.2 Structural Description

The operation of the energy transfer system **1602** is now described for down-converting the FSK signal **816** to a PSK signal, with reference to the flowchart **4619** and to the timing diagrams of FIGS. **61**A-E. In step **4620**, the energy transfer module **1606** receives the FSK signal **816** (FIG. **61**A). In step **4622**, the energy transfer module **1606** receives the energy transfer signal **6107** (FIG. **61**C). In step **4624**, the energy transfer module **1606** transfers energy from the FSK signal **816** at the aliasing rate of the energy transfer signal **6107** to down-convert the FSK signal **816** to the PSK signal **6112** in FIG. **61**E or the PSK signal **6114** in FIG. **61**F.

3.2.2. Second Example Embodiment: Down-Converting an FM Signal to an AM Signal

3.2.2.1 Operational Description

A process for down-converting the FSK signal **816** in FIG. **8**C to an ASK signal is now described for the flowchart **4619** in FIG. **46**D.

The FSK signal **816** is re-illustrated in FIG. **62**A for convenience. The FSK signal **816** shifts between a first frequency **6206** and a second frequency **6208**. In the exemplary embodiment, the first frequency **6206** is lower than the second frequency **6208**. In an alternative embodiment, the first frequency **6206** is higher than the second frequency **6208**. For this example, the first frequency **6206** is approximately 899 MHZ and the second frequency **6208** is approximately 901 MHZ.

FIG. **62**B illustrates an FSK signal portion **6204** that represents a portion of the FSK signal **816** on an expanded time scale.

The process begins at step **4620**, which includes receiving an FM signal. This is represented by the FSK signal **816**.

Step **4622** includes receiving an energy transfer signal having an aliasing rate F_{AR}. FIG. **62**C illustrates an example energy transfer signal **6207** on approximately the same time scale as FIG. **62**B. The energy transfer signal **6207** includes a train of energy transfer pulses **6209** having non-negligible apertures that tend away from zero time in duration. The energy transfer pulses **6209** repeat at the aliasing rate F_{AR}, which is determined or selected as described above. Generally, when down-converting an FM signal to a non-FM signal, the aliasing rate is substantially equal to a harmonic or, more typically, a sub-harmonic of a frequency within the FM signal.

In this example, where an FSK signal is being down-converted to an ASK signal, the aliasing rate is substantially equal to a harmonic or, more typically, a sub-harmonic, of either the first frequency **6206** or the second frequency **6208**. In this example, where the first frequency **6206** is 899 MHZ and the second frequency **6208** is 901 MHZ, the aliasing rate can be substantially equal to a harmonic or sub-harmonic of 899 MHZ or 901 MHZ.

Step **4624** includes transferring energy from the FM signal at the aliasing rate to down-convert it to the non-FM signal $F_{(NON\text{-}FM)}$. In FIG. **62**D, an affected FSK signal **6218** illustrates effects of transferring energy from the FSK signal **816** at the aliasing rate F_{AR}. The affected FSK signal **6218** is illustrated on substantially the same time scale as FIGS. **62**B and **62**C.

FIG. **62**E illustrates an ASK signal **6212**, which is generated by the modulation conversion process. ASK signal **6212** is illustrated with an arbitrary load impedance. Load impedance optimizations are discussed in Section 5 below.

The ASK signal **6212** includes portions **6210**A, which correlate with the energy transfer pulses **6209** in FIG. **62**C. The ASK signal **6212** also includes portions **6210**B, which are between the energy transfer pulses **6209**. Portions **6210**A represent energy transferred from the FSK **816** to a storage device, while simultaneously driving an output load. Portions **6210**A occur when a switching module is closed by the energy transfer pulses **6207**. Portions **6210**B represent energy stored in a storage device continuing to drive the load. Portions **6210**B occur when the switching module is opened after energy transfer pulses **6207**.

In FIG. **62**F, an ASK signal **6214** represents a filtered version of the ASK signal **6212**, on a compressed time scale. The present invention can output the unfiltered demodulated baseband signal **6212**, the filtered demodulated baseband signal **6214**, a partially filtered demodulated baseband signal, a stair step output signal, etc. The choice between these embodiments is generally a design choice that depends upon the application of the invention. The ASK signals **6212** and **6214** can be demodulated with a conventional demodulation technique(s).

The aliasing rate of the energy transfer signal is preferably controlled to optimize the down-converted signal for amplitude output and/or polarity, as desired.

The drawings referred to herein illustrate modulation conversion in accordance with the invention. For example, the ASK signals **6212** in FIG. **62**E and **6214** in FIG. **62**F illustrate that the FSK signal **816** was successfully down-converted to an ASK signal by retaining enough baseband information for sufficient reconstruction.

3.2.2.2 Structural Description

The operation of the energy transfer system **1602** is now described for down-converting the FSK signal **816** to an ASK signal, with reference to the flowchart **4619** and to the timing diagrams of FIGS. **62**A-F. In step **4620**, the energy transfer module **6304** receives the FSK signal **816** (FIG. **62**A). In step **4622**, the energy transfer module **6304** receives the energy transfer signal **6207** (FIG. **62**C). In step **4624**, the energy transfer module **6304** transfers energy from the FSK signal **818** at the aliasing rate of the energy transfer signal **6207** to down-convert the FSK signal **816** to the ASK signal **6212** in FIG. **62**E or the ASK signal **6214** in FIG. **62**F.

3.2.3 Other Example Embodiments

The embodiments described above are provided for purposes of illustration. These embodiments are not intended to limit the invention. Alternate embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate embodiments fall within the scope and spirit of the present invention.

Example implementations of the energy transfer module **6302** are disclosed in Sections 4 and 5 below.

3.3 Implementation Examples

Exemplary operational and/or structural implementations related to the method(s), structure(s), and/or embodiments described above are presented in Sections 4 and 5 below. These implementations are presented for purposes of illustration, and not limitation. The invention is not limited to the particular implementation examples described therein. Alternate implementations (including equivalents, extensions,

variations, deviations, etc., of those described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

4. Implementation Examples

Exemplary operational and/or structural implementations related to the method(s), structure(s), and/or embodiments described above are presented in this section (and its subsections). These implementations are presented herein for purposes of illustration, and not limitation. The invention is not limited to the particular implementation examples described herein. Alternate implementations (including equivalents, extensions, variations, deviations, etc., of those described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

FIG. **63** illustrates an energy transfer system **6302**, which is an exemplary embodiment of the generic aliasing system **1302** in FIG. **13**. The energy transfer system **6302** includes an energy transfer module **6304**, which receives the EM signal **1304** and an energy transfer signal **6306**. The energy transfer signal **6306** includes a train of energy transfer pulses having non-negligible apertures that tend away from zero time in duration. The energy transfer pulses repeat at an aliasing rate F_{AR}.

The energy transfer module **6304** transfers energy from the EM signal **1304** at the aliasing rate of the energy transfer signal **6306**, as described in the sections above with respect to the flowcharts **4601** in FIG. **46**A, **4607** in FIG. **46**B, **4613** in FIG. **46**C and **4619** in FIG. **46**D. The energy transfer module **6304** outputs a down-converted signal **1308**B, which includes non-negligible amounts of energy transferred from the EM signal **1304**.

FIG. **64**A illustrates an exemplary gated transfer system **6402**, which is an example of the energy transfer system **6302**. The gated transfer system **6402** includes a gated transfer module **6404**, which is described below.

FIG. **64**B illustrates an exemplary inverted gated transfer system **6406**, which is an alternative example of the energy transfer system **6302**. The inverted gated transfer system **6406** includes an inverted gated transfer module **6408**, which is described below.

4.1 The Energy Transfer System as a Gated Transfer System

FIG. **64**A illustrates the exemplary gated transfer system **6402**, which is an exemplary implementation of the energy transfer system **6302**. The gated transfer system **6402** includes the gated transfer module **6404**, which receives the EM signal **1304** and the energy transfer signal **6306**. The energy transfer signal **6306** includes a train of energy transfer pulses having non-negligible apertures that tend away from zero time in duration. The energy transfer pulses repeat at an aliasing rate F_{AR}.

The gated transfer module **6404** transfers energy from the EM signal **1304** at the aliasing rate of the energy transfer signal **6306**, as described in the sections above with respect to the flowcharts **4601** in FIG. **46**A, **4607** in FIG. **46**B, **4613** in FIG. **46**C and **4619** in FIG. **46**D. The gated transfer module **6404** outputs the down-converted signal **1308**B, which includes non-negligible amounts of energy transferred from the EM signal **1304**.

4.1.1 The Gated Transfer System as a Switch Module and a Storage Module

FIG. **65** illustrates an example embodiment of the gated transfer module **6404** as including a switch module **6502** and a storage module **6506**. Preferably, the switch module **6502** and the storage module **6506** transfer energy from the EM signal **1304** to down-convert it in any of the manners shown in the operational flowcharts **4601** in FIG. **46**A, **4607** in FIG. **46**B, **4613** in FIG. **46**C and **4619** in FIG. **46**D.

For example, operation of the switch module **6502** and the storage module **6506** is now described for down-converting the EM signal **1304** to an intermediate signal, with reference to the flowchart **4607** and the example timing diagrams in FIG. **83**A-F.

In step **4608**, the switch module **6502** receives the EM signal **1304** (FIG. **83**A). In step **4610**, the switch module **6502** receives the energy transfer signal **6306** (FIG. **83**C). In step **4612**, the switch module **6502** and the storage module **6506** cooperate to transfer energy from the EM signal **1304** and down-convert it to an intermediate signal. More specifically, during step **4612**, the switch module **6502** closes during each energy transfer pulse to couple the EM signal **1304** to the storage module **6506**. In an embodiment, the switch module **6502** closes on rising edges of the energy transfer pulses. In an alternative embodiment, the switch module **6502** closes on falling edges of the energy transfer pulses. While the EM signal **1304** is coupled to the storage module **6506**, non-negligible amounts of energy are transferred from the EM signal **1304** to the storage module **6506**. FIG. **83**B illustrates the EM signal **1304** after the energy is transferred from it. FIG. **83**D illustrates the transferred energy stored in the storage module **6506**. The storage module **6506** outputs the transferred energy as the down-converted signal **1308**B. The storage module **6506** can output the down-converted signal **1308**B as an unfiltered signal such as signal shown in FIG. **83**E, or as a filtered down-converted signal (FIG. **83**F).

4.1.2 The Gated Transfer System as Break-Before-Make Module

FIG. **67**A illustrates an example embodiment of the gated transfer module **6404** as including a break-before-make module **6702** and a storage module **6716**. Preferably, the break before make module **6702** and the storage module **6716** transfer energy from the EM signal **1304** to down-convert it in any of the manners shown in the operational flowcharts **4601** in FIG. **46**A, **4607** in FIG. **46**B, **4613** in FIG. **46**C and **4619** in FIG. **46**D.

In FIG. **67**A, the break-before-make module **6702** includes a includes a normally open switch **6704** and a normally closed switch **6706**. The normally open switch **6704** is controlled by the energy transfer signal **6306**. The normally closed switch **6706** is controlled by an isolation signal **6712**. In an embodiment, the isolation signal **6712** is generated from the energy transfer signal **6306**. Alternatively, the energy transfer signal **6306** is generated from the isolation signal **6712**. Alternatively, the isolation signal **6712** is generated independently from the energy transfer signal **6306**. The break-before-make module **6702** substantially isolates an input **6708** from an output **6710**.

FIG. **67**B illustrates an example timing diagram of the energy transfer signal **6306**, which controls the normally open switch **6704**. FIG. **67**C illustrates an example timing diagram of the isolation signal **6712**, which controls the normally closed switch **6706**. Operation of the break-before-make module **6702** is now described with reference to the example timing diagrams in FIGS. **67**B and **67**C.

Prior to time t0, the normally open switch **6704** and the normally closed switch **6706** are at their normal states.

At time t0, the isolation signal **6712** in FIG. **67**C opens the normally closed switch **6706**. Thus, just after time t0, the normally open switch **6704** and the normally closed switch **6706** are open and the input **6708** is isolated from the output **6710**.

At time t1, the energy transfer signal **6306** in FIG. **67**B closes the normally open switch **6704** for the non-negligible duration of a pulse. This couples the EM signal **1304** to the storage module **6716**.

Prior to t2, the energy transfer signal **6306** in FIG. **67**B opens the normally open switch **6704**. This de-couples the EM signal **1304** from the storage module **6716**.

At time t2, the isolation signal **6712** in FIG. **67**C closes the normally closed switch **6706**. This couples the storage module **6716** to the output **6710**.

The storage module **6716**, is similar to the storage module **6506** FIG. **65**. The break-before-make gated transfer system **6701** down-converts the EM signal **1304** in a manner similar to that described with reference to the gated transfer system **6501** in FIG. **65**.

4.1.3 Example Implementations of the Switch Module

The switch module **6502** in FIG. **65** and the switch modules **6704** and **6706** in FIG. **67**A can be any type of switch device that preferably has a relatively low impedance when closed and a relatively high impedance when open. The switch modules **6502**, **6704** and **6706** can be implemented with normally open or normally closed switches. The switch modules need not be ideal switch modules.

FIG. **66**B illustrates the switch modules **6502**, **6704** and **6706** as a switch module **6610**. Switch module **6610** can be implemented in either normally open or normally closed architecture. The switch module **6610** (e.g., switch modules **6502**, **6704** and **6706**) can be implemented with any type of suitable switch device, including, but not limited, to mechanical switch devices and electrical switch devices, optical switch devices, etc., and combinations thereof. Such devices include, but are not limited to transistor switch devices, diode switch devices, relay switch devices, optical switch devices, micro-machine switch devices, etc., or combinations thereof.

In an embodiment, the switch module **6610** can be implemented as a transistor, such as, for example, a field effect transistor (FET), a bi-polar transistor, or any other suitable circuit switching device.

In FIG. **66**A, the switch module **6610** is illustrated as a FET **6602**. The FET **6602** can be any type of FET, including, but not limited to, a MOSFET, a JFET, a GaAsFET, etc. The FET **6602** includes a gate **6604**, a source **6606** and a drain **6608**. The gate **6604** receives the energy transfer signal **6306** to control the switching action between the source **6606** and the drain **6608**. In an embodiment, the source **6606** and the drain **6608** are interchangeable.

It should be understood that the illustration of the switch module **6610** as a FET **6602** in FIG. **66**A is for example purposes only. Any device having switching capabilities could be used to implement the switch module **6610** (i.e., switch modules **6502**, **6704** and **6706**), as will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

In FIG. **66**C, the switch module **6610** is illustrated as a diode switch **6612**, which operates as a two lead device when the energy transfer signal **6306** is coupled to the output **6613**.

In FIG. **66**D, the switch module **6610** is illustrated as a diode switch **6614**, which operates as a two lead device when the energy transfer signal **6306** is coupled to the output **6615**.

4.1.4 Example Implementations of the Storage Module

The storage modules **6506** and **6716** store non-negligible amounts of energy from the EM signal **1304**. In an exemplary embodiment, the storage modules **6506** and **6716** are implemented as a reactive storage module **6801** in FIG. **68**A, although the invention is not limited to this embodiment. A reactive storage module is a storage module that employs one or more reactive electrical components to store energy transferred from the EM signal **1304**. Reactive electrical components include, but are not limited to, capacitors and inductors.

In an embodiment, the storage modules **6506** and **6716** include one or more capacitive storage elements, illustrated in FIG. **68**B as a capacitive storage module **6802**. In FIG. **68**C, the capacitive storage module **6802** is illustrated as one or more capacitors illustrated generally as capacitor(s) **6804**.

The goal of the storage modules **6506** and **6716** is to store non-negligible amounts of energy transferred from the EM signal **1304**. Amplitude reproduction of the original, unaffected EM input signal is not necessarily important. In an energy transfer environment, the storage module preferably has the capacity to handle the power being transferred, and to allow it to accept a non-negligible amount of power during a non-negligible aperture period.

A terminal **6806** serves as an output of the capacitive storage module **6802**. The capacitive storage module **6802** provides the stored energy at the terminal **6806**. FIG. **68**F illustrates the capacitive storage module **6802** as including a series capacitor **6812**, which can be utilized in an inverted gated transfer system described below.

In an alternative embodiment, the storage modules **6506** and **6716** include one or more inductive storage elements, illustrated in FIG. **68**D as an inductive storage module **6808**.

In an alternative embodiment, the storage modules **6506** and **6716** include a combination of one or more capacitive storage elements and one or more inductive storage elements, illustrated in FIG. **68**E as a capacitive/inductive storage module **6810**.

FIG. **68**G illustrates an integrated gated transfer system **6818** that can be implemented to down-convert the EM signal **1304** as illustrated in, and described with reference to, FIGS. **83**A-F.

4.1.5 Optional Energy Transfer Signal Module

FIG. **69** illustrates an energy transfer system **6901**, which is an example embodiment of the energy transfer system **6302**. The energy transfer system **6901** includes an optional energy transfer signal module **6902**, which can perform any of a variety of functions or combinations of functions including, but not limited to, generating the energy transfer signal **6306**.

In an embodiment, the optional energy transfer signal module **6902** includes an aperture generator, an example of which is illustrated in FIG. **68**J as an aperture generator **6820**. The aperture generator **6820** generates non-negligible aperture pulses **6826** from an input signal **6824**. The input signal **6824** can be any type of periodic signal, including, but not limited to, a sinusoid, a square wave, a saw-tooth wave, etc. Systems for generating the input signal **6824** are described below.

The width or aperture of the pulses **6826** is determined by delay through the branch **6822** of the aperture generator **6820**. Generally, as the desired pulse width increases, the difficulty in meeting the requirements of the aperture generator **6820** decrease. In other words, to generate non-negligible aperture pulses for a given EM input frequency, the components utilized in the example aperture generator **6820** do not require as fast reaction times as those that are required in an undersampling system operating with the same EM input frequency.

The example logic and implementation shown in the aperture generator **6820** are provided for illustrative purposes only, and are not limiting. The actual logic employed can take many forms. The example aperture generator **6820** includes an optional inverter **6828**, which is shown for polarity consistency with other examples provided herein.

An example implementation of the aperture generator **6820** is illustrated in FIG. **68**K. Additional examples of aperture generation logic are provided in FIGS. **68**H and **68**I. FIG.

68H illustrates a rising edge pulse generator **6840**, which generates pulses **6826** on rising edges of the input signal **6824**. FIG. **68**I illustrates a falling edge pulse generator **6850**, which generates pulses **6826** on falling edges of the input signal **6824**.

In an embodiment, the input signal **6824** is generated externally of the energy transfer signal module **6902**, as illustrated in FIG. **69**. Alternatively, the input signal **6924** is generated internally by the energy transfer signal module **6902**. The input signal **6824** can be generated by an oscillator, as illustrated in FIG. **68**L by an oscillator **6830**. The oscillator **6830** can be internal to the energy transfer signal module **6902** or external to the energy transfer signal module **6902**. The oscillator **6830** can be external to the energy transfer system **6901**. The output of the oscillator **6830** may be any periodic waveform.

The type of down-conversion performed by the energy transfer system **6901** depends upon the aliasing rate of the energy transfer signal **6306**, which is determined by the frequency of the pulses **6826**. The frequency of the pulses **6826** is determined by the frequency of the input signal **6824**. For example, when the frequency of the input signal **6824** is substantially equal to a harmonic or a sub-harmonic of the EM signal **1304**, the EM signal **1304** is directly down-converted to baseband (e.g. when the EM signal is an AM signal or a PM signal), or converted from FM to a non-FM signal. When the frequency of the input signal **6824** is substantially equal to a harmonic or a sub-harmonic of a difference frequency, the EM signal **1304** is down-converted to an intermediate signal.

The optional energy transfer signal module **6902** can be implemented in hardware, software, firmware, or any combination thereof.

4.2 The Energy Transfer System as an Inverted Gated Transfer System

FIG. **64**B illustrates an exemplary inverted gated transfer system **6406**, which is an exemplary implementation of the energy transfer system **6302**. The inverted gated transfer system **6406** includes an inverted gated transfer module **6408**, which receives the EM signal **1304** and the energy transfer signal **6306**. The energy transfer signal **6306** includes a train of energy transfer pulses having non-negligible apertures that tend away from zero time in duration. The energy transfer pulses repeat at an aliasing rate F_{AR}. The inverted gated transfer module **6408** transfers energy from the EM signal **1304** at the aliasing rate of the energy transfer signal **6306**, as described in the sections above with respect to the flowcharts **4601** in FIG. **46**A, **4607** in FIG. **46**B, **4613** in FIG. **46**C and **4619** in FIG. **46**D. The inverted gated transfer module **6408** outputs the down-converted signal **1308**B, which includes non-negligible amounts of energy transferred from the EM signal **1304**.

4.2.1 The Inverted Gated Transfer System as a Switch Module and a Storage Module

FIG. **74** illustrates an example embodiment of the inverted gated transfer module **6408** as including a switch module **7404** and a storage module **7406**. Preferably, the switch module **7404** and the storage module **7406** transfer energy from the EM signal **1304** to down-convert it in any of the manners shown in the operational flowcharts **4601** in FIG. **46**A, **4607** in FIG. **46**B, **4613** in FIG. **46**C and **4619** in FIG. **46**D.

The switch module **7404** can be implemented as described above with reference to FIGS. **66**A-D. The storage module **7406** can be implemented as described above with reference to FIGS. **68**A-F.

In the illustrated embodiment, the storage module **7206** includes one or more capacitors **7408**. The capacitor(s) **7408** are selected to pass higher frequency components of the EM signal **1304** through to a terminal **7410**, regardless of the state of the switch module **7404**. The capacitor **7408** stores non-negligible amounts of energy from the EM signal **1304**. Thereafter, the signal at the terminal **7410** is off-set by an amount related to the energy stored in the capacitor **7408**.

Operation of the inverted gated transfer system **7401** is illustrated in FIGS. **75**A-F. FIG. **75**A illustrates the EM signal **1304**. FIG. **75**B illustrates the EM signal **1304** after transferring energy from it. FIG. **75**C illustrates the energy transfer signal **6306**, which includes a train of energy transfer pulses having non-negligible apertures.

FIG. **75**D illustrates an example down-converted signal **1308**B. FIG. **75**E illustrates the down-converted signal **1308**B on a compressed time scale. Since the storage module **7406** is a series element, the higher frequencies (e.g., RF) of the EM signal **1304** can be seen on the down-converted signal. This can be filtered as illustrated in FIG. **75**F.

The inverted gated transfer system **7401** can be used to down-convert any type of EM signal, including modulated carrier signals and unmodulated carrier signals.

4.3 Rail to Rail Operation for Improved Dynamic Range

4.3.1 Introduction

FIG. **110**A illustrates aliasing module **11000** that down-converts EM signal **11002** to down-converted signal **11012** using aliasing signal **11014** (sometimes called an energy transfer signal). Aliasing module **11000** is an example of energy transfer module **6304** in FIG. **63**. Aliasing module **11000** includes UFT module **11004** and storage module **11008**. As shown in FIG. **110**A, UFT module **11004** is implemented as a n-channel FET **11006**, and storage module **11008** is implemented as a capacitor **11010**, although the invention is not limited to this embodiment.

FET **11006** receives the EM signal **11002** and aliasing signal **11014**. In one embodiment, aliasing signal **11014** includes a train of pulses having non-negligible apertures that repeat at an aliasing rate. The aliasing rate may be harmonic or sub-harmonic of the EM signal **11002**. FET **11006** samples EM signal **11002** at the aliasing rate of aliasing signal **11014** to generate down-converted signal **11012**. In one embodiment, aliasing signal **11014** controls the gate of FET **11006** so that FET **11006** conducts (or turns on) when the FET gate-to-source voltage (V_{GS}) exceeds a threshold voltage (V_T). When the FET **11006** conducts, a channel is created from source to drain of FET **11006** so that charge is transferred from the EM signal **11002** to the capacitor **11010**. More specifically, the FET **11006** conductance (1/R) vs V_{GS} is a continuous function that reaches an acceptable level at V_T, as illustrated in FIG. **110**B. The charge stored by capacitor **11010** during successive samples forms down-converted signal **11012**.

As stated above, n-channel FET **11006** conducts when V_{GS} exceeds the threshold voltage V_T. As shown in FIG. **110**A, the gate voltage of FET **11006** is determined by aliasing signal **11014**, and the source voltage is determined by the input EM signal **11002**. Aliasing signal **11014** is preferably a plurality of pulses whose amplitude is predictable and set by a system designer. However, the EM signal **11002** is typically received over a communications medium by a coupling device (such as antenna). Therefore, the amplitude of EM signal **11102** may be variable and dependent on a number of factors including the strength of the transmitted signal, and the attenuation of the communications medium. Thus, the source voltage on FET **11006** is not entirely predictable and will affect V_{GS} and the conductance of FET **11006**, accordingly.

For example, FIG. **111**A illustrates EM signal **11102**, which is an example of EM signal **11002** that appears on the

source of FET **11006**. EM signal **11102** has a section **11104** with a relatively high amplitude as shown. FIG. **111**B illustrates the aliasing signal **11106** as an example of aliasing signal **11014** that controls the gate of FET **11006**. FIG. **111**C illustrates V_{GS} **11108**, which is the difference between the gate and source voltages shown in FIGS. **111**B and **111**A, respectively. FET **11006** has an inherent threshold voltage V_T **11112** shown in FIG. **111**C, above which FET **11006** conducts. It is preferred that $V_{GS}>V_T$ during each pulse of aliasing signal **11106**, so that FET **11006** conducts and charge is transferred from the EM signal **11102** to the capacitor **11010** during each pulse of aliasing signal **11106**. As shown in FIG. **111**C, the high amplitude section **11104** of EM signal **11102** causes a V_{GS} pulse **11110** that does exceed the V_T **11112**, and therefore FET **11006** will not fully conduct as is desired. Therefore, the resulting sample of EM signal **11102** may be degraded, which potentially negatively affects the down-converted signal **11012**.

As stated earlier, the conductance of FET **11006** vs V_{GS} is mathematically continuous and is not a hard cutoff. In other words, FET **11006** will marginally conduct when controlled by pulse **11110**, even though pulse **11110** is below V_T **11112**. However, the insertion loss of FET **11006** will be increased when compared with a V_{GS} pulse **11111**, which is greater than V_T **11112**. The performance reduction caused by a large amplitude input signal is often referred to as clipping or compression. Clipping causes distortion in the down-converted signal **11012**, which adversely affects the faithful down-conversion of input EM signal **11102**. Dynamic range is a figure of merit associated with the range of input signals that can be faithfully down-converted without introducing distortion in the down-converted signal. The higher the dynamic range of a down-conversion circuit, the larger the input signals that can down-converted without introducing distortion in the down-converted signal.

4.3.2 Complementary UFT Structure for Improved Dynamic Range

FIG. **112** illustrates aliasing module **11200**, according to an embodiment of the invention, that down-converts EM signal **11208** to generate down-converted signal **11214** using aliasing signal **11220**. Aliasing module **11200** is able to down-convert input signals over a larger amplitude range as compared to aliasing module **11000**, and therefore aliasing module **11200** has an improved dynamic range when compared with aliasing module **11000**. The dynamic range improvement occurs because aliasing module **11200** includes two UFT modules that are implemented with complementary FET devices. In other words, one FET is n-channel, and the other FET is p-channel, so that at least one FET is always conducting during an aliasing signal pulse, assuming the input signal does not exceed the power supply constraints. Aliasing module **11200** includes: delay **11202**; UFT modules **11206**, **11216**; nodes **11210**, **11212**; and inverter **11222**. Inverter **11222** is tied to voltage supplies V_+ **11232** and V_- **11234**. UFT module **11206** comprises n-channel FET **11204**, and UFT module **11216** comprises p-channel FET **11218**.

As stated, aliasing module **11200** operates two complementary FETs to extend the dynamic range and reduce any distortion effects. This requires that two complementary aliasing signals **11224**, **11226** be generated from aliasing signal **11220** to control the sampling by FETs **11218**, **11204**, respectively. To do so, inverter **11222** receives and inverts aliasing signal **11220** to generate aliasing signal **11224** that controls p-channel FET **11218**. Delay **11202** delays aliasing signal **11220** to generate aliasing signal **11226**, where the amount of time delay is approximately equivalent to that associated with inverter **11222**. As such, aliasing signals **11224** and **11226** are approximately complementary in amplitude.

Node **11210** receives EM signal **11208**, and couples EM signals **11227**, **11228** to the sources of n-channel FET **11204** and p-channel FET **11218**, respectively, where EM signals **11227**, **11228** are substantially replicas of EM signal **11208**. N-channel FET **11204** samples EM signal **11227** as controlled by aliasing signal **11226**, and produces samples **11236** at the drain of FET **11204**. Likewise, p-channel FET **11218** samples EM signal **11228** as controlled by aliasing signal **11224**, and produces samples **11238** at the drain of FET **11218**. Node **11212** combines the resulting charge samples into charge samples **11240**, which are stored by capacitor **11230**. The charge stored by capacitor **11230** during successive samples forms down-converted signal **11214**. Aliasing module **11200** offers improved dynamic range over aliasing module **11000** because n-channel FET **11204** and p-channel FET **11214** are complementary devices. Therefore, if one device is cutoff because of a large input EM signal **11208**, the other device will conduct and sample the input signal, as long as the input signal is between the power supply voltages V_+ **11232** and V_- **11234**. This is often referred to as rail-to-rail operation as will be understood by those skilled in the arts.

For example, FIG. **113**A illustrates EM signal **11302** which is an example of EM signals **11227**, **11228** that are coupled to the sources of n-channel FET **11204** and p-channel FET **11218**, respectively. As shown, EM signal **11302** has a section **11304** with a relatively high amplitude including pulses **11303**, **11305**. FIG. **113**B illustrates the aliasing signal **11306** as an example of aliasing signal **11226** that controls the gate of n-channel FET **11204**. Likewise for the p-channel FET, FIG. **113**D illustrates the aliasing signal **11314** as an example of aliasing signal **11224** that controls the gate of p-channel FET **11218**. Aliasing signal **11314** is the amplitude complement of aliasing signal **11306**.

FIG. **113**C illustrates V_{GS} **11308**, which is the difference between the gate and source voltages on n-channel FET **11204** that are depicted in FIGS. **113**B and **113**A, respectively. FIG. **113**C also illustrates the inherent threshold voltage V_T **11309** for FET **11204**, above which FET **11204** conducts. Likewise for the p-channel FET, FIG. **113**E illustrates V_{GS} **11316**, which is the difference between the gate and source voltages for p-channel FET **11218** that are depicted in FIGS. **113**D and **113**A, respectively. FIG. **113**E also illustrates the inherent threshold voltage V_T **11317** for FET **11218**, below which FET **11218** conducts.

As stated, n-channel FET **11204** conducts when V_{GS} **11308** exceeds V_T **11309**, and p-channel FET **11218** conducts when V_{GS} **11316** drops below V_T **11317**. As illustrated by FIG. **113**C, n-channel FET **11204** conducts over the range of EM signal **11302** depicted in FIG. **113**A, except for the EM signal pulse **11305** that results in a corresponding V_{GS} pulse **11310** (FIG. **113**C) that does not exceed V_T **11309**. However, p-channel FET **11218** does conduct because the same EM signal pulse **11305** causes a V_{GS} pulse **11320** (FIG. **113**E) that drops well below that of V_T **11317** for the p-channel FET. Therefore, the sample of the EM signal **11302** is properly taken by p-channel FET **11218**, and no distortion is introduced in down-converted signal **11214**. Similarly, EM signal pulse **11303** results in V_{GS} pulse **11322** (FIG. **113**E) that is inadequate for the p-channel FET **11218** to fully conduct. However, n-channel FET **11204** does fully conduct because the same EM signal pulse **11303** results in a V_{GS} **11311** (FIG. **113**C) that greatly exceeds V_T **11309**.

As illustrated above, aliasing module **11200** offers an improvement in dynamic range over aliasing module **11000**

because of the complimentary FET structure. Any input signal that is within the power supply voltages V_+ **11232** and V_- **11234** will cause either FET **11204** or FET **11218** to conduct, or cause both FETs to conduct, as is demonstrated by FIGS. **113**A-**113**E. This occurs because any input signal that produces a V_{GS} that cuts-off the re-channel FET **11204** will push the p-channel FET **11218** into conduction. Likewise, any input signal that cuts-off the p-channel FET **11218** will push the n-channel FET **11204** into conduction, and therefore prevent any distortion of the down-converted output signal.

4.3.3 Biased Configurations

FIG. **114** illustrates aliasing module **11400**, which is an alternate embodiment of aliasing module **11200**. Aliasing module **11400** includes positive voltage supply (V_+) **11402**, resistors **11404**, **11406**, and the elements in aliasing module **11200**. V_+ **11402** and resistors **11404**,**11406** produce a positive DC voltage at node **11405**. This allows node **11405** to drive a coupled circuit that requires a positive voltage supply, and enables unipolar supply operation of aliasing module **11400**. The positive supply voltage also has the effect of raising the DC level of the input EM signal **11208**. As such, any input signal that is within the power supply voltages V_+ **11402** and ground will cause either FET **11204** or FET **11218** to conduct, or cause both FETs to conduct, as will be understood by those skilled in the arts based on the discussion herein.

FIG. **115** illustrates aliasing module **11500**, which is an alternate biased configuration of aliasing module **11200**. Aliasing module **11500** includes positive voltage supply **11502**, negative voltage supply **11508**, resistors **11504**, **11506**, and the elements in aliasing module **11200**. The use of both a positive and negative voltage supply allows for node **11505** to be biased anywhere between V_+ **11502** and V_- **11508**. This allows node **11505** to drive a coupled circuit that requires either a positive or negative supply voltage. Furthermore, any input signal that is within the power supply voltages V_+ **11502** and V_- **11508** will cause either FET **11204** or FET **11218** to conduct, or cause both FETs to conduct, as will be understood by those skilled in the arts based on the discussion herein.

4.3.4 Simulation Examples

As stated, an aliasing module with a complementary FET structure offers improved dynamic range when compared with a single (or unipolar) FET configuration. This is further illustrated by comparing the signal waveforms associated aliasing module **11602** (of FIG. **116**) which has a complementary FET structure, with that of aliasing module **11702** (of FIG. **117**) which has a single (or unipolar) FET structure.

Aliasing module **11602** (FIG. **116**) down-converts EM signal **11608** using aliasing signal **11612** to generate down-converted signal **11610**. Aliasing module **11602** has a complementary FET structure and includes n-channel FET **11604**, p-channel FET **11606**, inverter **11614**, and aliasing signal generator **11608**. Aliasing module **11602** is biased by supply circuit **11616** as is shown. Aliasing module **11702** (FIG. **117**) down-converts EM signal **11704** using aliasing signal **11708** to generate down-converted signal **11706**. Aliasing module **11702** is a single FET structure comprising n-channel FET **11712** and aliasing signal generator **11714**, and is biased using voltage supply circuit **11710**.

FIGS. **118**-**120** are signal waveforms that correspond to aliasing module **11602**, and FIGS. **121**-**123** are signal waveforms that correspond to aliasing module **11702**. FIGS. **118**, **121** are down-converted signals **11610**, **11706**, respectively. FIGS. **119**, **122** are the sampled EM signal **11608**, **11704**, respectively. FIGS. **120**, **123** are the aliasing signals **11612**, **11708**, respectively. Aliasing signal **11612** is identical to aliasing signal **11708** in order that a proper comparison between modules **11602** and **11702** can be made.

EM signals **11608**, **11704** are relatively large input signals that approach the power supply voltages of ±1.65 volts, as is shown in FIGS. **119**, **122**, respectively. In FIG. **119**, sections **11902** and **11904** of signal **11608** depict energy transfer from EM signal **11608** to down-converted signal **11610** during by aliasing module **11602**. More specifically, section **11902** depicts energy transfer near the −1.65 v supply, and section **11904** depicts energy transfer near the +1.65 v supply. The symmetrical quality of the energy transfer near the voltage supply rails indicates that at least one of complementary FETs **11604**, **11606** are appropriately sampling the EM signal during each of the aliasing pulses **11612**. This results in a down-converted signal **11610** that has minimal high frequency noise, and is centered between −1.0 v and 1.0 v (i.e. has negligible DC voltage component).

Similarly in FIG. **122**, sections **12202** and **12204** illustrate the energy transfer from EM signal **11704** to down-converted signal **11706** by aliasing module **11702** (single FET configuration). More specifically, section **12202** depicts energy transfer near the −1.65 v supply, and section **12204** depicts energy transfer near the +1.65 v supply. By comparing sections **12202**, **12204** with sections **11902**, **11904** of FIG. **119**, it is clear that the energy transfer in sections **12202**, **12204** is not as symmetrical near the power supply rails as that of sections **11902**, **11904**. This is evidence that the EM signal **11704** is partially pinching off single FET **11712** over part of the signal **11704** trace. This results in a down-converted signal **11706** that has more high frequency noise when compared to down-converted signal **11610**, and has a substantial negative DC voltage component.

In summary, down-converted signal **11706** reflects distortion introduced by a relatively large EM signal that is pinching-off the single FET **11712** in aliasing module **11702**. Down-converted signal **11610** that is produced by aliasing module **11602** is relatively distortion free. This occurs because the complementary FET configuration in aliasing module **11602** is able to handle input signals with large amplitudes without introducing distortion in the down-converted signal **11610**. Therefore, the complementary FET configuration in the aliasing module **11602** offers improved dynamic range when compared with the single FET configuration of the aliasing module **11702**.

4.4 Optimized Switch Structures

4.4.1 Splitter in CMOS

FIG. **124**A illustrates an embodiment of a splitter circuit **12400** implemented in CMOS. This embodiment is provided for illustrative purposes, and is not limiting. In an embodiment, splitter circuit **12400** is used to split a local oscillator (LO) signal into two oscillating signals that are approximately 90° out of phase. The first oscillating signal is called the I-channel oscillating signal. The second oscillating signal is called the Q-channel oscillating signal. The Q-channel oscillating signal lags the phase of the I-channel oscillating signal by approximately 90°. Splitter circuit **12400** includes a first I-channel inverter **12402**, a second I-channel inverter **12404**, a third I-channel inverter **12406**, a first Q-channel inverter **12408**, a second Q-channel inverter **12410**, an I-channel flip-flop **12412**, and a Q-channel flip-flop **12414**.

FIGS. **124**F-J are example waveforms used to illustrate signal relationships of splitter circuit **12400**. The waveforms shown in FIGS. **124**F-J reflect ideal delay times through splitter circuit **12400** components. LO signal **12416** is shown in FIG. **124**F. First, second, and third I-channel inverters **12402**, **12404**, and **12406** invert LO signal **12416** three times, outputting inverted LO signal **12418**, as shown in FIG. **124**G.

First and second Q-channel inverters **12408** and **12410** invert LO signal **12416** twice, outputting non-inverted LO signal **12420**, as shown in FIG. **124**H. The delay through first, second, and third I-channel inverters **12402**, **12404**, and **12406** is substantially equal to that through first and second Q-channel inverters **12408** and **12410**, so that inverted LO signal **12418** and non-inverted LO signal **12420** are approximately 180° out of phase. The operating characteristics of the inverters may be tailored to achieve the proper delay amounts, as would be understood by persons skilled in the relevant art(s).

I-channel flip-flop **12412** inputs inverted LO signal **12418**. Q-channel flip-flop **12414** inputs non-inverted LO signal **12420**. In the current embodiment, I-channel flip-flop **12412** and Q-channel flip-flop **12414** are edge-triggered flip-flops. When either flip-flop receives a rising edge on its input, the flip-flop output changes state. Hence, I-channel flip-flop **12412** and Q-channel flip-flop **12414** each output signals that are approximately half of the input signal frequency. Additionally, as would be recognized by persons skilled in the relevant art(s), because the inputs to I-channel flip-flop **12412** and Q-channel flip-flop **12414** are approximately 180° out of phase, their resulting outputs are signals that are approximately 90° out of phase. I-channel flip-flop **12412** outputs I-channel oscillating signal **12422**, as shown in FIG. **1241**. Q-channel flip-flop **12414** outputs Q-channel oscillating signal **12424**, as shown in FIG. **124**J. Q-channel oscillating signal **12424** lags the phase of I-channel oscillating signal **12422** by 90°, also as shown in a comparison of FIGS. **124**I and **124**J.

FIG. **124**B illustrates a more detailed circuit embodiment of the splitter circuit **12400** of FIG. **124**. The circuit blocks of FIG. **124**B that are similar to those of FIG. **124**A are indicated by corresponding reference numbers. FIGS. **124**C-D show example output waveforms relating to the splitter circuit **12400** of FIG. **124**B. FIG. **124**C shows I-channel oscillating signal **12422**. FIG. **124**D shows Q-channel oscillating signal **12424**. As is indicated by a comparison of FIGS. **124**C and **124**D, the waveform of Q-channel oscillating signal **12424** of FIG. **124**D lags the waveform of I-channel oscillating signal **12422** of FIG. **124**C by approximately 90°.

It should be understood that the illustration of the splitter circuit **12400** in FIGS. **124**A and **124**B is for example purposes only. Splitter circuit **12400** may be comprised of an assortment of logic and semiconductor devices of a variety of types, as will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

4.4.2 I/Q Circuit

FIG. **124**E illustrates an example embodiment of a complete I/Q circuit **12426** in CMOS. I/Q circuit **12426** includes a splitter circuit **12400** as described in detail above. Further description regarding I/Q circuit implementations are provided herein, including the applications referenced above.

4.5 Example I and Q Implementations

4.5.1 Switches of Different Sizes

In an embodiment, the switch modules discussed herein can be implemented as a series of switches operating in parallel as a single switch. The series of switches can be transistors, such as, for example, field effect transistors (FET), bipolar transistors, or any other suitable circuit switching devices. The series of switches can be comprised of one type of switching device, or a combination of different switching devices.

For example, FIG. **125** illustrates a switch module **12500**. In FIG. **125**, the switch module is illustrated as a series of FETs **12502***a-n*. The FETs **12502***a-n* can be any type of FET, including, but not limited to, a MOSFET, a JFET, a GaAsFET, etc. Each of FETs **12502***a-n* includes a gate **12504***a-n*, a source **12506***a-n*, and a drain **12508***a-n*, similarly to that of FET **2802** of FIG. **28**A. The series of FETs **12502***a-n* operate in parallel. Gates **12504***a-n* are coupled together, sources **12506***a-n* are coupled together, and drains **12508***a-n* are coupled together. Each of gates **12504***a-n* receives the control signal **1604**, **8210** to control the switching action between corresponding sources **12506***a-n* and drains **12508***a-n*. Generally, the corresponding sources **12506***a-n* and drains **12508***a-n* of each of FETs **12502***a-n* are interchangeable. There is no numerical limit to the number of FETs. Any limitation would depend on the particular application, and the "a-n" designation is not meant to suggest a limit in any way.

In an embodiment, FETs **12502***a-n* have similar characteristics. In another embodiment, one or more of FETs **12502***a-n* have different characteristics than the other FETs. For example, FETs **12502***a-n* may be of different sizes. In CMOS, generally, the larger size a switch is (meaning the larger the area under the gate between the source and drain regions), the longer it takes for the switch to turn on. The longer turn on time is due in part to a higher gate to channel capacitance that exists in larger switches. Smaller CMOS switches turn on in less time, but have a higher channel resistance. Larger CMOS switches have lower channel resistance relative to smaller CMOS switches. Different turn on characteristics for different size switches provides flexibility in designing an overall switch module structure. By combining smaller switches with larger switches, the channel conductance of the overall switch structure can be tailored to satisfy given requirements.

In an embodiment, FETs **12502***a-n* are CMOS switches of different relative sizes. For example, FET **12502***a* may be a switch with a smaller size relative to FETs **12502***b-n*. FET **12502***b* may be a switch with a larger size relative to FET **12502***a*, but smaller size relative to FETs **12502***c-n*. The sizes of FETs **12502***c-n* also may be varied relative to each other. For instance, progressively larger switch sizes may be used. By varying the sizes of FETs **12502***a-n* relative to each other, the turn on characteristic curve of the switch module can be correspondingly varied. For instance, the turn on characteristic of the switch module can be tailored such that it more closely approaches that of an ideal switch. Alternately, the switch module could be tailored to produce a shaped conductive curve.

By configuring FETs **12502***a-n* such that one or more of them are of a relatively smaller size, their faster turn on characteristic can improve the overall switch module turn on characteristic curve. Because smaller switches have a lower gate to channel capacitance, they can turn on more rapidly than larger switches.

By configuring FETs **12502***a-n* such that one or more of them are of a relatively larger size, their lower channel resistance also can improve the overall switch module turn on characteristics. Because larger switches have a lower channel resistance, they can provide the overall switch structure with a lower channel resistance, even when combined with smaller switches. This improves the overall switch structure's ability to drive a wider range of loads. Accordingly, the ability to tailor switch sizes relative to each other in the overall switch structure allows for overall switch structure operation to more nearly approach ideal, or to achieve application specific requirements, or to balance trade-offs to achieve specific goals, as will be understood by persons skilled in the relevant arts(s) from the teachings herein.

It should be understood that the illustration of the switch module as a series of FETs **12502***a-n* in FIG. **125** is for example purposes only. Any device having switching capabilities could be used to implement the switch module (e.g.,

switch modules **2802**, **2702**, **2404** and **2406**), as will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

4.5.2 Reducing Overall Switch Area

Circuit performance also can be improved by reducing overall switch area. As discussed above, smaller switches (i.e., smaller area under the gate between the source and drain regions) have a lower gate to channel capacitance relative to larger switches. The lower gate to channel capacitance allows for lower circuit sensitivity to noise spikes. FIG. **126**A illustrates an embodiment of a switch module, with a large overall switch area. The switch module of FIG. **126**A includes twenty FETs **12602-12640**. As shown, FETs **12602-12640** are the same size ("Wd" and "lng" parameters are equal). Input source **12646** produces the input EM signal. Pulse generator **12648** produces the energy transfer signal for FETs **12602-12640**. Capacitor C**1** is the storage element for the input signal being sampled by FETs **12602-12640**. FIGS. **126**B-**126**Q illustrate example waveforms related to the switch module of FIG. **126**A. FIG. **126**B shows a received 1.01 GHz EM signal to be sampled and downconverted to a 10 MHZ intermediate frequency signal. FIG. **126**C shows an energy transfer signal having an aliasing rate of 200 MHZ, which is applied to the gate of each of the twenty FETs **12602-12640**. The energy transfer signal includes a train of energy transfer pulses having non-negligible apertures that tend away from zero time in duration. The energy transfer pulses repeat at the aliasing rate. FIG. **126**D illustrates the affected received EM signal, showing effects of transferring energy at the aliasing rate, at point **12642** of FIG. **126**A. FIG. **126**E illustrates a down-converted signal at point **12644** of FIG. **126**A, which is generated by the down-conversion process.

FIG. **126**F illustrates the frequency spectrum of the received 1.01 GHz EM signal. FIG. **126**G illustrates the frequency spectrum of the received energy transfer signal. FIG. **126**H illustrates the frequency spectrum of the affected received EM signal at point **12642** of FIG. **126**A. FIG. **1261** illustrates the frequency spectrum of the down-converted signal at point **12644** of FIG. **126**A.

FIGS. **126**J-**126**M respectively further illustrate the frequency spectrums of the received 1.01 GHz EM signal, the received energy transfer signal, the affected received EM signal at point **12642** of FIG. **126**A, and the down-converted signal at point **12644** of FIG. **126**A, focusing on a narrower frequency range centered on 1.00 GHz. As shown in FIG. **126**L, a noise spike exists at approximately 1.0 GHz on the affected received EM signal at point **12642** of FIG. **126**A. This noise spike may be radiated by the circuit, causing interference at 1.0 GHz to nearby receivers.

FIGS. **126**N-**126**Q respectively illustrate the frequency spectrums of the received 1.01 GHz EM signal, the received energy transfer signal, the affected received EM signal at point **12642** of FIG. **126**A, and the down-converted signal at point **12644** of FIG. **126**A, focusing on a narrow frequency range centered near 10.0 MHZ. In particular, FIG. **126**Q shows that an approximately 5 mV signal was downconverted at approximately 10 MHZ.

FIG. **127**A illustrates an alternative embodiment of the switch module, this time with fourteen FETs **12702-12728** shown, rather than twenty FETs **12602-12640** as shown in FIG. **126**A. Additionally, the FETs are of various sizes (some "Wd" and "lng" parameters are different between FETs).

FIGS. **127**B-**127**Q, which are example waveforms related to the switch module of FIG. **127**A, correspond to the similarly designated figures of FIGS. **126**B-**126**Q. As FIG. **127**L shows, a lower level noise spike exists at 1.0 GHz than at the same frequency of FIG. **126**L. This correlates to lower levels of circuit radiation. Additionally, as FIG. **127**Q shows, the lower level noise spike at 1.0 GHz was achieved with no loss in conversion efficiency. This is represented in FIG. **127**Q by the approximately 5 mV signal downconverted at approximately 10 MHZ. This voltage is substantially equal to the level downconverted by the circuit of FIG. **126**A. In effect, by decreasing the number of switches, which decreases overall switch area, and by reducing switch area on a switch-by-switch basis, circuit parasitic capacitance can be reduced, as would be understood by persons skilled in the relevant art(s) from the teachings herein. In particular this may reduce overall gate to channel capacitance, leading to lower amplitude noise spikes and reduced unwanted circuit radiation.

It should be understood that the illustration of the switches above as FETs in FIGS. **126**A-**126**Q and **127**A-**127**Q is for example purposes only. Any device having switching capabilities could be used to implement the switch module, as will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

4.5.3 Charge Injection Cancellation

In embodiments wherein the switch modules discussed herein are comprised of a series of switches in parallel, in some instances it may be desirable to minimize the effects of charge injection. Minimizing charge injection is generally desirable in order to reduce the unwanted circuit radiation resulting therefrom. In an embodiment, unwanted charge injection effects can be reduced through the use of complementary n-channel MOSFETs and p-channel MOSFETs. N-channel MOSFETs and p-channel MOSFETs both suffer from charge injection. However, because signals of opposite polarity are applied to their respective gates to turn the switches on and off, the resulting charge injection is of opposite polarity. Resultingly, n-channel MOSFETs and p-channel MOSFETs may be paired to cancel their corresponding charge injection. Hence, in an embodiment, the switch module may be comprised of n-channel MOSFETs and p-channel MOSFETS, wherein the members of each are sized to minimize the undesired effects of charge injection.

FIG. **129**A illustrates an alternative embodiment of the switch module, this time with fourteen n-channel FETs **12902-12928** and twelve p-channel FETs **12930-12952** shown, rather than twenty FETs **12602-12640** as shown in FIG. **126**A. The n-channel and p-channel FETs are arranged in a complementary configuration. Additionally, the FETs are of various sizes (some "Wd" and "lng" parameters are different between FETs).

FIGS. **129**B-**129**Q, which are example waveforms related to the switch module of FIG. **129**A, correspond to the similarly designated figures of FIGS. **126**B-**126**Q. As FIG. **129**L shows, a lower level noise spike exists at 1.0 GHz than at the same frequency of FIG. **126**L. This correlates to lower levels of circuit radiation. Additionally, as FIG. **129**Q shows, the lower level noise spike at 1.0 GHz was achieved with no loss in conversion efficiency. This is represented in FIG. **129**Q by the approximately 5 mV signal downconverted at approximately 10 MHZ. This voltage is substantially equal to the level downconverted by the circuit of FIG. **126**A. In effect, by arranging the switches in a complementary configuration, which assists in reducing charge injection, and by tailoring switch area on a switch-by-switch basis, the effects of charge injection can be reduced, as would be understood by persons skilled in the relevant art(s) from the teachings herein. In particular this leads to lower amplitude noise spikes and reduced unwanted circuit radiation.

It should be understood that the use of FETs in FIGS. **129**A-**129**Q in the above description is for example purposes only. From the teachings herein, it would be apparent to

persons of skill in the relevant art(s) to manage charge injection in various transistor technologies using transistor pairs.

4.5.4 Overlapped Capacitance

The processes involved in fabricating semiconductor circuits, such as MOSFETs, have limitations. In some instances, these process limitations may lead to circuits that do not function as ideally as desired. For instance, a non-ideally fabricated MOSFET may suffer from parasitic capacitances, which in some cases may cause the surrounding circuit to radiate noise. By fabricating circuits with structure layouts as close to ideal as possible, problems of non-ideal circuit operation can be minimized.

FIG. **128**A illustrates a cross-section of an example n-channel enhancement-mode MOSFET **12800**, with ideally shaped n+ regions. MOSFET **12800** includes a gate **12802**, a channel region **12804**, a source contact **12806**, a source region **12808**, a drain contact **12810**, a drain region **12812**, and an insulator **12814**. Source region **12808** and drain region **12812** are separated by p-type material of channel region **12804**. Source region **12808** and drain region **12812** are shown to be n+ material. The n+ material is typically implanted in the p-type material of channel region **12804** by an ion implantation/diffusion process. Ion implantation/diffusion processes are well known by persons skilled in the relevant art(s). Insulator **12814** insulates gate **12802** which bridges over the p-type material. Insulator **12814** generally comprises a metal-oxide insulator. The channel current between source region **12808** and drain region **12812** for MOSFET **12800** is controlled by a voltage at gate **12802**.

Operation of MOSFET **12800** shall now be described. When a positive voltage is applied to gate **12802**, electrons in the p-type material of channel region **12804** are attracted to the surface below insulator **12814**, forming a connecting near-surface region of n-type material between the source and the drain, called a channel. The larger or more positive the voltage between the gate contact **12806** and source region **12808**, the lower the resistance across the region between.

In FIG. **128**A, source region **12808** and drain region **12812** are illustrated as having n+ regions that were formed into idealized rectangular regions by the ion implantation process. FIG. **128**B illustrates a cross-section of an example n-channel enhancement-mode MOSFET **12816** with non-ideally shaped n+ regions. Source region **12820** and drain region **12822** are illustrated as being formed into irregularly shaped regions by the ion implantation process. Due to uncertainties in the ion implantation/diffusion process, in practical applications, source region **12820** and drain region **12822** do not form rectangular regions as shown in FIG. **128**A. FIG. **128**B shows source region **12820** and drain region **12822** forming exemplary irregular regions. Due to these process uncertainties, the n+ regions of source region **12820** and drain region **12822** also may diffuse further than desired into the p-type region of channel region **12818**, extending underneath gate **12802** The extension of the source region **12820** and drain region **12822** underneath gate **12802** is shown as source overlap **12824** and drain overlap **12826**. Source overlap **12824** and drain overlap **12826** are further illustrated in FIG. **128**C. FIG. **128**C illustrates a top-level view of an example layout configuration for MOSFET **12816**. Source overlap **12824** and drain overlap **12826** may lead to unwanted parasitic capacitances between source region **12820** and gate **12802**, and between drain region **12822** and gate **12802**. These unwanted parasitic capacitances may interfere with circuit function. For instance, the resulting parasitic capacitances may produce noise spikes that are radiated by the circuit, causing unwanted electromagnetic interference.

As shown in FIG. **128**C, an example MOSFET **12816** may include a gate pad **12828**. Gate **12802** may include a gate extension **12830**, and a gate pad extension **12832**. Gate extension **12830** is an unused portion of gate **12802** required due to metal implantation process tolerance limitations. Gate pad extension **12832** is a portion of gate **12802** used to couple gate **12802** to gate pad **12828**. The contact required for gate pad **12828** requires gate pad extension **12832** to be of non-zero length to separate the resulting contact from the area between source region **12820** and drain region **12822**. This prevents gate **12802** from shorting to the channel between source region **12820** and drain region **12822** (insulator **12814** of FIG. **128**B is very thin in this region). Unwanted parasitic capacitances may form between gate extension **12830** and the substrate (FET **12816** is fabricated on a substrate), and between gate pad extension **12832** and the substrate. By reducing the respective areas of gate extension **12830** and gate pad extension **12832**, the parasitic capacitances resulting therefrom can be reduced. Accordingly, embodiments address the issues of uncertainty in the ion implantation/diffusion process. it will be obvious to persons skilled in the relevant art(s) how to decrease the areas of gate extension **12830** and gate pad extension **12832** in order to reduce the resulting parasitic capacitances.

It should be understood that the illustration of the n-channel enhancement-mode MOSFET is for example purposes only. The present invention is applicable to depletion mode MOSFETs, and other transistor types, as will be apparent to persons skilled in the relevant art(s) based on the discussion contained herein.

4.6 Other Implementations

The implementations described above are provided for purposes of illustration. These implementations are not intended to limit the invention. Alternate implementations, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

5. Optional Optimizations of Energy Transfer at an Aliasing Rate

The methods and systems described in sections above can be optimized with one or more of the optimization methods or systems described below.

5.1 Doubling the Aliasing Rate (FAR) of the Energy Transfer Signal

In an embodiment, the optional energy transfer signal module **6902** in FIG. **69** includes a pulse generator module that generates aliasing pulses at twice the frequency of the oscillating source. The input signal **6828** may be any suitable oscillating source.

FIG. **71**A illustrates a circuit **7102** that generates a doubler output signal **7104** (FIG. **71**C) that may be used as an energy transfer signal **6306**. The circuit **7102** generates pulses on both rising and falling edges of the input oscillating signal **7106** of FIG. **71**B. The circuit **7102** can be implemented as a pulse generator and aliasing rate (F_{AR}) doubler. The doubler output signal **7104** can be used as the energy transfer signal **6306**.

In the example of FIG. **71**A, the aliasing rate is twice the frequency of the input oscillating signal F_{ocs} **7106**, as shown by EQ. (9) below.

$$F_{AR}=2\cdot F_{osc} \quad \text{EQ. (9)}$$

The aperture width of the aliasing pulses is determined by the delay through a first inverter **7108** of FIG. **71**A. As the delay is increased, the aperture is increased. A second inverter

7112 is shown to maintain polarity consistency with examples described elsewhere. In an alternate embodiment inverter 7112 is omitted. Preferably, the pulses have non-negligible aperture widths that tend away from zero time. The doubler output signal 7104 may be further conditioned as appropriate to drive the switch module with non-negligible aperture pulses. The circuit 7102 may be implemented with integrated circuitry, discretely, with equivalent logic circuitry, or with any valid fabrication technology.

5.2 Differential Implementations

The invention can be implemented in a variety of differential configurations. Differential configurations are useful for reducing common mode noise. This can be very useful in receiver systems where common mode interference can be caused by intentional or unintentional radiators such as cellular phones, CB radios, electrical appliances etc. Differential configurations are also useful in reducing any common mode noise due to charge injection of the switch in the switch module or due to the design and layout of the system in which the invention is used. Any spurious signal that is induced in equal magnitude and equal phase in both input leads of the invention will be substantially reduced or eliminated. Some differential configurations, including some of the configurations below, are also useful for increasing the voltage and/or for increasing the power of the down-converted signal 1308B.

Differential systems are most effective when used with a differential front end (inputs) and a differential back end (outputs). They can also be utilized in the following configurations, for example:

a) A single-input front end and a differential back end; and

b) A differential front end and a single-output back end.

Examples of these system are provided below, with a first example illustrating a specific method by which energy is transferred from the input to the output differentially.

While an example of a differential energy transfer module is shown below, the example is shown for the purpose of illustration, not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations etc.) of the embodiment described herein will be apparent to those skilled in the relevant art based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

5.2.1 An Example Illustrating Energy Transfer Differentially

FIG. 76A illustrates a differential system 7602 that can be included in the energy transfer module 6304. The differential system 7602 includes an inverted gated transfer design similar to that described with reference to FIG. 74. The differential system 7602 includes inputs 7604 and 7606 and outputs 7608 and 7610. The differential system 7602 includes a first inverted gated transfer module 7612, which includes a storage module 7614 and a switch module 7616. The differential system 7602 also includes a second inverted gated transfer module 7618, which includes a storage module 7620 and a switch module 7616, which it shares in common with inverted gated transfer module 7612.

One or both of the inputs 7604 and 7606 are coupled to an EM signal source. For example, the inputs can be coupled to an EM signal source, wherein the input voltages at the inputs 7604 and 7606 are substantially equal in amplitude but 180 degrees out of phase with one another. Alternatively, where dual inputs are unavailable, one of the inputs 7604 and 7606 can be coupled to ground.

In operation, when the switch module 7616 is closed, the storage modules 7614 and 7620 are in series and, provided they have similar capacitive values, accumulate charge of equal magnitude but opposite polarities. When the switch module 7616 is open, the voltage at the output 7608 is relative to the input 7604, and the voltage at the output 7610 is relative to the voltage at the input 7606.

Portions of the signals at the outputs 7608 and 7610 include signals resulting from energy stored in the storage modules 7614 and 7620, respectively, when the switch module 7616 was closed. The portions of the signals at the outputs 7608 and 7610 resulting from the stored charge are generally equal in amplitude to one another but 180 degrees out of phase.

Portions of the signals at the outputs 7608 and 7610 also include ripple voltage or noise resulting from the switching action of the switch module 7616. But because the switch module is positioned between the two outputs 7608 and 7610, the noise introduced by the switch module appears at the outputs as substantially equal and in-phase with one another. As a result, the ripple voltage can be substantially canceled out by inverting the signal at one of the outputs 7608 or 7610 and adding it to the other remaining output. Additionally, any noise that is impressed with equal amplitude and equal phase onto the input terminals 7604 and 7606 by any other noise sources will tend to be canceled in the same way.

5.2.1.1 Differential Input-to-Differential Output

FIG. 76B illustrates the differential system 7602 wherein the inputs 7604 and 7606 are coupled to equal and opposite EM signal sources, illustrated here as dipole antennas 7624 and 7626. In this embodiment, when one of the outputs 7608 or 7610 is inverted and added to the other output, the common mode noise due to the switching module 7616 and other common mode noise present at the input terminals 7604 and 7606 tend to substantially cancel out.

5.2.1.2 Single Input-to-Differential Output

FIG. 76C illustrates the differential system 7602 wherein the input 7604 is coupled to an EM signal source such as a monopole antenna 7628 and the input 7606 is coupled to ground. In this configuration, the voltages at the outputs 7608 and 7610 are approximately one half the value of the voltages at the outputs in the implementation illustrated in FIG. 76B, given all other parameters are equal.

FIG. 76E illustrates an example single input to differential output receiver/down-converter system 7636. The system 7636 includes the differential system 7602 wherein the input 7606 is coupled to ground as in FIG. 76C. The input 7604 is coupled to an EM signal source 7638 through an optional input impedance match 7642. The EM signal source impedance can be matched with an impedance match system 7642 as described in section 5 below.

The outputs 7608 and 7610 are coupled to a differential circuit 7644 such as a filter, which preferably inverts one of the outputs 7608 or 7610 and adds it to the other output 7608 or 7610. This substantially cancels common mode noise generated by the switch module 7616. The differential circuit 7644 preferably filters the higher frequency components of the EM signal 1304 that pass through the storage modules 7614 and 7620. The resultant filtered signal is output as the down-converted signal 1308B.

5.2.1.3 Differential Input-to-Single Output

FIG. 76D illustrates the differential input to single output system 7629 wherein the inputs 7604 and 7606 of the differential system 7602 are coupled to equal and opposite EM signal dipole antennas 7630 and 7632. In system 7629, the common mode noise voltages are not canceled as in systems shown above. The output is coupled from terminal 7608 to a load 7648.

5.2.2 Specific Alternative Embodiments

In specific alternative embodiments, the present invention is implemented using a plurality of gated transfer modules controlled by a common energy transfer signal with a storage

module coupled between the outputs of the plurality of gated transfer modules. For example, FIG. **99** illustrates a differential system **9902** that includes first and second gated transfer modules **9904** and **9906**, and a storage module **9908** coupled between. Operation of the differential system **9902** will be apparent to one skilled in the relevant art(s), based on the description herein.

As with the first implementation described above in section 5.5.1 and its sub-sections, the gated transfer differential system **9902** can be implemented with a single input, differential inputs, a single output, differential outputs, and combinations thereof. For example, FIG. **100** illustrates an example single input-to-differential output system **10002**.

Where common-mode rejection is desired to protect the input from various common-mode effects, and where common mode rejection to protect the output is not necessary, a differential input-to-single output implementation can be utilized. FIG. **102** illustrates an example differential-to-single ended system **10202**, where a balance/unbalance (balun) circuit **10204** is utilized to generate the differential input. Other input configurations are contemplated. A first output **10206** is coupled to a load **10208**. A second output **10210** is coupled to ground point **10212**.

Typically, in a balanced-to-unbalanced system, where a single output is taken from a differential system without the use of a balun, (i.e., where one of the output signals is grounded), a loss of about 6 db is observed. In the configuration of FIG. **102**, however, the ground point **10212** simply serves as a DC voltage reference for the circuit. The system **10202** transfers charge from the input in the same manner as if it were full differential, with its conversion efficiency generally affected only by the parasitics of the circuit components used, such as the Rds(on) on FET switches if used in the switch module. In other words, the charge transfer still continues in the same manner of a single ended implementation, providing the necessary single-ended ground to the input circuitry when the aperture is active, yet configured to allow the input to be differential for specific common-mode rejection capability and/or interface between a differential input and a single ended output system.

5.2.3 Specific Examples of Optimizations and Configurations for Inverted and Non-Inverted Differential Designs

Gated transfer systems and inverted gated transfer systems can be implemented with any of the various optimizations and configurations disclosed through the specification, such as, for example, impedance matching, tanks and resonant structures, bypass networks, etc. For example, the differential system **10002** in FIG. **100**, which utilizes gated transfer modules with an input impedance matching system **10004** and a tank circuit **10006**, which share a common capacitor. Similarly, differential system **10102** in FIG. **101**, utilizes an inverted gated transfer module with an input impedance matching system **10104** and a tank circuit **10106**, which share a common capacitor.

5.3 Smoothing the Down-Converted Signal

The down-converted signal **1308**B may be smoothed by filtering as desired. The differential circuit **7644** implemented as a filter in FIG. **76**E illustrates but one example. This may be accomplished in any of the described embodiments by hardware, firmware and software implementation as is well known by those skilled in the arts.

5.4 Impedance Matching

The energy transfer module has input and output impedances generally defined by (1) the duty cycle of the switch module, and (2) the impedance of the storage module, at the frequencies of interest (e.g. at the EM input, and intermediate/baseband frequencies).

Starting with an aperture width of approximately ½ the period of the EM signal being down-converted as a preferred embodiment, this aperture width (e.g. the "closed time") can be decreased. As the aperture width is decreased, the characteristic impedance at the input and the output of the energy transfer module increases. Alternatively, as the aperture width increases from ½ the period of the EM signal being down-converted, the impedance of the energy transfer module decreases.

One of the steps in determining the characteristic input impedance of the energy transfer module could be to measure its value. In an embodiment, the energy transfer module's characteristic input impedance is 300 ohms. An impedance matching circuit can be utilized to efficiently couple an input EM signal that has a source impedance of, for example, 50 ohms, with the energy transfer module's impedance of, for example, 300 ohms. Matching these impedances can be accomplished in various manners, including providing the necessary impedance directly or the use of an impedance match circuit as described below.

Referring to FIG. **70**, a specific embodiment using an RF signal as an input, assuming that the impedance **7012** is a relatively low impedance of approximately 50 Ohms, for example, and the input impedance **7016** is approximately 300 Ohms, an initial configuration for the input impedance match module **7006** can include an inductor **7306** and a capacitor **7308**, configured as shown in FIG. **73**. The configuration of the inductor **7306** and the capacitor **7308** is a possible configuration when going from a low impedance to a high impedance. Inductor **7306** and the capacitor **7308** constitute an L match, the calculation of the values which is well known to those skilled in the relevant arts.

The output characteristic impedance can be impedance matched to take into consideration the desired output frequencies. One of the steps in determining the characteristic output impedance of the energy transfer module could be to measure its value. Balancing the very low impedance of the storage module at the input EM frequency, the storage module should have an impedance at the desired output frequencies that is preferably greater than or equal to the load that is intended to be driven (for example, in an embodiment, storage module impedance at a desired 1 MHz output frequency is 2K ohm and the desired load to be driven is 50 ohms). An additional benefit of impedance matching is that filtering of unwanted signals can also be accomplished with the same components.

In an embodiment, the energy transfer module's characteristic output impedance is 2K ohms. An impedance matching circuit can be utilized to efficiently couple the down-converted signal with an output impedance of, for example, 2K ohms, to a load of, for example, 50 ohms. Matching these impedances can be accomplished in various manners, including providing the necessary load impedance directly or the use of an impedance match circuit as described below.

When matching from a high impedance to a low impedance, a capacitor **7314** and an inductor **7316** can be configured as shown in FIG. **73**. The capacitor **7314** and the inductor **7316** constitute an L match, the calculation of the component values being well known to those skilled in the relevant arts.

The configuration of the input impedance match module **7006** and the output impedance match module **7008** are considered to be initial starting points for impedance matching, in accordance with the present invention. In some situations, the initial designs may be suitable without further optimization. In other situations, the initial designs can be optimized in accordance with other various design criteria and considerations.

As other optional optimizing structures and/or components are utilized, their affect on the characteristic impedance of the energy transfer module should be taken into account in the match along with their own original criteria.

5.5 Tanks and Resonant Structures

Resonant tank and other resonant structures can be used to further optimize the energy transfer characteristics of the invention. For example, resonant structures, resonant about the input frequency, can be used to store energy from the input signal when the switch is open, a period during which one may conclude that the architecture would otherwise be limited in its maximum possible efficiency. Resonant tank and other resonant structures can include, but are not limited to, surface acoustic wave (SAW) filters, dielectric resonators, diplexers, capacitors, inductors, etc.

An example embodiment is shown in FIG. **94**A. Two additional embodiments are shown in FIG. **88** and FIG. **97**. Alternate implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Alternate implementations fall within the scope and spirit of the present invention. These implementations take advantage of properties of series and parallel (tank) resonant circuits.

FIG. **94**A illustrates parallel tank circuits in a differential implementation. A first parallel resonant or tank circuit consists of a capacitor **9438** and an inductor **9420** (tank**1**). A second tank circuit consists of a capacitor **9434** and an inductor **9436** (tank**2**).

As is apparent to one skilled in the relevant art(s), parallel tank circuits provide:

low impedance to frequencies below resonance;

low impedance to frequencies above resonance; and

high impedance to frequencies at and near resonance.

In the illustrated example of FIG. **94**A, the first and second tank circuits resonate at approximately 920 Mhz. At and near resonance, the impedance of these circuits is relatively high. Therefore, in the circuit configuration shown in FIG. **94**A, both tank circuits appear as relatively high impedance to the input frequency of 950 Mhz, while simultaneously appearing as relatively low impedance to frequencies in the desired output range of 50 Mhz.

An energy transfer signal **9442** controls a switch **9414**. When the energy transfer signal **9442** controls the switch **9414** to open and close, high frequency signal components are not allowed to pass through tank**1** or tank**2**. However, the lower signal components (50 Mhz in this embodiment) generated by the system are allowed to pass through tank**1** and tank**2** with little attenuation. The effect of tank**1** and tank**2** is to further separate the input and output signals from the same node thereby producing a more stable input and output impedance. Capacitors **9418** and **9440** act to store the 50 Mhz output signal energy between energy transfer pulses.

Further energy transfer optimization is provided by placing an inductor **9410** in series with a storage capacitor **9412** as shown. In the illustrated example, the series resonant frequency of this circuit arrangement is approximately 1 GHz. This circuit increases the energy transfer characteristic of the system. The ratio of the impedance of inductor **9410** and the impedance of the storage capacitor **9412** is preferably kept relatively small so that the majority of the energy available will be transferred to storage capacitor **9412** during operation. Exemplary output signals A and B are illustrated in FIGS. **94**B and **94**C, respectively.

In FIG. **94**A, circuit components **9404** and **9406** form an input impedance match. Circuit components **9432** and **9430** form an output impedance match into a 50 ohm resistor **9428**. Circuit components **9422** and **9424** form a second output impedance match into a 50 ohm resistor **9426**. Capacitors **9408** and **9412** act as storage capacitors for the embodiment. Voltage source **9446** and resistor **9402** generate a 950 Mhz signal with a 50 ohm output impedance, which are used as the input to the circuit. Circuit element **9416** includes a 150 Mhz oscillator and a pulse generator, which are used to generate the energy transfer signal **9442**.

FIG. **88** illustrates a shunt tank circuit **8810** in a single-ended to-single-ended system **8812**. Similarly, FIG. **97** illustrates a shunt tank circuit **9710** in a system **9712**. The tank circuits **8810** and **9710** lower driving source impedance, which improves transient response. The tank circuits **8810** and **9710** are able store the energy from the input signal and provide a low driving source impedance to transfer that energy throughout the aperture of the closed switch. The transient nature of the switch aperture can be viewed as having a response that, in addition to including the input frequency, has large component frequencies above the input frequency, (i.e. higher frequencies than the input frequency are also able to effectively pass through the aperture). Resonant circuits or structures, for example resonant tanks **8810** or **9710**, can take advantage of this by being able to transfer energy throughout the switch's transient frequency response (i.e. the capacitor in the resonant tank appears as a low driving source impedance during the transient period of the aperture).

The example tank and resonant structures described above are for illustrative purposes and are not limiting. Alternate configurations can be utilized. The various resonant tanks and structures discussed can be combined or utilized independently as is now apparent.

5.6 Charge and Power Transfer Concepts

Concepts of charge transfer are now described with reference to FIGS. **109**A-F. FIG. **109**A illustrates a circuit **10902**, including a switch S and a capacitor **10906** having a capacitance C. The switch S is controlled by a control signal **10908**, which includes pulses **19010** having apertures T.

In FIG. **109**B, Equation 10 illustrates that the charge q on a capacitor having a capacitance C, such as the capacitor **10906**, is proportional to the voltage V across the capacitor, where:

q=Charge in Coulombs

C=Capacitance in Farads

V=Voltage in Volts

A=Input Signal Amplitude

Where the voltage V is represented by Equation 11, Equation 10 can be rewritten as Equation 12. The change in charge Δq over time t is illustrated as in Equation 13 as $\Delta q(t)$, which can be rewritten as Equation 14. Using the sum-to-product trigonometric identity of Equation 15, Equation 14 can be rewritten as Equation 16, which can be rewritten as equation 17.

Note that the sin term in Equation 11 is a function of the aperture T only. Thus, $\Delta q(t)$ is at a maximum when T is equal to an odd multiple of π (i.e., π, 3π, 5π, . . .). Therefore, the capacitor **10906** experiences the greatest change in charge when the aperture T has a value of π or a time interval representative of 180 degrees of the input sinusoid. Conversely, when T is equal to 2π, 4π, 6π, . . . , minimal charge is transferred.

Equations 18, 19, and 20 solve for q(t) by integrating Equation 10, allowing the charge on the capacitor **10906** with respect to time to be graphed on the same axis as the input sinusoid sin(t), as illustrated in the graph of FIG. **109**C. As the aperture T decreases in value or tends toward an impulse, the phase between the charge on the capacitor C or q(t) and sin(t) tend toward zero. This is illustrated in the graph of FIG. **109**D, which indicates that the maximum impulse charge transfer

occurs near the input voltage maxima. As this graph indicates, considerably less charge is transferred as the value of T decreases.

Power/charge relationships are illustrated in Equations 21-26 of FIG. **109**E, where it is shown that power is proportional to charge, and transferred charge is inversely proportional to insertion loss.

Concepts of insertion loss are illustrated in FIG. **109**F. Generally, the noise figure of a lossy passive device is numerically equal to the device insertion loss. Alternatively, the noise figure for any device cannot be less that its insertion loss. Insertion loss can be expressed by Equation 27 or 28.

From the above discussion, it is observed that as the aperture T increases, more charge is transferred from the input to the capacitor **10906**, which increases power transfer from the input to the output. It has been observed that it is not necessary to accurately reproduce the input voltage at the output because relative modulated amplitude and phase information is retained in the transferred power.

5.7 Optimizing and Adjusting the Non-Negligible Aperture Width/Duration

5.7.1 Varying Input and Output Impedances

In an embodiment of the invention, the energy transfer signal **6306** of FIG. **63** is used to vary the input impedance seen by the EM Signal **1304** and to vary the output impedance driving a load. An example of this embodiment is described below using the gated transfer module **6404** shown in FIG. **68**G, and in FIG. **82**A. The method described below is not limited to the gated transfer module **6404**, as it can be applied to all of the embodiments of energy transfer module **6304**.

In FIG. **82**A, when switch **8206** is closed, the impedance looking into circuit **8202** is substantially the impedance of storage module illustrated as the storage capacitance **8208**, in parallel with the impedance of the load **8212**. When the switch **8206** is open, the impedance at point **8214** approaches infinity. It follows that the average impedance at point **8214** can be varied from the impedance of the storage module illustrated as the storage capacitance **8208**, in parallel with the load **8212**, to the highest obtainable impedance when switch **8206** is open, by varying the ratio of the time that switch **8206** is open to the time switch **8206** is closed. Since the switch **8206** is controlled by the energy transfer signal **8210**, the impedance at point **8214** can be varied by controlling the aperture width of the energy transfer signal, in conjunction with the aliasing rate.

An example method of altering the energy transfer signal **6306** of FIG. **63** is now described with reference to FIG. **71**A, where the circuit **7102** receives the input oscillating signal **7106** and outputs a pulse train shown as doubler output signal **7104**. The circuit **7102** can be used to generate the energy transfer signal **6306**. Example waveforms of **7104** are shown on FIG. **71**C.

It can be shown that by varying the delay of the signal propagated by the inverter **7108**, the width of the pulses in the doubler output signal **7104** can be varied. Increasing the delay of the signal propagated by inverter **7108**, increases the width of the pulses. The signal propagated by inverter **7108** can be delayed by introducing a R/C low pass network in the output of inverter **7108**. Other means of altering the delay of the signal propagated by inverter **7108** will be well known to those skilled in the art.

5.7.2 Real Time Aperture Control

In an embodiment, the aperture width/duration is adjusted in real time. For example, referring to the timing diagrams in FIGS. **98**B-F, a clock signal **9814** (FIG. **98**B) is utilized to generate an energy transfer signal **9816** (FIG. **98**F), which includes energy transfer pluses **9818**, having variable apertures **9820**. In an embodiment, the clock signal **9814** is inverted as illustrated by inverted clock signal **9822** (FIG. **98**D). The clock signal **9814** is also delayed, as illustrated by delayed clock signal **9824** (FIG. **98**E). The inverted clock signal **9814** and the delayed clock signal **9824** are then ANDed together, generating an energy transfer signal **9816**, which is active—energy transfer pulses **9818**—when the delayed clock signal **9824** and the inverted clock signal **9822** are both active. The amount of delay imparted to the delayed clock signal **9824** substantially determines the width or duration of the apertures **9820**. By varying the delay in real time, the apertures are adjusted in real time.

In an alternative implementation, the inverted clock signal **9822** is delayed relative to the original clock signal **9814**, and then ANDed with the original clock signal **9814**. Alternatively, the original clock signal **9814** is delayed then inverted, and the result ANDed with the original clock signal **9814**.

FIG. **98**A illustrates an exemplary real time aperture control system **9802** that can be utilized to adjust apertures in real time. The example real time aperture control system **9802** includes an RC circuit **9804**, which includes a voltage variable capacitor **9812** and a resistor **9826**. The real time aperture control system **9802** also includes an inverter **9806** and an AND gate **9808**. The AND gate **9808** optionally includes an enable input **9810** for enabling/disabling the AND gate **9808**. The RC circuit **9804**. The real time aperture control system **9802** optionally includes an amplifier **9828**.

Operation of the real time aperture control circuit is described with reference to the timing diagrams of FIGS. **98**B-F. The real time control system **9802** receives the input clock signal **9814**, which is provided to both the inverter **9806** and to the RC circuit **9804**. The inverter **9806** outputs the inverted clock signal **9822** and presents it to the AND gate **9808**. The RC circuit **9804** delays the clock signal **9814** and outputs the delayed clock signal **9824**. The delay is determined primarily by the capacitance of the voltage variable capacitor **9812**. Generally, as the capacitance decreases, the delay decreases.

The delayed clock signal **9824** is optionally amplified by the optional amplifier **9828**, before being presented to the AND gate **9808**. Amplification is desired, for example, where the RC constant of the RC circuit **9804** attenuates the signal below the threshold of the AND gate **9808**.

The AND gate **9808** ANDs the delayed clock signal **9824**, the inverted clock signal **9822**, and the optional Enable signal **9810**, to generate the energy transfer signal **9816**. The apertures **9820** are adjusted in real time by varying the voltage to the voltage variable capacitor **9812**.

In an embodiment, the apertures **9820** are controlled to optimize power transfer. For example, in an embodiment, the apertures **9820** are controlled to maximize power transfer. Alternatively, the apertures **9820** are controlled for variable gain control (e.g. automatic gain control—AGC). In this embodiment, power transfer is reduced by reducing the apertures **9820**.

As can now be readily seen from this disclosure, many of the aperture circuits presented, and others, can be modified in the manner described above (e.g. circuits in FIG. **68** H-K). Modification or selection of the aperture can be done at the design level to remain a fixed value in the circuit, or in an alternative embodiment, may be dynamically adjusted to compensate for, or address, various design goals such as receiving RF signals with enhanced efficiency that are in distinctively different bands of operation, e.g. RF signals at 900 MHz and 1.8 GHz.

5.8 Adding a Bypass Network

In an embodiment of the invention, a bypass network is added to improve the efficiency of the energy transfer module. Such a bypass network can be viewed as a means of synthetic aperture widening. Components for a bypass network are selected so that the bypass network appears substantially lower impedance to transients of the switch module (i.e., frequencies greater than the received EM signal) and appears as a moderate to high impedance to the input EM signal (e.g., greater that 100 Ohms at the RF frequency).

The time that the input signal is now connected to the opposite side of the switch module is lengthened due to the shaping caused by this network, which in simple realizations may be a capacitor or series resonant inductor-capacitor. A network that is series resonant above the input frequency would be a typical implementation. This shaping improves the conversion efficiency of an input signal that would otherwise, if one considered the aperture of the energy transfer signal only, be relatively low in frequency to be optimal.

For example, referring to FIG. **95** a bypass network **9502** (shown in this instance as capacitor **9512**), is shown bypassing switch module **9504**. In this embodiment the bypass network increases the efficiency of the energy transfer module when, for example, less than optimal aperture widths were chosen for a given input frequency on the energy transfer signal **9506**. The bypass network **9502** could be of different configurations than shown in FIG. **95**. Such an alternate is illustrated in FIG. **90**. Similarly, FIG. **96** illustrates another example bypass network **9602**, including a capacitor **9604**.

The following discussion will demonstrate the effects of a minimized aperture and the benefit provided by a bypassing network. Beginning with an initial circuit having a 550 ps aperture in FIG. **103**, its output is seen to be 2.8 mVpp applied to a 50 ohm load in FIG. **107**A. Changing the aperture to 270 ps as shown in FIG. **104** results in a diminished output of 2.5 Vpp applied to a 50 ohm load as shown in FIG. **107**B. To compensate for this loss, a bypass network may be added, a specific implementation is provided in FIG. **105**. The result of this addition is that 3.2 Vpp can now be applied to the 50 ohm load as shown in FIG. **108**A. The circuit with the bypass network in FIG. **105** also had three values adjusted in the surrounding circuit to compensate for the impedance changes introduced by the bypass network and narrowed aperture. FIG. **106** verifies that those changes added to the circuit, but without the bypass network, did not themselves bring about the increased efficiency demonstrated by the embodiment in FIG. **105** with the bypass network. FIG. **108**B shows the result of using the circuit in FIG. **106** in which only 1.88 Vpp was able to be applied to a 50 ohm load.

5.9 Modifying the Energy Transfer Signal Utilizing Feedback

FIG. **69** shows an embodiment of a system **6901** which uses down-converted Signal **1308**B as feedback **6906** to control various characteristics of the energy transfer module **6304** to modify the down-converted signal **1308**B.

Generally, the amplitude of the down-converted signal **1308**B varies as a function of the frequency and phase differences between the EM signal **1304** and the energy transfer signal **6306**. In an embodiment, the down-converted signal **1308**B is used as the feedback **6906** to control the frequency and phase relationship between the EM signal **1304** and the energy transfer signal **6306**. This can be accomplished using the example logic in FIG. **85**A. The example circuit in FIG. **85**A can be included in the energy transfer signal module **6902**. Alternate implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Alternate implementations fall within the scope and spirit of the present invention. In this embodiment a state-machine is used as an example.

In the example of FIG. **85**A, a state machine **8504** reads an analog to digital converter, A/D **8502**, and controls a digital to analog converter, DAC **8506**. In an embodiment, the state machine **8504** includes 2 memory locations, Previous and Current, to store and recall the results of reading A/D **8502**. In an embodiment, the state machine **8504** utilizes at least one memory flag.

The DAC **8506** controls an input to a voltage controlled oscillator, VCO **8508**. VCO **8508** controls a frequency input of a pulse generator **8510**, which, in an embodiment, is substantially similar to the pulse generator shown in FIG. **68**J. The pulse generator **8510** generates energy transfer signal **6306**.

In an embodiment, the state machine **8504** operates in accordance with a state machine flowchart **8519** in FIG. **85**B. The result of this operation is to modify the frequency and phase relationship between the energy transfer signal **6306** and the EM signal **1304**, to substantially maintain the amplitude of the down-converted signal **1308**B at an optimum level.

The amplitude of the down-converted signal **1308**B can be made to vary with the amplitude of the energy transfer signal **6306**. In an embodiment where the switch module **6502** is a FET as shown in FIG. **66**A, wherein the gate **6604** receives the energy transfer signal **6306**, the amplitude of the energy transfer signal **6306** can determine the "on" resistance of the FET, which affects the amplitude of the down-converted signal **1308**B. The energy transfer signal module **6902**, as shown in FIG. **85**C, can be an analog circuit that enables an automatic gain control function. Alternate implementations will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Alternate implementations fall within the scope and spirit of the present invention.

5.10 Other Implementations

The implementations described above are provided for purposes of illustration. These implementations are not intended to limit the invention. Alternate implementations, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate implementations fall within the scope and spirit of the present invention.

6. Example Energy Transfer Downconverters

Example implementations are described below for illustrative purposes. The invention is not limited to these examples.

FIG. **86** is a schematic diagram of an exemplary circuit to down convert a 915 MHz signal to a 5 MHz signal using a 101.1 MHz clock.

FIG. **87** shows example simulation waveforms for the circuit of FIG. **86**. Waveform **8602** is the input to the circuit showing the distortions caused by the switch closure. Waveform **8604** is the unfiltered output at the storage unit. Waveform **8606** is the impedance matched output of the downconverter on a different time scale.

FIG. **88** is a schematic diagram of an exemplary circuit to downconvert a 915 MHz signal to a 5 MHz signal using a 101.1 MHz clock. The circuit has additional tank circuitry to improve conversion efficiency.

FIG. **89** shows example simulation waveforms for the circuit of FIG. **88**. Waveform **8802** is the input to the circuit showing the distortions caused by the switch closure. Waveform **8804** is the unfiltered output at the storage unit. Waveform **8806** is the output of the downconverter after the impedance match circuit.

FIG. **90** is a schematic diagram of an exemplary circuit to downconvert a 915 MHz signal to a 5 MHz signal using a 101.1 MHz clock. The circuit has switch bypass circuitry to improve conversion efficiency.

FIG. **91** shows example simulation waveforms for the circuit of FIG. **90**. Waveform **9002** is the input to the circuit showing the distortions caused by the switch closure. Waveform **9004** is the unfiltered output at the storage unit. Waveform **9006** is the output of the downconverter after the impedance match circuit.

FIG. **92** shows a schematic of the example circuit in FIG. **86** connected to an FSK source that alternates between 913 and 917 MHz, at a baud rate of 500 Kbaud. FIG. **93** shows the original FSK waveform **9202** and the downconverted waveform **9204** at the output of the load impedance match circuit.

IV. MATHEMATICAL DESCRIPTION OF THE PRESENT INVENTION

As described and illustrated in the preceding sections and sub-sections, embodiments of the present invention down-convert an electromagnetic signal by repeatedly transferring energy from portions of the electromagnetic signal. This section describes the operation of the present invention mathematically using matched filter theory, sampling theory, and frequency domain techniques. The concepts and principles of these theories are used to describe the present invention's waveform processing and would be known to persons skilled in the relevant arts.

As will be apparent to persons skilled in the relevant arts based on the teachings contained herein, the description of the present invention contained herein is a unique and specific application of matched filter theory, sampling theory, and frequency domain techniques. It is not taught or suggested in the present literature. Therefore, a new transform has been developed, based on matched filter theory, sampling theory, and frequency domain techniques, to describe the present invention. This new transform is referred to as the UFT transform, and it is described in Section 8, below.

It is noted that the following describes embodiments of the invention, and it is provided for illustrative purposes. The invention is not limited to the descriptions and embodiments described below. It is also noted that characterizations such as "optimal," "sub-optimal," "maximum," "minimum," "ideal," "non-ideal," and the like, contained herein, denote relative relationships.

1. Overview of the Invention

Embodiments of the present invention down-convert an electromagnetic signal by repeatedly performing a matched filtering or correlating operation on a received carrier signal. Embodiments of the invention operate on or near approximate half cycles (e.g., ½, 1½, 2½, etc.) of the received signal. The results of each matched filtering/correlating process are accumulated, for example using a capacitive storage device, and used to form a down-converted version of the electromagnetic signal. In accordance with embodiments of the invention, the matched filtering/correlating process can be performed at a sub-harmonic or fundamental rate.

Operating on an electromagnetic signal with a matched filtering/correlating process or processor produces enhanced (and in some cases the best possible) signal-to-noise ration (SNR) for the processed waveform. A matched filtering/correlating process also preserves the energy of the electromagnetic signal and transfers it through the processor.

Since it is not always practical to design a matched filtering/correlating processor with passive networks, the sub-sections that follow also describe how to implement the present invention using a finite time integrating operation and an RC processing operation. These embodiments of the present invention are very practical and can be implemented using existing technologies, for example but not limited to CMOS technology.

1.1 High Level Description of a Matched Filtering/Correlating Characterization/Embodiment of the Invention

In order to understand how embodiments of the present invention operate, it is useful to keep in mind the fact that such embodiments do not operate by trying to emulate an ideal impulse sampler. Rather, the present invention operates by accumulating the energy of a carrier signal and using the accumulated energy to produce the same or substantially the same result that would be obtained by an ideal impulse sampler, if such a device could be built. Stated more simply, embodiments of the present invention recursively determine a voltage or current value for approximate half cycles (e.g., ½, 1½, 2½, etc.) of a carrier signal, typically at a sub-harmonic rate, and use the determined voltage or current values to form a down-converted version of an electromagnetic signal. The quality of the down-converted electromagnetic signal is a function of how efficiently the various embodiments of the present invention are able to accumulate the energy of the approximate half cycles of the carrier signal.

Ideally, some embodiments of the present invention accumulate all of the available energy contained in each approximate half cycle of the carrier signal operated upon. This embodiment is generally referred to herein as a matched filtering/correlating process or processor. As described in detail below, a matched filtering/correlating processor is able to transfer substantially all of the energy contained in a half cycle of the carrier signal through the processor for use in determining, for example, a peak or an average voltage value of the carrier signal. This embodiment of the present invention produces enhanced (and in some cases the best possible) signal-to-noise ration (SNR), as described in the sub-sections below.

FIG. **148** illustrates an example method **14800** for down-converting an electromagnetic signal using a matched filtering/correlating operation. Method **14800** starts at step **14810**.

In step **14810**, a matched filtering/correlating operation is performed on a portion of a carrier signal. For example, a match filtering/correlating operation can be performed on a 900 MHz RF signal, which typically comprises a 900 MHz sinusoid having noise signals and information signals superimposed on it. Many different types of signals can be operated upon in step **14810**, however, and the invention is not limited to operating on a 900 MHz RF signal. In embodiments, Method **14800** operates on approximate half cycles of the carrier signal.

In an embodiment of the invention, step **14810** comprises the step of convolving an approximate half cycle of the carrier signal with a representation of itself in order to efficiently acquire the energy of the approximate half cycle of the carrier signal. As described elsewhere herein, other embodiments use other means for efficiently acquiring the energy of the approximate half cycle of the carrier signal. The matched filtering/correlating operation can be performed on any approximate half cycle of the carrier signal (although the invention is not limited to this), as described in detail in the sub-sections below.

In step **14820**, the result of the matched filtering/correlating operation in step **14810** is accumulated, preferably in an energy storage device. In an embodiment of the present invention, a capacitive storage devise is used to store a portion of the energy of an approximate half cycle of the carrier signal.

Steps **14810** and **14820** are repeated for additional half cycles of the carrier signal. In an embodiment of the present invention, steps **14810** and **14820** are normally performed at a sub-harmonic rate of the carrier signal, for example at a third sub-harmonic rate. In another embodiment, steps **14810** and **14820** are repeated at an off-set of a sub-harmonic rate of the carrier signal.

In step **14830**, a down-converted signal is output. In embodiments, the results of steps **14810** and **14820** are passed on to a reconstruction filter or an interpolation filter.

FIG. **149** illustrates an example gated matched filtering/correlating system **14900**, which can be used to implement method **14800**. Ideally, in an embodiment, an impulse response of matched filtering/correlating system **14900** is identical to the modulated carrier signal, $S_i(t)$, to be processed. As can be seen in FIG. **149**, system **14900** comprises a multiplying module **14902**, a switching module **14904**, and an integrating module **14906**.

System **14900** can be thought of as a convolution processor. System **14900** multiplies the modulated carrier signal, $S_i(t)$, by a representation of itself, $S_i(t-\tau)$, using multiplication model **14902**. The output of multiplication module **14902** is then gated by switching module **14904** to integrating module **14906**. As can be seen in FIG. **149**, switching module **14904** is controlled by a windowing function, $u(t)-u(t-T_A)$. The length of the windowing function aperture is T_A, which is in an embodiment equal to an approximate half cycle of the carrier signal. Switching module **14904** in an embodiment ensures that approximate half cycles of the carrier signal are normally operated upon at a sub-harmonic rate. In an embodiment shown in FIG. **72**, preprocessing is used to select a portion of the carrier signal to be operated upon in accordance with the present invention. In an embodiment of system **14900**, the received carrier signal is operated on at an off-set of a sub-harmonic rate of the carrier signal. Integration module **14906** integrates the gated output of multiplication module **14902** and passes on its result, $S_0(t)$. This embodiment of the present invention is described in more detail in subsequent sub-sections.

As will be apparent to persons skilled in the relevant arts given the discussion herein, the present invention is not a traditional realization of a matched filter/correlator.

1.2 High Level Description of a Finite Time Integrating Characterization/Embodiment of the Invention

As described herein, in some embodiments, a matched filter/correlator embodiment according to the present invention provides maximum energy transfer and maximum SNR. A matched filter/correlator embodiment, however, might not always provide an optimum solution for all applications. For example, a matched filter/correlator embodiment might be too expensive or too complicated to implement for some applications. In such instances, other embodiments according to the present invention may provide acceptable results at a substantially lower cost, using less complex circuitry. The invention is directed to those embodiments as well.

As described herein in subsequent sub-sections, a gated matched filter/correlator processor can be approximated by a processor whose impulse response is a step function having a duration substantially equal to the time interval defined for the waveform, typically a half cycle of the electromagnetic signal, and an integrator. Such an approximation of a gated matched filter/correlator is generally referred to as a finite time integrator. A finite time integrator in accordance with an embodiment of the present invention can be implemented with, for example, a switching device controlled by a train of pulses having apertures substantially equal to the time interval defined for the waveform. The energy transfer and SNR of a finite time integrator implemented in accordance with an embodiment of the present invention is nearly that of a gated matched filter/correlator, but without having to tailor the matched filter/correlator for a particular type of electromagnetic signal. As described in sub-section 6, a finite time integrator embodiment according to the present invention can provide a SNR result that differs from the result of matched filter/correlator embodiment by only 0.91 dB.

FIG. **150** illustrates an example method **15000** for down-converting an electromagnetic signal using a matched filtering/correlating operation. Method **15000** starts at step **15010**.

In step **15010**, a matched filtering/correlating operation is performed on a portion of a carrier signal. For example, a match filtering/correlating operation can be performed on a 900 MHz RF signal, which typically comprises a 900 MHz sinusoid having noise signals and information signals superimposed on it. Many different types of signals can be operated upon in step **15010**, however, and the invention is not limited to operating on a 900 MHz RF signal. In embodiments, Method **15000** operates on approximate half cycles of the carrier signal.

In an embodiment of the invention, step **15010** comprises the step of convolving an approximate half cycle of the carrier signal with a representation of itself in order to efficiently acquire the energy of the approximate half cycle of the carrier signal. As described elsewhere herein, other embodiments use other means for efficiently acquiring the energy of the approximate half cycle of the carrier signal. The matched filtering/correlating operation can be performed on any approximate half cycle of the carrier signal (although the invention is not limited to this), as described in detail in the sub-sections below.

In step **15020**, the result of the matched filtering/correlating operation in step **15010** is accumulated, preferably in an energy storage device. In an embodiment of the present invention, a capacitive storage devise is used to store a portion of the energy of an approximate half cycle of the carrier signal.

Steps **15010** and **15020** are repeated for additional half cycles of the carrier signal. In one embodiment of the present invention, steps **15010** and **15020** are performed at a sub-harmonic rate of the carrier signal. In another embodiment, steps **15010** and **15020** are repeated at an off-set of a sub-harmonic rate of the carrier signal.

In step **15030**, a down-converted signal is output. In embodiments, the results of steps **15010** and **15020** are passed on to a reconstruction filter or an interpolation filter.

FIG. **151** illustrates an example finite time integrating system **15100**, which can be used to implement method **15000**. Finite time integrating system **15100** has an impulse response that is approximately rectangular, as further described in sub-section 4. As can be seen in FIG. **151**, system **15100** comprises a switching module **15102** and an integrating module **15104**.

Switching module **15102** is controlled by a windowing function, $u(t)-u(t-T_A)$. The length of the windowing function aperture is T_A, which is equal to an approximate half cycle of the received carrier signal, $S_i(t)$. Switching module **15102** ensures that approximate half cycles of the carrier signal can be operated upon at a sub-harmonic rate. In an embodiment of system **15100**, the received carrier signal is operated on at an off-set of a sub-harmonic rate of the carrier signal.

Integration module **15104** integrates the output of switching module **15102** and passes on its result, $S_0(t)$. This embodiment of the present invention is described in more detail in sub-section 4 below.

1.3 High Level Description of an RC Processing Characterization/Embodiment of the Invention

The prior sub-section describes how a gated matched filter/correlator can be approximated with a finite time integrator. This sub-section describes how the integrator portion of the finite time integrator can be approximated with a resistor/capacitor (RC) processor. This embodiment of the present invention is generally referred to herein as an RC processor, and it can be very inexpensive to implement. Additionally, the RC processor embodiment according to the present invention can be implemented using only passive circuit devices, and it can be implemented, for example, using existing CMOS technology. This RC processor embodiment, shown in FIG. **153**, utilizes a very low cost integrator or capacitor as a memory across the aperture or switching module. If the capacitor is suitably chosen for this embodiment, the performance of the RC processor approaches that of the matched filter/correlator embodiments described herein.

FIG. **152** illustrates an example method **15200** for down-converting an electromagnetic signal using a matched filtering/correlating operation. Method **15200** starts at step **15210**.

In step **15210**, a matched filtering/correlating operation is performed on a portion of a carrier signal. For example, a match filtering/correlating operation can be performed on a 900 MHz RF signal, which typically comprises a 900 MHz sinusoid having noise signals and information signals superimposed on it. Many different types of signals can be operated upon in step **15210**, however, and the invention is not limited to operating on a 900 MHz RF signal. In embodiments, Method **15200** operates on approximate half cycles of the carrier signal.

In an embodiment of the invention, step **15210** comprises the step of convolving an approximate half cycle of the carrier signal with a representation of itself in order to efficiently acquire the energy of the approximate half cycle of the carrier signal. As described elsewhere herein, other embodiments use other means for efficiently acquiring the energy of the approximate half cycle of the carrier signal. The matched filtering/correlating operation can be performed on any approximate half cycle of the carrier signal (although the invention is not limited to this), as described in detail in the sub-sections below.

In step **15220**, the result of the matched filtering/correlating operation in step **15210** is accumulated, preferably in an energy storage device. In an embodiment of the present invention, a capacitive storage devise is used to store a portion of the energy of an approximate half cycle of the carrier signal.

Steps **15210** and **15220** are repeated for additional half cycles of the carrier signal. In an embodiment of the present invention, steps **15210** and **15220** are normally performed at a sub-harmonic rate of the carrier signal, for example at a third sub-harmonic rate. In another embodiment, steps **15210** and **15220** are repeated at an off-set of a sub-harmonic rate of the carrier signal.

In step **15230**, a down-converted signal is output. In embodiments, the results of steps **15210** and **15220** are passed on to a reconstruction filter or an interpolation filter.

FIG. **153** illustrates an example RC processing system **15300**, which can be used to implement method **15200**. As can be seen in FIG. **153**, system **15300** comprises a source resistance **15302**, a switching module **15304**, and a capacitance **15306**. Source resistance **15302** is a lumped sum resistance.

Switching module **15304** is controlled by a windowing function, $u(t)-u(t-T_A)$. The length of the windowing function aperture is T_A, which is equal to an approximate half cycle of the received carrier signal, $S_i(t)$. Switching module **15304** ensures that approximate half cycles of the carrier signal are normally processed at a sub-harmonic rate. In an embodiment of system **15300**, the received carrier signal is processed on at an off-set of a sub-harmonic rate of the carrier signal.

Capacitor **15306** integrates the output of switching module **15304** and accumulates the energy of the processed portions of the received carrier signal. RC processor **15300** also passes on its result, $S_0(t)$, to subsequent circuitry for further processing. This embodiment of the present invention is described in more detail in subsequent sub-sections.

It is noted that the implementations of the invention presented above are provided for illustrative purposes. Other implementations will be apparent to persons skilled in the art based on the herein teachings, and the invention is directed to such implementations.

2. Representation of a Power Signal as a Sum of Energy Signals

This sub-section describes how a power signal can be represented as a sum of energy signals. The detailed mathematical descriptions in the sub-sections below use both Fourier transform analysis and Fourier series analysis to describe embodiments of the present invention. Fourier transform analysis typically is used to describe energy signals while Fourier series analysis is used to describe power signals. In a strict mathematical sense, Fourier transforms do not exist for power signals. It is occasionally mathematically convenient, however, to analyze certain repeating or periodic power signals using Fourier transform analysis.

Both Fourier series analysis and Fourier transform analysis can be used to describe periodic waveforms with pulse like structure. For example, consider the ideal impulse sampling train in EQ. (10).

$$x(t) = \sum_{m=-\infty}^{\infty} \delta(t - mT_s) \qquad \text{EQ. (10)}$$

Suppose that this sampling train is convolved (in the time domain) with a particular waveform s(t), which is of finite duration T_A. Hence s(t) is an energy waveform. Then:

$$s(t) * x(t) = \sum_{m=-\infty}^{\infty} \delta(t - mT_s) * s(t) \qquad \text{EQ. (11)}$$

$$= \sum_{m=-\infty}^{\infty} s(t - mT_s) \qquad \text{EQ. (12)}$$

The above equation is a well known form of the sampler equation for arbitrary pulse shapes which may be of finite time duration rather than impulse-like. The sampler equation possesses a Fourier transform on a term-by-term basis because each separate is an energy waveform.

Applying the convolution theorem and a term-by-term Fourier transform yields:

$$\Im\{s(t) * x(t)\} \Delta \Im\left\{\sum_{m=-\infty}^{\infty}\right\} \delta(t - mT_s) s(f) \qquad \text{EQ. (13)}$$

$$= \sum_{m=-\infty}^{\infty} T_s^{-1} \delta(f - m/T_s) S(n/T_s)$$

where $f_s=T_s^{-1}$. In this manner the Fourier transform may be derived for a train of pulses of arbitrary time domain definition provided that each pulse is of finite time duration and each pulse in the train is identical to the next. If the pulses are not deterministic then techniques viable for stochastic signal analysis may be required. It is therefore possible to represent the periodic signal, which is a power signal, by an infinite linear sum of finite duration energy signals. If the power signal is of infinite time duration, an infinite number of energy waveforms are required to create the desired representation.

FIG. **154** illustrates a pulse train **15402**. Each pulse of pulse deterministic train **15402**, for example pulse **15404**, is an energy signal.

FIG. **155** illustrates one heuristic method based on superposition for combining pulses to form pulse deterministic train **15402**.

The method of FIG. **155** shows how a power signal can be obtained from a linear piece-wise continuous sum of energy signals.

2.1 De-Composition of a Sine Wave into an Energy Signal Representation

The heuristic discussion presented in the previous section can be applied to the piecewise linear reconstruction of a sine wave function or carrier. FIG. **156** illustrates a simple way to view such a construction.

Using the previously developed equations, the waveform y(t) can be represented by:

$$\sin(\omega_c t+\phi)\,|_{t=0}^{mT} = \qquad \text{EQ. (14)}$$

$$\sum_{l=0}^{m=even} \sin(\omega_c t+\phi)\left[u(t)-u\left(t-\frac{T_c}{2}\right)\right]*\delta\left(t-l\cdot\frac{T_s}{2}\right)+$$

$$\sum_{k=1}^{m=odd} \sin(\omega_c t+\phi)\left[u\left(t-\frac{T_c}{2}\right)-u\left(t-\frac{3T_c}{2}\right)\right]*\delta\left(t-k\frac{T_s}{2}\right)$$

and y(t) can be rewritten as:

$$y(t) = \qquad \text{EQ. (15)}$$

$$\sum_{l=0}^{m=even}\left[u\left(t-\frac{lT_s}{2}\right)-u\left(t-\frac{lT_s}{2}-\frac{T_c}{2}\right)\right]\cdot\sin\left(\omega_c\left(t-\frac{lT_s}{2}\right)+\phi\right)+$$

$$\sum_{k=1}^{m=odd}\left[u(t-kT_s)-u(t-kT_s)\right]\cdot\sin\left(\omega_c\left(t-kT_s-\frac{T_c}{2}\right)\right)$$

$$\sin(\omega_c(t-kT_s)+\phi)$$

In general, T_s is usually integrally related to T_c. That is, the sampling interval T_s divided by T_c usually results in an integer, which further reduces the above equation. The unit step functions are employed to carve out the portion of a sine function applicable for positive pulses and negative pulse, respectively. The point is a power signal may be viewed as an infinite linear sum of energy signals.

2.2 Decomposition of Sine Waveforms

FIG. **157** illustrates how portions of a carrier signal or sine waveform are selected for processing according to embodiments of the present invention. Embodiments of the present invention operate recursively, at a sub-harmonic rate, on a carrier signal (i.e., sine wave waveform). FIG. **157** shows the case where there is synchronism in phase and frequency between the clock of the present invention and the carrier signal. This sub-section, as well as the previous sub-sections, illustrates the fact that each half-sine segment of a carrier signal can be viewed as an energy signal, and may be partitioned from the carrier or power signal by a gating process.

3. Matched Filtering/Correlating Characterization/Embodiment

3.1 Time Domain Description

Embodiments of the present invention are interpreted as a specific implementation of a matched filter and a restricted Fourier sine or cosine transform. The matched filter of such embodiments is not a traditional realization of a matched filter designed to extract information at the data bandwidth. Rather, the correlation properties of the filter of the embodiments exploit specific attributes of bandpass waveforms to efficiently down convert signals from RF. A controlled aperture specifically designed to the bandpass waveform is used. In addition, the matched filter operation of embodiments of the present invention is applied recursively to the bandpass signal at a rate sub-harmonically related to the carrier frequency. Each matched filtered result or correlation of embodiments of the present invention is retained and accumulated to provide an initial condition for subsequent recursions of the correlator. This accumulation is approximated as a zero order data hold filter.

An attribute of bandpass waveforms is that they inherently possess time domain structure, which can be compared to sampling processes. For example, FIG. **158** illustrates a double sideband large carrier AM waveform **15802**, with a dashed reference **15804** and black sample dots **15806**. Each half sine above or below the dashed reference **15804** can represent a finite duration pulse that possesses information impressed on the carrier by the modulation process.

Sampled systems attempt to extract information in the envelope, at the black sample dots **15806**, if possible. The sample times illustrated by the black sample dots **15806** are shown here at optimum sampling times.

Difficulties arise when the bandpass waveform is at RF. Then sampling is difficult because of sample rate, sample aperture, and aperture uncertainty. When the traditional sampler acquires, the aperture and aperture uncertainty must be minimized such that the number associated with the acquired waveform value possesses great accuracy at a particular instant in time with minimum variance. Sample rate can be reduced by sampling sub-harmonically. However, precisely controlling a minimized aperture makes the process very difficult, if not impossible, at RF.

In FIG. **158**, the area under a half-sine cycle **15808** is illustrated with hatched marks. In accordance with embodiments of the present invention, instead of obtaining a sample of a single waveform voltage value, energy in the hatched area is acquired. By acquiring energy in the hatched area, the effects of aperture uncertainty can be minimized. Moreover, the waveform itself possesses the sampling information between the half sine zero crossings. This is true because the total energy of the hatched area is proportional to the peak of the modulated half sine peak. This is illustrated by EQ. (16), below. All that remains is to extract that latent information. IN embodiments, the underlying theory for optimal extractions of the energy is in fact matched filter theory.

$$E_A=\int_{-\infty}^{\infty}S_i(t)^2dt=2A^2\int_0^{T_A/2}(\sin(2\pi ft))^2dt=\frac{A^2T_A}{2} \qquad \text{EQ. (16)}$$

Historically, an optimization figure of merit is signal-to-noise ration (SNR) at the system output. FIG. **159** illustrates a block diagram of an example optimum processor system

15902, which considers additive white Gaussian noise (AWGN). The general theory described herein can be extended to systems operating in the presence of colored noise as well.

Although an RF carrier with modulated information is typically a power signal, the analysis which follows considers the power signal to be a piece-wise construct of sequential energy signals where each energy waveform is a half sine pulse (single aperture) or multiple sine pulses (see sub-section 2 above). Hence, theorems related to finite time observations, Fourier transforms, etc., may be applied throughout.

Analysis begins with the assumption that a filtering process can improve SNR. No other assumptions are necessary except that the system is casual and linear. The analysis determines the optimum processor for SNR enhancement and maximum energy transfer.

The output of the system is given by the convolution integral illustrated in EQ. (17):

$$S_0(t)=\int_0^\infty h(\tau)S_i(t-\tau)d\tau \quad \text{EQ. (17)}$$

where $h(\tau)$ is the unknown impulse response of the optimum processor.

The output noise variance is found from EQ. (18):

$$\sigma_0^2=N_0\int_0^\infty h^2(\tau)d\tau \quad \text{EQ. (18)}$$

The signal to noise ratio at time t_0 is given by EQ. (19):

$$\frac{S_0^2(t_0)}{\sigma_0^2}=\frac{\left[\int_0^\infty h(\tau)S_i(t_0-\tau)d\tau\right]^2}{N_0\int_0^\infty h^2(\tau)d\tau} \quad \text{EQ. (19)}$$

The Schwarz inequality theorem may be used to maximize the above ratio by recognizing, in EQ. (20), that:

$$\frac{S_0^2(t_0)}{\sigma_0^2}\le\frac{\int_0^\infty h^2(\tau)\int_0^\infty S_i^2(t_0-\tau)d\tau}{N_0\int_0^\infty h^2(\tau)d\tau} \quad \text{EQ. (20)}$$

The maximum SNR occurs for the case of equality in EQ. 20, which yields EQ. (21):

$$\left|\frac{S_0^2(t_0)}{\sigma_0^2}\right|_{\max}=\frac{1}{N_0}\int_0^\infty S_i^2(t_0-\tau)d\tau \quad \text{EQ. (21)}$$

In general therefore:

$$h(\tau)=kS_1(t_0-\tau)u(\tau) \quad \text{EQ. (22)}$$

where $u(\tau)$ is added as a statement of causality and k is an arbitrary gain constant. Since, in general, the original waveform $S_i(t)$ can be considered as an energy signal (single half sine for the present case), it is important to add the consideration of t_0, a specific observation time. That is, an impulse response for an optimum processor may not be optimal for all time. This is due to the fact that an impulse response for realizable systems operating on energy signals will typically die out over time. Hence, the signal at t_0 is said to possess the maximum SNR.

This can be verified by maximizing EQ. (21) in general.

$$\left(\frac{d}{dt}\right)\frac{S_0^2(t)}{\sigma_0^2}=0 \quad \text{EQ. (23)}$$

It is of some interest to rewrite EQ. (21) by a change of variable, substituting $t=t_0-\tau$. This yields:

$$k\int_0^\infty S_i^2(t_0-\tau)d\tau=k\int_{-\infty}^{t_0}S_i^2(t)dt \quad \text{EQ. (24)}$$

This is the energy of the waveform up to time t_0. After t_0, the energy falls off again due to the finite impulse response nature of the processor. EQ. (24) is of great importance because it reveals an often useful form of a matched filter known as a correlator. That is, the matched filter may be implemented by multiplying the subject waveform by itself over the time interval defined for the waveform, and then integrated. In this realization the maximum output occurs when the waveform and its optimal processor aperture are exactly overlapped for $t_0=T_a$. It should also be evident from the matched filter equivalency stated in EQ. (24) that the maximum SNR solution also preserves the maximum energy transfer of the desired waveform through the processor. This may be proven using the Parseval and/or Rayliegh energy theorems. EQ. (24) relates directly to Parseval's theorem.

3.2 Frequency Domain Description

The previous sub-section derived an optimal processor from the time domain point-of-view according to embodiments of the invention. Alternately, Fourier transforms may be applied to obtain a frequency domain representation for h(t). This result is shown below.

$$H(f)=kS_i^*(f)e^{-j2\pi ft_0} \quad \text{EQ. (25)}$$

Letting $j\omega=j2\,Bf$ and $t_0=T_A$, we can write the following EQ. (26) for

$$H(j\omega)=\frac{2}{T_A}e^{-j\omega T_A/2}\frac{\sin(\omega T_A/2)}{\omega T_A/2} \quad \text{EQ. (20)}$$

FIGS. **160** and **161**.

The frequency domain representation in FIG. **160** represents the response of an optimum processor according to embodiments. FIG. **161** illustrates responses of processors that use parameters different than T_A. For $t_0<<T_A$, the frequency domain response possesses too wide a bandwidth which captures too little of the main lobe of desired energy with respect to out of band noise power. Conversely, when $t_0>>T_A$, the energy transfer from the signal's main lobe is very inefficient. Therefore, proper selection of T_A is key for implementation efficiency.

Another simple but useful observation is gleaned from EQ. (24) and Rayleigh's Energy Theorem for Fourier transforms:

$$E=\int_{-\infty}^\infty|S_i(t)|^2dt=\int_{-\infty}^\infty|H(f)|^2df \quad \text{EQ. (27)}$$

EQ. (27) verifies that the transform of the optimal filter of various embodiments should substantially match the transform of the specific pulse, which is being processed, for efficient energy transfer.

4. Finite Time Integrating Characterization/Embodiment

It is not always practical to design the matched filter with passive networks. Sometimes the waveform correlation of $S_i(t)$ is also cumbersome to generate exactly. However, a single aperture realization of embodiments of the present invention is practical, even in CMOS, with certain concessions.

Consider FIGS. **162** and **163**, which illustrate an optimum single aperture realization of embodiments of the present invention using sub harmonic sampling (3rd harmonic) and a processor **16310** according to such embodiments. Ideally over the aperture of interest, T_A, a half sine impulse response or waveform is used to operate on the original gated $S_i(t)$. Suppose for ease of implementation, however, that a rectangular impulse response is used, as illustrated in FIGS. **164**A and **164**B. The Fourier transform of this processor still overlaps the Fourier transform for the original pulse $S_i(t)$ with exactly the same nulls, as shown in FIG. **164**C. Although the Fourier correlation is not perfect, it is still quite good. Furthermore, it can be implemented using a simple switch that lets the half sine through in order to charge a capacitor, which acquires the total energy of the half sine at $t_0 \approx T_A$.

Applying EQ. (26) for both the matched filter and non-matched filter embodiments yields:

$$E_{A0} = \int_0^{T_A} S_i^2(t)dt = \frac{A^2 T_A}{2}$$

Optimal Matched Filter Embodiment Result; and

$$E_{AS0} = \left(\int_0^{T_A} A \cdot S(t)\right)^2 dt = \left(\frac{2T_A A}{\pi}\right)^2$$

Finite Time Integrator Embodiment Result

It turns out in practice that realizable apertures are not perfectly rectangular and do possess a finite rise and fall time. In particular, they become triangular or nearly sinusoidal for very high frequency implementations. Thus, the finite time integrating processor result tends toward the matched filtering/correlating processor result when the aperture becomes sine-like, if the processor possesses constant impedance across the aperture duration. Even though the matched filter/correlator response produces a lower output value at T_A, it yields a higher SNR by a factor of 0.9 dB, as further illustrated below in sub-section 6.

5. RC Processing Characterization/Embodiment

Sometimes a precise matched filter is difficult to construct, particularly if the pulse shape is complex. Often, such complexities are avoided in favor of suitable approximations, which preserve the essential features. The single aperture realization of embodiments of the present invention is usually implemented conceptually as a first order approximation to a matched filter where the pulse shape being matched is a half-sine pulse. As shown in above, in embodiments, the matched filter is applied recursively to a carrier waveform. The time varying matched filter output correlation contains information modulated onto the carrier. If many such matched filter correlation samples are extracted, the original information modulated onto the carrier is recovered.

A baseband filter, matched or otherwise, may be applied to the recovered information to optimally process the signal at baseband. The present invention should not be confused with this optimal baseband processing. Rather embodiments of the present invention are applied on a time microscopic basis on the order of the time scale of a carrier cycle.

FIG. **165** illustrates a basic circuit **16502** that can be used to describe an example RC processor according to embodiments of the present invention. Circuit **16502** comprises a switch **16504**. The switch **16504** is closed on a T_A basis in order to sample $V_i(t)$. In the analysis that follows, the transfer function and impulse response are derived for circuit **16502**.

The switch **16504** functions as a sampler, which possesses multiplier attributes. Heviside's operator is used to model the switch function. The operator is multiplied in the impulse response, thus rendering it essential to the matched filtering/correlating process.

In the analysis that follows, only one aperture event is considered. That is, the impulse response of the circuit is considered to be isolated aperture-to-aperture, except for the initial value inherited from the previous aperture.

For circuit **16502**, shown in FIG. **165**:

$$V_0(t) = \frac{1}{C}\int i(t)dt \qquad \text{EQ. (28)}$$

$$i(t) = \frac{V_i(t)[u(t) - u(t - T_A)] - V_0(t)}{R} \qquad \text{EQ. (29)}$$

$$V_0(t) = \int \frac{V_i(t)[u(t) - (t - T_A)] - V_0(t)}{RC} dt \qquad \text{EQ. (30)}$$

$$V_0(t) + \int \frac{V_0(t)}{RC} dt = \int \frac{V_i(t)[u(t) - u(t - T_A)]}{RC} dt \qquad \text{EQ. (31)}$$

EQ. (31) represents the integro-differential equation for circuit **16502**. The right hand side of EQ. (31) represents the correlation between the input waveform $V_i(t)$ and a rectangular window over the period T_A.

The Laplace transform of EQ. (31) is:

EQ. (32)

$$V_0(s)\left(1 + \frac{1}{sRC}\right) + \frac{V_0(0)}{sRC} = V_i(s)\left(\frac{1 - e^{-sT_A}}{s^2 RC}\right) + \frac{V_i(0)}{sRC}$$

(initial condition) (initial condition)

Consider that the initial condition equal to zero, then:

$$H(s) = \frac{V_0(s)}{V_i(s)} = RC^{-1} \cdot \left(\frac{1 - e^{-sT_A}}{s}\right) \cdot \left(\frac{1}{s + (RC)^{-1}}\right) \qquad \text{EQ. (33)}$$

$$\therefore h(t) = \left(\frac{e^{\frac{t}{-RC}}}{RC}\right)[u(t) - u(t - T_A)] \qquad \text{EQ. (34)}$$

Suppose that

$$V_i(t) = A\sin\left(2\pi\frac{f_A}{2}t + \phi\right),$$

as illustrated in FIG. **166**, where $f_A = T_A^{-1}$ and ϕ is an arbitrary phase shift. (FIG. **166** also shows h(t).) Note in FIG. **166** that h(t) is not ideally a sine pulse. However, the cross correlation of h(t) and $V_i(t)$ can still be quite good if RC is properly selected. This is the optimization, which is required in order to approximate a matched filter result (namely SNR optimization given h(t) and $V_i(t)$).

$$V_0(t) = V_i(t) * h(t) = A\sin(\pi f_A t) * h(t);\ 0 \le t \le T_A \qquad \text{EQ. (35)}$$

-continued

$$V_0(t) = \int_0^{\infty} \sin(\pi f_A(t-\tau)) \frac{e^{\frac{-\tau}{RC}}}{RC} d\tau \quad \text{EQ. (36)}$$

By a change of variables;

$$V_0(t) = \quad \text{EQ. (37)}$$

$$\int_{-\infty}^{t} A\sin(\pi f_A \tau + \phi) \cdot \frac{e^{\frac{-(t-\tau)}{RC}}}{RC} [u(t-\tau) - u(t-\tau-T_A)] d\tau$$

where $f_A \Delta 2f = T_A^{-1}$

$$\therefore V_0(t) =$$

$$\frac{A}{1+(\pi f_A RC)^2}(-\pi f_A t + \phi) + \sin(\pi f_A t + \phi) - Ae^{-t/RC}$$

$$\left(\sin\phi - \frac{(\pi f_A RC)^2}{1+(\pi f_A RC)^2} \cdot \sin\phi - \frac{\pi f_A RC}{1+(\pi f_A RC)^2} \cdot \cos\phi\right)$$

$$0 \le t \le T_A$$

$$V_0(t) = \left[\frac{1}{1+(RC\pi f_A)^2}\right]$$

$$(\sin(\pi f_A t) - \pi f_A RC \cdot \cos(\pi f_A t) + \pi f_A RC \cdot e^{-t/RC})$$

$$0 \le t \le T_A, \phi = 0$$

Notice that the differential equation solution provides for carrier phase skew, ϕ. It is not necessary to calculate the convolution beyond T_A since the gating function restricts the impulse response length.

FIG. **167** illustrates the response $V_0(t)$. The output peaks just before T_A because the example RC processor is not a perfect matched filtering/correlating processor, but rather an approximation. FIG. **168** illustrates that the maximum of the function occurs at t≈0.75 T_A, for a β=2.6, which can be verified by evaluating:

$$\frac{\partial}{\partial t} V_0(t) = 0 \quad \text{EQ. (38)}$$

Solving the differential equation for $V_0(t)$ permits an optimization of $\beta=(RC)^{-1}$ for maximization of V_0.

FIG. **169** illustrates a spread of values for beta. In embodiments, the peak β occurs at approximately β≈2.6. FIG. **169** illustrates a family of output responses for processors according to embodiments of the present invention having different beta values. In embodiments, the definition used for optimality to obtain β=2.6 is the highest value of signal obtained at the cutoff instant, T_A. Other criteria can be applied, particularly for multiple pulse accumulation and SNR consideration.

In embodiments, one might be tempted to increase β and cutoff earlier (i.e., arbitrarily reduce T_A). However, this does not necessarily always lead to enhanced SNR, and it reduces charge transfer in the process. It can also create impedance matching concerns, and possibly make it necessary to have a high-speed buffer. That is, reducing T_A and C is shown below to decrease SNR. Nevertheless, some gain might be achieved by reducing T_A to 0.75 for β=2.6, if maximum voltage is the goal.

In embodiments, in order to maximize SNR, consider the following. The power in white noise can be found from:

$$\sigma^2 = N_0 \int_0^{\infty} h^2(\lambda) d\lambda \quad \text{EQ. (39)}$$

$$\sigma^2 = N_0 \int_0^{\infty} \left(\frac{e^{\frac{-2\lambda}{RC^2}}}{RC}\right)(u(t) - u(\lambda - T_A)) d\lambda \quad \text{EQ. (40)}$$

$$\sigma^2 = \frac{\beta N_0(1-e^{-2\beta N_0 T_A})}{2} @ T_A \quad \text{EQ. (41)}$$

$$\beta = (RC)^{-1}$$

Notice that σ^2 is a function of RC.

The signal power is calculated from:

$$(V_0(t))^2 = \left(\frac{1}{1+(\beta^{-1}\pi f_A)^2}\right)^2 \quad \text{EQ. (42)}$$

$$(\sin(\pi f_A t) - \beta^{-1}\pi f_A \cdot \cos(\pi f_A t) + \beta^{-1}\pi f_A e^{-\beta t})^2$$

Hence, the SNR at T_A is given by:

$$\frac{(V_0(r))^2}{\sigma^2}\Big|_{t=T_1} = \frac{2}{\beta N_0(1-e^{-2\beta N_0 T_A})} \quad \text{EQ. (43)}$$

$$\left(\frac{1}{1+(\beta^{-1}\pi f_A)^2}\right)^2 (\beta^{-1}\pi f_A + \beta^{-1}\pi f_A e^{-\beta T_A})^2$$

Maximizing the SNR requires solving:

$$\frac{\partial}{\partial\beta}\left(\frac{V_0(t)^2}{\sigma^2}\right) = 0 \quad \text{EQ. (44)}$$

Solving the SNR_{max} numerically yields β values that are ever decreasing but with a diminishing rate of return.

As can be seen in FIG. **170**, in embodiments, β=2.6 for the maximum voltage response, which corresponds to a normalized SNR relative to an ideal matched filter of 0.431. However, in embodiments, selecting a β of 1/10 the β, which optimizes voltage, produces a superior normalized SNR of 0.805 (about 80.5% efficiency) This is a gain in SNR performance of about 2.7 dB.

In certain embodiments, it turns out that for an ideal matched filter the optimum sampling point corresponding to correlator peak is precisely T_A. However, in embodiments, for the RC processor, the peak output of occurs at approximately 0.75 T_A for large β (i.e., β=2.6). That is because the impulse response is not perfectly matched to the carrier signal. However, as β is reduced significantly, the RC processor response approaches the efficiency of the finite time integrating processor response in terms of SNR performance. As β is lowered, the optimal SNR point occurs closer to T_A, which simplifies design greatly. Embodiments of the present invention provides excellent energy accumulation over T_A for low β, particularly when simplicity is valued.

5.1 Charge Transfer and Correlation

The basic equation for charge transfer is:

$$\frac{dq}{dt} = C\frac{dv}{dt}, \text{ (assuming } C \text{ constant over time)} \quad \text{EQ. (45)}$$

$$q = CV$$

Similarly the energy u stored by a capacitor can be found from:

$$u = \int_0^q \frac{q_x}{C} dq_x = \frac{q^2}{2C} \quad \text{EQ. (46)}$$

From EQs. (45) and (46):

$$u = \frac{Cv^2}{2} \quad \text{EQ. (47)}$$

Thus, the charge stored by a capacitor is proportional to the voltage across the capacitor, and the energy stored by the capacitor is proportional to the square of the charge or the voltage. Hence, by transferring charge, voltage and energy are also transferred. If little charge is transferred, little energy is transferred, and a proportionally small voltage results unless C is lowered.

The law of conversation of charge is an extension of the law of the conservation of energy. EQ. (45) illustrates that if a finite amount of charge must be transferred in an infinitesimally short amount of time then the voltage, and hence voltage squared, tends toward infinity. The situation becomes even more troubling when resistance is added to the equation. Furthermore,

$$V_c = \frac{1}{C}\int_0^{T_A} i dt \quad \text{EQ. (48)}$$

This implies an infinite amount of current must be supplied to create the infinite voltage if T_A is infinitesimally small. Clearly, such a situation is impractical, especially for a device without gain.

In most radio systems, the antenna produces a small amount of power available for the first conversion, even with amplification from an LNA. Hence, if a finite voltage and current restriction do apply to the front end of a radio then a conversion device, which is an impulse sampler, must by definition possess infinite gain. This would not be practical for a switch. What is usually approximated in practice is a fast sample time, charging a small capacitor, then holding the value acquired by a hold amplifier, which preserves the voltage from sample to sample.

The analysis that follows shows that given a finite amount of time for energy transfer through a conversion device, the impulse response of the ideal processor, which transfers energy to a capacitor when the input voltage source is a sinusoidal carrier and possesses a finite source impedance, is represented by embodiments of the present invention. If a significant amount of energy can be transferred in the sampling process then the tolerance on the charging capacitor can be reduced, and the requirement for a hold amplifier is significantly reduced or even eliminated.

In embodiments, the maximum amount of energy available over a half sine pulse can be found from:

$$u = \int_0^{T_A} S_i^2(t) dt = \frac{A^2 T_A}{2} \quad \text{EQ. (49)}$$

This points to a correlation processor or matched filter processor. If energy is of interest then a useful processor, which transfers all of the half sine energy, is revealed in EQ. (48), where T_A is an aperture equivalent to the half sine pulse. In embodiments, EQ. (49) provides the clue to an optimal processor.

Consider the following equation sequence.

$$\int_0^{\infty} h(\tau) S_i(t-\tau) d\tau \Rightarrow \int_0^{T_A} k S_i^2(T_A - \tau) d\tau \Rightarrow \int_{-0}^{T_A} S_i^2(t) dt \quad \text{EQ. (50)}$$

where $h(\theta)=S_i(T_A-\theta)$ and $t=T_A-\theta$.

This is the matched filter equation with the far most right hand side revealing a correlator implementation, which is obtained by a change of variables as indicated. The matched filter proof for $h(\tau)=S_i(T_A-\tau)$ is provided in sub-section 8.4 below. Note that the correlator form of the matched filter is exactly a statement of the desired signal energy. Therefore a matched filter/correlator accomplishes acquisition of all the energy available across a finite duration aperture. Such a matched filter/correlator can be implemented as shown in FIG. **171**.

In embodiments, when optimally configured, the example matched filter/correlator of FIG. **171** operates in synchronism with the half sine pulse $S_i(t)$ over the aperture T_A. Phase skewing and phase roll will occur for clock frequencies, which are imprecise. Such imprecision can be compensated for by a carrier recovery loop, such as a Costas Loop. A Costas Loop can develop the control for the acquisition clock, which also serves as a sub-harmonic carrier. However, phase skew and non-conherency does not invalidate the optimal form of the processor provided that the frequency or phase errors are small, relative to $T^{-1}{}_A$. Non-coherent and differentially coherent processors may extract energy from both I and Q with a complex correlation operation followed by a rectifier or phase calculator. It has been shown that phase skew does not alter the optimum SNR processor formulation. The energy which is not transferred to I is transferred to Q and vice versa when phase skew exists. This is an example processor for a finite duration sample window with finite gain sampling function, where energy or charge is the desired output.

A matched filter/correlator embodiment according to the present invention might be too expensive and complicated to build for some applications. In such cases, however, other processes and processors according to embodiments of the invention can be used. The approximation to the matched filter/correlator embodiment shown in FIG. **172** is just one embodiment that can be used in such instances. The finite time integrator embodiment of FIG. **172** requires only a switch and an integrator. Sub-section 6 below shows that this embodiment of the present invention has only a 0.91 dB difference in SNR compared to the matched filter/correlator embodiment.

Another very low cost and easy to build embodiment of the present invention is the RC processor. This embodiment, shown in FIG. **173**, utilizes a very low cost integrator or capacitor as a memory across the aperture. If C is suitable

chosen for this embodiment, its performance approaches that of the matched filter/correlator embodiment, shown in FIG. **171**. Notice the inclusion of the source impedance, R, along with the switch and capacitor. This simple embodiment nevertheless can approximate the optimum energy transfer of the matched filter/correlator embodiment if properly designed.

When maximum charge is transferred, the voltage across the capacitor **17304** in FIG. **173** is maximized over the aperture period for a specific RC combination.

Using EQs. (45) and (48) yields:

$$q = C \cdot \frac{1}{C}\int_0^{T_A} i_c dt \qquad \text{EQ. (51)}$$

If it is accepted that an infinite amplitude impulse with zero time duration is not available or practical, due to physical parameters of capacitors like ESR, inductance and breakdown voltages, as well as currents, then EQ. (51) reveals the following important considerations for embodiments of the invention:

- The transferred charge, q, is influenced by the amount of time available for transferring the charge;
- The transferred charge, q, is proportional to the current available for charging the energy storage device; and
- Maximization of charge, q, is a function of i_c, C, and T_A.

Therefore, it can be shown that for embodiments:

$$q_{max} = Cv_{max} = C\left[\frac{1}{C}\int_0^{T_A} i_c dt\right]_{max} \qquad \text{(EQ. 52)}$$

The impulse response for the RC processing network was found in sub-section 5.2 below to be;

$$h(t) = \frac{e^{\frac{-\tau}{RC}}}{RC}[u(\tau) - u(\tau - T_A)] \qquad \text{EQ. (53)}$$

Suppose that T_A is constrained to be less than or equal to ½ cycle of the carrier period. Then, for a synchronous forcing function, the voltage across a capacitor is given by EQ. (54).

$$V_0(t) = \int_{-\infty}^{\infty} \sin(\pi f_A \tau) \cdot \frac{e^{\frac{-(t-\tau)}{RC}}}{RC} d\tau \qquad \text{EQ. (54)}$$

Maximizing the charge, q, requires maximizing EQ. (37) with respect to t and β.

$$\frac{\partial^2 V_0(t)}{\partial t \partial \beta} = 0 \qquad \text{EQ. (55)}$$

It is easier, however, to set R=1, T_A=1, A=1, f_A=T_A^{-1} and then calculate q=cV_0 from the previous equations by recognizing that

$$q = \frac{\beta^{-1}}{R} V_0 = cV_0,$$

which produces a normalized response.

FIG. **174** illustrates that increasing C is preferred in embodiments of the invention. It can be seen in FIG. **174** that as C increases (i.e., as ∃ decreases) the charge transfer also increases. This is what is to be expected based on the optimum SNR solution. Hence, for embodiments of the present invention, an optimal SNR design results in optimal charge transfer. As C is increased, bandwidth considerations should be taken into account.

In embodiments, EQ. (49) establishes T_A as the entire half sine for an optimal processor. However, in embodiments, optimizing jointly for t and β reveals that the RC processor response creates an output across the energy storage capacitor that peaks for t_{max}≈0.75 T_A, and β_{max}≈2.6, when the forcing function to the network is a half sine pulse.

In embodiments, if the capacitor of the RC processor embodiment is replaced by an ideal integrator then $t_{max} \rightarrow T_A$.

$$\beta T_A \approx 1.95 \qquad \text{EQ. (56)}$$

where ∃=$(RC)^{-1}$

For example, for a 2.45 GHz signal and a source impedance of 50Ω, EQ. (56) above suggests the use of a capacitor of ≈2 pf. This is the value of capacitor for the aperture selected, which permits the optimum voltage peak for a single pulse accumulation. For practical realization of the present invention, the capacitance calculated by EQ. (56) is a minimum capacitance. SNR is not considered optimized at βT_A≈1.95. As shown earlier, a smaller β yields better SNR and better charge transfer. In embodiments, as discussed below, it turns out that charge can also be optimized if multiple apertures are used for collecting the charge.

In embodiments, for the ideal matched filter/correlator approximation, βT_A is constant and equivalent for both consideration of optimum SNR and optimum charge transfer, and charge is accumulated over many apertures for most practical designs. Consider the following example, β=0.25, and T_A=1.

Thus βT_A=0.25. At 2.45 GHz, with R=50Ω, C can be calculated from:

$$C \geqq \frac{T_A}{R(.25)} \geq 16.3 \text{ pf} \qquad \text{EQ. (57)}$$

The charge accumulates over several apertures, and SNR is simultaneously optimized melding the best of two features of the present invention. Checking CV for βT_A≅1.95 vs. βT_A=0.25 confirms that charge is optimized for the latter.

5.2 Load Resistor Consideration

The general forms of the differential equation and transfer function, described above, for embodiments of the present invention are the same as for a case involving a load resistor, R_L, applied across capacitor, C. FIG. **175**A illustrates an example RC processor embodiment **17502** of the present invention having a load resistance **17504** across a capacitance **17506**.

Consider RC processing embodiment **17502** (without initial conditions).

EQ. (33) becomes:

$$H(s) = \frac{1 - e^{-sT_A}}{s}\left(\frac{1}{sCR + k}\right) \quad \text{EQ. (58)}$$

$$k = (R/R_L + 1) \quad \text{EQ. (59)}$$

$$h(t) = \left(\frac{e^{-\frac{t \cdot k}{RC}}}{RC}\right)[u(t) - (t - T_A)] \quad \text{EQ. (60)}$$

It should be clear that R_L **17504**, and therefore k, accelerate the exponential decay cycle.

$$V_0(t) = \int_{-\infty}^{t} \sin(\pi f_a \tau) \cdot \frac{e^{-\frac{k(t-\tau)}{RC}}}{RC} d\tau \quad \text{EQ. (61)}$$

$$V_0(t) = \left(\frac{1}{k^2 + (\pi f_A)^2}\right)\left[k \cdot \sin(\pi f_A t) - \pi f_A RC \cdot \cos(\pi f_A t) + RCe^{-\frac{kt}{RC}}\right] 0 \le t \le T_A \quad \text{EQ. (62)}$$

This result is valid only over the acquisition aperture. After the switch is opened, the final voltage that occurred at the sampling instance $t \approx T_A$ becomes an initial condition for a discharge cycle across R_L **17504**. The discharge cycle possesses the following response:

$$V_D = \frac{V_A \cdot e^{-\frac{t}{R_L C}}}{R_L C} u(t - T_A)(\text{single event discharge}) \quad \text{EQ. (63)}$$

V_A is defined as V_0 ($t \approx T_A$). Of course, if the capacitor **17506** does not completely discharge, there is an initial condition present for the next acquisition cycle.

FIG. **175**B illustrates an example implementation of the invention, modeled as a switch S, a capacitor C_S, and a load resistance R. FIG. **175**D illustrates example energy transfer pulses, having apertures A, for controlling the switch S. FIG. **175**C illustrates an example charge/discharge timing diagram for the capacitor C_S, where the capacitor C_S charges during the apertures A, and discharge between the apertures A.

Equations 63.1 through 63.15 derive a relationship between the capacitance of the capacitor C_S ($C_S(R)$), the resistance of the resistor R, the duration of the aperture A (aperture width), and the frequency of the energy transfer pulses (freq LO). Equation 63.11 illustrates that optimum energy transfer occurs when x=0.841. Based on the disclosure herein, one skilled in the relevant art(s) will realize that values other that 0.841 can be utilized.

$$\phi = \frac{1}{C}\int i(t)\partial t + Ri(t) \quad \text{EQ. (63.1)}$$

$$\frac{\partial}{\partial t}\phi = \frac{\partial}{\partial t}\left[\frac{1}{C}\int i(t)\partial t + Ri(t)\right] \quad \text{EQ. (63.2)}$$

$$\phi = \frac{i(t)}{C_s} + \frac{R\partial i(t)}{\partial t} \quad \text{EQ. (63.3)}$$

$$\phi = \frac{1}{C_s} + R \cdot s \quad \text{EQ. (63.4)}$$

-continued

$$s = \frac{-1}{C_s \cdot R}, \text{ by definition } i_{init}(t) = \frac{V_{C_s}init}{R} \quad \text{EQ. (63.5)}$$

$$i(t) = \left(\frac{V_{C_s}init}{R}\right) \cdot e^{\left(\frac{-t}{C_s \cdot R}\right)} \quad \text{EQ. (63.6)}$$

$$V_{out}(t) = R \cdot i(t) = V_{C_s}init \cdot e^{\left(\frac{-t}{C_s \cdot R}\right)} \quad \text{EQ. (63.7)}$$

Maximum power transfer occurs when:

$$\text{Power\_Final} = \frac{1}{\sqrt{2}} \cdot \text{Peak\_Power} \quad \text{EQ. (63.8)}$$

$$\text{Power\_Peak} = \frac{(V_{C_s}\text{peak})^2}{R} \quad \text{EQ. (63.9)}$$

$$\text{Power\_Final} = \frac{(x \cdot V_{C_s}\text{peak})^2}{R} \quad \text{EQ. (63.10)}$$

$$\frac{(x \cdot V_{C_s}\text{peak})^2}{R} = \frac{(V_{C_s}\text{peak})^2}{R} \cdot \frac{1}{\sqrt{2}} \text{ yields} \quad \text{EQ. (63.11)}$$

$x = 0.841$

Let V_{Cs}init=1, then V_{out}(t)=0.841 when

$$t = \frac{1}{freqLO} - \text{Aperture\_Width} \quad \text{EQ. (63.12)}$$

$$0.841 = 1 \cdot e^{\left(\frac{\frac{1}{freqLO} - Aperture\_Width}{C_s \cdot R}\right)} \quad \text{EQ. (63.13)}$$

$$\ln(0.841) = \left(\frac{\frac{1}{freqLo} - \text{Aperture\_Width}}{C_s \cdot R}\right) \quad \text{EQ. (63.14)}$$

$$C_s(R) = \left(\frac{\frac{1}{freqLO} - \text{Aperture\_Width}}{-\ln(0.841) \cdot R}\right) \quad \text{EQ. (63.15)}$$

6. Signal-to-Noise Ratio Comparison of the Various Embodiments

The prior sub-sections described the basic SNR definition and the SNR of an optimal matched filter/correlator processor according to embodiments of the present invention. This subsection section describes the SNR of additional processor embodiments of the present invention and compares their SNR with the SNR of a optimal matched filter/correlator embodiment. The description in this sub-section is based on calculations relating to single apertures and not accumulations of multiple aperture averages. Since SNR is a relative metric, this method is useful for comparing different embodiments of the present invention.

EQ. (65), which can be obtained from EQ. (64), represents the output SNR for a single aperture embodiment assuming a constant envelope sine wave input. The results could modify according to the auto-correlation function of the input process, however, over a single carrier half cycle, this relationship is exact.

$$SNR_{opt} \Delta \frac{1}{N_0}\int_0^{\infty} S_i^2(t_0-\tau)d\tau \quad \text{EQ. (64)}$$

$$SNR_{opt} \Delta \frac{T_A A^2}{2N_0} \text{(single aperture case)} \quad \text{EQ. (65)}$$

The description that follows illustrates the SNR for three processor embodiments of the present invention for a given input waveform. These embodiments are:

An Example Optimal Matched Filter/Correlator Processor Embodiment;

An Example Finite Time Integrator processor Embodiment; and

An Example RC Processor Embodiment

The relative value of the SNR of these three embodiments is accurate for purposes of comparing the embodiments. The absolute SNR may be adjusted according to the statistic and modulation of the input process and its complex envelope.

Consider an example finite time integrator processor, such as the one illustrated in FIG. **1648**. The impulse response of the finite time integrator processor is given by EQ. (66):

$$h(t)=k,\ 0\le t\le T_A \quad \text{EQ. (66)}$$

where k is defined as an arbitrary constant.

The output of the finite time integrator processor, y(t), is found from the input, x(t), using:

$$y(t)=\int_{t-T_A}^{t} x(u)du \quad \text{EQ. (67)}$$

A change of variables yields EQ. (68):

$$y(t-\tau)=\int_{t-\tau-T_A}^{t-\tau} x(v)dv \quad \text{EQ. (68)}$$

The output auto correlation then becomes that shown in EQ. (69):

$$R_y(\tau)=\int_{t-T_A}^{t}du\int_{t-\tau-T_A}^{t-\tau} R_x(u-v)dv \quad \text{EQ. (69)}$$

which leads to:

$$R_x(u-v)=\frac{1}{2\pi}\int_{-\infty}^{\infty} S_x(\omega)e^{j\omega(u-v)}d\omega \quad \text{EQ. (70)}$$

This Fourier transform may be substituted into the expression for $R_y(\tau)$, in EQ. (71), which becomes:

$$R_y(\tau)=\frac{1}{2\pi}\int_{-\infty}^{\infty} S_x(\omega)d\omega\int_{t-T_A}^{t} e^{S\omega u}du\int_{t-\tau-T_A}^{t-\tau} e^{-j\omega v}dv \quad \text{EQ. (71)}$$

$$R_y(\tau)= \quad \text{EQ. (72)}$$
$$\frac{1}{2\pi}\int_{-\infty}^{\infty} S_x(\omega)\left[\frac{e^{j\omega t}(1-e^{-j\omega T_A})}{j\omega}\right]\left[\frac{e^{-j\omega t(i-\tau)}(1-e^{-j\omega T_A})}{j\omega}\right]d\omega$$

$$\therefore S_y(\omega)=S_x(\omega)\frac{\sin^2\omega T_A/2}{(\omega/2)^2} \quad \text{EQ. (73)}$$

$S_y(\omega)$ is the power spectral density at the output of the example finite time integrator, whose integration aperture is T_A and whose input power spectrum is defined by $S_x(\omega)$. For the case of wide band noise:

$$S(\omega)=\frac{N_0}{2\pi}\frac{\sin^2\omega T_A/2}{(\omega/2)^2} \quad \text{EQ. (74)}$$

The total noise power across the band can be found from EQ. (75):

$$\int_{-\infty}^{\infty} S_{yn}(\omega)d\omega=\frac{N_0}{2\pi}\int_{-\infty}^{\infty}\frac{\sin^2(\omega T_A/2)}{(\omega/2)^2}d\omega=T_A N_0 \quad \text{EQ. (75)}$$

This result can be verified by EQ. (76):

$$\overline{Y^2}N_0\int_0^{\infty}h^2(\tau)d\tau \quad \text{EQ. (76)}$$

The signal power over a single aperture is obtained by EQ. (77):

$$y(t)^2=(2A\int_0^{T_A/2}\sin(\omega t)dt)^2 \quad \text{EQ. (77)}$$

Choosing A=1, the finite time integrator output SNR becomes:

$$SNR_{int}=\frac{4T_A}{\pi^2 N_0} \quad \text{EQ. (78)}$$

An example RC filter can also be used to model an embodiment of the present invention. The mean squared output of a linear system may be found from EQ. (79):

$$\overline{Y^2}=\int_0^{\infty}d\tau_1\int_0^{\infty}R_x(\tau_A-\tau_1)h(\tau_1)h(\tau_2)d\tau_2 \quad \text{EQ. (79)}$$

For the case of input AWGN:

$$R_{xn}(\tau)=N_0\delta(\tau) \quad \text{EQ. (80)}$$

$$\overline{Y^2}=N_0\int_0^{\infty}d\tau_1\int_0^{\infty}\delta(\tau_2-\tau_1)h(\tau_1)h(\tau_2)d\tau_2 \quad \text{EQ. (81)}$$

$$\overline{Y_n^2}=N_0\int_0^{\infty}h^2(\tau)d\tau \quad \text{EQ. (82)}$$

This leads to the result in EQ. (83):

$$H(s)=\frac{1/RC}{s+1/RC}*\left(\frac{1-e^{-sT_A}}{s}\right) \quad \text{EQ. (83)}$$

R is the resistor associated with processor source, and C is the energy storage capacitor.

Therefore;

$$h(t)=\frac{1}{RC}e^{-t/RC}(u(t)-u(t-T_A)) \quad \text{EQ. (84)}$$

And finally:

$$\overline{Y_n^2}=\frac{N_0}{2RC}(1-e^{-(2N_0T_A/RC)}) \quad \text{EQ. (85)}$$

The detailed derivation for the signal voltage at the output to the RC filter is provided in sub-section 5 above. The use of the β parameter is also described in sub-section 5. Hence, the SNR_{RC} is given by:

$$SNR_{RC} = \frac{2(V_0(t_s))^2}{\beta N_0} T_A = 1, A = 1 \quad \text{EQ. (86)}$$

Illustrative SNR performance values of the three example processor embodiments of the present invention are summarized in the table below:

Example Matched Filter	Performance Relative to the Performance of an Optimal Matched Filter Embodiment
$SNR_{MF} = \frac{T_A}{2N_0}$	0 dB
Example Integrator Approximate	
$SNR_{INT} = \frac{4T_A}{\pi^2 N_0}$	−.91 dB
Example RC Approximate (3 example cases for reference)	
$SNR_{RC} = \frac{V_0(t)^2 \cdot 2}{\beta N_0} \cong \frac{.2142}{N_0}$	−3.7 dB, at $T_A = 1, \beta = 2.6$
$SNR_{RC} \cong \frac{.377}{N_0}$	−1.2 dB, at $T_A = .75, \beta = 2.6$
$SNR_{RC} \cong \frac{.405}{N_0}$	−.91 dB, at $T_A = 1, \beta \leq .25$

Notice that as the capacitor becomes larger, the RC processor behaves like a finite time integrator and approximates its performance. As described above in sub-section 5, with a β of 0.25, a carrier signal of 2450 MHz, and R=50Ω, the value for C becomes C≥16.3 pf.

FIG. **176** illustrates the output voltage waveforms for all three processor embodiments. (Note that two curves are shown for the RC correlator processor, ∃=2.6 and ∃=0.25). FIG. **177**A illustrates the relative SNR's over the aperture.

6.2 Carrier Offset and Phase Skew Characteristics of Embodiments of the Present Invention

FIG. **177**B illustrates some basic matched filter waveforms that are common to some communications applications. The first waveform **17750** is a baseband rect function. Since this waveform is symmetric it is easy to visualize the time reversed waveform corresponding to the ideal matched filter impulse response, h(t), which is also a rect function:

$$h(t) * S_i(t-\tau) \int_{t_1}^{t_2} S_i(t-\tau) h(t)\, dt \quad \text{EQ. (86.1)}$$

The second waveform **17760** illustrates the same rect function envelope at passband (RF) and it's matched filter impulse response. Notice the sine function phase reversal corresponding to the required time axis flip. FIG. **177**C shows a waveform **17770**. Waveform **17770** is a single half sine pulse whose time reversed representation is identical. This last impulse response would be optimal but as pointed out earlier may be difficult to implement exactly. Fortunately, an exact replica is not required.

FIG. **177**D illustrates some exemplary approaches for a complex matched filter/correlator processor applied to a variety of waveforms. As shown in FIG. **177**D, approaches **17780** and **17785** are classical ways to producing a complex matched filter/correlator processor. FIG. **177**E shows approach **17790**. Approach **17790** shows one embodiment of a complex matched filter/correlator processor implemented with the UFT as the processor. The only difference in the UFT approach **17790** is the duration of the pulse envelope. The fact that the gating pulse is small compared to other applications for a correlator is of little consequence to the complex baseband processor. When there is no phase skew then all of the correlated energy is transferred to the I output. When there is a phase skew then a portion of the aliased down converted energy is transferred to the I output and the remainder to the Q. All of the correlated energy is still available, in its optimally filtered form, for final processing in the BB processor.

The fact that a non-coherent processor is used or a differentially coherent BB processor used in lieu of a coherent Costas Loop in no way diminishes the contribution of the UFT correlator effect obtained by selecting the optimal aperture T_A based on matched filter theory.

Consider FIG. **177**E which illustrates an aperture with a phase shifted sine function. In addition, a derivation is provided which indicates that the aperture with phase skew, as referenced to the half sine function, can be represented by the fundamental correlator kernel multiplied by a constant. This provides insight into the interesting SNR properties of the UFT which are based on matched filter principles over the aperture regardless of phase skew ϕ.

Moreover, Section IV, part 5.1 above illustrates that a complex UFT downconverter which utilizes a bandpass filter actually resembles the optimal matched filter/correlator kernel in complex form with the in phase result scaled by cos ϕ and the quadrature phase component scaled by sin ϕ. This process preserves all the energy of the downconverter signal envelope (minus system loses) with a part of the energy in I and the remainder in Q.

7. Multiple Aperture Embodiments of the Present Invention

The above sub-sections describe single aperture embodiments of the present invention. That is, the above sub-sections describe the acquisition of single half sine waves according to embodiments of the invention. Other embodiments of the present invention are also possible, however, and the present invention can be extended to other waveform partitions that capture multiple half sine waves. For example, capturing two half sine waves provides twice the energy compared to capturing only a single half sine. Capturing n half sines provides n times the energy, et cetera, until sub harmonic sampling is no longer applicable. The invention is directed to other embodiments as well. Of course, the matched filter waveform requires a different correlating aperture for each new n. This aspect of the present invention is illustrated in FIGS. **178**A and **178**B.

In the example of FIG. **178**B, the sample aperture window is twice as long as the examples in the previous sub-sections. The matched filter impulse response in FIG. **178**B is bipolar to accommodate a full sine cycle. The embodiment of this example can be implemented, for example, with a rectangular bipolar function (Haar's Wavelet) gating device.

Fourier transforming the components for the example processor yields the results shown in FIG. **179** and EQ. (87).

$$S(f) \cong \sum_{n=-\infty}^{\infty} \frac{Af_s T_A}{2} \left[\begin{array}{l} \frac{\sin(\pi(nf_s - Nf_s)T_A)}{(\pi(nf_s - Nf_s)T_A)} + \\ \frac{\sin(\pi nf_s + Nf_s)T_A}{(\pi(nf_s + Nf_s)T_A)} \end{array} \right] \delta(f - nf_s) \quad \text{EQ. (87)}$$

The transform of the periodic, sampled, signal is first given a Fourier series representation (since the Fourier transform of a power signal does not exist in strict mathematical sense) and each term in the series is transformed sequentially to produce the result illustrated. Notice that outside of the desired main lobe aperture response that certain harmonics are nulled by the (sin x)/x response. Even those harmonics, which are not completely nulled, are reduced by the side lobe attenuation. Some sub-harmonics and super-harmonics are eliminated or attenuated by the frequency domain nulls and side lobes of the bipolar matched filter/correlator processor, which is a remarkable result.

Theoretically, arbitrary impulse responses may be constructed in the manner above, particularly if weighting is applied across the aperture or if multiple apertures are utilized to create a specific Fourier response. FIR filters and convolvers may be constructed by extending the aperture and utilizing the appropriate weighting factors. Likewise, disjoint or staggered apertures may be constructed to provide a particular desired impulse response. These apertures can be rearranged and tuned 'on the fly'.

FIG. **180** (I/Q Bipolar Aperture for 2.4-2.5 GHz 3rd Harmonic Down Converter Application) and FIG. **181** (Down Converted I/Q Waveforms-Slight Carrier Offset) illustrate the results from an actual circuit design and simulation targeting the 2.4-2.5 GHz ISM band and implementing a bipolar weighted aperture. FIG. **180** illustrates actual gating pulses, which form the apertures for I−, I+, Q−, and Q+. FIG. **181** illustrates the baseband I and Q outputs corresponding to the down converter. In embodiments, the sequence I−, I+, Q− and Q+ apertures are repeated every three carrier cycles, nominally. Hence, out of six sine carrier segments, four are captured. Conversion losses well below 10 dB are possible with this embodiment of the present invention.

8. Mathematical Transform Describing Embodiments of the Present Invention

8.1 Overview

The operation of the present invention represents a new signal-processing paradigm. Embodiments of the invention can be shown to be related to particular Fourier sine and cosine transforms. Hence, the new term UFT transform is utilized to refer to the process. As already stated, in embodiments of the present invention can be viewed as a matched filter or correlator operation, which in embodiments is normally applied recursively to the carrier signal at a sub-harmonic rate. A system equation may be written to describe this operation, assuming a rectangular sample aperture and integrators as operators, as shown in FIG. **182** and EQ. (88). The process integrates across an acquisition aperture then stores that value, or a significant portion thereof, to be accumulated with the next aperture. Hence, energy from the input is acquired during T_A and held for T_S−T_A until the next acquisition.

$$D_n\Delta\sum_{n=1}^{k}\int_{nT_S}^{nT_S+T_A}(u(t-nT_s)-u(t-(nT_S+T_A)))\cdot A_n \sin(\omega t+\phi_{(n-l)})dt - \alpha\sum_{n=1}^{k}\int_{(n+l)T_S}^{(n+l)T_S+T_A}(u(t-(n-l)T_S)- u(t-(n-(1-l))T_S+T_A))\cdot A_{(n-l)}S_i(\omega t+\phi_{(n-l)})dt \quad \text{EQ. (88)}$$

where:

T_A is the aperture duration;

T_s is the sub-harmonic sample period;

k is the total number of collected apertures;

l is the sample memory depth;

∀ is the UFT leakage coefficient;

A_n is the amplitude weighting on the nth aperture due to modulation, noise, etc.; and

ν_n is the phase domain shift of nth aperture due to modulation, noise, carrier offset, etc.

D_n represents the UFT transform applicable to embodiments of the invention. The first term defines integration over a rectangular segment of the carrier signal of T_A time duration. k pulses are summed to form a memory of the recursively applied kernel. The second term in the equation provides for the fact that practical implementations possess finite memory. Hence, embodiments of the present invention are permitted to leak after a fashion by selecting α and l. This phenomena is reflected in the time variant differential equation, EQ. (31), derived in sub-section 5. In embodiments, for a perfect zero order data hold function, α=0.

8.2 the Kernel for Embodiments of the Invention

The UFT kernel applicable to embodiments of the invention is given by EQ. (89):

$$D_1=\int_0^{T_A}(u(t)-u(t-T_A))\cdot A\sin(\omega t+\phi)dt \quad \text{EQ. (89)}$$

EQ. 89 accounts for the integration over a single aperture of the carrier signal with arbitrary phase, ϕ, and amplitude, A. Although A and ϕ are shown as constants in this equation, they actually may vary over many (often hundreds or thousands) of carrier cycles. Actually, ϕ(t) and A(t) may contain the modulated information of interest at baseband. Nevertheless, over the duration of a pulse, they may be considered as constant.

8.3 Waveform Information Extraction

Ever since Nyquist developed general theories concerning waveform sampling and information extraction, researchers and developers have pursued optimum sampling techniques and technologies. In recent years, many radio architectures have embraced these technologies as a means to an end for ever more 'digital like' radios. Sub sampling, IF sampling, syncopated sampling, etc., are all techniques employed for operating on the carrier to extract the information of interest. All of these techniques share a common theory and common technology theme, i.e., Nyquist's theory and ideal impulse samplers. Clearly, Nyquist's theory is truly ideal, from a theoretical perspective, while ideal impulse samplers are pursued but never achieved.

Consider the method of developing an impulse sample using functions with shrinking apertures, as illustrated in FIG. **183**. The method illustrated in FIG. **183** utilizes a pulse shape, for example a normalized Gaussian, a modified sin c, or some other suitable type, and permits the pulse width to shrink as the peak amplitude grows. As the pulse width shrinks, the area of the pulse becomes unity. These pulse generation methods are formulated using distribution mathematics techniques. Typically, such formulations require the assumption that causality is violated as is illustrated by the precursors in FIG. **183**. Hence, such pulses are not practical because they are non-causal. In addition, since impulse samplers are implemented to store the sample value at an instantaneous waveform point, they typically utilize a sample and hold approach, which typically implies the charging of a capacitor. As would be known to persons skilled in the relevant arts given the discussion herein, parasitics can present significant charging concerns for such pulses because of the relationships represented by EQ. (90) and EQ. (91).

$$\frac{dq}{dt} = C\frac{dv}{dt}(\text{Charge Differential}) \quad \text{EQ. (90)}$$

$$u = \int_0^q \frac{q_x}{c} - dq_x = \frac{q^2}{2c} = \frac{Cv^2}{2}(\text{Energy}) \quad \text{EQ. (91)}$$

As would be apparent to persons skilled in the relevant arts given the discussion herein, an arbitrary capacitance, c, cannot be charged in an infinitesimally short time period without an infinite amount of energy. Even approximations to an ideal impulse therefore can place unrealistic demands on analog sample acquisition interface circuits in terms of parasitic capacitance vs. pulse width, amplitude, power source, etc. Therefore, a trade-off is typically made concerning some portion of the mix.

The job of a sample and hold circuit is to approximate an ideal impulse sampler followed by a memory. There are limitations in practice, however. A hold capacitor of significant value must be selected in order to store the sample without droop between samples. This requires a healthy charging current and a buffer, which isolates the capacitor in between samples, not to mention a capacitor, which is not 'leaky,' and a buffer without input leakage currents. In general, ideal impulse samplers are very difficult to approximate when they must operate on RF waveforms, particularly if IC implementations and low power consumption are required.

The ideal sample extraction process is mathematically represented in EQ. (92) by the sifting function.

$$\int_{-\infty}^{\infty} x(t)\delta(t - T_A/2)dt = x\left(\frac{T_A}{2}\right) \quad \text{EQ. (92)}$$

where:

$\frac{T_A}{2} \triangleq$ Sample Time;

$x(t) \triangleq$ Sampled Function; and $\delta(t) \triangleq$ Impulse Sample Function.

Suppose now that:

$$x(t) = A\sin(t+\phi) \quad \text{EQ. (93)}$$

then:

$$\int_{-\infty}^{\infty} A\sin(t+\phi)\delta(t - T_A/2)dt = A\sin(T_A/2 + \phi) = A\cos(\phi)\int_{-\infty}^{\infty}\sin(t)\delta(t - T_A/2)dt + A\sin(\phi)\int_{-\infty}^{\infty}\cos(t)\delta(t - T_A/2)dt \quad \text{EQ. (94)}$$

$$= A\cos(\phi)\sin(T_A/2) = A\cos(\phi);\ T_A = \pi \quad \text{EQ. (95)}$$

This represents the sample value acquired by an impulse sampler operating on a carrier signal with arbitrary phase shift ϕ. EQ. (95) illustrates that the equivalence of representing the output of the sampler operating on a signal, $\tilde{X}(t)$, without phase shift, ϕ, weighted by cos ϕ, and the original sampled X(t), which does have a phase shift. The additional requirement is that a time aperture of T_A corresponds to π radians.

Next, consider the UFT kernel:

$$D_1\Delta\int_{\infty}^{\infty}(u(t)-u(t-T_A))\sin(t+\phi)dt \quad \text{EQ. (96)}$$

Using trigonometric identities yields:

$$D_1\Delta A\cos(\phi)\int_{-\infty}^{\infty}(u(t)-u(t-T_A))\sin(t)dt \quad \text{EQ. (97)}$$

Now the kernel does not possess a phase term, and it is clear that the aperture straddles the sine half cycle depicted in FIG. **184**. In EQ. (97), cos ϕ is a weighting factor on the result, which originally illustrated the non-ideal alignment of the present invention clock and carrier signal. Trigonometric identities provide a means of realigning the present invention clock and carrier signal while accounting for the output result due to phase skew.

Consider the ideal aperture of embodiments of the invention shown in FIG. **185**. Notice that the ideal aperture is illustrated as possessing two equal ½ aperture components. Hence the UFT kernel for embodiments of the invention can be rewritten as:

$$D_1\Delta A\cos(\phi)\left[\int_{-\infty}^{\infty}(u(t) - u(T_A/2))\sin(t)dt + \int_{-\infty}^{\infty}(u(t - T_A/2) - u(t - T_A))\sin(t)dt\right] \quad \text{EQ. (98)}$$

It should also be apparent to those skilled in the relevant arts given the discussion herein that the first integral is equivalent to the second, so that;

$$D_1 = 2A\cos(\phi)\int_{-\infty}^{\infty}(u(t) - u(t - T_A/2))\sin(t)dt \quad \text{EQ. (99)}$$

As illustrated in FIG. **186**, a property relating unit step functions and delta functions is useful. In FIG. **186**, a step function is created by integrating a delta function. Therefore;

$$D_1 = 2A\cos(\phi)\int_{-\infty}^{\infty}\left[\int_{-\infty}^{t}\delta(t')dt' - \int_{-\infty}^{t}\delta(t' - T_A/2)dt'\right]\sin(t)dt \quad \text{EQ. (100)}$$

Using the principle of integration by parts yields EQ. (101).

$$D_1 = 2A\cos(\phi)\int_{-\infty}^{t}\cos(t')\delta(t')dt' + 2A\cos(\phi)\int_{-\infty}^{t}\cos(t')\delta(t' - T_A/2)dt = 2A\cos\phi\int_{-\infty}^{t}\sin(t')\delta(t - T_A/2)dt' = 2A\cos(\phi),\ \text{for } T_A = \pi \quad \text{EQ. (101)}$$

This is a remarkable result because it reveals the equivalence of the output of embodiments of the present invention with the result presented earlier for the arbitrarily phased ideal impulse sampler, derived by time sifting. That is, in embodiments, the UFT transform calculates the numerical result obtained by an ideal sampler. It accomplishes this by averaging over a specially constructed aperture. Hence, the impulse sampler value expected at $T_A/2$ is implicitly derived by the UFT transform operating over an interval, T_A. This leads to the following very important implications for embodiments of the invention:

The UFT transform is very easy to construct with existing circuitry hardware, and it produces the results of an ideal impulse sampler, indirectly, without requiring an impulse sampler.

Various processor embodiments of the present invention reduce the variance of the expected ideal sample, over that obtained by impulse sampling, due to the averaging process over the aperture.

8.4 Proof Statement for UFT Complex Downconverter Embodiment of the Present Invention

The following analysis utilizes concepts of the convolution property for the sampling waveform and properties of the Fourier transform to analyze the complex clock waveform for the UFT as well as the down conversion correlation process. FIG. **187** illustrates this process.

In addition r(t) is considered filtered, by a bandpass filter. In one exemplary embodiment, sub-optimal correlators approximate the UFT. This analysis illustrates that some performance is regained when the front-end bandpass filter is used, such that the derived correlator kernel resembles the optimal form obtained from matched filter theory. Furthermore, the analysis illustrates that the arbitrary phase shift of a carrier on which the UFT operates, does not alter the optimality of the correlator structure which can always be modeled as a constant times the optimal kernel. This is due to the fact that UFT is by definition matched to a pulse shape resembling the carrier half cycle which permits phase skew to be viewed as carrier offset rather than pulse shape distortion.

Using the pulse techniques described above, describing pulse trains, the clock signal for UFT may be written as equation **18802** of FIG. **188**.

$p_c(t) \triangleq$ A basic pulse shape of the clock (gating waveform), in our case defined to have specific correlation properties matched to the half sine of the carrier waveform.

$T_s \triangleq$ Time between recursively applied gating waveforms.

$T_A \triangleq$ Width of gating waveform

In FIG. **188**, $C_I(t)$ in equation **18804** and $C_Q(t)$ in equation **18806** are considered to be complex clocks shifted in phase by $T_A/2$. The received carrier is related to T_A by $f_c \approx (2\,T_A)^{-1}$

Although the approximation is used, ideal carrier tracking for coherent demodulation will yield an equal sign after lock. However, this is not required to attain the excellent benefit from UFT processing. Other sections herein provide embodiments that develop expressions for C_I and C_Q from Fourier series analysis to illustrate the components of the gating waveforms at the Carrier frequency which are harmonically related to T_s.

By the methods described above, the Fourier transform of the clock is found from:

$$C_I(f) = \Im\left\{\sum_{m=-\infty}^{\infty} \delta(t - mT_s)\right\} P_c(f) \quad \text{EQ. (102)}$$

$$C_I(f) = \sum_{n=-\infty}^{\infty} \frac{T_A}{T_s} \frac{\sin(n\pi f_s T_A)}{n\pi f_s T_A} \cdot \delta(f - nf_s) \quad \text{EQ. (103)}$$

C_Q possesses the same magnitude response of course but is delayed or shifted in phase and therefore may be written as:

$$C_Q(f) = C_I(f) e^{-jn\pi f T_A} \quad \text{EQ. (104)}$$

When T_A corresponds to a half sine width then the above phase shift related to a

$$\frac{\pi}{2}$$

radians phase skew for C_Q relative to C_I.

In one exemplary embodiment, consider then the complex UFT processor operating on a shifted carrier for a single recursion only,

$$S_0(t) = \int_0^{T_A} r(t) C_I(t) dt + \int_{T_A/2}^{3T_A/2} r(t) C_Q(t) dt \quad \text{EQ. (105.1)}$$

$$S_0(t) = \int_0^{T_A} (A\sin(\omega t + \phi) + n(t)) C_I(t) dt + \int_{T_A/2}^{3T_A/2} (A\sin(\omega t + \phi) + n(t)) C_Q(t) dt \quad \text{EQ. (105.2)}$$

This analysis assumes that r(t), the input carrier plus noise, is band limited by a filter. In this case therefore the delta function comb evident in the transform of C_I and C_Q are ignored except for the components at the carrier. Embodiments in other sections break C_I and C_Q into a Fourier series. In this series, only the harmonic of interest would be retained when the input waveform r(t) is bandpass limited because all other cross correlations tend to zero. Hence,

$$S_0(t) \simeq K \int_0^{T_A} (A\sin(\omega t + \phi) + n(t))\sin(\omega t) dt + K \int_{T_A/2}^{3T_A/2} (A\sin(\omega t + \phi) + n(t))\cos(\omega t) dt \quad \text{EQ. (105.3)}$$

$$S_0(t) \simeq K \int_0^{T_A} (A\sin(\omega t)\cos\phi + \cos(\omega t)\sin\phi + n(t))\sin(\omega t) dt + K \int_{T_A/2}^{3T_A/2} (A\sin(\omega t)\cos\phi + \cos(\omega t)\sin\phi + n(t))\cos(\omega t) dt \quad \text{EQ. (105.4)}$$

The clock waveforms have been replaced by the single sine and cosine components from the Fourier transform and Fourier series, which produce the desired result due to the fact that a front-end filter filters all other spectral components. This produces a myriad of cross correlations for the complex UFT processor. K is included as a scaling factor evident in the transform.

$$S_0(t) = KA\cos\phi \overbrace{\int_0^{T_A} (\sin(\omega t))^2 dt}^{optimal\ correlator} + K \int_0^{T_A} n(t)\sin\omega t dt + KA\sin\phi \overbrace{\int_{T_A/2}^{3T_A/2} (\cos(\omega t))^2 dt}^{optimal\ correlator} + K \int_{T_A/2}^{3T_A/2} n(t)\cos\omega t dt \quad \text{EQ. (106.1)}$$

$$\therefore S_0(t) = \left(\frac{KA\pi}{2}\cos\phi + \tilde{n}_I\right) I \text{ component} \quad \text{EQ. (106.2)}$$

$$+\left(\frac{KA\pi}{2}\sin\phi + \tilde{n}_Q\right) Q \text{ component} \quad \text{EQ. (106.2.1)}$$

$$\text{where } K = \left(\frac{T_A}{T_s} \frac{\sin\left(n\pi \frac{T_A}{T_s}\right)}{\left(n\pi \frac{T_A}{T_s}\right)}\right) \quad \text{EQ. (106.3)}$$

A and ϕ are the original components of the complex modulation envelope (amplitude and phase) for the carrier and are assumed to vary imperceptibly over the duration for T_A. What is very interesting to note is that the above equations are exactly the optimum form for the complex correlator whose pulse shape is a half sine with components weighted by cosine for I, and sine for Q. Furthermore, when an input bandpass filter is considered as a part of the system then the approximate kernels used throughout various analyses based on the gating function become replaced by the ideal matched filter analogy. Hence, the approximation in CMOS using rectangular gating functions, which are known to cause only a 0.91 dB hit in performance if C is selected correctly, probably can be considered pessimistic if the receiver front end is filtered.

8.5 Acquisition and Hold Processor Embodiment

As illustrated in FIG. **189**, embodiments of the present invention can be approximately modeled as a particular case of a sampling system. In the example model in FIG. **189**, both an acquisition phase and a hold phase for each T_s cycle is shown, where:

r(t)≜ Input Waveform RF Modulated Carrier Plus Noise

C_A (t)≜ Present Invention Aperture Waveform Pulse Train

δ_H(t)≜ Holding Phase Impulse Train

h_A(t)≜ Integrator Impulse Response of the present Invention

h_H (t)≜ ≠0 DH Portion of Present Invention Impulse Response

The embodiment in FIG. **189** consists of a gating device followed by a finite time integrator, then an ideal sampler, and finally a holding filter, which accumulates and stores the energy from the acquisition phase. This is called an acquisition and hold processor. The acquisition phase of the operation is described by:

$$X(t) = C_T(t)r(t) * h_A(t) \quad \text{EQ. (107)}$$

$$X(t) = \sum_{k=-\infty}^{\infty} (u(t-kT_s) - u(t-(kT_s+T_A))A_k(\sin(\omega_c t + \phi_k)) * h_A(t)) \quad \text{EQ. (108)}$$

The ultimate output includes the hold phase of the operation and is written as:

$$S_0(t) = (X(t)\delta_H(t)) * h_H(t) \quad \text{EQ. (109)}$$

$$S_0(t) = \sum_{k=-\infty}^{\infty} (X(t)\delta_H(t-k(T_s))) * u(t-(kT_s+T_A)) - u(t-(k+1)T_s) \quad \text{EQ. (110)}$$

$$T = T_s - T_A \quad \text{EQ. (111)}$$

This embodiment considers the aperture operation as implemented with an ideal integrator and the hold operation as implemented with the ideal integrator. As shown elsewhere herein, this can be approximated by energy storage in a capacitor under certain circumstances.

The acquisition portion of the operation possesses a Fourier transform given by:

$$X_0(\omega) = \Im_0\{X_0(t)\} = \sum_{k=-\infty}^{\infty} \frac{1}{2\pi T_s} \overbrace{\delta(\omega - k\omega_s)}^{Harmonic\ Sifter} \underbrace{\overbrace{\left(\frac{T_A}{2} e^{j\omega T_A/2} \frac{\sin(\omega T_A/2)}{\omega T_A/2}\right)}^{Finite\ Time\ Integrator} S_i(\omega)_c}_{Original\ Information\ Spectrum\ Chopped\ by\ C(t)}$$

$S_I(\omega)=\Im\{r(t)\}$ (Modulated Information Spectrum)

$S_0(\omega)$ can be found in a similar manner.

$$\Im\{S_0(t)\} = \sum_{k=-\infty}^{\infty} \frac{1}{2\pi T_s} \overbrace{\delta(\omega - k\omega_s)}^{Harmonic\ Sifter} \overbrace{\left(\frac{T}{2} e^{j\omega T_A/2} \frac{\sin(\omega T_A/2)}{\omega T_A/2}\right)}^{Z0DH\ Response} X(\omega)$$

$$T = T_s - T_A$$

The example of FIG. **190** illustrates the various components of the above transform superimposed on the same graph, for a down conversion case, where T_A is chosen as a single aperture realization and the 3rd sub harmonic is used for down conversion. The analysis does not consider the affect of noise, although, it is straightforward to accomplish, particularly in the case of AWGN. The lowpass spectrum possesses nulls at nf_{sA}, n=0, ±1, ±2, . . . , where $f_s=(T_s-T_A)^{-1}$. This Z0DH spectral response is also present at each harmonic of f_s, although it is not indicated by the graphic.

The acquisition portion of the Fourier transform yields the following an important insight:

$$X_0(\omega) = \frac{KT_A}{T_s} \sum_{k=-\infty}^{\infty} \delta(\omega - k\omega_s)\left(e^{j\omega T_A/2} \frac{\sin(\omega T_A/2)}{\omega T_A/2}\right) \cdot S_i(\omega)_c \quad \text{EQ. (112)}$$

$$S_i(\omega)_c = A_k T_A e^{j\omega T_A/2} \frac{\sin(\omega(T_A/2))}{\omega(T_A/2)} (\delta(\omega-\omega_c) + \delta(\omega+\omega_c)) \quad \text{EQ. (113)}$$

As should be apparent to persons skilled in the relevant arts given the discussion herein, down conversion occurs whenever $k\omega_s=\omega_c$. It is useful to find T_A, which maximizes the component of the spectrum at ω_c, which is subject to down conversion and is the desired signal. This is accomplished simply by examining the kernel.

$$\tilde{X} \triangleq \left|\frac{T_A}{T_s} \frac{\sin(\omega(T_A/2))}{\omega(T_A/2)}\right| \quad \text{EQ. (114)}$$

For $\omega=\omega_c$,

$$\tilde{X} = \left|\frac{T_A}{n \cdot T_c} \frac{\sin\left(\pi \frac{T_A}{T_c}\right)}{\left(\pi \frac{T_A}{T_c}\right)}\right|, nT_c = T_s$$

for Harmonic Conversion

$$\therefore \tilde{X} = \frac{1}{n\pi}\sin\left(\pi\frac{T_A}{T_c}\right) \quad \text{EQ. (115)}$$

The kernel is maximized for values of

$$\frac{T_A}{T_c} = \frac{1}{2}, \frac{3}{2}, \frac{5}{2}, \ldots$$

Advocates of impulse samplers might be quick to point out that letting $T_A \to 0$ maximizes the sin c function. This is true, but the sin c function is multiplied by T_A in the acquisition phase. Hence, a delta function that does not have infinite amplitude will not acquire any energy during the acquisition phase of the sampler process. It must possess infinite amplitude to cancel the effect of $T_A \to 0$ so that the multiplier of the sine function possesses unity weighting. Clearly, this is not possible for practical circuits.

On the other hand, embodiments of the present invention with

$$\frac{T_A}{T_c} = \frac{1}{2}, \frac{3}{2}, \frac{5}{2}, \ldots \text{ etc.,}$$

does pass significant calculable energy during the acquisition phase. This energy is directly used to drive the energy storage element of $\not\equiv$ 0DH filter or other interpolation filter, resulting in practical RF impedance circuits. The cases for

$$\frac{T_A}{T_c}$$

other than ½ can be represented by multiple correlators, for example, operating on multiple half sine basis.

Moreover, it has been shown that the specific gating aperture, C(t), does not destroy the information. Quite the contrary, the aperture design for embodiments of the present invention produces the result of the impulse sampler, scaled by a gain constant, and possessing less variance. Hence, the delta sifting criteria, above trigonometric optimization, and correlator principles all point to an aperture of

$$\frac{T_A}{T_c} = \frac{1}{2}$$

nominal.

If other impulse responses are added around the present invention (i.e., energy storage networks, matching networks, etc.) or if the present invention is implemented by simple circuits (such as the RC processor) then in embodiments the optimal aperture can be adjusted slightly to reflect the peaking of these other embodiments. It is also of interest to note that the Fourier analysis above predicts greater DC offsets for increasing ratios of

$$\frac{T_A}{T_c}.$$

Therefore, for various embodiments,

$$\frac{T_A}{T_c} = \frac{1}{2}$$

is probably the best design parameter for a low DC offset system.

9. Comparison of the UFT Transform to the Fourier Sine and Cosine Transforms

The sine and cosine transforms are defined as follows:

$$F_c(\omega)\Delta\int_0^\infty f(t)\sin\omega t dt \omega \geq 0 \text{ (sine transform)} \quad \text{EQ. (116)}$$

$$F_s(\omega)\Delta\int_0^\infty f(t)\cos\omega t dt \omega \geq 0 \text{ (cosine transform)} \quad \text{EQ. (117)}$$

Notice that when f(t) is defined by EQ. (118):

$$f(t)=u(t)-u(u-T_A) \quad \text{EQ. (118)}$$

the UFT transform kernel appears as a sine or cosine transform depending on ϕ. Hence, many of the Fourier sine and cosine transform properties may be used in conjunction with embodiments of the present invention to solve signal processing problems.

The following sine and cosine transform properties predict the following results of embodiments of the invention:

Sine and Cosine Transform Property	Prediction of Embodiments of the Invention
Frequency Shift Property	Modulation and Demodulation Preserving Information
Time Shift Property	Aperture Values Equivalent to Constant Time Delta Time Sift.
Frequency Scale Property	Frequency Division and Multiplication

Of course many other properties are applicable as well. The subtle point presented here is that for embodiments the UFT transform does in fact implement the transform, and therefore inherently possesses these properties.

Consider the following specific example:
let $f(t)=u(t)-u(t-T_A)$ and let $\omega=2\pi f=\pi f_A=1$.

$$\Im_c[f(t)] = \int_0^{T_A}\cos(\omega t)dt = \frac{1}{\omega}\sin\omega T_A = 0 \quad \text{EQ. (119)}$$

$$\Im_s[f(t)] = \frac{1}{\omega} - \frac{1}{\omega}\cos\omega T_A = 2 \quad \text{EQ. (120)}$$

This is precisely the result for D_{1c} and D_{1s}. Time shifting yields: $\Im_s[f_0(t+T_S)+f_0(t-T_s)]=2\ F_s(\omega)\cos(T_s\omega)$ (Time Shift Property) Let the time shift to be denoted by T_s.

$$f(t) = u(t) - u(t - T_A) \quad \text{EQ. (121)}$$

$$f_0(t)\Delta\frac{1}{2}(u(t+T_s)-u(t)) + \frac{1}{2}(u(t)-u(t-T_s)) \quad \text{EQ. (122)}$$

Notice that $f_0(t)$ has been formed due to the single sided nature of the sine and cosine transforms. Nevertheless, the

amplitude is adjusted by ½ to accommodate the fact that the energy must be normalized to reflect the odd function extension. Then finally:

$$\Im_s[f_0(t+T_s)+f_0(t-T_s)]=\frac{2}{2}F_s(\omega)\cos(T_s\omega)=2\cos\left(\frac{\pi T_s}{T_A}\right) \quad \text{EQ. (123)}$$

which is the same solution for phase offset obtained earlier by other means.

The implications of this transform may be far reaching when it is considered that the discrete Fourier sine and cosine transforms are originally based on the continuous transforms as follows:

$$\Im_c\{f(t)\}=\int_0^{\infty} f(t)\cos\omega t\,dt \quad \text{EQ. (124)}$$

$$\mathcal{J}_{DC}\{f(t)\}\triangleq\mathcal{J}\{f(n)\}=\sqrt{\frac{2}{N}}\sum_{m=0}^{N}\alpha_m\alpha_n\cos\left(\frac{mn\pi}{N}\right)f(n) \quad \text{EQ. (125)}$$

That is, the original kernel cos (ωt) and function f(t) are sampled such that:

f(n)≙ Sampled Version of f(t)

$\omega_m=2\pi_m\Delta f$

$t_n=n\Delta t$

Δf≙ Frequency Sample Interval

Δt≙ Time Sample Interval

Hence the new discrete cosine transform kernel is:

$$k_c(m,n)=\cos(2\pi mn\Delta f\Delta t)=\cos(\pi mn/n)\Delta f\Delta t=\tfrac{1}{2}N \quad \text{EQ. (126)}$$

N is the total number of accumulated samples for m, n, or the total record length.

In recent years, the discrete cosine transform (DCT) and discrete sine transform (DST) have gained much recognition due to their efficiency for waveform coding compression, spectrum analysis, etc. In fact, it can be shown that these transforms can approach the efficiency of Karhunen-Loeve transforms (KLT), with minimal computational complexity. The implication is that the sifted values from D_1 could be used as DCT sample values f(n). Then the DCT and DST properties will apply along with their processing architectures. In this manner, communications signals, like OFDM, could be demodulated in a computationally efficient manner. Many other signal processing applications are possible using the present invention, and the possibilities are rich and varied.

10. Conversion, Fourier Transform, and Sampling Clock Considerations

The previous sub-sections described how embodiments of the present invention involve gating functions of controlled duration over which integration can occur. This section now addresses some consideration for the controlling waveform of the gating functions.

For sub harmonic sampling:

$f_s=f_c/M$

f_s≙ Sample Rate

f_c≙ Carrier Frequency

M≙ As an integer such that 0<M<∞

The case M=1 represents a classic down conversion scenario since $f_s=f_c$. In general though, M will vary from 3 to 10 for most practical applications. Thus the matched filtering operation of embodiments of the present invention is applied successively at a rate, f_s, using the approach of embodiments of the present invention. Each matched filter/correlator operation represents a new sample of the bandpass waveform.

The subsequent equations illustrate the sampling concept, with an analysis base on approximations that ignore some circuit phenomena. A more rigorous analysis requires explicit transformation of the circuit impulse response. This problem can be solved by convolving in the time domain as well, as will be apparent to persons skilled in the relevant arts given the discussion herein. The results will be the same. The analysis presented herein is an abbreviated version of one provided above. As in the subsection 8, the acquisition portion of the present invention response is analyzed separately from the hold portion of the response to provide some insight into each. The following sub-section uses a shorthand notation for convenience.

$$X_0(t)=S_i(t)\sum_{k=-\infty}^{\infty}\tilde{C}(t-kT_s) \quad \text{EQ. (127)}$$

(approximate output of acquisition)

$X_0(t)$≙ Output of Sample

$S_i[t]$≙ Waveform being Sampled

k≙ Sampling Index

T_s≙ Sampling Interval=f_s^{-1}

$\tilde{C}(t-kT_s)$≙ Quasi-Matched Filter/Correlator Sampling Aperture, which includes averaging over the Aperture.

EQ. (127) can be rewritten a:

$$X_0(t)\cong\sum_{k=-\infty}^{\infty}S_i(kT_s)*\tilde{C}(t-kT_s) \quad \text{EQ. (128)}$$

If $\tilde{C}(t)$ possesses a very small aperture with respect to the inverse information bandwidth, $T_A<<BW_i^{-1}$, then the sampling aperture will weight the frequency domain harmonics of f_s. The Fourier transform and the modulation property may be applied to EQ. (128) to obtain EQ. (129) (note this problem was solved above by convolving in the time domain).

$$X_0(\omega)=\left(S_i(\omega)_c\tilde{C}(\omega)\right) \quad \text{EQ. (129)}$$

$$\therefore X_0(\omega)\cong \quad \text{EQ. (130)}$$

$$\frac{K}{T_s}\sum_{k=-\infty}^{\infty}\delta_i(\omega-k\omega_s)\left[\frac{T_A\cdot e^{j\omega T_A/2}}{2}\frac{\sin(\omega T_A/2)}{\omega T_A/2}\right]\cdot S_i(\omega)_c$$

K≙ Arbitrary Gain Constant, which includes a ½π factor ω≙ 2πf

Essentially, on the macroscopic frequency scale, there is a harmonic sample comb generated, which possesses components at every Nf_s for N=1, 2, 3 . . . ∞, with nulls at every $Z\cdot f_A$, where f_A is defined as T_A^{-1}. FIG. **191** illustrates this result.

The thickness of each spike in FIG. **191** illustrates the surrounding band produced from $S_i(\omega)$. $S_i(\omega)$ is a complex transform including magnitude and phase, which can be assigned a vector representation in the time domain (i.e., I and Q components). The natural action of embodiments of the present invention, in the hold portion of the response, acts as a lowpass filter in the down conversion case, thereby reducing the levels of all the harmonic sidebands. Likewise, the up converter utilizes a bandpass matched filter to extract the desired carrier and reject unwanted images.

Notice that each harmonic including baseband possesses a replica of $S_i(\omega)$ which is in fact the original desired signal. $\{S_i(\omega)$ is the original information spectrum and is shown to survive the acquisition response of the present invention (i.e., independent integration over each aperture)). Lathi and many others pointed out that $\tilde{C}(\omega)$ could be virtually any harmonic function and that conversion to baseband or passband will result from such operations on $S_i(t)$.

Each discrete harmonic spectrum provides a potential down conversion source to baseband (at DC). Of course, theoretically, there cannot be a conversion of $Z \cdot f_a$ because of the spectral nulls. FIG. **191** illustrates the important relationships between f_s, f_a, and the relative harmonic conversion efficiency related to the sin c^2 function harmonic comb weighting, resulting from a simple rectangular sampling aperture.

It should also be noted that in all practical cases, $f_s >> 2 \cdot BW_i$, so that Nyquist criteria are more than satisfied. The lowpass response of embodiments of the present invention can be ideally modeled as a zero order data hold filter, with a finite time integrator impulse response duration of $T=T_s-T_A$. The ultimate output Fourier transform is given by EQ. (131).

$$S_0(\omega) = \sum_{k=-\infty}^{\infty} \underbrace{\frac{K}{T_s}\delta(\omega - k\omega_s)}_{\text{Harmonic Sifter}} \underbrace{\left(\frac{T}{2} e^{j\omega T/2} \frac{\sin\omega T/2}{\omega T/2}\right)}_{\text{Z0DH Reponse}} \cdot \underbrace{X(\omega)}_{\text{Acquisition Response}} \quad \text{EQ. (131)}$$

The Z0DH is a type of lowpass filter or sample interpolator which provides a memory in between acquisitions. Each acquisition is accomplished by a correlation over T_A, and the result becomes an accumulated initial condition for the next acquisition.

10.1 Phase Noise Multiplication

Typically, processor embodiments of the present invention sample at a sub-harmonic rate. Hence the carrier frequency and associated bandpass signal are down converted by a $M \cdot f_s$ harmonic. The harmonic generation operation can be represented with a complex phasor.

$$S_{amp}(t) \underline{\Delta} (e^{-j\omega_s t + \phi(t)})^m \quad \text{EQ. (132)}$$

S_{amp} (t) can be rewritten as:

$$S_{amp}(t) = e^{-jM\omega_s t} \cdot e^{M\phi(t)} \quad \text{EQ. (133)}$$

$\phi(t) \underline{\Delta}$ Phase Noise on the Conversion Clock

As EQ. (133) indicates, not only is the frequency content of the phasor multiplied by M but the phase noise is also multiplied by M. This results in an M-tuple convolution of the phase noise spectrum around the harmonic. The total phase noise power increase is approximated by EQ. (134).

$$\phi = \underline{\Delta} 20 \log_{10} M \text{ (Phase Noise)} \quad \text{EQ. (134)}$$

That is, whatever the phase jitter component, $\theta(t)$, existing on the original sample clock at Mf_s, it possesses a phase noise floor degraded according to EQ. (134).

10.2 AM-PM Conversion and Phase Noise

This section describes what the conversion constant and the output noise is for AM to PM conversion according to embodiments of the present invention, considering the noise frequency of the threshold operation. As illustrated in FIG. **192**, suppose that the output of a sine signal source must be filtered and compared, in order to obtain a suitable clock signal. For cases where the equivalent input noise power of the threshold device can be considered to be much less than the input power source sine wave, a single zero crossing per cycle of sine wave can be assumed to occur. For such low noise cases, the threshold operation may be viewed as an AM to PM conversion device.

The slope at the zero crossings of a pure sine wave, $s(t)=A \sin \omega t$, can be calculated. Differentiating s(t) with respect to t yields $s(t)'=\omega A \cos \omega t$. For $\omega A \neq 0$, the zero crossings occur at $\omega t=\pi/2, 3\pi/2, 5\pi/2 \ldots$.

$$\therefore t = 1/4f, 3/4f, 5/4f \ldots \{\text{for } s(t)\} \quad \text{EQ. (135)}$$

These zero crossings represent the points of minimum slope or crests of the original s(t). The maximum slope is found at the zero crossings of. s(t) at $\omega t=0, \pi, 2\pi, \ldots$ etc. Plugging those arguments into s(t)' give slopes of: Slope=ωA, $-\omega A, \omega A, -\omega A \ldots$ etc. The time at which these zero crossings occur is given by: $\omega t=\pi, 2\pi, 3\pi \ldots$ t=1/2f,1/f,3/2f, . . . {for s(t)}.

It stands to reason that for the low noise power assumption, which implies one zero crossing per carrier cycle, the slope at the zero crossing will be modified randomly if a Gaussian process (n(t) is summed to the signal. Of course, if the change in slope of the signal is detectable, the delta time of the zero crossing is detectable, and hence phase noise is produced. The addition of noise to the signal has the effect of moving the signal up and down on the amplitude axis while maintaining a zero mean. This can be written more formally as:

$$\left|\frac{\partial s(t)}{\partial t}\right| = \omega A = \text{for } \omega t = n\pi/2 \quad \text{EQ. (136)}$$

If A is replaced by $A-\Delta a$, where Δa represents the noise deviation, then one will not always observe a zero crossing at the point of maximum slope ωA. Sometimes the zero crossing will occur at $\omega(A-\Delta a)$. This leads to the low noise approximation:

$$\omega(A - \Delta a) = \omega A \cos[\omega(t \pm \varepsilon)] \quad \text{EQ. (137)}$$

$$\arccos\left(\frac{\frac{A-\Delta a}{A}}{\omega}\right) = t \pm \varepsilon \quad \text{EQ. (138)}$$

The low noise assumption implies that the low noise power prohibits the arcos function from transforming the Gaussian pdf of the noise. That is, $\pm\Delta a$ occurs over minute ranges for the argument of the arcos and hence the relationship is essentially linear. Secondly, since A is a peak deviation in the sine wave Δa will be considered as a peak deviation of the additive noise process. This is traditionally accepted as being 4σ where σ is the standard deviation of the process and σ^2 is the variance. Therefore we write K arcos $(1-4\sigma/A)=t \pm \in$, where $\in$ represents a peak time deviation in the zero crossing excursion, $K=1/\omega$, and t is the mean zero crossing time given previously as t=1/sf, 1/f, 3/2f, ... If only the deviation contribution to the above equation is retained, the equation reduces to:

$$K \cos^{-1}\left(\frac{4\sigma}{A}\right) = \varepsilon = \Delta t \quad \text{EQ. (139)}$$

Since for $4\sigma/A<<0.01$, the above function is quasi-linear, one can write the final approximation as:

$$K\frac{4\sigma}{A}=\Delta t=\frac{4\sigma}{\omega A}\text{ seconds (peak)} \quad \text{EQ. (140)}$$

An appropriate conversion to degrees becomes,

$$360^\circ\ f_c=\frac{4\sigma_x}{\frac{4\sigma}{\omega_c A}} \quad \text{EQ. (141)}$$

f_c=frequency of carrier
σ_x=phase noise in degrees rms
σ=standard deviation of equivalent input comparator noise

$$\therefore \sigma_x=\frac{(360)\sigma}{2\pi A}\text{ degrees rms} \quad \text{EQ. (142)}$$

$$\frac{\sigma_x}{57.3}=\text{radians rms}=\sigma_\phi$$

$\sigma_{\Phi_x}^2$=variance or power in dBc

Now a typical threshold operator may have a noise figure, NF, of approximately 15 dB. Hence, one can calculate σ_x (assume $\sigma_\Phi^2=2.4\times10^{-8}$ rad^2 source phase noise):

$$-174\text{ dBm/Hz}+15+10\log_{10}100\times10^6=-79\text{ dBm} \quad \text{EQ. (143)}$$

where 100 MHz of input bandwidth is assumed.

$$\text{anti log}-7.9=1.26\times10^{-8}\text{ milliwatts}=1.26\times10^{-11}\text{ watts} \quad \text{EQ. (144)}$$

$$\therefore \sigma=\sqrt{1.26\times10^{-11}}\approx3.55\times10^{-6} \quad \text{EQ. (145)}$$

$$\sigma_x=\frac{(360)3.55\times10^{-6}}{2\pi(.6)}\simeq3.39\times10^{-4}\text{ degrees rms}$$

$\sigma_{\Phi_x}\approx5.92\times10^{-6}$ rad rms
$\sigma_{\Phi_2}^2=\sigma_\theta^2+\sigma_{\Phi_x}^2\cong2.4\times10^{-8}+3.5\times10^{-11}\approx2.4\times10^{-8}$ rad^2
σ_θ=phase noise of source before threshold device

Therefore, the threshold device has little to no impact on the total phase noise modulation on this particular source because the original source phase noise dominates. A more general result can be obtained for arbitrarily shaped waveforms (other than simple sine waves) by using a Fourier series expansion and weighting each component of the series according to the previously described approximation. For simple waveforms like a triangle pulse, the slope is simply the amplitude divided by the time period so that in the approximation:

$$\Delta t\approx\frac{k4\sigma T_r}{A_T} \quad \text{EQ. (146)}$$

k; an arbitrary scaling constant
T_r; time period for the ramping edge of the triangle

Hence, the ratio of $(\sigma T_r/A_r)$ is important and should be minimized. As an example, suppose that the triangle pulse rise time is 500 nsec. Furthermore, suppose that the amplitude, A_T, is 35 milli volts. Then, with a 15 dB NF, the Δt becomes:

$$\Delta t=\frac{k\cdot4\cdot(3.55\times10^{-6})V500\text{ nsec}}{.035}\simeq203\text{ ps}$$

$\sigma\cong203/4\approx50.7$ ps (1Ω)

This is all normalized to a 1Ω system. If a 50Ω system were assumed then: $\sigma\cong358.5$ ps (50Ω)

In addition, it is straight forward to extend these results to the case of DC offset added to the input of the threshold device along with the sine wave.

Essentially the zero crossing slope is modified due to the virtual phase shift of the input sine function at the threshold. DC offset will increase the phase noise component on the present invention clock, and it could cause significant degradation for certain link budgets and modulation types.

11. Pulse Accumulation and System Time Constant

11.1 Pulse Accumulation

Examples and derivations presented in previous sub-sections illustrate that in embodiments single aperture acquisitions recover energies proportional to:

$$E_f=\int_0^{T_A}S_i^2(t)dt=\frac{A_n^2T_A}{2}\text{ (optimum aperture)} \quad \text{EQ. (147)}$$

$A_n\underline{\Delta}$ as the carrier envelope weighting of the nth sample.

In addition, sub-section 8 above, describes a complete UFT transform over many pulses applicable to embodiments of the invention. The following description therefore is an abbreviated description used to illustrate a long-term time constant consideration for the system.

As described elsewhere herein, the sample rate is much greater than the information bandwidth of interest for most if not all practical applications.

$$f_s>>BW_i \quad \text{EQ. (148)}$$

Hence, many samples may be accumulated as indicated in previous sub-sections, provided that the following general rule applies:

$$\frac{f_s}{f}>BW_i \quad \text{EQ. (149)}$$

where l represents the total number of accumulated samples. EQ. (149) requires careful consideration of the desired information at baseband, which must be extracted. For instance, if the baseband waveform consists of sharp features such as square waves then several harmonics would necessarily be required to reconstruct the square wave which could require BW_i of up to seven times the square wave rate. In many applications however the base band waveform has been optimally prefiltered or bandwidth limited apriori (in a transmitter), thus permitting significant accumulation. In such circumstances, f_s/l will approach BW_i.

This operation is well known in signal processing and historically has been used to mimic an average. In fact it is a means of averaging scaled by a gain constant. The following equation relates to EQ. (127).

$$\sum_{n=1}^{\ell} E_\ell = \sum_{\ell=1}^{x} \frac{A_n^2 T_A}{2} \cong \frac{\ell A^2 T_A}{2} \quad \text{EQ. (150)}$$

Notice that the nth index has been removed from the sample weighting. In fact, the bandwidth criteria defined in EQ. (149) permits the approximation because the information is contained by the pulse amplitude. A more accurate description is given by the complete UFT transform, which does permit variation in A. A cannot significantly vary from pulse to pulse over an l pulse interval of accumulation, however. If A does vary significantly, l is not properly selected. A must be permitted to vary naturally, however, according to the information envelope at a rate proportional to BW_i. This means that l cannot be permitted to be too great because information would be lost due to filtering. This shorthand approximation illustrates that there is a long term system time constant that should be considered in addition to the short-term aperture integration interval.

In embodiments, usually the long term time constant is controlled by the integration capacitor value, the present invention source impedance, the present invention output impedance, and the load. The detailed models presented elsewhere herein consider all these affects. The analysis in this section does not include a leakage term that was presented in previous sub-sections.

EQs. (149) and (150) can be considered a specification for slew rate. For instance, suppose that the bandwidth requirement can be specified in terms of a slew rate as follows:

$$SR = \times \frac{\text{volts}}{\mu\text{sec}} \quad \text{EQ. (151)}$$

The number of samples per μsec is given by:

$l_s = f_s \times 1 \times 10^{-6}$ (f_s is derived from the present invention clock rate)

If each sample produces a voltage proportional to $A^2\ T_A/2$ then the total voltage accumulated per microsecond is:

$$V_{\mu sec} \cong \ell_s \frac{A^2 T_A}{2} \quad \text{EQ. (152)}$$

The previous sub-sections illustrates how the present invention output can accumulate voltage (proportional to energy) to acquire the information modulated onto a carrier. For down conversion, this whole process is akin to lowpass filtering, which is consistent with embodiments of the present invention that utilize a capacitor as a storage device or means for integration.

11.2 Pulse Accumulation by Correlation

The previous sub-sections introduced the idea that in embodiments information bandwidth is much less than the bandwidth associated with the present invention's impulse response for practical applications. The concept of single aperture energy accumulation was used above to describe the central ideas of the present invention. As shown in FIG. **193**, multiple aperture accumulation permits baseband waveform reconstruction. FIG. **193** illustrates the results from simulation of actual circuits according to embodiments of the present invention implemented with CMOS and passive components.

The staircase output of the example in FIG. **193** follows the complex modulation envelope for the input signal. Sub-section 5 predicts this result via the time variant linear differential equation. FIG. **193** illustrates the staircase accumulation of half sine energy for three apertures based on 3× sampling. As can be seen in FIG. **193**, the leakage between accumulations is very small.

12. Energy Budget Considerations

Consider the following equation for a window correlator aperture:

$$E_{ASO} = \int_0^{TA} A \cdot S_i(t) dt \quad \text{EQ. (153)}$$

In EQ. (153), the rectangular aperture correlation function is weighted by A. For convenience, it is now assumed to be weighted such that:

$$E_{ASO} = \int_0^{TA} kA \cdot S_i(t) dt = 2A \text{ (normalized)} \quad \text{EQ. (154)}$$

Since embodiments of the present invention typically operate at a sub-harmonic rate, not all of the energy is directly available due to the sub-harmonic sampling process. For the case of single aperture acquisition, the energy transferred versus the energy available is given by:

$$\frac{E_0}{E_1} = \frac{E_{ASO}}{2N} = \frac{A}{N} \quad \text{EQ. (155)}$$

NΔ harmonic of operation

The power loss due to harmonic operation is:

$$E_{LN} = 10 \log_{10}(2N) \quad \text{EQ. (156)}$$

There is an additional loss due to the finite aperture, T_A, which induces (sin x/x) like weighting onto the harmonic of interest. This energy loss is proportional to:

$$E_{LSINC} \simeq \left(\frac{\sin(\pi N f_s T_A)}{\pi N f_s T_A} \right) \text{ (up conversion only)} \quad \text{EQ. (157)}$$

N·f_sΔ operating carrier frequency

f_sΔ sampling rate (directly related to the clock rate)

EQ. (157) indicates that the harmonic spectrum attenuates rapidly as N·f_s approaches T_A^{-1}. Of course there is some attenuation even if that scenario is avoided. EQ. (157) also reveals, however, that in embodiments for single aperture operation the conversion loss due to E_{LSINC} will always be near 3.92 dB. This is because:

$$(2 \cdot N f_s = T_A \text{ (}\sim 3.92 \text{ dB condition)} \quad \text{EQ. (158)}$$

Another way of stating the condition is that T_A is always ½ the carrier period.

Consider an ideal implementation of an embodiment of the present invention, without any circuit losses, operating on a 5th harmonic basis. Without any other considerations, the energy loss through the device is at minimum:

$$E_L = E_{LN} + E_{LSINC} = 10 \text{ dB} + 3.92 \cong 14 \text{ dB (for up conversion)} \quad \text{EQ. (159)}$$

Down conversion does not possess the 3.92 dB loss so that the baseline loss for down conversion is that represented by EQ. (156). Parasitics will also affect the losses for practical systems. These parasitics must be examined in detail for the particular technology of interest.

Next suppose that a number of pulses may be accumulated using the multi-aperture strategy and diversity means of an embodiment of the present invention, as described above. In this case, some of the energy loss calculated by EQ. (159) can

be regained. For example, if four apertures are used then the pulse energy accumulation gain is 6 dB. For the previous example, this results in an overall gain of 6 dB-14 dB, or −8 dB (instead of −14 dB). This energy gain is significant and will translate to system level specification improvements in the areas of noise frequency, intercept point, power consumption, size, etc. It should be recognized, however, that a diversity system with active split or separate amplifier chains would use more power and become more costly. In addition, in embodiments, energy storage networks coupled to the circuitry of the present invention may be used to accumulate energy between apertures so that each aperture delivers some significant portion of the stored energy from the network. In this manner, some inefficiencies of the sub harmonic sampling process can be removed by trading impedance matching vs. complexity, etc., as further described below.

12.1 Energy Storage Networks

Embodiments of the present invention have been shown to be a type of correlator, which is applied to the carrier on a sub harmonic basis. It is also been shown herein that certain architectures according to embodiments of the invention benefit significantly from the addition of passive networks, particular when coupled to the front end of a processor according to the present invention used as a receiver. This result can be explained using linear systems theory.

To understand this, it is useful to consider the following. Embodiments of the present invention can be modeled as a linear, time-variant (LTV) device. Therefore, the following concepts apply:

- The LTV circuits can be modeled to have an average impedance; and
- The LTV circuits can be modeled to have an average power transfer or gain.

These are powerful concepts because they permit the application of the maximum bilateral power transfer theorem to embodiments of the present invention. As a result, in embodiments, energy storage devices/circuits which fly wheel between apertures to pump up the inter sample power can be viewed on the many sample basis (long time average) as providing optimum power transfer through matching properties. The between sample model on the time microscopic scale is best viewed on a differential equation basis while the time macroscopic view can utilize simpler analysis techniques such as the maximum power transfer equations for networks, correlator theory, etc. The fact that the differential equations can be written for all time unifies the theory between the short time (between sample) view and long time (many sample accumulation) view. Fortunately, the concepts for information extraction from the output of the present invention are easily formulated without differential equation analysis.

Network theory can be used to explain why certain networks according to the present invention provide optimum power gain. For example, network theory explains embodiments of the present invention when energy storage networks or matching networks are utilized to 'fly wheel' between apertures, thereby, on the average, providing a good impedance match. Network theory does not explain, however, why T_A is optimal. For instance, in some embodiments, one may deliberately utilize an aperture that is much less than a carrier half cycle. For such an aperture, there is an optimal matching network nonetheless. That is, a processor according to an embodiment of the present invention utilizing an improper aperture can be optimized, although it will not perform as well as a processor according to an embodiment of the present invention that utilizes an optimal aperture accompanied by an optimal matching network.

The idea behind selecting an optimal aperture is matched filter theory, which provides a general guideline for obtaining the best correlation properties between the incoming waveform and the selected aperture. Any practical correlator or matched filter is constrained by the same physical laws, however, which spawned the maximum power transfer theorems for networks. It does not do any good to design the optimum correlator aperture if the device possesses extraordinary impedance mismatches with its source and load. The circuit theorems do predict the optimal impedance match while matched filter theory does not. The two work hand in hand to permit a practical explanation for:

- Why T_4 is optimal; and
- How processors according to embodiments of the present invention are optimized for performance in practical circuits.

The following sub-section analyzes the present invention on a macroscopic scale using the notions of average impedance and power transfer.

12.2 Impedance Matching

When a processor embodiment according to the present invention is 'off,' there is one impedance, and when a processor embodiment according to the present invention is 'on,' there is another impedance due to the architecture of the present invention and its load. In practice, the aperture will affect the 'on' impedance. Hence, on the average, the input impedance looking into the circuitry of an embodiment of the present invention (i.e., its ports) is modified according to the present invention clock and T_A. Impedance matching networks must take this into account.

$$Z_{av} = \frac{V}{I_{av}} \qquad \text{EQ. (160)}$$

EQ. (160) illustrates that the average impedance, Z_{BV}, is related to the voltage, V, divided by the average current flow, I_{av}, into a device, for example a processor according to an embodiment of the present invention. EQ. (160) indicates that for a processor according to an embodiment of the present invention the narrower T_A and the less frequent a sample is acquired, the greater Z_{av} becomes.

To understand this, consider the fact that a 10th harmonic system according to an embodiment of the present invention operates with half as many samples as a 5th harmonic sample according to the present invention. Thus, according to EQ. (160), a 5th harmonic sample according to an embodiment of the present invention would typically possess a higher input/output impedance than that a 10th harmonic system according to the present invention. Of course, practical board and circuit parasitics will place limits on how much the impedance scaling properties of the present invention processor clock signals control the processor's overall input/output impedance.

As will be apparent to persons skilled in the relevant arts given the discussion herein, in embodiments, matching networks should be included at the ports of a processor according to the present invention to accommodate Z_{av}, as measured by a typical network analyzer.

13. Time Domain Analysis

All signals can be represented by vectors in the complex signal plane. Previous sub-sections derived the result for down converting (or up converting) $S_i(t)$ in the transform domain via $S_i(\omega)$. An I/Q modem embodiment of the present invention, however, was developed using a time domain analysis. This time domain analysis is repeated here and provides a complementary view to the previous sub-sections.

FIG. **194** illustrates an embodiment of the present invention implementing a complex down converter architecture. Operation of this embodiment is described given by:

$$S_0(t_k) \cong \sum_{k=0}^{\infty} (S_i(t_k) + n(t_k))(C_{Ik} + C_{Qk}) \quad \text{EQ. (161.1)}$$

where $S_i(t_k)$ is defined as the kth sample from the UFT transform such that $S_i(t_k)$ is filtered over the kth interval, $n(t_k)$ is defined as the noise sample at the output of the kth present invention kernel interval such that it has been averaged by the present invention process over the interval, C_{ik} is defined as the kth in phase gating waveform (the present invention clock), and C_{Qk} is defined as the kth quadrature phase gating waveform (the present invention clock).

The 'goodness' of $S_i(t_k)$ and $n_i(t_k)$ has been shown previously herein as related to the type of present invention processor used (e.g., matched filtering/correlating processor, finite time integrating processor, or RC processor). Each t_k instant is the time tick corresponding to the averaging of input waveform energy over a T_A (aperture) duration. It has been assumed that C_{ik} and C_{Qk} are constant envelope and phase for the current analysis, although in general this is not required. Many different, interesting processors according to embodiments of the present invention can be constructed by manipulating the amplitudes and phases of the present invention clock.

C_{ik} and C_{Qk} can be expanded as follows:

$$C_{Ik} = \quad \text{EQ. (161.2)}$$

$$K\frac{T_A}{T_s}\left[1+2\left(\frac{\sin\pi\frac{T_A}{T_s}}{\pi\frac{T_A}{T_s}}\cdot\cos 2\pi f_s t_k + \frac{\sin 2\pi\frac{T_A}{T_s}}{\pi\frac{T_A}{T_s}}\cdot\cos 4\pi f_s t_k + \frac{\sin 3\pi\frac{T_A}{T_s}}{3\pi\frac{T_A}{T_s}}\cdot\cos 6\pi f_s t_k + \ldots \frac{\sin n\pi\frac{T_A}{T_s}}{n\pi\frac{T_A}{T_s}}\cdot\cos n\cdot 2\pi f_s t_k\right)\right]$$

$$C_{Qk} = \quad \text{EQ. (161.3)}$$

$$K\frac{T_A}{T_s}\left[1+2\left(\frac{\sin\pi\frac{T_A}{T_s}}{\pi\frac{T_A}{T_s}}\cdot\sin 2\pi f_s t_k - \frac{\sin 2\pi\frac{T_A}{T_s}}{\pi\frac{T_A}{T_s}}\cdot\cos 4\pi f_s t_k - \frac{\sin 3\pi\frac{T_A}{T_s}}{3\pi\frac{T_A}{T_s}}\cdot\sin 6\pi f_s t_k \ldots \frac{\sin n\pi\frac{T_A}{T_s}}{n\pi\frac{T_A}{T_s}}\cdot\cos(n\cdot 2\pi f_s t_k + n\phi)\right)\right]$$

The above treatment is a Fourier series expansion of the present invention clocks where:

K $\underline{\Delta}$ Arbitrary Gain Constant

T_A $\underline{\Delta}$ Aperture Time=f_s^{-1}

T_s $\underline{\Delta}$ The Present Invention Clock Interval or Sample Time

n $\underline{\Delta}$ Harmonic Spectrum Harmonic Order

ϕ $\underline{\Delta}$ As phase shift angle usually selected as 90° ($\pi/2$) for orthogonal signaling

Each term from C_{Ik}, C_{Qk} will down convert (or up convert). However, only the odd terms in the above formulation (for $\phi=\pi/2$) will convert in quadrature. ϕ could be selected otherwise to utilize the even harmonics, but this is typically not done in practice.

For the case of down conversion, r(t) can be written as:

$$r(t_k)=\sqrt{2}A(\tilde{S}_{iI}(t_k)\cos(m\cdot 2\pi f t_k+\Theta)-\tilde{S}_{iQ}(t_k)\sin(m\cdot 2\pi f t_k+\Theta)+n(t)) \quad \text{EQ. (162)}$$

After applying (C_{Ik}, C_{Qk}) and lowpass filtering, which in embodiments is inherent to the present invention process, the down converted components become:

$$S_0(t_k)_I=AS_{iI}(t_k)+\tilde{n}_{Ik} \quad \text{EQ. (163)}$$

$$S_0(t_k)_Q=AS_{iQ}(t_k)+\tilde{n}_{Qk} \quad \text{EQ. (164)}$$

where:

$S_{iI}(t_k)\underline{\Delta}$ The In phase component of the desired baseband signal.

$S_{iQ}(t_k)\underline{\Delta}$ The quadrature phase component of the desired baseband signal.

$\tilde{n}_i$, $\tilde{n}_Q$ $\underline{\Delta}$ In phase and quadrature phase noise samples

m $\underline{\Delta}$ Is the harmonic of interest equal to one of the 'n' numbers, for perfect carrier synchronization.

Now m and n can be selected such that the down conversion ideally strips the carrier (mf_s), after lowpass filtering.

If the carrier is not perfectly coherent, a phase shift occurs as described in previous sub-section. The result presented above would modify to:

$$S_0(t)=(S_0(t)_I+jS_0(t)_Q)e^{j\phi} \quad \text{EQ. (165)}$$

where ϕ is the phase shift. This is the same phase shift affect derived earlier as cos ϕ in the present invention transform. When there is a slight carrier offset then ϕ can be written as $\phi(t)$ and the I and Q outputs represent orthogonal, harmonically oscillating vectors super imposed on the desired signal output with a beat frequency proportional to:

$$f_{error}\underline{\Delta}nf_s\pm m(f_s\pm f_\Delta)=f_s(n-m)+mf_\Delta \quad \text{EQ. (166)}$$

f_Δ $\underline{\Delta}$ as a slight frequency offset between the carrier and the present invention clock

This entire analysis could have been accomplished in the frequency domain as described herein, or it could have been formulated from the present invention kernel as:

$$S_0(t)=D_{IQ}(S_i(t)+n(t)) \quad \text{EQ. (167)}$$

The recursive kernel D_{IQ} is defined in sub-section 8 and the I/Q version is completed by superposition and phase shifting the quadrature kernel.

The previous equation for r(t) could be replaced with:

$$BB(t)=\tilde{S}_{iI}\pm\tilde{S}_{iQ} \text{ where } f=0 \text{ and } \Theta=\pi/4 \text{ and } n(t)=0 \quad \text{EQ. (168)}$$

BB(t) could be up converted by applying C_I, C_Q. The desired carrier then is the appropriate harmonic of C_I, C_Q whose energy is optimally extracted by a network matched to the desired carrier.

14. Complex Passband Waveform Generation Using the Present Invention Cores

This sub-section introduces the concept of using a present invention core to modulate signals at RF according to embodiments of the invention. Although many specific modulator architectures are possible, which target individual signaling schemes such as AM, FM, PM, etc., the example architecture presented here is a vector signal modulator. Such

a modulator can be used to create virtually every known useful waveform to encompass the whole of analog and digital communications applications, for "wired" or "wireless," at radio frequency or intermediate frequency. In essence, a receiver process, which utilizes the present invention, may be reversed to create signals of interest at passband. Using I/Q waveforms at baseband, all points within the two dimensional complex signaling constellation may be synthesized when cores according to the present invention are excited by orthogonal sub-harmonic clocks and connected at their outputs with particular combining networks. A basic architecture that can be used is shown in FIG. **195**.

FIG. **195** depicts one embodiment of a based vector modulator according to the present invention. FIG. **195** shows I and Q inputs that can accept analog or balanced digital waveforms. By selecting I and Q appropriately, AM, FM, BPSK, QPSK, MSK, QAM, OFDM, multi-tone, and a host of other signals can be synthesized. In this embodiment of the present invention, the present invention cores are driven differentially on I and Q. C_I, $C_{\overline{I}}$, C_Q, $C_{\overline{Q}}$ are the in phase and quadrature sub-harmonic clocks, respectively, with their inverted phases as well. C_I and C_Q can be created in quadrature for I Q operation if the output power combiner is a 0° combiner. On the other hand, C_I and C_Q can be in phase when a 90° output power combiner is utilized at RF. This latter architecture can be used whenever the signaling bandwidth is very small with respect to the RF center frequency of the output and small with respect to the 1 dB passband response of the combiner. If one assumes constant values on I and $\overline{I}$, the waveform diagrams in FIG. **196** can be constructed. As indicated in FIG. **195**, the power combiner and bandpass reconstruction filter are optional components.

In FIG. **196**, C_I and $\overline{C_I}$ are out of phase by 180° if referenced back to the clock. In this case, clock refers to the sub-harmonic waveform used to generate C_I and $\overline{C_I}$. C_I is coincident with the rising edges of clock with a pulse width of T_A while $\overline{C_I}$ is coincident with the falling edges of clock with a pulse width of T_A. C_I and $\overline{C_I}$ activate two of the processors according to the present invention, as shown in FIG. **195**, which are driven by differential signals. I_c is illustrated as if the system is ideal without losses, parasitics, or distortions. The time axis for I_c may be arranged in a manner to represent the waveform as an odd function. For such an arrangement, the Fourier series is calculated to obtain EQ. (169).

$$I_c(t) = \sum_{n=1}^{\infty} \left(\frac{4\sin\left(\frac{n\pi T_A}{T_s}\right) \cdot \sin\left(\frac{n\pi}{2}\right)}{n\pi} \right) \cdot \sin\left(\frac{2n\pi t}{T_s}\right) \quad \text{EQ. (169)}$$

To illustrate this, if a passband waveform must be created at five times the frequency of the sub-harmonic clock then a baseline power for that harmonic extraction can be calculated for n=5. For the case of n=5, it is found that the 5th harmonic yields:

$$I_c(t)|_{n=5} = \frac{4}{5\pi}(\sin(5\omega_s t)) \quad \text{EQ. (170)}$$

This component can be extracted from the Fourier series via a bandpass filter centered around f_s. This component is a carrier at 5 times the sampling frequency.

This illustration can be extended to show the following:

$$m(t) \cdot I_c(t)|_{\theta=(t)}^{n=5} = \frac{4 \cdot m(t)}{5\pi}(\sin(5\omega_s t + 5\phi(t))) \quad \text{EQ. (171)}$$

This equation illustrates that a message signal may have been superposed on I and $\overline{I}$ such that both amplitude and phase are modulated, i.e., m(t) for amplitude and $\phi(t)$ for phase. In such cases, it should be noted that $\phi(t)$ is augmented modulo n while the amplitude modulation m(t) is scaled. The point of this illustration is that complex waveforms may be reconstructed from their Fourier series with multi-aperture processor combinations, according to the present invention.

In a practical system according to an embodiment of the present invention, parasitics, filtering, etc., may modify $I_c(t)$. In many applications according to the present invention, charge injection properties of processors play a significant role. However, if the processors and the clock drive circuits according to embodiments of the present invention are matched then even the parasitics can be managed, particularly since unwanted distortions are removed by the final bandpass filter, which tends to completely reconstruct the waveform at passband.

Like the receiver embodiments of the present invention, which possess a lowpass information extraction and energy extraction impulse response, various transmitter embodiments of the present invention use a network to create a bandpass impulse response suitable for energy transfer and waveform reconstruction. In embodiments, the simplest reconstruction network is an L-C tank, which resonates at the desired carrier frequency $N \cdot f_s = f_c$.

V. ADDITIONAL EMBODIMENTS

1. Example I/Q Modulation Receiver Embodiment

FIG. **197** illustrates an example I/Q modulation receiver **19700**, according to an embodiment of the present invention. I/Q modulation receiver **19700** comprises a first Processing module **19702**, a first optional filter **19704**, a second Processing module **19706**, a second optional filter **19708**, a third Processing module **19710**, a third optional filter **19712**, a fourth Processing module **19714**, a fourth filter **19716**, an optional LNA **19718**, a first differential amplifier **19720**, a second differential amplifier **19722**, and an antenna **19772**.

I/Q modulation receiver **19700** receives, down-converts, and demodulates a I/Q modulated RF input signal **19782** to an I baseband output signal **19784**, and a Q baseband output signal **19786**. I/Q modulated RF input signal comprises a first information signal and a second information signal that are I/Q modulated onto an RF carrier signal. I baseband output signal **19784** comprises the first baseband information signal. Q baseband output signal **19786** comprises the second baseband information signal.

Antenna **19772** receives I/Q modulated RF input signal **19782**. I/Q modulated RF input signal **19782** is output by antenna **19772** and received by optional LNA **19718**. When present, LNA **19718** amplifies I/Q modulated RF input signal **19782**, and outputs amplified I/Q signal **19788**.

First Processing module **19702** receives amplified I/Q signal **19788**. First Processing module **19702** down-converts the I-phase signal portion of amplified input I/Q signal **19788** according to an I control signal **19790**. First Processing module **19702** outputs an I output signal **19798**.

In an embodiment, first Processing module **19702** comprises a first storage module **19724**, a first UFT module

19726, and a first voltage reference 19728. In an embodiment, a switch contained within first UFT module 19726 opens and closes as a function of I control signal 19790. As a result of the opening and closing of this switch, which respectively couples and de-couples first storage module 19724 to and from first voltage reference 19728, a down-converted signal, referred to as I output signal 19798, results. First voltage reference 19728 may be any reference voltage, and is ground in some embodiments. I output signal 19798 is stored by first storage module 19724.

In an embodiment, first storage module 19724 comprises a first capacitor 19774. In addition to storing I output signal 19798, first capacitor 19774 reduces or prevents a DC offset voltage resulting from charge injection from appearing on I output signal 19798

I output signal 19798 is received by optional first filter 19704. When present, first filter 19704 is a high pass filter to at least filter I output signal 19798 to remove any carrier signal "bleed through". In an embodiment, when present, first filter 19704 comprises a first resistor 19730, a first filter capacitor 19732, and a first filter voltage reference 19734. Preferably, first resistor 19730 is coupled between I output signal 19798 and a filtered I output signal 19707, and first filter capacitor 19732 is coupled between filtered I output signal 19707 and first filter voltage reference 19734. Alternately, first filter 19704 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant arts. First filter 19704 outputs filtered I output signal 19707.

Second Processing module 19706 receives amplified I/Q signal 19788. Second Processing module 19706 down-converts the inverted I-phase signal portion of amplified input I/Q signal 19788 according to an inverted I control signal 19792. Second Processing module 19706 outputs an inverted I output signal 19701.

In an embodiment, second Processing module 19706 comprises a second storage module 19736, a second UFT module 19738, and a second voltage reference 19740. In an embodiment, a switch contained within second UFT module 19738 opens and closes as a function of inverted I control signal 19792. As a result of the opening and closing of this switch, which respectively couples and de-couples second storage module 19736 to and from second voltage reference 19740, a down-converted signal, referred to as inverted I output signal 19701, results. Second voltage reference 19740 may be any reference voltage, and is preferably ground. Inverted I output signal 19701 is stored by second storage module 19736.

In an embodiment, second storage module 19736 comprises a second capacitor 19776. In addition to storing inverted I output signal 19701, second capacitor 19776 reduces or prevents a DC offset voltage resulting from above described charge injection from appearing on inverted I output signal 19701.

Inverted I output signal 19701 is received by optional second filter 19708. When present, second filter 19708 is a high pass filter to at least filter inverted I output signal 19701 to remove any carrier signal "bleed through". In an embodiment, when present, second filter 19708 comprises a second resistor 19742, a second filter capacitor 19744, and a second filter voltage reference 19746. In an embodiment, second resistor 19742 is coupled between inverted I output signal 19701 and a filtered inverted I output signal 19709, and second filter capacitor 19744 is coupled between filtered inverted I output signal 19709 and second filter voltage reference 19746. Alternately, second filter 19708 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant arts. Second filter 19708 outputs filtered inverted I output signal 19709.

First differential amplifier 19720 receives filtered I output signal 19707 at its non-inverting input and receives filtered inverted I output signal 19709 at its inverting input. First differential amplifier 19720 subtracts filtered inverted I output signal 19709 from filtered I output signal 19707, amplifies the result, and outputs I baseband output signal 19784. Other suitable subtractor modules may be substituted for first differential amplifier 19720, and second differential amplifier 19722, as would be understood by persons skilled in the relevant arts from the teachings herein. Because filtered inverted I output signal 19709 is substantially equal to an inverted version of filtered I output signal 19707, I baseband output signal 19784 is substantially equal to filtered I output signal 19709, with its amplitude doubled. Furthermore, filtered I output signal 19707 and filtered inverted I output signal 19709 may comprise substantially equal noise and DC offset contributions of the same polarity from prior down-conversion circuitry, including first Processing module 19702 and second Processing module 19706, respectively. When first differential amplifier 19720 subtracts filtered inverted I output signal 19709 from filtered I output signal 19707, these noise and DC offset contributions substantially cancel each other.

Third Processing module 19710 receives amplified I/Q signal 19788. Third Processing module 19710 down-converts the Q-phase signal portion of amplified input I/Q signal 19788 according to an Q control signal 19794. Third Processing module 19710 outputs an Q output signal 19703.

In an embodiment, third Processing module 19710 comprises a third storage module 19748, a third UFT module 19750, and a third voltage reference 19752. In an embodiment, a switch contained within third UFT module 19750 opens and closes as a function of Q control signal 19794. As a result of the opening and closing of this switch, which respectively couples and de-couples third storage module 19748 to and from third voltage reference 19752, a down-converted signal, referred to as Q output signal 19703, results. Third voltage reference 19752 may be any reference voltage, and is preferably ground. Q output signal 19703 is stored by third storage module 19748.

In an embodiment, third storage module 19748 comprises a third capacitor 19778. In addition to storing Q output signal 19703, third capacitor 19778 reduces or prevents a DC offset voltage resulting from above described charge injection from appearing on Q output signal 19703.

Q output signal 19703 is received by optional third filter 19716. When present, third filter 19716 is a high pass filter to at least filter Q output signal 19703 to remove any carrier signal "bleed through". In an embodiment, when present, third filter 19712 comprises a third resistor 19754, a third filter capacitor 19758, and a third filter voltage reference 19758. In an embodiment, third resistor 19754 is coupled between Q output signal 19703 and a filtered Q output signal 19711, and third filter capacitor 19756 is coupled between filtered Q output signal 19711 and third filter voltage reference 19758. Alternately, third filter 19712 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant arts. Third filter 19712 outputs filtered Q output signal 19711.

Fourth Processing module 19714 receives amplified I/Q signal 19788. Fourth Processing module 19714 down-converts the inverted Q-phase signal portion of amplified input I/Q signal 19788 according to an inverted Q control signal 19796. Fourth Processing module 19714 outputs an inverted Q output signal 19705.

In an embodiment, fourth Processing module **19714** comprises a fourth storage module **19760**, a fourth UFT module **19762**, and a fourth voltage reference **19764**. In an embodiment, a switch contained within fourth UFT module **19762** opens and closes as a function of inverted Q control signal **19796**. As a result of the opening and closing of this switch, which respectively couples and de-couples fourth storage module **19760** to and from fourth voltage reference **19764**, a down-converted signal, referred to as inverted Q output signal **19705**, results. Fourth voltage reference **19764** may be any reference voltage, and is preferably ground. Inverted Q output signal **19705** is stored by fourth storage module **19760**.

In an embodiment, fourth storage module **19760** comprises a fourth capacitor **19780**. In addition to storing inverted Q output signal **19705**, fourth capacitor **19780** reduces or prevents a DC offset voltage resulting from above described charge injection from appearing on inverted Q output signal **19705**.

Inverted Q output signal **19705** is received by optional fourth filter **19716**. When present, fourth filter **19716** is a high pass filter to at least filter inverted Q output signal **19705** to remove any carrier signal "bleed through". In an embodiment, when present, fourth filter **19716** comprises a fourth resistor **19766**, a fourth filter capacitor **19768**, and a fourth filter voltage reference **19770**. In an embodiment, fourth resistor **19766** is coupled between inverted Q output signal **19705** and a filtered inverted Q output signal **19713**, and fourth filter capacitor **19768** is coupled between filtered inverted Q output signal **19713** and fourth filter voltage reference **19770**. Alternately, fourth filter **19716** may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant arts. Fourth filter **19716** outputs filtered inverted Q output signal **19713**.

Second differential amplifier **19722** receives filtered Q output signal **19711** at its non-inverting input and receives filtered inverted Q output signal **19713** at its inverting input. Second differential amplifier **19722** subtracts filtered inverted Q output signal **19713** from filtered Q output signal **19711**, amplifies the result, and outputs Q baseband output signal **19786**. Because filtered inverted Q output signal **19713** is substantially equal to an inverted version of filtered Q output signal **19711**, Q baseband output signal **19786** is substantially equal to filtered Q output signal **19713**, with its amplitude doubled. Furthermore, filtered Q output signal **19711** and filtered inverted Q output signal **19713** may comprise substantially equal noise and DC offset contributions of the same polarity from prior down-conversion circuitry, including third Processing module **19710** and fourth Processing module **19714**, respectively. When second differential amplifier **19722** subtracts filtered inverted Q output signal **19713** from filtered Q output signal **19711**, these noise and DC offset contributions substantially cancel each other.

2. Example I/Q Modulation Control Signal Generator Embodiments

FIG. **198** illustrates an exemplary block diagram for an example I/Q modulation control signal generator **19800**, according to an embodiment of the present invention. I/Q modulation control signal generator **19800** generates I control signal **19790**, inverted I control signal **19792**, Q control signal **19794**, and inverted Q control signal **19796** used by I/Q modulation receiver **19700** of FIG. **197**. I control signal **19790** and inverted I control signal **19792** operate to down-convert the I-phase portion of an input I/Q modulated RF signal. Q control signal **19794** and inverted Q control signal **19796** act to down-convert the Q-phase portion of the input I/Q modulated RF signal. Furthermore, I/Q modulation control signal generator **19800** has the advantage of generating control signals in a manner such that resulting collective circuit re-radiation is radiated at one or more frequencies outside of the frequency range of interest. For instance, potential circuit re-radiation is radiated at a frequency substantially greater than that of the input RF carrier signal frequency.

I/Q modulation control signal generator **19800** comprises a local oscillator **19802**, a first divide-by-two module **19804**, a 180 degree phase shifter **19806**, a second divide-by-two module **19808**, a first pulse generator **19810**, a second pulse generator **19812**, a third pulse generator **19814**, and a fourth pulse generator **19816**.

Local oscillator **19802** outputs an oscillating signal **19818**. FIG. **199** shows an exemplary oscillating signal **19818**.

First divide-by-two module **19804** receives oscillating signal **19818**, divides oscillating signal **19818** by two, and outputs a half frequency LO signal **19820** and a half frequency inverted LO signal **19826**. FIG. **199** shows an exemplary half frequency LO signal **19820**. Half frequency inverted LO signal **19826** is an inverted version of half frequency LO signal **19820**. First divide-by-two module **19804** may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant arts.

180 degree phase shifter **19806** receives oscillating signal **19818**, shifts the phase of oscillating signal **19818** by 180 degrees, and outputs phase shifted LO signal **19822**. 180 degree phase shifter **19806** may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant arts. In alternative embodiments, other amounts of phase shift may be used.

Second divide-by two module **19808** receives phase shifted LO signal **19822**, divides phase shifted LO signal **19822** by two, and outputs a half frequency phase shifted LO signal **19824** and a half frequency inverted phase shifted LO signal **19828**. FIG. **199** shows an exemplary half frequency phase shifted LO signal **19824**. Half frequency inverted phase shifted LO signal **19828** is an inverted version of half frequency phase shifted LO signal **19824**. Second divide-by-two module **19808** may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant arts.

First pulse generator **19810** receives half frequency LO signal **19820**, generates an output pulse whenever a rising edge is received on half frequency LO signal **19820**, and outputs I control signal **19790**. FIG. **199** shows an exemplary I control signal **19790**.

Second pulse generator **19812** receives half frequency inverted LO signal **19826**, generates an output pulse whenever a rising edge is received on half frequency inverted LO signal **19826**, and outputs inverted I control signal **19792**. FIG. **199** shows an exemplary inverted I control signal **19792**.

Third pulse generator **19814** receives half frequency phase shifted LO signal **19824**, generates an output pulse whenever a rising edge is received on half frequency phase shifted LO signal **19824**, and outputs Q control signal **19794**. FIG. **199** shows an exemplary Q control signal **19794**.

Fourth pulse generator **19816** receives half frequency inverted phase shifted LO signal **19828**, generates an output pulse whenever a rising edge is received on half frequency inverted phase shifted LO signal **19828**, and outputs inverted Q control signal **19796**. FIG. **199** shows an exemplary inverted Q control signal **19796**.

In an embodiment, control signals **19790**, **19792**, **19794** and **19796** output pulses having a width equal to one-half of a period of I/Q modulated RF input signal **19782**. The invention, however, is not limited to these pulse widths, and control

signals **19790**, **19792**, **19794**, and **19796** may comprise pulse widths of any fraction of, or multiple and fraction of, a period of I/Q modulated RF input signal **19782**. Also, other circuits for generating control signals **19790**, **19792**, **19794**, and **19796** will be apparent to persons skilled in the relevant arts based on the herein teachings.

First, second, third, and fourth pulse generators **19810**, **19812**, **19814**, and **19816** may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant arts.

As shown in FIG. **199**, in embodiments control signals **19790**, **19792**, **19794**, and **19796** comprise pulses that are non-overlapping. Furthermore, in this example, pulses appear on these signals in the following order: I control signal **19790**, Q control signal **19794**, inverted I control signal **19792**, and inverted Q control signal **19796**. Potential circuit re-radiation from I/Q modulation receiver **19700** may comprise frequency components from a combination of these control signals.

For example, FIG. **200** shows an overlay of pulses from I control signal **19790**, Q control signal **19794**, inverted I control signal **19792**, and inverted Q control signal **19796**. When pulses from these control signals leak through first, second, third, and fourth Processing modules **19702**, **19706**, **19710**, and **19714** to antenna **19782** (shown in FIG. **197**), they may be radiated from I/Q modulation receiver **19700**, with a combined waveform that appears to have a primary frequency equal to four times the frequency of any single one of control signals **19790**, **19792**, **19794**, and **19796**. FIG. **199** shows an example combined control signal **19902**.

FIG. **200** also shows an example I/Q modulation RF input signal **19782** overlaid upon control signals **19790**, **19792**, **19794**, and **19796**. As shown in FIG. **200**, pulses on I control signal **19790** overlay and act to down-convert a positive I-phase portion of I/Q modulation RF input signal **19782**. Pulses on inverted I control signal **19792** overlay and act to down-convert a negative I-phase portion of I/Q modulation RF input signal **19782**. Pulses on Q control signal **19794** overlay and act to down-convert a rising Q-phase portion of I/Q modulation RF input signal **19782**. Pulses on inverted Q control signal **19796** overlay and act to down-convert a falling Q-phase portion of I/Q modulation RF input signal **19782**.

As FIG. **200** further shows in this example, the frequency ratio between the combination of control signals **19790**, **19792**, **19794**, and **19796** and I/Q modulation RF input signal **19782** is 4:3. Because the frequency of the potentially re-radiated signal, combined control signal **19902**, is substantially different from that of the signal being down-converted, I/Q modulation RF input signal **19782**, it does not interfere with signal down-conversion as it is out of the frequency band of interest, and hence may be filtered out. In this manner, I/Q modulation receiver **19700** reduces problems due to circuit re-radiation. As will be understood by persons skilled in the relevant arts from the teachings herein, frequency ratios other than 4:3 may be implemented to achieve similar reduction of problems of circuit re-radiation.

It should be understood that the above control signal generator circuit example is provided for illustrative purposes only. The invention is not limited to these embodiments. Alternative embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) for I/Q modulation control signal generator **19800** will be apparent to persons skilled in the relevant arts from the teachings herein, and are within the scope of the present invention.

3. Detailed Example I/Q Modulation Receiver Embodiment with Exemplary Waveforms

FIG. **201** illustrates a more detailed example circuit implementation of I/Q modulation receiver **19700**, according to an embodiment of the present invention. FIGS. **202-40** show waveforms related to an example implementation of I/Q modulation receiver **19700** of FIG. **201**.

FIGS. **202** and **203** show first and second input data signals **20102** and **20104** to be I/Q modulated with a RF carrier signal frequency as the I-phase and Q-phase information signals, respectively.

FIGS. **205** and **206** show the signals of FIGS. **202** and **203** after modulation with a RF carrier signal frequency, respectively, as I-modulated signal **20106** and Q-modulated signal **20108**.

FIG. **204** shows an I/Q modulation RF input signal **19782** formed from I-modulated signal **20106** and Q-modulated signal **20108** of FIGS. **205** and **206**, respectively.

FIG. **211** shows an overlaid view of filtered I output signal **21102** and filtered inverted I output signal **21104**.

FIG. **212** shows an overlaid view of filtered Q output signal **21202** and filtered inverted Q output signal **21204**.

FIGS. **207** and **208** show I baseband output signal **19784** and Q baseband output signal **19786**, respectfully. A data transition **20402** is indicated in both I baseband output signal **19784** and Q baseband output signal **19786**. The corresponding data transition **20402** is indicated in I-modulated signal **20106** of FIG. **205**, Q-modulated signal **20108** of FIG. **206**, and I/Q modulation RF input signal **19782** of FIG. **204**.

FIGS. **209** and **210** show I baseband output signal **19784** and Q baseband output signal **19786** over a wider time interval.

4. Example Single Channel Receiver Embodiment

FIG. **213** illustrates an example single channel receiver **21300**, corresponding to either the I or Q channel of I/Q modulation receiver **19700**, according to an embodiment of the present invention. Single channel receiver **21300** can down-convert an input RF signal **21306** modulated according to AM, PM, FM, and other modulation schemes. Refer to the section above for further description on the operation of single channel receiver **21300**.

5. Example Automatic Gain Control (AGC) Embodiment

According to embodiments of the invention, the amplitude level of the down-converted signal can be controlled by modifying the aperture of the control signal that controls the switch module. Consider FIG. **43**, that illustrates an equation that represents the change in charge in the storage device of embodiments of the UFT module, such as a capacitor. This equation is a function of T, which is the aperture of the control signal. Thus, by modifying the aperture T of the control signal, it is possible to modify the amplitude level of the down-converted signal.

Some embodiments may include a control mechanism to enable manual control of aperture T, and thus manual control of the amplitude level of the down-converted signal. Other embodiments may include automatic or semi-automatic control modules to enable automatic or semi-automatic control of aperture T, and thus automatic or semi-automatic control of the amplitude level of the down-converted signal. Such embodiments are herein referred to (without limitation) as automatic gain control (AGC) embodiments. Other embodiments include a combination of manual and automatic control of aperture T.

6. Other Example Embodiments

Additional aspects/embodiments of the invention are considered in this section.

In one embodiment of the present invention there is provided a method of transmitting information between a transmitter and a receiver comprising the steps of transmitting a first series of signals each having a known period from the transmitter at a known first repetition rate; sampling by the receiver each signal in the first series of signals a single time and for a known time interval the sampling of the first series of signals being at a second repetition rate that is a rate different from the first repetition rate by a known amount; and generating by the receiver an output signal indicative of the signal levels sampled in step B and having a period longer than the known period of a transmitted signal.

In another embodiment of the invention there is provided a communication system comprising a transmitter means for transmitting a first series of signals of known period at a known first repetition rate, a receiver means for receiving the first series of signals, the receiver means including sampling means for sampling the signal level of each signal first series of signals for a known time interval at a known second repetition rate, the second repetition rate being different from the first repetition rate by a known amount as established by the receiver means. The receiver means includes first circuit means for generating a first receiver output signal indicative of the signal levels sampled and having a period longer than one signal of the first series of signals. The transmitter means includes an oscillator for generating an oscillator output signal at the first repetition rate, switch means for receiving the oscillator output signal and for selectively passing the oscillator output signal, waveform generating means for receiving the oscillator output signal for generating a waveform generator output signal having a time domain and frequency domain established by the waveform generating means.

The embodiment of the invention described herein involves a single or multi-user communications system that utilizes coherent signals to enhance the system performance over conventional radio frequency schemes while reducing cost and complexity. The design allows direct conversion of radio frequencies into baseband components for processing and provides a high level of rejection for signals that are not related to a known or controlled slew rate between the transmitter and receiver timing oscillators. The system can be designed to take advantage of broadband techniques that further increase its reliability and permit a high user density within a given area. The technique employed allows the system to be configured as a separate transmitter-receiver pair or a transceiver.

An objective of the present system is to provide a new communication technique that can be applied to both narrow and wide band systems. In its most robust form, all of the advantages of wide band communications are an inherent part of the system and the invention does not require complicated and costly circuitry as found in conventional wide band designs. The communications system utilizes coherent signals to send and receive information and consists of a transmitter and a receiver in its simplest form. The receiver contains circuitry to turn its radio frequency input on and off in a known relationship in time to the transmitted signal. This is accomplished by allowing the transmitter timing oscillator and the receiver timing oscillator to operate at different but known frequencies to create a known slew rate between the oscillators. If the slew rate is small compared to the timing oscillator frequencies, the transmitted waveform will appear stable in time, i.e., coherent (moving at the known slew rate) to the receiver's switched input. The transmitted waveform is the only waveform that will appear stable in time to the receiver and thus the receiver's input can be averaged to achieve the desired level filtering of unwanted signals. This methodology makes the system extremely selective without complicated filters and complex encoding and decoding schemes and allows the direct conversion of radio frequency energy from an antenna or cable to baseband frequencies with a minimum number of standard components further reducing cost and complexity. The transmitted waveform can be a constant carrier (narrowband), a controlled pulse (wideband and ultra-wideband) or a combination of both such as a dampened sinusoidal wave and or any arbitrary periodic waveform thus the system can be designed to meet virtually any bandwidth requirement. Simple standard modulation and demodulation techniques such as AM and Pulse Width Modulation can be easily applied to the system.

Depending on the system requirements such as the rate of information transfer, the process gain, and the intended use, there are multiple preferred embodiments of the invention. The embodiment discussed herein will be the amplitude and pulse width modulated system. It is one of the simplest implementations of the technology and has many common components with the subsequent systems. A amplitude modulated transmitter consists of a Transmitter Timing Oscillator, a Multiplier, a Waveform Generator, and an Optional Amplifier. The Transmitter Timing Oscillator frequency can be determined by a number of resonate circuits including an inductor and capacitor, a ceramic resonator, a SAW resonator, or a crystal. The output waveform is sinusoidal, although a squarewave oscillator would produce identical system performance.

The Multiplier component multiplies the Transmitter Timing Oscillator output signal by 0 or 1 or other constants, K**1** and K**2**, to switch the oscillator output on and off to the Waveform Generator. In this embodiment, the information input can be digital data or analog data in the form of pulse width modulation. The Multiplier allows the Transmitter Timing Oscillator output to be present at the Waveform Generator input when the information input is above a predetermined value. In this state the transmitter will produce an output waveform. When the information input is below a predetermined value, there is no input to the Waveform Generator and thus there will be no transmitter output waveform. The output of the Waveform Generator determines the system's bandwidth in the frequency domain and consequently the number of users, process gain immunity to interference and overall reliability), the level of emissions on any given frequency, and the antenna or cable requirements. The Waveform Generator in this example creates a one cycle pulse output which produces an ultra-wideband signal in the frequency domain. An optional power Amplifier stage boosts the output of the Waveform Generator to a desired power level.

With reference now to the drawings, the amplitude and pulse width modulated transmitter in accord with the present invention is depicted at numeral **13000** in FIGS. **130** and **131**. The Transmitter Timing Oscillator **13002** is a crystal-controlled oscillator operating at a frequency of 25 MHZ. Multiplier **13004** includes a two-input NAND gate **13102** controlling the gating of oscillator **13002** output to Waveform Generator **13006**. Waveform Generator **13006** produces a pulse output as depicted at **13208** in FIGS. **132**D and **133**, which produces a frequency spectrum **13402** in FIG. **134**. Amplifier **13008** is optional. The transmitter **13000** output is applied to antenna or cable **13010**, which as understood in the art, may be of various designs as appropriate in the circumstances.

FIGS. **132**A-**132**D, **133**, and **134** illustrate the various signals present in transmitter **13000**. The output of transmitter **13000** at "A" may be either a sinusoidal or squarewave signal **13202** that is provided as one input into NAND gate **13102**. Gate **13102** also receives an information signal **13204** at "B" which, in the embodiment shown, is digital in form. The output **13206** of Multiplier **13004** can be either sinusoidal or squarewave depending upon the original signal **13202**. Waveform Generator **13006** provides an output of a single cycle impulse signal **13208**. The single cycle impulse **13210** varies in voltage around a static level **13212** and is created at 40 nanoseconds intervals. In the illustrated embodiment, the frequency of transmitter **13002** is 25 MHZ and accordingly, one cycle pulses of 1.0 GHZ are transmitted every 40 nanoseconds during the total time interval that gate **13102** is "on" and passes the output of transmitter oscillator **13002**.

FIG. **135** shows the preferred embodiment receiver block diagram to recover the amplitude or pulse width modulated information and consists of a Receiver Timing Oscillator **13510**, Waveform Generator **13508**, RF Switch Fixed or Variable Integrator **13506**, Decode Circuit **13514**, two optional Amplifier/Filter stages **13504** and **13512**, antenna or cable input **13502**, and Information Output **13516**. The Receiver Timing Oscillator **13510** frequency can be determined by a number of resonate circuits including an inductor and capacitor, a ceramic resonator, a SAW resonator, or a crystal. As in the case of the transmitter, the oscillator **13510** shown here is a crystal oscillator. The output waveform is a squarewave, although a sinewave oscillator would produce identical system performance. The squarewave timing oscillator output **13602** is shown in FIG. **136**A. The Receiver Timing Oscillator **13510** is designed to operate within a range of frequencies that creates a known range of slew rates relative to the Transmitter Timing Oscillator **13002**. In this embodiment, the Transmitter Timing Oscillator **13002** frequency is 25 MHZ and the Receiver Timing Oscillator **13510** outputs between 25.0003 MHZ and 25.0012 MHZ which creates a+300 to +1200 Hz slew rate.

The Receiver Timing Oscillator **13510** is connected to the Waveform Generator **13508** which shapes the oscillator signal into the appropriate output to control the amount of the time that the RF switch **13506** is on and off. The on-time of the RF switch **13506** should be less than ½ of a cycle (1/10 of a cycle is preferred) or in the case of a single pulse, no wider than the pulse width of the transmitted waveform or the signal gain of the system will be reduced. Examples are illustrated in Table A1. Therefore the output of the Waveform Generator **13508** is a pulse of the appropriate width that occurs once per cycle of the receiver timing oscillator **13510**. The output **13604** of the Waveform Generator is shown in FIG. **136**B.

TABLE A1

Transmitted Waveform	Gain Limit on-time	Preferred on-time
Single 1 nanosecond pulse	1 nanosecond	100 picoseconds
1 Gigahertz 1, 2, 3 . . . etc. cycle output	500 picoseconds	50 picoseconds
10 Gigahertz 1, 2, 3 . . . etc. cycle output	50 picoseconds	5 picoseconds

The RF Switch/Integrator **13506** samples the RF signal **13606** shown in FIG. **136**C when the Waveform Generator output **13604** is below a predetermined value. When the Waveform Generator output **13604** is above a predetermined value, the RF Switch **13506** becomes a high impedance node and allows the Integrator to hold the last RF signal sample **13606** until the next cycle of the Waveform Generator **13508** output. The Integrator section of **13506** is designed to charge the Integrator quickly (fast attack) and discharge the Integrator at a controlled rate (slow decay). This embodiment provides unwanted signal rejection and is a factor in determining the baseband frequency response of the system. The sense of the switch control is arbitrary depending on the actual hardware implementation.

In an embodiment of the present invention, the gating or sampling rate of the receiver **13500** is 300 Hz higher than the 25 MHZ transmission rate from the transmitter **13000**. Alternatively, the sampling rate could be less than the transmission rate. The difference in repetition rates between the transmitter **13000** and receiver **13500**, the "slew rate," is 300 Hz and results in a controlled drift of the sampling pulses over the transmitted pulse which thus appears "stable" in time to the receiver **13500**. With reference now to FIGS. **132**A-**132**D and **136**A-**136**G, an example is illustrated for a simple case of an output signal **13608** (FIG. **136**D) that is constructed of four samples from four RF input pulses **13606** for ease of explanation. As can be clearly seen, by sampling the RF pulses **13606** passed when the transmitter information signal **13204** (FIG. **132**B) is above a predetermine threshold the signal **13608** is a replica of a signal **13606** but mapped into a different time base. In the case of this example, the new time base has a period four times longer than real time signal. The use of an optional amplifier/filter **13512** results in a further refinement of the signal **13608** which is present shown as signal **13610** in FIG. **136**E.

Decode Circuitry **13514** extracts the information contained in the transmitted signal and includes a Rectifier that rectifies signal **13608** or **13610** to provide signal **13612** in FIG. **136**G. The Variable Threshold Generator circuitry in circuit **13514** provides a DC threshold signal level **13614** for signal **13610** that is used to determine a high (transmitter output on) or low (transmitter output off) and is also shown in FIG. **136**G. The final output signal **13616** shown in FIG. **136**F is created by an output voltage comparator in circuit **13514** that combines signals **13612** and **13614** such that when the signal **13612** is a higher voltage than signal **13614**, the information output signal goes high. Accordingly, signal **13616** represents, for example, a digital "1" that is now time-based to a 1:4 expansion of the period of an original signal **13606**. While this illustration provides a 4:1 reduction in frequency, it is sometimes desired to provide a reduction of more than 50,000:1; in the preferred embodiment, 100,000:1 or greater is achieved. This results in a shift directly from RF input frequency to low frequency baseband without the requirement of expensive intermediate circuitry that would have to be used if only a 4:1 conversion was used as a first stage. Table A2 provides information as to the time base conversion and includes examples.

TABLE A2

Units

s = 1 ps = 1_10^{12} ns = 1_10^{-9} us = 1_10^{-6} MHz = 1_10^{6} KHz = 1_10^{3}

Receiver Timing Oscillator Frequency = 25.0003 MHz

Transmitter Timing Oscillator Frequency = 25 MHz

$$\text{period} = \frac{1}{\text{Transmitter Timing Oscillator Frequency}}$$

period = 40 ns

TABLE A2-continued

$$\text{slew rate} = \frac{1}{\text{Receiver Timing Oscillator Frequency} - \text{Transmitter Timing Oscillator Frequency}}$$

slew rate = 0.003 s

$$\text{time base multiplier} = \frac{\text{slew rate}}{\text{period}} \text{ seconds per nanosecond}$$

time base multiplier = 8.333_10^4

Example 1:

1 nanosecond translates into 83.33 microseconds
time base = (1 ns)_ time base multiplier
time base = 83.333 us

Example 2:

2 Gigahertz translates into 24 Kilohertz
2 Gigahertz = 500 picosecond
period
time base = (500 ps)_ time base multiplier
time base = 41.667 us

$$\text{frequency} = \frac{1}{\text{time base}}$$

frequency = 24 KHz

In the illustrated embodiment, the signal **13616** at "F" has a period of 83.33 usec, a frequency of 12 KHz and it is produced once every 3.3 msec for a 300 Hz slew rate. Stated another way, the system is converting a 1 gigahertz transmitted signal into an 83.33 microsecond signal.

Accordingly, the series of RF pulses **13210** that are transmitted during the presence of an "on" signal at the information input gate **13102** are used to reconstruct the information input signal **13204** by sampling the series of pulses at the receiver **13500**. The system is designed to provide an adequate number of RF inputs **13606** to allow for signal reconstruction.

An optional Amplifier/Filter stage or stages **13504** and **13512** may be included to provide additional receiver sensitivity, bandwidth control or signal conditioning for the Decode Circuitry **13514**. Choosing an appropriate time base multiplier will result in a signal at the output of the Integrator **13506** that can be amplified and filtered with operational amplifiers rather than RF amplifiers with a resultant simplification of the design process. The signal **13610** shown in FIG. **136**E illustrates the use of Amplifier/Filter **13512** (FIG. **137**). The optional RF amplifier **13504** shown as the first stage of the receiver should be included in the design when increased sensitivity and/or additional filtering is required. Example receiver schematics are shown in FIGS. **137-139**.

FIGS. **140-143** illustrate different pulse output signals **14002** and **14202** and their respective frequency domain at **14102** and **14302**. As can be seen from FIGS. **140** and **141**, the half-cycle signal **14002** generates a spectrum less subject to interference than the single cycle of FIG. **133** and the 10-cycle pulse of FIG. **142**. The various outputs determine the system's immunity to interference, the number of users in a given area, and the cable and antenna requirements. FIGS. **133** and **134** illustrate example pulse outputs.

FIGS. **144** and **145** show example differential receiver designs. The theory of operation is similar to the non-differential receiver of FIG. **135** except that the differential technique provides an increased signal to noise ratio by means of common mode rejection. Any signal impressed in phase at both inputs on the differential receiver will attenuated by the differential amplifier shown in FIGS. **144** and **145** and conversely any signal that produces a phase difference between the receiver inputs will be amplified.

FIGS. **146** and **147** illustrate the time and frequency domains of a narrow band/constant carrier signal in contrast to the ultra-wide band signals used in the illustrated embodiment.

VI. ADDITIONAL FEATURES OF THE INVENTION

1. Architectural Features of the Invention

The present invention provides, among other things, the following architectural features:

optimal baseband signal to noise ratio regardless of modulation (programmable RF matched filter);

exceptional linearity per milliwatt consumed;

easily integrated into bulk C-MOS (small size/low cost, high level of integration);

fundamental or sub-harmonic operation (does not change conversion efficiency);

transmit function provides frequency multiplication and signal gain; and

optimal power transfer into a scalable output impedance (independent of device voltage or current);

The present invention provides simultaneous solutions for two domains: power sampling and matched filtering. A conventional sampler is a voltage sampling device, and does not substantially affect the input signal. A power sampler according to the present invention attempts to take as much power from the input to construct the output, and does not necessarily preserve the input signal.

2. Additional Benefits of the Invention

2.1 Compared to an Impulse Sampler

The present invention out-performs a theoretically perfect impulse sampler. The performance of a practical implementation of the present invention exceeds the performance of a practical implementation of an impulse sampler. The present invention is easily implemented (does not require impulse circuitry).

2.2 Linearity

The present invention provides exceptional linearity per milliwatt. For example, rail to rail dynamic range is possible with minimal increase in power. In an example integrated circuit embodiment, the present invention provides +55 dmb IP2, +15 dbm IP3, @ 3.3V, 4.4 ma, −15 dmb LO. GSM system requirements are +22 dbm IP2, −10.5 dmb IP3. CDMA system requirements are +50 dmb IP2, +10 dbm IP3.

2.3 Optimal Power Transfer into a Scalable Output Impedance

In an embodiment of the present invention, output impedance is scalable to facilitate a low system noise figure. In an embodiment, changes in output impedance do not affect power consumption.

2.4 System Integration

In an embodiment, the present invention enables a high level of integration in bulk C-MOS. Other features include:

small footprint;

no multiplier circuits (no device matching or balancing transistors);

transmit and receive filters at baseband;

low frequency synthesizers;

DC offset solutions;

Referring to FIG. **218**A, a single-switch, differential input, differential output receiver **21800**, according to an embodiment of the present invention, is shown. If an I/Q signal is being received, receiver **21800** could be implemented for

each of the I- and Q-phase signals. No balanced transistor is required in receiver **21800**. Any charge injection that creates a DC offset voltage on a first switch input **21802** creates a substantially equal DC offset voltage on a second switch input **21804**, so that any resulting DC offset due to charge injection is substantially canceled.

In an embodiment, LO signal **21806** runs at a sub-harmonic. Gilbert cells lose efficiency when run at a sub-harmonic, as compared to the receiver of the present invention.

FIG. **218**A shows a substantially maximal linearity configuration. The drain and source voltages are virtually fixed in relation to V_{gs}. The DC voltage across first switch input **21802** and second switch input **21804** remains substantially constant.

Single-switch, differential input, differential output receiver embodiments according to the present invention, are discussed in further detail elsewhere herein.

architecturally reduces re-radiation;

Referring to FIG. **218**A, re-radiation is substantially all common mode. With a perfect splitter, the re-radiation will be substantially eliminated.

Referring to FIG. **218**B, a first switch **21810** and a second switch **21812** are implemented in a receiver **21814**, according to an embodiment of the present invention. Receiver **21814** moves re-radiation off frequency to the next even harmonic frequency higher. Referring to FIG. **218**D, re-radiation was substantially shifted from 2.49 GHz (see re-radiation spike **21818**) to 3.29 GHz (see larger re-radiation spike **21820**).

Receiver embodiments, according to the present invention, for reducing or eliminating circuit re-radiation, such as receiver **21814**, are discussed in further detail elsewhere herein.

inherent noise rejection; and

lower cost.

2.5 Fundamental or Sub-Harmonic Operation

Sub-harmonic operation is preferred for many direct down-conversion implementations because it tends to avoid oscillators and/or signals near the desired operating frequency.

Conversion efficiency is generally constant regardless of the sub-harmonic. Sub-harmonic operation enables micro power receiver designs.

2.6 Frequency Multiplication and Signal Gain

A transmit function in accordance with the present invention provides frequency multiplication and signal gain. For example, a 900 MHz design example (0.35μ CMOS) embodiment features −15 dbm 180 MHz LO, 0 dbm 900 MHz I/O output, 5 VDC, 5 ma. A 2400 MHz design example (0.35μ CMOS) embodiment features −15 dbm 800 MHz LO, −6 dbm 2.4 GHz I/O output, 5 VDC, 16 ma.

A transmit function in accordance with the present invention also provides direct up-conversion (true zero IF).

3. Controlled Aperture Sub-Harmonic Matched Filter Features

3.1 Non-Negligible Aperture

A non-negligible aperture, as taught herein, substantially preserves amplitude and phase information, but not necessarily the carrier signal. A general concept is to under-sample the carrier while over sampling the information.

The present invention transfers optimum energy. Example embodiments have been presented herein, including DC examples and carrier half cycle examples.

3.2 Bandwidth

With regard to input bandwidth, optimum energy transfer generally occurs every n+½ cycle. Output bandwidth is generally a function of the LO.

3.3 Architectural Advantages of a Universal Frequency Down-Converter

A universal frequency down-converter (UDF), in accordance with the invention, can be designed to provides, among other things, the following features:

filter Q's of 100,000+;

filters with gain;

filter integration in CMOS;

electrically modified center frequency and bandwidth;

stable filter parameters in the presence of high level signals;

and UDF's can be mass produced without tuning.

3.4 Complimentary FET Switch Advantages

Complimentary FET switch implementations of the invention provide, among other things, increased dynamic range (lower Rds_{on}-increased conversion efficiency, higher IIP2, IIP3, minimal current increase (+CMOS inverter), and lower re-radiation (charge cancellation). For example, refer to FIGS. **240** and **241**.

3.5 Differential Configuration Characteristics

Differential configuration implementations of the invention provide, among other things, DC off-set advantages, lower re-radiation, input and output common mode rejection, and minimal current increase. For example, refer to FIG. **242**.

3.6 Clock Spreading Characteristics

Clock spreading aspects of the invention provide, among other things, lower re-radiation, DC off-set advantages, and flicker noise advantages. For example, refer to FIGS. **243**-**245**.

3.7 Controlled Aperture Sub Harmonic Matched Filter Principles

The invention provides, among other things, optimization of signal to noise ratio subject to maximum energy transfer given a controlled aperture, and maximum energy transfer while preserving information. The invention also provides bandpass wave form auto sampling and pulse energy accumulation

3.8 Effects of Pulse Width Variation

Pulse width can be optimized for a frequency of interest. Generally, pulse width is n plus ½ cycles of a desired input frequency. Generally, in CMOS implementations of the invention, pulse width variation across process variations and temperature of interest is less than +/−16 percent.

4. Conventional Systems

4.1 Heterodyne Systems

Conventional heterodyne systems, in contrast to the present invention, are relatively complex, require multiple RF synthesizers, require management of various electromagnetic modes (shield, etc.), require significant inter-modulation management, and require a myriad of technologies that do not easily integrate onto integrated circuits.

4.2 Mobile Wireless Devices

High quality mobile wireless devices have not been implemented via zero IF because of the high power requirements for the first conversion in order to obtain necessary dynamic range, the high level of LO required (LO re-radiation), adjacent channel interference rejection filtering, transmitter modulation filtering, transmitter LO leakage, and limitations on RF synthesizer performance and technology.

5. Phase Noise Cancellation

The complex phasor notation of a harmonic signal is known from Euler's equation, shown here as equation 172.

$$S(t)=e^{-j(\omega_c t+\phi)} \quad \text{EQ. (172)}$$

Suppose that ϕ is also some function of time $\phi(t)$. $\phi(t)$ represents phase noise or some other phase perturbation of the waveform. Furthermore, suppose that $\phi(t)$ and $-\phi(t)$ can

be derived and manipulated. Then if follows that the multiplication of $S_1(t)$ and $S_2(t)$ will yield equation 173.

$$S(t)=S_1(t)\cdot S_2(t)=e^{-j(\omega_c t+\phi(t))}\cdot e^{-j(\omega_c t-\phi(t))}=e^{-j2\omega_c t} \quad \text{EQ. (173)}$$

Thus, the phase noise $\phi(t)$ can be canceled. Trigonometric identities verify the same result except for an additional term at DC. This can be implemented with, for example, a four-quadrant version of the invention. FIG. **268** illustrates an implementation for a doubler (2× clock frequency and harmonics thereof). FIG. **269** illustrates another implementation (harmonics with odd order phase noise canceling).

In an embodiment two clocks are utilized for phase noise cancellation of odd and even order harmonics by cascading stages. A four quadrant implementation of the invention can be utilized to eliminate the multiplier illustrated in FIG. **269**.

6. Multiplexed UFD

In an embodiment, parallel receivers and transmitters are implemented using single pole, double throw, triple throw, etc., implementations of the invention.

A multiple throw implementation of the invention can also be utilized. In this embodiment, many frequency conversion options at multiple rates can be performed in parallel or serial. This can be implemented for multiple receive functions, multi-band radios, multi-rate filters, etc.

7. Sampling Apertures

Multiple apertures can be utilized to accomplish a variety of effects. For example, FIG. **270** illustrates a bipolar sample aperture and a corresponding sine wave being sampled. The bipolar sample aperture IS operated at a sub harmonic of the sine wave being sampled. By calculating the Pourier transform of each component within the Pourier series, it can be shown that the sampling power spectrum goes to zero at the sub harmonics and super harmonics. As a result, the comb spectrum is substantially eliminated except at the conversion frequency.

Similarly, the number of apertures can be extended with associated bipolar weighting to form a variety of impulse responses and to perform filtering at RF.

8. Diversity Reception and Equalizers

The present invention can be utilized to implement maximal ratio post detection combiners, equal gain post detection combiners, and selectors.

FIG. **271** illustrates an example diversity receiver implemented in accordance with the present invention.

FIG. **272** illustrates an example equalizer implemented in accordance with the present invention.

The present invention can serve as a quadrature down converter and as a unit delay function. In an example of such an implementation, the unit delay function is implemented with a decimated clock at baseband.

VII. CONCLUSIONS

Example embodiments of the methods, systems, and components of the present invention have been described herein. As noted elsewhere, these example embodiments have been described for illustrative purposes only, and are not limiting. Other embodiments are possible and are covered by the invention. Such other embodiments include but are not limited to hardware, software, and software/hardware implementations of the methods, systems, and components of the invention. Such other embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

VIII. GLOSSARY OF TERMS

A.M.	Amplitude Modulation
A/D	Analog/Digital
AWGN	Additive White Gaussian
C	Capacitor
CMOS	Complementary Metal Oxide Semiconductor
dB	Decibel
dBm	Decibels with Respect to One Milliwatt
DC	Direct Current
DCT	Discrete Cosine Transform
DST	Discrete Sine Transform
FIR	Finite Impulse Response
GHz	Giga Hertz
I/Q	In Phase/Quadrature Phase
IC	Integrated Circuits, Initial Conditions
IF	Intermediate Frequency
ISM	Industrial, Scientific, Medical Band
L-C	Inductor-Capacitor
LO	Local Oscillator
NF	Noise Frequency
OFDM	Olihogonal Frequency Division Multiplex
R	Resistor
RF	Radio Frequency
rms	Root Mean Square
SNR	Signal to Noise Ratio
WT"AN	Wireless T "ocal Area Network
UFT	Universal Frequency Translation

What is claimed is:

1. A system for frequency down-converting a modulated carrier signal to a baseband signal, comprising:

a first switch coupled to a first control signal which comprises a sampling aperture with a specified frequency, wherein the first switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal as an output of said first switch during the sampling aperture of the first control signal;

a first energy storage element that stores the transferred energy from the modulated carrier signal and outputs a down-converted in-phase baseband signal portion of said modulated carrier signal;

a second switch coupled to a second control signal which comprises a sampling aperture with a specified frequency, wherein the second switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal as an output of said second switch during the sampling aperture of the second control signal;

a second energy storage element that stores the transferred energy from the modulated carrier signal and outputs a down-converted inverted in-phase baseband signal portion of said modulated carrier signal;

wherein the portions of transferred energy from each of the first and second switch are integrated over time to accumulate said portions of transferred energy from which said down-converted in-phase baseband signal portion and said down-converted inverted in-phase baseband signal portion are derived; and

a first differential amplifier circuit that combines said down-converted in-phase baseband signal portion with said down-converted inverted in-phase baseband signal portion and outputs a first channel down-converted differential in-phase baseband signal.

2. The system of claim **1**, wherein said modulated carrier signal includes an amplitude variation.

3. The system of claim 1, wherein said modulated carrier signal includes a phase variation.

4. The system of claim 1, wherein said modulated carrier signal includes a combination of amplitude variation and phase variation.

5. The system of claim 1, wherein the first switch is on for less than one-half cycle of the modulated carrier signal.

6. The system of claim 1, wherein the second switch is on for approximately one-tenth of a cycle of the modulated carrier signal.

7. The system of claim 1, wherein the apertures of the first and second control signals are defined by a windowing function $u(t)-u(t-T_A)$, where the length of the windowing function aperture is T_A, which is equal to an approximate half cycle of the received carrier signal, $S_i(t)$.

8. The system of claim 1, wherein the first and second control signals each control a charging and discharging cycle of their respective energy storage element by respectively controlling the first and second switching devices so that for each switching device said portion of energy that is distinguishable from noise is transferred to the respective storage element when the switch is on during the charging cycle, and a portion of the transferred energy is discharged during the discharging part of the cycle for each respective switching device when the switching device is off.

9. The system of claim 8, wherein for each respective storage element, the energy discharged during any given discharge cycle is not completely discharged, with the remaining undischarged energy from the given discharge cycle becoming an initial condition for the next charging cycle.

10. The system of claim 8, wherein each said control signal operates at an aliasing rate selected so that energy of the modulated carrier signal is sampled and differentially applied to the respective energy storage element at the frequency of the respective control signal's aperture, and each respective energy storage element outputs, respectively, said differential down-converted in-phase baseband signal portion and said down-converted inverted in-phase baseband signal portion of said modulated carrier signal as a result of the alternate charging and discharging applied to the respective energy storage elements.

11. The system of claim 1, wherein the frequencies of the first and second apertures have periods that are two (2) percent or greater of the modulated carrier signal's period.

12. The system of claim 1, wherein the frequencies of the first and second apertures have periods that are five (5) percent or greater of the modulated carrier signal's period.

13. The system of claim 1, wherein the frequencies of the first and second apertures have periods that are ten (10) percent or greater of the modulated carrier signal's period.

14. The system of claim 1, wherein the frequencies of the first and second apertures have periods that are twelve and a half (12.5) percent or greater of the modulated carrier signal's period.

15. The system of claim 1, further comprising:

a first filter that filters said down-converted in-phase baseband signal portion; and

a second filter that filters said down-converted inverted in-phase baseband signal portion.

16. The system of claim 15, wherein the first and second filters each comprise a low-pass filter.

17. The system of claim 1, wherein said portions of transferred energy from each of the first and second switch which are integrated over time to accumulate said portions of transferred energy are integrated by a separate integration module coupled to the output of each said first and second switch.

18. The system of claim 1, wherein said first and second storage elements are capacitive storage circuits, and wherein said portions of transferred energy from each of the first and second switch which are integrated over time to accumulate said portions of transferred energy are integrated by the capacitive storage circuits as they accumulate charge during successive sampling apertures.

19. The system of claim 1, further comprising:

a third switch coupled to a third control signal which comprises a sampling aperture with a specified frequency, wherein the third switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal as an output of said third switch during the sampling aperture of the third control signal;

a third energy storage element that stores the transferred energy from the modulated carrier signal and outputs a down-converted quadrature-phase baseband signal portion of said modulated carrier signal;

a fourth switch coupled to a fourth control signal which comprises a sampling aperture with a specified frequency, wherein the fourth switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal as an output of said fourth switch during the sampling aperture of the fourth control signal;

a fourth energy storage element that stores the transferred energy from the modulated carrier signal and outputs a down-converted differential quadrature-phase baseband signal portion of said modulated carrier signal;

wherein the portions of transferred energy from each of the third and fourth switch are integrated over time to accumulate said portions of transferred energy from which said down-converted quadrature-phase baseband signal portion and said down-converted differential quadrature-phase baseband signal portion are derived; and

a second differential amplifier circuit that combines said down-converted quadrature-phase baseband signal portion with said down-converted differential quadrature-phase baseband signal portion and outputs a second channel down-converted differential quadrature-phase baseband signal.

20. The system of claim 19, wherein said modulated carrier signal includes an amplitude variation.

21. The system of claim 19, wherein said modulated carrier signal includes a phase variation.

22. The system of claim 19, wherein said modulated carrier signal includes a combination of amplitude variation and phase variation.

23. The system of claim 19, wherein the third switch is on for less than one-half cycle of the modulated carrier signal.

24. The system of claim 19, wherein the fourth switch is on for approximately one-tenth of a cycle of the modulated carrier signal.

25. The system of claim 19, wherein the apertures of the third and fourth control signals are defined by a windowing function $u(t)-u(t-T_A)$, where the length of the windowing function aperture is T_A, which is equal to an approximate half cycle of the received carrier signal, $S_i(t)$.

26. The system of claim 19, wherein the third and fourth control signals each control a charging and discharging cycle of their respective third and fourth energy storage element by respectively controlling the third and fourth switching devices so that for each third and fourth switching device a portion of energy that is distinguishable from noise is transferred to the respective third and fourth storage element when the respective switch is on during the charging cycle, and a portion of the transferred energy is discharged during the

discharging part of the cycle for each respective third and fourth switching device when the respective switching device is off.

27. The system of claim **26**, wherein for each respective energy storage element, the energy discharged during any given discharge cycle is not completely discharged, with the remaining undischarged energy from the given discharge cycle becoming an initial condition for the next charging cycle.

28. The system of claim **26**, wherein each said third and fourth control signal operates at an aliasing rate selected so that energy of the modulated carrier signal is sampled and differentially applied to the respective energy storage element at the frequency of the respective third and fourth control signal's aperture, and each respective third and fourth energy storage element generates, respectively, said differential down-converted in-phase baseband signal portion and said down-converted inverted in-phase baseband signal portion of said modulated carrier signal from the alternate charging and discharging applied to the respective energy storage elements.

29. The system of claim **19**, wherein the frequencies of the third and fourth apertures have periods that are two (2) percent or greater of the modulated carrier signal's period.

30. The system of claim **19**, wherein the frequencies of the third and fourth apertures have periods that are five (5) percent or greater of the modulated carrier signal's period.

31. The system of claim **19**, wherein the frequencies of the third and fourth apertures have periods that are ten (10) percent or greater of the modulated carrier signal's period.

32. The system of claim **19**, wherein the frequencies of the third and fourth apertures have periods that are twelve and a half (12.5) percent or greater of the modulated carrier signal's period.

33. The system of claim **19**, further comprising:

a first filter that filters said down-converted in-phase baseband signal portion;

a second filter that filters said down-converted inverted in-phase baseband signal portion;

a third filter that filters said down-converted quadrature-phase baseband signal portion;

a fourth filter that filters said down-converted inverted quadrature-phase baseband signal portion.

34. The system of claim **33**, wherein the first, second, third, and fourth filters each comprise a low-pass filter.

35. The system of claim **19**, wherein said portions of transferred energy from each of the first, second, third and fourth switch which are integrated over time to accumulate said portions of transferred energy are integrated by a separate integration module coupled to the output of each said first, second, third and fourth switch respectively.

36. The system of claim **19**, wherein said first, second, third and fourth storage elements are capacitive storage circuits, and wherein said portions of transferred energy from each of the first, second, third and fourth switch which are integrated over time to accumulate said portions of transferred energy are integrated by the capacitive storage circuits of the respective first, second, third and fourth storage elements as they accumulate charge during successive sampling apertures.

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