$$H(s)=\frac{V_0(s)}{V_i(s)}=RC^{-1}\cdot\left(\frac{1-e^{-sT_A}}{s}\right)\cdot\left(\frac{1}{s+(RC)^{-1}}\right) \qquad \text{EQ. (33)}$$

$$\therefore h(t)=\left(\frac{e^{-\frac{t}{RC}}}{RC}\right)[u(t)-u(t-T_A)] \qquad \text{EQ. (34)}$$

Suppose that $V_i(t)=A\sin\left(2\pi\frac{f_A}{2}t+\phi\right)$, as illustrated in FIG. 166, where $f_A = T_A^{-1}$ and ϕ is an arbitrary phase shift. (FIG. 166 also shows h(t).) Note in FIG. 166 that h(t) is not ideally a sine pulse. However, the cross correlation of h(t) and $V_i(t)$ can still be quite good if RC is properly selected. This is the optimization, which is required in order to approximate a matched filter result (namely SNR optimization given h(t) and $V_i(t)$).

$$V_0(t)=V_i(t)*h(t)=A\sin(\pi f_A t)*h(t)\ ;0\le t\le T_A \qquad \text{EQ. (35)}$$

$$V_0(t)=\int_0^{\infty}\sin(\pi f_A(t-\tau))\frac{e^{\frac{-\tau}{RC}}}{RC}\,d\tau \qquad \text{EQ. (36)}$$

By a change of variables;

$$V_0(t)=\int_{-\infty}^{t}A\sin(\pi f_A\tau+\phi)\cdot\frac{e^{\frac{-(t-\tau)}{RC}}}{RC}\,[u(t-\tau)-u(t-\tau-T_A)]d\tau$$

where $f_A \underline{\Delta} 2f = T_A^{-1}$ EQ. (37)

$$\therefore V_0(t)=\frac{A}{1+(\pi f_A RC)^2}(-\pi f_A t+\phi)+\sin(\pi f_A t+\phi)-Ae^{-t/RC}\left(\sin\phi-\frac{(\pi f_A RC)^2}{1+(\pi f_A RC)^2}\cdot\sin\phi-\frac{\pi f_A RC}{1+(\pi f_A RC)^2}\cdot\cos\phi\right)$$

$0\le t\le T_A$

$$V_0(t)=\left[\frac{1}{1+(RC\pi f_A)^2}\right]\left(\sin(\pi f_A t)-\pi f_A RC\cdot\cos(\pi f_A t)+\pi f_A RC\cdot e^{-t/RC}\right)0\le t\le T_A$$

, $\phi = 0$

Notice that the differential equation solution provides for carrier phase skew, ϕ. It is not necessary to calculate the convolution beyond T_A since the gating function restricts the impulse response length.

FIG. 167 illustrates the response $V_0(t)$. The output peaks just before T_A because the example RC processor is not a perfect matched filtering/correlating processor, but rather an approximation. FIG. 168 illustrates that the maximum of the function occurs at $t \cong .75T_A$, for a $\beta = 2.6$, which can be verified by evaluating:

$$\frac{\partial}{\partial t}V_0(t)=0 \qquad \text{EQ. (38)}$$

Solving the differential equation for $V_0(t)$ permits an optimization of $\beta = (RC)^{-1}$ for maximization of V_0.

FIG. 169 illustrates a spread of values for beta. In embodiments, the peak β occurs at approximately $\beta \cong 2.6$. FIG. 169 illustrates a family of output responses for processors according to embodiments of the present invention having different beta values. In embodiments, the definition used for optimality to obtain $\beta = 2.6$ is the highest value of signal obtained at the cutoff instant, T_A. Other criteria can be applied, particularly for multiple pulse accumulation and SNR consideration.

In embodiments, one might be tempted to increase β and cutoff earlier (i.e., arbitrarily reduce T_A). However, this does not necessarily always lead to enhanced SNR, and it reduces charge transfer in the process. It can also create impedance matching concerns, and possibly make it necessary to have a high-speed buffer. That is, reducing T_A and C is shown

below to decrease SNR. Nevertheless, some gain might be achieved by reducing T_A to .75 for $\beta = 2.6$, if maximum voltage is the goal.

In embodiments, in order to maximize SNR, consider the following. The power in white noise can be found from:

$$\sigma^2 = N_0 \int_0^{\infty} h^2(\lambda) d\lambda \qquad \text{EQ. (39)}$$

$$\sigma^2 = N_0 \int_0^{\infty} \left(\frac{e^{-2\lambda / RC^2}}{RC} \right) \left(u(t) - u(\lambda - T_A) \right) \, d\lambda \qquad \text{EQ. (40)}$$

$$\sigma^2 = \frac{\beta N_0 \left(1 - e^{-2\beta N_0 T_A} \right)}{2} \; @T_A \qquad \text{EQ. (41)}$$

$$\beta = (RC)^{-1}$$

Notice that σ^2 is a function of RC.

The signal power is calculated from:

$$(V_0(t))^2 = \left(\frac{1}{1 + (\beta^{-1} \pi f_A)^2} \right)^2 \left(\sin(\pi f_A t) - \beta^{-1} \pi f_A \cdot \cos(\pi f_A t) + \beta^{-1} \pi f_A e^{-\beta t} \right)^2$$

EQ. (42)

Hence, the SNR at T_A is given by:

$$\frac{(V_0(t))^2}{\sigma^2} \Big|_{t=T_A} = \frac{2}{\beta N_0 \left(1 - e^{-2\beta N_0 T_A} \right)} \left(\frac{1}{1 + (\beta^{-1} \pi f_A)^2} \right)^2 \left(\beta^{-1} \pi f_A + \beta^{-1} \pi f_A e^{-\beta T_A} \right)^2$$

EQ. (43)

Maximizing the SNR requires solving:

$$\frac{\partial}{\partial \beta} \left(\frac{V_0(t)^2}{\sigma^2} \right) = 0 \qquad \text{EQ. (44)}$$

Solving the SNR_{max} numerically yields β values that are ever decreasing but with a diminishing rate of return.

As can be seen in FIG. 170, in embodiments, $\beta = 2.6$ for the maximum voltage response, which corresponds to a normalized SNR relative to an ideal matched filter of 0.431. However, in embodiments, selecting a β of $1/10$ the β, which optimizes voltage, produces a superior normalized SNR of 0.805 (about 80.5% efficiency) This is a gain in SNR performance of about 2.7dB.

In certain embodiments, it turns out that for an ideal matched filter the optimum sampling point corresponding to correlator peak is precisely T_A. However, in embodiments, for the RC processor, the peak output of occurs at approximately 0.75 T_A for large β (i.e., $\beta = 2.6$). That is because the impulse response is not perfectly matched to the carrier signal. However, as β is reduced significantly, the RC processor response approaches the efficiency of the finite time integrating processor response in terms of SNR performance. As β is lowered, the optimal SNR point occurs closer to T_A, which simplifies design greatly. Embodiments of the present invention provides excellent energy accumulation over T_A for low β, particularly when simplicity is valued.

5.1 Charge Transfer and Correlation

The basic equation for charge transfer is:

$$\frac{dq}{dt} = C\frac{dv}{dt}, \text{ (assuming C constant over time)} \qquad \text{EQ. (45)}$$

$$q = CV$$

Similarly the energy u stored by a capacitor can be found from:

$$u = \int_0^q \frac{q_x}{C}\, dq_x = \frac{q^2}{2C} \qquad \text{EQ. (46)}$$

From EQs. (45) and (46):

$$u = \frac{Cv^2}{2} \qquad \text{EQ. (47)}$$

Thus, the charge stored by a capacitor is proportional to the voltage across the capacitor, and the energy stored by the capacitor is proportional to the square of the charge or the voltage. Hence, by transferring charge, voltage and energy are also transferred. If little charge is transferred, little energy is transferred, and a proportionally small voltage results unless C is lowered.

The law of conversation of charge is an extension of the law of the conservation of energy. EQ. (45) illustrates that if a finite amount of charge must be transferred in an infinitesimally short amount of time then the voltage, and hence voltage squared, tends toward infinity. The situation becomes even more troubling when resistance is added to the equation. Furthermore,

$$V_c = \frac{1}{C}\int_0^{T_A} idt \qquad \text{EQ. (48)}$$

This implies an infinite amount of current must be supplied to create the infinite voltage if T_A is infinitesimally small. Clearly, such a situation is impractical, especially for a device without gain.

In most radio systems, the antenna produces a small amount of power available for the first conversion, even with amplification from an LNA. Hence, if a finite voltage and current restriction do apply to the front end of a radio then a conversion device, which is an impulse sampler, must by definition possess infinite gain. This would not be practical for a switch. What is usually approximated in practice is a fast sample time, charging a small capacitor, then holding the value acquired by a hold amplifier, which

preserves the voltage from sample to sample.

The analysis that follows shows that given a finite amount of time for energy transfer through a conversion device, the impulse response of the ideal processor, which transfers energy to a capacitor when the input voltage source is a sinusoidal carrier and possesses a finite source impedance, is represented by embodiments of the present invention. If a significant amount of energy can be transferred in the sampling process then the tolerance on the charging capacitor can be reduced, and the requirement for a hold amplifier is significantly reduced or even eliminated.

In embodiments, the maximum amount of energy available over a half sine pulse can be found from:

$$u = \int_0^{T_A} S_i^2(t)dt = \frac{A^2 T_A}{2} \qquad \text{EQ. (49)}$$

This points to a correlation processor or matched filter processor. If energy is of interest then a useful processor, which transfers all of the half sine energy, is revealed in EQ. (48), where T_A is an aperture equivalent to the half sine pulse. In embodiments, EQ. (49) provides the clue to an optimal processor.

Consider the following equation sequence.

$$\int_0^{\infty} h(\tau)S_i(t-\tau)d\tau \Rightarrow \int_0^{T_A} kS_i^2(T_A-\tau)d\tau \Rightarrow \int_{-0}^{T_A} S_i^2(t)dt$$

EQ. (50)

where $h(\vartheta) = S_i(T_A - \vartheta)$ and $t = T_A - \vartheta$.

This is the matched filter equation with the far most right hand side revealing a correlator implementation, which is obtained by a change of variables as indicated. The matched filter proof for $h(\tau) = S_i(T_A - \tau)$ is provided in sub-section 8.4 below. Note that the correlator form of the matched filter is exactly a statement of the desired signal energy. Therefore a matched filter/correlator accomplishes acquisition of all the energy

available across a finite duration aperture. Such a matched filter/correlator can be implemented as shown in FIG. 171.

In embodiments, when optimally configured, the example matched filter/correlator of FIG. 171 operates in synchronism with the half sine pulse $S_i(t)$ over the aperture T_A. Phase skewing and phase roll will occur for clock frequencies, which are imprecise. Such imprecision can be compensated for by a carrier recovery loop, such as a Costas Loop. A Costas Loop can develop the control for the acquisition clock, which also serves as a sub-harmonic carrier. However, phase skew and non-conherency does not invalidate the optimal form of the processor provided that the frequency or phase errors are small, relative to T^{-1}_A. Non-coherent and differentially coherent processors may extract energy from both I and Q with a complex correlation operation followed by a rectifier or phase calculator. It has been shown that phase skew does not alter the optimum SNR processor formulation. The energy which is not transferred to I is transferred to Q and vice versa when phase skew exists. This is an example processor for a finite duration sample window with finite gain sampling function, where energy or charge is the desired output.

A matched filter/correlator embodiment according to the present invention might be too expensive and complicated to build for some applications. In such cases, however, other processes and processors according to embodiments of the invention can be used. The approximation to the matched filter/correlator embodiment shown in FIG. 172 is just one embodiment that can be used in such instances. The finite time integrator embodiment of FIG. 172 requires only a switch and an integrator. Sub-section 6 below shows that this embodiment of the present invention has only a 0.91dB difference in SNR compared to the matched filter/correlator embodiment.

Another very low cost and easy to build embodiment of the present invention is the RC processor. This embodiment, shown in FIG. 173, utilizes a very low cost integrator or capacitor as a memory across the aperture. If C is suitable chosen for this embodiment, its performance approaches that of the matched filter/correlator embodiment, shown in FIG. 171. Notice the inclusion of the source impedance, R, along with the switch and capacitor. This simple embodiment nevertheless can approximate the optimum energy transfer of the matched filter/correlator embodiment if properly designed.

When maximum charge is transferred, the voltage across the capacitor 17304 in FIG. 173 is maximized over the aperture period for a specific RC combination.

Using EQs. (45) and (48) yields:

$$q = C \cdot \frac{1}{C} \int_0^{T_A} i_c dt \qquad \text{EQ. (51)}$$

If it is accepted that an infinite amplitude impulse with zero time duration is not available or practical, due to physical parameters of capacitors like ESR, inductance and breakdown voltages, as well as currents, then EQ. (51) reveals the following important considerations for embodiments of the invention:

- The transferred charge, q, is influenced by the amount of time available for transferring the charge;
- The transferred charge, q, is proportional to the current available for charging the energy storage device; and
- Maximization of charge, q, is a function of i_c, C, and T_A.

Therefore, it can be shown that for embodiments:

$$q_{max} = Cv_{max} = C\left[\frac{1}{C}\int_0^{T_A} i_c dt\right]_{max} \qquad \text{(EQ. 52)}$$

The impulse response for the RC processing network was found in sub-section 5.2 below to be;

$$h(t) = \frac{e^{\frac{-\tau}{RC}}}{RC}\left[u(\tau) - u(\tau - T_A)\right] \qquad \text{EQ. (53)}$$

Suppose that T_A is constrained to be less than or equal to $^1/_2$ cycle of the carrier period. Then, for a synchronous forcing function, the voltage across a capacitor is given by EQ. (54).

$$V_0(t) = \int_{-\infty}^{t} \sin(\pi f_A \tau) \cdot \frac{e^{\frac{-(t-\tau)}{RC}}}{RC}\, d\tau \qquad \text{EQ. (54)}$$

Maximizing the charge, q, requires maximizing EQ. (37) with respect to t and β.

$$\frac{\partial^2 V_0(t)}{\partial t\ \partial \beta} = 0 \qquad \text{EQ. (55)}$$

It is easier, however, to set R = 1, T_A = 1, A =1, $f_A = T_A^{-1}$ and then calculate $q = cV_0$ from the previous equations by recognizing that $q = \frac{\beta^{-1}}{R}\ V_0 = cV_0$, which produces a normalized response.

FIG. 174 illustrates that increasing C is preferred in embodiments of the invention. It can be seen in FIG. 174 that as C increases (i.e., as $\exists$ decreases) the charge transfer also increases. This is what is to be expected based on the optimum SNR solution. Hence, for embodiments of the present invention, an optimal SNR design results in optimal charge transfer. As C is increased, bandwidth considerations should be taken into account.

In embodiments, EQ. (49) establishes T_A as the entire half sine for an optimal processor. However, in embodiments, optimizing jointly for t and β reveals that the RC processor response creates an output across the energy storage capacitor that peaks for $t_{max} \cong .75T_A$, and $\beta_{max} \cong 2.6$, when the forcing function to the network is a half sine pulse.

In embodiments, if the capacitor of the RC processor embodiment is replaced by an ideal integrator then $t_{max} \rightarrow T_A$.

$$\beta\, T_A \simeq 1.95 \qquad \text{EQ. (56)}$$

where $\exists = (RC)^{-1}$

For example, for a 2.45 GHz signal and a source impedance of 50 Ω, EQ. (56) above suggests the use of a capacitor of ≅ 2pf. This is the value of capacitor for the aperture selected, which permits the optimum voltage peak for a single pulse accumulation. For practical realization of the present invention, the capacitance calculated by EQ. (56) is a minimum capacitance. SNR is not considered optimized at $\beta\, T_A \simeq 1.95$. As shown earlier, a smaller β yields better SNR and better charge transfer. In embodiments, as discussed below, it turns out that charge can also be optimized if multiple apertures are used for collecting the charge.

In embodiments, for the ideal matched filter/correlator approximation, βT_A is constant and equivalent for both consideration of optimum SNR and optimum charge transfer, and charge is accumulated over many apertures for most practical designs. Consider the following example, β = .25, and $T_A = 1$.

Thus $\beta\, T_A = .25$. At 2.45 GHz, with R =50Ω, C can be calculated from:

$$C \geqq \frac{T_A}{R(.25)} \geq 16.3\,pf \qquad \text{EQ. (57)}$$

The charge accumulates over several apertures, and SNR is simultaneously optimized melding the best of two features of the present invention. Checking CV for $\beta T_A \simeq 1.95$ vs. $\beta T_A = .25$ confirms that charge is optimized for the latter.

5.2 Load Resistor Consideration

The general forms of the differential equation and transfer function, described above, for embodiments of the present invention are the same as for a case involving a load resistor, R_L, applied across capacitor, C. FIG. 175A illustrates an example RC processor embodiment 17502 of the present invention having a load resistance 17504 across a capacitance 17506.

Consider RC processing embodiment 17502 (without initial conditions).

EQ. (33) becomes:

$$H(s) = \frac{1 - e^{-sT_A}}{s}\left(\frac{1}{sCR + k}\right) \qquad \text{EQ. (58)}$$

$$k = \left(R/R_L + 1\right) \qquad \text{EQ. (59)}$$

$$h(t) = \left(\frac{e^{-\frac{t \cdot k}{RC}}}{RC}\right)\left[u(t) - (t - T_A)\right] \qquad \text{EQ. (60)}$$

It should be clear that R_L 17504,and therefore k, accelerate the exponential decay cycle.

$$V_0(t) = \int_{-\infty}^{t} \sin(\pi f_a \tau) \cdot \frac{e^{-\frac{k(t-\tau)}{RC}}}{RC} \, d\tau \qquad \text{EQ. (61)}$$

$$V_0(t) = \left(\frac{1}{k^2 + (\pi f_A)^2}\right)\left[k \cdot \sin(\pi f_A t) - \pi f_A RC \cdot \cos(\pi f_A t) + RCe^{-\frac{kt}{RC}}\right] \quad 0 \le t \le T_A$$

EQ.(62)

This result is valid only over the acquisition aperture. After the switch is opened, the final voltage that occurred at the sampling instance $t \cong T_A$ becomes an initial condition for a discharge cycle across R_L 17504. The discharge cycle possesses the following response:

$$V_D = \frac{V_A \cdot e^{-\frac{t}{R_L C}}}{R_L C} u(t - T_A) \textit{ (single event discharge)}$$

EQ. (63)

V_A is defined as $V_0(t \cong T_A)$. Of course, if the capacitor 17506 does not completely discharge, there is an initial condition present for the next acquisition cycle.

FIG. 175B illustrates an example implementation of the invention, modeled as a switch S, a capacitor C_S, and a load resistance R. FIG. 175D illustrates example energy transfer pulses, having apertures A, for controlling the switch S. FIG. 175C illustrates an example charge/discharge timing diagram for the capacitor C_S, where the capacitor C_S charges during the apertures A, and discharge between the apertures A.

Equations 63.1 through 63.15 derive a relationship between the capacitance of the capacitor C_S ($C_S(R)$), the resistance of the resistor R, the duration of the aperture A (aperture width), and the frequency of the energy transfer pulses (freq LO). Equation 63.11 illustrates that optimum energy transfer occurs when x = 0.841. Based on the disclosure herein, one skilled

in the relevant art(s) will realize that values other that 0.841 can be utilized.

$$\phi = \frac{1}{C}\int i(t)\partial t + Ri(t) \qquad \text{EQ. (63.1)}$$

$$\frac{\partial}{\partial t}\phi = \frac{\partial}{\partial t}\left[\frac{1}{C}\int i(t)\partial t + Ri(t)\right] \qquad \text{EQ. (63.2)}$$

$$\phi = \frac{i(t)}{C_s} + \frac{R\partial i(t)}{\partial t} \qquad \text{EQ. (63.3)}$$

$$\phi = \frac{1}{C_s} + R \cdot s \qquad \text{EQ. (63.4)}$$

$$s = \frac{-1}{C_s \cdot R}, \text{ by definition: } i_{init}(t) = \frac{V_{C_s} init}{R} \qquad \text{EQ. (63.5)}$$

$$i(t) = \left(\frac{V_{C_s} init}{R}\right) \cdot e^{\left(\frac{-t}{C_s \cdot R}\right)} \qquad \text{EQ. (63.6)}$$

$$V_{out}(t) = R \cdot i(t) = V_{C_s} init \cdot e\left(\frac{-t}{C_s \cdot R}\right) \qquad \text{EQ. (63.7)}$$

Maximum power transfer occurs when:

$$Power_Final = \frac{1}{\sqrt{2}} \cdot Peak_Power \qquad \text{EQ. (63.8)}$$

$$Power_Peak = \frac{\left(V_{C_s} peak\right)^2}{R}$$ EQ. (63.9)

$$Power_Final = \frac{\left(x \cdot V_{C_s} peak\right)^2}{R}$$ EQ. (63.10)

$$\frac{\left(x \cdot V_{C_s} peak\right)^2}{R} = \frac{\left(V_{C_s} peak\right)^2}{R} \cdot \frac{1}{\sqrt{2}}$$ yields x = 0.841 EQ. (63.11)

Let V_{Cs}init = 1, then $V_{out}(t)$ =0.841 when

$$t = \frac{1}{freqLO} - Aperture_Width.$$ EQ. (63.12)

$$0.841 = 1 \cdot e^{\left(\frac{\frac{1}{freqLO} - Aperture_Width}{C_s \cdot R}\right)}$$ EQ. (63.13)

$$\ln(0.841) = \left(\frac{\frac{1}{freqLO} - Aperture_Width}{C_s \cdot R}\right)$$ EQ. (63.14)

$$C_s(R) = \left(\frac{\frac{1}{freqLO} - Aperture_Width}{-\ln(0.841) \cdot R}\right)$$ EQ. (63.15)

6. Signal-To-Noise Ratio Comparison of the Various Embodiments

The prior sub-sections described the basic SNR definition and the SNR of an optimal matched filter/correlator processor according to embodiments of the present invention. This sub-section section describes the SNR of additional processor embodiments of the present invention and compares their SNR with the SNR of a optimal matched filter/correlator embodiment. The description in this sub-section is based on calculations relating to single apertures and not accumulations of multiple aperture averages. Since SNR is a relative metric, this method is useful for comparing different embodiments of the present invention.

EQ. (65), which can be obtained from EQ. (64), represents the output SNR for a single aperture embodiment assuming a constant envelope sine wave input. The results could modify according to the auto-correlation function of the input process, however, over a single carrier half cycle, this relationship is exact.

$$SNR_{opt} \Delta \frac{1}{N_0} \int_0^{\infty} S_i^2(t_0 - \tau)\ d\tau \qquad \text{EQ. (64)}$$

$$SNR_{opt} \Delta \frac{T_A A^2}{2N_0} \quad \text{(single aperture case)} \qquad \text{EQ. (65)}$$

The description that follows illustrates the SNR for three processor embodiments of the present invention for a given input waveform. These embodiments are:

- An Example Optimal Matched Filter/Correlator Processor Embodiment;
- An Example Finite Time Integrator processor Embodiment; and
- An Example RC Processor Embodiment

The relative value of the SNR of these three embodiments is accurate for purposes of comparing the embodiments. The absolute SNR may be

adjusted according to the statistic and modulation of the input process and its complex envelope.

Consider an example finite time integrator processor, such as the one illustrated in FIG. 164B. The impulse response of the finite time integrator processor is given by EQ. (66):

$$h(t) = k, \ 0 \le t \le T_A \qquad \text{EQ. (66)}$$

where k is defined as an arbitrary constant.

The output of the finite time integrator processor, $y(t)$, is found from the input, $x(t)$, using:

$$y(t) = \int_{t-T_A}^{t} x(u) \ du \qquad \text{EQ. (67)}$$

A change of variables yields EQ. (68):

$$y(t-\tau) = \int_{t-\tau-T_A}^{t-\tau} x(v) \ dv \qquad \text{EQ. (68)}$$

The output auto correlation then becomes that shown in EQ. (69):

$$R_y(\tau) = \int_{t-T_A}^{t} du \int_{t-\tau-T_A}^{t-\tau} R_x(u-v) \ dv \qquad \text{EQ. (69)}$$

which leads to:

$$R_x(u-v) = \frac{1}{2\pi} \int_{-\infty}^{\infty} S_x(\omega) \ e^{j\omega(u-v)} d\omega \qquad \text{EQ. (70)}$$

This Fourier transform may be substituted into the expression for $R_y(\tau)$, in EQ. (71), which becomes:

$$R_y(\tau) = \frac{1}{2\pi}\int_{-\infty}^{\infty} S_x(\omega)d\omega \int_{t-T_A}^{t} e^{S\omega u} du \int_{t-\tau-T_A}^{t-\tau} e^{-j\omega v} dv \qquad \text{EQ. (71)}$$

$$R_y(\tau) = \frac{1}{2\pi}\int_{-\infty}^{\infty} S_x(\omega)\left[\frac{e^{j\omega t}\left(1-e^{-j\omega T_A}\right)}{j\omega}\right]\left[\frac{e^{-j\omega(t-\tau)}\left(1-e^{-j\omega T_A}\right)}{j\omega}\right] d\omega$$

EQ. (72)

$$\therefore\ S_y(\omega) = S_x(\omega)\frac{\sin^2 \omega T_A/2}{(\omega/2)^2} \qquad \text{EQ. (73)}$$

$S_y(\omega)$ is the power spectral density at the output of the example finite time integrator, whose integration aperture is T_A and whose input power spectrum is defined by $S_x(\omega)$. For the case of wide band noise:

$$S_{yn}(\omega) = \frac{N_0}{2\pi}\frac{\sin^2 \omega T_A/2}{(\omega/2)^2} \qquad \text{EQ. (74)}$$

The total noise power across the band can be found from EQ. (75):

$$\int_{-\infty}^{\infty} S_{yn}(\omega)d\omega = \frac{N_0}{2\pi}\int_{-\infty}^{\infty}\frac{\sin^2(\omega T_A/2)}{(\omega/2)^2}\ d\omega = T_A N_0 \qquad \text{EQ. (75)}$$

This result can be verified by EQ. (76):

$$\overline{Y^2} = N_0\int_0^{\infty} h^2(\tau)\ d\tau \qquad \text{EQ. (76)}$$

The signal power over a single aperture is obtained by EQ. (77):

$$y(t)^2 = \left(2A\int_0^{T_A/2}\sin(\omega t)dt\right)^2 \qquad \text{EQ. (77)}$$

Choosing A = 1, the finite time integrator output SNR becomes:

$$SNR_{\text{int}} = \frac{4T_A}{\pi^2 N_0} \qquad \text{EQ. (78)}$$

An example RC filter can also be used to model an embodiment of

the present invention. The mean squared output of a linear system may be found from EQ. (79):

$$\overline{Y^2} = \int_0^\infty d\tau_1 \int_0^\infty R_x(\tau_A - \tau_1) h(\tau_1) h(\tau_2)\ d\tau_2 \quad \text{EQ. (79)}$$

For the case of input AWGN:

$$R_{xn}(\tau) = N_0 \delta(\tau) \quad \text{EQ. (80)}$$

$$\overline{Y^2} = N_0 \int_0^\infty d\tau_1 \int_0^\infty \delta(\tau_2 - \tau_1) h(\tau_1) h(\tau_2)\ d\tau_2 \quad \text{EQ. (81)}$$

$$\overline{Y_n^2} = N_0 \int_0^\infty h^2(\tau)\ d\tau \quad \text{EQ. (82)}$$

This leads to the result in EQ. (83):

$$H(s) = \frac{1/RC}{s + 1/RC} * \left(\frac{1 - e^{-sT_A}}{s} \right) \quad \text{EQ. (83)}$$

R is the resistor associated with processor source, and C is the energy storage capacitor.

Therefore;

$$h(t) = \frac{1}{RC} e^{-t/RC} \left(u(t) - u(t - T_A) \right) \quad \text{EQ. (84)}$$

And finally:

$$\overline{Y_n^2} = \frac{N_0}{2RC} \left(1 - e^{-\left(2N_0 T_A / RC\right)} \right) \quad \text{EQ. (85)}$$

The detailed derivation for the signal voltage at the output to the RC filter is provided in sub-section 5 above. The use of the β parameter is also described in sub-section 5. Hence, the SNR_{RC} is given by:

$$SNR_{RC} = \frac{2(V_0(t_s))^2}{\beta N_0} \quad T_A = 1, \quad A = 1 \qquad \text{EQ. (86)}$$

Illustrative SNR performance values of the three example processor embodiments of the present invention are summarized in the table below:

Example Matched Filter Performance of an	Performance Relative to the Optimal Matched Filter Embodiment
$SNR_{MF} = \frac{T_A}{2N_0}$	0dB
Example Integrator Approximate	
$SNR_{INT} = \frac{4T_A}{\pi^2 N_0}$	-.91dB
Example RC Approximate (3 example cases for reference)	
$SNR_{RC} = \frac{V_0(t)^2 \cdot 2}{\beta N_0} \cong \frac{.2142}{N_0}$	-3.7dB, at $T_A = 1$, $\beta = 2.6$
$SNR_{RC} \cong \frac{.377}{N_0}$	-1.2dB, at $T_A = .75$, $\beta = 2.6$
$SNR_{RC} \cong \frac{.405}{N_0}$	-.91dB at $T_A = 1$, $\beta \leq .25$

Notice that as the capacitor becomes larger, the RC processor behaves like a finite time integrator and approximates its performance. As described above in sub-section 5, with a β of 0.25, a carrier signal of 2450 MHz, and R = 50Ω, the value for C becomes $C \geq 16.3pf$.

FIG. 176 illustrates the output voltage waveforms for all three processor embodiments. (Note that two curves are shown for the RC correlator processor, $\exists$ = 2.6 and $\exists$ =0.25). FIG. 177A illustrates the relative SNR's over the aperture.

6.2 Carrier Offset and Phase Skew Characteristics of Embodiments of the Present Invention

FIG. 177B illustrates some basic matched filter waveforms that are common to some communications applications. The first waveform 17750 is a baseband rect function. Since this waveform is symmetric it is easy to visualize the time reversed waveform corresponding to the ideal matched filter impulse response, $h(t)$, which is also a rect function:

$$h(t) * S_i(t-\tau)\int_{t_1}^{t_2} S_i(t-\tau)h(t)dt \qquad \text{EQ. (86.1)}$$

The second waveform 17760 illustrates the same rect function envelope at passband (RF) and it's matched filter impulse response. Notice the sine function phase reversal corresponding to the required time axis flip. FIG. 177C shows a waveform 17770. Waveform 17770 is a single half sine pulse whose time reversed representation is identical. This last impulse response would be optimal but as pointed out earlier may be difficult to implement exactly. Fortunately, an exact replica is not required.

FIG. 177D illustrates some exemplary approaches for a complex matched filter/correlator processor applied to a variety of waveforms. As shown in FIG. 177D, approaches 17780 and 17785 are classical ways to producing a complex matched filter/correlator processor. FIG. 177E shows approach 17790. Approach 17790 shows one embodiment of a complex matched filter/correlator processor implemented with the UFT as the processor. The only difference in the UFT approach 17790 is the duration of the pulse envelope. The fact that the gating pulse is small compared to other applications for a correlator is of little consequence to the complex baseband processor. When there is no phase skew then all of the correlated energy is transferred to the I output. When there is a phase skew then a portion of the aliased down converted energy is transferred to the I output and the remainder to the Q. All of the correlated energy is still available, in its optimally filtered form, for final processing in the BB processor.

The fact that a non-coherent processor is used or a differentially coherent BB processor used in lieu of a coherent Costas Loop in no way diminishes the contribution of the UFT correlator effect obtained by selecting the optimal aperture T_A based on matched filter theory.

Consider FIG. 177E which illustrates an aperture with a phase shifted sine function. In addition, a derivation is provided which indicates that the aperture with phase skew, as referenced to the half sine function, can be represented by the fundamental correlator kernel multiplied by a constant. This provides insight into the interesting SNR properties of the UFT which are based on matched filter principles over the aperture regardless of phase skew ϕ.

Moreover, Section IV, part 5.1 above illustrates that a complex UFT downconverter which utilizes a bandpass filter actually resembles the optimal matched filter/correlator kernel in complex form with the in phase result scaled by $\cos\phi$ and the quadrature phase component scaled by $\sin\phi$. This process preserves all the energy of the downconverter signal envelope (minus system loses) with a part of the energy in I and the remainder in Q.

7. Multiple Aperture Embodiments of the Present Invention

The above sub-sections describe single aperture embodiments of the present invention. That is, the above sub-sections describe the acquisition of single half sine waves according to embodiments of the invention. Other embodiments of the present invention are also possible, however, and the present invention can be extended to other waveform partitions that capture multiple half sine waves. For example, capturing two half sine waves provides twice the energy compared to capturing only a single half sine. Capturing n half sines provides n times the energy, et cetera, until sub harmonic sampling is no longer applicable. The invention is directed to other embodiments as well. Of course, the matched filter waveform requires a different correlating aperture for each new n. This aspect of the present invention is illustrated in FIGS. 178A and 178B.

In the example of FIG. 178B, the sample aperture window is twice as long as the examples in the previous sub-sections. The matched filter impulse response in FIG. 178B is bipolar to accommodate a full sine cycle. The embodiment of this example can be implemented, for example, with a rectangular bipolar function (Haar's Wavelet) gating device.

Fourier transforming the components for the example processor yields the results shown in FIG. 179 and EQ. (87).

$$S(f) \cong \sum_{n=-\infty}^{\infty} \frac{Af_sT_A}{2}\left[\frac{\sin(\pi(nf_s - Nf_s)T_A)}{(\pi(nf_s - Nf_s)T_A)} + \frac{\sin(\pi nf_s + Nf_s)T_A}{(\pi(nf_s + Nf_s)T_A)}\right]\delta(f - nf_s)$$

EQ. (87)

The transform of the periodic, sampled, signal is first given a Fourier series representation (since the Fourier transform of a power signal does not exist in strict mathematical sense) and each term in the series is transformed sequentially to produce the result illustrated. Notice that outside of the desired main lobe aperture response that certain harmonics are nulled by the (sinx)/x response. Even those harmonics, which are not completely nulled, are reduced by the side lobe attenuation. Some sub-harmonics and super-harmonics are eliminated or attenuated by the frequency domain nulls and side lobes of the bipolar matched filter/correlator processor, which is a remarkable result.

Theoretically, arbitrary impulse responses may be constructed in the manner above, particularly if weighting is applied across the aperture or if multiple apertures are utilized to create a specific Fourier response. FIR filters and convolvers may be constructed by extending the aperture and utilizing the appropriate weighting factors. Likewise, disjoint or staggered apertures may be constructed to provide a particular desired impulse response. These apertures can be rearranged and tuned 'on the fly'.

FIG. 180 (I/Q Bipolar Aperture for 2.4 – 2.5 GHz 3rd Harmonic Down Converter Application) and FIG. 181 (Down Converted I/Q Waveforms - Slight Carrier Offset) illustrate the results from an actual circuit design and simulation targeting the 2.4 – 2.5 GHz ISM band and implementing a bipolar weighted aperture. FIG. 180 illustrates actual gating pulses, which form the apertures for I-, I+, Q-, and Q+. FIG. 181 illustrates the baseband I and Q outputs corresponding to the down converter. In embodiments, the sequence I-, I+, Q- and Q+ apertures are repeated every

three carrier cycles, nominally. Hence, out of six sine carrier segments, four are captured. Conversion losses well below 10dB are possible with this embodiment of the present invention.

8. Mathematical Transform Describing Embodiments of the Present Invention

8.1 Overview

The operation of the present invention represents a new signal-processing paradigm. Embodiments of the invention can be shown to be related to particular Fourier sine and cosine transforms. Hence, the new term UFT transform is utilized to refer to the process. As already stated, in embodiments of the present invention can be viewed as a matched filter or correlator operation, which in embodiments is normally applied recursively to the carrier signal at a sub-harmonic rate. A system equation may be written to describe this operation, assuming a rectangular sample aperture and integrators as operators, as shown in FIG. 182 and EQ. (88). The process integrates across an acquisition aperture then stores that value, or a significant portion thereof, to be accumulated with the next aperture. Hence, energy from the input is acquired during T_A and held for T_s - T_A until the next acquisition.

$$D_n \triangleq \sum_{n=1}^{k} \int_{nT_S}^{nT_S+T_A} \left(u\left(t - nT_s\right) - u\left(t - \left(nT_S + T_A\right)\right)\right) \cdot A_n \sin\left(\omega t + \phi_{(n-\ell)}\right) dt$$

$$-\alpha \sum_{n=1}^{k} \int_{(n+\ell)T_S}^{(n+\ell)T_S+T_A} \left(u\left(t - (n-\ell)T_S\right) - u\left(t - \left(n - (1-\ell)\right)T_S + T_A\right)\right) \cdot A_{(n-\ell)} S_i\left(\omega t + \phi_{(n-\ell)}\right) dt$$

EQ. (88)

where:

T_A is the aperture duration;

T_S is the sub-harmonic sample period;

k is the total number of collected apertures;

ℓ is the sample memory depth;

$\forall$ is the UFT leakage coefficient;

A_n is the amplitude weighting on the nth aperture due to modulation, noise, etc.; and

ν_n is the phase domain shift of nth aperture due to modulation, noise, carrier offset, etc.

D_n represents the UFT transform applicable to embodiments of the invention. The first term defines integration over a rectangular segment of the carrier signal of T_A time duration. k pulses are summed to form a memory of the recursively applied kernel. The second term in the equation provides for the fact that practical implementations possess finite memory. Hence, embodiments of the present invention are permitted to leak after a fashion by selecting α and ℓ. This phenomena is reflected in the time variant differential equation, EQ. (31), derived in sub-section 5. In embodiments, for a perfect zero order data hold function, $\alpha = 0$.

8.2 The Kernel for Embodiments of the Invention

The UFT kernel applicable to embodiments of the invention is given by EQ. (89):

$$D_1 = \int_0^{T_A} \left(u(t) - u(t - T_A)\right) \cdot A \sin\left(\omega t + \phi\right) dt \qquad \text{EQ. (89)}$$

EQ. 89 accounts for the integration over a single aperture of the carrier signal with arbitrary phase, ϕ, and amplitude, A. Although A and ϕ are shown as constants in this equation, they actually may vary over many (often hundreds or thousands) of carrier cycles. Actually, $\phi(t)$ and $A(t)$ may contain the modulated information of interest at baseband. Nevertheless,

over the duration of a pulse, they may be considered as constant.

8.3 Waveform Information Extraction

Ever since Nyquist developed general theories concerning waveform sampling and information extraction, researchers and developers have pursued optimum sampling techniques and technologies. In recent years, many radio architectures have embraced these technologies as a means to an end for ever more 'digital like' radios. Sub sampling, IF sampling, syncopated sampling, etc., are all techniques employed for operating on the carrier to extract the information of interest. All of these techniques share a common theory and common technology theme, i.e., Nyquist's theory and ideal impulse samplers. Clearly, Nyquist's theory is truly ideal, from a theoretical perspective, while ideal impulse samplers are pursued but never achieved.

Consider the method of developing an impulse sample using functions with shrinking apertures, as illustrated in FIG. 183. The method illustrated in FIG. 183 utilizes a pulse shape, for example a normalized Gaussian, a modified sinc, or some other suitable type, and permits the pulse width to shrink as the peak amplitude grows. As the pulse width shrinks, the area of the pulse becomes unity. These pulse generation methods are formulated using distribution mathematics techniques. Typically, such formulations require the assumption that causality is violated as is illustrated by the precursors in FIG. 183. Hence, such pulses are not practical because they are non-causal. In addition, since impulse samplers are implemented to store the sample value at an instantaneous waveform point, they typically utilize a sample and hold approach, which typically implies the charging of a capacitor. As would be known to persons skilled in the relevant arts given the discussion herein, parasitics can present significant charging concerns for such pulses because of the

relationships represented by EQ. (90) and EQ. (91).

$$\frac{dq}{dt} = C\frac{dv}{dt} \text{ (Charge Differential)} \qquad \text{EQ. (90)}$$

$$u = \int_0^q \frac{q_x}{c} - dq_x = \frac{q^2}{2c} = \frac{Cv^2}{2} \text{ (Energy)} \qquad \text{EQ. (91)}$$

As would be apparent to persons skilled in the relevant arts given the discussion herein, an arbitrary capacitance, *c*, cannot be charged in an infinitesimally short time period without an infinite amount of energy. Even approximations to an ideal impulse therefore can place unrealistic demands on analog sample acquisition interface circuits in terms of parasitic capacitance vs. pulse width, amplitude, power source, etc. Therefore, a trade-off is typically made concerning some portion of the mix.

The job of a sample and hold circuit is to approximate an ideal impulse sampler followed by a memory. There are limitations in practice, however. A hold capacitor of significant value must be selected in order to store the sample without droop between samples. This requires a healthy charging current and a buffer, which isolates the capacitor in between samples, not to mention a capacitor, which is not 'leaky,' and a buffer without input leakage currents. In general, ideal impulse samplers are very difficult to approximate when they must operate on RF waveforms, particularly if IC implementations and low power consumption are required.

The ideal sample extraction process is mathematically represented in EQ. (92) by the sifting function.

$$\int_{-\infty}^{\infty} x(t)\delta\left(t - {T_A}/{2}\right)\, dt = x\left(\frac{T_A}{2}\right) \qquad \text{EQ. (92)}$$

where: $\frac{T_A}{2}$ $\underline{\Delta}$ Sample Time; $x(t)$ $\underline{\Delta}$ Sampled Function; and $\delta(t)$ $\underline{\Delta}$ Impulse Sample Function.

Suppose now that:

$$x(t) = A\sin(t + \phi) \qquad \text{EQ. (93)}$$

then:

$$\int_{-\infty}^{\infty} A\sin(t+\phi)\delta\left(t - {T_A}/{2}\right)dt = A\sin\left({T_A}/{2} + \phi\right)$$

$$= A\cos(\phi)\int_{-\infty}^{\infty}\sin(t)\delta\left(t - {T_A}/{2}\right)dt + A\sin(\phi)\int_{-\infty}^{\infty}\cos(t)\delta\left(t - {T_A}/{2}\right)\, dt$$

EQ. (94)

$$= A\cos(\phi)\sin\left({T_A}/{2}\right) = A\cos(\phi); T_A = \pi \qquad \text{EQ. (95)}$$

This represents the sample value acquired by an impulse sampler operating on a carrier signal with arbitrary phase shift ϕ. EQ. (95) illustrates that the equivalence of representing the output of the sampler operating on a signal, $\tilde{X}(t)$, without phase shift, ϕ, weighted by $\cos\phi$, and the original sampled $X(t)$, which does have a phase shift. The additional requirement is that a time aperture of T_A corresponds to π radians.

Next, consider the UFT kernel:

$$D_1 \triangleq \int_{-\infty}^{\infty} (u(t) - u(t - T_A))\sin(t + \phi)dt \qquad \text{EQ. (96)}$$

Using trigonometric identities yields:

$$D_1 \triangleq A\cos(\phi)\int_{-\infty}^{\infty} (u(t) - u(t - T_A))\sin(t)dt \qquad \text{EQ. (97)}$$

Now the kernel does not possess a phase term, and it is clear that the aperture straddles the sine half cycle depicted in FIG. 184. In EQ. (97), $\cos\phi$ is a weighting factor on the result, which originally illustrated the non-ideal alignment of the present invention clock and carrier signal. Trigonometric identities provide a means of realigning the present invention clock and carrier signal while accounting for the output result due to phase skew.

Consider the ideal aperture of embodiments of the invention shown in FIG. 185. Notice that the ideal aperture is illustrated as possessing two equal ½ aperture components. Hence the UFT kernel for embodiments of the invention can be rewritten as:

$$D_1 \triangleq A\cos(\phi)\left[\int_{-\infty}^{\infty}\left(u(t)-u\left(T_A/2\right)\right)\sin(t)dt+\int_{-\infty}^{\infty}\left(u\left(t-T_A/2\right)-u(t-T_A)\right)\sin(t)dt\right]$$

EQ. (98)

It should also be apparent to those skilled in the relevant arts given the discussion herein that the first integral is equivalent to the second, so that;

$$D_1 = 2A\cos(\phi)\int_{-\infty}^{\infty}\left(u(t)-u\left(t-T_A/2\right)\right)\sin(t)dt$$

EQ. (99)

As illustrated in FIG. 186, a property relating unit step functions and delta functions is useful. In FIG. 186, a step function is created by integrating a delta function. Therefore;

$$D_1 = 2A\cos(\phi)\int_{-\infty}^{\infty}\left[\int_{-\infty}^{t'}\delta(t')\,dt' - \int_{-\infty}^{t'}\delta\left(t' - T_A/2\right)dt'\right]\sin(t)\,dt$$

EQ. (100)

Using the principle of integration by parts yields EQ. (101).

$$D_1 = 2A\cos(\phi)\int_{-\infty}^{t'}\cos(t')\,\delta(t')\,dt' + 2A\cos(\phi)\int_{-\infty}^{t'}\cos(t')\,\delta\left(t' - T_A/2\right)dt$$

$$= 2A\cos\phi\int_{-\infty}^{t'}\sin(t')\delta\left(t - T_A/2\right)dt$$

$$= 2A\cos(\phi), \text{ for } T_A = \pi \qquad \text{EQ. (101)}$$

This is a remarkable result because it reveals the equivalence of the output of embodiments of the present invention with the result presented earlier for the arbitrarily phased ideal impulse sampler, derived by time sifting. That is, in embodiments, the UFT transform calculates the numerical result obtained by an ideal sampler. It accomplishes this by averaging over a specially constructed aperture. Hence, the impulse sampler value expected at $T_A/2$ is implicitly derived by the UFT transform operating over an interval, T_A. This leads to the following very important implications for embodiments of the invention:

- The UFT transform is very easy to construct with existing circuitry hardware, and it produces the results of an ideal impulse sampler, indirectly, without requiring an impulse sampler.
- Various processor embodiments of the present invention reduce the variance of the expected ideal sample, over that obtained by

impulse sampling, due to the averaging process over the aperture.

8.4 Proof Statement for UFT Complex Downconverter Embodiment of the Present Invention

The following analysis utilizes concepts of the convolution property for the sampling waveform and properties of the Fourier transform to analyze the complex clock waveform for the UFT as well as the down conversion correlation process. FIG. 187 illustrates this process.

In addition *r(t)* is considered filtered, by a bandpass filter. In one exemplary embodiment, sub-optimal correlators approximate the UFT. This analysis illustrates that some performance is regained when the front-end bandpass filter is used, such that the derived correlator kernel resembles the optimal form obtained from matched filter theory. Furthermore, the analysis illustrates that the arbitrary phase shift of a carrier on which the UFT operates, does not alter the optimality of the correlator structure which can always be modeled as a constant times the optimal kernel. This is due to the fact that UFT is by definition matched to a pulse shape resembling the carrier half cycle which permits phase skew to be viewed as carrier offset rather than pulse shape distortion.

Using the pulse techniques described above, describing pulse trains, the clock signal for UFT may be written as equation 18802 of FIG. 188.

$p_c(t)\underline{\Delta}$ A basic pulse shape of the clock (gating waveform), in our case defined to have specific correlation properties matched to the half sine of the carrier waveform.

$T_s\underline{\Delta}$ Time between recursively applied gating waveforms.

$T_A\underline{\Delta}$ Width of gating waveform

In FIG. 188, $C_I(t)$ in equation 18804 and $C_Q(t)$ in equation 18806 are considered to be complex clocks shifted in phase by $T_A/2$. The received carrier is related to T_A by $f_c \approx (2T_A)^{-1}$

Although the approximation is used, ideal carrier tracking for coherent demodulation will yield an equal sign after lock. However, this is not required to attain the excellent benefit from UFT processing. Other sections herein provide embodiments that develop expressions for C_I and C_Q from Fourier series analysis to illustrate the components of the gating waveforms at the Carrier frequency which are harmonically related to T_s.

By the methods described above, the Fourier transform of the clock is found from:

$$C_I(f) = \Im\left\{\sum_{m=-\infty}^{\infty}\delta(t - mT_s)\right\}P_c(f) \qquad \text{EQ. (102)}$$

$$C_I(f) = \sum_{n=-\infty}^{\infty}\frac{T_A}{T_s}\frac{\sin(n\pi f_s T_A)}{n\pi f_s T_A}\cdot\delta(f - nf_s) \qquad \text{EQ. (103)}$$

C_Q possesses the same magnitude response of course but is delayed or shifted in phase and therefore may be written as:

$$C_Q(f) = C_I(f)e^{-jn\pi f T_A} \qquad \text{EQ. (104)}$$

When T_A corresponds to a half sine width then the above phase shift related to a $\frac{\pi}{2}$ radians phase skew for C_Q relative to C_I.

In one exemplary embodiment, consider then the complex UFT processor operating on a shifted carrier for a single recursion only,

$$S_0(t) = \int_0^{T_A} r(t)C_I(t)dt + \int_{T_A/2}^{3T_A/2} r(t)C_Q(t)dt \quad \text{EQ. (105.1)}$$

$$S_0(t) = \int_0^{T_A} (A\sin(\omega t + \phi) + n(t))C_I(t)dt + \int_{T_A/2}^{3T_A/2} (A\sin(\omega t + \phi) + n(t))C_Q(t)dt \quad \text{EQ. (105.2)}$$

This analysis assumes that *r(t),* the input carrier plus noise, is band limited by a filter. In this case therefore the delta function comb evident in the transform of C_I and C_Q are ignored except for the components at the carrier. Embodiments in other sections break C_I and C_Q into a Fourier series. In this series, only the harmonic of interest would be retained when the input waveform *r(t)* is bandpass limited because all other cross correlations tend to zero. Hence,

$$S_0(t) \simeq K\int_0^{T_A} (A\sin(\omega t + \phi) + n(t))\sin(\omega t)dt + K\int_{T_A/2}^{3T_A/2} (A\sin(\omega t + \phi) + n(t))\cos(\omega t)dt \quad \text{EQ. (105.3)}$$

$$S_0(t) \simeq K\int_0^{T_A} (A\sin(\omega t)\cos\phi + \cos(\omega t)\sin\phi + n(t))\sin(\omega t)dt + K\int_{T_A/2}^{3T_A/2} (A\sin(\omega t)\cos\phi + \cos(\omega t)\sin\phi + n(t))\cos(\omega t)dt \quad \text{EQ. (105.4)}$$

The clock waveforms have been replaced by the single sine and cosine components from the Fourier transform and Fourier series, which

produce the desired result due to the fact that a front-end filter filters all other spectral components. This produces a myriad of cross correlations for the complex UFT processor. K is included as a scaling factor evident in the transform.

$$S_0(t) = KA\cos\phi \overbrace{\int_0^{T_A} (\sin(\omega t))^2 dt}^{optimal\,correlator} +$$

$$K\int_0^{T_A} n(t)\sin\omega t dt + KA\sin\phi \int_{T_A/2}^{3T_A/2} \overbrace{(\cos(\omega t))^2}^{optimal\,correlator} dt + K\int_{T_A/2}^{3T_A/2} n(t)\cos\omega t dt$$

EQ. (106.1)

$$\therefore S_0(t) = \left(\frac{KA\pi}{2}\cos\phi + \tilde{n}_I\right) \; I \text{ component} \quad \text{EQ. (106.2)}$$

$$+\left(\frac{KA\pi}{2}\sin\phi + \tilde{n}_Q\right) \; Q \text{ component} \quad \text{EQ. (106.2.1)}$$

where $$K = \left(\frac{T_A}{T_s}\frac{\sin\left(n\pi\frac{T_A}{T_s}\right)}{\left(n\pi\frac{T_A}{T_s}\right)}\right) \qquad \text{EQ. (106.3)}$$

A and ϕ are the original components of the complex modulation envelope (amplitude and phase) for the carrier and are assumed to vary imperceptibly over the duration for T_A. What is very interesting to note is that the above equations are exactly the optimum form for the complex correlator whose pulse shape is a half sine with components weighted by cosine for I, and sine for Q. Furthermore, when an input bandpass filter is

considered as a part of the system then the approximate kernels used throughout various analyses based on the gating function become replaced by the ideal matched filter analogy. Hence, the approximation in CMOS using rectangular gating functions, which are known to cause only a 0.91 dB hit in performance if C is selected correctly, probably can be considered pessimistic if the receiver front end is filtered.

8.5 Acquisition and Hold Processor Embodiment

As illustrated in FIG. 189, embodiments of the present invention can be approximately modeled as a particular case of a sampling system. In the example model in FIG. 189, both an acquisition phase and a hold phase for each T_s cycle is shown, where:

$r(t)\underline{\Delta}$	Input Waveform RF Modulated Carrier Plus Noise
$C_A(t)\underline{\Delta}$	Present Invention Aperture Waveform Pulse Train
$\delta_H(t)\underline{\Delta}$	Holding Phase Impulse Train
$h_A(t)\underline{\Delta}$	Integrator Impulse Response of the present Invention
$h_H(t)\underline{\Delta}$	Ƶ0DH Portion of Present Invention Impulse Response

The embodiment in FIG. 189 consists of a gating device followed by a finite time integrator, then an ideal sampler, and finally a holding filter, which accumulates and stores the energy from the acquisition phase. This is called an acquisition and hold processor. The acquisition phase of the operation is described by:

$$X(t) = C_T(t)r(t) * h_A(t) \qquad \text{EQ. (107)}$$

$$X(t) = \sum_{k=-\infty}^{\infty}\left(u(t-kT_s) - u(t-(kT_s+T_A))\right)A_k\left(\sin(\omega_c t+\phi_k)\right) * h_A(t)\Big) \qquad \text{EQ. (108)}$$

The ultimate output includes the hold phase of the operation and is written as:

$$S_0(t) = (X(t)\delta_H(t)) * h_H(t) \qquad \text{EQ. (109)}$$

$$S_0(t) = \sum_{k=-\infty}^{\infty} (X(t)\delta_H(t - k(T_s))) * u(t - (kT_s + T_A)) - u(t - (k+)T_s)$$

EQ. (110)

$$T = T_s - T_A \qquad \text{EQ. (111)}$$

This embodiment considers the aperture operation as implemented with an ideal integrator and the hold operation as implemented with the ideal integrator. As shown elsewhere herein, this can be approximated by energy storage in a capacitor under certain circumstances.

The acquisition portion of the operation possesses a Fourier transform given by:

$$X_0(\omega) = \Im_0\{X_0(t)\} = \sum_{k=-\infty}^{\infty} \frac{1}{2\pi T_s} \overbrace{\delta(\omega - k\omega_s)}^{Harmonic\ Sifter} \overbrace{\left(\frac{T_A}{2} e^{j\omega T_A/2} \frac{\sin(\omega T_A/2)}{\omega T_A/2}\right)}^{Finite\ Time\ Integrator} \underbrace{S_i(\omega)_C}_{Original\ Information\ Specturm\ Chopped\ by\ C(t)}$$

$S_i(\omega) = \Im\{r(t)\}$ (Modulated Information Spectrum)

$S_0(\omega)$ can be found in a similar manner.

$$\Im\{S_0(t)\} = \sum_{k=-\infty}^{\infty} \frac{1}{2\pi T_s} \overbrace{\delta(\omega - k\omega_s)}^{Harmonic\ Sifter} \overbrace{\left(\frac{T}{2} e^{j\omega T_A/2} \frac{\sin(\omega T/2)}{\omega T/2}\right)}^{Z0DH\ Response} X(\omega)$$

$$T = T_s - T_A$$

The example of FIG. 190 illustrates the various components of the above transform superimposed on the same graph, for a down conversion case, where T_A is chosen as a single aperture realization and the 3rd sub

harmonic is used for down conversion. The analysis does not consider the affect of noise, although, it is straightforward to accomplish, particularly in the case of AWGN. The lowpass spectrum possesses nulls at nf_{SA}, $n = 0,\ \pm 1,\ \pm 2, \ldots,$ where $f_s = (T_s - T_A)^{-1}$. This Z0DH spectral response is also present at each harmonic of f_s, although it is not indicated by the graphic.

The acquisition portion of the Fourier transform yields the following an important insight:

$$X_0(\omega) = \frac{KT_A}{T_s} \sum_{k=-\infty}^{\infty} \delta(\omega - k\omega_s) \left(e^{j\omega T_A/2} \frac{\sin\left(\omega T_A/2\right)}{\omega T_A/2} \right) \cdot S_i(\omega)_c$$

EQ. (112)

$$S_i(\omega)_c = A_k T_A e^{j\omega T_A/2} \frac{\sin\left(\omega\left(T_A/2\right)\right)}{\omega\left(T_A/2\right)} \left(\delta(\omega - \omega_c) + \delta(\omega + \omega_c)\right)$$

EQ. (113)

As should be apparent to persons skilled in the relevant arts given the discussion herein, down conversion occurs whenever $k\omega_s = \omega_c$. It is useful to find T_A, which maximizes the component of the spectrum at ω_c, which is subject to down conversion and is the desired signal. This is accomplished simply by examining the kernel.

$$\tilde{X} \triangleq \left| \frac{T_A}{T_s} \frac{\sin\left(\omega\left(T_A/2\right)\right)}{\omega\left(T_A/2\right)} \right| \qquad \text{EQ. (114)}$$

For $\omega = \omega_c$,

$$\widetilde{X} = \left| \frac{T_A}{n \cdot T_c} \; \frac{\sin\left(\pi \frac{T_A}{T_c}\right)}{\left(\pi \frac{T_A}{T_c}\right)} \right|, \quad nT_c = T_s \text{ for Harmonic Conversion}$$

$$\therefore \widetilde{X} = \frac{1}{n\pi} \sin\left(\pi \frac{T_A}{T_c}\right) \qquad \text{EQ. (115)}$$

The kernel is maximized for values of $\frac{T_A}{T_c} = 1/2,\ 3/2,\ 5/2, \cdots$

Advocates of impulse samplers might be quick to point out that letting $T_A \to 0$ maximizes the sinc function. This is true, but the sinc function is multiplied by T_A in the acquisition phase. Hence, a delta function that does not have infinite amplitude will not acquire any energy during the acquisition phase of the sampler process. It must possess infinite amplitude to cancel the effect of $T_A \to 0$ so that the multiplier of the sinc function possesses unity weighting. Clearly, this is not possible for practical circuits.

On the other hand, embodiments of the present invention with $\frac{T_A}{T_c} = 1/2,\ 3/2,\ 5/2, \ldots$ etc., does pass significant calculable energy during the acquisition phase. This energy is directly used to drive the energy storage element of Z0DH filter or other interpolation filter, resulting in practical RF impedance circuits. The cases for T_A/T_c other than $1/2$ can be represented by multiple correlators, for example, operating on multiple half sine basis.

Moreover, it has been shown that the specific gating aperture, $C(t)$, does not destroy the information. Quite the contrary, the aperture design for embodiments of the present invention produces the result of the impulse sampler, scaled by a gain constant, and possessing less variance. Hence, the

delta sifting criteria, above trigonometric optimization, and correlator principles all point to an aperture of $\frac{T_A}{T_c} = \frac{1}{2}$ nominal.

If other impulse responses are added around the present invention (i.e., energy storage networks, matching networks, etc.) or if the present invention is implemented by simple circuits (such as the RC processor) then in embodiments the optimal aperture can be adjusted slightly to reflect the peaking of these other embodiments. It is also of interest to note that the Fourier analysis above predicts greater DC offsets for increasing ratios of $\frac{T_A}{T_c}$. Therefore, for various embodiments, $\frac{T_A}{T_c} = \frac{1}{2}$ is probably the best design parameter for a low DC offset system.

9. Comparison of the UFT Transform to the Fourier Sine and Cosine Transforms

The sine and cosine transforms are defined as follows:

$$F_c(\omega) \triangleq \int_0^\infty f(t) \sin \omega t \, dt \quad \omega \geq 0 \text{ (sine transform)} \quad \text{EQ. (116)}$$

$$F_s(\omega) \triangleq \int_0^\infty f(t) \cos \omega t \, dt \quad \omega \geq 0 \text{ (cosine transform)} \quad \text{EQ. (117)}$$

Notice that when $f(t)$ is defined by EQ. (118):

$$f(t) = u(t) - u(u - T_A) \qquad \text{EQ. (118)}$$

the UFT transform kernel appears as a sine or cosine transform depending on ϕ. Hence, many of the Fourier sine and cosine transform properties may be used in conjunction with embodiments of the present invention to solve signal processing problems.

The following sine and cosine transform properties predict the following results of embodiments of the invention:

Sine and Cosine Transform Property	Prediction of Embodiments of the Invention
Frequency Shift Property	Modulation and Demodulation while Preserving Information
Time Shift Property	Aperture Values Equivalent to Constant Time Delta Time Sift.
Frequency Scale Property	Frequency Division and Multiplication

Of course many other properties are applicable as well. The subtle point presented here is that for embodiments the UFT transform does in fact implement the transform, and therefore inherently possesses these properties.

Consider the following specific example:

let $f(t) = u(t) - u(t - T_A)$ and let $\omega = 2\pi f = \pi f_A = 1$.

$$\Im_c[f(t)] = \int_0^{T_A} \cos(\omega t)\ dt = \frac{1}{\omega}\ \sin \omega T_A = 0 \qquad \text{EQ. (119)}$$

$$\Im_s[f(t)] = \frac{1}{\omega} - \frac{1}{\omega}\ \cos \omega T_A = 2 \qquad \text{EQ. (120)}$$

This is precisely the result for D_{1c} and D_{1s}. Time shifting yields:

$$\Im_s[f_0(t + T_s) + f_0(t - T_s)] = 2F_s(\omega)\cos(T_s\omega) \qquad \text{(Time Shift Property)}$$

Let the time shift to be denoted by T_s.

$$f(t) = u(t) - u(t - T_A) \qquad \text{EQ. (121)}$$

$$f_0(t) \triangleq \frac{1}{2}(u(t + T_s) - u(t)) + \frac{1}{2}(u(t) - u(t - T_s)) \qquad \text{EQ. (122)}$$

Notice that $f_0(t)$ has been formed due to the single sided nature of the sine

and cosine transforms. Nevertheless, the amplitude is adjusted by $\frac{1}{2}$ to accommodate the fact that the energy must be normalized to reflect the odd function extension. Then finally:

$$\Im_s\left[f_0(t+T_s)+f_0(t-T_s)\right]=\frac{2}{2}F_s(\omega)\cos(T_s\omega)=2\cos\left(\pi T_s/T_A\right)$$

EQ. (123)

which is the same solution for phase offset obtained earlier by other means.

The implications of this transform may be far reaching when it is considered that the discrete Fourier sine and cosine transforms are originally based on the continuous transforms as follows:

$$\Im_c\{f(t)\}=\int_0^\infty f(t)\cos\omega t\ dt \qquad \text{EQ. (124)}$$

$$\Im_{DC}\{f(t)\}\ \underline{\Delta}\ \Im\{f(n)\}=\sqrt{\frac{2}{N}}\sum_{m=0}^{N}\alpha_m\alpha_n\cos\left(\frac{mn\pi}{N}\right)f(n) \qquad \text{EQ. (125)}$$

That is, the original kernel $\cos(\omega t)$ and function $f(t)$ are sampled such that:

$f(n)\ \underline{\Delta}$ Sampled Version of $f(t)$

$\omega_m = 2\pi_m\Delta f$

$t_n = n\Delta t$

$\Delta f\ \underline{\underline{\Delta}}$ Frequency Sample Interval

$\Delta t\ \underline{\underline{\Delta}}$ Time Sample Interval

Hence the new discrete cosine transform kernel is:

$$k_c(m,n)=\cos(2\pi mn\ \Delta f\Delta t)=\cos(\pi mn/n)\ \Delta f\Delta t=\frac{1}{2N}$$

EQ. (126)

N is the total number of accumulated samples for m, n, or the total record length.

In recent years, the discrete cosine transform (DCT) and discrete sine transform (DST) have gained much recognition due to their efficiency for waveform coding compression, spectrum analysis, etc. In fact, it can be shown that these transforms can approach the efficiency of Karhunen-Loeve transforms (KLT), with minimal computational complexity. The implication is that the sifted values from D_1 could be used as DCT sample values $f(n)$. Then the DCT and DST properties will apply along with their processing architectures. In this manner, communications signals, like OFDM, could be demodulated in a computationally efficient manner. Many other signal processing applications are possible using the present invention, and the possibilities are rich and varied.

10. Conversion, Fourier Transform, and Sampling Clock Considerations

The previous sub-sections described how embodiments of the present invention involve gating functions of controlled duration over which integration can occur. This section now addresses some consideration for the controlling waveform of the gating functions.

For sub harmonic sampling:

$$f_s = f_c / M$$

$f_s \triangleq$ Sample Rate

$f_c \triangleq$ Carrier Frequency

$M \triangleq$ As an integer such that $0 < M < \infty$

The case M=1 represents a classic down conversion scenario since $f_s = f_c$. In general though, M will vary from 3 to 10 for most practical applications. Thus the matched filtering operation of embodiments of the present invention is applied successively at a rate, f_s, using the approach of

embodiments of the present invention. Each matched filter/correlator operation represents a new sample of the bandpass waveform.

The subsequent equations illustrate the sampling concept, with an analysis base on approximations that ignore some circuit phenomena. A more rigorous analysis requires explicit transformation of the circuit impulse response. This problem can be solved by convolving in the time domain as well, as will be apparent to persons skilled in the relevant arts given the discussion herein. The results will be the same. The analysis presented herein is an abbreviated version of one provided above. As in the subsection 8, the acquisition portion of the present invention response is analyzed separately from the hold portion of the response to provide some insight into each. The following sub-section uses a shorthand notation for convenience.

$$X_0(t) = S_i(t) \sum_{k=-\infty}^{\infty} \widetilde{C}(t - kT_s) \quad \text{(approximate output of acquisition)}$$

EQ. (127)

$X_0(t) \triangleq$ Output of Sample

$S_i[t] \triangleq$ Waveform being Sampled

$k \triangleq$ Sampling Index

$T_s \triangleq$ Sampling Interval $= f_s^{-1}$

$\widetilde{C}(t - kT_s) \triangleq$ Quasi-Matched Filter/Correlator Sampling Aperture, which includes averaging over the Aperture.

EQ. (127) can be rewritten a:

$$X_0(t) \cong \sum_{k=-\infty}^{\infty} S_i(kT_s) * \widetilde{C}(t - kT_s) \qquad \text{EQ. (128)}$$

If $\widetilde{C}(t)$ possesses a very small aperture with respect to the inverse information bandwidth, $T_A << BW_i^{-1}$, then the sampling aperture will

weight the frequency domain harmonics of f_s. The Fourier transform and the modulation property may be applied to EQ. (128) to obtain EQ. (129) (note this problem was solved above by convolving in the time domain).

$$X_0(\omega) = \left(S_i(\omega)_c \, \tilde{C}(\omega) \right) \qquad \text{EQ. (129)}$$

$$\therefore X_0(\omega) \cong \frac{K}{T_s} \sum_{k=-\infty}^{\infty} \delta_i(\omega - k\omega_s) \left[\frac{T_A \cdot e^{j\omega T_A/2}}{2} \frac{\sin(\omega T_A/2)}{\omega T_A/2} \right] \cdot S_i(\omega)_c$$

EQ. (130)

$K\Delta$ Arbitrary Gain Constant, which includes a $1/2\pi$ factor $\omega \triangleq 2\pi f$

Essentially, on the macroscopic frequency scale, there is a harmonic sample comb generated, which possesses components at every Nf_s for N = 1,2,3...∞, with nulls at every $Z \cdot f_A$, where f_A is defined as T_A^{-1}. FIG. 191 illustrates this result.

The thickness of each spike in FIG. 191 illustrates the surrounding band produced from $S_i(\omega)$. $S_i(\omega)$ is a complex transform including magnitude and phase, which can be assigned a vector representation in the time domain (i.e., I and Q components). The natural action of embodiments of the present invention, in the hold portion of the response, acts as a lowpass filter in the down conversion case, thereby reducing the levels of all the harmonic sidebands. Likewise, the up converter utilizes a bandpass matched filter to extract the desired carrier and reject unwanted images.

Notice that each harmonic including baseband possesses a replica of $S_i(\omega)$ which is in fact the original desired signal. { $S_i(\omega)$ is the original information spectrum and is shown to survive the acquisition response of the present invention (i.e., independent integration over each aperture)}. Lathi and many others pointed out that $\tilde{C}(\omega)$ could be virtually any harmonic function and that conversion to baseband or passband will result

from such operations on $S_i(t)$.

Each discrete harmonic spectrum provides a potential down conversion source to baseband (at DC). Of course, theoretically, there cannot be a conversion of $Z \cdot f_a$ because of the spectral nulls. FIG. 191 illustrates the important relationships between f_s, f_a, and the relative harmonic conversion efficiency related to the sinc^2 function harmonic comb weighting, resulting from a simple rectangular sampling aperture.

It should also be noted that in all practical cases, $f_s >> 2 \cdot BW_i$, so that Nyquist criteria are more than satisfied. The lowpass response of embodiments of the present invention can be ideally modeled as a zero order data hold filter, with a finite time integrator impulse response duration of $T = T_s - T_A$. The ultimate output Fourier transform is given by EQ. (131).

$$S_0(\omega) = \underbrace{\sum_{k=-\infty}^{\infty} \frac{K}{T_s} \delta(\omega - k\omega_s)}_{Harmonic\,Sifter} \underbrace{\left(\frac{T}{2} e^{j\omega T/2} \frac{\sin \omega T/2}{\omega T/2} \right)}_{Z0DH\ \text{Response}} \cdot \underbrace{X(\omega)}_{Acquisition\ \text{Response}}$$

EQ. (131)

The $Z0DH$ is a type of lowpass filter or sample interpolator which provides a memory in between acquisitions. Each acquisition is accomplished by a correlation over T_A, and the result becomes an accumulated initial condition for the next acquisition.

10.1 Phase Noise Multiplication

Typically, processor embodiments of the present invention sample at a sub-harmonic rate. Hence the carrier frequency and associated bandpass signal are down converted by a $M \cdot f_s$ harmonic. The harmonic generation operation can be represented with a complex phasor.

$$S_{amp}(t) \underline{\Delta} \left(e^{-j\omega_s t + \phi(t)} \right)^m \qquad \text{EQ. (132)}$$

$S_{amp}(t)$ can be rewritten as:

$$S_{amp}(t) = e^{-jM\omega_s t} \cdot e^{M\phi(t)} \qquad \text{EQ. (133)}$$

$\phi(t) \triangleq$ Phase Noise on the Conversion Clock

As EQ. (133) indicates, not only is the frequency content of the phasor multiplied by M but the phase noise is also multiplied by M. This results in an M-tuple convolution of the phase noise spectrum around the harmonic. The total phase noise power increase is approximated by EQ. (134).

$$\phi = \triangleq 20 \log_{10} M \text{ (Phase Noise)} \qquad \text{EQ. (134)}$$

That is, whatever the phase jitter component, $\phi(t)$, existing on the original sample clock at Mf_s, it possesses a phase noise floor degraded according to EQ. (134).

10.2 AM–PM Conversion and Phase Noise

This section describes what the conversion constant and the output noise is for AM to PM conversion according to embodiments of the present invention, considering the noise frequency of the threshold operation. As illustrated in FIG. 192, suppose that the output of a sine signal source must be filtered and compared, in order to obtain a suitable clock signal. For cases where the equivalent input noise power of the threshold device can be considered to be much less than the input power source sine wave, a single zero crossing per cycle of sine wave can be assumed to occur. For such low noise cases, the threshold operation may be viewed as an AM to PM conversion device.

The slope at the zero crossings of a pure sine wave, $s(t) = A \sin \omega t$, can be calculated. Differentiating s(t) with respect to t yields

$s(t)' = \omega A \cos \omega t$. For ω A≠0, the zero crossings occur at $\omega t = \pi/2, 3\pi/2, 5\pi/2 \ldots$

$$\therefore t = \frac{1}{4f}, \frac{3}{4f}, \frac{5}{4f} \cdots \{\text{for } s(t)\} \qquad \text{EQ. (135)}$$

These zero crossings represent the points of minimum slope or crests of the original *s(t)*. The maximum slope is found at the zero crossings of. s(t) at ωt = 0, π, 2π, . . . etc. Plugging those arguments into $s(t)'$ give slopes of: Slope = ωA, -ωA, ωA, -ωA . . . etc. The time at which these zero crossings occur is given by: ωt = π, 2π, 3π . . . $t = \frac{1}{2f}, \frac{1}{f}, \frac{3}{2f}, \ldots \{for\ s(t)\}$.

It stands to reason that for the low noise power assumption, which implies one zero crossing per carrier cycle, the slope at the zero crossing will be modified randomly if a Gaussian process *(n(t))* is summed to the signal. Of course, if the change in slope of the signal is detectable, the delta time of the zero crossing is detectable, and hence phase noise is produced. The addition of noise to the signal has the effect of moving the signal up and down on the amplitude axis while maintaining a zero mean. This can be written more formally as:

$$\left| \frac{\partial\ s(t)}{\partial\ t} \right| = \omega A = \text{ for } \omega\ t = n\pi/2 \qquad \text{EQ. (136)}$$

If A is replaced by *A*-Δa, where Δa represents the noise deviation, then one will not always observe a zero crossing at the point of maximum slope *ωA*. Sometimes the zero crossing will occur at ω(A-Δa). This leads to the low noise approximation:

$$\omega(\mathrm{A} - \Delta \mathrm{a}) = \omega \mathrm{A} \cos[\omega(\mathrm{t} \pm \varepsilon)] \qquad \text{EQ. (137)}$$

$$\text{arcos}\left(\frac{\frac{A-\Delta a}{A}}{\omega}\right) = t \pm \varepsilon \qquad \text{EQ. (138)}$$

The low noise assumption implies that the low noise power prohibits the arcos function from transforming the Gaussian pdf of the noise. That is, $\pm\Delta a$ occurs over minute ranges for the argument of the arcos and hence the relationship is essentially linear. Secondly, since A is a peak deviation in the sine wave Δa will be considered as a peak deviation of the additive noise process. This is traditionally accepted as being 4σ where σ is the standard deviation of the process and σ^2 is the variance. Therefore we write K $\text{arcos}(1-4\sigma/\text{A}) = \text{t} \pm \varepsilon$, where ε represents a peak time deviation in the zero crossing excursion, $K = 1/\omega$, and t is the mean zero crossing time given previously as: $t = 1/sf, 1/f, 3/2f, \ldots$ If only the deviation contribution to the above equation is retained, the equation reduces to:

$$K\cos^{-1}\left(\frac{4\sigma}{A}\right) = \varepsilon = \Delta t \qquad \text{EQ. (139)}$$

Since for $4\sigma / A << .01$, the above function is quasi-linear, one can write the final approximation as:

$$K\frac{4\sigma}{A} = \Delta t = \frac{4\sigma}{\omega A} \text{ seconds (peak)} \qquad \text{EQ. (140)}$$

An appropriate conversion to degrees becomes,

$$360^\circ f_c = \frac{4\sigma_x}{\frac{4\sigma}{\omega_c A}} \qquad \text{EQ. (141)}$$

f_c = frequency of carrier

σ_x = phase noise in degrees rms

σ = standard deviation of equivalent input comparator noise

$$\therefore \sigma_x = \frac{(360)\sigma}{2\pi A} \text{ degrees rms} \qquad \text{EQ. (142)}$$

$\frac{\sigma_x}{57.3}$ = radians rms = σ_ϕ

$\sigma_{\phi_x}{}^2$ = variance or power in dBc

Now a typical threshold operator may have a noise figure, NF, of approximately 15 dB. Hence, one can calculate σ_x (assume $\sigma_\phi{}^2 = 2.4x10^{-8} rad^2$ source phase noise):

$$-174 dBm/Hz + 15 + 10\log_{10} 100x10^6 = -79 dBm \qquad \text{EQ. (143)}$$

where 100 MHz of input bandwidth is assumed.

$$anti\log -7.9 = 1.26x10^{-8} milliwatts = 1.26x10^{-11} watts \qquad \text{EQ. (144)}$$

$$\therefore \sigma = \sqrt{1.26\text{x}10^{-11}} \cong 3.55\text{x}10^{-6} \qquad \text{EQ. (145)}$$

$$\sigma_x = \frac{(360)3.55x10^{-6}}{2\pi(.6)} \simeq 3.39x10^{-4} \text{ degrees rms}$$

$$\sigma_{\phi_x} \cong 5.92x10^{-6} \text{ rad rms}$$

$$\sigma_{\phi_t}{}^2 = \sigma_\theta{}^2 + \sigma_{\phi_x}{}^2 \simeq 2.4x10^{-8} + 3.5x10^{-11} \cong 2.4x10^{-8} rad^2$$

$\sigma_\theta{}^2$ = phase noise of source before threshold device

Therefore, the threshold device has little to no impact on the total phase noise modulation on this particular source because the original source phase noise dominates. A more general result can be obtained for arbitrarily shaped waveforms (other than simple sine waves) by using a Fourier series expansion and weighting each component of the series according to the previously described approximation. For simple waveforms like a triangle

pulse, the slope is simply the amplitude divided by the time period so that in the approximation:

$$\Delta t \simeq \frac{k4\sigma T_r}{A_T} \qquad \text{EQ. (146)}$$

k; an arbitrary scaling constant

T_r; time period for the ramping edge of the triangle

Hence, the ratio of $\left(\sigma T_r / A_r \right)$ is important and should be minimized. As an example, suppose that the triangle pulse rise time is 500 nsec. Furthermore, suppose that the amplitude, A_T, is 35 milli volts. Then, with a 15 dB NF, the Δt becomes:

$$\Delta t = \frac{k \cdot 4 \cdot (3.55 \times 10^{-6}) V 500 nsec}{.035} \simeq 203 \text{ ps}$$

$\sigma \simeq 203/4 \cong 50.7$ ps (1Ω)

This is all normalized to a 1Ω system. If a 50Ω system were assumed then:

$\sigma \simeq 358.5$ ps (50Ω)

In addition, it is straight forward to extend these results to the case of DC offset added to the input of the threshold device along with the sine wave.

Essentially the zero crossing slope is modified due to the virtual phase shift of the input sine function at the threshold. DC offset will increase the phase noise component on the present invention clock, and it could cause significant degradation for certain link budgets and modulation types.

11. Pulse Accumulation and System Time Constant

11.1 Pulse Accumulation

Examples and derivations presented in previous sub-sections illustrate that in embodiments single aperture acquisitions recover energies proportional to:

$$E_\ell = \int_0^{T_A} S_i^2(t)dt = \frac{A_n^2 T_A}{2} \text{ (optimum aperture) EQ. (147)}$$

$A_n \triangleq$ as the carrier envelope weighting of the *nth* sample.

In addition, sub-section 8 above, describes a complete UFT transform over many pulses applicable to embodiments of the invention. The following description therefore is an abbreviated description used to illustrate a long-term time constant consideration for the system.

As described elsewhere herein, the sample rate is much greater than the information bandwidth of interest for most if not all practical applications.

$$f_s >> BW_i \qquad \text{EQ. (148)}$$

Hence, many samples may be accumulated as indicated in previous sub-sections, provided that the following general rule applies:

$$\frac{f_s}{\ell} > BW_i \qquad \text{EQ. (149)}$$

where ℓ represents the total number of accumulated samples. EQ. (149) requires careful consideration of the desired information at baseband, which must be extracted. For instance, if the baseband waveform consists of sharp features such as square waves then several harmonics would necessarily be required to reconstruct the square wave which could require BW_i of up to seven times the square wave rate. In many applications however the base band waveform has been optimally prefiltered or bandwidth limited apriori (in a transmitter), thus permitting significant accumulation. In such circumstances, f_s / ℓ will approach BW_i.

This operation is well known in signal processing and historically has been used to mimic an average. In fact it is a means of averaging scaled by a gain constant. The following equation relates to EQ. (127).

$$\sum_{n=1}^{\ell} E_\ell = \sum_{\ell=1}^{x} \frac{A_n^2 T_A}{2} \cong \frac{\ell A^2 T_A}{2} \qquad \text{EQ. (150)}$$

Notice that the *nth* index has been removed from the sample weighting. In fact, the bandwidth criteria defined in EQ. (149) permits the approximation because the information is contained by the pulse amplitude. A more accurate description is given by the complete UFT transform, which does permit variation in A. A cannot significantly vary from pulse to pulse over an ℓ pulse interval of accumulation, however. If A does vary significantly, ℓ is not properly selected. A must be permitted to vary naturally, however, according to the information envelope at a rate proportional to BW_i. This means that ℓ cannot be permitted to be too great because information would be lost due to filtering. This shorthand approximation illustrates that there is a long term system time constant that should be considered in addition to the short- term aperture integration interval.

In embodiments, usually the long term time constant is controlled by the integration capacitor value, the present invention source impedance, the present invention output impedance, and the load. The detailed models presented elsewhere herein consider all these affects. The analysis in this section does not include a leakage term that was presented in previous sub-sections.

EQs. (149) and (150) can be considered a specification for slew rate. For instance, suppose that the bandwidth requirement can be specified in terms of a slew rate as follows:

$$SR = \times \frac{volts}{\mu \sec} \qquad \text{EQ. (151)}$$

The number of samples per μsec is given by:

$\ell_s = f_s \times 1 \times 10^{-6}$ (f_s is derived from the present invention clock rate)

If each sample produces a voltage proportional to $A^2 T_A / 2$ then the total voltage accumulated per microsecond is:

$$V_{\mu \sec} \cong \ell_s \frac{A^2 T_A}{2} \qquad \text{EQ. (152)}$$

The previous sub-sections illustrates how the present invention output can accumulate voltage (proportional to energy) to acquire the information modulated onto a carrier. For down conversion, this whole process is akin to lowpass filtering, which is consistent with embodiments of the present invention that utilize a capacitor as a storage device or means for integration.

11.2 Pulse Accumulation by Correlation

The previous sub-sections introduced the idea that in embodiments information bandwidth is much less than the bandwidth associated with the

present invention's impulse response for practical applications. The concept of single aperture energy accumulation was used above to describe the central ideas of the present invention. As shown in FIG. 193, multiple aperture accumulation permits baseband waveform reconstruction. FIG. 193 illustrates the results from simulation of actual circuits according to embodiments of the present invention implemented with CMOS and passive components.

The staircase output of the example in FIG. 193 follows the complex modulation envelope for the input signal. Sub-section **5** predicts this result via the time variant linear differential equation. FIG. 193 illustrates the staircase accumulation of half sine energy for three apertures based on 3x sampling. As can be seen in FIG. 193, the leakage between accumulations is very small.

12. Energy Budget Considerations

Consider the following equation for a window correlator aperture:

$$E_{ASO} = \int_0^{TA} A \cdot S_i(t)dt \qquad \text{EQ. (153)}$$

In EQ. (153), the rectangular aperture correlation function is weighted by A. For convenience, it is now assumed to be weighted such that:

$$E_{ASO} = \int_0^{TA} kA \cdot S_i(t)dt = 2A \text{ (normalized)} \qquad \text{EQ. (154)}$$

Since embodiments of the present invention typically operate at a sub-harmonic rate, not all of the energy is directly available due to the sub-harmonic sampling process. For the case of single aperture acquisition, the energy transferred versus the energy available is given by:

$$\frac{E_0}{E_i} = \frac{E_{ASO}}{2N} = \frac{A}{N} \qquad \text{EQ. (155)}$$

N$\underline{\Delta}$ harmonic of operation

The power loss due to harmonic operation is:

$$E_{LN} = 10 \ \log_{10}(2N) \qquad \text{EQ. (156)}$$

There is an additional loss due to the finite aperture, T_A, which induces (sin x/x) like weighting onto the harmonic of interest. This energy loss is proportional to:

$$E_{LSINC} \simeq \left(\frac{\sin(\pi N f_s T_A)}{\pi N f_s T_A} \right) \text{(up conversion only)} \quad \text{EQ. (157)}$$

$N \cdot f_s \underline{\Delta}$ operating carrier frequency

$f_s \underline{\Delta}$ sampling rate (directly related to the clock rate)

EQ. (157) indicates that the harmonic spectrum attenuates rapidly as $N \cdot f_s$ approaches T_A^{-1}. Of course there is some attenuation even if that scenario is avoided. EQ. (157) also reveals, however, that in embodiments for single aperture operation the conversion loss due to E_{LSINC} will always be near 3.92dB. This is because:

$$(2 \cdot N f_s)^{-1} = T_A \ \text{(~3.92dB condition)} \qquad \text{EQ. (158)}$$

Another way of stating the condition is that T_A is always $^1/_2$ the carrier period.

Consider an ideal implementation of an embodiment of the present invention, without any circuit losses, operating on a 5th harmonic basis. Without any other considerations, the energy loss through the device is at minimum:

$$E_L = E_{LN} + E_{LSINC} = 10\text{dB} + 3.92 \simeq 14\text{dB (for up conversion)}$$

EQ. (159)

Down conversion does not possess the 3.92dB loss so that the baseline loss for down conversion is that represented by EQ. (156). Parasitics will also affect the losses for practical systems. These parasitics must be examined in detail for the particular technology of interest.

Next suppose that a number of pulses may be accumulated using the multi-aperture strategy and diversity means of an embodiment of the present invention, as described above. In this case, some of the energy loss calculated by EQ. (159) can be regained. For example, if four apertures are used then the pulse energy accumulation gain is 6dB. For the previous example, this results in an overall gain of 6dB – 14dB, or -8dB (instead of – 14dB). This energy gain is significant and will translate to system level specification improvements in the areas of noise frequency, intercept point, power consumption, size, etc. It should be recognized, however, that a diversity system with active split or separate amplifier chains would use more power and become more costly. In addition, in embodiments, energy storage networks coupled to the circuitry of the present invention may be used to accumulate energy between apertures so that each aperture delivers some significant portion of the stored energy from the network. In this manner, some inefficiencies of the sub harmonic sampling process can be removed by trading impedance matching vs. complexity, etc., as further described below.

12.1 Energy Storage Networks

Embodiments of the present invention have been shown to be a type of correlator, which is applied to the carrier on a sub harmonic basis. It is also been shown herein that certain architectures according to embodiments of the invention benefit significantly from the addition of passive networks, particular when coupled to the front end of a processor according to the present invention used as a receiver. This result can be explained using linear systems theory.

To understand this, it is useful to consider the following. Embodiments of the present invention can be modeled as a linear, time-variant (LTV) device. Therefore, the following concepts apply:

- The LTV circuits can be modeled to have an average

impedance; and

- The LTV circuits can be modeled to have an average power transfer or gain.

These are powerful concepts because they permit the application of the maximum bilateral power transfer theorem to embodiments of the present invention. As a result, in embodiments, energy storage devices/circuits which fly wheel between apertures to pump up the inter sample power can be viewed on the many sample basis (long time average) as providing optimum power transfer through matching properties. The between sample model on the time microscopic scale is best viewed on a differential equation basis while the time macroscopic view can utilize simpler analysis techniques such as the maximum power transfer equations for networks, correlator theory, etc. The fact that the differential equations can be written for all time unifies the theory between the short time (between sample) view and long time (many sample accumulation) view. Fortunately, the concepts for information extraction from the output of the present invention are easily formulated without differential equation analysis.

Network theory can be used to explain why certain networks according to the present invention provide optimum power gain. For example, network theory explains embodiments of the present invention when energy storage networks or matching networks are utilized to 'fly wheel' between apertures, thereby, on the average, providing a good impedance match. Network theory does not explain, however, why T_A is optimal. For instance, in some embodiments, one may deliberately utilize an aperture that is much less than a carrier half cycle. For such an aperture, there is an optimal matching network nonetheless. That is, a processor according to an embodiment of the present invention utilizing an improper aperture can be optimized, although it will not perform as well as a

processor according to an embodiment of the present invention that utilizes an optimal aperture accompanied by an optimal matching network.

The idea behind selecting an optimal aperture is matched filter theory, which provides a general guideline for obtaining the best correlation properties between the incoming waveform and the selected aperture. Any practical correlator or matched filter is constrained by the same physical laws, however, which spawned the maximum power transfer theorems for networks. It does not do any good to design the optimum correlator aperture if the device possesses extraordinary impedance mismatches with its source and load. The circuit theorems do predict the optimal impedance match while matched filter theory does not. The two work hand in hand to permit a practical explanation for:

- Why T_A is optimal; and
- How processors according to embodiments of the present invention are optimized for performance in practical circuits.

The following sub-section analyzes the present invention on a macroscopic scale using the notions of average impedance and power transfer.

12.2 Impedance Matching

When a processor embodiment according to the present invention is 'off,' there is one impedance, and when a processor embodiment according to the present invention is 'on,' there is another impedance due to the architecture of the present invention and its load. In practice, the aperture will affect the 'on' impedance. Hence, on the average, the input impedance looking into the circuitry of an embodiment of the present invention (i.e., its ports) is modified according to the present invention clock and T_A. Impedance matching networks must take this into account.

$$\mathcal{Z}_{av} = \frac{V}{I_{av}} \qquad \text{EQ. (160)}$$

EQ. (160) illustrates that the average impedance, $\mathcal{Z}_{av}$, is related to the voltage, V, divided by the average current flow, I_{av}, into a device, for example a processor according to an embodiment of the present invention. EQ. (160) indicates that for a processor according to an embodiment of the present invention the narrower T_A and the less frequent a sample is acquired, the greater $\mathcal{Z}_{av}$ becomes.

To understand this, consider the fact that a 10th harmonic system according to an embodiment of the present invention operates with half as many samples as a 5th harmonic sample according to the present invention. Thus, according to EQ. (160), a 5th harmonic sample according to an embodiment of the present invention would typically possess a higher input/output impedance than that a 10th harmonic system according to the present invention. Of course, practical board and circuit parasitics will place limits on how much the impedance scaling properties of the present invention processor clock signals control the processor's overall input/output impedance.

As will be apparent to persons skilled in the relevant arts given the discussion herein, in embodiments, matching networks should be included at the ports of a processor according to the present invention to accommodate Z_{av}, as measured by a typical network analyzer.

13. Time Domain Analysis

All signals can be represented by vectors in the complex signal plane. Previous sub-sections derived the result for down converting (or up converting) $S_i(t)$ in the transform domain via $S_i(\omega)$. An I/Q modem embodiment of the present invention, however, was developed using a time domain analysis. This time domain analysis is repeated here and provides a complementary view to the previous sub-sections.

FIG. 194 illustrates an embodiment of the present invention implementing a complex down converter architecture. Operation of this embodiment is described given by:

$$S_0(t_k) \cong \sum_{k=0}^{\infty} \left(S_i(t_k) + n(t_k)\right) \left(C_{Ik} + C_{Qk}\right) \quad \text{EQ. (161.1)}$$

where $S_i(t_k)$ is defined as the kth sample from the UFT transform such that $S_i(t_k)$ is filtered over the kth interval, $n(t_k)$ is defined as the noise sample at the output of the kth present invention kernel interval such that it has been averaged by the present invention process over the interval, C_{Ik} is defined as the kth in phase gating waveform (the present invention clock), and C_{Qk} is defined as the kth quadrature phase gating waveform (the present invention clock).

The 'goodness' of $S_i(t_k)$ and $n_i(t_k)$ has been shown previously herein as related to the type of present invention processor used (e.g.., matched filtering/correlating processor, finite time integrating processor, or RC processor). Each t_k instant is the time tick corresponding to the

averaging of input waveform energy over a T_A (aperture) duration. It has been assumed that C_{Ik} and C_{Qk} are constant envelope and phase for the current analysis, although in general this is not required. Many different, interesting processors according to embodiments of the present invention can be constructed by manipulating the amplitudes and phases of the present invention clock.

C_{Ik} and C_{Qk} can be expanded as follows:

$$C_{Ik} = K\frac{T_A}{T_s}\left[1+2\left(\frac{\sin\pi\frac{T_A}{T_s}}{\pi\frac{T_A}{T_s}}\cdot\cos 2\pi f_s t_k + \frac{\sin 2\pi\frac{T_A}{T_s}}{\pi\frac{T_A}{T_s}}\cdot\cos 4\pi f_s t_k + \frac{\sin 3\pi\frac{T_A}{T_s}}{3\pi\frac{T_A}{T_s}}\cdot\cos 6\pi f_s t_k + \ldots\frac{\sin n\pi\frac{T_A}{T_s}}{n\pi\frac{T_A}{T_s}}\cdot\cos n\cdot 2\pi f_s t_k\right)\right]$$

EQ. (161.2)

$$C_{Qk} = K\frac{T_A}{T_s}\left[1+2\left(\frac{\sin\pi\frac{T_A}{T_s}}{\pi\frac{T_A}{T_s}}\cdot\sin 2\pi f_s t_k - \frac{\sin 2\pi\frac{T_A}{T_s}}{\pi\frac{T_A}{T_s}}\cdot\cos 4\pi f_s t_k - \frac{\sin 3\pi\frac{T_A}{T_s}}{3\pi\frac{T_A}{T_s}}\cdot\sin 6\pi f_s t_k \ldots\frac{\sin n\pi\frac{T_A}{T_s}}{n\pi\frac{T_A}{T_s}}\cdot\cos(n\cdot 2\pi f_s t_k + n\phi)\right)\right]$$

EQ. (161.3)

The above treatment is a Fourier series expansion of the present invention clocks where:

$K \triangleq$ Arbitrary Gain Constant

$T_A \triangleq$ Aperture Time $= f_s^{-1}$

T_s $\underline{\Delta}$ The Present Invention Clock Interval or Sample Time

n $\underline{\Delta}$ Harmonic Spectrum Harmonic Order

ϕ $\underline{\Delta}$ As phase shift angle usually selected as 90° $\left(\pi/2\right)$ for orthogonal signaling

Each term from $C_{Ik,}$ C_{Qk} will down convert (or up convert). However, only the odd terms in the above formulation (for $\phi = \pi/2$) will convert in quadrature. ϕ could be selected otherwise to utilize the even harmonics, but this is typically not done in practice.

For the case of down conversion, $r(t)$ can be written as:

$$r(t_k) = \sqrt{2}A\left(\tilde{S}_{iI}(t_k)\cos(m \cdot 2\pi f t_k + \Theta) - \tilde{S}_{iQ}(t_k)\sin(m \cdot 2\pi f t_k + \Theta) + n(t)\right)$$

EQ. (162)

After applying ($C_{Ik,}$ C_{Qk}) and lowpass filtering, which in embodiments is inherent to the present invention process, the down converted components become:

$$S_0(t_k)_I = A\ S_{iI}(t_k) + \tilde{n}_{Ik} \qquad \text{EQ. (163)}$$

$$S_0(t_k)_Q = A\ S_{iQ}(t_k) + \tilde{n}_{Qk} \qquad \text{EQ. (164)}$$

where:

$S_{iI}(t_k)$ $\underline{\Delta}$ The In phase component of the desired baseband signal.

$S_{iQ}(t_k)$ $\underline{\Delta}$ The quadrature phase component of the desired baseband signal.

$\tilde{n}_I, \tilde{n}_Q$ $\underline{\Delta}$ In phase and quadrature phase noise samples

m $\underline{\Delta}$ Is the harmonic of interest equal to one of the 'n' numbers, for perfect carrier synchronization.

Now m and n can be selected such that the down conversion ideally strips

the carrier (mf_s), after lowpass filtering.

If the carrier is not perfectly coherent, a phase shift occurs as described in previous sub-section. The result presented above would modify to:

$$S_0(t) = \left(S_0(t)_I + jS_0(t)_Q\right) e^{j\phi} \qquad \text{EQ. (165)}$$

where ϕ is the phase shift. This is the same phase shift affect derived earlier as $\cos\phi$ in the present invention transform. When there is a slight carrier offset then ϕ can be written as $\phi(t)$ and the I and Q outputs represent orthogonal, harmonically oscillating vectors super imposed on the desired signal output with a beat frequency proportional to:

$$f_{error} \triangleq nf_s \pm m(f_s \pm f_\Delta) = f_s(n-m) + mf_\Delta \text{ EQ. (166)}$$

$f_\Delta \triangleq$ as a slight frequency offset between the carrier and the present invention clock

This entire analysis could have been accomplished in the frequency domain as described herein, or it could have been formulated from the present invention kernel as:

$$S_0(t) = \mathrm{D}_{IQ}\left(S_i(t) + n(t)\right) \qquad \text{EQ. (167)}$$

The recursive kernel D_{IQ} is defined in sub-section 8 and the I/Q version is completed by superposition and phase shifting the quadrature kernel.

The previous equation for $r(t)$ could be replaced with:

$$BB(t) = \tilde{S}_{iI} \pm \tilde{S}_{iQ} \text{ where } f = 0 \text{ and } \Theta = \pi/4 \text{ and } n(t) = 0 \text{ EQ. (168)}$$

BB(t) could be up converted by applying C_I, C_Q. The desired carrier then is the appropriate harmonic of C_I, C_Q whose energy is optimally extracted by a network matched to the desired carrier.

14. Complex Passband Waveform Generation Using the Present

Invention Cores

This sub-section introduces the concept of using a present invention core to modulate signals at RF according to embodiments of the invention. Although many specific modulator architectures are possible, which target individual signaling schemes such as AM, FM, PM, etc., the example architecture presented here is a vector signal modulator. Such a modulator can be used to create virtually every known useful waveform to encompass the whole of analog and digital communications applications, for "wired" or "wireless," at radio frequency or intermediate frequency. In essence, a receiver process, which utilizes the present invention, may be reversed to create signals of interest at passband. Using I/Q waveforms at baseband, all points within the two dimensional complex signaling constellation may be synthesized when cores according to the present invention are excited by orthogonal sub-harmonic clocks and connected at their outputs with particular combining networks. A basic architecture that can be used is shown in FIG. 195.

FIG. 195 depicts one embodiment of a based vector modulator according to the present invention. FIG. 195 shows I and Q inputs that can accept analog or balanced digital waveforms. By selecting I and Q appropriately, AM, FM, BPSK, QPSK, MSK, QAM, OFDM, multi-tone, and a host of other signals can be synthesized. In this embodiment of the present invention, the present invention cores are driven differentially on I and Q. $C_I, C_{\bar{I}}, C_Q, C_{\bar{Q}}$ are the in phase and quadrature sub-harmonic clocks, respectively, with their inverted phases as well. C_I and C_Q can be created in quadrature for I Q operation if the output power combiner is a 0° combiner. On the other hand, C_I and C_Q can be in phase when a 90° output power combiner is utilized at RF. This latter architecture can be used whenever the signaling bandwidth is very small with respect to the RF center

frequency of the output and small with respect to the 1dB passband response of the combiner. If one assumes constant values on I and $\bar{I}$, the waveform diagrams in FIG 196 can be constructed. As indicated in FIG. 195, the power combiner and bandpass reconstruction filter are optional components.

In FIG. 196, C_I and $\overline{C_I}$ are out of phase by 180° if referenced back to the clock. In this case, clock refers to the sub-harmonic waveform used to generate C_I and $\overline{C_I}$. C_I is coincident with the rising edges of clock with a pulse width of T_A while $\overline{C_I}$ is coincident with the falling edges of clock with a pulse width of T_A. C_I and $\overline{C_I}$ activate two of the processors according to the present invention, as shown in FIG. 195, which are driven by differential signals. I_c is illustrated as if the system is ideal without losses, parasitics, or distortions. The time axis for I_c may be arranged in a manner to represent the waveform as an odd function. For such an arrangement, the Fourier series is calculated to obtain EQ. (169).

$$I_c(t) = \sum_{n=1}^{\infty} \left(\frac{4\,sin\left(\frac{n\pi T_A}{T_s}\right) \cdot sin\left(\frac{n\pi}{2}\right)}{n\pi} \right) \cdot sin\left(\frac{2n\pi t}{T_s}\right) \qquad \text{EQ. (169)}$$

To illustrate this, if a passband waveform must be created at five times the frequency of the sub-harmonic clock then a baseline power for that harmonic extraction can be calculated for $n = 5$. For the case of $n = 5$, it is found that the 5th harmonic yields:

$$I_c(t)\big|_{n=5} = \frac{4}{5\pi}\left(sin(5\omega_s t)\right) \qquad \text{EQ. (170)}$$

This component can be extracted from the Fourier series via a bandpass filter centered around f_s. This component is a carrier at 5 times the sampling frequency.

This illustration can be extended to show the following:

$$m(t)\cdot I_c(t)\Big|_{\substack{n=5\\ \emptyset=(t)}} = \frac{4\cdot m(t)}{5\pi}\left(\sin\left(5\omega_s t + 5\phi(t)\right)\right) \quad \text{EQ. (171)}$$

This equation illustrates that a message signal may have been superposed on I and $\bar{I}$ such that both amplitude and phase are modulated, i.e., $m(t)$ for amplitude and $\phi(t)$ for phase. In such cases, it should be noted that $\phi(t)$ is augmented modulo n while the amplitude modulation $m(t)$ is scaled. The point of this illustration is that complex waveforms may be reconstructed from their Fourier series with multi-aperture processor combinations, according to the present invention.

In a practical system according to an embodiment of the present invention, parasitics, filtering, etc., may modify $I_c(t)$. In many applications according to the present invention, charge injection properties of processors play a significant role. However, if the processors and the clock drive circuits according to embodiments of the present invention are matched then even the parasitics can be managed, particularly since unwanted distortions are removed by the final bandpass filter, which tends to completely reconstruct the waveform at passband.

Like the receiver embodiments of the present invention, which possess a lowpass information extraction and energy extraction impulse response, various transmitter embodiments of the present invention use a network to create a bandpass impulse response suitable for energy transfer and waveform reconstruction. In embodiments, the simplest reconstruction network is an L-C tank, which resonates at the desired carrier frequency $N\cdot f_s = f_c$.

V. Additional Embodiments

1. Example I/Q Modulation Receiver Embodiment

FIG. 197 illustrates an example I/Q modulation receiver 19700, according to an embodiment of the present invention. I/Q modulation receiver 19700 comprises a first Processing module 19702, a first optional filter 19704, a second Processing module 19706, a second optional filter 19708, a third Processing module 19710, a third optional filter 19712, a fourth Processing module 19714, a fourth filter 19716, an optional LNA 19718, a first differential amplifier 19720, a second differential amplifier 19722, and an antenna 19772.

I/Q modulation receiver 19700 receives, down-converts, and demodulates a I/Q modulated RF input signal 19782 to an I baseband output signal 19784, and a Q baseband output signal 19786. I/Q modulated RF input signal comprises a first information signal and a second information signal that are I/Q modulated onto an RF carrier signal. I baseband output signal 19784 comprises the first baseband information signal. Q baseband output signal 19786 comprises the second baseband information signal.

Antenna 19772 receives I/Q modulated RF input signal 19782. I/Q modulated RF input signal 19782 is output by antenna 19772 and received by optional LNA 19718. When present, LNA 19718 amplifies I/Q modulated RF input signal 19782, and outputs amplified I/Q signal 19788.

First Processing module 19702 receives amplified I/Q signal 19788. First Processing module 19702 down-converts the I-phase signal portion of amplified input I/Q signal 19788 according to an I control signal 19790. First Processing module 19702 outputs an I output signal 19798.

In an embodiment, first Processing module 19702 comprises a first storage module 19724, a first UFT module 19726, and a first voltage reference 19728. In an embodiment, a switch contained within first UFT module 19726 opens and closes as a function of I control signal 19790. As a result of the opening and closing of this switch, which respectively couples and de-couples first storage module 19724 to and from first voltage

reference 19728, a down-converted signal, referred to as I output signal 19798, results. First voltage reference 19728 may be any reference voltage, and is ground in some embodiments. I output signal 19798 is stored by first storage module 19724.

In an embodiment, first storage module 19724 comprises a first capacitor 19774. In addition to storing I output signal 19798, first capacitor 19774 reduces or prevents a DC offset voltage resulting from charge injection from appearing on I output signal 19798

I output signal 19798 is received by optional first filter 19704. When present, first filter 19704 is a high pass filter to at least filter I output signal 19798 to remove any carrier signal "bleed through". In an embodiment, when present, first filter 19704 comprises a first resistor 19730, a first filter capacitor 19732, and a first filter voltage reference 19734. Preferably, first resistor 19730 is coupled between I output signal 19798 and a filtered I output signal 19707, and first filter capacitor 19732 is coupled between filtered I output signal 19707 and first filter voltage reference 19734. Alternately, first filter 19704 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant arts. First filter 19704 outputs filtered I output signal 19707.

Second Processing module 19706 receives amplified I/Q signal 19788. Second Processing module 19706 down-converts the inverted I-phase signal portion of amplified input I/Q signal 19788 according to an inverted I control signal 19792. Second Processing module 19706 outputs an inverted I output signal 19701.

In an embodiment, second Processing module 19706 comprises a second storage module 19736, a second UFT module 19738, and a second voltage reference 19740. In an embodiment, a switch contained within second UFT module 19738 opens and closes as a function of inverted I control signal 19792. As a result of the opening and closing of this switch,

which respectively couples and de-couples second storage module 19736 to and from second voltage reference 19740, a down-converted signal, referred to as inverted I output signal 19701, results. Second voltage reference 19740 may be any reference voltage, and is preferably ground. Inverted I output signal 19701 is stored by second storage module 19736.

In an embodiment, second storage module 19736 comprises a second capacitor 19776. In addition to storing inverted I output signal 19701, second capacitor 19776 reduces or prevents a DC offset voltage resulting from above described charge injection from appearing on inverted I output signal 19701.

Inverted I output signal 19701 is received by optional second filter 19708. When present, second filter 19708 is a high pass filter to at least filter inverted I output signal 19701 to remove any carrier signal "bleed through". In an embodiment, when present, second filter 19708 comprises a second resistor 19742, a second filter capacitor 19744, and a second filter voltage reference 19746. In an embodiment, second resistor 19742 is coupled between inverted I output signal 19701 and a filtered inverted I output signal 19709, and second filter capacitor 19744 is coupled between filtered inverted I output signal 19709 and second filter voltage reference 19746. Alternately, second filter 19708 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant arts. Second filter 19708 outputs filtered inverted I output signal 19709.

First differential amplifier 19720 receives filtered I output signal 19707 at its non-inverting input and receives filtered inverted I output signal 19709 at its inverting input. First differential amplifier 19720 subtracts filtered inverted I output signal 19709 from filtered I output signal 19707, amplifies the result, and outputs I baseband output signal 19784. Other suitable subtractor modules may be substituted for first differential amplifier 19720, and second differential amplifier 19722, as would be understood by

persons skilled in the relevant arts from the teachings herein. Because filtered inverted I output signal 19709 is substantially equal to an inverted version of filtered I output signal 19707, I baseband output signal 19784 is substantially equal to filtered I output signal 19709, with its amplitude doubled. Furthermore, filtered I output signal 19707 and filtered inverted I output signal 19709 may comprise substantially equal noise and DC offset contributions of the same polarity from prior down-conversion circuitry, including first Processing module 19702 and second Processing module 19706, respectively. When first differential amplifier 19720 subtracts filtered inverted I output signal 19709 from filtered I output signal 19707, these noise and DC offset contributions substantially cancel each other.

Third Processing module 19710 receives amplified I/Q signal 19788. Third Processing module 19710 down-converts the Q-phase signal portion of amplified input I/Q signal 19788 according to an Q control signal 19794. Third Processing module 19710 outputs an Q output signal 19703.

In an embodiment, third Processing module 19710 comprises a third storage module 19748, a third UFT module 19750, and a third voltage reference 19752. In an embodiment, a switch contained within third UFT module 19750 opens and closes as a function of Q control signal 19794. As a result of the opening and closing of this switch, which respectively couples and de-couples third storage module 19748 to and from third voltage reference 19752, a down-converted signal, referred to as Q output signal 19703, results. Third voltage reference 19752 may be any reference voltage, and is preferably ground. Q output signal 19703 is stored by third storage module 19748.

In an embodiment, third storage module 19748 comprises a third capacitor 19778. In addition to storing Q output signal 19703, third capacitor 19778 reduces or prevents a DC offset voltage resulting from above described charge injection from appearing on Q output signal 19703.

Q output signal 19703 is received by optional third filter 19716. When present, third filter 19716 is a high pass filter to at least filter Q output signal 19703 to remove any carrier signal "bleed through". In an embodiment, when present, third filter 19712 comprises a third resistor 19754, a third filter capacitor 19758, and a third filter voltage reference 19758. In an embodiment, third resistor 19754 is coupled between Q output signal 19703 and a filtered Q output signal 19711, and third filter capacitor 19756 is coupled between filtered Q output signal 19711 and third filter voltage reference 19758. Alternately, third filter 19712 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant arts. Third filter 19712 outputs filtered Q output signal 19711.

Fourth Processing module 19714 receives amplified I/Q signal 19788. Fourth Processing module 19714 down-converts the inverted Q-phase signal portion of amplified input I/Q signal 19788 according to an inverted Q control signal 19796. Fourth Processing module 19714 outputs an inverted Q output signal 19705.

In an embodiment, fourth Processing module 19714 comprises a fourth storage module 19760, a fourth UFT module 19762, and a fourth voltage reference 19764. In an embodiment, a switch contained within fourth UFT module 19762 opens and closes as a function of inverted Q control signal 19796. As a result of the opening and closing of this switch, which respectively couples and de-couples fourth storage module 19760 to and from fourth voltage reference 19764, a down-converted signal, referred to as inverted Q output signal 19705, results. Fourth voltage reference 19764 may be any reference voltage, and is preferably ground. Inverted Q output signal 19705 is stored by fourth storage module 19760.

In an embodiment, fourth storage module 19760 comprises a fourth capacitor 19780. In addition to storing inverted Q output signal 19705,

fourth capacitor 19780 reduces or prevents a DC offset voltage resulting from above described charge injection from appearing on inverted Q output signal 19705.

Inverted Q output signal 19705 is received by optional fourth filter 19716. When present, fourth filter 19716 is a high pass filter to at least filter inverted Q output signal 19705 to remove any carrier signal "bleed through". In an embodiment, when present, fourth filter 19716 comprises a fourth resistor 19766, a fourth filter capacitor 19768, and a fourth filter voltage reference 19770. In an embodimnet, fourth resistor 19766 is coupled between inverted Q output signal 19705 and a filtered inverted Q output signal 19713, and fourth filter capacitor 19768 is coupled between filtered inverted Q output signal 19713 and fourth filter voltage reference 19770. Alternately, fourth filter 19716 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant arts. Fourth filter 19716 outputs filtered inverted Q output signal 19713.

Second differential amplifier 19722 receives filtered Q output signal 19711 at its non-inverting input and receives filtered inverted Q output signal 19713 at its inverting input. Second differential amplifier 19722 subtracts filtered inverted Q output signal 19713 from filtered Q output signal 19711, amplifies the result, and outputs Q baseband output signal 19786. Because filtered inverted Q output signal 19713 is substantially equal to an inverted version of filtered Q output signal 19711, Q baseband output signal 19786 is substantially equal to filtered Q output signal 19713, with its amplitude doubled. Furthermore, filtered Q output signal 19711 and filtered inverted Q output signal 19713 may comprise substantially equal noise and DC offset contributions of the same polarity from prior down-conversion circuitry, including third Processing module 19710 and fourth Processing module 19714, respectively. When second differential amplifier 19722 subtracts filtered inverted Q output signal 19713 from

filtered Q output signal 19711, these noise and DC offset contributions substantially cancel each other.

2. *Example I/Q Modulation Control Signal Generator Embodiments*

FIG. 198 illustrates an exemplary block diagram for an example I/Q modulation control signal generator 19800, according to an embodiment of the present invention. I/Q modulation control signal generator 19800 generates I control signal 19790, inverted I control signal 19792, Q control signal 19794, and inverted Q control signal 19796 used by I/Q modulation receiver 19700 of FIG. 197. I control signal 19790 and inverted I control signal 19792 operate to down-convert the I-phase portion of an input I/Q modulated RF signal. Q control signal 19794 and inverted Q control signal 19796 act to down-convert the Q-phase portion of the input I/Q modulated RF signal. Furthermore, I/Q modulation control signal generator 19800 has the advantage of generating control signals in a manner such that resulting collective circuit re-radiation is radiated at one or more frequencies outside of the frequency range of interest. For instance, potential circuit re-radiation is radiated at a frequency substantially greater than that of the input RF carrier signal frequency.

I/Q modulation control signal generator 19800 comprises a local oscillator 19802, a first divide-by-two module 19804, a 180 degree phase shifter 19806, a second divide-by-two module 19808, a first pulse generator 19810, a second pulse generator 19812, a third pulse generator 19814, and a fourth pulse generator 19816.

Local oscillator 19802 outputs an oscillating signal 19818. FIG. 199 shows an exemplary oscillating signal 19818.

First divide-by-two module 19804 receives oscillating signal 19818, divides oscillating signal 19818 by two, and outputs a half frequency LO

signal 19820 and a half frequency inverted LO signal 19826. FIG. 199 shows an exemplary half frequency LO signal 19820. Half frequency inverted LO signal 19826 is an inverted version of half frequency LO signal 19820. First divide-by-two module 19804 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant arts.

180 degree phase shifter 19806 receives oscillating signal 19818, shifts the phase of oscillating signal 19818 by 180 degrees, and outputs phase shifted LO signal 19822. 180 degree phase shifter 19806 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant arts. In alternative embodiments, other amounts of phase shift may be used.

Second divide-by two module 19808 receives phase shifted LO signal 19822, divides phase shifted LO signal 19822 by two, and outputs a half frequency phase shifted LO signal 19824 and a half frequency inverted phase shifted LO signal 19828. FIG. 199 shows an exemplary half frequency phase shifted LO signal 19824. Half frequency inverted phase shifted LO signal 19828 is an inverted version of half frequency phase shifted LO signal 19824. Second divide-by-two module 19808 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant arts.

First pulse generator 19810 receives half frequency LO signal 19820, generates an output pulse whenever a rising edge is received on half frequency LO signal 19820, and outputs I control signal 19790. FIG. 199 shows an exemplary I control signal 19790.

Second pulse generator 19812 receives half frequency inverted LO signal 19826, generates an output pulse whenever a rising edge is received on half frequency inverted LO signal 19826, and outputs inverted I control

signal 19792. FIG. 199 shows an exemplary inverted I control signal 19792.

Third pulse generator 19814 receives half frequency phase shifted LO signal 19824, generates an output pulse whenever a rising edge is received on half frequency phase shifted LO signal 19824, and outputs Q control signal 19794. FIG. 199 shows an exemplary Q control signal 19794.

Fourth pulse generator 19816 receives half frequency inverted phase shifted LO signal 19828, generates an output pulse whenever a rising edge is received on half frequency inverted phase shifted LO signal 19828, and outputs inverted Q control signal 19796. FIG. 199 shows an exemplary inverted Q control signal 19796.

In an embodiment, control signals 19790, 19792, 19794 and 19796 output pulses having a width equal to one-half of a period of I/Q modulated RF input signal 19782. The invention, however, is not limited to these pulse widths, and control signals 19790, 19792, 19794, and 19796 may comprise pulse widths of any fraction of, or multiple and fraction of, a period of I/Q modulated RF input signal 19782. Also, other circuits for generating control signals 19790, 19792, 19794, and 19796 will be apparent to persons skilled in the relevant arts based on the herein teachings.

First, second, third, and fourth pulse generators 19810, 19812, 19814, and 19816 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant arts.

As shown in FIG. 199, in embodiments control signals 19790, 19792, 19794, and 19796 comprise pulses that are non-overlapping. Furthermore, in this example, pulses appear on these signals in the following order: I control signal 19790, Q control signal 19794, inverted I control signal 19792, and inverted Q control signal 19796. Potential circuit

re-radiation from I/Q modulation receiver 19700 may comprise frequency components from a combination of these control signals.

For example, FIG. 200 shows an overlay of pulses from I control signal 19790, Q control signal 19794, inverted I control signal 19792, and inverted Q control signal 19796. When pulses from these control signals leak through first, second, third, and fourth Processing modules 19702, 19706, 19710, and 19714 to antenna 19782 (shown in FIG. 197), they may be radiated from I/Q modulation receiver 19700, with a combined waveform that appears to have a primary frequency equal to four times the frequency of any single one of control signals 19790, 19792, 19794, and 19796. FIG. 199 shows an example combined control signal 19902.

FIG. 200 also shows an example I/Q modulation RF input signal 19782 overlaid upon control signals 19790, 19792, 19794, and 19796. As shown in FIG. 200, pulses on I control signal 19790 overlay and act to down-convert a positive I-phase portion of I/Q modulation RF input signal 19782. Pulses on inverted I control signal 19792 overlay and act to down-convert a negative I-phase portion of I/Q modulation RF input signal 19782. Pulses on Q control signal 19794 overlay and act to down-convert a rising Q-phase portion of I/Q modulation RF input signal 19782. Pulses on inverted Q control signal 19796 overlay and act to down-convert a falling Q-phase portion of I/Q modulation RF input signal 19782.

As FIG. 200 further shows in this example, the frequency ratio between the combination of control signals 19790, 19792, 19794, and 19796 and I/Q modulation RF input signal 19782 is 4:3. Because the frequency of the potentially re-radiated signal, combined control signal 19902, is substantially different from that of the signal being down-converted, I/Q modulation RF input signal 19782, it does not interfere with signal down-conversion as it is out of the frequency band of interest, and hence may be filtered out. In this manner, I/Q modulation receiver 19700 reduces

problems due to circuit re-radiation. As will be understood by persons skilled in the relevant arts from the teachings herein, frequency ratios other than 4:3 may be implemented to achieve similar reduction of problems of circuit re-radiation.

It should be understood that the above control signal generator circuit example is provided for illustrative purposes only. The invention is not limited to these embodiments. Alternative embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) for I/Q modulation control signal generator 19800 will be apparent to persons skilled in the relevant arts from the teachings herein, and are within the scope of the present invention.

3. Detailed Example I/Q Modulation Receiver Embodiment with Exemplary Waveforms

FIG. 201 illustrates a more detailed example circuit implementation of I/Q modulation receiver 19700, according to an embodiment of the present invention. FIGS. 202-40 show waveforms related to an example implementation of I/Q modulation receiver 19700 of FIG. 201.

FIGS. 202 and 203 show first and second input data signals 20102 and 20104 to be I/Q modulated with a RF carrier signal frequency as the I-phase and Q-phase information signals, respectively.

FIGS. 205 and 206 show the signals of FIG. 202 and 203 after modulation with a RF carrier signal frequency, respectively, as I-modulated signal 20106 and Q-modulated signal 20108.

FIG. 204 shows an I/Q modulation RF input signal 19782 formed from I-modulated signal 20106 and Q-modulated signal 20108 of FIGS. 205 and 206, respectively.

FIG. 211 shows an overlaid view of filtered I output signal 21102 and filtered inverted I output signal 21104.

FIG. 212 shows an overlaid view of filtered Q output signal 21202 and filtered inverted Q output signal 21204.

FIGS. 207 and 208 show I baseband output signal 19784 and Q baseband output signal 19786, respectfully. A data transition 20402 is indicated in both I baseband output signal 19784 and Q baseband output signal 19786. The corresponding data transition 20402 is indicated in I-modulated signal 20106 of FIG. 205, Q-modulated signal 20108 of FIG. 206, and I/Q modulation RF input signal 19782 of FIG. 204.

FIGS. 209 and 210 show I baseband output signal 19784 and Q baseband output signal 19786 over a wider time interval.

4. Example Single Channel Receiver Embodiment

FIG. 213 illustrates an example single channel receiver 21300, corresponding to either the I or Q channel of I/Q modulation receiver 19700, according to an embodiment of the present invention. Single channel receiver 21300 can down-convert an input RF signal 21306 modulated according to AM, PM, FM, and other modulation schemes. Refer to the section above for further description on the operation of single channel receiver 21300.

5. Example Automatic Gain Control (AGC) Embodiment

According to embodiments of the invention, the amplitude level of the down-converted signal can be controlled by modifying the aperture of the control signal that controls the switch module. Consider FIG. 43, that illustrates an equation that represents the change in charge in the storage device of embodiments of the UFT module, such as a capacitor. This equation is a function of T, which is the aperture of the control signal. Thus, by modifying the aperture T of the control signal, it is possible to modify the amplitude level of the down-converted signal.

Some embodiments may include a control mechanism to enable manual control of aperture T, and thus manual control of the amplitude level of the down-converted signal. Other embodiments may include automatic or semi-automatic control modules to enable automatic or semi-automatic control of aperture T, and thus automatic or semi-automatic control of the amplitude level of the down-converted signal. Such embodiments are herein referred to (without limitation) as automatic gain control (AGC) embodiments. Other embodiments include a combination of manual and automatic control of aperture T.

6. Other Example Embodiments

Additional aspects/embodiments of the invention are considered in this section.

In one embodiment of the present invention there is provided a method of transmitting information between a transmitter and a receiver comprising the steps of transmitting a first series of signals each having a known period from the transmitter at a known first repetition rate; sampling by the receiver each signal in the first series of signals a single time and for a known time interval the sampling of the first series of signals being at a second repetition rate that is a rate different from the first repetition rate by a known amount; and generating by the receiver an output signal indicative of the signal levels sampled in step B and having a period longer than the known period of a transmitted signal.

In another embodiment of the invention there is provided a communication system comprising a transmitter means for transmitting a first series of signals of known period at a known first repetition rate, a receiver means for receiving the first series of signals, the receiver means including sampling means for sampling the signal level of each signal first series of signals for a known time interval at a known second repetition rate,

the second repetition rate being different from the first repetition rate by a known amount as established by the receiver means. The receiver means includes first circuit means for generating a first receiver output signal indicative of the signal levels sampled and having a period longer than one signal of the first series of signals. The transmitter means includes an oscillator for generating an oscillator output signal at the first repetition rate, switch means for receiving the oscillator output signal and for selectively passing the oscillator output signal, waveform generating means for receiving the oscillator output signal for generating a waveform generator output signal having a time domain and frequency domain established by the waveform generating means.

The embodiment of the invention described herein involves a single or multi-user communications system that utilizes coherent signals to enhance the system performance over conventional radio frequency schemes while reducing cost and complexity. The design allows direct conversion of radio frequencies into baseband components for processing and provides a high level of rejection for signals that are not related to a known or controlled slew rate between the transmitter and receiver timing oscillators. The system can be designed to take advantage of broadband techniques that further increase its reliability and permit a high user density within a given area. The technique employed allows the system to be configured as a separate transmitter-receiver pair or a transceiver.

An objective of the present system is to provide a new communication technique that can be applied to both narrow and wide band systems. In its most robust form, all of the advantages of wide band communications are an inherent part of the system and the invention does not require complicated and costly circuitry as found in conventional wide band designs. The communications system utilizes coherent signals to send and receive information and consists of a transmitter and a receiver in its

simplest form. The receiver contains circuitry to turn its radio frequency input on and off in a known relationship in time to the transmitted signal. This is accomplished by allowing the transmitter timing oscillator and the receiver timing oscillator to operate at different but known frequencies to create a known slew rate between the oscillators. If the slew rate is small compared to the timing oscillator frequencies, the transmitted waveform will appear stable in time, i.e., coherent (moving at the known slew rate) to the receiver's switched input. The transmitted waveform is the only waveform that will appear stable in time to the receiver and thus the receiver's input can be averaged to achieve the desired level filtering of unwanted signals. This methodology makes the system extremely selective without complicated filters and complex encoding and decoding schemes and allows the direct conversion of radio frequency energy from an antenna or cable to baseband frequencies with a minimum number of standard components further reducing cost and complexity. The transmitted waveform can be a constant carrier (narrowband), a controlled pulse (wideband and ultra-wideband) or a combination of both such as a dampened sinusoidal wave and or any arbitrary periodic waveform thus the system can be designed to meet virtually any bandwidth requirement. Simple standard modulation and demodulation techniques such as AM and Pulse Width Modulation can be easily applied to the system.

Depending on the system requirements such as the rate of information transfer, the process gain, and the intended use, there are multiple preferred embodiments of the invention. The embodiment discussed herein will be the amplitude and pulse width modulated system. It is one of the simplest implementations of the technology and has many common components with the subsequent systems. A amplitude modulated transmitter consists of a Transmitter Timing Oscillator, a Multiplier, a Waveform Generator, and an Optional Amplifier. The Transmitter Timing

Oscillator frequency can be determined by a number of resonate circuits including an inductor and capacitor, a ceramic resonator, a SAW resonator, or a crystal. The output waveform is sinusoidal, although a squarewave oscillator would produce identical system performance.

The Multiplier component multiplies the Transmitter Timing Oscillator output signal by 0 or 1 or other constants, K1 and K2, to switch the oscillator output on and off to the Waveform Generator. In this embodiment, the information input can be digital data or analog data in the form of pulse width modulation. The Multiplier allows the Transmitter Timing Oscillator output to be present at the Waveform Generator input when the information input is above a predetermined value. In this state the transmitter will produce an output waveform. When the information input is below a predetermined value, there is no input to the Waveform Generator and thus there will be no transmitter output waveform. The output of the Waveform Generator determines the system's bandwidth in the frequency domain and consequently the number of users, process gain immunity to interference and overall reliability), the level of emissions on any given frequency, and the antenna or cable requirements. The Waveform Generator in this example creates a one cycle pulse output which produces an ultra-wideband signal in the frequency domain. An optional power Amplifier stage boosts the output of the Waveform Generator to a desired power level.

With reference now to the drawings, the amplitude and pulse width modulated transmitter in accord with the present invention is depicted at numeral 13000 in FIGS. 130 and 131. The Transmitter Timing Oscillator 13002 is a crystal-controlled oscillator operating at a frequency of 25 MHZ. Multiplier 13004 includes a two-input NAND gate 13102 controlling the gating of oscillator 13002 output to Waveform Generator 13006. Waveform Generator 13006 produces a pulse output as depicted at 13208 in FIGS.

132D and 133, which produces a frequency spectrum 13402 in FIG. 134. Amplifier 13008 is optional. The transmitter 13000 output is applied to antenna or cable 13010, which as understood in the art, may be of various designs as appropriate in the circumstances.

FIGS. 132A – 132D, 133, and134 illustrate the various signals present in transmitter 13000. The output of transmitter 13000 at "A" may be either a sinusoidal or squarewave signal 13202 that is provided as one input into NAND gate 13102. Gate 13102 also receives an information signal 13204 at "B" which, in the embodiment shown, is digital in form. The output 13206 of Multiplier 13004 can be either sinusoidal or squarewave depending upon the original signal 13202. Waveform Generator 13006 provides an output of a single cycle impulse signal 13208. The single cycle impulse 13210 varies in voltage around a static level 13212 and is created at 40 nanoseconds intervals. In the illustrated embodiment, the frequency of transmitter 13002 is 25 MHZ and accordingly, one cycle pulses of 1.0 GHZ are transmitted every 40 nanoseconds during the total time interval that gate 13102 is "on" and passes the output of transmitter oscillator 13002.

FIG. 135 shows the preferred embodiment receiver block diagram to recover the amplitude or pulse width modulated information and consists of a Receiver Timing Oscillator 13510, Waveform Generator 13508, RF Switch Fixed or Variable Integrator 13506, Decode Circuit 13514, two optional Amplifier/Filter stages 13504 and 13512, antenna or cable input 13502, and Information Output 13516. The Receiver Timing Oscillator 13510 frequency can be determined by a number of resonate circuits including an inductor and capacitor, a ceramic resonator, a SAW resonator, or a crystal. As in the case of the transmitter, the oscillator 13510 shown here is a crystal oscillator. The output waveform is a squarewave, although a sinewave oscillator would produce identical system performance. The

squarewave timing oscillator output 13602 is shown in FIG. 136A. The Receiver Timing Oscillator 13510 is designed to operate within a range of frequencies that creates a known range of slew rates relative to the Transmitter Timing Oscillator 13002. In this embodiment, the Transmitter Timing Oscillator 13002 frequency is 25 MHZ and the Receiver Timing Oscillator 13510 outputs between 25.0003 MHZ and 25.0012 MHZ which creates a +300 to +1200 Hz slew rate.

The Receiver Timing Oscillator 13510 is connected to the Waveform Generator 13508 which shapes the oscillator signal into the appropriate output to control the amount of the time that the RF switch 13506 is on and off. The on-time of the RF switch 13506 should be less than ½ of a cycle (1/10 of a cycle is preferred) or in the case of a single pulse, no wider than the pulse width of the transmitted waveform or the signal gain of the system will be reduced. Examples are illustrated in Table A1. Therefore the output of the Waveform Generator 13508 is a pulse of the appropriate width that occurs once per cycle of the receiver timing oscillator 13510. The output 13604 of the Waveform Generator is shown in FIG. 136B.

Transmitted Waveform	Gain Limit on-time	Preferred on-time
Single 1 nanosecond pulse	1 nanosecond	100 picoseconds
1 Gigahertz 1,2,3..etc. cycle output	500 picoseconds	50 picoseconds
10 Gigahertz 1,2,3..etc. cycle output	50 picoseconds	5 picoseconds

Table A1

The RF Switch/Integrator 13506 samples the RF signal 13606 shown in FIG. 136C when the Waveform Generator output 13604 is below a predetermined value. When the Waveform Generator output 13604 is above a predetermined value, the RF Switch 13506 becomes a high impedance node and allows the Integrator to hold the last RF signal sample 13606 until the next cycle of the Waveform Generator 13508 output. The Integrator section of 13506 is designed to charge the Integrator quickly (fast attack) and discharge the Integrator at a controlled rate (slow decay). This embodiment provides unwanted signal rejection and is a factor in determining the baseband frequency response of the system. The sense of the switch control is arbitrary depending on the actual hardware implementation.

In an embodiment of the present invention, the gating or sampling rate of the receiver 13500 is 300 Hz higher than the 25 MHZ transmission rate from the transmitter 13000. Alternatively, the sampling rate could be less than the transmission rate. The difference in repetition rates between the transmitter 13000 and receiver 13500, the "slew rate," is 300 Hz and results in a controlled drift of the sampling pulses over the transmitted pulse which thus appears "stable" in time to the receiver 13500. With reference now to FIGS. 132A – 132D and 136A – 136G, an example is illustrated for a simple case of an output signal 13608 (FIG. 136D) that is constructed of four samples from four RF input pulses 13606 for ease of explanation. As can be clearly seen, by sampling the RF pulses 13606 passed when the

transmitter information signal 13204 (FIG. 132B) is above a predetermine threshold the signal 13608 is a replica of a signal 13606 but mapped into a different time base. In the case of this example, the new time base has a period four times longer than real time signal. The use of an optional amplifier/filter 13512 results in a further refinement of the signal 13608 which is present shown as signal 13610 in FIG 136E.

Decode Circuitry 13514 extracts the information contained in the transmitted signal and includes a Rectifier that rectifies signal 13608 or 13610 to provide signal 13612 in FIG. 136G. The Variable Threshold Generator circuitry in circuit 13514 provides a DC threshold signal level 13614 for signal 13610 that is used to determine a high (transmitter output on) or low (transmitter output off) and is also shown in FIG 136G. The final output signal 13616 shown in FIG. 136F is created by an output voltage comparator in circuit 13514 that combines signals 13612 and 13614 such that when the signal 13612 is a higher voltage than signal 13614, the information output signal goes high. Accordingly, signal 13616 represents, for example, a digital "1" that is now time-based to a 1:4 expansion of the period of an original signal 13606. While this illustration provides a 4:1 reduction in frequency, it is sometimes desired to provide a reduction of more than 50,000:1; in the preferred embodiment, 100,000:1 or greater is achieved. This results in a shift directly from RF input frequency to low frequency baseband without the requirement of expensive intermediate circuitry that would have to be used if only a 4:1 conversion was used as a first stage. Table A2 provides information as to the time base conversion and includes examples.

Units

s = 1 ps = 1_10^{12} ns = 1_10^{-9} us = 1_10^{-6} MHz = 1_10^{6} KHz = 1_10^{3}

Receiver Timing Oscillator Frequency = 25.0003 MHz

Transmitter Timing Oscillator Frequency = 25 MHz

$$\text{period} = \frac{1}{\text{Transmitter Timing Oscillator Frequency}}$$

period = 40 ns

$$\text{slew rate} = \frac{1}{\text{Receiver Timing Oscillator Frequency} - \text{Transmitter Timing Oscillator Frequency}}$$

slew rate =0.003 s

$$\text{time base multiplier} = \frac{\text{slew rate}}{\text{period}} \text{ seconds per nanosecond}$$

time base multiplier = 8.333_10^{4}

Example 1:

1 nanosecond translates into 83.33 microseconds

time base = (1 ns)_ time base multiplier

time base = 83.333 us

Example 2:

2 Gigahertz translates into 24 Kilohertz 2 Gigahertz = 500 picosecond period

time base = (500 ps)_ time base multiplier

time base = 41.667 us

$$\text{frequency} = \frac{1}{\text{time base}}$$

frequency = 24 KHz

Table A2

In the illustrated embodiment, the signal 13616 at "F" has a period of 83.33 usec, a frequency of 12 KHz and it is produced once every 3.3 msec for a 300 Hz slew rate. Stated another way, the system is converting a 1 gigahertz transmitted signal into an 83.33 microsecond signal.

Accordingly, the series of RF pulses 13210 that are transmitted during the presence of an "on" signal at the information input gate 13102 are used to reconstruct the information input signal 13204 by sampling the series of pulses at the receiver 13500. The system is designed to provide an adequate number of RF inputs 13606 to allow for signal reconstruction.

An optional Amplifier/Filter stage or stages 13504 and 13512 may be included to provide additional receiver sensitivity, bandwidth control or signal conditioning for the Decode Circuitry 13514. Choosing an appropriate time base multiplier will result in a signal at the output of the Integrator 13506 that can be amplified and filtered with operational amplifiers rather than RF amplifiers with a resultant simplification of the design process. The signal 13610 shown in FIG 136E illustrates the use of Amplifier/Filter 13512 (FIG. 137). The optional RF amplifier 13504 shown as the first stage of the receiver should be included in the design when increased sensitivity and/or additional filtering is required. Example receiver schematics are shown in FIGS. 137-139.

FIGS. 140-143 illustrate different pulse output signals 14002 and 14202 and their respective frequency domain at 14102 and 14302. As can be seen from FIGS. 140 and 141, the half-cycle signal 14002 generates a spectrum less subject to interference than the single cycle of FIG. 133 and the 10-cycle pulse of FIG. 142. The various outputs determine the system's immunity to interference, the number of users in a given area, and the cable and antenna requirements. FIGS. 133 and 134 illustrate example pulse outputs.

FIGS. 144 and 145 show example differential receiver designs. The theory of operation is similar to the non-differential receiver of FIG. 135 except that the differential technique provides an increased signal to noise ratio by means of common mode rejection. Any signal impressed in phase at both inputs on the differential receiver will attenuated by the differential amplifier shown in FIGS. 144 and 145 and conversely any signal that produces a phase difference between the receiver inputs will be amplified.

FIGS. 146 and 147 illustrate the time and frequency domains of a narrow band/constant carrier signal in contrast to the ultra-wide band signals used in the illustrated embodiment.

VI. Additional Features of the Invention

1. Architectural Features of the Invention

The present invention provides, among other things, the following architectural features:

optimal baseband signal to noise ratio regardless of modulation (programmable RF matched filter);

exceptional linearity per milliwatt consumed;

easily integrated into bulk C-MOS (small size/low cost, high level of integration);

fundamental or sub-harmonic operation (does not change conversion efficiency);

transmit function provides frequency multiplication and signal gain; and

optimal power transfer into a scalable output impedance (independent of device voltage or current);

The present invention provides simultaneous solutions for two domains: power sampling and matched filtering. A conventional sampler is a voltage sampling device, and does not substantially affect the input signal. A power sampler according to the present invention attempts to take as much power from the input to construct the output, and does not necessarily preserve the input signal.

2. Additional Benefits of the Invention

2.1 Compared to an Impulse Sampler

The present invention out-performs a theoretically perfect impulse sampler. The performance of a practical implementation of the present invention exceeds the performance of a practical implementation of an impulse sampler. The present invention is easily implemented (does not require impulse circuitry).

2.2 Linearity

The present invention provides exceptional linearity per milliwatt. For example, rail to rail dynamic range is possible with minimal increase in power. In an example integrated circuit embodiment, the present invention provides +55dmb IP2, +15 dbm IP3, @ 3.3V, 4.4ma, -15dmb LO. GSM

system requirements are +22dbm IP2, -10.5dmb IP3. CDMA system requirements are +50dmb IP2, +10dbm IP3.

2.3 Optimal Power Transfer into a Scalable Output Impedance

In an embodiment of the present invention, output impedance is scalable to facilitate a low system noise figure. In an embodiment, changes in output impedance do not affect power consumption.

2.4 System Integration

In an embodiment, the present invention enables a high level of integration in bulk C-MOS. Other features include:

small footprint;

no multiplier circuits (no device matching or balancing transistors);

transmit and receive filters at baseband;

low frequency synthesizers;

DC offset solutions;

Referring to FIG. 218A, a single-switch, differential input, differential output receiver 21800, according to an embodiment of the present invention, is shown. If an I/Q signal is being received, receiver 21800 could be implemented for each of the I- and Q-phase signals. No balanced transistor is required in receiver 21800. Any charge injection that creates a DC offset voltage on a first switch input 21802 creates a substantially equal DC offset voltage on a second switch input 21804, so that any resulting DC offset due to charge injection is substantially canceled.

In an embodiment, LO signal 21806 runs at a sub-harmonic. Gilbert cells lose efficiency when run at a sub-harmonic, as compared to the receiver of the present invention.

FIG. 218A shows a substantially maximal linearity configuration. The drain and source voltages are virtually fixed in relation to V_{gs}. The DC voltage across first switch input 21802 and second switch input 21804 remains substantially constant.

Single-switch, differential input, differential output receiver embodiments according to the present invention, are discussed in further detail elsewhere herein.

architecturally reduces re-radiation;

Referring to FIG. 218A, re-radiation is substantially all common mode. With a perfect splitter, the re-radiation will be substantially eliminated.

Referring to FIG. 218B, a first switch 21810 and a second switch 21812 are implemented in a receiver 21814, according to an embodiment of the present invention. Receiver 21814 moves re-radiation off frequency to the next even harmonic frequency higher. Referring to FIG. 218D, re-radiation was substantially shifted from 2.49 GHz (see re-radiation spike 21818) to 3.29 GHz (see larger re-radiation spike 21820).

Receiver embodiments, according to the present invention, for reducing or eliminating circuit re-radiation, such as receiver 21814, are

discussed in further detail elsewhere herein.

inherent noise rejection; and
lower cost.

2.5 Fundamental or Sub-Harmonic Operation

Sub-harmonic operation is preferred for many direct down-conversion implementations because it tends to avoid oscillators and/or signals near the desired operating frequency.

Conversion efficiency is generally constant regardless of the sub-harmonic. Sub-harmonic operation enables micro power receiver designs.

2.6 Frequency Multiplication and Signal Gain

A transmit function in accordance with the present invention provides frequency multiplication and signal gain. For example, a 900 MHz design example (0.35 μ CMOS) embodiment features -15 dbm 180 MHz LO, 0 dbm 900 MHz I/O output, 5 VDC, 5 ma. A 2400 MHz design example (0.35 μ CMOS) embodiment features -15 dbm 800 MHz LO, -6 dbm 2.4 GHz I/O output, 5 VDC, 16 ma.

A transmit function in accordance with the present invention also provides direct up-conversion (true zero IF).

3. Controlled Aperture Sub-Harmonic Matched Filter Features

3.1 Non-Negligible Aperture

A non-negligible aperture, as taught herein, substantially preserves amplitude and phase information, but not necessarily the carrier signal. A general concept is to under-sample the carrier while over sampling the information.

The present invention transfers optimum energy. Example embodiments have been presented herein, including DC examples and carrier half cycle examples.

3.2 Bandwidth

With regard to input bandwidth, optimum energy transfer generally occurs every n + ½ cycle. Output bandwidth is generally a function of the LO.

3.3 Architectural Advantages of a Universal Frequency Down-Converter

A universal frequency down-converter (UDF), in accordance with the invention, can be designed to provides, among other things, the following features:

filter Q's of 100,000+;
filters with gain;
filter integration in CMOS;
electrically modified center frequency and bandwidth;
stable filter parameters in the presence of high level signals; and
UDF's can be mass produced without tuning.

3.4 Complimentary FET Switch Advantages

Complimentary FET switch implementations of the invention provide, among other things, increased dynamic range (lower Rds_{on} - increased conversion efficiency, higher IIP2, IIP3, minimal current increase (+ CMOS inverter), and lower re-radiation (charge cancellation). For example, refer to FIGS. 240 and 241.

3.5 Differential Configuration Characteristics

Differential configuration implementations of the invention provide, among other things, DC off-set advantages, lower re-radiation, input and output common mode rejection, and minimal current increase. For example, refer to FIG. 242.

3.6 Clock Spreading Characteristics

Clock spreading aspects of the invention provide, among other things, lower re-radiation, DC off-set advantages, and flicker noise advantages. For example, refer to FIGS. 243-245.

3.7 Controlled Aperture Sub Harmonic Matched Filter Principles

The invention provides, among other things, optimization of signal to noise ratio subject to maximum energy transfer given a controlled aperture, and maximum energy transfer while preserving information. The invention also provides bandpass wave form auto sampling and pulse energy accumulation

3.8 Effects of Pulse Width Variation

Pulse width can be optimized for a frequency of interest. Generally, pulse width is n plus ½ cycles of a desired input frequency. Generally, in CMOS implementations of the invention, pulse width variation across process variations and temperature of interest is less than +/- 16 percent.

4. Conventional Systems

4.1 Heterodyne Systems

Conventional heterodyne systems, in contrast to the present invention, are relatively complex, require multiple RF synthesizers, require management of various electromagnetic modes (shield, etc.), require significant inter-modulation management, and require a myriad of technologies that do not easily integrate onto integrated circuits.

4.2 Mobile Wireless Devices

High quality mobile wireless devices have not been implemented via zero IF because of the high power requirements for the first conversion in order to obtain necessary dynamic range, the high level of LO required (LO re-radiation), adjacent channel interference rejection filtering, transmitter modulation filtering, transmitter LO leakage, and limitations on RF synthesizer performance and technology.

5. Phase Noise Cancellation

The complex phasor notation of a harmonic signal is known from Euler's equation, shown here as equation 172.

$$S(t) = e^{-j(\omega_c t + \varphi)}$$

EQ. (172)

Suppose that φ is also some function of time φ(t). φ(t) represents phase noise or some other phase perturbation of the waveform. Furthermore, suppose that φ(t) and -φ(t) can be derived and manipulated. Then if follows that the multiplication of $S_1(t)$ and $S_2(t)$ will yield equation 173.

$$S(t) = S_1(t) \bullet S_2(t) = e^{-j(\omega_c t + \varphi(t))} \bullet e^{-j(\omega_c t - \varphi(t))} = e^{-j2\omega_c t}$$

EQ. (173)

Thus, the phase noise φ(t) can be canceled. Trigonometric identities verify the same result except for an additional term at DC. This can be implemented with, for example, a four-quadrant version of the invention. FIG. 268 illustrates an implementation for a doubler (2X clock frequency and harmonics thereof). FIG. 269 illustrates another implementation (harmonics with odd order phase noise canceling).

In an embodiment two clocks are utilized for phase noise cancellation of odd and even order harmonics by cascading stages. A four quadrant implementation of the invention can be utilized to eliminate the multiplier illustrated in FIG. 269.

6. Multiplexed UFD

In an embodiment, parallel receivers and transmitters are implemented using single pole, double throw, triple throw, etc.,

implementations of the invention.

A multiple throw implementation of the invention can also be utilized. In this embodiment, many frequency conversion options at multiple rates can be performed in parallel or serial. This can be implemented for multiple receive functions, multi-band radios, multi-rate filters, etc.

7. Sampling Apertures

Multiple apertures can be utilized to accomplish a variety of effects. For example, FIG. 270 illustrates a bipolar sample aperture and a corresponding sine wave being sampled. The bipolar sample aperture IS operated at a sub harmonic of the sine wave being sampled. By calculating the Pourier transform of each component within the Pourier series, it can be shown that the sampling power spectrum goes to zero at the sub harmonics and super harmonics. As a result, the comb spectrum is substantially eliminated except at the conversion frequency.

Similarly, the number of apertures can be extended with associated bipolar weighting to form a variety of impulse responses and to perform filtering at RF.

8. Diversity Reception and Equalizers

The present invention can be utilized to implement maximal ratio post detection combiners, equal gain post detection combiners, and selectors.

FIG. 271 illustrates an example diversity receiver implemented in accordance with the present invention.

Electronic Patent Application Fee Transmittal

Application Number:	14172392
Filing Date:	04-Feb-2014
Title of Invention:	Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same, and Aperture Relationships
First Named Inventor/Applicant Name:	David F. Sorrells
Filer:	Rick D. Nydegger/Ralene Eller
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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/172,392	02/04/2014	David F. Sorrells	19200.1.1.1.2.2.1.2	8448

TITLE OF INVENTION: Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same, and Aperture Relationships

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	06/12/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
BHATTACHARYA, SAM	2646	455-313000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Workman Nydegger
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: ParkerVision, Inc.
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Jacksonville, Florida

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
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- ☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 23-3178 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ☐ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ☐ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Rick D. Nydegger/ Date April 28, 2015
Typed or printed name Rick D. Nydegger Registration No. 28,651

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Electronic Acknowledgement Receipt

EFS ID:	22185116
Application Number:	14172392
International Application Number:	
Confirmation Number:	8448
Title of Invention:	Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same, and Aperture Relationships
First Named Inventor/Applicant Name:	David F. Sorrells
Customer Number:	22913
Filer:	Rick D. Nydegger/Ralene Eller
Filer Authorized By:	Rick D. Nydegger
Attorney Docket Number:	19200.1.1.1.2.2.1.2
Receipt Date:	28-APR-2015
Filing Date:	04-FEB-2014
Time Stamp:	10:08:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$960
RAM confirmation Number	11989
Deposit Account	233178
Authorized User	NYDEGGER, RICK D.

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	19200-1-1-1-2-2-1-2_2015-04-28_Issue-fee-transmittal.pdf	145992 39094d245765a0bcdc6c093dda1c3f5f756316a0	no	1
Warnings:					
Information:					
2	Miscellaneous Incoming Letter	19200-1-1-1-2-2-1-2_2015-04-28_Comment-on-Reasons-for-Allowance.pdf	91096 9861351c6f6e4a79bbd0b43809902ce5edfd0452	no	1
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30582 e5896aafb38c33c488d7ce000c7d2147906f84fd	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	267670		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

FILED ELECTRONICALLY

PATENT APPLICATION
Docket No: 19200.1.1.1.2.2.1.2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	David F. Sorrells et al.	)
Serial No.:	14/172,392	) Art Unit) 2646
Filed:	Feb. 4, 2014	)
Conf. No.:	8448	)
For:	Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same, and Aperture Relationships	)
Examiner:	Sam Bhattacharya	)
Customer No.:	22913	)

Comments on Statement of Reasons for Allowance

Applicants respectfully submit that the claimed invention as set forth in each of the independent claims and the dependent claims must be read as a whole, and not as a single feature or subcombination of features which represent less than the entirety of the claimed invention as a whole. While a particular feature or subcombination of features referred to by the Examiner in the Statement of Reasons for Allowance may represent a basis for distinguishing the claimed invention over the prior art, Applicants further submit that this may not necessarily be the *sole* ground for distinguishing the claimed invention over the prior art of record. Accordingly, the Examiner's statement should, in Applicants' view, not be read as constituting or meaning that the invention can or should be reduced to a single "feature" of the invention or to a subcombination of features that is less than the entire invention claimed as a whole, nor that the single feature referenced by the Examiner or subcombination of features referenced by the Examiner in the Statement of Reasons for Allowance is the only or sole grounds for distinguishing the invention over the prior art of record, or that applicants necessarily agree with any characterization of the prior art set forth in the Statement of Reasons for Allowance.

Dated this 28th day of April, 2015.

Respectfully submitted,

Rick D. Nydegger
Attorney for Applicant
Registration No. 28,651
Customer No. 047973

RDN:re
5107671_1

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14/172,392
	Filing Date	2014-02-04
	First Named Inventor	David F. Sorrells
	Art Unit	2646
	Examiner Name	Sam Bhattacharya
	Attorney Docket Number	19200.1.1.1.2.2.1.2

U.S. PATENT APPLICATIONS

Examiner Initials*	Cite No.	Document Number	Filing Date	Name of Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

U.S. PATENTS

Examiner Initials*	Cite No.	Patent Number	Issue Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	3241078	1966-03-15	Jones, Howard E.	

U.S. PATENT APPLICATION PUBLICATIONS

Examiner Initials*	Cite No.	Publication Number	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.	Foreign Patent Document	Country Code	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [1]

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published	T [1]
	2	CLARKE, Kenneth K. et al., *Communication Circuits: Analysis and Design*, Reading, MA: Addison-Wesley,1971, pgs. 467.	☐

OFFICE ACTION / NOTICE OF ALLOWANCE DOCUMENTS

Examiner Initials*	Cite No.	Application Number	Mail Date	Document

EXAMINER SIGNATURE

Examiner Signature	/Sam Bhattacharya/	Date Considered	05/18/2015

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant is to place a check mark here if English language translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14/172,392
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	Art Unit	2646
	Examiner Name	Sam Bhattacharya
	Attorney Docket Number	19200.1.1.1.2.2.1.2

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

☒ The Commissioner is hereby authorized to charge payment of any of the following fees that may be applicable to this communication, or credit any overpayment, to Deposit Account No. 23-3178: (1) any filing fees required under 37 CFR § 1.16; and/or (2) any patent application and reexamination processing fees under 37 CFR § 1.17.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Rick D. Nydegger/	Date	2015-03-11
Name/Print	Rick D. Nydegger	Registration Number	28,651

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

2113423_1.DOC

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14/172,392
	Filing Date	2014-02-04
	First Named Inventor	David F. Sorrells
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	Attorney Docket Number	19200.1.1.1.2.2.1.2

U.S. PATENT APPLICATIONS

Examiner Initials*	Cite No.	Document Number	Filing Date	Name of Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

U.S. PATENTS

Examiner Initials*	Cite No.	Patent Number	Issue Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

U.S. PATENT APPLICATION PUBLICATIONS

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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.	Foreign Patent Document	Country Code	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [1]

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published	T [1]
	1	IPR2014-00948 Petition for Inter Partes Review of U.S. Patent No. 6,370,371 dated June 12, 2014	☐
	2	IPR2014-00948 Patent Owner Preliminary Response dated September 24, 2014	☐
	3	IPR2014-00948 Decision Institute of Inter Partes Review dated December 18, 2014	☐
	4	IPR2014-00946 Petition for Inter Partes Review of U.S. Patent No. 6,266,518 dated June 12, 2014	☐
	5	IPR2014-00946 Patent Owner Preliminary Response dated September 24, 2014	☐
	6	IPR2014-00946 Decision Institute of Inter Partes Review dated December 18, 2014	☐
	7	IPR2014-00946 Petitioner's Request for Rehearing dated January 2, 2015	☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.E

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14/172,392
	Filing Date	2014-02-04
	First Named Inventor	David F. Sorrells
	Art Unit	2646
	Examiner Name	Sam Bhattacharya
	Attorney Docket Number	19200.1.1.1.2.2.1.2

	8	IPR2014-00946 Decision Petitioner's Request for Rehearing dated January 27, 2015	☐
	9	IPR2014-00946 Exhibit 1004 Asad Abidi Declaration dated June 7, 2014, filed in IPR Proceedings June 12, 2014	☐
	10	IPR2014-00946 Exhibit 1007 ParkerVision's Motion for Summary Judgment of No Invalidity dated May 22, 2013, filed in IPR Proceedings June 12, 2014	☐
	11	IPR2014-00946 Exhibit 1008 Order of Judge Roy Dalton dated February 20, 2013, filed in IPR Proceedings June 12, 2014	☐
	12	IPR2014-00946 Exhibit 1009 Transcript of Markman Hearing dated August 13, 2012, filed in IPR Proceedings June 12, 2014	☐
	13	IPR2014-00946 Exhibit 1010 Rebuttal Expert Report of Peter Weisskopf dated April 1, 2013, filed in IPR Proceedings June 12, 2014	☐
	14	IPR2014-00946 Exhibit 1011 Transcript of Jury Trial Day Six dated October 16, 2013, filed in IPR Proceedings June 12, 2014	☐
	15	IPR2014-00946 Exhibit 1012 Joint Claim Construction Statement dated May 29, 2012, filed in IPR Proceedings June 12, 2014	☐
	16	IPR2014-00946 Exhibit 1013 Transcript of Jury Trial Day Two dated October 9, 2013 filed in IPR Proceedings June 12, 2014	☐
	17	IPR2014-00946 Exhibit 1014 Transcript of Jury Trial Day Three dated October 10, 2013 filed in IPR Proceedings June 12, 2014	☐
	18	IPR2014-00946 Exhibit 1015 Transcript of Jury Trial Day Four dated October 11, 2013 filed in IPR Proceedings June 12, 2014	☐
	19	IPR2014-00946 Exhibit 1016 ParkerVision's Reply to Qualcomm's Opposition to ParkerVision's Motion for Summary Judgment of No Invalidity dated July 11, 2013 filed in IPR Proceedings June 12, 2014	☐
	20	IPR2014-00946 Exhibit 1017 Order dated August 25, 2013 filed in IPR Proceedings June 12, 2014	☐
	21	IPR2014-00946 Exhibit 1018 Declaration of Paul Prucnal, Ph.D. in Support of Plaintiff ParkerVision, Inc.'s Rebuttal Claim Construction Brief dated July 27, 2012 filed in IPR Proceedings June 12, 2014	☐
	22	IPR2014-00946 Exhibit 1020 Plaintiff ParkerVision, Inc.'s Rebuttal Claim Construction Brief dated July 27, 2012 filed in IPR Proceedings June 12, 2014	☐
	23	IPR2014-00946 Exhibit 1021 ParkerVision, Inc.'s Response in Opposition to Qualcomm's Motion for Judgment as a Matter of Law of Noninfringement dated July 27, 2012 filed in IPR Proceedings June 12, 2014	☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.E

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14/172,392
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	First Named Inventor	David F. Sorrells
	Art Unit	2646
	Examiner Name	Sam Bhattacharya
	Attorney Docket Number	19200.1.1.1.2.2.1.2

	24	EASTABROOK, Polly, Ph.D. "The Direct Conversion Receiver: Analysis and Design of the Front-end Components" Ph.D. dissertation, Stanford University, August 1989.	☐
	25	WEISSKOPF, Peter A.,"Subharmonic Sampling of Microwave Signal Processing Requirements", *Microwave Journal*, Vol. 35, No. 5, May 1992, pgs. 239-247.	☐
	26	AVITABILE, G., et al., "S-band Digital Downcoverter for Radar Applications Based on a GaAs MMIC Fast Sample-and-Hold" *IEEE Proc. on Circuits Devices and Systems.*, Vol. 143, No. 6, December 1996, pgs. 337-342.	☐
	27	Shannon, C.E., "Communication in the presence of Noise," *Proceedings of the IRE,* Vol. 37, No. 1, 1949, ppgs. 10-21.	☐
	28	BLACK, Harold S., *Modulation Theory*, ser. The Bell Telephone Laboratory Series. New York: Van Nostrand, pgs 55-57, 1953.	☐
	29	MANGELSDORF, Chris, et al., "200-MSPS 8-Bit IC A/D Converter Has 250-MHz Bandwidth", *Analog Dialogue* Vol. 22, No. 2, pgs. 3-7, 1988.	☐
	30	COCHRANE, P., "Sampling Principles," in *Microwave Measurements,* 2nd ed., A.E. Bailey, Ed. London: Peter Peregrinus, 1989, Chapter 15, pgs. 344-358.	☐
	31	JANSSEN, J.M.L., "An Experimental 'Stroboscopic' Oscilloscope for Frequencies up to About 50 Mc/s" *Philips Technical Review*, Volume 12, No. 2, pgs. 52 – 81, 1950.	☐
	32	BENNETTT, W.R. "Pulse Modulation" in *Communication Systems and Techniques*, M. Schwartz, et al. Eds. New York: McGraw-Hill, 1966, pgs. 244-245.	☐
	33	LINDEN, D.A., "A Discussion of Sampling Theorems", *Proceedings of the IRE* Vol. 47, No. 7, July 1959, pgs. 1219-1226.	☐
	34	RAGAZZINI, John R., "*Sampled-Data Control Systems*, New York: McGraw-Hill, 1958, Chapter 2, pgs. 12-28.	☐
	35	YEN, Chu-Sun, "Phase-Locked Sampling Instruments" *IEEE Transactions on Instrumentation and Measurement,* Vol. 14, No. 1 and 2, pgs. 64-68, 1965.	☐
	36	HOWARD, Dar, et al., "The Wideband Sampling Gate, An Analysis, Characterization and Application Discussion" in WESCON 1966, Conference Proceedings, 23/1/1-11.	☐
	37	COCHRANE, P., Sampling Principles, in *Microwave Measurements 2nd ed.,* A.E. Bailey, Ed. London: Peter Peregrinus,1989, chapter 16, pgs. 360-384.	☐
	38	DETHLEFSEN, Michael et al., "Design Considerations in the Microwave Transition Analyzer", *Hewlett-Packard Journal,* Vol. 43, No. 5, October 1992, pgs. 63-71.	☐
	39	"SAMPLING NOTES" *Tektronix,* Application Note 85W-23777-0, *1964.*	☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.E

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14/172,392
	Filing Date	2014-02-04
	First Named Inventor	David F. Sorrells
	Art Unit	2646
	Examiner Name	Sam Bhattacharya
	Attorney Docket Number	19200.1.1.1.2.2.1.2

	40	GROVE, W.M., "Sampling for Oscilloscopes and Other RF Systems: Dc Through X-Band", *IEEE Transactions on Microwave Theory and Techniques,* December, 1966, pgs. 629-635	☐
	41	FAULKNER, Neil D. et al., "Subharmonic Sampling for the Measurement of Short-Term Stability of Microwave Oscillators", *IEEE Translations on Instrumentation and Measurement,* Volume MITT-14, No. 12, March 1966, pgs. 208-213.	☐
	42	"Fundamentals of RF and Microwave Noise Figure Measurements" Hewlett Packard Application Note AN 57-1, 1983.	☐
	43	TAUB, Herbert et al., "*Principles of Communication Systems*, 2nd Ed, New York: McGraw-Hill, 1986, pgs. 615-623.	☐
	44	BALLO, David J., et al. "The Microwave Transition Analyzer: A New Instrument Architecture for Component and Signal Analysis" *Hewlett-Packard Journal*, Vol. 43, No. 5, October 1992, Pgs. 48-62.	☐
	45	CLARKE, Kenneth K. et al., *Communication Circuits: Analysis and Design*, Reading, MA:Addison-Wesley,1971, pgs. 353-385.	☐
	46	GIBBONS, James F., *Semiconductor Electronics.* New York: McGraw-Hill, 1966.	☐
	47	GUILLEMIN, Ernst A. *Introductory Circuit Theory*, New York: Wiley, 1953, pgs. 520-521.	☐
	48	DESOER, Charles A. et al., *Basic Circuit Theory*, New York: McGraw-Hill, 1969, Chapter 9, pgs. 396-397.	☐
	49	ESTABROOK, P. et al., "A Mixer Computer-Aided Design Tool Based in the Time Domain" IEEE MTT-5 Digest, 1988, pgs. 1107-1110.	☐
	50	IPR2014-00947 Petition for Inter Partes Review of U.S. Patent No. 6,061,551 dated June 12, 2014	☐
	51	IPR2014-00947 Patent Owner Preliminary Response dated September 24, 2014	☐
	52	IPR2014-00947 Decision Institute of Inter Partes Review dated December 18, 2014	☐
	53	IPR2014-001107 Petition for Inter Partes Review of U.S. Patent No. 7,496,342 dated July 2, 2014	☐
	54	IPR2014-001107 Patent Owner Preliminary Response dated October 10, 2014	☐
	55	IPR2014-001107 Decision Institute of Inter Partes Review dated January 8, 2014	☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.E

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14/172,392
	Filing Date	2014-02-04
	First Named Inventor	David F. Sorrells
	Art Unit	2646
	Examiner Name	Sam Bhattacharya
	Attorney Docket Number	19200.1.1.1.2.2.1.2

	56	IPR2014-001107 Asad Abidi Declaration dated July 2, 2014, filed in IPR Proceedings July 2, 2014	☐
	57	OXNER, Ed, "FETs in Balanced Mixers" *Siliconix,* Application Note, AN-72-1, 1979, pgs. 6-29 to 6-38	☐
	58	RAZAVI, Behzad, *Principles of Data Conversion System Design*, IEEE Press, 1995, pgs. 7-28.	☐
	59	BULT, Klaas et al., "A CMOS Four-Quadrant Analog Multiplier" IEEE Journal of Solid-State Circuits, Vol. sc-21, No. 3, June 1986, pgs. 430-435.	☐
	60	Thornton, Richard D. et al. *MultiStage Transistor Circuits,* New York: Wiley, 1965	☐
	61	DeMaw, Doug, *Practical RF Design Manual,* Prentice-Hall, 1982, pgs. 118-213.	☐
	62	IPR2014-01107 Parkervision's Response in Opposition to Qualcomm's Renewed Motion for Judgment as a Matter of Law and Motion for New Trial Regarding Invalidity, dated January 24, 2014 filed in IPR Proceedings July 2, 2014.	☐
	63	Zimmerman, H.J. et al. *Electronic Circuit Theory*. NewYork: Wiley, 1959, pgs. 142-144.	☐
	64	"U430/431 Matched N-Channel JFET Pairs" Siliconix, Data Sheet P-37405 – Rev.D., 1994.	☐
	65	Schelkunoff, S.A., et al. *Antennas: Theory and Practice*. New York: Wiley, 1952, pgs. 324-325.	☐

OFFICE ACTION / NOTICE OF ALLOWANCE DOCUMENTS				
Examiner Initials*	Cite No.	Application Number	Mail Date	Document

EXAMINER SIGNATURE			
Examiner Signature	/Sam Bhattacharya/	Date Considered	05/18/2015

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.E

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14/172,392
	Filing Date	2014-02-04
	First Named Inventor	David F. Sorrells
	Art Unit	2646
	Examiner Name	Sam Bhattacharya
	Attorney Docket Number	19200.1.1.1.2.2.1.2

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

☒ The Commissioner is hereby authorized to charge payment of any of the following fees that may be applicable to this communication, or credit any overpayment, to Deposit Account No. 23-3178: (1) any filing fees required under 37 CFR § 1.16; and/or (2) any patent application and reexamination processing fees under 37 CFR § 1.17.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	Rick D. Nydegger	Date	2015-03-10
Name/Print	Rick D. Nydegger	Registration Number	28,651

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

5023839_1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.E

Response to Rule 312 Communication	Application No.	Applicant(s)
	14/172,392	SORRELLS ET AL.
	Examiner	**Art Unit**
	Sam Bhattacharya	2646

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☒ The amendment filed on *22 April 2015* under 37 CFR 1.312 has been considered, and has been:

   a) ☐ entered.

   b) ☒ entered as directed to matters of form not affecting the scope of the invention.

   c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
   Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

   d) ☐ disapproved. See explanation below.

   e) ☐ entered in part. See explanation below.

/Sam Bhattacharya/
Primary Examiner, Art Unit 2646

Electronically Filed via *EFS*

PATENT APPLICATION
Docket: 19200.1.1.1.2.2.1.2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:		)
	David F. Sorrells et al.	)
		)
Serial No.:	14/172,392	)
		)
Confirmation No.:	8448	)
		)
Filed:	February 4, 2014	)
		)
For:	Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same, and Aperture Relationships	)

RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

In response to the Notice to File Corrected Application Papers mailed April 10, 2015, please amend the above-identified application as follows:

Remarks/Arguments begin on page 2 of this paper.

Please Enter
sb
5/15/15

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/172,392	02/04/2014	2646	6620	19200.1.1.1.2.2.1.2	1	1

CONFIRMATION NO. 8448

CORRECTED FILING RECEIPT

22913
Workman Nydegger
60 East South Temple
Suite 1000
Salt Lake City, UT 84111

Date Mailed: 05/29/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

David F. Sorrells, Jacksonville, FL;
Michael J. Bultman, Jacksonville, FL;
Robert W. Cook, Switzerland, FL;
Richard C. Looke, Jacksonville, FL, Deceased;
Charley D. Moses, Jacksonville, FL;
Gregory S. Rawlins, Lake Mary, FL;
Michael W. Rawlins, Lake Mary, FL;

Applicant(s)

ParkerVision, Inc., Jacksonville, FL;

Power of Attorney: The patent practitioners associated with Customer Number 22913

Domestic Priority data as claimed by applicant

This application is a CON of 13/549,213 07/13/2012 PAT 8660513
which is a CON of 12/976,839 12/22/2010 PAT 8340618
which is a CON of 12/349,802 01/07/2009 PAT 7865177
which is a DIV of 09/550,644 04/14/2000 PAT 7515896
which is a CIP of 09/293,342 04/16/1999 PAT 6687493
which is a CIP of 09/176,022 10/21/1998 PAT 6061551

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 02/20/2014

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/172,392**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

Method and System for Down-Converting an Electromagnetic Signal, and Transforms for Same, and Aperture Relationships

Preliminary Class

455

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14/172,392
	Filing Date	2014-02-04
	First Named Inventor	David F. Sorrells
	Art Unit	2646
	Examiner Name	Sam Bhattacharya
	Attorney Docket Number	19200.1.1.1.2.2.1.2

	26	8649753	11-Feb-2014	Rofougaran et al.	
	27	8660513	25-Feb-2014	Sorrells et al.	
	28	8824993	~~2-Aug-2014~~	Sorrells et al.	September 2, 2014

Change(s) applied to document, /D.D./ 5/22/2015

U.S. PATENT APPLICATION PUBLICATIONS

Examiner Initials*	Cite No.	Publication Number	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	29	20030227983	~~22-Jan-2008~~	Milne et al.	December 11, 2003
	30	20130109338	2-May-2013	Sorrells et al.	
	31	20130115906	9-May-2013	Forman et al.	
	32	20130122835	16-May-2013	Sorrells et al.	
	33	20130122846	16-May-2013	Sorrells et al.	
	34	20130182749	18-Jul-2013	Sorrells et al.	
	35	20130202070	8-Aug-2013	Sorrells et al.	
	36	20130225110	29-Aug-2013	Karlquist, Richard K.	
	37	20140226751	14-Aug-2014	Sorrells et al.	
	38	20140233670	21-Aug-2014	Sorrells et al.	
	39	20140308909	16-Oct-2014	Sorrells et al.	
	40	20140308911	16-Oct-2014	Sorrells et al.	
	41	20140308912	16-Oct-2014	Sorrells et al.	
	42	20140308913	16-Oct-2014	Sorrells et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.	Foreign Patent Document	Country Code	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [1]
	43	WO 9722185	WO	19-Jun-1997	Ericsson GE Mobile Inc (US)		☐

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published	T [1]
	44	MAAS S. A. "A Gaas Mesfet Mixer with Very Low Intermodulation", IEEE Transactions on Microwave Theory and Techniques, IEEE Service Center, Piscataway, NJ, US, vol. MTT-35, no. 4, 1-April-1987, pages 425-429.	☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.E

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/172,392	08/25/2015	9118528	19200.1.1.1.2.2.1.2	8448

22913 7590 08/05/2015
Workman Nydegger
60 East South Temple
Suite 1000
Salt Lake City, UT 84111

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

David F. Sorrells, Jacksonville, FL;
ParkerVision, Inc., Jacksonville, FL;
Michael J. Bultman, Jacksonville, FL;
Robert W. Cook, Switzerland, FL;
Richard C. Looke, Jacksonville, FL, Deceased;
Charley D. Moses, Jacksonville, FL;
Gregory S. Rawlins, Lake Mary, FL;
Michael W. Rawlins, Lake Mary, FL;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

IR103 (Rev. 10/09)

AO 120 (Rev. 08/10)

TO:	**Mail Stop 8** **Director of the U.S. Patent and Trademark Office** **P.O. Box 1450** **Alexandria, VA 22313–1450**	**REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK**

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the **U.S. District Court for the District of New Jersey** on the following:
____ Trademarks or **X** Patents. (____ the patent action involves 35 U.S.C. § 292.)

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:17–cv–05359–MCA–LDW	7/24/2017	NEWARK, NJ

PLAINTIFF	DEFENDANT
PARKERVISION, INC.	LG ELECTRONICS, INC.

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 US 6,879,817 B1	Apr. 12, 2005	ParkerVlslon, Inc.
2 US 7,929,638 B2	Apr. 19, 2011	ParkerVision, Inc.
3 US 8,571,135 B2	Oct. 29, 2013	ParkerVision, Inc.
4 US 9,118,528 B2	Aug. 25, 2015	ParkerVision, Inc.
5 US 9,118,528 B2	Aug. 25, 2015	ParkerVision, Inc.

In the above––entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ___ Amendment ___ Answer ___ Cross Bill ___ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
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5		

In the above––entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
William T. Walsh	s/ John Reilly	7/24/2017

Copy 1––Upon initiation of action, mail this copy to Director Copy 3––Upon termination of action, mail this copy to Director
Copy 2––Upon filing document adding patent(s), mail this copy to Director Copy 4––Case file copy

AO 120 (Rev. 08/10)

TO:	**Mail Stop 8** **Director of the U.S. Patent and Trademark Office** **P.O. Box 1450** **Alexandria, VA 22313–1450**	**REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK**

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the **U.S. District Court for the District of New Jersey** on the following:
____ Trademarks or **X** Patents. (____ the patent action involves 35 U.S.C. § 292.)

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:17–cv–05359–MCA–LDW	7/24/2017	NEWARK, NJ

PLAINTIFF	DEFENDANT
PARKERVISION, INC.	LG ELECTRONICS, INC.

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 US 6,879,817 B1	Apr. 12, 2005	ParkerVlslon, Inc.
2 US 7,929,638 B2	Apr. 19, 2011	ParkerVision, Inc.
3 US 8,571,135 B2	Oct. 29, 2013	ParkerVision, Inc.
4 US 9,118,528 B2	Aug. 25, 2015	ParkerVision, Inc.
5 US 9,118,528 B2	Aug. 25, 2015	ParkerVision, Inc.

In the above––entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ___ Amendment ___ Answer ___ Cross Bill ___ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above––entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
William T. Walsh	s/ John Reilly	7/24/2017

Copy 1––Upon initiation of action, mail this copy to Director Copy 3––Upon termination of action, mail this copy to Director
Copy 2––Upon filing document adding patent(s), mail this copy to Director Copy 4––Case file copy

AO 120 (Rev. 08/10)

TO:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court for the Central District of California on the following

☐ Trademarks or ☐ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
5:20cv1030 GW-SHK	5/14/2020	for the Central District of California

PLAINTIFF	DEFENDANT
PARKERVISION, INC.	TCL TECHNOLOGY GROUP CORP. and TTE TECHNOLOGY, INC.

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,049,706	4/11/2000	ParkerVision, Inc.
2 6,266,518	7/24/2001	ParkerVision, Inc.
3 6,580,902	6/17/2003	ParkerVision, Inc.
4 7,110,444	9/19/2006	ParkerVision, Inc.
5 7,292,835	11/6/2007	ParkerVision, Inc.

In the above---entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above---entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT
Voluntary Dismissal

CLERK	(BY) DEPUTY CLERK	DATE
Kiry K. Gray	/s/ Margo Mead	10/09/2020

Copy 1---Upon initiation of action, mail this copy to Director Copy 3---Upon termination of action, mail this copy to Director
Copy 2---Upon filing document adding patent(s), mail this copy to Director Copy 4---Case file copy

AO 120 (Rev. 08/10)

TO:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court for the Central District of California on the following

☐ Trademarks or ☐ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED 5/14/2020	U.S. DISTRICT COURT for the Central District of California
PLAINTIFF PARKERVISION, INC.		DEFENDANT TCL TECHNOLOGY GROUP CORP. and TTE TECHNOLOGY, INC.

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 8,588,725	11/19/2013	ParkerVision, Inc.
2 8,660,513	2/25/2014	ParkerVision, Inc.
3 9,118,528	8/25/2015	ParkerVision, Inc.
4 9,246,736	1/26/2016	ParkerVision, Inc.
5 9,444,673	9/13/2016	ParkerVision, Inc.

In the above---entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
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In the above---entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1---Upon initiation of action, mail this copy to Director Copy 3---Upon termination of action, mail this copy to Director
Copy 2---Upon filing document adding patent(s), mail this copy to Director Copy 4---Case file copy

AO 120 (Rev. 08/10)

TO:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas - Waco Division on the following

☐ Trademarks or ☐ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
	5/21/2021	Western District of Texas - Waco Division

PLAINTIFF	DEFENDANT
ParkerVision, Inc.	LG Electronics, Inc.

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,049,706	4/11/2000	ParkerVision, Inc.
2 6,266,518	7/24/2001	ParkerVision, Inc.
3 6,580,902	6/17/2003	ParkerVision, Inc.
4 7,110,444	9/19/2006	ParkerVision, Inc.
5 7,292,835	11/6/2007	ParkerVision, Inc.

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 8,588,725	11/19/2013	ParkerVision, Inc.
2 8,660,513	2/25/2014	ParkerVision, Inc.
3 9,118,528	8/25/2015	ParkerVision, Inc.
4 9,246,736	1/26/2016	ParkerVision, Inc.
5 9,444,673	9/13/2016	ParkerVision, Inc.

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

TO:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas - Waco Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:20-cv-01009	10/30/2020	Western District of Texas - Waco Division

PLAINTIFF	DEFENDANT
ParkerVision, Inc.	Buffalo Inc.

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,049,706	4/11/2000	ParkerVision, Inc.
2 6,266,518	7/24/2001	ParkerVision, Inc.
3 6,580,902	6/17/2003	ParkerVision, Inc.
4 7,110,444	9/19/2006	ParkerVision, Inc.
5 7,292,835	11/6/2007	ParkerVision, Inc.

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
6 8,588,725	11/19/2013	ParkerVision, Inc.
7 8,660,513	2/25/2014	ParkerVision, Inc.
8 9,118,528	8/25/2015	ParkerVision, Inc.
9 9,246,736	1/26/2016	ParkerVision, Inc.
10 9,444,673	9/13/2016	ParkerVision, Inc.

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

9/13/2021 ORDER GRANTING JOINT Motion to Dismiss (document 16)

CLERK	(BY) DEPUTY CLERK	DATE
Jeannette J. Clack	L. Rivera	09/13/2021

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AO 120 (Rev. 08/10)

TO:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas - Waco Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:20-cv-00870	9/24/2020	Western District of Texas - Waco Division

PLAINTIFF	DEFENDANT
ParkerVision, Inc.	Hisense Co., Ltd. and Hisense Visual Technology Co., Ltd. (f/k/a Qingdao Hisense Electronics Co., Ltd. and Hisense Electric Co., Ltd.)

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,049,706	4/11/2000	ParkerVision, Inc.
2 6,266,518	7/24/2001	ParkerVision, Inc.
3 6,580,902	6/17/2003	ParkerVision, Inc.
4 7,110,444	9/19/2006	ParkerVision, Inc.
5 7,292,835	11/6/2007	ParkerVision, Inc.

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
6 8,588,725	11/19/2013	ParkerVision, Inc.
7 8,660,513	2/25/2014	ParkerVision, Inc.
8 9,118,528	8/25/2015	ParkerVision, Inc.
9 9,246,736	1/26/2016	ParkerVision, Inc.
10 9,444,673	9/13/2016	ParkerVision, Inc.

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

11/30/2022 Doc #81 STIPULATION of Dismissal

CLERK	(BY) DEPUTY CLERK	DATE
PHILIP J. DEVLIN		11/30/2022

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AO 120 (Rev. 08/10)

TO:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas - Waco Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:23-cv-00374	5/16/2023	Western District of Texas - Waco Division

PLAINTIFF	DEFENDANT
ParkerVision, Inc.	Realtek Semiconductor Corp.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,879,817	4/12/2005	ParkerVision, Inc.
2	7,865,177	1/4/2011	ParkerVision, Inc.
3	9,118,528	8/25/2015	ParkerVision, Inc.
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

AO 120 (Rev. 08/10)

TO:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas - Waco Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:23-cv-00384	5/18/2023	Western District of Texas - Waco Division

PLAINTIFF	DEFENDANT
ParkerVision, Inc.	Texas Instruments Incorporated

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,496,342	2/24/2009	ParkerVision, Inc.
2 7,865,177	1/4/2011	ParkerVision, Inc.
3 9,118,528	8/25/2015	ParkerVision, Inc.
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

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AO 120 (Rev. 08/10)

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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas - Waco Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:23-cv-00389	5/19/2023	Western District of Texas - Waco Division

PLAINTIFF	DEFENDANT
ParkerVision, Inc.	NXP Semiconductors N.V., NXP B.V., NXP USA, Inc. d/b/a NXP Semiconductors USA, Inc.

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,483,686	1/27/2009	ParkerVision, Inc.
2 7,865,177	1/4/2011	ParkerVision, Inc.
3 9,118,528	8/25/2015	ParkerVision, Inc.
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

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