IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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U.S. Patent No.:	9,118,528	
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Appl. Serial No.:	14/172,392	
Filing Date:	February 4, 2014	
Title:	METHOD AND SYSTEM FOR DOWN-CONVERTING AN ELECTROMAGNETIC SIGNAL, AND TRANSFORMS FOR SAME, AND APERTURE RELATIONSHIPS	

DECLARATION OF IAN GALTON, PH.D.

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I, Dr. Ian Galton of La Jolla, CA, declare that:

I. ASSIGNMENT

1. I have been retained by Fish & Richardson P.C. as an independent expert on behalf of Petitioner Texas Instruments ("TI"). I understand that TI is petitioner in an *inter partes* review ("IPR") of U.S. Patent No. 9,118,528 (the "'528 patent") (EX1001) before the Patent Trial and Appeal Board ("PTAB" or "Board"). I understand the '528 patent is assigned to Patent Owner ParkerVision, Inc. ("ParkerVision"). I have been asked to provide my independent analysis of the '528 patent in light of the materials cited below and my knowledge and experience in this field during the relevant period. I have been asked to consider what a person of ordinary skill in the art at the time of the alleged invention of the '528 patent (a "POSITA") would have understood from the teachings of the '528 patent, including scientific and technical knowledge related to the '528 patent.

2. I am not, and never have been, an employee of TI. I am being compensated at my standard consulting rate for my time providing my independent analysis, plus reasonable out-of-pocket expenses. I have received no additional compensation for my work in this matter, and my compensation does not depend upon the content of my opinions, any testimony that I may provide, or the ultimate outcome of the matter. All of the opinions set forth in this declaration are my own.

II. BACKGROUND AND QUALIFICATIONS

3. I am currently a Professor of Electrical Engineering at the University of California at San Diego (UCSD) where I manage the Integrated Signal Processing Group. My qualifications for formulating my analysis on this matter are summarized here with full descriptions of my educational background, professional work, qualifications, and publications set forth more fully in my *curriculum vitae*, which is attached to this declaration as Appendix A.

4. I received my Bachelor of Science in Electrical Engineering from Brown University in Providence, RI in 1984. I received my Masters and Ph.D. in Electrical Engineering from the California Institute of Technology in 1989 and 1992, respectively.

5. After receiving my B.S. degree, I worked as a design engineer at Mindset Corporation in Sunnyvale, CA, which was an early innovator in the personal computer market, from 1984 to 1985. I then worked as a design engineer at Mead Data Central in Menlo Park, CA, a leading database service responsible for services such as LEXIS and NEXIS, from 1985 to 1986. From 1986 to 1988 I worked as a design engineer for Acuson, Inc. in Mountain View, CA which leveraged current developments in computing technology to improve diagnostic ultrasound technology.

6. After receiving my Ph.D. in 1992 I began teaching at the University of California at Irvine as an Assistant Professor of Electrical Engineering before moving to UCSD in 1996, initially joining as a tenured Associate Professor of Electrical Engineering prior to my current position as a tenured Professor of Electrical Engineering. I currently hold the "Skyworks Endowed Chair in High Performance Communications Devices and Circuits." My work at UCSD includes teaching and conducting research in the field of mixed-signal integrated circuits and systems for communications. My work with the Integrated Signal Processing Group at UCSD includes leading graduate and post-doctorial students in developing enabling technology for highly-integrated, high-performance, low-cost, communication systems. The research involves the invention, development, analysis, and proof-of-principle integrated circuit (IC) implementation of key communication system blocks such as data converters and frequency synthesizers. The emphases of the research are on the development of new digital signal processing techniques and new digital-like analog circuits that exploit the strengths of advanced IC technology to mitigate the effects of non-ideal analog circuit behavior in mixed-signal and radio frequency ICs.

7. In addition to my teaching and academic research responsibilities at UCSD, I regularly consult at several semiconductor companies and teach industry-oriented short courses on the design of mixed-signal integrated circuits. I am a

Fellow of the IEEE, and have served on a corporate Board of Directors, on several corporate Technical Advisory Boards, as the Editor-in-Chief of the IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, as a member of the IEEE Solid-State Circuits Society Administrative Committee, as a member of the IEEE Circuits and Systems Society Board of Governors, as a member of the IEEE International Solid-State Circuits Conference Technical Program Committee, and as a member of the IEEE Solid-State Circuits Society Distinguished Lecturer Program.

8. I have authored or co-authored well over 100 scientific papers in peer-reviewed academic journals and conferences. I am also a named inventor on 25 issued U.S. Patents. I have received numerous awards from leading organizations in the area of Electrical Engineering, including IEEE. A complete list of my publications, patents, awards, and recognitions is included in my CV (Appendix A).

9. In addition to gaining expertise via my academic training, professional experiences, and research accomplishments described above, I have kept abreast of the field of RF and other mixed-signal integrated circuits specifically and electrical engineering in general by reading technical literature, attending and presenting at conferences, and attending and presenting at symposia. I have been invited to participate in the peer review process for various technical journals, and conferences, and have reviewed manuscripts submitted by other engineers relating to integrated

circuit design and communications technology. Furthermore, I have collaborated with or have communicated with many other engineers in the field.

III. MATERIALS REVIEWED AND CONSIDERED

10. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field of the art, and have considered the viewpoint of a POSITA at the time of the alleged invention. I have also reviewed and considered the documents listed in the Exhibit List of this declaration. Although this declaration refers to selected portions of the cited references for the sake of brevity, it should be understood that these are examples, and that a POSITA would have viewed the references cited herein in their entirety and in combination with other references cited herein or cited within the references themselves. The references used in this declaration, therefore, should be viewed as being considered herein in their entireties.

11. Specifically, I have analyzed the following publications and materials, in addition to other materials I cite in my declaration:

- U.S. Patent No. 9,118,528 (Exhibit 1001), and its accompanying prosecution history (Exhibit 1002)
- U.S. Patent No. 6,230,000 ("Tayloe") (TI-1004)

- SN74CBT3253 Dual 1-of-4 FET Multiplexer/Demultiplexer Datasheet (TI-1005)[1]
- Razavi, *A 900-MHz CMOS Direct Conversion Receiver* ("Razavi") (TI-1017)
- C. Cahn, *Combined Digital Phase and Amplitude Modulation Communication Systems* ("Cahn") (TI-1007)
- U.S. Patent No. 7,065,327 ("Macnally") (TI-1021)
- U.S. Provisional Patent Application 60/099,723 ("MacNally-Provisional") (TI-1022)

12. Each of these foregoing article references indicate on their face that they were published in journals or conference proceedings that I am familiar with, and which would have been available to and disseminated to members of the general technical community prior to October 21, 1998.

IV. LEGAL UNDERSTANDING

13. I understand that issues such as invalidity and claim construction are analyzed based on certain legal standards. Counsel for TI has provided me with an

[1] A POSITA reviewing Tayloe would have visited TI's website to find information pertaining to this mux/demux. I understand that TI datasheet was publicly accessible to those interested in the operation of TI products on TI's searchable website, beginning July 28, 1998.

understanding of these standards, and I have applied them in my analysis set forth in this declaration.

A. Anticipation

14. I have been informed that a patent claim is invalid as anticipated under 35 U.S.C. § 102 if each and every element of a claim, as properly construed, is found either explicitly or inherently in a single prior art reference. Under the principles of inherency, if the prior art necessarily functions in accordance with, or includes the claimed elements, it anticipates.

15. I have been informed that a claim is invalid under 35 U.S.C. § 102(a) if the claimed invention was known or used by others in the U.S., or was patented or published anywhere, before the Applicant's invention. I further have been informed that a claim is invalid under 35 U.S.C. § 102(b) if the invention was patented or published anywhere, or was in public use, on sale, or offered for sale in this country, more than one year prior to the filing date of the patent application (critical date). And a claim is invalid, as I have been informed, under 35 U.S.C. § 102(e), if an invention described by that claim was described in a U.S. patent granted on an application for a patent by another that was filed in the U.S. before the date of invention for such a claim.

B. Obviousness

16. I have been informed that a patent claim is invalid as "obvious" under 35 U.S.C. § 103 in light of one or more prior art references if it would have been obvious to a person of ordinary skill in the art at the time of the alleged invention ("POSITA"), taking into account (1) the scope and content of the prior art, (2) the differences between the prior art and the claims, (3) the level of ordinary skill in the art, and (4) any so called "secondary considerations" of non-obviousness, which include: (i) "long felt need" for the claimed invention, (ii) commercial success attributable to the claimed invention, (iii) unexpected results of the claimed invention, and (iv) "copying" of the claimed invention by others. For purposes of my analysis here, I have applied a date of October 21, 1998, as the date of the alleged invention in my obviousness analyses.

17. I have been informed that a claim can be obvious in light of a single prior art reference or multiple prior art references. To be obvious in light of a single prior art reference or multiple prior art references, there must be a reason that would have prompted a POSITA to modify the single prior art reference, or combine two or more references, in a manner that provides the elements of the claimed invention. This reason may come from a teaching, suggestion, or motivation to combine, or may come from the reference(s) themselves, the knowledge or "common sense" of a POSITA, or from the nature of the problem to be solved, and this reason may be

explicit or implicit from the prior art as a whole. I have been informed that, under the law, the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand it is improper to rely on hindsight in making the obviousness determination.

C. Claim Construction

18. I have been informed by counsel that, for purposes of my analysis in this *inter partes* review proceeding, the terms appearing in the patent claims should be interpreted according to their "ordinary and customary meaning." In determining the ordinary and custom meaning, the words of a claim are first given their plain meaning that those words would have had to a POSITA. I understand that the structure of the claims, the specification, and the file history also may be used to better construe a claim insofar as the plain meaning of the claims cannot be understood. Moreover, treatises and dictionaries may be used, albeit under limited circumstances, to determine the meaning attributed by a POSITA to a claim term at the time of filing. I have followed this approach in my analysis.

19. I also understand that the words of the claims should be interpreted as they would have been interpreted by a POSITA at the time the alleged invention was made (not today).

20. Because I do not know at what date the invention as claimed was made, I have used the earliest priority date of U.S. Patent No 9,118,528 as the point in time

for claim interpretation purposes. That date was October 21, 1998. I have been asked to provide my interpretation of the following terms and phrases of the '528 patent set forth below.

D. The Person of Ordinary Skill in the Art

21. I understand that POSITA is a hypothetical person who is presumed to be aware of all pertinent prior art, thinks along conventional wisdom in the art, and is a person of ordinary creativity—not an automaton.

22. I understand the level of ordinary skill in the art is evaluated based on various factors, including: the level of education and work experience of persons in the field; the type of problems encountered in the field; and the sophistication of the technology at issue. As of the '528 patent's alleged priority date (October 21, 1998), a POSITA would have had at least a bachelor's degree in electrical engineering or a related subject and two or more years of experience in the field of electromagnetic (EM) circuit design. Less work experience may be compensated by a higher level of education, such as a master's degree.

V. SUMMARY OF OPINIONS

23. For purposes of this declaration, I have been asked to analyze claims 1-5, 8, 9, 11-23, 26, 27, and 29-36 of the '528 Patent ("the Challenged Claims") in view of the prior art. In my opinion, the Challenged Claims are obvious based on the following grounds:

Ground 1A: Claims 1, 5, 8-9, 11-14, 15-19, 23, 26-27, 29-36 are obvious based on U.S. Patent No. US 6,230,000 ("Tayloe") in combination with TI Datasheet, and U.S. Patent No. US 7,065,327 ("Macnally").

Ground 1B: Claims 2-4, 20-22 are obvious based on Tayloe, TI Datasheet, Macnally, and C. Cahn, *Combined Digital Phase and Amplitude Modulation Communication Systems*, 1960 IEEE/IRE Transaction on Communication Systems, vol. 8, Issue 3 pp. 150-55 ("Cahn").

Ground 2A: Claims 1, 5, 8-9, 11-14, 15-19, 23, 26-27, 29-36 are obvious based on Razavi, *A 900-MHz CMOS Direct Conversion Receiver*, IEEE Symposium on VLSI Circuits, Kyoto, Japan, 1997, pp. 113-114, doi: 10.1109/VLSIC.1997.623833 ("Razavi"), and Macnally.

Ground 2B: Claims 2-4, 20-22 are obvious based on Razavi, Macnally, and Cahn.

24. I provide the bases for my opinions in the following sections.

VI. TECHNOLOGY BACKGROUND

25. In this section, I provide a high-level overview of technical concepts and design principles underlying direct conversion technology and the '528 Patent.

A. Superheterodyne Receivers

26. A received radio frequency (RF) signal has a frequency spectrum that is centered at the signal's carrier frequency, e.g., 900 MHz, and is non-zero over a

band of frequencies, e.g., 5 MHz, centered about the carrier frequency. The objective of the down-conversion process in a wireless receiver is to shift the spectrum of the RF signal so that it is centered about zero-frequency, a process which is sometimes, albeit infrequently, referred to as "removing the carrier." The down-converted signal is typically referred to as the baseband signal. As the frequency spectrum of the RF signal has real and imaginary parts that are not necessarily conjugate symmetric about the carrier frequency, usually the baseband signal must be represented as a pair of signals, one corresponding the baseband signal's real component and one corresponding to the baseband signal's imaginary component. These two signals are typically called the in-phase and quadrature baseband signal components.

27. Unwanted RF signals with different carrier frequencies are usually present in the signal captured by the antenna, so it is necessary for a receiver to filter out these unwanted signals in addition to performing frequency down-conversion. Furthermore, the power of the signal at the antenna is usually extremely low, so the receiver must provide a large amount of amplification in addition to down-conversion and filtering operations.

28. Practical circuits used to process analog information-bearing signals often have small unwanted DC components arising from non-ideal circuit behavior. However, despite these DC components being small, they are often much larger than the received signal at the receiver's antenna output. Unfortunately, the large gains

required in radio receivers have the potential to amplify these offsets so much that they overload the circuitry within the receiver, thereby rendering the receiver non-functional. This was a significant problem ever since the early days of wireless receivers, and it was solved in the early part of the 20th century by Edwin H. Armstrong with an invention called the superheterodyne receiver. The gist of the idea is to first perform frequency down-conversion to a non-zero intermediate frequency (IF) along with filtering and amplification. As the desired signal after this initial frequency down-conversion step, known is the IF signal, occupies a frequency band centered at the IF and does not overlap zero-frequency, any DC offset can be removed without affecting the desired signal. Typically, the IF signal is passed through a so-called bandpass filter centered at the IF to suppress unwanted received signals above and below the spectrum of the desired signal (including the DC component), and the result is frequency down-converted from the IF to generate the in-phase and quadrature baseband signals mentioned above, along with additional amplification. Lowpass filtering is generally applied to the baseband signals to further suppress unwanted components.

B. Direct Conversion Receivers

29. Superheterodyne receiver architectures are still used, and were extremely widely used until the 1990s. The shift away from superheterodyne receivers arose because high-quality, low-power, low-noise, and low-area bandpass

filters are not amenable to integrated circuit (IC) implementation. Therefore, IC-based superheterodyne receivers generally require off-chip bandpass filters, typically surface acoustic wave (SAW) bandpass filters, to perform the necessary bandpass filtering. Such filters are expensive and their use requires dedicated IC input and output pins which are also expensive. These issues induced significant research and development efforts to develop direct conversion receivers, i.e., receivers that down-convert the received RF signal directly to baseband without first down-converting to a non-zero IF. The benefit of doing this is that lowpass filters, which are amenable to IC implementation can be applied to the baseband signals to remove unwanted signals without the need for bandpass filters.

C. Mixers

30. The term mixer in the context of wireless receivers refers to a class of circuits that perform the above-mentioned frequency shift operation. The classic communication system textbook definition of a mixer is a circuit that multiplies an input signal by a sinusoidal oscillator signal and filters the result. However, most modern practical mixer circuits perform multiplication by "squared-up" oscillator signals, i.e., by oscillator signals which resemble square waves that ideally have the same mid-point crossing times as the corresponding sinusoidal oscillator signals. In this case the multiplication function is equivalent to multiplying the sign of the mixer's input signal by 1 or −1 as a function of the sign of the mixer's squared-up

oscillator signal and can be implemented using simple transistor switches as in the prior art discussed below. Not only are such switch-based ±1 multipliers far easier to implement than precise analog multipliers, but the use of squared up oscillator signals greatly improves noise performance [I. Galton and C. Weltin-Wu, "Understanding Phase Error and Jitter: Definitions, Implications, Simulations, and Measurement," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 1, pp. 1-19, Jan. 2019.]

31. The in-phase and quadrature baseband signals mentioned above are generated by applying the RF input signal or the IF input signal to the inputs of a pair of such mixers, where the squared up oscillator signals applied to the two mixers differ in phase by 90 degrees. Lowpass filtering is always required following the mixer multiplication process, but engineers sometimes refer to just the ±1 multiplication process as the mixing process. Either way, by the 1990s it was commonly understood that lowpass filtering is essential following the ±1 multipliers in the baseband down-conversion process.

1. Synchrony

32. A well-known way to avoid the need to create two baseband signals, i.e., in-phase and quadrature baseband signals, is to use a single mixer that multiplies by ±1 with a frequency and phase which precisely matches those of the carrier of the received signal. In such cases, the required oscillator signal is generated by a carrier

synchronization circuit (also know as a carrier recovery circuit). The carrier synchronization circuit's input is the RF or IF signal, and its output is an oscillator signal with a frequency and phase that ideally match those of the input signal.

D. Amplifiers

33. As mentioned above, amplification is essential to the wireless reception process. The overall amplification gain from the antenna through to a receiver's baseband signals is typically many orders of magnitude. Amplifier nonlinearity has the potential to convert power from unwanted signals to distortion components that land within the frequency band of the desired signal, thereby corrupting the desired signal. As the distortion components grow disproportionately with the power of the unwanted signals and the unwanted signals often have much higher power than the desired signal, the amplifiers in wireless receivers must be designed to have a high degree of linearity.

1. Differential Circuits

34. IC implementations of circuit blocks such as amplifiers are often differential, meaning that they process pairs of signals wherein the signal information is represented as the difference between the two signals of each pair. For example, suppose the differential inputs to an amplifier circuit are denoted as v_{in+} and v_{in-}. Then the so-called differential-mode signal, defined as $v_{in} = v_{in+} - v_{in-}$, conveys the desired information content of the differential signal. Note that this

definition implies $v_{in+} = v_{in\text{-}cm} + v_{in}/2$ and $v_{in-} = v_{in\text{-}cm} - v_{in}/2$, where $v_{in\text{-}cm} = (v_{in+} + v_{in-})/2$. The $v_{in\text{-}cm}$ signal is called the common-mode signal. Therefore, the differential-mode signal is the difference between the two voltages and the common-mode signal is the average of the two voltages. As the signal information is conveyed by the differential-mode signal and differential circuits are designed not to process the common-mode signal (e.g., a differential amplifier amplifies its differential-mode input signal but does not significantly amplify its common-mode input signal), differential circuits are not sensitive to noise and distortion that equally affects the two signals which make up each of its differential signals.

35. Differential circuits are designed and laid out on an IC as symmetrically as possible, so it is the case that much of the inevitable non-ideal circuit behavior which corrupts any given differential signal, does so in the same way to both of the differential signal's two constituent signals. For example, even order nonlinear distortion corrupts each signal nearly equally, so differential circuits tend to be insensitive to even order nonlinear distortion. However, this benefit requires good symmetry between the two halves of a differential circuit. For example, two inputs of a differential amplifier must have matching input impedances for the above-mentioned benefit to occur.

36. Another benefit of a differential circuit is that it has twice the signal range as that of a comparable non-differential circuit. This quadruples the signal

power, whereas it only doubles power of the noise introduced by the circuit, which corresponds to a signal-to-noise ratio (SNR) improvement of 3 dB. Modifying the non-differential circuit to improve its SNR by 3 dB would typically double its power consumption. As differential circuits typically consume less than twice the power of corresponding non-differential circuits with comparable SNRs, differential circuits are generally more efficient than non-differential circuits in terms of power consumption.

37. For the above reasons, as would have been recognized by a POSITA in the mid 1990's, differential circuits that are designed and laid out to be as symmetrical as possible are generally preferable to non-differential circuits in IC implementations.

2. Low-pass filter or Antialiasing filter

38. Lowpass filters are essential components in direct-conversion receivers as described above. In applications where the baseband signals are to be subsequently sampled, lowpass filters are also sometimes called an antialiasing filters.

39. One particular differential lowpass filter is shown in Fig. 1, as presented in Macnally (TI-1021/TI-1022) as an antialias filter. As explained in Macnally, this is a fourth-order Butterworth filter implemented as a cascade of two of the differential Rauch biquads. Each antialiasing filter described in Macnally has this

form, although Macnally does not specify the component values. Instead, Macnally states that the filter is a Butterworth filter with a −3 dB bandwidth of 2.4 MHz, and a gain of 15.6 dB. The purpose of this section is to analyze the circuit shown in Fig. 1 and choose component values, i.e., values of R_1, R_2, R_3, R_4, C_1, C_2, C_3, and C_4, which cause Fig. 1 to achieve the same −3 dB bandwidth and gain as the corresponding filter presented in Macnally under the constraint that the component values are appropriate for integration in a 0.6 micron CMOS process (the IC technology in which the circuit presented in Macnally was implemented)

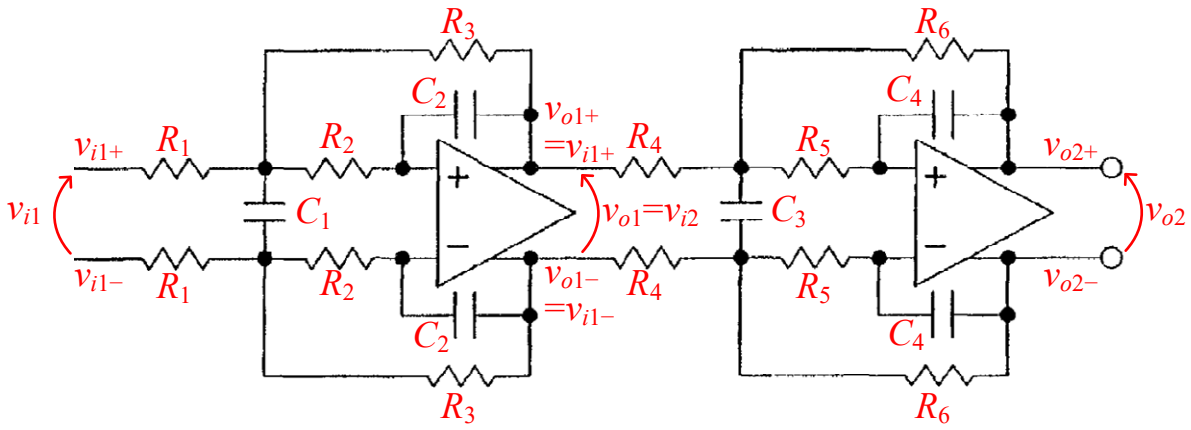


Figure 1: Annotated copy of the antialiasing filter shown in Fig. 3 of Macnally(TI-1021/TI-1022)

40. A POSITA would recognize that differential-mode behavior of the circuit of Fig. 1 can be analyzed via the differential-mode half circuit shown in Fig. 2, and that each stage can be analyzed in isolation from the other stage [K. R. Laker, W. M. C. Sansen, "Design of Analog Integrated Circuits and Systems," First. Ed., McGraw-Hill, 1994 ("Laker")], [E. Foster, "Active low-pass filter design," *IEEE Transactions on Audio*, vol. AU-13, no. 5, pp. 104-111, September-October 1965

("Foster"]. A POSITA would also recognize that each operational amplifier in such a circuit would be designed to have an open loop DC gain that is much higher than the closed-loop gain of each filter stage over the bandwidth of the filter, and, consequently, that

$$v_{m1}(s) = 0 \quad \text{and} \quad v_{m2}(s) = 0, \tag{1}$$

to a good approximation.

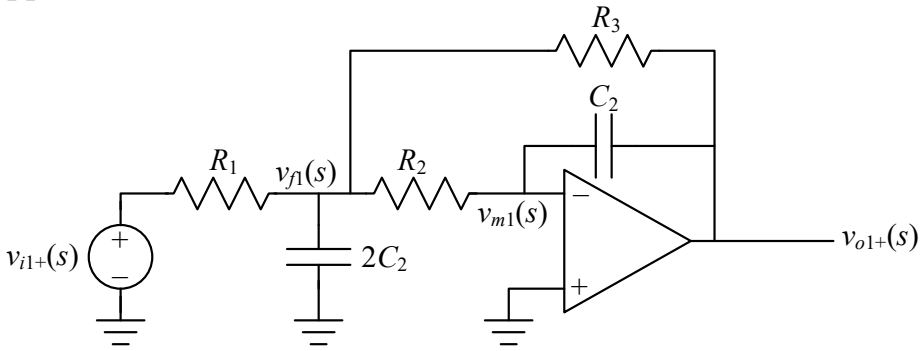


Figure 2: Differential-mode half-circuit corresponding to the first stage of Figure 1.

41. Applying Kirchoff's Current Law with (1) to the node at the negative terminal of the first op-amp and to the $v_{f1}(s)$ node in Fig. 1 yields

$$v_{o1+}(s)sC_2 + \frac{v_{f1}(s)}{R_2} = 0, \tag{2}$$

and

$$\frac{v_{f1}(s) - v_{i1+}(s)}{R_1} + v_{f1}(s)2sC_1 + \frac{v_{f1}(s) - v_{o1+}(s)}{R_3} + \frac{v_{f1}(s)}{R_2} = 0, \tag{3}$$

respectively.

42. Equation (3) can be rearranged as

$$v_{f1}(s)\left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + 2sC_1\right] - \frac{v_{i1+}(s)}{R_1} - \frac{v_{o1+}(s)}{R_3} = 0, \tag{4}$$

43. Solving (2) for $v_{f1}(s)$ and substituting the result into (4) gives

$$-v_{o1+}(s)sR_2C_2\left[\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}+2sC_1\right]-\frac{v_{i1+}(s)}{R_1}-\frac{v_{o1+}(s)}{R_3}=0, \tag{5}$$

Rearranging (5) gives

$$\frac{v_{o1+}(s)}{v_{i1+}(s)}=-\frac{1}{s^2\left(2R_1C_1R_2C_2\right)+s\left(R_1+R_2+\frac{R_1R_2}{R_3}\right)C_2+\frac{R_1}{R_3}}, \tag{6}$$

By symmetry, it follows that

$$\frac{v_{o1-}(s)}{v_{i1-}(s)}=\frac{v_{o1+}(s)}{v_{i1+}(s)}, \tag{7}$$

44. By definition, the differential-mode input and output signals of the first filter stage are $v_{i1}(s) = v_{i1+}(s) - v_{i1-}(s)$ and $v_{o1}(s) = v_{o1+}(s) - v_{o1-}(s)$, respectively, $v_{i1-}(s) = -v_{i1+}(s)$, and $v_{o1-}(s) = -v_{o1+}(s)$ (this is a small-signal analysis, so the common-mode voltages are taken to be zero). As this implies $v_{i1+}(s) = v_{i1}(s)/2$, and $v_{i1-}(s) = -v_{i1}(s)/2$, it follows from (7) that the differential-mode gain of the first stage, i.e., $A_1(s) = v_{o1}(s)/v_{i1}(s)$, is given by the right side of (6), i.e.,

$$A_1(s)=-\frac{1}{s^2\left(2R_1C_1R_2C_2\right)+s\left(R_1+R_2+\frac{R_1R_2}{R_3}\right)C_2+\frac{R_1}{R_3}}, \tag{8}$$

45. By identical reasoning, the differential-mode gain of the second filter stage, i.e., $A_2(s) = v_{o2}(s)/v_{i2}(s)$, is

$$A_2(s)=-\frac{1}{s^2\left(2R_4C_3R_5C_4\right)+s\left(R_4+R_5+\frac{R_4R_5}{R_6}\right)C_4+\frac{R_4}{R_6}}, \tag{9}$$

46. Therefore, the differential-mode frequency response of the filter shown in Fig. 1 is given by the product of (8) and (9) with *s* replaced by $j2\pi f$, i.e.,

$$A(j2\pi f) = A_1(j2\pi f)\,A_2(j2\pi f), \tag{10}$$

where *f* denotes frequency in Hz and *j* is the unit-magnitude imaginary number.

47. As shown in [Foster], the circuit with

$$R_1 = R_2 = R_3 = R_4 = R_5 = R_6 = R \tag{11}$$

for any positive value of *R* implements a Butterworth filter with a −3 dB bandwidth of f_0 and unity gain provided the capacitor values are chosen as:

$$C_1 = \frac{1}{2}\cdot\frac{3.91969}{2\pi f_0 R},\quad C_2 = \frac{0.25512}{2\pi f_0 R},\quad C_3 = \frac{1}{2}\cdot\frac{1.62359}{2\pi f_0 R},\text{ and }\ C_4 = \frac{0.61592}{2\pi f_0 R}. \tag{12}$$

Given that f_0 = 2.4 MHz, choosing *R* = 1000 Ω in (12) yields capacitor values which are easily realizable in the 0.6 micron CMOS technology used in [Macnally, TI-1021/1022], and large enough that the circuit's noise performance is unlikely to be problematic. The resulting capacitor values are:

$$C_1 = 130\text{ pF},\quad C_2 = 17\text{ pF},\quad C_3 = 53.8\text{ pF},\text{ and }\ C_4 = 40.8\text{ pF}. \tag{13}$$

48. While these component values in the circuit of Fig. 1 yield a Butterworth filter with the desired −3 dB bandwidth, its DC gain is 0 dB whereas the target DC gain of the overall filter is 15.6 dB. Therefore, it is necessary to modify these component values. A generally good design choice is to have each filter stage contribute half the DC gain, i.e.,

$$A_1(0) = A_2(0) = A_0 \quad \text{where} \quad A_0 = 10^{\frac{15.6/2}{20}} = 2.4547\,. \tag{14}$$

49. Setting $s = 0$ in (8) and (9) shows that the DC gains of the first and second filter stages are given by $-R_3/R_1$ and $-R_6/R_4$, respectively. For good noise performance, it is preferable to increase the DC gain of the two stages by increasing R_3 and R_6 rather than decreasing R_1 and R_4. Therefore, setting $R_3 = R_6 =$ 2454.7 Ω and keeping the other resistors at 1000 Ω gives the desired DC gain. However, to maintain the same frequency response, the capacitor values must be changed to maintain the original pole frequencies. This can be done by ensuring that the coefficients of s^2 and s in (8) and (9) change by the same factor of A_0^{-1} by which the new values of R_3 and R_6 caused the s^0 coefficients to change. Inspection of (8) and (9) shows that this requirement is achieved if C_2 and C_4 are changed to

$$C_2 \frac{R_1 + R_2 + \frac{R_1 R_2}{R_3} A_0}{A_0\left(R_1 + R_2 + \frac{R_1 R_2}{R_3}\right)}, \quad \text{and} \quad C_4 \frac{R_4 + R_5 + \frac{R_4 R_5}{R_6} A_0}{A_0\left(R_4 + R_5 + \frac{R_4 R_5}{R_6}\right)}, \tag{15}$$

respectively, and C_1 and C_3 are changed to

$$C_1 \frac{R_1 + R_2 + \frac{R_1 R_2}{R_3}}{R_1 + R_2 + \frac{R_1 R_2}{R_3} A_0}, \quad \text{and} \quad C_3 \frac{R_4 + R_5 + \frac{R_4 R_5}{R_6}}{R_4 + R_5 + \frac{R_4 R_5}{R_6} A_0}, \tag{16}$$

respectively. Therefore, the revised component values are

$$R_1 = R_2 = R_4 = R_5 = 1000\,\Omega \quad \text{and} \quad R_3 = R_6 = 2454.7\,\Omega \tag{17}$$

and

$$C_1 = 104.3 \text{ pF}, \quad C_2 = 8.6 \text{ pF}, \quad C_3 = 43.2 \text{ pF}, \text{ and } \quad C_4 = 20.7 \text{ pF}. \tag{18}$$

50. The above shows that circuit of Fig. 1 with the component values given by (17) and (18) implements the desired filter. It also shows that the filter's frequency response is given by (10) with $A_1(s)$ and $A_2(s)$ given by (8) and (9), respectively, with component values given by (17) and (18) and s replaced by $j2\pi f$. Fig. 3 shows a plot of the magnitude of the filter's frequency response in dB, i.e., a plot of $20\log(|A(j2\pi f)|)$, versus frequency in Hz on a log scale. As can be seen from the plot, the DC gain of the filter is 15.6 dB and the filter's −3 dB frequency is 2.4 MHz, as intended.

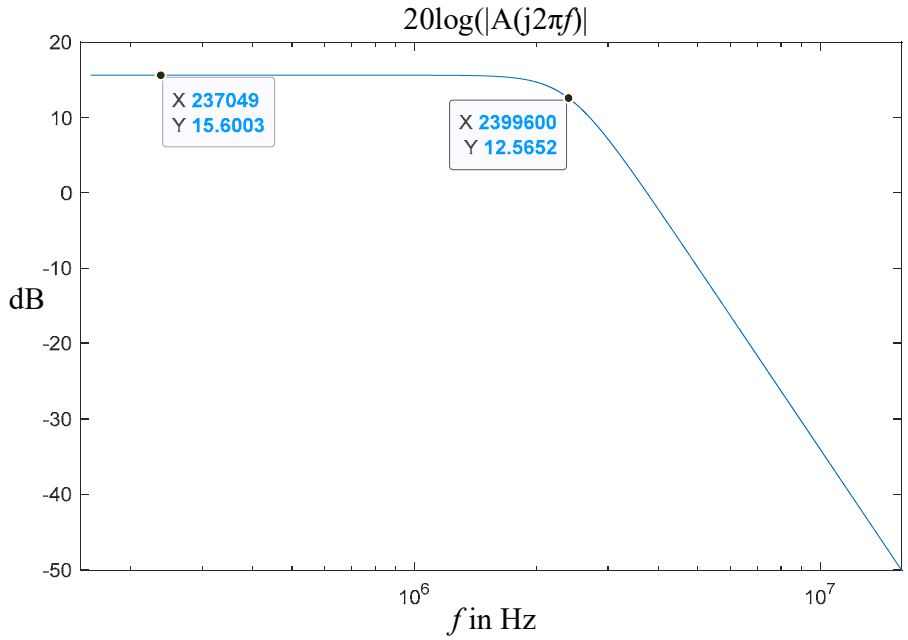


Figure 3: Magnitude of the differential-mode frequency response of the filter shown in Fig. 1 with component values given by (17) and (18).

51. In my opinion, the challenged claims of the '528 Patent represent obvious combinations of the features and technologies described above, as further discussed below.

VII. THE '528 PATENT

52. In this section, I provide an overview of the '528 Patent, a summary of the prosecution history, and a listing of the challenged claims.

A. Overview

53. The '528 Patent is titled "*Method and System for Down-converting an Electromagnetic Signal, and Transforms for Same, and Aperture Relationships*." EX1001. The underlying application was filed on February 4, 2014, and is continuation of application No. 13/549,213, filed on Jul. 13, 2012, now Pat. No. 8,660,513, which is a continuation of application No. 12/976,839, filed on Dec. 22, 2010, now Pat. No. 8,340,618, which is a continuation of application No. 12/349,802, filed on Jan. 7, 2009, now Pat. No. 7,865,177, which is a division of application No. 09/550,644, filed on Apr. 14, 2000, now Pat. No. 7,515,896, which is a continuation in-part of application No. 09/293,342, filed on Apr. 16, 1999, now Pat. No. 6,687,493, which is a continuation-in-part of application No. 09/176,022, filed on Oct. 21, 1998, now Pat. No. 6,061,551.

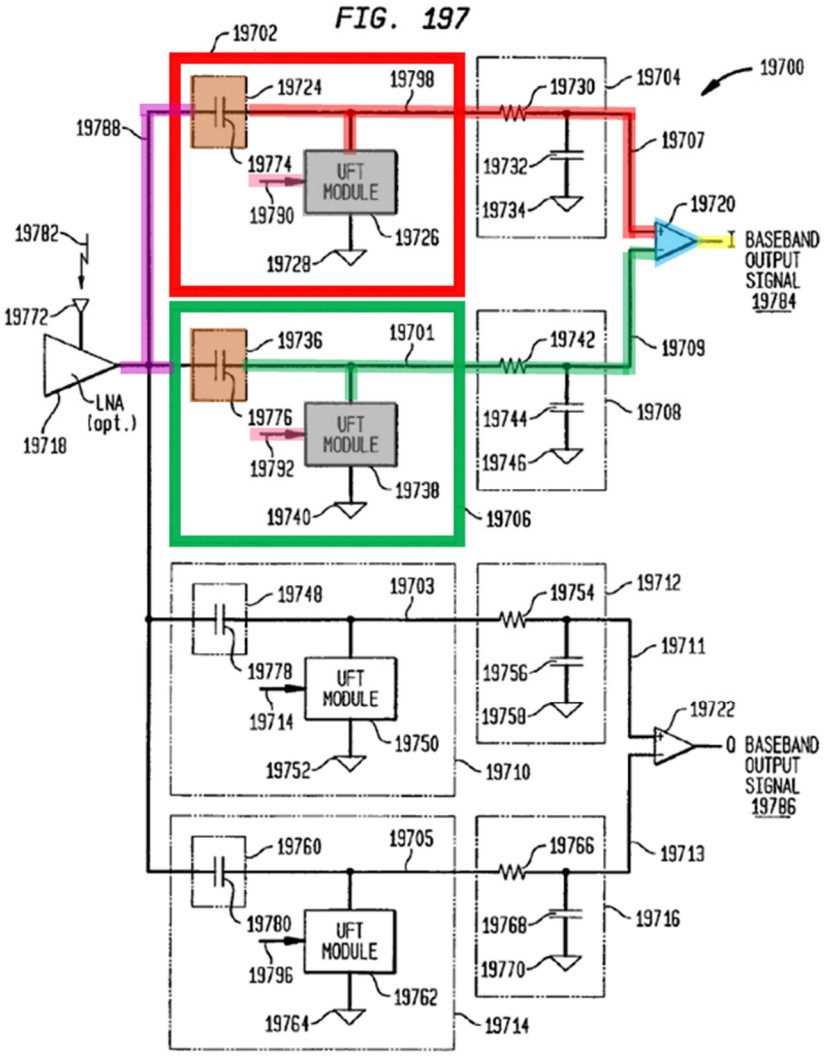
54. For purposes of my analysis, I have been informed that the priority date of the '528 patent is not presumed to be October 21, 1998. However, I have been informed that references in the proposed grounds (below) qualify as prior art because each of those references was filed and/or published before this date, referred to as Critical Date in my declaration. I understand that claims of the '528 Patent may not be entitled to the priority date of October 21, 1998, and TI may challenge the priority date of the claims in other proceedings.

B. Specification

55. The '528 Patent purports to improve "conventional signal processing technology [that] is limited in operational speed," (TI-1001, 2:28-32), by "down-converting an electromagnetic (EM) signal." *Id.*, Abstract ("In another embodiment, the EM signal is down-converted to a baseband information signal").

56. Specifically, the '528 Patent describes "an example I/Q modulation receiver 19700 [that] receives, down-converts, and demodulates a I/Q modulated RF input signal 19782 to an I baseband output signal 19784, and a Q baseband output signal 19786." TI-1001, 176:38-55, 56-60 ("LNA 19718 amplifies I/Q modulated RF input signal 19782, and outputs amplified I/Q signal 19788."). The I/Q modulation receiver 19700 includes four modules, namely, first processing module 19702, second processing module 19706, third processing module 19710, and fourth

processing module 19714, all of which receives amplified I/Q signal 19788. *Id.*, 176:61-179:52.



TI-1001, FIG. 197 (annotated)

57. First Processing module 19702 [red] down-converts the I-phase signal portion of amplified input I/Q signal 19788 [purple] according to an I control signal 19790 [orange]." TI-1001, 176:61-177:10 ("first Processing module 19702 comprises a first storage module 19724 [(brown)], a first UFT module 19726

[(gray)]" and "a switch contained within first UFT module 19726 opens and closes as a function of control signal 19790 [to generate] a down-converted signal, referred to as I output signal 19798").

58. "Second Processing module 19706 down-converts the inverted I-phase signal portion of amplified input I/Q signal 19788 according to an inverted I control signal 19792." TI-1001, 177:32-34, 36-48 ("second Processing module 19706 comprises a second storage module 19736, a second UFT module 19738" and "a switch contained within second UFT module 19738 opens and closes as a function of inverted I control signal 19792 [to generate] a down-converted signal, referred to as inverted I output signal 19701").

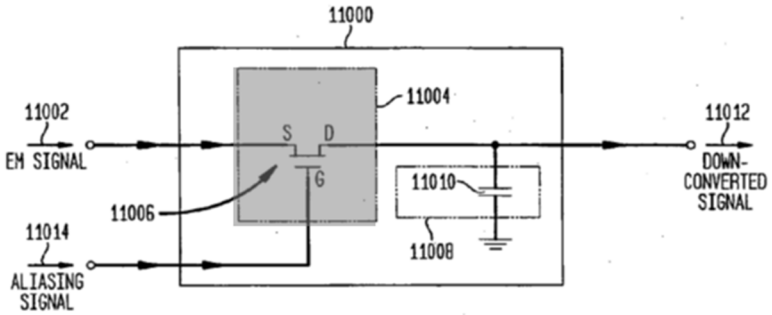
59. I output signal 19798 and inverted I output signal 19701 are filtered to generate, respectively, filtered I output signal 19707 and filtered inverted I output signal 19709. TI-1001, 177:16-30, 177:55-178:2. "First differential amplifier 19720 receives filtered I output signal 19707 at its non-inverting input and receives filtered inverted I output signal 19709 at its inverting input" to generate "I baseband output signal 19784." *Id.*, 178:3-8.

60. Similarly, third processing module 19710 and fourth processing module 19714 also operate on amplified input I/Q signal 19788 and produce, respectively, a Q output signal 19703 and an inverted Q output signal 19705. TI-1001, 178:26-179:22. The Q output signal 19703 and the inverted Q output signal

19705 are filtered by respective filters to generate filtered Q output signal 19711 and filtered inverted Q output signal 19713. *Id.*, 178:48-61. "Second differential amplifier 19722 receives filtered Q output signal 19711 at its non-inverting input and receives filtered inverted Q output signal 19713 at its inverting input" to generate Q baseband output signal 19786. *Id.*, 179:34-40.

61. The '528 Patent discloses examples of UFT module as FET switches. *See e.g.*, 108:30-31("As shown in FIG. 110A [annotated below], UFT module 11004 [green] is implemented as an-channel FET 11006"), 109:56-57 ("UFT module 11206 [in Fig. 112] comprises n-channel FET 11204, and UFT module 11216 comprises p-channel FET 11218."), 108:40-51 ("signal 11014 controls the gate of FET 11006 so that FET 11006 conducts (or turns on) when the FET gate to-source voltage (V Gs) exceeds a threshold voltage (V r)When the FET 11006 conducts, a channel is created from source to drain of FET 11006 so that charge is transferred from the EM signal 11002 to the capacitor 11010").

FIG. 110A



TI-1001, FIG. 110A (annotated)

62. The Challenged Claims are directed to the down-conversion apparatus shown in Fig. 197. For example, independent claim 1 recites two of the four processing modules, while dependent claim 19 recites the other two of the four processing modules. The remaining dependent claims are directed to other aspects. TI-1001, 192:32-196:29.

63. In my opinion, these limitations were well-known before the Priority Date.

C. Prosecution History

64. The Challenged Claims were allowed when Applicant replaced original claim 1 with a new set of claims 2-37 citing, e.g., Fig. 197 of the specification. TI-1002, 1601-13 (Response on 3/9/2015 to Office Action). The new set of claims became issued claims 1-36.

65. Applicant alleged that US 6,192,225 (Arpaia), the prior art applied by the Examiner, "does not mention any kind of sampling signal that, as applied to a switch, *serves to provide energy of the modulated carrier signal [that] is sampled and differentially applied to the respective integration module and energy storage elements at the frequency of the respective control signal's aperture as set forth in the claims*." *Id.*, 1603 (emphasis original). Applicant further asserted that Arpaia does not teach or suggest "the portions of transferred energy from each of the first

and second switch [being] integrated over time to accumulate said portions of transferred energy from which said down-converted in-phase baseband signal portion and said down-converted inverted in-phase baseband signal portion are derived," as recited by issued claim 1. *Id.*, 1604.

66. In my opinion, the alleged features were well-known by the Critical Date.

D. Claims

67. I understand that TI challenges 1-5, 8-9, 11-14, 15-19, 23, 26-27, 29-36 of the '528 patent, which I reproduce below:

Claim 1	
1(a)	A system for frequency down-converting a modulated carrier signal to a baseband signal, comprising:
1(b)	a first switch coupled to a first control signal which comprises a sampling aperture with a specified frequency, wherein the first switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal as an output of said first switch during the sampling aperture of said first switch;
1(c)	a first energy storage element that stores the transferred energy from the modulated carrier signal and outputs a down-converted in-phase baseband signal portion of said modulated carrier signal;
1(d)	a second switch coupled to a second control signal which comprises a sampling aperture with a specified frequency, wherein the second switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal as an output of said second switch during the sampling aperture of the second control signal;
1(e)	a second energy storage element that stores the transferred energy from the modulated carrier signal and outputs a down-converted inverted in-phase baseband signal portion of said modulated carrier signal;

1(f)	wherein the portions of transferred energy from each of the first and second switch are integrated over time to accumulate said portions of transferred energy from which said down-converted in-phase baseband signal portion and said down-converted inverted in-phase baseband signal portion are derived; and
1(g)	a first differential amplifier circuit that combines said down-converted in-phase baseband signal portion with said down-converted inverted in-phase baseband signal portion and outputs a first channel down-converted differential in-phase baseband signal.
Claim 2	
2	The system of claim 1, wherein said modulated carrier signal includes an amplitude variation.
Claim 3	
3	The system of claim 1, wherein said modulated carrier signal includes a phase variation.
Claim 4	
4	The system of claim 1, wherein said modulated carrier signal includes a combination of amplitude variation and phase variation.
Claim 5	
5	The system of claim 1, wherein the first switch is on for less than one-half cycle of the modulated carrier signal.
Claim 8	

8	The system of claim 1, wherein the first and second control signals each control a charging and discharging cycle of their respective energy storage element by respectively controlling the first and second switching devices[2] so that for each switching device[3] said portion of energy that is distinguishable from noise is transferred to the respective storage element when the switch is on during the charging cycle, and a portion of the transferred energy is discharged during the discharging part of the cycle for each respective switching device[4] when the switching device[5] is off.
Claim 9	
9	The system of claim 8, wherein for each respective storage element, the energy discharged during any given discharge cycle is not completely discharged, with the remaining undischarged energy from the given discharge cycle becoming an initial condition for the next charging cycle
Claim 11	
11	The system of claim 1, wherein the frequencies of the first and second apertures have periods that are two (2) percent or greater of the modulated carrier signal's period.
Claim 12	
12	The system of claim 1, wherein the frequencies of the first and second apertures have periods that are five (5) percent or greater of the modulated carrier signal's period.
Claim 13	
13	The system of claim 1, wherein the frequencies of the first and second apertures have periods that are ten (10) percent or greater of the modulated carrier signal's period.
Claim 14	

[2] "switches"

[3] "switch"

[4] "switch"

[5] "switch"

14	The system of claim 1, wherein the frequencies of the first and second apertures have periods that are twelve and a half (12.5) percent or greater of the modulated carrier signal.
Claim 15	
15	The system of claim 1, further comprising: a first filter that filters said down-converted in-phase baseband signal portion; and a second filter that filters said down-converted inverted in-phase baseband signal portion
Claim 16	
16	The system of claim 15, wherein the first and second filters each comprise a low-pass filter.
Claim 17	
17	The system of claim 1, wherein said portions of transferred energy from each of the first and second switch which are integrated over time to accumulate said portions of transferred energy are integrated by a separate integration module coupled to the output of each said first and second switch.
Claim 18	
18	The system of claim 1, wherein said first and second storage elements are capacitive storage circuits, and wherein said portions of transferred energy from each of the first and second switch which are integrated over time to accumulate said portions of transferred energy are integrated by the capacitive storage circuits as they accumulate charge during successive sampling apertures.
Claim 19	
19(a)	The system of claim 1, further comprising:
19(b)	a third switch coupled to a third control signal which comprises a sampling aperture with a specified frequency, wherein the third switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal as an output of said third switch during the sampling aperture of the third control signal;

19(c)	a third energy storage element that stores the transferred energy from the modulated carrier signal and outputs a down-converted quadrature-phase baseband signal portion of said modulated carrier signal
19(d)	a fourth switch coupled to a fourth control signal which comprises a sampling aperture with a specified frequency, wherein the fourth switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal as an output of said fourth switch during the sampling aperture of the fourth signal;
19(e)	a fourth energy storage element that stores the transferred energy from the modulated carrier signal and outputs a down-converted differential[6] quadrature-phase baseband signal portion of said modulated carrier signal;
19(f)	wherein the portions of transferred energy from each of the third and fourth switch are integrated over time to accumulate said portions of transferred energy from which said down-converted quadrature-phase baseband signal portion and said down-converted differentia[7]l quadrature-phase baseband signal portion are derived; and
19(g)	a second differential amplifier circuit that combines said down-converted quadrature-phase baseband signal portion with said down-converted differential[8] quadrature-phase baseband signal portion and outputs a second channel down-converted differential quadrature-phase baseband signal.
Claim 20	
20	The system of claim 19, wherein said modulated carrier signal includes an amplitude variation..
Claim 21	
21	The system of claim 19, wherein said modulated carrier signal includes a phase variation.
Claim 22	

[6] "inverted"

[7] "inverted"

[8] "inverted"

22	The system of claim 19, wherein said modulated carrier signal includes a phase variation.
Claim 23	
23	The system of claim 19, wherein the third switch is on for less than one-half cycle of the modulated carrier signal.
Claim 26	
26	The system of claim 19, wherein the third and fourth control signals each control a charging and discharging cycle of their respective third and fourth energy storage element by respectively controlling the third and fourth switching devices so that for each third and fourth switching device a portion of energy that is distinguishable from noise is transferred to the respective third and fourth storage element when the respective switch is on during the charging cycle, and a portion of the transferred energy is discharged during the discharging part of the cycle for each respective third and fourth switching device when the respective switching device is off
Claim 27	
27	The system of claim 26, wherein for each respective energy storage element, the energy discharged during any given discharge cycle is not completely discharged, with the remaining undischarged energy from the given discharge cycle becoming an initial condition for the next charging cycle.
Claim 28	
28.	The system of claim 19, wherein the frequencies of the third and fourth apertures have periods that are two (2) percent or greater of the modulated carrier signal's period
Claim 30	
30	The system of claim 19, wherein the frequencies of the third and fourth apertures have periods that are five (5) percent or greater of the modulated carrier signal's period.
Claim 31	
31	The system of claim 19, wherein the frequencies of third and fourth apertures have periods that are ten (10) percent or greater of the modulated carrier signal's period

Claim 32	
32	The system of claim 19, wherein the frequencies of third and fourth apertures have periods that are twelve and a half (12.5) percent or greater of the modulated carrier signal's period
Claim 33	
33	The system of claim 19, further comprising: a first filter that filters said down-converted in-phase baseband signal portion; a second filter that filters said down-converted inverted in-phase base-band signal portion; a third filter that filters said down-converted quadrature-phase baseband signal portion; a fourth filter that filters said down-converted inverted quadrature-phase baseband signal portion.
Claim 34	
34	The system of claim 33, wherein the first, second, third, and fourth filters each comprise a low-pass filter.
Claim 35	
35	The system of claim 19, wherein said portions of transferred energy from each of the first, second, third and fourth switch which are integrated over time to accumulate said portions of transferred energy are integrated by a separate integration module coupled to the output of each said first, second, third and fourth switch respectively
Claim 36	
36	The system of claim 19, wherein said first, second, third and fourth storage elements are capacitive storage circuits, and wherein said portions of transferred energy from each of the first, second, third, and fourth switch which are integrated over time to accumulate said portions of transferred energy are integrated by the capacitive storage circuits of the respective first, second, third and fourth storage elements as they accumulate charge during successive sampling apertures.

VIII. LEVEL OF ORDINARY SKILL IN THE ART

68. In my opinion, based upon my knowledge and experience in this area, a POSITA as of October 21, 1998 would have had at least a bachelor's degree in electrical engineering or a related subject and two or more years of experience in the field of electromagnetic (EM) circuit design.

69. Less work experience may be compensated by a higher level of education, such as a master's degree.

70. The following factors support my opinion. My analysis is thus based on the perspective of a POSITA having this level of knowledge and skill at the relevant time of the invention.

71. For purposes of my analysis, I have been informed that the priority date of the '528 patent is deemed to be no earlier than October 21, 1998, and I have applied this timeframe as being the relevant time for the perspective of a POSITA.

IX. CLAIM CONSTRUCTION

72. As discussed above, for purposes of this proceeding, I have applied the ordinary and customary meaning of the claim terms as they would have been recognized and understood to a POSITA at the time of the alleged invention of the '528 Patent, and I have considered that meaning in the context of the patent and its prosecution history.

73. Based upon my review of the ’528 Patent and its prosecution history, as well as my knowledge and experience in this field, the claim terms do not require further explanation or elaborative definitions except the terms “storage element” and “energy storage element.” To the extent necessary, I am open for opining on other claims terms.

74. The terms “storage element” or “energy storage element” are used interchangeably. For example, claim 1 recites “a first energy storage element that stores the transferred energy from the modulated carrier signal and outputs a down-converted in-phase baseband signal portion of said modulated carrier signal” and “a second energy storage element that stores the transferred energy from the modulated carrier signal and outputs a down-converted inverted in-phase baseband signal portion of said modulated carrier signal.” TI-1001, Claim 1. Claim 18, which directly depends on claim 1, recites “said first and second storage elements.” Id., claim 18. Various dependent claims recite both terms interchangeably. See e.g., dependent claims 8-9.

75. The two terms are synonyms and should be construed to mean “***an element of a system that stores non-negligible amounts of energy from an input EM signal***.” The construction was determined by the Board when invalidating claim 3 of a related patent, namely, US, 7,110,444 (the ’444 patent). IPR2020-01265, Paper 44 at 36. The Board’s determination was subsequently affirmed by the Federal

Circuit on December 15, 2023. *ParkerVision, Inc. v. Vidal*, Case No. 22-1548 (Fed. Cir. Dec. 15, 2023), Slip Op. pp 10-12. In affirming the Board's decision, the Federal Circuit held that "ParkerVision acted as its own lexicographer to define the term 'storage element'" and "the Board's construction of 'storage element' [as quoted above] correctly tracks the lexicography provided by [ParkerVision]" from US6,061,551 ("551 patent), 66:55-67. *Id.*

76. The Board's construction of "storage element" in that case was based on the '444 patent's "incorporation of the '551 patent by reference." IPR2020-01265, Paper 44, 32. The same patent 6,061,551 is incorporated by reference in the '528 patent. TI-1001, 1:30-34.

77. As affirmed by the Federal circuit, "[t]he critical paragraph ['551 patent, 66:55-67] clearly expresses an intent to define the term 'storage element'" and "ParkerVision concedes as much." *ParkerVision,* Slip Op. pp 10-12 ("… this paragraph of the '551 patent then shifts to generally defining the terms 'storage module' and 'storage capacitance' … as 'terms,' [used by] the patent document as a whole…."). The Federal Circuit thus rejected ParkerVision's contention that "restricts a 'storage element' to an element of *an energy transfer system"* as if "this term ['storage element'] by itself necessarily invokes *an entire energy transfer system*." *Id.*, pp. 12-13; *see also* IPR2020-01265, Paper 44, 35-36 ("[t]his [critical]

portion of the ’551 patent specification [66:59–67] provides a lexicographic definition of the systems to which the terms refer”).

78. The ’528 patent includes an identical disclosure to that deemed dispositive from the incorporated by reference ’551 patent. TI-1001, 73:9-22 (defining “storage module” and “storage capacitance”). Thus, the terms “energy storage element” and “storage element” should be construed in accordance with the express definition provided in the specification.

79. Nothing from the claims, the specification, or the file history contradicts a different read. Claim 1 of the ’528 patent merely mentions “system,” “energy,” and “transfer” in isolation, but does not recite “energy transfer system,” let alone restrict the claimed “storage element” to any energy transfer system. The five sentences from the specification relied on by ParkerVision are the same five sentences from the ’551 patent incorporated by reference. *Compare* TI-1001, 73:9-22 (cited by TI-1010 at 16-17) *with* ‘551 patent, 66:55-67 (cited by *ParkerVision,* Slip Op. pp. 10-12). The file history likewise does not support a different construction.

80. I understand that in the parallel district court proceeding, TI and ParkerVision have submitted claim construction proposals for certain terms of the ’528 Patent. TI-1012. For the reasons detailed in the element-by-element analysis below, the prior art combinations that I analyzed herein would have achieved a

predictable result that is similar to the embodiment described in the '528 patent. Accordingly, based upon my review of the '528 Patent and the prior art combinations analyzed below, the Challenged Claims are rendered obvious regardless of whether any of those constructions were imposed in this proceeding. When the prior art combinations are rightfully understood, those construction proposals would not change the result in this proceeding.

X. OVERVIEW OF THE PRIOR ART

81. In this section, I provide an overview of the prior art references that I have relied on to inform my opinions.

A. U.S. Patent No. US 6,230,000 ("Tayloe")

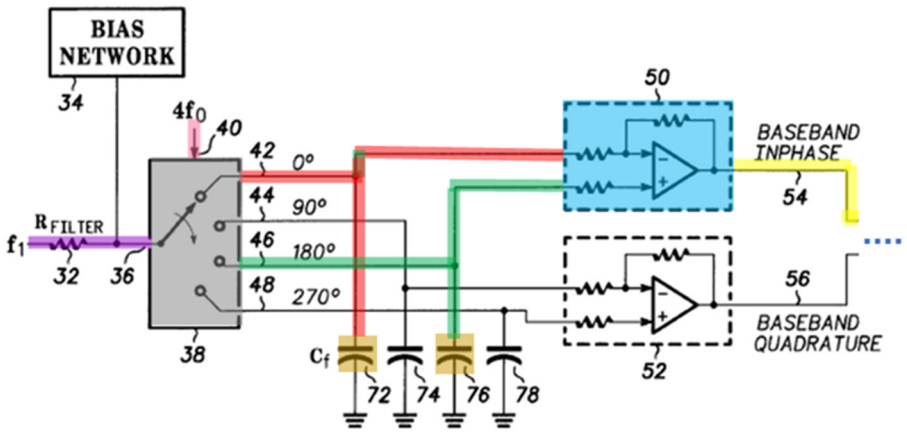
82. Tayloe is titled "*Product Detector and Method Thereof*." EX1004. It was filed on October 15, 1998.

83. Tayloe describes a direct conversion (i.e., the product detector) "for converting a signal to baseband." TI-1004, Abstract, 1:51-52 (de-scribing Figure 3). Tayloe explains that its direct conversion receiver:

> includes a commutating switch which serves to sample an RF waveform four times per period at the RF frequency. The samples are integrated over time to produce an average voltage at 0 degrees, 90 degrees, 180 degrees and 270 degrees. The average voltage at 0 degrees is the baseband in-phase signal . . . .

Id., Abstract. Tayloe discloses that, "to increase gain, the 0 degree average can be differentially summed with the 180 degree average to form the baseband in-phase signal . . . ." *Id.* Tayloe states that "[d]irect conversion receivers are desirable in part because they convert signals of interest directly to baseband (or near zero hertz) from a radio frequency (RF) or an intermediate frequency (IF)." *Id.* at 1:10–13.

84. In more detail, Tayloe discloses an example of a direct conversion receiver in Figure 3:



30 FIG. 3

TI-1004, Figure 3 (annotated).

85. The receiver receives an RF input signal f_I and down-converts this signal. *Id.*, 2:13-67 ("[A]n RF … signal f_I [purple] is received at resistor 32…. After passing through resistor 32, the input signal is received by commutating switch 38 [gray] at input 36. Commutating switch 38 switches input 36 to outputs 42 [red], 44,

46 [green], and 48…. As commutating switch 38 cycles through the four outputs, capacitors 72-78 charge to voltage values substantially equal to the average value of the input signal during their respective quadrants…. The outputs of commutating switch 38 are input to summing amplifiers 50 [light blue] and 52. Summing amplifier 50 [light blue] differentially sums the 0 degree output [42 (red)] and the 180 degree output [46 (green)], thereby producing baseband in-phase signal 54 [yellow]. The resulting signals are then summed by summing amplifier 60 to produce the signal of interest 62").

86. Like the '528 Patent, Tayloe's receiver has four frequency down-conversion modules, labeled "0º," "90º," "180º," and "270º," each including a switch and a storage element (*e.g.*, capacitor).

87. The 0º frequency down-conversion module provides a 0º down-converted signal 42 (red). TI-1004, 2:13-18 ("[A]n RF … signal f_1 [purple] is received at resistor 32…. After passing through resistor 32, the input signal is received by commutating switch 38 [gray] at input 36. Commutating switch 38 switches input 36 to output[] 42 [red]…."), 2:46-48 ("Output 42 [red represents the average value of the [RF] input signal [f_1 (purple)] during the first quarter wave of the period [of the input signal f_1], and is termed the 0 degree output.").

88. The 0º frequency down-conversion module includes a switch 38 (gray), which periodically couples the input signal f_1 (purple) to the output 42. TI-

1004,2:16-26. Moreover, the rate at which the switch 38 periodically couples the input signal f_1 at input 36 (purple) to the output 42 is determined by a control signal ($4f_0$, pink) supplied to a control input 40 of the switch. *Id.*, 2:18-20 ("The rate at which commutating switch 38 operates is controlled by a signal present at control input 40.").

89. While Tayloe shows commutating switch 38 as a single component without its specific structure. As explained below, a POSITA would have understood that Tayloe's commutating switch 38, especially in view of TI Datasheet and Kawada, comprises multiple switches. Accordingly, as noted below, a POSITA would understand that each down-conversion module includes its own switch within the commutating switch 38. Accordingly, as noted below, a POSITA would understand that each down-conversion module includes its own switch within the switch 38.

90. The 0º frequency down-conversion module also includes a capacitor 72 (brown). "During the time that [the] switch 38 connects input 36 [receiving the RF input signal f_1] to output 42, charge builds up on capacitor 72." TI-1004, 2:32-33. The voltage across the capacitor 72 corresponding to this charge constitutes the average value of the RF input signal f_1 during first quarter of the period of the signal f_1 and is output from the 0 degree frequency down-conversion module as the 0º down-converted signal 42 (red). *Id.*, 2:46-48 ("Output 42 [red] represents the

average value of the input signal during the first quarter wave of the period, and is termed the 0 degree output."), 2:18-26.

91. Similarly, the 180º frequency down-conversion module provides a 180º down-converted signal 46 (green). TI-1004, 2:13-18 ("After passing through resistor 32, the [RF] input signal [f_1] is received by commutating switch 38 [gray] at input 36. Commutating switch 38 switches input 36 to output[] … 46 [green]…."), 2:50-53 ("Output 46 [green] represents the average value of the input signal [f_1 (purple)] during the third quarter wave of the period [of the input signal f_1], and is termed the 180 degree output."), 2:18-26.

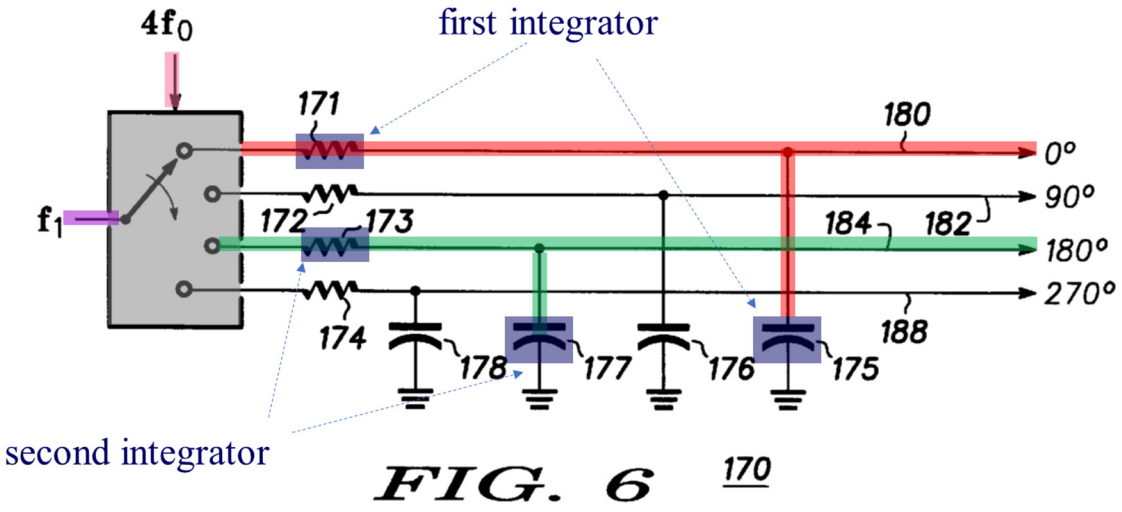
92. The 180º frequency down-conversion module includes the switch 38 (gray) and a capacitor 76 (brown). When the switch 38 couples the input signal f_1 (purple) to the output 46, charge builds up on the capacitor 76 (brown) in the same manner as charge builds up on the capacitor 72 described above. TI-1004, 2:18-38 ("During the time that commutating switch 38 connects input 36 to output 42, charge builds up on capacitor 72…. The same principle holds true for capacitor[] 76 … when commutating switch 38 connects input 36 to output[] 46….").) Thus, voltage across the capacitor 76 constitutes the average values of the RF input signal f_1 during the third quarter of the period of the signal f_1 and is output from the 180º frequency down-conversion module as the 180º down-converted signal 46 (green). *Id.*, 2:50-

53 ("Output 46 [green] represents the average value of the input signal during the third quarter wave of the period, and is termed the 180 degree output."), 2:18-26.

93. The 90º and 270º frequency down-conversion modules each have a similar operation and structure. TI-1004, 2:35-39 ("Likewise, during the time commutating switch 38 connects input 36 to output 44, charge builds up on capacitor 74. The same principle holds true for capacitor[] 78 when commutating switch 38 connects input 36 to output[] 48"). "As commutating switch 38 cycles through the four outputs, capacitors 72–78 charge to voltage values substantially equal to the average value of the input signal during their respective quadrants" *Id.*, 2:39-43. "Output 44 represents the average value of the input signal during the second quarter wave of the period, and is termed the 90 degree output." *Id.*, 2:48-50. "Output 48 represents the average value of the input signal during the fourth quarter wave of the period, and is termed the 270 degree output." *Id.*, 2:53-55.

94. Tayloe also discloses "an alternate embodiment in which each integrating capacitor has its own resistor." TI-1004, 4:48-49. Compared to Figure 3 (above), Figure 6 (below) of Tayloe shows "0 degree output 180 has a voltage controlled by the combination of capacitor 175 and resistor 171" and "180 degree output 184 has a voltage controlled by the combination of capacitor 177 and resistor 173." *Id.*, 4:49- 57 (further noting "90 degree output 182 has a voltage controlled

by the combination of capacitor 176 and resistor 172" and "270 degree output 188 has a voltage controlled by the combination of capacitor 178 and resistor 174.").



TI-1004, Figure 6 (annotated)

95. "Resistor 171 and capacitor 175 form a first integrator [(dark blue) for the 0° output (red) where the switch (gray)] connects the input to this first integrator for substantially 90 degree of the input signal [f_1 (purple)]." TI-1004, 4:57-60. Tayloe explains that "the remaining resistor/capacitor pairs [in Figure 6] also form integrators [including a second integrator (dark blue) for the 180° output (green)], each of which preferably integrates for substantially 90 degrees of the input signal [f_1 (purple)]." *Id.*, 4:60-67 (noting the integrators can have same or different time constants).

96. Capacitors 72 and 74 are connected to the top inputs of 50 and 52, respectively as indicated in Fig. 3. Each of 50 and 52 is a differential-input summing amplifier implemented as an operational amplifier with a resistor that connects its output to its negative input terminal two input resistors connected to the two operational amplifier input terminals. A POSITA would recognize that the feedback around the operational amplifier in conjunction with the operational amplifier's high DC gain causes the node to which the negative terminal of the operational amplifier is connected to have a very low resistance (typically well below a few ohms). Therefore, the input resistance looking into the top input of each of 50 and 52 is approximately equal to the resistance of the top-left resistor. A POSITA would understand that these resistors would have resistances on the order of kilo-ohms or less, so the Capacitors 72 and 74 are not connected to high-impedances. In particular, they will discharge with a voltage proportional to $e^{-t/RC}$, where t is time, R is the above-mentioned resistance (on the order of kilo-ohms), and C is the capacitance value of Capacitors 72 an 74.

97. Returning to the example in Figure 3 annotated *supra*, Tayloe discloses:

> The outputs of commutating switch 38 are input to summing amplifiers 50 and 52. Summing amplifier 50 [light blue] differentially sums the 0 degree output [red] and the 180 degree output [green], thereby producing baseband in-phase signal 54. Summing amplifier 52 differentially sums the 90 degree

output and the 270 degree output, thereby producing base band quadrature signal 56.

(*Id.*, 2:56-67)

98. I have provided explanation of fully differential amplifiers in Section VI.

99. As explained above, the direct conversion receiver operates switch 38, which is "controlled by a signal [pink] present at control input 40." TI-1004, 2:17-20. This control signal (pink) causes switch 38 to couple the RF input signal f_1 to one of the four outputs 42, 44, 46, and 48 so that the RF input signal f_1 is sampled four times during a full cycle in which, as illustrated in Figure 4 (below), "[p]oint 105 represents the voltage to which capacitor 72 (FIG. 3) charges," "point 110 represents the voltage to which capacitor 74 charges, point 115 represents the voltage to which capacitor 76 charges, and point 120 represents the voltage to which capacitor 78 charges." *Id.*, 3:41-48.

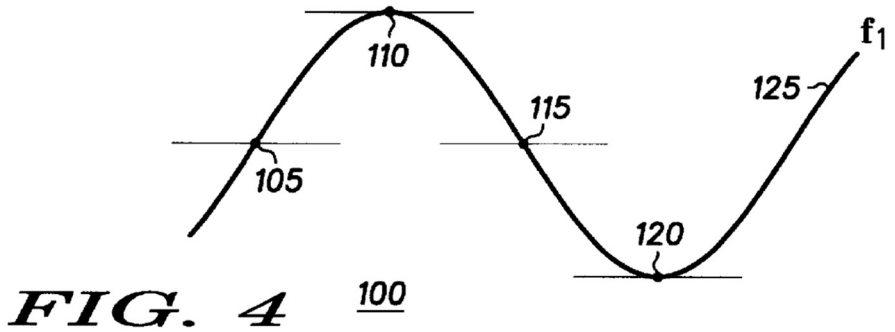
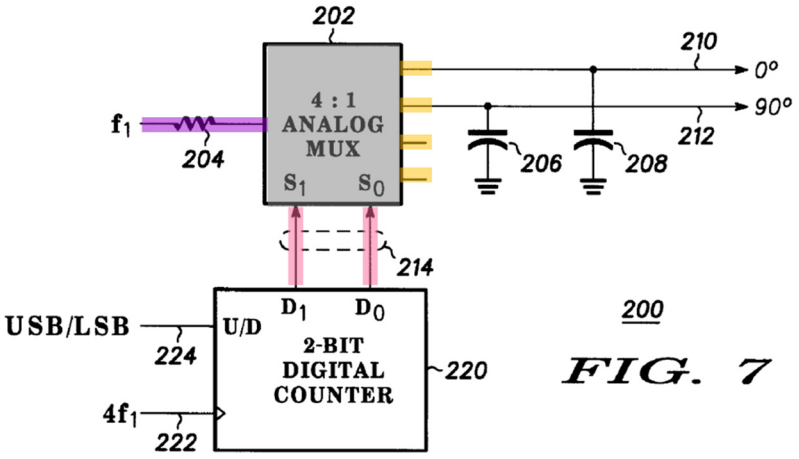


FIG. 4

TI-1004, Figure 4

100. Tayloe further expressly discloses implementing "direct conversion receiver 30 (FIG. 3) utilizing an analog multiplexer and a digital counter as shown in FIG. 7 [annotated below]." TI-1004, 5:33-37.



TI-1004, Figure 7 (annotated)

101. As an embodiment of switch 38 (Figure 3), multiplexer 202 (above) acts as a demultiplexer, connecting a single input signal f_1 (purple) to one of four outputs (orange) based on control signals 214 (pink) (corresponding to the control input 40 in Figure 3). Tayloe specifically discloses that "[t]he analog multiplexer is a Texas Instruments SN74BCT3253D." *Id.*, 5:33-37, 5:1-16 ("… input signal f_1 is connected to each of the four outputs of analog multiplexer 202 for substantially 90 degrees of the input signal.").

102. Tayloe specifically refers to a TI "SN74BCT3253D" multiplexer. The "BCT" lettering (as opposed to "CBT") appears a typographical error. The TI Datasheet is also descriptive of all SN74BCT3253 multiplexers, explaining that the

"D" in the product number refers to a packaging option ("Plastic Small-Outline (D)") for the SN74BCT3253 multiplexer.

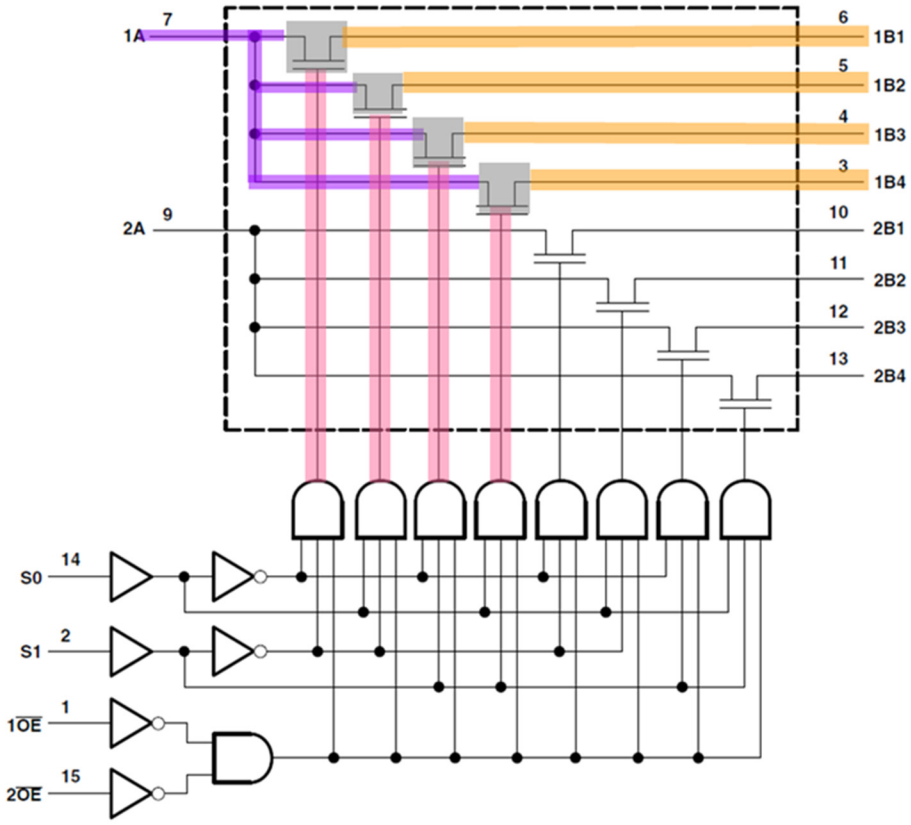
103. I discuss the implementation details of the SN74CBT3253D multiplexer/demultiplexer are disclosed in TI Datasheet (TI-1005) below.

B. TI Datasheet

104. The TI Datasheet describes the SN74CBT3253 multiplexer/demultiplexer, a commercially available electronic component that can be used in a radio receiver such as Tayloe's receiver. TI-1005, 1; TI-1004, 5:33-37 (describing radio receiver including the SN74CBT3253 multiplexer)).

105. Multiplexers are well-known electronic devices that receive multiple input signals and select one signal to be output. A multiplexer such as the one disclosed in TI Datasheet can also operate in reverse as a demultiplexer—receiving a single input signal and routing it to one of several output lines—as reflected in the device's name ("SN74CBT3253 Dual 1 of 4 FET ***Multiplexer/Demultiplexer***").

106. Tayler uses the SN74CBT3253 multiplexer/demultiplexer as a demultiplexer. This SN74CBT3253 multiplexer/demultiplexer shows additional details of how Tayloe's switch 38 would connect the single input signal to one of multiple output lines, and in particular, the demultiplexing operation is shown below.



107. The TI multiplexer/demultiplexer has four switches (gray) that selectively supply the input signal 1A (purple) to one of four outputs 1B1-1B4 (orange) according to four control signals (pink), respectively. The control signals are generated based on control logic that ensures only one of the four switches is turned on at a time. TI-1005, 1("1$\overline{OE}$, 2$\overline{OE}$, S0, and S1 select the appropriate output for the A-input data"). The functional mapping of the control signals is shown in Table 1 below:

FUNCTION TABLE

INPUTS				FUNCTION
$1\overline{OE}$	$2\overline{OE}$	S1	S0	
X	H	X	X	Disconnect 1A and 2A
H	X	X	X	Disconnect 1A and 2A
L	L	L	L	1A to 1B1 and 2A to 2B1
L	L	L	H	1A to 1B2 and 2A to 2B2
L	L	H	L	1A to 1B3 and 2A to 2B3
L	L	H	H	1A to 1B4 and 2A to 2B4

control signals values

TI-1005, Table 1

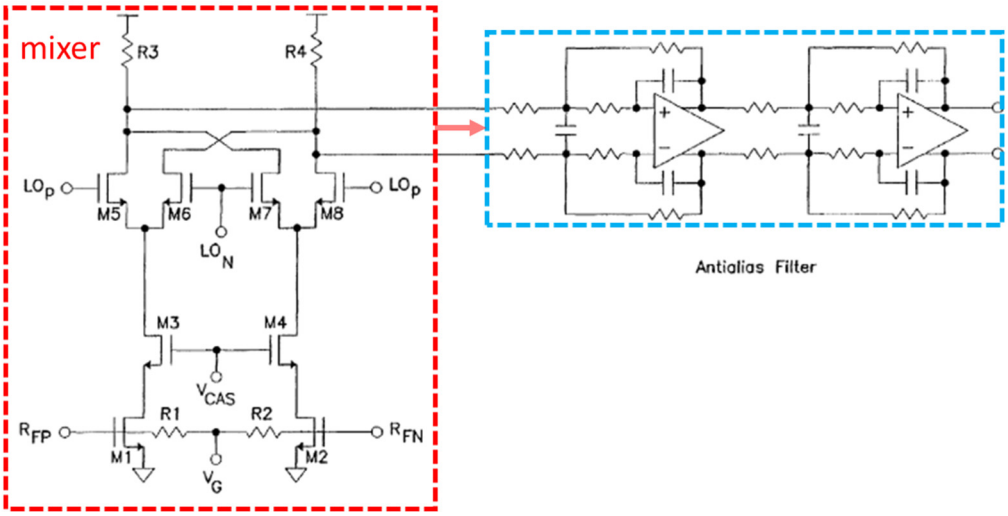
C. U.S. Patent No. 7,065,327 ("Macnally")

108. Macnally is titled *Single-Chip Direct Conversion Transceiver*. TI-1021; TI-1022. Macnally describes "a single-chip CMOS direct conversion transceiver." TI-1021, 1:10-12, 1:44-46 ("A high level of integration is critical in lowering the cost of electronics for communication systems such as cellular phones, cordless phones, and wireless LANs"); TI-1022, 4[9].

109. Macnally shows "[a] diagram of a mixer 142 and an antialiasing filter 144 with a cut-off frequency …," (TI-1021, 7:7-8; TI-1022, 8), as annotated below:

[9] Citations reference PDF pages.

FIG. 3



TI-1021, Fig. 3; TI-1022, Fig. 3

110. Macnally discloses "[t]he output of the mixer [] is fed to a four-pole Butterworth antialiasing filter [] with a cut-off frequency of 2.4MHz." TI-1021, 7:7-16, 7:17-29 ("Two biquad stages form the four-pole Butterworth anti-alias filter"), Fig. 1; TI-1022, 8, Fig. 1.

111. In each of the two biquad stages illustrated above, Macnally shows a fully differential amplifier. Moreover, a POSITA would readily recognize that an antialiasing filter for baseband processing, as used in Macnally, is a low-pass filter. Further, a POSITA would understand Macnally is not limited to using a specific example of two biquad stages and one biquad stage can also be used to achieve the same goal of amplification and low-pass filtering.

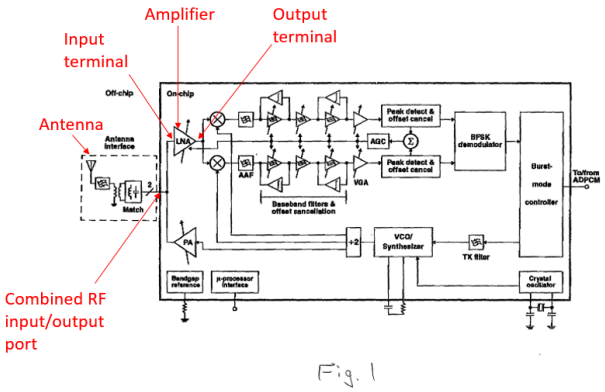
112. I understand Macnally had a provisional application, which I refer to as Macnally-Provisional, filed on September 10, 1998. I note that Macnally and

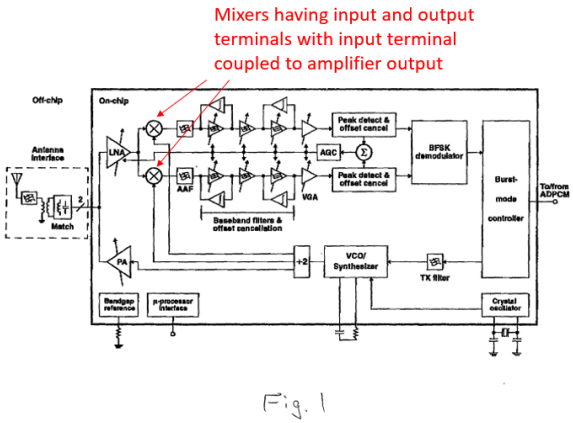
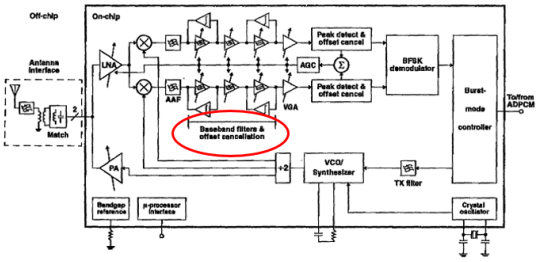
Macnally-Provisional share virtually identical figures and largely similar specifications. In fact, my review indicates Macnally-Provisional only omits: priority paragraph, embodiment paragraphs in Macnally's summary, overview paragraphs of Macnally's detailed description, as well as the abstract and claims of Macnally.

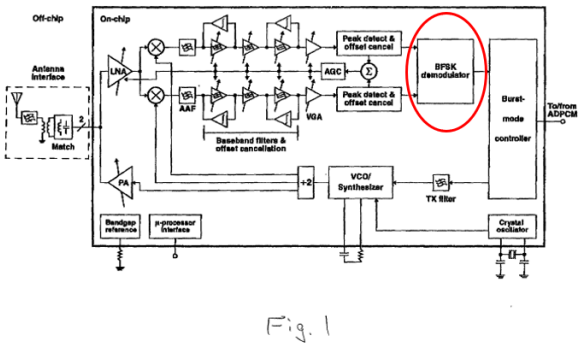
113. My view is that Macnally-Provisional clearly supports at least one claim of Macnally, given their corresponding disclosures. For example, the direct conversion receiver of independent claim 7 (i.e., amplifier, mixer, baseband filter, and demodulator) is disclosed in Macnally-Provisional at Fig. 1 (system showing amplifier (LNA), mixer, baseband filter, and BFSK demodulator), 10 (LNA depicted in Fig, 2), 11 (mixer and baseband filter (i.e., antialias filter) depicted in Fig. 3), 12 (BFSK demodulator). A more detailed table is provided below:

Macnally Claim 7	**Support in Macnally-Provisional**
A single-chip direct conversion receiver, comprising:	TI-1022, 5:15-18 [10] ("a single-chip CMOS direct-conversion transceiver."), 7:10-8:2 (describing the "fully9integrated transceiver" having a transmitter and receiver), 6:4-5, FIG. 1.

[10] Citations reference PDF pages.

an amplifier having an input terminal and an output terminal, the amplifier input terminal interfacing with an external antenna via a combined RF input/output port;	TI-1022, 9:9-13 (The low noise amplifier (LNA) and the power amplifier (PA) designs make it possible to share a common RF port… The transmitter and receiver are attached to the filter/antenna port of a radio transceiver."), 10:10-15 ("the antenna interface requires only one RF combined input/output port"), 10:16-21 (describing the low noise amplifier of FIG. 2 which includes input and output terminals), FIG. 2.  TI-1022, FIG. 1

a mixer having an input and output terminal, the mixer input terminal being coupled to the amplifier output terminal;	 Fig. 1 TI-1022, FIG. 1, 6:7-8, 11:3-9, FIG. 8.
a baseband filter coupled to the mixer, the baseband filter comprising switched capacitor technology; and	 Fig. 1 TI-1022, FIG. 1. 11:8-12:6 (“The output of the mixer is fed to a four-pole Butterworth antialias filter… ***Switched-capacitor I and Q baseband filters*** sample the output of the antialias filter.”), 5:11-13, 13:22-14:4.

a demodulator coupled to the baseband filter.	 Fig. 1 TI-1022, FIG. 1, 12:1-13 ("The offset is then subtracted from the baseband filter output, and the resulting I and Q signals are fed to a BFSK demodulator"), 13:22-14:4, 5:11-13.

114. In my declaration, I provide parallel citations to Macnally (TI-1021) and Macnally-Provisional (TI-1022).

D. "Razavi"

115. Razavi is an IEEE conference paper published in 1997 and is titled *A 900-MHz CMOS Direct Conversion Receiver*. TI-1017.

116. Razavi describes "the design of a single-chip 900-MHz CMOS direct conversion receiver (DCR) [including, among others,] quadrature mixers [blue], simple low-pass filters (LPFs), [and] baseband amplifiers, A1," as annotated in Fig. 1 below.

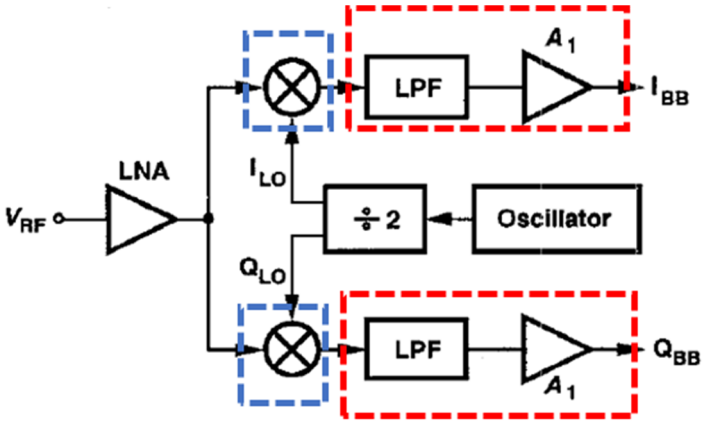
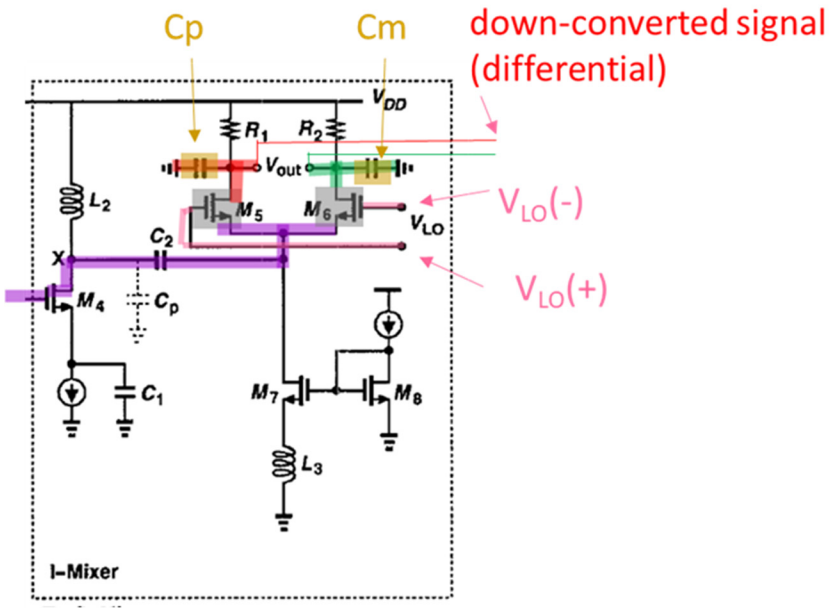


Fig. 1. Receiver architecture.

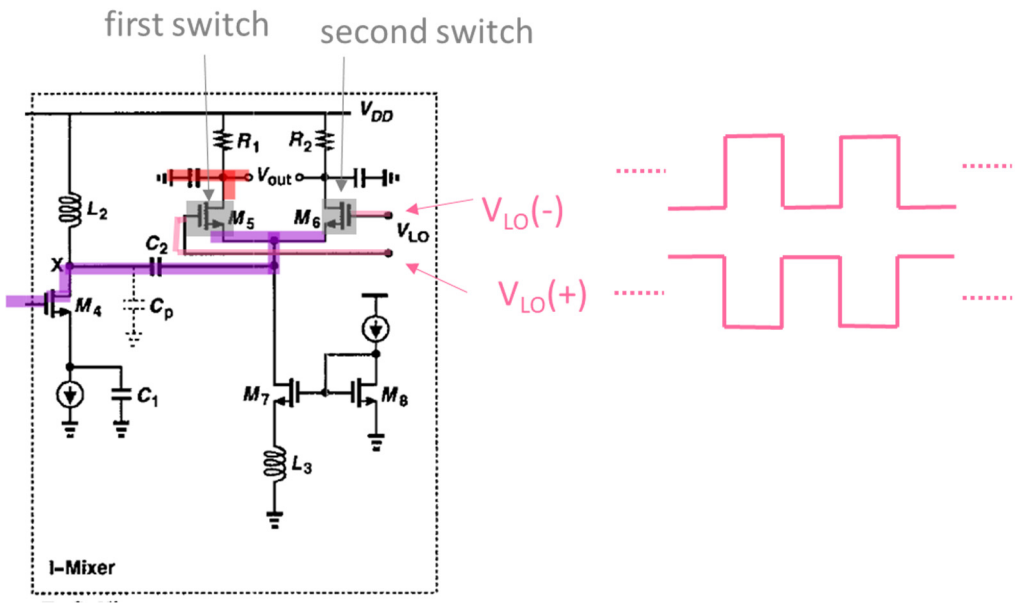
TI-1017, 114

117. Razavi's mixer "employs a single-balanced topology [including, among others,] a switching pair M_5-M_6 [gray]," as annotated in Fig. 2 (cropped to show mixer) below.



TI-1017, 114

118. In the illustrated in-phase mixer, the switching pair M_5 and M_6 are alternately turned on or off under the control of V_{LO}, which has an upper component ($V_{LO}(-)$) and a lower component ($V_{LO}(+)$) oscillating in complementary manner relative to each other. I provide a diagram below illustrating square waveforms of complementary V_{LO} components operating on the switching pair).



119. Each time one switch of the pair (e.g., first switch M_5) is turned on, the transistor switch is CLOSED and the drain terminal is conducting so that charge is accumulated on a corresponding capacitor in the presence of resistor R_1. This on-duration corresponds to the period where $V_{LO}(+)$ is high. In the meantime, the other switch (e.g., second switch M_6) is turned off because $V_{LO}(-)$ is low. When first switch (M_5) is turned off, a portion of the accumulated charge is discharged through resistor R_2. During this period first switch (M_5) is off, $V_{LO}(-)$ is high and second

switch (M_6) is turned on so that charge is accumulated on a corresponding capacitor in the presence of resistor R_2. A portion of the accumulated charge is similarly discharged through R_2 when second switch (M_6) is turned off. The cycle then repeats.

120. Significantly, the above annotation shows in-phase (I) mixer with symmetric pairs of switching transistors (M_5 and M_6), capacitors, and resistors (R_1 and R_2), Razavi also labels the quadrature (Q) mixer. TI-1017, 114, Fig. 2. A POSITA would understand both mixers are similarly constructed. The I-mixer and the Q-mixer respectively output an in-phase down-converted signal and a quadrature down-converted signal, both in differential format. *Id.*, Fig. 1. Razavi further describes design options for further processing of the down-converted signal using baseband amplifier and low-pass filter (red in above-annotated Fig. 1), with preliminary measured performance of the receiver summarized at Table 1. TI-1017, 113-114, Figs. 4-5 (design options).

E. "Cahn"

121. Cahn is an IEEE/IRE journal paper published in 1960 and is titled *Combined Digital Phase and Amplitude Modulation Communication Systems*.

122. Cahn describes modulation techniques including amplitude modulation, phase modulation, and combined amplitude and phase modulation. TI-1007. After noting that "the use of multiple amplitude level to transmit digital

information … is well-known under the name quantized pulse-amplitude modulation," and that "the possibility of employing multiple phase positions for the same purpose was [recently] explored," Cahn describes "[a] combination of digital-amplitude and digital-phase modulation." *Id.*, 150-51. Cahn is widely known as the seminal paper on modulation techniques developed in the 1960s and remain in active use today.

XI. OBVIOUSNESS ANALYSIS FOR THE CHALLENGED CLAIMS

123. In this section, I provide an analysis of how the prior art renders obvious claims 1-5, 5-8, 8-9, 11-19, 20-23, 26-27, and 29-36 of the '528 Patent. I have organized my analysis into the following grounds:

Grounds	Claims	Statutory Basis	Prior Art
1A	1, 5, 8-9, 11-19, 23, 26-27, 29-36	§103	Tayloe, TI datasheet, and Macnally
1B	2-4, 20-22	§103	Tayloe, TI datasheet, Macnally, and Cahn
2A	1, 5, 8-9, 11-19, 23, 26-27, 29-36	§103	Razavi, and Macnally
2B	2-4, 20-22	§103	Razavi, Macnally, and Cahn

124. For each ground, I address motivation to combine and reasonable expectation of success, and then analyze the teachings of the prior art on an element-by-element basis.

A. Ground 1A: Tayloe, TI datasheet, and Macnally Render Obvious Claims 1, 5, 8-9, 11-19, 23, 26-27, 29-36

125. For the reasons set forth in detail below, and based on my review of the '528 patent, file history, and the prior art references cited in my analysis, a POSITA would have readily understood that the combined teachings of Tayloe, TI datasheet, and Macnally provide all elements of claims 1, 5, 8-9, 11-14, 15-19, 23, 26-27, 29-36.

1. Predictable Combination for Tayloe, TI-Datasheet, and Macnally

126. Based upon my review of the references and my knowledge and experience in this field, it is clear that a POSITA would have been motivated to combine the teachings of Tayloe, TI Datasheet, and Macnally.

127. As I explain above under §X.A, Tayloe discloses a direct conversion receiver using a commutating switch to "sample an RF waveform four times per period at the RF frequency" in which "[t]he samples are integrated over time to produce an average voltage at 0 degrees, 90 degrees, 180 degrees and 270 degrees" across the 360-degree full cycle. TI-1004, Abstract, *see also* 2:13-67 (for each of the four sampling events, charge builds up on a respective one of capacitors 72, 74, 76, and 78), Figs. 3 (diagram example), 4 (waveform example). Tayloe also discloses "an alternate embodiment in which each integrating capacitor has its own resistor." TI-1004, 4:48-57 (each resistor/capacitor pair in Figure 6 form an

integrator), Fig. 6. Tayloe further discloses that the switch 38 can be implemented using an analog multiplexer/demultiplexer, such as the Texas Instruments ("TI") SN74CBT3253D multiplexer/demultiplexer. TI-1004, 5:33-37, 5:1-16, Fig. 7 (multiplexer/demultiplexer example).

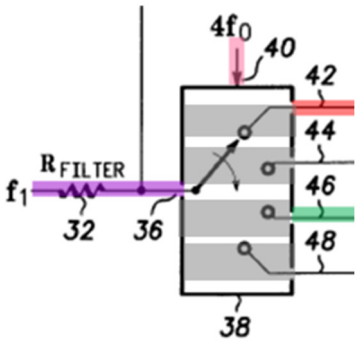
128. As I have explained under §X.B, TI Datasheet describes SN74CBT3253, a "dual 1-of-4 high-speed [transistor-transistor logic]-compatible [field-effect transistor] multiplexer/demultiplexer." TI-1005, 1. TI Datasheet states "[t]he low on-state resistance of the switch allows connections to be made with minimal propagation delay." *Id*.

129. As I have explained under §X.C, Macnally discloses examples of using antialiasing filters in an TI-1021, Fig. 3, 1:44-46, 7:7-29; TI-1022, Fig. 3, pp. 6-8.

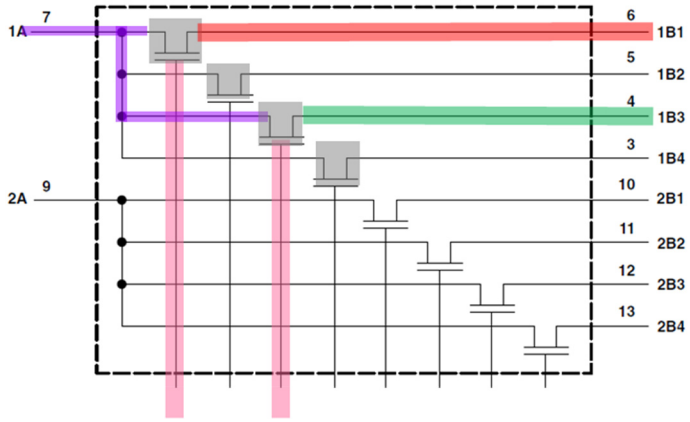
130. A POSITA would have found it obvious to combine relevant teachings from Tayloe, TI Datasheet, and Macnally.

131. ***First***, as a preliminary matter, Tayloe expressly teaches four switches in a "direct conversion receiver 30 (FIG. 3) utilizing an analog multiplexer … shown in FIG. 7" and specifically states "[t]he analog multiplexer is a Texas Instruments SN74BCT3253D." TI-1004, 5:33-37. The characteristics described in the TI Datasheet are expressly included in Tayloe's implementation, and as evidenced by at least Tayloe's reference to the TI Datasheet, POSITA knew the characteristics of the referenced TI multiplexer.

132. Additionally, a POSITA would have also found it obvious to combine Tayloe and the TI Datasheet, using any four of the multiplexer switches (gray) from the multiplexer to implement Tayloe's switch box 38 of Figure 3, such as annotated below.



TI-1004, Fig 3 (switch 38)



TI-1005, 1 (multiplexer/demultipler)

133. Because Tayloe expressly discloses the SN74CBT3253 multiplexer/demultiplexer and a datasheet is a well-known resource for learning detailed information of the multiplexer/demultiplexer, a POSITA would have been motivated to consult the TI Datasheet for a more complete understanding of Tayloe's express teachings of the SN74CBT3253 multiplexer, the only matching multiplexer available at the time, as evidenced by the declaration by Maureen Honeycutt, the TI Senior Paralegal.

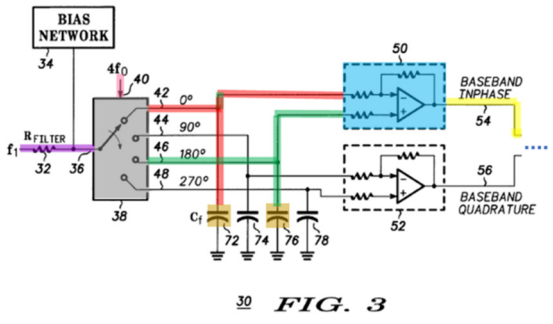
134. A POSITA would have also been motivated to use the multiplexer of the TI Datasheet in Tayloe's implementation of switch box 38 at least because

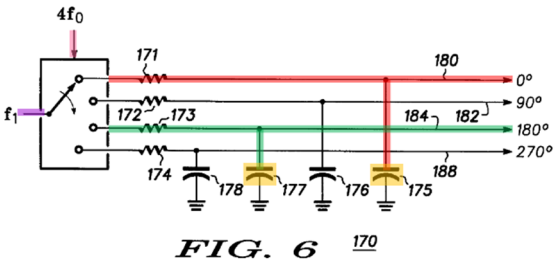
Tayloe expressly teaches using a multiplexer, and the multiplexer of TI's datasheet is a suitable multiplexer because Tayloe demonstrated experiment results using it.

135. When viewing the detailed diagram of the SN74CBT3253 multiplexer, a POSITA would have been motivated to apply four of the multiplexer switches (gray squares (TI-1005, 1)) because the architecture of one multiplexer switch on the analog multiplexer is analogous to one of the four switching paths when using Tayloe's commutating switch 38 (gray stripes (TI-1004, Fig. 3)). Thus, a POSITA would have been inspired to implement the multiplexer switches from TI Datasheet in an analogous manner by "simple substitution of one known element for another."

136. A POSITA would have a reasonable expectation of success at combining Tayloe with TI Datasheet because the combination would have yielded only predictable results (e.g., "low on-state resistance of the switch [which] allows connections to be made with minimal propagation delay"). TI-1005, 1.

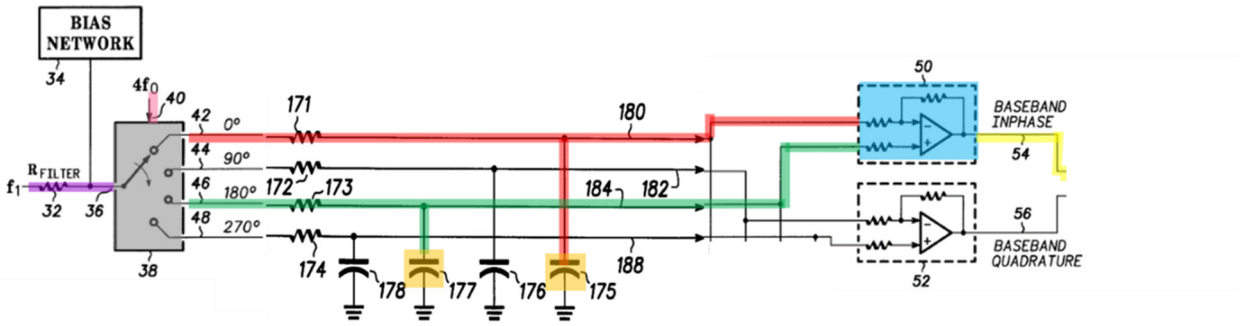
137. As a ***second*** reason, a POSITA would have found it obvious to apply the separate integrator example from Fig. 6 of Tayloe to Tayloe's receiver depicted in Fig. 3, as annotated below.



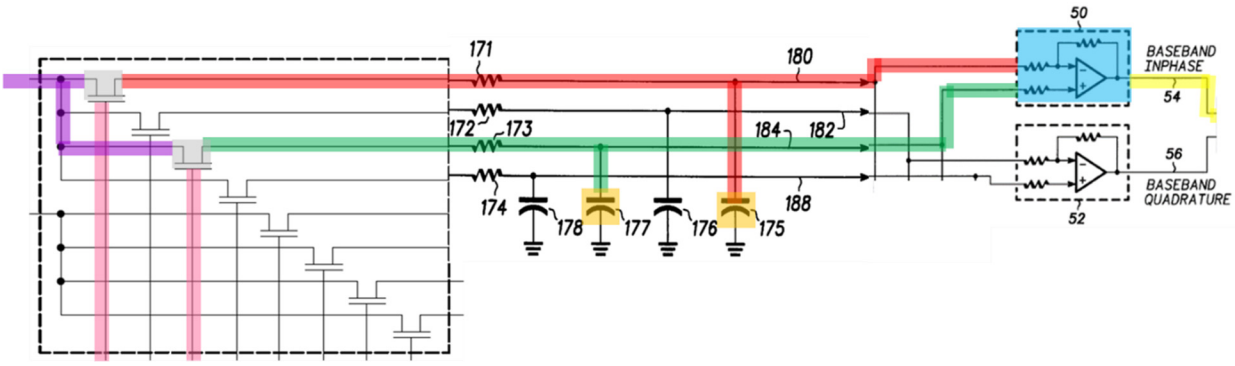


TI-1004, Fig. 3

TI-1004, Fig. 6



Combined Teachings of Tayloe



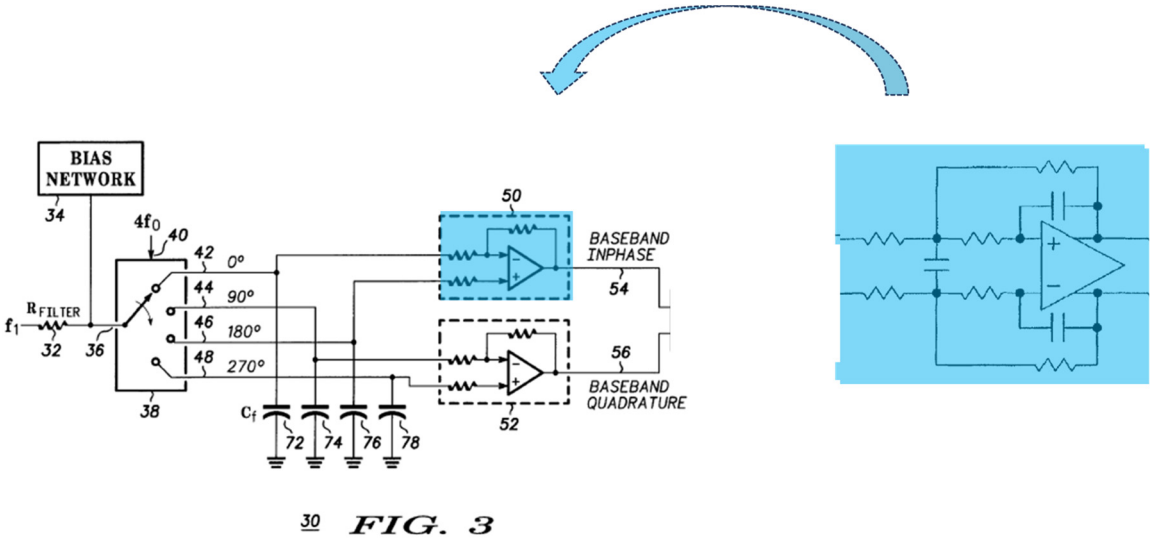
Combination System (using switch of TI-1005)

138. A POSITA would have been motivated to combine Figure 6 with Figure 3 of Tayloe at least because Tayloe specifically describes Figure 6 as "an alternate embodiment in which each integrating capacitor has its own resistor." TI-1004,

4:46-49. As "an alternate embodiment" relative to the embodiment where capacitors 72-78 share a resistor 32, i.e., Figure 3, a POSITA would have understood Figure 6 to be used in lieu of the comparable circuit portion of Figure 3. A POSITA would have found further motivation in that Figure 6 performs a similar function to the comparable circuit portion of Figure 3, and alone, does not produce the signal of interest 62 based on RF input signal f_1. Thus, a POSITA, seeking to generate signal of interest 62 with the circuit portion of Figure 6 would have found it obvious to replace the existing arrangement of capacitors in Figure 3 using the alternate arrangement where "each integrating capacitor has its own resistor," as depicted in Figure 6 of Tayloe.

139. A POSITA would have a reasonable expectation of success because the replacement is no more than "a simple substitution of one known element for another" to obtain predictable results (i.e., "each integrating capacitor has its own resister"). For example, the combination can have separate integrators on each of the four signal paths where the integrators have consistent characteristics such as discharging times.

140. As a ***third*** reason, a POSITA would have found it obvious to implement each of Tayloe's differential amplifier circuits (light blue) (TI-1004, Fig. 3) as a fully differential operational amplifier configuration (light blue), as taught in Macnally (TI-1021/TI-1022, Fig. 3).



TI-1004, Fig. 3 (left) TI-1021/TI-1022, Fig. 3 (right)

141. A POSITA would have been motivated to adapt Tayloe's system as a single-chip (i.e., integrated circuit known as IC) for the size, packaging advantages, and low unit cost of an IC and to meet market demand. TI-1021, 5:5-7; TI-1022, 5 ("high level of integration is critical in lowering the cost of electronics for communication systems such as cellular phones, cordless phones, and wireless LANs")). In doing so, a POSITA would have been in-spired by several known advantages of using fully differential amplifiers and Macnally's topology for baseband processing on an IC. *First*, fully differential amplifiers operate on complementary signal components such that interference which equally corrupts both complementary signal components can be can-celled by taking the difference between the two complementary signal components. This known feature can

minimize even order harmonic distortion, thus improving the linearity of amplifier output. Background explanation of harmonic distortion can be found at, for example, TI-1027. *Second*, each fully differential amplifier is laid out symmetrically on an integrated circuit (IC) to provide "a fully differential analog signal path [that] minimizes supply and substrate noise coupling [e.g., interference coupling from the substrate, power supply lines, and ground lines]." TI-1021, 6:64-65; TI-1022, 9; TI-1027, 1389 ("To minimize distortion due to second-order harmonics and avoid substrate coupling, the amplifiers were built fully differential."). *Third*, among available design options for fully differential amplifiers, Macnally's configuration employs the Rauch biquad topology known for reducing the number of operational amplifiers on an IC, thereby "lowering power and reducing the noise and distortion contributors." TI-1027, 1388, Fig. 12 (Rauch biquad topology as used in Macnally and Macnally-Provisional).

142. The differential output of Macnally's configuration is characteristic of on-chip baseband signals for subsequent on-chip processing, also in differential format. In other words, a POSITA would understand the subsequent on-chip components are likewise differential. A POSITA would likewise understand standard practice to implement Tayloe's circuit on an IC using differential counterparts. For example, Tayloe's phase shifter had well-known counterparts for IC designs.

143. Indeed, the implementation would have been a simple substitution of one known element (fully differential amplifier circuit of Macnally performing both amplification and low-pass filtering at baseband) for another (summing amplifier circuit of Tayloe) to obtain predictable results (e.g., improved linearity and reduced power consumption for on-chip performance), and hence would have had a reasonable expectation of success. Moreover, a POSITA would have recognized that the lowpass filtering function of the Macnally differential amplifier is beneficial in the Tayloe's circuits as lowpass filtering of the baseband signals in direct conversion receives is beneficial as explained in Section VI. Indeed, success stories for building integrated direct down-conversion receivers had been reported, for example, in TI-1021/TI-1022 (Fig. 1), by Macnally. I have also conducted an analysis of a representative Macnally circuit example in Section VI and determined the input resistance to be 1 kilo ohm. §VI.D.

2. Claim 1

144. Based on my review of Tayloe, TI Datasheet, and Macnally, and my knowledge and experience in the field, a POSITA would have found it obvious that Macnally's suggestions, predictably combined with the teachings of Tayloe and the TI Datasheet, provide all elements of claim 1. I explain in detail below how each limitation of claim 1 is disclosed by the combination of Tayloe, TI Datasheet and Macnally.

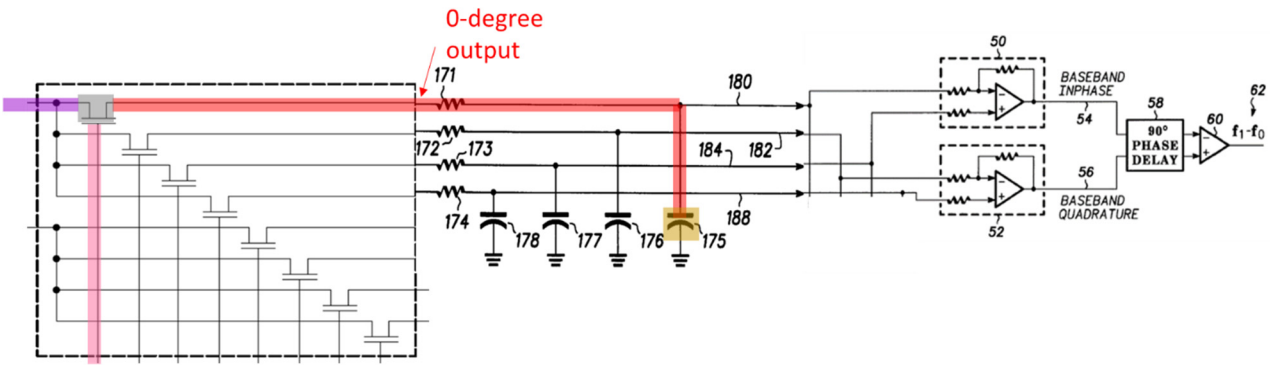
a) Element 1(a): A system for frequency down-converting a modulated carrier signal to a base-band signal, comprising:

145. The combination provides the recited system of element 1(a). The combination system (Tayloe's system using a multiplexor/demultiplexer design taught by TI-Datasheet) is a system for frequency down-converting a modulated carrier signal to a baseband signal. See e.g., TI-1004, FIG. 3 (sys-tem that down-converts RF input signal f1 from input 36 to generate signal of interest 62 that combines baseband in-phase signal 54 and baseband quadra-ture signal 56), 4-7 (various aspects of the system), 1:5-6, 1:10-21 ("Ddirect conversion receivers … convert signals of interest directly to basebandfor con-verting a signal to baseband"), 2:6-8, 2:13-26, 2:46-55, 2:56-67, 3:58-4:45 (de-scribing down-converting from frequency f_1 to Δf), 6:3-4, Abstract; §X.A.

146. In the combination, each of the capacitor arrangements depicted in Fig. 3 (capacitors 72 to 78 sharing resister 32) and Fig. 6 (capacitors 175 to 178 each has a pairing resister) separately satisfy this element.

b) Element1(b): a first switch coupled to a first control signal which comprises a sampling aperture with a specified frequency, wherein the first switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal as an output of said first switch during the sampling aperture of said first switch;

147. The combination system provides 1[b]. As explained *supra* §§X, XI-A.1, and annotated below, the combination system includes a ***first switch*** (gray) coupled to a ***first control signal*** (pink). TI-1004, 2:5-26 ("… the input signal [f_1 (purple)] is received by commutating switch 38 at input 36 [and] input 36 is switched [by a control signal (pink)] to each of the four outputs substantially once during each period of the input signal f_1"), Figs. 3 (system diagram), 6 (separate integrator). In the combination system, commutating switch 38 is implemented as an analog multiplexor/demultiplexer 202, one example of which is the "Texas Instruments SN74[CBT]3253D" multiplexer/demultiplexer. TI-1004, 5:33-37, Fig. 7 (depicting analog multiplexor/demultiplexer 202 controlled by control signal 214); TI-1005, 2 (logic diagram of the TI SN74CBT3253D multiplexer/demultiplexer incorporated in the annotation below):



Combination System (annotated using multiplexor/demultiplexer of TI-1005

148. Although the integrator of FIG. 6 is depicted, the FIG. 3 embodiment also provides the relevant elements of claim 1.

149. The first control signal (pink) has a sampling aperture (e.g., up to 90 degree at the frequency of the input signal f1) with a specified frequency (e.g., the rate of toggling the first switch (gray)). TI-1004, 2:18-20 ("The rate at which commutating switch 38 operates is controlled by a signal present at control in-put."), 2:27-32 ("… [switch] remains closed at each of the four outputs for substantially 90 degrees at the frequency of the input signal," or "[switch] re-mains closed at each of the four outputs for less than 90 degrees"), 5:5-12 ("Analog multiplexer 202 is controlled by control signals 214 which are generated by digital counter 220. Digital counter 220 runs at a clock frequency of substantially 4f1 [such that] input signal f1 is connected to each of the four out-puts of analog multiplexer 202 for substantially 90 degrees of the input signal.")

150. The first switch (gray) is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal (i.e., RF input signal f1 (purple)) as an output (i.e., the 0-degree output) of said first switch during the sampling aperture (e.g., up to 90 degrees at the frequency of the in-put signal f1) of said first switch. TI-1004, 2:27-32 ("… commutating switch 38 [implemented as the TI multiplexer/demultiplexer] remains closed at each of the four outputs for substantially 90 degrees at the frequency of the input sig-nal"), 2:33-45 ("During the time that commutating switch 38 [implemented as the TI multiplexer/demultiplexer having the first switch] connects input 36 to output 42 [the 0-degree output], charge builds up on capacitor 72 [correspond-ing to capacitor 175 in Fig. 6]").

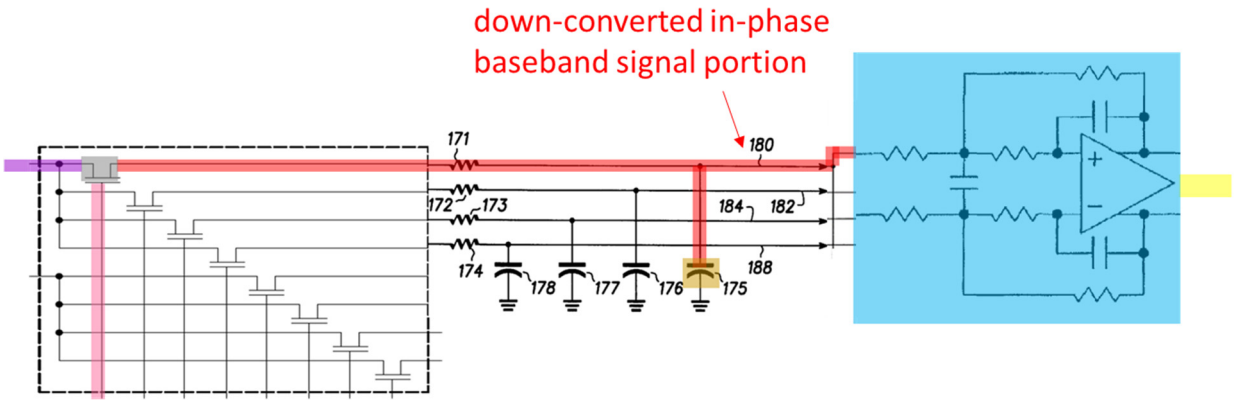
151. Tayloe makes clear the portion of energy is ***distinguishable from noise*** when "[o]utput 42 [the 0 degree output] represents the average value of the input signal during the first quarter wave of the period." TI-1004, 2:46-55, 5:1-16 ("0 degree output [is] used to generate baseband in-phase [] signal[]"), Figs. 3 (system diagram), 4 (waveform example where "[p]oint 105 represents the voltage to which capacitor 72 (FIG. 3) charges," 3:40-48)), 6 (separate integrator), 7 (analog multiplexor/demultiplexer). The fact that the capacitor is charged by the output signal, which is the average value of the input signal during the first quarter wave, indicates that the portion of energy is distinguishable from noise. Furthermore, Tayloe describes "information bearing signals…super imposed on f_1" converted to

a baseband "signal of interest." TI-1004, 3:62-4:8, 6:10-14. The energy therefore includes the "signal of interest" and a POSITA would have recognized that to send a usable signal, the signal to noise ratio would be implemented to sufficiently convey a meaningful "signal of interest" to convey the "information."

152. Moreover, if a system operates to down-convert an electromagnetic signal, as described by Tayloe, (TI-1004, 5:30-60 (experiment results for "proto-typed direct conversion receiver")), then sufficient energy distinguishable from noise is transferred by virtue of the down-conversion process.

c) Element1(c): a first energy storage element that stores the transferred energy from the modu-lated carrier signal and outputs a down-converted in-phase baseband signal portion of said modulated carrier signal;

153. The combination system provides 1[c]. As explained *supra* §§X.A, XI.A, and annotated below, the combination system includes ***a first energy storage element*** (e.g., capacitor 175 (brown), or capacitor 72 of Fig. 3) that ***stores*** the transferred energy from the modulated carrier signal (purple) and ***outputs a down-converted in-phase baseband signal portion*** (red portion feeding into differential amplifier 50 implemented using Macnally's circuit) of said modulated carrier signal (purple).



Combination System (using switch of TI-1005 and circuit of TI-1021/TI-1022)

154. In the combination annotated above, "commutating switch 38 [implemented as the TI multiplexer/demultiplexer] remains closed at each of the four outputs for substantially 90 degrees at the frequency of the input signal." TI-1004, 2:27-32, 2:13-18. "During the time that commutating switch 38 [implemented as the TI multiplexer/demultiplexer] connects input 36 [receiving input signal (purple)] to output 42 [0-degree output], charge builds up on capacitor 72 [corresponding to capacitor 175 in Fig. 6]." *Id.*, 2:33-45, 2:46-55 ("Output 42 [0-degree output corresponding to output 180 in Fig. 6] represents the average value of the input signal during the first quarter wave of the period, and is termed the 0 degree output …."), 2:56-59 ("…producing baseband in-phase signal"), 4:49-51 ("FIG. 6 shows … 0 degree output 180 has a voltage controlled by the combination of capacitor 175 and resistor 171 …."). Figs. 3 (system diagram) 4 (waveform example), 6 (separate integrator). In fact, the average value results in down-conversion while the

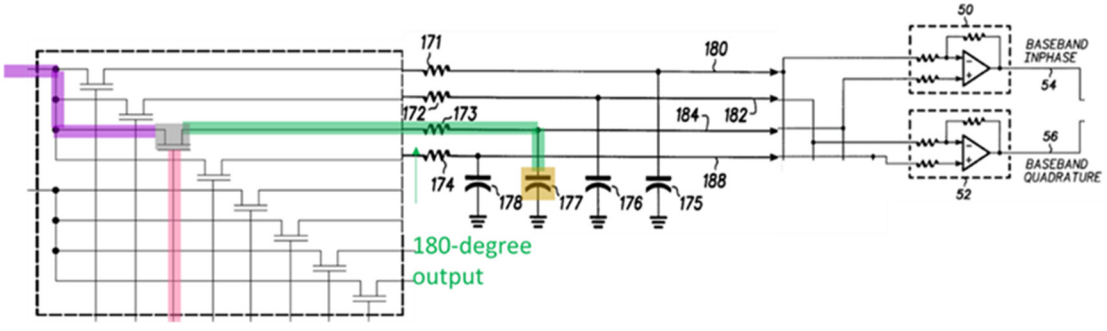
capacitor-resister combination operates to approximate an average operation. A POSTIA would have recognized that a 0-degree output provides an in-phase signal.

155. Referring to Fig. 7 showing a multiplexer example in an analogous configuration, Tayloe specifically describes that "0 degree output [is] used to generate baseband in-phase … signal[]," (TI-1004, 5:1-16), consistent with descriptions from the '528 Patent. TI-1001, Fig. 197 (first processing module 19702), 176:61-177:15 ("a switch … opens and closes as a function of I control signal [to generate] a down-converted signal … a first capacitor stor[es] I output signal").

156. Consistent with my opinion regarding proposed claim construction *supra* §IV.B, Tayloe's capacitor 175 (brown) (or capacitor 72 of Fig. 3) "***stores non-negligible amounts of energy from an input EM signal,***" i.e., the RF input signal f_1. The differential amplifier circuit of Macnally provides low impedance load typically in the kilo ohm range, (*supra* §VI.C), which "goes to the heart of what makes an element, a 'storage' element," as alleged by ParkerVision. *See e.g.*, IPR2020-01265, Paper 26 (PO Sur-reply) at 13; Paper 18 (POR) at 46-50.

d) Element 1(d): a second switch coupled to a second control signal which comprises a sampling aperture with a specified frequency, wherein the second switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal as an output of said second switch during the sampling aperture of the second control signal;

157. As explained *supra* §§III.A.1-4 and annotated below (similar to [1b]), the combination system includes ***a second switch*** (gray) coupled to ***a second control signal*** (pink) which comprises ***a sampling aperture*** (e.g., up to 90 degrees at the frequency of the input signal f_I) ***with a specified frequency*** (e.g., the rate of toggling the second switch (gray)). TI-1004, 2:5-26 ("… the input signal [f_I (purple)] is received by commutating switch 38 [implemented as the TI multiplexer/demultiplexer] at input 36 [and] input 36 is switched [by a control signal (pink)] to each of the four outputs substantially once during each period of the input signal f_I"), 2:27-32 (switch "remains closed at each of the four outputs for substantially 90 degrees at the frequency of the input signal" or "for less than 90 degrees"), 5:1-16; Figs. 3, 6-7; TI-1005, 2; §XI.A.2 (element 1[b]).



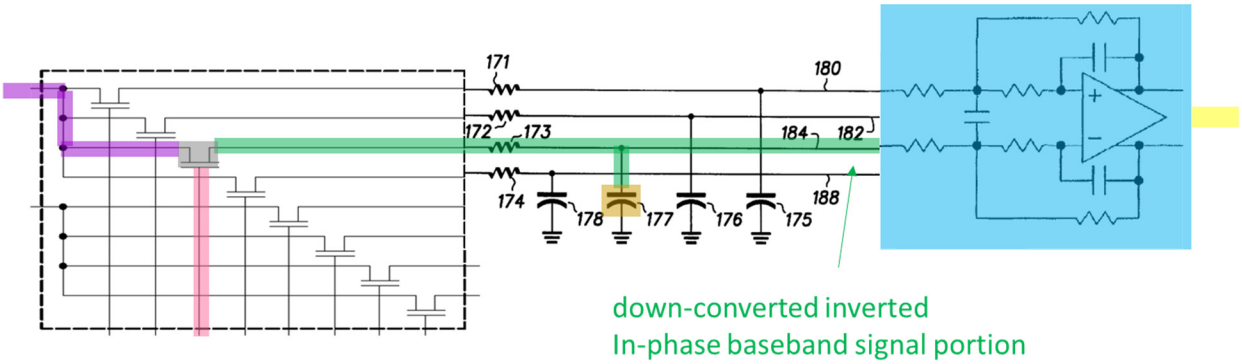
Combination System (using switch of TI-1005)

158. The second switch (gray) is on and ***a portion of energy*** that is distinguishable from noise is transferred ***from the modulated carrier signal*** (i.e., RF input signal f_1 (purple)) as an output (i.e., the 180-degree output) of said second switch ***during the sampling aperture*** (e.g., up to 90 degrees at the frequency of the input signal f_1) of the second control signal. TI-1004, 2:27-32 ("commutating switch 38 [implemented as the TI multiplexer/demultiplexer] remains closed at each of the four outputs for substantially 90 degrees at the frequency of the input signal"), 2:33-45 ("… when commutating switch 38 [implemented as the TI multiplexer/demultiplexer] connects input 36 to output[s] 46 [the 180-degree output corresponding to output 184 in the combination system]," charge builds up on capacitor 76 (corresponding to capacitor 177 in the combination system)), 2:46-55 ("… Output 46 represents the average value of the input signal during the third quarter wave of the period, and is termed the 180 degree output …."), 4:53-55 (describing "180 degree output 184"), 5:1-16 (180-degree output "can be utilized as embodied in FIG. 3 to achieve greater gain"), Figs. 3-4, 6-7.

159. Tayloe describes "information bearing signals…super imposed on f1" converted to a baseband "signal of interest." TI-1004, 3:62-4:8, 6:10-14. The energy therefore includes the "signal of interest" and a POSITA would have recognized that to send a usable signal, the signal to noise ratio would be implemented to sufficiently convey a meaningful "signal of interest" to convey the "information."

e) Element1 (e): a second energy storage element that stores the transferred energy from the modulated carrier signal and outputs a down-converted inverted in-phase baseband signal portion of said modulated carrier signal;

160. As explained *supra* §§XI.A,1 and annotated below, the combination system includes ***a second energy storage element*** (e.g., capacitor 177 (brown), or capacitor 76 of Fig. 3) that ***stores*** the transferred energy from the modulated carrier signal (purple) and ***outputs a down-converted in-phase inverted baseband signal portion*** (green portion feeding into Macnally's circuit (light blue)) of said modulated carrier signal (purple).



Combination System (using switch of TI-1005 and circuit of TI-1021/TI-1022)

161. In the combination system annotated above, "commutating switch 38 [implemented as the TI multiplexer/demultiplexer] remains closed at each of the four outputs for substantially 90 degrees at the frequency of the input signal." TI-1004, 2:27-32, 2:13-18. Tayloe explains that "when commutating switch 38 [implemented as the TI multiplexer/demultiplexer] connects input 36 to output[] 46 [the 180-

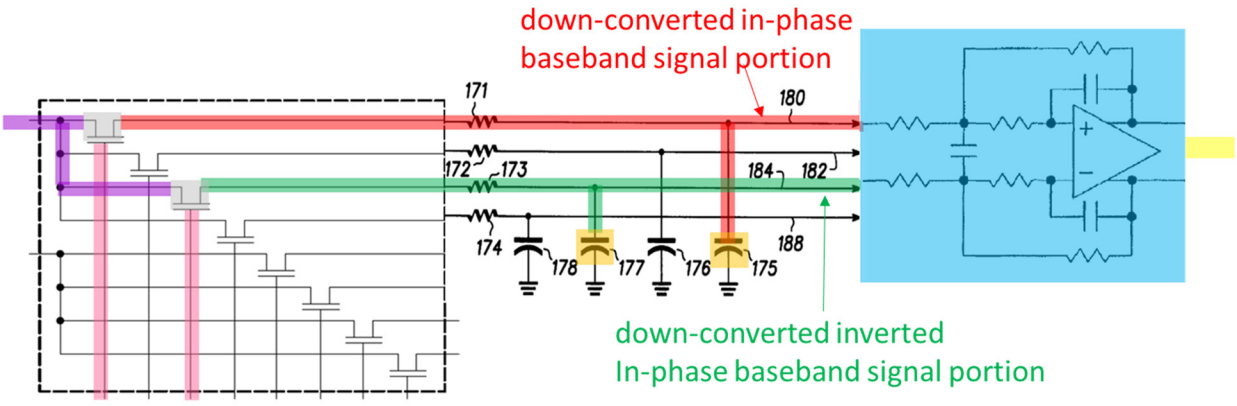
degree output corresponding to output 184 in the combination system]," charge builds up on capacitor 76 (corresponding to capacitor 177 in the combination system)). *Id.* 2:33-45, 2:46-55 ("… Output 46 represents the average value of the input signal during the third quarter wave of the period, and is termed the 180 degree output …."), 4:49-51 ("FIG. 6 shows … 180 degree output 184 has a voltage controlled by the combination of capacitor and resistor 173 …."), Figs. 3-4, 6-7. A POSTIA would have recognized that the 180-degree output is an inverted signal because it is 180 degree out of phase with the 0-degree output.

162. Tayloe explains that the 180-degree output "can be utilized as embodied in FIG. 3 to achieve greater gain" because the 180-degree output is an inverted version of the 0-degree output, and hence the inverted in-phase baseband sig-nal, as described by the '528 Patent. TI-1001, Fig. 197 (second processing module 19706), 177:31-54 ("a switch … opens and closes as a function of in-verted I control signal … As a result of the opening and closing of this switch … a down-converted signal, referred to as the inverted I output signal, re-sults"). In fact, the 180-degree output is generated when the commutating switch is turned on at an inverted phase during the carrier period when compared to the 0-degree output. Further, the form of differential amplifiers in Tayloe and Macnally both require the two inputs of the amplifier to be inverted versions of each other.

163. Consistent with my earlier discussed claim construction proposal *supra* §IX and similar to 1[c], Tayloe's capacitor 177 (brown) (or capacitor 74 of Fig. 3) "***stores non-negligible amounts of energy from an input EM signal,***" i.e., the RF input signal V_{RF}. I have demonstrated low input impedance of Macnally's circuit, which provides a low impedance load to the capacitor of Tayloe. This means Tayloe's capacitor would meet ParkerVision's requirement of low impedance load.

> *f) Element1 (f): wherein the portions of transferred energy from each of the first and second switch are integrated over time to accumulate said portions of transferred energy from which said down-converted in-phase baseband signal portion and said down-converted inverted in-phase baseband signal portion are derived; and;*

164. As explained *supra* §§III.A.1-4 and annotated below, in the combination system, ***the portions of transferred energy*** from each of the first and second switch ***are integrated*** over time to accumulate said portions of transferred energy ***from which said down-converted in-phase baseband signal portion*** (red portion feeding into Macnally's circuit) ***and said down-converted inverted in-phase baseband signal portion*** (green portion feeding into Macnally's circuit) ***are derived***.



Combination System (using switch of TI-1005 and circuit of TI-1021/TI-1022)

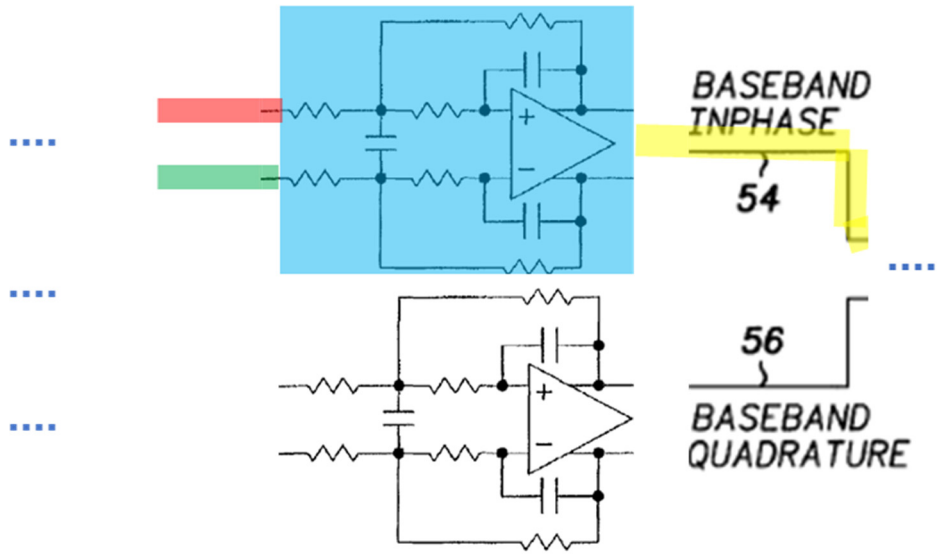
165. Tayloe describes that each capacitor 175, 176, 177, and 178 (and the corresponding capacitors in FIG. 3) are "integrating capacitors" with each having "its own resistor … 0 degree output 180 has a voltage controlled by the combination of capacitor 175 and resistor 171 [forming a first integrator for the 0-degree output] … 180 degree output 184 has a voltage controlled by the combination of capacitor 177 and resistor 173 [forming a separate integrator for the 180-degree output] … each [integrator] preferably integrates for substantially 90 degrees of the input signal." TI-1004, 3:54-4:4, 4:46-67, Abstract ("A product detector for converting a signal to baseband includes a commutating switch which serves to sample an RF waveform four times per period at the RF frequency. ***The samples are integrated over time*** to produce an average voltage at 0 degrees, 90 degrees, 180 degrees and 270 degrees. The average voltage at 0 degrees is the baseband in-phase signal....

Alternatively, …the 0 degree average can be differentially summed with the 180 degree average to form the baseband in-phase signal....").

166. Moreover, Tayloe discloses similar integrator operation in the example of Figure 3 using capacitors 72 and 76 respectively for the 0-degree and 180-degree outputs. TI-1004, 2:33-55 ("Each of the capacitors functions as a separate integrator, each integrating a separate quarter wave of the input signal."), Figs. 3-4, 6-7.

g) Element1 (g): a first differential amplifier circuit that combines said down-converted in-phase baseband signal portion with said down-converted inverted in-phase baseband signal portion and outputs a first channel down-converted differential in-phase baseband signal.

167. As explained *supra* §§III.A.1-4 and annotated below, the combination system includes ***a first differential amplifier circuit*** (light blue) that ***combines said down-converted in-phase baseband signal portion*** (red portion feeding into Macnally's circuit) ***with said down-converted inverted in-phase baseband signal portion*** (green portion feeding into Macnally's circuit) ***and outputs a first channel down-converted differential in-phase baseband signal*** (yellow).



Combined System (zoomed portions using circuit of TI-1021/TI-1022)

168. "Summing amplifier 50 [replaced using a fully differential amplifier circuit of Macnally] differentially sums the 0 degree output 42 and the 180 de-gree output 46, thereby producing [first channel down-converted differential] baseband in-phase signal [as a differential output having two complementary components]." TI-1004, 2:56-67 , Abstract, Fig. 3; TI-1021, 5:64-67 ("fully-differential analog signal path")/TI-1022, 9, Fig. 3.

169. As I explain supra §VI.C, a fully differential amplifier generates differential output signal having two complementary components, each combining the two complementary components of the differential input signal. A POSITA would have understood that a single-ended amplifier, depicted in summing amplifier

50 of Tayloe, was usually used to generate the output signal off-chip, and would have found it obvious to use a singled-ended amplifier, as needed.

170. Accordingly, my opinion is that the combination system renders obvious claim 1.

3. Claim 5: *The system of claim 1, wherein the first switch is on for less than one-half cycle of the modulated carrier signal.*

171. In the combination system (whether capacitors share a resister (Fig. 3), or each capacitor is paired with a separate resister (Fig. 6)), the first switch (gray) is on for less than one-half cycle of the modulated carrier signal (i.e., input signal).

172. Tayloe explains that "commutating switch 38 [implemented as the TI multiplexer/demultiplexer] remains closed at each of the four outputs for substantially 90 degrees [less than one-half cycle] at the frequency of the input signal." TI-1004, 2:27-32, 2:33-45 ("During the time that commutating switch 38 [implemented as the TI multiplexer/demultiplexer] connects input 36 to output 42 [the 0-degree output], charge builds up on capacitor 72 [corresponding to capacitor 175 in the combination system]"), 2:46-55 ("Output 42 represents the average value of the input signal during the first quarter wave of the period, and is termed the 0 degree output …."), 5:1-16 ("[I]nput signal f_I is connected to each of the four outputs of analog multiplexer 202 [implemented as the TI multiplexer/demultiplexer] for substantially 90 degrees of the input signal. As embodied in FIG. 7, 0 degree output

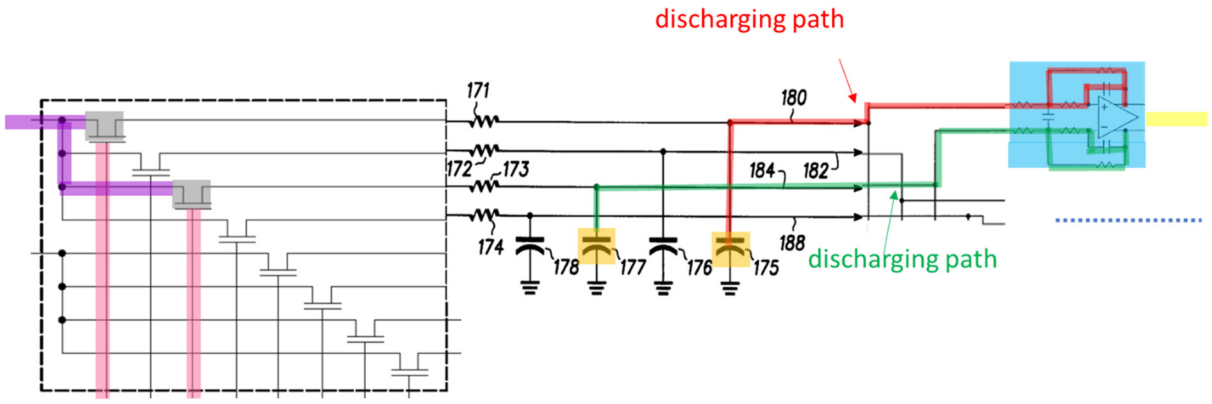
[is] used to generate baseband in-phase … signal[]"), Figs. 3 (system diagram), 4 (waveform example where "[p]oint 105 represents the voltage to which capacitor 72 (FIG. 3) charges," 3:40-48)), 6 (separate integrator), 7 (analog multiplexer/demultiplexer).

4. Claim 8: ***The system of claim 1, wherein the first and second control signals each control a charging and discharging cycle of their respective energy storage element by respectively controlling the first and second switching devices so that for each switching device said portion of energy that is distinguishable from noise is transferred to the respective storage element when the switch is on during the charging cycle, and a portion of the transferred energy is discharged during the discharging part of the cycle for each respective switching device when the switching device is off.***

173. In the combination system (whether capacitors share a resister (Fig. 3), or each capacitor is paired with a separate resister (Fig. 6)), the first and second control signals (pink) each control a charging and discharging cycle for respective energy storage element (brown) by respectively controlling the first and second switches (gray). *Supra* 1[b], 1[d].

174. Specifically, for each switch (gray), the portion of energy that is distinguishable from noise is transferred to the respective storage element (brown) when the switch is on (i.e., CLOSED) during the charging cycle. Id. When the switch (gray) is off (i.e., OPEN), a portion of the transferred energy (e.g., charge accumulated) is discharged, as annotated below for two discharging paths.

175. Each capacitor is coupled to the input impedance of the fully differential amplifier, which is typically in the kilo ohm range, and as a result, incomplete discharge of accumulated charges.



Combination System (using switch of TI-1005 and circuit of TI-1021/TI-1022)

5. Claim 9: ***The system of claim 8, wherein for each respective storage element, the energy discharged during any given discharge cycle is not completely discharged, with the remaining undischarged energy from the given discharge cycle becoming an initial condition for the next charging cycle.***

176. In the combination system (whether capacitors share a resister (Fig. 3), or each capacitor is paired with a separate resister (Fig. 6)), for each storage device (capacitor in brown), the energy discharged during any given discharge cycle is not completely discharged. Specifically, the discharge rate would be determined by the RC characteristic of the underlying circuit, and given the typical parameters, the discharge of accumulated charges would not be complete by the end of the period the switch is open. Further. the low-pass filter in the feedback circuit of the

differential amplifier would also lead to incomplete discharge. The remaining undischarged energy from the given discharge cycle thus becomes an initial condition for the next charging cycle (when the switch is closed).

6. Claim 11: ***The system of claim 1, wherein the frequencies of the first and second apertures have periods that are two (2) percent or greater of the modulated carrier signal's period.***

177. In the combination system (whether capacitors share a resister (Fig. 3), or each capacitor is paired with a separate resister (Fig. 6)), the frequencies of the first and second apertures (i.e., respective periods during which the first and second switches are closed to generate the 0-degree and 180-degree outputs) have periods that are ***two (2) percent or greater*** (e.g., substantially 25%) of the modulated carrier signal's period. TI-1004, Abstract ("The samples are integrated over time to produce average voltage at 0 degrees, 90 degrees, 180 degrees and 270 degrees."), 2:18-27, 4:28-45; 4:58-63 ("each [integrator] preferably integrates for substantially 90 degrees of the input signal"); §XI.A.1. A POSITA would understand each quadrant (90-degree) is 25%.

7. Claim 12: ***The system of claim 1, wherein the frequencies of the first and second apertures have periods that are five (5) percent or greater of the modulated carrier signal's period.***

178. In the combination system (whether capacitors share a resister (Fig. 3), or each capacitor is paired with a separate resister (Fig. 6)), the frequencies of the first and second apertures (i.e., respective periods during which the first and second

switches are closed to generate the 0-degree and 180-degree outputs) have periods that are ***five (5) percent or greater*** (e.g., substantially 25%) of the modulated carrier signal's period.

8. Claim 13: ***The system of claim 1, wherein the frequencies of the first and second apertures have periods that are ten (10) percent or greater of the modulated carrier signal's period.***

179. In the combination system (whether capacitors share a resister (Fig. 3), or each capacitor is paired with a separate resister (Fig. 6)), the frequencies of the first and second apertures (i.e., respective periods during which the first and second switches are closed to generate the 0-degree and 180-degree outputs) have periods that are ***ten (10) percent or greater*** (e.g., substantially 25%) of the modulated carrier signal's period.

9. Claim 14: ***The system of claim 1, wherein the frequencies of the first and second apertures have periods that are twelve and a half (12.5) percent or greater of the modulated carrier signal.***

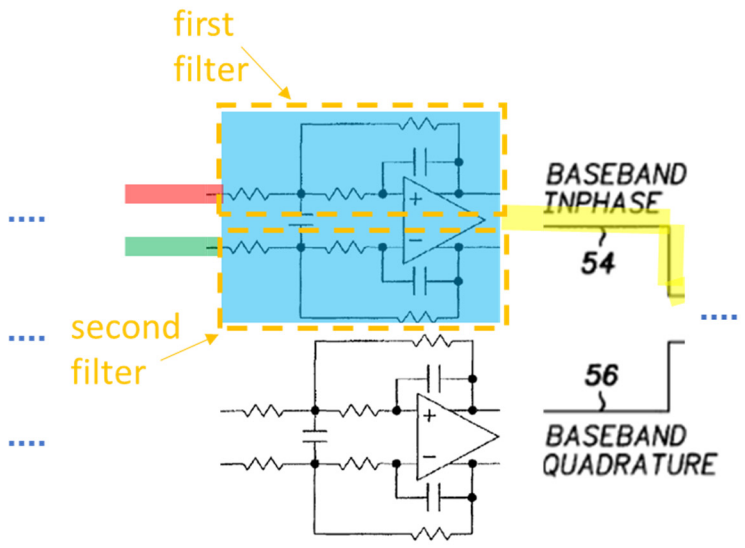
180. In the combination system (whether capacitors share a resister (Fig. 3), or each capacitor is paired with a separate resister (Fig. 6)), the frequencies of the first and second apertures (i.e., respective periods during which the first and second switches are closed to generate the 0-degree and 180-degree outputs) have periods that are ***twelve and a half (12.5) percent or greater*** (e.g., substantially 25%) of the modulated carrier signal's period.

10. Claim 15: 15. The system of claim 1, further comprising:

a first filter that filters said down-converted in-phase baseband signal portion; and

a second filter that filters said down-converted in-phase inverted baseband signal portion.

181. In the combination system (whether capacitors share a resister (Fig. 3), or each capacitor is paired with a separate resister (Fig. 6)), the differential amplifier circuits include a ***first filter*** (orange box) that filters the down-converted in-phase baseband signal portion (red), and a ***second filter*** (orange box) that filters the down-converted inverted in-phase baseband signal portion (green), as annotated below. §§XI.A.1, XI.A.2 (1[c] (in-phase baseband), 1[e] (inverted in-phase baseband), 1[g] (differential amplifier circuit)).



Combined System (zoomed portion using circuits of TI-1021/TI-1022)

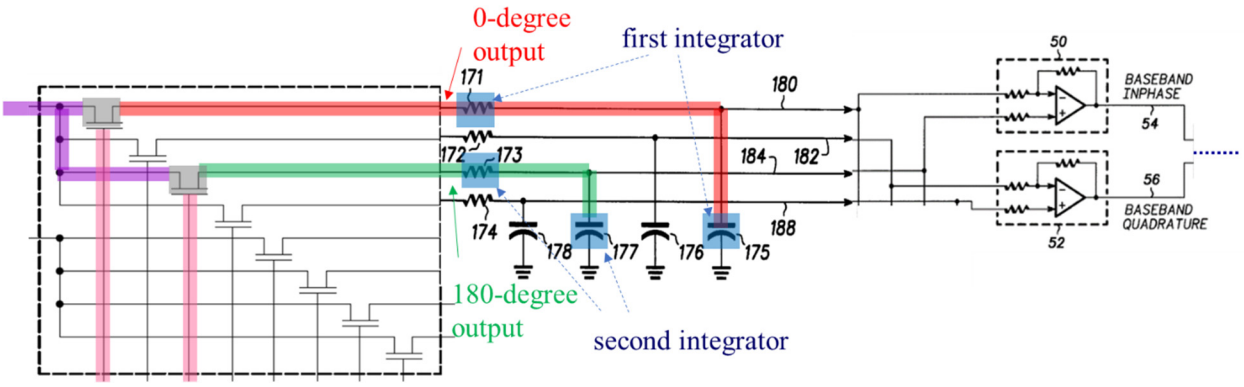
11. Claim 16: ***The system of claim 15, wherein the first and second filters each comprise a low-pass filter.***

182. In the combination system (whether capacitors share a resister (Fig. 3), or each capacitor is paired with a separate resister (Fig. 6)), the first and second filters (orange boxes annotated above) each comprise a low-pass filter. §§III.A.3-4; TI-1014, 7:7-29 (discussing cut-off frequency). I note that ParkerVision submitted infringement chart showing the RC network in conjunction with the amplifier forms a classical low-pass filter. TI-1012.

12. Claim 17: ***The system of claim 1, wherein said portions of transferred energy from each of the first and second switch which are integrated over time to accumulate said portions of transferred energy are integrated by a separate integration module coupled to the output of each said first and second switch.***

183. The combination system (each capacitor is paired with a separate resister (Fig. 6)) renders obvious claim 17. As explained *supra* §§III.A.1-3 and annotated below, the combination system has ***a separate integration module coupled to the output of each said first and second switch*** (e.g., first integration module (combination of capacitor 175 and resistor 171) coupled to the 0-degree output (red), and second integration module (combination of capacitor 177 and resister 173) coupled to the 180-degree output (green). TI-1004, 4:48-49 ("… each integrating capacitor [namely, capacitors 175-178] has its own resister"), 49-57 ("… 0 degree output 180 has a voltage controlled by the combination of capacitor 175

and resistor 171 … 180 degree output 184 has a voltage controlled by the combination of capacitor 177 and resistor 173").



Combination System (using switch of TI-1005)

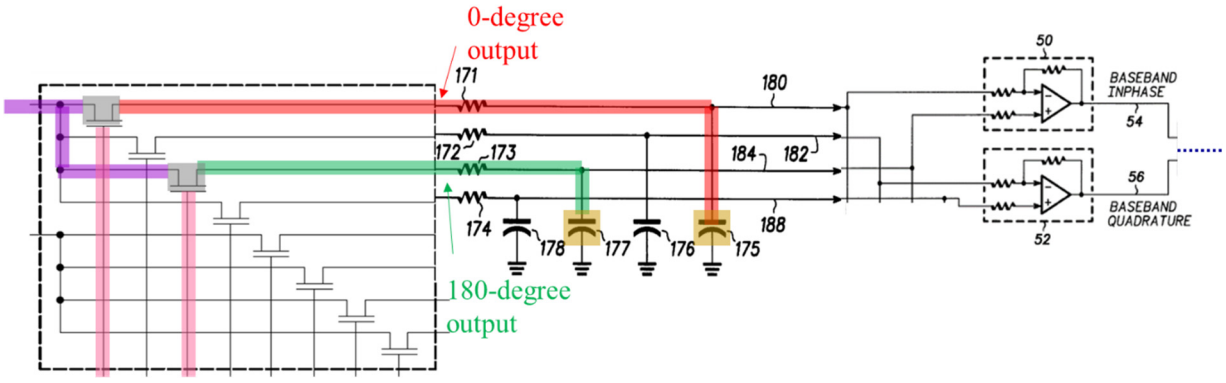
184. In the combination system, the first and second integration modules are ***separate*** from each other. The first integration module is not the same as first energy storage element (capacitor 175). Nor is second integration module identical to second energy storage element (capacitor 177).

185. Moreover, ***the portions of transferred energy from each of the first and second switch which are integrated over time to accumulate said portions of transferred energy are integrated by a separate integration module.*** *Id.*, 4:57-63 ("Resistor 171 and capacitor 175 form a first integrator. The commutating switch of product detector 170 connects the input to this first integrator for substantially 90 degrees of the input signal. A POSITA readily understand that the remaining resistor/capacitor pairs also form integrators, each of which preferably integrates for

substantially 90 degrees of the input signal."), Fig. 6; *see also* Abstract, 2:27-55, 5:1-16, Fig. 3.

13. Claim 18: ***The system of claim 1, wherein said first and second storage elements are capacitive storage circuits, and wherein said portions of transferred energy from each of the first and second switch which are integrated over time to accumulate said portions of transferred energy are integrated by the capacitive storage circuits as they accumulate charge during successive sampling aperture.***

186. The combination system (whether capacitors share a resister (Fig. 3), or each capacitor is paired with a separate resister (Fig. 6)) renders obvious claim 18. As explained *supra* §§X.A-C, XI.A.1 and annotated below, ***the first and second storage elements are capacitive elements*** (i.e., capacitor 175 (brown) for the 0-degree output (red) and capacitor 177 (brown) for the 180-degree output (green)). TI-1004, 4:48-51 (discussing "each integrating capacitor [including capacitor 175 for the 0-degree output and capacitor 177 for the 180-degree output]").



Combination System (using switch of TI-1005)

187. In the combination system, ***the portions of transferred energy from each of the first and second switch which are integrated over time to accumulate said portions of transferred energy are integrated by the capacitive storage circuits as they accumulate charge during successive sampling apertures*** (e.g., duration of switch closures). Tayloe explains that "commutating switch 38 [implemented as the TI multiplexer/demultiplexer] remains closed at each of the four outputs for substantially 90 degrees at the frequency of the input signal." TI-1004, 2:27-32, 2:13-18, Abstract ("… commutating switch which serves to sample an RF waveform four times per period at the RF frequency. The samples are integrated over time to produce an average voltage at 0 degrees, 90 degrees, 180 degrees and 270 degrees. The average voltage at 0 degrees is the baseband in-phase signal.... Alternatively, ...the 0 degree average can be differentially summed with the 180 degree average to form the baseband in-phase signal....")

188. "During the time that commutating switch 38 [implemented as the TI multiplexer/demultiplexer] connects input 36 [receiving input signal (purple)] to output 42 [0-degree output], charge builds up on capacitor 72 [corresponding to capacitor 175 in the combination system]." TI-1004, 2:33-45 (further noting "when commutating switch 38 [implemented as the TI multiplexer/demultiplexer] connects input 36 to output[] 46 [the 180-degree output]," charge builds up on capacitor 76 (corresponding to capacitor 177 in the combination)), 5:1-16 ("As embodied in FIG.

7, 0 degree output [can be] used to generate baseband in-phase [] signal[]" and noting "180-degree output "can be utilized as embodied in FIG. 3 to achieve greater gain"), Figs. 3 (system diagram) 4 (waveform example), 6 (separate integrator), 7 (analog multiplexer/demultiplexer).

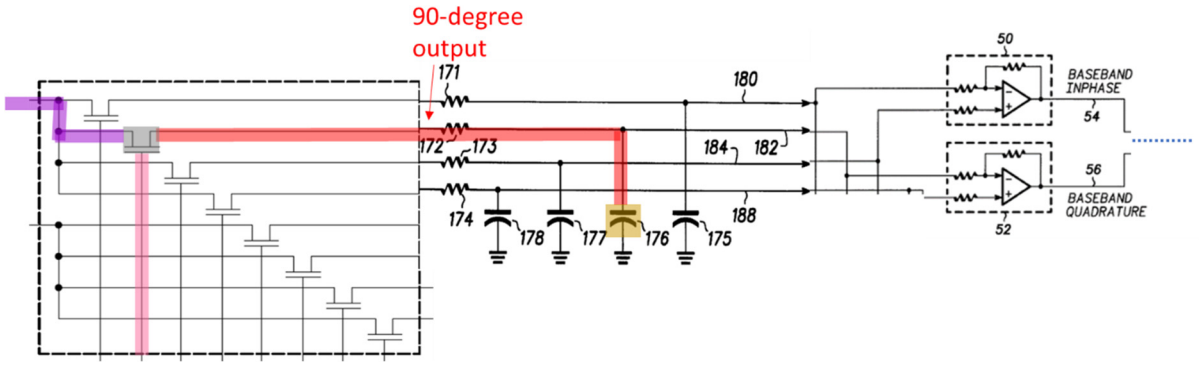
14. Claim 19:

a) Element 19(a): The system of claim 1, further comprising:

189. I have explained, *supra* §XI.A.2 (claim 1), the combination system muse the capacitor arrangements depicted in Fig. 3 (capacitors 72 to 78 sharing resister 32) or Fig. 6 (capacitors 175 to 178 each has a pairing resister)).

b) Element 19(b): a third switch coupled to a third control signal which comprises a sampling aperture with a specified frequency, wherein the third switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal as an output of said third switch during the sampling aperture of the third control signal;

190. As explained *supra* §§III.A.1-4 and annotated below, the combination system provides a ***third switch*** (gray) coupled to a ***third control signal*** (pink) which comprises a ***sampling aperture*** (e.g., up to 90 degree at the frequency of the input signal f_1) with a ***specified frequency*** (i.e., rate of toggling the third switch). TI-1004, 2:5-32, 5:33-37, Figs. 3, 6-7; TI-1005, 2 (logic diagram of the TI SN74CBT3253D multiplexer/demultiplexer incorporated in the annotation below); §III.A.4 (details of the combination system).



Combination System (using switch of TI-1005)

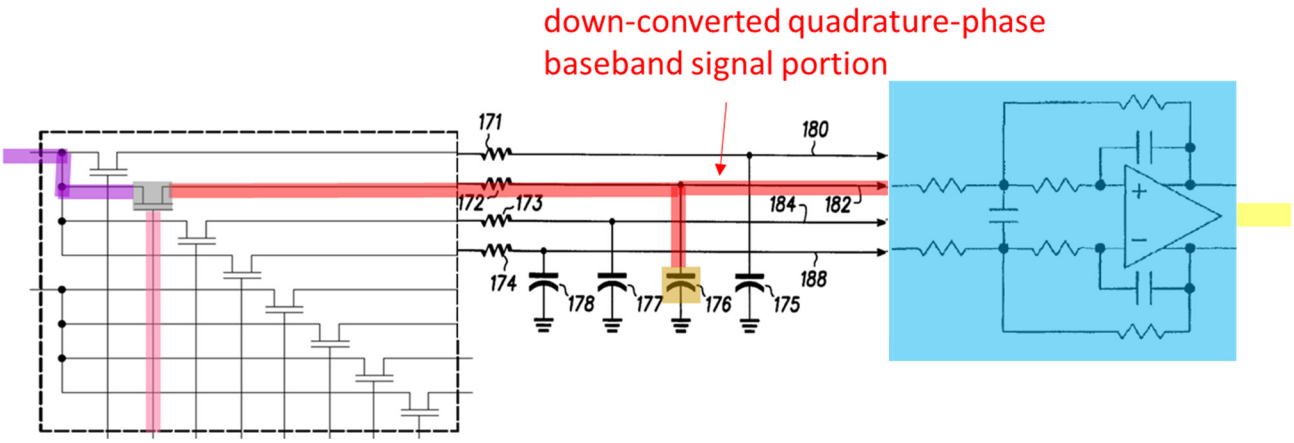
191. The third switch (gray) is on and ***a portion of energy*** that is distinguishable from noise is transferred ***from the modulated carrier signal*** (RF input signal f_1 (purple)) ***as an output*** (the 90-degree output) of said switch during the sampling aperture of the third control signal. TI-1004, 2:27-55, 5:1-16, Figs. 3-4, 6-7; §§XI.A.1 (combination system), XI.A.2 (element 1[b] including "energy distinguishable from noise is transferred").

> *c) Element 19(c): a third energy storage element that stores the transferred energy from the modulated carrier signal and outputs a down-converted quadrature-phase baseband signal portion of said modulated carrier signal;*

192. As explained *supra* §§X.A-C, XI.A.1 and annotated below, the combination system includes ***a third energy storage element*** (e.g., capacitor 176 (brown), or capacitor 74 of Fig. 3) that ***stores*** the transferred energy from the modulated carrier signal (purple) and ***outputs a down-converted quadrature-phase baseband signal portion*** (red portion feeding into differential amplifier 52

implemented using Macnally's circuit) of said modulated carrier signal (purple). TI-1004, 2:13-45 ("… during the time that commutating switch 38 [implemented as the TI multiplexer/demultiplexer] connects input 36 [receiving input signal (purple)] to output 44 [90-degree output corresponding to output 182 in the combination system], charge builds up on capacitor 74 [corresponding to capacitor 176 in the combination system]"), 2:46-55 ("Output 44 [90-degree output corresponding to output 182 in the combination system] represents the average value of the input signal during the second quarter wave of the period, and is termed the 90 degree output …."), 4:49-51 ("… 90 degree output 182 has a voltage controlled by the combination of capacitor 176 and resistor 172 …."), Figs. 3-4, 6-7.

193. Tayloe also describes "90 degree output [can be] used to generate baseband … quadrature signal[]", (TI-1004, 5:1-16), consistent with descriptions from the '528 Patent. TI-1001, Fig. 197, 178:34-42 ("a switch … opens and closes as a function of Q control signal [to generate] a down converted signal").



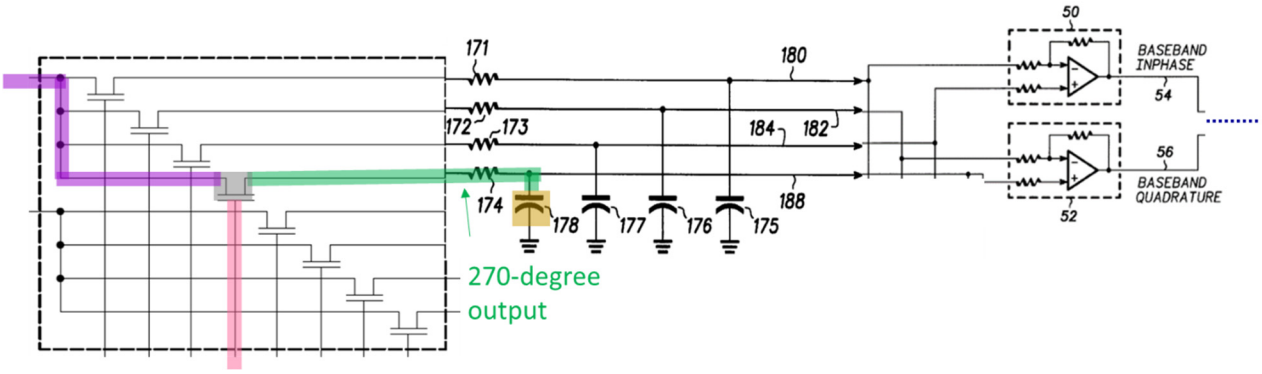
Combination System (using switch of TI-1005 and circuit of TI-1021)

194. Consistent with my earlier discussed claim construction proposal *supra* §IX, Tayloe's capacitor 177 (brown) (or capacitor 74 of Fig. 3) "***stores non-negligible amounts of energy from an input EM signal,***" i.e., the RF input signal f_1. §XI.A.2 (1[c]). Each capacitor has a low impedance load when using Macnally's differential amplifier circuit, thereby meeting ParkerVision's alleged condition of low input impedance.

> *d) Element 19(d): a fourth switch coupled to a fourth control signal which comprises a sampling aperture with a specified frequency, wherein the fourth switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal as an output of said fourth switch during the sampling aperture of the fourth signal;*

195. As explained *supra* §§X.A-C, XI.A.1 and annotated below (similar to 19[b]), the combination system includes a ***fourth switch*** (gray) coupled to a ***fourth***

control signal (pink) which comprises a ***sampling aperture*** (e.g., up to 90 degrees at the frequency of the input signal f_I) with a ***specified frequency*** (e.g., rate of toggling the fourth switch (gray)). TI-1004, 2:5-26, 2:27-32, 5:1-16, Figs. 3, 6-7; TI-1005, 2; §XI.A.1 (element 19[b]).



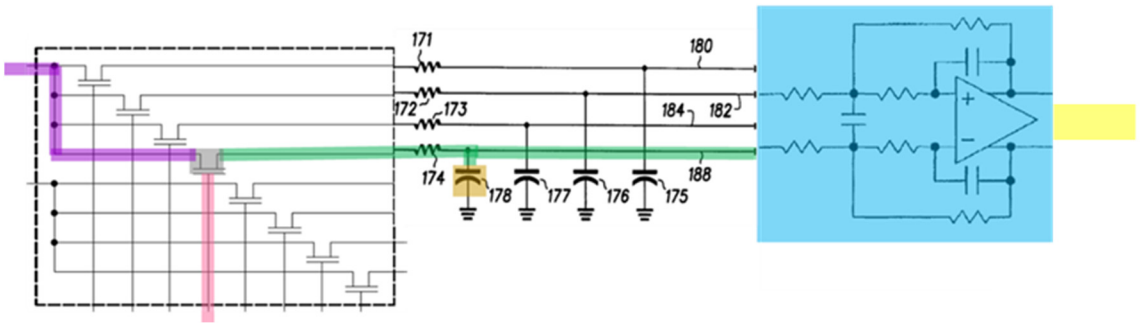
Combination System (using switch of TI-1005)

196. The fourth switch (gray) is on and ***a portion of energy*** that is distinguishable from noise is transferred ***from the modulated carrier signal*** (i.e., RF input signal f_I (purple)) as an output (i.e., the 270-degree output) of said second switch ***during the sampling aperture*** (e.g., up to 90 degrees at the frequency of the input signal f_I) of the fourth control signal. TI-1004, 2:27-32, 2:33-45 ("… when commutating switch 38 [implemented as the TI multiplexer/demultiplexer] connects input 36 to output[s] 48 [the 270-degree output corresponding to output 188 in the combination system]," charge builds up on capacitor 78 (corresponding to capacitor 178 in the combination)), 2:46-55 ("… Output 48 represents the average value of the input signal during the fourth quarter wave of the period, and is termed the 270

degree output"), 5:1-16 (270-degree output "can be utilized as embodied in FIG. 3 to achieve greater gain"), Figs. 3-4, 6-7.

e) Element 19(e): a fourth energy storage element that stores the transferred energy from the modulated carrier signal and outputs a down-converted differential[11] quadrature-phase baseband signal portion of said modulated carrier signal;

197. As explained *supra* §§X.A-C, XI.A.1 and annotated below, the combination system includes ***a fourth energy storage element*** (e.g., capacitor 178 (brown), or capacitor 78 in Fig. 3) that ***stores*** the transferred energy from the modulated carrier signal (purple) and ***outputs a down-converted inverted quadrature-phase baseband signal portion*** (green portion feeding into Macnally's circuit) of said modulated carrier signal (purple). TI-1004, 2:27-45 (describing switch operations and capacitor charge build-up), 4:55-57 (describing "270 degree output 188"); §XI.A.2 (element 19[d])).



Combination System (using switch of TI-1005 and circuit of TI-1021/TI-1022)

[11] "inverted"

198. Tayloe explains that the 270-degree output "can be utilized as embodied in FIG. 3 to achieve greater gain" (TI-1005, 5:1-16) because the 270-degree output is an inverted version of the 90-degree output, and hence the inverted in-phase baseband signal consistent with descriptions provided by the '528 Patent. TI-1001, Fig. 197 (fourth processing module 19714), 179:4-10 ("a switch … opens and closes as a function of inverted Q control signal … As a result of the opening and closing of this switch … a down-converted signal, referred to as the inverted Q output signal, results").

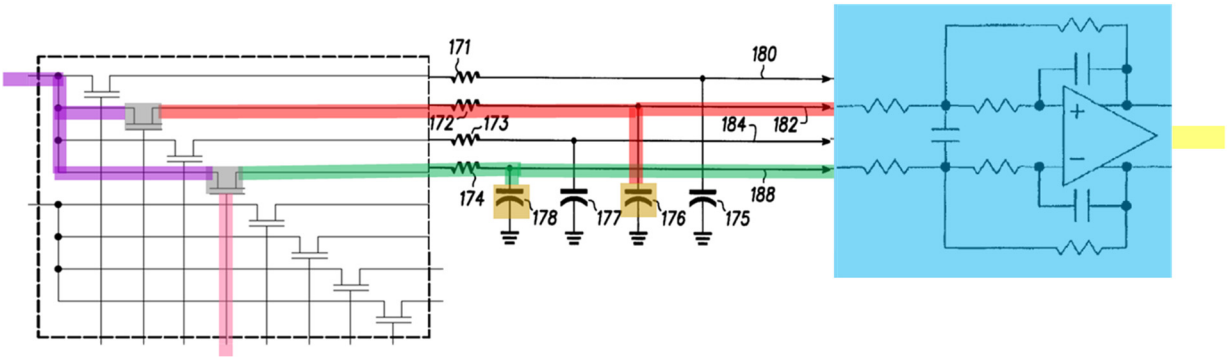
199. According to the claim construction proposal supra §IV.C and similar to 19[c], Tayloe's capacitor 178 (brown) (or capacitor 78 of Fig. 3) "stores non-negligible amounts of energy from an input EM signal," i.e., the RF input signal VRF. I have analyzed Macnally's circuit supra VI.C, which demonstrates low input impedance of Macnally's circuit. This provides a low impedance load to the capacitor of Tayloe, which comports with ParkerVision's requirement of low impedance load.

f) Element 19(f): wherein the portions of transferred energy from each of the third and fourth switch are integrated over time to accumulate said portions of transferred energy from which said down-converted quadrature-phase baseband signal portion and said down-converted differential[12] quadrature-phase baseband signal portion are derived; and;

200. As explained *supra* §§X.A-C, XI.A.1 and annotated below, in the combination system, ***the portions of transferred energy*** from each of the third and fourth switch ***are integrated*** over time to accumulate said portions of transferred energy ***from which said down-converted quadrature-phase baseband signal portion*** (red portion feeding into Macnally's circuit) ***and said down-converted inverted quadrature-phase baseband signal portion*** (green portion feeding into Macnally's circuit) ***are derived***. TI-1004, 4:46-67 ("… 90 degree output 182 has a voltage controlled by the combination of capacitor 176 and resistor 172 … 270 degree output 188 has a voltage controlled by the combination of capacitor 178 and resistor 174 … [these] resistor/capacitor pairs also form integrators, each of which preferably integrates for substantially 90 degrees of the input signal …."), Abstract. Moreover, Tayloe discloses similar integrator operation in the example of Figure 3 using capacitors 74 and 78 respectively for the 90-degree and 270-degree outputs. TI-1004, 2:33-55 ("Each of the capacitors [including capacitors 74 and 77] functions

[12] "inverted"

as a separate integrator, each integrating a separate quarter wave of the input signal."), Figs. 3-4, 6-7; §XI.A.1 (element 1[f]).



Combination System (using switch of TI-1005 and circuit of TI-1021)

g) *Element 19(g): a second differential amplifier circuit that combines said down- converted quadrature-phase baseband signal portion with said down-converted differential*[13] *quadrature-phase baseband signal portion and outputs a second channel down-converted differential quadrature-phase baseband signal.*

201. As explained *supra* §§X.A-C, XI.A.1 and annotated below, the combination system includes a ***second differential amplifier circuit*** (light blue) that ***combines said down-converted quadrature-phase baseband signal portion*** (red portion feeding into Macnally's circuit) ***with said down-converted inverted quadrature-phase baseband signal portion*** (green portion feeding into Macnally's

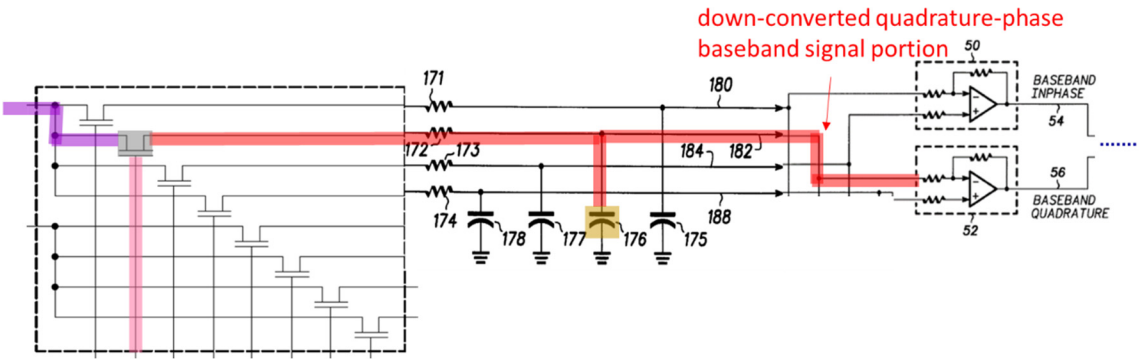
[13] "inverted"

circuit) ***and outputs a second channel down-converted differential quadrature-phase baseband signal*** (yellow). TI-1004, 2:56-67 (noting "[s]umming amplifier 52 [implemented using MacNally's circuit] differentially sums the 90 degree output and the 270 degree output, thereby producing base band quadrature signal 56" and discuss explaining baseband in-phase signal are combined with baseband quadrature signal to generate signal of interest 62), Abstract, Fig. 3; §III.A.5 (1[g]). As I explained VI, a fully differential amplifier generates differential output signal having two complementary components, each combining the two complementary components of the differential input signal.

202. Therefore, my opinion is that the combination system teaches claim 19.

15. Claim 23: *The system of claim 19, wherein the third switch is on for less than one-half cycle of the modulated carrier signal.*

203. In the combination system (whether capacitors share a resister (Fig. 3), or each capacitor is paired with a separate resister (Fig. 6)), the third switch (gray), as annotated below, is on for less than one-half cycle of the modulated carrier signal (i.e., input signal). TI-1004, 2:27-32, 33-45, 46-55, 5:1-16, Figs. 3-4, 6-7; §III.A.5 (claim 5).

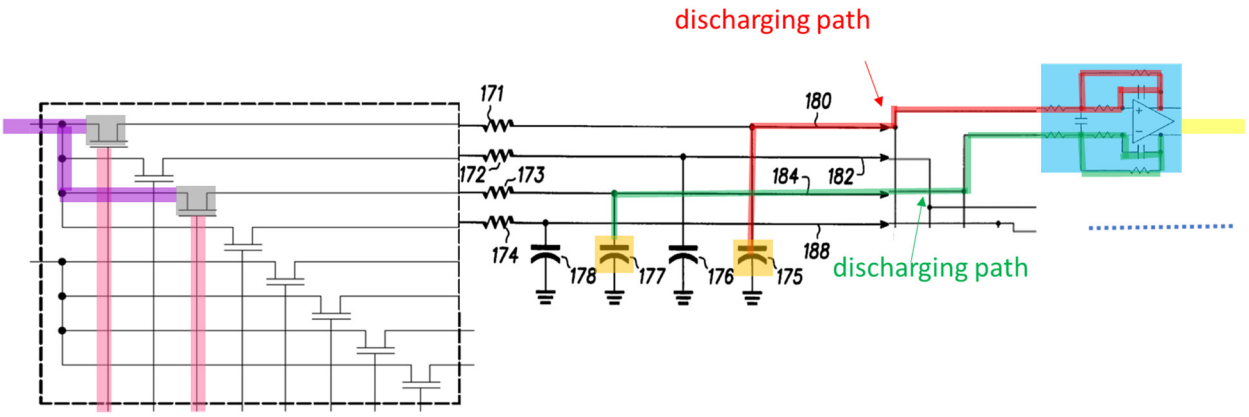


Combination System (using switch of TI-1005 and circuit of TI-1021/TI-1022)

16. Claim 26: ***The system of claim 19, wherein the third and fourth control signals each control a charging and discharging cycle of their respective third and fourth energy storage element by respectively controlling the third and fourth switching devices so that for each third and fourth switching device a portion of energy that is distinguishable from noise is transferred to the respective third and fourth storage element when the respective switch is on during the charging cycle, and a portion of the transferred energy is discharged during the discharging part of the cycle for each respective third and fourth switching device when the respective switching device is off.***

204. Similar to claim 8, in the combination system (whether capacitors share a resister (Fig. 3), or each capacitor is paired with a separate resister (Fig. 6)), the third and fourth control signals (pink) each control a charging and discharging cycle for respective energy storage element (brown) by respectively controlling the third and fourth switches (gray). *Supra* 19[b], 19[d]. Specifically, for each switch (gray), the portion of energy that is distinguishable from noise is transferred to the respective storage element (brown) when the switch is on (i.e., CLOSED) during the charging

cycle. *Id.* When the switch (gray) is off (i.e., OPEN), a portion of the transferred energy (e.g., charge accumulated) is discharged, as annotated below.



Combination System (using switch of TI-1005 and circuit of TI-1021/TI-1022)

17. Claim 27:. ***The system of claim 26, wherein for each respective energy storage element, the energy discharged during any given discharge cycle is not completely discharged, with the remaining undischarged energy from the given discharge cycle becoming an initial condition for the next charging cycle.***

205. Similar to claim 9, in the combination system (whether capacitors share a resister (Fig. 3), or each capacitor is paired with a separate resister (Fig. 6)), for each storage device (capacitor in brown), the energy discharged during any given discharge cycle is not completely discharged. The remaining undischarged energy from the given discharge cycle thus becomes an initial condition for the next charging cycle (when the switch is closed).

18. Claim 28:. ***The system of claim 26, wherein for each respective energy storage element, the energy discharged during any given discharge cycle is not completely discharged, with the remaining undischarged energy from the given***

discharge cycle becoming an initial condition for the next charging cycle.

206. Similar to claim 11, in the combination system (whether capacitors share a resister (Fig. 3), or each capacitor is paired with a separate resister (Fig. 6)), the frequencies of the third and fourth apertures (i.e., respective periods during which the third and fourth switches are closed to generate the 90-degree and 270-degree outputs) have periods that are **two (2) percent or greater** (e.g., substantially 25%) of the modulated carrier signal's period. TI-1004, Abstract, 2:18-27, 4:28-45; 4:58-63, §XI.A.1-2 (claim 11). A POSITA would understand each quadrant (90-degree) is 25%.

19. Claim 30: ***The system of claim 19, wherein the frequencies of the third and fourth apertures have periods that are five (5) percent or greater of the modulated carrier signal's period.***

207. Similar to claim 12, in the combination system (whether capacitors share a resister (Fig. 3), or each capacitor is paired with a separate resister (Fig. 6)), the frequencies of the third and fourth apertures (i.e., respective periods during which the third and fourth switches are closed to generate the 90-degree and 270-degree outputs) have periods that are **five (5) percent or greater** (e.g., substantially 25%) of the modulated carrier signal's period. TI-1004, Abstract, 2:18-27, 4:28-45; 4:58-63, §XI.A.1-2 (claim 12). A POSITA would understand each quadrant (90-degree) is 25%.

20. Claim 31: ***The system of claim 19, wherein the frequencies of third and fourth apertures have periods that are ten (10) percent or greater of the modulated carrier signal's period.***

208. Similar to claim 13, in the combination system (whether capacitors share a resister (Fig. 3), or each capacitor is paired with a separate resister (Fig. 6)), the frequencies of the third and fourth apertures (i.e., respective periods during which the third and fourth switches are closed to generate the 90-degree and 270-degree outputs) have periods that are **ten (10) percent or greater** (e.g., substantially 25%) of the modulated carrier signal's period. TI-1004, Abstract, 2:18-27, 4:28-45; 4:58-63, §XI.1-2 (claim 13). A POSITA would understand each quadrant (90-degree) is 25%.

21. Claim 32: ***The system of claim 19, wherein the frequencies of third and fourth apertures have periods that are twelve and a half (12.5) percent or greater of the modulated carrier signal's period.***

209. Similar to claim 14, in the combination system (whether capacitors share a resister (Fig. 3), or each capacitor is paired with a separate resister (Fig. 6)), the frequencies of the third and fourth apertures (i.e., respective periods during which the third and fourth switches are closed to generate the 90-degree and 270-degree outputs) have periods that are **twelve and a half (12.5) percent or greater** (e.g., substantially 25%) of the modulated carrier signal's period. TI-1004, Abstract,

2:18-27, 4:28-45; 4:58-63, §XI.A.1-2 (claim 14). A POSITA would understand each quadrant (90-degree) is 25%.

22. Claim 33: ***The system of claim 19, further comprising:***

a first filter that filters said down-converted in-phase baseband signal portion;

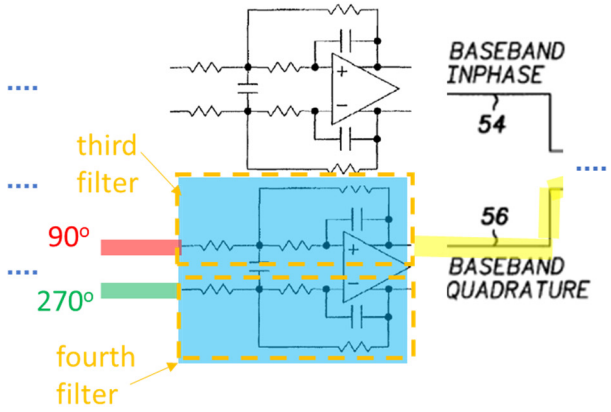
a second filter that filters said down-converted inverted in-phase baseband signal portion;

a third filter that filters said down-converted quadrature-phase baseband signal portion;

a fourth filter that filters said down-converted inverted quadrature-phase baseband signal portion.

210. As explained *supra* §XI.A.1-2 (claim 15), in the combination system (whether capacitors share a resister (Fig. 3), or each capacitor is paired with a separate resister (Fig. 6)), the differential amplifier circuits include a ***first filter*** that filters the down-converted in-phase baseband signal portion, and a ***second filter*** that filters the down-converted inverted in-phase baseband signal portion.

211. As annotated below, the combination system also includes a ***third filter*** (orange box) that filters the down-converted quadrature-phase baseband signal portion (red), and a ***fourth filter*** (orange box) that filters the down-converted inverted quadrature baseband signal portion (green). §§X.A-C, §XI.A.1 (19[c] (quadrature-phase baseband), 19[e] (inverted quadrature-phase baseband), 19[g] (differential amplifier circuit).



Combined System (zoomed portion using circuits of TI-1021/TI-1022)

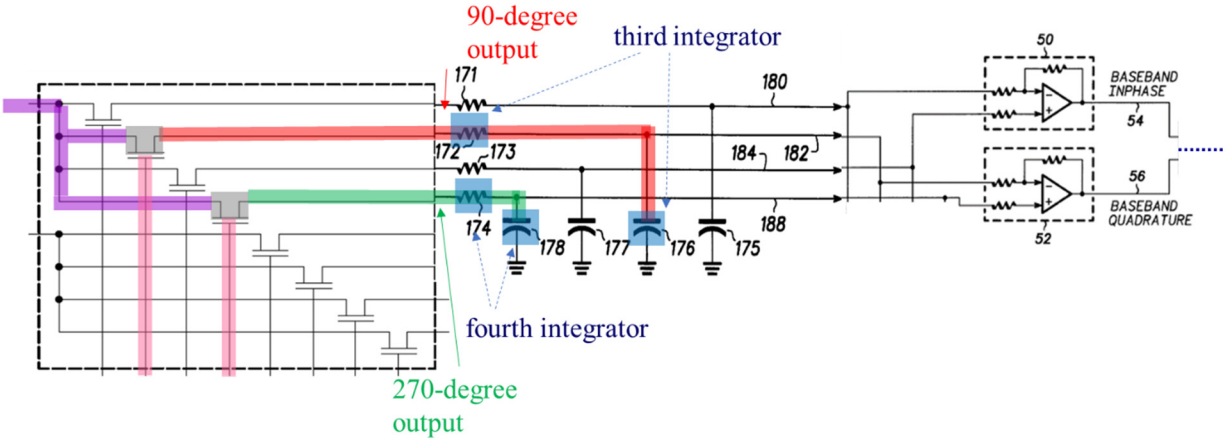
23. Claim 34: ***The system of claim 33, wherein the first, second, third, and fourth filters each comprise a low-pass filter.***

212. As explained *supra* §XI.A.2 (claim 16), in the combination system (whether capacitors share a resister (Fig. 3), or each capacitor is paired with a separate resister (Fig. 6)), the first and second filters each comprise a low-pass filter. Further, the third and fourth filters each comprise a low-pass filter. §§X.A-C, XI-A-1; TI-1014, 7:7-29 (discussing cut-off frequency). Here, a RC network in conjunction with an amplifier forms a classical low-pass filter, consistent with ParkerVision's infringement read on accused products. TI-1012 (PV's infringement chart).

24. Claim 35: ***The system of claim 19, wherein said portions of transferred energy from each of the first, second, third and fourth switch which are integrated over time to accumulate said portions of transferred energy are integrated by a***

separate integration module coupled to the output of each said first, second, third and fourth switch respectively.

213. Similar to explanation *supra* §III.A.5 (claim 17), the combination system (each capacitor is paired with a separate resister (Fig. 6)) has ***a separate integration module*** (separate capacitor-resister pair) ***coupled to the output of each of the first, second, third*** (gray)***,*** and ***fourth*** (gray) ***switch***. TI-1004, 4:48-49, 49-57. The integration modules are separate from each other. Each integration module is not the same as an energy storage element.

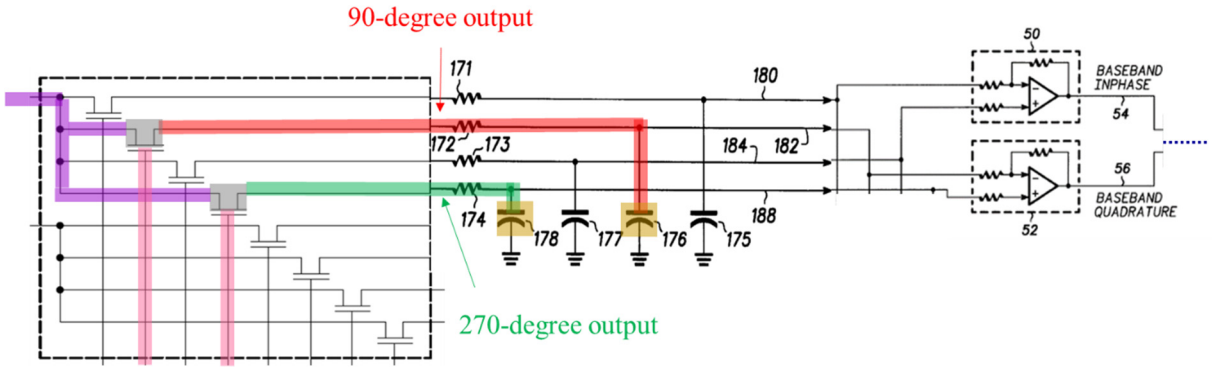


Combination System (using switch of TI-1005)

214. Moreover, ***the portions of transferred energy from each of the first, second, third, and fourth switch which are integrated over time to accumulate said portions of transferred energy are integrated by a separate integration module.*** *Id.*, 4:57-63 ("each [integration module] preferably integrates for substantially 90 degrees of the input signal."), Fig. 6; *see also* Abstract, 2:27-55, 5:1-16, Fig. 3.

25. Claim 36: ***The system of claim 19, wherein said first, second, third and fourth storage elements are capacitive storage circuits, and wherein said portions of transferred energy from each of the first, second, third, and fourth switch which are integrated over time to accumulate said portions of transferred energy are integrated by the capacitive storage circuits of the respective first, second, third and fourth storage elements as they accumulate charge during successive sampling apertures.***

215. Similar to explanation *supra* §III.A.5 (claim 18), in the combination system (whether capacitors share a resister (Fig. 3), or each capacitor is paired with a separate resister (Fig. 6)), ***the first, second, third, and fourth storage elements are capacitive elements*** (i.e., capacitors). TI-1004, 4:48-51 (discussing "each integrating capacitor ….").



Combination System (using switch of TI-1005)

216. In the combination system, ***the portions of transferred energy from each of the first, second, third, and fourth switch which are integrated over time to accumulate said portions of transferred energy are integrated by the capacitive storage circuits as they accumulate charge during successive sampling apertures***

(e.g., duration of switch closures). Tayloe explains that "commutating switch 38 [implemented as the TI multiplexer/demultiplexer] remains closed at each of the four outputs for substantially 90 degrees at the frequency of the input signal." TI-1004, 2:27-32, 2:13-18, Abstract ("… commutating switch which serves to sample an RF waveform four times per period at the RF frequency. The samples are integrated over time to produce an average voltage at 0 degrees, 90 degrees, 180 degrees and 270 degrees."). "During the time that commutating switch 38 [implemented as the TI multiplexer/demultiplexer] connects input 36 [receiving input signal (purple)] to output 42 [0-degree output], charge builds up on capacitor 72 [corresponding to capacitor 175 of Fig. 6]." TI-1004, 2:33-45 (further noting "when commutating switch 38 [implemented as the TI multiplexer/demultiplexer] connects input 36 to output[] 46 [the 180-degree output]," charge builds up on capacitor 76 (corresponding to capacitor 177 of Fig. 6), and "during the time commutating switch 38 connects input 36 to output 44 [the 90-degree output], charge builds up on capacitor 74 [corresponding to capacitor 176 in Fig. 6]"), 5:1-16 ("… 0 degree output [] and 90 degree output [] are used to generate baseband in-phase and quadrature signals" and "the remaining two outputs (180 degrees and 270 degrees) can be utilized as embodied in FIG. 3 to achieve greater gain"), Figs. 3 (system diagram) 4 (waveform example), 6 (separate integrator), 7 (analog multiplexer/demultiplexer).

B. Ground 1B: Tayloe, TI datasheet, Macnally, and Cahn Render Obvious Claims 2-4, 20-22

217. Tayloe discloses modulation by noting "information bearing signals are superimposed on f_1," (TI-1004, 4:5-8), after discussing an example in which "the integrated voltages on capacitors 72-78 … change at a rate equal to Δf, which is the frequency of the signal of interest at baseband," (*id.*, 3:62-4:5), which a POSITA would recognize to include phase modulation.

1. Predictable combination of Tayloe, TI Datasheet, Macnally, and Cahn

218. Further, a POSITA would have found it obvious to apply the combination system to down-convert a RF signal modulated using amplitude modulation, phase modulation, or combined amplitude and phase modulation, because these were well-known established techniques commonly used to modulate signals for receivers. For example, Macnally disclosed the use of BFSK. TI-1021, 7:45-51; TI-1022, 12. Indeed, the application would have been a combination of prior art elements according to known methods to yield predictable results (i.e., applying well-known modulation techniques).

2. Claim 2: *The system of claim 1, wherein said modulated carrier signal includes an amplitude variation*.

219. As explained *supra* §X.A-D and XI.B.1, it would have been obvious for the combination system to operate on modulated carrier signal that includes an amplitude variation so that the integrated voltages on the corresponding capacitors

vary in amplitude to generate baseband signals that track "the information bearing signals." TI-1004, 4:5-8; TI-1007, 150-51. An example of such modulation/demodulation design is pulse amplitude modulation (PAM), as discussed in Cahn.

3. Claim 3: *The system of claim 1, wherein said modulated carrier signal includes a phase variation.*

220. As explained *supra* §§X.A-D and XI.B.1, in addition to Tayloe's example using phase modulation, (TI-1004, 3:62-4:5), it would have been obvious for the combination system to operate on modulated carrier signal that includes a phase variation so that the integrated voltages on the corresponding capacitors vary in phase to generate baseband signals that track "the information bearing signals." TI-1007, 150-51. An example of such modulation/demodulation design is frequency shift keying (FSK), as discussed in Cahn.

4. Claim 4: *The system of claim 1, wherein said modulated carrier signal includes a combination of amplitude variation and phase variation.*

221. As explained *supra* §III.B.1-2 and III.A.1-4, it would have been obvious for the combination system to operate on modulated carrier signal that includes a combination of amplitude and phase variation so that the integrated voltages on the corresponding capacitors vary in both amplitude and phase to jointly provide baseband signals that track "the information bearing signals." TI-1007, 150-

51. An example of such modulation/demodulation design is quadrature amplitude modulation (QAM).

5. Claim 20: *The system of claim 19, wherein said modulated carrier signal includes an amplitude variation*.

222. The combination combination renders obvious claim 20 for reasons I discussed above with respect to claim 2. §§XI.B.2 (claim 2), XI.B.1, and X.A-D.

6. Claim 21: *The system of claim 19, wherein said modulated carrier signal includes an phase variation*.

223. The combination renders obvious claim 21 for reasons I discussed above with respect to claim 3. §§XI.B.2 (claim 3), XI.B.1, and X.A-D.

7. Claim 22: *The system of claim 19, wherein said modulated carrier signal includes a combination of amplitude and variation*.

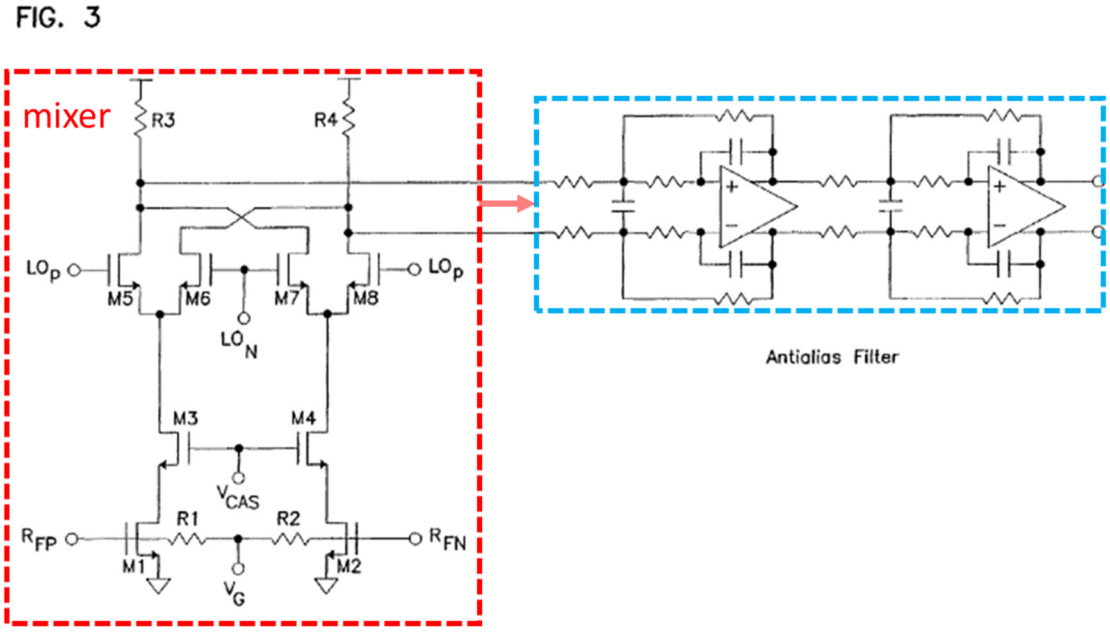
224. The combination renders obvious claim 22 for reasons I discussed above with respect to claim 3. §§XI.B.2 (claim 3), XI.B.1, and X.A-D.

C. Ground 2A – Razavi and Macnally Render Obvious Claims 1, 5, 8-9, 11-19, 23, 26-28, 30-36

225. Based upon my review of the references and my knowledge and experience in this field, it is clear that the Razavi-Macnally combination renders obvious claims 1, 5, 8-9, 11-19, 23, 26-28, 30-36.

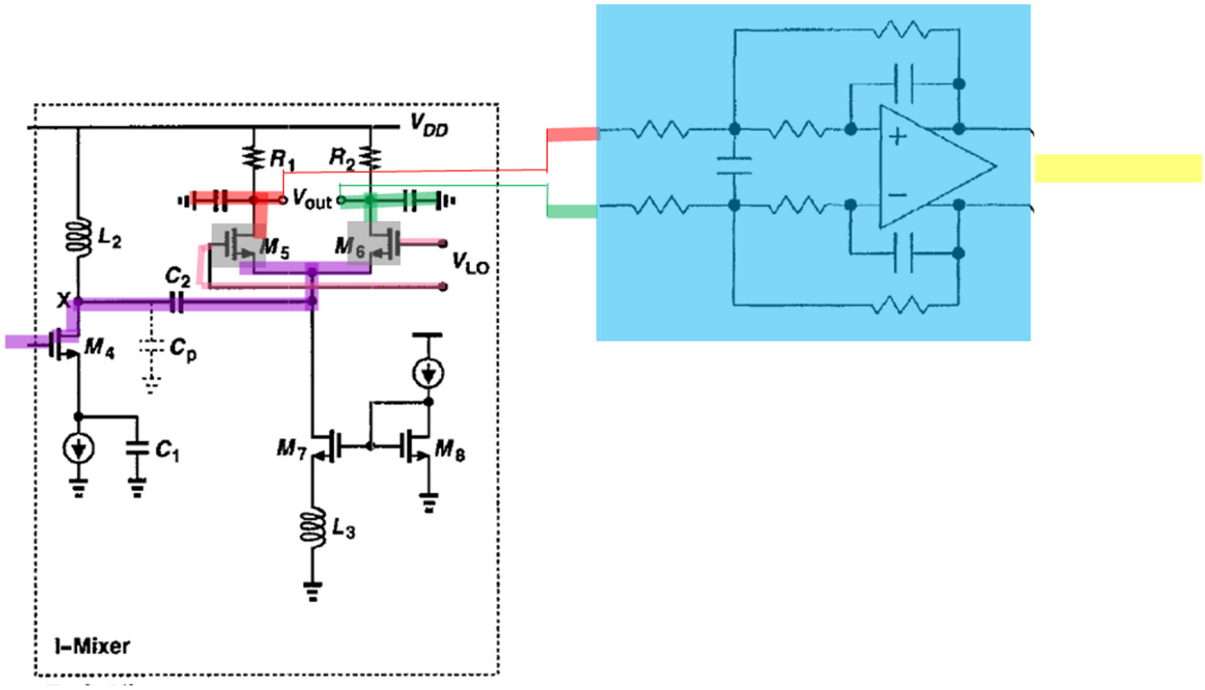
1. Predictable combination of Imai and Higashi

226. As explained earlier under §X-D, Macnally discloses examples of using anti-aliasing filters in an integrated transceiver device. TI-1021, Fig. 3 (annotated below), 1:10-12, 1:44-46, 7:7-8; TI-1022, Fig. 3, pp. 4, 8.



TI-1021/TI-1022, Fig. 3 (annotated)

227. A POSITA would have found it obvious to combine the teachings of Razavi and Macnally by, e.g., incorporating Macnally's fully differential amplifier circuits in Razavi's receiver to process the down-converted signals, as annotated below. TI-1017, Figs. 1-2, 4-5; TI-1021/TI-1022, Fig. 3.



Combination Receiver (using Macnally's circuit (light blue))

228. POSITA would have been motivated to incorporate Macnally's fully differential amplifier circuits in Razavi's receiver to further the objective of Razavi's "single chip" receiver. *Id.*; TI-1021, 1:35-50; TI-1022, 4. Acknowledging "output nodes of the mixer are loaded with on-chip capacitors to suppress high-frequency components," Razavi states "channel-selection filtering is not included," thus suggesting the desire for channel-selection filtering, which a POSITA would understand as low-pass filtering because Razavi performs "direction conversion" to baseband. TI-1017, 113. Indeed, Razavi provides "three permutations in Fig. 4 [depicting high-level examples of] "a low-pass filter suppresses out-of-channel interferers," (*id.*), albeit with no further details of filter design. As explained *supra* §X.D, Macnally provides details of a fully differential amplifier circuit to process

"mixer output." TI-1021, 7:7-16, 7:17-29 ("anti-alias filter"), Fig. 1; TI-1022, 8 (same), Fig. 1. A POSITA would have recognized the benefits of applying the example circuit of Macnally to complement Razavi's receiver design and achieve both amplification and "channel-selection filtering" at baseband. TI-1017, 113.

229. The modification would have had a reasonable expectation of success because it would have been a combination of prior art elements according to known methods to yield predictable results (using Macnally's fully differential amplifier circuit consistent with one design option disclosed by Razavi). TI-1021/TI-1022, Fig. 3; TI-1017, Fig. 4(a).

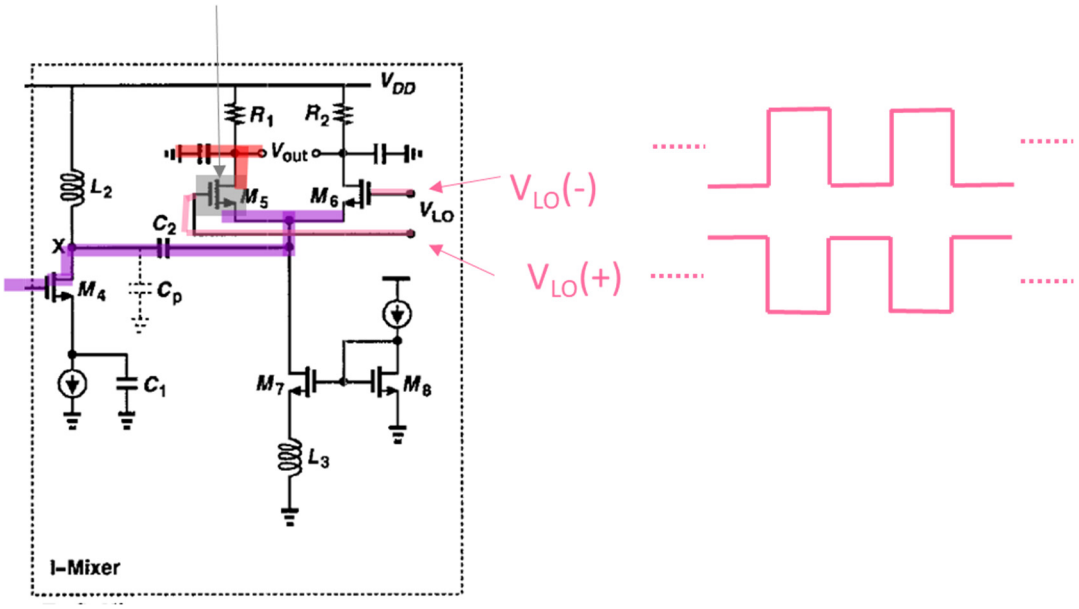
2. Claim 1

a) Element 1(a): A system for frequency down-converting a modulated carrier signal to a baseband signal, comprising:

230. The combination receiver (Razavi's receiver using Macnally's fully differential circuits) is a system for frequency down-converting a modulated carrier signal to a baseband signal. TI-1017 113 ("a single-chip 900-MHz CMOS direct conversion receiver (DCR)"), Fig. 1 (showing down-converting V_{RF} to baseband (BB) signal); TI-1021/TI-1022, Figs. 1, 3.

b) Element 1(b): a first switch coupled to a first control signal which comprises a sampling aperture with a specified frequency, wherein the first switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal as an output of said first switch during the sampling aperture of said first switch;

231. The combination receiver provides 1[b]. As explained supra §§XI.C.1, X.C-D and annotated below, the combination receiver includes a first switch (M5 (gray)) coupled to a first control signal (VLO(+)(pink)) which comprises a sampling aperture (the period when M5 is CLOSED, which lasts approximately half the period of the oscillating frequen-cy of VLO) with a specified frequency (the oscillating frequency of VLO). TI-1017, 1 ("oscillator operates at 1.8 GHz while directly driving the divider.").

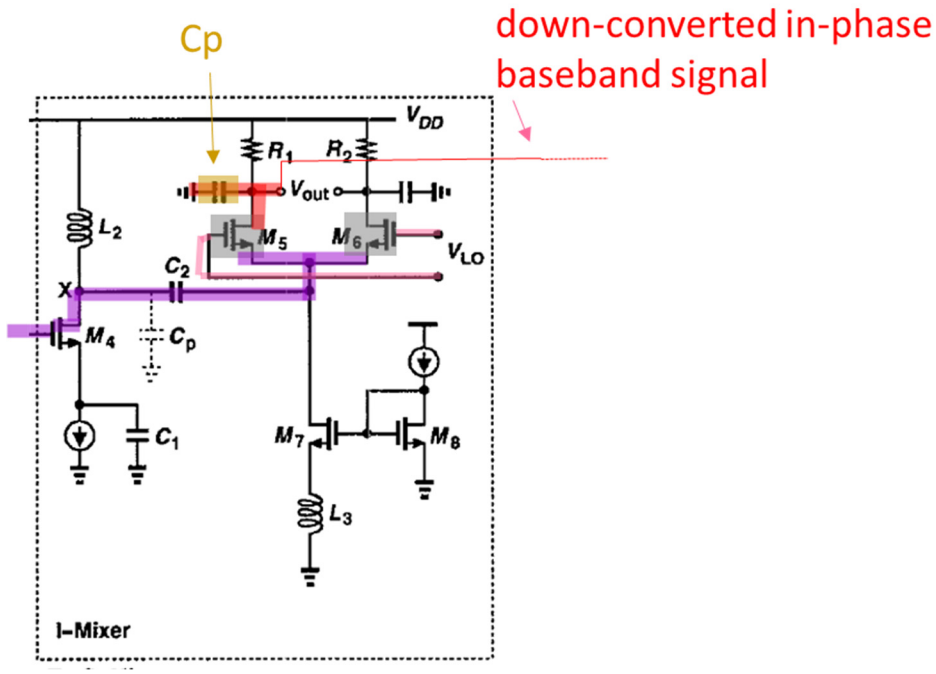


TI-1017, Fig. 2 (annotated)

232. In the combination receiver, the first switch (M_5 (gray)) is on so that the drain terminal starts conducting and ***a portion of energy that is distinguishable from noise*** is transferred from the modulated carrier signal (V_{RF} (purple)) as an output of said first switch (V_{out} (red) above M_5 (gray)) during the sampling aperture of said first switch (when M_5 is ON), consistent with portions of the '528 Specification that allegedly lend support to the Challenged Claims. TI-1001, Fig. 197, 176:66-177:16 ("a switch … opens and closes as a function of I control signal… As a result of the opening and closing of this switch … a down-converted signal, referred to as I output signal, results"). Razavi describes experiment results, further demonstrating sufficient energy distinguishable from noise is transferred by virtue of direct conversion. TI-1017, Table 1; §XI.A.2(1[b]).

c) Element 1[c]: a first energy storage element that stores the transferred energy from the modulated carrier signal and outputs a down-converted in-phase baseband signal portion of said modulated carrier signal;

233. The combination receiver provides [1c]. As explained *supra* §§XI.C.1, X.C-D and annotated below, the combination receiver includes a ***first energy storage element*** (capacitor Cp (brown)) coupled to a ***first control signal*** (V_{LO} bottom (pink)) and outputs a ***down-converted in-phase baseband signal portion*** (red portion exiting in-phase (I) mixer) of said modulated carrier signal (V_{RF} (purple)).



TI-1017 (annotated)

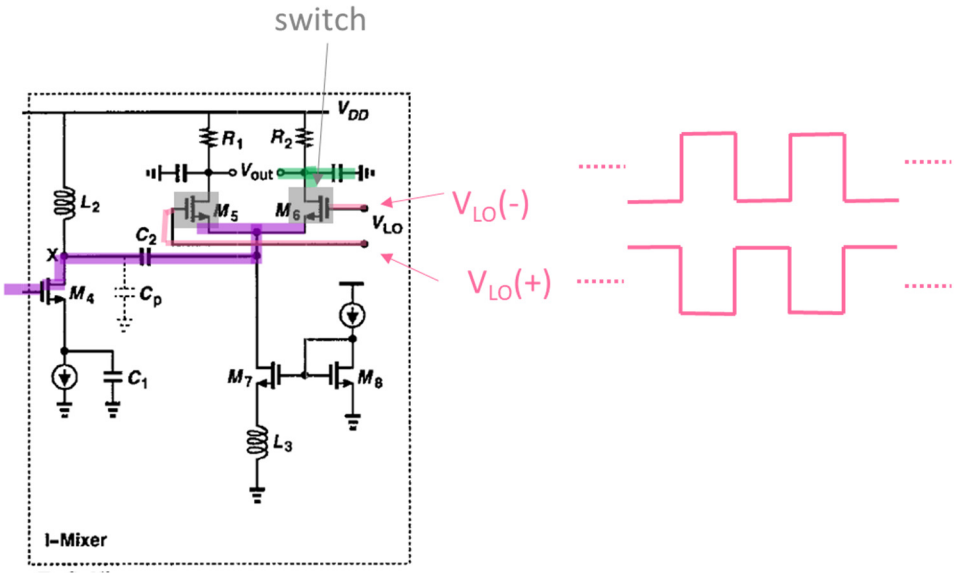
234. As explained in 1[b], when M_5 (gray) is on, the drain terminal starts conducting and the capacitor Cp (brown) stores the transferred energy and outputs a down-converted in-phase baseband portion (red portion) of V_{RF} (purple) in the same manner as described by the '528 Patent. TI-1001, Fig. 197 (first processing module 19702), 176:61-177:15 ("a switch … opens and closes as a function of control signal [to generate] a down-converted signal … a first capacitor stor[es] I output signal").

235. In accordance with the proposed construction *supra* §IX, Razavi's capacitor Cp (brown) "***stores non-negligible amounts of energy from an input EM signal,***" i.e., the RF input signal V_{RF}, to provide sufficient energy for outputting the down-converted signal. Further, the differential amplifier circuit of Macnally provides low impedance load typically in the kilo ohm range, which allegedly "goes

to the heart of what makes an element, a 'storage' element." *See e.g.*, IPR2020-01265, Paper 26 (PO Sur-reply) at 13; Paper 18 (POR) at 46-50.

d) Element 1(d): a second switch coupled to a second control signal which comprises a sampling aperture with a specified frequency, wherein the second switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal as an output of said second switch during the sampling aperture of the second control signal;

236. As explained *supra* §§XI.C.1, X.C-D and annotated below, the combination receiver includes a ***second switch*** (M_6 (gray)) coupled to a ***second control signal*** (V_{LO} (-) (pink)) which comprises a sampling aperture (the period when M_6 is CLOSED, which lasts approximately half the period of the oscillating frequency of V_{LO}) with a specified frequency (the oscillating frequency of V_{LO}).



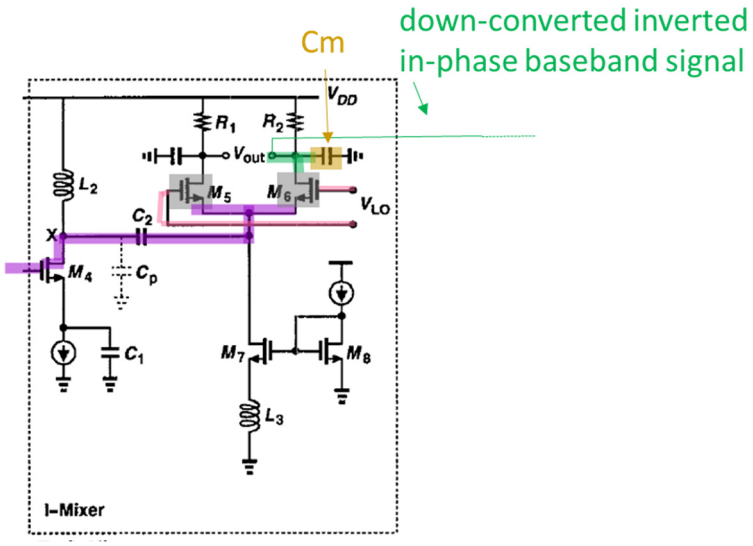
TI-1017, Fig. 2 (annotated)

237. In the combination receiver, the second switch (M_6 (gray)) is on so that the drain terminal starts conducting and ***a portion of energy that is distinguishable from noise*** is transferred from the modulated carrier signal (V_{RF} (purple)) as an output of said first switch (V_{out} (green) above M_6 (gray)) during the sampling aperture of said first switch (when M_6 is ON), consistent with portions of the '528 Specification that allegedly lend support to the Challenged Claims. TI-1001, Fig. 197, 177:31-48 ("a switch … opens and closes as a function of inverted I control signal… As a result of the opening and closing of this switch … a down-converted signal, referred to as inverted I output signal, results"). Significantly, signals on the terminals of Vout are complementary.

e) Element 1(e): a second energy storage element that stores the transferred energy from the modulated carrier signal and outputs a down-converted inverted in-phase baseband signal portion of said modulated carrier signal;

238. The combination receiver provides 1[e]. *Supra* §§XI.C, X.C-D.

239. As further annotated below, the combination receiver includes a ***second energy storage element*** (capacitor Cm (brown)) coupled to a ***second control signal*** (V_{LO} (-) (pink)) and outputs a ***down-converted in-phase baseband signal portion*** (green portion exiting in-phase (I) mixer) of said modulated carrier signal (V_{RF} (purple)).



TI-1017, Fig. 2 (annotated)

240. In accordance with the proposed construction proposal *supra* §IX and similar to 1[c], Razavi's capacitor Cm (brown) "***stores non-negligible amounts of energy from an input EM signal,***" i.e., the RF input signal V_{RF}, to provide sufficient energy for outputting the down-converted signal. Additionally, the low input impedance of Macnally's circuit provides a low impedance load to capacitor Cm of Razavi.

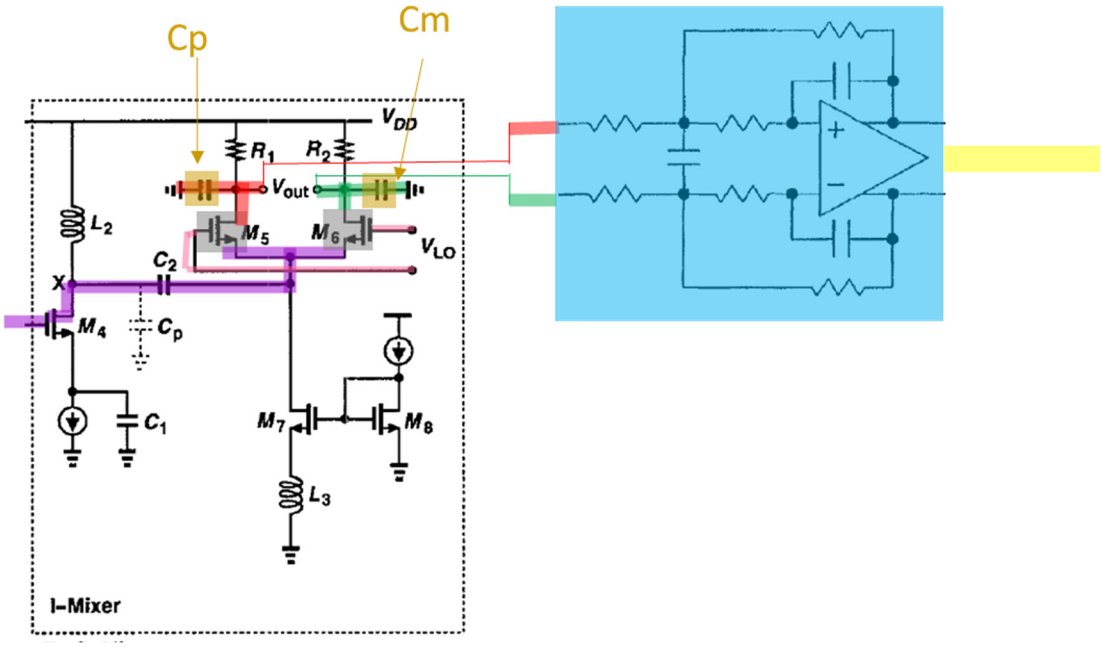
241. As explained in 1[d], when M_6 (gray) is on, the drain terminal starts conducting and the second capacitor (brown) stores the transferred energy and outputs a down-converted inverted in-phase baseband portion (green portion) of V_{RF}

(purple) in the same manner as described by the '528 Patent. TI-1001, Fig. 197 (second processing module 19706), 177:31-54 ("a switch … opens and closes as a function of control signal … As a result of the opening and closing of this switch … a down-converted signal, referred to as the inverted I output signal, results … Inverted I output signa [] is stored by … a second capacitor stor[es] inverted I output signal").

f) Element 1(f): wherein the portions of transferred energy from each of the first and second switch are integrated over time to accumulate said portions of transferred energy from which said down-converted in-phase baseband signal portion and said down-converted inverted in-phase baseband signal portion are derived; and.

242. The combination receiver teaches element 1[f]. §§XI.C.1, X.C-D.

243. As further annotated below, in the combination system, the portions of transferred energy from each of the first and second switch are integrated (e.g., on each respective capacitor Cp/Cm (brown)) over time (when the coupled-to transistor switch is on) to accumulate said portions of transferred energy from which said down-converted in-phase baseband signal portion (red portion feeding into MacNally's Macnally's circuit) and said down-converted inverted in-phase baseband signal portion (green portion feeding into MacNally's Macnally's circuit) are derived. §XI.C.1 (1[c], 1[e]).

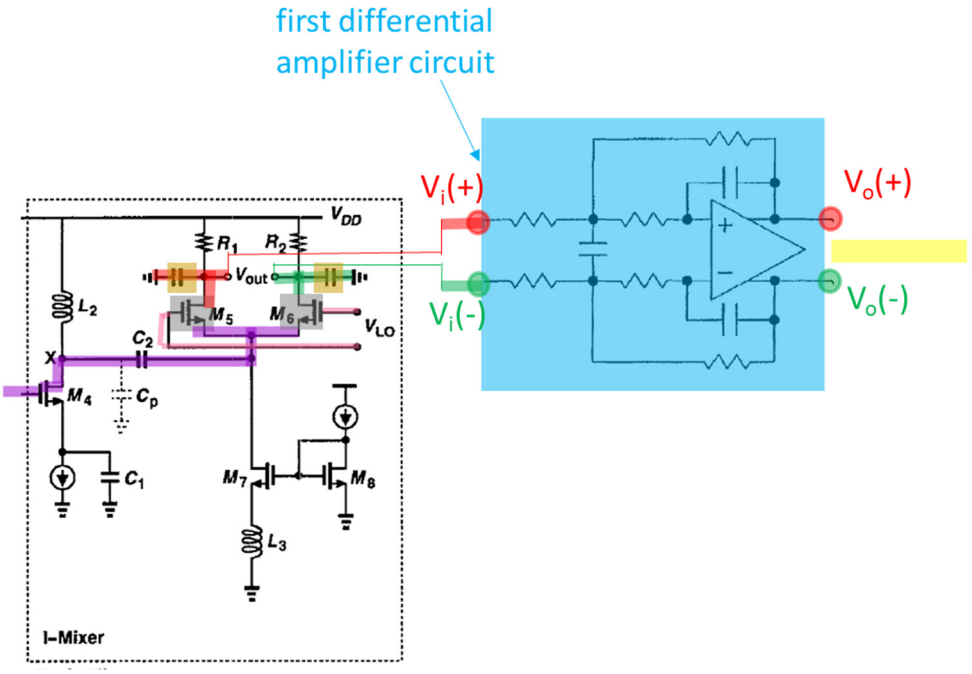


Combination Receiver (using circuit of TI-1021/1022)

g) *Element 1(g): a first differential amplifier circuit that combines said down-converted in-phase baseband signal portion with said down-converted inverted in-phase baseband signal portion and outputs a first channel down-converted differential in-phase baseband signal.*

244. The combination receiver teaches element 1[g]. §§XI.C.1, X.C-D.

245. As further annotated below, the combination receiver includes a ***first differential amplifier circuit*** (light blue) that ***combines*** said down-converted in-phase baseband signal portion (red portion) with said down-converted inverted in-phase baseband signal portion (green portion) and outputs a first channel down-converted differential in-phase baseband signal (yellow portion).



Combined Receiver (using circuit of TI-1021/1022)

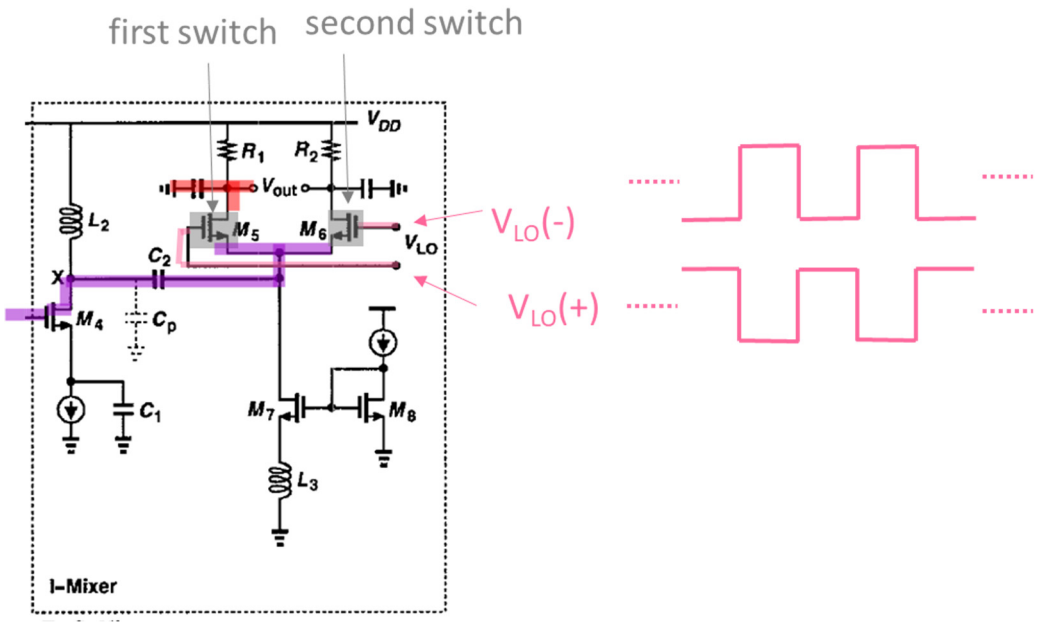
246. The first differential amplifier circuit (light blue) combines the down-converted in-phase baseband signal portion (red portion) with the down-converted inverted in-phase baseband signal portion (green portion) because each of the two complementary signal components at the output (i.e., $V_o(+)$ and $V_o(-)$) is a result of both of the two complementary signal components at the input (i.e., $V_i(+)$ and $V_i(-)$). As illustrated. $V_o(+) = A \cdot (V_i(+) - V_{in-})/2$, and $V_o(-) = -A \cdot (V_i(+) - V_i(-))/2$, where A is the amplification factor. Thus, each of the output component combines both the input components. Moreover, a POSITA would have understood that a single-ended amplifier was usually used to generate the output signal off-chip, and would have found it obvious to use a singled-ended amplifier, as needed.

247. Accordingly, my opinion is that the combination receiver renders obvious claim 1.

3. Claim 5: The system of claim 1, wherein the first switch is on for less than one-half cycle of the modulated carrier signal..

248. The combination system teaches claim 2. §§XI.C.1, X.C-D.

249. In the combination receiver, the first switch is on for less than one-half cycle of the modulated carrier signal (V_{RF}). As explained *supra* §§X.C, XI,C.1, the first switch (M_5) turns on when $V_{LO}(+)$ is substantially larger than $V_{LO}(-)$, and the second switch (M_6) turns on when $V_{LO}(-)$ is substantially larger than $V_{LO}(+)$. As annotated below, $V_{LO}(+)$ and $V_{LO}(-)$ are complementary components of V_{LO}, a differential signal.



TI-1017, Fig. 2 (annotated)

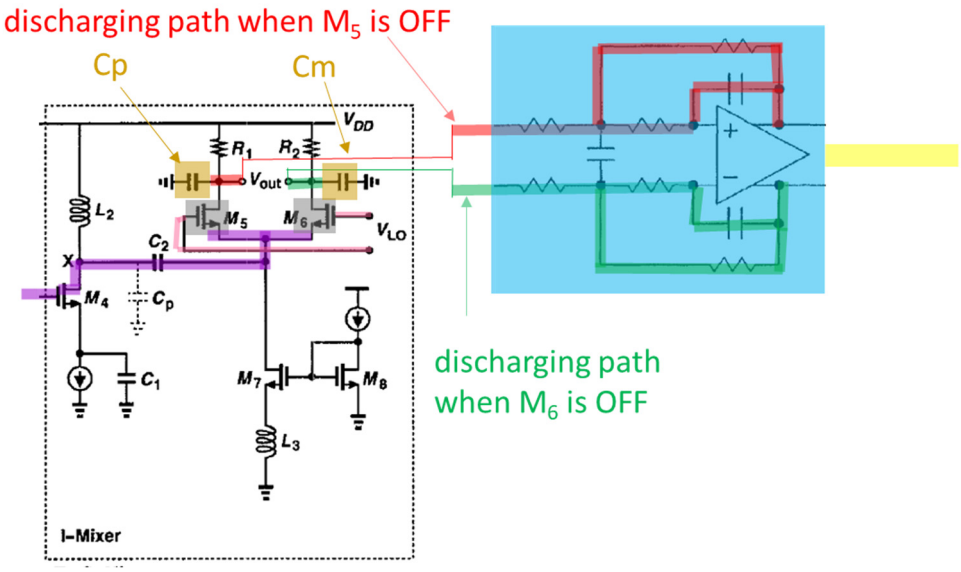
250. As a direct conversion receiver, the oscillating frequency of V_{LO} is nominally the same as the carrier frequency of the input RF signal. As a result of transistor switching time, the period for each switch to be turned on is less than one-half cycle of the modulated carrier signal (i.e., input RF signal).

4. Claim 8: The system of claim 1, wherein the first and second control signals each control a charging and discharging cycle of their respective energy storage element by respectively controlling the first and second switching devices so that for each switching device said portion of energy that is distinguishable from noise is transferred to the respective storage element when the switch is on during the charging cycle, and a portion of the transferred energy is discharged during the discharging part of the cycle for each respective switching device when the switching device is off.

251. The combination receiver teaches the added element of claim 8. §§XI.C.1, X.C-D.

252. In the combination system receiver, the first and second control signals (pink) each control a charging and discharging cycle for respective energy storage element (brown) by respectively controlling the first and second switches (gray). *Supra* XI.C.2(1[b], 1[d]). Specifically, for each switch (gray), the portion of energy that is distinguishable from noise is transferred to the respective storage element (brown) when the switch is on during the charging cycle. *Id.* When the switch (gray) is off (i.e., OPEN), a portion of the transferred energy (e.g., charge accumulated) is discharged, as annotated below for one switch. Cp (brown) also discharges via R_1

and Cm (brown) also discharges via R_2. Each capacitor is coupled to the input impedance of the fully differential amplifier, which is low and typically in the kilo ohm range, and as a result, the circuit coupling to each capacitor is leaky and discharging is expected.



Combination Receiver (using circuit of TI-1021/TI-1022)

5. Claim 9: ***The system of claim 8, wherein for each respective storage element, the energy discharged during any given discharge cycle is not completely discharged, with the remaining undischarged energy from the given discharge cycle becoming an initial condition for the next charging cycle.***

253. The combination system teaches claim 9. §§XI.C.1, X.C-D.

254. In the combination receiver, for each storage device (capacitor in brown), the energy discharged during any given discharge cycle is not completely discharged. "As the capacitors discharge through resistive circuitry, the voltage

across each capacitor, and, therefore, the charge stored on each capacitor discharges proportionally to $e^{-t/RC}$, where t is time, C is the capacitance, and R is the equivalent resistance through which the capacitor is discharged. While $e^{-t/RC}$ decreases with time, it never gets to zero, i.e., $e^{-t/RC} > 0$ for all t, so the capacitor never fully discharges."

6. Claim 11: The system of claim 1, wherein the frequencies of the first and second apertures have periods that are two (2) percent or greater of the modulated carrier signal's period.

255. The combination receiver teaches claim 11. §§XI.C.1, X.C-D.

256. Similar to claim 5, the frequencies of the first and second apertures (i.e., respective periods during which the first and second switches are closed to generate in-phase baseband signal and in-phase inverted baseband signal) have periods that are ***two (2) percent or greater*** (e.g., less than and close to 50%) of the modulated carrier signal's period.

7. Claim 12: *The system of claim 1, wherein the frequencies of the first and second apertures have periods that are five (5) percent or greater of the modulated carrier signal's period.*

257. The combination receiver teaches claim 12. §§XI.C.1, X.C-D.

258. Similar to claim 5, the frequencies of the first and second apertures (i.e., respective periods during which the first and second switches are closed to generate in-phase baseband signal and in-phase inverted baseband signal) have periods that

are ***five (5) percent or greater*** (e.g., less than and close to 50%) of the modulated carrier signal's period.

8. Claim 13: ***The system of claim 1, wherein the frequencies of the first and second apertures have periods that are ten (10) percent or greater of the modulated carrier signal's period.***

259. The combination receiver teaches claim 13. §§XI.C.1, X.C-D.

260. Similar to claim 5, the frequencies of the first and second apertures (i.e., respective periods during which the first and second switches are closed to generate in-phase baseband signal and in-phase inverted baseband signal) have periods that are ***ten (10) percent or greater*** (e.g., less than and close to 50%) of the modulated carrier signal's period.

9. Claim 14: ***The system of claim 1, wherein the frequencies of the first and second apertures have periods that are twelve and a half (12.5) percent or greater of the modulated carrier signal.***

261. The combination receiver teaches claim 14. §§XI.C.1, X.C-D.

262. Similar to claim 5, the frequencies of the first and second apertures (i.e., respective periods during which the first and second switches are closed to generate in-phase baseband signal and in-phase inverted baseband signal) have periods that are ***twelve and a half (12.5) percent or greater*** (e.g., less than and close to 50%) of the modulated carrier signal's period.

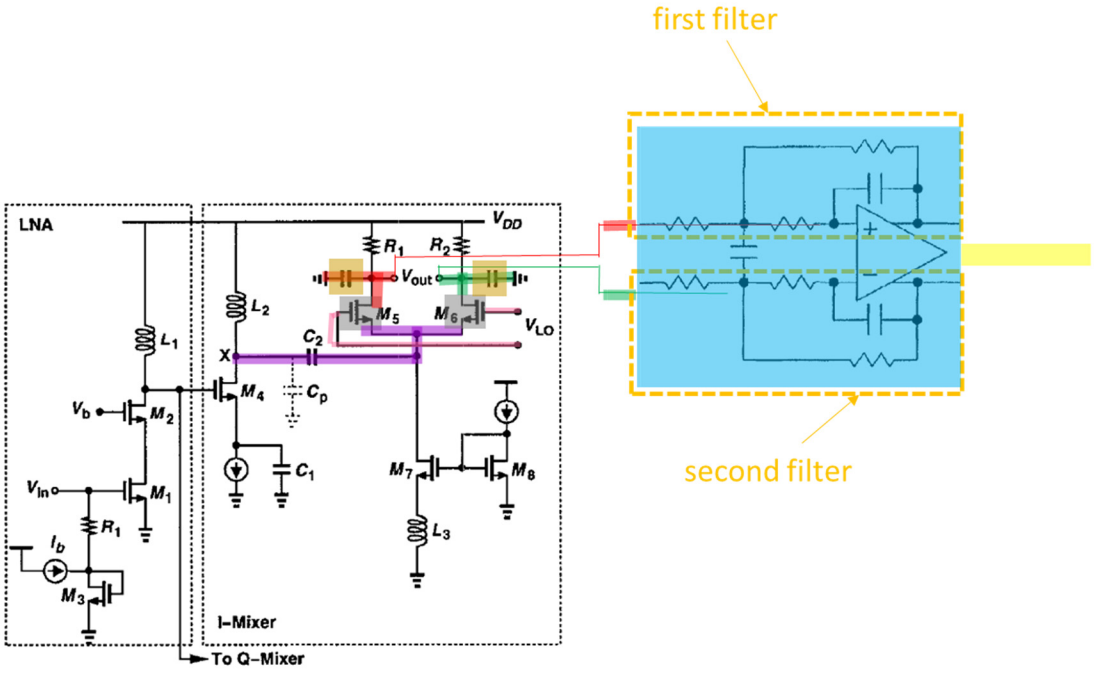
10. Claim 15: ***The system of claim 1, further comprising:***

a first filter that filters said down-converted in-phase baseband signal portion; and

a second filter that filters said down-converted inverted in-phase baseband signal portion.

263. The combination receiver teaches claim 15. §§XI.C.1, X.C-D.

264. In the combination receiver, the differential amplifier circuits include a ***first filter*** (orange box) that filters the down-converted in-phase baseband signal portion (red), and a ***second filter*** (orange box) that filters the down-converted inverted in-phase baseband signal portion (green), as annotated below. §§XI.C.2 (1[c] (in-phase baseband), 1[e] (inverted in-phase baseband), [1g] (differential amplifier circuit).



Combined Receiver (using circuit of TI-1021/TI-1022)

11. Claim 16: The system of claim 15, wherein the first and second filters each comprise a low-pass filter.

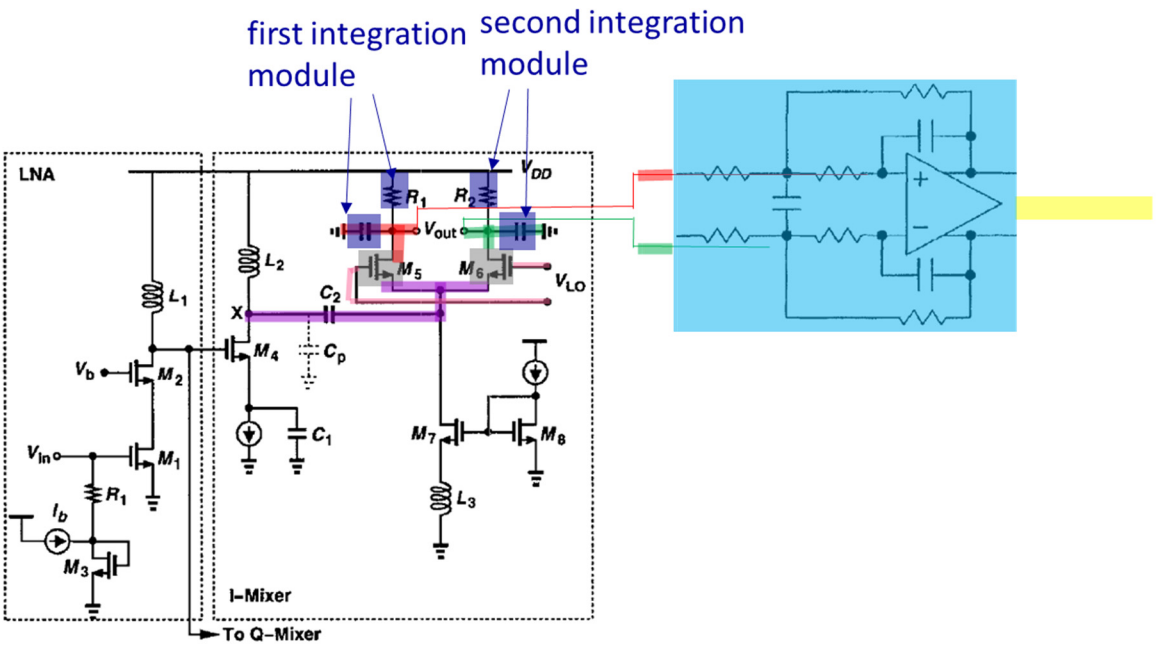
265. The combination receiver teaches claim 16. §§XI.C.1, X.C-D.

266. In the combination receiver, the first and second filters (orange boxes annotated above) each comprise a low-pass filter. TI-1021, 7:7-29 (discussing cut-off frequency); TI-1022, 11 (same). Here, the RC network forms a classical low-pass filter, in similar manner as presented by ParkerVision's infringement chart. TI-1012

12. Claim 17: The system of claim 1, wherein said portions of transferred energy from each of the first and second switch which are integrated over time to accumulate said portions of transferred energy are integrated by a separate integration module coupled to the output of each said first and second switch.

267. The combination receiver teaches claim 16. §§XI.C.1, X.C-D.

268. As further annotated below, in the combination receiver, portions of transferred energy from each of ***the first and second switch*** (gray) which are integrated over time to accumulate said portions of transferred energy are integrated by ***a separate integration module*** (brown) coupled to the output of each said ***first*** (M_5) and ***second*** (M_6) switch.



Combined Receiver (using Macnally's circuit for baseband processing)

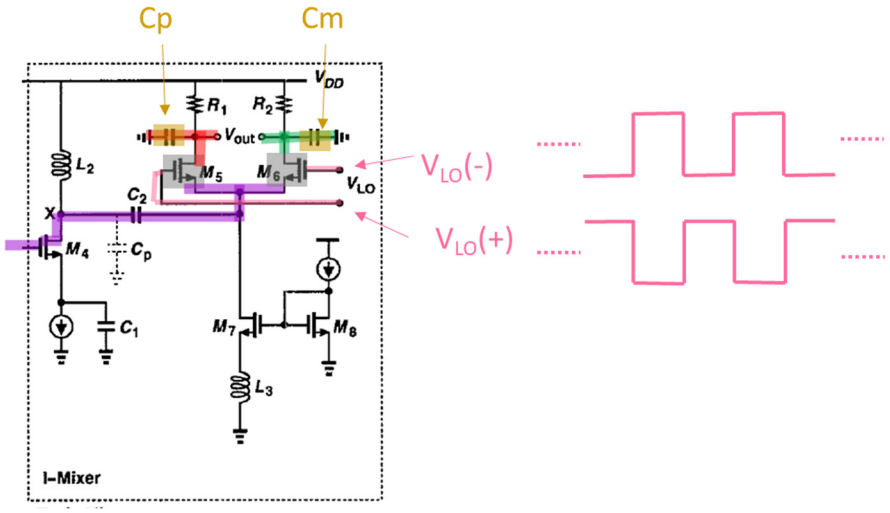
269. In operation, each ***separate integration module*** (brown) integrates portions of transferred energy from the coupled-to switch (M_5 or M_6) to accumulate the portions of transferred energy, as commonly performed by RC network. This is similar to Tayloe's integrator using capacitor-resister pair.

13. Claim 18: ***The system of claim 1, wherein said first and second storage elements are capacitive storage circuits, and wherein said portions of transferred energy from each of the first and second switch which are integrated over time to accumulate said portions of transferred energy are integrated by the capacitive storage circuits as they accumulate charge during successive sampling apertures.***

270. The combination receiver teaches claim 16. §§XI.C.1, X.C-D.

271. As further annotated below, in the combination receiver, portions of transferred energy from each of the ***first*** (M_5) and ***second*** (M_6) ***switch*** (gray) which

are integrated over time to accumulate said portions of transferred energy are integrated by the ***capacitive storage circuits*** (capacitors Cp and Cm (brown)) as they accumulate charge during ***successive sampling apertures*** (successive windows when the coupled-to switch is ON as controlled by $V_{LO}(+)$ and $V_{LO}(-)$ (pink)).



TI-1017, Fig. 2 (annotated)

272. In operation, the capacitive storage circuits (brown) integrate portions of transferred energy from the coupled-to switches (M_5 and M_6) to accumulate the portions of transferred energy during successive windows when the coupled-to switch is ON, consistent with the '528 Specification. TI-1001, Fig. 197 (first processing module 19702), 176:61-177:15 ("… a first capacitor stor[es] I output signal"). This aspect of integrating capacitor is similar to Tayloe.

14. Claim 19

273. The combination receiver teaches claim 19. §§XI.C.1, X.C-D.

274. The limitations of claim 19 are nearly identical to those of claims 1 by adding a duplicative section. Therefore, my analysis for claim 19 refers back to my analysis of those claims and addresses differences.

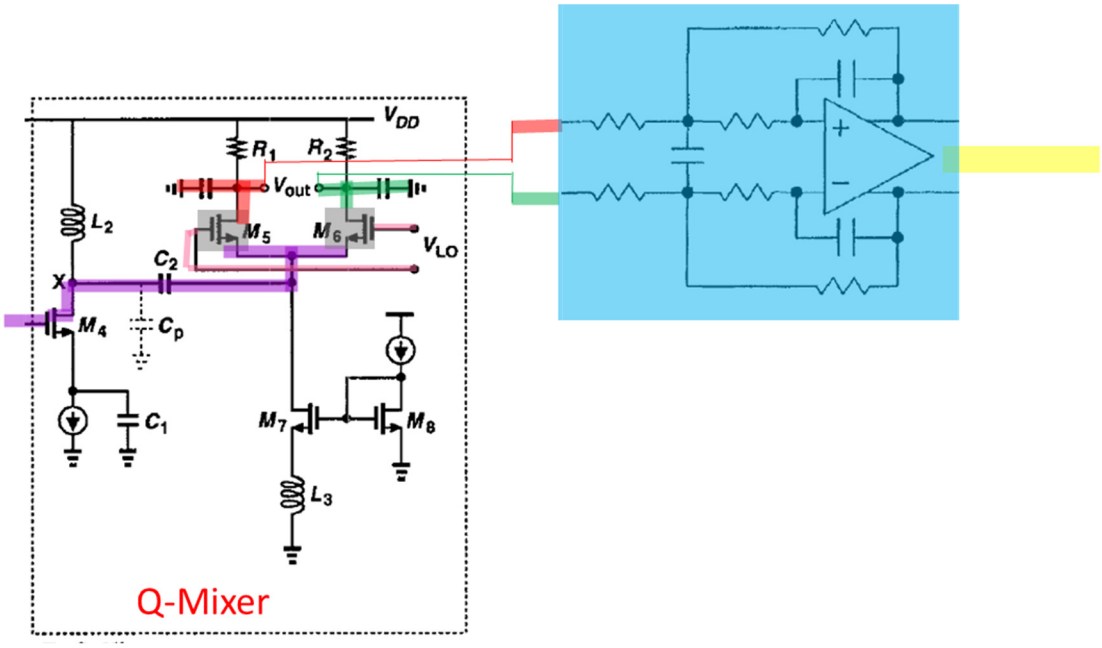
a) Element 19(a): The system of claim 1, further comprising:

275. The combination receiver teaches element 19(a). *See* §§XI.1, X.C-D.

b) Element 19(b): a third switch coupled to a third control signal which comprises a sampling aperture with a specified frequency, wherein the third switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal as an output of said third switch during the sampling aperture of the third control signal;

276. The combination receiver teaches element 19(b). *See* §§XI.C.1, X.C-D.

277. As further annotated below, the combination system provides a quadrature (Q) mixer (similar to the I-mixer) that includes a ***third switch*** (M_5 (gray)) coupled to a ***third control signal*** (V_{LO} (+) (pink)) which comprises a ***sampling aperture*** (e.g., on-duration of the third switch) with a ***specified frequency*** (i.e., a toggling rate of the third switch). TI-1017, 113, Fig. 2 (Q-mixer instantiated below).



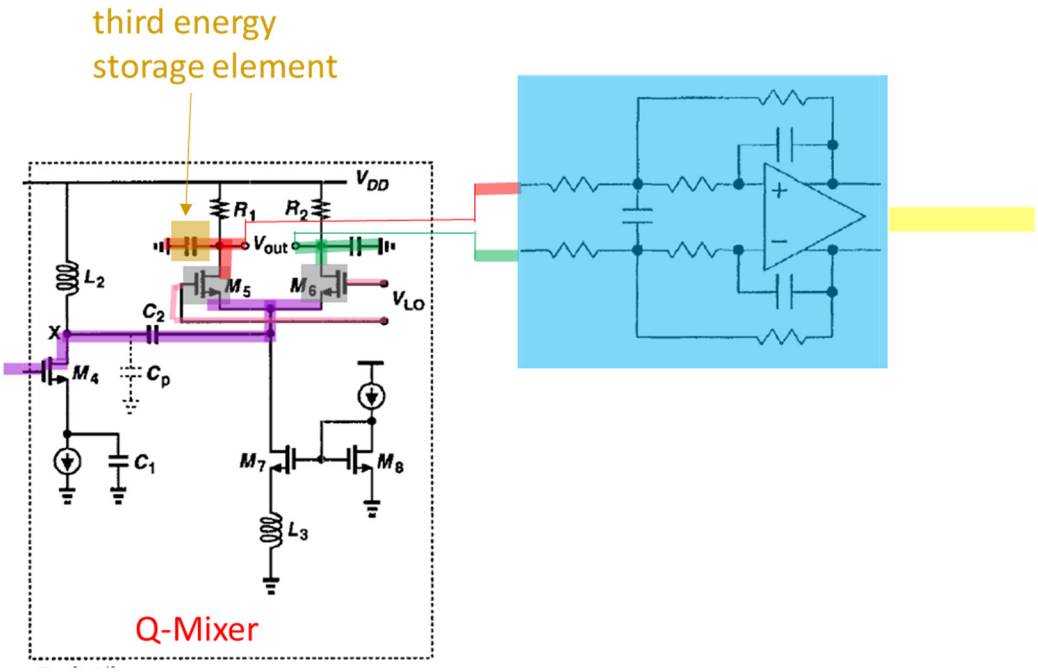
Combination Receiver (using circuits of TI-1021/TI-1022)

278. The third switch (M_5 (gray)) is on and ***a portion of energy*** that is distinguishable from noise is transferred ***from the modulated carrier signal*** (RF input signal (purple)) ***as an output*** (red) of said switch during the sampling aperture (on-duration) of the third control signal. TI-1017, 113, Fig. 2; §§XI.C.1, III.A.2 (element 1[b] including "energy distinguishable from noise is transferred").

> c) *Element 19(c): a third energy storage element that stores the transferred energy from the modulated carrier signal and outputs a down-converted quadrature-phase baseband signal portion of said modulated carrier signal;*

279. The combination receiver teaches element 19(c). *See* §§XI.C.1, X.C-D.

280. As further annotated below, the combination receiver includes ***a third energy storage element*** (e.g., capacitor (brown)) that ***stores*** the transferred energy from the modulated carrier signal (purple) and ***outputs a down-converted quadrature-phase baseband signal portion*** (red portion feeding into Macnally's circuit (light blue)) of said modulated carrier signal (purple). TI-1017, 113, Fig. 2; TI-1021/TI-1022, Fig. 3.



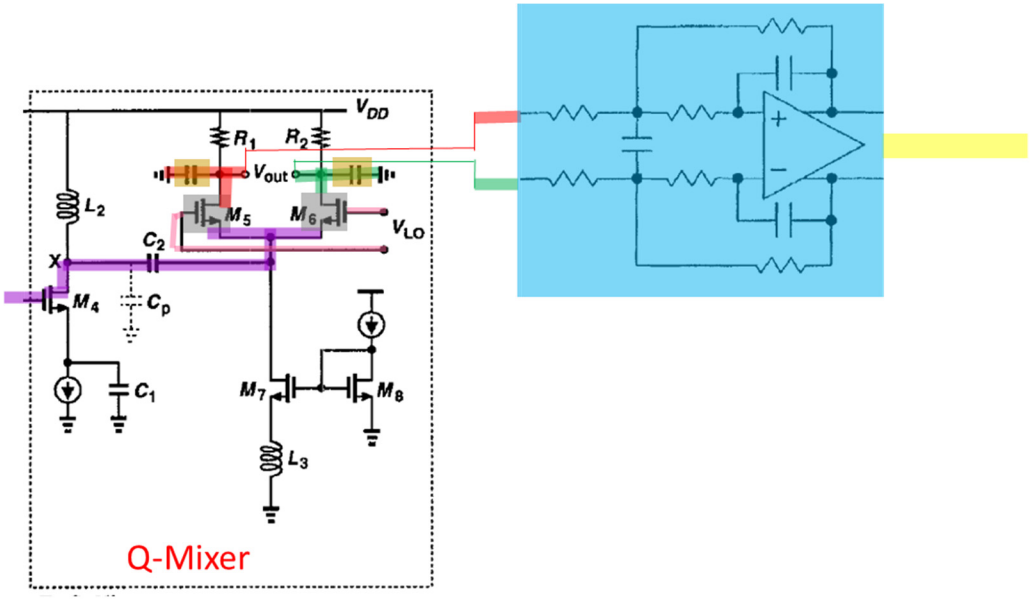
Combination Receiver (using circuit of TI-1021/TI-1022)

281. In accordance with the proposed claim construction *supra* §IX, Razavi's capacitor (brown) "***stores non-negligible amounts of energy from an input EM signal,***" i.e., the RF input signal. §X1.C.1 (1[c]). Notably, each capacitor has a low impedance load when using Macnally's differential amplifier circuit.

d) Element 19(d): a fourth switch coupled to a fourth control signal which comprises a sampling aperture with a specified frequency, wherein the fourth switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal as an output of said fourth switch during the sampling aperture of the fourth signal;

282. The combination receiver teaches element 19(d). *See* §§XI.C.1, X.C-D.

283. As further annotated below, the combination system provides a quadrature (Q) mixer (similar to the I-mixer) that includes a ***fourth switch*** (M_6 (gray)) coupled to a ***fourth control signal*** (V_{LO}(-)(pink)) which comprises a ***sampling aperture*** (e.g., on-duration of the fourth switch) with a ***specified frequency*** (i.e., a toggling rate of the fourth switch). TI-1017, 113, Fig. 2 (Q-mixer instantiated below); §XI.C.1.



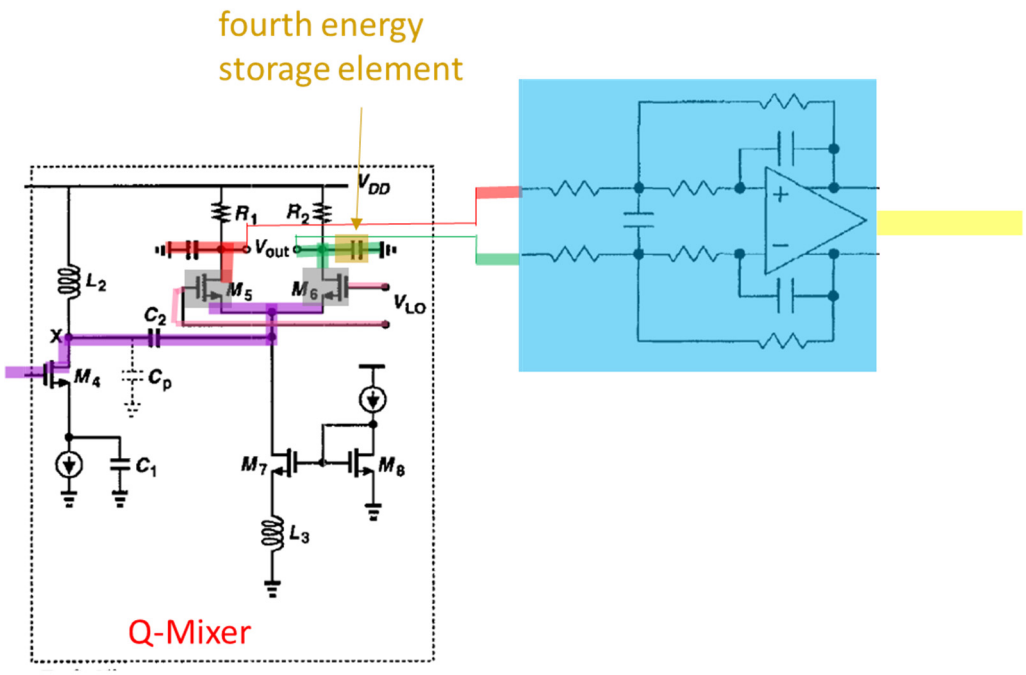
Combination Receiver (using circuits of Macnally)

284. The fourth switch (M_6 gray) is on and ***a portion of energy*** that is distinguishable from noise is transferred ***from the modulated carrier signal*** (RF input signal (purple)) ***as an output*** (red) of said switch during the sampling aperture (on-duration) of the fourth control signal. TI-1017, 113, Fig. 2; §§XI.C.1, XI.A.2 (element 1[b] including "energy distinguishable from noise is transferred").

1. *Element 19(e): a fourth energy storage element that stores the transferred energy from the modulated carrier signal and outputs a down-converted differential quadrature-phase baseband signal portion of said modulated carrier signal*

285. The combination receiver teaches element 19(e). See §§XI.C.1, X.C-D.

286. As further annotated below, the combination receiver includes ***a fourth energy storage element*** (e.g., capacitor (brown)) that ***stores*** the transferred energy from the modulated carrier signal (purple) and ***outputs a down-converted quadrature-phase baseband signal portion*** (green portion feeding into Macnally's circuit) of said modulated carrier signal (purple). TI-1017, 113, Fig. 2; TI-1021/TI-1022, Fig. 3.



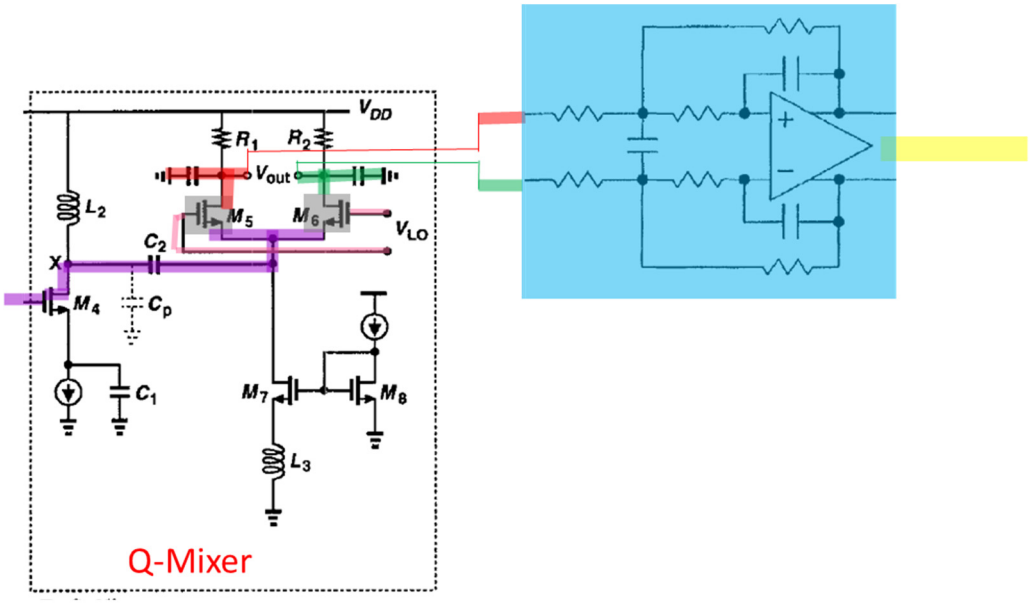
Combination Receiver (using circuit (light blue) of TI-1021/TI-1022)

287. In accordance with claim construction proposal supra §IX, Razavi's capacitor (brown) likewise "stores non-negligible amounts of energy from an input EM signal," i.e., the RF input signal. §XI.C.2 (1[c]). Each capacitor has a low impedance load when using Macnally's differential amplifier circuit.

> e) *Element 19(f): wherein the portions of transferred energy from each of the third and fourth switch are integrated over time to accumulate said portions of transferred energy from which said down-converted quadrature-phase baseband signal portion and said down-converted differential quadrature-phase baseband signal portion are derived; and;*

288. The combination receiver teaches element 19(f). See §§XI.C.1, X.C-D.

289. As further annotated below, in the combination receiver, ***the portions of transferred energy*** from each of the third and fourth switch ***are integrated*** over time to accumulate said portions of transferred energy ***from which said down-converted quadrature-phase baseband signal portion*** (red portion feeding into Macnally's circuit (light blue)) ***and said down-converted differential quadrature-phase baseband signal portion*** (green portion feeding into Macnally's circuit (light blue)) ***are derived***.



Combination Receiver (using circuit (light blue) of TI-1021/TI-1022)

1. *Element 19(g): a second differential amplifier circuit that combines said down- converted quadrature-phase baseband signal portion with said down-converted differen-tial quadrature-phase baseband signal portion and outputs a second channel down-converted differential quadrature-phase baseband signal.*

290. The combination receiver teaches element 19(f). See §§XI.C.1, X.C-D.

291. As further annotated below, the combination system includes a second differential amplifier circuit (light blue) that combines said down-converted quadrature-phase baseband signal portion (red portion feeding into Macnally's circuit) with said down-converted differential quadrature-phase baseband signal portion (green portion feeding into Macnally's circuit) and outputs a second channel down-converted differential quadrature-phase baseband signal (yellow). TI-1017, 113, Figs. 2, 4-5; TI-1021/TI-1022, Fig. 3; §III.A.5 (1[g]). In §VI.C, I have provided detailed explanation that a fully differential amplifier generates differential output signal having two complementary components, each combining the two complementary components of the differential input signal.

292. Accordingly, my opinion is that the combination receiver renders obvious claim 19.

15. Claim 23: The system of claim 19, wherein the third switch is on for less than one-half cycle of the modulated carrier signal.

293. The combination receiver teaches claim 23. See §§XI.C.1, X.C-D.

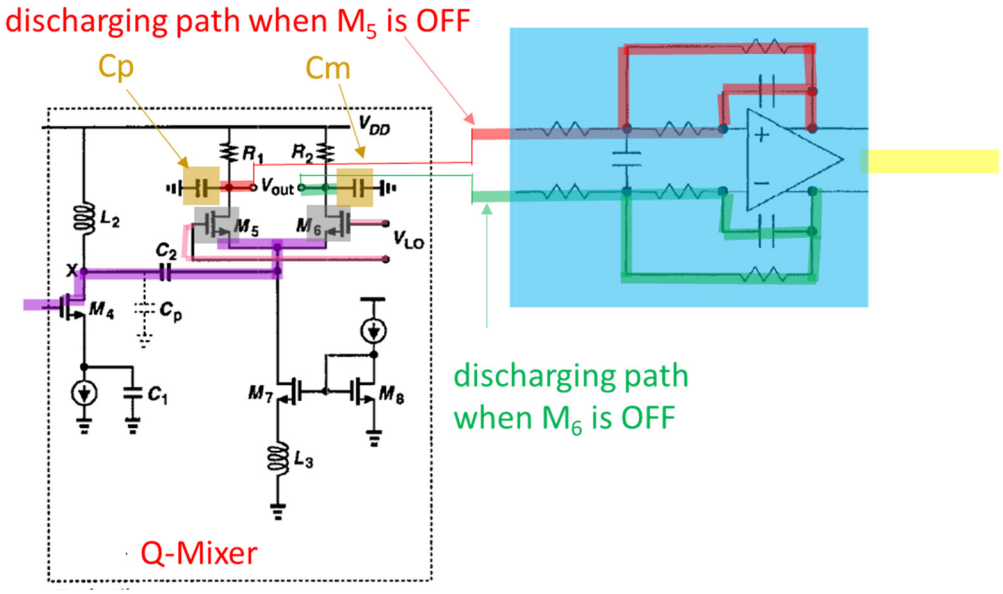
294. In the combination receiver, Razavi further provides a quadrature (Q) mixer configured in the same manner as the in-phase mixer. Like the first switch on the in-phase mixer, the third switch on the Q-mixer of the combination receiver is on for less than one-half cycle of the modulated carrier signal. §XI.C.2 (claims 5 and 19).

16. Claim 26: ***The system of claim 19, wherein the third and fourth control signals each control a charging and discharging cycle of their respective third and fourth energy storage element by respectively controlling the third and fourth switching devices so that for each third and fourth switching device a portion of energy that is distinguishable from noise is transferred to the respective third and fourth storage element when the respective switch is on during the charging cycle, and a portion of the transferred energy is discharged during the discharging part of the cycle for each respective third and fourth switching device when the respective switching device is off.***

295. The combination receiver teaches claim 26. See §§XI.C.1, X.C-D.

296. Similar to claim 8, in the combination receiver with the quadrature (Q) mixer, the third and fourth control signals (V_{LO}(+) and V_{LO}(-) pink) each control a charging and discharging cycle for respective energy storage element (Cp and Cm (brown)) by respectively controlling the third and fourth switches (M_5 and M_6 (gray)). *Supra* §§XI.C.1, 2 (8, 19[b], 19[d]). Specifically, for each switch (gray), the portion of energy that is distinguishable from noise is transferred to the respective storage element (brown) when the switch is on (i.e., CLOSED) during the charging

cycle. *Id.* When the switch (gray) is off (i.e., OPEN), a portion of the transferred energy (e.g., charge accumulated) is discharged, as annotated below. The discharging path also involves passing through each coupled-to resister (e.g., R_1 and R_2).



Combination Receiver (Q-mixer (TI-1017) coupled to circuit (TI-1021/TI-1022))

17. Claim 27: The system of claim 26, wherein for each respective energy storage element, the energy discharged during any given discharge cycle is not completely discharged, with the remaining undischarged energy from the given discharge cycle becoming an initial condition for the next charging cycle.

297. The combination receiver teaches claim 27. See §§XI.C.1, X.C-D.

298. Similar to claim 9, in the combination receiver with the quadrature (Q) mixer, for each storage device (capacitor Cp and Cm (brown as annotated above)), the energy discharged during any given discharge cycle is not completely

discharged. The remaining undischarged energy from the given discharge cycle thus becomes an initial condition for the next charging cycle (when the switch is closed).

18. Claim 28: The system of claim 19, wherein the frequencies of the third and fourth apertures have periods that are two (2) percent or greater of the modulated carrier signal's period.

299. The combination receiver teaches claim 28. See §§XI.C.1, X.C-D.

300. Similar to claim 11, in the combination receiver with the quadrature (Q) mixer, the frequencies of the third and fourth apertures (i.e., respective periods during which the third and fourth switches are closed to generate the quadrature baseband signal and the quadrature inverted baseband signal) likewise have periods that are **two (2) percent or greater** (e.g., less than but close to 50%) of the modulated carrier signal's period. §XI.C.1-2 (claims 11, 19)

19. Claim 30: The system of claim 19, wherein the frequencies of the third and fourth apertures have periods that are five (5) percent or greater of the modulated carrier signal's period.

301. The combination receiver teaches claim 30. See §§XI.C.1, X.C-D.

302. Similar to claim 11, in the combination receiver with the quadrature (Q) mixer, the frequencies of the third and fourth apertures (i.e., respective periods during which the third and fourth switches are closed to generate the quadrature baseband signal and the quadrature inverted baseband signal) likewise have periods

that are **five (5) percent or greater** (e.g., less than but close to 50%) of the modulated carrier signal's period. §XI.C.1-2 (claims 11, 19).

20. Claim 31: The system of claim 19, wherein the frequencies of third and fourth apertures have periods that are ten (10) percent or greater of the modulated carrier signal's period.

303. The combination receiver teaches claim 31. See §§XI.C.1, X.C-D.

304. Similar to claim 11, in the combination receiver with the quadrature (Q) mixer, the frequencies of the third and fourth apertures (i.e., respective periods during which the third and fourth switches are closed to generate the quadrature baseband signal and the quadrature inverted baseband signal) likewise have periods that are ***twelve and a half* (12.5) percent or greater** (e.g., less than but close to 50%) of the modulated carrier signal's period. §XI.C.1-2 (claims 11, 19).

21. Claim 32: The system of claim 19, wherein the frequencies of third and fourth apertures have periods that are twelve (12.5) percent or greater of the modulated carrier signal's period.

305. The combination receiver teaches claim 32. See §§XI.C.1, X.C-D.

306. Similar to claim 11, in the combination receiver with the quadrature (Q) mixer, the frequencies of the third and fourth apertures (i.e., respective periods during which the third and fourth switches are closed to generate the quadrature baseband signal and the quadrature inverted baseband signal) likewise have periods that are ***twelve and a half* (12.5) percent or greater** (e.g., less than but close to 50%) of the modulated carrier signal's period. §XI.C.1-2 (claims 11, 19).

22. Claim 33: ***The system of claim 19, further comprising:***

a first filter that filters said down-converted in-phase baseband signal portion;

a second filter that filters said down-converted inverted in-phase baseband signal portion;

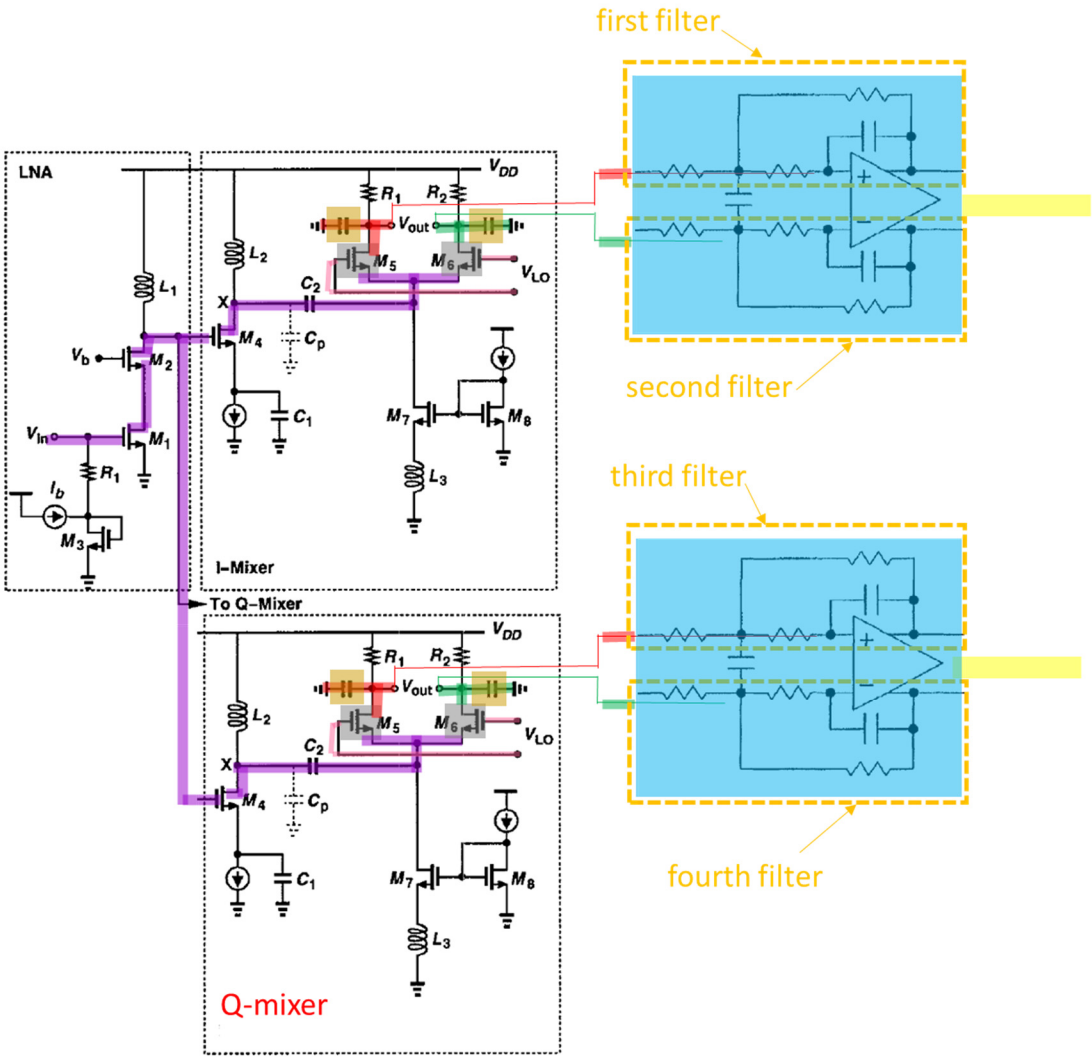
a third filter that filters said down-converted quadrature-phase baseband signal portion;

a fourth filter that filters said down-converted inverted quadrature-phase baseband signal portion.

307. The combination receiver teaches claim 33. See §§XI.C.1, X.C-D.

308. As explained above for claim 15, the combination receiver has an in-phase (I) mixer coupled to a ***first filter*** (orange box) that filters the down-converted in-phase baseband signal portion (red), and a ***second filter*** (orange box) that filters the down-converted inverted in-phase baseband signal portion (green).

309. As annotated below, the combination receiver also has a quadrature (Q) mixer coupled to a ***third filter*** (orange box) that filters the down-converted quadrature-phase baseband signal portion (red), and a ***fourth filter*** (orange box) that filters the down-converted inverted quadrature baseband signal portion (green). §§III.C.1-2, §III.C.3 (19[c] (quadrature-phase baseband), 19[e] (inverted quadrature-phase baseband), 19[g] (differential amplifier circuit).



Combination Receiver (I-mixer/Q-mixer of TI-1017, circuits of TI-1021/TI-1022)

23. Claim 34: The system of claim 33, wherein the first, second, third, and fourth filters each comprise a low-pass filter.

310. The combination receiver teaches claim 34. See §§XI.C.1, X.C-D.

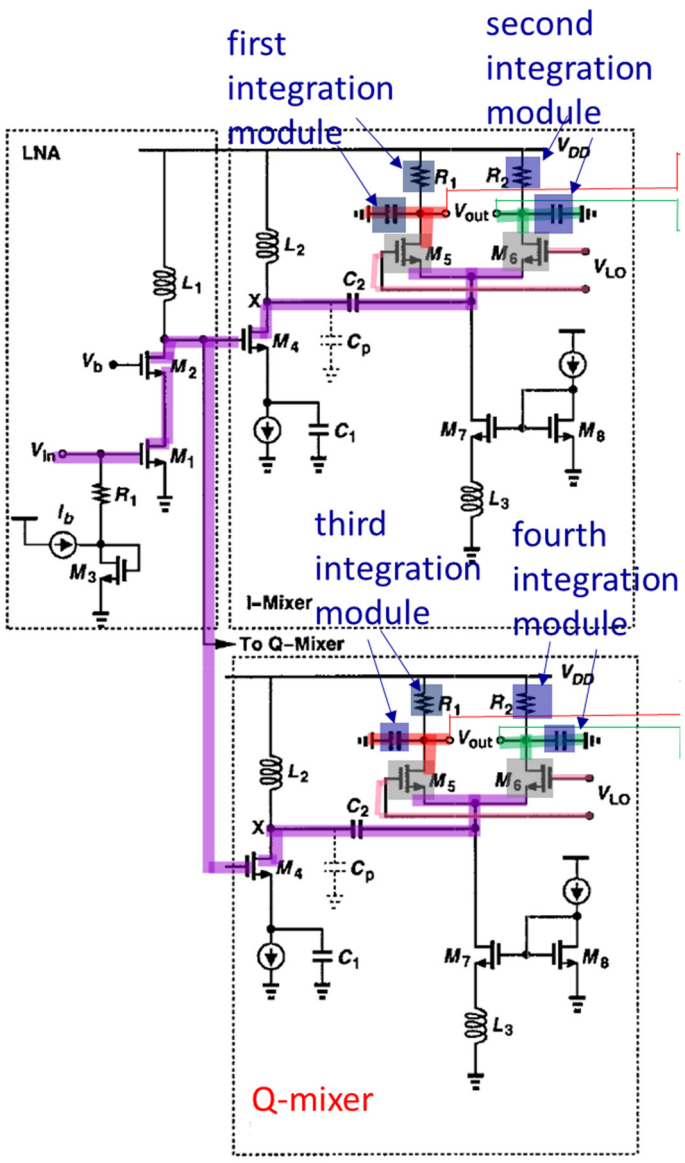
311. As explained under claim 16, the first and second filters each comprise a low-pass filter. Further, the third and fourth filters each comprise a low-pass filter. §§XI.C.1-2; TI-1021, 7:7-29 (discussing cut-off frequency); TI-1022, 11 (same).

Significantly, the RC network in conjunction with an amplifier forms a classical low-pass filter, as relied on by ParkerVision's infringement chart. TI-1012.

24. Claim 35: The system of claim 19, wherein said portions of transferred energy from each of the first, second, third and fourth switch which are integrated over time to accumulate said portions of transferred energy are integrated by a separate integration module coupled to the output of each said first, second, third and fourth switch respectively.

312. The combination receiver teaches claim 35. See §§XI.C.1, X.C-D.

313. Similar to claim 17, which I have explained above, the combination receiver has a separate integration module (separate capacitor-resister pair) coupled to the output of each of the first, second, third (gray), and fourth (gray) switch. TI-1017, Fig. 2. The integration modules are positioned separately on the I-mixer and the Q-mixer.



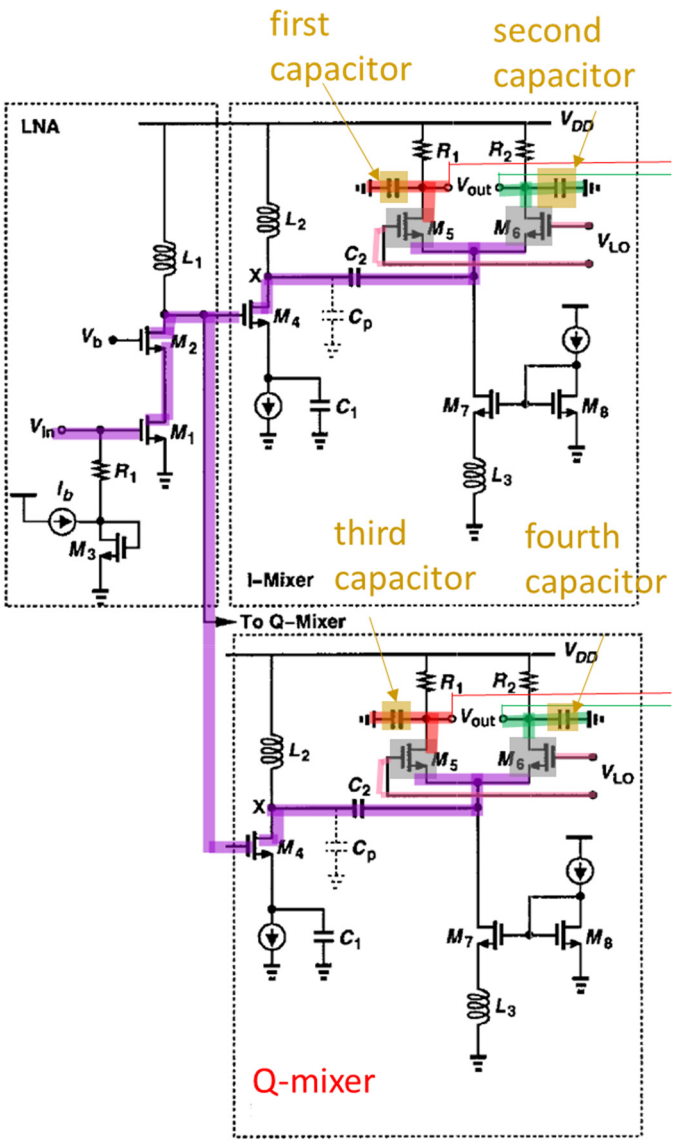
Combination Receiver (zoomed portions of I-mixer/Q-mixer of TI-1017)

314. Each separate integration module integrates the portions of transferred energy from each of the first, second, third, and fourth switch which are integrated over time to accumulate said portions of transferred energy. §XI.C.1; TI-1017, Fig. 2. Both the capacitor and the resister in each separate capacitor-resister pair are involved in charging and hence the integration operation.

25. Claim 36: The system of claim 19, wherein said first, second, third and fourth stor-age elements are capacitive storage circuits, and wherein said portions of trans-ferred energy from each of the first, second, third, and fourth switch which are integrated over time to accumulate said portions of transferred energy are inte-grated by the capacitive storage circuits of the respective first, second, third and fourth storage elements as they accumulate charge during successive sampling apertures..

315. The combination receiver teaches claim 36. See §§XI.C.1, X.C-D.

316. Similar to claim 18, which I have explained above, and as annotated below, in the com-bination receiver, the first, second, third, and fourth storage elements are capacitive elements (i.e., capacitors Cp and Cm on I-mixer and Q-mixer). TI-1017, Fig. 2.



Combination Receiver (zoomed portions of I-mixer/Q-mixer of TI-1017)

317. In the combination receiver, ***the portions of transferred energy from each of the first, second, third, and fourth switch which are integrated over time to accumulate said portions of transferred energy are integrated by the capacitive storage circuits as they accumulate charge during successive sampling apertures*** (e.g., duration of switch closures).

D. Ground 2B – Razavi, Macnally, and Cahn Render Obvious Claims 2-4, 20-22

1. Predictable combination of Imai, Higashi, and Grzesik combination

318. As explained supra §III.B.1, Cahn discloses amplitude modulation, phase modulation, and combined amplitude and phase modulation. TI-1007, 150-51. Razavi reveals receiver design options "depending on … the type of modulation"). TI-1017, 113. Macnally describes an example where "the re-sulting I and Q signals are fed to BFSK demodulator." TI-1021, 7:46-47; TI-1022, 12. Aside from such disclosures, A POSITA would have found it obvious to apply the combination receiver to down-convert a RF signal modulated using these well-known established techniques. Indeed, the application would have been a combination of prior art elements according to known methods to yield predictable results (i.e., ap-plying well-known modulation techniques).

2. Claim 2: *The system of claim 1, wherein said modulated carrier signal includes an amplitude variation*.

319. As explained supra §XI.D.1 and XI.C.1, it would have been obvious for the combination receiver to operate on modulated carrier signal that includes an amplitude variation so that the amplitude of the baseband signal tracks such amplitude variation. TI-1017, Figs. 1-2; TI-1007, 150-51. One example of amplitude modulation is pulse amplitude modulation, known as PAM. *Id.*

3. Claim 3: *The system of claim 1, wherein said modulated carrier signal includes a phase variation*.

320. As explained *supra* §III.D.1 and III.C.1-3, in addition to Macnally's example using phase modulation, (TI-1021, 7:46-47; TI-1022, 12), it would have been obvious for the combination receiver to operate on modulated carrier signal that includes a phase variation so that the down-converted baseband signals track the phase variation. TI-1007, 150-51. One example of phase modulation is frequency shift keying. *Id.*

4. Claim 4: *The system of claim 1, wherein said modulated carrier signal includes a combination of amplitude variation and phase variation.*

321. As explained supra §III.D.1 and III.C.1-3, it would have been obvious for the combination receiver to operate on modulated carrier signal that in-cludes a combination of amplitude and phase variation so that the baseband signals track the combination of amplitude and phase variation. TI-1007, 150-51 (providing one example of combined amplitude and phase modulation).

5. Claim 20: The system of claim 19, wherein said modulated carrier signal includes an amplitude variation.

322. For reasons similar to what I have provided for claim 2, the combination receiver renders obvious claim 20.

6. Claim 21: The system of claim 19, wherein said modulated carrier signal includes a phase variation.

323. For reasons similar to what I have provided for claim 3, the combination receiver renders obvious claim 21.

7. Claim 22: The system of claim 19, wherein said modulated carrier signal includes a phase variation.

324. For reasons similar to what I have provided for claim 4, the combination receiver renders obvious claim 22.

E. Secondary Considerations

325. I am not aware of any evidence regarding secondary considerations of non-obviousness, and ParkerVision did not identify any documentary such evidence in the patent specification, prosecution history, or in related district court complaints. To the extent ParkerVision identifies evidence of secondary considerations at a later point in the proceeding, I reserves the right to address it at that time.

XII. CONCLUSION

326. For the aforementioned reasons, a POSITA would have recognized that a number of predictable prior art combinations (articulated in the grounds above) would have achieved all elements of claims 1-5, 8, 9, 11-23, 26, 27, and 29-36 of the '528 Patent are invalid in view of the prior art, for the reasons discussed above.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on the information and belief are believed to be true; I declare under penalty of perjury that the foregoing is true and correct, and understand that willful false statements and the like are punishable by fine or imprisonment, or both pursuant to 18 U.S.C. 1001.

Dated: May 17, 2024 By: /Dr. Ian Galton/

Dr. Ian Galton

APPENDIX A

Ian Galton

Education

Brown University, Providence, RI	**ScB** in Electrical Engineering	1984
California Institute of Technology, Pasadena, CA	**MS**/**PhD** in Electrical Engineering	1989/1992

Employment

Professor of Electrical Engineering, **University of California at San Diego**, La Jolla, CA	7/02 – present
Associate Professor of Electrical Engineering, **University of California at San Diego**, La Jolla,	11/96 – 6/02
Assistant Professor of Electrical Engineering, **University of California at Irvine**, Irvine, CA	7/92 – 10/96
Design Engineer, **Acuson, Inc.**, Mountain View, CA	8/86 – 9/88
Design Engineer, **Mead Data Central**, Menlo Park, CA	2/85 – 8/86
Design Engineer, **Mindset Corporation**, Sunnyvale, CA	7/84 – 1/85

UCSD Research Overview

Ian Galton manages the Integrated Signal Processing Group at the University of California, San Diego (UCSD). The group develops enabling technology for highly-integrated, high-performance, low-cost, communication systems. The research involves the invention, development, analysis, and proof-of-principle integrated circuit (IC) implementation of key communication system blocks such as data converters and frequency synthesizers. The emphases of the research are on the development of new digital signal processing techniques and new digital-like analog circuits that exploit the strengths of advanced IC technology to mitigate the effects of non-ideal analog circuit behavior in mixed-signal and radio frequency ICs.

Selected Accomplishments, Activities, Honors, and Awards

- Author or co-author of ~100 scientific papers in peer-reviewed academic journals and conferences
- Inventor or co-inventor on ~22 U.S. Patents
  Holder of the "Skyworks Endowed Chair in High Performance Communications Devices and Circuits"
- Fellow of the Institute of Electrical and Electronics Engineers (IEEE)
- Recipient of the 2015-2016 and the 2016-2017 UCSD Electrical and Computer Engineering Department "Best Graduate Teacher" award
- Co-recipient of the 2015 IEEE International Solid-State Circuits Conference (ISSCC) Lewis Winner Award
- Recipient of the Brown Engineering Alumni Medal, 2012
- Co-recipient of the 2008 IEEE Transactions on Circuits and Systems Darlington Award
- Co-recipient of the 2008 IEEE ISSCC Jack Kilby Award
- Member of the IEEE Solid-State Circuits Society Distinguished Lecturer Program, 2007-2010
- Organizer of the IEEE ISSCC Short Courses, 2007-2010
- Member of the IEEE ISSCC Technical Program Committee, 2005-2011
- Recipient of the 2005-2006 UCSD Electrical and Computer Engineering Department "Best Teacher Award"
- IEEE Solid State Circuits Society Administrative Committee, 2002-2005
- IEEE Circuits and Systems Society Board of Governors, 1998-2001, 2002-2005
- Editor-in-Chief of the *IEEE Transactions on Circuits and Systems II: Analog to Digital Signal Processing*, 2001-2003
- Board of Directors of innoCOMM Wireless, San Diego, CA, through its 2001 purchase by National Semiconductor Corporation
- Technical consultant and/or Technical Advisory Board member for several semiconductor and communications companies
- Instructor in over 80 industry-oriented short courses on the design of data converters, PLLs, and wireless transceivers at IEEE conferences and through Mead Education
- Recipient of the California Institute of Technology Charles Wilts PhD Thesis Prize, 1992

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