DECLARATION OF JUNE ANN MUNFORD

1. My name is June Ann Munford. I am over the age of 18, have personal knowledge of the facts set forth herein, and am competent to testify to the same.

2. I earned a Master of Library and Information Science (MLIS) from the University of Wisconsin-Milwaukee in 2009. I have over ten years of experience in the library/information science field. Beginning in 2004, I have served in various positions in the public library sector including Assistant Librarian, Youth Services Librarian and Library Director. I have attached my Curriculum Vitae as Appendix CV.

3. During my career in the library profession, I have been responsible for materials acquisition for multiple libraries. In that position, I have cataloged, purchased and processed incoming library works. That includes purchasing materials directly from vendors, recording publishing data from the material in question, creating detailed material records for library catalogs and physically preparing that material for circulation. In addition to my experience in acquisitions, I was also responsible for analyzing large collections of library materials, tailoring library records for optimal catalog

search performance and creating lending agreements between libraries during my time as a Library Director.

4. I am fully familiar with the catalog record creation process in the library sector. In preparing a material for public availability, a library catalog record describing that material would be created. These records are typically written in Machine Readable Catalog (herein referred to as “MARC”) code and contain information such as a physical description of the material, metadata from the material’s publisher, and date of library acquisition. In particular, the 008 field of the MARC record is reserved for denoting the date of creation of the library record itself. As this typically occurs during the process of preparing materials for public access, it is my experience that an item’s MARC record indicates the date of an item’s public availability.

5. Typically, in creating a MARC record, a librarian would gather various bits of metadata such as book title, publisher and subject headings among others and assign each value to a relevant numerical field. For example, a book’s physical description is tracked in field 300 while title/attribution is tracked in field 245. The 008 field of the MARC record is reserved for denoting the creation of the library record itself. As this is the only date reflecting the inclusion of said materials within the library’s collection, it is my experience

that an item's 008 field accurately indicates the date of an item's public availability.

6. I have reviewed Exhibit TI-1007, "Combined Digital Phase and Amplitude Modulation Communication Systems" by Charles R. Cahn as published in *IRE Transactions on Communication*, September 1960.

7. Attached hereto as Appendix CAHN01 is a true and correct copy of the MARC record for *IRE Transactions on Communication* as held by the University of Pittsburgh library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix CAHN01 accurately describes the title, author, publisher, and ISSN number of *IRE Transactions on Communication.* The 'Location Items' field of this record visible on page 2 indicates this collection includes the September 1960 edition of *IRE Transactions on Communication* containing "Combined Digital Phase and Amplitude Modulation Communication Systems".

8. Attached hereto as Appendix CAHN02 is a true and correct copy of "Combined Digital Phase and Amplitude Modulation Communication Systems" as published in *IRE Transactions on Communication* as held by the University of Pittsburgh library. I secured these scans myself from the

library's collection. In comparing Exhibit TI-1007 to Appendix CAHN02, it is my determination that Exhibit TI-1007 is a true and correct copy of "Combined Digital Phase and Amplitude Modulation Communication Systems" by Charles R. Cahn as published in *IRE Transactions on Communication* September 1960.

9. The 008 field of the MARC record in Appendix CAHN01 indicates the date of record creation. The 008 field of Appendix CAHN01 indicates the University of Pittsburgh library first acquired this journal as of June 20, 1976. Considering this information, it is my determination that *IRE Transactions on Communication* September 1960 and therefore "Combined Digital Phase and Amplitude Modulation Communication Systems" was made available to the public by the University of Pittsburgh as of June 20, 1976 and was likely available to the public after its initial release in September 1960.

10. I have reviewed Exhibit TI-1032, "A 1.5 GHz Highly Linear CMOS Downconversion Mixer" by Jan Crols and Michel S.J. Steyaert as published in *IEEE Journal of Solid-State Circuits*, July 1995.

11. Attached hereto as Appendix CROLS01 is a true and correct copy of the MARC record for *IEEE Journal of Solid-State Circuits* as held by the Carnegie Library of Pittsburgh. I secured this record myself from the library's public catalog. The MARC record contained within Appendix CROLS01 accurately describes the title, author, publisher, and ISSN number of *IEEE Journal of Solid-State Circuits.* The 'Lib Has' field of this record visible on page 2 indicates this collection includes the July 1995 edition of *IEEE Journal of Solid-State Circuits* containing "Combined Digital Phase and Amplitude Modulation Communication Systems".

12. Attached hereto as Appendix CROLS02 is a true and correct copy of "A 1.5 GHz Highly Linear CMOS Downconversion Mixer" as published in *IEEE Journal of Solid-State Circuits* as held by the Carnegie Library of Pittsburgh. I secured these scans myself from the library's collection. In comparing Exhibit TI-1032 to Appendix CROLS02, it is my determination that Exhibit TI-1032 is a true and correct copy of "A 1.5 GHz Highly Linear CMOS Downconversion Mixer" by Jan Crols and Michel S.J. Steyaert as published in *IEEE Journal of Solid-State Circuits* July 1995.

13. The 008 field of the MARC record in Appendix CROLS01 indicates the date of record creation. The 008 field of Appendix CROLS01 indicates the

Carnegie Library of Pittsburgh first acquired this journal as of September 1, 1975. Considering this information, it is my determination that *IEEE Journal of Solid-State Circuits* July 1995 and therefore "A 1.5 GHz Highly Linear CMOS Downconversion Mixer" was made available to the public by the Carnegie Library of Pittsburgh shortly after its initial release in July 1995.

14. I have reviewed Exhibit TI-1016, *Practical RF Design Manual* by Doug DeMaw.

15. Attached hereto as Appendix DEMAW01 is a true and correct copy of the MARC record for *Practical RF Design Manual* as held by the Penn State University library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix DEMAW01 accurately describes the title, author, publisher, and ISBN number of *Practical RF Design Manual.*

16. Attached hereto as Appendix DEMAW02 is a true and correct copy of selections from *Practical RF Design Manual* as held by the Penn State University library. I secured these scans myself from the library's collection. In comparing Exhibit TI-1016 to Appendix DEMAW02, it is my

determination that Exhibit TI-1016 is a true and correct copy of *Practical RF Design Manual* by Doug DeMaw.

17. The 008 field of the MARC record in Appendix DEMAW01 indicates the date of record creation. The 008 field of Appendix DEMAW01 indicates Penn State University library first acquired this book as of November 8. 1982. Considering this information, it is my determination that *Practical RF Design Manual* was made available to the public shortly after its initial acquisition as of November 8. 1982.

18. I have reviewed Exhibit TI-1025, "Active Low Pass Filter Design" by Edward J. Foster as published in *IEEE Transactions on Audio*, September/October 1965.

19. Attached hereto as Appendix FOSTER01 is a true and correct copy of the MARC record for *IEEE Transactions on Audio* as held by the Carnegie Library of Pittsburgh. I secured this record myself from the library's public catalog. The MARC record contained within Appendix FOSTER01 accurately describes the title, author, publisher, and ISSN number of *IEEE Transactions on Audio.* The 'Lib Has' field of this record visible on page 2 indicates this collection includes the September/October 1965 edition of

IEEE Transactions on Audio containing “Active Low Pass Filter Design”. In comparing Exhibit TI-1025 to Appendix FOSTER01, it is my determination that Exhibit TI-1025 is a true and correct copy of “Active Low Pass Filter Design” by Edward J. Foster as published in *IEEE Transactions on Audio* September/October 1965.

20. The 008 field of the MARC record in Appendix FOSTER01 indicates the date of record creation. The 008 field of Appendix FOSTER01 indicates the Carnegie Library of Pittsburgh first acquired this journal as of September 20, 1975. Considering this information, it is my determination that *IEEE Transactions on Audio* September/October 1965 and therefore “Active Low Pass Filter Design” was made available to the public by the Carnegie Library of Pittsburgh as of September 20, 1975 and was likely publicly available after its initial release in September/October 1965.

21. I have reviewed Exhibit TI-1027, "A BiCMOS Analog Front-End Circuit for an FDM-Based ADSL System" by D. Scott Langford, et. al as published in *IEEE Journal of Solid-State Circuits*, September 1998.

22. Attached hereto as Appendix LANGFORD01 is a true and correct copy of the MARC record for *IEEE Journal of Solid-State Circuits* as held by the

Carnegie Library of Pittsburgh. I secured this record myself from the library's public catalog. The MARC record contained within Appendix LANGFORD01 accurately describes the title, author, publisher, and ISSN number of *IEEE Journal of Solid-State Circuits*. The 'Lib Has' field of this record visible on page 2 indicates this collection includes the September 1998 edition of *IEEE Journal of Solid-State Circuits* containing "A BiCMOS Analog Front-End Circuit for an FDM-Based ADSL System".

23. Attached hereto as Appendix LANGFORD02 is a true and correct copy of "A BiCMOS Analog Front-End Circuit for an FDM-Based ADSL System" as published in *IEEE Journal of Solid-State Circuits* as held by the Carnegie Library of Pittsburgh. I secured these scans myself from the library's collection. In comparing Exhibit TI-1027 to Appendix LANGFORD02, it is my determination that Exhibit TI-1027 is a true and correct copy of "A BiCMOS Analog Front-End Circuit for an FDM-Based ADSL System" by D. Scott Langford, et. al as published in *IEEE Journal of Solid-State Circuits* September 1998.

24. The 008 field of the MARC record in Appendix LANGFORD01 indicates the date of record creation. The 008 field of Appendix LANGFORD01 indicates the Carnegie Library of Pittsburgh first acquired this journal as of

September 1, 1975. Considering this information, it is my determination that *IEEE Journal of Solid-State Circuits* September 1998 and therefore "A BiCMOS Analog Front-End Circuit for an FDM-Based ADSL System" was made available to the public by the Carnegie Library of Pittsburgh shortly after its initial release in September 1998.

25. I have reviewed Exhibit TI-1020, *The Design of CMOS Radio-Frequency Integrated Circuits* by Thomas H. Lee.

26. Attached hereto as Appendix LEE01 is a true and correct copy of the MARC record for *The Design of CMOS Radio-Frequency Integrated Circuits* as held by the University of Akron library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix LEE01 accurately describes the title, author, publisher, and ISBN number of *The Design of CMOS Radio-Frequency Integrated Circuits.* In comparing Exhibit TI-1020 to Appendix LEE01, it is my determination that Exhibit TI-1020 is a true and correct copy of *The Design of CMOS Radio-Frequency Integrated Circuits* by Thomas H. Lee.

27. The 008 field of the MARC record in Appendix LEE01 indicates the date of record creation. The 008 field of Appendix LEE01 indicates University of

Akron library first acquired this book as of July 21, 1997. Considering this information, it is my determination that *The Design of CMOS Radio-Frequency Integrated Circuits* was made available to the public shortly after its initial acquisition in July 21, 1997.

28. I have reviewed Exhibit TI-1017, "A 900-MHz CMOS Direct Conversion Receiver" by Behzad Razavi as published in *1997 Symposium on VLSI Circuits*.

29. Attached hereto as Appendix RAZAVI01 is a true and correct copy of the MARC record for *1997 Symposium on VLSI Circuits* as held by the SUNY Polytechnic Institute library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix RAZAVI01 accurately describes the title, author, publisher, and ISBN number of *1997 Symposium on VLSI Circuits.* In comparing Exhibit TI-1017 to Appendix RAZAVI01, it is my determination that Exhibit TI-1017 is a true and correct copy of "A 900-MHz CMOS Direct Conversion Receiver" by Behzad Razavi as published in *1997 Symposium on VLSI Circuits*.

30. The 008 field of the MARC record in Appendix RAZAVI01 indicates the date of record creation. The 008 field of Appendix RAZAVI01 indicates the

SUNY Polytechnic Institute library first acquired these proceedings as of October 13, 1997. Considering this information, it is my determination that *1997 Symposium on VLSI Circuits* and therefore “A 900-MHz CMOS Direct Conversion Receiver” was made available to the public shortly after its initial acquisition as of October 13, 1997.

31. I have reviewed Exhibit TI-1028, "A 1.9-GHz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications" by Jacques C. Rudell, et. al as published in *IEEE Journal of Solid-State Circuits*, December 1997.

32. Attached hereto as Appendix RUDELL01 is a true and correct copy of the MARC record for *IEEE Journal of Solid-State Circuits* as held by the Carnegie Library of Pittsburgh. I secured this record myself from the library’s public catalog. The MARC record contained within Appendix RUDELL01 accurately describes the title, author, publisher, and ISSN number of *IEEE Journal of Solid-State Circuits.* The ‘Lib Has’ field of this record visible on page 2 indicates this collection includes the December 1997 edition of *IEEE Journal of Solid-State Circuits* containing "A 1.9-GHz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications". In comparing Exhibit TI-1028 to Appendix RUDELL01, it is

my determination that Exhibit TI-1028 is a true and correct copy of "A 1.9-GHz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications" by Jacques C. Rudell, et. al as published in *IEEE Journal of Solid-State Circuits* December 1997.

33. The 008 field of the MARC record in Appendix RUDELL01 indicates the date of record creation. The 008 field of Appendix RUDELL01 indicates the Carnegie Library of Pittsburgh first acquired this journal as of September 1, 1975. Considering this information, it is my determination that *IEEE Journal of Solid-State Circuits* December 1997 and therefore "A 1.9-GHz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications" was made available to the public by the Carnegie Library of Pittsburgh shortly after its initial release in December 1997.

34. I have reviewed Exhibit TI-1026, "The Synchronous Oscillator: A Synchronization and Tracking Network" by Vasil Uzunoglu and Marvin H. White as published in *IEEE Journal of Solid-State Circuits*, December 1985.

35. Attached hereto as Appendix UZUNOGLU01 is a true and correct copy of the MARC record for *IEEE Journal of Solid-State Circuits* as held by the Carnegie Library of Pittsburgh. I secured this record myself from the

library's public catalog. The MARC record contained within Appendix UZUNOGLU01 accurately describes the title, author, publisher, and ISSN number of *IEEE Journal of Solid-State Circuits.* The 'Lib Has' field of this record visible on page 2 indicates this collection includes the December 1985 edition of *IEEE Journal of Solid-State Circuits* containing "The Synchronous Oscillator: A Synchronization and Tracking Network".

36. Attached hereto as Appendix UZUNOGLU02 is a true and correct copy of "The Synchronous Oscillator: A Synchronization and Tracking Network" as published in *IEEE Journal of Solid-State Circuits* as held by the Carnegie Library of Pittsburgh. I secured these scans myself from the library's collection. In comparing Exhibit TI-1026 to Appendix UZUNOGLU02, it is my determination that Exhibit TI-1026 is a true and correct copy of "The Synchronous Oscillator: A Synchronization and Tracking Network" by Vasil Uzunoglu and Marvin H. White as published in *IEEE Journal of Solid-State Circuits* December 1985.

37. The 008 field of the MARC record in Appendix UZUNOGLU01 indicates the date of record creation. The 008 field of Appendix UZUNOGLU01 indicates the Carnegie Library of Pittsburgh first acquired this journal as of September 1, 1975. Considering this information, it is my determination that

IEEE Journal of Solid-State Circuits December 1985 and therefore "The Synchronous Oscillator: A Synchronization and Tracking Network" was made available to the public by the Carnegie Library of Pittsburgh shortly after its initial release in December 1985.

38. I have reviewed Exhibit TI-1024, “Subharmonic Sampling of Microwave Signal Processing Requirements” by Peter A. Weisskopf as published in *Microwave Journal*, May 1992.

39. Attached hereto as Appendix WEISSKOPF01 is a true and correct copy of the MARC record for *Microwave Journal* as held by the Penn State University library. I secured this record myself from the library’s public catalog. The MARC record contained within Appendix WEISSKOPF01 accurately describes the title, author, publisher, and ISSN number of *Microwave Journal*. The ‘Availability’ field of this record visible on page 5 indicates this collection includes the May 1992 edition of *Microwave Journal* containing “Subharmonic Sampling of Microwave Signal Processing Requirements”.

40. Attached hereto as Appendix WEISSKOPF02 is a true and correct copy of “Subharmonic Sampling of Microwave Signal Processing Requirements” as

published in *Microwave Journal* as held by the Penn State University library. I secured these scans myself from the library's collection. In comparing Exhibit TI-1024 to Appendix WEISSKOPF02, it is my determination that Exhibit TI-1024 is a true and correct copy of "Subharmonic Sampling of Microwave Signal Processing Requirements" by Peter A. Weisskopf as published in *Microwave Journal* May 1992.

41. The 008 field of the MARC record in Appendix WEISSKOPF01 indicates the date of record creation. The 008 field of Appendix WEISSKOPF01 indicates the Penn State University library first acquired this journal as of June 26, 1979 and held the journal in perpetuity until 2006. Considering this information, it is my determination that *Microwave Journal* May 1992 and therefore "Subharmonic Sampling of Microwave Signal Processing Requirements" was made available to the public shortly after its initial release in May 1992.

42. I have reviewed Exhibit TI-1019, *Principles of Communications: Systems, Modulation and Noise* by Rodger E. Ziemer.

43. Attached hereto as Appendix ZIEMER01 is a true and correct copy of the MARC record for *Principles of Communications: Systems, Modulation and*

Noise as held by the Library of Congress. I secured this record myself from the library's public catalog. The MARC record contained within Appendix ZIEMER01 accurately describes the title, author, publisher, and ISBN number of *Principles of Communications: Systems, Modulation and Noise*.

44. I have reviewed the declaration of Rickea McLeod (Exhibit TI-1015), a description of *Principles of Communications: Systems, Modulation and Noise* as held by the Library of Congress. In comparing Exhibit TI-1019 to Appendix ZIEMER01 and the description of the library's holdings from the McLeod declaration, it is my determination that Exhibit TI-1019 is a true and correct copy of *Principles of Communications: Systems, Modulation and Noise* by Rodger E. Ziemer.

45. The 008 field of the MARC record in Appendix ZIEMER01 indicates the date of record creation. The 008 field of Appendix ZIEMER01 indicates the Library of Congress first acquired this book as of July 21, 1997. Considering this information, it is my determination that *Principles of Communications: Systems, Modulation and Noise* was made available to the public shortly after its initial acquisition as of July 21, 1997.

46. I have been retained on behalf of the Petitioner to provide assistance in the above-illustrated matter in establishing the authenticity and public availability of the documents discussed in this declaration. I am being compensated for my services in this matter at the rate of $200.00 per hour plus reasonable expenses. My statements are objective, and my compensation does not depend on the outcome of this matter.

47. I declare under penalty of perjury that the foregoing is true and correct. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: 5/15/2024

June Ann Munford

APPENDIX CV

June A. Munford
Curriculum Vitae

Education

University of Wisconsin-Milwaukee - MS, Library & Information Science, 2009
Milwaukee, WI

- Coursework included cataloging, metadata, data analysis, library systems, management strategies and collection development.
- Specialized in library advocacy, cataloging and public administration.

Grand Valley State University - BA, English Language & Literature, 2008
Allendale, MI

- Coursework included linguistics, documentation and literary analysis.
- Minor in political science with a focus in local-level economics and government.

Professional Experience

Researcher / Expert Witness, October 2017 – present
Freelance ● Pittsburgh, Pennsylvania & Grand Rapids, Michigan

- Material authentication and public accessibility determination. Declarations of authenticity and/or public accessibility provided upon research completion. Experienced with appeals and deposition process.

- Research provided on topics of public library operations, material publication history, digital database services and legacy web resources.

- Past clients include Alston & Bird, Arnold & Porter, Baker Botts, Fish & Richardson, Erise IP, Irell & Manella, O'Melveny & Myers, Perkins-Coie, Pillsbury Winthrop Shaw Pittman and Slayden Grubert Beard.

Library Director, February 2013 - March 2015
Dowagiac District Library ● Dowagiac, Michigan

- Executive administrator of the Dowagiac District Library. Located in

Southwest Michigan, this library has a service area of 13,000, an annual operating budget of over $400,000 and total assets of approximately $1,300,000.

● Developed careful budgeting guidelines to produce a 15% surplus during the 2013-2014 & 2014-2015 fiscal years while being audited.

● Using this budget surplus, oversaw significant library investments including the purchase of property for a future building site, demolition of existing buildings and building renovation projects on the current facility.

● Led the organization and digitization of the library's archival records.

● Served as the public representative for the library, developing business relationships with local school, museum and tribal government entities.

● Developed an objective-based analysis system for measuring library services - including a full collection analysis of the library's 50,000+ circulating items and their records.

November 2010 - January 2013
Librarian & Branch Manager, Anchorage Public Library ● Anchorage, Alaska

● Headed the 2013 Anchorage Reads community reading campaign including event planning, staging public performances and creating marketing materials for mass distribution.

● Co-led the social media department of the library's marketing team, drafting social media guidelines, creating original content and instituting long-term planning via content calendars.

● Developed business relationships with The Boys & Girls Club, Anchorage School District and the US Army to establish summer reading programs for children.

June 2004 - September 2005, September 2006 - October 2013
Library Assistant, Hart Area Public Library
Hart, MI

● Responsible for verifying imported MARC records and original MARC

cataloging for the local-level collection as well as the Michigan Electronic Library.

● Handled OCLC Worldcat interlibrary loan requests & fulfillment via ongoing communication with lending libraries.

Professional Involvement

Alaska Library Association - Anchorage Chapter
● Treasurer, 2012

Library Of Michigan
● Level VII Certification, 2008
● Level II Certification, 2013

Michigan Library Association Annual Conference 2014
● New Directors Conference Panel Member

Southwest Michigan Library Cooperative
● Represented the Dowagiac District Library, 2013-2015

Professional Development

Library Of Michigan Beginning Workshop, May 2008
Petoskey, MI
● Received training in cataloging, local history, collection management, children's literacy and reference service.

Public Library Association Intensive Library Management Training, October 2011
Nashville, TN
● Attended a five-day workshop focused on strategic planning, staff management, statistical analysis, collections and cataloging theory.

Alaska Library Association Annual Conference 2012 - Fairbanks, February 2012
Fairbanks, AK
● Attended seminars on EBSCO advanced search methods, budgeting, cataloging, database usage and marketing.

Depositions

2019 ● Fish & Richardson

Apple v. Qualcomm (IPR2018-001281, 39521-00421IP, IPR2018-01282 and 39521-00421IP2)

2019 ● Erise IP

Implicit, LLC v. Netscout Systems, Inc (Civil Action No. 2:18-cv-53-JRG)

2019 ● Perkins-Coie

Adobe Inc. v. RAH Color Technologies LLC (Cases IPR2019-00627, IPR2019-00628, IPR2019-00629 and IPR2019-00646)

2020 ● O'Melveny & Myers

Maxell, Ltd. v. Apple Inc. (Case No. 5:19-cv-00036-RWS)

2021 ● Pillsbury Winthrop Shaw Pittman LLP

Intel v. SRC (IPR2020-1449)

2022 ● Perkins-Coie

Realtek v. Future Link (IPR2021-01182)

2023 ● Fish & Richardson

Neuroderm Ltd. v. Abbvie, Inc (Case No. PGR2022-00040)

2023 ● Fish & Richardson

Nearmap US Inc. v. Pictometry International Corp. (IPR2022-00735)

2023 ● Fish & Richardson

Samsung Electronics v. MemoryWeb LLC (Case No. 39843-0136PS1)

2023 ● Pillsbury Winthrop Shaw Whitman LLP

Gravel Rating Systems v. Costco Wholesale Corp. (Civil Action No. 4:21-cv-149-ALM)

Limited Case and Clientele History

Alston & Bird

- Ericsson

  v. Collision Communications (IPR2022-01233)

- Nokia

  v. Neptune Subsea, Xtera (Case No. 1:17-cv-01876)

- Universal Electronics Inc

  v. Roku Inc (IPR2022-00818)

Arnold & Porter

- Ivantis

  v. Glaukos (Case No. 8:18-cv-00620)

- Samsung

  v. Jawbone (Case No. 2:21-cv-00186)

Benesch Friedlander Coplan & Aronoff

- Voyis

  v. Cathx (Case No. 5:21-cv-00077-RWS)

Erise I.P.

- Apple
  - v. Ericsson Inc. (IPR2022-00715)
  - v. Future Link Systems (IPRs 6317804, 6622108, 6807505, and 7917680)
  - v. INVT (Case No. 20-1881)
  - v. Navblazer LLC (IPR2020-01253)
  - v. Qualcomm (IPR2018-001281, 39521-00421IP, IPR2018-01282, 39521-00421IP2)
  - v. Quest Nettech Corp (Case No. 2:19-cv-00118-JRG)
  - v. Telefonaktiebolaget LM Ericsson (IPR2022-00275)

- Fanduel
  - v. CGT (Case No. 19-1393)

- Garmin
  - v. Phillips North America LLC (Case No. 2:19-cv-6301-AB-KS)

- Netscout
  - v. Longhorn HD LLC (Case No. 2:20-cv-00349)
  - v. Implicit, LLC (Civil Action No. 2:18-cv-53-JRG)

- Sony Interactive Entertainment LLC
  - v. Bot M8 LLC (IPR2020-01288)
  - v. Infernal Technology LLC (Case No. 2:19-CV-00248-JRG)

- Unified Patents

v. GE Video Compression (Civil Action No. 2:19-cv-248)

Fish & Richardson

- Apple

  v. AliveCor (3:21-cv-03958)

  v. LBS Innovations (Case No. 2:19-cv-00119-JRG-RSP)

  v. Koss Corporation (IPR2021-00305)

  v. Masimo (IPR 50095-0012IP1, 50095-0012IP2, 50095-0013IP1, 50095-0013IP2, 50095-0006IP1, 50095-0135IP1)

  v. Neonode (Case No. 21-cv-08872-EMC)

  v. Qualcomm (IPR2018-001281, 39521-00421IP, IPR2018-01282, 39521-00421IP2)

- Dell

  v. Neo Wireless (IPR2022-00616)

- Dish Network

  v. Entropic Communications, LLC (Case No. 2:2023-CV-01043)

  v. Realtime Adaptive Streaming (Case No. 1:17-CV-02097-RBJ)

  v. TQ Delta LLC (Case No. 18-1798)

- Evapco Dry Cooling

  v. SPG Dry Cooling (IPR2021-00688)

- Genetec

  v. Sensormatic Electronics (Case No. 1:20-CV-00760)

- Huawei

v. Bell Northern Research LLC (IPR2019-01174)

- Kianxis

  v. Blue Yonder (Case No. 3:20-cv-03636)

- LG Electronics

  v. Bell Northern Research LLC (Case No. 3:18-cv-2864-CAB-BLM)

- Metaswitch

  v. Sonus Networks (IPR2018-01719)

- Microsoft

  v. Throughputer Inc (IPR2022-00757)

- Mom Enterprises

  v. Ddrops Company (Case No. 1:22-cv-00332)

- MLC Intellectual Property

  v. MicronTech (Case No. 3:14-cv-03657-SI)

- Nearmap Inc

  v. EagleView Technologies (IPR2022-01009)

- Neuroderm Ltd.

  v. Abbvie, Inc (Case No. PGR2022-00040)

- Realtek Semiconductor

v. Future Link (IPR2021-01182)

- Quectel

  v. Koninklijke Philips (Case No. 1:20-cv-01710)

- Samsung

  v. Aire Technology (IPR2022-00877)

  v. Bell Northern Research (Case No. 2:19-cv-00286-JRG)

  v. Communication Technologies Inc (IPR2022-01221)

  v. Jawbone Innovations (IPR2022-00865)

  v. MemoryWeb LLC (IPR2022-00885)

  v. Dodots Licensing Solutions (IPR2023-00701)

  v. Telefonaktiebolaget LM Ericsson (IPR2021-00615)

- Texas Instruments

  v. Vantage Micro LLC (IPR2020-01261)

- Xilinx

  v. Sentient Sensors LCC (Case No. 1:22-cv-00173)

Irell & Manella

- Curium

O'Melveny & Myers

- Apple

  v. Maxell (Case No. 5:19-cv-00036-RWS)

- Micron Technology Inc.

  v. Besang Inc (IPR2023-00900)

- Samsung

  v. Daedalus Prime LLC (1335 Investigation)

Perkins-Coie

- Heru Industries

  v. The UAB Research Foundation (IPR2022-01148)

- Intel Corporation

  v. BitMICRO (Case No. 5:23-cv-00625)

- Realtek Semiconductor

  v. Future Link (IPR2021-01182)

- Twitter Inc

  v. VOIP-Pal.com (Case No. 3:20-cv-02397-JD)

- TCL Industries

  v. Koninklijke Philips NV (IPR2021-00495, IPR2021-00496 and IPR2021-00497)

Pillsbury Winthrop Shaw Pittman

- Intel

  v. FG SRC LLC (Case No. 6:20-cv-00315)

- Gravel Rating Systems

v. Costco (Case No. 4:21-cv-149)
v. Lowe's Home Centers (Case No. 4:21-cv-150)
v. T-Mobile USA (Case No. 4:21-cv-152)
v. Kohl's Inc. (Case No. 4:21-cv-258)
v. Under Armor (Case No. 4:21-cv-356)

Quinn Emanuel

- Wolfspeed

    v. The Trustees of Purdue University (Case No. 1:2021-cv-00840)

Stern, Kessler, Goldstein & Fox

- Preliminary Research

Sheppard, Mullin, Richter & Hampton LLP

- Cadence Design Systems Inc.

    v. Semiconductor Design Technologies (Case No. 3:23-cv-01001)

APPENDIX CAHN01

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The signal duration is $T = m\tau$, and by (2) m is proportional to R. Therefore, we define a *reduced signal-to-noise ratio* d_0 by

$$d_0^2 = \frac{1}{RN} \sum_i p_i \sum_j r_j^{(i)} d_j^2. \tag{44}$$

Systems will now be compared by plotting the quantity $2^{-U/RN}$ vs d_0.

Using the convexity of the function $\log x$, we can derive the inequality

$$U \geq -\log \bar{Q} \quad \text{(or)} \quad \bar{Q} \geq 2^{-U}, \tag{45}$$

where

$$\bar{Q} = \sum_i p_i Q_i$$

is the average probability of correct reception of the letters of the alphabet. Equality holds when all signals have equal probabilities of correct reception ($Q_i \equiv Q$). We then have $U = -\log Q$ and $2^{-U/RN} = Q_e$, and we are back to the equal-bandwidth comparison derived earlier. The source possesses maximum entropy[1] when all signals are sent equally often: $p_i \equiv 1/L$, and we then have $H = \log L$ and $\log L_e = (\log L)/RN$ as before. Our reduced signal-to-noise ratio becomes that defined in (8) when all transmitted signals have the same energy.

If one follows a similar line of reasoning, it is not hard to show that for the equal-rate comparison of a number of systems one calculates for each the quantity $2^{-U/R}$ for the same set of values of an equivalent signal-to-noise ratio d_e given now by

$$d_e^2 = \frac{1}{H} \sum_i p_i \sum_j r_j^{(i)} d_j^2. \tag{46}$$

The bandwidth W required when the signal durations are adjusted for this comparison is proportional to $RN/H = 1/\log L_e$. Again the equal-bandwidth and the equal-rate comparisons rank strictly comparable systems in the same order of preference.

In this formulation the performance of a system depends upon the quantity U of (42); the smaller U the better. One would like to minimize U for each given system by varying the probabilities p_i and, possibly, the distribution of power among the several signals, as well perhaps as even the decision rules at the receiver. These variations will be subject to such constraints as a fixed average transmitter power and a fixed entropy H. Consideration of the problems that arise here lies outside the scope of this paper.

VI. Acknowledgment

We wish to thank E. Scherer, Dr. R. Filipowsky, and others of the Communications Group, Advanced Development, Westinghouse Electronics Division, Baltimore, Md., whose discussions of communication problems stimulated the work described here.

Combined Digital Phase and Amplitude Modulation Communication Systems*

CHARLES R. CAHN†, MEMBER IRE

Summary—**The performance of phase modulation communication systems is investigated for the asymptotic case of a high signal-to-noise ratio. A simple and excellent approximation to the probability of error is derived for both coherent and phase-comparison demodulation. In addition, a simple expression is derived for the asymptotic degradation of phase-comparison demodulation.**

When the number of bits per sample of the signal is large, a combination of digital amplitude and phase modulation is found to make more efficient use of transmitter power than phase modulation alone. The number of amplitude levels may be optimized for either minimum peak power or minimum average power, using the approximate expressions for probability of error. While an analytical solution can be found for the peak power case, a numerical solution with restriction to powers of two appears preferable, and is necessary for the average power case. Accordingly, tables showing the optimum number of levels with this restriction are presented.

* Received by the IRE PGSC, March 14, 1960.
† Space Tech. Labs., Inc., Los Angeles, Calif.

Introduction

THE use of multiple amplitude levels to transmit digital information in a restricted bandwidth is well-known under the name quantitized pulse-amplitude modulation (PAM). In a recent paper,[1] the possibility of employing multiple phase positions for the same purpose was explored. Performance calculations for the case of a nonfading signal in Gaussian noise indicate that digital multiphase modulation requires a lower signal-to-noise ratio than PAM to maintain a specified error rate. However, since multiphase modulation produces an essentially constant amplitude signal, its use is not consistent with

[1] C. R. Cahn, "Performance of digital phase-modulation communication systems," IRE Trans. on Communication Systems, vol. CS-7, pp. 3–6; May, 1959.

Shannon's result that a Gaussian amplitude distribution provides maximum transmission capacity when the signal is average-power limited. A combination of digital-amplitude and digital-phase modulation is thereby suggested as a desirable form of digital modulation.

It is the purpose of this paper to analyze the performance of combined phase and amplitude modulation systems, with emphasis on obtaining asymptotic, or high signal-to-noise ratio comparisons of various modulation combinations. The asymptotic comparison is justified because it applies, with reasonable accuracy, over the practical range of error rate; in addition, simple results may be obtained and related to significant geometrical parameters. It will be possible, thereby, to select combinations which are asymptotically optimum from the point of view of minimum required signal-to-noise ratio, or other suitable criteria.

The amplitude and phase modulations are considered as separately applied to each independent sample of the signal. An envelope detector is assumed for amplitude demodulation in the receiver. (This is equivalent to coherent detection for high signal-to-noise ratios.) However, two methods of practical importance for phase demodulation are considered: 1) coherent detection with a synchronized local reference and 2) phase comparison of two successive received samples. As discussed in previous papers,[1,2] the former is theoretically optimum but may not be applicable because of fluctuations of the propagation medium or oscillator instability. The latter requires only short-term phase stability in the transmission system, but engenders an inherent degradation in performance.

Only systems in which the same number of phase positions is used with each amplitude level are considered. As pointed out by J. Taber of Space Technology Laboratories, a further saving in transmitter power will result if this restriction is removed. However, in view of the problem of practical equipment implementation, this paper has been limited to a consideration of systems with independent phase and amplitude modulations.

Asymptotic Performance of Digital Multiphase System

Coherent Phase Demodulation

A digital multiphase system utilizes a set of n equally spaced phase positions of the carrier to transmit data expressed in terms of an n-level alphabet. Coherent detection of such a signal is relatively simple to analyze because of the geometrical symmetry. Thus, if there are n possible phases, an error in transmission will occur if noise causes the received signal to be displaced in phase by more than π/n radians. In a previous paper,[1] curves showing the variation of the required signal-to-noise ratio with number of phase positions were presented for several specified probabilities of error. An excellent analytic approximation to these curves is derived in the following, and will facilitate analytical comparison of different modulation systems. It has been shown[1] that when the signal-to-noise ratio, S/N, is high, the probability density of phase for a sine wave in Gaussian noise may be approximated by

$$p(\theta) \cong \sqrt{\frac{S/N}{\pi}} \cos\theta \exp\left(-\frac{S}{N}\sin^2\theta\right), \quad |\theta| < \pi/2, \quad (1)$$

where θ denotes the phase displacement from the noise-free carrier. By an appropriate change of variable, (1) may be directly integrated to yield the probability of error, the result being

$$P_e \cong 2\left[1 - \Phi\left(\sqrt{2\frac{S}{N}}\sin\pi/n\right)\right] \cong \frac{\exp\left(-\frac{S}{N}\sin^2\pi/n\right)}{\sqrt{\pi S/N}\sin\pi/n}, \quad (2)$$

where $\Phi(u)$ denotes the probability integral (*i.e.*, the Gaussian distribution) and the last term in (2) is an asymptotic evaluation for large values of $\sqrt{2S/N}\sin\pi/n$.

Eq. (2) is a "normalized" or "universal" curve providing an approximation to the probability of error for any number of phase positions. The equation is plotted in Fig. 1 as the curve marked $n = \infty$, the notation indicating

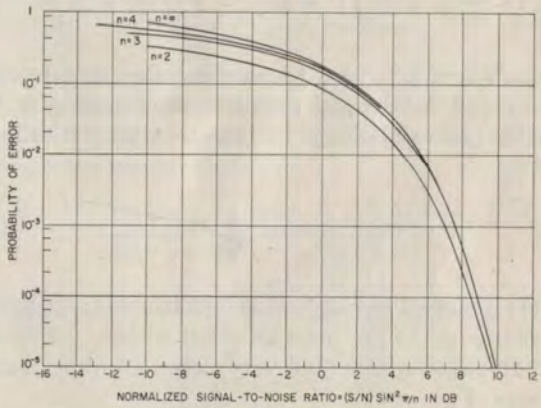

Fig. 1—Probability of error for phase-modulation systems with coherent phase demodulation.

that the approximation is exact in the limit as n becomes large. The other curves in Fig. 1 are exact curves obtained by numerical integration for small values of n, and are plotted by using the indicated normalization on the abscissa. It is seen that the approximation ($n = \infty$) is extremely good for $n \geq 3$ and is fairly close even for the binary case, $n = 2$. The closed form evaluation for $n = 2$ shows that (2) is in error only by a factor of two for this case.

The exponential form of (2)may be seen to be related to the amplitude distribution of random noise. The dependence of the exponent upon the number of n phases

[2] J. G. Lawton, "Theoretical error rates of 'differentially-coherent' binary and 'kineplex' data transmission systems," Proc., IRE vol. 47, pp. 333–334; February, 1959.

can be obtained by a simple geometric argument, as follows. Because of the exponential nature of the Gaussian distribution, the dominant behavior of the probability of error is determined by the smallest noise amplitude which can cause the resultant of signal and noise to cross a decision threshold. This shortest distance is proportional to $\sin \pi/n$, as shown in Fig. 2. By a quantitative extension of this argument, in fact, (2) may be derived without initial recourse to an approximation of the phase distribution.

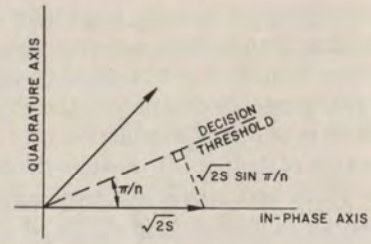

Fig. 2—Illustration of minimum distance to decision threshold.

Phase-Comparison Demodulation

In a previous paper,[1] demodulation by phase-comparison of successive independent signal samples was shown to introduce a 3-db degradation, for large n. On the other hand, the limiting degradation is zero for a binary system.[2] The exact asymptotic degradation for any intermediate value of n can be derived by an extension of the geometric argument used above. It may be seen that an error in transmission is caused by any combination of phase displacements in the two samples, the difference of which exceeds π/n in magnitude. Again, because of the characteristics of Gaussian noise, the dominant contribution to the error probability occurs for phase displacements each of magnitude $\pi/2n$, but in opposite directions. The exponential behavior of this dominant contribution is, accordingly,

$$\left[\exp\left(-\frac{S}{N}\sin^2 \pi/2n\right)\right]^2 = \exp\left(-2\frac{S}{N}\sin^2 \pi/2n\right). \tag{3}$$

Comparison of (2) and (3) shows that the signal-to-noise ratios required for equal probabilities of error with the two-phase demodulation procedures are asymptotically related by

$$\frac{(S/N)_{\text{phase comparison}}}{(S/N)_{\text{coherent}}} = \frac{\sin^2 \pi/n}{2\sin^2 \pi/2n}. \tag{4}$$

Eq. (4) is plotted in Fig. 3. It is seen that the asymptotic degradation is 1.8 db for a tri-phase system, 2.3 db for a quadri-phase system, and very close to 3 db for larger numbers of phases.

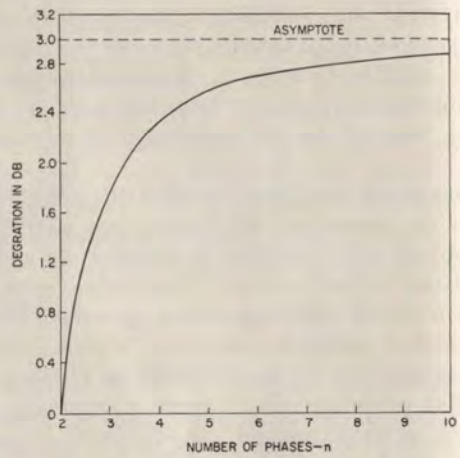

Fig. 3—Limiting degradation of phase-comparison demodulation over coherent phase demodulation.

Eq. (4) may be combined with (2) to obtain a universal curve for probability of error with phase-comparison demodulation. Thus,

$$P_e \cong 2\left[1 - \Phi\left(2\sqrt{\frac{S}{N}}\sin \pi/2n\right)\right]$$

$$\cong \frac{\exp\left(-2\frac{S}{N}\sin^2 \pi/2n\right)}{\sqrt{\pi 2S/N}\sin \pi/2n}. \tag{5}$$

Eq. (5) is plotted in Fig. 4 as the curve labeled $n = \infty$, the notation having the same significance described for (2). For comparison, exact curves, obtained by numerical integration for small values of n, are also plotted in Fig. 4.

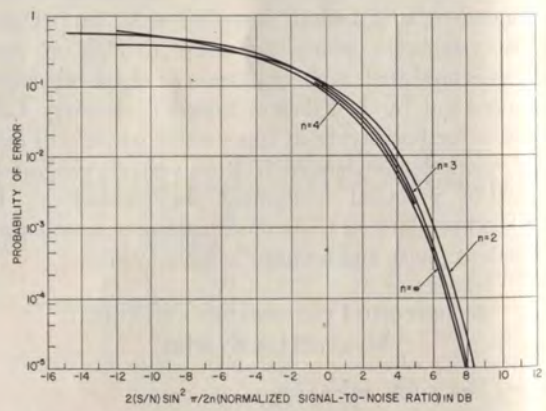

Fig. 4—Probability of error for phase-modulation systems with phase-comparison demodulation.

It appears that (5) is an excellent approximation for all values of n.

Combined Multiamplitude and Multiphase Modulation

A modulation combination of m amplitude levels and n phase positions will allow transmission of digital data having an alphabet size $r = nm$. All modulation combinations with equal alphabet sizes will yield the same channel capacity when the number of signal samples per second

is fixed. A qualitative explanation showing why a power saving can result when several amplitude levels are used is easily obtained, as follows. Suppose that it is desired to double the alphabet size in a phase-modulation system to provide an additional bit per sample. This can, of course, be accomplished by doubling the number n of phases. However, if n is sufficiently large that $\sin \pi/n$ may be replaced by its argument, (2) shows a 6-db additional power requirement to maintain a specified error rate with the doubled number of phases. Alternatively, the additional bit can be provided by use of two amplitude levels rather than by an increase in the number of phases. To a good approximation, the two amplitudes need be spaced only by the distance between the tips of signal phasors in adjacent phase positions (see Fig. 2) and, therefore, both peak and average power requirements are increased by amounts less than 6 db when n is large.

A more accurate specification of the spacing between amplitude levels may be obtained by consideration of the probability distribution of the envelope. Since the quadrature noise component can be neglected when the signal-to-noise ratio is high, this distribution is essentially Gaussian. Consequently, for uniform probabilities of error, the m amplitudes should be equally spaced, and the amplitude-decision thresholds should be symmetrically located between adjacent levels. Denoting the ratio of amplitude spacing to *rms* noise by γ, the average probability of error in demodulating the amplitude level is easily shown to be,

$$(P_e)_{\text{amplitude}} = \frac{2(m-1)}{m}[1 - \Phi(\gamma/2)] \cong \frac{2(m-1)e^{-\gamma^2/8}}{m\sqrt{2\pi}\,\gamma/2}. \tag{6}$$

The probability of error in demodulating the phase position is given in (2); however, it depends upon the amplitude level used for each sample. The dominant contribution is from the lowest level, which is used $1/m$ of the time. The total probability of error is then essentially the sum of the two individual probabilities of error, when these are small. Since the amplitude level and the phase position are often selected from separate binary data, it is desirable that the two probabilities of error be approximately equal. Thus, equating the exponential parts of (6) and either (2) or (5) will determine the proper amplitnde spacing. The resulting levels are given by the expressions

$$S_k/S_1 = [1 + 2(k-1)\sin \pi/n]^2 \tag{7a}$$

for coherent phase demodulation, and

$$S_k/S_1 = [1 + \sqrt{8}\,(k-1)\sin \pi/2n]^2 \tag{7b}$$

for phase-comparison demodulation. In (7), S_k denotes the power of the kth level. The power S_1 of the lowest amplitude level is then the parameter establishing the error rate (when the number of phase positions is specified).

The optimum choice for number of amplitude levels m and number of phase positions n, for a given required number of states $r = nm$, of course, depends upon the optimization criterion employed. Two criteria will be considered here: 1) minimum peak power, and 2) minimum average power. More complex criteria incorporating the relative costs of modulation and demodulation equipment can be formulated; however, the above are of direct interest in many practical situations. The peak and average powers can be expressed using (7). Thus, for coherent phase demodulation

$$\frac{S_{\text{peak}}}{S_1} = [1 + 2(m-1)\sin \pi/n]^2 \tag{8}$$

$$\frac{S_{\text{average}}}{S_1} = \frac{1}{m}\sum_{k=0}^{m-1}[1 + 2k\sin \pi/n]^2, \tag{9}$$

and for phase-comparison demodulation

$$\frac{S_{\text{peak}}}{S_1} = [1 + \sqrt{8}\,(m-1)\sin \pi/2n]^2 \tag{8a}$$

$$\frac{S_{\text{average}}}{S_1} = \frac{1}{m}\sum_{k=0}^{m-1}[1 + \sqrt{8}\,k\sin \pi/2n]^2. \tag{9a}$$

A meaningful optimizing procedure requires that the probability of error be introduced as a fixed constraint. Using the asymptotic approximation or (2) or (5), this constraint becomes

$$S_1 \sin^2 \pi/n = \text{constant} \tag{10a}$$

for coherent phase demodulation, and

$$S_1 \sin^2 \pi/2n = \text{constant} \tag{10b}$$

for phase-comparison demodulation.

The minimization can be very easily carried through for the peak power case, and for reasonably large $r = nm$ the approximate solutions are

$$m = \sqrt{\frac{r}{2\pi}}; \quad \frac{n}{m} = 2\pi \tag{11a}$$

for coherent phase demodulation, and

$$m = \sqrt{\frac{r}{\sqrt{2\pi}}}; \quad \frac{n}{m} = \sqrt{2\pi} \tag{11b}$$

for phase-comparison demodulation. However, it is unlikely that the true minimum would be used in practice, since restriction to a number of levels which is a power of two appears desirable in view of the coding complexity otherwise generated. Table I presents the optimum choice of levels when this restriction is made. Both coherent phase demodulation and phase-comparison demodulation lead to the same result.

The minimization procedure for the average power case leads to considerable algebraic complexity, and a simple analytic solution does not appear to be feasible. Since the primary interest is for solutions which are powers of two, a numerical minimization can be performed with this restriction, yielding the results of Table II. The

TABLE I
OPTIMUM NUMBER OF AMPLITUDE LEVELS AND PHASE POSITIONS FOR MINIMUM PEAK POWER
(NUMBERS RESTRICTED TO POWERS OF 2)

Bits per sample	Total number of states	Number of amplitude levels	Number of phase positions
1	2	1	2
2	4	1	4
3	8	1	8
4	16	2	8
5	32	2	16
6	64	4	16
7	128	4	32
8	256	8	32

TABLE II
OPTIMUM NUMBER OF AMPLITUDE LEVELS AND PHASE POSITIONS FOR MINIMUM AVERAGE POWER
(NUMBER RESTRICTED TO POWERS OF 2)

Bits per sample	Total number of states	Number of amplitude levels	Number of phase positions
1	2	1	2
2	4	1	4
3	8	2	4
4	16	2	8
5	32	4	8
6	64	4	16
7	128	8	16
8	256	8	32

asymptotic saving of transmitter power with use of the optimum (restricted to powers of 2) modulation combination is indicated in Figs. 5 and 6. These figures compare the increase in peak and in average power to maintain a specified probability of error as the total number of states r is increased from two for; 1) the optimum combination of phase and amplitude modulation, and 2) a single amplitude level (phase modulation only).

CONCLUSIONS

The results presented in the above discussion are of particular interest, since they indicate the existence of excellent and relatively simple approximations of the probability of error in digital multiphase systems. These approximations should facilitate the analysis of such systems, much as PAM systems have been analyzed in the past, and may point the way toward useful concepts not easily discovered by graphical techniques.

The solution for the asymptotic degradation introduced by phase-comparison demodulation is believed to be a new result and replaces previous approximations which do not fully take into account the nonlinear relation between phase displacement and noise amplitude.

Optimum combinations of multiamplitude and multiphase modulations have been obtained which take maximum advantage of available transmitter power. Of course, the solutions for a large alphabet size may have only limited applications in practice, because of the difficulties of instrumenting multistate systems. When the number

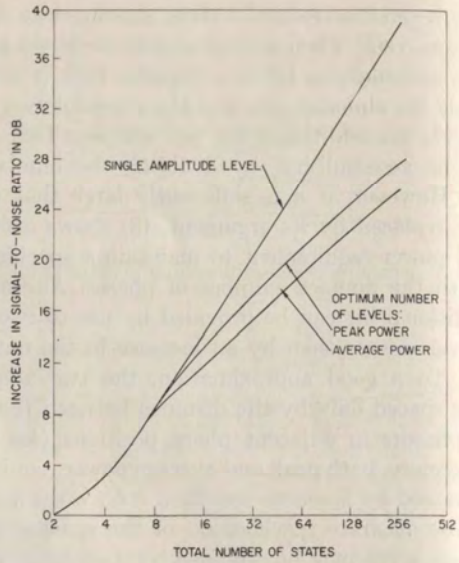

Fig. 5—Increase in signal-to-noise ratio to maintain fixed error rate with coherent phase demodulation.

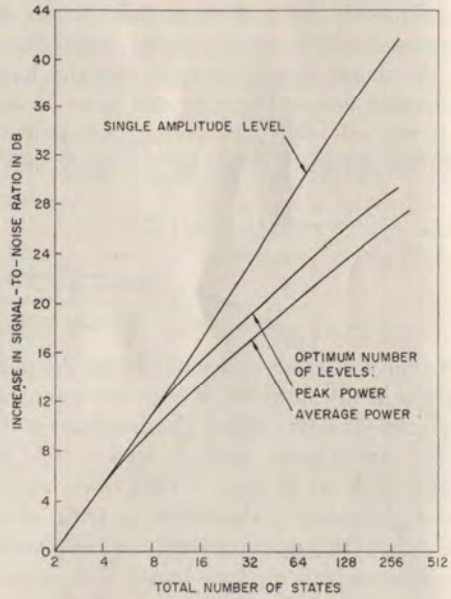

Fig. 6—Increase in signal-to-noise ratio to maintain fixed error rate with phase-comparison demodulation.

of states is relatively small, as is the usual case, phase modulation alone is found to be optimum. On the other hand, the theory indicates that significant power savings can be realized by use of combined amplitude and phase modulation when the information per sample of the signal is required to be high. A transition case is 4 bits per sample (16 states), in which a choice of 2 amplitude levels and 8 phase positions, is preferred.

From the point of view of equipment complexity, a system with combined amplitude and phase modulation is probably more simply instrumented than one using phase modulation alone, particularly when binary data are to be encoded for transmission. For example, when 4

bits per sample are transmitted by a choice of 8 phase positions and 2 amplitude levels, code conversion from binary to octal form is required. With the use of 16 phase positions, code conversion from binary to the 16-state form is necessary. Thus, practical benefits in addition to a saving in power may be obtained by employing combined amplitude and phase modulation in a digital communication system.

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A New Transmission Method for Pulse-Code Modulation Communication Systems*

A. P. BROGLE†

Summary—**This paper presents the results of a study of the basic factors underlying the selection of a preferable method of transmission for pulse-code modulation communication systems. A new method of transmission, called biternary, is described and is compared with quaternary transmission, as a means of doubling the channel capacity of PCM systems without requiring increased bandwidth or transmission facilities. It is found that biternary transmission is more tolerant of the effects of all types of interference than quaternary transmission, and significantly reduces a major problem of quaternary transmission excessive errors, caused by low frequency cut-off effects. The use of biternary transmission is planned in present and future military pulse-code modulation communication systems.**

INTRODUCTION

PULSE-CODE modulation systems are being developed to serve as the major means of multichannel communications for the Army. In addition to the need for these systems to satisfy the requirements for combat communications, future plans include widespread use of these systems for global communications.

A fundamental problem of these developments is the selection of the method of transmission which yields best over-all performance for least total cost in required equipment. For an acceptable solution, this choice must be made within the permissible limits of these factors and under the constraints of restricted bandwidth, specified transmission media and modulations, given power outputs and transmission losses, predicted noise levels, and so forth. The demands for high accuracy, together with the wide range of transmission conditions to be overcome in these systems, further restrict this choice to a very few types of known transmission techniques which could conceivably satisfy the requirements.

In PCM, the signals to be transmitted are sampled at regular intervals, and the amplitude of each sample is sent by a coded group of pulses. The usual method of coding is to represent each sample by a group of on-off or binary pulses. However, the definition of PCM does not preclude coding of these samples by higher order numerical forms, such as ternary, quaternary, quinary etc., codes.

At the receiving end, the radio frequency carrier, if any, is amplified and demodulated. The resulting signal is then resampled and applied to a slicing circuit, which produces regenerated PCM pulses whenever the voltage applied to it falls within the prescribed range. Because of noise on the transmission path, bandwidth limitations and system imperfections, the received pulses before sampling and regeneration will differ in shape from the transmitted pulses. These distortions and uncertainties will affect the output, however, only if they are of sufficient amplitude at the sampling times to cause the slicing circuit to make an improper decision. The principal problem of pulse transmission is to find out how often this will happen for given system characteristics and noise.

TRANSMISSION CAPACITY

In PCM, the bandwidth establishes the maximum rate at which pulses can be transmitted through a perfect low-pass channel, without mutual interference between pulses. The presence of Gaussian noise in the channel then limits the number of independent pulse amplitudes that can be reliably detected in any pulse interval. Thus, the use of PCM, in theory, allows bandwidth and signal-to-noise ratio to be exchanged according to the same law as an ideal channel.

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† RCA Corp., New York, N. Y. Formerly with U. S. Army Signal Corp, Ft. Monmouth, N. J.

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A 1.5 GHz Highly Linear CMOS Downconversion Mixer

Jan Crols, *Student Member, IEEE* and Michel S. J. Steyaert, *Senior Member, IEEE*

***Abstract*—A CMOS mixer topology for use in highly integrated downconversion receivers is presented. The mixing is based on the modulation of nMOS transistors in the triode region which renders an excellent linearity independent of mismatch. With two extra capacitors added to the classical cross-coupled MOSFET-C lowpass filter structure, GHz signals can be processed while only a low-frequency opamp is required as output amplifier. The downconversion mixer has an input bandwidth of 1.5 GHz. The measured third-order intercept point (IP3) of 45.2 dBm demonstrates the high linearity. The mixer has been implemented in a 1.2 μm CMOS process. It takes up 1 mm^2 of total chip area and its power consumption is 1.3 mW from a single 5 V power supply.**

I. Introduction

THE NEED FOR highly integrated receivers in the 1–2 GHz range has grown considerably with the introduction of new wireless telecommunication services like digital cellular telephone. Key issues in the design of receivers for these applications are the quality of the signal reception, the level of integration, the power consumption and the cost prize. Several realizations of the RF part for these receivers have been presented in the past [1]–[4]. They are all realized in either a GaAs or Si bipolar process. The use of the bipolar technology is often prefered over GaAs for its lower cost prize and equally good performance in the 1–2 GHz range. A further integration, i.e., combining the analog RF, the analog LF and the digital part on one chip, will be the next goal. The analog LF and the digital part are preferably realized in a CMOS technology. Combining these with the RF part would require the use of a BiCMOS technology and although these technologies are ever more used in telecommunication applications, they are not suited for the realization of receivers for frequencies above 1 GHz. The quality of the bipolar devices is in todays BiCMOS processes not sufficient. The value of their f_t and more important of their r_b is not so good as what is available in bipolar only processes. At this time, using CMOS is the only way to obtain a further and full integration. With the ongoing further decreasing of CMOS gatelengths this becomes ever more feasible [5]–[8].

In this paper a full CMOS downconversion mixer is presented. It is a key building block for the realization of a fully integrated CMOS 1 GHz zero-IF receiver. The presented downconversion mixer is not only important for the fact that it is implemented in CMOS, its linearity is also much better than any bipolar or GaAs realization that has been previously presented. A CMOS 1 GHz downconversion mixer has been proposed before [5], but it was based on the use of subsampling. Such a circuit can only cope with smallband input signals, resulting in the need for the use of a high-quality HF filter which can not be realized in an integrated way. The mixer which is presented in this paper is a true double balanced multiplier, capable of downconverting broadband input signals by multiplication with a sinusoidal local oscillator.

The second section of this paper describes the topology of the presented downconversion mixer. The topology is based on the use of four cross-coupled CMOS transistors operated in the triode region and connected to a virtual ground point [6]. Two important capacitors of 25 pF have been added to this topology on the virtual ground points. With these capacitors it becomes possible to realize a very high input bandwidth (as high as 1.5 GHz) with the use of a low-frequency opamp (10 MHz). The third and fourth part of this text describe the design aspects. The fifth and sixth part are respectively on the noise capabilities of the presented structure and the relationschips between linearity, noise and power consumption. The last two parts describe the practical realization and the measurement results.

II. Mixer Topology

The linearity of an RF mixer is in most cases rather limited. The Gilbert topology is the most common used in a bipolar technology [9]. Its operation is based on a translinear configuration, i.e., the use of the exponential voltage to current conversion of the bipolar transistor. Techniques like predistortion and emittor degeneration are necessary to obtain a reasonable linearity. Imperfections in this structure combined with a limited matching will render a third-order intercept point (IP3) which can only be slightly larger than 0 dBm [10]. In CMOS a double balanced structure which cancels out the quadratic term of the MOS transistor can be used [11], [12]. These mixer have not only a limited linearity which highly depends on matching, even more important is their limited frequency range. The input transistors of these mixers can only be biased with a relatively small $V_{GS} - V_T$ in order to keep them in saturation at all times. The result is large input transistors which limits the maximal achievable input bandwidth to about 100 MHz.

A better solution is to use the transistors in the linear region, preferably with a large $V_{GS} - V_t$. In this way a small R_{on} can be realized with a small transistor, allowing a high input bandwidth. This property has been used to realize high frequency GaAs commutating mixers [13]. The

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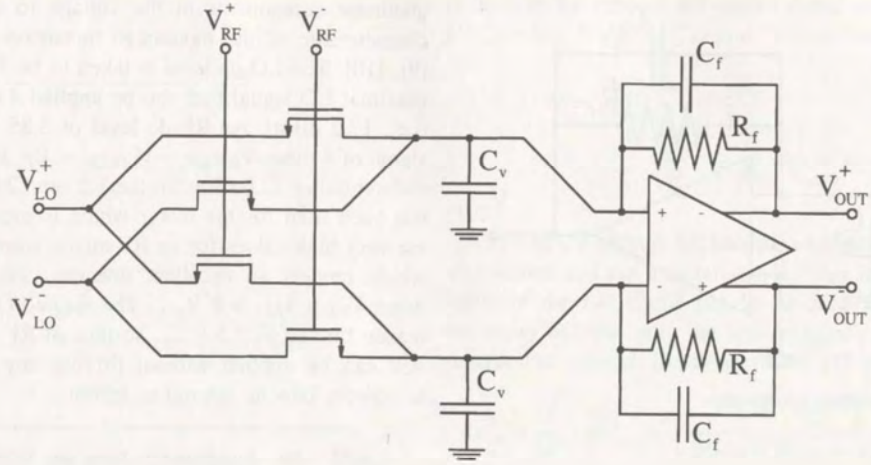

Fig. 1. The mixer topology with the extra capacitor on the virtual ground nodes.

transistors are being used as pass-transistors and the linearity of these mixers does therefore not depend on the voltage to current conversion characteristic of the transistors. The linearity is mainly determined by the speed limitation of the pass-transistor and by the generation of spurious signals during switching. This technique can also be used in CMOS. The output signal after commutation is however still a high-frequency signal and it can therefore not be further processed in CMOS. However, receivers only require a downconversion mixer and this means that the output bandwidth may be limited. A solution based on subsampling with a switched-capacitor structure has been proposed in [5]. The MOS-transistors are used as pass-transistors and an IP3 of 27 dBm has been reported.

A CMOS mixer with very high linearity can be realized by using the linear voltage to current charateristic of the MOS transistor in its triode region [6]. The use of a double balanced structure cancels out the common-mode dc biasing signals and the nonlinear dependence of g_{DS} on V_{DS}. The remaining problem is still the further processing of the high-frequency output current. This limits in [6] the bandwidth to 200 MHz at the cost of a high power consumption and a reduced linearity of the output stage. The mixer presented in this paper is based on this topology (see Fig. 1). There are however two very important capacitors added on the virtual ground nodes of this topology (the capacitors C_v in Fig. 1). Indeed, the output stage, the opamp and the feedback resistors, which convert the output current of the mixing transistors back into a voltage, must, in a downconversion mixer, only be able to produce low-frequency output signals. However, in order to let the input structure operate correctly for all frequencies, there may not be a signal on the virtual ground nodes of the mixer at any time. This is normally done with the feedback structure over the opamp which creates the virtual ground at its inputs. The transistors in the input structure would operate as pass-transistor for high-frequency signals when the frequency capability of the opamp would not be high enough. Therefore the capacitors C_v have been added. They make sure that all high-frequency currents injected to the virtual ground nodes are filtered out and not converted into voltages. The opamp still generates the virtual ground for low-frequencies. By using this structure, it becomes possible to split the design of the input structure and the opamp. The input structure can now be optimized for operation at very high frequencies (more than 1 GHz), while the opamp can be designed for low-frequency operation (a few MHz).

With a perfect virtual ground the currents through the modulated transistors are

$$\begin{aligned}
I_{DS,1} &= \beta_1 \cdot \left(V_{RF}^{+} - V_{LO,DC} - V_{Tn1} - \frac{V_{LO}^{+} - V_{LO,DC}}{2}\right) \cdot (V_{LO}^{+} - V_{LO,DC}) \\
I_{DS,2} &= \beta_2 \cdot \left(V_{RF}^{-} - V_{LO,DC} - V_{Tn,2} - \frac{V_{LO}^{-} - V_{LO,DC}}{2}\right) \cdot (V_{LO}^{-} - V_{LO,DC}) \\
I_{DS,3} &= \beta_3 \cdot \left(V_{RF}^{+} - V_{LO,DC} - V_{Tn,3} - \frac{V_{LO}^{-} - V_{LO,DC}}{2}\right) \cdot (V_{LO}^{-} - V_{LO,DC}) \\
I_{DS,4} &= \beta_4 \cdot \left(V_{RF}^{-} - V_{LO,DC} - V_{Tn,4} - \frac{V_{LO}^{+} - V_{LO,DC}}{2}\right) \cdot (V_{LO}^{+} - V_{LO,DC}).
\end{aligned} \tag{1}$$

The bulk effect gives in first order a linear change around the bias point which is cancelled with the double balanced structure [6]. Assuming perfect matching and no bulk-effect, the output signal is then

$$\begin{aligned}
V_{out}^{+} - V_{out}^{-} &= R_f \cdot ((I_1 - I_4) - (I_3 - I_2)) \\
&= \beta \cdot R_f \cdot (V_{RF}^{+} - V_{RF}^{-}) \cdot (V_{LO}^{+} - V_{LO}^{-}).
\end{aligned} \tag{2}$$

Mismatch between the input transistors has two effects. β and V_T mismatches both result in the appearance of residual dc-offset voltages. These offset voltages either appear directly on the output of the mixer or they result in direct feedthrough of the RF and LO signal to the output caused by multiplication

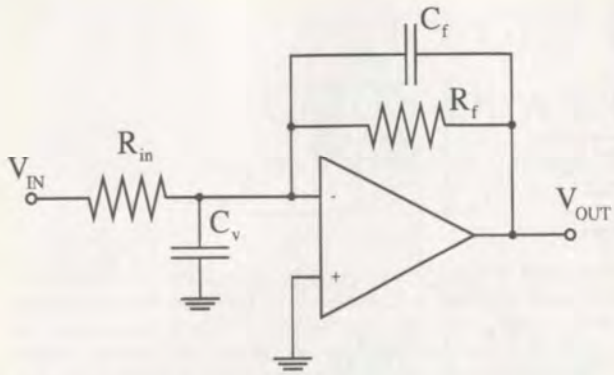

Fig. 2. The negative feedback configuration.

of these signals with the offset voltage. The RF and LO signal are however high-frequency signals. They will therefore be strongly suppressed by the added capacitors C_v. The second effect, caused by β mismatch, is the appearance of a quadratic V_{LO} component in the output signal.

$$V_{\mathrm{out}}^{+} - V_{\mathrm{out}}^{-} = \beta \cdot R_f \cdot (V_{\mathrm{RF}}^{+} - V_{\mathrm{RF}}^{-})(V_{\mathrm{LO}}^{+} - V_{\mathrm{LO}}^{-}) + \Delta\beta \cdot R_f \cdot (V_{\mathrm{LO}}^{+} - V_{\mathrm{LO}}^{-})^2. \quad (3)$$

This explains why the RF signal is best applied to the gates of the modulating transistors. A quadratic V_{RF} component would be highly unwanted. The squared RF signal has frequency components at twice its center frequency and at the baseband. The high-frequency components are filtered out, but the baseband components will degrade the wanted baseband signal. The bandwidth of this parasitic baseband signal is equal to the bandwidth of the RF signal (e.g., 100 MHz), but most of its power will be situated at the lower frequencies, in a band equal to the correlation bandwidth of the RF signal, which is about equal to the bandwidth of a transmission channel (e.g., 200 kHz). The squared LO signal results only in an extra dc component at the output of the opamp. This dc signal can also be a problem. It can be as large as the wanted signal and in that case it will saturate the succeeding filters. There are however techniques available to suppres the dc component without generating to much distortion. One of them is the use of a DSP which measures the dc component and then suppresses it, using a dynamic and nonlinear algoritm [14].

III. Mixer Design

The dc biasing levels of the RF and LO signal must be chosen carefully. There will be a lot of distortion when the modulating transistors are not kept in the triode region at all times. The smallest possible level that can appear at the gates (i.e., $V_{\mathrm{RF,DC}} - V_{\mathrm{RF,AC}}$) must be at least a V_T higher than the largest possible source level (i.e., $V_{\mathrm{LO,DC}}$). Otherwise the transistors will be turned off during a mixing period. Saturation of the modulated transistors will appear when the largest drain-source voltage V_{DS} (i.e., $V_{\mathrm{LO,AC}}$) becomes higher than the smallest $V_{\mathrm{GS}} - V_T$ (i.e., $V_{\mathrm{RF,DC}} - V_{\mathrm{RF,AC}} - V_{\mathrm{LO,DC}} - V_T$). However, saturation does not directly result in distortion. The cross-coupled double balanced structure makes sure that all quadratic components in the voltage to current conversion characteristic of the modulated transistors are cancelled out [9], [10]. The LO dc level is taken to be 1.15 V, making the maximal LO signal that can be applied 4.6 V_{ptp} differential (i.e., 17.2 dBm). An RF dc level of 3.85 V allows an input signal of 4 times $V_{\mathrm{RF,DC}} - V_{\mathrm{LO,DC}} - V_T$, which gives 8 V_{ptp} differential or 22.0 dBm for the 1.2 μm CMOS process which has been used for the mixer which is presented here. These are very high values for an RF mixer, resulting in a topology which renders an excellent linearity. Saturation will occur when $V_{\mathrm{RF}} + V_{\mathrm{LO}} > 8$ V_{ptp}. The applied LO signal is for this reason limited to 2.5 V_{ptp}, so that an RF signal of 5.5 V_{ptp} still can be applied without driving any of the modulated transistors into its saturation region.

IV. Frequency Domain Behavior

The well known negative feedback configuration of Fig. 2 suppresses any signal at the virtual ground node when a perfect opamp is used. An opamp has however always a limited gain-bandwidth GBW and dc-gain A_0. With a limited GBW becomes the transfer function from the input to the virtual ground (A_0, C_f, and C_v are not taken into account)

$$\frac{V_v}{V_{\mathrm{in}}} = \frac{\dfrac{R_f}{R_{\mathrm{in}}} \cdot j\dfrac{\omega}{2\pi \cdot \mathrm{GBW}}}{1 + \dfrac{R_f + R_{\mathrm{in}}}{R_{\mathrm{in}}} \cdot j\dfrac{\omega}{2\pi \cdot \mathrm{GBW}}} \approx \frac{A \cdot j\dfrac{\omega}{2\pi \cdot \mathrm{GBW}}}{1 + A \cdot j\dfrac{\omega}{2\pi \cdot \mathrm{GBW}}}. \quad (4)$$

The transfer function from the input to the output is

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{-\dfrac{R_f}{R_{\mathrm{in}}}}{1 + \dfrac{R_f + R_{\mathrm{in}}}{R_{\mathrm{in}}} \cdot j\dfrac{\omega}{2\pi \cdot \mathrm{GBW}}} \approx \frac{-A}{1 + A \cdot j\dfrac{\omega}{2\pi \cdot \mathrm{GBW}}}. \quad (5)$$

Normally, the conclusion to be drawn from these equations is that the GBW must be a certain factor higher than the highest frequency component that has to be processed. This is also true if the circuit would be used as lowpass filter with an extra capacitor C_f in the feedback loop. However, here in the mixer topology is the situation different. There is a very large spectrum of input currents to the virtual ground node, basically starting from dc up to twice the LO frequency (more than 2 GHz), but the wanted signal takes up only a few hundred kHz situated at the baseband. The output bandwith BW, given in (5) as GBW/A, only has to be 500 kHz or more. By designing it to be 1 MHz this specification is fulfilled independent of absolute parameter variations. Equation (5) shows that this limited bandwidth can be realized by using an opamp with a small GBW. In combination with a feedback capacitor C_f can the bandwidth be lowered further and can it be positioned more accurately. The use of an opamp with a small GBW poses however a problem. As (4) reflects, beyond the BW is the input signal directly transferred to the virtual ground node. It is not suppressed anymore by the opamp via the feedback construction. The solution for this problem can

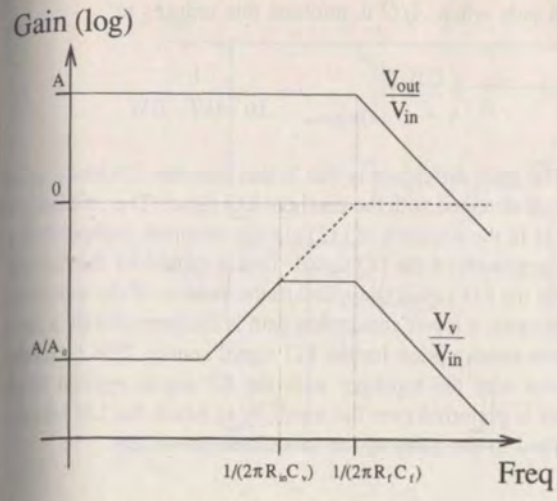

Fig. 3. Transfer function of the mixer used as amplifier.

be found in adding extra capacitance to the virtual ground nodes. This introduces an extra pole in both (4) and (5) situated at $1/(2\pi \cdot R_{\text{in}}C_v)$. In order to suppres the signals appearing on the virtual ground without changing the output bandwidth, its value must be positioned between $1/(2\pi \cdot R_f C_f)$ and the BW. Fig. 3 displays the transfer function from the input to the virtual ground and the output.

V. Noise, Power Consumption, and Optimization

The noise figure (NF) of the HF mixer is a very important parameter in receiver design. In a receiver is the mixer positioned directly after the LNA and a mixer with a high NF can only be used in combination with a high-quality LNA. In this case the LNA must have a high gain which, in turn, can only be allowed when the antenna signal is first filtered with a high Q HF filter. The problem with mixers is that its NF can not be made arbitrarely small. Their NF can not even be in the proximity of the NF's that can be achieved with LNA's. This is due to the intrinsic nature of the mixing process.

The two main noise sources in the presented mixer are the modulated input transistors in the triode region and the input stage of the LF opamp. The thermal output noise density generated by these devices is (with the factor 2 introduced by the differential operation)

$$dv_{\text{out}}^2 = 2 \cdot 4kT \cdot \left(\frac{2}{3} \cdot \frac{1}{g_{m,\text{in,eq}}} \cdot (R_f \cdot 2g_{\text{DS}})^2 + 2g_{\text{DS}} \cdot R_f^2 \right) \cdot df. \tag{6}$$

Equation (6) gives the output noise density for the mixer biased in its static operation point. The modulated transistors have however, under transient conditions, always the same impedance ($2g_{\text{DS}}$) to the virtual ground nodes. For this reason in (6), for the presented topology, also a good measure for the output noise density under transient operation conditions. The equivalent input noise can be found by deviding this expression by the conversion gain G. The conversion gain is defined as the ratio of the output signal over the input signal $(V_{\text{out}}^+ - V_{\text{out}}^-/V_{\text{RF}}^+ - V_{\text{RF}}^-)$ and follows from (2):

$$G = \frac{(V_{\text{out}}^+ - V_{\text{out}}^-)_{\text{ptp}}}{(V_{\text{RF}}^+ - V_{\text{RF}}^-)_{\text{ptp}}} = \frac{1}{\sqrt{2}} \cdot \frac{1}{\sqrt{2}} \cdot \beta \cdot R_f \cdot (V_{\text{LO}}^+ - V_{\text{LO}}^-)_{\text{ptp}}. \tag{7}$$

The first $\sqrt{2}$ appears because the multiplication is performed with a sine and not a square wave. This implies that the rms value of the LO signal has to be used. The second $\sqrt{2}$ is necessary because only the low-frequency mixing product is regarded as wanted. Deviding (6) by (7) results in

$$\begin{aligned} dv_{\text{in}}^2 = \frac{1}{G^2} \cdot dv_{\text{out}}^2 &= \left(\frac{2}{R_f \cdot \beta \cdot (V_{\text{LO}}^+ - V_{\text{LO}}^-)_{\text{ptp}}} \right)^2 \cdot dv_{\text{out}}^2 \\ &= 8kT \cdot \left(\frac{4g_{\text{DS}}}{\beta \cdot (V_{\text{LO}}^+ - V_{\text{LO}}^-)_{\text{ptp}}} \right)^2 \\ &\quad \cdot \left(\frac{2}{3} \cdot \frac{1}{g_{m,\text{in,eq}}} + \frac{1}{2g_{\text{DS}}} \right) \cdot df \\ &\equiv 8kT \cdot \left(2 \cdot \frac{2g_{\text{DS}}}{\Delta g_{\text{DS}}} \right)^2 \cdot \left(\frac{2}{3} \cdot \frac{1}{g_{m,\text{in,eq}}} + \frac{1}{2g_{\text{DS}}} \right) \cdot df. \end{aligned} \tag{8}$$

The factor $4g_{\text{DS}}/\Delta g_{\text{DS}}$ is the extra term intrinsic to any mixer or double balanced structure. It is equal to the ratio between the gain of the mixer used as single balanced amplifier and the conversion gain A/G. For low noise, this term should be as low as possible. The noise can also be lowered by using a larger $g_{m,\text{in,eq}}$ and g_{DS}, but this is at the expense of a higher power consumption. The minimal value for this extra term is found when the swing of the LO signal is maximal.

$$\frac{A}{G} = 2 \cdot \frac{2g_{\text{DS}}}{\Delta g_{\text{DS}}} = \frac{4 \cdot \beta \cdot (V_{\text{GS}} - V_T)}{\beta \cdot (V_{\text{LO}}^+ - V_{\text{LO}}^-)_{\text{ptp}}} = 4 \cdot \frac{V_{\text{RF,DC}} - V_{\text{LO,DC}} - V_T}{(V_{\text{LO}}^+ - V_{\text{LO}}^-)_{\text{ptp}}} \tag{9}$$

$$\left(\frac{A}{G} \right)_{\text{min,RF@gates}} = \frac{4 \cdot (V_{\text{RF,DC}} - V_{\text{LO,DC}} - V_T)}{2 \cdot V_{\text{LO,DC}}} \tag{10}$$

$$\left(\frac{A}{G} \right)_{\text{min,LO@gates}} = \frac{4 \cdot (V_{\text{RF,DC}} - V_{\text{LO,DC}} - V_T)}{2 \cdot (V_{\text{RF,DC}} - V_{\text{LO,DC}} - V_T)} = 2. \tag{11}$$

So, according to (11) for the case in which the LO signal is applied to the gates of the modulated transistors, this means that the mixing function adds at least 6 dB to the NF. For the rest is the NF directly determined by the conductivity of a single modulated transistor (g_{DS}) and by the transconductance value of the opamp input stage ($g_{m,\text{in,eq}}$), just like in any other amplifier with negative feedback. The noise of the opamp input stage can be made sufficiently small without requiring too much power by using large input transistors (and a small $V_{\text{GS}} - V_T$). This is possible because the opamp only has to be LF and there is already standing 25 pF (C_v) at the input nodes. The value of g_{DS} can not be made arbitrarely large because this conductor has to be driven by the LO.

From (10) it might seem that the NF can be made arbitrarely small when the RF signal is applied to the gates by taking $V_{\mathrm{RF,DC}} - V_T < 2 \cdot V_{\mathrm{LO,DC}}$. This implies however a reduction of the input swing and in this way the dynamic range (DR) at the input is not improved. It is not only necessary to minimize the NF of a mixer. It is the input signal capability (i.e., the DR) which must be compared with the power consumption. A good measure for the performance of a mixer is therefore the DR per Watt. Here this gives

$$\begin{aligned}\left(\frac{\mathrm{DR}}{P}\right)_{\mathrm{RF@gates}} &= \left(\frac{S}{N}\right)^2 \cdot \frac{1}{P} \\ &= \frac{(V_{\mathrm{RF,DC}} - V_{\mathrm{LO,DC}} - V_T)^2}{8kT \cdot \left(\frac{A}{G}\right)^2 \cdot \frac{1}{2g_{\mathrm{DS}}} \cdot \mathrm{BW}} \\ &\quad \cdot \frac{1}{(V_{\mathrm{LO}}^{+} - V_{\mathrm{LO}}^{-})^2 \cdot g_{\mathrm{DS}}} \\ &= \frac{1}{16 \cdot 4kT \cdot \mathrm{BW}}. \end{aligned} \tag{12}$$

Equation (12) takes does not take the power consumption and the noise of the opamp into account. Only a low-frequency opamp is needed and its power consumption and noise can therefore be made sufficiently small. $4kT \cdot$ BW is the intrinsic noise power of a signal with bandwidth BW and the noise of any electronic buiding block with input bandwidth BW can thus never be lower than this value. The factor 1/16 can herefore be defined as the power efficiency for this mixer. It is independant of the choosen input swing, noise level, input bandwidth, or power consumption. In fact, this power efficiency depends, for the presented topology and in first order, only on the topology itself and it can be defined for many other building blocks likes LNA's, amplifiers, filters, A/D converters and any other type of mixer.

$$\eta = \frac{S_{\mathrm{input}}^2}{P_{\mathrm{total}}} \cdot \frac{P_{\mathrm{intrinsic\ noise}}}{N_{\mathrm{input}}^2} \left[\frac{V^2}{\mathrm{Watt}} \cdot \frac{4kT}{V^2/\mathrm{Hz}} = \mathrm{dimensionless}\right]. \tag{13}$$

The power efficiency of a high-quality low-frequency amplifier can be almost 50%. The power efficiency of the presented mixer topology, not taking the power efficiency of the LO signal source into account, is almost 6% and this is, for high-frequency mixers, a very high value.

Equation (12) is slightly different when the LO signal instead of the RF signal is applied to the gates of the modulated transistors

$$\begin{aligned}\left(\frac{\mathrm{DR}}{P}\right)_{\mathrm{LO@gates}} &= \frac{S}{N} \cdot \frac{1}{P} \frac{V_{\mathrm{LO,DC}}^2}{8kT \cdot \left(\frac{A}{G}\right)^2 \cdot \frac{1}{2g_{\mathrm{DS}}} \cdot \mathrm{BW}} \\ &\quad \cdot \frac{1}{4 \cdot V_{\mathrm{LO,DC}}^2 \cdot g_{\mathrm{DS}}}. \end{aligned} \tag{14}$$

And only when A/G is minimal this reduces to

$$\left(\frac{\mathrm{DR}}{P}\right)_{\mathrm{LO@gates}} = \frac{1}{16 \cdot 4kT \cdot \mathrm{BW}}. \tag{15}$$

The main difference is that in this case the efficiency of 6% is only obtained with the maximal LO signal. The efficiency of 6% is in the situation of (12) always obtained, independant of the amplitude of the LO signal. This is caused by the fact that, when the LO signal is applied to the sources of the modulated transistors, a lower conversion gain is compensated by a lower power consumption for the LO signal source. This is another reason why the topology with the RF signal applied to the gates is preferred over the topology in which the LO signal is applied to the gates of the modulated transistors.

VI. Realization

The mixer has been designed and realized in a 1.2 μm CMOS process to illustrate the high linearity and high input frequency capabilities of the proposed topology. The RF and LO signal are externally made differential by means of baluns. They are, as stated in Section III, chosen to be biased at, respectively, 3.85 V (for the RF signal, applied at the gates) and 1.15 V (for the LO signal, applied at the sources and drains) because this renders a $V_{\mathrm{GS}} - V_T$ for the modulated transistors of 2.5 V. Such a large value for the $V_{\mathrm{GS}} - V_T$ results in an excellent linearity and a high input bandwidth. The applicable voltage swing for the RF input is peak-to-peak four times this $V_{\mathrm{GS}} - V_T$. The large $V_{\mathrm{GS}} - V_T$ makes it also possible to realize a large g_{DS} with a small transistor, which gives small parasitic capacitances (less than 20 fF) and thus a high input bandwidth. The W/L of the modulated transistors is 6, their g_{DS} is 1 mS. These four modulated transistors are the only high frequency part on the chip and they take up very little area. Because of their small parasitic capacitances is the on-chip RF to LO crosstalk, which is mainly determined by the absolute mismatch between C_{GS} values, also very small. Hence, RF to LO crosstalk is mainly caused by off-chip crosstalk and crosstalk between the bonding wires. The input bandwidth is also completely determined by the bonding pads capacitances and as a result extremely high frequency performances can be achieved.

The opamp topology is shown in Fig. 4. It is a load compensated folded cascode structure succeeded by a source follower which performs buffering and level shifting. The opamp runs on a single 5 V power supply. The output dc level is 1.15 V. It is kept on this level with a standard type common-mode feedback. The GBW of the opamp is 100 MHz, but because of the partial feedback the second nondominant pole is situated at only 30 MHz. The feedback resistors over the opamp are 60 kΩ, which makes the conversion gain very high. The conversion gain is almost 20 dB for a 12 dBm LO signal. An extra lowpass filter of 1 MHz is implemented with the feedback capacitors C_f (2.5 pF). This small output bandwidth and the high conversion gain are required by the zero-IF structure. The extra filtering and amplification that is performed in the output stage of the mixer relaxes the

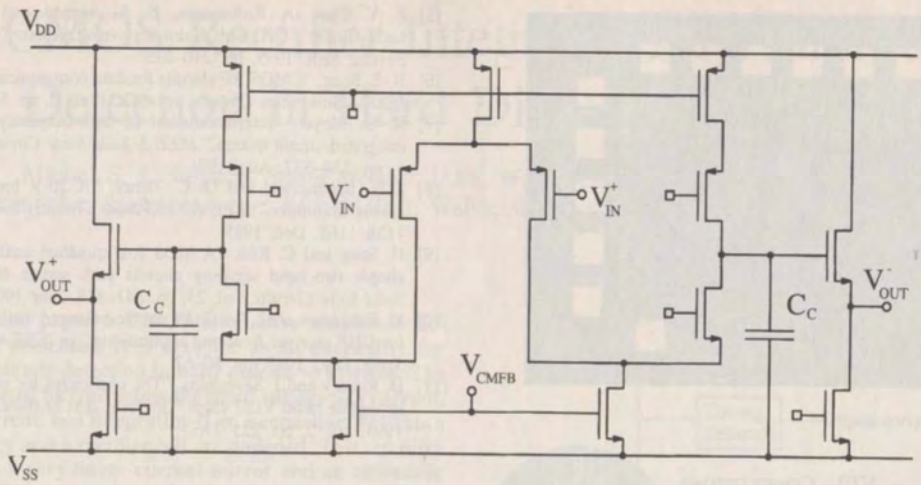

Fig. 4. The opamp topology.

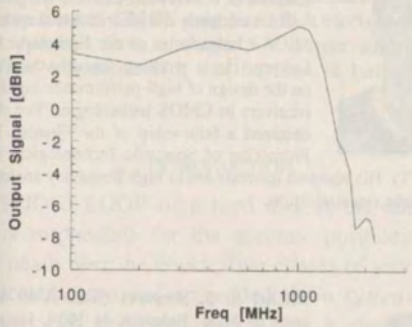

Fig. 5. The input bandwidth measurement.

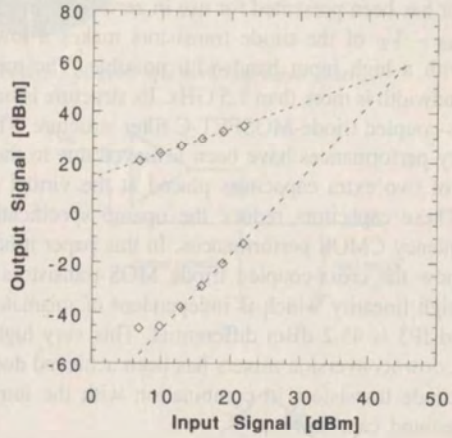

Fig. 6. The IP3 measurement.

specifications for the output stage of the opamp and for the succeeding stages of the reciever.

VII. Results

The realized mixer is measured via external high frequency baluns for both the RF and LO input. These baluns are transformers which convert a 50 Ω signal source into two symmetrical 100 Ω signals sources superimposed on a common-mode dc bias voltage. Fig. 5 shows the measured input bandwidth. It is from dc to 1.5 GHz. The input bandwidth is measured at 6 dB attenuation, because both input signals are falling off at the same time. The measured 1.5 GHz maximum input bandwidth is equal to the specified bandwidth of the baluns which have been used to generate the differential input signals. The output bandwidth is determined by the untuned value of $1/R_f C_f$. For the application in mind it must be at least 500 kHz and it is designed to be 1 MHz so that it can cope with the large absolute processing value spreads. The measured output bandwidth is 780 kHz. The measured conversion gain is 18 dB for a 12 dBm differential LO signal.

The IP3 measurement, shown in Fig. 6, proves that the linearity is very high. The IP3 is 45.2 dBm. This value does not depend on the magnitude of the LO signal. An input signal of 22 dBm, the theoretic value for the maximal applicable input swing, gives an IM3 of −46.4 dB. The IM3 measurement was performed with the downconverted carriers lying out of the output band (at 10 MHz) and the IM3 product lying in the passband (at 200 kHz). This made it possible to measure the distortion of the input stage and not the output stage for signals which would normally produce an output signal of up to 40 dBm. The measured noise figure (NF, compared to a 50 Ω noise source) is 32 dB. This is mainly caused by the input stage of the opamp which has not been optimized for low noise. By using large input transistors for the low-frequency opamp, which has no effect on the high frequency performance of the mixer, the noise figure can easily be improved down to 24 dB. The intermodulation free dynamic range (IMFDR3) of this mixer is 59.6 dB. The mixer is designed in a 1.2 μm CMOS process. The measured power consumption is 1.3 mW which is all taken up in the low-frequency opamp. The total chip area is 1 mm^2. The modulated transistors only take up 300 μm^2 of this area. A microphotograph of the realized chip is shown in Fig. 7.

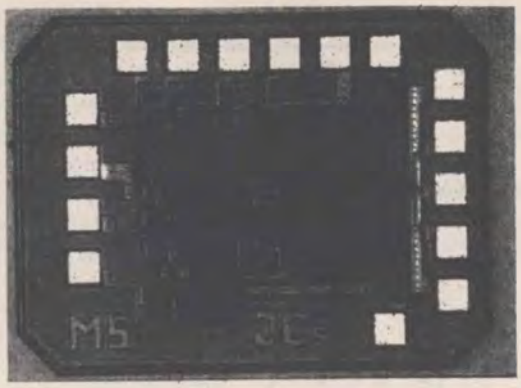

Fig. 7. Chip microphotograph.

VIII. Conclusions

In this paper it is shown how the low resistance of small MOS transistors in the triode area can be used to design a high frequency downconversion mixer. A continuous-time multiplier has been presented for use in zero-IF receivers. The large $V_{GS} - V_T$ of the triode transistors makes a low noise mixer with a high input bandwidth possible. The measured input bandwidth is more than 1.5 GHz. Its structure is based on the cross-coupled triode-MOSFET-C filter structure. The high frequency performances have been achieved due to the introduction of two extra capacitors placed at the virtual ground nodes. These capacitors reduce the opamp specifications to low frequency CMOS performances. In this paper it has been shown how the cross-coupled triode MOS-transistors render a very high linearity which is independent of mismatch. The measured IP3 is 45.2 dBm differential. This very high value for GHz downconversion mixers has been achieved due to the use of triode transistors in combination with the introduced virtual ground capacitors.

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Doug DeMaw

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Doug DeMaw

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6

MIXERS, BALANCED MODULATORS AND DETECTORS

There is little difference between the functions of mixers, balanced modulators, and detectors in standard communications circuits. All three operate on the principle of combining two frequencies to produce a third one. The design goals are, therefore, quite similar. We are interested in having any of the three circuits perform with high dynamic range, minimum distortion, and good suppression or isolation between the various ports of the circuit device.

We have a number of choices open to us when choosing a particular mixer, modulator, or detector, and the best circuit for the application will be founded on cost effectiveness, performance standards, and available circuit space in the composite product. In all examples we can expect optimum performance from balanced circuits as opposed to single-ended circuits. We need to make a choice between passive and active versions of the three types of circuits, since passive devices yield a conversion loss, and active circuits usually ensure a conversion gain. It should be said, however, that an active mixer, modulator, or detector can exhibit unity gain, or even a conversion loss. This will depend upon how the device is used in the circuit, as we will learn later in the chapter. Figure 6.1 provides a relative comparison between the three circuits we shall examine in this discussion.

6.1. MIXERS

The most common use of mixers is found in receivers and heterodyne-frequency generators in transmitters. We have our choice between

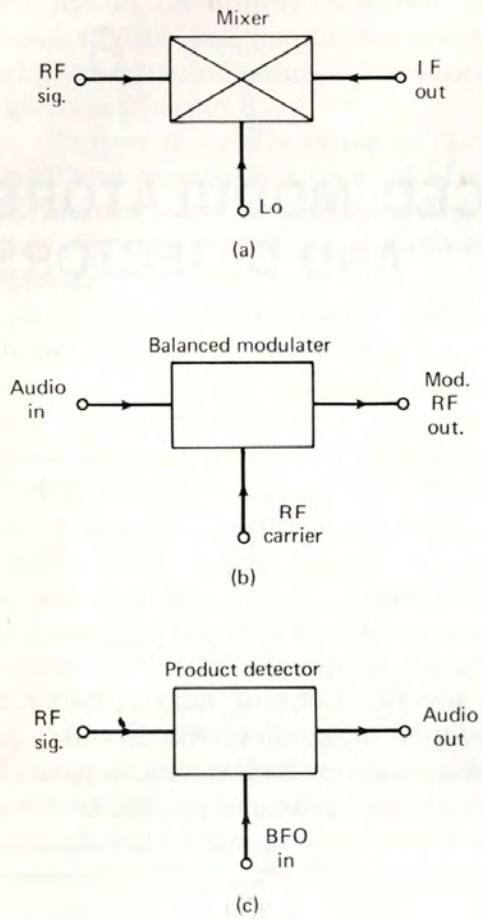


Figure 6.1 Comparison of a mixer, balanced modulator, and product detector.

passive (no operating voltage required) and active (operating voltage needed) devices. Furthermore, we can elect to use the most fundamental form of mixer, the single-ended variety, if high performance is not mandatory, and when equipment cost must be held within specified constraints. The simplest passive mixer is one that contains a single diode. Circuits of this type are sometimes used in UHF and microwave receivers, but are not attractive in circuits that operate below approximately 450 MHz. In the lower VHF region and at high and medium frequencies, it is more desirable to use two diodes in a singly balanced configuration or four diodes in a doubly balanced mixer (DBM). In all instances there will be a conversion loss that is usually of the order of -5 to -8 dB. Additionally, diode passive mixers require substantially greater local-oscillator (LO) power levels to provide the required amount of LO injection to the mixer, as referenced to an active mixer.

Objectively, we want the mixer to withstand strong applied RF signals without creating excessive distortion products. It should also be able to accommodate strong signals without producing cross-modula-

tion effects and gain compression. Gain compression is the point at which a 1-dB reduction in mixer output occurs when the RF input signal level is increased until that value of compression takes place.

Another important consideration is the mixer noise figure (NF). This is especially important above, say, 15 MHz, where the atmospheric noise is often lower in amplitude than is the receiver front-end noise. Mixers are much noisier in mixer service than they are as RF amplifiers when the same device is used in each application. When the mixer noise becomes too great for the operating frequency, we can reduce the effective receiver NF by using a low-noise RF amplifier ahead of the mixer. Its gain must exceed that of the mixer if an improvement is to be realized. Also, the local oscillator and its associated amplifiers must be as spectrally pure as possible in terms of noise before the LO energy is injected into the mixer. Excessive noise output from the LO system will effectively increase the mixer noise figure. Eliminating this noise is an important design problem if we are to strive for high receiver performance. The penalty for using a preamplifier is observed in reduced mixer dynamic range, owing to the increased RF signal level that is applied to the mixer input port. It can be seen from this discussion that all manner of design trade-offs accompany the implementation of a mixer.

Still another important mixer parameter is the intermodulation distortion (IMD) products generated within the device. The IMD should be as low as possible to ensure high dynamic range. IMD is manifested as additional unwanted receiver responses to one or more strong signals in the receiver passband. The effect is one of having a single incoming signal appear in several places as the receiver is tuned away from the signal that is causing the IMD responses. The IMD products are numerically related to the interfering signal and another strong signal nearby in the receiver passband. The IMD characteristics of a given mixer can be determined in laboratory tests by applying two RF signals at the mixer input (two-tone test) and observing the third-order distortion products at the mixer output. A block diagram of a suitable setup for mixer evaluation is shown in Fig. 6.2. A spectrum analyzer, two signal sources, a LO source, step attenuators, a combiner, and post-mixer amplifier and lattice filter are required. The post-mixer amplifier must be as good as or better than the mixer under test (MUT) in terms of IMD. A CATV bipolar transistor (2N5109) meets the requirement easily when operated in a linear broadband configuration.

Port-to-port signal isolation is a vital mixer consideration. That is, we do not want the LO energy to appear at the RF or IF ports of a mixer in sufficient magnitude to create additional frequencies through unwanted mixing action. Doubly balanced mixers offer the best solution to port isolation. Singly balanced mixers are the second choice, and single-ended mixers are the worst we might select for resolving the problem.

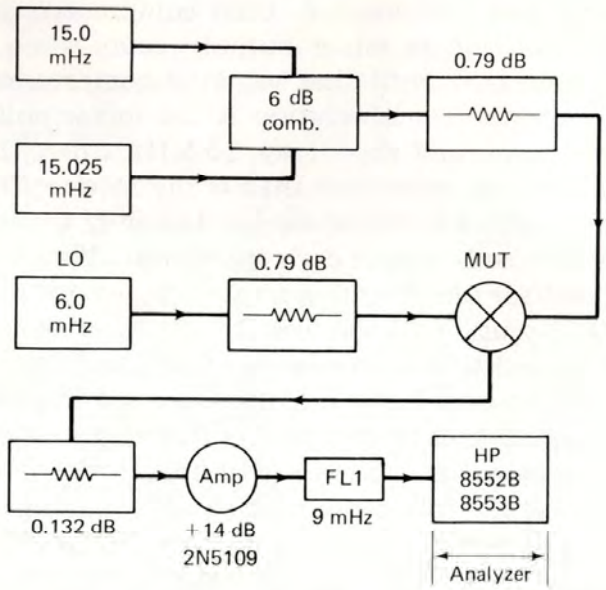


Figure 6.2 Block diagram showing the test setup for measuring mixer dynamic range.

Maximum mixer conversion gain will occur only when the input and output of the mixer are well matched to the characteristic impedances of the source and load. Intentional mismatch is often applied to reduce the conversion gain and to enhance the IMD characteristics by operating the output of an active mixer at low impedance levels. This technique reduces the ac voltage swing and helps to keep the collector or drain of a mixer transistor within a more linear operating range.

6.1.1 Single-Ended Mixers

The practicality of active single-ended mixers is realized in the design of inexpensive receivers, such as the pocket-sized AM band transistor radio. A bipolar-transistor mixer is capable of delivering conversion gains as great as 30 dB under well-matched conditions and careful biasing. Unfortunately, the dynamic range of such a mixer is very poor, which helps to explain the unsatisfactory strong-signal performance of most imported "pocket radios." But this type of mixer contributes to a reduction in receiver stages with respect to overall receiver gain. RF amplifiers are seldom used in receivers of this general variety.

Figure 6.3 contains the circuit of a typical single-ended bipolar mixer. Approximate values are listed for the components and operating voltages for best performance. A mixer is necessarily a nonlinear device and would operate, ideally, with a square-law response. Therefore, the

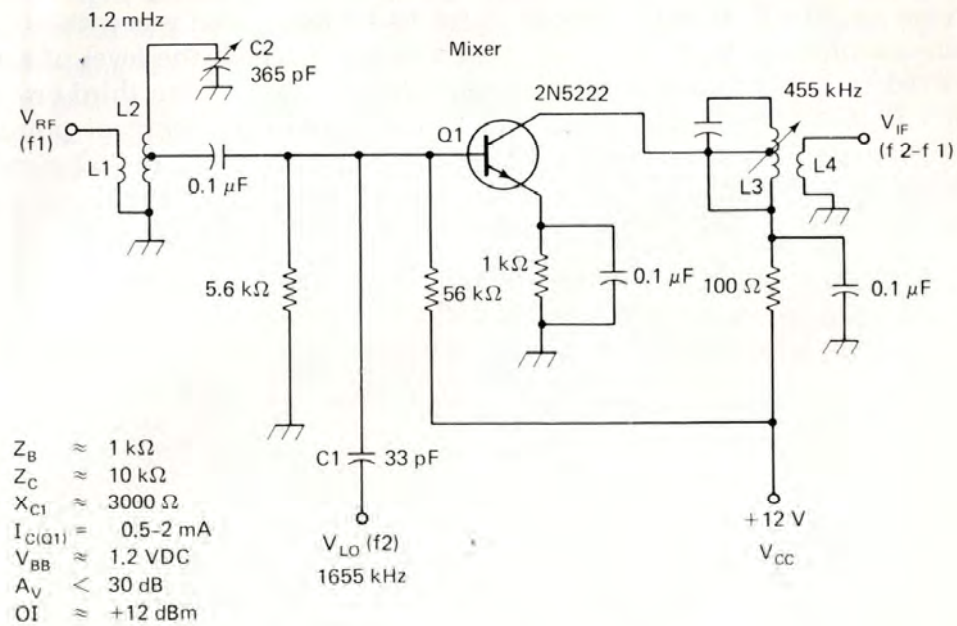


Figure 6.3 Practical circuit for a bipolar-transistor mixer.

forward bias on $Q1$ of Fig. 6.3 is held to a low value. The V_{BB} used will aid conversion gain and enhance the weak-signal response of the mixer. The base of $Q1$ is tapped toward the grounded end of $L2$ to effect an impedance match between the mixer input and the antenna. Typically, the input impedance of this kind of mixer is 1000 Ω.

The collector could be connected directly to the top end of $L3$, since the characteristic impedance of the collector will be on the order of 10,000 Ω with the biasing specified in Fig. 6.3. By tapping the collector down on the tuned circuit we can control the conversion gain (reduce it) to a desired value. Also, as the collector is tapped down on the tuned circuit, we are minimizing the loading effects on the tuned circuit, thereby elevating the Q. This provides increased selectivity at the mixer output. This mixer requires very low injection power from the LO. Since we are applying 0.5 V rms of LO signal across the base-emitter port, the power requirements will be minimal. $C1$ should have fairly high reactance at the signal frequency to prevent undue loading of the input tuned circuit by the LO circuitry. Light coupling via $C1$ will also help reduce oscillator pulling when $C2$ is adjusted.

Mixer distortion (IMD) can be defined either in terms of the IMD products being a specified number of decibels below the desired output signal level (IF) or by means of the third-order output intercept number. The intercept point is an imaginary point established when a 10-dB increase in the two input test tones causes the desired mixer output

products to increase by 10 dB, but the third-order IMD products increase by 30 dB. In other words, if we had a mixer that was without a gain-compression trait, we could find a point at which the level of the desired output product would be equivalent to that of the third-order IMD product. We would define this as the third-order intercept point, the position on a set of curves where the desired output-product curve intersected with the curve of the third-order product. This is shown in Fig. 6.4. The curves in this hypothetical example converge at the +20

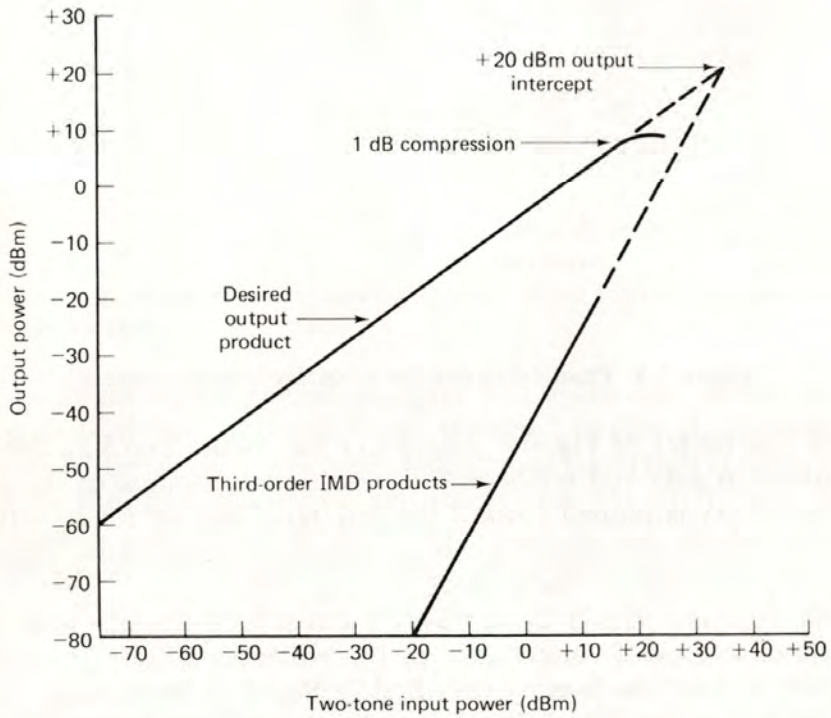


Figure 6.4 Curves that show the third-order output intercept point of a mixer.

dBm output intercept point. It becomes apparent that the greater the output intercept number, the higher is the dynamic range of the mixer. In the case of the circuit of Fig. 6.3 the output intercept is quite low, +12 dBm. Strong mixers yield numbers as great as +45 dBm. A typical number for a medium-quality receiver would be on the order of +25 dBm.

In terms of mixer performance our concern is for the third-order *input intercept* characteristic, even though it is related directly to the output intercept number. The input intercept can be obtained by subtracting the conversion gain of the mixer from the output. Hence, if the conversion gain were 10 dB and the output intercept were +35 dBm,

the input intercept would be +25 dBm. It can be seen from this that it is important to minimize the mixer conversion gain in the interest of elevating the input-intercept characteristic. Frequently, this is done in an active mixer by using broadband techniques and introducing intentional mismatches at the input and output ports. Irrespective of the mixer input intercept, the final determination of receiver performance is based on the *receiver input intercept* number. This dictates that care must be given to the design of the input circuitry, inclusive of the RF amplifier that precedes the mixer, in the event that such a stage is used.

A JFET is capable of better performance in a single-ended mixer, compared to a bipolar transistor. Figure 6.5 illustrates how we might

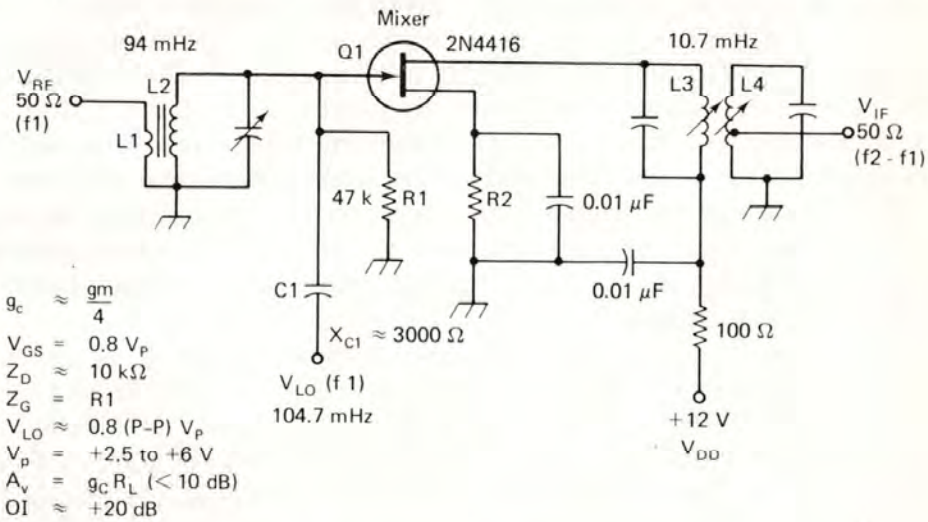


Figure 6.5 Practical JFET single-ended mixer.

use a 2N4416 or similar FET as a mixer. Conversion transconductance (g_c) will be approximately 0.25 the g_m of the same device in amplifier service. Hence, if the FET was rated at 5000 μS as an amplifier, the conversion transconductance would be roughly equal to 5000/4, or 1250 μS. Once we know this number we can approximate the conversion gain by

$$A_V = g_c R_L$$

where A_V is the voltage gain in decibels, g_c is the conversion transconductance in siemens, and R_L is the drain load in ohms. Therefore, if we had a 1250 μS (0.0125 S) g_c and an effective mixer drain load of 1000 Ω, the gain would be

$$A_V = 0.0125 \times 1000 = 12.5 \text{ dB}$$

We will impair mixer performance, however, if we attempt to elevate the conversion gain by increasing the drain load impedance. In the

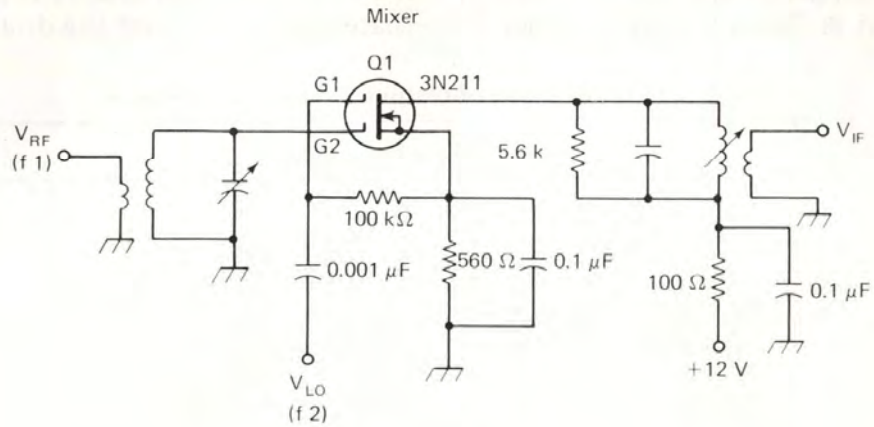
circuit of Fig. 6.5 we would be prudent to tap the FET drain toward the V_{DD} end of $L3$ to force the drain down to a lower impedance than it sees in the circuit, as shown. Typically, the drain impedance will be approximately 10 kΩ with a circuit such as that of Fig. 6.5. This technique will reduce the peak drain-voltage swing, thereby reducing the change in junction capacitance. The latter, which introduces a *varactor effect*, results in the generation of harmonic currents.

Source resistor $R2$ is selected to yield a gate-source dc potential that is 0.8 the pinchoff voltage (V_p) of the FET. In practice, this will be a somewhat arbitrary number, as the manufacturers' data sheets are not specific. V_p is not listed in most of the literature, but we can use the more common parameter, $V_{GS(\text{off})}$, which is of equal magnitude to V_p, but of opposite polarity. For a 2N4416 the spread is listed as -2.5 to -6 V, equating to a V_p of +2.5 to +6 V. Arbitrarily, we can assume a midrange value for V_p, accepting in our design example a voltage of 4.25. Therefore, $R2$ will be chosen to yield a V_{GS} of 0.8 × 4.25, or 3.4 V. Because the listed $V_{GS(\text{off})}$ values are rather nebulous, we will fare much better in the final analysis by making empirical adjustments to the V_{GS} while the mixer is in operation. A compromise between IMD and conversion gain must be made when establishing the operating conditions. Ideally, the g_c should be held below 10 dB in the interest of good mixer performance.

Under the foregoing guidelines the LO injection should be approximately 0.8 p-p the V_p value. An output intercept of +20 dBm is typical for the mixer of Fig. 6.5, although a theoretical value of +30 dBm exists for FETs such as the U310 in a fully optimized circuit. Since gate injection of the LO is suggested in our circuit example, $C1$ should follow the rule set forth for the circuit in Fig. 6.3. Source injection can be used in this style of circuit, but substantially more LO power will be required and mixer instability may result.

Dual-gate MOSFETs provide comparable performance to JFETs in mixer circuits. They offer the advantage of having a pair of gates rather than a single gate, thus making it easy to introduce the LO and RF signals at separate ports. Normally, the LO energy is applied to gate 2 and the RF input signal is routed to gate 1, as demonstrated in Fig. 6.6. This type of FET is rather fragile in terms of excessive gate voltage, compared to a JFET, but the isolation between the two gates is advantageous toward minimizing LO pulling effects and interaction between the LO output circuitry and the RF signal input circuit. Some manufacturers rate the gate-to-gate isolation as high as 50 dB, but in a practical circuit that magnitude of signal separation would be difficult to achieve. A 25- to 30-dB isolation value is more common, owing to stray coupling external to the MOSFET.

Gate 2 can be biased separately by means of a resistive voltage divider connected to the V_{DD} line. Comparable performance can be ob-



$$g_c \approx \frac{gm}{4}$$
$$V_{G2S} \approx 2\text{ mA}$$
$$I_D \approx 1\text{ V}$$
$$V_{LO} \approx 5\ V_{P\text{-}P}$$
$$OI \approx +16\text{ dBm}$$
$$A_V = g_c R_L\ (< 10\text{ dB})$$

Figure 6.6 Improved single-ended mixer performance can be realized by using a dual-gate MOSFET, which permits two-port injection.

tained, however, by strapping gate 2 to the source through a 100-kΩ resistor, as seen in Fig. 6.6. With a 560-Ω source-bias resistor, an effective gate 2 potential of 1 V will result. Under these conditions, a peak-to-peak LO injection of 5 V will enable the mixer to have reasonable conversion gain and acceptable IMD characteristics. Optimum third-order output intercept for a 3N211 was noted during laboratory tests when V_{g2s} was set at 4.2 V, and with an 8-V p-p LO injection level. This resulted in a third-order output intercept of +16 dBm. Lowering the drain load impedance of $Q1$ in Fig. 6.6 would have aided the output intercept number. The 5.6 kΩ resistor across the output tuned circuit pulls the drain down to an impedance that yields better IMD performance. In a test circuit that contained two 3N211 transistors in a singly balanced mixer, and with broadband coupling transformers at the input and output of the mixer, a third-order output intercept of +20 dBm was observed. The gates and drains were operated at a 200-Ω impedance. Conversion gain was approximately 6 dB when 4.2 V of V_{g2s} was applied, and with an 8-V p-p LO injection level. A 560-Ω resistor was used in each source return.

6.1.2 Balanced Mixers

Balanced mixers offer better port-to-port signal isolation than is possible with single-ended mixers. A comparison of the output products

from single-ended, singly balanced and doubly balanced mixers is presented in Table 6.1. It becomes immediately apparent that the doubly

TABLE 6.1 Comparison of Output Products from Mixers

(N)	Single-Ended Mixer				
	f_o	$2f_o$	$3f_o$	$4f_o$	$5f_o$
f_s	$f_o \pm f_s$	$2f_o \pm f_s$	$3f_o \pm f_s$	$4f_s \pm f_s$	$5f_o \pm f_s$
$2f_s$	$2f_s \pm f_o$	$2f_o \pm 2f_s$	$3f_o \pm 2f_s$	$4f_o \pm 2f_s$	$5f_o \pm 2f_s$
$3f_s$	$3f_s \pm f_o$	$3f_s \pm 3f_o$	$3f_o \pm 3f_s$	$4f_o \pm 3f_s$	$5f_o \pm 3f_s$
$4f_s$	$4f_s \pm f_o$	$4f_s \pm 2f_o$	$4f_s \pm 3f_s$	$4f_o \pm 4f_s$	$5f_o \pm 4f_s$
$5f_s$	$5f_s \pm f_o$	$5f_s \pm 2f_o$	$5f_s \pm 3f_o$	$5f_s \pm 4f_o$	$5f_o \pm 5f_s$
(0.5 N)	**Singly Balanced Mixer**				
	f_o	$2f_o$	$3f_o$	$4f_o$	$5f_o$
f_s	$f_o \pm f_s$	$2f_o \pm f_s$	$3f_o \pm f_s$	$4f_o \pm f_s$	$5f_o \pm f_s$
$2f_s$	—	—	—	—	—
$3f_s$	$3f_s \pm f_o$	$3f_s \pm 2f_o$	$3f_s \pm 3f_o$	$4f_o \pm 3f_s$	$5f_o \pm 3f_s$
$4f_s$	—	—	—	—	—
$5f_s$	$5f_s \pm f_o$	$5f_s \pm 2f_o$	$5f_s \pm 3f_o$	$5f_s \pm 4f_o$	$5f_o \pm 5f_s$
(0.25 N)	**Doubly Balanced Mixer**				
	f_o	$2f_o$	$3f_o$	$4f_o$	$5f_o$
f_s	$f_o \pm f_s$	—	$3f_o \pm f_s$	—	$5f_o \pm f_s$
$2f_s$	—	—	—	—	—
$3f_s$	$3f_s \pm f_o$	—	$3f_o \pm 3f_s$	—	$5f_o \pm 3f_s$
$4f_s$	—	—	—	—	—
$5f_s$	$5f_s \pm f_o$	—	$5f_s \pm 3f_o$	—	$5f_o \pm 5f_s$

LO = f_o, signal frequency = f_s
$2f_o \pm f_s$ = third-order product
$3f_s \pm 3f_o$ = sixth-order product, etc.
N = number of mixer products

balanced mixer is the stellar performer in terms of isolation and product suppression. It is, thus, the mixer preferred by designers of high-performance equipment.

An example of properly designed JFET singly balanced mixer is seen in Fig. 6.7. It is similar to a circuit suggested by E. Oxner of Siliconix in *Application Note AN72-1*. Dynamic balance is assured through the use of a U430 dual-FET unit. $R1$ is selected to give a V_{gs} of 0.8 the pinchoff voltage, which will be on the order of 2 V, allowing for the published spread of -1 to -4 V, $V_{gs(off)}$. Symmetrical feed is used at the mixer input by means of $T1$, $T2$, and $T3$, providing a 180° phase dif-

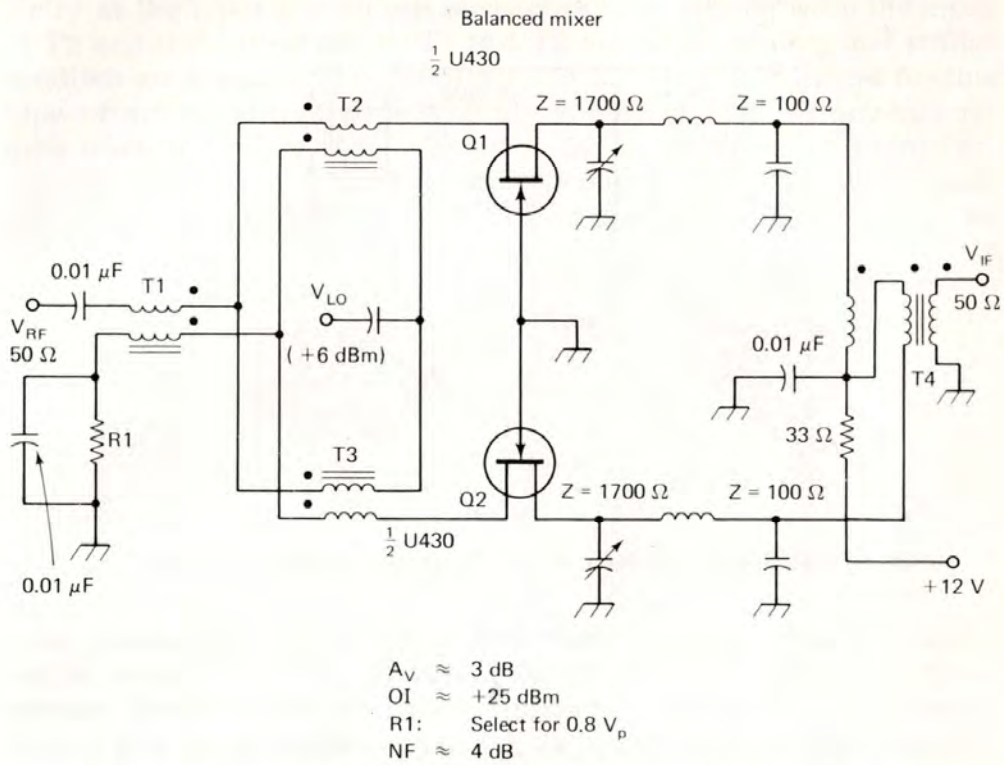


Figure 6.7 Dual FET balanced mixer using a Siliconix U430 device.

ferential between the sources of $Q1$ and $Q2$. The transformers are all wound on 125 μ_i ferrite toroid cores, 0.37-in. diameter. $T1$, $T2$, and $T3$ contain bifilar windings of 15 turns of number 26 enameled wire. $T4$ is wound on a 0.5-in. diameter ferrite core (μ_i = 125), trifilar fashion, with 15 turns of number 26 enameled wire. These transformer dimensions are suitable for use from 3 to 30 MHz.

Low-pass matching networks are used in the drains of the FETs to lower the drain impedance to 1700 Ω. They are structured to transform the impedance from 1700 ohms to 100 Ω. The 4 : 1 impedance ratio of $T4$ matches the mixer to a 50-Ω load. Best performance results when V_{LO} is 0.8 p-p $V_{gs(off)}$.

A singly balanced diode mixer is presented in Fig. 6.8. It suffers the same limitations found in singly balanced active mixers, and in addition it yields a conversion loss of approximately 6 to 8 dB. $T1$ is a trifilar-wound toroidal broadband transformer. $T2$ is also a broadband transformer, which is used to provide a step-up transformation to the mixer load. The turns ratio is chosen accordingly. Matched silicon switching diodes are satisfactory in this circuit, but hot-carrier diodes will offer improved performance.

A quad of matched silicon or hot-carrier diodes can be used to

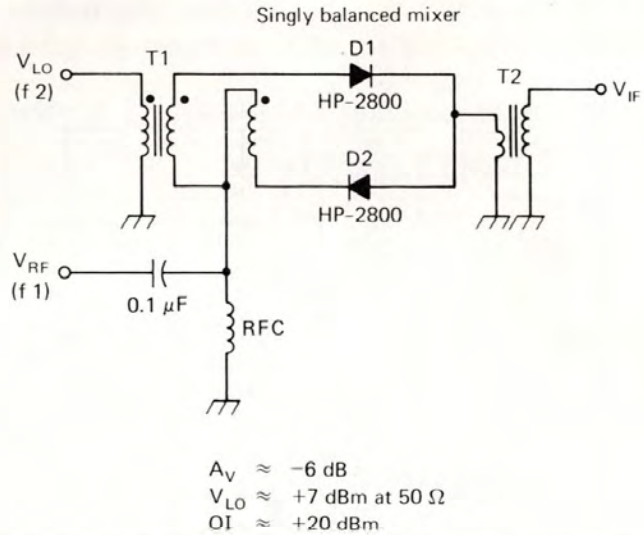


Figure 6.8 Singly balanced two-diode mixer using broadband transformers.

create a doubly balanced diode-ring mixer of the type shown schematically in Fig. 6.9. The circuit, minus $T1$ and $T4$, is typical of the manufactured DBM mixer modules found on the industrial market. Well-designed mixers of this kind offer excellent broadband characteristics, with effective bandwidths of more than 100 MHz. A typical DBM might be rated from 500 kHz to 500 MHz. Medium-level DBMs require an LO power of approximately +7 dBm, whereas the high-level DBMs call for LO powers of +15 dBm or greater. Conversion loss is comparable to that of the mixer in Fig. 6.8, being roughly 6 dB.

Transformers $T1$ and $T4$ of Fig. 6.9 can be added to serve as baluns. This aids the overall balance of the mixer by maintaining sym-

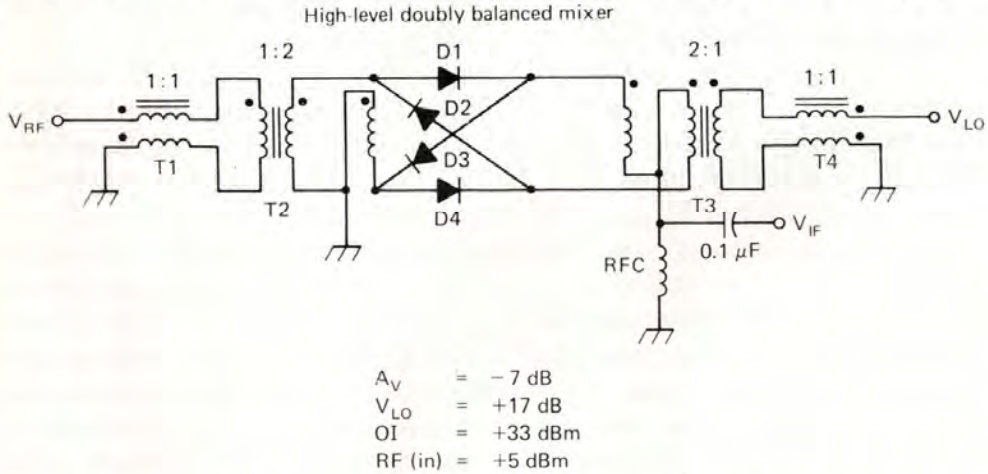


Figure 6.9 High dynamic range and good port-to-port isolation can be had from a doubly balanced diode-ring mixer.

metry at the input and output ports of the circuitry between the input of $T2$ and the output of $T3$. $T1$ and $T2$ are bifilar wound, and trifilar windings are laid on the cores of $T2$ and $T3$. Output intercept for this type of mixer (high level) is typically +33 dBm. Best performance results when the mixer is terminated in 50 Ω by means of a diplexer.

An example of a diplexed DBM is seen in Fig. 6.10. A high-pass network consisting of $L1$, $C1$, and $C2$ is connected to the IF port of the

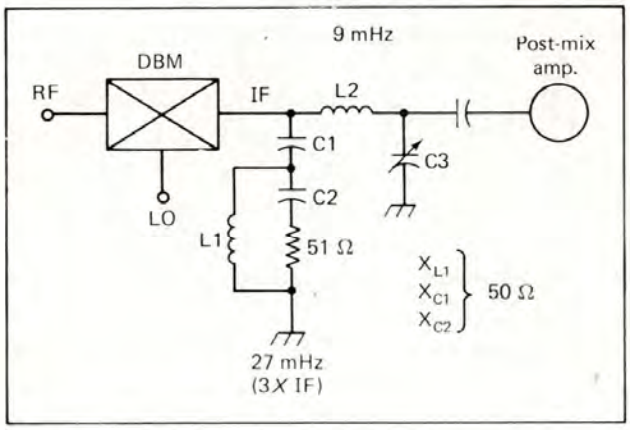


Figure 6.10 A diplexer can be added to a DBM for the purpose of presenting a 50-Ω termination. This improves mixer IMD.

mixer. It is designed for a cutoff frequency of three times the IF. A Q_L of 1 is satisfactory; hence we can use an X_L and X_c of 51 for the resistive termination of 51 Ω. A simple low-pass L network is used between the IF port of the DBM and the post-mixer amplifier to provide an impedance match to 50 Ω. The transformation ratio will be dependent upon the input impedance of the amplifier that succeeds the mixer. Improvements in mixer IMD of 2 to 4 dB have been observed by the addition of the diplexer.

6.1.3 IC Mixers

We could spend countless hours discussing the various types of IC mixers and their respective virtues. Such a treatment is beyond the scope of this text. Therefore, we will examine two of the more common IC mixers for illustrative purposes.

An advantage found in the application of balanced mixers that use ICs is the inherent balance and tracking with temperature that prevails. This is because the bipolar transistors and resistors that are within the IC were all formed at the same time on a common slice of silicon (substrate). This yields transistors with nearly identical dynamic characteristics. Also, when there are temperature excursions of the operating

IC, balance will be maintained through excellent tracking of the component values within the IC package.

A singly balanced IC mixer is depicted in Fig. 6.11(a). It employs an RCA CA3028A IC, which is seen in schematic form in Fig. 6.11(b). The device consists of a differentially arranged pair of *npn* silicon tran-

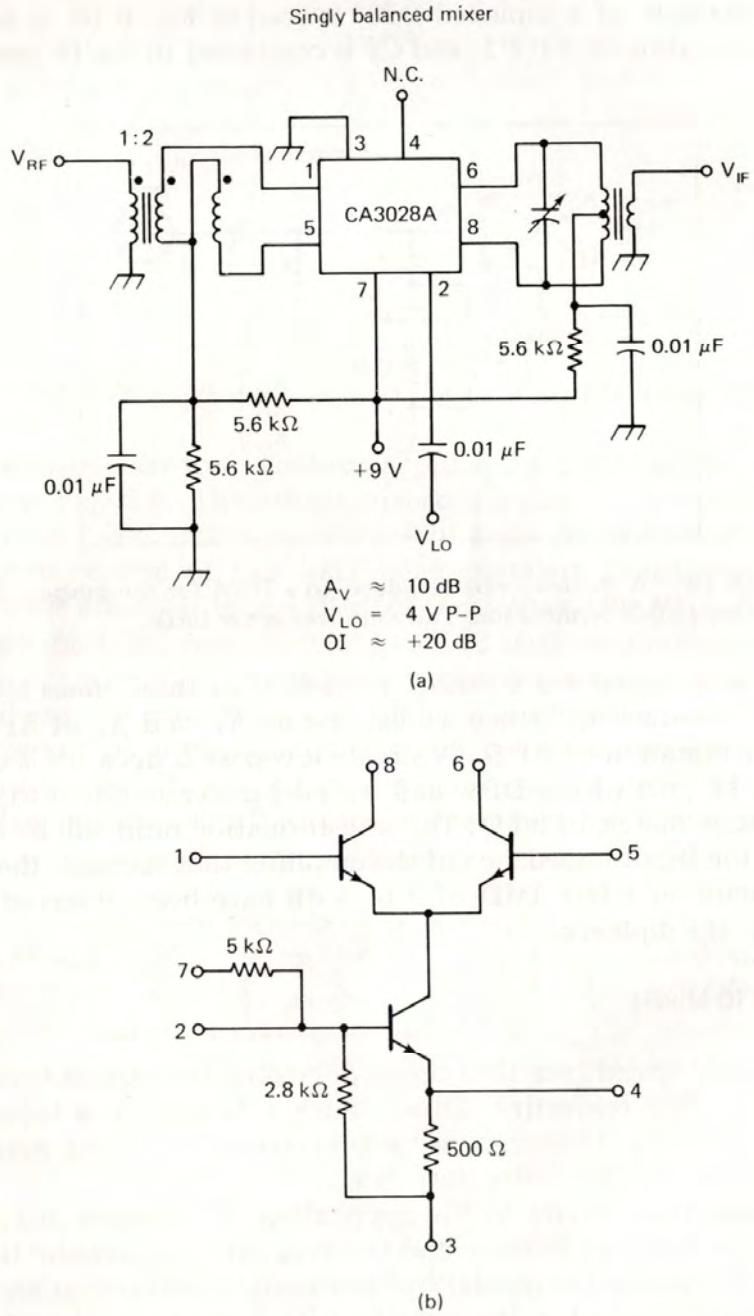


Figure 6.11 CA3028A IC used as a singly balanced mixer; (b) internal circuit of the IC.

sistors. A third transistor functions as a current source in the emitter returns of the differential pair. This IC offers good mixer performance up to at least 100 MHz. As configured in Fig. 6.11(a), it will provide a conversion gain of about +10 dB with an output intercept of approximately +20 dBm. A broadband transformer is used at the input of the mixer to establish a 180° phase difference at the bases of the differential pair. A tuned transformer is used at the mixer output to provide filtering action and a positive conversion gain. The turns ratio of the tuned transformer is chosen to provide a match between the mixer output and the load. The CA3028A has a base-to-base input impedance of approximately 2000 Ω. The collector-to-collector output impedance is on the order of 8000 Ω.

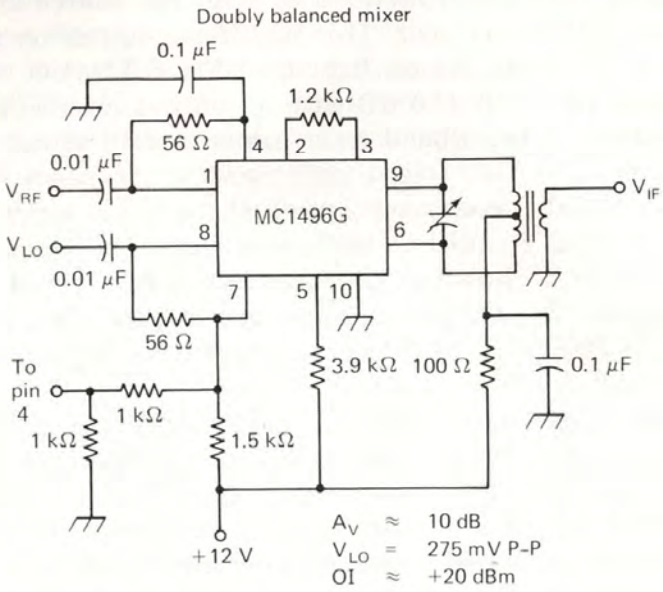
A doubly balanced IC mixer is presented in Fig. 6.12(a). It contains a Motorola MC1496G, which is seen schematically in Fig. 6.12(b). In balanced operation the two differential pairs of *npn* transistors are cross-connected to give a doubly balanced arrangement. Optimum performance will be obtained through experimentation with the biasing values of the circuit. The component values in Fig. 6.12(a) are approximately those suggested by the manufacturer, but the author has seen laboratory reports that indicated improved IMD performance by optimizing the biasing of the IC.

The input and output impedances of the MC1496G are similar to those that characterize the CA3028A of Fig. 6.11. LO suppression at the mixer output is between 40 and 65 dB, depending on the operating frequency and the degree of circuit balance.

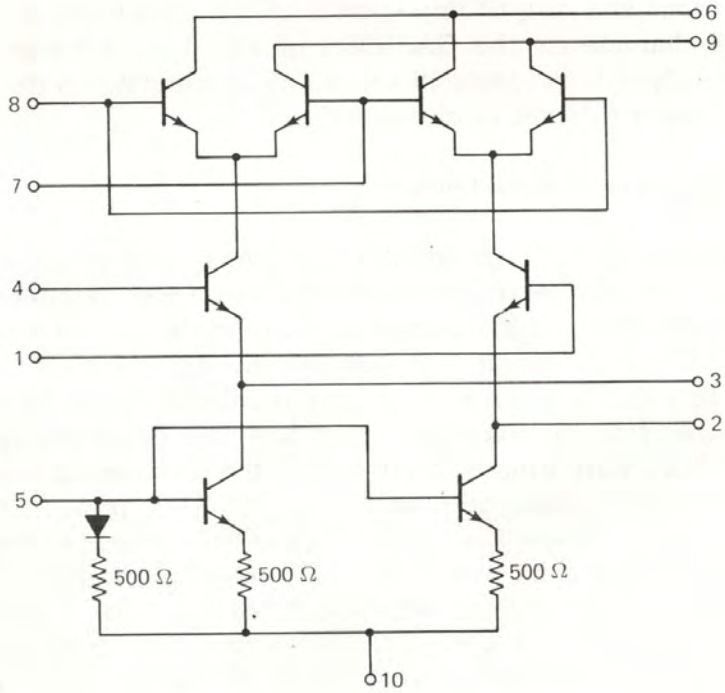
6.1.4 High-Level Balanced Mixers

In the interest of high orders of mixer dynamic range, we can utilize mixers that are more powerful than those just described. One IC type of mixer chip that has proved effective in this regard is the Plessey SL6440C. Although similar in concept to the MC1496G, it can be programmed to exhibit a third-order output intercept of +31 dBm. The programmable feature entails the controlled flow of current into pin 11 of the IC. Maximum quiescent current in the differential transistors is 50 mA. Total device dissipation at 25°C is 1200 MW maximum.

Figure 6.13 depicts the laboratory test circuit used to evaluate the SL6440C. Broadband balun transformers are used to provide balanced input and output conditions. This arrangement results in a 50-Ω impedance being presented to the input and output ports of the IC. Conversion gain was measured as 0 dB, although the manufacturer rates it at -1 dB. This number was determined with 50-Ω input and output terminations on the IC (desired to lower the A_V and improve the input intercept) and a programmed current (I_p) of 35 mA. The author measured the noise figure at a signal frequency of 15 MHz and found it



(a)



(b)

Figure 6.12 (a) Doubly balanced active mixer with a Motorola MC1496G IC; (b) the inner workings of the chip.

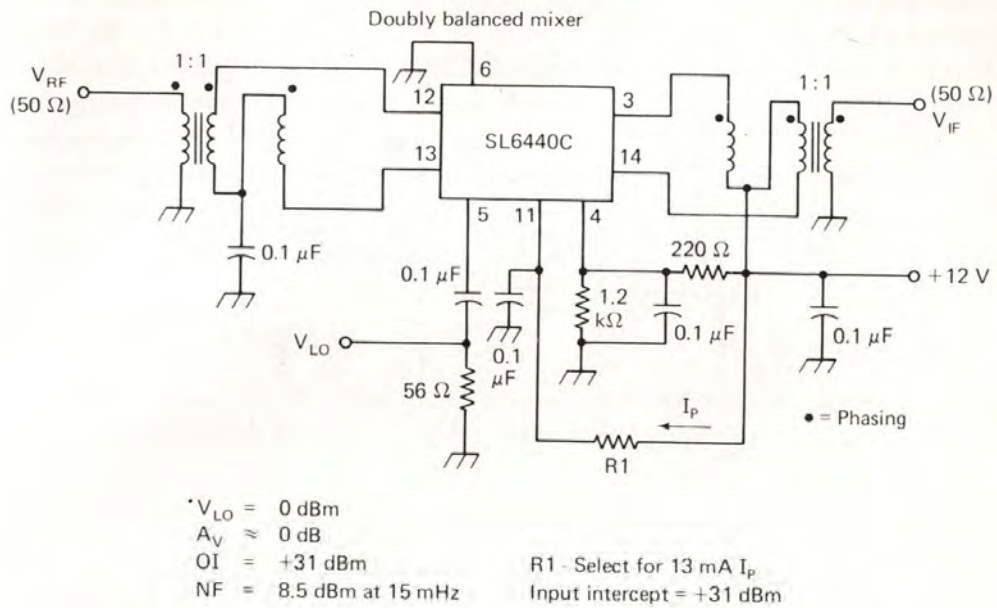


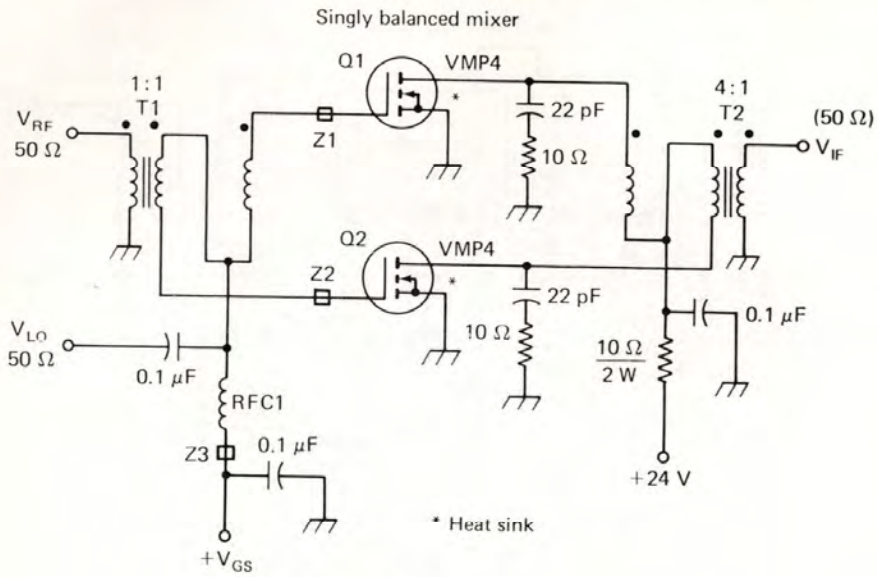
Figure 6.13 A high-level doubly balanced mixer can be obtained by using the Plessey SL6440C IC. Excellent dynamic range is possible with this circuit.

to be 8.5 dB. Plessey rates it at 11 dB at a signal frequency of 100 MHz, the same frequency at which the -1-dB gain was determined.

In the circuit of Fig. 6.13, $R1$ is chosen to permit the desired value of I_p. In the author's tests it was noted that an I_p of 13 mA resulted in optimum mixer performance with an LO level of 0 dBm and an RF signal input of -5 dBm. Under these conditions the LO isolation at the mixer output was 30 dB. The $2f$ LO energy was measured at -75 dB.

If we desire a very strong mixer, we might consider using VMOS power FETs as the active devices. Once again there is the matter of cost-effectiveness to consider, plus the physical bulk of the mixer module. The power FETs are substantially larger than ICs or small-signal devices, and because of the power they dissipate it is necessary to employ heat sinks. Moreover, the power consumption of a VMOS mixer is rather high, placing still another constriction on the design. However, the performance of this variety of mixer offers many advantages, the most significant being high dynamic range if the conversion gain is minimized.

A practical circuit for a high-level, singly balanced VMOS power FET mixer is shown in Fig. 6.14. VHF transistors are used in this laboratory test model, primarily to take advantage of the strip-line packaging format, which lends itself well to heat sinking. Some of the less expensive VMOS units would no doubt yield similar performance, such as the Siliconix VN66AKs, but the TO-5 package would impose restrictions



I_{DQ} = 100 mA
V_{LO} = +16 dBm
V_{GS} = +2 V Input intercept = +33 dBm
A_V ≤ 16 dB
OI = +43 dBm
NF = 5.5 dB at 15 MHz

Figure 6.14 Exceptional dynamic range can be obtained when using VMOS power FETs in a singly or doubly balanced high-level mixer. This circuit yields an output intercept of +43 dBm.

with concern to heat sinking of adequate magnitude. The TO-3 equivalent to the VN66AK would probably be a good low-cost alternative to the VMP4s of Fig. 6.14.

In the test circuit we find broadband balun transformers used at the mixer input and output. This forces a 50-Ω gate-to-gate impedance when the generator impedance is 50 Ω. We should keep in mind that, no matter how spectacular the mixer output intercept number, the input intercept is governed by the conversion gain (or loss) of the mixer. Therefore, the mixer gain should be as low as possible, consistent with the design objectives. It is suggested that the *T*1 matching transformer be configured to provide a 50-Ω input impedance (forced through intentional mismatch). We might even wind the transformer to decrease the effective imepdance to some value much lower than 50 Ω. Ideally, the mixer gain should be on the order of unity, thereby yielding an input intercept of +43 dBm. *Z*1 and *Z*2 are necessary in order to damp a VHF parasitic oscillation that became manifest duirng the tests. *Z*3 aids stability by lowering the *Q* of RFC1.

An output intercept of +38 dBm was obtained with a forward gate voltage of 2, an LO injection power of +16 dBm, and a drain current

(both transistors) of 160 mA. Under these test conditions an RF signal level of -1 dBm was applied. Similar high performance was observed with a gate voltage of +1.5 and a drain current of less than 100 mA, using the same LO and RF signal powers. LO suppression at the mixer output was 36 dB. The one parameter that may cause concern to us is the conversion gain. It can be as great as +20 dB under some operating conditions. This requires an attenuator pad at the mixer output to protect post-mixer circuitry.

6.2. AM DETECTORS

AM detectors are the least complicated of the various demodulators used in communications circuits. Many receivers, for example, rely on

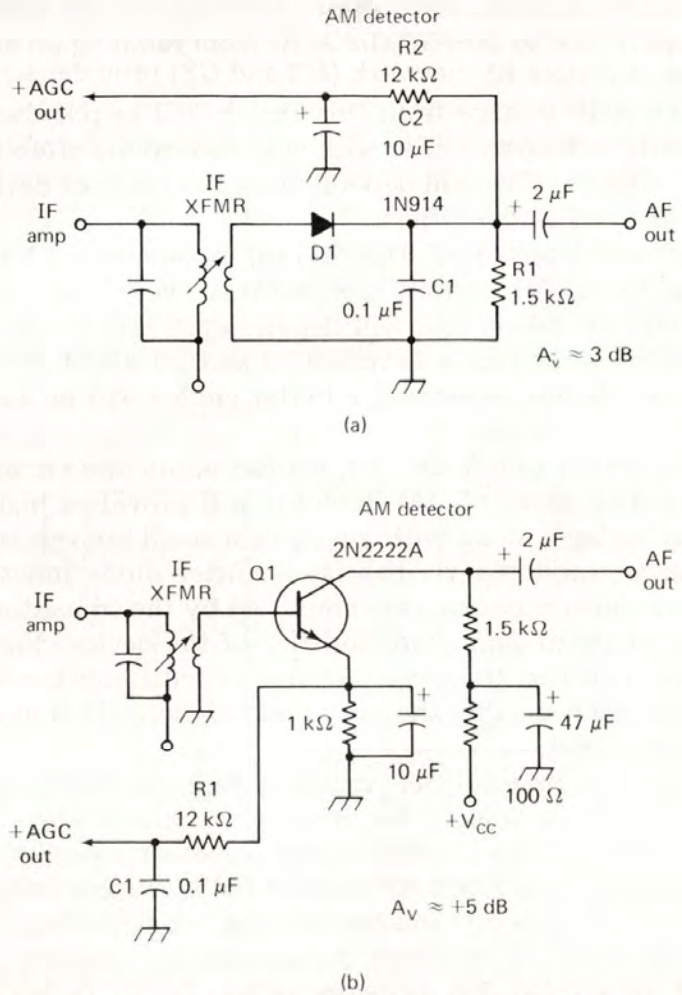


Figure 6.15 (a) One diode is used in this simple AM detector; (b) this circuit utilizes a bipolar transistor as an AM detector to provide a small conversion gain.

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A BiCMOS Analog Front-End Circuit for an FDM-Based ADSL System

D. Scott Langford, Bruce J. Tesch, *Member, IEEE*, Brian E. Williams, *Member, IEEE*, and G. Rodney Nelson, Jr., *Member, IEEE*

Abstract— **This BiCMOS analog front-end (AFE) integrated circuit contains the analog transmit function and a low-noise receiver for FDM-based ADSL systems. The IC includes a current steered 14-bit 5-Msps D/A converter, laser trimmed third-order reconstruction and anti-alias filters, a programmable attenuator with 200-ohm output drive capability, 60-dB of RX programmable gain, and a serial interface. Trimmable thin-film resistors allow ±4% filter cutoff frequency and absolute gain accuracy. The multitone power ratio performance of the part is approximately 65 dB with a spurious free dynamic range >70 dBc. The CMRR of the RX channel is >90 dB @ 1.1 MHz. PSRR for transmit and receive are greater than 60 dB. The isolation features of the 1.2-μm BiCMOS technology allow transmit and receive to operate in full-duplex mode with greater than 80 dB of cross- talk isolation. The chip size is 25.8 mm² which includes bond pads and electrostatic discharge protection devices.**

Index Terms— **ANSI standards, asymetric digital subscriber line, BiCMOS integrated circuits, continuous time filters, digital-analog conversion, distortion, modems, operational-amplifiers, signal reconstruction.**

I. Introduction

An AYMMETRICAL digital subscriber line (ADSL) is being touted as a near-term solution for the high-speed Internet access bottle neck that is developing around the world [1]. This paper describes an analog front-end circuit (AFE) that can be used in frequency division multiplex (FDM) ADSL systems. The currently accepted ANSI standard for ADSL is a discrete multitone (DMT) line code. The DMT signal is a multicarrier signal where channel frequency allocations may overlap or be spectrally separated. Transmit (TX) and receive (RX) chains operate in full duplex mode. The two techniques used to separate the near-end transmit signal from the far-end receive signal are echo cancelling (EC) and FDM. Systems with nonoverlapping channel allocations are FDM systems which rely on bandpass filtering for channel separation. The bandwidth of the DMT signal is approximately 1.1 MHz. This bandwidth is divided into upstream (U/S) and downstream (D/S) channels. The D/S channel delivers data rates of 6–10 Mbps down existing copper twisted pair depending on the line condition and length. The U/S channel delivers approximately 220–640 Kbps.

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The DMT time-domain signal, being the aggregate of multiple carriers, is near-Gaussian in distribution. As such, the time-domain signal occasionally exceeds the full-scale value of the DAC. The ADSL standard requires a DAC clipping rate of less than 1 in 10^7 samples. Given this requirement the DAC is loaded with a peak to rms ratio of 5.33. Operating at this high crest factor or peak to average ratio (PAR) requires a large dynamic range with good linearity over a 1.1-MHz bandwidth. A 14-bit D/A converter, amplifier, and filter blocks with THD < -75 dB over a 1.1-MHz bandwidth are required in the TX and RX channels. A figure of merit for the linearity is multitone power ratio (MTPR). The MTPR is measured by generating a DMT waveform which has a specific crest factor with specific carriers missing. The waveform is then passed through the TX or RX chain. The total integrated power of the notch at the location of the missing carriers is measured with respect to the adjacent carriers. Notch depth is measured for several DMT waveforms with different PAR's. The notch depths for each DMT waveform are averaged to give an MTPR number. Much of the transistor- and system-level design of this IC is aimed at achieving high MTPR numbers. High MTPR correlates directly with low bit error rate (BER) and thus longer reach over the copper twisted pair.

Fig. 1 shows a block diagram of the IC. There are separate fully differential TX and RX paths. The gain control is provided through a four-wire serial interface. The IC is designed such that it can be used at the ATU-C (central office side) or the ATU-R (customer premise or user side). A typical application diagram is shown in Fig. 2. Band separation filters are off-chip between the output of the TX and at the input of the RX channel.

II. System Considerations

Discrete multitone (DMT) was selected as the line code for ADSL for several reasons. The premise behind DMT is the division of the available bandwidth into smaller bands or "bins" each of which is assigned a low-rate modulated carrier at the bin center. Over the smaller subbands the channel looks relatively benign, requiring minimal channel equalization, thus simplifying implementation of the demodulators. Because multiple carriers are used, the bit loading on each individual carrier can be adjusted based on the available signal-to-noise ratio (SNR) in that subband to maximize the aggregate data rate for the system. Given a maximum total power for all carriers, carriers in subbands with low noise are allocated more power, allowing higher bit loading, and those carriers in bins with high noise or external interferers

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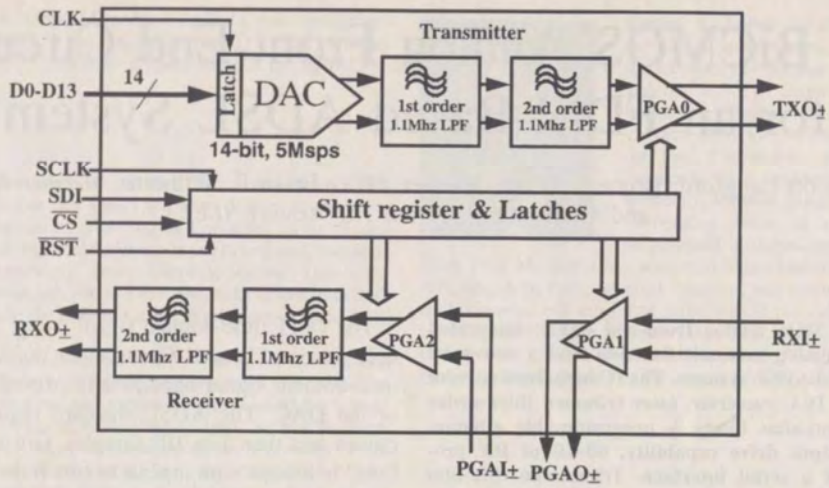

Fig. 1. Block diagram of AFE.

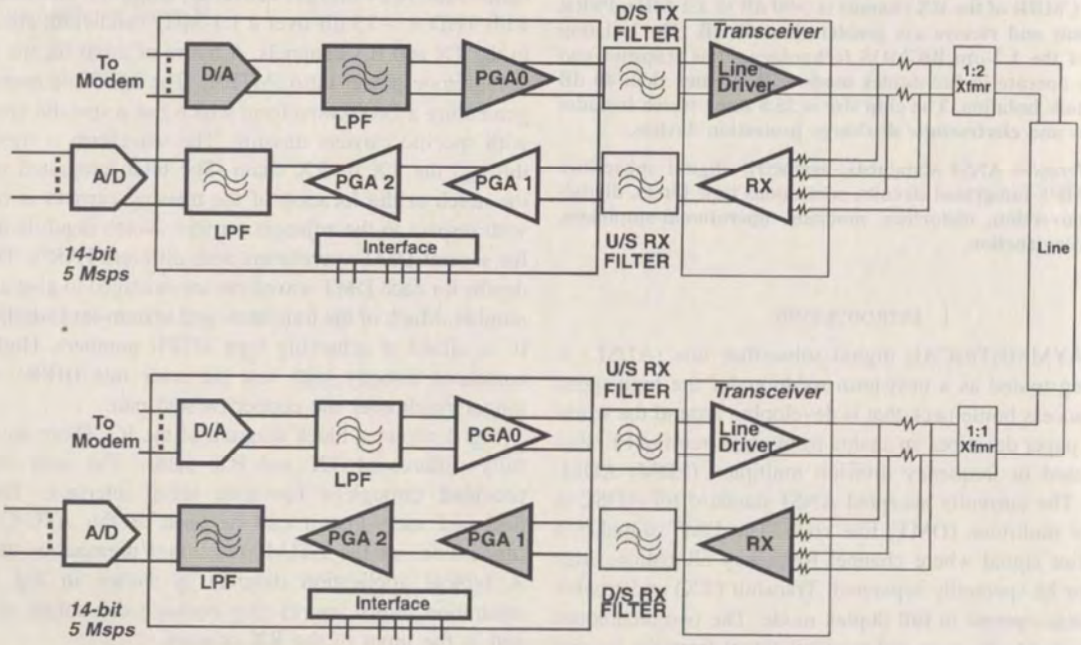

Fig. 2. Typical application diagram.

are allocated lower power. The ADSL standard allows over 200 downstream carriers (central office to customer premise), which permits the aggregate data rate to be matched very precisely to the to available line conditions.

Each of the subcarriers in the ADSL waveform is modulated with multilevel quadrature amplitude modulation (QAM). Each of the possible 255 carriers are on 4.313-kHz spacing for a total occupied bandwidth of 1.104 MHz. The drawback to DMT is the high peak-to-average ratio (PAR) of the waveform due to the instantaneous summation of up to 255 carriers. The theoretical limit on the PAR given constant envelope signaling on each DMT carrier is

$$\mathrm{PAR} = 10 \cdot \log_1 0(M) \tag{1}$$

where M = Number of DMT carriers.

The theoretical limit is very high (24 dB) for the downstream signal. Although this limit is rarely approached, the high PAR places severe circuit noise and linearity requirements on the analog front end (AFE).

Several mechanisms contribute to the noise in the AFE. Two major sources of noise are the quantization noise and overload noise in the digital-to-analog converters (DAC's) and analog-to-digital converters (ADC's). Both quantization noise and overload noise occur in the ADC due to quantization of a continuous analog waveform to discrete levels. Overload noise occurs when the analog waveform amplitude exceeds the peak input of the converter. Quantization and overload noise for the DAC actually occurs when the digital signal processor (DSP) truncates the precision of the transmit samples prior to appli-

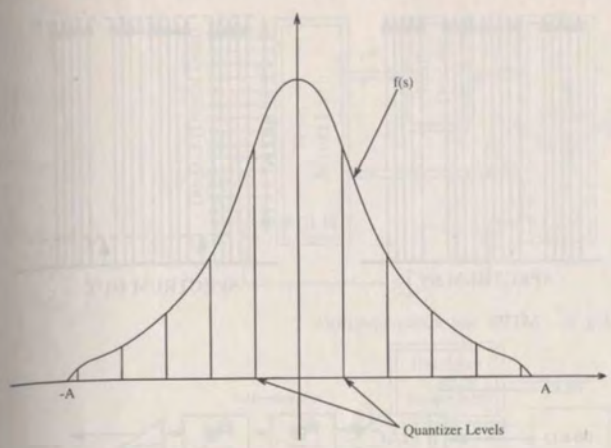

Fig. 3. Amplitude distribution of analog waveform.

cation to the DAC. To establish the number and fidelity of the quantizer levels for the converter, analysis of the quantization effects on the DMT waveform must be considered.

A. DMT Waveform

Given an analog waveform of a specific amplitude distribution as shown in Fig. 3, the noise due to quantization can be shown to be

$$N_q = \frac{A^2}{3 \cdot M^2} \tag{2}$$

where A = peak amplitude and M = number of quantizer levels.

Equation (2) assumes the amplitude distribution of the analog waveform lies totally within the range of the converter ($-A$ to $+A$) [2]. Due to the high theoretical PAR of (1) the amplitude distribution of the ADSL waveform is truncated to reduce the requirements on the AFE linearity. The amplitude distribution of DMT results from the summation of a large number of carriers, which on a per sample basis can be shown to be Gaussian based on the central limit theorem [3]. Equation (2) then becomes

$$N_q = \frac{(k \cdot \sigma)^2}{3 \cdot M^2} + \xi(k) \tag{3}$$

where

- k number of standard deviations passed;
- σ standard deviation of waveform;
- M number of quantizer levels;
- $\xi(k)$ overload noise.

Note that $k * \sigma = A$.

For a Gaussian amplitude pdf the overload noise can be shown to be [3]

$$\xi(k) = \sqrt{\frac{2}{\pi}} \cdot \frac{\sigma_s^2}{k} \cdot \left(1 + \frac{2 \cdot k^2}{3 \cdot M^2}\right) \cdot e^{-k^2/2} \tag{4}$$

where

- σ standard deviation of the voltage waveform;
- k number of standard deviations passed;
- M number of quantizer levels.

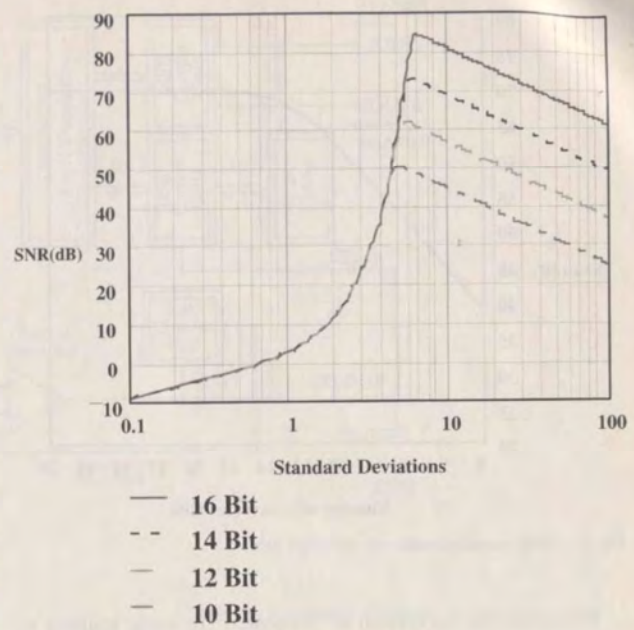

Fig. 4. SNR versus k for various quantizer levels.

B. Converter Requirements

Clearly, for a specified number of quantizer levels there is a tradeoff between quantizer noise and overload noise. As the overload noise is reduced by allowing more of the waveform to pass (k is larger), the quantization noise will begin to increase after a certain point. As k gets larger the upper quantizer levels are used less frequently due to the Gaussian amplitude pdf. This results is less quantizer levels being available for that part of the amplitude pdf which occurs most frequently. The converse is also true, as the overload noise is increased by making k smaller, the quantizer noise is reduced as more levels are available for quantizing that part of the waveform which occurs more frequently.

Derivation of an expression for SNR dependent on the number of standard deviations k allows one to plot the tradeoff between overload noise and quantization noise for a Gaussian amplitude pdf.

Let

$$\mathrm{SNR} = \frac{\sigma^2}{N_q} \tag{5}$$

where σ = standard deviation of the voltage waveform.

Then

$$\mathrm{SNR} = \frac{\sigma_s^2}{\dfrac{(k \cdot \sigma_s)^2}{3 \cdot M^2} + \sqrt{\dfrac{2}{\pi}} \cdot \dfrac{\sigma^2}{k} \cdot \left(1 + \dfrac{2 \cdot k^2}{3 \cdot M^2}\right) \cdot e^{-k^2/2}}. \tag{6}$$

If (6) is plotted verses k for various quantizer levels the trade between quantizer levels and k is readily apparent, as shown in Fig. 4.

From Fig. 4, it can be seen that for any quantizer, there is an optimum number of standard deviations k that maximizes the SNR for a Gaussian amplitude pdf.

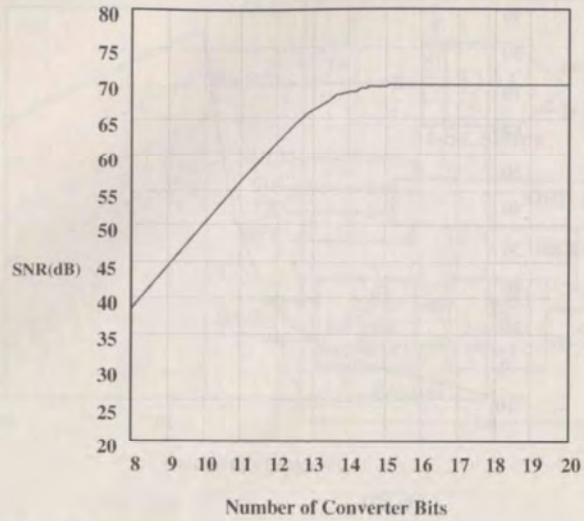

Fig. 5. SNR versus number of converter bits.

Whenever the waveform is "truncated" to some number of standard deviations "k" the result is clipping in the analog front end. The clipping or overload noise will occur for those few samples which are outside the bounds of the converter. The upper levels in the communications protocol must take in account the periodic clipping to ensure proper bit-error rate (BER) performance. This is usually handled through interleavers and various coding methods in the MODEM's. For the ADSL DMT waveform the clipping rate is specified in the T1E1.413 standard as one in 10^7 samples. The clipping rate is also specified at a PAR of 5.33 : 1. To relate PAR to the previous analysis, let

$$\mathrm{PAR} = \frac{V_{\mathrm{PEAK}}}{V_{\mathrm{RMS}}} \tag{7}$$

where $V_{\mathrm{RMS}} = \sqrt{\mathrm{Power}}$.

For the Gaussian ADSL amplitude pdf, (7) can be reduced to

$$\mathrm{PAR} = \frac{k \cdot \sigma}{\sqrt{\sigma^2}} \tag{8}$$

where

$$k \cdot \sigma = \mathrm{Peak}$$
$$V_{\mathrm{RMS}} = \sqrt{\mathrm{Power}}$$
$$\sigma^2 = \mathrm{Power}$$

then

$$\mathrm{PAR} = k. \tag{9}$$

The number of standard deviations k is just the PAR of the Gaussian waveform. Using a PAR of 5.33 and Fig 4 it is apparent that a 12-bit quantizer is almost optimum (offers the highest SNR with the lowest number of quantizer levels). Larger quantizers offer only slightly higher SNR. If SNR is plotted verses a fixed k of 5.33 for various quantizer levels as shown in Fig. 5. it can be seen that above 12 bits the increase in SNR by adding more bits becomes less and less and reaches a theoretical limit of about 70-dB SNR.

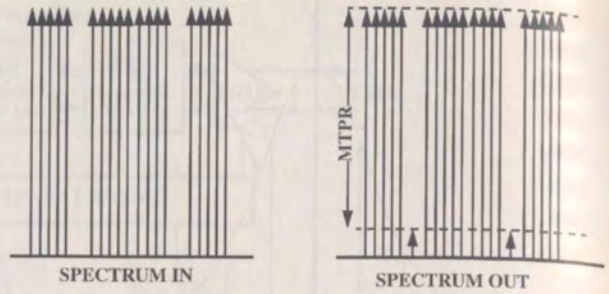

Fig. 6. MTPR test vector spectrum.

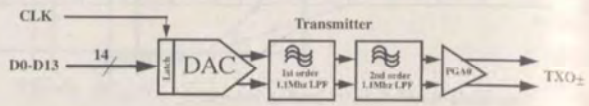

Fig. 7. TX chain.

It should be noted, however, that the previous analysis assumes perfect quantization (perfectly linear converter). In order to implement a converter with 12 effective bits a larger quantizer must be built to account for the nonlinearity of the converter. A 14-bit converter was implemented such that a minimum of 12 effective bits could be guaranteed.

C. Amplifier Requirements

Determining the linearity requirements for the amplifiers in the AFE is difficult using traditional methods due to the nature of the ADSL waveform previously discussed. Single-tone performance measures such as total harmonic distortion (THD) and two-tone intermodulation distortion (IMD) rely on sinusoids as the test signal. The amplitude pdf of a sinusoid is very different from the pdf of the ADSL waveform. Because of the zero mean Gaussian nature of the ADSL waveform, the most probable value for the waveform is 0 V. Amplifiers which exhibit crossover distortion would severely impact the spectral purity of ADSL, but would not necessarily impact a sinusoid to the same extent. Instead of attempting to relate classic measures of noise and distortion to the performance of ADSL, a new test waveform was devised which encompassed the linearity and noise measurements for the amplifier into a single test.

Modifying a classic technique from FDM analog technology for testing system linearity, the concept of a MTPR (multitone power ratio) test was defined. This test consists of a plethora of frequency domain impulse, uniformly spaced over a bandwidth of interest, with the characteristic that periodically a frequency impulse is "missing" giving the appearance of a spectral notch. The time series representation of the waveform for the case where every sixteenth tone is absent is given as

$$s(k) = \sum_{i}^{L} \cos(\Omega_i k + \theta), \qquad i \neq 16, 32, \text{etc.} \tag{10}$$

where $L = 256$ for ADSL, $\Omega_i = 2\pi/L$, and the term θ_i represents the starting phase of the ith tone. Fig. 6 represents the spectrum of this test vector. Notice that the comb spectrum

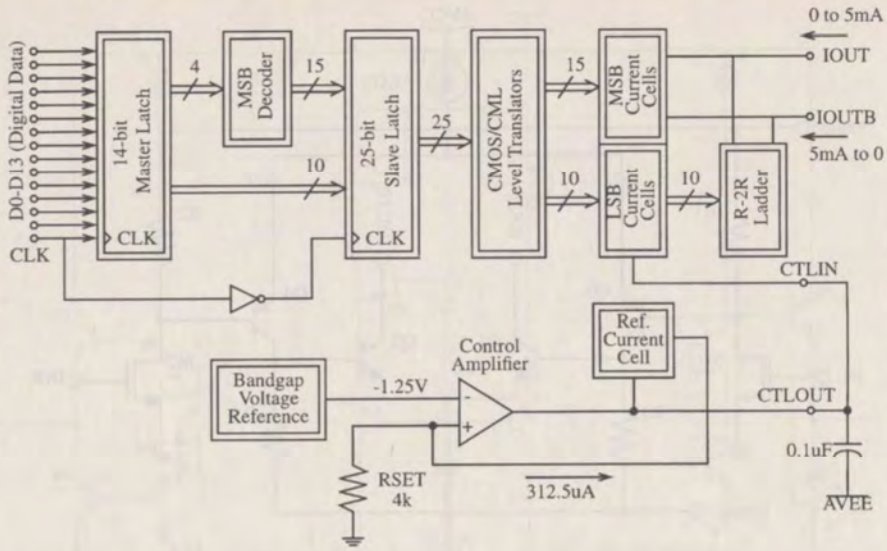

Fig. 8. D/A functional block diagram.

has suppressed tones located periodically in the spectrum. The frequency impulses are separated by the DMT carrier spacing [4] and each carrier of the comb is given a controlled starting phase θ_i [5] to constrain the PAR. Specifically, each tone's starting phase is adjusted to establish a PAR and the average signal level of the test vector is adjusted for a certain "backoff level" below full scale.

The object of the test is to pass this test waveform through the amplifier under test and observe at the output the depth of the "Notches" with respect to the level of the adjacent carriers. Factors that contribute to "filling-in" of the output notches are the intermodulation characteristics of the analog amplifier and the residual noise floor. It is felt that this testing technique better represents the actual scenario present in the case of the DMT/OFDM spectrum, where it is important to maintain a high signal–to-distortion ratio in each of the frequency bins.

Because the amplifier noise and nonlinearities are super imposed on that of the converter, an MTPR goal can be established for the entire AFE. The MTPR is essentially a measure of SNR within a frequency bin. If we assume the noise is spectrally flat as is the signal, the SNR for a frequency bin will be the same as the SNR for the entire waveform. If we construct an MTPR test signal with a PAR of 5.33 and apply it to the front end such that the waveform peak is just within the converter limits no overload noise will occur. Based on (5) and (3), the SNR is then

$$\mathrm{SNR} = \frac{\sigma_s^2}{\dfrac{(k \cdot \sigma_s)^2}{3 \cdot M^2}}. \tag{11}$$

Equation (11) can then be reduced to

$$\mathrm{SNR} = \frac{3}{k^2} \cdot M^2. \tag{12}$$

With $M = 4096$ (12 bits effective) and $k = 5.33$, the MTPR design goal for the AFE was 62.5 dB minimum.

III. Transmit Chain

The TX chain is shown in Fig. 7. It consists of a 14-bit current steered D/A converter, a reconstruction/bandshaping filter, and a programmable attenuator.

A. Functional Description 14-bit D/A Converter

The TX path begins with CMOS input buffers which are compatible with both 3- and 5-V logic. The data is then sent to a 14-bit 5-MHz current steered D/A converter based on a previous 14-bit 100-MHz D/A converter architecture [6]. The functional block diagram of the DAC is given in Fig. 8. Input data first passes through the master latches then the MSB's are decoded by a 4–15-thermometer decoder. Next, the data is resynchronized by the slave latches and finally translated to control 25 precision current cells. Ten LSB cells connect to the R-2R ladder, controlled by $D0$–$D9$, while the remaining 15 connect directly to the outputs, controlled by $D10$–$D13$. One additional precision current cell is connected in a feedback configuration with the bandgap voltage reference and control amplifier to establish the full-scale output current (I_{FS}). The resistor which sets the full-scale output current (R_{SET}) is included on-chip in order to track the I–V conversion resistors following the DAC.

Segmentation of the four most significant bits (MSB's) into 15 equally weighted current sources is a standard technique used to reduce DNL, glitch, and harmonic distortion. A 0.1 μF external capacitor is connected from the control amplifier output to the analog -5.2 V supply to reduce output noise and improve settling time [7].

B. CMOS/CML Level Translator

Aside from reducing I_{FS} from 20.48 to 5 mA, all digital logic was implemented in CMOS rather than CML to reduce power dissipation compared to the 100-MHz version [6]. Otherwise, the two designs are essentially identical except for the CMOS/CML level translator shown in Fig. 9. In this circuit $V\mathrm{Bias1} = 0.3$ V and $V\mathrm{Bias2}$ is temperature compensated so

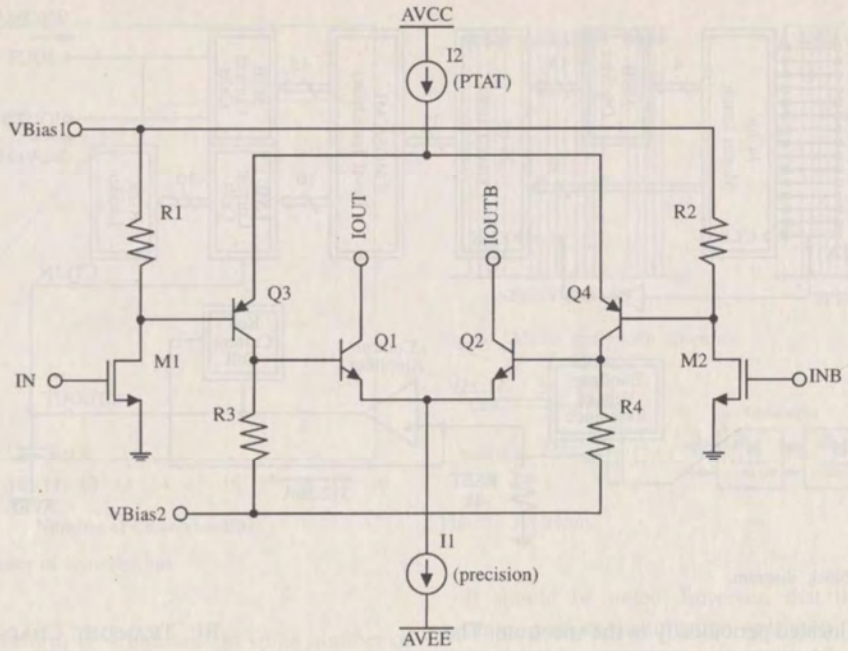

Fig. 9. D/A CMOS/CML level translator.

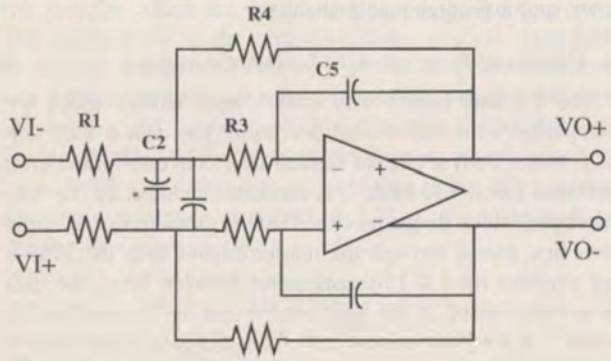

Fig. 10. Rauch biquad.

that the "high" voltage at the base of $Q1$ or $Q2$ is always 1.5 V. This helps to maximize VCE of $Q1, Q2$ and the BJT in precision current source $I1$ over the operating temperature range of the chip. Input devices $M1$ and $M2$ are sized as small as possible to minimize capacitive coupling of the 0–5 and 5–0 V input swings to the bases of $Q3$ and $Q4$ while maintaining a ± 0.25 V minimum differential output voltage swing. As in the 100-MHz version, current source $I2$ is proportional to absolute temperature (PTAT) in order to eliminate the temperature dependence of the $I_{\mathrm{OUT}}/I_{\mathrm{OUTB}}$ ratio, thereby giving the least possible glitch energy over temperature [7]. Finally, the value of resistors $R1$–$R4$ has been chosen to minimize power dissipation while maintaining adequate switching speed for 5-MHz operation.

C. Reconstruction Filters

The current output of the D/A is converted to a voltage by a third-order active R-C Chebyshev filter. This filter acts to reconstruct the sample and held signal of the D/A. The filter cutoff frequency and gain are trimmed by using NiCr links

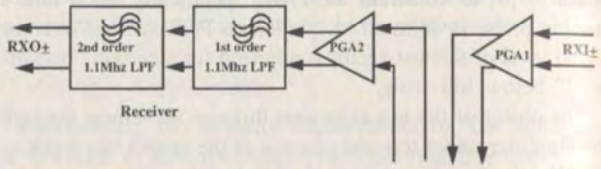

Fig. 11. RX chain.

for the resistive sections of the filter network. The third-order filter is constructed of a single-order section and a biquad. This third-order configuration allows independent setting of the gain and frequency response. The second order section is a Rauch biquad, shown in Fig. 10, utilizing only one amplifier with no positive feedback thus minimizing the required gain bandwidth product. The amplifier used for these filter sections is described below. The Rauch topology minimizes the number of opamps in the transmit chain thus lowering the power and reducing the noise and distortion contributors. The first-order section can be reconfigured into a second-order section with a limited number of mask changes to achieve a fourth-order response. The filter cutoff frequency is trimmed to within $\pm 4\%$ of the theoretical value.

D. TX Power Control

The final stage of the TX chain is a programmable attenuator (-12 to 0 dB) that is capable of driving a 220-ohm differential load at 12 $V_{p\text{-}p}$ diff. This attenuator is used to adjust the TX power levels depending on the line length and FCC transmission requirements.

IV. Receive (RX) Chain

The RX path contains programmable gain and attenuation and an anti-aliasing filter. The gain and attenuation are programmed to achieve maximum SNR while meeting the

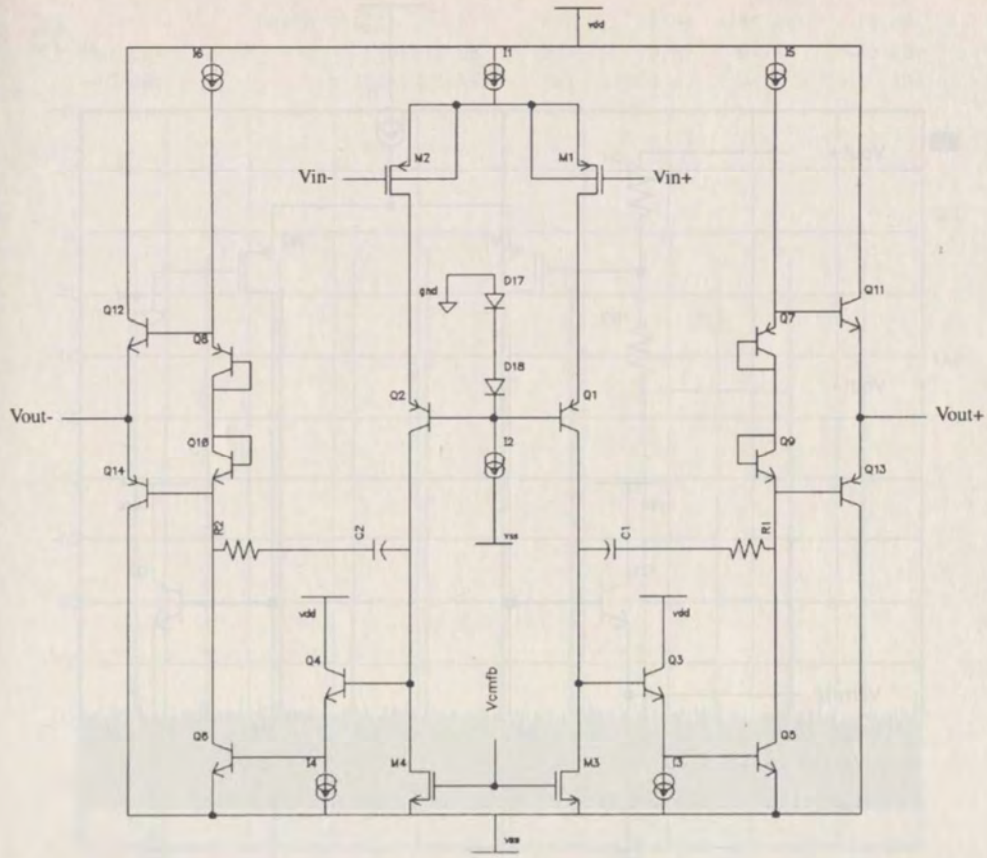

Fig. 12. Schematic of opamp.

dynamic range requirements of the A/D converter (4 $V_{p\text{-}p}$ diff). The PGA settings cover a wide range of line types and lengths. A block diagram of the RX chain is shown in Fig. 11.

A. PGA

The input PGA (PGA1) is a high-impedance (MOS input) with 0–24 dB of programmable range. The input referred noise density of this RX chain is 12 nV/$\sqrt{\text{Hz}}$. The output of PGA1 goes off-chip such that AC coupling and or additional filtering can be added. There can be line cases where the composite in band and out-of-band energy would exceed the dynamic range of the second PGA (PGA2), thus additional filtering between the PGA's can be used to avoid this problem. The signal then comes back on chip to PGA2 with -9 to $+18$ dB of gain. This stage is programmed to maximize the received signal or reduce it to fit into the dynamic range of the ADC.

B. Anti-Alias Filter

The next block is a third order anti-alias filter constructed in a similar fashion to the TX reconstruction filter. This block is trimmed for RX absolute gain error and cutoff frequency accuracy.

V. Operational Amplifier Design

Spectral purity is critical for any amplifier in the signal path of an ADSL analog front end circuit. Any source of spectral contamination can degrade the MTPR performance of the system and thus lower the ability of the system to handle worst case conditions, specifically very short or very long transmission loops. To maximize the MTPR performance, the operational amplifiers for the transmit chain and receive chain must have excellent THD, CMRR, PSRR, and noise performance. Power consumption is important as several amplifiers are used in the reconstruction filters, the anti-alias filters, and the programmable gain amplifiers in both the TX and RX chains. In order to obtain high linearity over the 1.1-MHz signal bandwidth, the amplifiers were designed with a 70-MHz nominal gain bandwidth product which provides >35 dB of loop gain at 1 MHz. Nonlinearities due to the amplifier are reduced by 35 dB by the feedback.

A simplified diagram of the amplifiers used is shown in Fig 12. To minimize distortion due to second-order harmonics and avoid substrate coupling, the amplifiers were built fully differential. The amplifier consists of a PMOS input pair ($M1$–$M2$), PNP cascode transistors ($Q1$–$Q2$), buffer emitter followers ($Q3$–$Q4$), second gain stage common-emitter NPN transistors ($Q5$–$Q6$), and class A-B output driver stages ($Q7$–$Q14$).

The input differential pair ($M1$–$M2$) was chosen to be PMOS for three reasons. First, the amplifier was used in an active R-C filter which had input resistances on the order of 2 kΩ. At these impedance levels the noise contribution of the

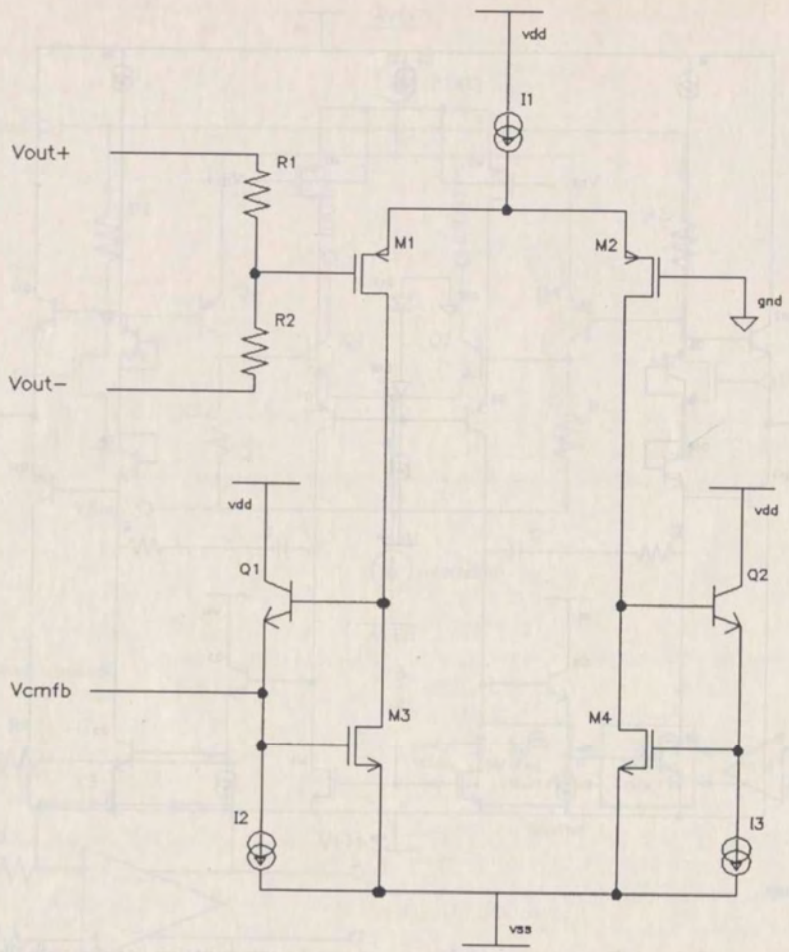

Fig. 13. Common mode feedback circuit.

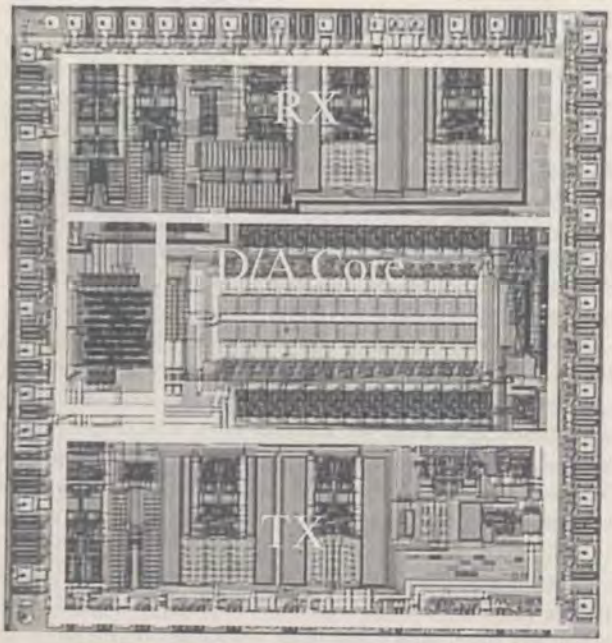

Fig. 14. Die photomicrograph.

input current noise of a BJT differential pair and active load was too large. PMOS transistors were used to reduce this input referred current noise contribution. PMOS, instead of NMOS, transistors were used due to their lower $1/f$ noise corner. The final advantage was the large transconductance ratio between the second gain stage bipolar transistors ($Q5$–$Q6$) and the input pair MOS transistors ($M1$–$M2$) allowed for smaller compensation capacitors ($C1$–$C2$). The body connections for the input pair were tied to their respective sources to maximize the power supply rejection ratio (PSRR) of this stage. A differential output signal can be generated by the power supply due to device mismatch in the differential pair and the modulation of the back gate by the supply if the body is tied to the supply. Tying the bodies to the source prevents the supply from modulating the threshold voltages of the differential pair. In order to maximize the bandwidth of the differential pair, a cascode pair of PNP transistors ($Q1$–$Q2$) was used to remove the impact of the miller capacitance that would appear at the gates of differential pair. These cascode transistors also improve CMRR and PSRR [8]. It is important to note that a straight cascode was used and not a folded cascode stage. This was done for two reasons, the primary of which was to avoid the extra leg of current which would be necessary to

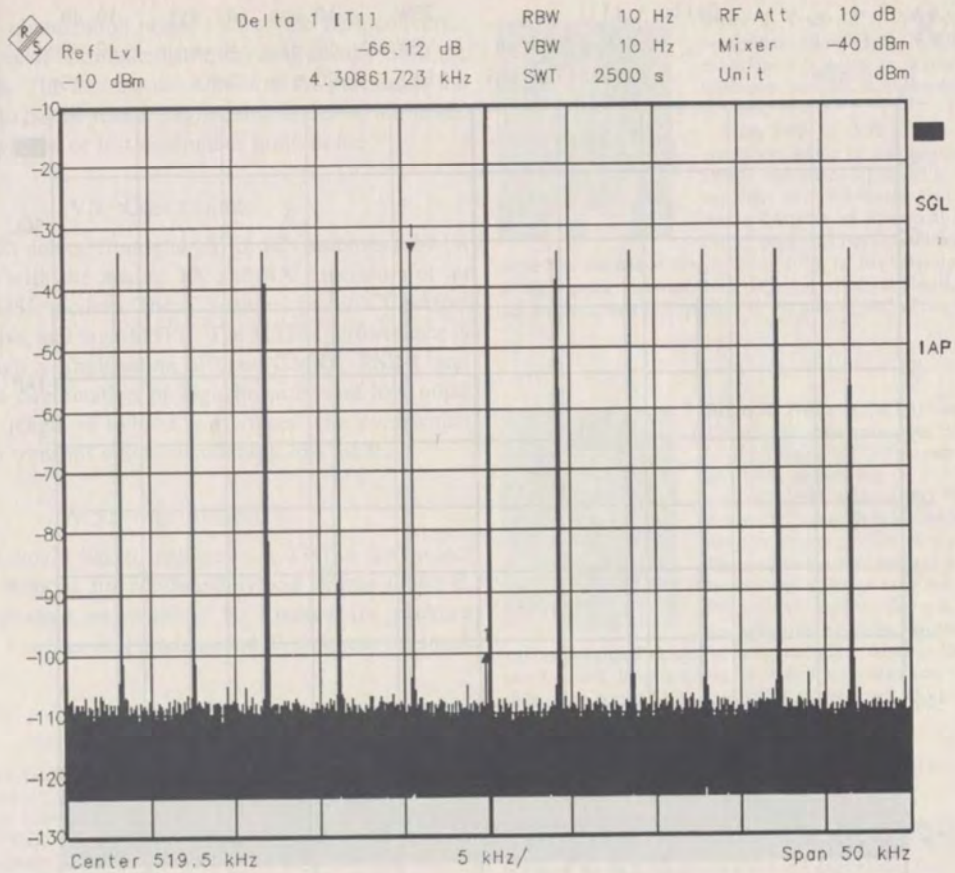

Fig. 15. TX MTPR.

bias the folded device, thus lowering the power necessary to achieve the same bandwidth. The second reason the straight cascode was used was that the dynamic range needed for the input differential pair was very small due to the fact that the amplifiers were all to be used in fully differential systems. The input dynamic range can be quite large for single-ended amplifier architectures, especially some noninverting unity gain buffer configurations where both input terminals track the input voltage. In fully differential amplifiers, there is no equivalent circuit to the typical noninverting unity gain buffer—only circuits where both inputs stay at a virtual ground potential.

The input referred offset was reduced by using low-voltage NMOS devices as the active load of the input pair. The low-voltage devices exhibit better matching (with slightly reduced output impedance) than the high-voltage devices due to the absence of the extension implant. The low-voltage devices can be used in this case as the drain voltage is clamped and the common mode feedback circuit takes out dc errors.

Emitter follower devices ($Q3$–$Q4$) were needed to maintain a high dc gain over process variation. Most of the gain of the amplifier comes from the high impedance node at the collector of devices $Q1$&$Q2$. Without these devices here, the bases of $Q5$–$Q6$ would be attached to the collectors of $Q1$–$Q2$, respectively. The Beta of PNP devices $Q13$–$Q14$ varies greatly over process and causes the impedance of second gain stage $Q5$–$Q6$ to vary equally. This made it difficult to derive a high gain from the second stage, so the majority of the gain was moved to the first gain stage by increasing the impedance at the collectors of $Q1$–$Q2$ with the buffers $Q3$–$Q4$. The insertion of these devices also lead to problems with gain margin due to additional parasitics which caused some peaking beyond the gain bandwidth of the amplifier. The amplifiers were compensated across the second gain stage with pole-splitting miller capacitors $C1$–$C2$ and right-half plane zero cancelling resistors $R1$–$R2$. This compensation network is the same network used to compensate the common mode feedback circuit.

The output drivers consisting of devices $Q7$–$Q14$ are a standard single stage class A-B resistive drive output stage. The amplifiers were required to drive resistive loads from 220 Ω to 2 kΩ. A two-stage A-B buffer would have increased the output dynamic range by one diode drop and improved THD. Unfortunately this configuration would require two extra legs of current to bias the emitter–follower devices. The tradeoff in favor of lower power consumption was made in this case.

The common-mode feedback circuit (shown in Fig. 13) was uncomplicated because of the resistive drive capability of the amplifiers. The common mode output is sensed with a simple pair of resistors $R1$–$R2$, and compared with a reference voltage which in this case is ground. The comparison circuit drives the diode-connected NMOS $M3$–$M4$ which sets the gate voltage for $M3$–$M4$ in Fig. 12. The buffer device (Fig. 13) $Q1$ acts to move the parasitic pole at the gate

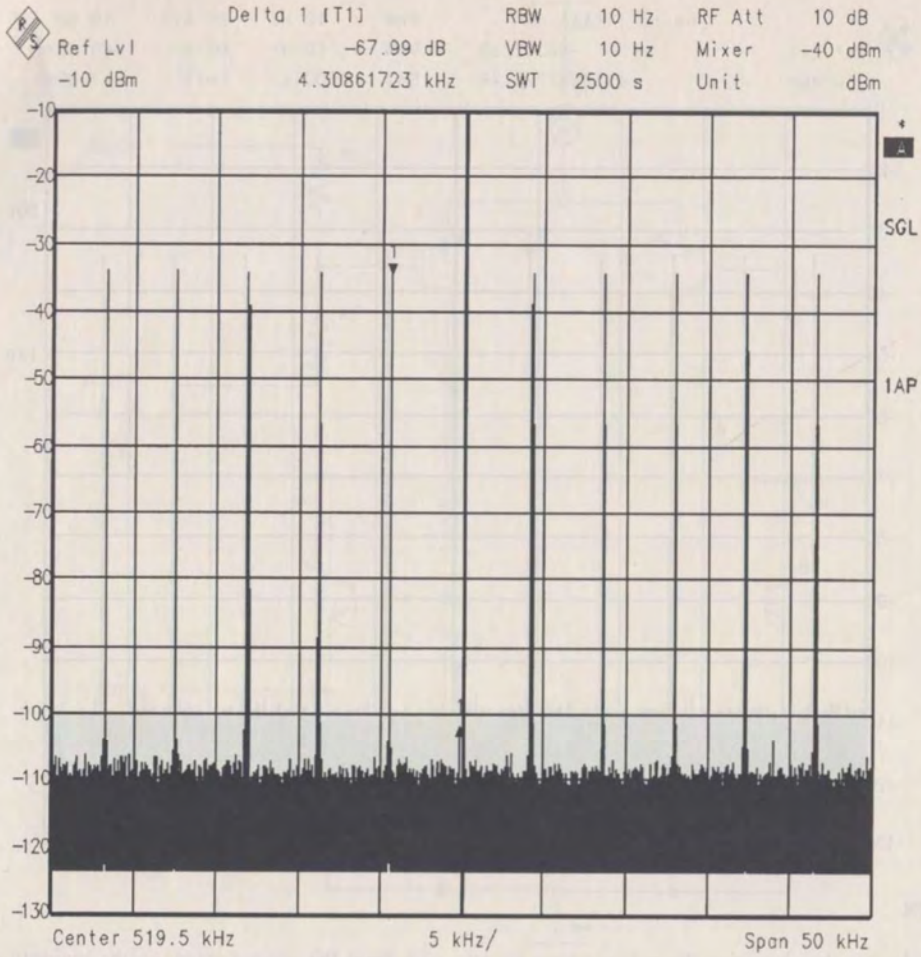

Fig. 16. RX MTPR.

TABLE I
SUMMARY PERFORMANCE DATA

Parameter	Measured	Units
Supply Voltage	±5	V
Signal frequency range	.01 - 1.1	MHz
Quiescent Power Dissipation	750	mW
TX MTPR	65	dB
RX MTPR	65	dB
Maximum Output Level	12	Vppdiff
Absolute TX gain accuracy at 0 dB setting	1	%
Output Gain Adjust Relative Accuracy	0.285	dB
RX input referred noise	12	nV/rthz
RX CMRR	>90	dB
RX PSRR	>60	dB
TX PSRR	>60	dB
TX-RX isolation	>80	dB

of $M3$ out in frequency so that the dominant pole in the compensation of the common-mode feedback loop is set by the same dominant pole as the compensation for the amplifier.

The input referred offset was reduced by using low-voltage NMOS device as the active load of the input stage. The low-voltage device can be used in this application as the drain voltage is clamped and the common mode feedback circuit takes out dc errors.

VI. INTEGRATION CONSIDERATIONS AND EXPERIMENTAL RESULTS

A photomicrograph of the die is shown in Fig. 14. measuring 25.8 mm^2 in area. Key integration considerations center around integration of the TX and RX chains on a single substrate. Of particular importance are nonlinear leakage paths, which would bypass band separation filtering. The other coupling problem is substrate noise caused by the relatively high-speed operation of the digital portion of the D/A converter. The output driver of the TX chain is designed to deliver 12 $V_{p\text{-}p}$ diff into a 220-ohm load while maintaining 65-dB MTPR. This requires a technology which supports 10 V.

Spurious energy and cross-talk issues are addressed with circuit design techniques and process isolation. Fully differential circuit techniques are used. Separate supplies are used for the D/A, TX chain and RX chain and the serial interface.

Table I shows a summary of the AFE. Total power dissipation is about 750 mW. Figs. 15 and 16 show typical MTPR results from a section of the TX and RX spectrum.

Thermal noise, quantization noise, INL of the D/A converter and other sources of harmonic distortion theoretically limit the MTPR to 74 dB. The thermal noise floor of the part limits the MTPR further to 68 dB. Other degradation is due to harmonic distortion of opamps or test equipment limitations.

VII. Conclusion

This BiCMOS analog front-end (AFE) IC combines a 14-bit D/A converter with the analog TX and RX functions for an FDM-based ADSL modem. The IC features 14-bit TX performance, low noise, and high MTPR. The MTPR performance is achieved through a combination of good CMRR, PSRR, and low THD. The combination of high linearity and low noise maximizes the length of twisted pair copper wire over which the system can transmit while maintaining low BER.

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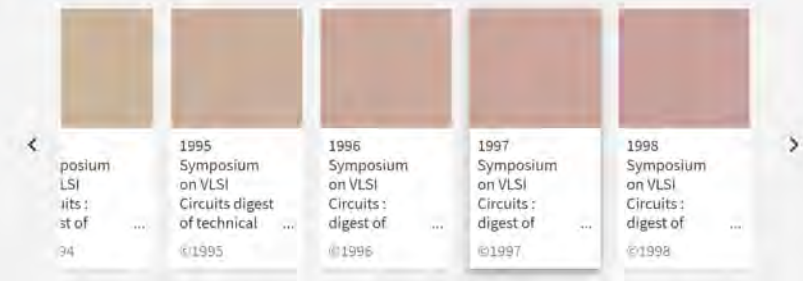

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The Synchronous Oscillator: A Synchronization and Tracking Network

VASIL UZUNOGLU, MEMBER, IEEE, AND MARVIN H. WHITE, FELLOW, IEEE

Abstract —The synchronous oscillator (SO) is a free-running oscillator which oscillates at its natural frequency in the absence of an externally applied signal. In the presence of a signal, the oscillator synchronizes with and tracks the input waveform with an acquisition time inversely proportional to the tracking bandwidth. The SO possesses a constant output signal amplitude in the tracking region and an adaptive tracking bandwidth proportional to the input signal level. In operation, a decrease in the input carrier-to-noise ratio reduces the SO's tracking bandwidth to maintain a constant carrier-to-noise ratio at the SO's output. An SO can track signals which have very low carrier-to-noise ratio. For example, a 70-MHz SO can perform phase acquisition in less than 400 ns and track a 140-MHz carrier with an input carrier-to-noise ratio of −40 dB (wide-band noise), while maintaining a 400-kHz tracking range. The SO has a very narrow resolution bandwidth, similar to a spectrum analyzer, which is independent of the tracking range and makes the noise rejection properties of an SO very high. Resolution bandwidth is a function of the regeneration process within the SO network, which is not found in other tracking networks. The paper presents the theory and experimental characterization of SO's in terms of selectivity, noise rejection, carrier-to-noise improvement, tracking range, and acquisition time. A specific application is described for SO carrier and clock recovery networks in a 60- and 120-Mbits/s QPSK modem with bit-error-rate (BER) performance approaching that of hard-wired connection.

I. Introduction

SYNCHRONIZATION is an important concept in coherent digital communication systems, where both the carrier and clock must be regenerated in the receiver. The benefits of synchronization lie in the conservation of bandwidth and signal power as well as error-free identification. A synchronization network element must possess the following properties:

1) excellent filtering properties (high selectivity) for noise rejection;
2) high sensitivity to recover the signal buried in noise (low-injection signal conditions);
3) wide tracking bandwidth;
4) fast acquisition time in burst-mode operation;
5) recovered output amplitude must be independent of injection frequency and amplitude;
6) phase difference between input and output must be linear with frequency and amplitude;
7) low steady-state phase error between input and output signals;
8) low bit-error-rate (BER);
9) internal memory (storage) in absence of synchronization pulses; and
10) frequency stability with power supply and temperature variations.

In addition to the above properties, the synchronization network must be cost-effective, operate with low-power requirements, and occupy a small storage area. In this paper we will describe a synchronization network comprised of an injection-locked synchronous oscillator to achieve the above requirements for coherent digital communication systems. In addition to carrier and clock recovery applications, the synchronous oscillator (SO) possesses additional features such as frequency division, adaptive bandwidth, and operation under the injection of a signal which is harmonic of the free-running frequency of the SO. The independence of the tracking range from the resolution bandwidth enables the SO to achieve superior performance over conventional phase-locked loops.

Van der Pol [1], [2] first introduced the concept of controlling the frequency of oscillators by externally injected signals. Adler [3] analyzed an early injection-type oscillator and derived a differential equation describing the oscillator phase as a function of time, which yielded an understanding of the basic locking phenomena in terms of a simple physical model, namely, the motion of a pendulum suspended in a viscous fluid inside a rotating container. Adler's work provide the foundation for subsequent papers by Kurokawa [4], [5], Khohlow [6], Minorski [7], Hayaski [8], Dewan [9], [10], and Runge [11]. Runge introduced current injection into a VCO to increase the pull-in range of the Van der Pol oscillator [11] operating in a phase-locked loop.

The SO described in this paper is a unique free-running oscillator which oscillates at its natural frequency ω_o in the absence of an externally applied input signal ω_i [12], [14]. The latter is referred to as the injected frequency or carrier. When ω_i is applied to the SO and if it lies within the tracking range $-\Delta\omega$ of the SO (i.e., $|\omega_o - \omega_i| < \Delta\omega$), then the SO starts "tracking" the external signal. The acquisition time of the SO is several orders of magnitude faster than conventional PLL's, which are limited by the trade-off between noise rejection and acquisition time in the loop filters [15]. Once the process of acquisition (synchronization) is completed, a phase difference exists between the

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input and output terminals of the SO. This phase offset per unit frequency is very low in a SO due to the high internal gain and wide tracking range. An important aspect of the SO is its performance as an adaptive filter, where the tracking range is proportional to the input signal amplitude. A reduction in the input carrier-to-noise ratio decreases the tracking bandwidth to maintain a constant output carrier-to-noise ratio. The main noise rejection property of a SO lies in its narrow resolution bandwidth. It is interesting to note that the resolution bandwidth is independent of the tracking range; yet both affect the noise rejection properties of a SO, the resolution bandwidth being by far the most effective one.

We will present an example of the SO in carrier and clock recovery networks with specific application to QPSK modems in order to illustrate their importance in satellite communication systems; however, the requirements of these systems fail to exercise the actual capabilities of the SO. In contrast to conventional filter approaches, the SO through its adaptive tracking bandwidth and very narrow resolution bandwidth permits the extraction of information from signals with extremely low carrier-to-noise ratios, such as -40 dB while tracking at several hundred kilohertz to permit rapid phase acquisition. This paper will describe the basic theory and experimental results obtained on injected-locked synchronous oscillators with emphasis on selectivity, noise rejection, carrier-to-noise improvement, tracking range, and phase acquisition.

II. Theory of the Synchronous Oscillator

Fig. 1 illustrates the basic injection-locked synchronous oscillator circuit and a functional description of its operation. The oscillator is a modified Colpitts oscillator with two active elements: transistor T_1 accepts the injected signal, amplifies it, and injects current into transistor T_2. Transistor T_1 is a active emitter load for transistor T_2. The dc current in both transistors is determined mainly by the bias resistor G. Transistor T_2 has three feedback paths: 1) a path thru C_1 to the base of T_2 (the value of C_1 is large and is considered a "short" at the frequency range of interest); 2) a path from the point between C_2 and C_3 to the emitter of T_2; and 3) a series negative feedback to T_2 provided by T_1. Feedbacks 1) and 2) are positive while feedback 3) is negative. The bias resistor G is adjusted so that both transistors operate in their linear-active region with equal collector-to-emitter voltage drops. L_c is an RF choke (isolation) and L, C_2, C_3 form the tank circuit. The variable resistor R_A controls the injection level and secures the isolation of the SO from the input drive circuit. The supply voltage is typically 5 V, and the power dissipation is approximately 5–10 mW.

In operation the SO is a nonlinear oscillator with high internal gain and a saturated output amplitude in the tracking range. The injected input signal only modulates the phase and does not disturb the output amplitude of the oscillator. This phase modulation is the key to SO operation. With reference to Fig. 1, the transconductance G_{m1}

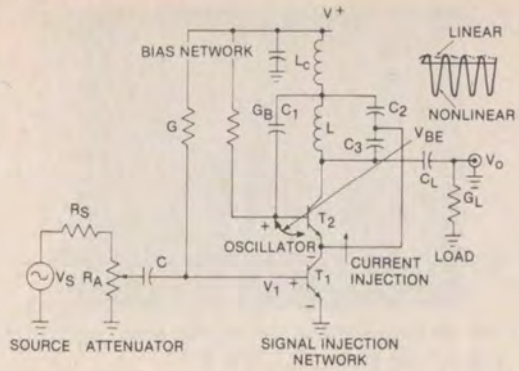


Fig. 1. Functional description of the SO circuit.

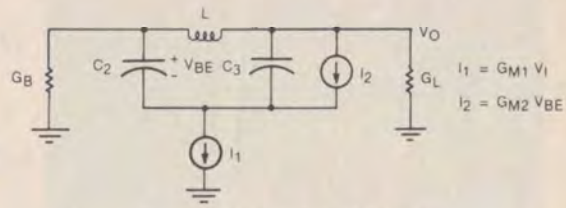


Fig. 2. Linear analysis of the SO.

of T_1 provides signal injection of current into T_2, while the transconductance G_{m2} of T_2 overcomes circuit losses. In general these transconductances are nonlinear [17]. In order to understand the concept of synchronization, we approach the SO operation with a linear analysis of the oscillator output voltage V_o, as shown in Fig. 2. A small-signal analysis of the circuit in Fig. 2 requires $G_{m2} \geqslant G_L C_2/C_3$ to sustain circuit oscillations, and $G_L \gg G_B$ yields

$$\omega_o^2 = \frac{C_2 + C_3}{LC_2C_3} \tag{1}$$

for the "free-running" oscillator frequency and

$$\ddot{V}_o + \omega_o^2 V_o = \frac{G_{m1}}{C}\dot{V}_i \tag{2}$$

for the fundamental differential equation, which describes the small-signal operation of the injection-locked synchronous oscillator subjected to an input signal voltage V_i, where $C = C_3(1 + C_3/C_2)$.

We may analyze the operation of the SO by assuming solutions of the form

$$V_o = \overline{V}_o e^{j(\omega_i t + \theta_o)} \tag{3}$$

$$V_i = \overline{V}_i e^{j(\omega_i t + \theta_i)} \tag{4}$$

and defining

$$\phi = \theta_o(t) - \theta_i \tag{5}$$

as the instantaneous differential phase and

$$\Delta\omega = \omega_o - \omega_i \tag{6}$$

as the instantaneous tracking range. Substituting (3)–(6)

into (2) yields the transformed equation

$$\dot{\phi} = -3K(\sin\phi - \Delta\omega/K) \tag{7}$$

where

$$K = \frac{G_{m1}\overline{V}_i}{2C\overline{V}_o} \tag{8}$$

is the injection constant for the synchronous oscillator.

There are two regions of operation for the SO

1) driven but unlocked $\Delta\omega/K > 1$, and
2) driven and locked $\Delta\omega/K \leqslant 1$.

The condition for synchronization or "lock-in" is given by the requirement

$$\Delta\omega/K \leqslant 1, \qquad \text{for synchronization and "lock-in"} \tag{9}$$

with the SO's tracking bandwidth

$$\Delta f_o = \frac{G_{m1}\overline{V}_i}{2C\overline{V}_o\pi} \tag{10}$$

which is an instantaneous adaptive tracking bandwidth proportional to the magnitude of the input signal $\overline{V}_i$. We may define a gain-tracking-bandwidth product as

$$\frac{\overline{V}_o}{\overline{V}_i} \times \frac{G_{m1}\overline{V}_i}{2C\overline{V}_o\pi} = \frac{G_{m1}}{2\pi C}. \tag{11}$$

In (10) $\overline{V}_o$ is a constant and with a specified bias condition (i.e., fixed G_{m1}), the tracking bandwidth will adaptively follow changes in the input signal level to preserve the relationship shown in (11).

The driven but unlocked SO may be analyzed, following the technique of Adler [3], to find a solution of (7) for ϕ

$$\tan[\phi/2] = \frac{K}{\Delta\omega} + \frac{K}{\Delta\omega}\sqrt{(\Delta\omega/K)^2 - 1} \cdot \tan\left[\frac{3K(t-t_o)}{2}\sqrt{(\Delta\omega/K)^2-1}\right] \tag{12}$$

where t_0 is an integration constant. The differential phase ϕ can be seen from (12) to be a periodic function of time and, therefore, the output voltage V_o has a discrete Fourier spectrum. The spectrum component of the SO's output voltage at the injection frequency ω_i may be found, following the method of Armand [16], as

$$\overline{V}_o(\omega_i) = \frac{j\overline{V}_i}{\dfrac{\Delta\omega}{K} + \sqrt{(\Delta\omega/K)^2 - 1}} e^{j\omega_i t}. \tag{13}$$

Thus, the unsynchronized but driven SO produces a discrete Fourier component at the injection frequency whose phase is $\pm\pi/2$ and changes sign with the frequency difference. We also observe the amplitude characteristics provide frequency discrimination or filtering, an important property of the SO.

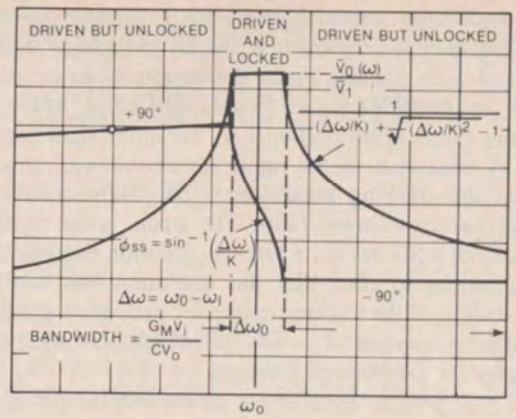


Fig. 3. Transfer function (gain-phase) for the simple SO circuit.

An analysis of the driven and locked SO shows that the steady-state phase error in the lock-in range becomes

$$\phi_{ss} = \sin^{-1}(\Delta\omega/K) \tag{14}$$

while the amplitude of the SO's output signal $\overline{V}_o$ is constant. An exact analysis of the SO operation in the lock-in region requires a nonlinear treatment [17]. The high internal gain of the SO maintains the output voltage constant within the lock-in range, while the input signal modulates the phase of the oscillator. Fig. 3 illustrates the amplitude and phase behavior of a SO as studied experimentally with a network analyzer with the vertical axis representing the steady-state gain $\overline{V}_o/\overline{V}_i(\omega_i)$, at the injection frequency.

We have discussed the steady-state characteristics of the SO; however, an important measurement is the phase acquisition time which is the time for the SO to reach steady-state from an unlocked condition. An analysis of (7) for the "driven and locked" region gives the time for the phase error

$$\tau(1 \text{ percent}) = \frac{1}{K\sqrt{1-(\Delta\omega/K)^2}} \tag{15}$$

to settle to within 1 percent of the final steady-state value, as given by (14). The importance of the injection constant K and the offset frequency difference $\Delta\omega$ are observed in (15). Low offsets, increased signal drive, and high G_m/C ratios lead to fast phase acquisition in SO's. We observe the phase acquisition time increases in (15) as $\Delta\omega$ approaches the edge of the lock-in range and this increase is countered by the high internal gain of the SO.

An important aspect of SO operation is the response of the SO to an injection signal at harmonics of the fundamental free-running oscillator frequency ω_o. An analysis of an SO under harmonic excitation indicates the injection constant K is increased by the order of the harmonic N.[1]

[1] Insertion of $N\omega_i$ for ω_i in (4) provides an injection constant $K = NG_{m1}\overline{V}_i/2C\overline{V}_o$ in place of (8). An SO in the fundamental mode exhibits a $\pm 90°$ phase shift over the tracking range, while an SO operating in the nonfundamental mode with harmonic excitation N exhibits a $\pm 90°/N$ phase shift over the tracking range.

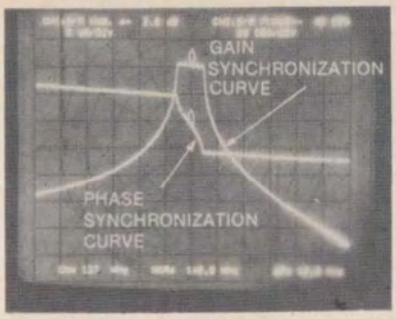


Fig. 4. Gain-phase synchronization curves of an SO.

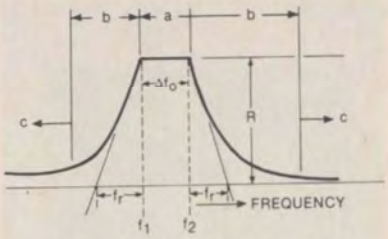


Fig. 5. Operation regions of an SO.

Thus, there is an improvement in the "tracking" bandwidth by N and the phase offset is reduced by N for small frequency offsets. In addition, the effective time constant for phase acquisition is also decreased by N for small frequency offsets. A perhaps more interesting aspect of harmonic excitation lies in the dramatic selectivity improvement in the frequency discrimination characteristics of the SO about the free-running SO frequency. The selectivity of the SO under harmonic excitation is improved by the $Q = \omega_o/\Delta\omega$ of the filter. A feature of harmonic excitation is the improved selectivity and the reduction in total phase shift across the lock-in range.

III. Experimental Results

Fig. 4 illustrates the gain-phase synchronization curves for an experimental SO. Fig. 5 illustrates the various regions of operation, which we will describe in detail. There are three distinct regions in an SO synchronization curve. Region "a" is the tracking range or the so-called driven and locked region, where the SO is synchronized to the injected carrier between the frequencies f_1 and f_2 ($\Delta f_o = f_2 - f_1$). The output amplitude is constant in this region of operation. The second region, "b", is the transition region or the so-called driven but unlocked region. This region begins as the injected carrier starts to interact with the oscillator frequency and commences when the SO is "tracking" the injected carrier frequency. The nature of this transition region varies depending upon modifications to the basic SO circuit and the manner of signal excitation. In general, the transition region is abrupt. Region "c" is characterized by the external circuit elements (i.e., pre- and post-filtering) and represents a reduced interaction between the injected carrier and the SO.

The synchronization curves of an SO have several features worthy of mention. The flatness of the gain synchronization curve is a unique property of the SO and distinguishes the latter from linear networks and, in particular, injection-type Van der Pol oscillators which are characterized by an output amplitude dependent upon the injected carrier amplitude and frequency [1], [2]. The primary function of the injected signal is to modulate the phase of the SO, while the SO's amplitude remains unchanged in the lock-in region. Outside the lock-in region, the injected signal determines the frequency discrimination or filtering characteristics of the SO, while the SO's phase remains unchanged. If the SO were a linear network, then according to linear network theory [18], [19], the phase of the transfer characteristics should display abrupt changes and extend several octaves beyond the abrupt gain changes within the transition regions. An additional feature of the SO is the almost linear phase throughout the tracking region.

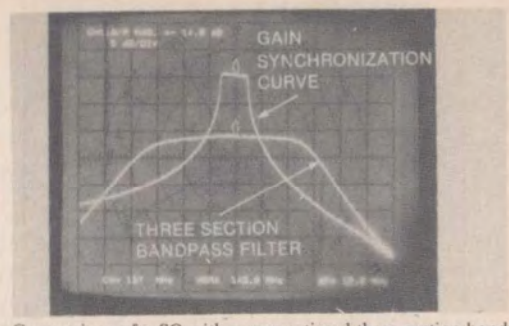


Fig. 6. Comparison of a SO with a conventional three-section bandpass filter. The SO is unmodified as shown in Fig. 1.

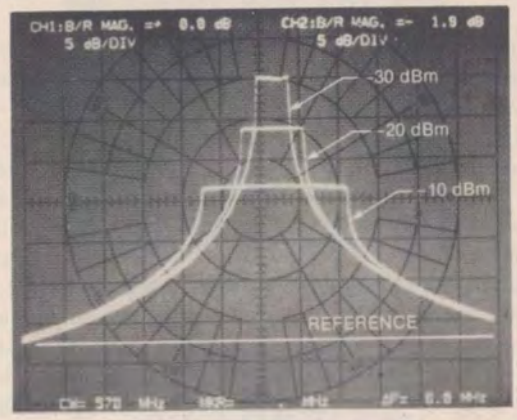


Fig. 7. Adaptive "tracking" bandwidth and "gain-attenuation" features of an SO.

The so-called "skirt" selectivity (R/f_r from Fig. 5) of a simple SO (unmodified by external networks and harmonic excitation) is considerably higher than a linear filter. Fig. 6 compares the skirt selectivity of a three-section 140-MHz bandpass filter to the filter characteristics of a simple SO operating at a center frequency of 140 MHz. The SO has a skirt selectivity of 10 dB/600 kHz compared with a three-section filter selectivity of 10 dB/2.4 MHz.

An important aspect of SO's is the adaptive "tracking" range as described in (10) and shown in Fig. 7 for injection carrier levels of -30, -20, and -10 dBm. Since the

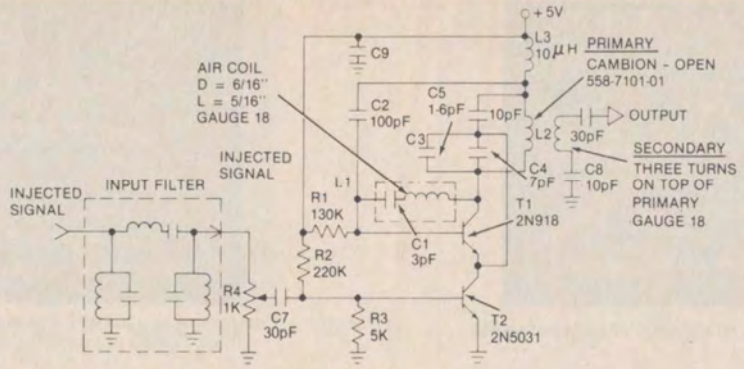


Fig. 8. Modified SO to enhance filtering performance.

output amplitude remains unchanged in the lock-in region, the network analyzer displays a different "gain" or "sensitivity"[2] characteristic for each input signal level. The −30-dBm carrier causes the highest "gain" with respect to the reference level 2, as defined in Fig. 5; however, if reference level 1 were used for the comparison, then the −30-dBm carrier would create the highest "attenuation" providing all curves are referenced to level 1. The SO features carrier selectivity, as illustrated in the decreasing bandwidth and upward swing in the curves of Fig. 7, with simultaneous improvement in noise rejection. For example, at an injection level of −100 dBm the tracking range reduces to 18 kHz. Thus, as a filter or as a tracking network, the bandwidth of a SO depends upon the injection level of the carrier. A transfer characteristic of a SO must specify the injection level. A SO is an RF filter with variable bandwidth and variable "gain-attenuation" level—a function of injected carrier amplitude—in contrast with linear filters, where gain and bandwidth are independent of injection level. Thus, the SO is an adaptive network element for signal processing.

A. Performance Enhancement Techniques

Several methods have been examined to enhance the performance of the SO's:

1) addition of a series-tuned circuit in the feedback path of the oscillator transistor;
2) addition of an external bandpass filter at the input of the SO;
3) harmonic injection into the SO;
4) combinations of 1)–3); and
5) cascaded operation of SO's.

The first four techniques are illustrated in Fig. 8 in the dotted lines. The SO of Fig. 8 oscillates at 560 MHz with the addition of the series L_1C_1 tuned circuit. The original transfer characteristics of the SO, without the L_1C_1 network, displayed a skirt selectivity of 15 dB/300 kHz. The

[2] The word "gain" or "sensitivity" is defined by (13) or $\bar{V}_o/\bar{V}_i$, but differs slightly from its standard usage. The output amplitude of the SO remains constant for varying input signal levels. The change of gain in (13) is due to $\bar{V}_i$ only.

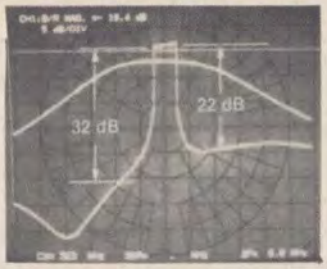


Fig. 9. Gain-synchronization curve of SO shown in Fig. 8 with L_1C_1 network. 560-MHz center frequency.

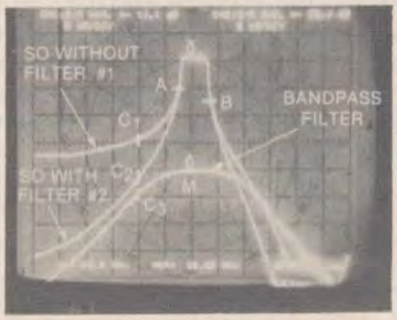


Fig. 10. Gain-synchronization curve of SO with input filter and 70-MHz center frequency.

incorporation of L_1C_1 increased the selectivity to 15 dB/40 kHz with 32 dB and 22 dB out-of-band rejection as shown in Fig. 9. Superimposed on the SO gain-synchronization curve is the transfer characteristics of a three-section 560-MHz bandpass filter. Fig. 10 illustrates a gain-synchronization curve of a standard 70-MHz SO, the transfer characteristics of a three-section 70-MHz bandpass filter, and the combined gain-synchronization curve with the bandpass filter connected to the input of the SO. The influence of the input filter illustrates the importance of the input coupling network on the regeneration process, where the latter increases the out-of-band attenuation of the SO faster than the attenuation provided by the input filter. We can observe the high internal gain of the SO is sufficient to compensate for filter losses within the lock-in range.

Fig. 11 illustrates the gain-synchronization curve of the 70-MHz SO with harmonic injection at 140 MHz. We notice the phase shift is ±45° due to the division process

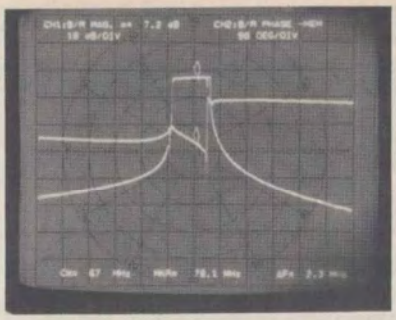


Fig. 11. Harmonic injection at 140 MHz into a 70-MHz SO.

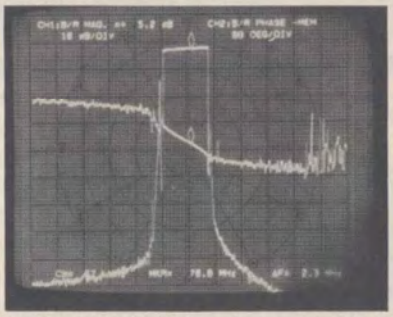


Fig. 12. The SO of Fig. 11 with a three-section 140-MHz filter connected to the input.

by the SO and the "gain-attenuation" level and skirt selectivity are dramatically increased with a gain scale of 10 dB/div. Fig. 12 demonstrates the gain-synchronization curve of the same SO with a 140-MHz filter connected to the input. We notice further enhancement of skirt selectivity and out-of-band attenuation. The former is approximately 24 dB/10 kHz in contrast with a three-section filter of 24-dB/3.6-MHz skirt selectivity. The performance enhancement with cascaded SO's will be described in the section on Carrier Recovery.

B. Frequency Division with SO's

SO's can divide by integers as well as rational integer numbers [20], such as 4, 1/4, and 3/2. Fig. 13 illustrates the injected waveform and the oscillator waveform in a division-by-1/4 process. We observe the synchronization occurs when the input waveform is at its maximum and the output waveform at it minimum. Fig. 14 depicts a division process by 3/2 where every third injected waveform synchronizes every second oscillator waveform. As the synchronization between the injected carrier and the oscillator waveform occurs at only one point in time, there cannot be false lock when SO's are employed in burst modem applications. Each division process by 2 reduces the phase shift between input and output of the SO by 90°.

C. Storage Time in SO's

Another interesting and useful feature of the SO is its capability to store or retain input frequency information. The degree of storage depends upon the input signal level.

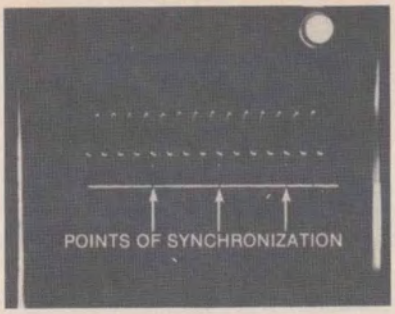


Fig. 13. Synchronization in a divide-by-1/4 process.

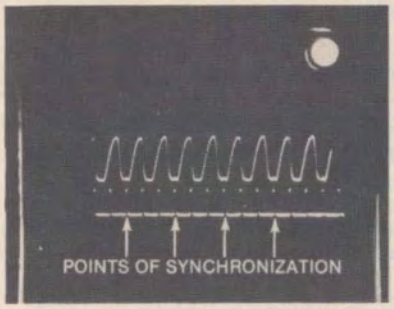


Fig. 14. Synchronization in a divide-by-3/2 process.

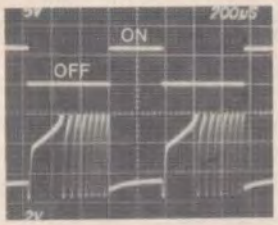


Fig. 15. Storage in an SO with −12-dBm signal drive.

This feature of the SO is especially useful in clock recovery networks [21] when the data consist of a time sequence of all "ones" or all "zeros" for an extended period of time, whereby no synchronization pulses are provided to the SO. During this period of time the SO continues to oscillate at the frequency or near the frequency of the original data transitions. Figs. 15 and 16 show the memory time of an SO driven by -12 and -3 dBm, respectively. During the positive pulses the injection frequency is applied to the SO, whereas during the negative pulses the SO is free-running. A phase detector detects the phase error between the injected carrier and the output of the SO and displays the error on a scope. When the SO is injected with the external carrier, the SO is synchronized and the phase detector supplies a dc output to the scope. In the absence of signal injection, the SO tries to return to its natural frequency and the difference of frequency appears on the scope. The time for the SO to return to its natural frequency is considered as the storage time.[3] While the SO tries to

[3] In general, clock recovery networks operate with signal-to-noise levels well above 0 dB and sufficient signal drive to utilize the inherent memory or storage in SO's.

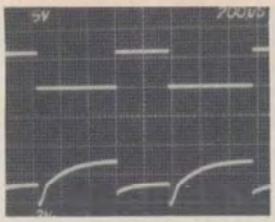


Fig. 16. Storage in an SO with −3-dBm signal drive.

return to its natural frequency, shortly after the injected carrier is turned off in Fig. 15, the phase detector output level remains at dc through the turn-off time in Fig. 16 indicating a higher storage time.

D. Acquisition Time in SO's

We can estimate the acquisition time of an SO which is synchronized by its natural frequency (i.e., low offset). In this case, (15) can be written as

$$\tau(1 \text{ percent}) \doteq \frac{1}{K} = \frac{2C_3\overline{V}_o}{G_{m1}\overline{V}_i} = \frac{1}{\pi(2\Delta f)} = \frac{1}{\pi\Delta f_o}. \quad (16)$$

For a 70-MHz SO with a 2-MHz tracking range we have the following measured parameters:

$$f_o = 70 \text{ MHz} \qquad G_{m1} = 100 \text{ mA/V} \qquad \overline{V}_i = 2 \text{ mV}$$
$$\Delta f_o = 2 \text{ MHz} \qquad C_3 = 8 \text{ pF} \qquad \overline{V}_o = 2 \text{ V}$$

which yields an acquisition time $\tau = 160$ ns in agreement with experimental results on SO's below 100 MHz. At higher frequencies the acquisition time becomes larger due to the input time constant of the SO and wiring/parasitic effects. The frequency offset affects the acquisition time when $\Delta\omega \to K$. In general, the maximum frequency offset in communication systems does not exceed ± 100 kHz, which justifies the approximation in (16).

E. SO's in the Nonfundamental Mode of Operation

We have discussed, in connection with Figs. 11 and 12, the performance of an SO with harmonic excitation. For example, a 70-MHz SO can be synchronized by 140, 210, 280 MHz, etc., and an output signal recovered through a bandpass filter. This output signal possesses superior signal-to-noise characteristics when compared with 70-MHz excitation, which is called the *fundamental-mode of operation*. The harmonic excitation or *nonfundamental mode of operation* is an important property of the SO and is enhanced by the nonlinear operation of the SO, which creates a high harmonic content in the output signal. For example, an SO which has a 130-MHz free-running frequency is synchronized by a 390-MHz carrier and the output is recovered at 390 MHz. The waveform of this specific SO is rich in the third harmonic (−36.2 dBm) as shown in Fig. 17. Experimental SO's with high third harmonics when injected with third harmonics have shown to have wide tracking range. Fig. 18 demonstrates the

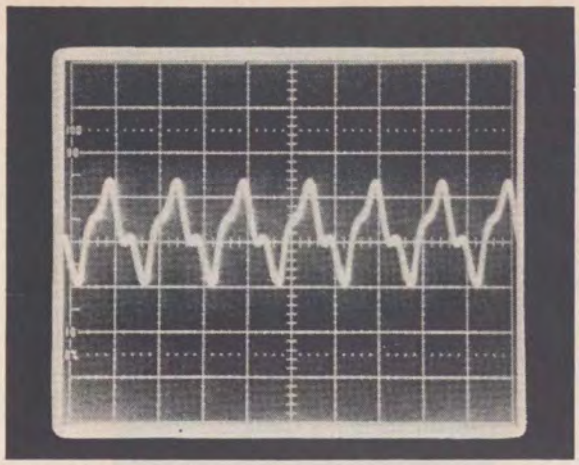


Fig. 17. High harmonic content in the SO's output waveform: 131 MHz (−26.3 dBm); 262 MHz (−45.1 dBm); 393 MHz (−36.2 dBm).

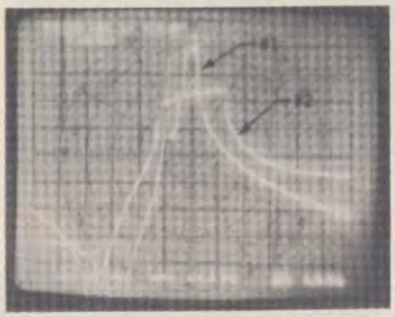


Fig. 18. Fundamental versus nonfundamental mode of operation: #1 — SO transfer function with fundamental (131-MHz) excitation; #2—SO transfer function with nonfundamental (393-MHz) excitation.

increase in tracking range for the harmonically pumped SO over the SO in the fundamental mode. The tracking range is increased by the order of the harmonic ($N = 3$) and the sensitivity is enhanced by the increased third harmonic content in the oscillator output signal. We should note that the analysis presented in this paper deals primarily with linear "pure" sinusoidal SO waveforms.

F. Filtering Properties of SO's

Due to the narrow resolution bandwidth the input thermal noise of the SO ($\overline{e}_f^2 = 4$ KTBR) is very low and thus the input sensitivity very high. It is interesting that the sensitivity (gain) increases as the input level reduces (see Fig. 7). This is why an SO can track signals as low as −100 dBm. The SO has two functional properties which determine noise rejection (filtering): the skirt selectivity of the tracking curve and the resolution bandwidth. The skirt selectivity defines the same functional properties as a linear filter is SOs operating in their fundamental mode. Steeper skirt selectivity means higher number of poles and thus better noise rejection [18], [19].

The SO has a resolution bandwidth similar to the operation of a spectrum analyzer. This is an important feature of an SO which does not exist in other tracking networks, such as phase-lock loops or Costas loops. In a phase-lock

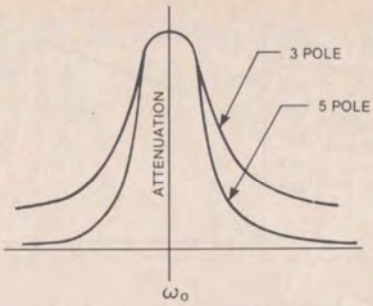


Fig. 19 Conventional filter transfer characteristics.

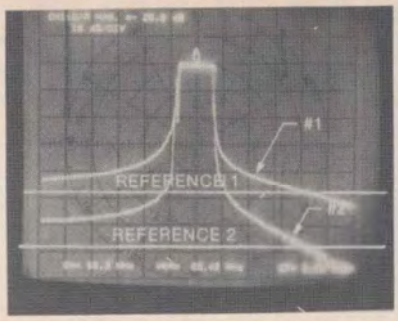


Fig. 20. Transfer characteristics of an SO with and without input filter.

loop when the loop filter bandwidth is defined, both the noise rejection and tracking range are fixed. They must be compromised in a given design. In a SO the tracking range and resolution bandwidth are independent of each other and can be optimized individually. The resolution bandwidth in an SO is a function of the internal regeneration process or Q-multiplication and can be less than 1 kHz. The external signal is incorporated in the regeneration process instantaneously. This is why an SO can track signals with -40-dB signal-to-noise ratio. The skirt selectivity of an SO can be improved by increasing the attenuation, not necessarily the gain. For example, Fig. 19 illustrates the transfer characteristics of two bandpass filters with three and five poles. The five-pole filter has steeper skirt selectivity and higher out-of band attenuation and, therefore, better noise-rejection properties. The bandpass gain level remains almost the same while the skirt selectivity increases in the five-pole filter. The transfer characteristics of four-terminal networks, whether linear or nonlinear, display the same functional properties. High skirt selectivity and low resolution bandwidth are the basic requirements for improved noise rejection. The SO's attenuation characteristics in the driven but unlocked region (see Fig. 3) are determined by the carrier injection level. Thus, two SO's which display the same relative transfer characteristics and identical skirt selectivities may have completely different noise rejection properties depending upon the variation in G_m's. From (13) and Fig. 3 we can write the out-of-band attenuation as

$$\text{attenuation (dB)} = -20 \log [2\Delta\omega/K]$$
$$= -20 \log [4C\overline{V}_o\Delta\omega/G_{m1}\overline{V}_i]. \quad (17)$$

Other factors remaining the same, the SO which has the lower G_mV_i product possesses the higher out-of-band rejection and steeper skirt selectivity. Fig. 20 illustrates two gain-synchronization curves for the same SO with (#2) and without (#1) an input filter to alter operating conditions. Thus, SO's require the specification of the carrier injection level V_i and the gain G_{m1} in order to assure uniform absolute transfer characteristics.

An SO exhibits high noise rejection while maintaining a wide tracking range. To illustrate the interesting properties of an SO we have performed noise measurements with the setup shown in Fig. 21. The carrier source is applied while

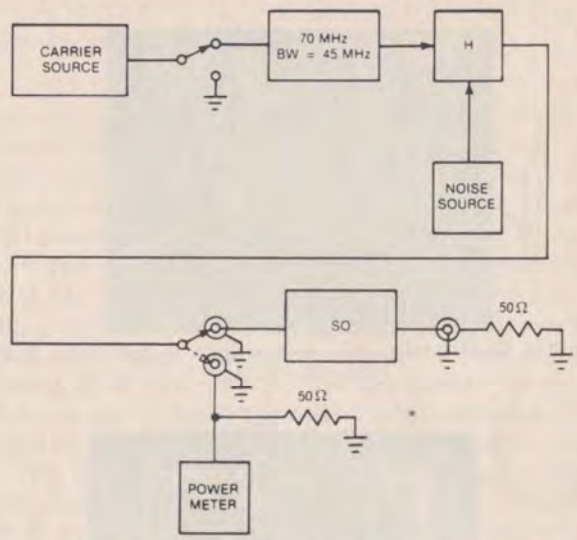


Fig. 21. Experimental determination of SO performance under noise injection.

the noise is inhibited and vice-versa to determine the carrier and noise power across the 50-Ω load. The carrier and noise sources are actuated and the output of the hybrid combiner H is applied to the SO. The 140-MHz bandpass filter with 45-MHz bandwidth serves as the reference for the injected carrier-to-noise level.

Fig. 22 shows the gain-synchronization curve of a 140-MHz SO with a -36-dBm carrier injection level while maintaining a 700-kHz tracking range. The carrier injection at the input of the SO is 4 mV. Fig. 23 shows the gain-synchronization of the same SO under a -11-dB carrier-to-noise power (same signal level). We observe the tracking range of the SO is reduced by approximately 50 kHz. The input and output waveforms of the SO under these noise conditions are illustrated in Fig. 24. The carrier-to-noise ratio at the output of the SO is 28 dB with an overall 39-dB improvement between input and output. In order to achieve the same improvement with a linear bandpass filter, the filter should have less than a 0.5-kHz bandwidth in contrast with a 650-kHz tracking range of the SO. Thus, the following conclusions may be drawn from these experiments: 1) the noise reduces (slightly) the tracking range; 2) the SO performs as a narrow bandpass filter for each frequency it tracks (resolution bandwidth);

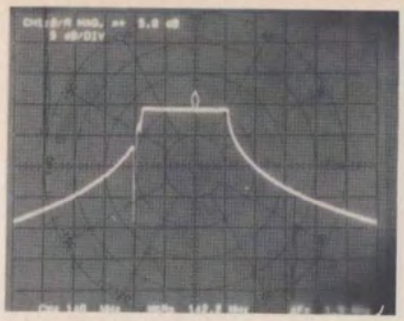


Fig. 22. 140-MHz SO with −36-dBm signal injection under low noise conditions.

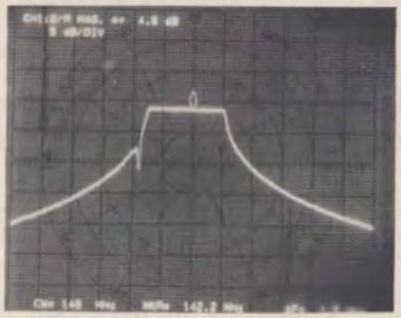
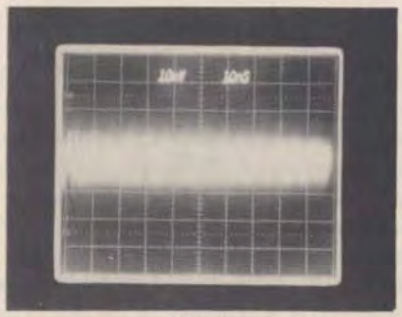
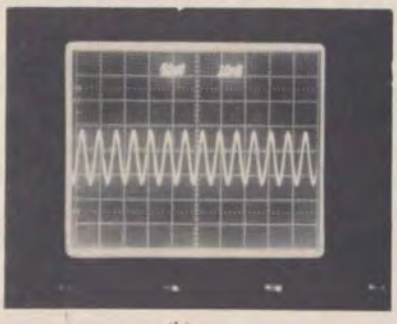


Fig. 23. 140-MHz SO with −36-dBm signal injection and −11-dB carrier-to-noise ratio.



(a)



(b)

Fig. 24. 140-MHz SO of Fig. 23. (a) Input signal. (b) Output signal.

3) the SO has a tracking range which is 1300 times its "effective" filtering noise bandwidth; and 4) as phase is a function of tracking range (see (14)), the phase error per frequency offset remains low. Thus, the SO is an adaptive wide-band tracking filter which has a very low resolution bandwidth and "locks" to the injected carrier within the tracking range with a high degree of noise rejection, while maintaining wide tracking range.

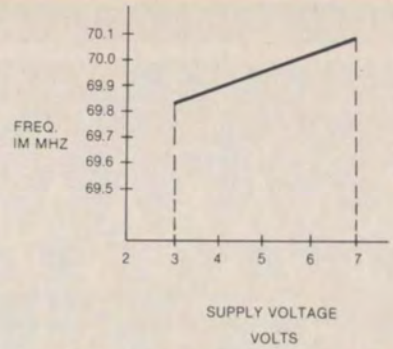


Fig. 25. Variation of SO's free-running frequency ω_o as a function of supply voltage V_c.

Due to resolution bandwidth SO's have substantially higher noise rejection properties than phase-lock loops and Costas loops for a given tracking range. The SAW devices, however, which have higher Q than LC filters, still are far behind in noise rejection compared to SO's.

G. Temperature Compensation of an SO

The frequency stability of an SO is influenced by temperature and supply voltage fluctuations. In practice, we desire a stable free-running SO frequency under high temperature and a reduced phase error caused by frequency offsets. Fig. 25 illustrates the variation of the SO's free-running frequency as a function of supply voltage. Experimentally the free-running frequency of the SO decreases as the temperature increases. Thus, we can temperature compensate the SO by the insertion of a negative temperature coefficient resistor in series with the power supply. For example, a 560-MHz carrier recovery SO demonstrates a 30-ppm stability (16.8-kHz frequency drift) with a deterioration in the BER of only 0.3 dB between 15°C and 31°C when operated over a 24-h period.

H. Carrier Recovery with SO's [22]–[24]

SO's may be used as both carrier and clock recovery networks in QPSK modems. Carrier recovery requirements are more demanding than their clock recovery counterparts because of the low carrier-to-noise levels and the need for a wider tracking range. Thus, we will concentrate on the carrier recovery network as shown in Fig. 26. In this example, a 70-MHz IF is applied through a noise source to 4× frequency multiplier whose output is applied to a 280-MHz bandpass filter. The carrier-to-noise ratio at the output of the combiner is −3 dB. The output of the filter is amplified and applied to the 70-MHz SO. In the process of multiplying there is a −40-dBm power loss and a −18-dB degradation in the carrier-to-noise ratio. The 280-MHz filter bandwidth is maintained at 10 MHz so as not to disturb the acquisition time. The 70-MHz SO is injected with the 280-MHz carrier and the output recovered at 70 MHz. Figs. 11 and 12, previously discussed, illustrate the

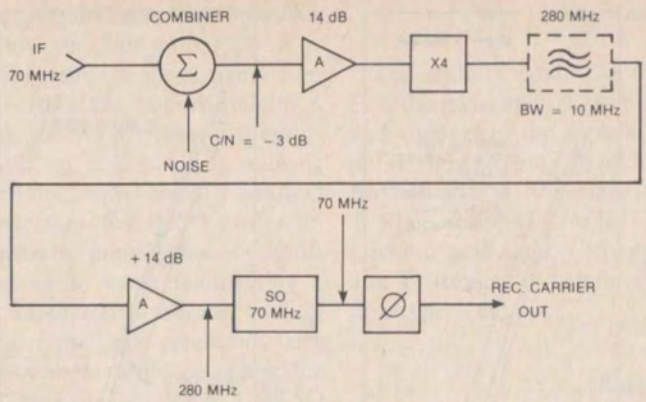


Fig. 26. SO carrier recovery network.

Fig. 27. Phase acquisition in the SO of Fig. 26.

gain synchronization curves of the SO carrier recovery network with and without the 280-MHz filter, respectively. The acquisition time of the carrier recovery network when the injected frequency is offset by 100 kHz from the free-running frequency is shown in Fig. 27. These results indicate acquisition occurs in less than 400 ns for the 100-kHz offset and less than 100 ns in the absence of frequency offset. Theoretical calculations based upon (15) for harmonic excitation ($N = 4$) indicate the acquisition time should be 160 ns, in excellent agreement with observations since experimental results include the delay time through the filter and the coupling networks. The input to the SO contains all the multiplication products and the filter characteristics of the SO are sufficient to remove these harmonics.

Clock and carrier recovery networks constructed with SO's have been tested in QPSK modems. The maximum deviation of the E_b/N_o ratio[4] (i.e., carrier-to-noise ratio at the output of the 70-MHz bandpass filter for a 60-Mbit/s data rate) from the theoretical value is 0.5 dB. The maximum deviation increases to 0.9 dB for a 150-kHz IF frequency offset. The unique synchronization properties of the SO (see Figs. 13 and 14) enable modem operation in the burst mode without false-lock. A test was carried out with no false-lock in the burst mode during a four-day operation period. The introduction of an interference signal, after acquisition to the synchronizing signal, does not disturb the original synchronization process. The SO remains locked to the synchronizing signal even though the interference signal has a comparable power level. The SO performance is illustrated in Figs. 28 and 29 for 60- and 120-Mbit/s modems. SO performance is *superior to standard PLL hardware*. The BER curve deviates only 0.2 dB from the hardwired case. The insignificant change in the BER performance due to frequency offsets and the improved performance over *the standard recovery networks*, using various versions of phase-lock loops, indicate the SO has a wider tracking range and higher noise rejection.

The 120-Mbit/s modems were tested in back-to-back operation and also while connected to the TDMA terminal. Tests were performed with a pseudorandom sequence of $2^{15}-1$ bits. The carrier recovery network shown in Fig. 26 was used for the 120-Mbit/s modem. The 140-MHz SO was driven by 560 MHz. Due to high losses at 560 MHz (38 dB) on the standard PC board the signal-to-noise ratio was low and the tracking range was reduced to 300 kHz at $E_b/N_0 = 7$ dB. For wider tracking range two cascaded SO's were used to reduce the phase shift per unit frequency offset. The difference between the latter and the former BER results can be detected when the frequency offset exceeds ± 20 kHz. At lower frequency offsets the two BER results are the same as shown in Fig. 29. The unique word consists of two consecutive 12 bits. The preamble consists of 176 symbols, 48 of which are for carrier recovery and 128 for clock recovery. The guard time between bursts is variable and can be reduced to zero. The input to the receiver is $+2$ to -10 dBm. An AGC is used with a ± 6-dB dynamic range.

In certain applications, we may desire additional performance enhancement in SO synchronization networks. We have performed experiments with two cascaded SO's by the insertion of a 280-MHz SO between the 280-MHz filter and the 70-MHz SO in Fig. 26. In addition, we have isolated the two SO's with 3-dB pads. The gain and phase synchronization curves are shown in Fig. 30. The cascaded SO carrier recovery network displays over 1-MHz tracking range with an injected carrier to noise (before the 4× frequency multiplier) of -3 dB, while its single SO coun-

[4] E_b/N_o (dB) $= C/N$ (dB) $- 10 \log (BW/BR)$, where C = carrier power, N = noise power, BW is the bandwidth of the IF filter, and BR the bit rate.

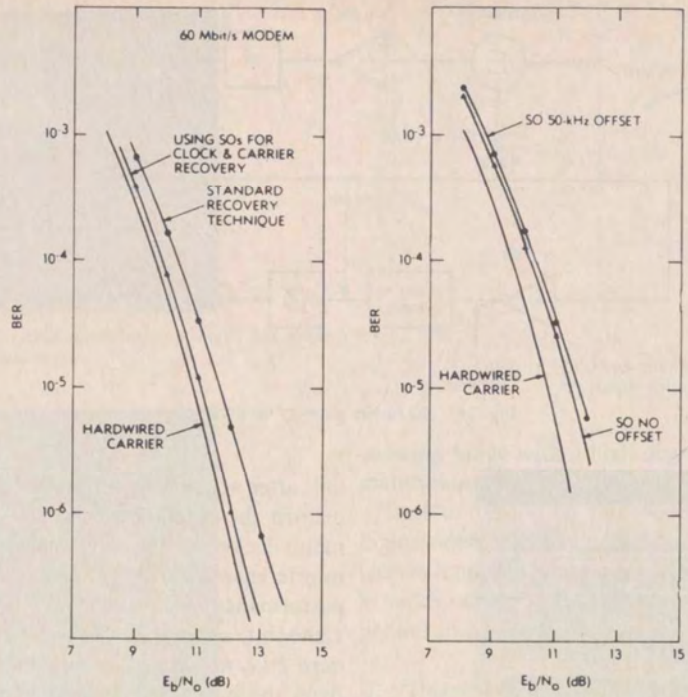


Fig. 28. BER performance of 60-Mbit/s modem.

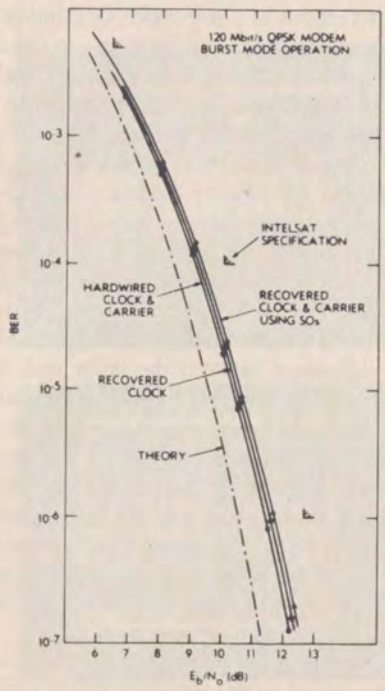


Fig. 29. BER performance for 120-Mbit/s modem.

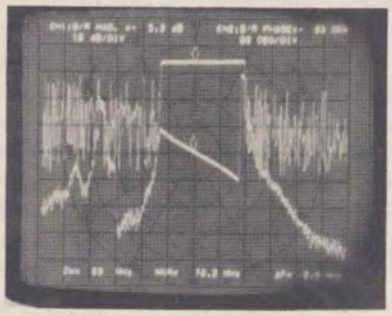


Fig. 30. Gain-phase characteristics for a cascaded carrier recovery network—SO_1 = 280 MHz, SO_2 = 70 MHz.

terpart, under identical conditions, displays a 150-kHz tracking range. In addition, the gain of the cascaded network is over 50 dB (see Fig. 30) as compared with 25 dB for the single SO network. The actual carrier-to-noise ratio at the input of the SO networks is −13 dB due to the −18-dB deterioration in the 4× multiplier and subsequent 8-dB improvement in the 280-MHz filter. In general, carrier recovery networks operate with carrier-to-noise ratios above 0 dB at the system input; therefore, cascaded operation of SO's in carrier recovery when the IF is under 140 MHz is usually not necessary.

IV. Conclusions

The synchronous oscillator (SO) is an important functional element for synchronization and tracking in communication systems. An SO is characterized by an adaptive instantaneous tracking bandwidth proportional to the magnitude of the input signal, while noise rejection is based mainly upon very narrow resolution bandwidth produced by the regeneration process of the oscillator. In the tracking range (i.e., the "lock-in" region) the output signal

amplitude remains constant and unaffected by variations in the input drive level; however, the output phase is modulated to synchronize and track the input signal even to power levels as low *as* -100 *dBm* while sustaining a 18-kHz tracking range. Thus, the SO performs like a narrow-band adaptive filter with an instantaneous tracking bandwidth, high skirt selectivity, and narrow resolution bandwidth for high noise rejection. Single SO carrier recovery networks have demonstrated improvement by 40 dB of the input signal-to-noise ratio, while maintaining a 800-kHz tracking range at input signal-to-noise level of -11 dB. Cascaded SO's under the same conditions have demonstrated a 60-dB improvement while extending the tracking range to 1.6 MHz. The acquisition time of the SO is inversely proportional to the tracking bandwidth ($2\Delta\omega = G_m\bar{V}_i/C\bar{V}_o$) for low-frequency offset. For example a 70-MHz SO can perform phase acquisition in less than 400 ns and track a 140-MHz carrier with an input signal-to-noise ratio of -40 dB while maintaining a 400-kHz tracking range. Extending the tracking range to 2 MHz in the same SO provides acquisition times less than 100 ns. The ability to achieve high-speed phase acquisition is an important feature in burst-modem applications. In addition to sensitivity, filtering (selectivity), wide tracking range, and fast acquisition, the SO possesses linear phase-shift characteristics for the useful tracking range which provides a *constant group delay*. The high internal gain of the SO reduces the steady-state phase error in synchronization to a low value ($\phi_{ss} \doteq \Delta\omega/K$) where $\Delta\omega$ is the frequency offset and K the injection constant defined by (14). An important aspect of SO's, especially in clock recovery networks, is an *inherent memory* (*storage time*) *corresponding to 20–25 bits* which may be adjusted so as not to deteriorate the acquisition time and BER. SO's may be used in applications other than carrier and clock recovery networks for modems. For example, SO's are excellent RF filters and integer (non-integer) frequency dividers/multipliers. In addition, SO's may be used as synchronization networks for minimum shift keying (MSK), phase-shift keying (PSK), and spread-spectrum communication systems. SO's can be used also in FM to improve selectivity and carrier-to-noise levels. (The BER results obtained on 60 and 120-Mbit/s QPSK modems indicate SO's can perform high-speed synchronization and tracking, especially in burst-mode operation, with performance near hard-wired transmission (0.4 dB from theory) without false locks and with long-term stability at elevated temperatures.)

This paper has described a new synchronization and tracking network, the *synchronous oscillator* (SO). We have discussed a particular application, namely, carrier and clock recovery in high-speed QPSK modems operating in the burst-mode; however, the useful properties of SO's extended well beyond the subject of this paper and impact applications where synchronization and tracking of signals embedded in noise are desired. The concepts presented in this paper can be realized together with support circuitry on a single integrated chip with *RC*-type continuous or switched capacitor filters.

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949 a| TK7800.M5 v.43 Jan-Apr 2000 w| LCPER c| 1 i| 000051832148 l| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 4/8/2003 z| 7754

949 a| TK7800.M5 v.43 May-Aug 2000 w| LC c| 1 i| 000047639461 d| 4/19/2005 l| CATO-2 m| UP-ANNEX q| 1 r| Y s| Y t| PERIODICAL u| 8/8/2001 z| 7754

949 a| TK7800.M5 v.43 Sept-Dec 2000 w| LC c| 1 i| 000047636941 l| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/28/2001 z| 7754

949 a| TK7800.M5 v.44 Jan-Apr 2001 w| LCPER c| 1 i| 000047636934 d| 7/11/2004 l| CATO-2 m| UP-ANNEX q| 3 r| Y s| Y t| PERIODICAL u| 4/12/2001 z| 6339

949 a| TK7800.M5 v.44 May-Aug 2001 w| LCPER c| 1 i| 000048399722 d| 5/28/2003 l| CATO-2 m| UP-ANNEX q| 1 r| Y s| Y t| PERIODICAL u| 8/9/2002 z| 6339

949 a| TK7800.M5 v.44 Sept-Dec 2001 w| LCPER c| 1 i| 000048399715 d| 4/19/2005 l| CATO-2 m| UP-ANNEX q| 4 r| Y s| Y t| PERIODICAL u| 8/9/2002 z| 6339

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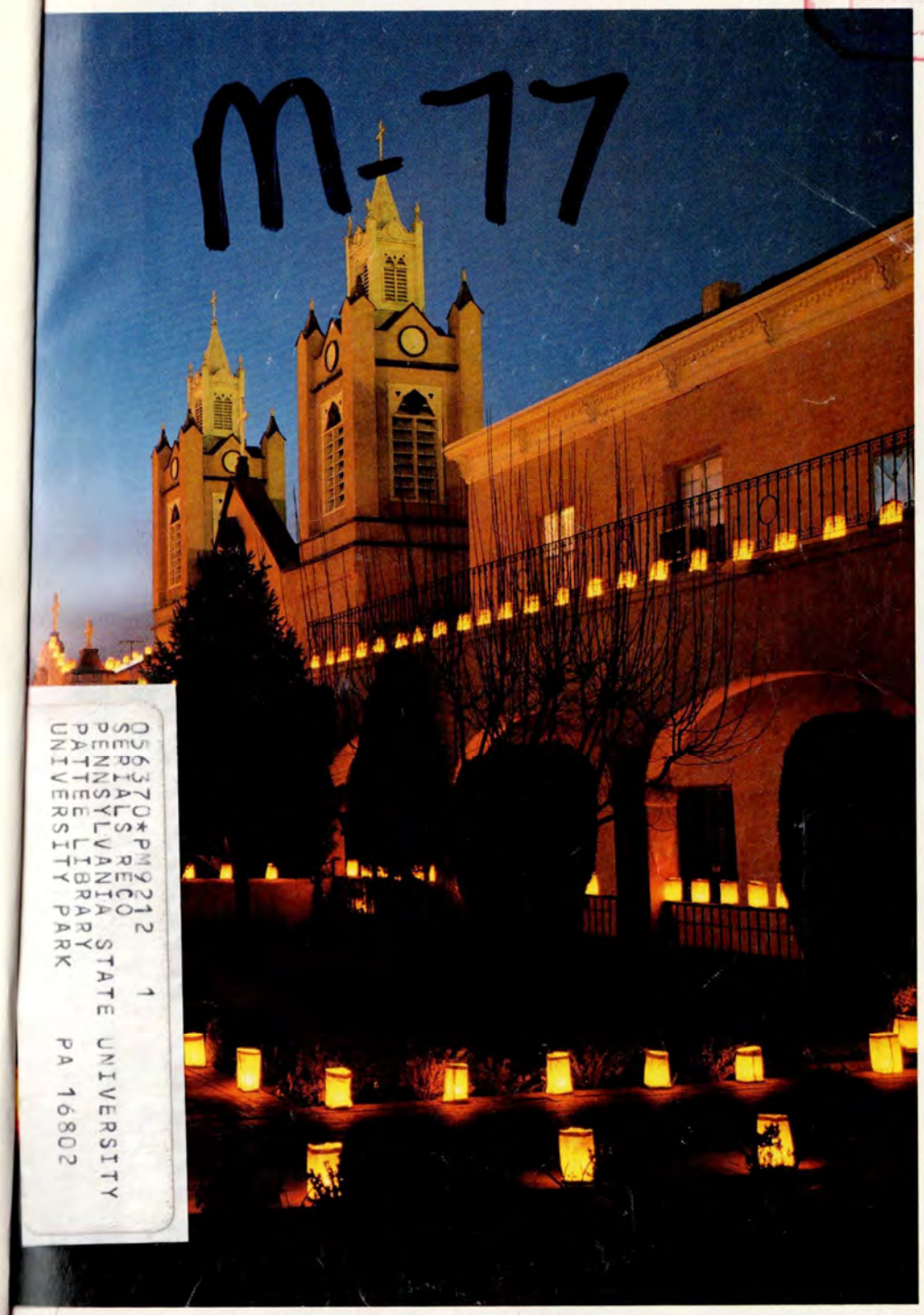

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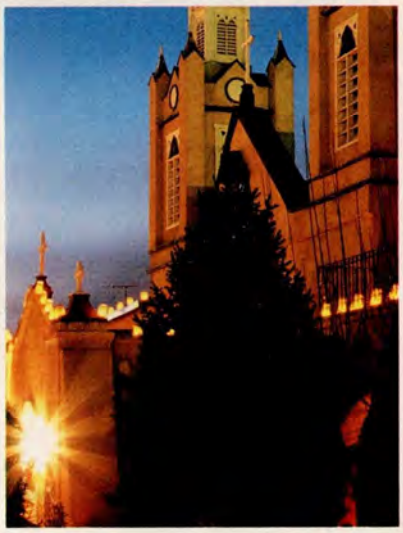
The San Felipe de Neri Church in Albuquerque, New Mexico. The photo was taken on Christmas Eve, when the church was lit up with luminarias, which are candles in bags of sand. Not only are luminarias the "lights" of the city around the holiday season, but they are representative of New Mexico's unique culture and heritage. Photo provided by Ron Behrmann Photography.



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Subharmonic Sampling of Microwave Signal Processing Requirements

Peter A. Weisskopf
Merit Microwave Corporation
Phoenix, AZ

Introduction

Modern microwave test instruments owe much of their capabilities to powerful microwave signal processing subsystems that employ high speed sampling circuitry. These sampling heads, as they are often called, can be found at the heart of the latest sampling oscilloscopes, frequency counters, time/frequency analyzers and vector network analyzers.[1-3] The sophistication at which these instruments analyze complex microwave signals is a testimony to the power of sampling techniques for use in extracting frequency, phase and vector information.[4]

Outside of the test equipment industry, sampling techniques have been employed by phase lock oscillator and synthesizer manufacturers for many years.[5] The emergence of commercially available sampling phase detectors is an indication of the need for these types of microwave signal processing components. Along with this demand comes the need for design and application information on microwave sampling hardware.

In this paper the theory behind subharmonic sampling is explored and the physics of the sample-and-hold process are examined when applied to microwave frequencies. Through time domain analysis, the criteria for optimum sampling hardware performance is established. Finally, a variety of microwave subharmonic sampling applications are presented.

Basis of Subharmonic Sampling

Subharmonic sampling as a microwave signal processing technique may be best understood by studying sampling theory. The basic premise of sampling theory states that when a signal f(t) of bandwidth β (Hz) is sampled at a rate of f_c, which is greater than or equal to twice the signal bandwidth or 2β, no information contained in the original signal is lost. Furthermore, taking the Fourier transform of the sampling function

$$fs(t) = f(t)S(t)$$

where S(t) is the periodic sampling function of pulse width τ and period $1/f_c$, the spectrum of the sampled signal may be derived. This results in a summation of individual Fourier transforms each centered at a positive and negative integer multiple of the sampling rate

$$Fs(\omega) = dF(\omega) + d\Sigma \sin \frac{(n\pi d)}{n\pi d * F}$$

$$(\omega - n\omega c)$$

For all $n = \pm\infty$ except $n = 0$

If the sampled signal is a baseband signal center at 0, then the reconstructed signal will be centered at 0. The frequencies of the first harmonic replica of the sampled signal are centered at 0, $\pm f_c$. The succeeding replicas ($\pm n \times f_c$) decrease in amplitude at the rate of $(\sin n\pi d)/n\pi d$. This theory is well suited for such applications as digitized voice. For this application the subharmonic sampling of a microwave signal must be considered.

In compliance with the guidelines of the sampling theory, the spectrum that results from a bandlimited microwave signal f(t) of bandwidth β that is sampled at the rate f_c, where $f_c \geq 2\beta$ and is also a subharmonic of f(t), or $n \times f_c = f(t)$ is considered. In this case, the fundamental replicas of the sampled signal is centered at f(t) with succeeding replicas of this reconstructed signal appearing at $\pm n \times f_c$. The FFTs, shown in Figure 1a where k = 512, show the (sin X)/X amplitude response of the sampled spectrum. The expanded FFT of Figure 1a, where k = 154, shows more clearly how the sampled RF input is reconstructed at the original frequency. The succeeding replicas of the RF input as shown are converted up and down in frequency and separated in frequency by the sampling rate F_c(Hz).

In this sampling simulation, the RF input was sampled at a subharmonic rate of one-tenth f(t). This is evident in the fact that there are indeed 10 replicas of the sampled signal in either upper or lower sideband of F(t). Typically, the baseband replica of F(t) located near DC, in this case

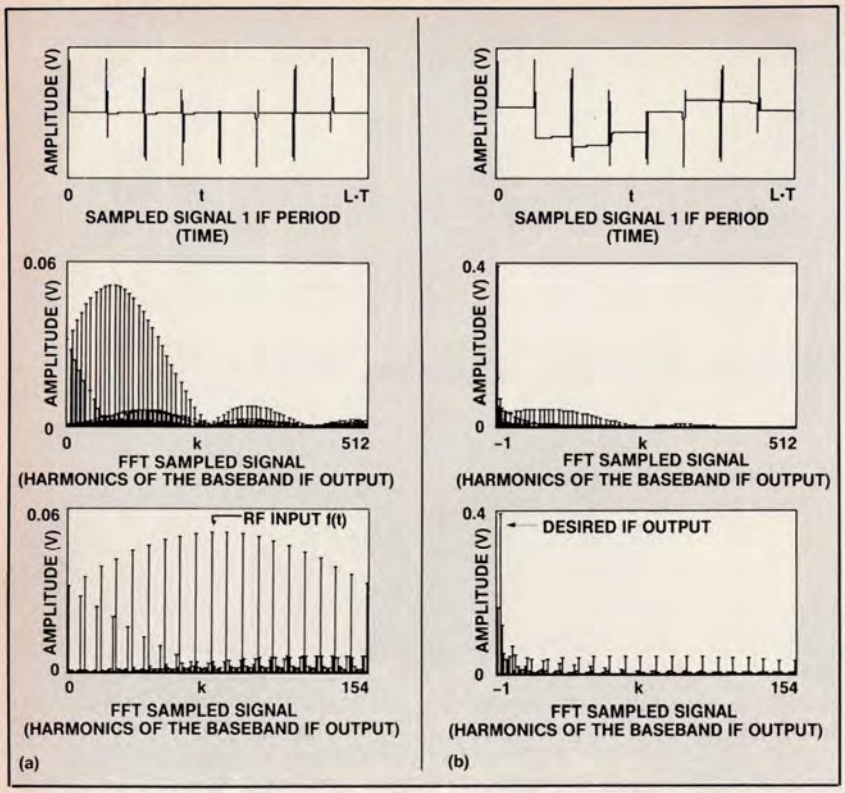

Fig. 1 Time domain analysis of the sampling process; (a) $fs(t) = f(t) \times S(t)$ periodic sampling, and (b) periodic sampling and hold into high impedance buffer.

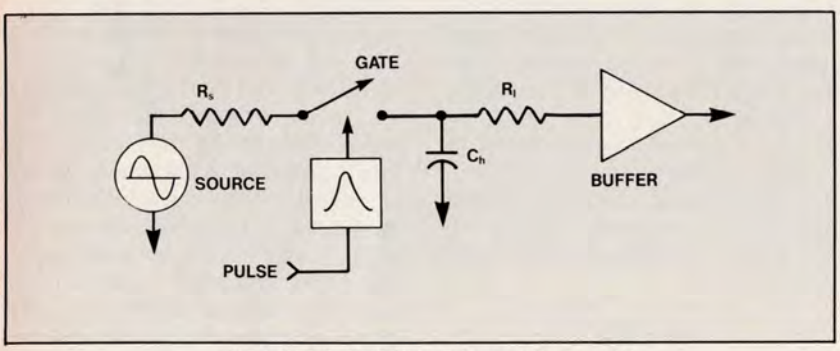

Fig. 2 An ideal subharmonic sampling model.

$f(t) - 10 \times f_c$, is the desired output signal. Extracting this baseband signal does require some circuit improvements.

Sample-and-Hold Circuit Offers Improvements Over Sampling

In order to perform sampling downconversion to baseband, the desired output of the FFT shown in Figure 1a would be the spectral replica at $f(t) - 10 \times f_c$. This is because the signal was sampled at the one-tenth subharmonic. All of the other spectral images in the FFT need to be rejected. To improve this situation, instead of multiplying F(t) by the periodic sampling function S(t), f(t) is sampled when S(t) is high and f(t) is held when S(t) is low. This logic statement allows emulation of the sample-and-hold process.

The output FFT spectrum of the defined subharmonic sample-and-hold process reveals its most significant property, which is the ability to downconvert a microwave or mm-wave signal to baseband with great efficiency and without loss of fidelity. Any loss in fidelity is due to the phase noise of the sampling clock degraded by 20 log of n. The Fourier transforms of Figure 1b show how the sample-and-hold process converts most of the sampled energy to the baseband spectral replica centered at $f(t) - n \times f_c$. This level of performance may be achieved in actual microwave and millimeter-wave subharmonic sample-and-hold circuitry when the circuit criteria are met.

Subharmonic Sample-and-Hold Circuit Modeling and Optimization

From the ideal subharmonic sample-and-hold model shown in Figure 2, parameters that must be considered during the design of a microwave sampling circuit may be defined. The source represents the microwave signal to be sampled. The source, defined by the function

$$f(s) = \sin(2\omega + \theta)$$

delivers a time variant voltage Vs of source impedance $R_s\ \Omega$. During the sampling cycle, the source signal is applied to the hold capacitor C_h via the gate. The sampling aperture (t_a) is the time the gate is closed. The resistance of the gate (R_d) has been included in the total source impedance (R_s).

The parameters that come into play during the hold cycle include the hold capacitance (C_h) and the load impedance of the buffer amplifier R_l. The hold time is the period of the sampling rate (f_c) minus the sampling aperture (t_a).

During the sample cycle, the gate closes for the duration of the sampling aperture and a charge is imposed on the hold capacitor. The charge on the hold capacitor in coulombs can be expressed by

$$q = \int f(i)*t\ dt$$

Because the value for Vs is a time variant function ($V(s) = \sin(\omega t)$), the integral becomes

$$q = \frac{(t_a - t_o)}{R_s} \int \sin(\omega t)*e^{\left(-\frac{(t_a - t_o)}{(R_s*C_h)}\right)} dt$$

over the interval of t_a through t_o

Integrating this function over the sampling aperture time for a given value of C_h and R_s yields the value for charge stored on the sampling capacitor in coulombs.

The value of the hold capacitor C_h is of significance as it is a parameter that the designer can easily control. Insight into the most judicious choice of sampling capacitance can be obtained by evaluating the

[Continued on page 242]

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160-240	MHz	500 W	4-7 µS
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210-225	MHz	1 MW	5 µS
400-420	MHz	14 KW	.0002 DC
950-1550	MHz	1 KW	.1 DC
900-1040	MHz	5/15 KW	1 µS
		20 KW	1 µS
1.2-1.35	GHz	500 KW	2 µS
1.25-1.35	GHz	4 MW	.2 µS
2.1-3.8	GHz	100 W	1.5-7 µS
3.2-3.3	MHz	10 KW	.001 DC
2.7-2.9	GHz	250 KW	0.8 µS
2.7-2.9	GHz	1 MW	1 µS
3.1-3.5	GHz	1 MW	1.3 µS
2.7-2.9	GHz	5 MW	2-3 µS
5.4-5.8	GHz	250 KW	.001 DC
5.4-5.9	GHz	500 W	.002 DC
5.4-5.8	GHz	5 MW	.001 DC
6	GHz	1 MW	1 µS
6.2-6.6	GHz	200 KW	.37 µS
8.7-8.9	GHz	1.2 KW	.045 DC
9.375	GHz	40 KW	.5-1-2 µS
8.5-9.6	GHz	250 KW	.0013 DC
9.375	GHz	100 KW	.5-1-2 µS
9.1	GHz	400 KW	1.8 µS
13.8-14.2	GHz	70 KW	.001 DC
15.5-17.5	GHz	135 KW	.33-1-3 µS
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125-450	KHz	4 KW
350-500	KHz	250 W
2-30	MHz	3 KW
4-21	MHz	40 KW
20-170	MHz	100 W
160-350	MHz	100 W
200-2000	MHz	40 W
385-575	MHz	1.5 KW
750-985	MHz	1 KW
950-1550	MHz	150 W
1.5-5.0	GHz	150 W
1.7-2.4	GHz	1 KW
1.7-2.4	GHz	10 KW
4.4-5.0	GHz	1 KW
7.25-8.8	GHz	150 W
7.4	GHz	2 KW
8.5-9.6	GHz	1 mw
8.7-10	GHz	150 W
16-17	GHz	40 mw

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5 KW Hard Tube	3 KV	2 A. 1.1 µS
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144 KW Hard Tube	12 KV	12 A. .001 DC
250 KW Hard Tube	16 KV	16 A. .002 DC
405 KW Float's Dk	20 KV	20 A. .1 DC
500 KW Line Type	22 KV	28 A. .001 DC
1 MW Hard Tube	25 KV	40 A. 002 DC
3 MW Line Type	50 KV	60 A. 30 µS
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13 MW Line Type	135 KV	112 A. 3 µS
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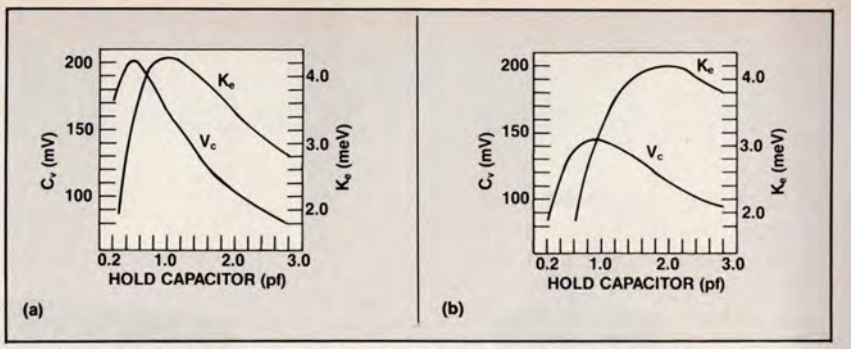

Fig. 3 Sampled voltage (Vc) and stored kinetic energy (K_e) per sample vs. hold capacitance; (a) source z transformer (50 to 25 Ω) and (b) source z transformer (50 to 12.5 Ω) with RF_{in} = 18.5 GHz @ 5 dBm and sampling aperture = 27 ps.

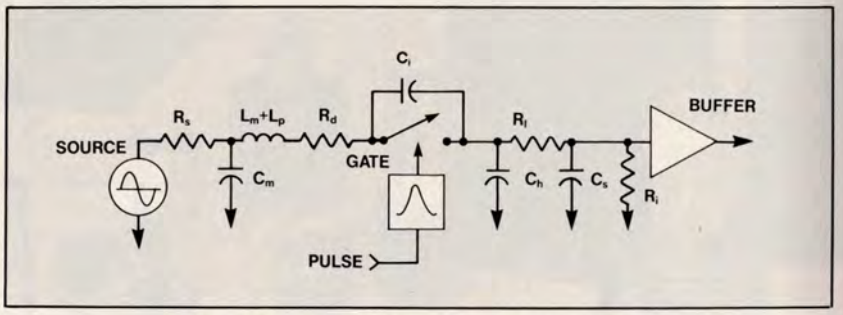

Fig. 4 An actual subharmonic sampling model.

kinetic energy stored during the sample cycle, which is equal to

$$K = \frac{(q^2)}{C_h}$$

The voltage stored on the capacitor is equal to

$$V_c = \frac{q}{C_h}$$

Figure 3 shows the effect of hold capacitance on the stored voltage V_c and the total kinetic energy for two values of R_s. The lower source impedance delivers the same kinetic energy to a larger hold capacitor that the higher impedance can only deliver to a small capacitance. The only difference for these two cases is the voltage (V_c), which decreases by the square root of the impedance ratio or by the square root of two. By increasing the incident power on the sampling circuit by 3 dB, the original voltage will be restored and the kinetic energy will be increased two fold. The hold circuit can achieve optimum performance with a larger capacitor.

Thus, it is important for the source to offer a low impedance to the gate-and-hold capacitor. In the actual sample-and-hold model, shown in Figure 4, the capacitor C_m has been included to demonstrate a matching structure that consists of C_m and $L_m + L_p$. This LC network makes convenient use of the series inductance of the bond wires in the sampling bridge diodes for the purpose of matching the 50 Ω source impedance to the 10 Ω gate impedance.

Output Buffer Amplifier Design Establishes IF Response

With R_s and C_h established to give maximum kinetic energy for a given sampling aperture, the effects of the buffer amplifier impedance on the stored voltage during the hold cycle are considered. An ideal sample-and-hold buffer circuit should be capable of measuring the voltage stored on the hold capacitor for the duration of the hold cycle without discharging the capacitor. The advantage of buffer circuitry, which can as nearly as possible meet this ideal requirement, is evident in the FFT of the ideal subharmonic sample-and-hold simulation, as shown in Figure 1b. Next, one may compare this to the output of a sample-

and-hold circuit that has a low impedance load, as shown in Figure 5.

The resulting poor hold duration manifests itself as an increasing inability of the sample-and-hold circuit to isolate the periodic sampling function discrete-line spectra from the output of the sample-and-hold circuit. On the other hand, if the buffer can be made to have a high impedance, the output signal will contain little harmonic energy and a much stronger baseband downconverted spectrum of the sampled signal.

Commercially available high impedance buffer amplifiers offer very impressive input impedances in the giga ohm ranges. However, these devices can have stray input capacitances of 3 pF. If connected in parallel with the hold capacitor, this capacitance would destroy the efficiency of the circuitry.

In a subharmonic sampling phase detector application, a 50 KΩ series input resistance connecting the hold capacitor to a high impedance op-amp with 3 pF of stray input capacitance would create a lowpass filter with a corner frequency at 1 MHz. This limited frequency response is adequate for phase lock loops that have bandwidths of less than 100 kHz. However, in microwave signal processing, where subharmonic sampling is used to extract information from a broadband modulated carrier or to downconvert a carrier to an IF frequency, the buffer amplifier will be required to have a frequency response as high as one-half the sampling rate. In this case, the buffer amplifier will need to have both high input impedance and very low input capacitance. A possible solution to this problem is to include the gate capacitance of a FET source follower into the total required value of hold capacitance.

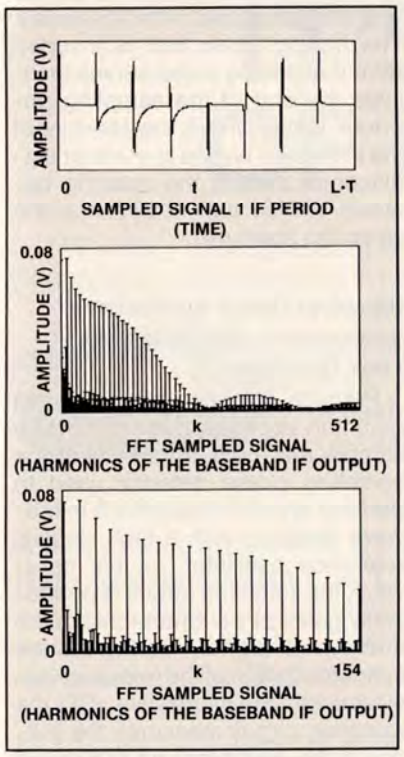

Fig. 5 Time domain analysis of periodic sampling and hold into a low impedance buffer.

Sampling Aperture Width Establishes Input RF Response

Maximum kinetic energy will be transferred to the hold capacitor when the sampling aperture is one-half the period of the frequency of the the sampled carrier. Sampling a

[Continued on page 244]

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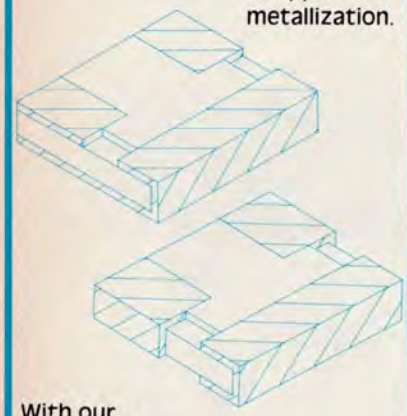

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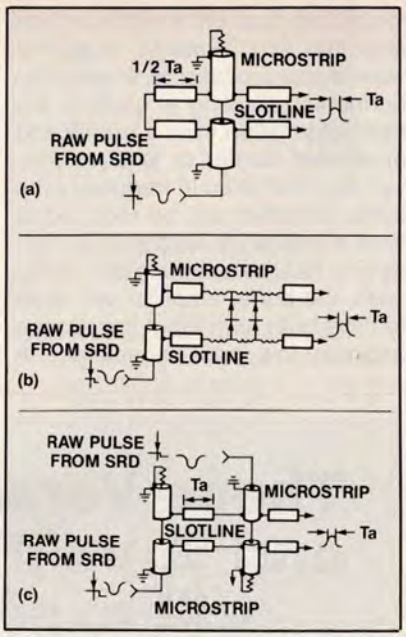

Fig. 6 Pulse compression techniques; (a) back short reflected pulse inversion, (b) nonlinear transmission line and (c) anti-parallel displaced pulses.

40 GHz carrier would require a sampling aperture of less than 15 ps. With this in mind, and to the extent of what is practical in the generation of the sampling aperture pulse, generating a pulse that is too narrow is challenging above C-band.

The best step recovery diodes (SRD) employed in pulse generation have a transition time of 35 ps, and a subsequent pulse width of 70 ps. Based on the above criteria, a sampling phase detector design that does not use a pulse compression technique will experience difficulty in operating at frequencies beyond 7 GHz.

A number of techniques can be employed to achieve the required pulse compression needed to operate at microwave and mm-wave frequencies. The ease at which the pulse compression hardware can be implemented is dependent on the type of 180° balun that is used to generate the balanced sampling aperture pulses to be applied to the sampling bridge diodes. The types of baluns that can find applications in sampling circuitry are generally those baluns employed in frequency mixers that offer multi-octave bandwidths with good 180° balance.

The most popular sampling phase detector balun is the floating dual resistive terminated balun found in the commercially available sampling phase detectors. This balun offers minimum bandwidth at microwave frequencies, suffers from DC drift and is not easily adapted to pulse compression techniques.

A more practical balun that offers multioctave bandwidth is the slotline-to-coplanar waveguide balun. Some very effective pulse compression techniques can be applied to these types of E-plane circuits. A collection of techniques is shown in Figure 6.

In the backshort circuit, the pulse travels in both directions at the microstrip-to-slotline transition. When the pulse strikes the shorted end of the slotline, it is inverted and reflected where it combines with the trailing edge of the forward traveling pulse. The trailing inverted pulse clips the forward pulse, which shortens the effective sampling aperture.

In Figure 6b, a nonlinear transmission line is used. The nonlinear transmission line uses varactor diodes to generate a voltage dependent time delay. The higher voltages of the pulse waveform propagate faster, which leads to a steepening of the leading edge of the pulse.[6]

The circuit shown in Figure 6c uses anti-parallel displaced pulses that are generated simultaneously. The trailing pulse that is inverted from the leading pulse serves to initiate the end of the sampling aperture. In this circuit, the aperture of the individual pulses is of minor significance as it is the spacing between pulses that establishes the sampling aperture.

Sampling Circuit Applications

Subharmonic Sampling Phase Lock Oscillators

Perhaps the simplest and most common application for microwave sample-and-hold circuitry is in the sampling phase detector used to perform synchronization of a microwave oscillator with a high stability reference oscillator. In this hardware, the sampling circuit is periodically gated at a subharmonic of the microwave signal. During phase synchronization of the reference oscillator with the microwave VCO, the sampling circuit measures the voltage of the zero crossing of a single half cycle of the microwave signal.

[Continued on page 246]

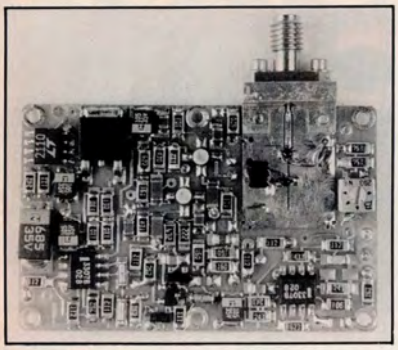

Fig. 7 A complete sampling PLL module without the VCO.

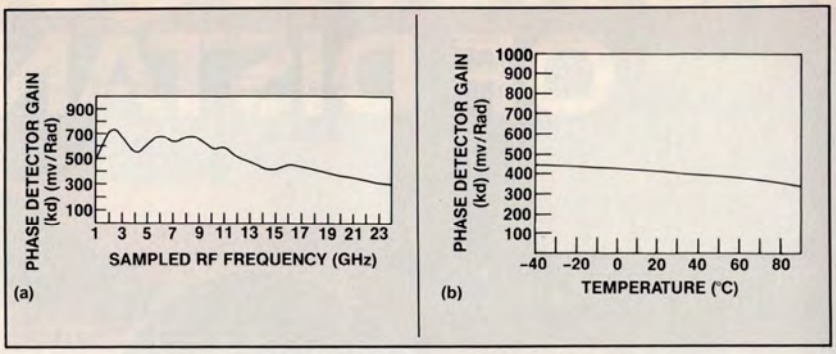

Fig. 8 Sampling phase detector performance; (a) typical gain and (b) temperature drift.

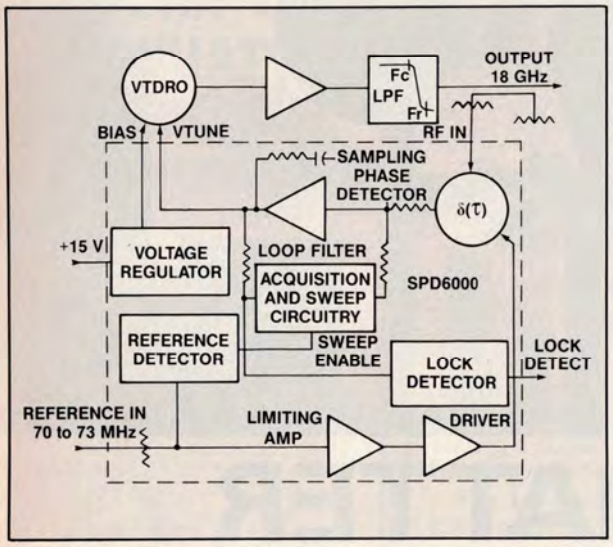

Fig. 9 A schematic diagram of a sampling PLL module.

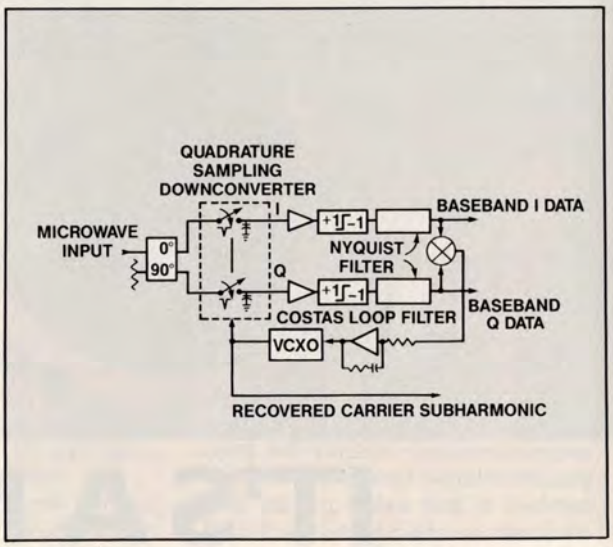

Fig. 10 A quadrature subharmonic sampling carrier recovery loop for direct demodulation of a MPSK microwave carrier.

Any advance or retardation of phase is indicated by a negative or positive DC shift at the IF output of the sample-and-hold circuit. When this signal is applied to the VCO tuning structure, the phase of the VCO can be forced to track the phase of the reference oscillator at a precise integer subharmonic.

Figure 7 is a complete sampling phase detector module measuring 1.2″ × 1.9″. This unit contains a sampling head that delivers a phase detector response of 400 mV/rad at 18 GHz from a 0 dBm input signal. The sampling head topology is a coplanar structure that features pulse compression of the type shown in Figure 4a. The coplanar-to-slotline balun offers multioctave bandwidth and is well suited for sampling head applications.[7,8] Actual performance of the sampling phase detector is shown in Figure 8. Contained in the module is the reference driver circuitry, loop filter, sweep and acquisition circuitry, reference detector and lock detector circuitry. The module is designed to be integrated with a VCO, such as a voltage tuned DRO, to form a complete PLO subsystem, as shown in Figure 9.

Direct Demodulation of Microwave MPSK Carriers

This commercial application employs two sampling heads and is an example that performs a great deal of microwave signal processing with a limited amount of microwave components. In Figure 10, the concept of quadrature subharmonic sampling for the purpose of coherent direct demodulation of an MPSK modulated microwave signal with suppressed carrier is introduced. Traditionally, this application would require a frequency converter with coherent microwave local oscillators and a Costas loop type of carrier recovery system. The quadrature subharmonic sampling module performs frequency conversion to baseband as well as I and Q vector demodulation, simultaneously. The carrier tracking oscillator is the sampling clock VCXO, which is operated at a subharmonic of the microwave carrier. The microwave carrier when split into quadrature and applied to the dual sampling downconverter module enables the I and Q signal to be generated, mixed and applied to the VCXO. The result of this is a quadrature subharmonically sampled carrier recovery loop (QSSCRL). The outputs of the QSSCRL can be digitized, which allows the remainder of the demodulation and decoding to be performed with conventional digital circuitry.

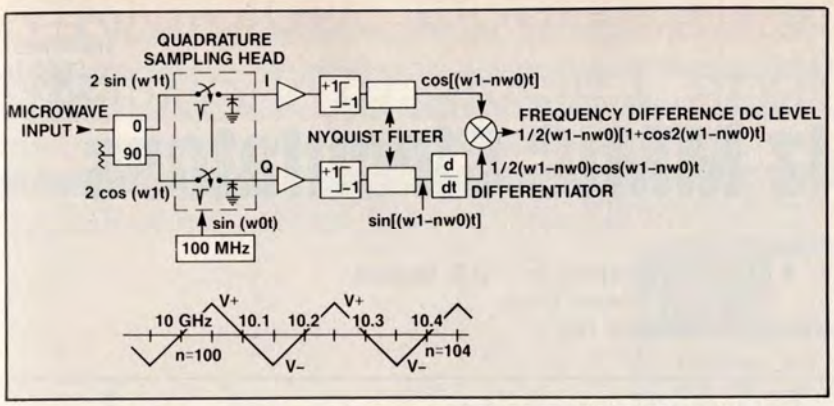

Fig. 11 (a) A subharmonically sampled quadricorrelator and (b) its DC output vs. input frequency.

Subharmonically Sampled Quadricorrelator

The concept of quadrature subharmonic sampling for vector demodulation is used in many signal processing applications. The circuit of Figure 11 shows how quadrature subharmonic sampling can be applied to an old technique for a modern application. The quadricorrelator is a type of wideband frequency discriminator first introduced in 1954.[9] The subharmonically sampled quadricorrelator allows this concept to be extended to microwave frequencies. Applications of the wideband frequency discriminator might include VCO linearization for microwave FM CW radar, FSK demodulation or precision frequency marker generation.

Conclusion

Key criteria for optimum sampling head performance have been discussed. When applied to microwave sampling hardware, the ability to perform vector demodulation of a microwave carrier is one example of the types of microwave signal processing that can be accomplished through subharmonic sampling. This blend of microwave circuitry and digital signal processing techniques represents the new age of microwave signal processing. ■

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Peter A. Weisskopf *received his BSEE from George Mason University in 1987. Prior to graduation, he was involved in mm-wave system development at Innovative Concepts Inc. for the Naval Research Laboratory, Washington DC. After graduation, he worked for M/A-COM AAD, where he designed phase locked DROs and microwave synthesizers. In 1990, he founded Merit Microwave in Phoenix, Arizona, where he is in engaged in the development of microwave and mm-wave signal processing components and systems.*

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